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Output filter design and control system implementation for a three phase AC grid emulator

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Abstract

The spread of hybrid and electric vehicles is leading to the development of increasingly efficient and compact On-Board Chargers (OBCs). These devices are essential for the power transfer from the grid to the battery and vice versa. Testing is a crucial aspect of the development of such components. Grid emulators are conceived to fulfil the need of testing grid connected converters like OBCs under several circumstances. Stability analysis or validation of proper functioning under grid disturbances are examples of tests. The goal of the thesis is to design the hardware and the software components of a grid emulator with the purpose of testing a 22 kW On-Board Charger which can also achieve bidirectional power flow.
In the thesis work, the analysis of a performing control system as well as a proper filter design is carried out. A normative documentation regarding harmonic compatibility is reviewed and considered as a guide for the design of the hardware. An existing two-level converter is selected to emulate the grid characteristics and deliver up to the full power required by the Device Under Test (DUT). The hardware design is mostly focused on the output filter of the converter. For this purpose, the equivalent impedance is examined to accurately emulate the grid. Different control methods are assessed to identify the most appropriate one for the application and a specific C-code is created. A research of the components is carried out to develop the filter stage. Those most suitable for the application are chosen.
A series of tests is conceived in order to validate the correct functioning of the grid emulator. The device is simulated in a Simulink environment before being realized on a physical testbench. To end with, an experimental setup is performed to test the system. In particular, specific Key Performance Indexes (KPIs) are defined to validate the filter performances and the control. These parameters mainly refer to the capability of the grid emulator to represent a grid poor of harmonic content due to the inverter modulation.

Introduction

Performance characterization on a proper testbench is the final step in component design. For grid-connected converters, this has to be carried out through grid simulators, which are fundamental for the assessment of the component under test. Furthermore, recent years have seen extensive research on power quality associated with the grid compatibility of grid-connected components. Those devices have to withstand typical grid disturbances like voltage sags, flicker, and unbalanced voltages. EMI questions have become of crucial importance for the PWM operation of grid-connected converters as well. Hence, in some cases, a harmonic measurement feature becomes unavoidable.
Since these phenomena are hardly predictable in power distribution system, a grid emulator may become essential to simulate the aforementioned perturbations.
However, such aspects are not the only ones typical of a grid emulator. A correct emulation of the grid to simulate specific grid conditions may be useful to test, for instance, the stability of the Converter Under Test (CUT). As stated later on, the control stability of a grid connected converter is deeply influenced by the Short Circuit Ratio (SCR) at the Point of Common Coupling (PCC) with the grid [1]. Moreover, the harmonic content produced by the emulator should be comparable to that of a normal grid, and the harmonics associated with PWM modulation must be minimal. The design of a suitable filter element is therefore crucial for a correct emulation condition.
The control of the grid emulator is another central point: many types of control are presented in the literature ([2], [3], [4], [5], [6]), part of which are based on resonant elements such as Proportional Resonant control or Repetitive Control. The stability of such a system is critical and requires careful evaluation. In certain situations, an open-loop control is implemented. Finally, a proper control has to hold the voltage at the reference value without causing undervoltages, overvoltages or high harmonic injections.

Chapter 1

State of art of grid emulators

Grid emulation is responsible for the test of the converter before it is connected to the main grid. It is common in the literature to simulate some typical grid disturbances in addition to only verifying the correct operation under nominal grid conditions. A summary of typical disturbances is provided.

1.1 Power Quality issues

The Power Quality (PQ) is a more general term to indicate a whole of problems related to the quality of the supply voltage. To be precise, it is any problem related to voltage, frequency and current variation which can cause wrong operation or damage to the electrical equipment. If modifications to the nominal values of the aforementioned electrical dimensions occur, there will be a decrease in power quality. The phenomena involved will be summarized hereafter, including the normative examined for the work.

- Voltage sag:
  It is a variation of the supply voltage between 90% and 10% of the Root Mean Square (RMS) nominal voltage for a period up to one minute.
- Voltage swell:
  It is the opposite of voltage sag, which is the brief rise in voltage between 10% and 90% of the nominal voltage over the course of a few seconds to a full cycle.
- Flicker:
  The fast fluctuation in screen and light bulb brightness that irritates the human eye is caused by the flicker phenomenon, which varies randomly and repeatedly by plus or minus 10% with regard to the nominal voltage.
- Voltage spike and overvoltage:
  Voltage spikes occur for a very short duration, while their RMS value is much higher than the voltage increase typical of an overvoltage. The latter, in fact, refers to an increase in the nominal voltage greater than 1.1 pu for a duration longer than one minute.

- Undervoltage
  On the other hand, with undervoltage, it is intended to cause a decrease in nominal voltage to a value lower than 0.9 pu for a time longer than a minute.

- Interruption and outage
  A power reduction to less than 0.1 pu within a minute is considered an interruption. It is different from an outage, which is the complete absence of voltage supply (that is, 0 pu).

- Harmonic disturbance
  Harmonics is a common power quality issue that results in a distorted supply waveform by superimposing multiples of the supply fundamental frequency. The phenomenon causes power losses, which result in inefficiency and overheating of components. It can cause failures too. Another important aspect of harmonics is the interference with nearby communication equipment. Harmonic distortion is typical of nonlinear loads. Given that the topic of this work focuses on a nonlinear power supply, it is worth mentioning the issues that result when a similar device is used. In a three-phase system, it is common to find odd harmonics (that is, the third, fifth, seventh, and so forth). In PWM inverters and rectifiers, multiple switching frequency disturbances are produced as well. The amount of frequencies and the amplitude of these are dependent on the modulation technique and number of levels, and a proper filter has to be sized to avoid injecting these harmonics into the connected equipment. [7], [8].

- Frequency fluctuation:
  It is a difference between the system's actual frequency and its nominal frequency. It is reliant on the equilibrium between load and demand, which must always be equal. [7].

- Voltage dip:
  it is a phenomenon related to three-phase systems characterized by the presence of unbalancing among the phases amplitudes [6].

For the purpose of the work, the standards related to harmonic content have been taken into account. In particular, the IEC 61851-21-1 (2017) [9], the IEC 61000-3-4 (1998) [10] and the IEEE 519 (2014) [11]. The cited standards will be further discussed later on.

1.2 Normative analysis

Any electrical equipment connected to the grid must comply with limits on harmonic emission into the main grid. Normative stipulate limits for low order harmonic content as well as high order harmonics. IEC 61851-21-1 (2017), IEC 61000-3-4 (1998), as well as IEEE 519, regulate harmonic emissions up to the 40th order harmonic with respect to the fundamental. From 9 kHz upwards, the radio frequency emissions range is defined, and consequently, Electromagnetic Interference (EMI). A distinction lies on the type of

emission, that is conducted (below 30 MHz), and radiated (above 30 MHz). CISPR regulation is the standard regulating the emissions in the range of radio frequency [12].
For the purpose of the thesis, some of the limits outlined by the normative related to conducted emission are taken into consideration, being most of the normative limits specified for the converter under test. Specifications for the test voltage source when harmonic measurement of CUT emissions is performed are given in [10].

The harmonic content depending on the grid is another important topic outlined by IEEE 519. The contribution of the examined work to the thesis is to provide voltage and current limits by voltage level and grid condition respectively. The Total Harmonic Distortion (THD) limits are presented and can be considered as THD limits for the CUT, whereas current limits are specified for several ratios between short circuit current and nominal load current [11]. Short circuit ratio is defined as $R_{sce} = S_{sc}/(3S_{equ})$ for single-phase systems and $R_{sce} = S_{sc}/S_{equ}$ for three-phase systems, where S_{sc} is the short circuit power at the point of common coupling (PCC), and S_{equ} is the apparent power of the equipment [10]. The previous ratio can be expressed as current ratio as well, valid both for single-phase and three-phase systems, as I_{sc}/I_l, being I_l the maximum demand load current of the component. The limit of the harmonic current in percent of I_l for each short circuit ratio is represented in the Table 1.1, referred to odd order harmonics.

I_{sc}/I_l	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h < 50$
<20	4.0	2.0	1.5	0.6	0.3
20<50	7.0	3.5	2.5	1.0	0.5
50<100	10.0	4.5	4.0	1.5	0.7
100<1000	12.0	5.5	5.0	2.0	1.0
>1000	15.0	7.0	6.0	2.5	1.4

Table 1.1: Limits of harmonic current in percent of the load current specified in the IEEE 519 documentation [11].

The term h represents the harmonic order. It is to be noted that even order harmonics are limited at 25% of odd harmonic limits.
Every short circuit ratio (SCR) represents a particular grid condition. A low SCR can represents a weak grid.

1.3 General aspect of grid emulation

As a general description, four concepts of emulation can be identified.

- Concept one refers to representing dynamic performances with under-scaled physical components;

- Concept two is the so-called power hardware in the loop, allowing real time simulation. The grid characteristic are simulated in real time by a power amplifier which receives the signals describing the behaviour of the converter under test;

- Concept three is based on power electronics converters to emulate grid characteristics and components (that is, generators, loads, line impedances);
- Concept four is focused on the terminal grid characteristics, and the behavior of the grid itself is replicated by emulating converters. In this concept, a terminal conversion stage structured with grid components (for instance, coupling inductances or transmission lines) may be added to recreate the desired context.

The grid emulation can also be extended when multiple converters and/or other devices have to be tested at the same PCC. Such a condition is called Multi-Input-Single-Output (MISO) or Multi-Input-Multi-Output (MIMO) grid emulation. The case to which the thesis is referring is instead a Single-Input-Single-Output (SISO) grid emulation.

The present work focuses on a grid representation through a power electronic converter plus an interconnection stage interposed between this and the device under test. For this reason, an overview of the system is provided below. The basic structure of a grid emulator consists of a source of power feeding the CUT, or the CUT feeding the grid emulator (depending on the CUT operation). A grid simulator then represents the grid, and provides the voltage to the CUT. The power is typically withdrawn from the grid and/or delivered to the grid by a topology in which the DC-link puts in communication a front-end converter connected to the main grid and the CUT side inverter. The mentioned components are called respectively energy feedback system and grid emulation system [3], [13], [4]. The basic schematic of a standard grid emulation system is represented in Figure 1.1.

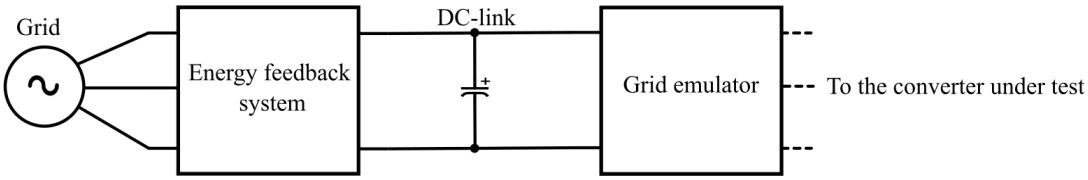

Figure 1.1: Basic schematic of a standard grid emulator.

Since the component to be tested has to be connected to the standard low-voltage grid, a simple two-level inverter is considered, as a great part of grid emulators refer to it. Similar considerations can be made with regard to the connection stage of the test-bench, given that an LC filter can be connected between the converter under test and the inverter, as shown in Figure 1.2. The filter has to provide good filtering performances of the voltage and current ripple due to the inverter modulation. As assessed in [3], the grid impedance seen from the CUT can be adjusted if an output inductor (that is, at the input of the CUT) is implemented.
When dealing with LC stage filters, resonances occur at specific frequencies. A damping of such disturbances may be applied (for instance, for control stability). The classic passive damping method is usually adopted instead of active damping to ease the control of the

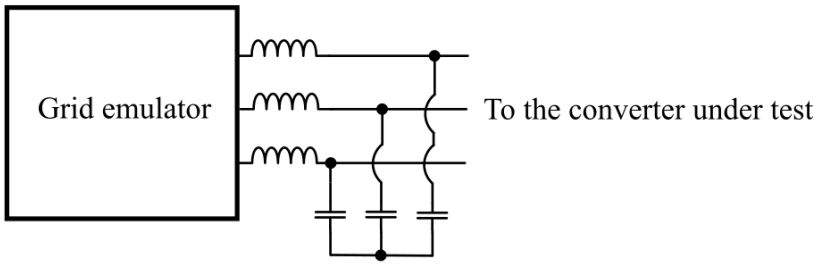

Figure 1.2: Circuital representation of an LC filter connected to a grid emulator.

converter, even though additional losses have to be dissipated. Besides, such a method is the most implemented one among the grid-connected converters [13]. For the software implementation of a grid emulator, several types of control can be taken into account, including Proportional Resonant (PR) Control or Repetitive Control (RC) to boost the capability of generating harmonics. The bandwidth of the converters can be limited, as most of the time the two-level converter is typically adopted. In the above case, the bandwidth can range from hundreds of Herz to several kilo Herz. In order to increase the available bandwidth, the equivalent switching frequency at the terminals of the converter can be increased. Two approaches are mainly adopted among the grid emulators: the first one consists of using two different converters; the second one is based on using topologies with higher equivalent switching frequencies. In addition, to achieve a higher switching frequency, MOSFETs or SiC devices can be used for their potential to reach frequencies above 50 kHz. The stability of the control is another important issue, seeing that interaction between the CUT and the simulator could occur. Apart from that, the stability may be caused mainly by two factors: the delays and the dynamics of emulating converters. The causes of delays can be output transmission delay, input transmission delay, sensor delay, computation delay, and modulation delay, caused respectively by digital controllers and by PWM modulation. Finally, the presence of delays, voltage/current controllers and passive filters affects the dynamics of the system and this can lead to stability issues [14].

1.4 Grid emulators main topologies and controls

Grid emulation for low-voltage grid-connected converters can take several forms, but most of the testbenches in the literature have some features in common, which are:

- The use of a PWM modulated electronic converter;
- The connection stage composed by filter elements (usually an LC filter).

Generally the filter capacitor voltage is closed-loop controlled emulating the grid voltage [2].

A simple design of a three-phase grid emulator is presented in [3], as an example of grid emulation system. The grid emulator is needed to verify the behaviour of grid-connected converters, and it can be used both as a source and as a load. Moreover, the paper focuses on experimental tests of voltage dips, even though the system is designed to simulate other disturbances too. The topology of the grid emulator is of the type already mentioned, that is, a two level three-phase inverter with an output LC filter. The DC link is connected to a three-phase rectifier interfaced with the grid, representing the energy feedback system. The system is represented in Figure 1.3. On the basis of the CUT operation, the power supplied to or withdrawn from the CUT can be exchanged with the other two elements.

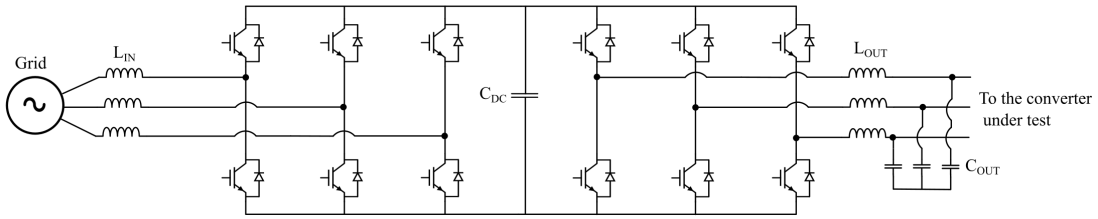

Figure 1.3: Topology of the considered grid emulator [3].

The system is closed-loop controlled via a cascaded controller consisting of an outer voltage control loop superimposed on an inner current control loop. The authors have extended it with a more performing control due to the poor performance of the only cascaded control. The simple block diagram of the cascaded control is represented in Figure 1.4.

Figure 1.4: Cascaded control block diagram [3].

The filter element consists of an LC stage for those components under test that have an output inductor. Its design is based on the desired voltage attenuation at the output of the converter, which is fixed at 10% of the DC link voltage value.

A similar design is proposed in [4]. The article is about a three-phase, back-to-back connected inverter having a common DC bus with a front-end converter interfaced with the grid. The topology is very similar to that of the converter previously analyzed, except for the output (that is, grid emulator side) LC filter, which is characterized by a passive damping method using small resistances in series with the filter capacitors. The cited damping method will be later analyzed in detail. The control of the front-end converter is

based on an outer voltage loop regulated by a Proportional Integral (PI) controller and an inner current loop regulated by Proportional Resonant (PR) controllers. The DC-Link is regulated with a PI controller. It is emphasized that fluctuations in DC link voltage happen when there are imbalanced disturbances. Hence, a four-wire configuration is needed. The topology of the grid simulator is represented in Figure 1.5

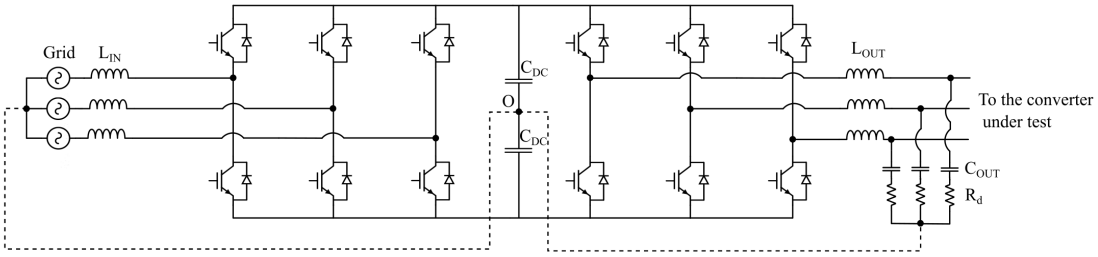

Figure 1.5: Topology of the grid emulator [4]. In this case, the LC filter resonance is damped with series resistors (R_d) to the filter capacitors.

Unlike conventional grid emulators, the device is open-loop controlled at the output side, making control easier, whereas a sophisticated control of the grid simulator status is envisioned. The reference disturbance is generated by a command generation algorithm operating through a Finite State Machine model, allowing a disturbance to be produced in correspondence with any angle referring to a specific phase [4].

A grid emulator can be even more simplified as suggested in [2], where a voltage source inverter (VSI) is used to test a PWM rectifier. The hardware is basically composed of the PWM inverter, which is not connected to any filter. The point of common coupling is the output of the inverter itself. The advantages of removing the filter element rely on:

- Higher bandwidth with respect to filter-composed grid emulators;
- Simplicity of construction;
- Cost effectiveness;

The removal of the filter is feasible only when the input of the converter is composed by inductive elements, otherwise a capacitive or a different input would not be practically realizable. The device is open-loop controlled, and the reference voltage is the same between the grid emulator inverter and the equipment under test. The open-loop control can increase robustness and velocity of the control, as well as the ease of control. The final topology of the grid emulator is shown in Figure 1.5.

The drawback linked with the proposed design is the discrepancy between the harmonic content of the grid emulator and that of the actual grid. This is reflected in the higher switching ripple at the input of the CUT.

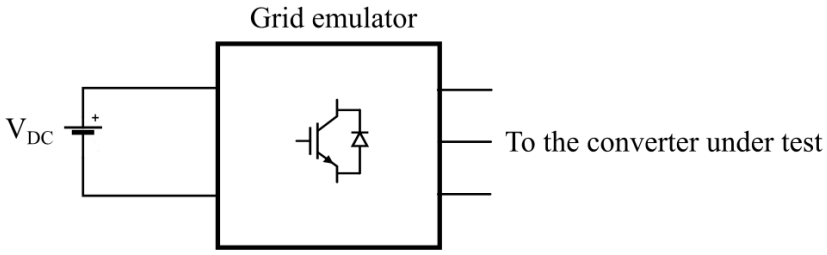

Figure 1.6: Representation of the grid emulator proposed in [2]. The filter is not present.

1.5 Advanced control of grid emulator

Among the simulators analyzed, some high performance controls can be implemented for specific grid disturbances and conditions, leading to high performance controls that can become very complex. Indeed, disturbance generation can include harmonic generation, and the voltage controller has to be able to achieve low order harmonic generation. The following section deals with two types of control normally used for this purpose, which are proportional resonant (PR) control and repetitive control (RC) [14], after a brief description of standard controls.

Standard controls

The conventional grid emulator is characterized by an inner current loop and an outer voltage loop which are similar to the typical grid-connected converter control, and it provides voltage control on the filter capacitor as shown in Figure 1.7. The controller is usually a PI controller in the form of the transfer function indicated by equation 1.1.

$$G_{PI} = K_P + \frac{K_I}{s} \tag{1.1}$$

where the integral gain is denoted by K_I and the proportional gain is denoted by K_P. The PI controller may require a Clarke and a Park transformation in a three-phase system, leading to a direct-quadrature (dq) frame of reference since the Proportional Integral control suffers from steady-state delay when the reference is sinusoidal (in general, when the reference is not a continuous signal) [2]. The direct-quadrature frame is called the Synchronous Reference Frame (SyncRF). For this reason, in single-phase systems, different controls such as Proportional Resonant control can be implemented to achieve zero phase error and steady-state error at the fundamental frequency. This approach is used among single-phase grid-connected inverters (for instance, in [15]). The conventional control just described is presented in Figure 1.7.

The open-loop control is the simplest control available for a grid emulator. The microcontroller is directly fed with only the reference signal. Thus, there is no calibration

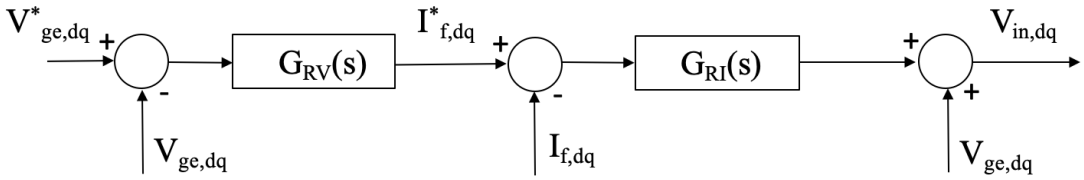

Figure 1.7: Conventional control of a grid emulator, as stated in [2].

of any controller. Some of the advantages of using an open-loop control are the increased velocity of the control and the simple and straightforward implementation. However, the complete removal of the steady-state error is not guaranteed and a current control is absent.

Proportional resonant control

The proportional resonant control differs from a normal Proportional Integral control for what regards the integral part, which is not present in the case study. The ideal form of Proportional Resonant control is described Equation 1.2:

$$G_h = \frac{K_h}{s^2 + \omega^2} \tag{1.2}$$

where the term h stands for h-th harmonic. The use of proportional resonant controller provides a massive gain in correspondence of the h-th harmonic, letting to achieve a zero steady-state error at the relative frequency. The complete form of a Proportional Resonant controller thus assumes the form of the Equation 1.3.

$$G_{PR} = K_{PR} + \frac{K_R}{s^2 + \omega_g^2} \tag{1.3}$$

where ω_g is the grid pulsation, generally speaking the selected harmonic for which zero steady-state error is imposed. When also further harmonic components are added (thus, the control is supplemented by an harmonic compensator), the complete equation becomes:

$$G_{PR} = K_{PR} + \frac{K_R}{s^2 + \omega_g^2} + \sum_{h=3,5...}^{n} \frac{K_h}{s^2 + \omega^2} \tag{1.4}$$

The Proportional Resonant control can be used in $\alpha\beta$ since resonant components are implemented. The PR control in the synchronous reference frame has a similar behaviour of a proportional integral control (in the SyncRF too) with a higher harmonic attenuation in correspondence of the desired harmonics.
The system stability is a crucial aspect of every control strategy, especially when dealing

with resonances. To improve the stability of the proportional resonant regulated system, the practical form of the PR controller (Equation 1.5) can be adopted (non ideal Proportional Resonant controller):

$$G_{PR} = K_{PR} + \frac{2K_R\omega_c s}{s^2 + 2\omega_c s + \omega_g^2} + \sum_{h=3,5...}^{n} \frac{2K_h\omega_c s}{s^2 + 2\omega_c s + \omega_h^2} \tag{1.5}$$

where ω_c is the cut-off frequency, which has to be much less than the grid frequency ω_g. The cut-off frequency ω_c is increased to improve the phase margin of the bode transfer function of the system. A Bode plot showing the comparison between ideal and non-ideal Proportional Resonant controller is displayed in Figure 1.8.

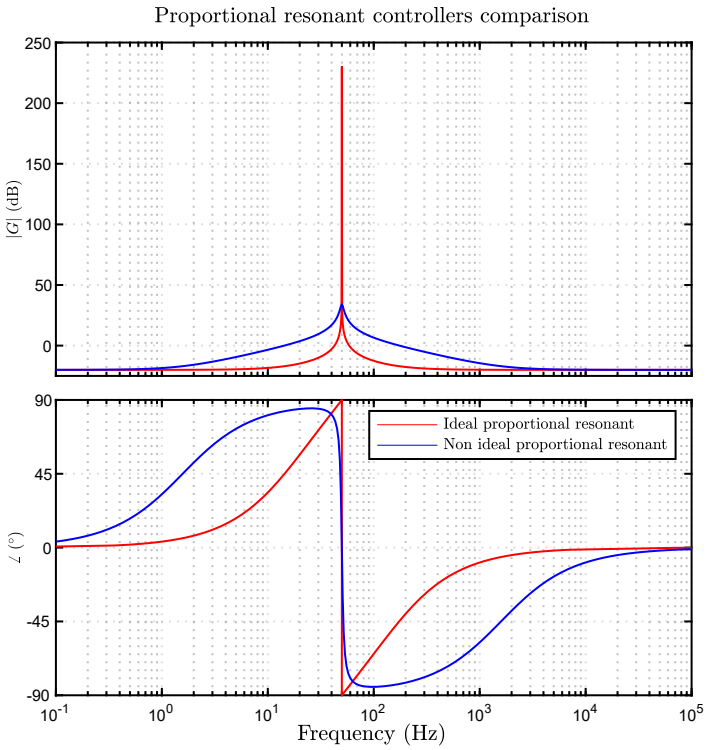

Figure 1.8: Bode plot showing the comparison between the ideal proportional resonant controller and the non ideal proportional controller having $\omega_c = 10 rad/s$.

The design of the PR controller can be actuated in two phases:

- Selecting the K_{PR} to obtain a stable control and at the same time a proper response;
- Adjusting the K_{IR} to achieve a steady state error on the desired harmonics without compromising the phase margin [16].

A Proportional Resonant control-based grid emulator is proposed [5] to test the performance of the equipment under test, composed of both passive and active loads. The topology of the simulator is similar to the one analyzed before [3], [4], with the exception of using an LCL input filter instead of a simple L filter as shown in Figure 1.9. Proportional Resonant control of current and voltage is implemented in the grid-side inverter as well as in the test-side inverter. The DC link control loop and power flow control loop are Proportional Integral regulated. The inner control structure of voltage and current is similar to the one represented in Figure 1.4, with Proportional Resonant controllers as regulators. The control of the emulation-side inverter is composed by the voltage and current loops just mentioned, while the grid-side inverter control is represented in Figure 1.9.

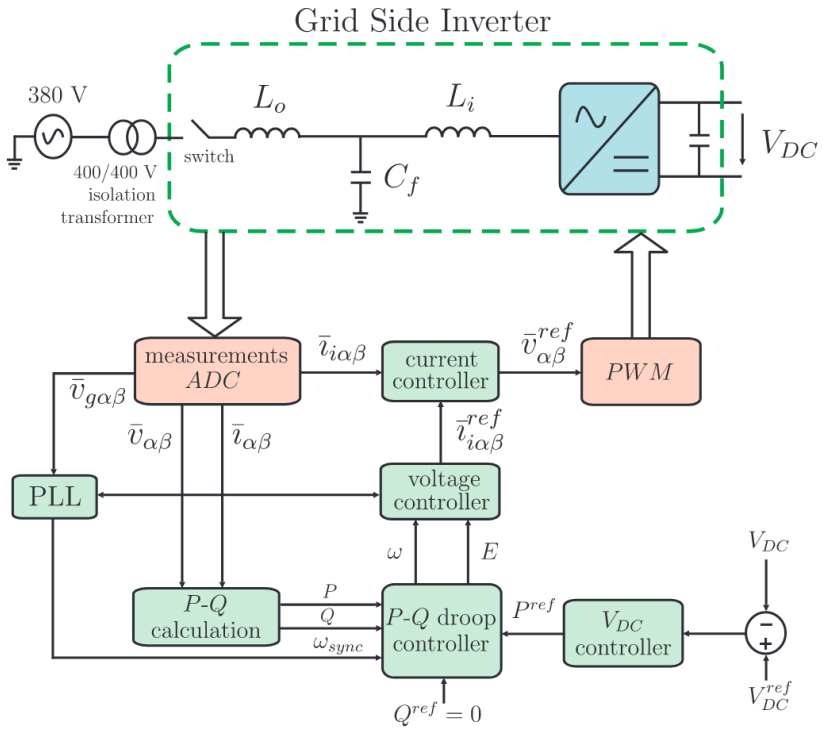

Figure 1.9: Control structure of the grid side inverter proposed in [5]. The emulation side inverter control is the same except from the DC link control and power flow control.

The purpose of the control is to generate the following disturbances: voltage sag, flicker, harmonic injection, unbalanced voltages. The PR control is in ideal form and is calibrated on the grid frequency (50 Hz), while for harmonics pure resonant terms are considered, according to the equation (1.4). The harmonics are tuned on the 5th, 7th, and 11th harmonic for the voltage controller and on the 5th and 7th harmonic for the current controller.
Results are proved experimentally. In particular, harmonic generation tests show how a Proportional Resonant control can be efficient both in generating harmonic disturbances

(for what regards the test side inverter) and in compensating them when a similar control is implemented in the device under test [5].

Repetitive control

The Repetitive Control is similar to the Resonant Control given that it provides a very high gain at specific frequencies. The control tracks repetitive references, letting it achieve a zero steady-state error at higher harmonic frequencies.
The basic structure of a Repetitive controller is characterized by a periodic signal generator having the transfer function represented in Equation 1.6.

$$G_{sg} = \frac{e^{-s\tau}}{1 - e^{-s\tau}} \tag{1.6}$$

where $e^{-s\tau}$ is a delay having a time constant τ and indicates the period of the reference harmonic. It is put before a conventional controller inside a standard control loop. Additional filters are added to improve the robustness of the system. The disadvantage of a grid emulator based on Repetitive Control is a scarce transient response and flexibility. For this reason, higher complexity RC control methods are implemented, however, there will not be a deeper study in the thesis [6].

1.6 Output filter stage

The filter stage represents a crucial element for PWM converters. The current state of the art of grid emulators makes use of passive LC converters [3], [4], [2]. Only differential mode filters are taken into account for the sizing of the filter stage. The transfer function of an LC filter describing the output voltage response (at the terminal of the filter capacitor) versus the input voltage is characterized by two poles at the pulsation $\frac{1}{\sqrt{LC}}$, as well as a resonance peak due to the mutual cancellation of the two passive element's impedances. Beyond the resonance frequency, the magnitude of the plot falls at -40 dB/dec. The transfer function of the filter is described by the equation 1.7:

$$G_{LC} = \frac{1}{s^2 LC + 1} \tag{1.7}$$

The advantages with respect the usage of a simple L filter is the better attenuation at higher frequencies, since the L filter has a magnitude falling of -20 dB/dec.

Combining an LC stage with an output inductance, an LCL filter can be conceived, and its single-phase equivalent circuit is represented in Figure 1.9. Even though this type of filter is not a popular concept among grid emulators, by having a further inductive output stage, it is possible to adjust the simulated grid impedance and increase the filtering effect. Indeed, above the resonance frequency, the magnitude decreases by -60 dB/dec. The filter behaves in the same way as an LC filter at no-load conditions, since in the output

the current is null. A transfer function of an LCL filter is identified by its output current versus input voltage ratio. The Equation (1.8) represents the cited transfer function.

$$Y(s) = \frac{i_{out}(s)}{v_{in}(s)} = \frac{1}{s(L_{in} + L_{out})} \cdot \frac{\omega_0^2}{s^2 + \omega_0^2} \tag{1.8}$$

where ω_0 is the resonance pulsation defined in Equation 1.9.

$$\omega_0 = \sqrt{\frac{L_{in} + L_{out}}{C \cdot L_{in} \cdot L_{out}}} \tag{1.9}$$

and the Bode diagram of the transfer function $Y(s)$ is shown in Figure 1.10.

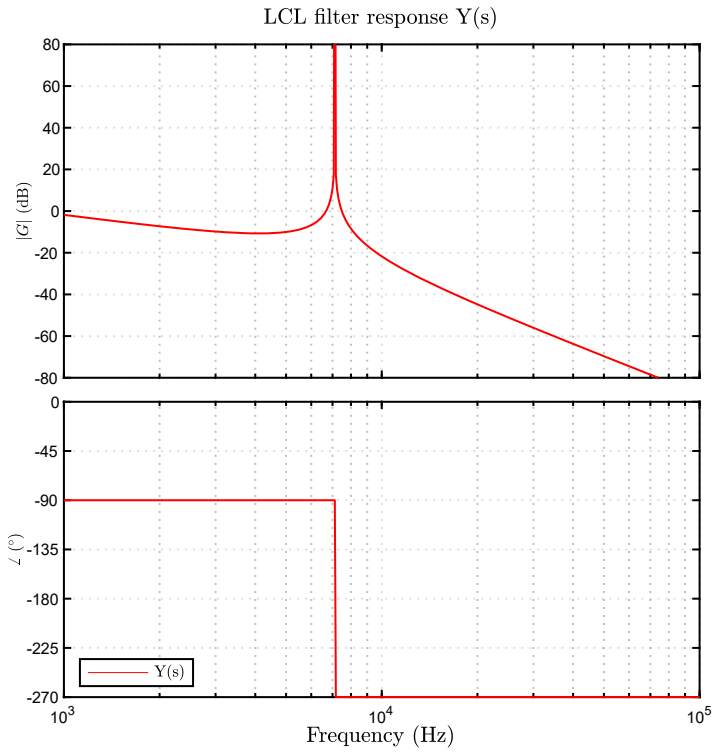

Figure 1.10: Transfer function $Y(s)$ of a generic undamped LCL filter.

The comparison among the three solution (i.e., L filter, LC filter, LCL filter) is represented in Figure 1.11: the response through a Bode plot of the transfer function $Z(s) = V_o/V_{in}$ is simulated, where V_o is the voltage at the terminals of a load resistance of value 10 Ω. The filter values are:

- $L_1 = L_2 = 100\mu H$
- $C = 10\mu F$

where L_1 has the same value for every filter, and L_2 is the output inductance of the LCL filter. It is to be noted that the load resistance of 10 Ω provides a significant damping effect of the resonance occurring in LC and LCL filter architecture, as well as a little decrease of the filtering effect.

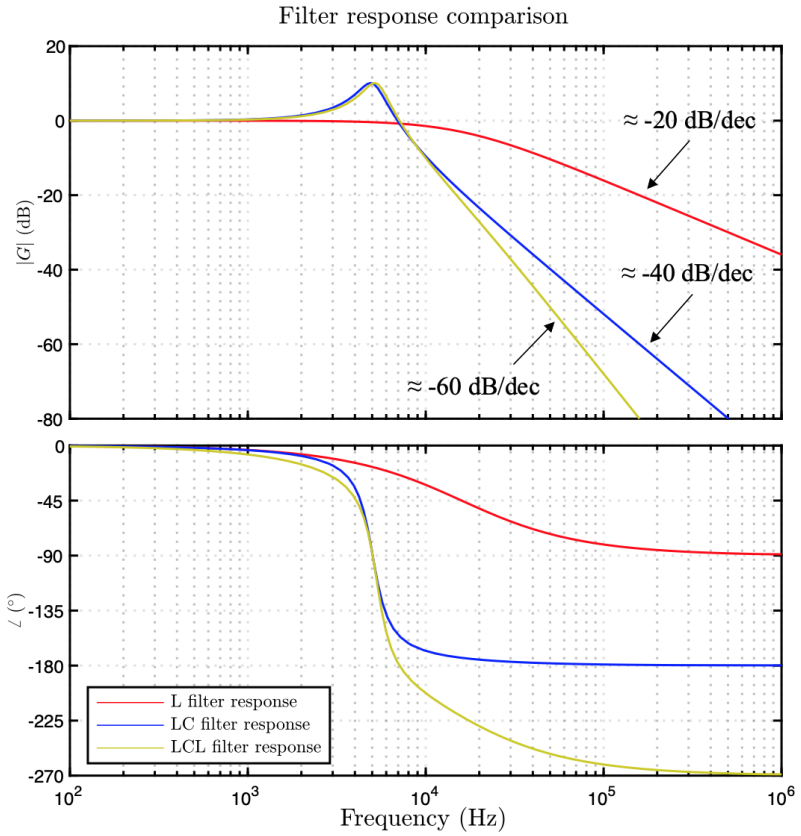

Figure 1.11: Transfer function $Z(s)$ when different filters are taken into account.

The LCL filter can be optimized by introducing the k_L parameter, defined as in Equation 1.10.

$$k_L = \frac{L_{out} + L_g}{L_{in}} \tag{1.10}$$

where L_g is the grid inductance. It is therefore necessary to have information about the grid conditions. The topic will be discussed in the next chapters. It is demonstrated how $k_L = 1$ is the condition for which the product between the capacitance and the overall inductance is minimized, thus leading to a smaller filter.

Both LC and LCL filters may be affected by resonance issues, which might lead to control instability and amplification of certain disturbances. In some cases, the series resistance of the filter elements can provide appropriate damping. In other cases, it is not sufficient. To deal with the resonances both active damping or passive damping can be implemented, reducing the resonance effect at the resonance frequency. The active damping provides improved control performance and stability, but increase the complexity of the control since feedback systems are added. The passive damping are achievable by inserting series or parallel resistors with respect to the elements of the filter. This leads to additional power losses and diminished filtering effect, though easier and simpler implementation are achieved. The next paragraph focuses on the analysis of the main passive damping solutions [1].

Main passive damping methods.

Many passive damping solutions are available among the literature. The simplest one is executed by putting a resistor in series with the filter capacitor (Figure 1.12). An LCL filter is taken as an example. The transfer function Y(s) of the filter is then changed due

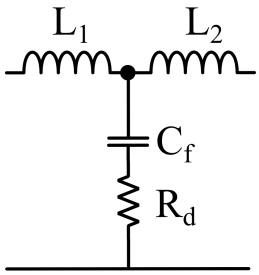

Figure 1.12: Topology of the series damping in a LCL filter [13].

to an additional damping element, in the form of Equation (1.11):

$$\zeta_0 = \frac{\omega_0 R_d C}{2} \tag{1.11}$$

Where R_d stands for damping resistance, therefore the transfer function (1.8) is turned into the Equation (1.12):

$$Y(s) = \frac{i_{out}(s)}{v_{in}(s)} = \frac{1}{s(L_{in} + L_{out})} \frac{2\zeta_0\omega_0 s + \omega_0^2}{s^2 + 2\zeta_0\omega_0 s + \omega_0^2} \tag{1.12}$$

The damping effect is well represented in figure 1.13.

The damping effect occurs for the whole frequency domain of the Bode diagram, given that the impedance of the capacitor is always affected by the damping resistor [13], [1].

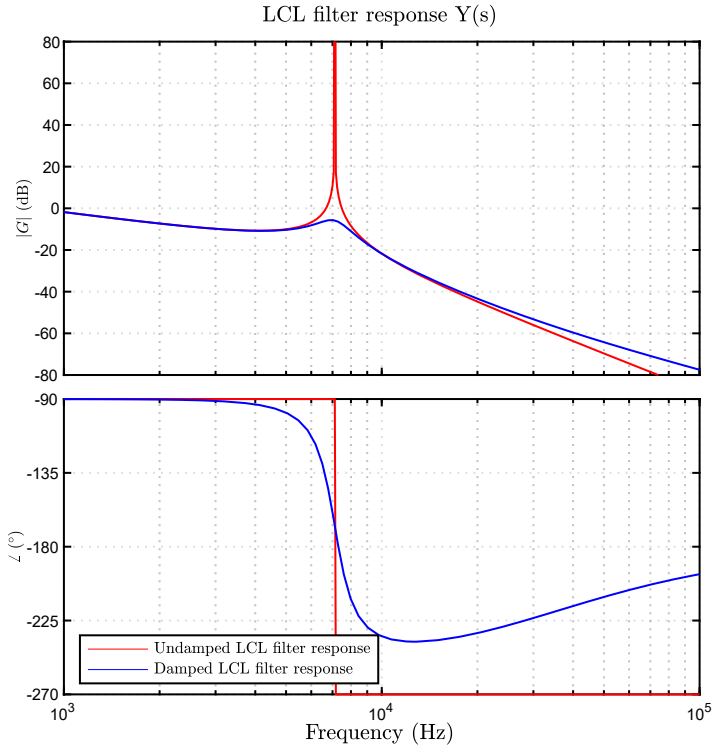

Figure 1.13: LCL filter response comparisons. It is to be noted that the filtering effect is reduced when the damping is implemented.

Another damping method consists of putting other reactive elements in parallel to the resistor, such as an inductor, as in Figure 1.14. The idea is to provide damping only when necessary, i.e., near the resonance frequency. By connecting a parallel inductor to the resistor, when the frequency is around the fundamental value, the impedance of the inductive branch is much lower than the resistive branch ($L_d\omega_g << R_d$), leading to a tiny current flow into the resistor. The consequences are minor losses in the correspondence of the base frequency and in the surroundings [13].

Damping can also be actuated by inserting resistors in parallel with the filter capacitance, including other reactive elements. The figure 1.15 shows a passive damping concept that includes a series RC branch as a way of damping. The aim of the considered topology is similar to the previous one, thus providing a damping effect in the range of the resonance frequency. If a proper sizing of the two elements is performed accordingly, the damping capacitor impedance of the RC branch is significantly higher than the resistor one, avoiding a large current at relatively low frequencies [13], [17].

Damping elements can be applied in parallel with the series inductor as well. In this case, a series RL branch is put in parallel with the main filter inductor. The purpose of

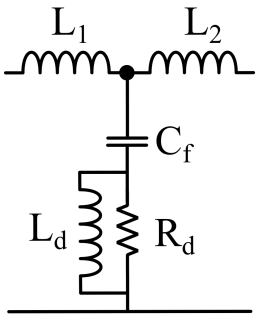

Figure 1.14: Topology of the series damping in a LCL filter with an inductor in parallel to the resistance [13].

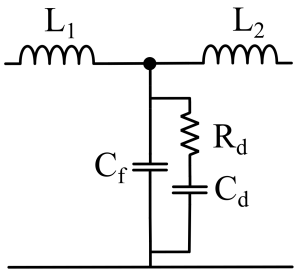

Figure 1.15: Topology of the parallel damping in a LCL filter [13].

putting a parallel branch inductor (i.e., the inductor L_d) is similar to that relative to the aforesaid examples. The disadvantage of the cited damping method is the decayed high frequency filtering effect. The topology of the above method is represented in Figure 1.16 [17].

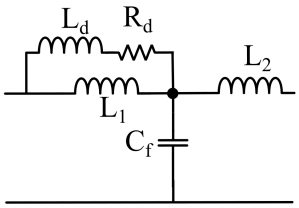

Figure 1.16: Topology of the damping parallel to the filter inductor in a LCL filter [13].

Other more complicated ways of damping can be implemented, which include multiple reactive elements in series or parallel to the damping resistors and are not considered in the present work [13].

Chapter 2

System under study

2.1 Requirements

The On-Board Charger is designed to work both in three-phase and single-phase operation. The main data of the OBC are described in Table 2.1. As a result, the testbench is created

Nominal three-phase power	22	kW
Nominal single-phase power	7.4	kW
Nominal phase voltage	230	V_{rms}
Maximum phase voltage	250	V_{rms}
Vehicle to grid operation	Enabled	
Nominal frequency	50/60	Hz
Power factor	>0.99	
Efficiency	>94	%

Table 2.1: Onboard charger data.

to replicate any working situation by modifying the hardware setup. In contrast to the prior options analyzed in literature, the grid emulator inverter's DC-link will be directly linked to a power source, the PSB 9750-60. For sake of a more efficient system, the output of the OBC (that is, the battery connection) is put in common between the DC-link of the grid emulator mentioned before and the power supply. A power circulation then occurs, with the power supply overcoming the losses. An additional DC/DC converter is needed to increase the output voltage of the OBC to the DC-link voltage. Moreover, the described working principle allows to test the full power functioning of the converter under test. SiC MOSFET devices are employed in the PFC as in the grid emulator inverter and in the DC/DC converter. The final topology is represented in Figure 2.1.

The grid emulator inverter specifications are instead presented in Table 2.2, to comply with both the OBC and the power supply features. A safety margin of 20% has been selected from the nominal current and voltage of the CUT.

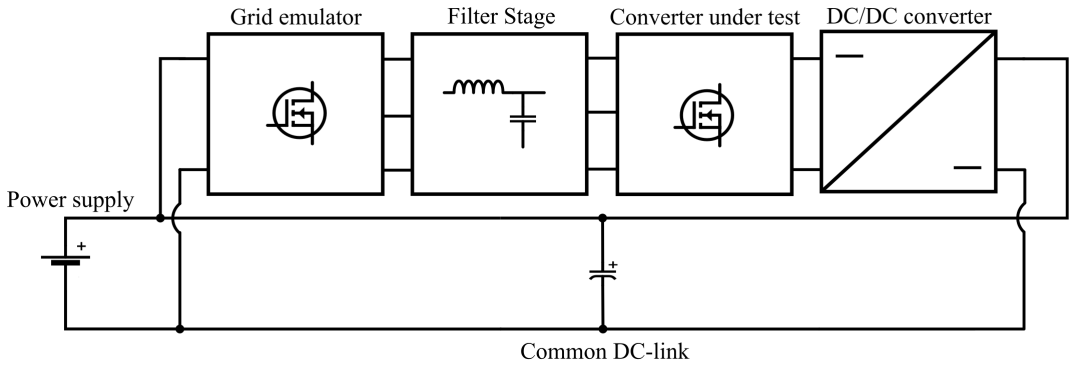

Figure 2.1: Overall system topology.

The DC-link voltage is kept at 750 V, which is the maximum voltage allowable from

Nominal three-phase power ($P_{n,\,3-phase}$)	22	kW
Nominal single-phase power ($P_{n,\,1-phase}$)	7.4	kW
Nominal phase voltage (V_n)	230	V_{rms}
Maximum phase voltage (V_{max})	276	V_{rms}
Nominal frequency (f_n)	50/60	Hz
Nominal phase current (I_n)	32	A_{rms}
Maximum phase current (I_{max})	38	A_{rms}
Maximum DC-link voltage ($V_{DC,\,max}$)	750 V	V
Liquid temperature (T_l)	20 to 50	$\circ\ C$

Table 2.2: Grid emulator inverter specifications.

the DC power supply. This choice has been made considering an eventual overvoltage working condition and the possibility of connecting the DC-link in common between the testbench converters. Indeed, the DC-link voltage should be kept as low as possible for lower component stress and dimensions. The threshold of the overvoltage protection of the power supply is set accordingly. The voltage limits and allowed ripple will be discussed in the following chapters.
In addition to the aforementioned specifications, some additional features related to the desired performance of the grid emulator have been defined. The performances are derived from the required OBC specification. As a result, the grid emulator must be able to supply the load in accordance with the OBC specifications. The grid emulator specifications can therefore be extended with some performance requirements that are listed in Table 2.3 and refer to the capability of the grid emulator to satisfy the load request. The table contains the Key Performance Indicators (KPIs) relative to every requirement. Some of those have been verified both during simulation and during test.

Requested performance	**Performance description**	**Relative KPI**
(1.a) Nominal working operation	The grid emulator has to act both as a sink and as a source for the OBC. The operation must be verified at the nominal voltage	Maximum of 10% deviation from nominal voltage and current ($\Delta V_{max} = 10\%$, $\Delta I_{max} = 10\%$).
(1.b) Undervoltage and overvoltage operations	The grid emulator has to provide/absorb power in a range between 200 V_{rms} and 240 V_{rms} (nominal power operation is not requested)	Maximum of 10% deviation from the expected reference over/undervoltage ($\Delta V_{max} = 10\%$).
(1.c) Nominal frequency operation	The grid emulator has to work at nominal power at the nominal frequencies of the OBC (50/60 Hz) and capable of providing/absorbing power in the range from 45 Hz to 65 Hz	Maximum of 5% deviation from the expected reference frequency ($\Delta f_{max} = 5\%$).
(1.d) Response to a reference power step	The grid emulator has to react properly to a reference power step of the CUT without causing permanent over/undervoltages and transitional over/undervoltages over the maximum expected value	Maximum transitional voltage deviation of 20% with respect to the reference voltage ($\Delta V_{max,\,transitional} = 20\%$).
(1.e) Module temperature	The module temperature has to remain beneath the maximum limit specified by the datasheet	Safety margin of 20 $^{\circ}$ C from the maximum module temperature ($\Delta T_{max} = 10\%$).

Table 2.3: Performance specification of the grid emulator.

An additional requirement derives from the study of current state-of-art grid emulators (called AC power sources), which are characterized by an output voltage noise specification depending on the source and a THD feature. The first prototype under development is characterized by less performing features since its only purpose is testing the correct operation and stability of the CUT. Thus, larger constraints have been prescribed for the grid emulator prototype with respect to the AC sources features. The THD can take into account the harmonics up to the 50^{th} as specified by the normative. Higher order harmonics may be included [11]. Thus, a voltage THD limit has been defined to assess the control performances, as the control affects the low harmonic distortion more than the high order ones. A voltage ripple limit has been set to evaluate the filter performances. In particular, the harmonics higher than the 50^{th} have been considered.

-

Harmonic specification	**Harmonic KPI**
(2.a) Limits coherent with the current state-of-art AC power sources during nominal voltage operation	Voltage ripple noise $V_{o\,rms} < 1\,V_{rms}$ & $THD < 5\%$.

Table 2.4: Harmonic specification of the grid emulator.

To validate the design results, it is necessary to stipulate a list of tests which derives directly from the just identified requirements. The basic functioning tests are listed in the upper part of Table 2.5 and refer to the verification of the fundamental operation of the grid emulator in providing power only, while the advanced tests are listed in the lower part of the table and are crucial to test the compliance of the performances with each requirement. It must be specified that the following tests will be executed when the hardware part is complete. At the time of the thesis work, it was not possible to perform every stated test. Thus, only a few of them have been executed.

Basic preliminary tests	
Nominal working operation	Voltage and current visualization and measurement in compliance with requirement (1.a)
Inverter temperature	Measure and verification according to requirement (1.e)

Advanced tests	
THD measurement	Measure of the harmonics in compliance with requirement (2.a)
Voltage ripple verification	Measure of the harmonics in compliance with requirement (2.a)
Power step of the CUT	Visualization and verification of the grid emulator response according to requirement (1.d)
Operation during conditions different other than nominal	Visualization and verification of the grid emulator response according to requirements (1.b) and (1.c).

Table 2.5: List of tests to be carried out on the grid emulator.

2.2 Grid characterization

The On-Board Charger is connected to the low-voltage public grid whose standards for Europe are 230 V_{rms} per phase at 50 Hz. Despite the grid features are highly variable from any PCC to another, the three-phase grid (and the single-phase grid too) is representable by an ideal voltage generator in series with an inductance having value the sum of cable inductance and transformer inductance. This is due to the mainly inductive behaviour of the grid. The equivalent circuit of the grid is represented in Figure 2.2 and it is the same approach adopted in [1].

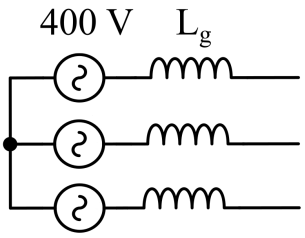

Figure 2.2: Equivalent circuit of the low-voltage grid [1].

In order the On-Board Charger to be tested so that it will operate properly under the majority of connection points (that is, also when the quality of the supply is scarce) bad grid conditions have been considered. Thus, an appropriate weak grid is needed, as the system stability tends to decrease when the grid equivalent inductance increase. This is because the resonance frequency caused by interaction with filter capacitors of the CUT reaches lower values, rising the resonance peak and leading to a loss of phase margin. Additionally, a greater grid inductance lowers the control bandwidth and decreases the low frequency phase margin causing a more nervous response [1].
The goal of the grid analysis here carried out is to identify a proper grid condition to be simulated complying with the previously mentioned requirement of weak grid. A weak grid is such when the short circuit ratio is sensibly low, as indicated in the Table 2.6. In

I_{sc}/I_l	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h < 50$
<20	4.0	2.0	1.5	0.6	0.3

Table 2.6: Limits of harmonic current in percent of the load current specified in the IEEE 519 documentation, focus on a weak grid [11].

the IEEE 519 standard, a suitable SCR parameter representing a reasonably weak grid can be identified in $R_{sce} = I_{SC}/I_l = 20$ ($Z_{SC} = 5\%Z_l$), which can be an acceptable condition due to the high grid impedance.In addition, a lower SCR could not be feasible for the difficulty in representing the corresponding type of grid, and a higher SCR might not denote a weak grid properly.

2.3 Grid impedance determination

For the SCR under exam, the short circuit current is:

$$I_{SC} = 20 \cdot I_l = 640\,A \tag{2.1}$$

with $I_l = 32\,A$. The grid impedance can be estimated by referring to phase quantities, and leading to:

$$Z_g = \frac{V_g}{I_{SC}} = 0.359\,\Omega \tag{2.2}$$

with $V_g = 230\,V$. At 50 Hz the grid inductance will be equal to:

$$L_g = \frac{Z_g}{2\pi\,50} \approx 1.1\,mH \tag{2.3}$$

The grid itself, due to its complexity and variability on the basis of the PCC, is not uniquely determined and its impedance could not be linear for an extended range of frequency. Therefore an assumption of inductive behaviour has been accomplished for a fixed range of frequencies. The choice of the range is made through the normative

analysis. The goal of the work is to design a grid emulator capable of testing the correct behaviour of the On-Board Charger. However, a future use for testing other products is not excluded, hence it is assumed a general range of frequencies specified by normative IEC 61851-21-1. The normative indicate harmonic current limits from the first harmonic up to the 40^{th} harmonic (at 2 kHz for 50 Hz operation) [9]. Higher order harmonics are less frequent, except from the PWM modulation harmonics. In this way a correct measure of harmonics from 0 to 2 kHz is possible. In case of capacitive elements of the filter, the linearity of the impedance characteristic is compromised, especially for higher frequencies.

2.4 Thermal management and switches selection

The thermal aspect is crucial for the design of every electronic converter, given that the performances and the efficiency are deeply affected by the thermal management. The efficiency of the system is not a primary goal of the project, on the other hand the harmonic content is it. For this reason, the direction of selecting a high switching frequency at the expense of consistent switching losses has been followed. A simulation to validate the thermal behaviour at high switching frequency has been made.

As the thermal simulation was not a key aspect of the thesis work, only an overview is provided hereunder. The design of the hardware part was based on the choice of the module among those available in the company, which have been analyzed under the point of view of minimum temperature reached during the nominal functioning (refer to the Table 2.3). A three-phase inverter delivering power to a passive load was considered.The temperature limit was set by looking at the maximum junction temperature the switch can stand specified by datasheet. It has been verified that the junction temperature can reach 175 °C as limit temperature. As a consequence it is necessary to avoid reaching a temperature close to that limit. As a consequence, a maximum limit of 150 °C has been selected in the simulations.
The cooling type is liquid cooling, and the cooling temperature is fixed at 25 $°C$, as these will be the testbench cooling conditions.
An initial frequency of 100 kHz was selected to first evaluate the inverter thermal performances. The results of a steady-state analysis at 100 kHz have shown that the Onsemi NXH006P120MNF2PTG module was the one with a superior thermal behaviour considering the requirements stated before.

The overall losses of the three-phase inverter amount to 414 W.

The just analyzed results indicate that 100 kHz lead to a manageable thermal situation in nominal conditions. For the work's aim, a higher switching condition would be desirable because it brings naturally to a more effective filtering effect and it is achievable. However, higher switching frequencies can make the inductor design hard to carry out due to losses dependent on current and voltage ripple frequency. Additionally, the safety margin with respect to the maximum temperature admissible is satisfying and finally it is to be considered that 100 kHz is a significantly high switching frequency. To conclude, as it will be explained in the next chapter, a frequency doubling effect will be present in the

single-phase operation due to the commutation technique. As a result, 100 kHz was the selected switching frequency for the filter sizing, and the Onsemi NXH006P120MNF2PTG was the chosen module (Figure 2.3).

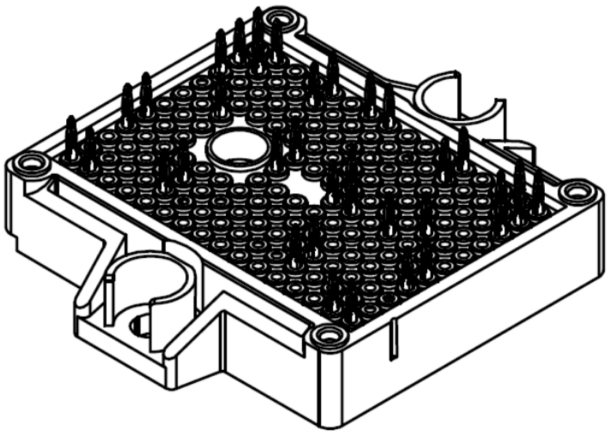

Figure 2.3: Onsemi NXH006P120MNF2PTG module.

The dead time for a SiC MOSFET cannot be defined beneath 100 ns. The high switching frequency imposes the use of the smallest dead time possible. A safety margin was taken and the dead time was set to:

$$t_{dead} = 200\,ns \tag{2.4}$$

2.5 Simulation circuit

The grid emulator has been simulated in Simulink to study the filter and the control performances. The three-phase simulation circuit has been implemented as in Figure 2.4. From the three-phase circuit, the single-phase circuit is obtained by using two phases only. The phase "v" is connected to a neutral.

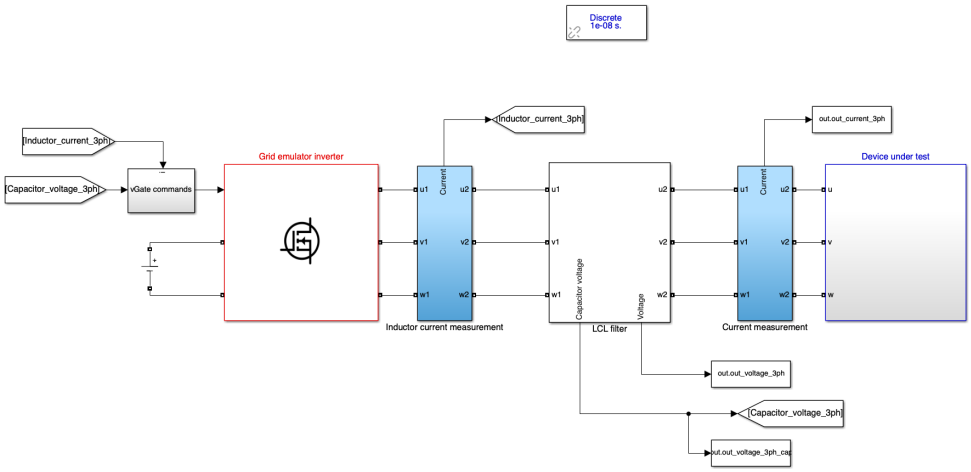

Figure 2.4: Simulink environment for the verification of the grid emulator control and validation of filter.

Chapter 3

Filter design

3.1 Modulation technique selection

The design of the filter is dependent on the commutation technique adopted for the working operation. What is more, voltage and current ripples are different between single-phase operation and three-phase operation.

For the purpose of the work, the unipolar modulation technique is chosen for the one phase operation. This allows to ease the sizing of the filter elements. The ripple frequency regarded for the filter sizing is in this case 200 kHz.

For the three-phase working operation, it has been opted for a regular sampled PWM modulation (RS-PWM), which lets to implement balanced enveloped modulation (BEM). The modulation index can be thus extended from m=1 to m $\approx$ 1.15. The peak ideal voltage in these conditions is $V_{peak} = V_{DC}/\sqrt{3} \approx 433V$. The voltage zero sequence determination is necessary and it has been by evaluated identifying the half current medium voltage among the triad, as in Equation 3.1 [8]:

$$v_{zs} = \frac{1}{2}(V_{max} + V_{min}) \tag{3.1}$$

Since the single-phase operation generates a ripple frequency doubled with respect to the switching frequency, the three-phase operation is the worst case scenario for the calculation of the voltage and current ripples, as it will be shown later on.

3.2 Filter constraints and equivalent circuits definition

By the literature review, the topology of output L filter can be excluded due to the low filtering effect with respect to the LC and LCL solutions. Another issue of the pure inductive filter is the absent filtering effect in no-load condition.
Both the LC as well the LCL filter topologies are suitable options for the filter. However,

for the considerations in subsection 1.3 and chapter 2.2, an output inductance makes it possible to smoothly adjust the grid impedance and obtaining the desired grid condition. Thus an LCL filter has been designated and developed. The Figure 3.1 shows the topology and nomenclature of the single-phase equivalent circuit of the LCL filter.

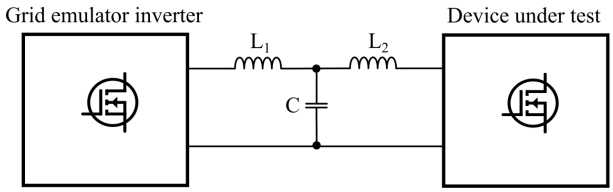

Figure 3.1: Topology and nomenclature of the single-phase equivalent filter stage.

For a correct evaluation of the filter elements it is necessary to consider specific constraints, laid down below, along with the mathematical expressions to calculate the relative parameter.

1. The resonance frequency has to be far enough from the grid frequency and from the switching frequency to avoid amplification of low order harmonics and switching harmonics [1]:
$$10\, f_g < f_{res} < f_{sw}/2 \tag{3.2}$$

2. The current ripple in the converter side inductor (L_1) should not exceed the 20 % of the nominal peak current [16], [18]:
$$L_1 \geq \frac{V_{DC}}{f_{sw} \cdot \Delta_{i,\,max} \cdot 8} \tag{3.3}$$
The above formula (typical for single-phase converters) has been assumed for the three-phase operation as well. $\Delta_{i,\,max}$ is the peak to peak admissible current ripple.

3. The maximum no-load current is limited to avoid excessive losses during no load operation. Consequently, a maximum reactive power of 10 % of the nominal power is set [1]:
$$C \leq \frac{Q_{max}}{3 \cdot \pi \cdot f_{grid} \cdot V_{pk}^2} \tag{3.4}$$
where V_{pk} is the peak fundamental voltage and Q_{max} is the maximum reactive power admissible.

4. The minimum filter attenuation must fulfil the harmonic requirements defined in chapter 2.

5. The equivalent impedance seen from the DUT has to be as much as possible attributable to an inductive characteristic typical of a grid in the range 0 - 2 kHz.

6. The grid inductance should be:

$$L_g = 1.1\,mH \tag{3.5}$$

as calculated in chapter 2.2. Hence, the sum of the filter inductances has to be equal to L_g.

$$L_1 + L_2 = L_g \tag{3.6}$$

The equivalent circuit for the verification of contraints 5 is conceived assuming the inverter as a short circuit. It is needed to verify the equivalent impedance seen from the CUT side. Thanks to symmetrical three-phase properties, it is possible to consider the single-phase equivalent scheme, as in Figure 3.2. A similar remark can be assumed for

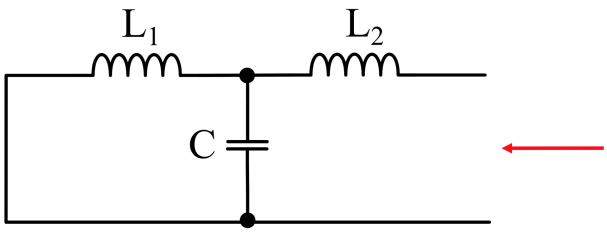

Figure 3.2: Equivalent circuit of the grid emulator from the DUT side. The arrow highlights the direction from which the equivalent impedance is studied.

the equivalent circuit of constraint number 6, but the converter is not short circuited, and it is assumed as an ideal high frequency voltage generator. In particular, two different situations can be identified in terms of harmonic disturbances:

- The worst condition for the harmonic current disturbances at the output of the filter is when the DUT is shorted (not occurring condition);
- The worst condition for the harmonic voltage disturbances is when the filter output is open circuited (no-load condition, it can occurr).

In the first situation, the consequent voltage disturbances can be derived with the hypotesis of pure resistive load at the terminals of the filter.
The second situation is instead a working condition of the grid emulator and represents the worse condition in terms of voltage harmonic. Being the constraints defined in Table 2.4 valid for the no-load working as well, it is possible to evaluate the voltage ripple at the terminal of the LCL filter through the equivalent circuit represented in Figure 3.3.

The transfer function under study has been already analyzed (1.7). However, the parasitic and the damping elements have been included for the computation of the filter, hence the transfer function assumes the form of equation 3.21.

$$G_{LC} = \frac{Z_2}{Z_2 + Z_1} \tag{3.7}$$

with:

$$Z_1 = R_{L_1} + s \cdot L_1 \tag{3.8}$$

$$Z_2 = ESR_C + s \cdot ESL_C + \frac{1}{s \cdot C} \tag{3.9}$$

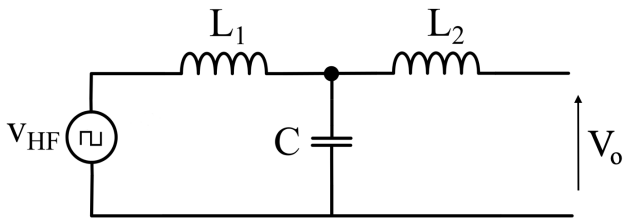

Figure 3.3: Equivalent circuit of the grid emulator from the DUT side. The ideal generator v_{HF} denotes the high frequency voltage disturbance, as it is the only voltage component of interest. V_o is the output voltage.

In order to evaluate the filtering effect three possibilities can be identified:

- The first one consists in evaluating the required voltage attenuation between input (v_{HF}) and output (V_o) through the transfer function and verifying the one relative to the filter under study [1];
- The second one is based on the acquisition of the non filtered voltage waveform of the converter by simulation, to be filtered analytically in a post-processing script. Even in such a case it is necessary to consider the transfer function of the filter.
- The third consists in measuring directly the RMS value of the ripple waveform for the frequency higher than the fundamental one in a simulation environment.

The second method has been followed: the simulation circuit is depicted in Figure 2.4. A measure of the high frequency RMS voltage value is post-processed in MATLAB by analyzing the harmonic spectrum resulting from the simulation.

3.3 Preliminary determination of the filter elements

With the previous imposed constraints, the results of the limit parameters are presented in Table 3.1 and refer to the maximum (minimum) allowable quantity according to equations (3.3), (3.4) and (3.6).

L_1	C	L_2
103.6 μH	44.12 μF	1 mH

Table 3.1: Preliminary filter parameters.

The resonance frequency of such design is calculated via equation 1.9, and it amounts to:

$$f_{res} = 2.52\,kHz \tag{3.10}$$

A visual verification of the equivalent impedance trend is provided in Figure 3.4, where both an ideal grid impedance with inductance $L_g = 1.1\,mH$ and the equivalent grid impedance at the terminals of the grid emulator is plotted against the frequency.

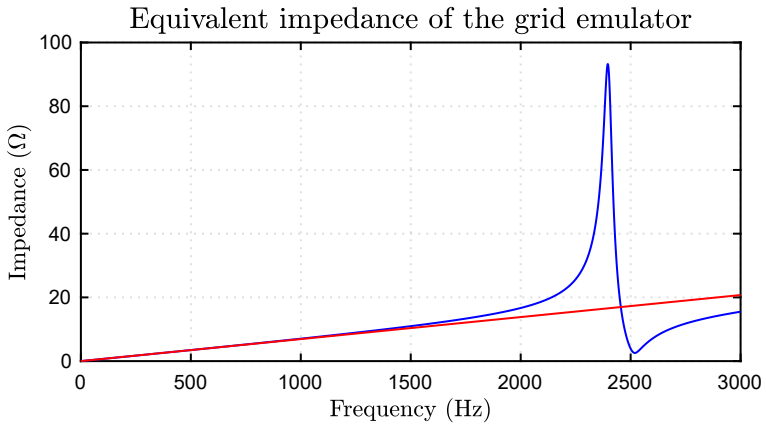

Figure 3.4: Equivalent impedance of the grid emulator (blue) together with an ideal grid impedance (red) against the frequency. It is noticeable the steep impedance variation due to the proximity of the resonance frequency.

The grid emulator impedance characteristic is obtained considering also typical Equivalent Series Resistance (ESR) of a 44 μF capacitor and typical DC resistance of an inductor, which are respectively 5 $\mu\Omega$ and 20 $m\Omega$, to provide damping of the resonance.
A deviation from the ideal grid impedance is observable from 1500 Hz, and the resonance frequency is close to the limit of 2 kHz. Therefore, a redefinition of the filter elements has been carried out to establish a considerable margin between the 2 kHz and the resonance

frequency.
The filter redefinition can be performed in two different ways: either by decreasing the capacitance or the inductance of the components. However, the overall inductance value is fixed by constraint number 6, and decreasing the low value inductance L_1 (i.e., the converter side inductance) is not possible due to constraint number 2. As a consequence the capacitance parameter has been varied. It is necessary to verify the feasibility of such a strategy in terms of filtering effect (constraint number 4).

3.4 New filter design

A new capacitance value was selected as $C = 20\,\mu F$, hence the resonance frequency is:

$$f'_{res} = 3.67\,kHz \tag{3.11}$$

With the new filter parameters fixed, the new impedance characteristic of the grid emulator appears as in Figure 3.5.

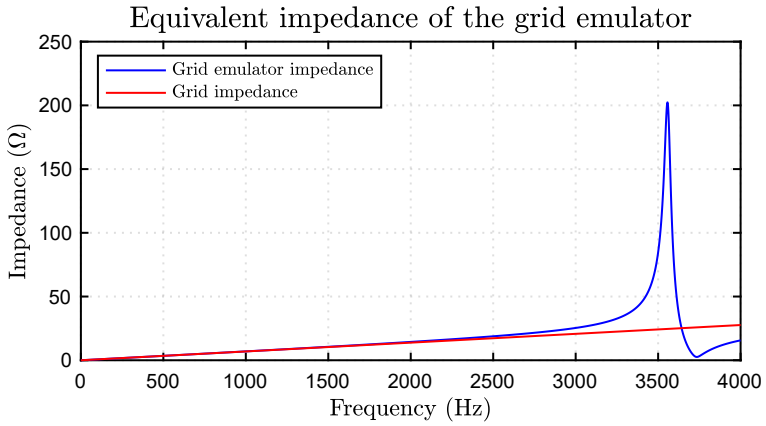

Figure 3.5: New equivalent impedance of the grid emulator (blue) together with an ideal grid impedance (red) against the frequency. The resonance frequency is far away from the interval of interest.

3.5 Preliminary simulations

Preliminary simulations have been realized to test the performances of the selected filter and its filtering effect. The circuit model is implemented as in Figure 2.4. The simulation data are listed in Table 3.2.

f_{sw}	100 kHz
V_{DC}	750 V
L_1	104 μH
L_2	1 mH
C	20 μF
ESR_C	5 $m\Omega$
ESL_C	40 nH
R_{L_1}	20 $m\Omega$
R_{L_2}	20 $m\Omega$

Table 3.2: Simulation parameters.

In Figure 3.6 three-phase voltages in no-load condition are depicted.

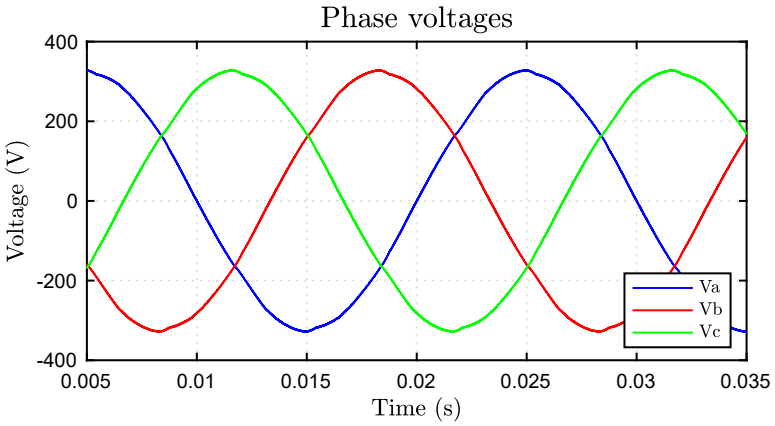

Figure 3.6: Phase voltage measured across the filter capacitors in no-load conditions.

The spectral analysis of the three-phase voltages (Figure 3.7) shows a little peak due to the resonance frequency. In these conditions, the RMS voltage ripple is:

$$V_{o,rms} = 0.44\, V_{rms} \tag{3.12}$$

A similar simulation has been performed for the single-phase system. The results appear as in Figure 3.8.

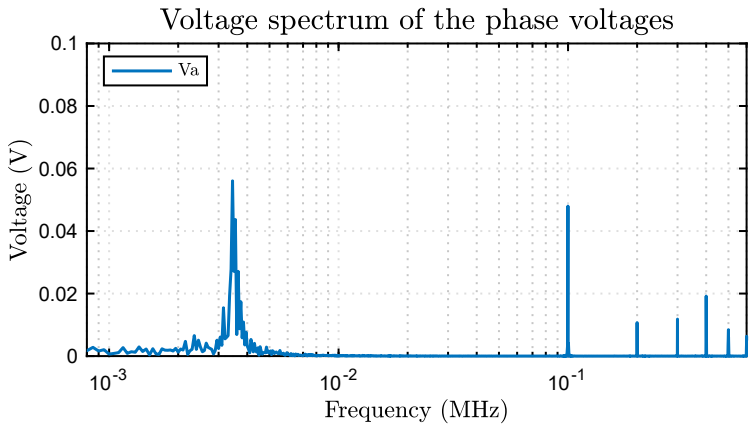

Figure 3.7: Phase voltages spectrum in three-phase no-load simulation.

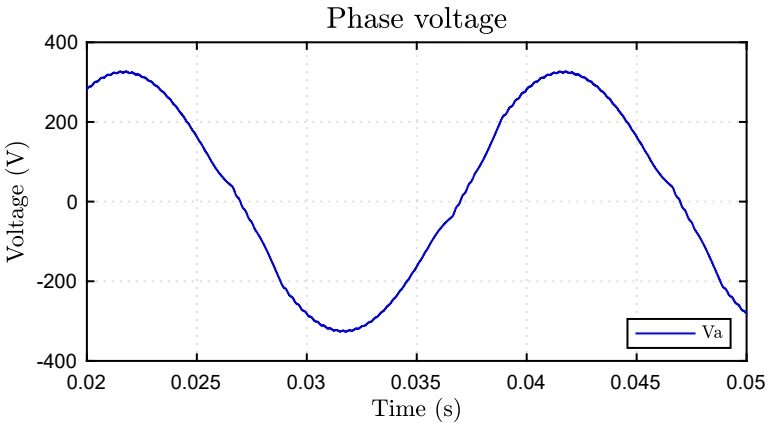

Figure 3.8: Single-phase voltage in no-load conditions.

Even in this case a spectrum analysis of the waveform shows a value of 0.07 V (Figure 3.9) caused by the resonance. The total RMS voltage ripple results in:

$$V_{o,rms} = 0.97\, V_{rms} \tag{3.13}$$

caused mainly by the relevant resonance effect. However, the constraint of maximum output voltage ripple is fulfilled.

3.6 Damping system sizing

The damping of the filter resonance can become essential in a controlled system because the stability may be severely compromised. When dealing with open-loop controls, it might not be necessary due to the natural damping effect of the reactive elements. However, the grid emulator under study has to be capable of standing perturbations coming

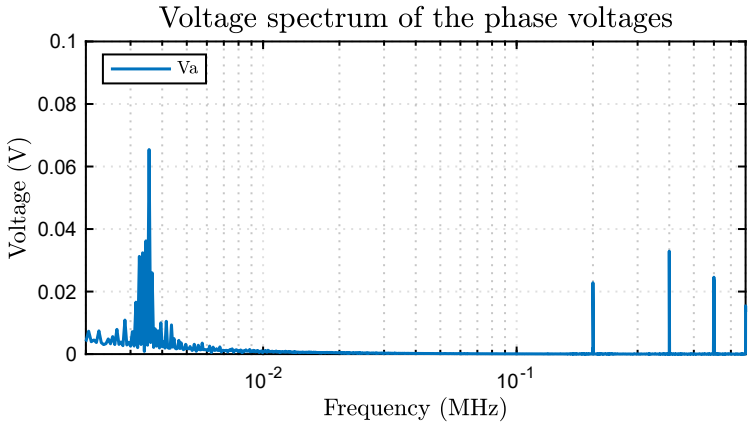

Figure 3.9: Phase voltage spectrum in single-phase no-load simulation

from the DUT (which, as has been said, can be different converters). In addition, the type of control was not yet defined, so the damping has been implemented anyway for protection reasons.

Two types of damping systems have been simulated, and the most performing one has been selected:

- series damping;
- parallel damping.

Series damping sizing

A first attempt has been made with the series damping, as it is the easiest one according to 1.6. The series resistance is calculated as suggested in [1]:

$$R_{damping} = \frac{1}{3 \cdot \omega_0 \cdot C} = 0.72\Omega \tag{3.14}$$

where ω_0 is the resonance pulsation of the filter. On the one hand, the damping effect brings benefits to system stability; on the other hand reduces the filtering effect. The effect of the series damping is well represented in Figure 1.13, where it can be seen a slight reduction of the steepness at higher frequencies. This reflects significantly on the filter performances, as at 100 kHz the no-load calculated voltage ripple is:

$$V_{o,rms,series\,3ph} = 1.10\,V_{rms} \tag{3.15}$$

$$V_{o,rms,series\,1ph} = 1.49\,V_{rms} \tag{3.16}$$

The worst-case voltage spectrum (single-phase functioning) is plotted in Figure 3.10.
which is not in compliance with the requirements stated in Table 2.4.

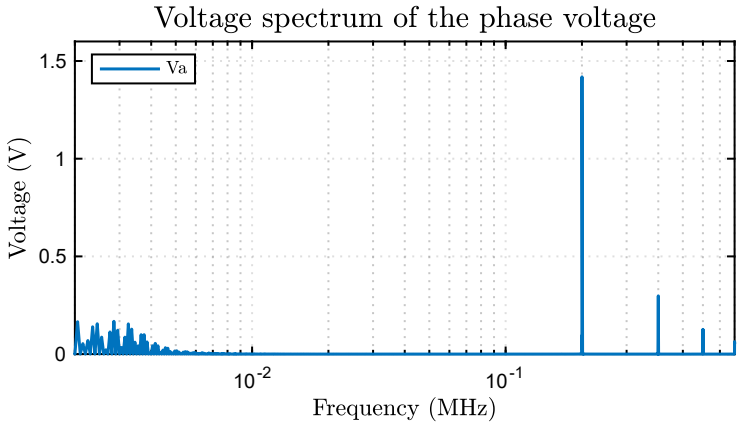

Figure 3.10: Voltage spectrum of the one phase no-load waveform

The peak-to-peak maximum voltage ripple has been examined too. The worst condition for the voltage ripple can be observed in the three-phase working operation when the zero crossing of the voltage occurs [19]. Though the same value is observed in one-phase operation, during the fundamental peak voltage. In these conditions, the ripple voltage is calculated as follows.

$$V_{ripple,pkpk,max} = \Delta_{i,pkpk,max} \cdot (R_{damping} + ESR_C) = 6.71V \tag{3.17}$$

This conditions does not verify during normal operation since it refers to a peak fundamental voltage of 375 V, which is not distant from the 325 V nominal operation. Even though it is not a primary requirement, the previous result could represent a high peak-to-peak value.

Parallel damping sizing

Another solution for the damping system has been studied. The parallel damping is described in Section 1.6. It is different from series damping due to the presence of two capacitors. The design process has been guided by the following three guidelines:

- the implementation of a more performing filter;
- a maximum total capacitance not exceeding the 20 uF;
- a damping effect as effective as possible.

The instructions reported in [17] have been considered for the design. Specifically, the document reports the relation between the filter elements to achieve the best damping effect.
The damping elements are named:

- C: filter capacitance;

- C_d: damping capacitance;
- R_d: damping resistance.

The circuit diagram is reported in Figure 1.15. The optimum damping of the resonance peak occurs when the following conditions are satisfied:

$$R_{d,opt} = \sqrt{\frac{L}{C}} \cdot \frac{n+1}{2 \cdot n} \cdot \sqrt{\frac{2 \cdot n^2 \cdot (4+n)}{(2+n) \cdot (4+3)}} \tag{3.18}$$

$$C_d = n \cdot C \tag{3.19}$$

with $n = 4$.

A better filtering effect can be obtained even when the total capacitance is reduced to 15 uF, and therefore:

- $C = 3\,\mu F$
- $C_d = 12\,\mu F$
- $R_d = 5.9\,\Omega$

The filtering effect has been computed by referring to typical parasitic parameters:

- ESR_C=20 $m\Omega$
- ESL_C=12 nH
- ESR_{C_d}=10 $m\Omega$
- ESL_{C_d}=23 nH

The impedance of the capacitor C at switching frequency is around 10 times lower than the series impedance $R_d + 1/(j\omega C_d)$. Thus, assuming a triangle-wave current ripple entering the main filter capacitor C (which is not exact), a conservative estimation of the maximum peak-to-peak voltage ripple is obtained in (3.20) during three-phase operation.

$$V_{ripple,pkpk,max} = \frac{1}{8} \cdot \frac{\Delta_{i,pkpk,max}}{C \cdot f_{sw}} = 3.77V \tag{3.20}$$

emerging at the voltage zero crossings. The advantage of such a damping configuration is its relative simplicity of implementation.

The transfer function can be described in the following way:

$$G_{LC} = \frac{Z_2}{Z_2 + Z_1} \tag{3.21}$$

with Z_1 and Z_2 expressed as:

$$Z_1 = R_{L_1} + s \cdot L_1 \tag{3.22}$$

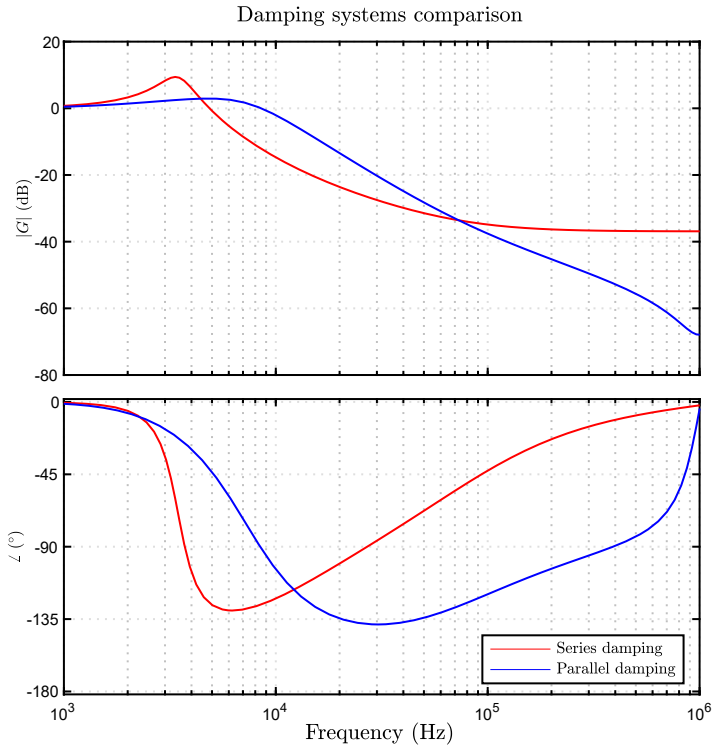

Figure 3.11: Comparison between the two analyzed damping solutions. A lower magnitude of the parallel damping in correspondence of 100 kHz is noticeable.

$$Z_2 = \frac{(R_d + \frac{1}{s \cdot C_d}) \cdot \frac{1}{s \cdot C}}{R_d + \frac{1}{s \cdot C_d} + \frac{1}{s \cdot C}} \tag{3.23}$$

A comparison between the two examined damping systems is hereafter illustrated through a Bode diagram in Figure 3.11. Finally, a summary of the two damping system features is given in Table 3.3.

	Series damping	**Parallel damping**
Resonance damping	+	++
Filtering effect attenuation	--	-
Simplicity	+	-

Table 3.3: Damping systems comparison.

3.7 Simulation of the proposed filter

The parallel damped configuration has been analyzed through a specific simulation. In particular, the following aspects have been validated:

- one-phase and three-phase RMS voltage ripple;
- peak-to-peak ripple: expected value 3.77 V.

The load is absent (no-load condition).
The RMS current flowing into the capacitors have been visualized to select proper capacitors. It is measured using the Simulink blocks implemented as in Figure 3.12. The specified fundamental frequency parameter is the grid frequency. At 60 Hz the capacitor impedance is lower, causing a higher no-load current flow. Consequently, the grid frequency is set at 60 Hz. Starting from the three-phase case, the no-load steady state-

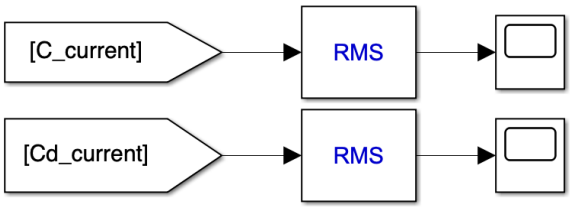

Figure 3.12: Simulink implementation for RMS current estimation.

voltages are depicted in Figure 3.13 and 3.14. It is visible how the high-frequency harmonic content is very low.

A Fourier analysis has been implemented offline, resulting in the voltage spectrum in Figure 3.15.

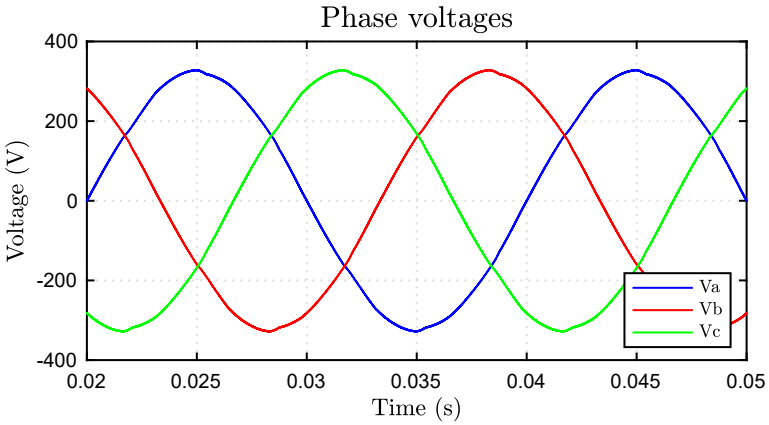

Figure 3.13: No-load three-phase voltages when parallel damping is implemented.

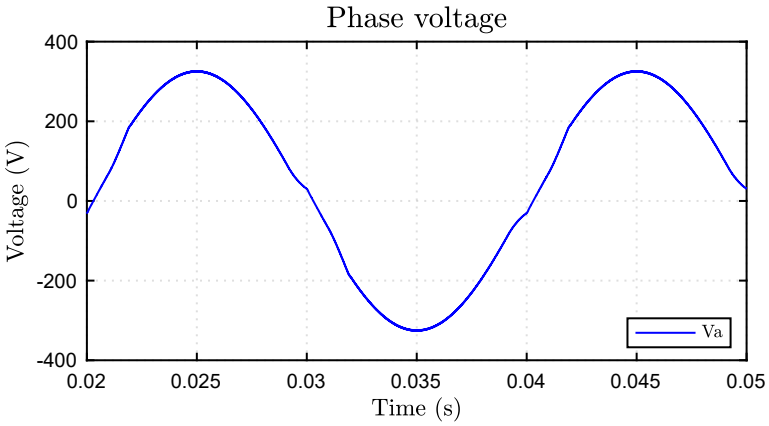

Figure 3.14: No-load single-phase voltage when parallel damping is implemented.

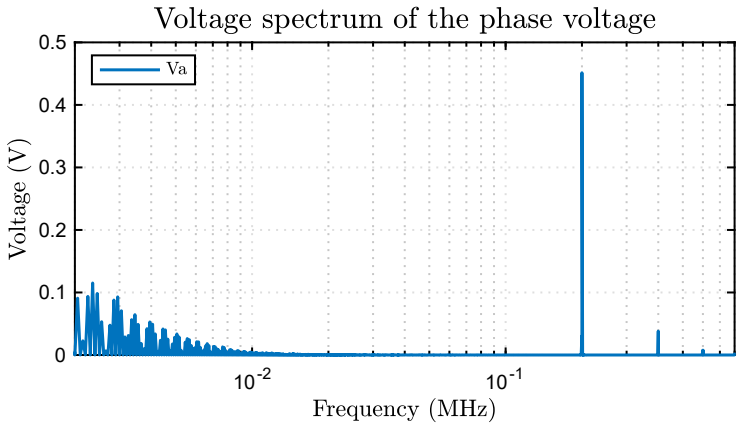

Figure 3.15: Voltage spectrum of the single-phase voltage in no-load condition. It is noticeable how the harmonics around the resonance frequency are negligible.

The result of the RMS voltage ripple is:

$$V_{o,rms,3-phase} = 0.57\, V_{rms} \tag{3.24}$$

$$V_{o,rms,1_phase} = 0.49\, V_{rms} \tag{3.25}$$

A representation of the peak-to-peak voltage ripple is provided in Figure 3.16, and corresponds to the voltage zero crossing instant.

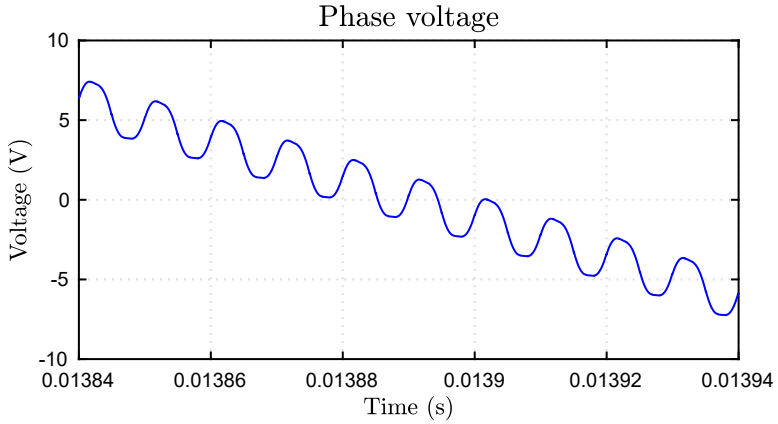

Figure 3.16: Detail on the phase voltage when zero-crossing occurs.

The measured peak to peak voltage during zero-crossing is around:

$$V_{o,\,pkpk,\,max} = 2.84V \tag{3.26}$$

The selected damping system is suitable for the application.
The RMS currents flowing into the capacitors C and C_d during normal conditions are, respectively:

$$I_{C,\,rms,\,3-phase} = 1.52\, A_{rms} \tag{3.27}$$

$$I_{C_d,\,rms,\,3-phase} = 1.05\, A_{rms} \tag{3.28}$$

during the three-phase operation.
In one phase operation, the RMS currents are:

$$I_{C,\,rms,\,1-phase} = 2.54\, A_{rms} \tag{3.29}$$

$$I_{C_d,\,rms,\,1-phase} = 1.04\, A_{rms} \tag{3.30}$$

3.8 Capacitor and resistance selection

A selection of the parts and the inductor design have been made using the prior results. Only available components at the time of the thesis's writing were selected. The data required for the capacitors search are contained in Tables 3.4 and 3.5.

Technology	Film	
Capacitance	3	μF
Total RMS current	2.54	A_{rms}
High-frequency RMS current	2.53	A_{rms}
Maximum voltage rating	750	V
AC voltage rating	265	V_{rms}

Table 3.4: Filter capacitor C requirements.

Technology	Film	
Capacitance	12	μF
Total RMS current	1.05	A_{rms}
High-frequency RMS current	0.14	A_{rms}
Maximum voltage rating	375	V
AC voltage rating	265	V_{rms}

Table 3.5: Damping capacitor C_d requirements.

Another important aspect to be considered is the resonance frequency of each capacitor, which has to be far enough from the ripple frequency. Such a feature has been verified from the datasheet, on the basis of the provided data.
The Film technology is required since electrolytic capacitors cannot stand AC voltages. Additionally, capacitors with the feature of being directly mounted on a proper support have been preferred. Thus, the search has been run among the capacitors with Lug terminations. Last but not least, the RMS AC voltage at low frequency (V_{AC}) has to comply with the maximum RMS voltage of the application (AC voltage rating; see Tables 3.5, 3.4).
The chosen capacitors are:

- Vishay MKP386M530125YT4;
- TDK B32656S8225J561;
- KEMET C4BTHBX5100ZALJ.

The TDK B32656S8225J561 and the KEMET C4BTHBX5100ZALJ are put in parallel to reach an overall capacity of $C_d = 12.2\,\mu F$. The specifications of each capacitor are described in each datasheet, reported respectively in Figure 3.17, Figure 3.18 and Figure 3.19.

VISHAY
www.vishay.com

MKP386M Snubber
Vishay Roederstein

ELECTRICAL DATA AND ORDERING CODE

U_{RDC} (V)	CAP. (µF)	DIMENSION (mm) (4) W	H	L	dU/dt (V/µs)	I_{peak} (A)	I_{RMS} (2) (A)	ESR (3) (mΩ)	tan δ 1 kHz < (10^{-4})	tan δ 10 kHz < (10^{-4})	tan δ 100 kHz < (10^{-4})	ORDERING CODE (1)
	U_{RAC} = 550 V; U_{pp} = 1550 V											
	0.33	22.0	30.5	33.5	800	264	7.0	16.0	4.0	8.0	40	MKP386M433125J**
	0.39	22.0	30.5	33.5	800	312	7.0	14.0	4.0	8.0	40	MKP386M439125J**
	0.47	22.0	30.5	33.5	800	376	8.0	11.0	4.0	8.0	40	MKP386M447125J**
	0.56	22.0	30.5	33.5	800	448	8.5	10.0	4.0	8.0	40	MKP386M456125J**
	0.68	22.0	30.5	33.5	800	544	9.5	8.0	4.0	8.0	40	MKP386M468125J**
	0.82	22.0	38.0	44.0	375	308	9.0	13.0	5.0	15.0	60	MKP386M482125J**
	1.0	22.0	38.0	44.0	375	375	10.0	10.0	5.0	15.0	60	MKP386M510125J**
	1.2	22.0	38.0	44.0	375	450	11.0	9.0	5.0	15.0	-	MKP386M512125J**
	1.5	30.0	46.0	44.0	375	563	14.0	7.0	5.0	15.0	-	MKP386M515125J**
1250	1.8	30.0	46.0	44.0	375	675	15.0	6.0	5.0	15.0	-	MKP386M518125J**
	2.0	30.0	46.0	44.0	375	750	16.0	5.5	5.0	15.0	-	MKP386M520125J**
	2.2	30.0	46.0	44.0	375	825	18.0	4.5	5.0	15.0	-	MKP386M522125J**
	U_{RAC} = 450 V; U_{pp} = 1300 V											
	2.2	25.0	45.0	58.0	225	495	14.0	6.0	7.5	20	-	MKP386M522125Y**
	2.5	25.0	45.0	58.0	225	563	15.0	5.0	7.5	20	-	MKP386M525125Y**
	3.0	25.0	45.0	58.0	225	675	16.5	4.0	7.5	20	-	MKP386M530125Y**
	3.3	30.0	45.0	58.0	225	743	18.0	4.0	7.5	20	-	MKP386M533125Y**
	4.0	35.0	50.0	58.0	225	900	21.5	3.0	7.5	20	-	MKP386M540125Y**
	4.7	35.0	50.0	58.0	225	1058	23.5	2.5	7.5	20	-	MKP386M547125Y**
	5.0	35.0	50.0	58.0	225	1125	24.5	2.5	7.5	20	-	MKP386M550125Y**

Figure 3.17: Vishay datasheet for the MKP386M capacitors series.

TDK

Metallized polypropylene film capacitors (MKP) **B32656S**

Snubber (wound)

Ordering codes and packing units

V_R V DC	V_{RMS} f ≤1kHz V AC	C_R nF	Max. dimensions w x h x l mm	I_{RMS} 100 kHz A	ESR_{typ} 100 kHz mΩ	Ordering code (composition see below)	Ter-minal	pcs./ MOQ
850	450	1800	28.0 x 37.0 x 42.0	15.5	4.5	B32656S8185+408	T8	108
		1800	28.0 x 37.0 x 42.0	15.5	4.5	B32656S8185+409	T9	108
		1800	28.0 x 37.0 x 42.0	15.5	4.5	B32656S8185+410	T10	80
		1800	28.0 x 37.0 x 42.0	15.5	4.5	B32656S8185+411	T11	72
		1800	28.0 x 37.0 x 42.0	15.5	4.5	B32656S8185+418	T18	108
		1800	28.0 x 37.0 x 42.0	15.5	4.5	B32656S8185+561	T1	108
		1800	28.0 x 37.0 x 42.0	15.5	4.5	B32656S8185+562	T2	108
		1800	28.0 x 37.0 x 42.0	15.5	4.5	B32656S8185+563	T3	96
		1800	28.0 x 37.0 x 42.0	15.5	4.5	B32656S8185+566	T6	108
		1800	28.0 x 37.0 x 42.0	15.5	4.5	B32656S8185+577	T7	96
		2200	30.0 x 45.0 x 42.0	17.0	4.0	B32656S8225+408	T8	48
		2200	30.0 x 45.0 x 42.0	17.0	4.0	B32656S8225+409	T9	48
		2200	30.0 x 45.0 x 42.0	17.0	4.0	B32656S8225+410	T10	80
		2200	30.0 x 45.0 x 42.0	17.0	4.0	B32656S8225+411	T11	64
		2200	30.0 x 45.0 x 42.0	17.0	4.0	B32656S8225+418	T18	48
		2200	30.0 x 45.0 x 42.0	17.0	4.0	B32656S8225+561	T1	48
		2200	30.0 x 45.0 x 42.0	17.0	4.0	B32656S8225+562	T2	48
		2200	30.0 x 45.0 x 42.0	17.0	4.0	B32656S8225+563	T3	96
		2200	30.0 x 45.0 x 42.0	17.0	4.0	B32656S8225+566	T6	48
		2200	30.0 x 45.0 x 42.0	17.0	4.0	B32656S8225+577	T7	96

Figure 3.18: TDK datasheet for the B32656S capacitors series.

Cap Value (µF)	VDC	VAC	Peak VDC	Size Code	Maximum Dimensions (mm)			Ripple Current	Peak Current	ESR (max)	ESL	dV/dt (V/µs)	Packaging Quantity	Part Number
					T	H	L	100 kHz 70°C (A)	(A)	100 kHz (mΩ)	(nH)			
2.5	600	330	800	F	20	40	41.5	18	176	5.7	41	70	52	C4BTHBX4250Z(1)FJ
2.5	600	330	800	F	20	40	41.5	18	176	5.7	41	70	48	C4BTHBX4250Z(2)FJ
2.5	600	330	800	F	20	40	41.5	18	176	5.7	41	70	40	C4BTHBX4250Z(4)FJ
3	600	330	800	F	20	40	41.5	20	211	4.8	41	70	52	C4BTHBX4300Z(1)FJ
3	600	330	800	F	20	40	41.5	20	211	4.8	41	70	48	C4BTHBX4300Z(2)FJ
3	600	330	800	F	20	40	41.5	20	211	4.8	41	70	40	C4BTHBX4300Z(4)FJ
4	600	330	800	F	20	40	41.5	23	281	3.6	41	70	52	C4BTHBX4400Z(1)FJ
4	600	330	800	F	20	40	41.5	23	281	3.6	41	70	48	C4BTHBX4400Z(2)FJ
4	600	330	800	F	20	40	41.5	23	281	3.6	41	70	40	C4BTHBX4400Z(4)FJ
5	600	330	800	F	20	40	41.5	25	351	2.9	41	70	52	C4BTHBX4500Z(1)FJ
5	600	330	800	F	20	40	41.5	25	351	2.9	41	70	48	C4BTHBX4500Z(2)FJ
5	600	330	800	F	20	40	41.5	25	351	2.9	41	70	40	C4BTHBX4500Z(4)FJ
6.8	600	330	800	J	28	37	42.5	31	478	2.2	41	70	36	C4BTHBX4680Z(3)JJ
8	600	330	800	H	24	44	41.5	34	562	1.9	43	70	44	C4BTHBX4800Z(1)HJ
8	600	330	800	H	24	44	41.5	34	562	1.9	43	70	40	C4BTHBX4800Z(2)HJ
10	600	330	800	L	30	45	42	40	703	1.6	43	70	32	C4BTHBX5100Z(3)LJ
12.5	600	330	800	M	30	45	57.5	35	592	2.5	45	47	24	C4BTHBX5125Z(3)MJ
15	600	330	800	M	30	45	57.5	38	710	2.1	45	47	24	C4BTHBX5150Z(3)MJ
20	600	330	800	N	35	50	57.5	47	947	1.7	48	47	21	C4BTHBX5200Z(3)NJ

Figure 3.19: KEMET datasheet for the C4BT capacitors series.

The criteria for choosing the damping resistance $R_d = 5.9\,\Omega$ were the availability of components and the feature of being easily mounted. The requirements for the resistor were:

- $R = 5.9\,\Omega$;
- $P_n > 4.5\,W$.

The damping resistance RHA0256R000FE02 has been chosen. The feature are:

- $R = 6\,\Omega$;
- $P_n = 12.5\,W$ (free air convection).

3.9 Inverter side inductor L_1 design

The inverter side inductor data necessary for the sizing are listed in Table 3.6. As for the capacitors, the materials have been identified among those available. The maximum

Inductance (L_1)	104	μH
Nominal RMS current ($I_{L1,rms}$)	32.11	A_{rms}
Maximum peak current ($\hat{I}_{L1}$)	58.8	A
AC voltage rating ($V_{AC,L_1,rms}$)	265	V_{rms}
Maximum voltage rating ($\hat{V}_{L_1}$)	750	V

Table 3.6: Inverter side inductor (L_1) requirements.

peak current has been identified considering a 20% overload operation. The RMS current

flowing into the component has been obtained from equation (3.31)

$$I_{L_1,rms} = \sqrt{I_{n,rms}^2 + \Delta i_{L_1,rms}^2} \tag{3.31}$$

A proper material has to be selected to stand the high frequency voltage ripple produced by PWM modulation ripple.
For the high availability of ferrite cores and the large use among power electronics systems, a ferrite material has been chosen. Multiple gap cores produced by the TDK have been chosen. According to the company, the main benefits related to the multi-gapped core (called distributed gap core by the company) are:

- Increased power density;
- Reduced losses arising from eddy currents and proximity effect;
- Improved thermal properties;
- Temperature stability till 180 $°C$ [20].

The TDK distributed air gap cores are mainly realized with N87, N95 and N97 materials. To identify an appropriate core specific constraints along with electrical and magnetic data have been fixed and summarized in Table 3.7. For N87, N95 and N97 ferrites the saturation point can be identified as slightly higher than 0.3 T. Thus, a limit of 0.32 T was decided (even when an overload of 20% occurs). A safe current density value for a copper wire was decided as 4 A/mm^2. The window utilization k_u was set to 0.25 assuming a Litz wire for the winding. A standard copper wire was selected, with winding resistivity $\rho_w = 1.68 \cdot 10^{-8}$ and with void permeability μ_0. The maximum permissible temperature increment has been set to 90 $°C$, assuming an ambient temperature of 25 $°C$.

$\hat{B}_{L_1}$	0.32	T
$J_{L_1,rms}$	4	A/mm^2
k_{u,L_1}	0.25	
ΔT_{L_1}	50	$°C$
ρ_w	$1.68 \cdot 10^{-8}$	$\frac{\Omega}{m}$
μ_0	$4\pi \cdot 10^{-8}$	$\frac{H}{m}$

Table 3.7: Inductor design data.

The area product is a useful parameter to evaluate the size of the needed core. It is expressed in equation (3.32) for the L_1 inductor.

$$A_p = \frac{L_1 \cdot \hat{I}_{L_1} \cdot I_{L_1,rms}}{k_{u,L_1} \cdot J_{L_1,rms} \cdot \hat{B}_{L_1}} = 66.27\, cm^4 \tag{3.32}$$

Once selected a core the inductance per turn A_l is provided. The total inductance can be obtained as in equation (3.33):

$$N = \sqrt{\frac{L_1}{A_l}} \tag{3.33}$$

The verification of the $\hat{B}$ can be made by the mean of equation (3.34).

$$\hat{B}_{L_1} = \frac{\hat{I} \cdot L_1}{N \cdot S_{fe}} \tag{3.34}$$

where S_{fe} is the iron surface. The winding has to fit into the available window. Thus, the equation (3.35) must hold.

$$A_w < k_{u,\,L_1} \cdot W_a \tag{3.35}$$

where A_w is the area occupied by the conductors.

Finally, the overall losses must be lower than the maximum dispersible power in free air conditions. An empirical formula to evaluate the maximum power is provided in equation (3.36).

$$P_{loss}^{max} = \frac{\Delta T}{R_{th}} \tag{3.36}$$

where R_{th} is the thermal resistance estimated from the empirical formula (3.37). The maximum temperature variation with respect to $25°C$ is defined equal to $\Delta T = 90°C$

$$R_{th} = \frac{0.06}{\sqrt{V_c}} \tag{3.37}$$

Hence:

$$P_{loss,\,L_1} < P_{loss,\,L_1}^{max} \tag{3.38}$$

The selected core was the TDK E 70/33/32 DG, one of the largest available. Its data are enumerated in Table 3.8. The core drawing and its measurements are represented in Figure 3.20. Such core does not let to have the required area product, which was:

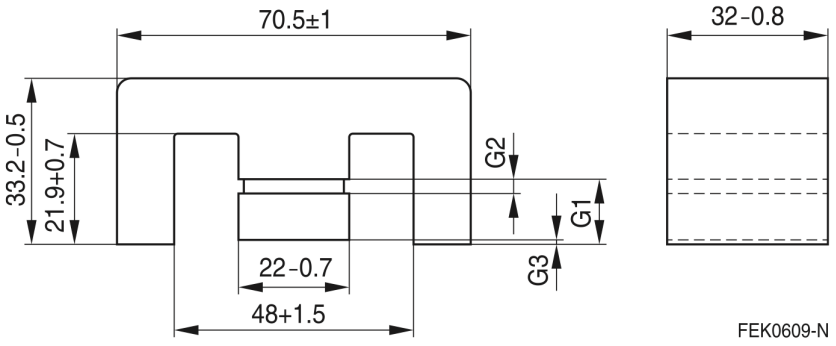

Figure 3.20: Core TDK E 70/33/32 DG dimensions.

$$A_{p,core} = 38.5\,cm^4 \tag{3.39}$$

Moreover, the corresponding coil former is designed to host 2 couples of E-cores, reaching $A_p = 77\,cm^4$ overall. Normally an optimal μ_{opt} can be calculated to obtain the maximum exploitation of the core. Nevertheless, the multi-gap cores allow to obtain few air gaps

Volume (V_c)	102000	mm^3
Effective magnetic path (l_c)	149	mm
Window area (W_a)	569.4	mm^2
Minimum iron surface (S_{fe})	676	mm^2
Mean turn length for two couples of cores (l_{mean})	230.5	mm

Table 3.8: E 70/33/32 DG data.

lengths depending on the model. No adding gap was selected and a direct comparison among different realizable solutions was carried out. For the selected core, two different air gap lengths have been taken into account. The comparison among the solutions is summarized in Table 3.9. The core is composed by two pair of E-core in parallel, to form a unique core to wrap. The material of both models is N87. The graphical representation of the ferrite N87 is represented in Figure 3.21.

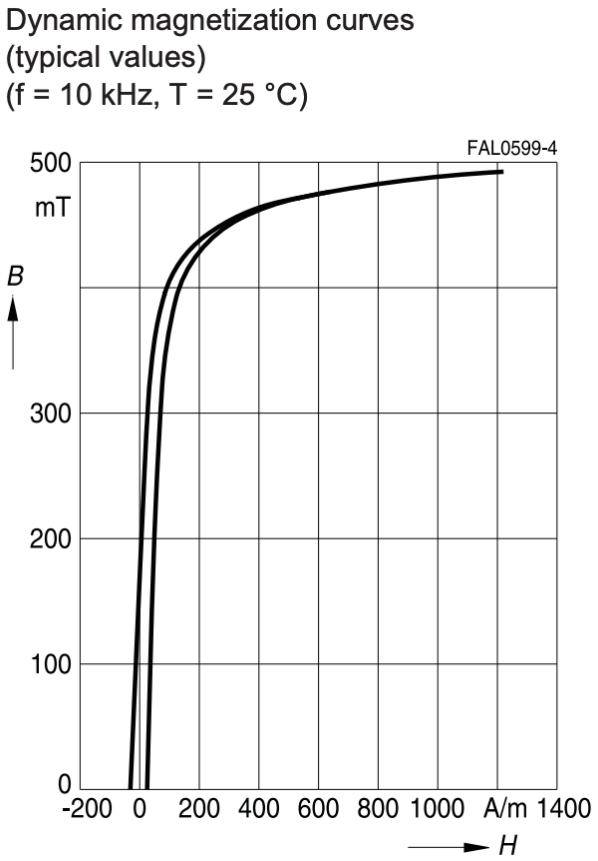

Figure 3.21: N87 B-H curve at $T = 25°C$.

The second solution has been selected for its better core exploitation and for the lower

$A_l(nH)$	N	$\hat{B}$(T)
100	23	0.20
250	15	0.32

Table 3.9: Comparison among two different inductor solutions.

number of turns which allows to better wrap the winding. The final inductance value is $L_1 = 112.5\mu H$. If the turns had been 14, the overall inductance would have been $98\mu H$. The copper wire section has been calculated from J_{L_1} as follows:

$$S_w = \frac{I_{L_1,rms}}{J_{L_1,rms}} = 8\,mm^2 \tag{3.40}$$

To ease the construction of the inductor, a parallel of two wires of diameter $d' = 2.24mm$ has been made, being the sum of conductor areas almost equal to the requirement.

Losses computation

The overall losses are caused by copper losses and iron losses. The copper losses can be further distinguished into DC and AC losses.
DC losses are calculated from the well-known equation (3.41).

$$P_{DC} = R_{DC} \cdot I^2_{L_1,rms} \tag{3.41}$$

where R_{DC} is equal to:

$$R_{DC} = \rho_w \cdot \frac{l_{mean}}{S'_w} \cdot N = 7.4m\Omega \tag{3.42}$$

As a consequence, DC losses are:

$$P_{DC} = 7.57\,W \tag{3.43}$$

AC losses result from:

- skin effect;
- proximity effect.

The proximity effect is caused by the mutual influence of current distribution between nearby conductors. This leads to resistance increasing. Such an effect is neglected for its difficulty to be estimated and/or simulated with finite elements method (FEM) analysis. In addition, the multiple air gap core permits decreased losses due to proximity effects and eddy currents. Alternatively, an additional margin from the maximum losses can be

taken.
The skin effect losses are due to the current high frequency ripple. The penetration thickness in worst condition ($f_{ripple} = 200kHz$) is calculated as in equation (3.44).

$$\delta = \frac{1}{\sqrt{\pi \cdot f_{ripple} \cdot \mu_0 \cdot {\rho_w}^{-1}}} = 0.15\,mm \tag{3.44}$$

From this result, a rough estimation of the AC resistance can be obtained for high frequency as in equation (3.45):

$$R_{AC} = \frac{\rho_w}{2} \cdot \frac{l}{\pi \cdot r^2 - \pi \cdot (r-\delta)^2} = 60.4m\Omega \tag{3.45}$$

The AC losses are approximated with the equation:

$$P_{AC} = R_{AC} \cdot \Delta i^2_{L_1,\,rms} = 0.18\,W \tag{3.46}$$

Specific iron losses are being calculated through the improved generalized Steinmetz equation (iGSE):

$$p_{fe} = \frac{1}{T}\int_0^T k_i \cdot \left|\frac{dB}{dT}\right| \cdot (\Delta B)^{\beta-\alpha} \cdot dt \tag{3.47}$$

where

$$k_i = \frac{K_c}{(2\pi)^{(\alpha-1)} \int_0^{2\pi} |cos(\theta)^\alpha| \cdot d\theta} \tag{3.48}$$

The overall iron losses are calculated through an already available program. A conservative estimation ot the iron losses is, therefore:

$$P_{fe} = p_{fe} \cdot V_c = 10\,W \tag{3.49}$$

leading to an overall amount of losses of:

$$P_{loss,\,L_1} = 17.6\,W \tag{3.50}$$

From equation (3.38) the total losses are $P^{max}_{loss} = 21.4\,W$. Thus the design is validated from the losses point of view considering the overload as a transitional operation.

3.10 Output side inductor $L2$ design

The main function of the output inductor L_2 is to provide a good representation of the grid impedance. As mentioned in chapter 2.2, the total inductance has to be $1.1\,mH$. For this reason, a $1\,mH$ inductor has been designed and built.
The high frequency voltage ripple across the inductor terminals is very low. In addition, the inductor does not have to necessarily provide a filtering effect. An inductor designed

Inductance (L_2)	1	mH
Nominal RMS current ($I_{L_2,rms}$)	32	A_{rms}
Maximum peak current ($\hat{I}_{L_2}$)	54	A
AC voltage rating ($V_{AC,L_2,rms}$)	265	V_{rms}
Maximum voltage rating ($\hat{V}_{L_2}$)	375	V

Table 3.10: Output side inductor (L_2) requirements.

for a low frequency operation (i.e. 0-2 kHz) has been developed.

The requirements of the L_2 inductor are listed in Table 3.10.

For the low performances required by the inductor, a grain oriented steel has been selected for the application. The material can reach a higher induction before starting to saturate. The saturation point can be assumed at $B_{sat} = 1.5\,T$. Figure 3.22 shows the permeability data of the material.

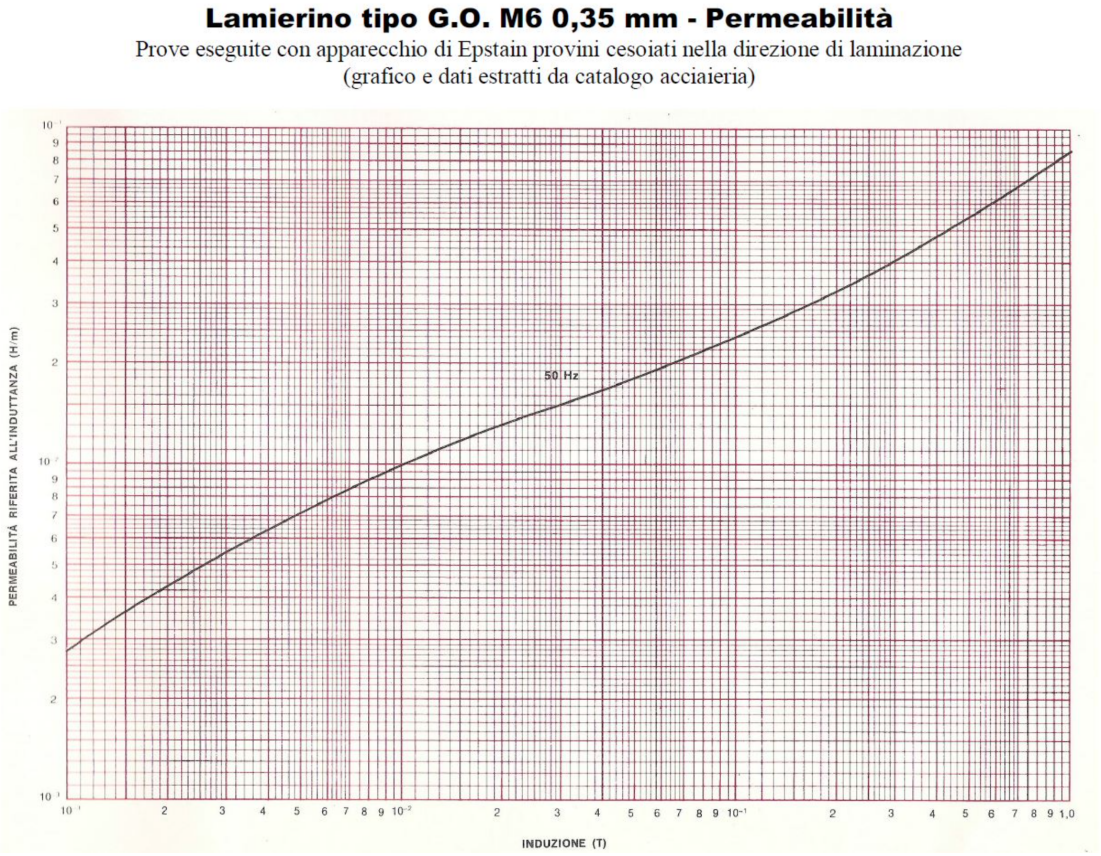

Figure 3.22: Sheet permeability data.

The current density was assumed equal to the previous case. A little higher fill factor

($k_u = 0.3$) has been assumed for the use of a standard copper wire. To sum up, the Table 3.11 contains the design parameters for the sizing.

$\hat{B}_{L_2}$	1.5	T
$J_{L_2,rms}$	4	A/mm^2
$k_{u,\,L_2}$	0.3	
ΔT_{L_2}	90	$°C$
ρ_w	$1.68 \cdot 10^{-8}$	$\frac{\Omega}{m}$
μ_0	$4\pi \cdot 10^{-8}$	$\frac{H}{m}$

Table 3.11: Inductor design data.

The area product is:

$$A_p = \frac{L_2 \cdot \hat{I}_{L_2} \cdot I_{L_2,rms}}{k_{u,\,L_2} \cdot J_{L_2,rms} \cdot \hat{B}_{L_2}} = 80.54\,cm^4 \tag{3.51}$$

The chosen sheet is an "EI" composition. Its dimensions are represented in Figure 3.23. The core volume can be adjustable depending on the amount of steel sheets and on the

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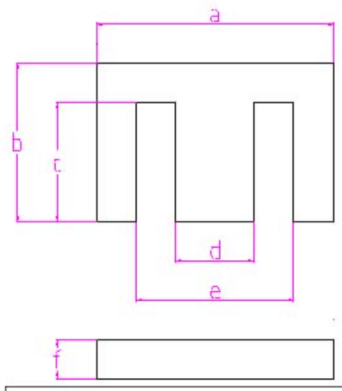


Tolleranze dimensionali in accordo con le raccomandazioni ISO R 286

TIPO	a	b	c	d	e	f	fori	g/10mm (7,65g/cm3)
EI 25	25,70	16,10	12,85	6,50	19,50	3,25	0,00	31,65
EI 30	30,00	20,00	15,00	10,00	20,00	5,00	0,00	45,90
EI 33	33,00	22,00	17,00	10,00	23,00	5,00	0,00	55,54
EI 38	38,40	25,60	19,20	12,80	25,60	6,40	0,00	75,20
EI 40	40,00	27,00	20,00	13,00	27,00	7,00	0,00	82,62
EI 42	42,00	28,00	21,00	14,00	28,00	7,00	3,50	89,96
EI 44	44,00	29,50	22,00	14,00	29,00	7,50	0,00	99,30
EI 48	48,00	32,00	24,00	16,00	32,00	8,00	3,50	117,50
EI 54	54,00	36,00	27,00	18,00	36,00	9,00	3,50	148,72
EI 57	57,00	38,00	28,50	19,00	38,00	9,50	0,00	165,70
EI 60	60,00	40,00	30,00	20,00	40,00	10,00	3,50	183,60
EI 66	66,00	44,00	33,00	22,00	44,00	11,00	4,50	222,16
EI 68	68,00	46,00	34,00	22,00	46,00	12,00	4,50	239,29
EI 75	75,00	50,00	37,50	25,00	50,00	12,50	4,50	286,88
EI 84	84,00	56,00	42,00	28,00	56,00	14,00	6,00	359,86
EI 96	96,00	64,00	48,00	32,00	64,00	16,00	6,00	470,02
EI120	120,00	80,00	60,00	40,00	80,00	20,00	7,00	734,40

Figure 3.23: Sheet dimensions and weight.

coil former dimensions. Thus, an iterative process to estimate the amount of iron has been formulated. A minimum air gap has been established to avoid an excessive concentration of magnetic energy in the iron. The consequence of an excessively tiny gap could be the large inductance variation with the current fundamental. The iterative process stops when the constraints listed in Table 3.12 are verified. The iteration process goal was to identify the configuration with the lowest iron quantity.

$A_w < W_a \cdot k_{u,\,L_2}$
$\hat{B} < \hat{B}_{L_2}$
$P_{DC} + P_{fe} < P_{loss}^{max}$

Table 3.12: Constraints for the output inductor to be satisfied during the iteration process

The DC losses limit and the maximum induction verification has been performed in the same way as for the inductor L_1. The same copper wire in the same configuration (a parallel of two wires of diameter $d = 2.24\,mm$ has been used).
The iron losses can be calculated by referring to the Figure 3.24, representing the losses in W/kg for the working frequencies of both 50 and 60 Hz. The iteration process results were:

- $V_c = 572000\,mm^3$;
- $A_p = 288\,cm^4$;
- $P_{loss}^{max} = 21\,W$;
- $N = 22$;
- $P_{DC} = 15.1\,W$;
- $P_{fe} = 6.2\,W$;
- $l_g\,(Gap\,length) = 1.6\,mm$;

The DC losses reach a maximum of:

$$P_{DC} = 15.1\,W \tag{3.52}$$

neglecting the high frequency contribute. NOMEX sheets have been used to create the gap.
An experimental verification of the inductance is provided in chapter 5.

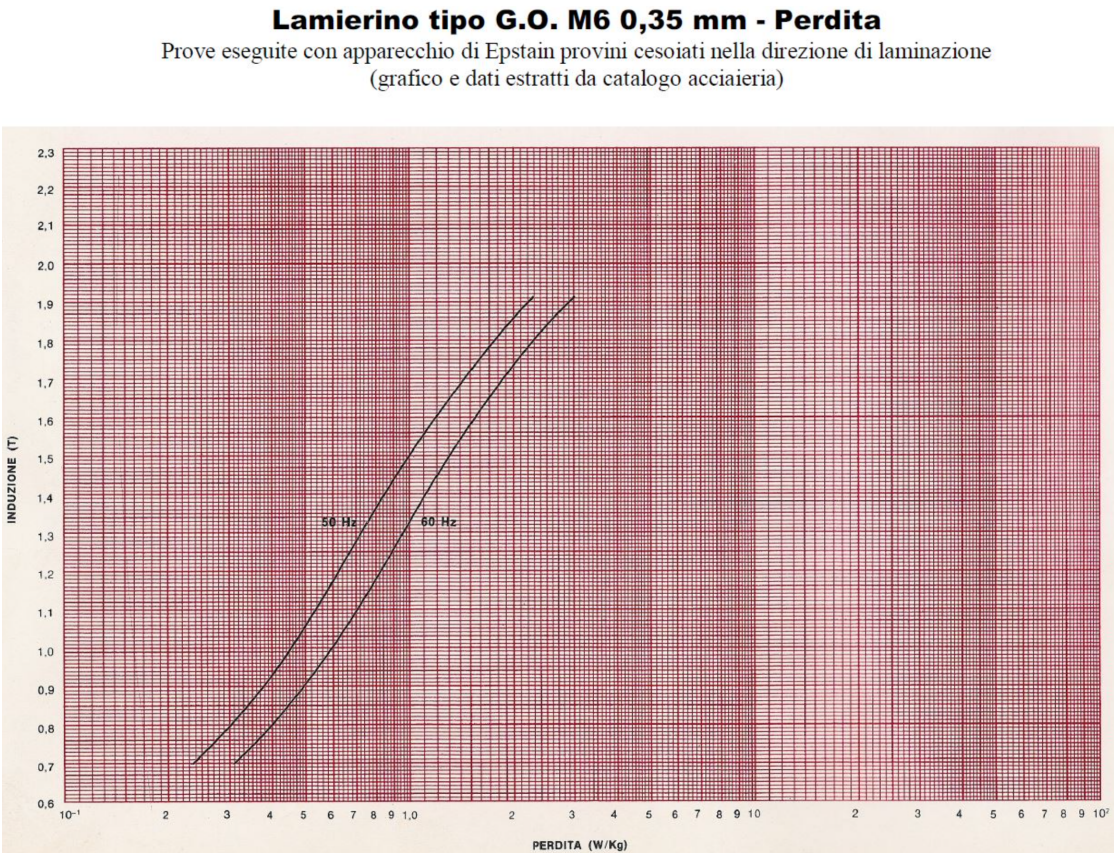


Figure 3.24: Iron losses per induction for a kg of material.

Chapter 4

Control design

The grid emulator control is a key aspect of the converter dimensioning. The typical control methods are illustrated in Chapter 1. The following control schemes can be identified for the grid emulator:

- open-loop control;
- closed-loop control with inner current loop and outer voltage loop;
- closed-loop control with the only voltage loop.

4.1 Control schemes comparison

A comparison among the control schemes should be performed on the basis of the performances and the capability to satisfy the requirements. The basic requirements taken into account are (see Chapter 2):

- (1.a): Nominal working operation;
- (1.c): Nominal frequency operation;
- (1.d): Response to a reference power step.

Other more advanced requirements include:

- (1.b): Undervoltage and overvoltage operations;
- (2.a): Compliance with the THD limit.

However, specific types of controls are excluded in advance. For the purpose of the work, the closed loop control with inner control loop has not been considered for the hereafter reasons:

- The current is dependent on the load: the OBC under test has already a current control loop;

- A unique voltage loop can achieve higher bandwidth.

The current can be limited by the usage of current protection to stop the PWM modulation.
The considerations reported in Chapter 1 suggest that the PI control not used in SyncRF should be excluded due to the impossibility of tracking a zero steady-state error. The previous conditions occur in the case of single-phase operation. A Proportional Resonant control is usually used for the single-phase functioning. Despite this, a simple open-loop control may represent a valid alternative thanks to its simplicity. Similarly, the control loop does not require a current control. The Repetitive Control has not been taken into account because of its complexity.
The block scheme related to each control is depicted in Figure 4.1.

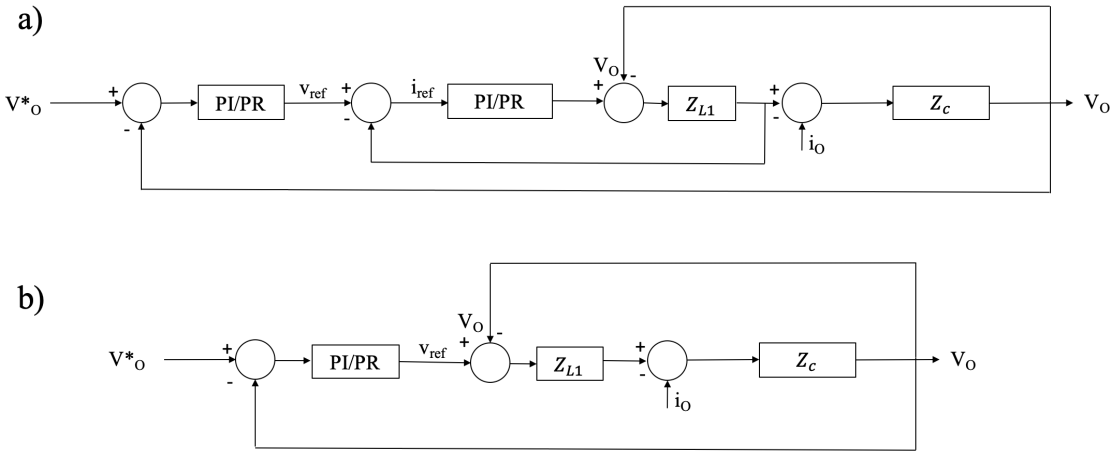


Figure 4.1: Control diagrams for a) inner current loop and outer voltage loop and b) single voltage loop. The controllers can be either PI or PR controllers.

The voltage is controlled on the impedance Z_c, i.e. the parallel between C and the series of C_d and R_d. It is equivalent to Z_2 cited in Chapter 3. Z_{L_1} is the impedance of the converter side inductor L_1 and i_o is the current requested by the load. The analyzed diagrams are simplifications of a more complex system, in which the CUT is presented in a less simplified way. They are useful for the tuning of each controller.
Other simplifications are represented by the actuator delays and sampling process. These are both effects due to the sampling period T_s necessary for the digital processing. Delay sources are:

- Interrupt service routine (ISR) operation at the interrupt frequency and consequent sampling period delay. The representation of such phenomenon is described by the transfer function in equation (4.1).

$$G_d = e^{-s \cdot T_s}; \tag{4.1}$$

- PWM actuation which causes a zero-order hold effect. The issue can be implemented

with equation (4.2).

$$G_{PWM} = \frac{1 - e^{-s \cdot T_{sw}}}{s \cdot T_{sw}} \tag{4.2}$$

- The oversampling and averaging operation, representable by a similar transfer function (equation (4.3)) [1].

$$G_s = \frac{1 - e^{-s \cdot T_s}}{s \cdot T_s} \tag{4.3}$$

The sampling frequency is often the same as the switching frequency. The open-loop control is the simplest control implementable. Its block diagram is represented in Figure 4.2.

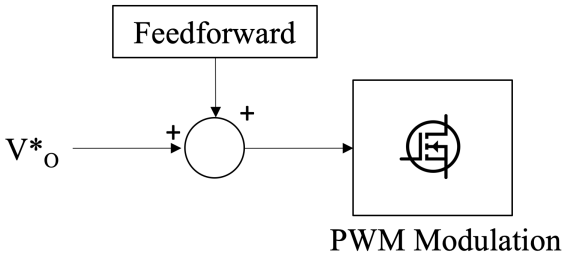


Figure 4.2: Open-loop diagram adopted for the first prototype for the grid emulator. The "Feedforward" block represents eventual feedforward components.

4.2 Control parameters definition

The switching frequency is very high in the application under study. As a result, it is necessary to apply a lower sampling frequency which has to be an integer dividend of the switching frequency. The selected sampling frequency is thus:

$$f_s = f_{sw}/2 = 50\,kHz \tag{4.4}$$

The maximum bandwidth of the closed-loop control cannot be too close to the sampling frequency. It has been limited to 1/20 of the interrupt frequency. Therefore:

$$f_{bw,\,max} = f_s/20 = 2.5\,kHz \tag{4.5}$$

Consequently, the sampling period is defined as:

$$T_s = 1/f_s = 20\,ms \tag{4.6}$$

4.3 Test under exam

The simulation circuit is represented in Figure 2.4. The delays presented before have been inserted as discrete delays (for the actuator) and sample and hold delays (for the acquisition). The PWM delay is inherent in the carrier compare. The Figure 2.4 shows the simulation circuit under discussion. The voltage is measured at the output of the grid emulator, as well as the current.
The filter of the Power Factor Corrector (PFC) stage of the OBC is implemented, while the PWM rectifier is simulated with a current generator, to emulate the load request. This choice was made to evaluate the effect of the resonance effects occurring between the grid impedance and the filter capacitors of the PFC.

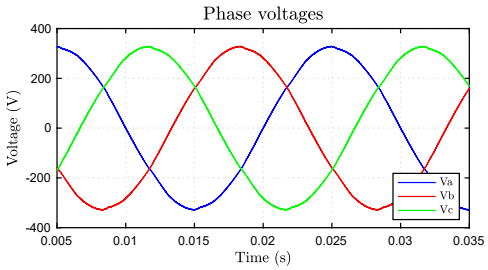
For emulating the load response, load ramps have been implemented from low load to full load conditions. The ramp steepness has been defined so that the full power requested by the CUT occurs in an electric period, thus 20 ms. The load current is first varied between zero and 10% of the nominal current, and then it is varied between zero and 100%. The THD is measured for each type of control. In Table 4.1 the test to be performed along with the requirement for the control assessment are listed (see Tables 2.3, 2.4).

Test	**Requirement**
No-load operation	Maximum of 2% of voltage displacement with respect to the reference value
Load operation	Maximum of 10% of voltage displacement with respect to the reference value
THD measurement	THD<5%
Undervoltage and overvoltage operation	Maximum of 10% voltage displacement with respect to the reference value
Operation in a frequency range of 45 to 65 Hz	Maximum deviation of 5% with respect to the reference value.

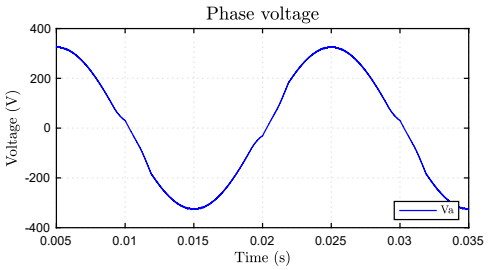
Table 4.1: Control tests for the grid emulator.

4.4 Open-loop control

As stated in chapter 1, the open-loop control may be a simple and straightforward method to control a grid emulator. In the three-phase system as well as in the single-phase system, the no-load response is already represented in Chapter 3. It is reported anyway in Figure 4.3.



Three-phase load no-load operation.



Single-phase no-load operation

Figure 4.3: No-load response of the open-loop control. The peak voltage is 325 V.

10% load ramp tests

The 10% load ramp results for three-phase operation are plotted in Figure 4.4. The reference voltages are marked as "Vxr", where x stands for a, b or c.

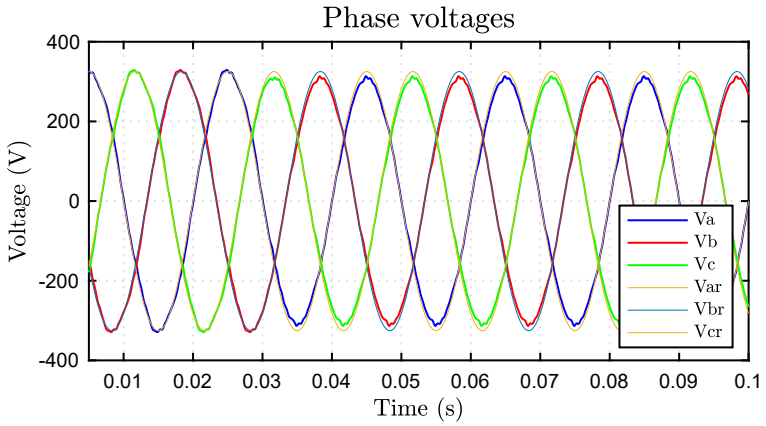


Figure 4.4: Three-phase voltages for a load ramp of 10% arising in $t = 0.03\,s$.

A slight reduction in voltage is visible when the load demand begins to rise. The peak voltage reduction is equal to $\Delta V_{o,load} = 15\,V$, thus the 4.6% of the nominal voltage.
The no-load THD is equal to 2.22%, which decreases to 1.51% under 10% load. The currents appear as in Figure 4.6, and present distortion issues. The significant oscillating effect (even when the current request is zero) is caused by resonance effects between the CUT's filter capacitor and the grid emulator impedance.

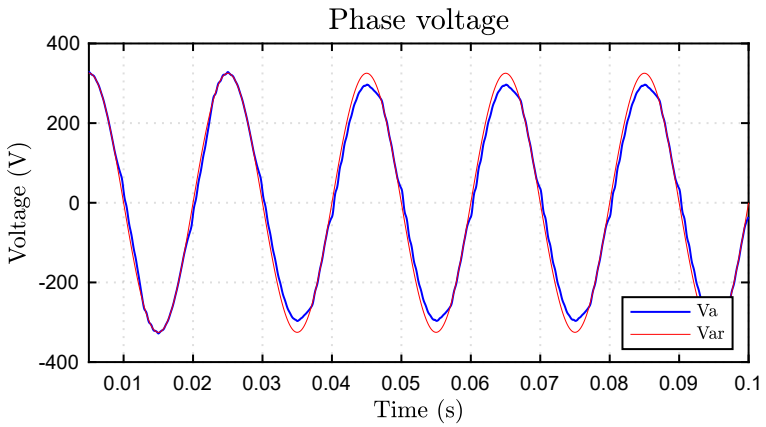
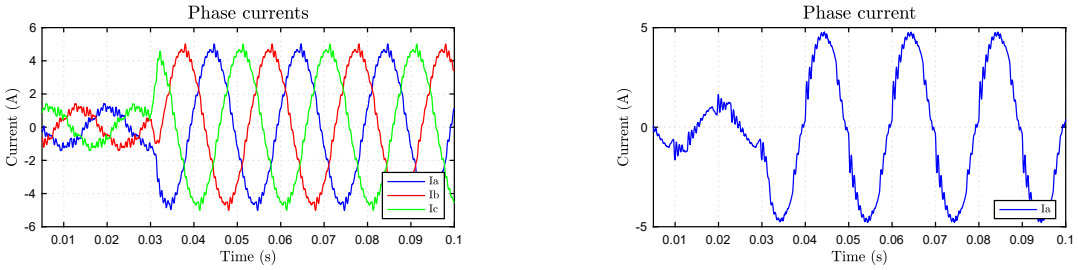


Figure 4.5: Single-phase voltage for a load ramp of 10% arising in $t = 0.03\,s$.



Three-phase currents. Single-phase current.

Figure 4.6: Currents of the three-phase and single-phase systems when a 10% load is requested.

The single-phase loading presents comparable results illustrated in Figure 4.5. The currents are characterized by a similar effect with respect to the three-phase system. A voltage drop of 8.7% is evident. The single-phase THD is worse with respect to the three-phase system one. The no-load condition is characterized by a THD of 4.3%, decreasing at 2.6% in load conditions.

100% load ramp tests

The same tests has been repeated for the 100% load. The results are depicted in Figures 4.7, 4.9, and 4.8.

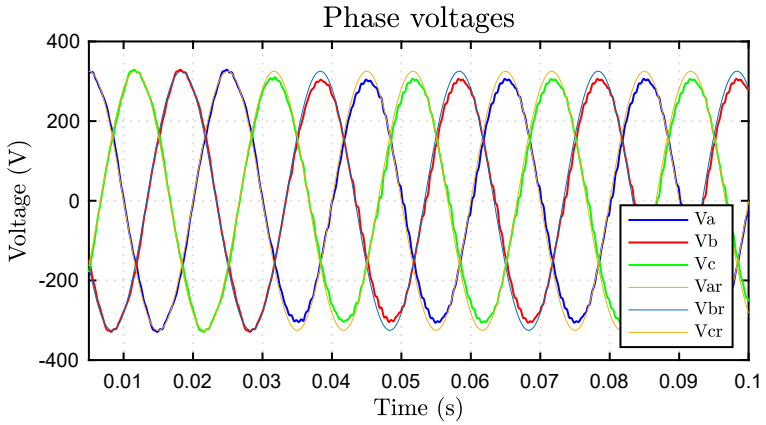


Figure 4.7: Three-phase voltages for a load ramp of 100% arising in $t = 0.03\,s$.

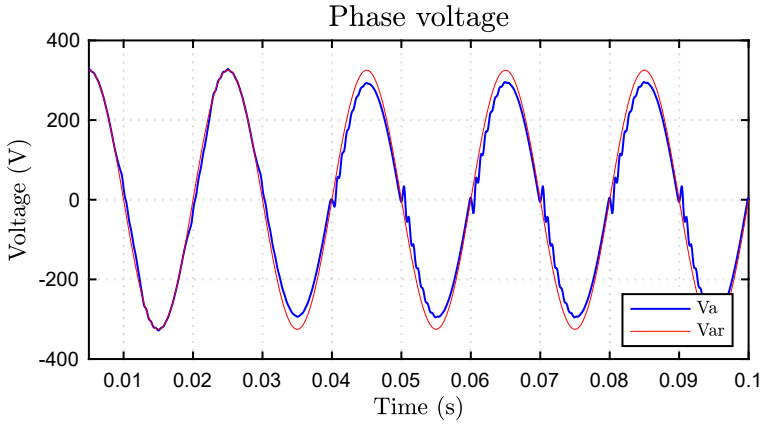
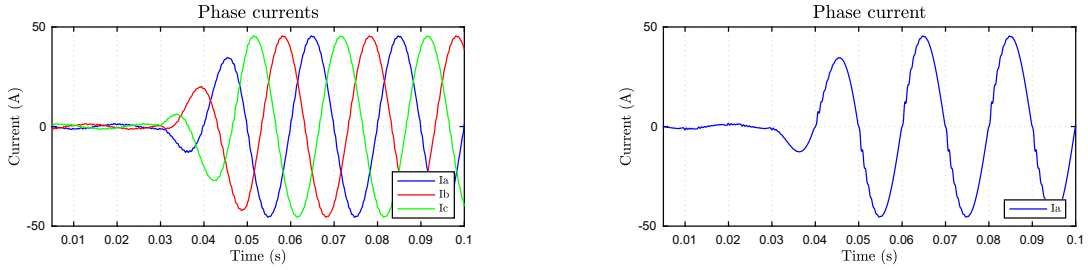


Figure 4.8: Single-phase voltage for a load ramp of 100% arising in $t = 0.03\,s$.



Three-phase currents. Single-phase current.

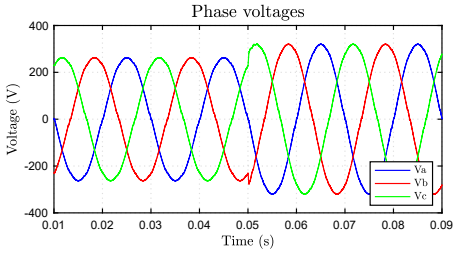
Figure 4.9: Currents of the three-phase and single-phase systems when a 100% load is requested.

The THD in load conditions is reduced to 1.98% in case of three-phase simulation. On

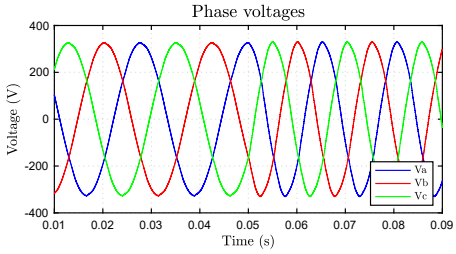
the contrary, the THD during single-phase operation reaches its worst value since it arrives at 7.56% during full load. Such a high distortion is beyond the THD limit defined, and it is due to the dead time distortion amplified by the resonance between the CUT filter and the grid impedance. Thus, it violates the requirement of THD<5%. As a consequence, single-phase tests might be performed only at low load. The maximum voltage displacement with respect of the nominal value corresponds to 9.5%. The currents appear less distorted.

Undervoltage/overvoltage and underfrequency/overfrequency operations.

To end with, a test in different voltage and frequency conditions has been made in no-load conditions. Figure 4.10 demonstrate the grid emulator's accurate behaviour under undervoltage and overvoltage conditions as well as when the frequency is changed from 45 Hz to 65 Hz.



Three-phase simulation where the voltage is varied from 200 V_{rms} to 240 V_{rms} without any significant error.



Three-phase simulation where the frequency is varied between 45 Hz and 65 Hz without any significant error.

Figure 4.10: Simulation of the grid emulator functioning under different voltage and frequency conditions.

Conclusions

The open-loop control can represent an alternative to emulate a poor grid. Even though the THD is very high in certain conditions, it can be implemented for simple low load tests. Because of the higher load request, the control is not capable of maintaining a constant output voltage over the loading. The maximum displacement with respect to the nominal value is 10%. Anyway, the control is compliant with the requirements of nominal voltage.

4.5 Closed-loop control

A closed-loop control of the capacitor voltage is hereinafter proposed. The purpose of such control is to prevent the voltage from assuming too large or too low voltage values with respect to the nominal one. The voltage control diagram is figured in 4.1. For simplicity,

a PI controller has been tuned despite it is not capable of following a variable reference frame with zero steady-state error during single-phase operation. The use of SyncRF (dq transformations) when operating in a three-phase configuration has been made. The following proposed design is a demonstration of the closed-loop performances. It will be improved in the future with appropriate controls more suitable for the application (for instance, Proportional Resonant control for the single-phase operation).

Controller tuning

The tuning of the Kp and the Ki parameters has been performed through the tool *Sisotool* in MATLAB. The transfer functions were evaluated both at no-load and at full-load conditions. The latter was first emulated through a resistive load of value $R_{load} = 6.6\,\Omega$. The controller has been tuned referring to the transfer function (4.8) since it was of higher interest. The term G_{PI} represents the PI controller transfer function 1.1. The Figure 4.11 shows the single-phase equivalent circuit for the transfer function evaluation. Z_1 and Z_2 have the same meaning of what asserted in Chapter 3, while Z_3 represents the output inductance ((4.7)):

$$Z_3 = s \cdot L_2 + R_{L_2} \tag{4.7}$$

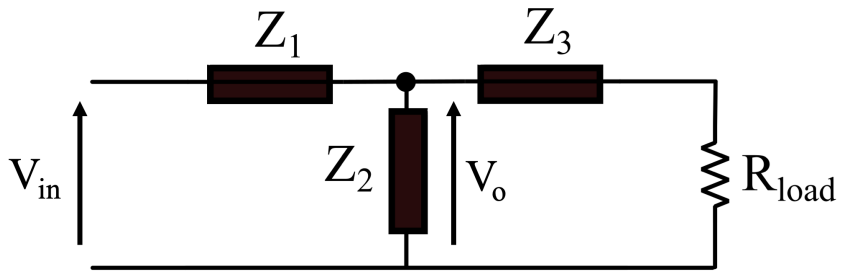


Figure 4.11: Single-phase equivalent circuit for PI controller tuning.

$$\frac{V_o}{V_{in}} = G_{PI} \cdot G_d \cdot \frac{\frac{Z_2 \cdot (Z_3 + R_{load})}{Z_2 + Z_3 + R_{load}}}{\frac{Z_2 \cdot (Z_3 + R_{load})}{Z_2 + Z_3 + R_{load}} + Z_1} \tag{4.8}$$

The integral and proportional gains were adjusted to achieve a proper bandwidth along with a phase margin of at least 45 degrees to ensure stability.

The closed-loop Bode diagram is represented in Figure 4.12. and the bandwidth is around 600 Hz.
The no-load responses are depicted in Figure 4.13, from which it is possible to measure the THD. Its value is, respectively, for the three-phase and the single-phase systems:

- $THD_{three-phase} = 0.72\%$;

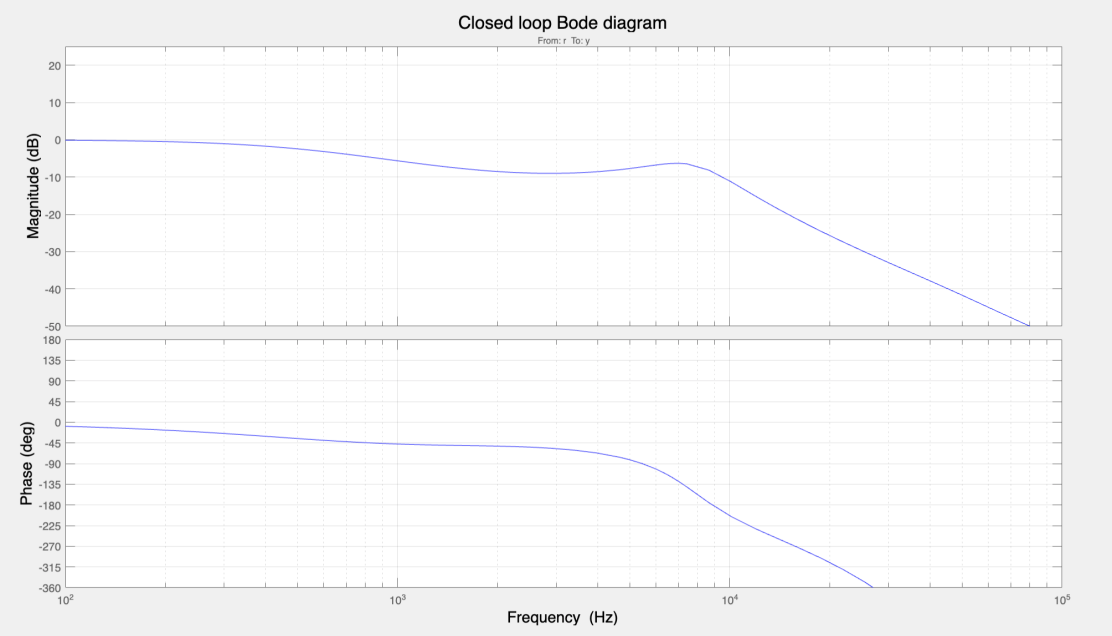
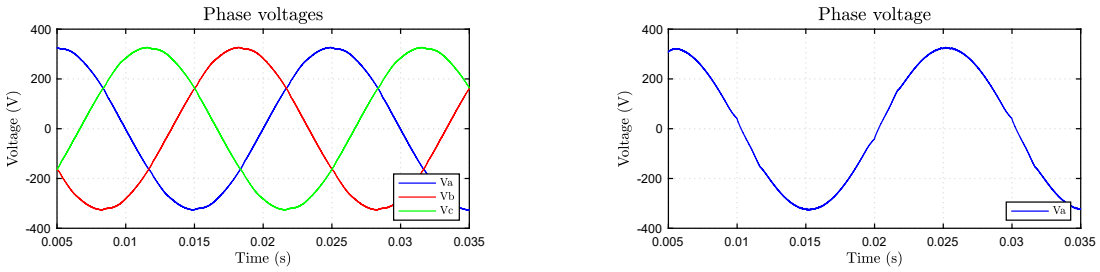


Figure 4.12: Closed-loop bode diagram for the transfer function (4.8).

- $THD_{one-phase} = 1.5\%$.



No-load three-phase simulation. No-load single-phase simulation.

Figure 4.13: No-load voltage responses for the three-phase and single-phase systems.

10% load ramp tests

The same tests executed for the open-loop control have been examined for the closed-loop voltage control. The response for a 10% load step are shown in Figures 4.14, 4.15 and 4.16.

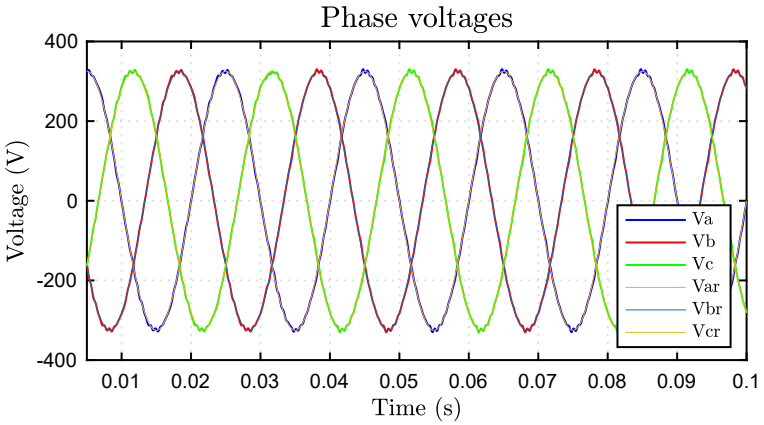


Figure 4.14: Three-phase voltages when a load ramp of 10% arises in $t = 0.03\,s$.

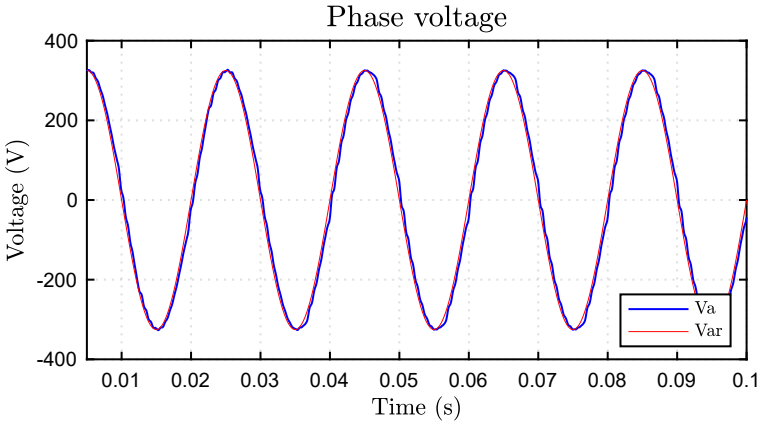
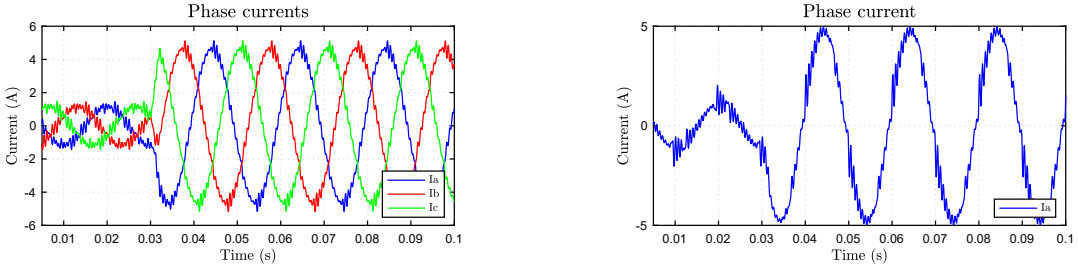


Figure 4.15: Single-phase voltage for a load ramp of 10% arising in $t = 0.03\,s$.



Three-phase currents. Single-phase current.

Figure 4.16: Currents for the three-phase and single-phase systems when a 10% load is requested.

The closed-loop voltage control maintains the peak voltage to 325 V throughout the

no-load operation whereas decreases to a minimum of 320 V when the load is 100 %. During the loaded operation, the three-phase THD reaches a maximum of 2.1 %. The maximum observed single-phase THD is 4.2 % under identical circumstances as before. The currents are affected by distortion as the open-loop case.

100% load ramp tests

Figures 4.17, 4.18 and 4.19 represent the waveforms related to the load reaching the 100% power request.

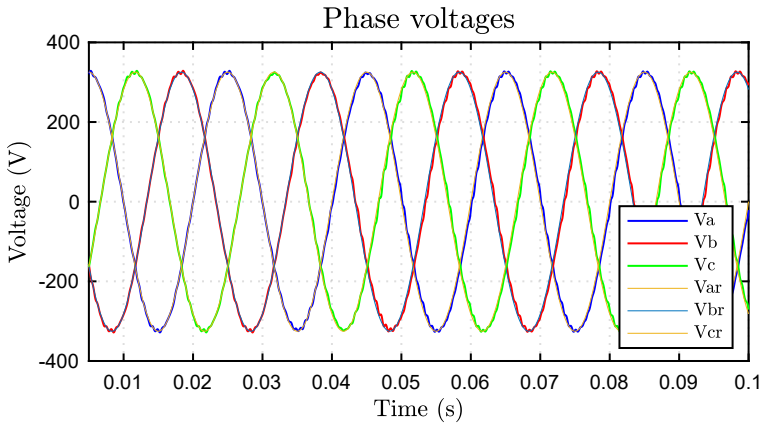


Figure 4.17: Three-phase voltages for a load ramp of 100% arising in $t = 0.03\,s$.

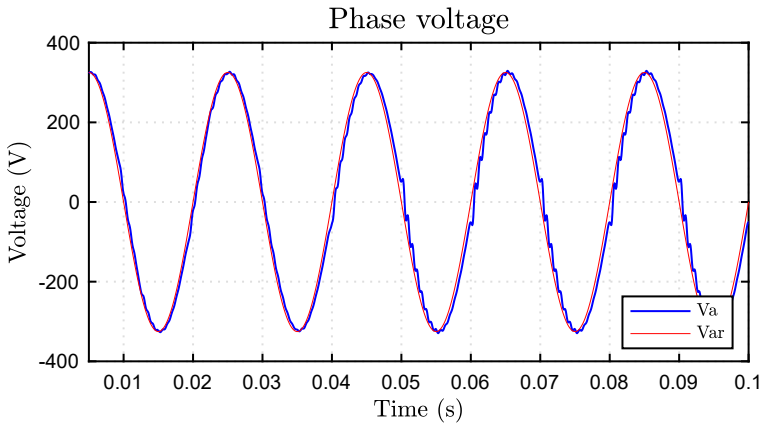
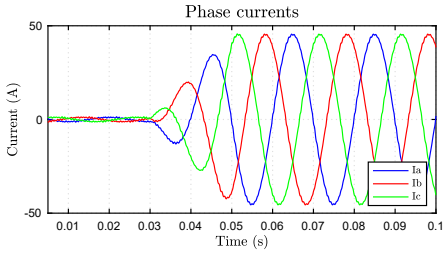
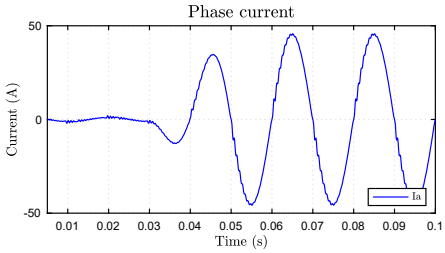


Figure 4.18: Single-phase voltage for a load ramp of 100% arising in $t = 0.03\,s$.



Three-phase currents.



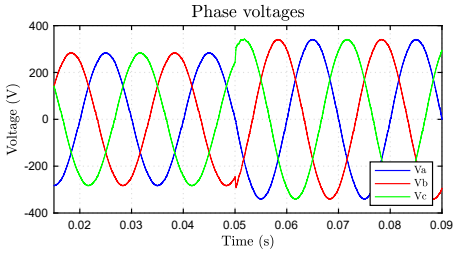
Single-phase current.

Figure 4.19: Currents for the three-phase and single-phase systems when a 100% load is requested.

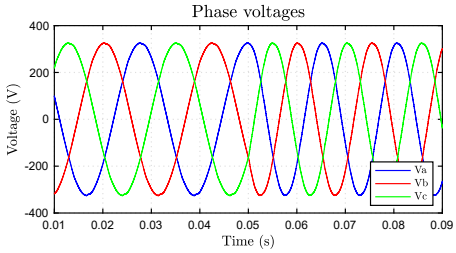
Unlike the open-loop control, the closed-loop control is capable of maintaining the voltage in correspondence of a value close to the nominal one. The THD is 1.6% during three-phase functioning and which is lower than the open-loop case due to the capability of attenuating the disturbances. The current distortions are reduced too.

Undervoltage/overvoltage and underfrequency/overfrequency operations.

The grid emulator's correct behaviour under voltage and frequency variations is shown in Figure 4.20 (no-load simulation).



Three-phase simulation where the voltage is varied between 200 V_{rms} to 240 V_{rms} without any significant error.



Three-phase simulation where the frequency is varied between 45 Hz and 65 Hz without any significant error.

Figure 4.20: Simulation of the grid emulator under different voltage and frequency conditions.

Conclusions

The control is capable of maintaining a constant voltage value of approximately 325 V. Harmonic injection issues are still present, which are even more evident during the full load simulations. Dead time distortion affects highly the THD, causing disturbances

amplified by resonance effects among the filter elements.
Table 4.2 summarizes the features of each examined control.

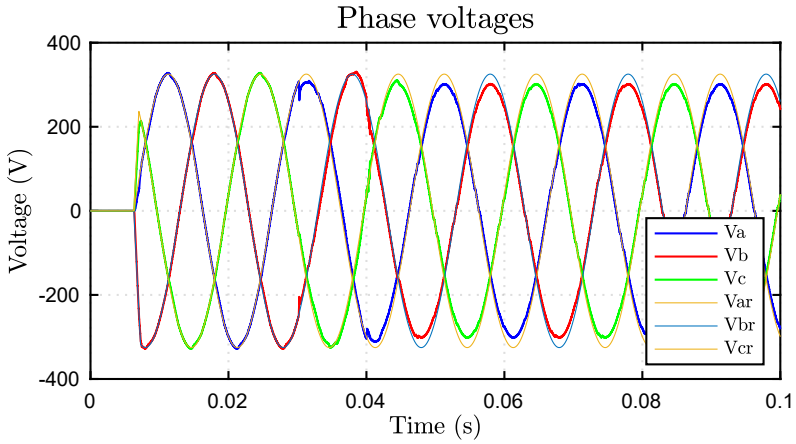
	Open-loop control	**Closed-loop voltage control**
Maximum no-load voltage displacement	$\approx 0\%$	0.3 %
Maximum load voltage displacement	9.5 %	1.5 %
Maximum THD	7.6 %	4.2 %

Table 4.2: Summary of each control's features.

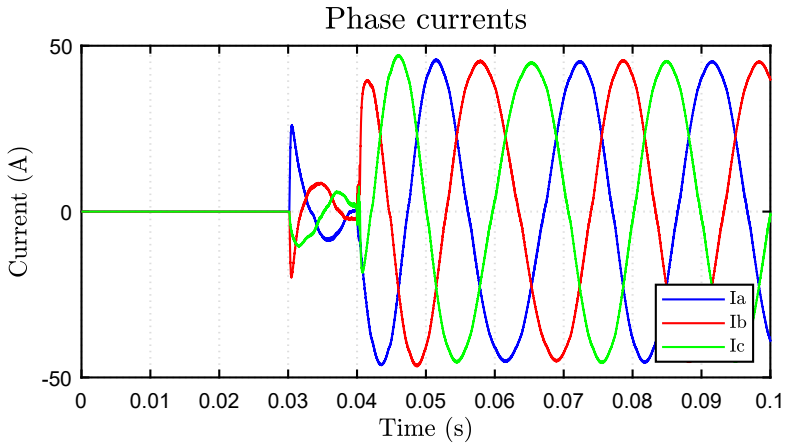
Given the simplicity of the open-loop control and its capability to satisfy the load an open-loop control of the voltage has been implemented for the experimental tests. Further tests will be executed in the future with more performing controls (e.g. closed-loop voltage control). The experimental part is focused on the validation of the filter element and the open-loop control.

4.6 Simulations including the Converter Under Test control

In order to analyze the response of the grid emulator when the converter under test is controlled properly, specific simulations have been run. The control include the DC-link precharge, the regulation of current and voltage through PI regulators, and the grid frequency acquisition through the PLL. Both three-phase and single-phase responses are analyzed with open-loop and closed-loop controls. The grid emulator control is implemented in form of C-code. The load, represented by the Power Factor Corrector (PFC) stage of the On-Board Charger, enables at $t = 0.03\,s$, and starts to absorb power at $t = 0.04\,s$. The current has been limited to 32 A_{rms}. For the following tests, the PFC filter was purely inductive. Hence, the voltage has been measure at the capacitors terminals. The current requested by the PFC was the maximum allowed. The power is assumed as positive (that is the grid emulator delivers power to the PFC) when the PFC current is negative (that is, the PFC absorbs power).
The three-phase open-loop control results are illustrated in Figure 4.21.



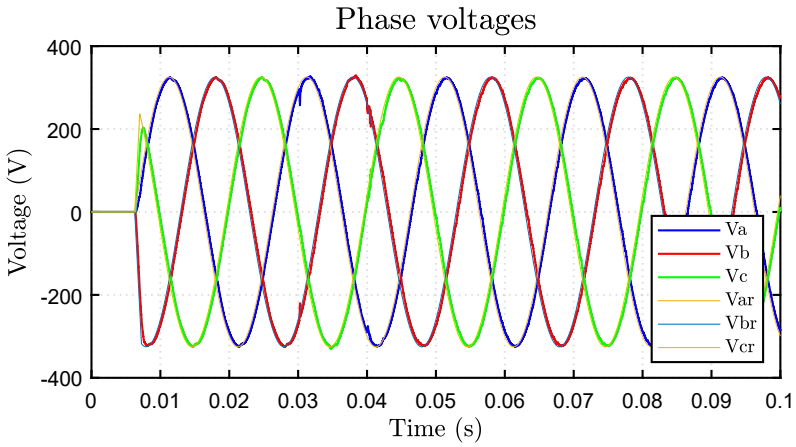
(a) Three-phase voltages of the grid emulator.



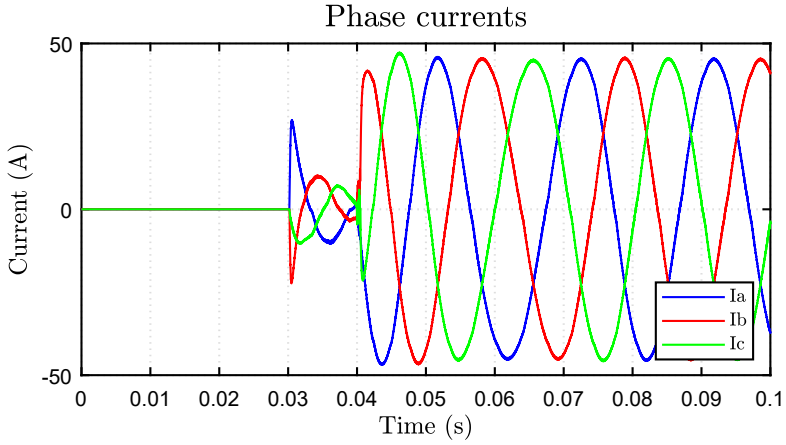
(b) Three-phase currents required by the PFC.

Figure 4.21: Voltage across the grid emulator's filter capacitors and required current by the PFC in open-loop conditions.

It is noticeable how the voltage drop is present and it is similar to the same voltage drop already observed in the simulations (Figure 4.7). Consequently, the power delivered to the PFC is reduced, since the current is limited to the nominal value of 32 A. The three-phase closed-loop control results are depicted in Figure 4.22.



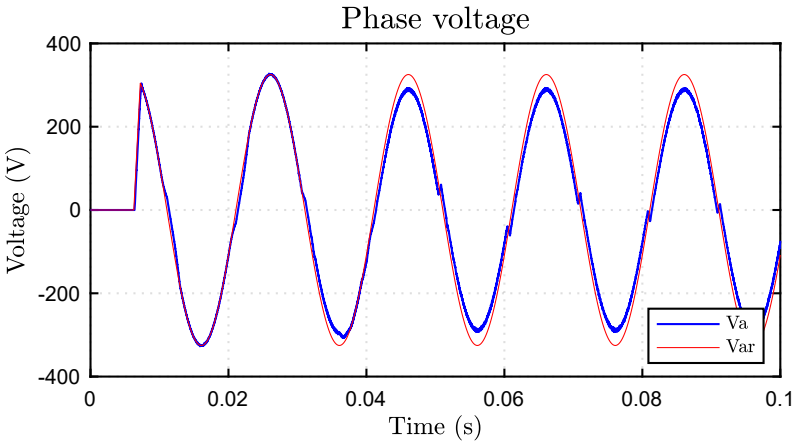
(a) Three-phase voltages of the grid emulator.



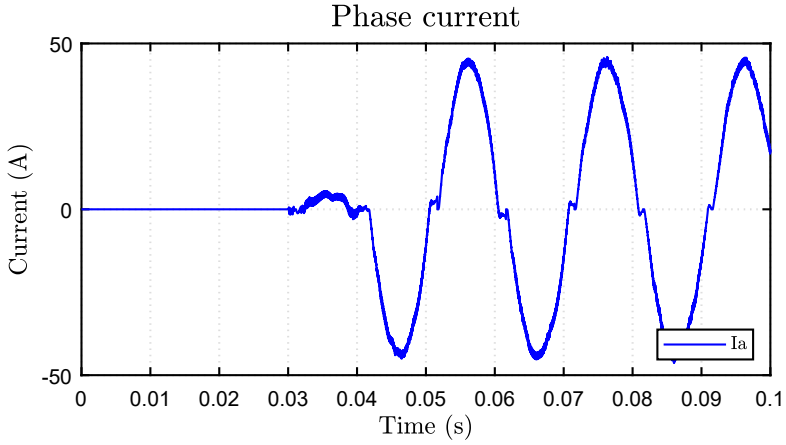
(b) Three-phase currents required by the PFC.

Figure 4.22: Voltage across the grid emulator's filter capacitors and required current by the PFC in closed-loop fashion.

When implementing a three-phase closed-loop control, the voltage is kept at its nominal value with a negligible deviation. Thus, it is possible for the grid emulator to deliver the full power required by the load.
The single-phase simulation results for the open-loop control are shown in Figure 4.23.



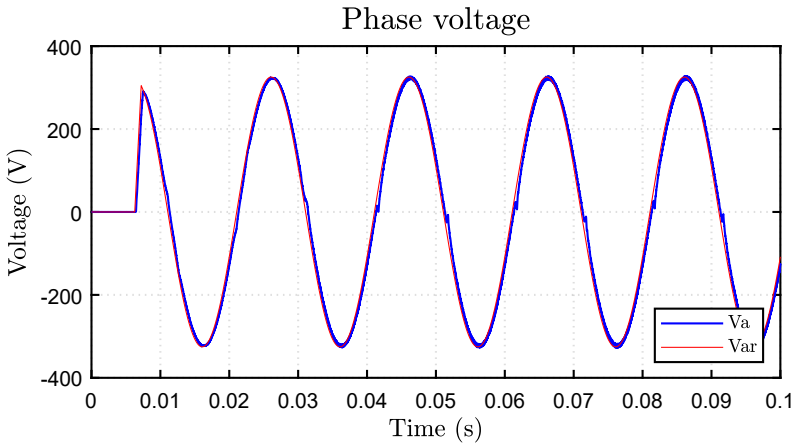
(a) Single-phase voltage of the grid emulator.



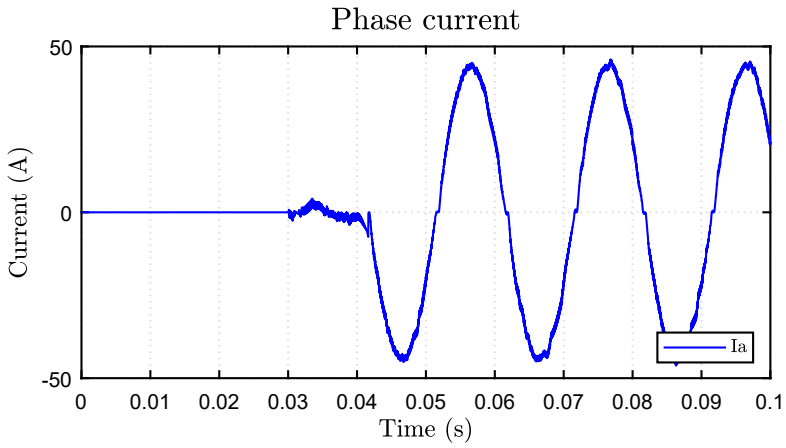
(b) Single-phase current required by the PFC.

Figure 4.23: Voltage across the grid emulator's filter capacitor and required current by the PFC in open-loop conditions.

As for the three-phase simulation, the single-phase open-loop control cannot completely deliver power to the load. The harmonics injected are instead reduced with respect to the simulations result of Figure 4.8. The power is reduced by 20% from the maximum.
The closed-loop single-phase simulation is represented in Figure 4.24.



(a) Single-phase voltage of the grid emulator.



(b) Single-phase current required by the PFC.

Figure 4.24: Voltage across the grid emulator's filter capacitor and required current by the PFC in closed-loop conditions.

The single-phase closed-loop control system allows to better control the voltage and supply the load without power limitations. What's more, both the voltage and the current waveforms appear as less distorted, thus the THD is reduced.

Conclusions

It is to be noted how the sudden load request does not cause voltage spikes or voltage deviations higher than the 20% from the nominal value under any circumstances and complying with the requirement (1.d). The open-loop control is suitable for working operation up to the 80% of the nominal power and it is affected by voltage deviations. The LCL filter is not critically affected by the switching operation of the PFC and can work properly. Finally, the THD is reduced when closed-loop fashion is realized, and the power is entirely delivered to the PFC since voltage drops do not occur.

Chapter 5

Experimental tests

The experimental tests could not be carried out on the whole system because the component to be tested had not been prepared yet. Thus, the objective of the experimental testing was to validate the grid emulator's filter and open-loop control. In particular, the following tests have been performed:

- measurement of the peak-to-peak voltage ripple at the terminals of the filter capacitor;
- measurement of the peak voltage of the fundamental voltage in compliance with requirement (1.a) for both no-load and load operations;
- frequency measurement in compliance with requirement (1.c);

5.1 Experimental setup

At the time of the work, the inverter designed to generate a PWM waveform at a frequency of 100 kHz was not ready yet. A different inverter was used with a different switching frequency. Specifically, the company's STDRIVE inverter was used (Figure 5.1). The selected switching frequency was $f_{sw} = 20\,kHz$ and a dead time of $t_d = 1\,\mu s$ was chosen. A voltage sensor (Pico TA057) was employed to visualize the voltage waveforms on the oscilloscopes. The oscilloscopes were:

- Teledyne Lecroy WaveSurfer 3024;
- Rohde & Schwarz RTB2004;

The impedance meter Keysight U1733C was used to check the component's inductance. The current sensor was the FLUKE i3000s. The inverter's DC-link has been connected to the power supply PSB 9750-60 or PSB 9060-360 depending on the test. Voltage probes TESTEC TT - SI 9110 and PICO TA057 have been used.

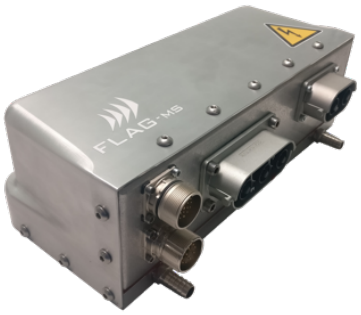


Figure 5.1: Inverter used for the experimental tests.

5.2 Inductors validation

The inductors needed a direct or indirect measurement to verify the inductance value. For the converter side inductor L_1, a direct measure with the impedance meter Keysight U1733C was made. Due to the low permeability of the grain-oriented steel in the meter's operating range, which led to an inaccurate inductance measurement, this was not achievable for the output side inductor L_2. Thus, a voltage impulse test has been carried out to identify the L_2 inductance and the saturation current of each inductor. The power supply was, in this case, the PSB 9060-360.

Converter-side inductor L_1 test

The converter-side inductor L_1 has been first verified through the impedance meter Keysight U1733C. The final inductance value is slightly variable among the inductors and all the values fall in the interval between 105 μH and 112 μH. Figure 5.2 shows the inductor realized for the testbench.

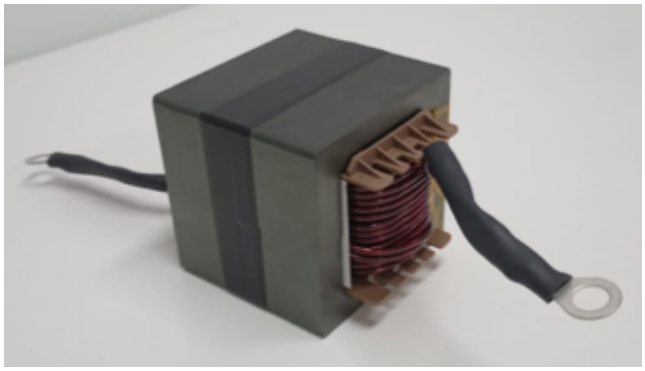


Figure 5.2: Inductor L_1.

In addition, the $L_1 = 112\,uH$ inductor has been tested through an impulse test. A voltage impulse of circa 46 V has been provided to the inductor terminals for a time of $\Delta t = 283\,\mu s$ and the current was acquired. Figure 5.3 shows the acquisition of the signals with the oscilloscope Rohde Schwarz RTB2004. Indications about the impulse duration, current trace, voltage trace and saturation point have been added.

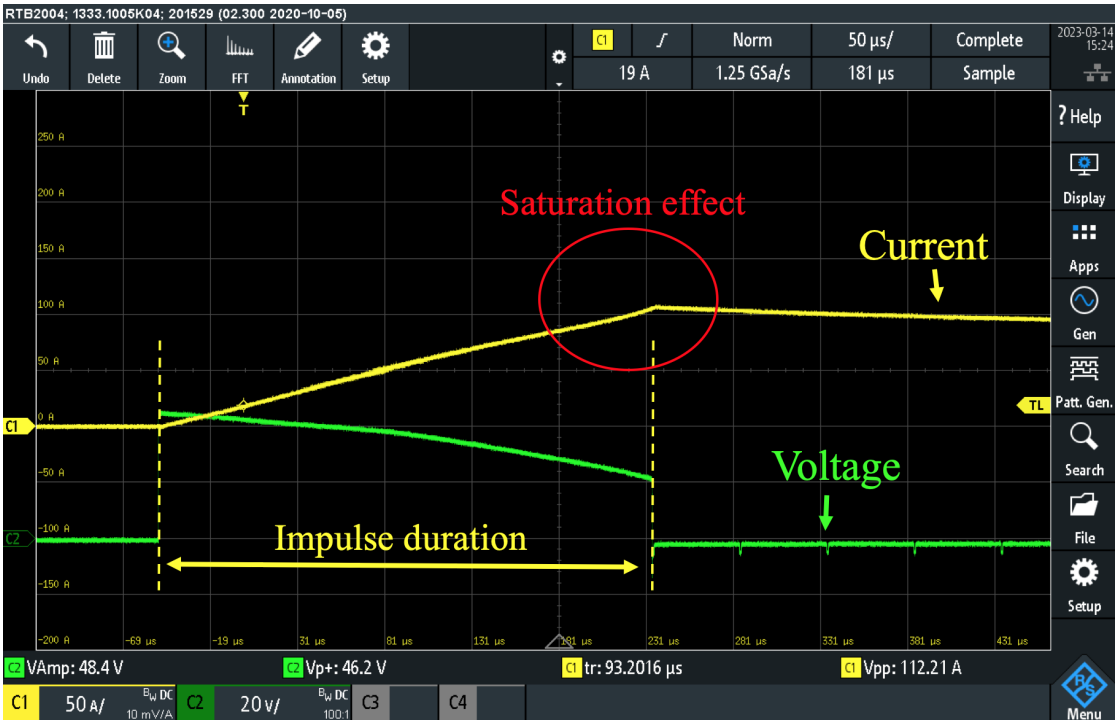


Figure 5.3: Oscilloscope screenshot of the impulse. The markers on the right (C1 and C2) indicate the zero of each signal.

The voltage is not constant due to the energy transfer from the DC-link to the system under test. From the data elaboration, it was noticed that the inductance starts decreasing from 80 A and from 100 A. The saturation effect is slightly visible. The test was carried out at 25 $°C$, thus the saturation current is higher than in the case of high temperature (for instance, 100 $°C$).

Output inductor L_2 test

As the inductor L_1, the inductor $L_2 = 1\,mH$ was tested through an impulse test. The goal was to estimate the inductance too. An impulse of 200 V was imposed at the terminals of the inductor for a limited time of 500 μs. Figure 5.4 is a screenshot of the impulse registered by the oscilloscope Teledyne Lecroy WaveSurfer 3024. Information about the impulse duration, current trace, voltage trace and interval of interest have been inserted. The interval of interest for the inductance calculation was the linear trend of

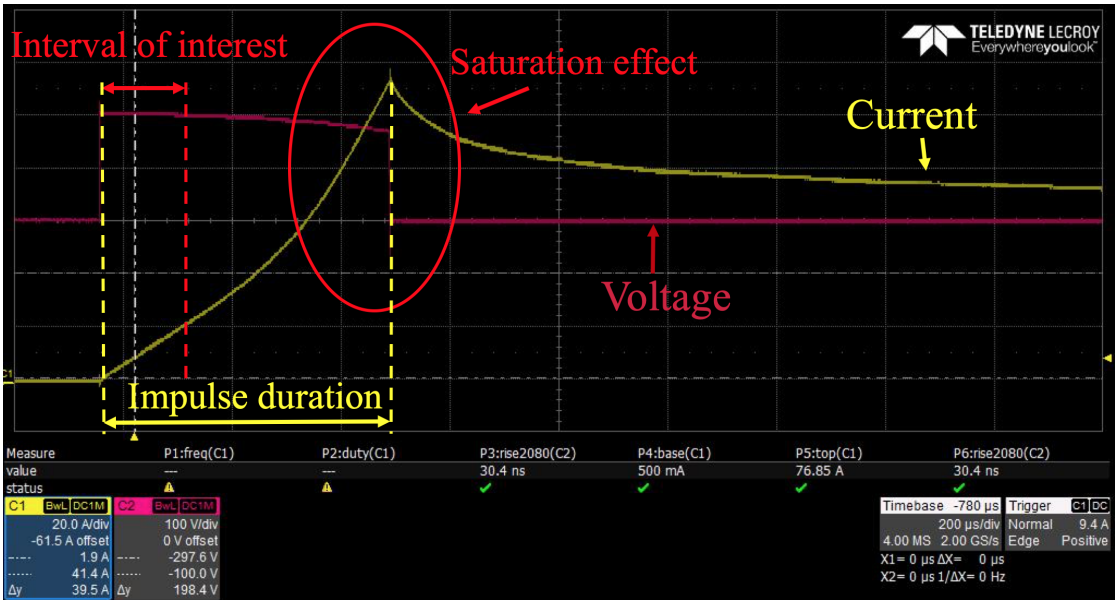


Figure 5.4: Oscilloscope screenshot of the impulse. The voltage scale zero corresponds to the oscilloscope zero, while the current y-axes is translated three divisions down for sake of clarity.

current at the beginning of the impulse. The voltage was reasonably constant during this interval. The saturation of the inductor starts from $I_{sat} = 60\,A$ upwards, as expected from the design process. The inductance is calculated by solving Equation (5.1), valid only for linear trends of current and constant voltage.

$$V = L \cdot \frac{\Delta i}{\Delta t} \tag{5.1}$$

The inductor is shown in Figure 5.5.

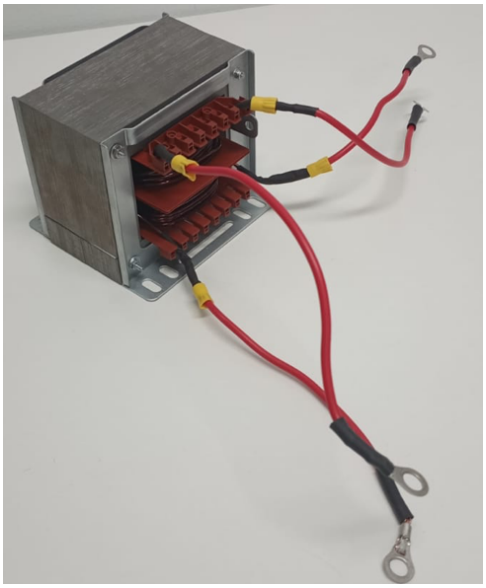


Figure 5.5: L_2 inductor.

5.3 Filtering effect test

The filter performance has been tested through a no-load test. In particular, the test inverter provided a sinusoidal voltage at the nominal frequency of 50 Hz for five fundamental periods. The test has been made for the single-phase system. For precautionary reasons, the DC-link voltage was set to $V_{DC} = 380\,V$ The results are plotted in Figure 5.6, where the acquisition signal (yellow) and the filtered acquisition signal (blue) are figured. Figure 5.6 reflects the simulated trend of no-load conditions depicted in Figure 5.7. The simulation has been performed under the same conditions as the test in terms of DC-link voltage, switching frequency, and dead time.

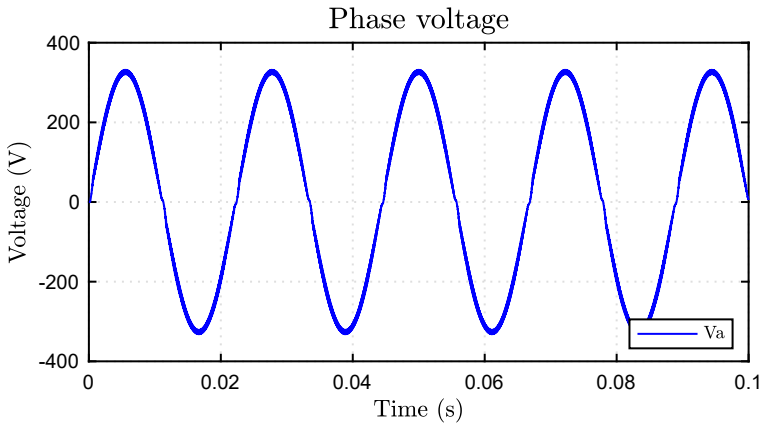


Figure 5.7: Single-phase no-load simulation at $f_{sw} = 20\,kHz$.

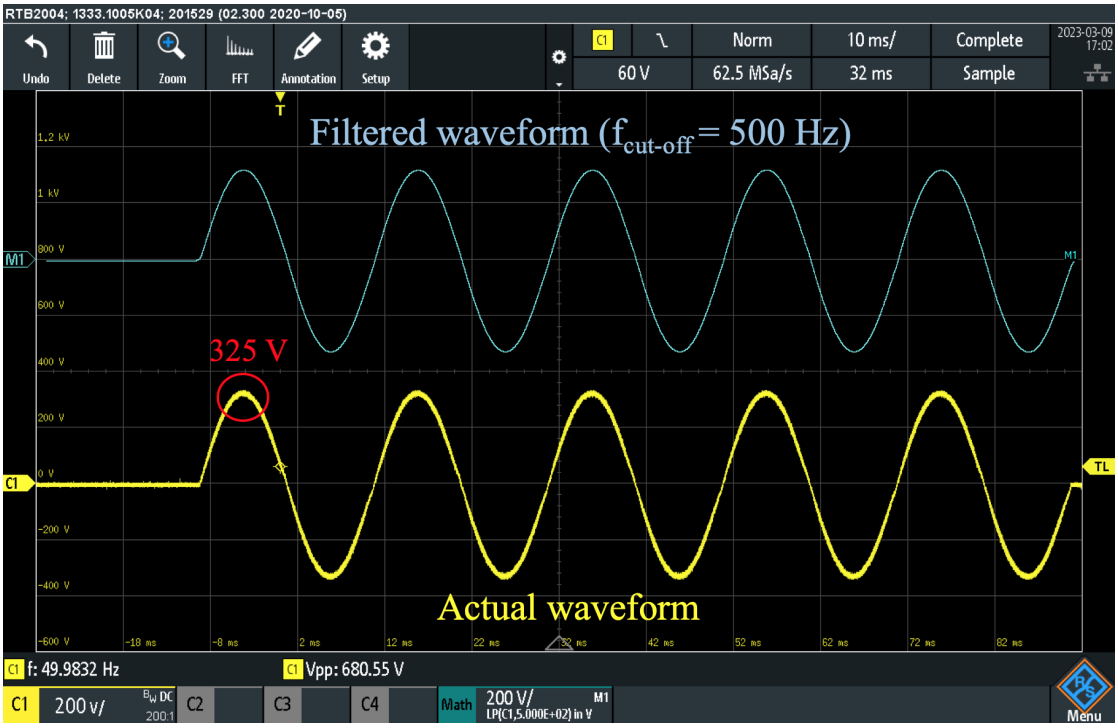


Figure 5.6: Acquisition signal at the terminal of the filter capacitor $C = 3\,\mu F$. The non-filtered signal is yellow, while the filtered signal is blue.

A comparison has been made between the simulated no-load peak-to-peak voltage ripple and the one visualized with the oscilloscope. To be specific, the peak-to-peak voltage in correspondence with the fundamental peak has been observed and reported in Figure 5.8. The signal has been filtered to remove the high frequency noise superimposed on the switching ripple. The acquired, non-filtered signal is the yellow trace. The simulation's peak-to-peak voltage corresponds to $V_{o,\,peak-peak} \approx 11\,V$, which is a similar value to the actual one visible on the oscilloscope $V_{o,\,peak-peak} \approx 12.2\,V$. A slight different between the peak-to-peak values is due to components uncertainty.

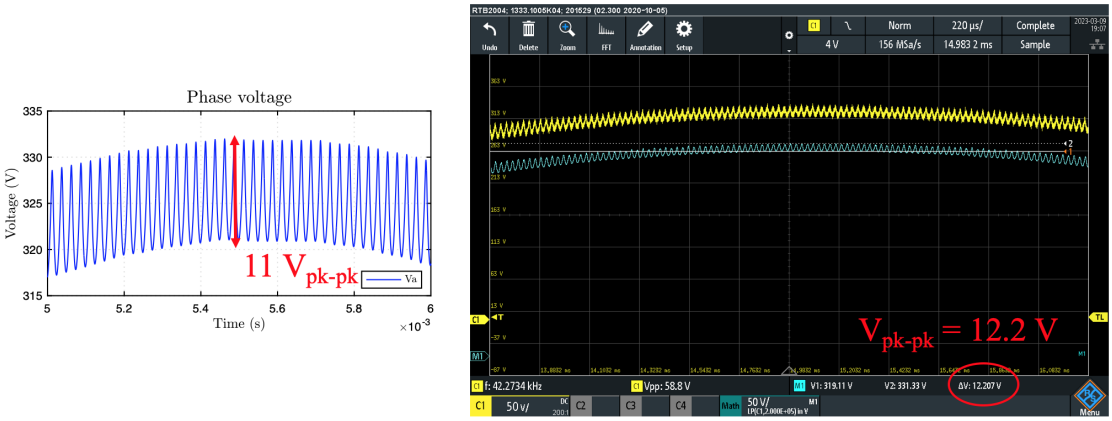


Figure 5.8: Focus on the voltage ripple in correspondence of the fundamental's peak. The simulation result is depicted on the left, whereas the oscilloscope screenshot is on the right. The non-filtered trace is yellow, while the filtered one is blue. It can be noted almost the same peak-to-peak voltage ripple between the simulation and the experimental results.

5.4 Test on a resistive load

A test on a resistive load has been executed to assess the grid emulator performances under load. The test conditions were the same as before ($V_{DC} = 380\,V, f_{sw} = 20\,kHz$), and a liquid cooling was necessary. The entire LCL filter has been set up and connected to a resistive electric heater. The testbench and the heater are represented respectively in Figures 5.9 and 5.10. The rated power of the heater is 3 kW and depending on the setup it could absorb three different levels of power. The oscilloscope employed was the Rohde & Schwarz RTB2004. The acquisition has been made for every level of power. Figure 5.11 shows the screenshot of the oscilloscope for every current absorbed by the heater. The yellow trace is the current, the orange and the green ones are respectively the output voltage at the terminals of the load and the PWM voltage at the terminals of the inverter. The supply voltage does not change when different load requests occur. The PWM varies between plus and minus 380 V as the unipolar modulation technique is applied. The voltage drop from the nominal value is $\Delta V = 8\,V$, corresponding to the 2.5% of the nominal voltage.

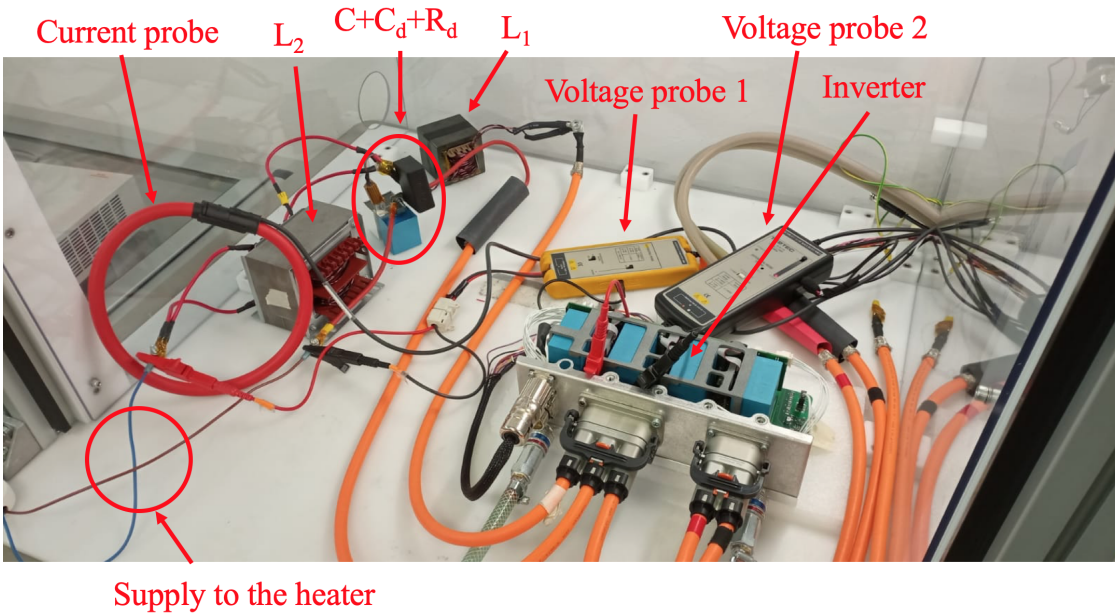
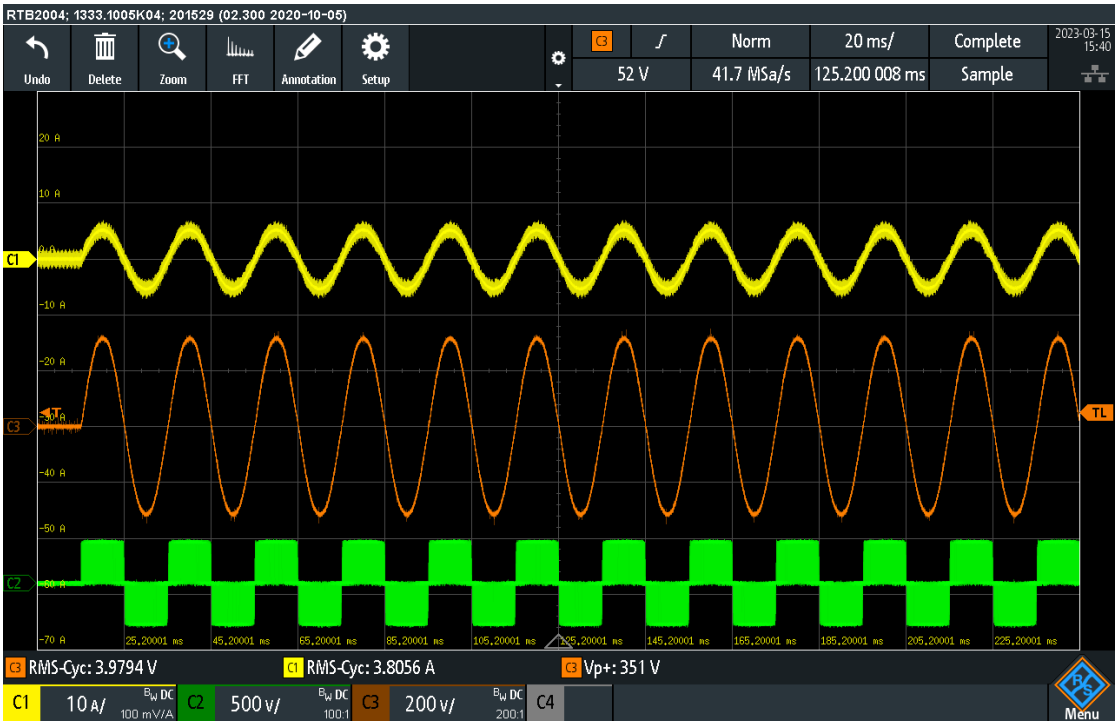
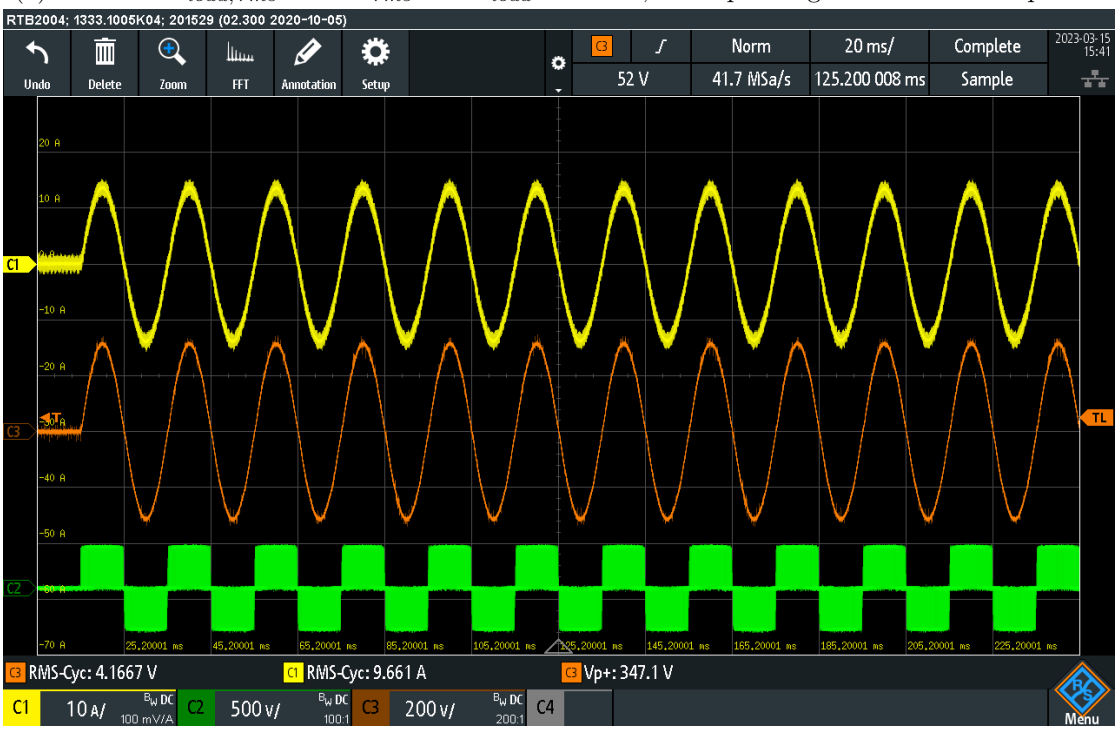


Figure 5.9: Testbench for the load test.

Figure 5.10: Heater used as load.



(a) Test with $I_{load,\,rms} = 3.9\,A_{rms}$ and $P_{load} = 880\,W$, corresponding to the minimum power.



(b) Test with $I_{load,\,rms} = 11.2\,A_{rms}$ and $P_{load} = 2530\,W$, corresponding to the maximum power.

Figure 5.11: screenshots of the tests characterized by different load setups.

5.5 Conclusions

As conclusion, it has been demonstrated that the grid emulator filter was characterized by the features and performances expected from simulations. The actual peak-to-peak voltage ripple when the switching frequency is 100 kHz could not be measured. Despite this, the peak-to-peak voltage ripple estimation from simulations was correct. It is therefore expected that it will be the same in the design conditions. Voltage impulses were used to test the inductors so that the saturation point could be determined. From these, a confirmation of the inductance value has been obtained. Finally, the grid emulator has been tested by connecting a resistive load and achieving a single-phase power of 2.5 kW. The output voltage seems stable except for a voltage drop not greater than the 2.5%.

Chapter 6

Conclusions

In this work, the development of the output filter stage and the control system of a grid emulator has been carried out. In particular, an available two-level converter was selected for the testing of an On-Board Charger designed by the company. Even though the OBC was not prepared yet, it was possible to test the filter performances and the open-loop control by basic experimental tests. An LCL filter has been identified as a feasible solution to represent a weak grid. The filter stage was realized analyzing the normative literature. According to voltage ripple limits and control design, a damping system is implementable to suppress the resonance and ease the tuning of a closed-loop control.
The filter performance was compliant with the requirements. On the contrary, the control design was more challenging. Both a simple open-loop control and a closed-loop control have been analyzed and designed. The drawback of the open-loop control is the poor capability to maintain the voltage at the nominal value and the higher harmonic content. A closed-loop voltage control achieves higher performances. For the first prototype, the tuning of a PI voltage control has been carried out for the ease of design. However, more performing controls will be studied in the future. In any case, the distortion due to dead time is present. Simulations results are provided for several test conditions such as load request satisfaction, underfrequency/overfrequency operation, voltage variation in the operating range of the OBC. In addition, simulations including the PFC control have been performed.
The model has been validated through experimental tests. A testbench has been set up. The designed inductors have been constructed and tested. Although the DC-link voltage and the switching frequency were different from those assumed in the design, it was possible to prove the filtering effect by comparing the results with specific simulations. As a conclusion, the tested grid emulator achieves approximately one-third of the nominal single-phase power on a resistive load with a stable response except from a small voltage drop. The entire testbench will be set up in the future to assess the full power operation.

6.1 Future developments

Future works on the existing grid emulator prototype will include experimental tests of the closed-loop control as well as the three-phase testing. It is possible to assess a control that can reduce the dead time distortion implementing a dead time compensation. In this way, both the harmonic injection issue and the voltage drop may be reduced. The filter has been designed for a determined DC-link voltage. This can be decreased if the fundamental voltage reaches the nominal value without any voltage clamping, improving the high-frequency harmonic content. This can be even more effective for the single-phase case. To end with, the complete testbench will be set up as in Figure 2.1.

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