POLITECNICO DI TORINO

MASTER's Degree in ELECTRONIC ENGINEERING

MASTER's Degree Thesis

Hardware development and prototyping of MIMO imaging RADAR adopting innovative single-chip mmWave FMCW sensor

Supervisor

Prof. RICCARDO MAGGIORA

Candidate

ANTONIO ZAPPATORE

DECEMBER 2022

"Strive not to be a success, but rather to be of value"
by Albert Einstein

Summary

Nowadays, RADAR systems are employed in a wide range of applications, they are used in the defense, aerospace, geolocation fields as well as in the automotive industry. In the latter, RADAR technology has become increasingly predominant for safety purposes.
Several integrated chips are developed every year with augmented processing capabilities allowing for a better targets detection present in the environment with the final goal to develop more effective systems.
Due to the critical applications where RADARs are utilized, a meticulous work is devoted during their design stage. For this reason, special measures are taken to avoid the possibility of failures during the normal operation of these electronic devices.

The project addressed in this thesis focuses on the implementation of a RADAR system integrated on a Printed Circuit Board exploiting the newest AWR2944 Automotive RADAR integrated chip developed by Texas Instruments. Then, the performance of the developed RADAR is verified and compared with the previous version of the system that integrates the AWR1843 chip.

The second-generation RADAR chip offers new features that can be leveraged for future projects or used to enhance the previous ones. The main advantage with respect to the first-generation chip are the increased ADC sampling frequency, the improved Noise Figure in the RF stage and the introduction of the fourth transmitting antenna, which is useful for increasing the azimuth detection capability when MIMO technique is employed together with the Minimum Redundancy scheme.
This chip also offers the opportunity to increase the amount of data exchanged with other sub-systems due to the presence of high-speed interfaces embedded in it. These high-speed interfaces are essential for handling complex algorithms used in modern applications, furthermore, the large number of usable peripherals can be exploited to develop a system with a massive number of devices.

The system that embeds the previous RADAR chip has been defined as the starting point of this work. The previously designed board and the evaluation board provided by Texas Instruments have been used as references for the actual design. Parts of the earlier design have been reused due to compliance with the requirements of the new chip. For instance, the supply chains composed by the DC-DC switching converter and the three Low-Dropout regulators have been taken directly from the previous version of this project.
However, further components have been added for handling the additional functionalities carried by the new device. The introduction of the fourth transmitting stage integrated in the device has been exploited by implementing an additional patch antenna array in the board layout. This gave the possibility to add the estimation of the target elevation angle, which is a missing feature in the previous system.
Another element of improvement was the ability to exploit either short range RADAR application or long range RADAR application with the same system using a pair of transmitting antennas at a time.

After the definition of the RADAR system from the schematic point-of-view, the layout of the board has been started considering the selection of the board stackup.
Since the quality and robustness of the hardware design are the primary factors for RADAR applications, particular attention has been paid to the development of the board in terms of Power Integrity and Signal Integrity since the early layout stages.
The six-layer board stack-up has been carefully chosen to match these requirements. In fact, high-quality materials, as Rogers 3003, have been used to match these constraints, especially when the design of the Radio Frequency part has been considered. Furthermore, the layer arrangement has been designed for getting the best performance and reducing EMI issues.
Then, the previous board layout has been adapted to integrate the new chipset. The needed changes have been employed in order to get a layout that complies with the position of the new chip pins. The arrangement of the re-used components on the board have been optimized, and additional components have been added to the new layout.
Particular attention has been paid in the layout of the supply chains together with the filtering circuitry for getting the correct reference output voltages and to eliminate the unwanted noise contributions.
The decoupling capacitors have been properly positioned to maximize their effectiveness. This arrangement is mandatory for stabilizing the input voltage to the chip power pins, providing the required current accordingly to the switching activity of the chip internal circuitry; otherwise, the latter could be subject to malfunction.

The communication interconnections have been routed following the high-speed design rules for minimizing the signal degradation and skew. For this reason, the interconnections that carry the data signals have been length matched and routed considering a well defined return current path. These arrangements allow to avoid cross-talk phenomena and possible impedance variation along the lines which can corrupt the propagating data.

The Power Delivery Network analysis has been performed for the supply rails in order to estimate the impact of the designed circuitry in providing the reference voltage to the chip pins. This analysis was useful in order to estimate the presence of fatal voltage drops in the final system.
The equivalent model of the used components and the approximated parasitic models of planes and traces have been employed during the creation of the PDN equivalent circuit. The simulation has been performed for all the power rails, with the duty to verify their impedance behavior in the frequency domain.

After the board has been manufactured and the components assembled on it; two embedded software have been prepared for the new RADAR system and the old one. The demo software provided by Texas Instruments have been modified according to the developed board. Since the demo software communicates with the host system through the UART interface, the receiving and transmitting pins have been configured in order to have access to them through the connector mounted on the board. The RADAR systems have been configured to perform the same tasks and prepared for a fair comparison.

The final part has been devoted to the analysis of the output results from the RADAR chips. The recorded data from the tests have been decoded and analyzed utilizing MATLAB. The first measurements have been taken considering the Received Power from a test target using the 10x1 transmitting antenna array and the 10x10 transmitting antenna array which are embedded on both the RADAR boards. Then, the Noise Floor level measurement has been addressed for both systems. The losses due to the AWR2944 chip issues reported by Texas Instruments have been taken into account during the comparison of the obtained results. Considering the losses related to the AWR2944, the Signal-to-Noise ratio results indicate an improvement in favor of the new chip compared to the old one by a factor of 2.2 dB when the results from the 10x1 transmitting antenna array have been considered, and by a factor of 2.7 dB when the results from the 10x10 transmitting antenna array have been examined.

Acknowledgements

I want to spend some lines to express my gratitude to anyone that supported my growing during my university career, from the beginning until the last steps taken in carrying out the thesis project.
First of all, I want to thank my parents, Giuseppe and Lucia; their infinite love allowed me to become the person that I am now. Their respect toward the others and their kindness were my greatest teachings. They allowed me to understand the meaning of sacrifice and determination of reaching the final goal, no matter how far and difficult it is.
I want to thank the person that supported me for this entire journey, Federica. Since we met in the first year of university, we have been very close. I am very glad to have her beside me, we are growing together and together we share the most beautiful moments of our life. Her courage and determination are always a source of inspiration for me.
I want to thank also her family, every time they make me feel at home.
I want to thank the rest of my family, my grandmother Giuseppina, my uncle Mario, my aunt Maria Rosaria and my cousin, Davide, with whom we treated ourselves as brothers since childhood. Although we have different lives today, a time for fun with him is always welcome. All of them have always given me good advice that I was able to take to heart and apply into my life.
I had the opportunity to meet some incredible people during my university career at Politecnico di Torino. I will not forget the infinite, but never tedious, study sessions with Angelo, Luigi, Antonio, Simone, Antonio, Sara. Together with them that time became a magic moment of sharing and joy.
I want to thank all my colleagues with which I could share study sessions or project works. Thank to them, I understood the importance of the teamwork.
I want to thank my roommates, Domenico and Luigi, with which a chat is always appreciated.
I want to greatly thank the Professor Riccardo Maggiora, who gave to me the opportunity to work on this very interesting thesis project. I really appreciated his availability that helped me to investigate in the best possible way on all the topics addressed during this thesis work.

I want to thank the RADARLab staff, Sara, Daniela, Mattia, Maurice and Gianluca. Their experience contributed to my professional growing, every single teaching will remain forever in my mind.
I want to thank Michele that helped me in the final part of this thesis project.

Table of Contents

List of Tables

List of Figures

Acronyms

1D-FFT
one-dimensional fast fourier transform

2D
two-dimensional

2D-FFT
two-dimensional fast fourier transform

AC
alternating current

ADC
analog-to-digital converter

AoA
angle of arrival

ARM
advanced risc machine

BPF
band-pass filter

BPM
binary phase modulation

BGA
ball grid array

CAD

computer-aided design

CAN-FD

controller area network - flexible data-rate

CFAR

constant false alarm rate

CMOS

complementary metal-oxide semiconductor

CPU

central processing unit

CSI2

camera serial interface v2.0

DC

direct current

DC-DC

direct current to direct current

DDM

doppler division multiplexing access

DPC

data processing chain

DPM

data path manager

DPU

data processing unit

DSP

digital signal processing

DUT

device under test

EDMA

enhanced direct memory access

EPC

equivalent parallel capacitance

EPR

equivalent parallel resistance

EMC

electromagnetic compatibility

EMI

electromagnetic interference

ESL

equivalent series inductance

ESR

equivalent series resistance

ePWM

enhanced pulse-width modulator

FFT

fast fourier transform

FMCW

frequency-modulated continuous wave

FOV

field-of-view

FR-4

flame retardant 4

GPIO

general purpose input-output

HWA

hardware accelerator

I/Q

in-phase and quadrature

I2C

inter-integrated circuit interface

IC

integrated circuit

IF

intermediate frequency

I/O

input-output

JTAG

joint test action group

LDO

low-dropout regulator

LED

light emitting diode

LNA

low noise amplifier

LO

local oscillator

LVDS

low-voltage differential signaling

MCU

microcontroller unit

MIMO

multiple-input multiple-output

MMWAVE

millimiter wave

OP-AMP
operational amplifier

PA
power amplifier

PC
personal computer

PCB
printed circuit board

PDN
power delivery network

PLL
phase-locked loop

PRF
pulse repetition frequency

PRI
pulse repetition interval

PSRR
power supply rejection ratio

PTFE
polytetrafluoroethylene

QSPI
quad-serial peripheral interface

RADAR
radio detection and ranging

RCS
radar cross section

RF
radio frequency

RS232

recommended standard 232

RX

receiver

SDK

software development kit

SMD

surface-mount device

SNR

signal-to-noise ratio

SoC

system-on-chip

SOP

sense on power

SPI

serial peripheral interface

TDM

time division multiplexing

TI

texas instruments

TLV

type-length-value

TX

transmitter

UART

universal asynchronous receiver-transmitter

UV

ultraviolet

VRM

voltage regulator module

Chapter 1

Introduction to RADAR

1.1 RADAR Background

RADAR stands for "RAdio Detection and Ranging", it indicates a system that uses electromagnetic waves to detect objects in the operative environment. The usage of these systems has been started since World War II with the duty to detect enemy airplanes. These electronic devices have been evolved significantly over the years, becoming highly accurate and used not only for military purposes but also for civilian purposes.
Independently from the application in which a RADAR system is used, the main principle remains the same. An impulse with a duration τ [s] is sent from the transmitter circuitry toward the direction of detection. The receiver circuitry detects the incoming echoes created by the transmitted signal when it hits one or more objects until the period of time T (PRI) [s] is finished. After that, another impulse is sent.
This chapter considers initially the rectangular pulse technique [1] shown in Figure 1.1, which is the basic methodology exploited in old RADAR systems. The FMCW technique [1] used in modern RADAR applications is described later in this chapter.

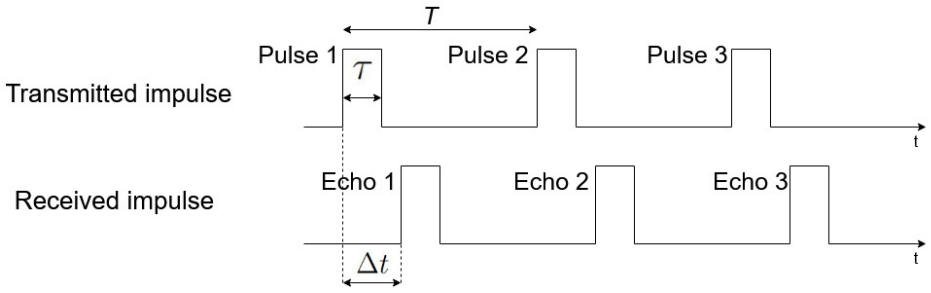

Figure 1.1: Transmitted and received pulses in time domain

A RADAR system is capable to detect targets, and get from them some valuable information; the target information that is possible to obtain are Range, Azimuth, Elevation and Velocity. More than one target could not be discriminated if the same value in all of these parameters occurs, for this reason the resolution of the RADAR on each parameter introduced previously is a crucial aspect of the entire system.

1.1.1 Range Estimation in Pulsed RADAR

[ch.1, 1]

In pulsed RADAR system, the time delay between the sent pulse and the received echo from the illuminated target, known as Δt, can be used to determine the distance between the RADAR and the target. By knowing the propagation speed in a medium, and assuming that the medium is the vacuum, the target range can be estimated as follows.

$$R = \frac{c \times \Delta t}{2} \quad [m] \tag{1.1}$$

Where c is the speed of light.
The range resolution is computed by taking into account the minimum time delay that is possible to appreciate between two consecutive received echoes in order to consider two close objects in the same trajectory as distinct. This value is strictly related to the pulse duration as shown in Equation 1.2.

$$\Delta R = \frac{c \times \tau}{2} \quad [m] \tag{1.2}$$

Another significant consideration is the maximum detectable range, usually called "Maximum Unambiguous Range". Due to the presence of echoes which belong to the current transmitted pulse can return after the transmission of the next pulse; the reception time of the incoming echoes must be limited up to a value equal to the pulse repetition interval (PRI).

$$R_{max} = \frac{c \times PRI}{2} \quad [m] \tag{1.3}$$

In the same manner it is possible to estimate the minimum detectable range, which corresponds to the value of the range resolution as shown in the following expression.

$$R_{min} = \frac{c \times \tau}{2} \quad [m] \tag{1.4}$$

Given these factors, it is possible to assume that the total detectable range can be divided into a number of bins as shown in Equation 1.5.

$$M = \frac{R_{max} - R_{min}}{\Delta R} \tag{1.5}$$

A target can be detected in each range bin corresponding to a specific range position; if many targets share the same bin, they cannot be discriminated until the range resolution is increased or more information are obtained.

The concept of resolution is related to the bandwidth of the signal. Supposing to work with a perfectly defined rectangular pulse in the time domain with a duration of T as described below.

$$x(t) = \begin{cases} 0 & \text{if } |t| > \mathrm{T}/2 \\ A & \text{if } |t| \leq \mathrm{T}/2 \end{cases}$$

The Fourier transform of this signal corresponds to a Sync function with a bandwidth:

$$B = \frac{1}{T} \quad \left[\frac{1}{s}\right] \tag{1.6}$$

This shows that the shorter the pulse duration, the wider the signal bandwidth, consequently the resolution improves.
However, if the transmitted instantaneous power (P_t) remains constant, the transmitted average power (P_{avg}) will decrease due to the shorter pulse duration. Increasing the instantaneous power is one way to solve this issue, but it is quite easy to reach extremely high power value that electrical components may not be able to handle or may it is not possible to comply with regulations.
Considering the duty cycle d_c, which corresponds to the duration of the transmitted pulse within the total period of time dictated by PRI:

$$d_c = \frac{\tau}{PRI} \tag{1.7}$$

The transmitted average power can be computed as follows.

$$P_{avg} = d_c \times P_t \quad [W] \tag{1.8}$$

The above equation shows that by lowering the duty cycle for better resolution, the transmitted average power decreases.

1.1.2 RADAR Equation

[ch.2, 1]

Assuming a system shown in Figure 1.2, the amount of power that returns to the RADAR after the complete propagation path is computed by means of the RADAR equation (Equation 1.9). After the complete path, the power that returns back is drastically decreased compared to the transmitted one, this can alter the probability to detect the target in the environment.

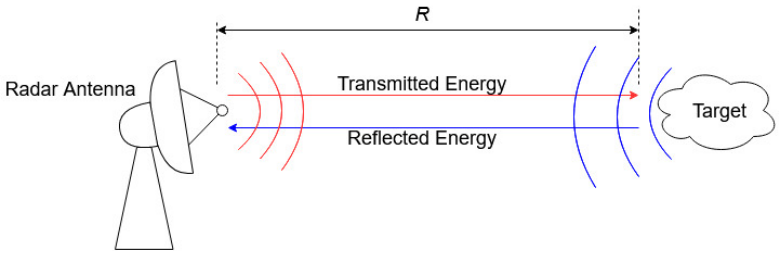

Figure 1.2: Reflected power toward the RADAR

$$P_r = \frac{P_t G \sigma A_e}{(4\pi R^2)^2} \quad [W] \tag{1.9}$$

Where:

- $\frac{P_t}{4\pi R^2}$ is the sphere power density that propagates
- G is the directional antenna gain
- σ is the target Radar Cross Section
- A_e is the antenna effective aperture

Some considerations must be noticed for the received power from the above equation:

- It decreases by the power of four as the range of the target increases
- It is directly proportional to the instantaneous transmitted power
- It is directly proportional to G
- It is directly proportional to RCS
- It is directly proportional to A_e

The situation worsens when noise contributions are considered in the above equation. The final result is more accurate if more of them are considered. The Signal-to-Noise ratio of a RADAR system is evaluated as follows:

$$\frac{S}{N} = \frac{P_t G \sigma A_e}{(4\pi R^2)^2 k T B_W L} \tag{1.10}$$

Where k is the Boltzmann's constant, T is the temperature value, B_W is the bandwidth and L comprehends the extra noise contributions that can affect the detection, for instance, beam shape loss, input to system noise, waveguide and microwave losses, signal processing loss, lens effect and fluctuation loss.

The following Figure 1.3 depicts how the signal power varies along the space propagation path from the transmitting antenna to the receiving antenna without considering external noise contributions.

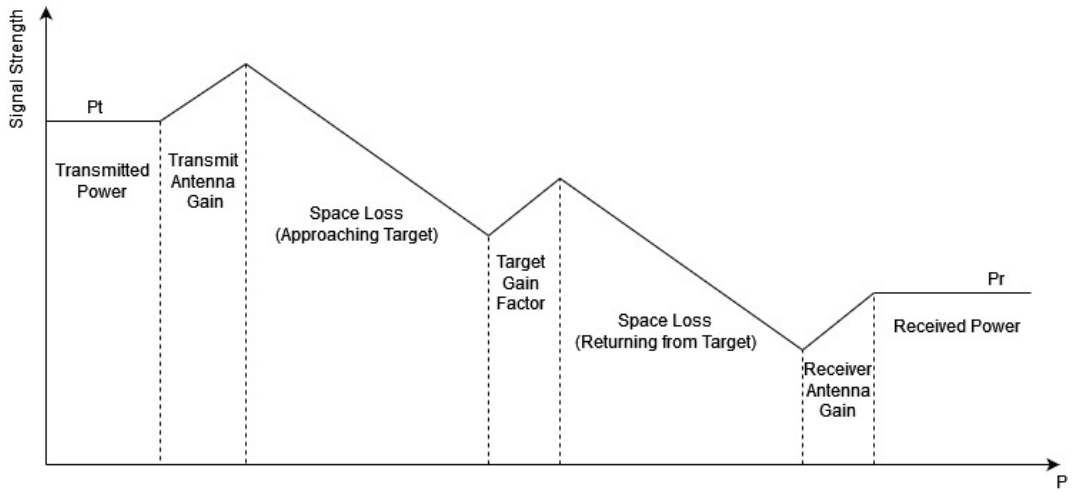

Figure 1.3: Signal strength vs position in space

The computation of the signal power is not an easy task, another factor that can be considered is the attenuation in free air. It can change within a wide range according to the frequency of the signal due to the presence of resonances. For this reason, the wavelength selection plays an important role during the system design in order to reduce the risk of over-attenuated signal. The working frequency range with low attenuation in dB per kilometer should be considered.
However, weather condition can largely influence the behavior of the RADAR detection during the working time. The weather could condition the received signal due to the continuous changing of the signal attenuation per kilometer.

1.1.3 Radar Cross Section

[ch.2, sec.7, 1]

As shown in Equation 1.9, an important parameter present in the RADAR equation is the Radar Cross Section of an object. It is defined as "the (fictional) area intercepting that amount of power which, when scattered equally in all directions, produces an echo at the radar equal to that from the target" as stated in [1].

$$\sigma = \frac{\frac{\text{power reflected toward source}}{\text{unit solid angle}}}{\frac{\text{incident power density}}{4\pi}} \quad [m^2] \tag{1.11}$$

The RCS Equation shown above and taken from [1] describes the ability of the illuminated object to reflect back the energy from the transmitted pulse. The estimation of this parameter is not straightforward due to it is influenced by the object material, the angle from which the target is detected, the physical size of the target and many others parameters. All these variations make the Radar Cross Section to fluctuate. A common methodology used to overcame this problem is to decompose a complex object into easier-to-estimate objects with specific geometry and simpler Radar Cross Section. An object with constant Radar Cross Section is useful for calibration purposes. For example, the corner reflector is meant for these kind of operations; it has a very valuable RCS due to its high value towards a particular direction over a wide angle[2], in fact its directivity is limited to about $\pm$ 60 degrees. The corner reflector RCS pattern is shown in Figure 1.4 and its value can be computed using Equation 1.12.

$$\sigma_{corner} = \frac{4\pi {A_e}^2}{\lambda^2} \quad [m^2] \tag{1.12}$$

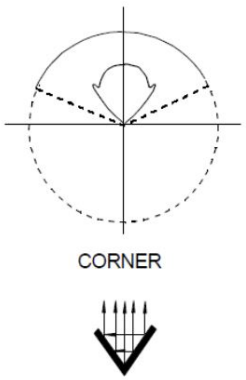

Figure 1.4: Corner reflector RCS pattern[2]

1.1.4 Azimuth and Elevation Estimation

The azimuth position or elevation position of a target can be estimated by using different techniques; for example, it is possible to estimate the AoA by mechanically steering the antenna beam and collecting the angle information from the position of the antenna where the target is detected. However, modern RADAR systems estimate the angle of arrival of a target without the mechanical movement of the antenna; these systems apply the Beamforming and/or MIMO.

Angular Resolution of Mechanically Steered Antenna

Assuming a single antenna pattern seen from above as shown in Figure 1.5, the antenna design used in the RADAR system determines the angular resolution which allows to identify two objects that are far apart at least this value in azimuth.

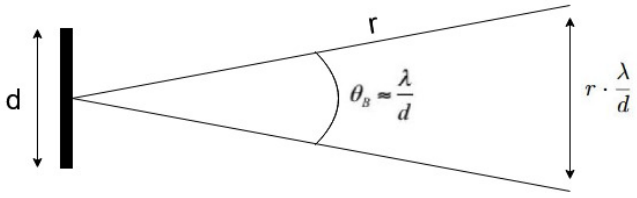

Figure 1.5: Angular resolution of single antenna pattern

$$\text{Angular resolution} = r \cdot \Theta_B = r \cdot \frac{\lambda}{d} \quad [m] \tag{1.13}$$

Equation 1.13 shows the angular resolution obtained from the antenna parameters. The minimum detectable space in both azimuth and elevation decreases if the wavelength (λ) decreases, or if the antenna length (d) increases. Notice that, this value is also dependent by the range position (r).

Digital Beamforming

New RADAR systems employ a phased array antenna, as that one utilized for this project. The phased array antenna is a set of multiple antennas mounted at a certain distance one from the other forming an array. This solution makes the radiation pattern change with respect to the single antenna. The usage of multiple antennas gives the possibility to compress the main lobe, giving two advantages, a better resolution in azimuth that depends on the number of the antennas utilized, and the capability to steer the main beam toward the wanted direction. Together with the phased array antenna, the digital beamforming[3] can be utilized to extract

the angular position of the targets by electronically steering the beam generated by the array [1]. Figure 1.6 shows the digital beamforming scheme.

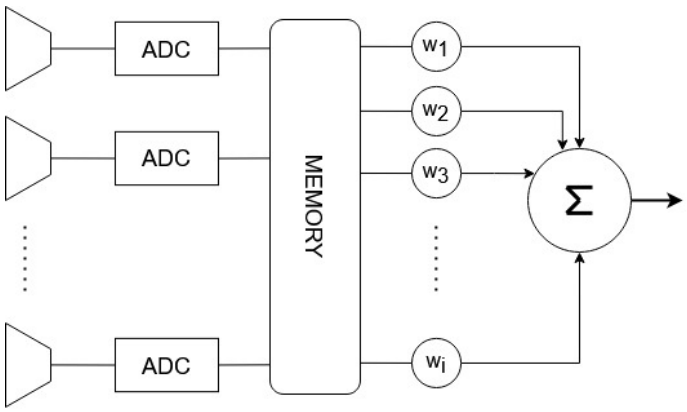

Figure 1.6: Digital beamforming scheme

The incoming signal is received by the N receiver antennas, each channel performs the Analog-to-Digital conversion and stores the results in the memory. Then, the ADC samples are multiplied by the weighting functions according to the angle from which the target must be revealed. This process is called "angular compression" and a fixed phase variation onto the received signals is applied in order to sense the targets presence at different angles. It is performed by the processor, which can extract the targets present in all the angle of arrival at the same time.

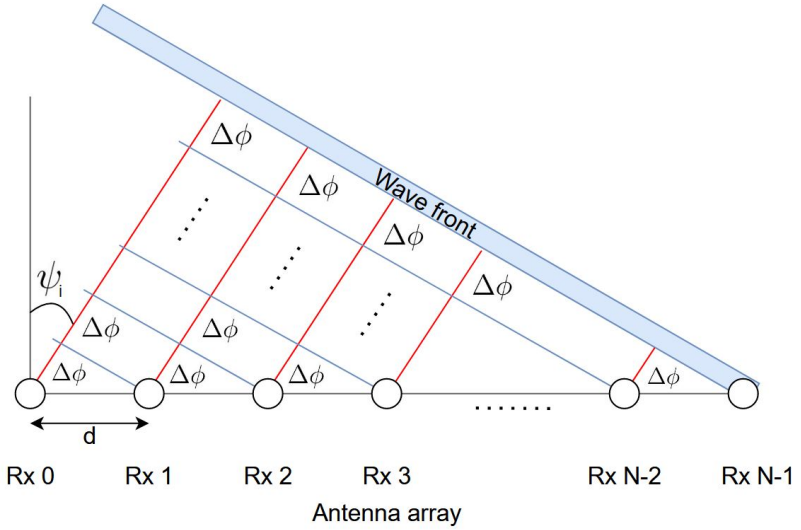

Figure 1.7: Beamforming applied to a received wave front

Figure 1.7 depicts the link between the angle of arrival of the wavefront and the phase difference between two consecutive antennas. As it is possible to notice, the wavefront angle corresponds to a value of $\Delta\phi$ between two consecutive antennas. The phase difference is defined by the following expression:

$$\Delta\phi(\psi_i) = sin(\psi_i)2\pi\frac{d}{\lambda} \quad [rad] \tag{1.14}$$

Given this phase difference, it is possible to evaluate the samples at a certain direction by considering the following reference function.

$$\vec{b}(\psi_i) = \begin{pmatrix} e^{j0\cdot\Delta\phi(\psi_i)} \\ e^{j1\cdot\Delta\phi(\psi_i)} \\ e^{j2\cdot\Delta\phi(\psi_i)} \\ . \\ . \\ . \\ e^{j(N-1)\cdot\Delta\phi(\psi_i)} \end{pmatrix}$$

The angular compressed signal is computed by multiplying the received signal by this reference function for the corresponding phase difference value of the angle of interest.

The angular resolution can be obtained by computing the first null (ψ_{fn}) of the angular compression function, which is shown below:

$$sin(\psi_{fn}) = \frac{1}{N\frac{d}{\lambda}} \quad [rad] \tag{1.15}$$

However, the distance that is usually employed between the antennas is $\frac{\lambda}{2}$, in this way the maximum detectable angle is maximized to $\pm\ \frac{\pi}{2}$ rad, and it is possible to eliminate the ambiguities.

The beamforming can be utilized adopting a matrix of antennas; in this case the samples can be also weighted considering the phase difference also in the elevation direction in order to extract the elevation information from the targets.

1.1.5 Velocity Estimation in Pulsed RADAR

[ch.3,sec.1, 1]

In classical RADAR system, the Doppler frequency shift is used to estimate the target relative velocity; it can be used to discriminate moving targets rather than static ones. Whenever a fixed frequency signal hits an object with a velocity other than zero, the wavelength of the return signal varies, in particular, it decreases if the target approaches the RADAR or it increases if the target moves away from the RADAR. Figure 1.8 shows the Doppler frequency shift that can be appreciated in the frequency domain for a closing target (left picture) or for an opening target (right picture).

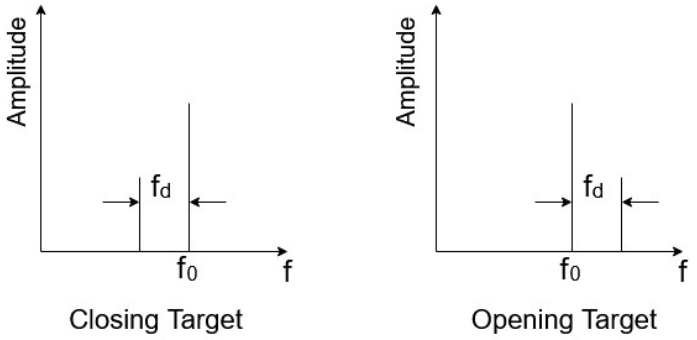

Figure 1.8: Doppler frequency shift for closing or opening target

Since the variation in range due to the movement of the target corresponds to a variation of the signal phase with respect to time, the Doppler frequency shift can be obtained as follows.

$$f_d = \frac{1}{2\pi}\frac{d\Phi}{dt} = \frac{1}{2\pi}\frac{4\pi}{\lambda}\frac{dR}{dt} \rightarrow f_d = \frac{2 \cdot v}{\lambda} \quad [Hz] \tag{1.16}$$

The maximum velocity and velocity resolution of the RADAR system can be computed using the relationships shown below; the former depends by the Pulse Repetition Frequency (PRF), which must be considered at least twice the maximum detectable Doppler frequency, and the latter is determined by the number of samples that are obtained.

$$v_{max} = \frac{\lambda \cdot PRF}{4} \quad \left[\frac{m}{s}\right] \tag{1.17}$$

$$\Delta f_d = \frac{1}{N \cdot PRI} \quad [Hz] \rightarrow \Delta v = \frac{\lambda}{2 \cdot N \cdot PRI} \quad \left[\frac{m}{s}\right] \tag{1.18}$$

Higher v_{max} value requires a higher PRF, but this introduces a trade-off with the Maximum Unambiguous Range as shown in equation 1.3.

1.2 RADAR Architecture and Processing

1.2.1 General RADAR Scheme

This section describes the architectures that are used in a RADAR system; in particular, it analyzes what are the devices present in the system and their role. Recent applications move in the direction of fully integrated RADAR in a SoC. Internally, these chips contain the required devices for the correct functioning with additional specialized modules, embedded in a monolithic implementation.
The block diagram of the main architecture for a pulse RADAR without compression is shown in Figure 1.9.

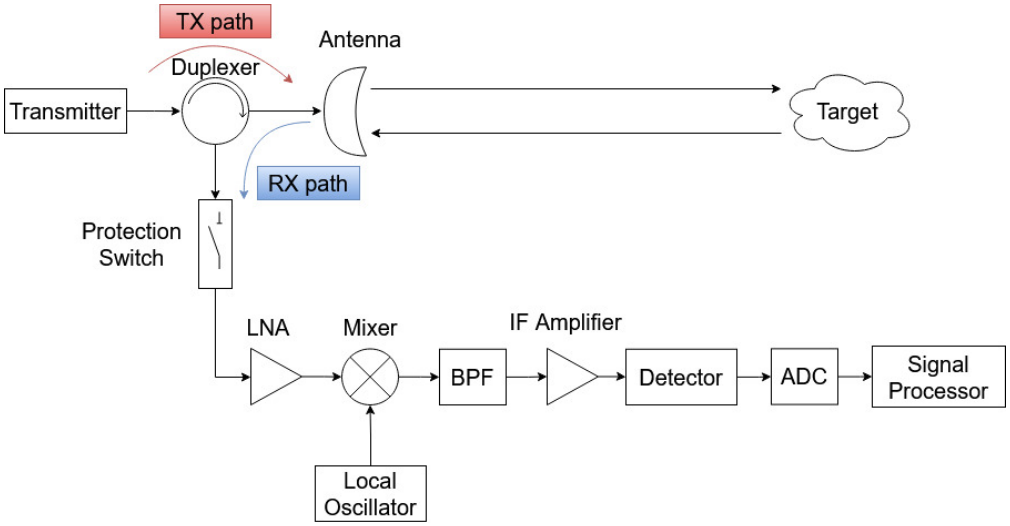

Figure 1.9: Basic RADAR architecture block diagram

The signal inside the architecture can follow two paths, the transmitter chain, which is devoted to generating the signal to be transmitted toward the environment; and the receiver chain, which role is to collect the signal from the environment and elaborate it.

Transmission chain:

- The transmitter creates the pulse signal that is transmitted with a predefined period and duty cycle.
- The duplexer is employed to separate the TX and RX systems, avoiding that the transmitted signal to be injected into the receiver chain or vice versa.

Receiver chain:

- A protection switch enables the listen operation. Once the signal from the antenna has been redirected toward the receiver, it can be analyzed by the receiver stage. The switch allows an additional degree of protection for the connected devices in this chain.
- A Low Noise Amplifier that amplifies the received signal, then it is mixed with the LO signal into the Mixer whose generates the IF frequency. The transmitter can be synchronized with the LO in order to maintain the coherence.
- The IF amplifier amplifies the signal at the output of the mixer.
- The Analog-to-Digital conversion is performed to convert the information into the digital domain.
- The digital information is then analyzed by the DSP unit, which is in charge to apply the processing algorithm to get the result of the detection.

1.2.2 Pulse Doppler Processing

Figure 1.10 shows an enhanced version of the general RADAR scheme, in this architecture the In-Phase and Quadrature method is considered at the receiver side.

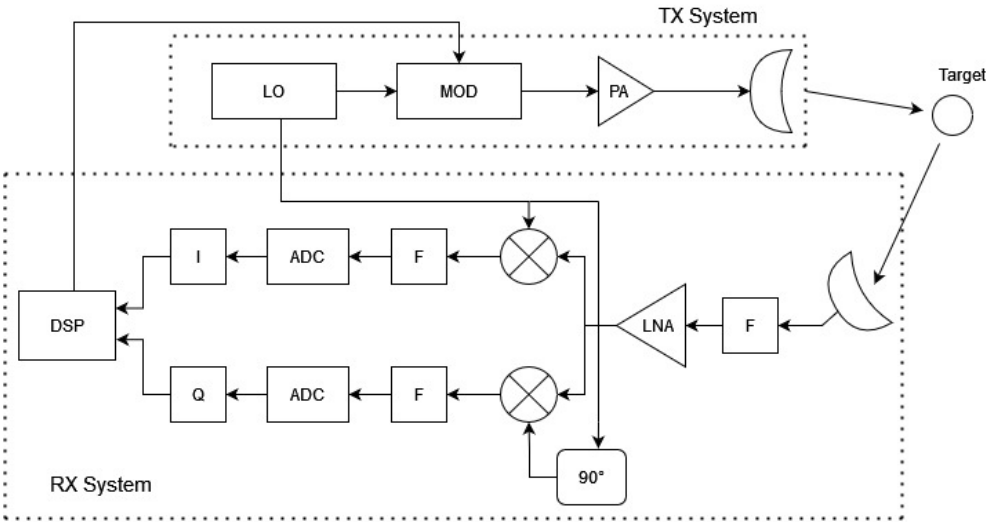

Figure 1.10: RADAR architecture with IQ receiver

The incoming signal is filtered, amplified, and then converted with the In-phase and Quadrature technique. The main advantage in using this method is the lack of information loss due to the sampling frequency. In this system the signal can be sampled with a frequency equal to the signal bandwidth. However, the main drawback relates to a more complex structure than the original one due to the storing and processing of twice the number of samples.
The real and imaginary parts of the sampled signal are stored into two separated matrices called "Data Matrix".

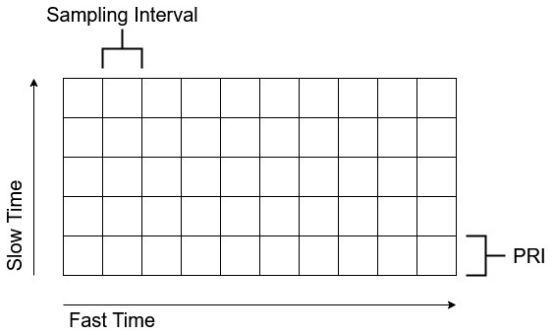

Figure 1.11: Data Matrix example

The Data Matrix in Figure 1.11 collects on the x-axis the samples from each pulse for the entire PRI, which is called "fast time". The received response that belongs to the next pulses are stored along the y-axis, which is called "slow time". If more than one receiving channels are used for detection, the Data Matrix became the "RADAR Cube", in which each plane represents the single receiver channel Data Matrix seen before. Figure 1.12 shows an example of a RADAR Cube with N receiver channels.

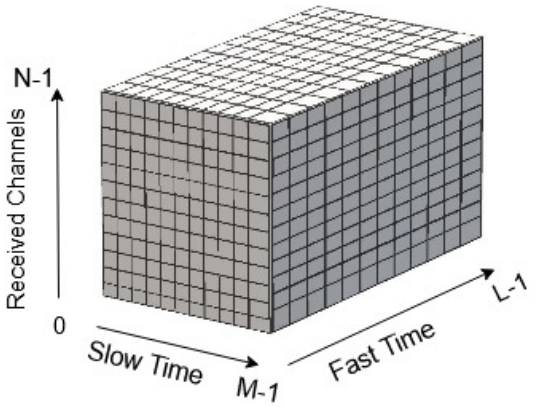

Figure 1.12: RADAR Cube example

Once the Data Matrix has been filled with the samples of the entire frame, the absolute value of range and velocity are computed by exploiting the Range-Doppler processing, the result of this operation is the Range-Doppler map. This map shows the range and velocity of the detected targets as peaks in the matrix.
The Range-Doppler process is described below:

1. It takes the input samples stored in the fast time axis of the Data Matrix and computes the Range-FFT in order to detect the presence of targets in each range bin.

2. It takes the Range-FFT output data, and performs the Doppler-FFT onto the slow time axis to discriminate the target velocity from the detected target for each range bin.

A final result example is shown in the following picture, where the range and velocity information of three objects are extracted using the Doppler-FFT processing (right picture) on the Range-FFT data (left picture).

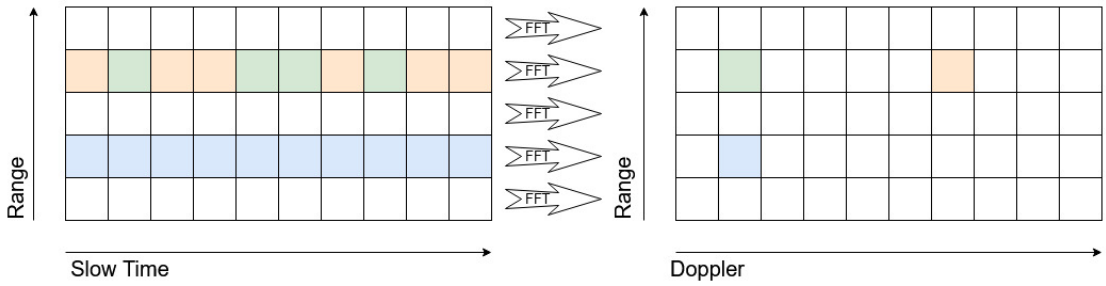

Figure 1.13: Doppler-FFT process example

After the procedure described before, the angle of arrival of the targets can be extracted from the obtained results. Since the RADAR Cube stores the data from several channels, a further FFT to each peak on the Range-Doppler map moving along the receiver channel direction can be used to distinguish objects with different relative angular positions with respect to the RADAR. This method is called Angle-FFT.

1.3 FMCW Imaging RADAR

[ch.3, sec.3, 1] [4]

In Section 1.1.1 it was pointed out that the range resolution increases if the bandwidth of the unmodulated signal increases, which means that for better performance the duty cycle of the pulsed signal must decrease. A RADAR that uses a short duty cycle pulse transmits less energy, due to this, the ability of the electromagnetic wave to reach long distances decreases as well as the ability to detect targets.
It is important to point out that the compression gain for an unmodulated signal is always unitary as stated in Equation 1.19.

$$B \cdot \tau = 1 \tag{1.19}$$

Modern RADAR devices, as that one used in this thesis project, exploit a different type of signal with which the compression gain can be improved. The application of modulated signal is called Frequency Modulated Continuous Wave. FMCW signal has a frequency that increases linearly during the transmission time, usually it is called "Chirp" (Figure 1.14). Mathematically, it is defined as:

$$x(t) = cos(2\pi f_0 t + \pi S t^2) \tag{1.20}$$

$$S = \frac{\Delta f}{T_c} = \frac{B}{T_c} \quad \left[\frac{Hz}{s}\right] \tag{1.21}$$

S is the slope of the signal, and it indicates how the frequency of the signal changes in a period of time T_c. The bandwidth is given by the sweep between the starting frequency and the final one as shown in Figure 1.15.

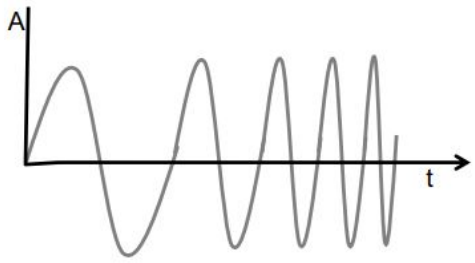

Figure 1.14: Frequency modulated signal in time domain [4]

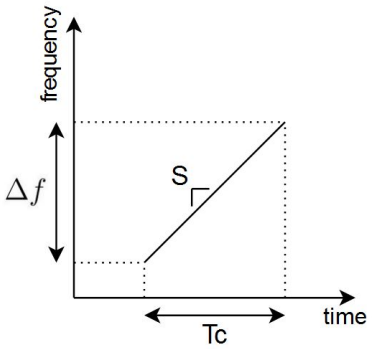

Figure 1.15: Frequency vs time of a chirp signal

Thus, the FMCW signal has a compression gain expressed by Equation 1.22; it is directly proportional to the frequency sweep during the chirp transmission time.

$$\text{compression gain} = B \cdot T_c \tag{1.22}$$

The corresponding matched filter function contains unwanted side lobes which could interfere with the detection of adjacent targets.
The general scheme for FMCW technique is depicted in Figure 1.16.
The transmitter continuously sends chirp signals with a period of T_c. At the receiver side, when the signal is received, it is directly down-converted by the mixer with the transmitted signal. The result of this operation is the Intermediate Frequency (IF) signal. Since the IF signal indicates the frequency difference between the transmitted and the received signal, this can be linked to the delay in time between these two signals as shown in Figure 1.17.

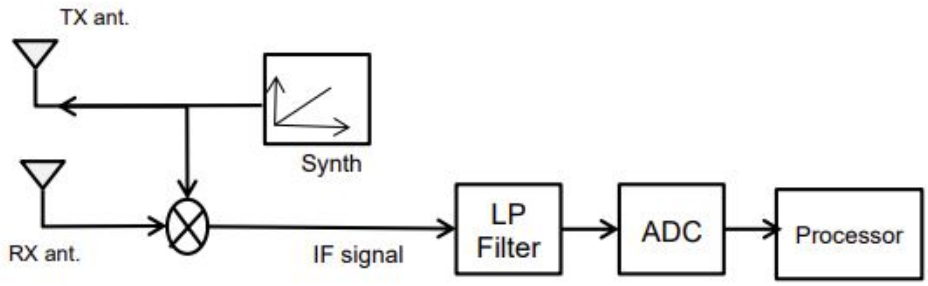

Figure 1.16: FMCW method block diagram [4]

The target range can be estimated considering the IF frequency value obtained after an FFT computation on the mixer output.

$$R = \frac{c}{2 \cdot S} IF \quad [m] \tag{1.23}$$

The maximum IF value that is possible to measure limits the maximum detectable range, meaning that this is strictly related to the maximum ADC sampling frequency. Considering at least a sampling frequency of $Fs = 2 \cdot IF$ [Hz] the maximum detectable range is given by:

$$R_{max} = \frac{c}{4 \cdot S} F_s \quad [m] \tag{1.24}$$

Two objects in the same trajectory can be solved if the related IF signals are at least $\Delta f = \frac{1}{T_c}$ distant, otherwise a single tone appears after the FFT, merging the targets. The range resolution obtained from the previous consideration is shown in Equation 1.25; which is only dependent by the bandwidth of the signal.

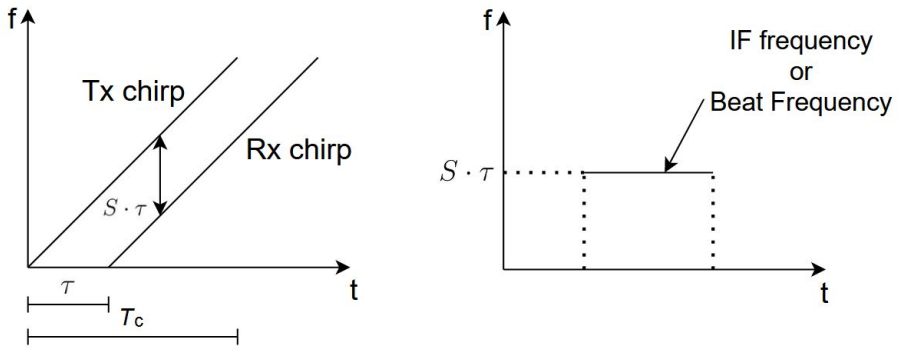

Figure 1.17: FMCW single target detection

$$\Delta R = \frac{c}{2 \cdot B} \quad [m] \tag{1.25}$$

The velocity of a target can be determined by sending repeated chirps and comparing the phase of the peaks obtained from the range-FFT previously examined. A moving target in the FMCW application will change the return chirp phase, but the IF frequency remains the same. Figure 1.18 shows the phase variation between two received chirps.

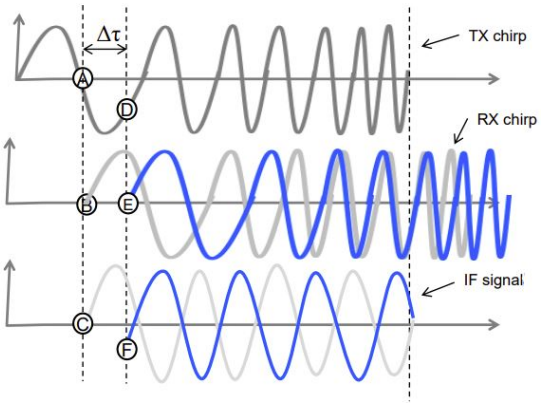

Figure 1.18: Phase changing of a small round-trip variation [4]

The phase difference is used to compute the velocity as follows.

$$v = \frac{\lambda}{4\pi T_c} \Delta\Phi \quad \left[\frac{m}{s}\right] \tag{1.26}$$

The maximum phase difference cannot be more than π, otherwise the direction from which the target arrives cannot be solved due to the ambiguity.

This leads to a maximum detectable velocity equal to:

$$v_{max} = \frac{\lambda}{4T_c} \quad \left[\frac{m}{s}\right] \tag{1.27}$$

Assuming that the RADAR sends N chirps with period T_c, the FFT on this frame length (T_f) can separate two frequencies that have a separation at least of $\Delta\Phi = \frac{2\pi}{N}$ rad, the resulting velocity resolution is computed below.

$$\Delta v = \frac{\lambda}{2T_f} \quad \left[\frac{m}{s}\right] \tag{1.28}$$

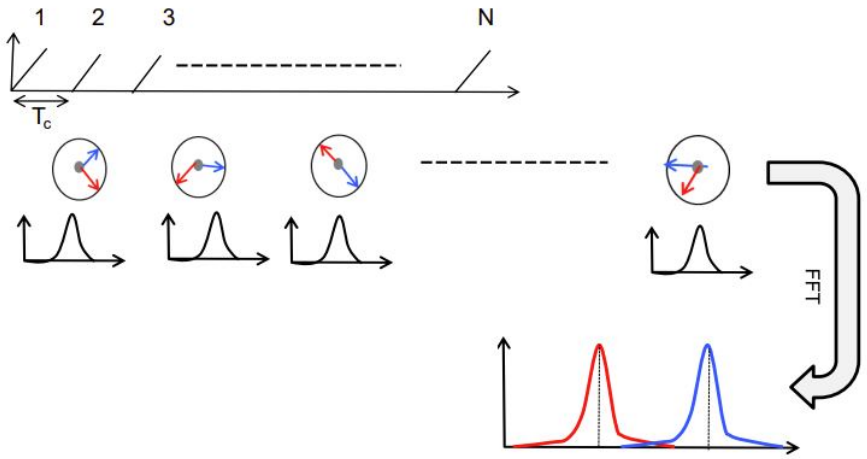

Figure 1.19: Doppler-FFT after N chirps for recognizing two targets in the same range bin [4]

The above figure depicts the Doppler-FFT made on the Range-FFT phasors in order to extract the velocity information of the two targets.

If multiple objects cannot be estimated either in range nor in velocity, the system must identify their presence extracting the angle of arrival of each target.
The angle of arrival of a target can be considered if the system employs more than one receiving antenna. In this case the phase information of the incoming signal must be taken into account performing a third FFT after the Doppler-FFT on its output peaks.

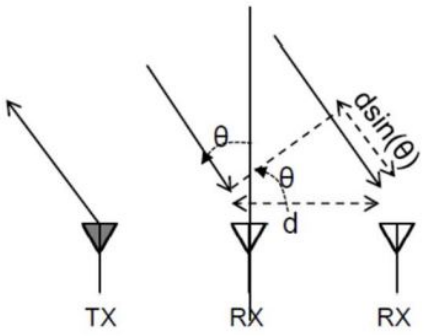

Figure 1.20: Angle of arrival FMCW RADAR [4]

Assuming an antenna pattern as shown in Figure 1.20, the corresponding target angle can be estimated by knowing the distance between the RX antennas, which is indicated as d.

$$\Delta\Phi = \frac{2\pi d sin(\theta)}{\lambda} \rightarrow \theta = sin^{-1}\left(\frac{\lambda}{2\pi d}\Delta\Phi\right) \quad [rad] \tag{1.29}$$

Due to the non linearity of the expression above, the accuracy decreases if the detected object approaches an angle of $\pm\frac{\pi}{2}$ rad.
Also in this case the ambiguity can occur if the phase difference of the signal that arrives to the adjacent antennas is greater than π rad. So the maximum detectable angle can be computed as follows.

$$\theta = sin^{-1}\left(\frac{\lambda}{2d}\right) \quad [rad] \tag{1.30}$$

The AoA field of view is maximized to $\pm\frac{\pi}{2}$ rad if the distance between the receiving antennas is $\frac{\lambda}{2}$. Instead, the angular resolution is related to the number of the employed receiving antennas.
Equation 1.31 shows the angular resolution when the spacing for maximizing the FOV and a value of $\theta \approx 0$ rad are considered.

$$\Delta\theta = \frac{2}{N} \quad [rad] \tag{1.31}$$

Figure 1.21 depicts the Angle-FFT on the Doppler-FFT results in order to get the angle of arrival of the targets.

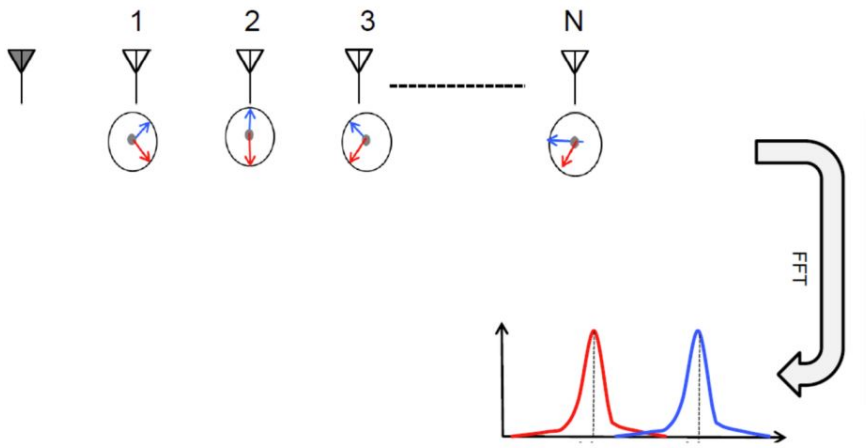

Figure 1.21: Angle of arrival FFT with N antennas [4]

1.4 MIMO Systems

At the end of Section 1.3 has been shown that the angular resolution depends on how many receiving antennas are used in the RADAR system. Following this trend, for a better angular resolution the complexity of the system increases exponentially. By doubling the number of RX antennas, the angular resolution will be half, but the receiving chains must double also.
The MIMO technique [5] is exploited in modern RADAR applications with the aim to get higher angular resolution without employing a large number of antennas in the design.

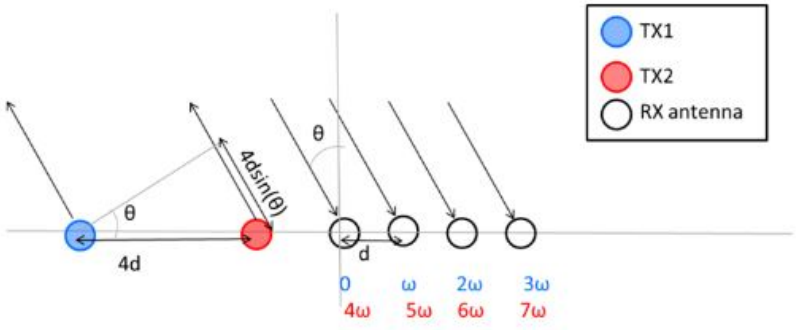

Figure 1.22: MIMO technique principle [5]

Figure 1.22 shown that MIMO architecture uses more than one transmitting antenna in order to benefit of the virtual array; the angular resolution is proportional to the number of the antennas that compose the virtual array.

$$\text{Virtual Array Elements} = N_{TX} \cdot N_{RX} \tag{1.32}$$

Where N_{TX} is the number of transmitting antennas and N_{RX} is the number of receiving antennas. The distance between TX antennas must be equal to the product of the number of RX antennas and their distance.
The resulting virtual array is shown in Figure 1.23.

Figure 1.23: MIMO virtual array [5]

In MIMO system the orthogonality of the transmitted signals must be ensured in order to distinguish each signal. Then, a matched filter is employed to extract the correct information from the incoming signal. Two main methods are usually employed for this purpose, the Time Division Multiplexing (TDM) or the Binary Phase Modulation (BPM).
The TDM method allocates on each transmitted block a number of chirps equal to the transmitting antennas separated in time, only one transmitter is active when transmitting the chirp.

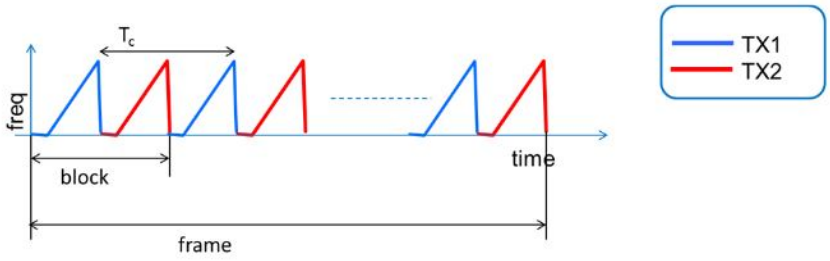

Figure 1.24: Time Division Multiplexing [5]

The figure above shows the transmitting pattern of the TDM method.

Range and velocity information for each virtual antenna are extracted using a 2D-FFT, and the angle of arrival is obtained using an angle-FFT from the previous results, as described in Section 1.3.

Instead, the latter technique uses all the TX antennas simultaneously, allowing to deliver more power than TDM. A frame is composed of a number of blocks, each block contains N_{TX} chirps. The orthogonality in this case is ensured in a digital manner.

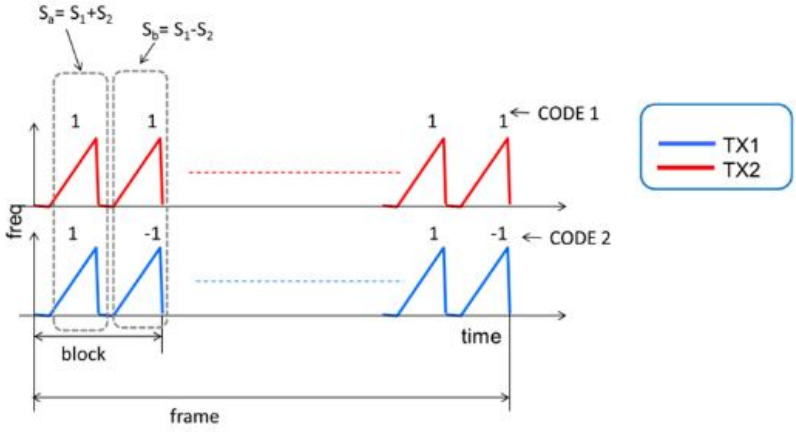

Figure 1.25: Binary Phase Modulation [5]

Is it is possible to notice from Figure 1.25, each chirp could be in phase or out of phase by 180° depending on the assigned code.

1.5 Minimum Redundancy in MIMO RADAR

The minimum redundancy linear array[6] can be utilized together with the Multiple-Input Multiple-Output technique in order to further increase the RADAR spatial resolution[7]. The design of the linear antenna array usually employs a separation between receiving antennas which is fixed. The uniform array is not optimal due to the presence of redundant spacings. Further improvement in the resolution can be achieved using the same number of antennas if redundancies are eliminated, allowing an increasing of the array length[6].
As stated by Dr. Chun-Yang Chen and Dr. P. P. Vaidyanathan in their article [7], the concept of the minimum redundancy can be extended also in MIMO RADAR when a non-uniform antenna pattern is considered. The usage of the Minimum Redundancy scheme improves the rejection of the mainlobe interferences, together with negligible degradation in sidelobe interference rejection capabilities[7].

Considering the case of this project, the custom RADAR system has been developed to work with four receiving antennas exploiting the four element scheme present in [6]. The elements that occupy the positions between the elements in the non-uniform array are obtained from the latters.
The following picture illustrates the Minimum Redundancy scheme that is utilized with a single transmitting antenna and four receiving elements (on the left), and the resulting virtual array composed of seven elements obtained after the signal processing (on the right).
u_0 is the unit spacing quantity, in this case it is equal to $\frac{\lambda}{2}$.

Figure 1.26: Minimum Redundacy scheme in a four elements array

The Minimum Redundancy concept is cost-effective. Thus, it is possible to use less antennas in the system without sacrificing performance, which translates into a less expensive solution than utilizing a uniform antenna array.

Chapter 2

The AWR2944 Chip

The second chapter is devoted to presenting the core device utilized in this project. In order to understand what are the main features of the device, a brief introduction on what is present inside the AWR2944 chip is addressed in the following sections. It is useful to know the device characteristics in order to recognize its capabilities before adopting it in the design. The design constraints have been analyzed to respect the chip requirements, allowing the latter to operate under good condition once the board is manufactured.

Before considering the main characteristics of the device, it is convenient to point out why modern RADARs move toward the high frequency range, especially in the mmWave spectrum.
As reported in [8], the primary cause has been the change of the working spectrum for short range RADAR application. From January 1, 2022, the ultra-wide band at 24 GHz is no longer available. Due to the need for an ultra-wide band for a high-resolution applications, the signal used in short range RADAR has been moved in the frequency range of 77-81 GHz, and the signal used in mid-range and long-range RADAR has been moved in the frequency range of 76-77 GHz. On the other hand, this allowed a greater integration of RADAR devices; one example is the massive introduction of these systems in the automotive field.

2.1 Chip Architecture

The AWR2944 chip is available in a BGA package and it embeds a complex micro-architecture which is structured into three main parts.
The RF and Analog subsystem manage the communication with the external world, it contains the Radio Processor for the manipulation of the RF signal in transmission and reception.
The Main subsystem contains the ARM Cortex-R5F processor, it is used for controlling the connected peripherals, and for the house-keeping activities of the device[9].
For the signal processing part, the TMS320C66x DSP unit is employed[9].

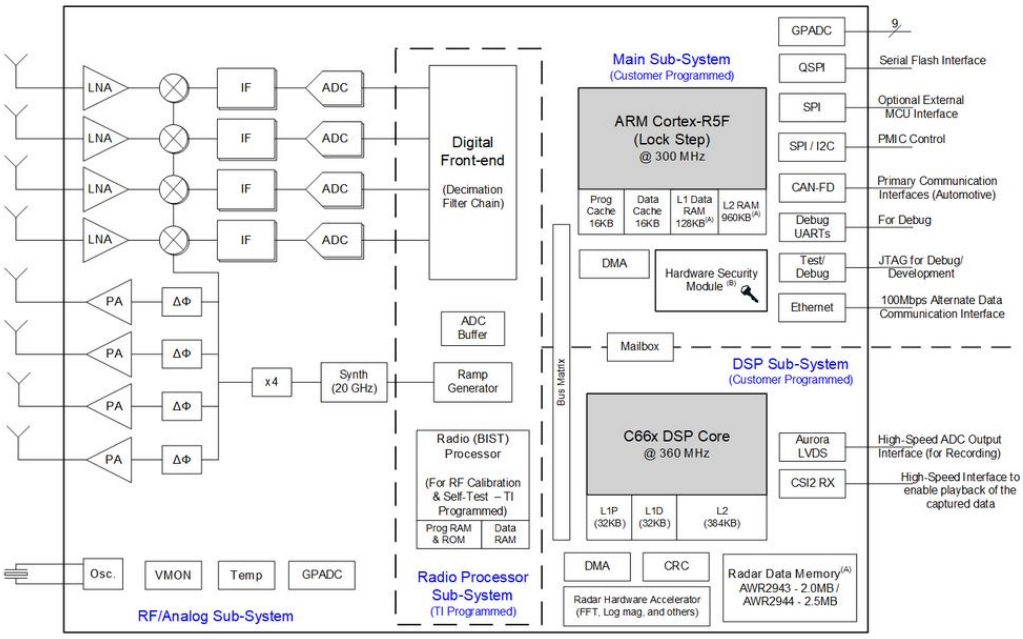

Figure 2.1: AWR2944 architecture block diagram taken from AWR2944 datasheet[9]

Figure 2.1 shows the complete architecture from a high-level point-of-view. Each individual subsystems are highlighted in the following sections.

2.1.1 RF and Analog Subsystem

The RF and Analog subsystem comprehends the front-end circuitry to manipulate the four TX chains for the transmission of the signal and the four RX chains for the signal reception.

It also embeds four ADC for the conversion of the analog signal into the digital domain.
The 76 to 81 GHz Local Oscillator signal is generated by the "RF Clock Subsystem" group[9] as shown in Figure 2.2, and it consists of the following elements:

- Built-in oscillator
- Analog PLL
- RF synthesizer
- x4 Multiplier
- Time Engine block

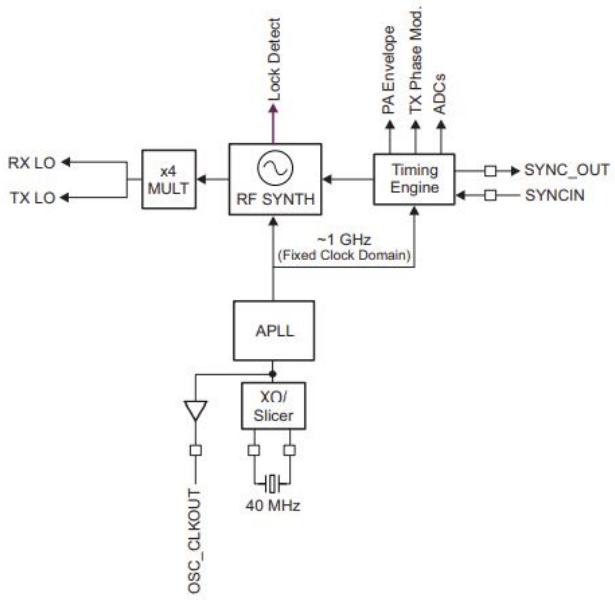

Figure 2.2: RF clock subsystem taken from AWR2944 datasheet[9]

The output signal generated from the RF clock subsystem goes directly to the "Transmit Subsystem"[9], here, it is amplified by the power amplifier and phase controlled for the transmission operation. The same signal is also sent to the "Receiver Subsystem"[9] that manages the down-conversion for getting the IF signal. The RX chain contains the LNA, the mixer, the Band-Pass filter, the ADC, and the decimation unit.
The Band-Pass filter supports a bandwidth up to 15 MHz[9].
Figure 2.3 and Figure 2.4 show the transmitting chain and receiving chain respectively that are implemented in the AWR2944 device.

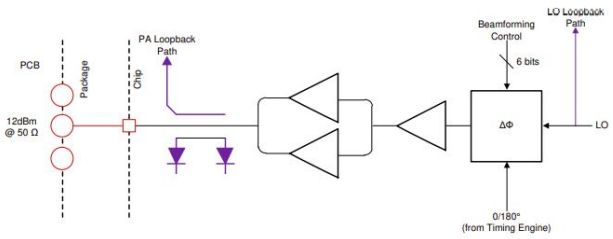

Figure 2.3: Transmit Subsystem taken from AWR2944 datasheet[9]

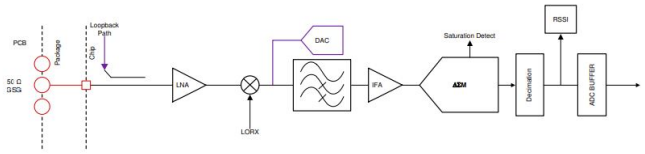

Figure 2.4: Receiver subsystem taken from AWR2944 datasheet[9]

2.1.2 Digital subsystem

The digital subsystem, which is shown in Figure 2.5, includes the Main Subsystem (Cortex-R5F processor), the Radio Processing Subsystem, the DSP Subsystem and other devices used for specialized function like the hardware accelerator and the interfaces for the peripherals.
The peripherals supported by the AWR2944 are:

- I2C
- JTAG
- UART
- SPI
- CAN-FD
- 10/100 Mbps Ethernet
- CSI2
- GPIOs
- QSPI

It is possible to notice that the chip includes a large number of peripherals that support high-speed protocols; the presence of these interfaces allows the chip to be used for high performance applications, enabling the possibility to run a complex algorithm and exchange a large quantity of data between different systems.

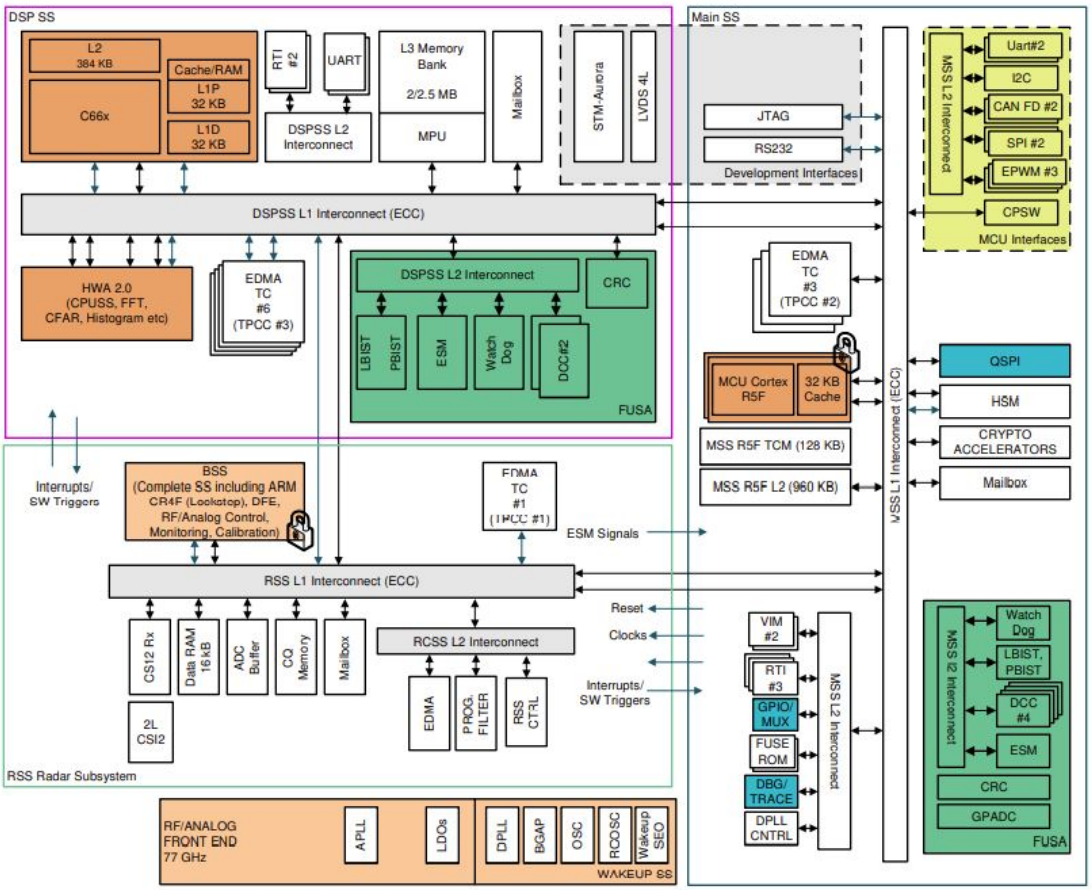

Figure 2.5: Digital subsystem taken from AWR2944 datasheet[9]

2.2 Chip Requirements

From the early stages of the hardware development, it is necessary to understand the requirements of each component inside the chip, especially for those which have a complex structure due to voltage and current constraints that could be quite stringent. Also the problem related to power dissipation must be taken into account from the beginning; a proper thermal dissipation of the chip ensures a long lifetime of the entire system.

This is a crucial factor that must be taken into account for the reliability of the product.
From the device datasheet[9], one can extract the information about voltages and currents for each power rail that must be ensured for a safe operation of the chip.

	MIN	NOM	MAX	UNIT
VDD VDD_SRAM VNWA	1.14	1.2	1.32	V
VIOIN	3.135	3.3	3.465	V
VIOIN_18 VDDA_18CLK VDDA_18PM VIOIN_18CSI VIOIN_18LVDS VDDA_18BB VDDA_18VCO	1.71	1.8	1.9	V
VDDA_10RF1 VDDA_10RF2	0.95	1.0	1.05	V

Table 2.1: AWR2944 recommended supply voltages from AWR2944 datasheet[9]

SUPPLY NAME	MAX	UNIT
VDD VDD_SRAM VNWA	2100	mA
VIOIN	50	mA
VIOIN_18 VDDA_18CLK VDDA_18PM VIOIN_18CSI VIOIN_18LVDS VDDA_18BB VDDA_18VCO	600	mA
VDDA_10RF1 VDDA_10RF2	2300	mA

Table 2.2: AWR2944 current consumption from AWR2944 datasheet[9]

Table 2.1 and Table 2.2 demonstrate how special care must be given while designing the supply chain; the first table points out that even a $\Delta V \approx 5\%$ deviation from the nominal value could be enough to cause the device to malfunction. The second table shows the maximum current consumed from each supply pin. These parameters affect largely the design of the supply chain due to the constraints introduced by the high current required and the small voltage deviation from the nominal values.

2.3 RF and Power Specifications

The performance of the chip is evaluated in this part to provide an overview of its features. The TX and RX system capabilities provide some helpful information regarding the accuracy that can be achieved in the final result.

PARAMETER		VALUE	UNIT
Receiver	Noise Figure	13	dB
	1-dB compression point	-11	dBm
	Maximum gain	44	dB
	IF Bandwidth	15	MHz
	ADC sampling rate	37.5	Msps
	ADC resolution	12	Bits
Transmitter	Output power	12	dBm
	Phase shifter accuracy	± 5	$^\circ$
	Amplitude noise	-145	dBc/Hz
Clock subsystem	Frequency range	76-81	GHz
	Ramp rate	250	MHz/μs
	Phase noise at 1-MHz offset	-95	dBc/Hz

Table 2.3: AWR2944 RF parameters taken from datasheet[9]

Table 2.3 summarizes the RF parameters of the AWR2944 chip.
As discussed above, high-performance devices dissipate a lot of heat during their working period; in general the power consumption is not constant, and it is based on many aspects of the actual operation of the chip, such as the number of digital blocks in use or the number of transmitting and receiving antennas that operate simultaneously. The power dissipated provided in the datasheet considers a scenario with 50% duty cycle and 70% CPU and DSP utilization; under these conditions the total consumed average power is about 2.25 W[9].

2.4 Differences with respect to AWR1843

The capabilities and requirements of the second-generation RADAR chip have been discussed in this second chapter. Nevertheless, it is important to highlight the differences with respect to the first-generation device in order to have a clear idea of the major improvements introduced by the AWR2944.
The differences between the two chips are highlighted below.

- The main improvement is given by the introduction of the fourth transmitting antenna. MIMO technique benefits from this major enhancement by making possible an overall performance increasing. Assuming a number of receiving antennas in azimuth equal to N_{RX}, an extra transmitting antenna implies an additional N_{RX} factor to the virtual array, which increases the angular resolution. However, another use of the additional TX antenna is in the implementation of a RADAR system which is capable of both short and long range applications. In this thesis project, TX1 and TX2 have been used for the short range RADAR application with elevation estimation; instead, TX3 and TX4 have been used for the long range RADAR application.
- A larger on-chip memory with a 4 MB storage capacity.
- The maximum IF frequency is increased to 15 MHz, which is related to an increase of the maximum sampling rate up to 37.5 Msps. This major change is due to the presence of the real sampling process instead of a complex one in the new device.
- A 1 dB lower Noise Figure than the AWR1843.
- A higher slope of the chirp transmitted signal than the AWR1843, which is equal to 250 MHz/μs in the new device.
- On the receiver side, the maximum gain and the gain range are reduced by a factor of 4 dB.
- The introduction of high-speed communication interface modules such as Ethernet or Aurora LVDS.
- The introduction of specialized Hardware Security Module.
- The package occupies a larger area of about 2.89 mm^2 than the previous generation chip.

Chapter 3

System Design

This chapter describes the design and the selection of the electronic components that have been used in the developed system, providing a detailed analysis of their usage. It details each aspect of the design starting from the system schematic.
Since the designed system is an upgrade of the previous version which embeds the AWR1843 chipset, as indicated in Section 2.4, some elements of the previous project have been re-used.
Nevertheless, Texas Instruments distributes the design files of the AWR2944EVM evaluation board project[10], which has been used as a reference design for the changes that have been made to the original board.

3.1 System Overview

The top level view of the AWR2944 system is introduced to emphasize the main blocks of which it is composed. Each block is described in depth in the following sections to offer the necessary knowledge about its use in this project.

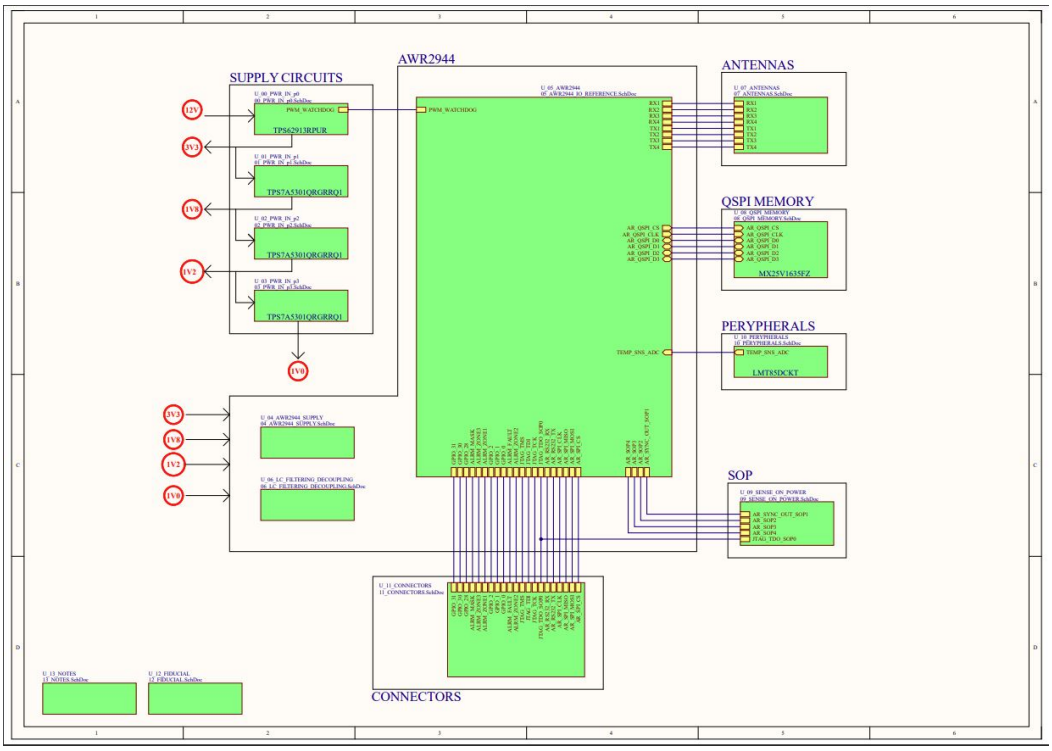

Figure 3.1: AWR2944 top-view schematic

A top-view of the entire system is shown in Figure 3.1. The system is composed of seven main blocks, which are described below.

- The supply chain block is utilized to supply the chip with the required voltages
- The AWR2944 block contains everything related to the chip such as:
  - Supply pins
  - Decoupling capacitors
  - Filtering circuitry
  - Interconnects for I/O operations
- The antenna block

- The QSPI Memory block
- The peripheral block contains the external peripherals that can be attached to the chip for additional operations, in this project a temperature sensor has been included.
- The Sense On Power circuitry is mandatory to configure the device with the proper functionality when the system boots
- The connector block in which the JTAG and the main connector are included to handle the communication with external systems and to provide the 12V DC input voltage to the system

3.2 Supply Chain

The AWR2944 chip requires four voltage levels for the correct powering. These voltages have been provided through a cascade of four DC-DC converters from the 12V DC input voltage. This solution is taken directly from the previous version of the circuit since the new chip requirements are respected. The reference design recommends the use of the LP87745 integrated circuit, which embeds four DC-DC converter in order to provide the needed voltages at the same time. The unavailability of this chip made that solution not suitable for this work. The solution that has been exploited in the design is shown in Figure 3.2.

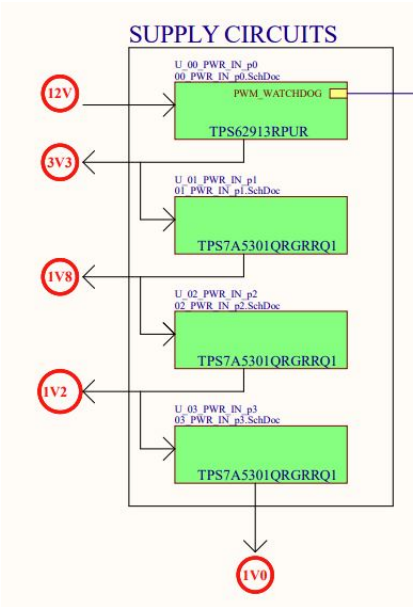

Figure 3.2: Top-view supply chain

3.2.1 12V to 3.3V Conversion Circuit

The 12V DC input voltage is converted to the 3.3V by means of a Buck converter; the large difference between the input voltage and the output voltage makes the choice of the switching converter suitable for this purpose.
The TPS62913[11] device developed by Texas Instruments has been used for this conversion. This IC regulates the output voltage exploiting low noise and low ripple techniques, making it compliant for applications which are sensitive to noise.
However, this device supports an output voltage ripple attenuation of about 30 dB when a second stage LC filter is used. The voltage ripple attenuation can be reached by adding a Ferrite Bead to the Buck converter output; the device embeds an integrated loop compensation for obtaining the correct output voltage level due to the presence of this filter. The schematic associated to this conversion block is shown in Figure A.2 in Appendix A.

In the following table the parameters of the used switching converter are summarized.

PARAMETER	VALUE	UNIT
Input voltage range	3.0 to 17	V
Output voltage range	0.8 to 5.5	V
Output voltage accuracy	± 1	%
Output current	3	A
Output voltage ripple (after ferrite bead)	< 10	μV_{RMS}
Power Supply Rejection Ratio	> 65	dB

Table 3.1: Buck regulator parameters taken from datasheet[11]

These parameters match the AWR2944 requirements, especially when the maximum output current of the converter is considered, which is enough to satisfy the required current from the RADAR chip.
According to the datasheet, the following components have been selected for its implementation. At the input pins there is a total of three capacitors (Figure 3.3). Two 10 μF bulk capacitors provide the filtering of the input voltage required to reduce the ripple and the spikes; after them, there is a small 2.2 nF capacitor used for the decoupling and to reduce the loop parasitic inductance.

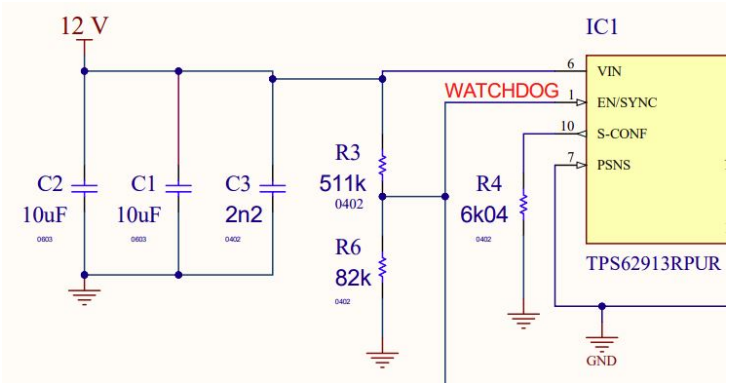

Figure 3.3: Buck converter input capacitors

The device has been configured to work with a switching frequency of 2.2 MHz together with the Spread Spectrum function enabled in Triangle Mode. This functionality allows to spread the noise produced by the switching frequency within a larger bandwidth reducing the peak amplitude. To enable this function a 6.04 $k\Omega$ resistor has been connected to the S-CONF pin.

A 470 nF capacitor has been connected to the NR/SS pin. This arrangement allows to reduce the low frequency noise and to set the soft-start time. The selected capacitor value provides a startup time of about 5 ms.

Since the device has been configured for the Low Ripple/Noise design goal, the following components have been employed.
At the device output there is the main inductor used for the conversion, as shown in Figure 3.4. Its value is fixed to 2.2 μH due to the selected switching frequency. In addition to the inductor, three 2.2 nF capacitors have been connected after it for the first filtering.

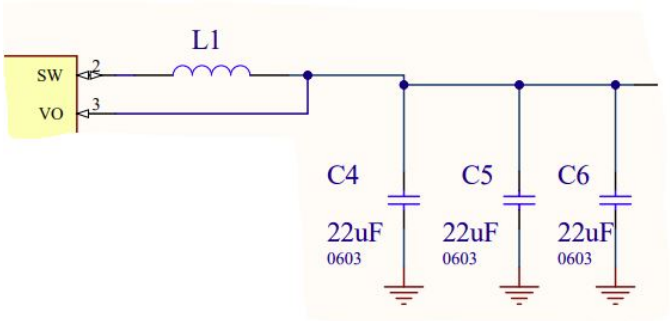

Figure 3.4: Buck converter first output LC filter

The additional filtering step, which is shown in Figure 3.5, has been achieved by utilizing a Ferrite bead mentioned before, which provides the second LC filter for further ripple and noise reduction. The buck converter datasheet informs that the chip stability is ensured with a Ferrite bead inductance less than 50 nH; for this reason, the Ferrite Bead that has been chosen has a maximum impedance at 100 MHz that is less than 31 Ω.

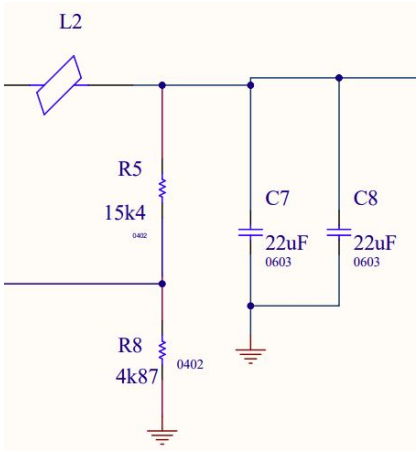

Figure 3.5: Buck converter second output LC filter

Since the Ferrite bead introduces a DC resistance, particular attention has been paid on this component. As shown in the Figure above, the feedback pin of the buck converter has been connected to the voltage divider from the output of the second LC filter, this provides for the voltage regulation considering also the voltage drop due to the Ferrite Bead parasitic resistance.
For the voltage divider, two resistances with 15.4 $k\Omega$ and 4.87 $k\Omega$ values have been employed to provide the 3.3V regulated output voltage.
After that, the output stage has been filtered with two additional 22 μF capacitors according to the datasheet recommendation.

The chip supports the "Enable" function, when it is asserted, the device starts supplying the output voltage; otherwise, it shuts down. When it is required, the enable pin is pulled down by a transistor that is connected to the output of a 14-stage digital counter which provides the shutdown of the supply rail. The latter can be driven by the PWM_WATCHDOG signal controlled by the RADAR chip, if programmed, or it can be bypassed by pulling the CLEAR pin to 5V by shorting the P1 connector. The supply voltage for the counter circuit has been provided by a low-cost step voltage regulator that convert the 12V input voltage directly to the required 5V. The default frequency of the counter has been set by the RC circuit connected to CLKO and $\overline{CLKO}$; a 10 $k\Omega$ resistor and a 0.01 μF capacitor

have been chosen to provide a 4kHz clock signal. With this frequency, the most significant bit is triggered after 4 seconds if the CLEAR pin is not pushed to a high logic value. The reset counter is present in the same schematic of the buck converter as shown in Figure A.2.

3.2.2 3.3V to 1.8V, 1.8V to 1.2V and 1.2V to 1.0V Conversion Chain

The second part of the supply chain is composed by a cascade of three stage LDO; each LDO provides the required supply voltages for the chip.
The Low-dropout voltage regulator that has been used for these conversions is the TPS7A53-Q1[12] chip developed by Texas Instruments. It is designed with the automotive grade, and it is suitable for supplying sensitive electronic components due to its high accuracy, low noise, high PSRR features.
Some of the main LDO features are summarized in Table 3.2.

PARAMETER	VALUE	UNIT
Input voltage range	-0.3 to 7.0	V
Output voltage range	-0.3 to V_{IN}+0.3	V
Output current	3	A
Dropout voltage (max) with BIAS and I_{OUT}=3A	180	mV
Output voltage noise	4.4	μV_{RMS}
Power Supply Rejection Ratio at 500 kHz	40	dB

Table 3.2: LDO parameters taken from datasheet[12]

Since these conversion circuits utilize the same voltage regulator chip, their schematics are similar; the only difference lies in the voltage divider resistors values, which have been selected to set the correct output voltage for each power rail.
For this reason, the schematic in Figure A.3 is considered as example for the following analysis. Some differences with respect to the others conversion circuit schematic are pointed out later in this section.

Figure 3.6 represents the basic circuit schematic of an LDO. The output voltage is regulated by selecting the correct resistors in the feedback path, which is composed by the op-amp and the voltage divider. For each supply chain, the value of the resistors has been calculated using the following formula.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad [V] \tag{3.1}$$

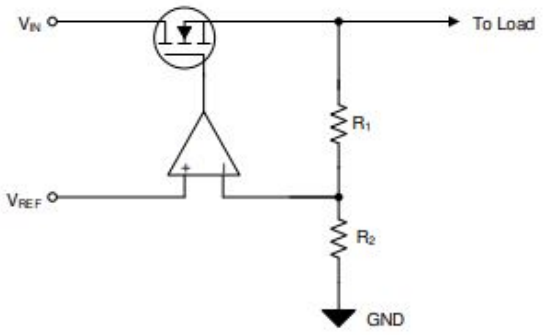

Figure 3.6: LDO simplified circuit schematic[12]

Table 3.3 provides the list of the feedback resistors that have been used in the LDO stage design for setting the regulated voltage.

OUTPUT VOLTAGE	R1	R2	UNIT
1.8 V	12.4	10	$k\Omega$
1.2 V	12.4	24.9	$k\Omega$
1.0 V	12.4	49.9	$k\Omega$

Table 3.3: LDO feedback resistor values

At the LDO input there are three capacitors with the following values $0.1\mu F$, 1 μF and 10 μF. They are essential to provide further input voltage stabilization in a large frequency spectrum. Figure 3.7 shows the implementation from the schematic point-of-view of the input capacitors.

Additional capacitors have been employed for the correct device operation.

- Noise Reduction/Soft start capacitor (NR/SS): a 10 nF capacitor has been used for low frequency range reduction and for setting the starting time of the LDO output, which is about 1.2 ms. This is also the recommended value for low-noise application.
- Feed-forward capacitor: a 10 nF capacitor has been used for the mid-band frequency range reduction and PSRR improvement, it has been connected between the output supply rail and the feedback pin.
- Output capacitors (Figure 3.8): a set of 47 μF, 22 μF and two 10 μF capacitors in parallel that provide high frequency range reduction.

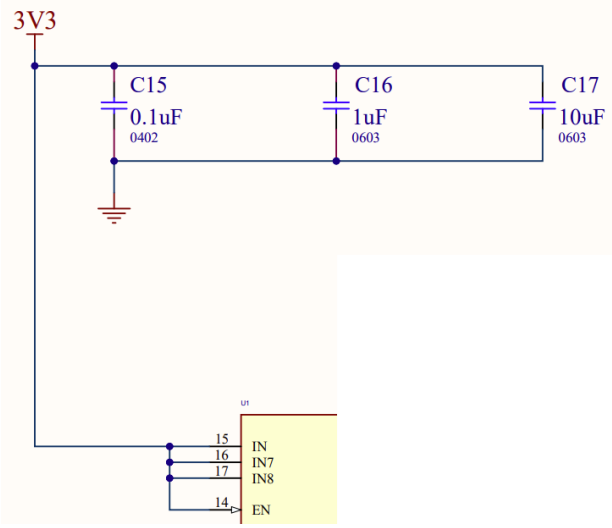

Figure 3.7: 3.3V to 1.8V conversion input capacitors

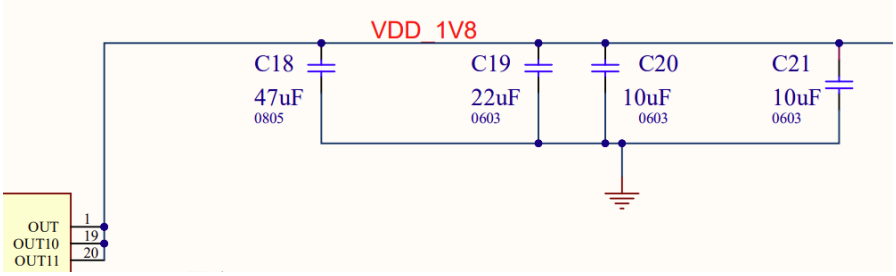

Figure 3.8: 3.3V to 1.8V conversion output capacitors

The same arrangements have been used for the 1.2V and 1.0V conversion chains. The difference lies in the BIAS pin. Due to the low input voltage level, the voltage regulator has no sufficient headroom to respond to the noise. So the bias input helps to mitigate this problem providing a higher voltage level for the internal regulation circuit. The BIAS pin has been connected to the 3.3V rail with a 10 μF capacitor.
The output of the three regulated LDOs has been filtered by a three-terminal feedthrough capacitor. This solution increases the EMI robustness on supply rails, however, the high frequency components that can be injected into the power rails will be suppressed.

3.3 AWR2944 Schematic

After the supply chain design, the AWR2944 schematic part is addressed in this section. The interconnections to the supply pins and to peripherals are discussed below.

The schematic in Figure A.6 shows the connections between the reference voltages to the corresponding chip pins.

Figure A.7 shows the schematic for the interconnections between the chip and the peripherals attached to it.
A 40 MHz oscillator has been used to produce the external clock reference signal for the device. Together with it, a couple of 4.7 pF capacitors have been connected to both CLKP and CLKM pins of the device.

The "Warm Reset" is an open drain signal which is used when the device goes through the reset state. The reset state can be asserted by pulling down the pin associated to this function due to the active low pin. To force the manual reset, a switch has been connected to this pin and a LED has been inserted to indicate whenever this event occurs.

"ERROR_OUT" is an open drain output pin, when it is pulled down means that a critical error in the AWR2944 system happened. To restore the chip functionality a reset event as indicated previously must occur. This output pin has been connected to a LED for a visual indication.

The Sense On Power pins configure the desired boot mode and they are used only when the chip startup. After the boot of the RADAR chip, these pins can perform different functions as shown below.

- TDO (pin D15) for SOP0
- MSS_MIBSPIB_CS2 (pin R14) for SOP1
- PMIC_CLKOUT (pin T17) for SOP2
- MSS_UARTB_TX (pin A14) for SOP3
- MSS_UARTA_TX (pin C16) for SOP4

The different meaning of each SOP combination is described in Table 3.4 and Table 3.5.

SOP(2)	SOP(1)	SOP(0)	MODE
0	0	1	Functional QSPI load mode
1	0	1	UART load mode
0	1	1	Debug and development mode

Table 3.4: SOP bootmode

SOP(4)	SOP(3)	XTAL CLOCK MODE
0	0	40 MHz
0	1	45.1584 MHz
1	0	49.152 MHz
1	1	50 MHz

Table 3.5: SOP reference crystal frequency selection

The other interconnections regard the communication interfaces that are used to establish the communication with the external systems.
For this project the protocols that have been embedded are the following:

- RS232/UART
- SPI
- QSPI
- JTAG

The RS232/UART and JTAG interfaces are used for the debug purpose. Two SPI interfaces have been included in the design; even if they are not directly used in this thesis work, they will be meant to handle high-speed communication for future applications. The communication between chip and memory is handled by the QSPI interface.

3.4 Supply Filtering and Decoupling

One of the major concerns in hardware design is in the providing of a clean path for the chip power supply pins from the output of the DC-DC converters. However, the switching regulator can introduce noise in the board, for this reason, particular attention has been payed to filter the unwanted noise in the power rails. Schematic in Figure A.8 illustrates the two required filtering parts, the one on the left helps

the power rails to comply with EMI, the part on the right collects the decoupling capacitors used for the AWR2944 device power pins.
The switching activity of the buck regulator could introduce unwanted spikes at the frequency where it operates as well as at its harmonics. The priority is to eliminate those spikes in order to keep the power rail as clean as possible and reduce the overall noise level in order to preserve the functionality of the sensitive chip internal circuitry.
The 3.3V filter has been performed by employing a series 1 μH inductor, two 22 μF shunt capacitors and other two 10 μF shunt capacitors. This arrangement creates a low-pass LC circuit in which the DC path is not influenced by the filtering process, instead, higher frequency signals are attenuated.

At low frequency, the inductor seems transparent and the signal passes through it; however, if the signal frequency increases, the impedance associated to the inductor increases as well. This is why the inductor ideally stop high-frequency components without disturbing the DC component.
Capacitor behaves inversely with respect to the inductance. Ideally, a sinusoidal signal at high frequency will pass without being attenuated; instead, the DC or the low frequency components are attenuated. Meaning that the impedance of the capacitor decreases if the frequency of the signal through it increases.
A simulation on this filter chain has been performed using the LTspice XVII simulation tool[13]. The test circuit presented in Figure 3.9 is composed of the elements that have been described above. The circuit output has been connected to a 50 Ω resistive load and then the frequency behavior has been analyzed.

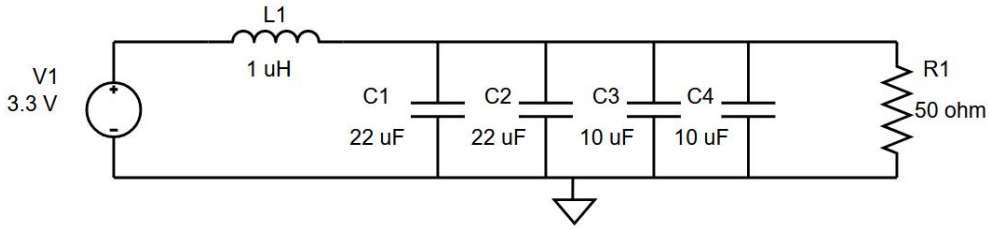

Figure 3.9: 3.3V rail filtering

The first analysis has been carried out with ideal components and the result of the simulation is shown in Figure 3.10. Using ideal components the analysis does not represent the real filter behavior; but it is useful as a first approximation. The transmission coefficient, the impedance of the inductor and the impedance of the 22 μF capacitor versus frequency are displayed below in a range from 100 Hz to 1 GHz. The axes are in logarithmic scale.

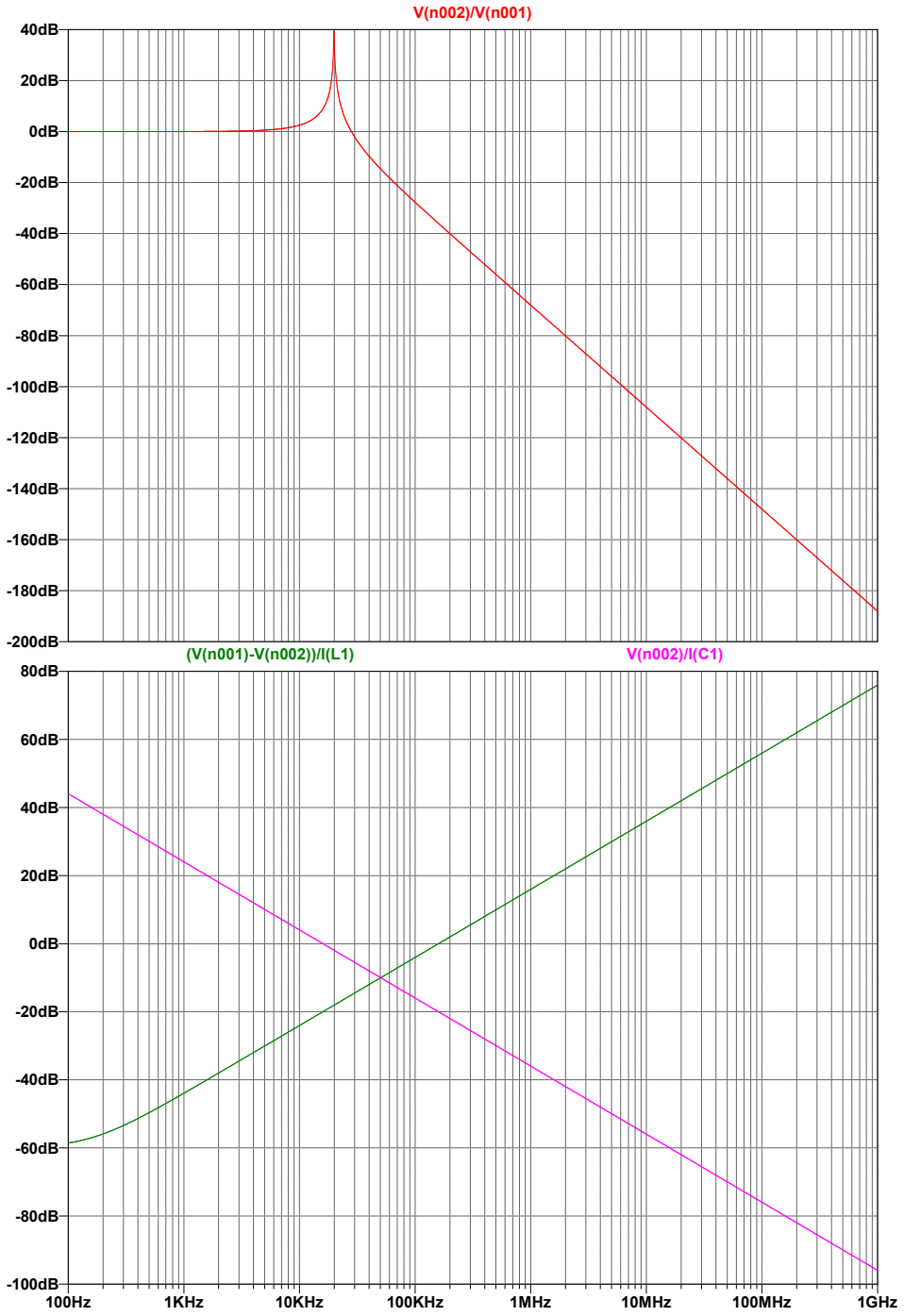

Figure 3.10: 3.3V rail filtering simulation with ideal components

The green curve shows the inductance impedance variation, instead, the purple curve shows the capacitor impedance variation.
The graph also shows the voltage attenuation in dB that it is possible to get at the filter output. This demonstrates that, a spike voltage at the switching activity of 2.2 MHz has an attenuation of about 80 dB. The peak that appears at 20 kHz is related to the resonance between the inductance and the capacitors.

In this kind of analysis, the equivalent model of the used elements should be used to have a good idea of the actual behavior of the circuit. The figure below shows the equivalent models for the inductor and the capacitor with their corresponding parasitic elements. A real inductor has a capacitive element that became predominant at high frequencies. And the same happens in the real capacitor, its inductive behavior became predominant at high frequencies.

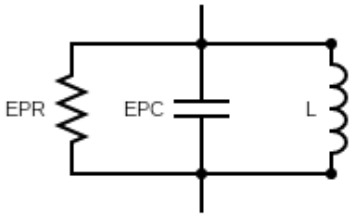

Figure 3.11: Inductor equivalent model

Figure 3.12: Capacitor equivalent model

The presence of the parasitic elements in the real components make the resulting behavior different with respect the ideal one. The equivalent Spice models of the devices have been taken from the website "SimSurfing"[14] created by muRata. These components have been substituted in the previous test circuit and the analysis has been redone.
The same results as in the previous analysis are represented in Figure 3.13.
The transmission coefficient trend change slightly, but the peak at 20 kHz is lowered; the attenuation at 2.2 MHz remained almost the same.
This LC circuit arrangement has been utilized for the other 1.8V and 1.2V filtering chains.

Figure 3.13: 3.3V rail filtering simulation with real components

A different filtering stage has been adopted for the 1.0V rails that supply the RF part of the chip due to the presence of particular noise sensitive electronic components in it. As a result of this, the series inductance has been replaced with a ferrite bead with 33 Ω at 100 MHz, corresponding to a value of inductance of 53 nH. The output voltage of this chain is shown in Figure 3.14. It exhibits a significant attenuation at high frequencies; however, the 3 dB attenuation starts at 100 kHz and continues to be under this value at the higher frequencies also.

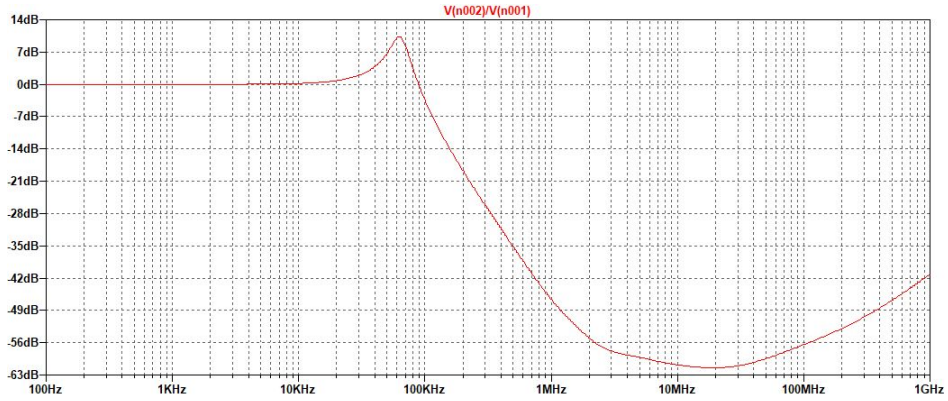

Figure 3.14: 1.0V rail filtering simulation

The decoupling part is another main aspect in any digital or analog circuit in order to work properly.
During typical application execution, each sub-circuit or component inside the chip sinks from the power rail a certain amount of current. For example, a digital CMOS circuit sinks current based on its switching activity, and in general this is not a constant parameter. When this occurs, a voltage drop on the supply rail caused by the existence of parasitic inductance on the path can happen. If the parasitic inductance is not negligible, this implies that the voltage on the power rails collapse and the usable voltage across the device decreases. Furthermore, switching noise fed directly into the power path can disturb other subsystems connected to the same supply network. The use of a decoupling capacitor provides the amount of charge required by the chip pin during its switching activities and decouple the presence of a component with respect the other ones. To limit the problem of rail collapse, the parasitic inductance introduced by the return path must be avoided through these capacitors.
Ceramic capacitors are commonly employed for decoupling due to their low ESR (equivalent series resistance), which optimizes the decoupling process. Also small packages help due to their low ESR and low ESL (equivalent series inductance) values.

The selection of these capacitors depends on the pin that must decouple, the size of these must be chosen depending from the quantity of charge required.
The decoupling capacitors have been embedded on the board considering the evaluation board reference design, these are represented in Figure A.8 on the right side of the schematic grouped by voltage level.

3.5 Peripherals Schematics

After the design of the core system and its supply network, the peripheral schematics are now taken into account.

The antenna schematic shown in Figure A.9 depicts the four transmitting antennas and the four receiving antennas which have been employed in the system. The latter group of antennas includes also dummy elements that surround the active ones in order to prevent problems related to the mismatching.

The Figure A.10 shows the implementation of the MX25V1635FZ 16 M-bit external memory in the system, which is the same as the previous project. It requires a 3.3V as supply voltage; also two decoupling capacitors have been used for this power pin for stabilizing the supply voltage. The QSPI interconnections are connected directly to the AWR2944 QSPI interface in the IO schematic.

The Sense On Power circuitry schematised in Figure A.11 shows the employed solution for the bootmode configuration. The two functionalities that have been used for this application are that one corresponding to the flashing mode (101) and to the functional mode (001). SOP0 has been fixed to high level voltage with a pull-up resistor and SOP1 also has been fixed to the low level voltage by means of a pull-down resistor since they do not change between the configurations discussed above. SOP2 can be modified according to the required mode thanks to a switch. SOP3 and SOP4 have been connected to ground in order to have the frequency selection fixed to 40 MHz.

The LMT85DCKT temperature sensor has been used in the system (Schematic A.12). Its output is connected to the AWR2944 general purpose Analog-to-Digital converter for the temperature measurement.

The schematic in Figure A.13 shows the presence of the connectors used on board. The connector on the top is used for the external 12V DC supply, UART interface, SPI interface, GPIO and other signals. The bottom one is used for the JTAG interface.

Chapter 4

Board Development

This chapter describes the layout development of the AWR2944 RADAR board which embeds the system analyzed previously. As aforementioned, due to the presence of high-speed interconnections and Radio Frequency components, the printed circuit board must comply several design constraints in term of Power and Signal Integrity. The following sections analyze the choices that have been made starting from the selection of the correct materials for the used stackup to the design of each plane and trace of the final layout. The followed strategies for the analog, digital, and RF parts are described in the sections below.
The PCB design has been developed using Altium Designer[15] CAD tool created by Altium. This professional PCB design tool allows to have the control of the entire project, and it has been utilized in all the layout stages.
However, in order to develop a board that works properly and optimized for RADAR application, Texas Instruments distributes the hardware design checklist[16], in which there are some useful layout strategies for the development stage.
In the final part of this chapter, a Power Integrity analysis has been performed in order to understand the supply networks behaviour within the final layout.

4.1 Board Stackup

The starting point of each PCB design is always the selection of the stackup. The stackup is the collection of different materials that are stacked one on the other to create the final board. A fine selection of these materials, and a good layer planning are the key factors to create a well functioning board.
This step is important not only for the functionality of the design, but also for the board cost, which is highly related to the materials used in the stackup.

Before starting the analysis of the designed stackup for this project, the PCB manufacturing process is reported due to some aspects of it are useful in order to understand the choices that have been made.
The laminate and the prepreg materials are the fundamental layers that are used to create the structure of the board; the former contains the dielectric layer in the middle, and on both sides, it is entirely covered with copper. Each laminate contains two copper layers. The latter contains the dielectric material with resin only, and it is used as a "glue" layer between two laminates.
PCB industry usually works with standard laminate and prepreg layers, in fact, manufacturers provide the datasheet in which the available materials together with their physical parameters are reported.
The dielectric layer that is present in both laminate and prepreg has the same construction, it is a composition of fiber glass woven and epoxy resin. The epoxy resin allows the stacking of more laminate one on the top of the other.
In this way, starting from the inner layers to the outer ones, a multi-layer board can be manufactured.
The development of each board layer is achieved exploiting the following procedure. Both sides of the laminate are covered with the photoresist, then the layer is exposed to UV light covered with the layer mask that contains the trace or plane pattern of the corresponding layer. The unhardened resist is removed to perform the etching of the unwanted copper and the remaining photoresist is removed. Both sides of the laminate are developed at the same time. Then, the developed layers and prepreg are stacked together in a process called "lamination" process.
After that, the Through-Hole VIAs are created to connect electrically different layers.

The board in this project has been designed with a six-layers stackup, which is the same used in the previous version of the board due to its good performance. Texas instruments point out a possible solution using eight layers. That solution has not been used due to the chosen stackup provided sufficient room to meet the routing requirement without making the board cost excessive.

A properly designed stackup helps to control five board parameters:

- Impedance control
- Crosstalk
- Interplane capacitance
- Loss
- Skew

Each of this parameter inherently belongs to the Power Integrity and the Signal Integrity of the board.
The layout stackup can influence the way how the reference voltages and signals behave in the system; for this reason, the definition of the different layer placement must be carefully considered from the beginning.
The layer arrangement used for this work is similar to the Model 2 presented on page 10 in this article [17] published by Texas Instruments. As stated in the article, the chosen six-layers stackup has good performance in terms of decoupling, EMC and Signal Integrity. The detailed stackup that has been used in this project is shown in Table 4.1.

	LAYER NAME	MATERIAL	TYPE	THICKNESS
1	Top	Copper	Signal	0.035 mm
	Dielectric 1	ROGERS 3003	Laminate	0.127 mm
2	RF GND	Copper	Plane	0.018 mm
	Dielectric 2	IS400 2116	Prepreg	0.119 mm
3	PWR1/SIG	Copper	Plane/Signal	0.018 mm
	Dielectric 3	IS400 5x7628	Laminate	0.991 mm
4	PWR2	Copper	Plane	0.018 mm
	Dielectric 4	IS400 2116	Prepreg	0.119 mm
5	GND/SIG	Copper	Plane/Signal	0.018 mm
	Dielectric 5	IS400 1x2116	Laminate	0.102 mm
6	Bottom	Copper	Signal	0.035 mm

Table 4.1: Board stackup

4.1.1 Material Selection

This section addresses the choice of the selected materials in the stackup showed above. The board stackup has been developed using three laminates and two prepreg layers. Table 4.2 reports the used materials and their physical characteristics. The materials characteristics data have been taken from ROGERS and ISOLA manufacturers.

MATERIAL	ϵ_r @ 10 GHz	tan(δ) @ 10GHz	RESIN CONTENT
ROGERS 3003	3.0	0.0010	NA
IS400 2116	4.12	0.0226	53%
IS400 5x7628	4.32	0.0201	45%
IS400 1x2116	4.05	0.0191	54%

Table 4.2: Materials parameters taken from manufacturers datasheet

The usage of the ROGERS 3003 laminate has been dictated due to its high-quality and excellent properties in Radio Frequency applications. This laminate has been selected for the first dielectric layer in order to handle as best as possible the RF part of the system which is positioned on the top layer of the board.
The ROGERS 3003 is characterized by low relative dielectric constant ϵ_r and low tan(δ) in a very large frequency spectrum. However, datasheet reports that their deviation from the nominal values, in a frequency range from 8 GHz to 40 GHz, can be considered negligible. This material characteristic helps to limit the problem of dispersion.
The possibility to employ a material with low dielectric constant and low dissipation factor reduces the losses during signal propagation related to the "Skin effect" and the energy dissipation into heat. This is why PTFE-based material as ROGERS 3003 is highly recommended when dealing with high frequency components. In the case of the 77 GHz antennas and their interconnections this material proprieties are essential.

For the remaining layers, the IS400 laminates manufactured by ISOLA have been used due to their good characteristics without being too expensive. These materials are characterized by a high reliability thanks to the excellent thermal performance. They are recommended for high-speed designs, and the manufacturing process is FR-4 compatible.

4.1.2 Layers Arrangement

The layer arrangement described in the following considers the proper component, interface interconnections, and power planes positioning on each layer using the stackup defined in Table 4.1.

On the top layer, the AWR2944 chip, the antennas, and the Buck converter for the 12V to 3.3V voltage conversion have been mounted.
The buck converter circuitry has been placed distant from the RADAR chip and the antennas in order to prevent them from the switching noise.
The patch antennas occupy the upper part of the top layer. Since very high frequency signals must propagate through them and their interconnections, the layer immediately below has been occupied by a solid ground plane for a better impedance control and insulation. The interconnections that connect each antenna to the relative chip pin act as a transmission line, meaning that a lot of care must be paid during their design.
The second layer has been filled with a solid ground plane as stated before for the following purposes; it must guarantee a reference plane for the traces positioned on the top layer ensuring a good impedance matching, and it separates the RF part from the analog and digital ones acting as a shield for the former. This is called "RF ground" layer. Since the analog or digital noise that can be injected into this ground plane could interfere directly with the high frequency components, the majority of the ground VIAs used by the voltage regulators or by the decoupling capacitors are not connected to this plane.
The layer three has been used for power planes and critical high-speed signal routing. In particular, on this layer there are the 1.2V supply rail and the 3.3V reference voltage, the latter is delivered by a thick trace toward the chip power pins to reduce the DC resistance and to comply with the current requirement. Also the SPI traces are routed on this layer due to the good return path ensured by the solid upper reference plane.
The fourth layer has been used for the power planes only. The supply planes on this layer carry the 3.3V, the 1.8V and the 1.0V reference voltages. On this level, the 12V plane is also present, which is connected to the input connector. The unused space on this layer has been filled with ground plane.
The fifth layer is mainly composed of the ground plane for the analog and the digital components mounted on the board. The ground plane on this layer must be as clean as possible from cuts in order to minimize the return current path. Whenever a signal trace is routed on the board, it is necessary to know how its return path behaves. Poor consideration on the return path leads to an increase in the loop area taken from the current which determines a loop inductance increasing. As consequence of this, issues related to EMI and ground bounce can arise. Considering

either DC or AC return currents, they take always the lowest impedance path to the ground. If the return path is not uniform, the return current can spread unpredictably generating noise coupling with other traces; the result of this is the noise interference that determines Power and Signal integrity problems in the layout. The JTAG interconnections that have been routed on this layer occupy only a compact portion of this plane in order to maintain the ground plane intact. In the bottom layer there are the decoupling capacitors for the supply of the RADAR chip, the LDO regulator circuitry, the QSPI memory and the external connectors.

4.2 Board Layout

There are infinite possibilities to make a board layout, but some solutions are more effective than other ones. A lot of attention has been paid to how the components are positioned and connected together.
This section focuses on the board layout decisions that have been made, and it provides insight into each component present in the system.
In the following, there are three separate aspects which have been dealt with. The analog part includes the placement and routing of the voltage regulators described in Section 3.2, the digital part includes the routing of the communication interfaces, and the RF part concerns the antenna placement and the characterization of their transmission lines.

4.2.1 Analog Part

The circuitry for the first conversion has been positioned on the right side of the top layer, that is shown in Figure B.1. It comprehends the following components: the Buck converter and the input/output filters for regulating the voltage.
The switching converter layout has been the first concern when this board layout has been started. Due to the high switching activity, the noise produced can create unwanted effects if not properly managed.
The TPS62913 datasheet[11] illustrates some useful hints that have been followed during the layout.

- The input and output capacitors have been mounted as near as possible to the device. Their ground reference pins have been connected to the same ground plane of the device.
- The switching inductance has been positioned as close as possible to the device, and the copper area at its input has been minimized in order to avoid capacitive coupling.

- The feedback trace has been routed as short as possible, this increases the voltage regulation effectiveness.
- The ferrite bead placement has been avoided inside the keep-out region.
- The voltage divider for the output voltage sensing has been kept sufficiently near to feedback pin.

Figure 4.1 depicts the implementation of the Buck converter layout.

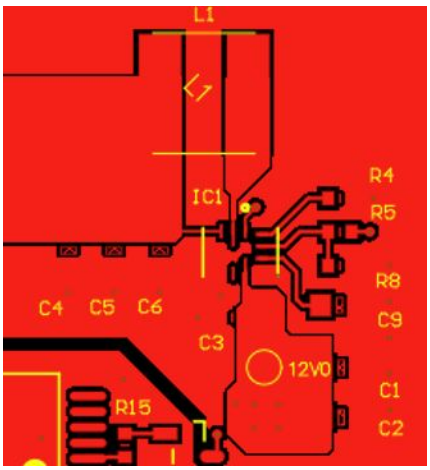

Figure 4.1: Buck converter layout

The analog ground plane that surrounds the switching regulator has been separated with respect to the other ground plane, preventing switching noise from spreading. Then, the second LC filter has been positioned immediately after the previous stage as shown in Figure 4.2.

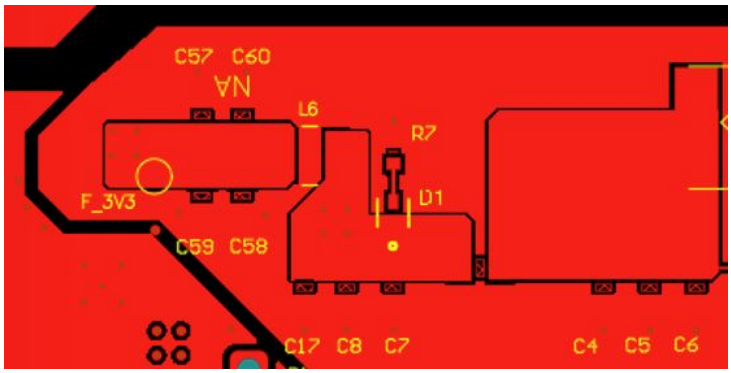

Figure 4.2: Buck filtering stage

The analog part incorporates the layout of the LDO chain, also in this case the optimized layout present in the datasheet has been utilized as reference.
This electronic component is not crucial in terms of noise because no high frequency switching signal is employed during its functioning. However, the usage of LDO is useful to spread the noise over a large bandwidth. Making the noise effect less critical. The following arrangements have been used:

- The components which compose the LDO circuity have been mounted on the same layer of the LDO chip, and as near as possible to their corresponding chip pin.
- The input and output capacitors refer to the same ground layer, and they have been mounted as close as possible to the chip pins for reducing the loop inductance.
- Each LDO ground plane has been separated with respect to the others LDO ground plane positioned on the bottom layer.
- A uniform ground layer below the chip has been ensured for better heat dissipation, and for shielding it against the noise.

Figure 4.3 shows one of the three LDO layout presents in the AWR2944 board.

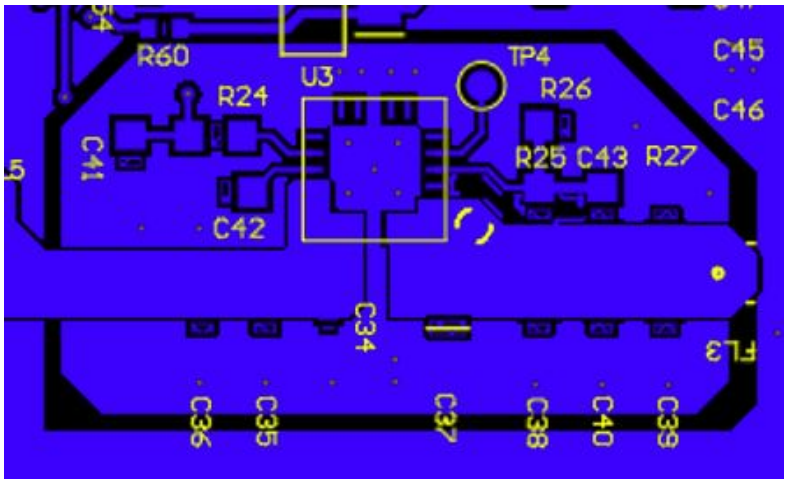

Figure 4.3: LDO layout example

To limit the danger of noise coupling between power planes, a spacing of 0.5 mm between them has been ensured. It is possible to notice in Figure 4.4 the power plane separation that has been utilized on the fourth layer.

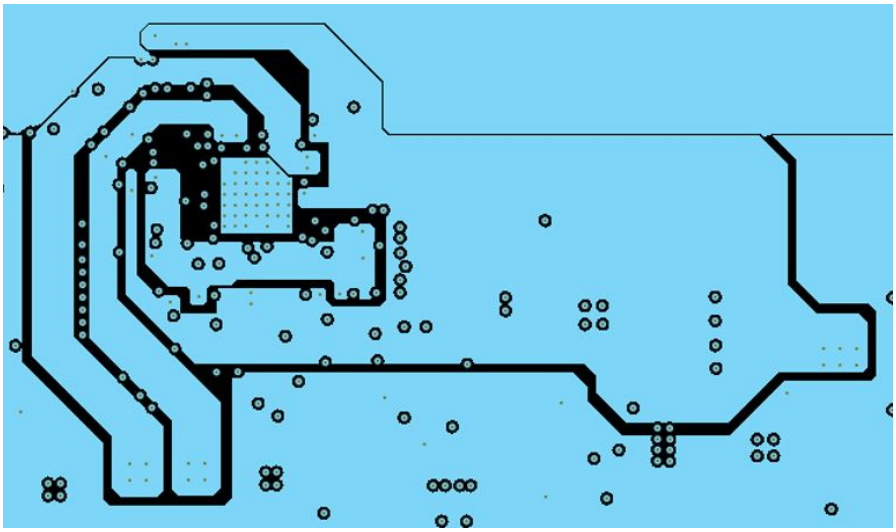

Figure 4.4: Power planes layout on the fourth layer

Particular care has been taken during the placement of the decoupling capacitors. The positioning of these components is a crucial factor, they must be as near as possible to the chip pins that must decouple. The correct arrangement avoids the introduction of the extra parasitic inductance, which can reduce the effectiveness of the decoupling. For this reason each capacitor has been positioned on the bottom side of the board, immediately below the chip pin.
Figure 4.5 shows the AWR2944 chip decoupling capacitors placement.

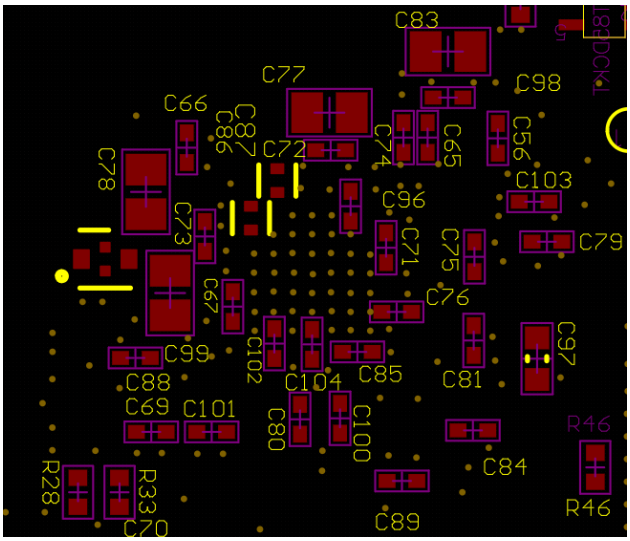

Figure 4.5: Decoupling capacitors placement under the AWR2944 chip

4.2.2 Digital Signal Part

Section 3.3 summarizes the digital communications that have been used in this project. Some layout considerations about the interface interconnections have been taken into account in order to get a signal that well propagates from the transmitter to the receiver and vice versa. Whenever the frequency of the signal increases toward high value, the trace in which the signal propagates does not act as an ideal connection; the correct model that should be used is that one related to the transmission line. The transmission line behavior is dictated by two factors: the length of the trace and the wavelength of the signal that propagates through it. If the propagating signal wavelength is comparable with respect to the trace length, the lumped model of the interconnect is not more sufficient. Once the signal starts propagating through the line, if a resistance mismatch occurs during the path, some reflections will appear and they start propagate in the opposite way with respect to the signal direction. This can generate critical voltage overshoot or voltage undershoot issues at the two ends of the line depending on the mismatching. A solution to solve this problem is to connect a series resistor to one end of the line in order to comply with the matching condition and avoiding the generation of reflections.
Another source of signal degradation is the impedance variation along the signal path related to the variation of the return current path. For this reason, the digital interconnections have been routed in the space where their reference plane is homogeneous for the entire trace length. The consideration about the signal integrity has been pointed out in Section 4.1.2, when the layer arrangement has been performed.

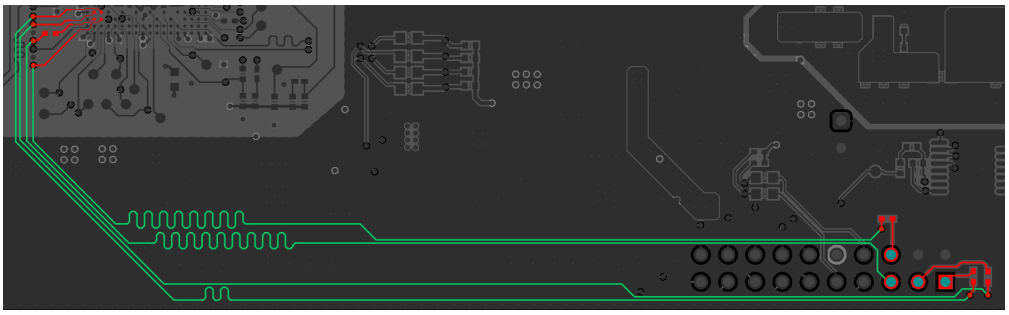

Figure 4.6: SPI 1 interface routing

Figure 4.6 shows the implementation of the SPI interface routing. The length of the interconnects has been length matched in order to avoid the risk of skew between the signals. In this layout, the following rules have been used during the routing of digital signals, the signal traces connected to the same interface have

been routed with the same length, and the same trace length has been ensured on each plane if the trace has been routed over multiple planes.

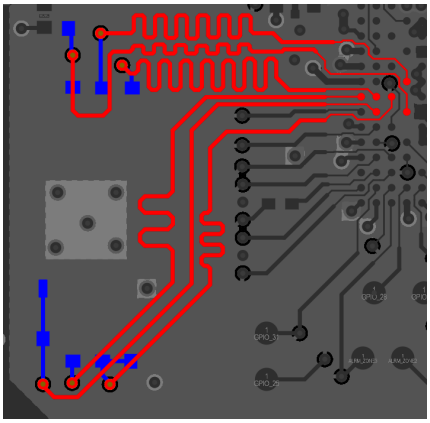

Figure 4.7: QSPI interface routing

This method has been used for SPI and QSPI (Figure 4.7) interfaces due to their high baud rate. The JTAG and UART interfaces have been adapted in length to reduce the risk of skew even if they work at lower speed than the previous ones. Considering the propagation of a digital signal, the Signal Integrity problem is not just related to the small signal period that propagates into the line. Nowadays, problems arise due to the short rise time and the fall time edges of the digital signal. This condition causes that the high frequency components of the signal must propagate as fast as the low frequency ones without being attenuated. However, the signal trace is made by real material, and this is characterized by a certain value of the effective dielectric constant and attenuation, which are frequency dependent. A signal that travels through the trace experiences the distortion effect due to its frequency components does not arrive to the other side of the line at the same time and with the original amplitude. A possible analysis used for measuring the behavior of a signal through a line is the "Eye Diagram". A random sequence of digital signals is launched repeatedly into the channel and the output waveforms are observed at the end of the line. If the output waveforms represent clearly the information that is sent, means that the signal is propagated correctly along the trace.
Another problem when routing the digital interconnections is the number of VIAs inserted along the signal path. VIAs can limit the propagation of the signal due to the introduction of the impedance variation. In this case, the reflections can appear and the effect of these have been discussed previously. For this reason, the usage of VIAs in a critical signal route must be minimized.
The distance between traces that run next to each other must correctly defined otherwise crosstalk became predominant. The presence of the capacitive coupling

makes that any voltage variation in a line, that act as the aggressor, can influence the neighbour line, called victim. The solution for this problem is to keep the tracks as distant as possible so that the capacitive coupling became negligible avoiding the possibility of false triggering in the victim line.

4.2.3 Radio Frequency Part

This part explains the layout of the antenna elements on the board, and how they are connected to the corresponding chip pins.
The antenna pattern is optimized for the MIMO adopting the Minimum Redundancy scheme. Figure 4.8 shows the layout implementation of the RF part.

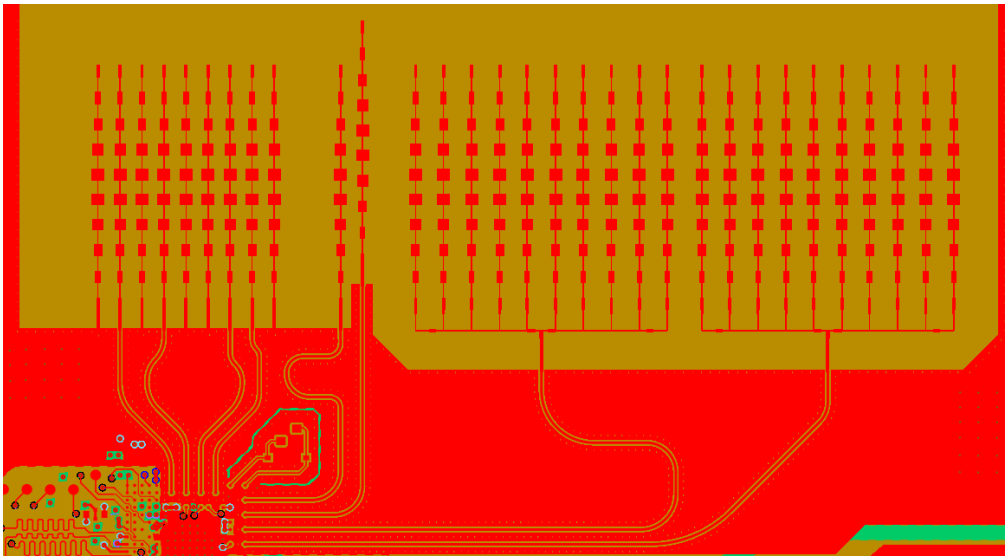

Figure 4.8: TX and RX antenna layout

The layout of the antennas has been developed following the Minimum Redundancy scheme described in Section 1.5.
Each receiver channel is composed by 1x10 array patch antenna. Since they are the same of the previous version of the board, they have not been modified.
The transmission antenna pattern is composed of two 1x10 array patch antennas connected to TX1 and TX2 for the short range RADAR application, and two 10x10 array patch antennas connected to TX3 and TX4 for the long range RADAR application. TX3 and TX4 have been spaced by a distance of 6.5λ for MIMO. TX2 is shifted vertically with respect to TX1 by a lambda factor in order to perform the elevation estimation. To comply with this change, the board height has been increased by the same amount.

The following picture depicts the antennas positioning in the layout.

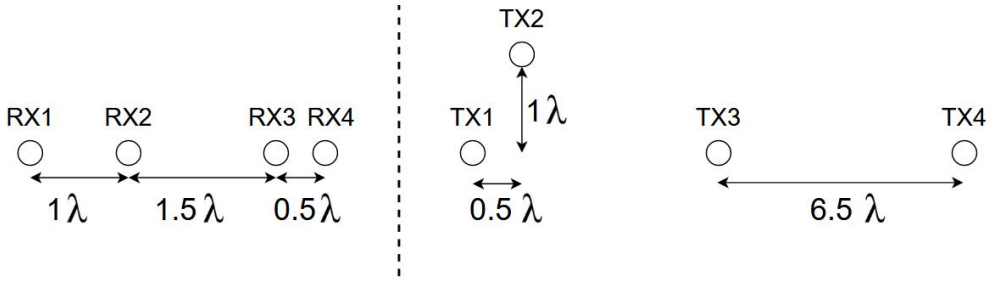

Figure 4.9: RX and TX antenna pattern exploited in the layout

The corresponding MIMO virtual array exploiting the Minimum Redundancy scheme is depicted in Figure 4.10. The elements depicted in grey are those obtained from the physical receiver antennas, instead the elements indicated in red are those elements extracted after the Minimum Redundancy processing.

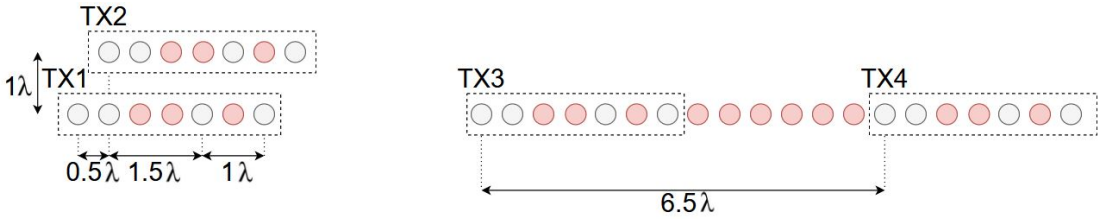

Figure 4.10: Virtual array using the Minimum Redundancy scheme for short range RADAR application on the left, and for the long range RADAR application on the right

The final number of elements in the virtual array for the short range RADAR is 14 used for the azimuth and elevation estimation; instead, for the long range RADAR there are 20 elements for the azimuth estimation.
Figure 4.11 highlights the active receiver antennas; the ones obscured are the dummy elements used to minimize mismatches.
The microstrip interconnections from the antennas toward the chip represented one of the major challenges in the board layout. They have been carefully designed in order to avoid corruption in the transmitted and received signals.
The receiver antenna microstrips have been designed to have a length which is an integer multiple of the signal wavelength and they have been length matched. The TX1 and TX2 have been length matched for the short range operation, and the TX3 and TX4 have been length matched for the long range operation.
The structure that has been used for these interconnections is the coplanar microstrip. The 2D field solver tool embedded in Altium Designer has been utilized to

perform the impedance matching. This tool takes the advantage of the data used for the stackup and microstrips to compute the width of the trace for obtaining the 50 Ω characteristic impedance without solder resist. The computed trace width of 0.3 mm has been used.

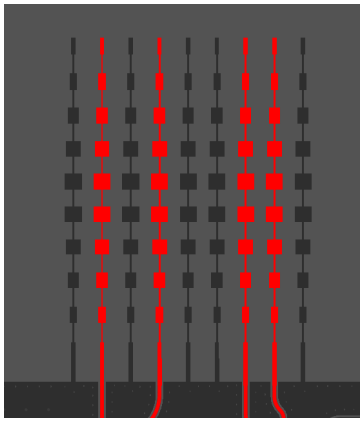

Figure 4.11: RX active antennas and dummy elements

Other arrangements for both TX and RX traces such as no sharp bends and symmetrical structure have been employed to minimize the phase variation between the signals arriving from the antennas. An opening on layer two below the chip RF pins have been created as recommended by Texas Instruments.
Finally, the shielding technique has been employed to protect the RF traces against noise and to create a uniform structure avoiding impedance change along the signal path. In Figure 4.12 is shown the application of this method on the RX lines.

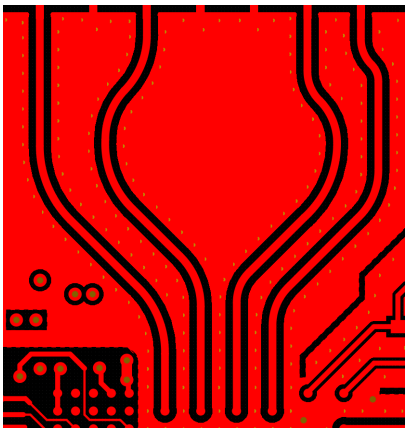

Figure 4.12: Shielding method used on RX lines

4.2.4 Other Layout Considerations

Two additional considerations about the external oscillator and thermal dissipation of the chip are discussed in the following.
The oscillator shown in Figure 4.13 has been mounted as near as possible to the chip pin for parasitic capacitance reduction, and a cut-out shape around it has been performed on top layer and layer two in order to insulate it.

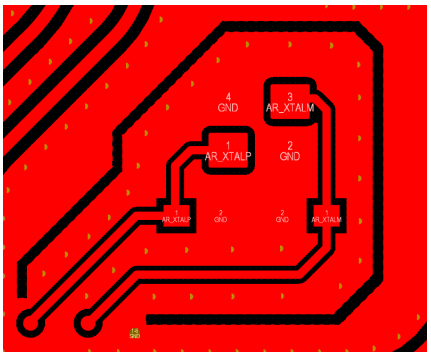

Figure 4.13: Oscillator layout

According to the device datasheet, the AWR2944 consumes about 2.25 W of power; the PCB should be able to dissipate the heat produced by this large power consumption. To improve the thermal dissipation through the layers, and to provide a well designed return path for the chip, the number of VIAs in the central part of the device has been maximized. The actual layout contains more than 40 VIAs as shown in Figure 4.14.

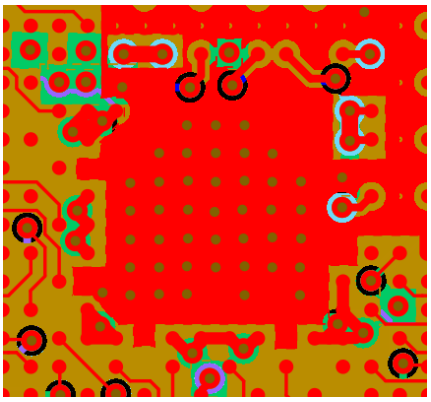

Figure 4.14: VIAs for thermal and return path optimization

The solder mask has been designed to cover the top and bottom layers in order to prevent copper from oxidation and preserving its integrity. However, the antenna part has not been covered with solder resist in order to ensure better radiation performance, and to get a value of the effective dielectric constant equal to that one used during the design stage. The effective dielectric constant can vary if the solder resist is applied, as a consequence of this, the characteristic impedance of the transmission line changes.
Figure 4.15 shows the presence of the solder mask on the antenna part to prevent the deposition of the solder resist on it during the manufacturing.

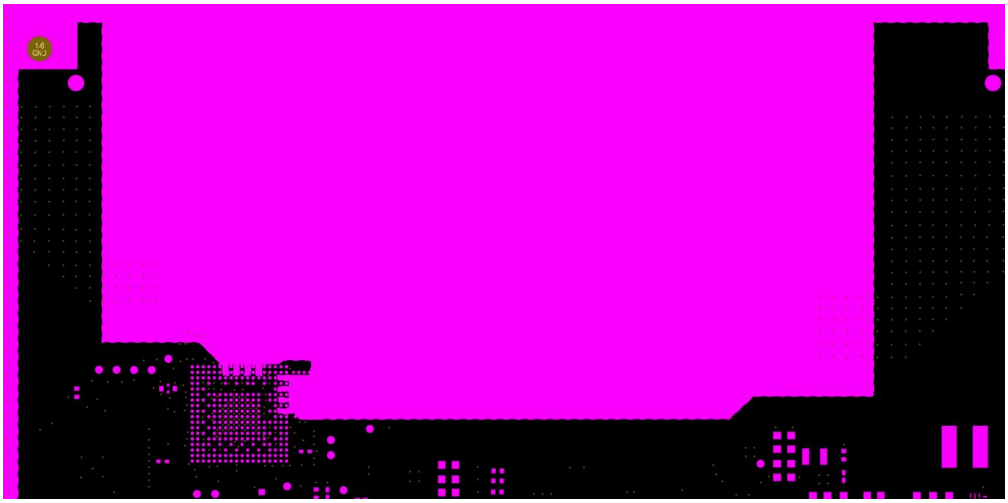

Figure 4.15: Solder mask on the RF part

Figure B.9 and Figure B.10 in Appendix B illustrate the top and bottom paste mask layout respectively. The paste mask has been used to define where the solder paste must be applied for soldering the components on the board.

4.3 Power Delivery Network Simulation

The Power Delivery Network simulation has been used as post-layout verification test, the reference book used for this part is "Signal and Power Integrity - Simplified"[18] written by Dr.Eric Bogatin. The goal of this analysis was to describe how the designed supply network influences the supply voltage on the chip pin whenever the latter asks for a certain amount of current.
The PDN analysis figures out the supply network impedance including the parasitic elements that can arise due to either the layout of the circuit and the real behaviour of the used components. The frequency domain analysis of the PDN gives a clear view on the presence of possible voltage ripple caused by the resonances due to the coupling of the inductive and capacitive elements in the network. The following image highlights the presence of the supply network impedance between the voltage source and the supplied chip pin.

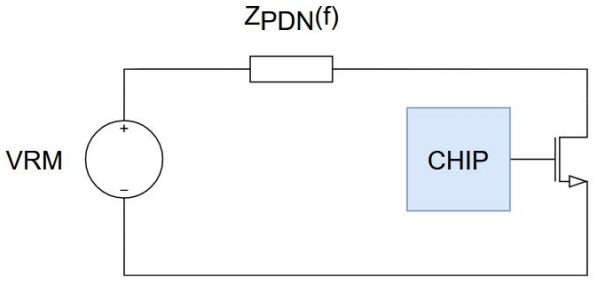

Figure 4.16: PDN impedance influence in a circuit[18]

The PDN model consists of the elements present in the path from the voltage source, called Voltage Regulator Module (VRM), to the supply pin of the chip. The resulting behavior of the network is described by the Z_{PDN} impedance, which is frequency dependent.
Since the PDN is composed of reactive elements, whenever the chip sink current from the VRM, the supply network reacts to that generating a voltage ripple. The generated ripple depends on the impedance profile of the PDN and the corresponding frequency components of the current that flow through it. The following expression defines the relation between the voltage ripple and the impedance of the power rail.

$$V_{ripple}(f) = Z_{PDN}(f) \cdot I(f) \quad [V] \tag{4.1}$$

I(f) is assumed to be the spectrum of the current required by the chip.
It is possible to notice that a low impedance value is required for getting a voltage ripple which is limited up to a maximum allowable value. The maximum allowable

voltage ripple inherently sets the maximum value of the impedance that must be ensured, called Z_{Target}; it is shown in the following expression.

$$Z_{target} = \frac{V_{DD} \cdot ripple\%}{I_{transient}} \quad [\Omega] \tag{4.2}$$

The transient current is defined as the maximum frequency component of the current required by the chip. Since an accurate description of the current frequency spectrum is generally unknown, the transient value can be estimated from the maximum current value available[18] on datasheet as shown in Equation 4.3. This approximation can be used as worst-case scenario.

$$I_{transient} = \frac{I_{max}}{2} \quad [A] \tag{4.3}$$

The following image represents the generic PDN scheme of a circuit. Five regions can be distinguished for describing the supply network: the VRM, the bulk capacitors, the decoupling capacitors, the PCB planes, and the package capacitors if present.

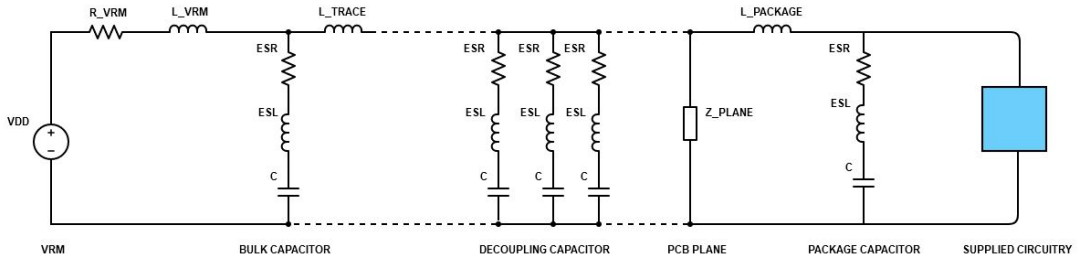

Figure 4.17: Generic PDN scheme[18]

The VRM part describes the voltage source behavior; it regulates the low frequency part of the PDN spectrum. Ideally the voltage source tries to maintain a constant voltage to the output. When the VRM is turned on, it maintains the impedance spectrum constant up to some kHz.
The mid-level frequency is dominated by the bulk and the decoupling capacitors. Since these capacitors can be selected during the board development, this is the part where board designers can play with and try to optimize the design.
The bulk capacitors usually are electrolytic capacitors with large value which are mounted near to the VRM output.
The decoupling capacitors are mounted as close as possible to the chip. The frequency range of influence of these capacitors starts from 10 kHz up to 100 MHz.
The last portion of the network is composed by the capacitors mounted directly on the chip package if present. Usually they are hidden from the board designer

point-of-view and it influences mainly the high frequency spectrum of the PDN. In the network analysis, the interconnections and planes play an important role in providing additional parasitic inductance or parasitic capacitance to the PDN network. Usually the parasitic capacitance introduced by the planes is small, thus, it influences mainly the high frequency part of the PDN impedance.

As described above, the PDN structure is quite complex, and the resulting impedance has real and imaginary part due to the resistive and reactive elements. The challenge in performing the PDN simulations is to obtain an accurate model for the used elements in order to get a result that corresponds as near as possible to the real behavior.
The impedance profile can be simulated in LTspice using the following test circuit[18].

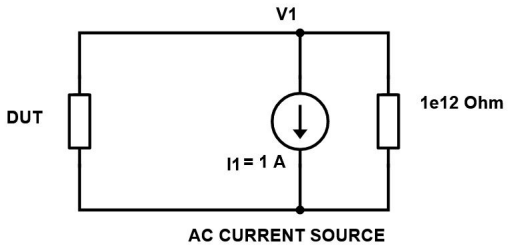

Figure 4.18: PDN test scheme

The DUT represents the supply network that is simulated in order to extract its impedance frequency behaviour.
The AC current source simulates the current that is required from the chip. It can be set to generate a sinusoidal signal with an amplitude of 1A; in this way it is possible to measure the impedance value directly from the voltage across the DUT as shown in Equation 4.4[18].

$$Z_{PDN}(f) = \frac{V_1(f)}{1A} \quad [\Omega] \tag{4.4}$$

The results that have been obtained for the developed system are an approximation of the real behavior due to the inability to have an exact model which describes the real behavior of each element present in the PDN.
The models for the mounted capacitors and inductors have been taken from SimSurfing[14] in order to include their parasitic elements in the simulation. The other elements that have been utilized for the PDN equivalent model are the power planes parasitic capacitance and the traces parasitic DC resistance and inductance. These parasitic elements have been calculated utilizing the "Saturn

PCB Design Toolkit Version 8.21"[19]. The model of VIAs has not been taken into account in the Power Delivery Network simulations due to their effect is negligible in the range of frequency that has been analyzed, that does not exceed 100 MHz.

The equivalent circuits utilized for each PDN simulation and their respective result are shown in Appendix C.
In the following part the 3.3V supply network simulation is described. The equivalent model of the supply network has been defined from the output of the voltage regulator, where the feedback pin is connected for obtaining the regulated voltage, to the farthest chip pin that is supplied by this voltage rail. The picture below highlights the PCB layout part that has been analyzed in the 3.3V PDN simulation.

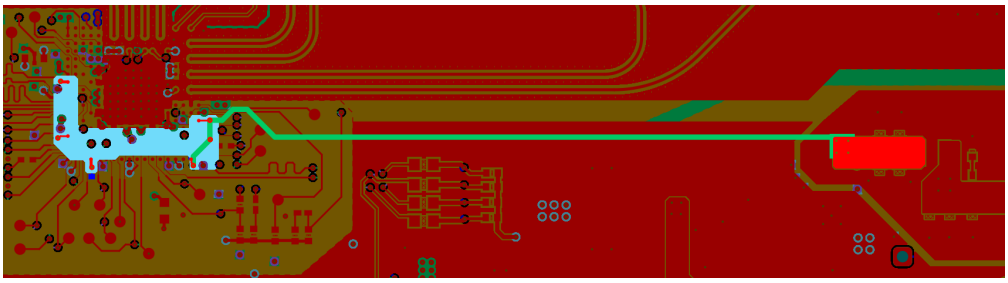

Figure 4.19: 2D view of the 3.3V supply network

The supply path has been decomposed in the elements discussed previously; the schematic shown in Figure C.1 has been used in LTspice for setting the simulation. The AC analysis from 1 Hz up to 100 MHz has been set with a frequency sweep in decades, taking one thousand points for each step.
The Figure C.2 depicts the PDN simulation result of the 3.3V supply network. The impedance at low frequency is maintained at the constant value of 180 mΩ up to approximately 2 kHz. The graph illustrates some resonant peaks due to the coupling between inductive and capacitive elements in the circuit. In particular, at 250 kHz and 20 MHz there are two relative minima points dictated by the self-resonant frequency. Instead, at 30 kHz and 4 MHz there are two relative maxima points due to the parallel resonant frequency. The first maxima point is the most dangerous one due to the PDN impedance at that frequency is about 1Ω. The high frequency behavior above 100 MHz is not considered due to it is influenced by the on-chip capacitors, which have not been considered in these simulations.
The presence of the second maxima is caused by the parasitic inductance introduced by the 3.3V supply trace on layer three, which is highlighted in the picture below.

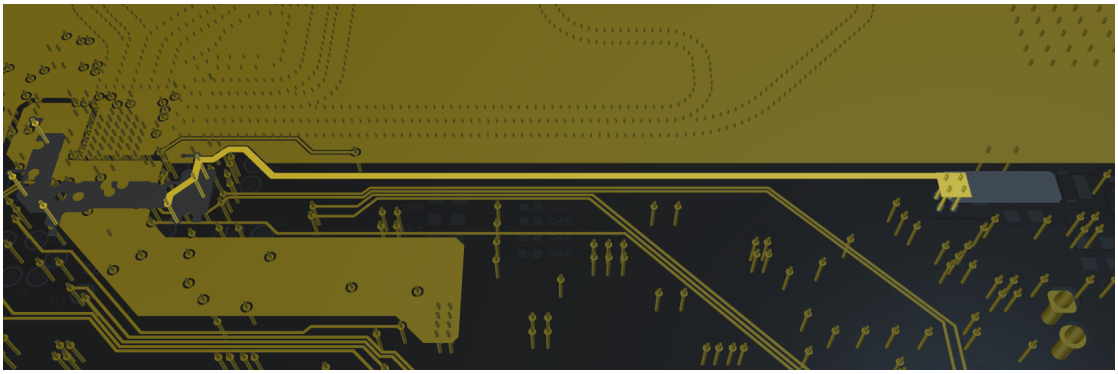

Figure 4.20: Critical trace in the 3.3V rail

The same method has been used for the analysis of the other supply rails. Considering the 1.2V and 1.8V rails, their trend is similar. The resistance value in the low frequency range is lower than 50 mΩ. Furthermore, the overall behavior is improved in the mid frequency range with respect to the 3.3V supply rail due to the lower peak at the resonant frequency. The unique maxima point is present at 23 kHz, and its value is about 480 $m\Omega$ in the 1.8V rail and about 550 $m\Omega$ in the 1.2V rail.
For what concerns the 1.0V rail, its impedance trend varies slightly from the previous ones. The low frequency resistance is about 50 mΩ, however, the peak is present at 62 kHz with a value that does not exceed 170 mΩ.

Chapter 5

Embedded Software Description for Comparison

The fifth chapter is devoted to the analysis of the RADAR embedded software used in the testing part. The demo software enables the processor to perform the required processing steps in order to get the results from the acquired ADC samples. However, it provides the possibility to configure the parameters associated with the RF part of the chip for the selection of the wanted chirp profile.
Texas Instruments provides the demo software for each evaluation board based on the corresponding chip platform. The demo software within the mmWave SDK MCU Plus version 4.2 for the AWR2944 chip is analyzed in the following. The processing steps are in common with the demo software developed for the AWR1843, the differences between the two software are highlighted later in this chapter.
The first part of this chapter describes the processing chain required to obtain the estimation of the targets and their information in the environment.
After that, the discussion moves toward the software modifications, explaining the changes that have been made to the original demo software in order to make them compatible with the actual designs. Then, the analysis of the customized chirp profile that has been used for the testing part is addressed.

5.1 Demo Software Processing Chain

The AWR2944 demo provides the required source files to implement the data processing chain. The profile defined by the user can be sent to the chip to configure the processing elements. Then, the processor will execute the program and it will extract the detected targets and their information in real-time. The configuration file and the processed data are exchanged between the Host PC and the chip through two separated ports exploiting the UART communication interface, as shown in the following figure.

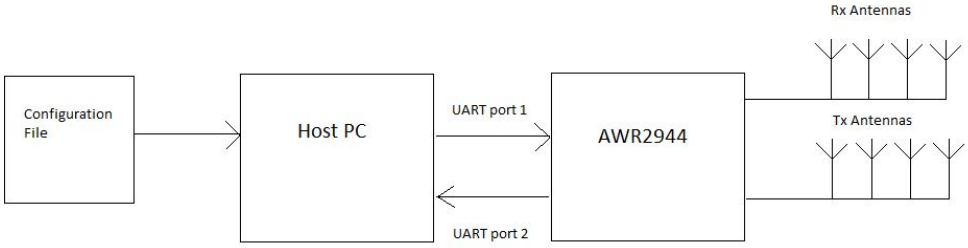

Figure 5.1: Host PC and AWR2944 chip interface

The demo supports both TDM or DDM MIMO techniques; the former is the Time Division Multiplexing Access, the orthogonality is ensured in time domain, which means that there is only one active antenna per time. The latter, is the Doppler Division Multiplexing Access, in this case the orthogonality is ensured in the Doppler spectrum. The benefit of the DDM method is that all TX antennas transmit at the same time, but the received signal requires further demodulation for getting the correct information. In the following, the TDM processing chain is considered, which is the one exploited to set the testing environment.

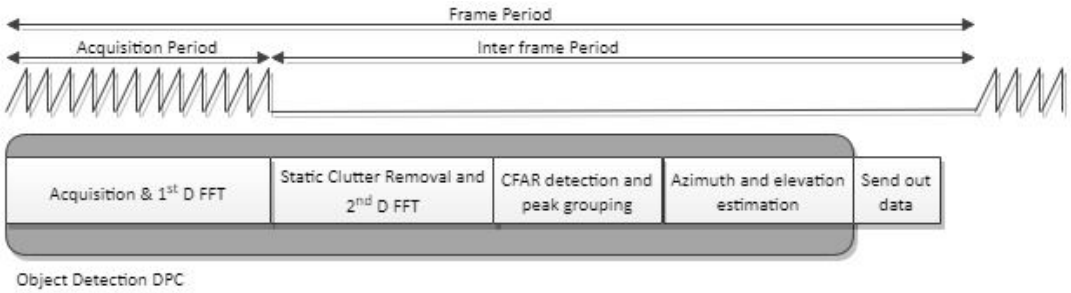

Figure 5.2: Signal processing flow taken from mmWave SDK MCU Plus v4.2

As shown in Figure 5.2, the data processing starts when the first chirp of the sub-frame is transmitted, and it ends before the successive sub-frame. The process continues until the last frame of chirps is analyzed. The execution of the single sub-frame is divided into two periods, one is called "Acquisition Period", during which the Doppler chirps are transmitted to the environment and simultaneously a Range-FFT on the received signal is performed. After that, there is the "Inter-Frame Period", in which the remaining data processing such as Doppler-FFT, CFAR and AoA are performed. Both the Acquisition Period and the Inter-Frame Period constitute the overall "Frame Period". Figure 5.3 shows the execution flow used to manage the data processing chain in the entire detection process.
The process starts calling the Data Path Manager (DPM) initialization, which initializes the Data Processing Chain (DPC) and its related Data Path Units (DPU). After that, follows the DPUs configuration for each sub-frame, if multiple sub-frame are defined. Then, the DPM configures the ADC to handle the acquisition process and trigger the Range DPU for starting the 1D-FFT computation. This is the first processing element invoked by the algorithm. The Range DPU outputs the RADAR Cube formatted in one of the supported formats. As consequent to this, the successive DPUs are called to process the data stored in the RADAR Cube. According to the actual demo implementation, the Doppler DPU, CFAR DPU and the AoA DPU are invoked respectively. The process described so far is repeated until the last sub-frame is reached. Once the sub-frame group finish the execution, the Data Path Manager and Data Processing Chain will stop. The information obtained from each frame is sent through the UART port in the form of packets. Each packet contains the header and the TLV items. The information collected as TLV items that is possible to extract from the RADAR chip are described below.

- List of detected objects which contains the target x,y and z relative positions with respect to the RADAR.
- Range profile
- Noise profile
- Azimuth static heatmap
- Range/Doppler heatmap
- Stats information
- Side information
- Temperature stats

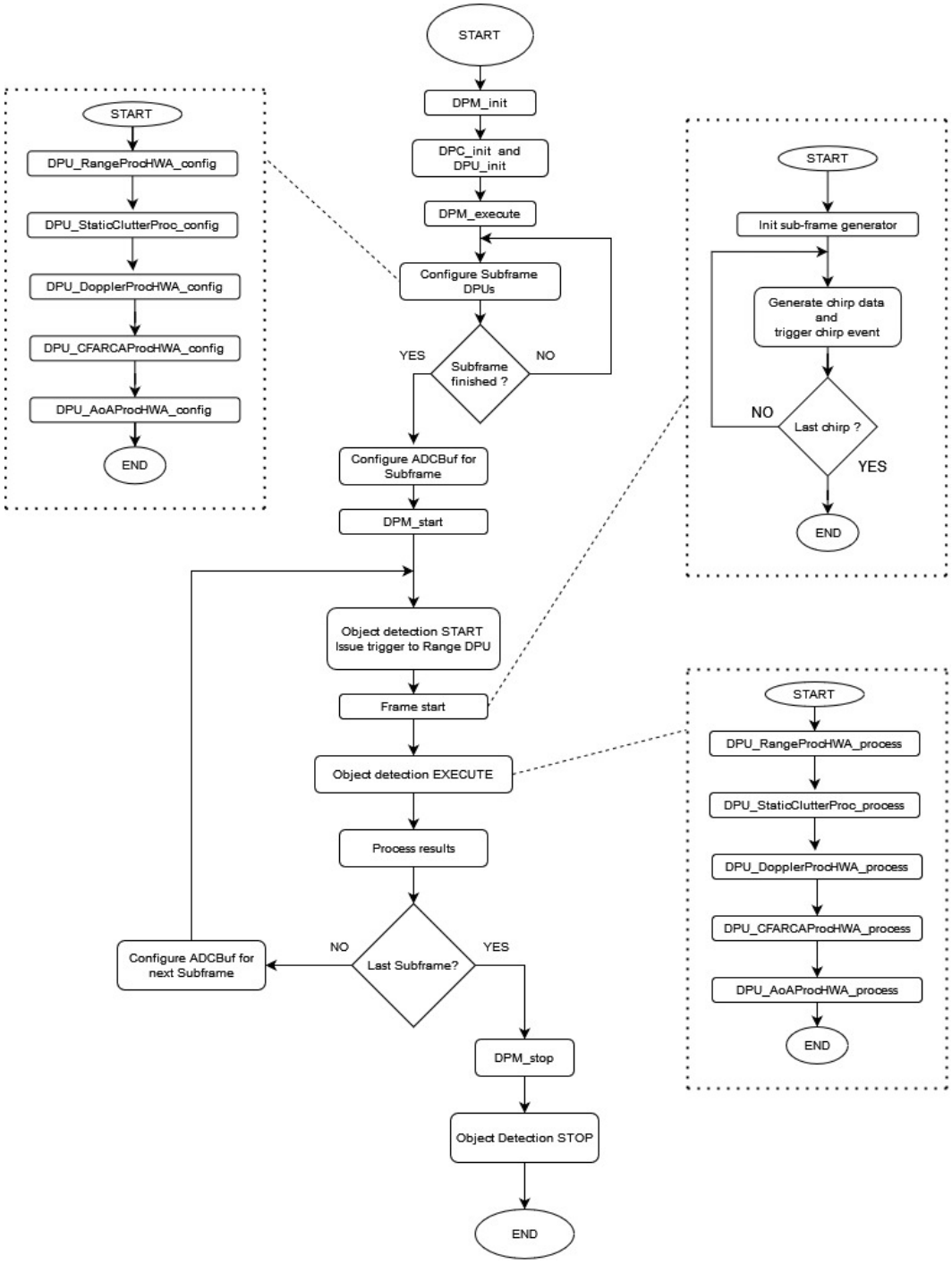

Figure 5.3: Application-DPC execution flow

The Range Profile outputs the data obtained corresponding to the zero Doppler bin for each range bin, so the corresponding values in the Range Profile belong to static targets only. This data has been extracted and analyzed in Chapter 6 in the comparison tests.

Based on the previous description, the complete detection processing chain is depicted in the following figure.

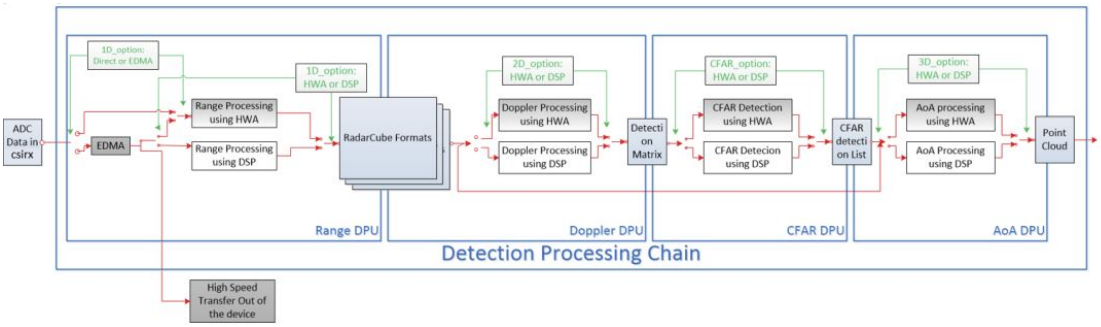

Figure 5.4: Detection processing chain taken from mmWave SDK MCU Plus v4.2 User Guide [20]

Each Data Path Unit is described in detail in the following subsections.

5.1.1 Range DPU

The Range DPU takes the sampled RF data from the ADC Buffer, it computes the 1D-FFT and save the results in the RADAR Cube in one of the supported format. This DPU exploits the Hardware Accelerator (HWA) for the FFT process, which starts when the received data are available to be copied into the internal memories activated by a hardware trigger.
When the FFT is completed, the EDMA will transfer the computed data in the RADAR Cube memory. At the end of the copy, the EDMA will raise an interrupt signal.
Figure 5.5 describes the Range DPU data path in a high-level of abstraction.

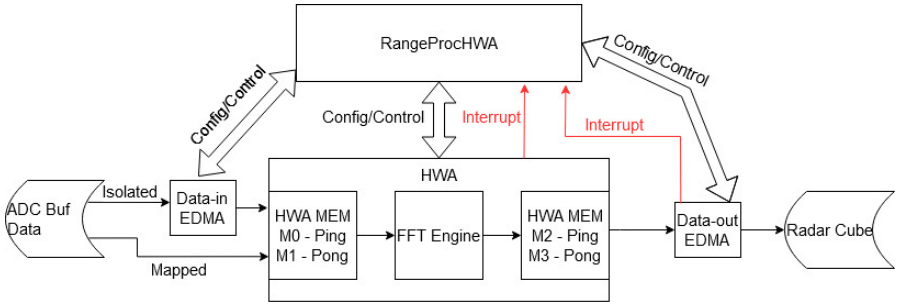

Figure 5.5: Range DPU data path

The internal process is based on the Ping-Pong strategy. This strategy allows the architecture to parallelize the Hardware Accelerator and the EDMA processing. When the Ping chain is busy in performing the FFT, the Pong chain can be used to transfer the incoming ADC data for the next FFT. As soon as the Ping chain ends the FFT process, and free the HWA, the Pong chain can start using the hardware accelerator for the new FFT.
Figure 5.6 shows the timing diagram of this process provided by Texas Instruments.

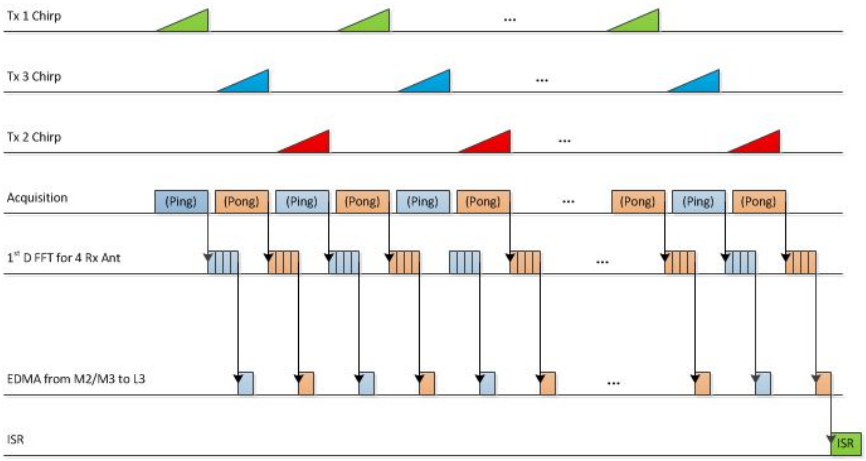

Figure 5.6: Range DPU timing diagram taken from mmWave SDK MCU Plus v4.2

Unlike the AWR1843, the AWR2944 chip supports only real ADC data. For this reason, the required memory size for collecting the samples is reduced with respect to the previous chip versions. Hence, the number of ADC samples that are supported increases to 2048 samples. Since the FFT is taken on real samples, the latter half of the FFT turns to be the complex conjugate of the former half, for this reason it is discarded from the HWA memory bank.

5.1.2 Doppler DPU

In the analyzed demo software, the Doppler DPU expects data from the RADAR Cube in Format 1, in which the 1D-FFT results are grouped by belonging to the same transmitting antenna.
Figure 5.7 shows the implemented Doppler DPU from a high-level of abstraction.

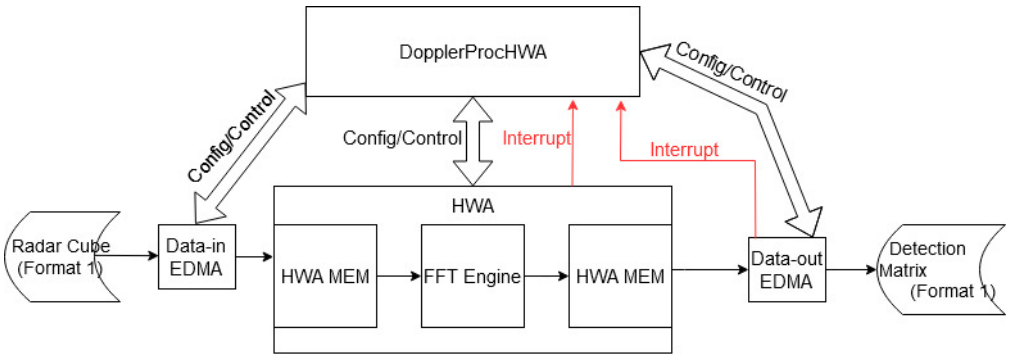

Figure 5.7: Doppler DPU data path

The Doppler DPU works with eight memory banks, they are managed for the Ping-Pong input/output processing as the Range DPU. The 2D-FFT starts when EDMA is triggered to transfer a column data from the RADAR cube into the internal memories. Before the FFT operation, the samples are multiplied by a window function, and the 2D-FFT together with the Log2 of the absolute value of each sample corresponding to the same range is computed. This processing step converts the number of input samples from the number of Doppler chirps to the number of the output samples which is equal to the Doppler bins. After that, the contributions provided by the virtual antennas are summed to get the resulting Doppler bin. Once the 2D-FFT is computed, the EDMA will transfer the results into the Detection Matrix. The Detection Matrix is the Range-Doppler Matrix, and its size is equal to the Range bins times Doppler bins.
Figure 5.8 shows the Doppler DPU operations in the time domain.

In this processing step it is possible to enable the Static Clutter Removal, feature that eliminates the unwanted objects from the detection. When it is asserted, the mean value of the input samples to the Doppler FFT is subtracted from the samples before the 2D-FFT operation.

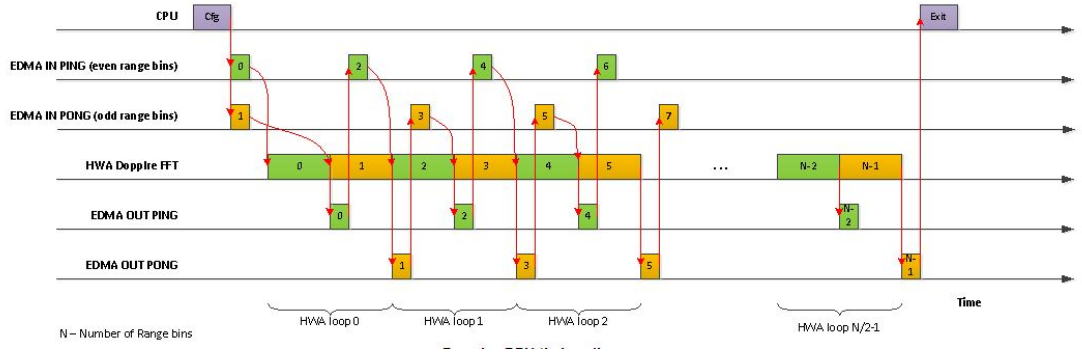

Figure 5.8: Doppler DPU timing diagram taken from mmWave SDK MCU Plus v4.2

5.1.3 CFAR DPU

CFAR DPU implements the object detection from the Range-Doppler Matrix. It exports a list of objects that are detected in both Range and Doppler domains.

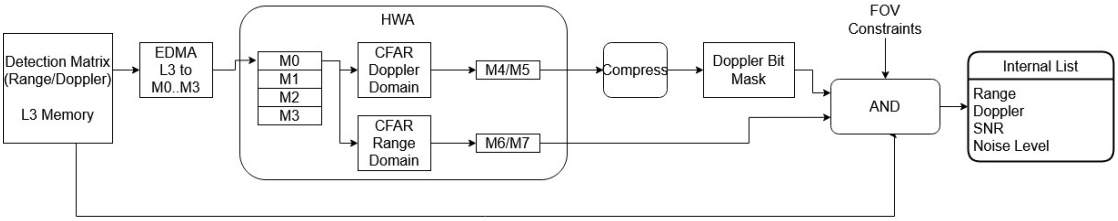

Figure 5.9: CFAR DPU data path

The detection process starts when the input EDMA is triggered, it copies the Detection Matrix from L3 memory to the Hardware Accelerator internal memories. Then, the CFAR in Doppler domain is performed and the results are stored into another internal memory. Upon completion, the CPU triggers the CFAR in the range domain, and in parallel calculates the bit mask from the previous results. This step outputs the detected objects in the Doppler domain.
After that, the processor takes the CFAR in range domain results and populates the output list. The objects within this list must respect two conditions: they must be detected in the Doppler domain (the bit in the bit mask must be set) and they must respect the field-of-view constraints passed at configuration time.
The CFAR can also perform the peak grouping function if enabled, when issuing the configuration of this DPU. The data processing described above is shown in Figure 5.9.

5.1.4 AoA DPU

This DPU implements the object angle-of-arrival estimation. The process takes advantage of the previous results and generates two lists which contain the coordinates and side information about the detected targets.
This step requires as input the RADAR Cube from the Range DPU and the CFAR objects detected list.
Due to the large number of processing sub-steps in this process, the AoA DPU takes more time compared to the previous ones. The following picture depicts the data flow from the input data up to the final result.

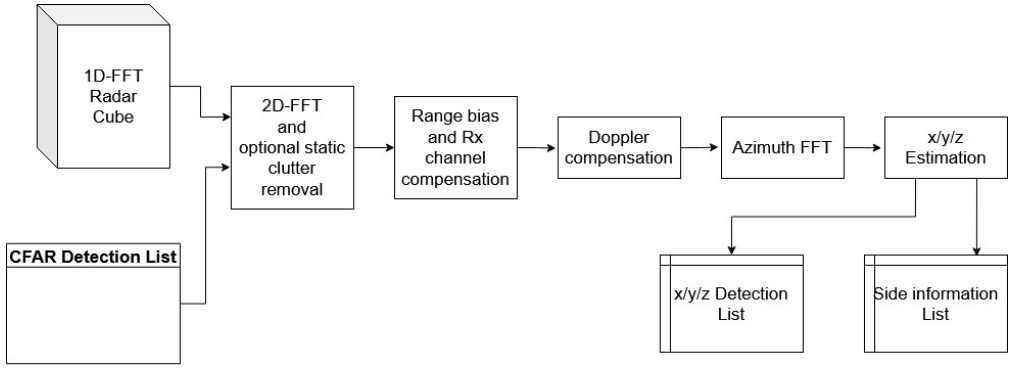

Figure 5.10: AoA DPU data flow

The AoA DPU supports the Ping-Pong processing, allowing two detected objects from the CFAR list to be analyzed simultaneously. It is possible to split the entire AoA processing into four parts:

1. 2D-FFT: the EDMA transfers the 1D-FFT data corresponding to the range index of the detected object in the CFAR list to the HWA memory. The HWA performs the static clutter removal, if this feature is enabled. Then, it calculates the 2D-FFT for each virtual antenna. The output EDMA transfers the Doppler bin data corresponding to the detected object Doppler index from the CFAR list into the local memory.

2. Compensation: CPU performs the RX channel phase compensation, the Doppler compensation and triggers the EDMA to copy back the data into HWA memory.

3. Azimuth FFT: HWA computes the azimuth FFT and elevation FFT from the respective TX antennas. Then, it calculates the magnitude square on the FFT output data of the azimuth TX antennas. Finally, the EDMA copies the data into the local memory.

4. Azimuth and elevation estimation: CPU performs the final azimuth and elevation estimation including the x,y and z calculation. At the end of this step, it appends the detected objects data to the output lists.

5.2 Communication Pins Adaptation

As stated at the beginning of Section 5.1, the communication between the Host PC and the RADAR devices is handled using the UART interface when using the demo software. For this reason, the UART input/output pins have been modified with respect to the original arrangement exploited by Texas Instruments for both the RADAR boards; this was a mandatory step in order to enable the exchange of data with the PC using the front connector mounted on the custom boards.
Two UART ports are required by the demo software to work, in particular, the UART_A is used to send the configuration data to the RADAR and to receive additional information from it; the UART_B is used to stream the processed output data from the RADAR.

The AWR1843 chip has been programmed using the demo software with the following pin configuration:

- UART_A TX: PIN N5
- UART_A RX: PIN N4
- UART_B TX: PIN P4

However, the same process has been applied also for the board which embeds the AWR2944 chip.
The AWR2944 chip has been programmed with the following pin configuration:

- UART_A TX: PIN E17
- UART_A RX: PIN F16
- UART_B TX: PIN G15

After these adaptations, the UART ports from the devices became accessible. The serial communication has been established using two UART-to-USB adapters.

5.3 Chirp Profile Configuration

Once the software has been modified to accommodate the design of the developed boards, before the RADAR chip starts working, a set of instructions must be sent through the UART_A port in order to configure the chip internal circuitry and the internal processing with the requested RADAR parameters. The complete command list in present in [20]; part of the entire configuration instruction set is described in the following. The commands listed below are those that configure the transmitting and receiving part of the device which have been used for the RADAR configuration during the test part.

- channelCfg: it allows to enable the transmitting and receiving chains through a bitmask operation. The user is allowed to select the TX antennas and RX antennas which are used through this command.
- profileCfg: it allows to set the general chirp profile used during the RADAR operation. It also sets the amount of transmitted power and the gain used at the receiver stage. The parameters configured by this command are: the start frequency, the ADC idle time, the ADC start time, the ramp end time, the chirp slope, the number of ADC sample during the acquisition and the ADC sample rate. Moreover, it allows to set the power back-off during the transmission and the gain utilized at the receiver stage, which is divided in RF chain and Baseband chain. The former include the gain control for the LNA and mixer, instead, the latter controls the gain after the down-conversion of the signal. Figure 5.11 illustrates the parameters which must be set with this command for correctly define the chirp profile.
- chirpCfg: it allows to define the set of chirp profile used, they could slightly differ with respect to the general one described previously. This command sets the used TX antenna for each chirp profile.
- frameCfg: it sets the number of chirps that are sent during the Frame time, this parameter determines the number of Doppler chirps. However, the total Frame duration can be set using this command.

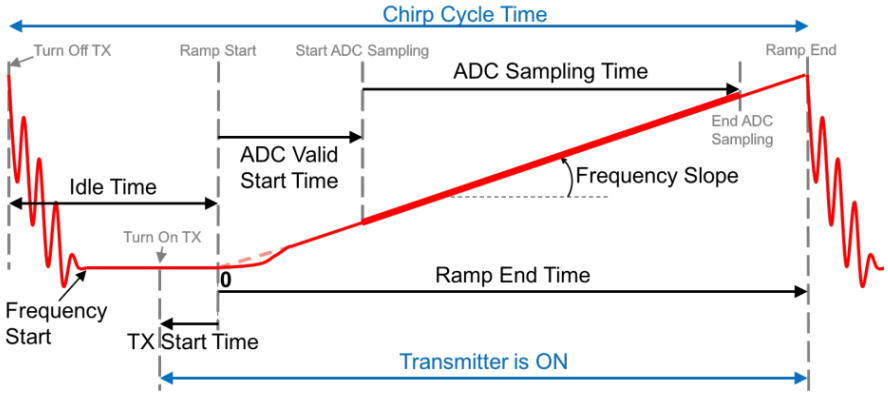

Figure 5.11: Configurable chirp profile parameters taken from mmWave SDK MCU Plus User Guide[20]

Once the instruction set is correctly configured for the wanted RADAR parameters in terms of maximum unambiguous range, range resolution, maximum velocity and velocity resolution; the instructions can be sent to the device through the TI mmWave Demo Visualizer interface.

Chapter 6

Results and Conclusions

The last chapter discusses the final steps that have been employed in order to set correctly the measurement environment for the comparison.
As aforementioned, the final goal was the creation of a fair testing environment in order to compare the performance of the AWR2944 system with respect to the AWR1843 one.
After that, the results that have been obtained from the tests are analyzed.
Additional notes regarding future improvements of the developed system are included at the end of this chapter.

After the board has been manufactured and the components have been mounted on it, the obtained AWR2944 RADAR system is shown in Figure 6.1 and in Figure 6.2.

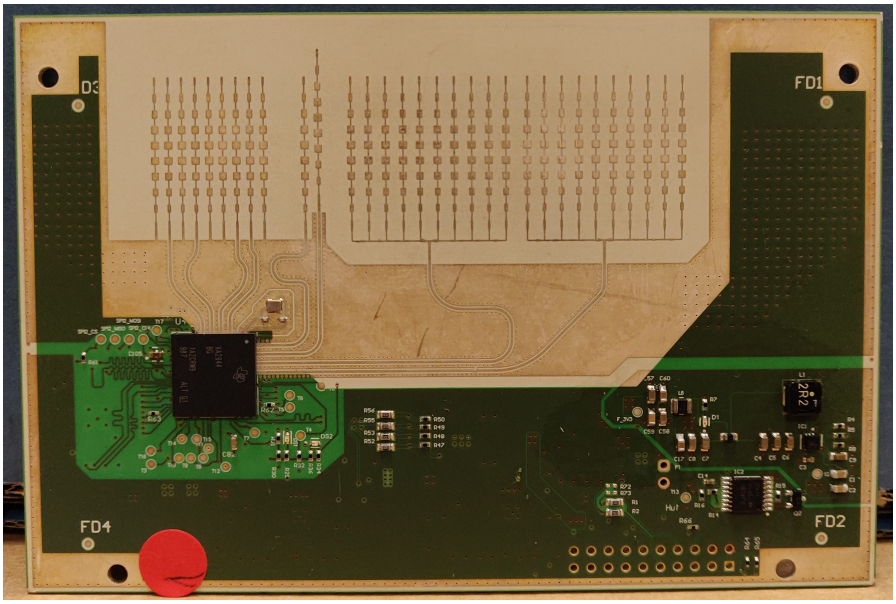

Figure 6.1: Top side of the manufactured AWR2944 board

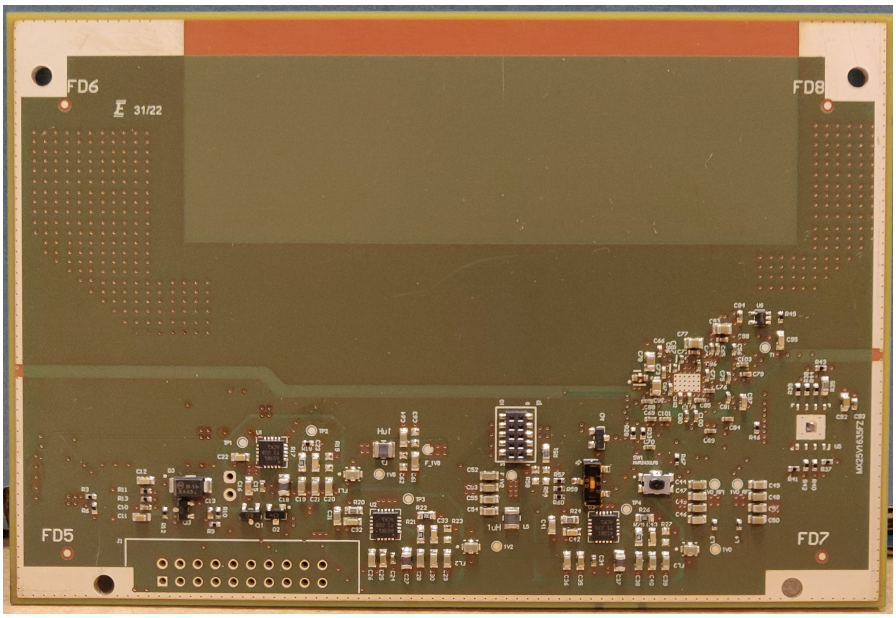

Figure 6.2: Bottom side of the manufactured AWR2944 board

Since the default chip UART pins have not been routed correctly, the developed board cannot be used to program the QSPI memory. To overcome this problem, the customized demo software has been loaded into the memory embedded in the AWR2944EVM Evaluation board, then, the programmed memory has been unsoldered from the original board and it has been soldered into the manufactured one.
However, during the components placement stage, it has been realized that the memory footprint has not been positioned with the correct pin arrangement. For this reason, a further step has been involved to correct this issue. To solve this problem a memory adapter PCB has been developed and it has been mounted to the RADAR board. The memory has been soldered on this adapter and the signals have been re-routed with the correct pin arrangement.
The following image shows the solution exploited to correct the routing of the memory signals.

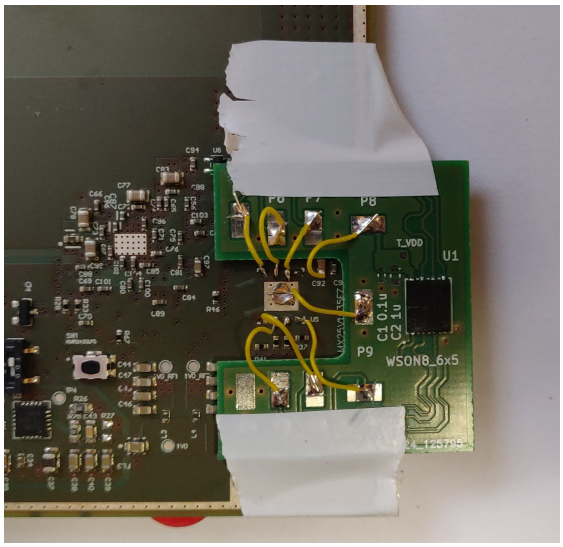

Figure 6.3: Memory adapter mounted on the AWR2944 board

The front connector and the 2x1 pin header have been mounted as the final step of the board development stage; the latter has been shorted for bypassing the watchdog signal that has not been used in this application.

The following Table summarizes the supply voltages measured at the output of each conversion chain and after the filtering circuitry. The digital multimeter Keysight U1232A has been used for these measurements.

SUPPLY VOLTAGE	VALUE	UNIT
3.3V	3.360	V
3.3V Filtered	3.360	V
1.8V	1.824	V
1.8V Filtered	1.818	V
1.2V	1.235	V
1.2V Filtered	1.197	V
1.0V	1.040	V
1.0V Filtered	1.040	V

Table 6.1: Supply voltage levels measured on the AWR2944 board

The measured supply voltages are compliant with the AWR2944 supply specifications.

Before taking into account the final results obtained from the comparison, a description of the next steps which have been involved is provided in the following. The connection between the Host PC and the RADAR chips has been established utilizing two UART-to-USB adapters exploiting the mmWave Demo Visualizer v3.6 for the AWR1843 board and the mmWave Demo Visualizer v4.2 for the AWR2944 board. The RADAR chips transfer out a sequence of data for each frame which contains the selected TLV items as stated in Section 5.1. The data obtained from the RADAR chips have been analyzed using a MATLAB script. The MATLAB script takes as input the recorded information, and it extracts the Range Profile data from each frame, which has been used for the comparison parameter. The script plots the range profile in terms of Received Power vs Range.

The Received Power has been computed using the formula that is used in the mmWave Demo Visualizer. The same formula has been used to obtain the results from the AWR2944 system and from the AWR1843 one; it is shown below.

$$\text{Received Power} = \text{rp} \times \frac{1}{256} \times 20 \times log_{10}(2) + 20 \times log_{10}(\frac{32}{N_{RangeBin}})[dB] \quad (6.1)$$

Where rp is the array vector extracted from the Range Profile TLV which is multiplied by $20 \times log10(2)$ for the conversion in dB and divided by the 256 constant normalization factor. $N_{RangeBin}$ is the number of range bin used in the Range Profile. The Received Power value is independent from the FFT size used to obtain the results, thus, it is useful when the results from different chirp configurations should be compared.

Two different measurement tests have been exploited for the systems comparison. The first one compares the amount of Received Power that is obtained from a static test target, assuming that the systems operate under the same conditions, which imply the same distance from the target and the same chirp profile. For this analysis, the MATLAB script computes the value of the Received Power averaged for 10 seconds for each range bin.
The second one involves the comparison of the Noise Floor measured by the two systems. For this kind of measurement, an absorbing material has been positioned in front of the RADARs in order to nullify the contribution of the received signals, thus, the measurement corresponds to noise contribution only. In this case, the script computes the mean value of the noise at the target range bin considering all the frames.

In order to have a fair comparison of the system performance, the same chirp configuration has been used in both the RADARs, and it is described below.

- Start frequency: 78 GHz
- ADC idle time: 25 us
- ADC start time: 7 us
- Ramp end time: 40 us
- Slope: 25 MHz/us
- ADC resolution: 12 bits
- ADC sample: 192 sample
- ADC sampling rate: 6000 ksps
- TX back-off: 0 dB
- RX gain: +30 dB

The RADAR parameters which have been set with this chirp configuration are shown in Table 6.2.

PARAMETER	AWR1843	AWR2944	UNIT
Bandwidth	0.8	0.8	GHz
Range resolution	0.188	0.188	m
Maximum unambiguous range	30	15	m

Table 6.2: RADAR parameters from chirp configuration

The velocity and angular information of the target have not been extracted from the measurements since a static scene has been considered, and only one transmitting and one receiving antenna have been used.
Due to the real sampling, the maximum unambiguous range of the AWR2944 is half than the AWR1843 maximum unambiguous range. The reason for this is that, in order to respect the Nyquist–Shannon sampling theorem[21], considering to use the same ADC sampling frequency, the maximum IF frequency that is possible to sample with the real sampling method is equal to $IF_{max} = \frac{ADC_{samplingfrequency}}{2}$ [Hz]. Instead, the maximum IF frequency that is possible to sample with the I/Q sampling method is equal to $IF_{max} = ADC_{samplingfrequency}$ [Hz]. Thus, follows that the AWR2944 maximum unambiguous range becomes half than the AWR1843 maximum unambiguous range when the same sample rate is exploited in both systems.

The testing environment used for taking the measurements has been selected such that the test target should be positioned at least 10 meters distant from the RADAR setup. For this reason, the measurement has been taken outdoor with a corner reflector, which has been used as test target positioned at a distance equal to 12 meters from the RADAR. The setup employed in the measurement part is depicted in Figure 6.4.

The procedure exploited before the data acquisition is described in the following. The RADAR has been regulated in azimuth and elevation until the maximum Received Power from the test target has been detected. This procedure has been utilized for all the measurements with both systems. After that, a 10 seconds data recording has been taken from each measurement.

Figure 6.4: Setup used for the measurements, the test target is positioned 12 meters distant from the RADAR setup

The first measurement part has been devoted in comparing the Received Power of the AWR2944 system with respect to the AWR1843 system. For this part, the measurements have been taken by activating one transmitting antenna at a time, first using the 10x1 transmitting antenna array (TX1 for both the RADARs) and subsequently using the 10x10 transmitting antenna array (TX4 for the AWR2944 board and TX3 for the AWR1843 board).
The second receiving antenna (RX2) has been used in both systems during the measurements.

The result averaged for 10 seconds obtained from the 10x1 transmitting antenna using the AWR2944 board is shown in Figure 6.5, and the result obtained from the 10x1 transmitting antenna using the AWR1843 board is shown in Figure 6.6.

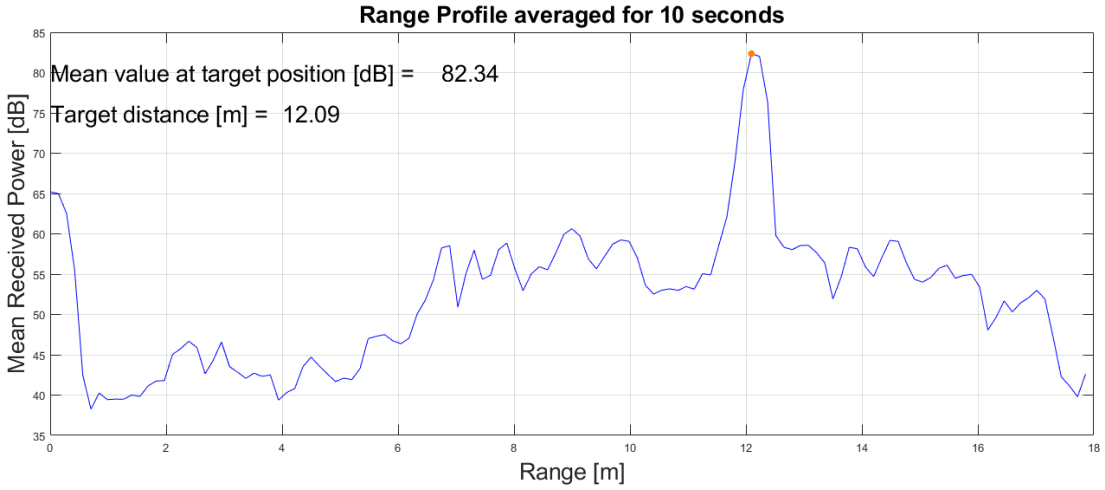

Figure 6.5: Averaged measurement for 10 seconds with AWR2944 using 10x1 transmitting antenna

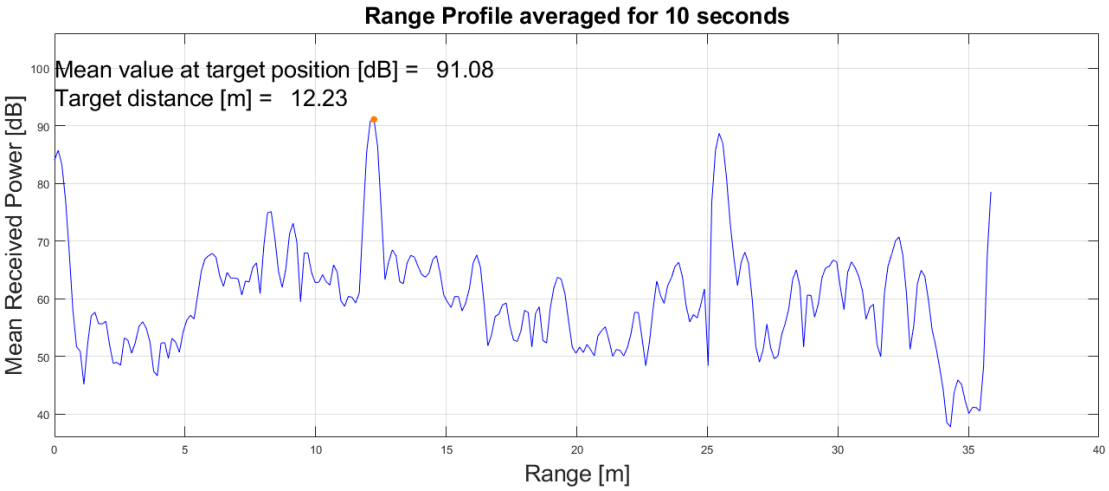

Figure 6.6: Averaged measurement for 10 seconds with AWR1843 using 10x1 transmitting antenna

As shown above, the corner reflector has been correctly detected at a distance of 12 meters; the difference between the mean values obtained from these measurements is 8.7 dB in favor of the AWR1843 RADAR system. Considering the Figure 6.6, it is possible to notice the presence of a strong target at a distance of 25 meters. Even if this target is not present in the testing scene, due to the low azimuth directivity of the 10x1 transmitting antenna, the RADAR caught a strong reflection belonging to a light pole positioned outside the testing environment.

The results averaged for 10 seconds obtained from the 10x10 transmitting antenna are shown in the following figures.

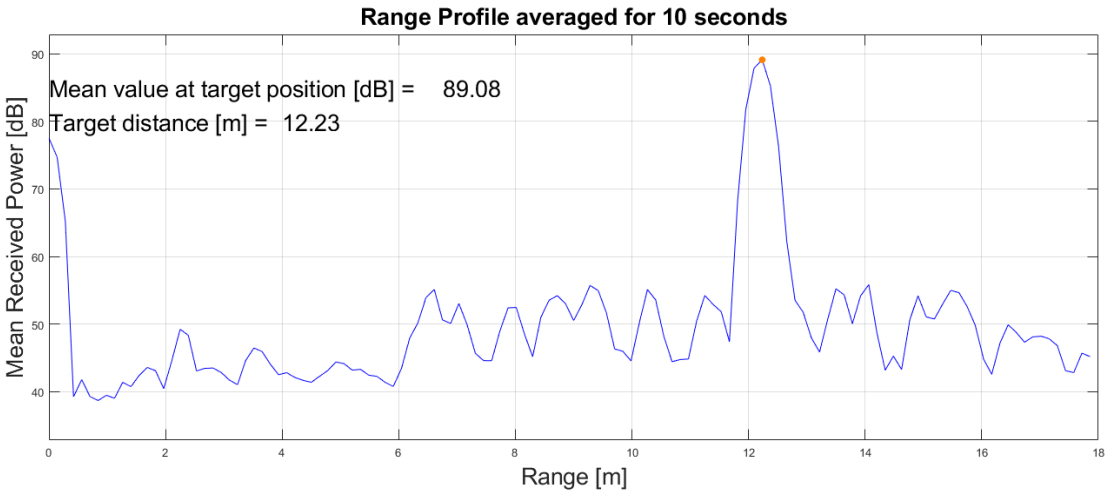

Figure 6.7: Averaged measurement for 10 seconds with AWR2944 using 10x10 transmitting antenna

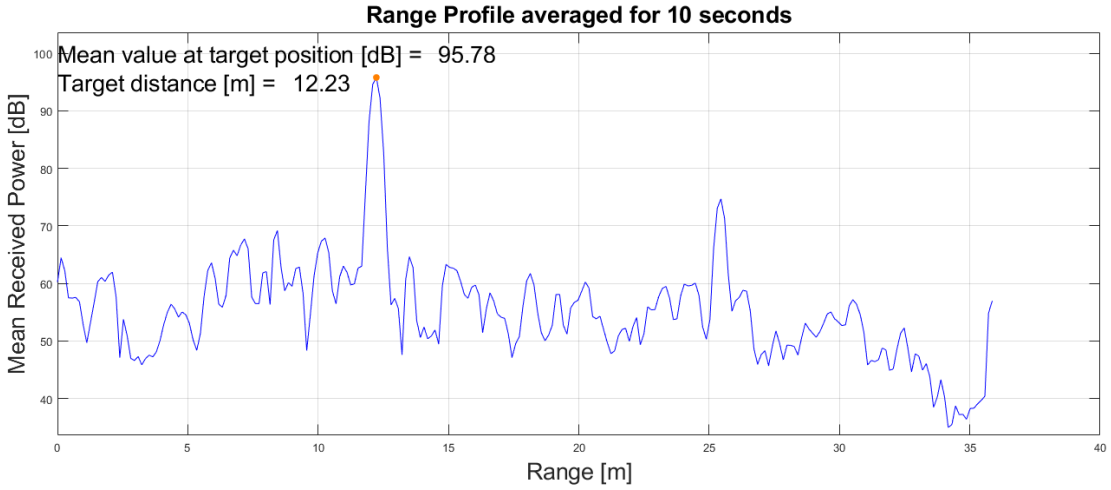

Figure 6.8: Averaged measurement for 10 seconds with AWR1843 using 10x10 transmitting antenna

Also in this case the target has been correctly detected, and its Received Power averaged for 10 seconds taken by the AWR1843 board is greater than that one obtained from the AWR2944 board by a value of 6.7 dB.

The results shown previously describe a context where the measured Received Power of the AWR2944 system is reduced with respect to the AWR1843 system. This behaviour is attributable to four factors:

- Considering the TX1 (10x1 array) antenna interconnection in both systems, the microstrip length used in the AWR2944 to connect the antenna to the chip is increased by an amount of 0.7 cm with respect to the microstrip length used in the AWR1843 board. Considering the signal loss in the ROGERS3003 material, as reported in [22], the increased microstrip length leads to a transmitting signal degradation of about 0.6 dB.
- Considering the TX1 (10x1 array) antenna in the AWR1843 board, it has been noticed the presence of an anomalous peak in the radiation pattern due to the antenna coupling. The measured maximum Received Power from the target when the TX1 is used gains a factor of 1.5 dB.
- As reported in [23], Texas Instruments pointed out that the AWR2944 chip is affected by a gain droop of about 6 dB in the full operating frequency range due to the LO. At 81 GHz, Texas Instruments reports that the gain value could be 5 dB lower than the programmed one. As consequence of that, a gain drop of 5 dB in the full operative frequency range has been considered.
- As reported in [23], the AWR2944 chip is affected by mismatching to the RX input pins; the S11 parameter does not match the -10 dB target condition. At 81 GHz, the S11 parameter reported by Texas Instruments is equal to -4 dB, which leads to a 1.8 dB of Received Power loss with respect to the AWR1843 chip considering the -10 dB condition successfully achieved in the latter platform.

The obtained differences from the measured results between the two systems are compliant to the expected values by taking into account the considerations above.

In the following is analyzed the comparison between the results obtained from the two transmitting antennas mounted on the same system. It is possible to notice that, the result obtained from the 10x10 antenna array mounted on the AWR2944 board gains 6.7 dB with respect to the result obtained using the 10x1 transmitting antenna array. Theoretically, the 10x10 antenna array should gain a factor of 10 dB than the 10x1 antenna array, but the longer microstrip length of the TX4 with respect to the TX1 limits the gain factor. The microstrip length difference between the TX1 and TX4 is 3 cm, which leads to a further signal attenuation for the 10x10 transmitting antenna array of 2.4 dB. Considering also an estimation of 1 dB loss due to the beamforming network, the measured gain difference is compliant to the expectation.

The result obtained from the AWR1843 board shows a different trend. The gain difference between the 10x10 antenna array and the 10x1 antenna array is lower than the AWR2944 board. In particular, the AWR1843 measurements report that this difference is equal to 4.7 dB. This behavior is dictated by the presence of the anomalous peak as stated before.

The second measurement part has been devoted in Noise Floor level comparison between the two boards. The following figures show the value of the Received Power at the target range bin averaged for 100 frames, corresponding to 10 seconds, using the absorbing material in front of the antennas. Also for these measurements the second receiving antenna has been used in both systems.

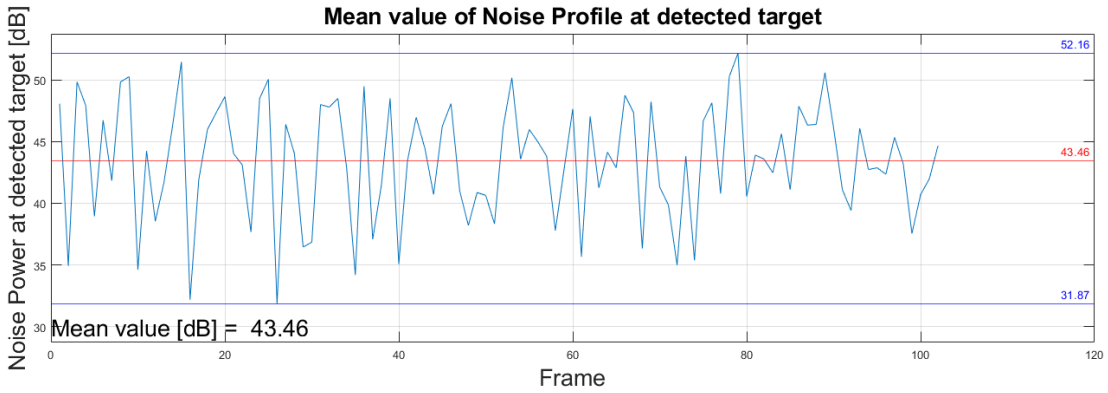

Figure 6.9: AWR2944 Noise Floor measurement, Received Power at target bin averaged for 100 frames

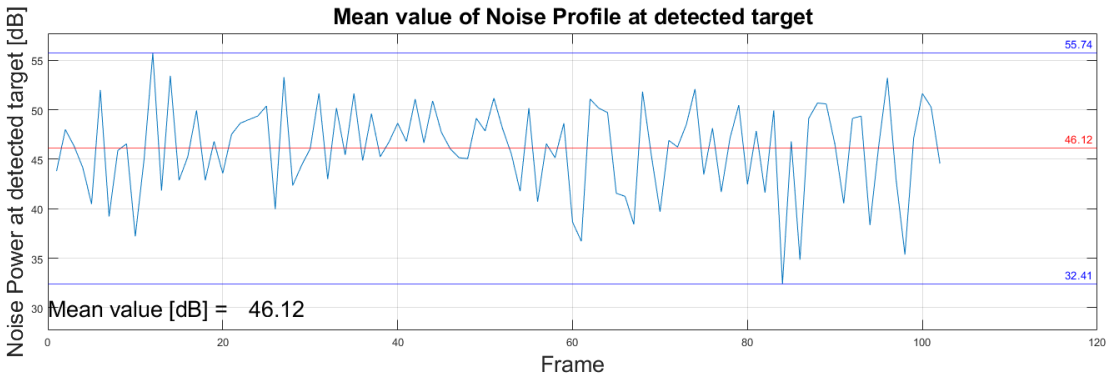

Figure 6.10: AWR1843 Noise Floor measurement, Received Power at target bin averaged for 100 frames

The measured Noise Floor level difference between the two systems is 2.7 dB in favor of the AWR2944 one.

Table 6.3 summarizes the Signal-to-Noise ratio computed from the results of the previous tests. It has been calculated as the difference between the Received Power and the Noise Floor level, which have been previously examined. The AWR2944 measurements used in this analysis have been corrected by adding the 6.8 dB of loss contributions on the Received Power in both the transmitting antennas measurements. The AWR1843 measurement taken with the 10x1 transmitting antenna has been corrected by subtracting 1.5 dB on the Received Power due to the contribution of the anomalous peak.

PLATFORM	TX ANTENNA	SNR	UNIT
AWR2944	10x1 array	45.7	dB
AWR2944	10x10 array	52.4	dB
AWR1843	10x1 array	43.5	dB
AWR1843	10x10 array	49.7	dB

Table 6.3: SNR obtained from measurements

Based on the results shown above, the SNR improves by a factor of 2.2 dB in favor of the AWR2944 chip when the 10x1 transmitting antenna array results are considered. In the other case, when the 10x10 transmitting antenna array results are examined, the measured SNR of the AWR2944 chip improves by a factor of 2.7 dB with respect to the AWR1843 chip.

Future improvements will be be achieved for the AWR2944 project discussed in this thesis work. They are listed below:

- The development of a custom software in order to handle the Minimum Redundancy MIMO and make the AWR2944 board working properly for the selected application.
- Memory footprint adjustment to solder the memory directly on the AWR2944 board without the usage of the memory adapter.
- Replace the on-board memory with the GD25B64C 64 M-bit memory as in the AWR2944EVM reference project.
- Routing the MSS_UARTA_TX and MSS_UARTA_RX pins in order to be able to program the external memory directly with the custom board.

Appendix A

Project Schematic

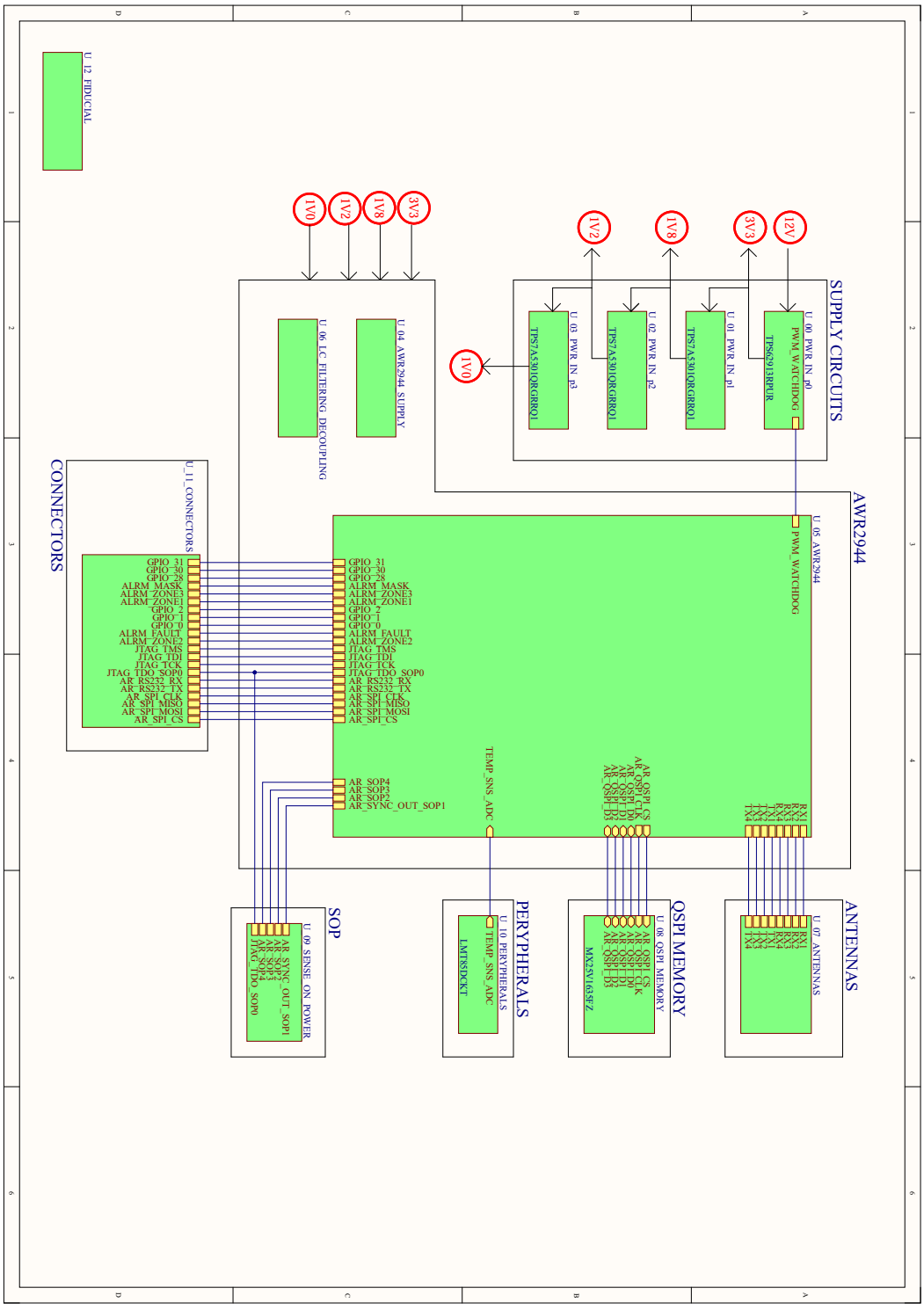

Figure A.1: Top level project schematic

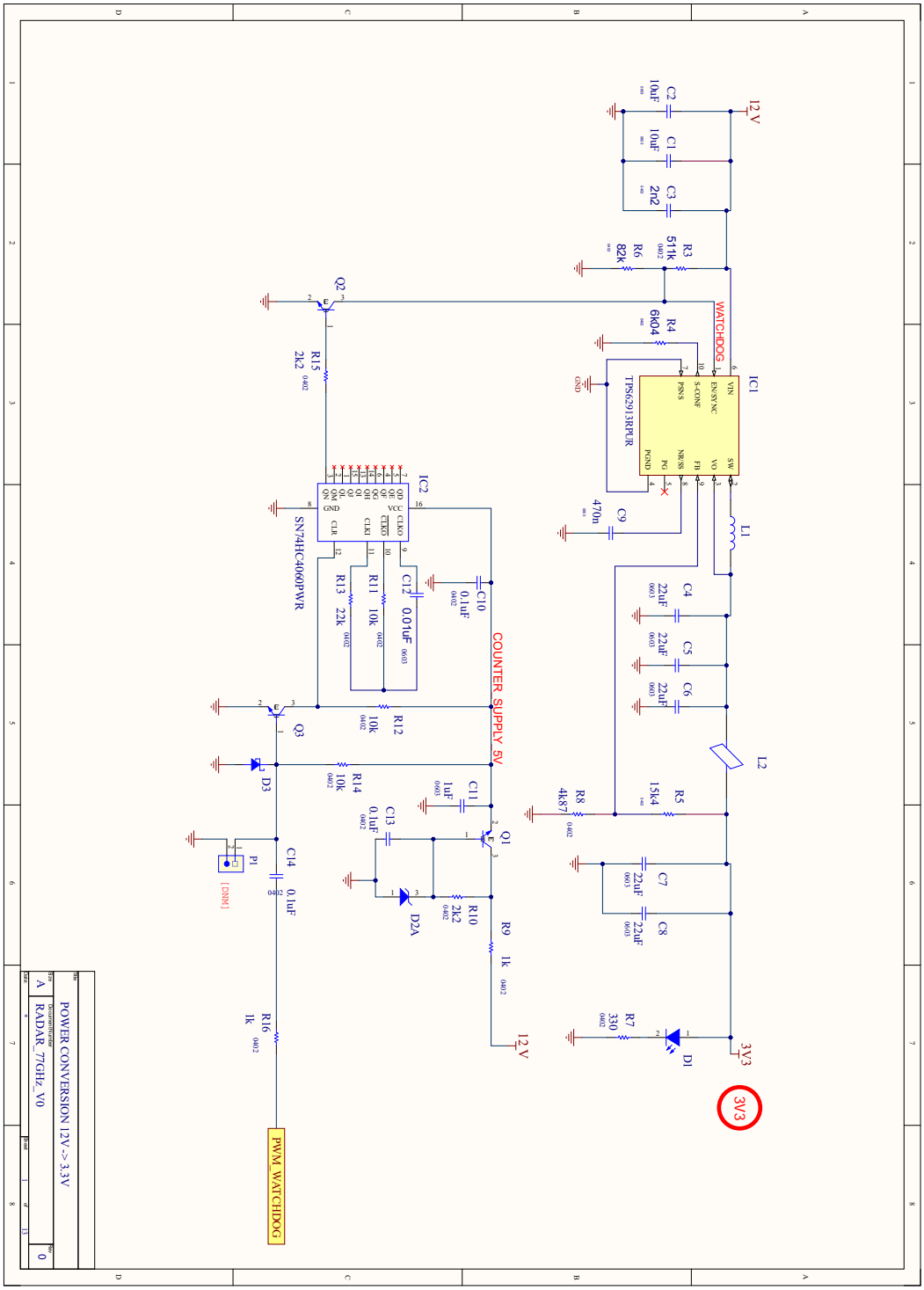

Figure A.2: 12V to 3.3V conversion schematic

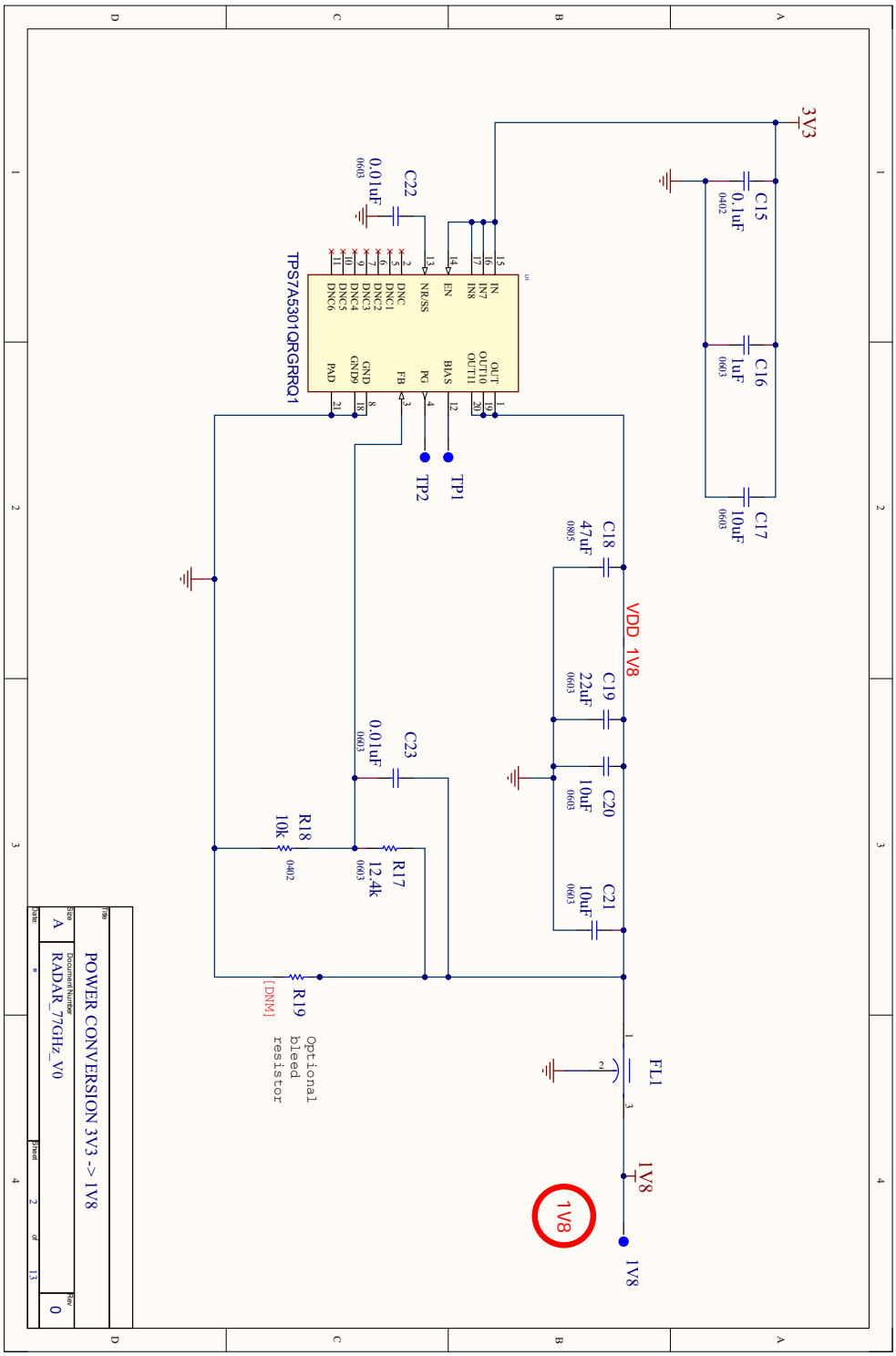

Figure A.3: 3.3V to 1.8V conversion schematic

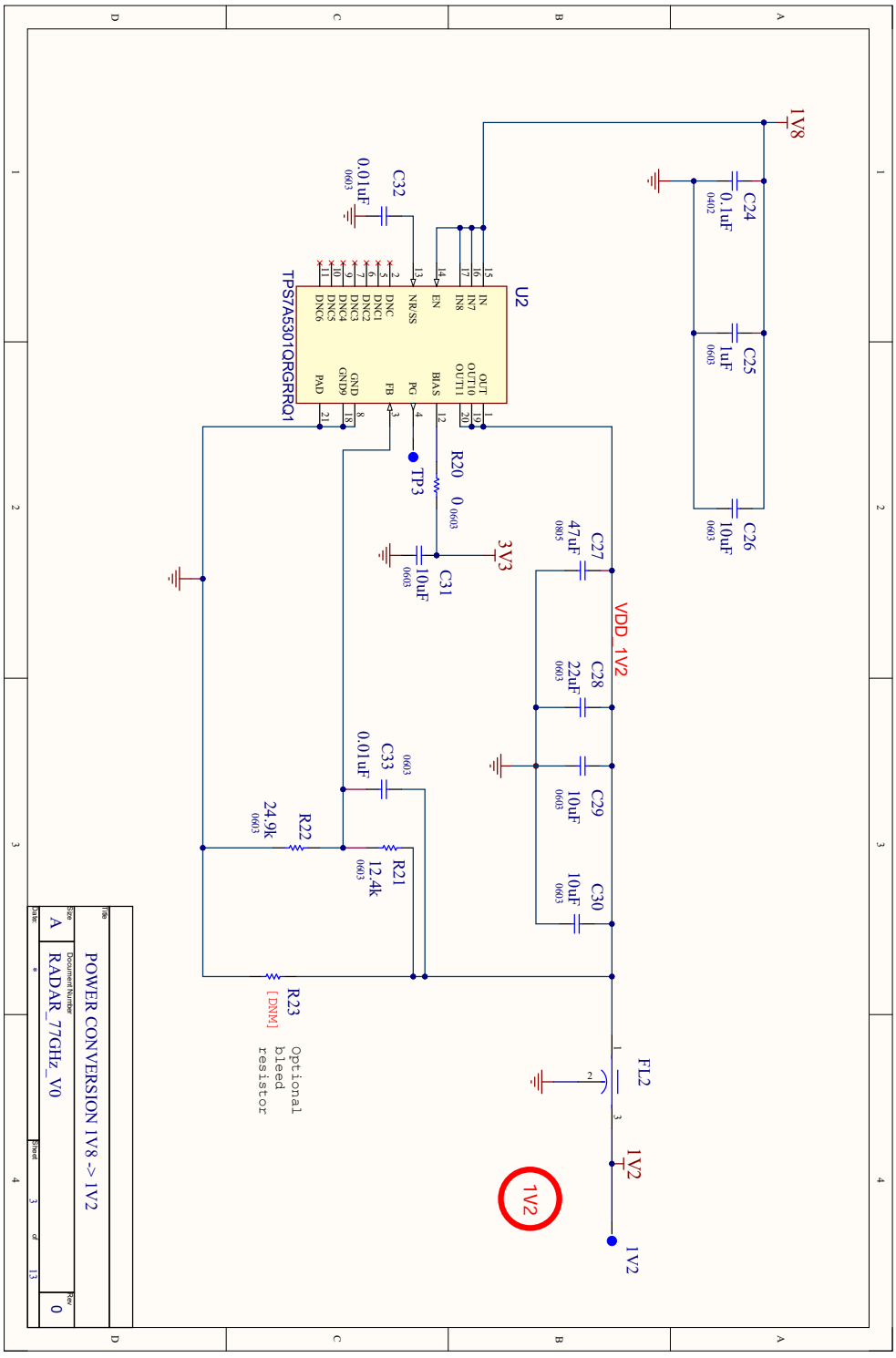

Figure A.4: 1.8V to 1.2V conversion schematic

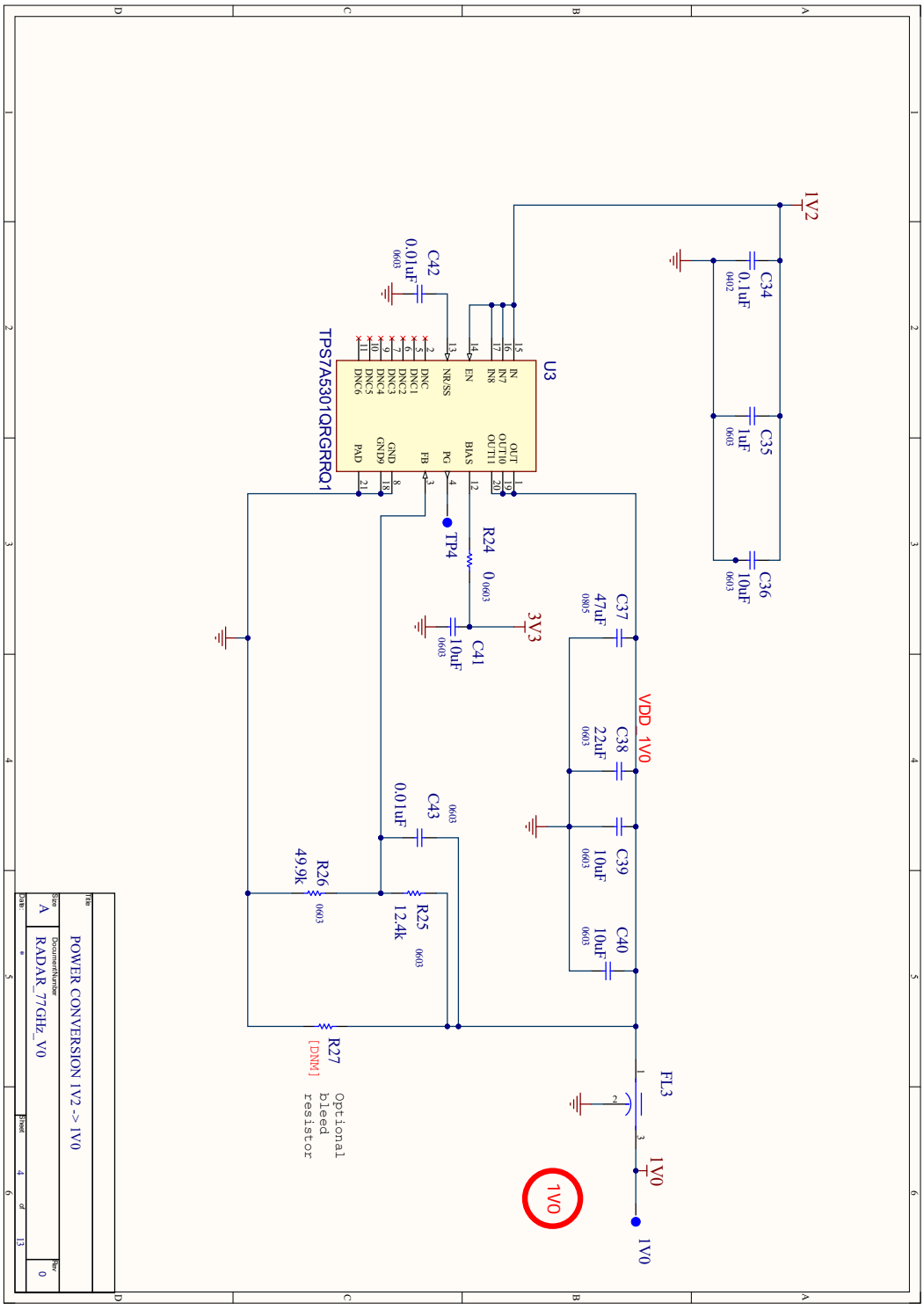

Figure A.5: 1.2V to 1.0V conversion schematic

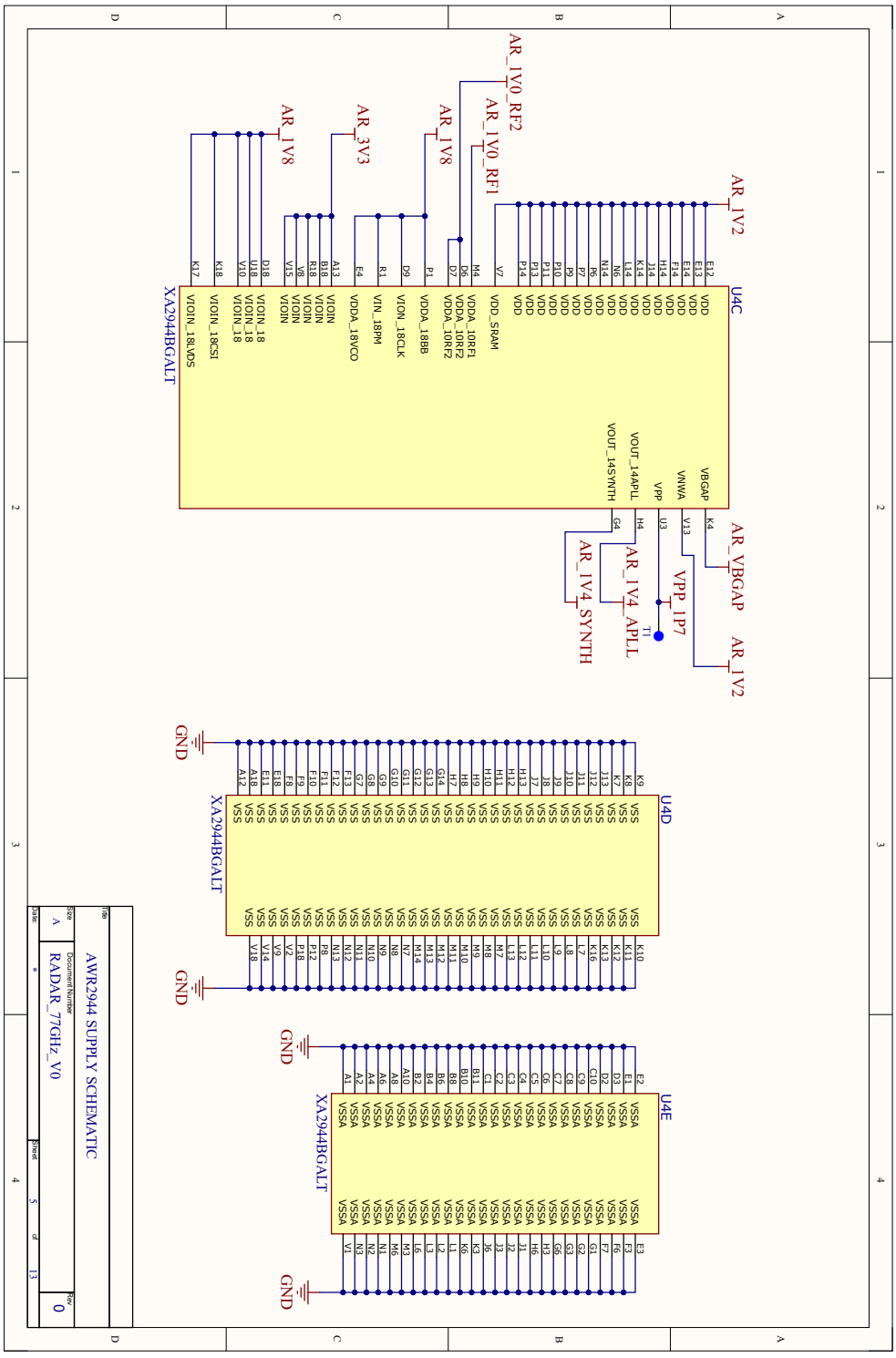

Figure A.6: AWR2944 power reference schematic

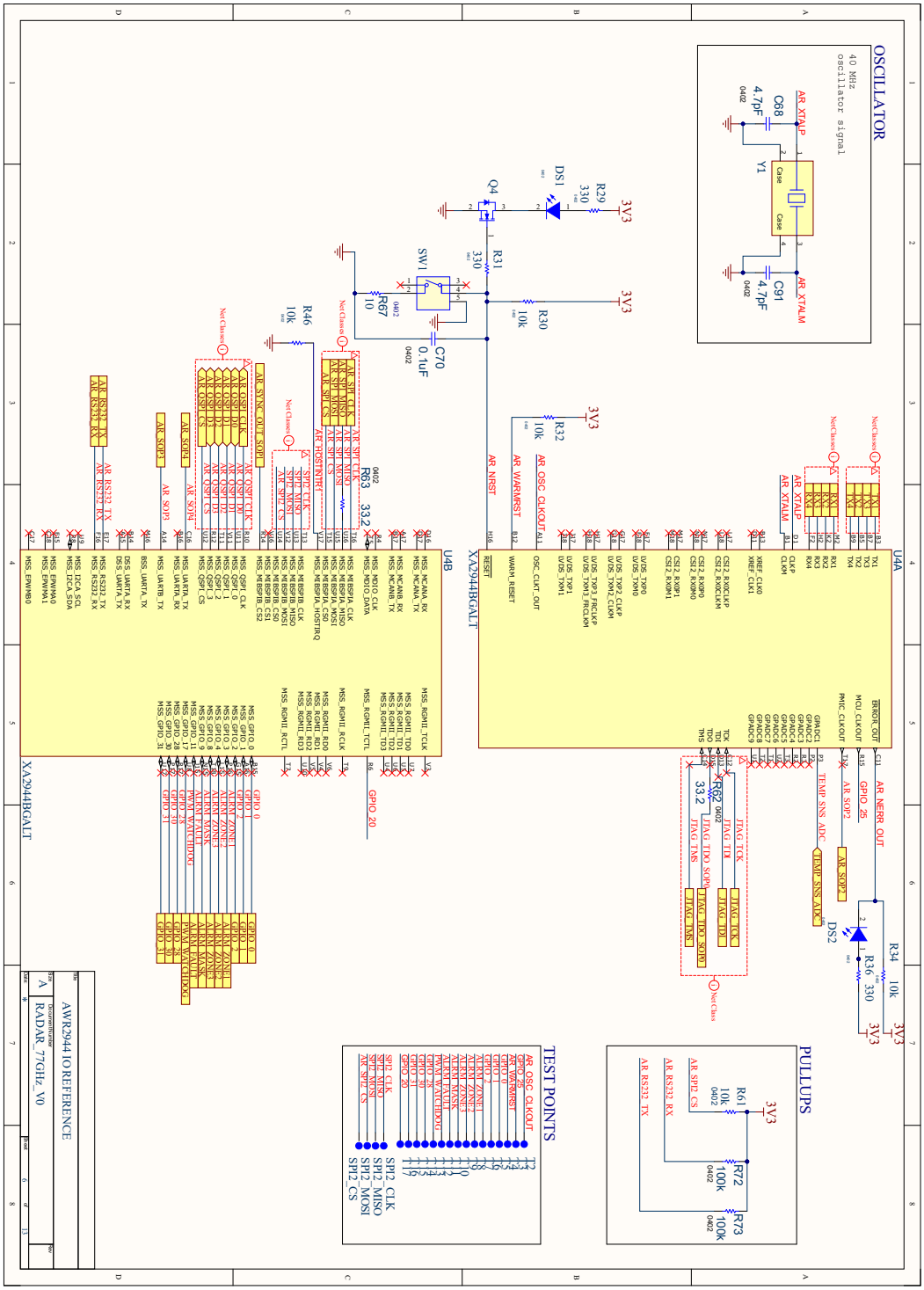

Figure A.7: AWR2944 I/O interconnections schematic

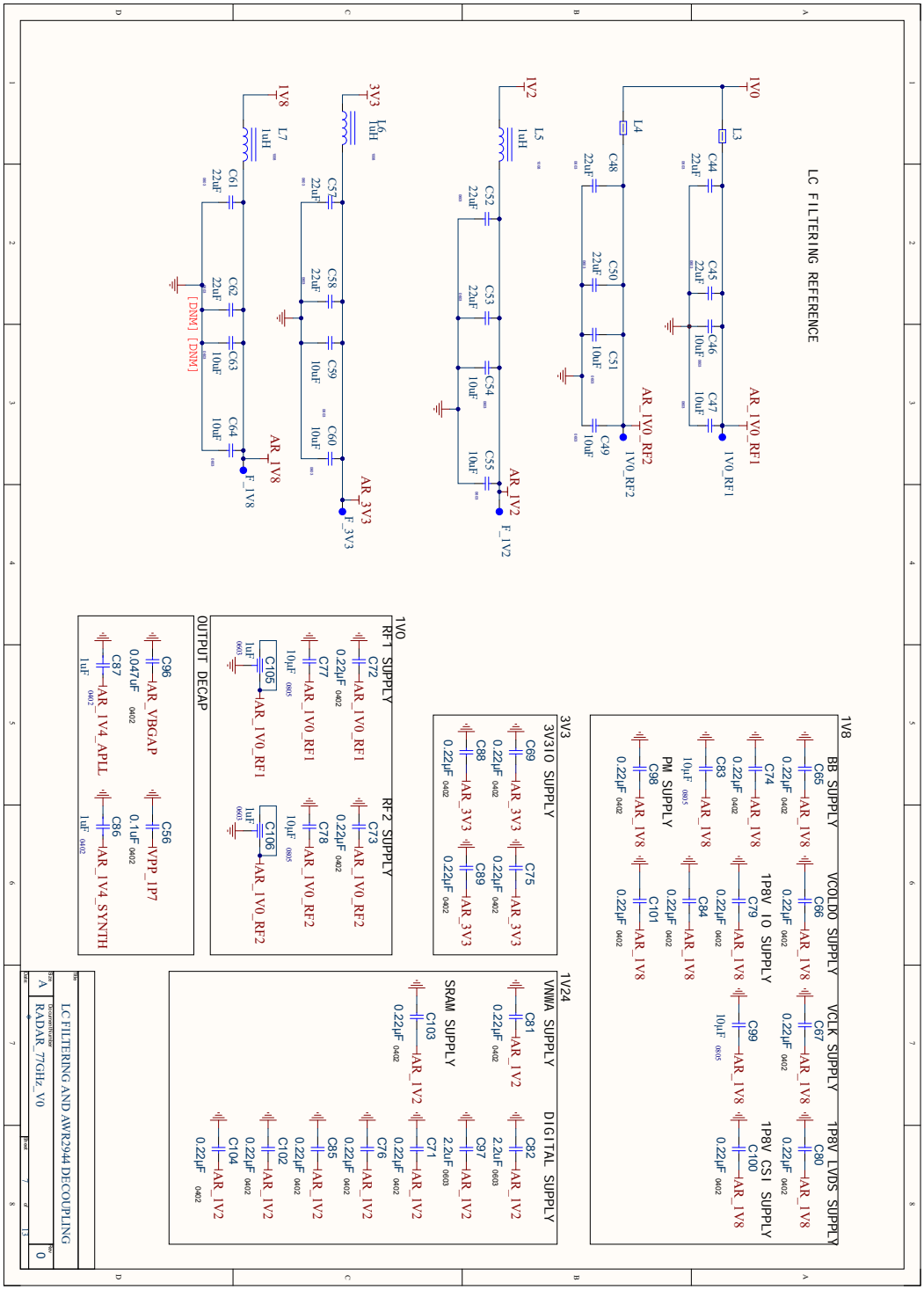

Figure A.8: Supply filtering and decoupling schematic

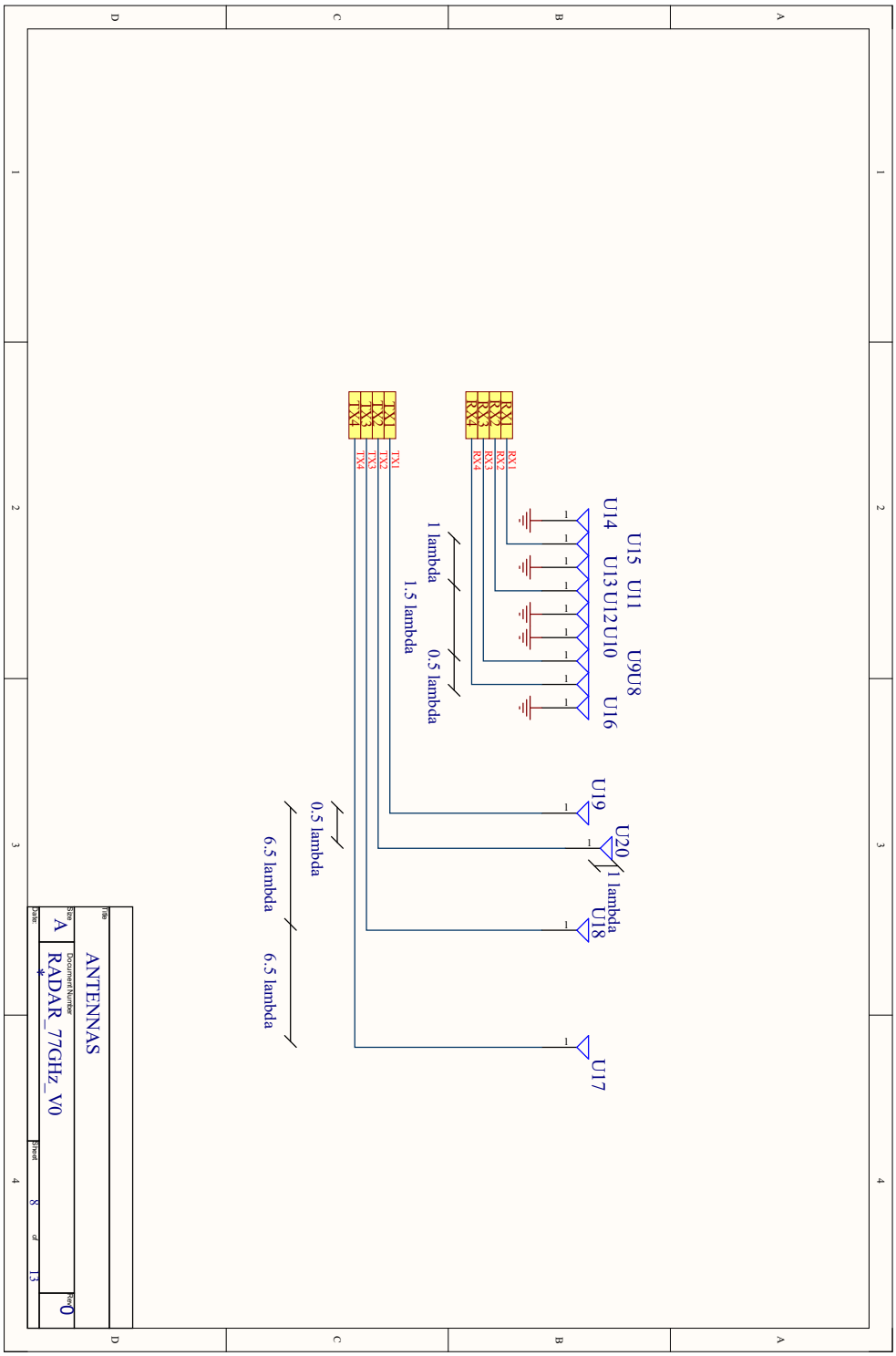

Figure A.9: Antennas schematic

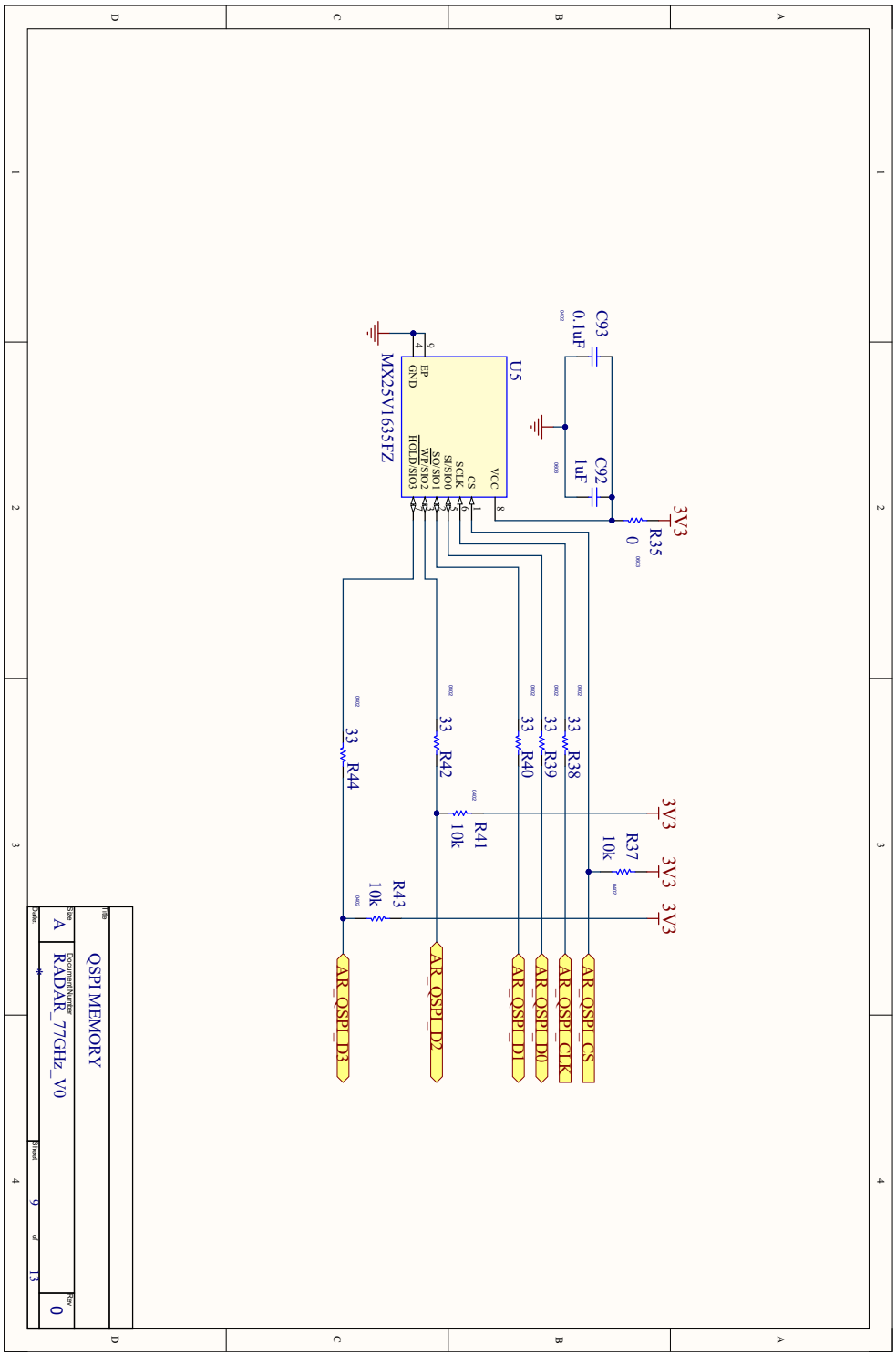

Figure A.10: QSPI memory schematic

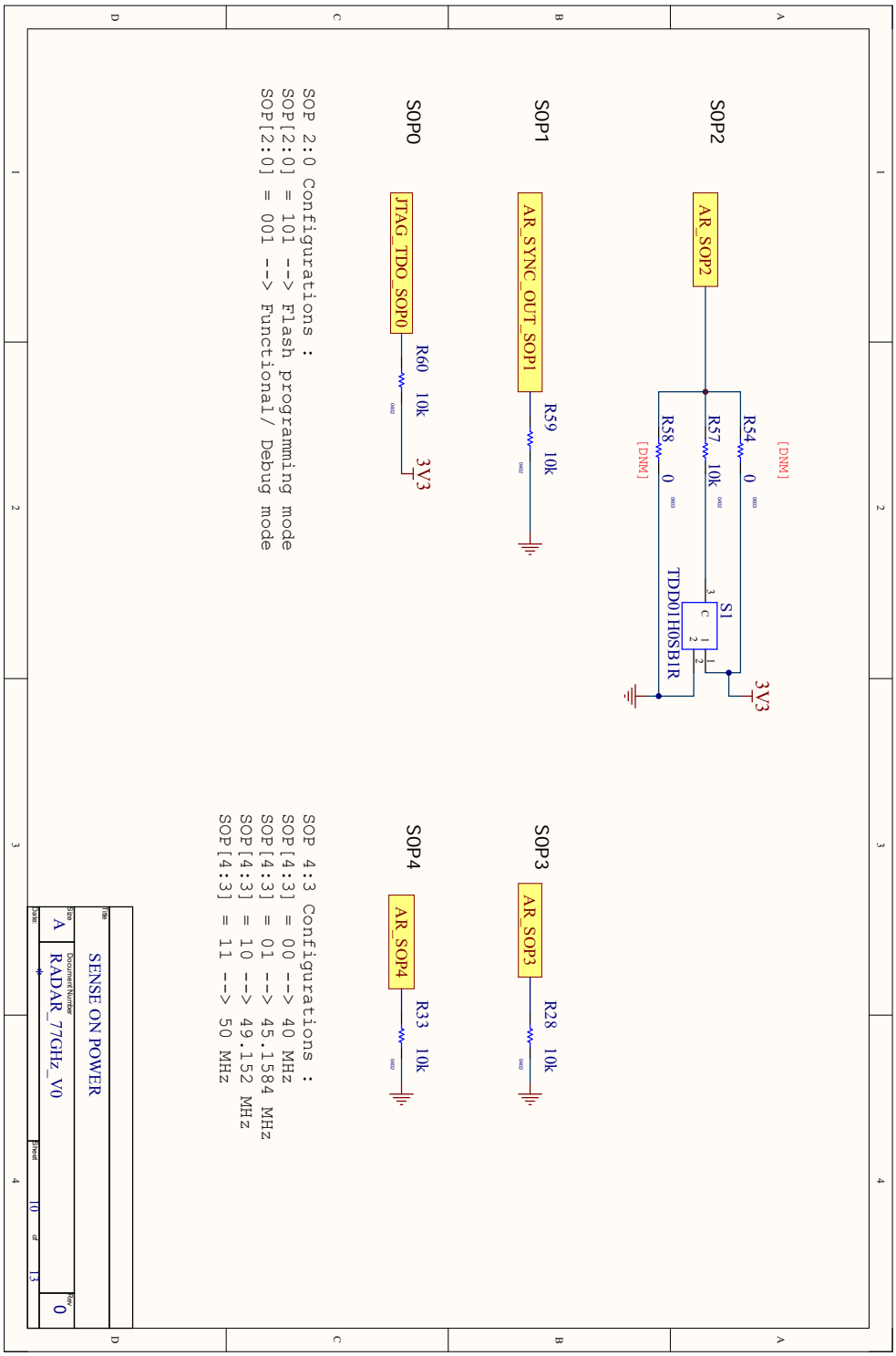

Figure A.11: Sense On Power schematic

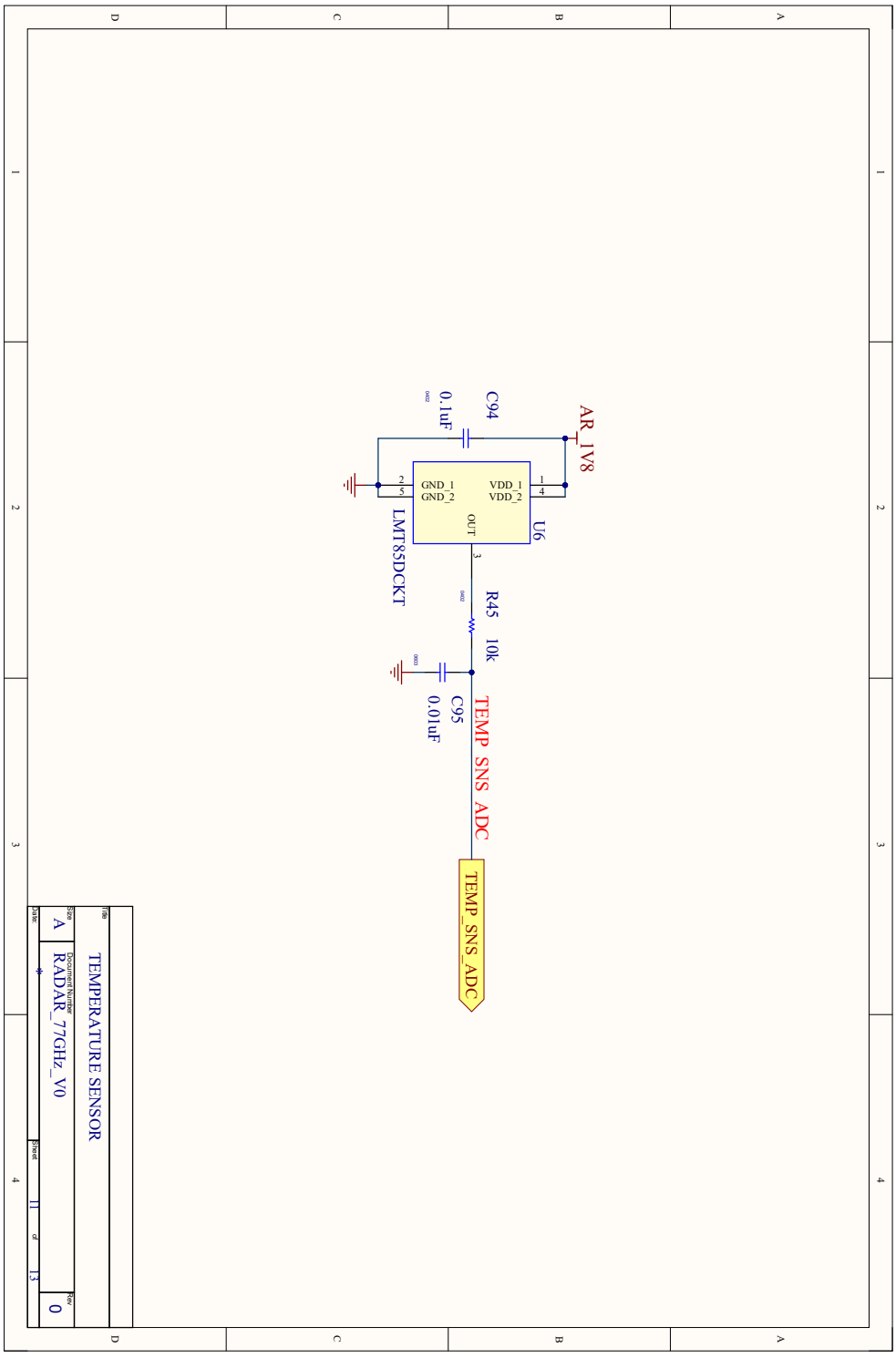

Figure A.12: Temperature sensor schematic

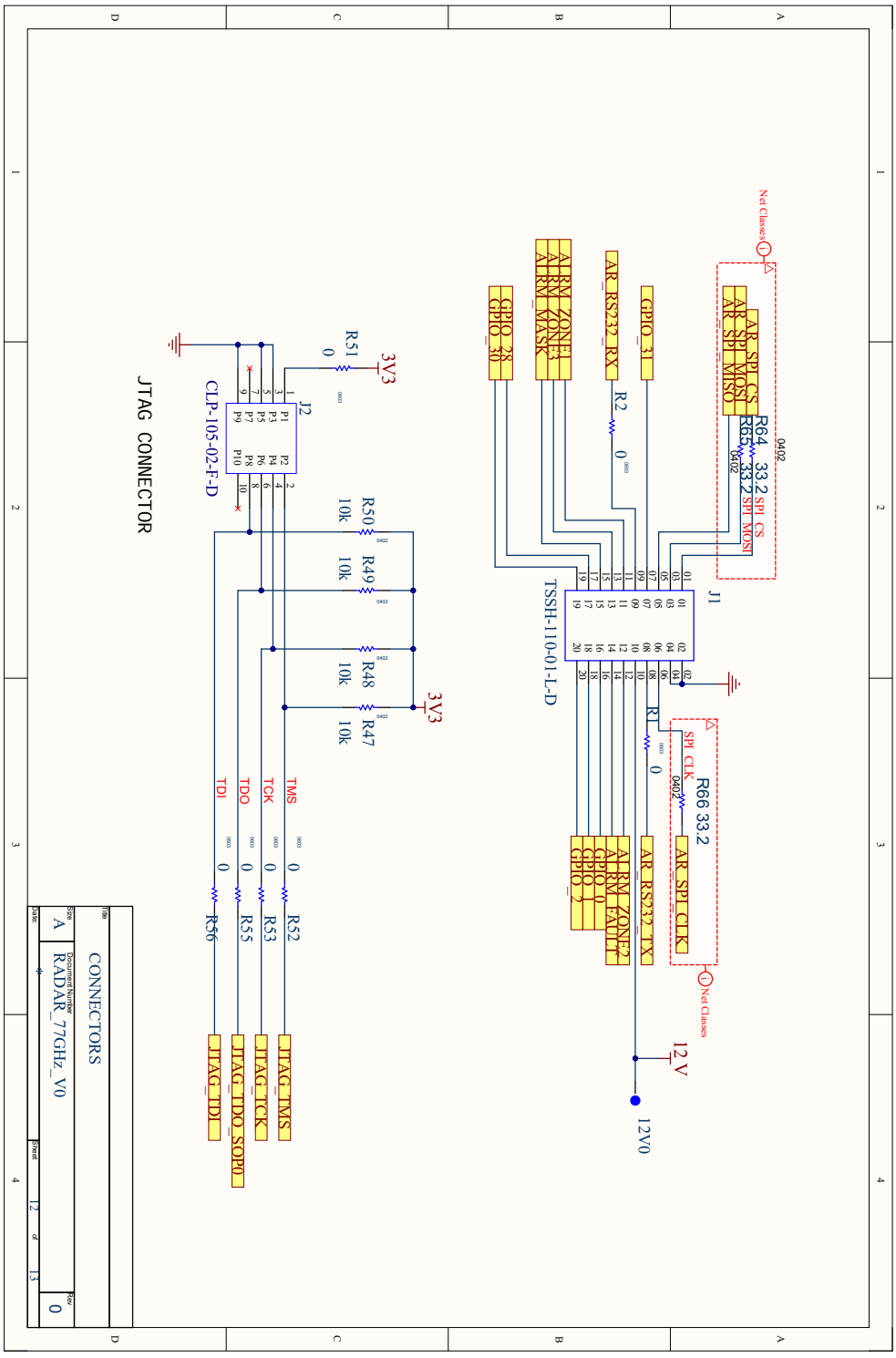

Figure A.13: Connectors schematic

Appendix B

Board Layout

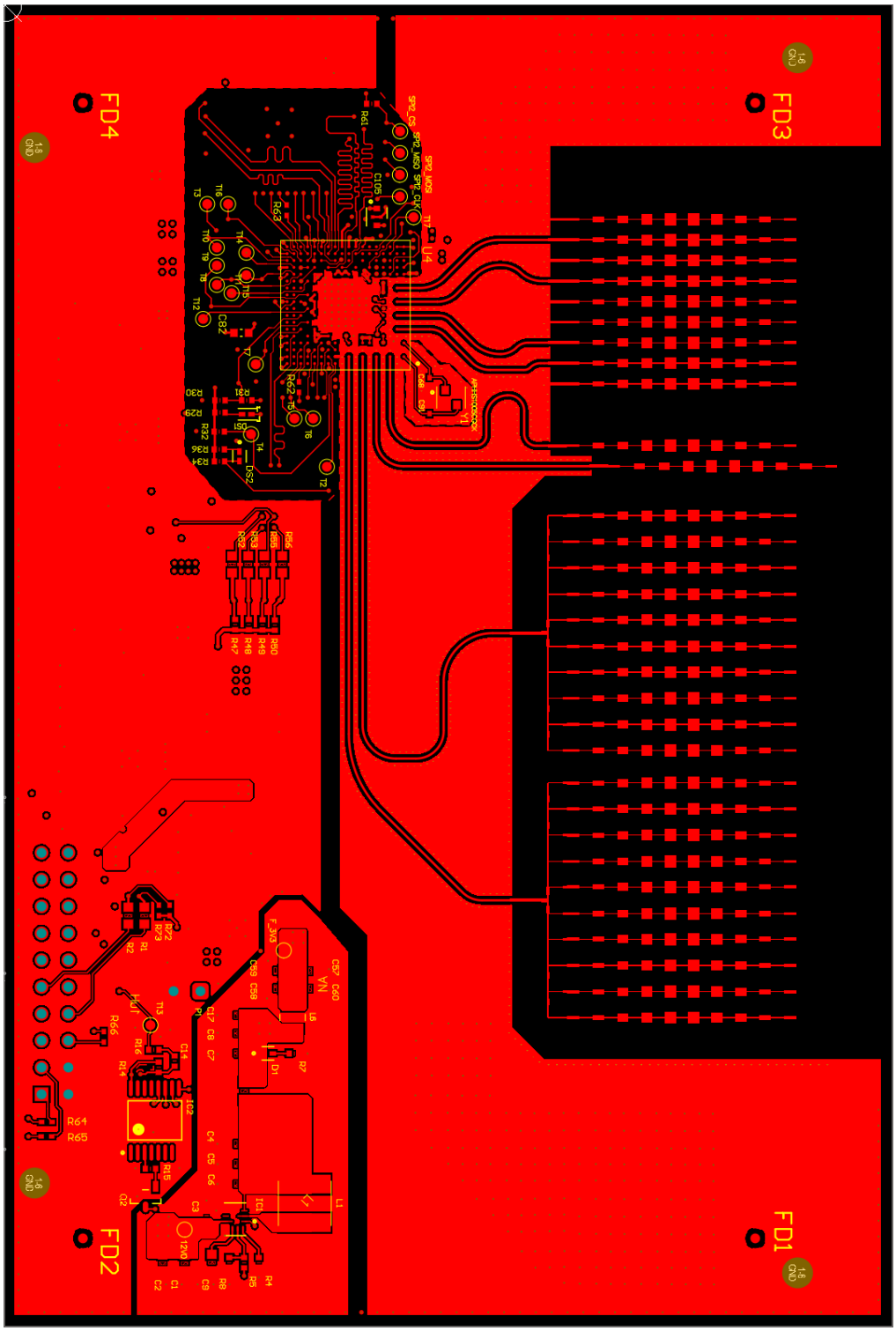

Figure B.1: Top layer layout

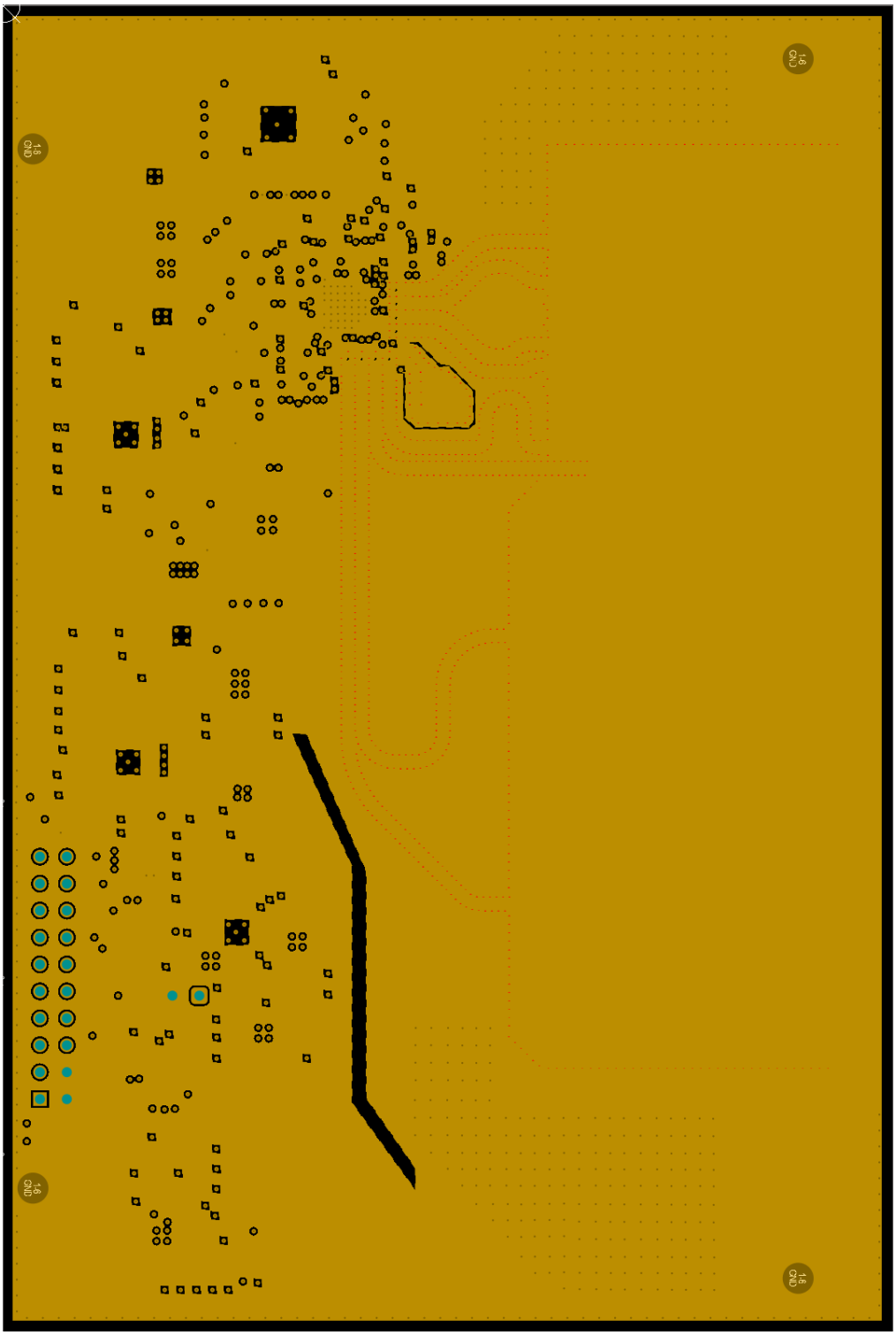

Figure B.2: Layer 2 layout

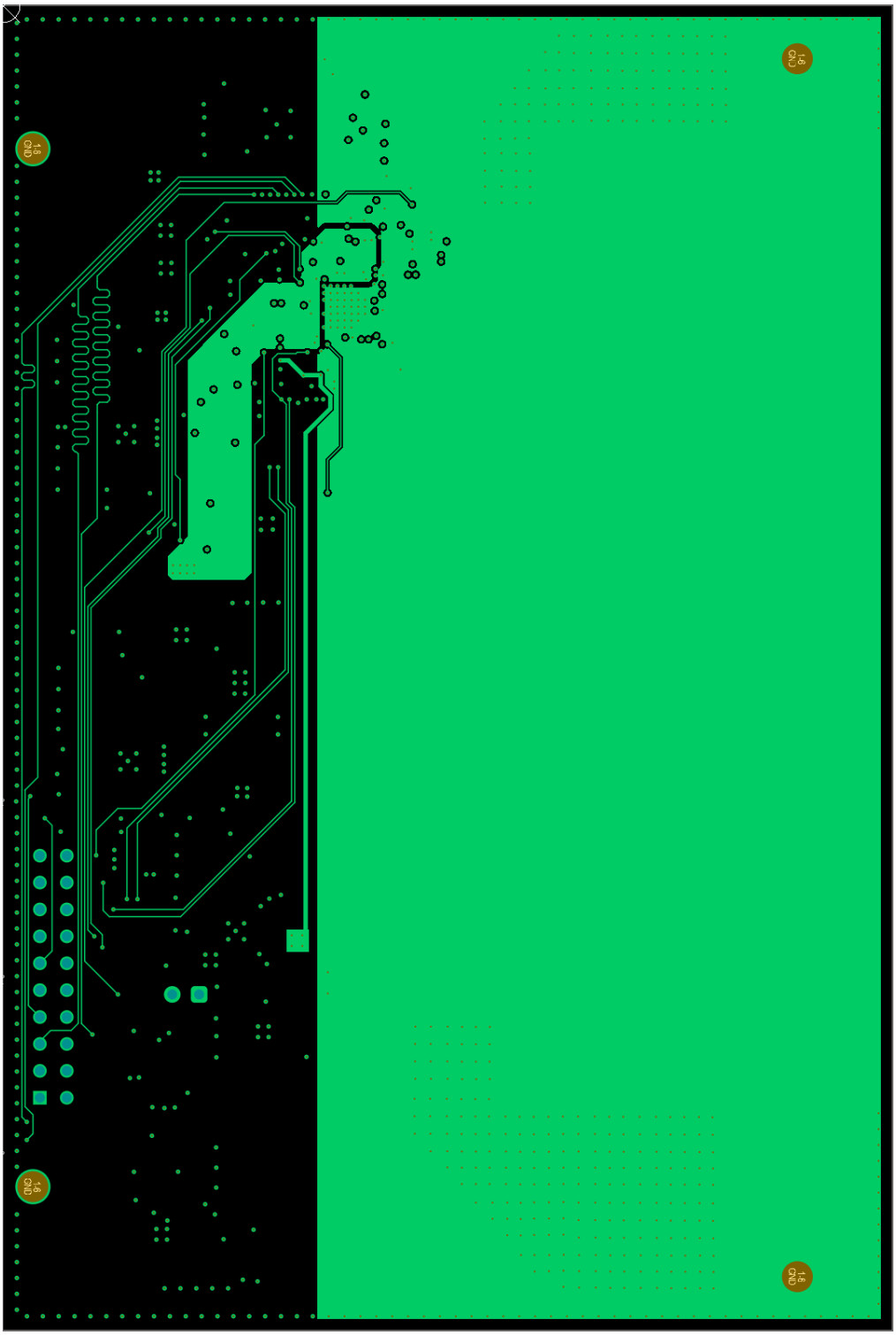

Figure B.3: Layer 3 layout

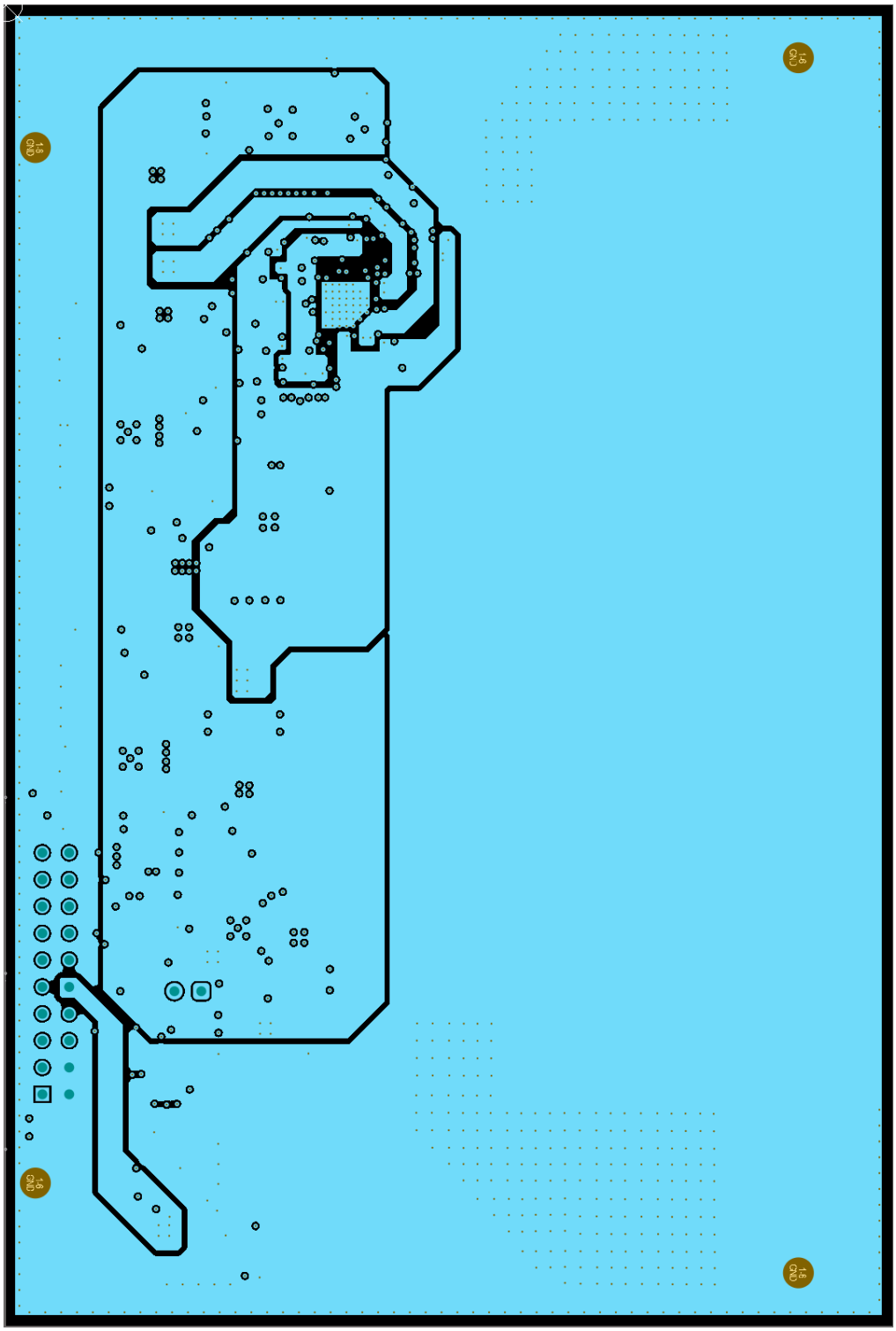

Figure B.4: Layer 4 layout

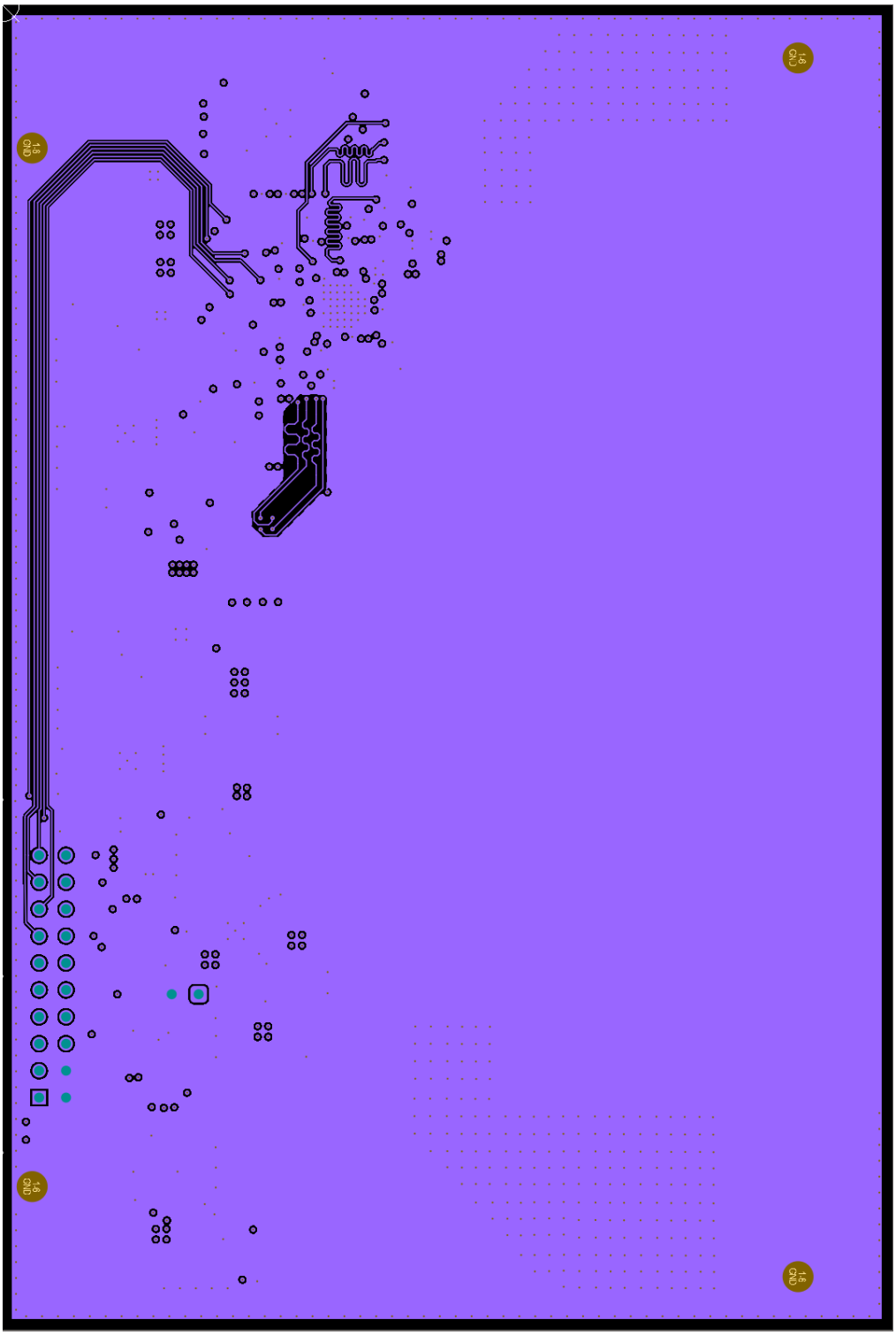

Figure B.5: Layer 5 layout

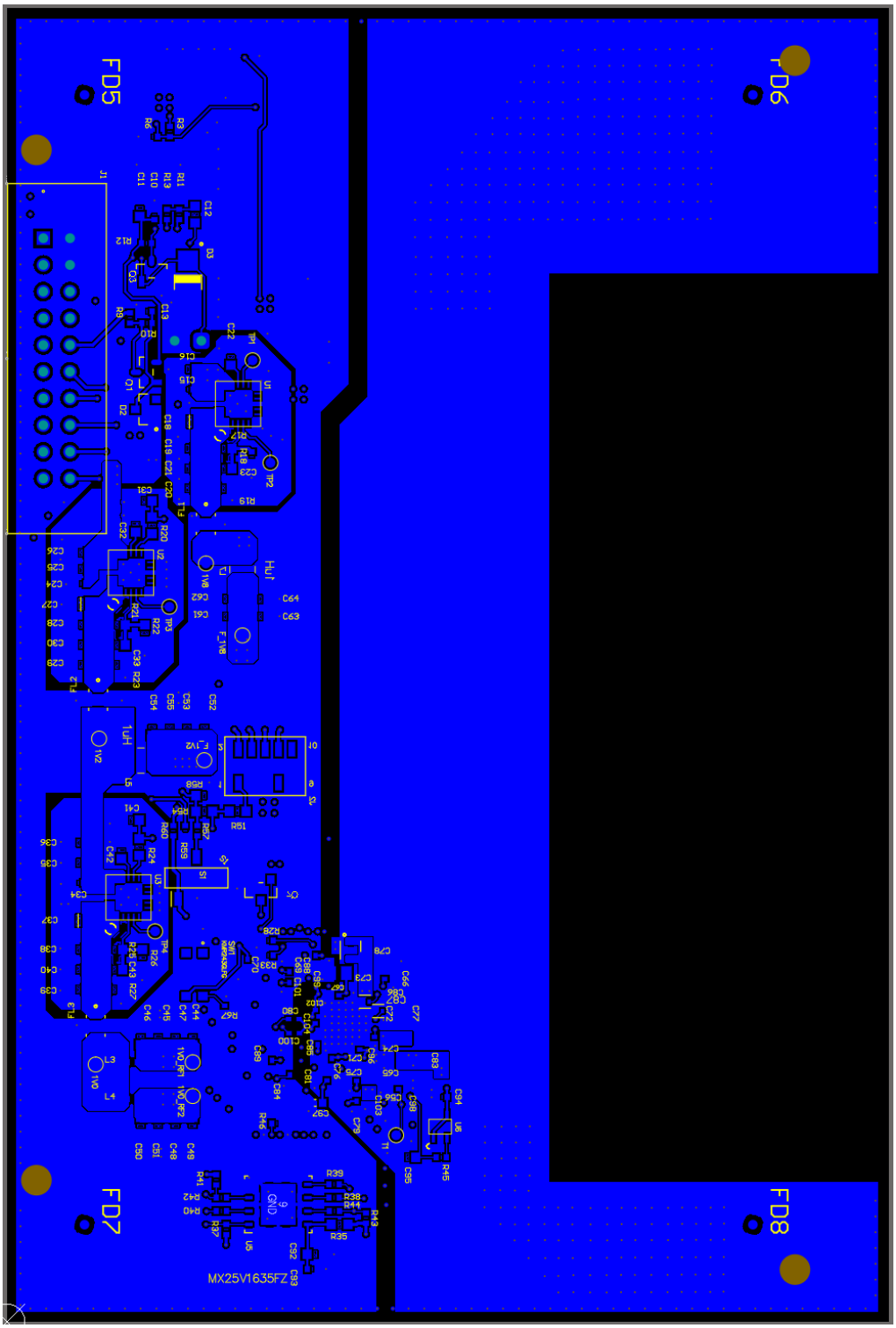

Figure B.6: Bottom layer layout

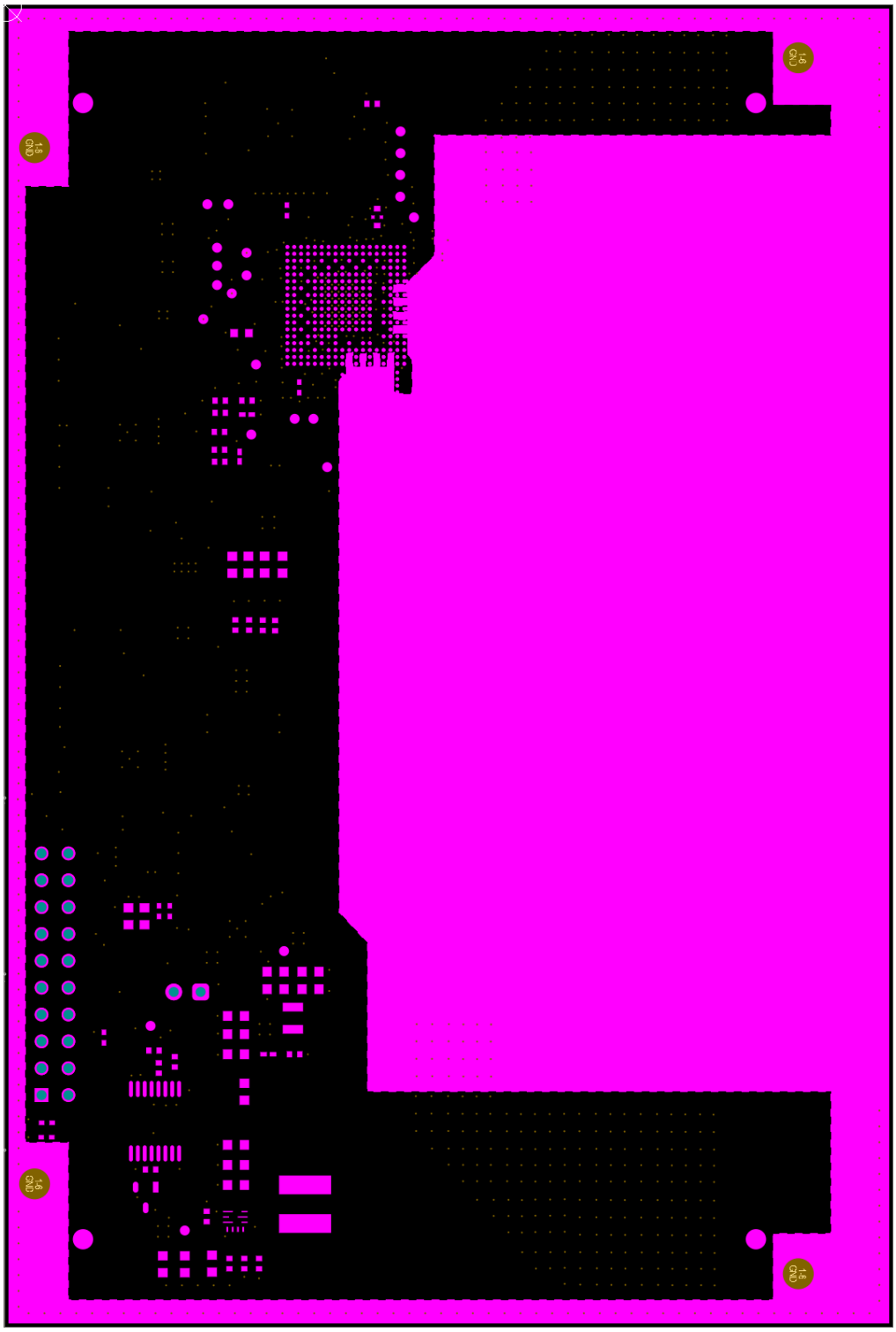

Figure B.7: Top solder mask layout

Figure B.8: Bottom solder mask layout

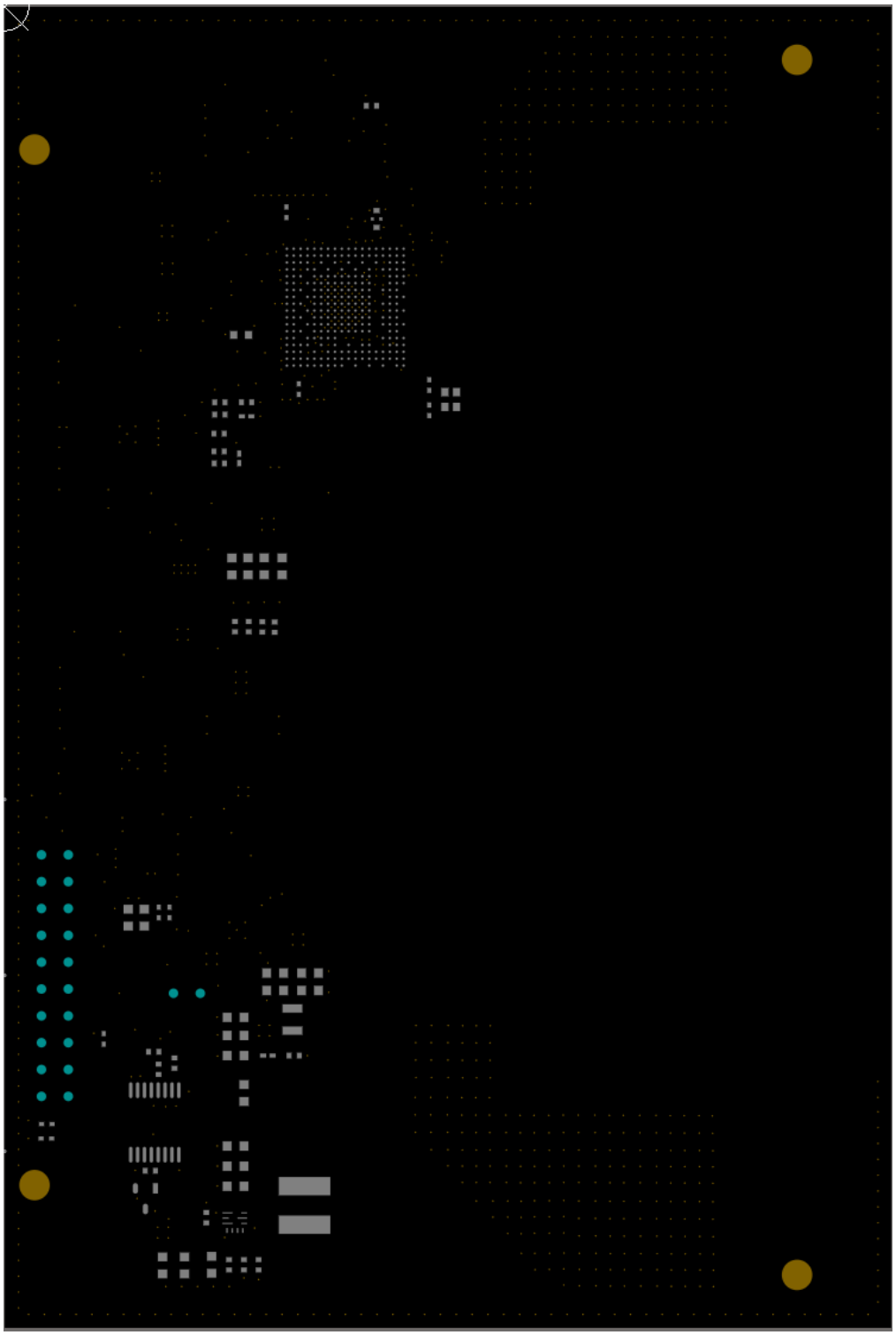

Figure B.9: Top paste mask layout

Figure B.10: Bottom paste mask layout

Appendix C

PDN Simulations

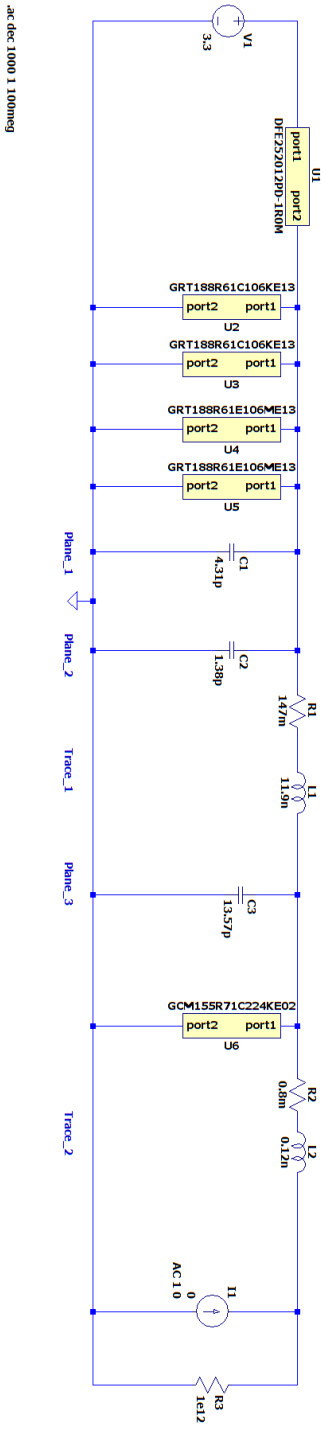

Figure C.1: 3.3V PDN schematic

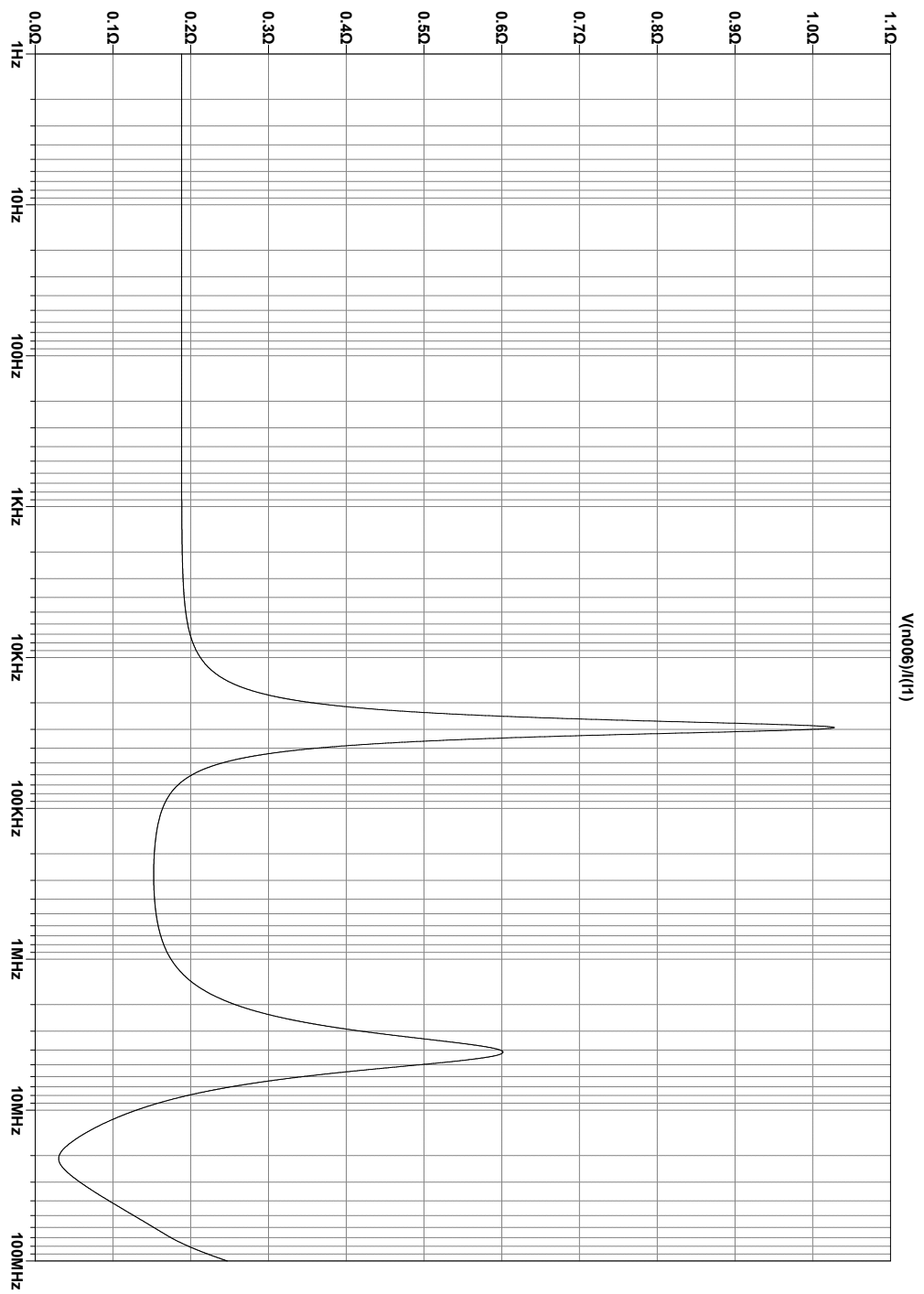

Figure C.2: 3.3V PDN simulation result

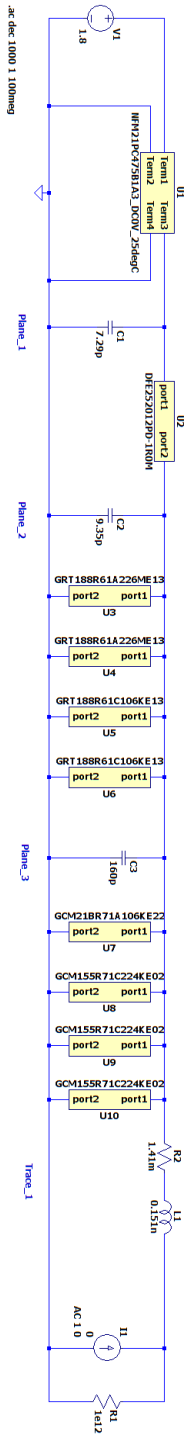

Figure C.3: 1.8V PDN schematic

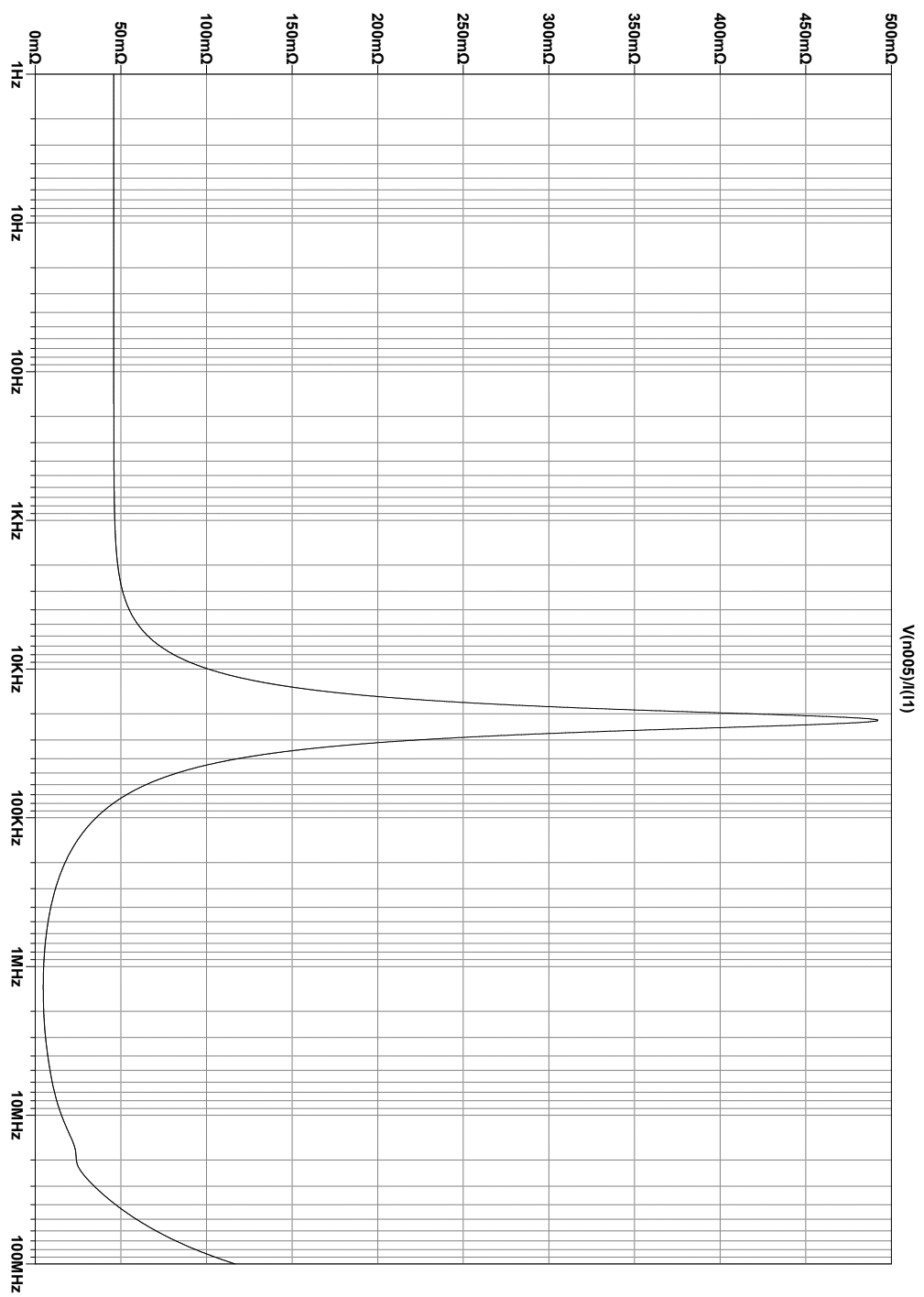

Figure C.4: 1.8V PDN simulation result

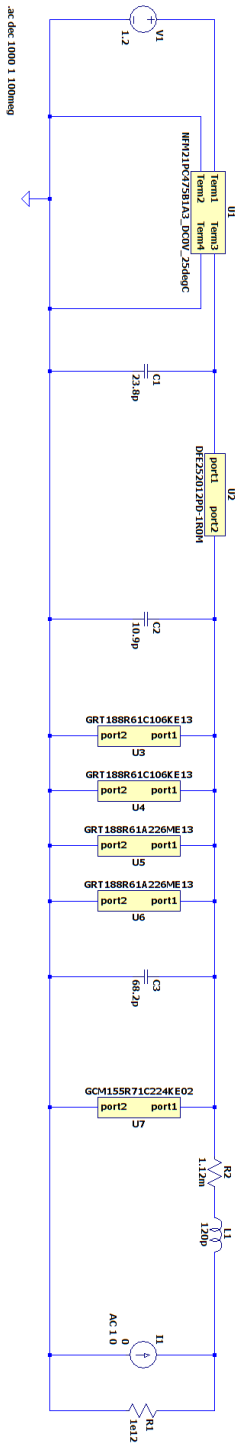

Figure C.5: 1.2V PDN schematic

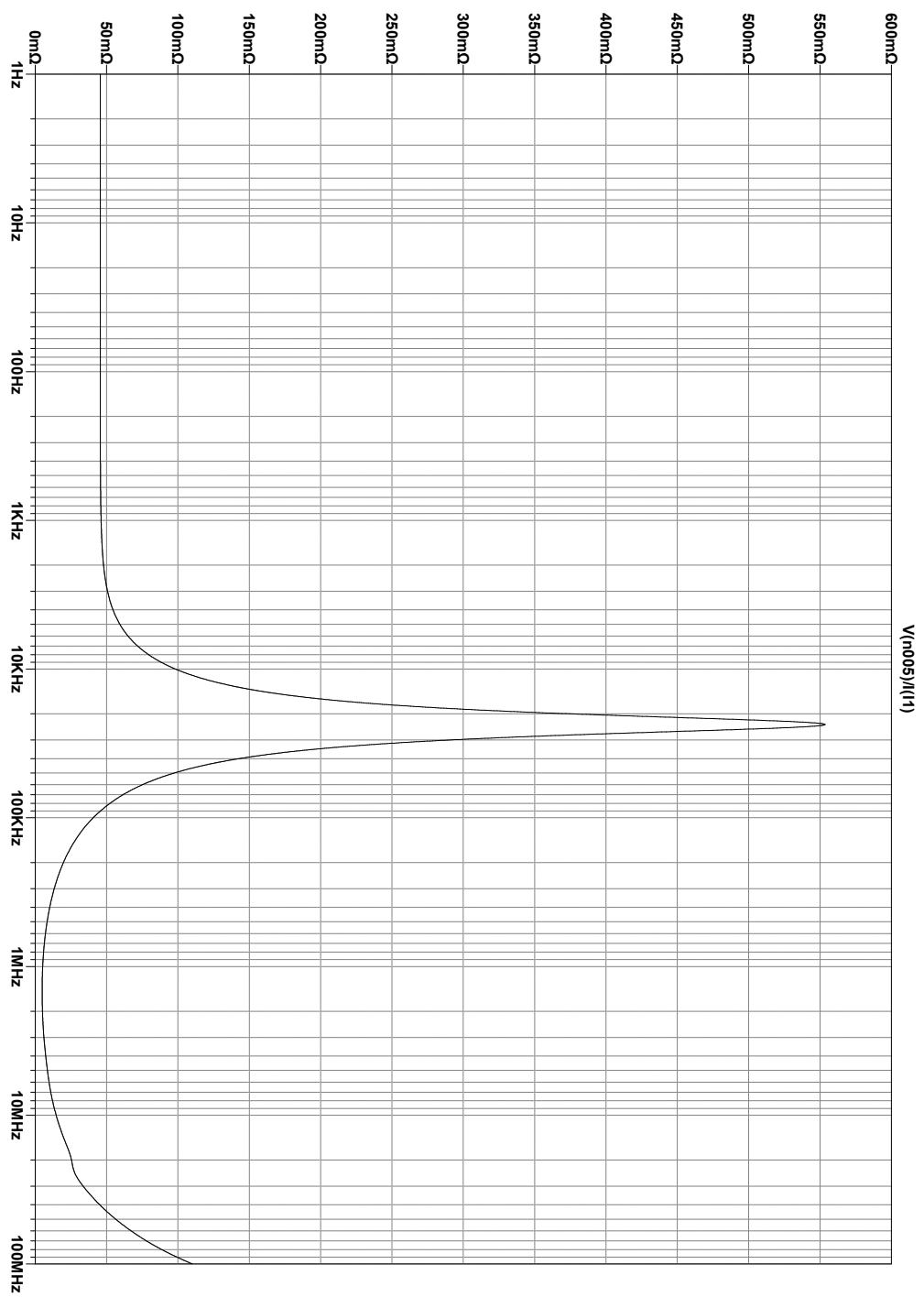

Figure C.6: 1.2V PDN simulation result

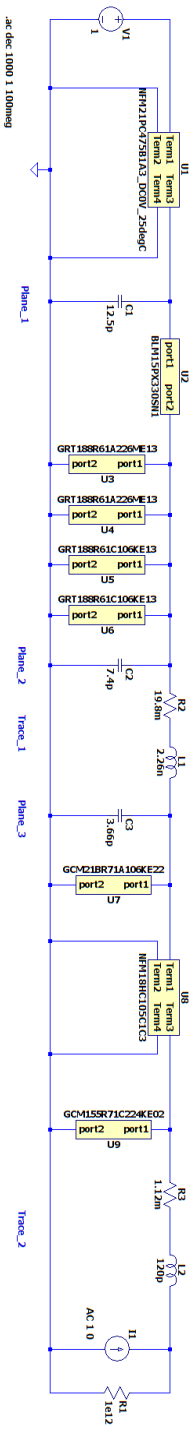

Figure C.7: 1.0V PDN schematic

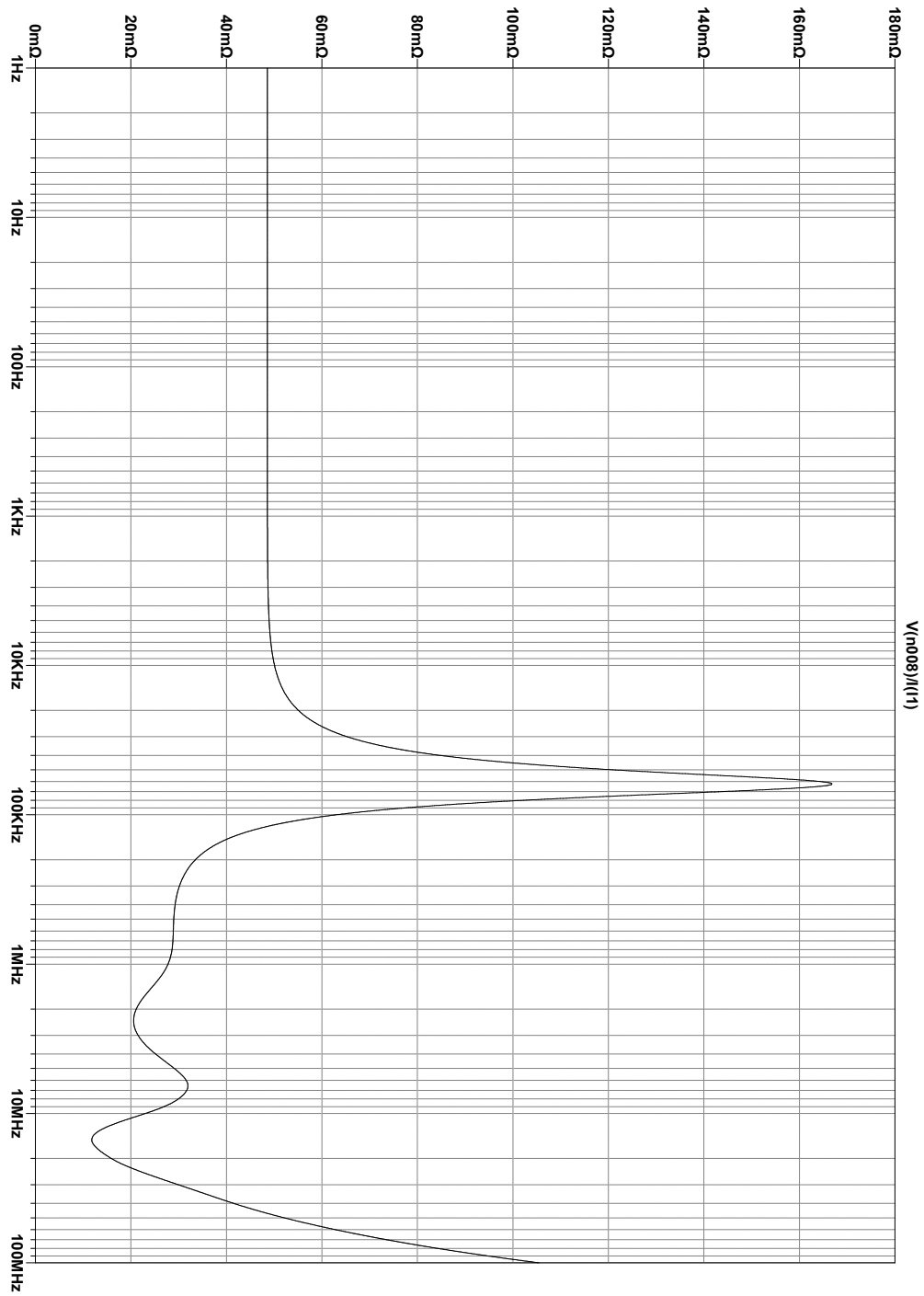

Figure C.8: 1.0V PDN simulation result

Bibliography

[1] Merrill I. Skolnik. *Introduction to radar systems*. McGraw-Hill, 1980 (cit. on pp. 1, 2, 4, 6, 8, 10, 15).

[2] L. Nicolaescu and T. Oroian. «Radar cross section». In: *5th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Service. TELSIKS 2001. Proceedings of Papers (Cat. No.01EX517)*. Vol. 1. 2001, 65–68 vol.1. DOI: 10.1109/TELSKS.2001.954850 (cit. on p. 6).

[3] Hans Steyskal. «Digital Beamforming». In: *1988 18th European Microwave Conference*. 1988, pp. 49–57. DOI: 10.1109/EUMA.1988.333796 (cit. on p. 7).

[4] Cesar Iovescu and Sandeep Rao. *The fundamentals of millimeter wave radar sensors*. Tech. rep. SPYY005A. MA: Texas Instruments: Texas Instruments, July 2020 (cit. on pp. 15–20).

[5] Sandeep Rao. *MIMO Radar*. Tech. rep. SWRA554A. MA: Texas Instruments: Texas Instruments, May 2017 (cit. on pp. 20–22).

[6] A. Moffet. «Minimum-redundancy linear arrays». In: *IEEE Transactions on Antennas and Propagation* 16.2 (1968), pp. 172–175. DOI: 10.1109/TAP.1968.1139138 (cit. on p. 23).

[7] Chun-Yang Chen and P. P. Vaidyanathan. «Minimum redundancy MIMO radars». In: *2008 IEEE International Symposium on Circuits and Systems (ISCAS)*. 2008, pp. 45–48. DOI: 10.1109/ISCAS.2008.4541350 (cit. on p. 23).

[8] Prajakta Desai. *How Radar is Displacing Traditional Technologies*. Tech. rep. SPRY346. MA: Texas Instruments: Texas Instruments, Mar. 2022 (cit. on p. 24).

[9] *AWR2944 Single-Chip 76- and 81-GHz FMCW Radar Sensor*. https://www.ti.com/lit/gpn/awr2944. Texas Instruments (cit. on pp. 25–30).

[10] Texas Instruments. *AWR2944EVM Schematic, Assembly, and BOM Files*. URL: https://www.ti.com/lit/zip/sprr440 (cit. on p. 32).

[11] *TPS6291x 3-V to 17-V, 2-A/3-A Low Noise and Low Ripple Buck Converter with Integrated Ferrite Bead Filter Compensation*. https://www.ti.com/lit/gpn/tps62913. Texas Instruments (cit. on pp. 35, 54).

[12] *TPS7A53-Q1 3-A, High-Accuracy, Automotive-Grade, Low-Noise, LDO Voltage Regulator*. https://www.ti.com/lit/gpn/tps7a53-q1. Texas Instruments (cit. on pp. 38, 39).

[13] Analog Devices. *LTspice*. URL: https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html (cit. on p. 43).

[14] muRata. *SimSurfing*. URL: https://ds.murata.co.jp/simsurfing/index.html?lcid=en-us (cit. on pp. 45, 67).

[15] Altium. *Altium Designer*. URL: https://www.altium.com/altium-designer/ (cit. on p. 49).

[16] Texas Instruments. *AWR2944 Hardware Design Checklist*. Mar. 2022. URL: https://www.ti.com/lit/zip/sprad30 (cit. on p. 49).

[17] Alexander Pakosta Alexander Weiler and Ankur Verma. *High-Speed Layout Guidelines*. Tech. rep. SCAA082A. MA: Texas Instruments: Texas Instruments, Nov. 2006 (cit. on p. 51).

[18] Bogatin Eric. *Signal and Power Integrity - Simplified*. Prentice Hall, 2018 (cit. on pp. 65–67).

[19] Saturn PCB Design, Inc. *Saturn PCB Design Toolkit Version 8.21*. URL: https://saturnpcb.com/saturn-pcb-toolkit/ (cit. on p. 68).

[20] *MMWAVE MCUPLUS SDK User Guide (4.2.0)*. https://dr-download.ti.com/software-development/software-development-kit-sdk/MD-U4MY7aGNn5/04.02.00.03/mmwave_mcuplus_sdk_user_guide.pdf. Texas Instruments (cit. on pp. 74, 80, 81).

[21] *Nyquist–Shannon sampling theorem*. https://en.wikipedia.org/wiki/Nyquist%E2%80%93Shannon_sampling_theorem. Wikipedia (cit. on p. 87).

[22] *RO3003G2 Circuit Materials*. https://www.rogerscorp.com/-/media/project/rogerscorp/documents/advanced-electronics-solutions/english/data-sheets/ro3003g2--data-sheet.pdf. ROGERS (cit. on p. 91).

[23] *AWR2944 Device Errata Silicon Revisions 1.0*. https://www.ti.com/lit/pdf/swrz102. Texas Instruments (cit. on p. 91).