POLITECNICO DI TORINO

Master degree in Electronic Enginnering

Master Degree Thesis

Design and characterization of a EMI filter for a switching DC-AC converter installed in an innovative agricultural machinery

Politecnico di Torino

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Acronyms

IL Insertion Loss

NA Network Analyzer

PCB Printed Circuit Board

CM Common Mode

DM Differential Mode

CMC Common Mode Choke

NA Network Analyzer

SNA Scalar Network Analyzer

VNA Vector Network Analyzer

DUT Device Under Test

ESR Equivalent Series Resistance

ESL Equivalent Series Inductance

PMSM Permanent Magnet Synchronous Motor

VSI Voltage Sourced Inverter

SVPWM Space Vector Pulse Width Modulation

MTL Multiconductor Transmission Lines

Chapter 1

Introduction

This project focuses on the electromagnetic compatibility, needed in modern high-frequency switching electronics circuits to comply with normatives. This topic is important in order to assure that electronic systems work correctly in the electromagnetic environment in which they operate without generating too much unintentional radiation and continuing to function in presence of unwanted interference. More specifically, this Thesis deals with the conducted emission generated by the operation of three-phase inverters.

This work is part of the MArcEL (Macchine Agricole ELettriche) project, founded by the Regione Piemonte and involving several partners among which the Department of Electronics of the Politecnico di Torino and FLAG-MS (which is supporting this Thesis work), which aims to develop a tractor equipped with a generator unit and electrically operated equipment.

The MArcEL project is active in the development of sustainable agriculture through electrically operated machines and equipment with the most advanced systems for precision agriculture [1]. The project has four goals:

1. 100% electrical system: a tractor equipped with a generation unit and a series of fully electrically operated equipment.

2. Innovative supply chain in Piemonte: collaboration of 17 partners for the creation of a new supply chain.

3. Precision Farming: environmental parameters, crop development, operations carried out, operating conditions adopted, functional parameters of the tractor and of the machines.

4. The + system: the system will be safer, cheaper, more efficient, more sustainable. All validated and certified in operating environments.

It is co-funded by the European Regional Development Fund and Regione Piemonte and adopts some of the key elements of the Horizon 2020 and Horizon Europe 2027 programs, specifically concerning sustainable agriculture and energy efficiency. The research involves 17 partners including the Department of Electronics and Telecommunications of the Polytechnic of Turin and the Department of Agricultural Forestry and Food Sciences of the University of Turin and leading companies in the production of tractors, motors and especially agricultural machinery. The mechanical components and pneumatic actuators of the machines are substituted with electrical actuators. The machines realized in this project are divided in low voltage and high voltage categories: the low voltage machinery consists of a straddle sprayer, a leveler and a sheeter all powered by a 48 V battery with power between 4.5 kW and 6.5 kW. The high voltage agricultural machines consist of a ditcher and a tedder which operate on a 700 V DC supply with inverters designed by FLAG-MS. The ditcher consists of a high power inverter with maximum power of 47 kW in excavation mode and 40 kW in cleaning mode. The tedder consists of four low power inverters in the same case running the four separate motors with combined maximum power of 48 kW and 25 kW in normal operation.

The goal of this project is to design and characterize an Electromagnetic Interference (EMI) filter to reduce the emissions of the two inverters, called ditcher and tedder and belonging to the respective machinery, in order to comply with the regulations.
First the choices made in a previous work are explored, highlighting the most important ones made by the designer. Then, since the components have been changed due to shortage, they have been characterized in order to use their model for the subsequent circuital simulations in LTspice to get their Insertion Loss (IL). The model of the inverters made in Simulink in the previous design has been used to prove the effectiveness of the filters.
In the fourth chapter are described the changes made to the PCB design in order to properly measure the IL, then the filters have been characterized by the measurement of the S_{21} with two Network Analyzers (NA), one made by Keysight and another made by HP, which has been converted into IL and compared to the previous simulations.

Afterwards the resonances found with the IL measurements have been manually identified using a circuital simulator, followed by the use of Keysight ADS PEPro, a software that allows to take into account the parasitic effects introduced by the Printed Circuit Board (PCB) and to simulate the scattering parameter measurement of the filter.
Finally the model of the system of the ditcher inverter is moved from Simulink to ADS and it is used in combination with the results form PEPro, performing a EM-circuit co-simulation, to simulate the LISN measurement.

Chapter 2

Preliminary EMI filter design

In the following chapter will be discussed the origin of this work and the previous design choices.

2.1 Inverters

This section aims to introduce the two inverters focus of this work, that have been modeled in a previous project [2]. An inverter allows to convert a DC voltage into an AC voltage and in this work it will drive an electric motor. Both the inverters have the following characteristics [2]:

- Three-phase inverters: three different outputs shifted by 120° each other.
- Voltage Sourced Inverters (VSI): the DC input is a constant voltage and the energy is stored on a parallel DC bus capacitor.
- A Space Vector Pulse Width Modulation (SVPWM) is employed to control both amplitude and frequency of the output AC voltage by a specific modulation scheme. It generates less distortion on the output and provides a more efficient use of the supply voltage in comparison with the sinusoidal PWM technique.

2.1.1 Tedder

The tedder inverter drives four identical motors so it has been divided into four single inverters all equal to each other as shown in figure 2.1. It is

designed to be supplied with 700 V, considered ideal, and stabilized at the input of the converter by a dc-link capacitor. It is rated to drive four 8.6 kW motors. In this application, four high-voltage capacitors are used in parallel, allowing to increase the equivalent total capacitance and to reduce the total ESL and ESR [2]. Their characteristics are shown in table 2.1. They work as a capacitor up to around 100 kHz as shown in the impedance graph from the datasheet in figure 2.2. After the resonant frequency its behavior is dominated by the parasitic resistance and inductance. The choice of this capacitor is important from the EMC point of view since it is very close to the inverter and allows to reduce the ripple of the supply and the differential mode currents entering, but it is not enough to be compliant with the normative. Furthermore a 100 nF capacitor with a voltage rating of 1 kV is placed in parallel to each leg as close as possible.

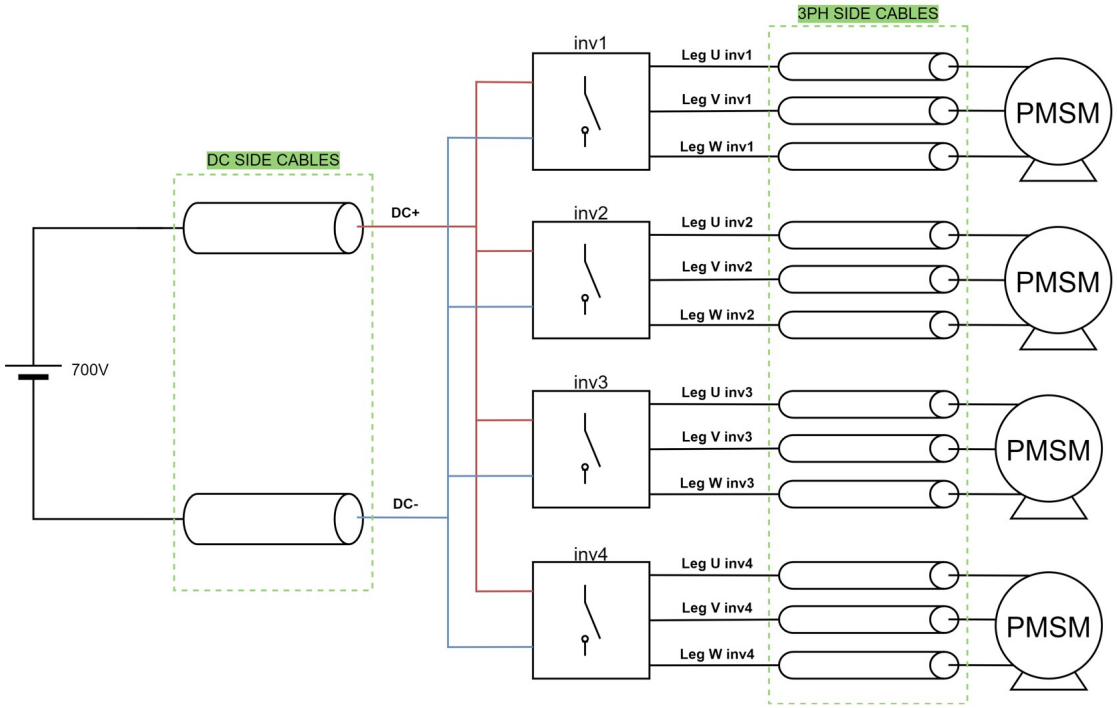


Figure 2.1. Concept scheme of the tedder system quadruple configuration. [2]

The switches employed are Silicon Carbide (SiC) Power MOSFETs belonging to the Cree family. Their main specifications are in table 2.2. The MOSFETs are driven using gate driver with the following voltage values:

Maximum voltage	900 V
Capacitance	50 μF
ESR	5.6 mΩ
ESL	15 nH

Table 2.1. Dc-link capacitor main parameters [3]

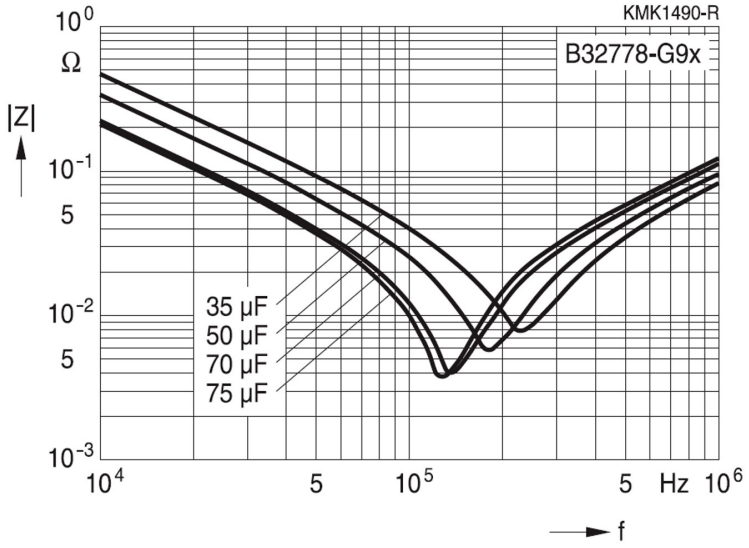


Figure 2.2. Dc-link capacitor impedance versus frequency [3]

$$\begin{cases} V_{on} = 15\ V \\ V_{off} = -3\ V \end{cases} \tag{2.1}$$

Then a resistor in series with the gate driver output and the the device's input is used to limit the current and consequently reducing the noise due to high dv/dt and di/dt.

2.1.2 Ditcher

The ditcher inverter is designed to drive a single 18 kW electric motor but for what possible the components were kept the same, for example the dc-link capacitors and the 100 nF SMD capacitors are the same. Otherwise the MOSFETs are not the same and in this case are used three SiC modules composed of two swtiches each. Their specifications are shown in table 2.3.

$V_{DS,max}$	1200 V
$V_{GS,op}$	-4/+15 V
I_D	115 A
$V_{TH,typ}$	2 V
$R_{DS,on,typ}$	16 mΩ

Table 2.2. SiC MOSFET main parameters [4]

$V_{DS,max}$	1200 V
$V_{GS,op}$	-5/+15 V
I_D	200 A
$V_{TH,typ}$	4.5 V
$R_{DS,on,typ}$	5.63 mΩ

Table 2.3. SiC power module main parameters [5]

2.2 Electromagnetic compatibility

By definition [6], a system is electromagnetically compatible with its environment if it satisfies the following three criteria:

- It does not cause interference with other systems;
- It does not cause interference with itself;
- It is not susceptible to emissions coming form the other systems.

In order to be sold a device must comply with the normative regarding its emission limits which are formulated by regulatory agencies. The reference normative for the two inverters is the E-ECE-324-Add.9-Rev.6 [7] and the measurement standard for the characterization of the EMI filters is the CISPR 17 [8].

2.2.1 Measurement setup

The LISN is a device that prevents the external noise to the test from contaminating the measurement and ensures that is independent form the measurement place. The normative imposes the use of a LISN with the specifications of figure 2.3 and the values of components of table 2.4.

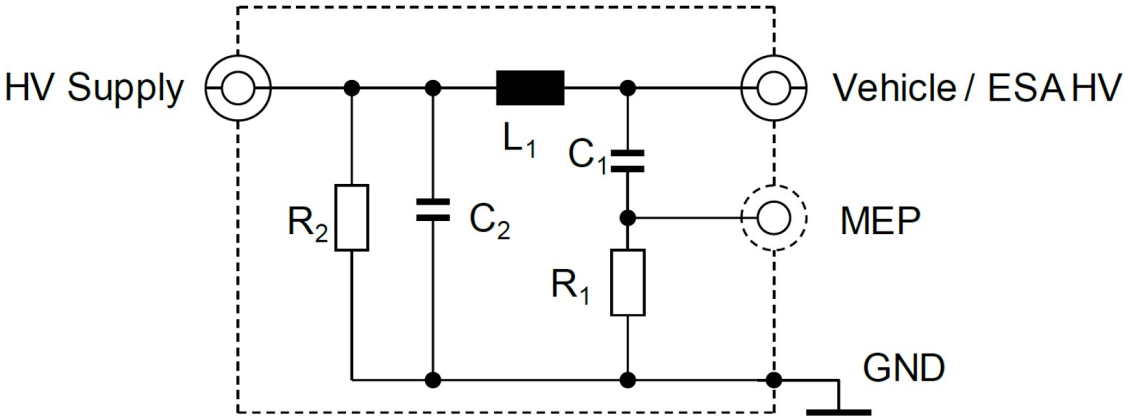


Figure 2.3. Normative HV-AN [7]

Component	Value
L_1	5 μH
C_1	0.1 μF
C_2	1 μF
R_1	1 kΩ
R_2	1 MΩ

Table 2.4. Normative LISN parameters.

The test for the conducted emissions needs to be performed according to CISPR 16-2-1. The test setup is reported in figure 2.4.

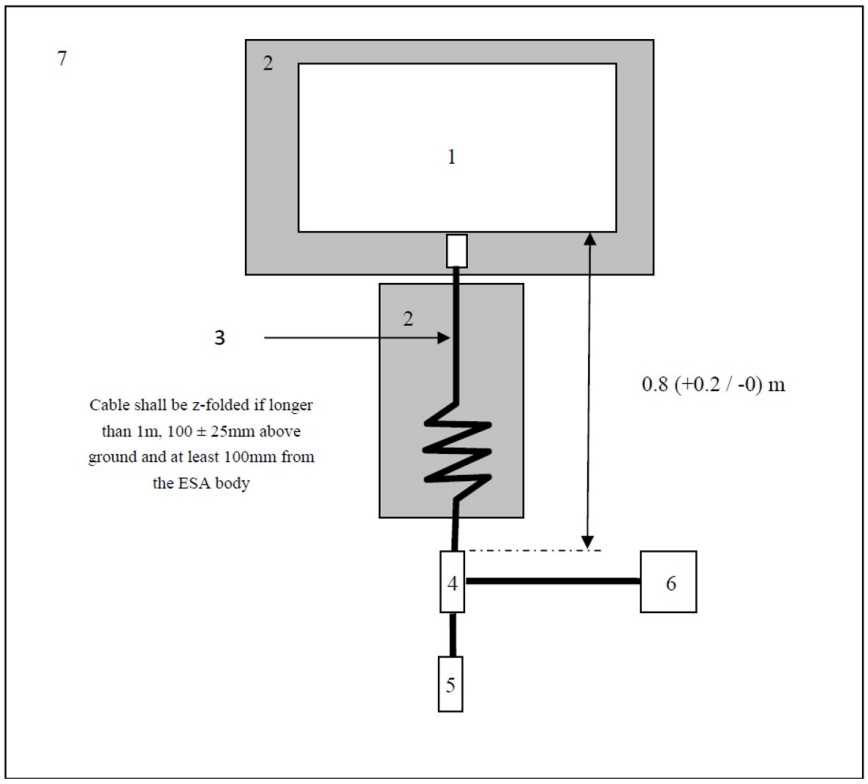


Figure 2.4. Conducted emission measurement setup [7]

Number	Description
1	ESA under test
2	Insulation support
3	Charging harness
4	LISN grounded
5	Power mains socket
6	Measuring receiver
7	Ground plane

Table 2.5. Conducted emission measurement setup legend

Emission limits

The limits on DC power lines for this work are the ones defined in IEC 61000-6-3 and are listed in table 2.6.

Frequency [MHz]	Limits and detector
0.15 to 0.5	79 dBμV (quasi-peak) 66 dBμV (average)
0.5 to 30	73 dBμV (quasi-peak) 60 dBμV (average)

Table 2.6. Maximum allowed radio frequency conducted disturbances on DC power lines. [2]

2.3 Cables model

The inverter is connected to the power supply using cables that will be called "DC side cables" or "DC cables". The connection from the inverter to the motor will be labeled "three-phase side cables" or "AC cables". Their choice was explained in a previous work [2] with their main parameters summarized in table 2.7.

	DC side	Tedder 3ph side	Ditcher 3ph side
l_{max}	1 m	2 m	1.5 m
r_{out}	7.9 mm	2.9 mm	5.1 mm
r_{in}	5.3 mm	1.4 mm	2.9 mm
t_{sh}	0.105 mm	0.08 mm	0.08 mm
r_{sh}	7.2 mm	2.3 mm	4.4 mm

Table 2.7. Power cables main geometry parameters [9]

The length of the DC cables could be of around 10 m in the final application but the model has been set to 1 m following the instructions provided by the normative measurement setup. The distance between the DC cables and the reference plane is set by the normative at 0.1 m. The same distance was also used for the AC cables. The distance between the wires has been chosen as 0.1 m. The cables model has been realized with the Multiconductor

Transmission Lines (MTL) concept which assumes that the Transverse Electromagnetic mode of propagation of field is present on the lines this means that the electric and magnetic fields do not have a component along the line axis. To predict the crosstalk effect, it is feasible to construct a per unit length model of the circuit for a small Δz section like shown in figure 2.5. Many section are then used to model a cable.

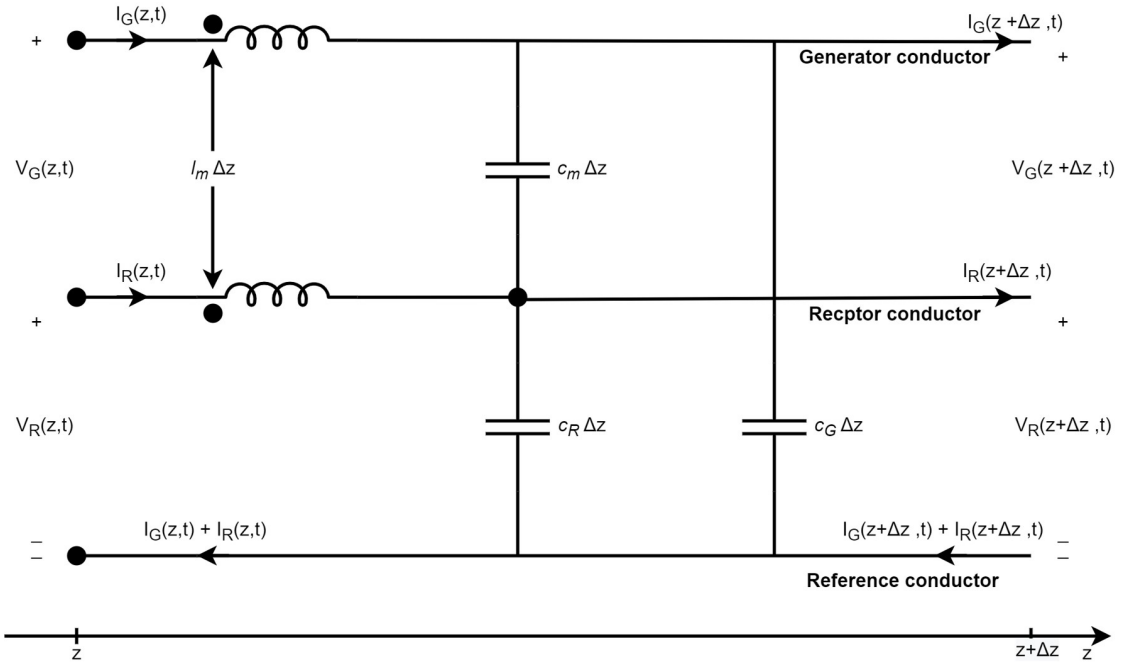


Figure 2.5. Per-unit-length MTL [2]

The sections were then chosen as shown in table 2.8.

	DC side	**Tedder 3ph side**	**Ditcher 3ph side**
Cable length	1 m	2 m	1.5 m
n° of sections	2	4	3

Table 2.8. Number of line sections for each power cable. [2]

A graphical representation of the DC cables model is represented in figure 2.6.

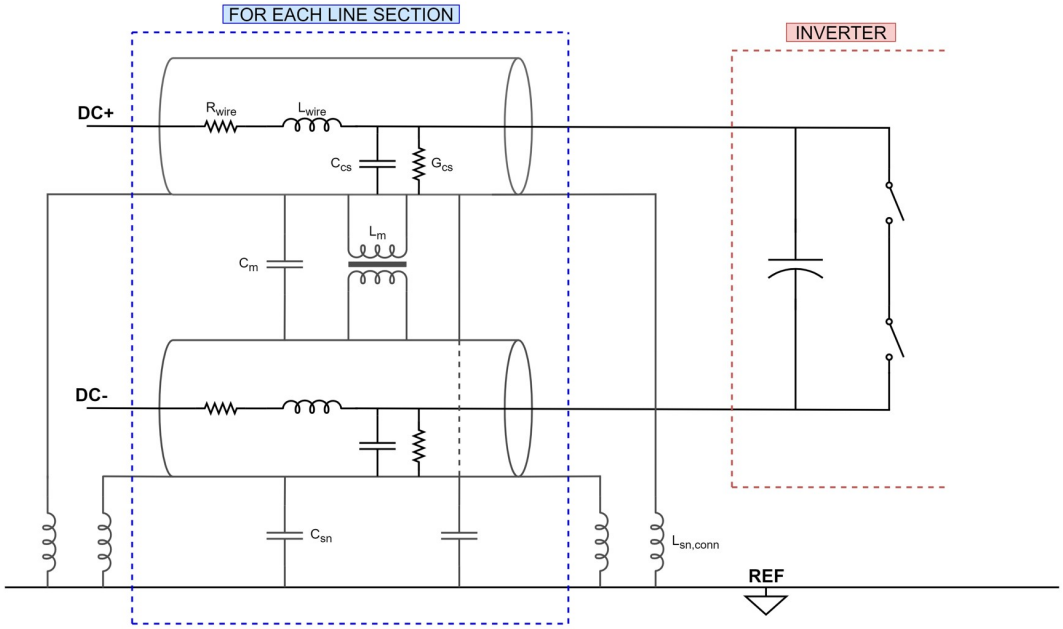


Figure 2.6. DC side cables and their parasitic elements. [2]

2.4 Electrical motors

Both motors are Permanent Magnet Synchronous Motors (PMSM) and are designed for the same 700 V supply but have substantial differences in terms of rated power, speed, current and torque. The PMSM is an AC motor which stator runs on three-phase AC excitation, while its rotor is a permanent magnet [2]. Either motors employed are designed for 700 V supply but the tedder motors have a 8.6 kW nominal power, whereas the ditcher motor has a 18 kW nominal power. All the other technical parameters are reported in table 2.9.

	Tedder motors	**Ditcher motor**
n_{nom}	250 rpm	3000 rpm
$f(2p)$	54.16 Hz (26)	200 Hz (8)
n_{max}	300 rpm	3500 rpm
K_e	1600 V_{rms}/K_{rpm}	140 V_{rms}/K_{rpm}
K_t	26 Nm/A_{rms}	2.3 Nm/A_{rms}
T_{nom}	330 Nm	60 Nm
I_{nom}	13 A_{rms}	27 A_{rms}
T_{max}	1000 Nm	170 Nm
I_{max}	45 A_{rms}	81 A_{rms}
R_{ff}	2.1 Ω	0.2 Ω
L_{ff}	80 mH	-
L_d	-	3.8 mH
L_d	-	3.6 mH

Table 2.9. Tedder and ditcher PMSM main parameters. [2]

2.5 Filter design

The filters were designed in a previous work [2] with the goal of providing attenuation for both CM and DM emissions of the ditcher and tedder inverters. The design started from the emissions of the tedder inverter increased by 6 dB as a safety margin shown in figure 2.7.

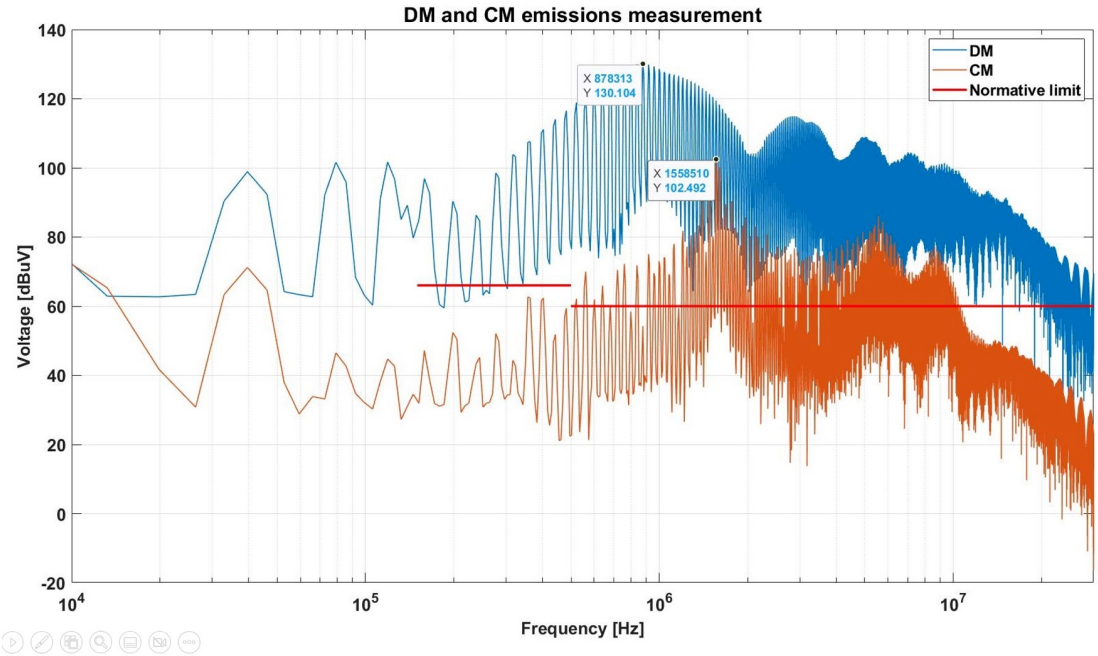


Figure 2.7. Insertion loss required for DM and CM emissions. [2]

Looking at the peaks of the emissions the required Insertion Losses were chosen:

$$\begin{cases} IL_{DM} = 42 \text{ dB}\mu\text{V} \text{ @ } 1.5 \text{ MHz} \\ IL_{CM} = 70 \text{ dB}\mu\text{V} \text{ @ } 870 \text{ kHz} \end{cases} \tag{2.2}$$

The topology chosen is based on LC filter composed of a Common Mode Choke, one X-capacitor for the DM emissions filtering and two Y-capacitors for the CM component.

Because of the direct connection to the supply voltage X and Y capacitors may be subjected to overvoltages and spikes, causing failures. When a class-X capacitor fails because of an overvoltage, it is likely to fail short and this would cause an overcurrent protective device to open. If a class-Y capacitor

fails, instead, this could lead to a fatal electric shock due to the ground connection. For this reason, class-Y safety capacitors are designed to fail open [10]. Following the ISO6469-3 normative standard in case of DC power lines [11] and supposing a large overvoltage $\Delta V = 1$ kV the maximum Y-capacitor value was estimated:

$$E_{imm} = \frac{1}{2}C(\Delta V^2) \leq 0.2 \text{ J} \Rightarrow C \leq 400 \text{ nF} \tag{2.3}$$

The X-capacitor does not have any design constrain on DC line applications and it can be chosen looking at its safety features and voltage rating. Since the CM IL is more stringent in both magnitude and frequency the design started from the CM filter.

Using $C_y = 100$ nF and the corner frequency $f_{CM} = 10$ kHz, the CM inductor is given by:

$$L_{CM} = \left(\frac{1}{2\pi f_{CM}}\right)^2 \cdot \frac{1}{2C_y} = 1.3 \text{ mH} \tag{2.4}$$

It was supposed that the common-mode choke is characterized by a coupling coefficient k=0.95:

$$L_{DM} = L_{leak} = 0.05 \cdot L_{CM} = 65 \ \mu\text{H} \tag{2.5}$$

Choosing a corner frequency $f_{DM} = 10$ kHz:

$$C_x = \frac{1}{(2\pi f_{DM})^2 2L_{DM}} = 2 \ \mu\text{F} \tag{2.6}$$

To guarantee system stability the output impedance of the input filter must be much smaller that the input impedance of the closed-loop converter [12]:

$$Z_{out,filter} \ll Z_{in,SMPS} \tag{2.7}$$

In this work the control loop acts until 400 Hz, which means that the stability problem should be limited to low frequencies. Nevertheless, wide band stability is guaranteed using the damping technique. By adding a resistive loss element to the filter circuit, the LC resonance can be damped and the $Z_{out,filter}$ peak is reduced at resonance, making easier separation with $Z_{in,SMPS}$ curve. In the previous project it was decided to use parallel damping as shown in figure 2.8. It is demonstrated that the peaking is minimized by using [13]:

$$\begin{cases} R_D = \sqrt{\frac{L_{DM}}{C_{DM}}} \\ C_D = 4 \cdot C_{DM} \end{cases} \tag{2.8}$$

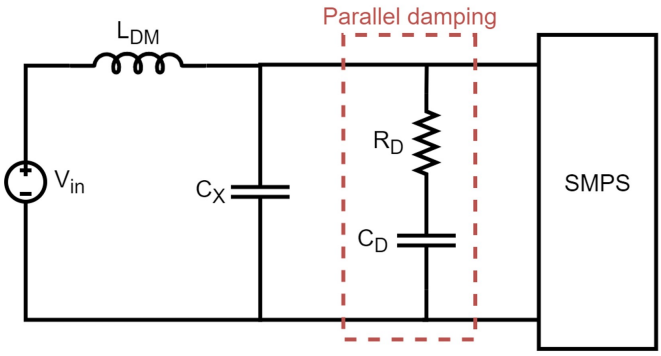


Figure 2.8. Parallel damped filter [2]

The input impedance of the inverter was estimated as:

$$|Z_{in,SMPS}| = \frac{V_{DC}^2}{4P_{DC}} = 12.7\ \Omega \tag{2.9}$$

Since the real $Z_{in,SMPS}$ is not flat, the computed value has been lowered by ten times to make a very safe comparison.

The choke was chosen taking taking into account the power involved:

$$I_{DC} = \frac{P_{DC}}{V_{DC}} = 57\ \text{A} \tag{2.10}$$

The X and Y capacitors have been placed on both left and right side of the choke, realizing a CLC filter, thus their values have been halved. The selected components are:

- CWS CM-161U-60A: 160 μH common mode choke;
- TDK B32022A3473M: 47nF Y2 capacitor;
- TDK B32914A5105M: 1 μF X1 capacitor:
- TDK B32916A5475M: 4.7 μF X1 capacitor for the damping;
- Vishay CRCW20101R50FNEF: 1.5 Ω resistor

It was decided to use two damping resistors in series. In table 2.10 are reported all the ESL and ESR values of the capacitors used in the filters, while in table 2.11 are listed the parasistic values of the CMC, whose model used in this project is represented in figure 2.9.

Capacitor values			
Part Number	**Value**	**ESR**	**ESL**
B32022A3473M	47 nF	90 mΩ	6.65 nH
B32914A5105M	1 μF	45 mΩ	4.8 nH
B32916A5475M	4.7 μF	10 mΩ	1.1 nH

Table 2.10. Capacitors values

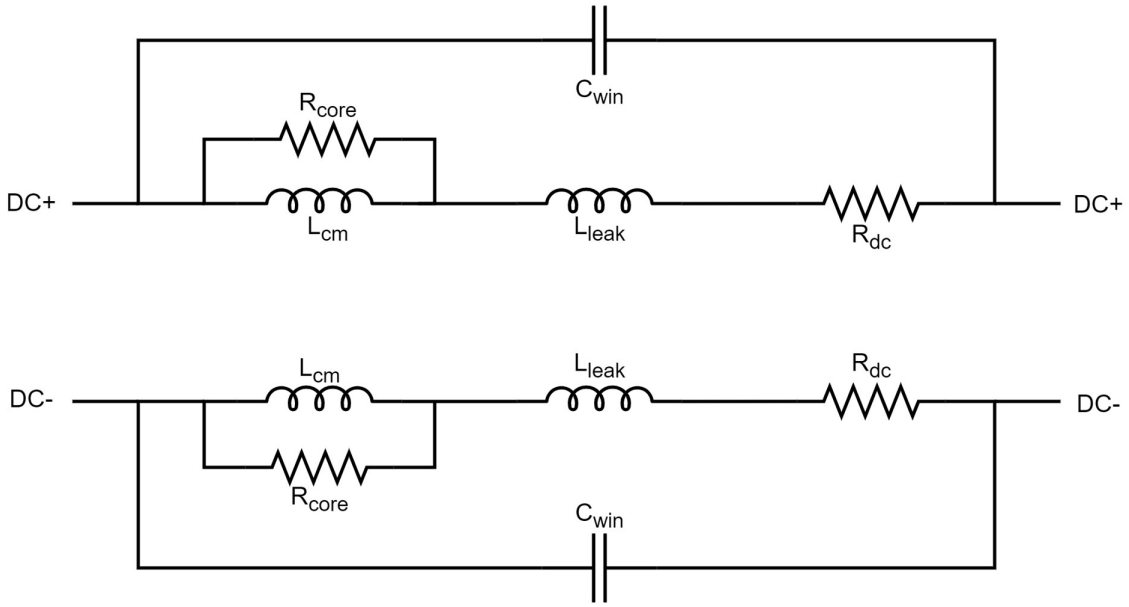


Figure 2.9. Equivalent circuit of a common mode choke [2]

Common Mode Choke values				
L_{cm}	L_{leak}	R_{DC}	C_{win}	R_{core}
160 μH	2 μH	0.5 mΩ	145 pF	800 Ω

Table 2.11. CMC values

In figure 2.10 is reported the schematic of the single stage filter while the schematic of the double stage filter is shown in figure 2.11.

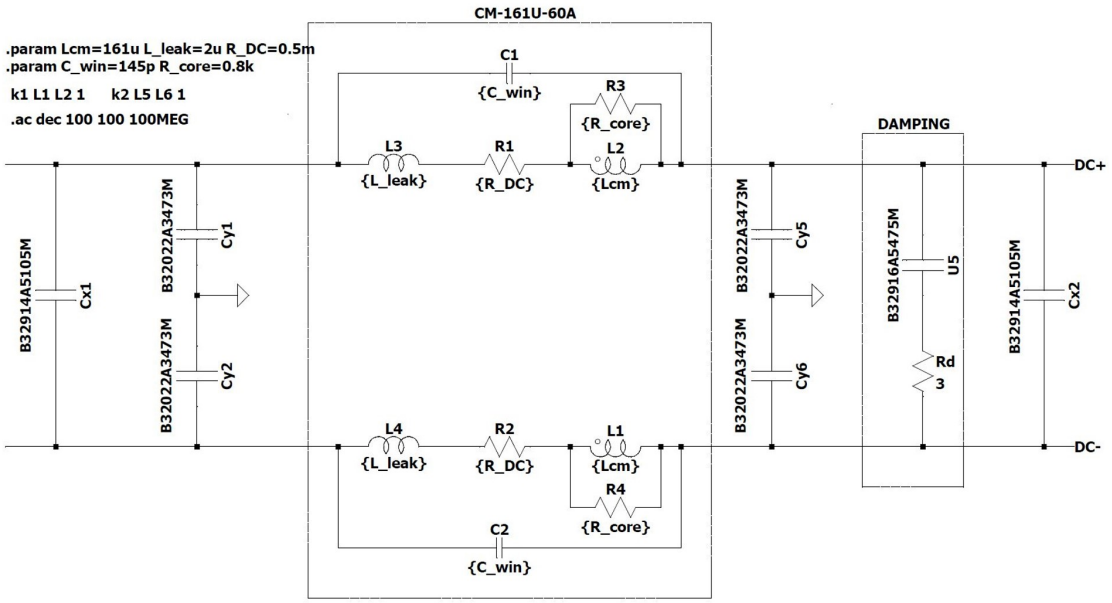


Figure 2.10. Schematic of the one stage EMI filter [2]

Since the value of the CM inductance is much less than the one predicted in the previous section the filter order was increased to get the required IL.

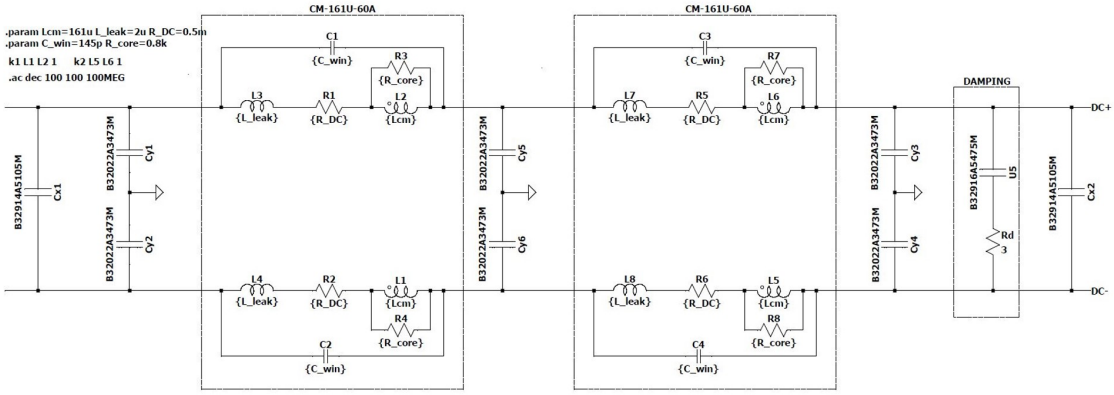


Figure 2.11. Schematic of the two stage EMI filter [2]

Both filters were characterized on a generic 50 Ω/50 Ω system: the setup for the Insertion Loss measurement is shown in figure 2.12.

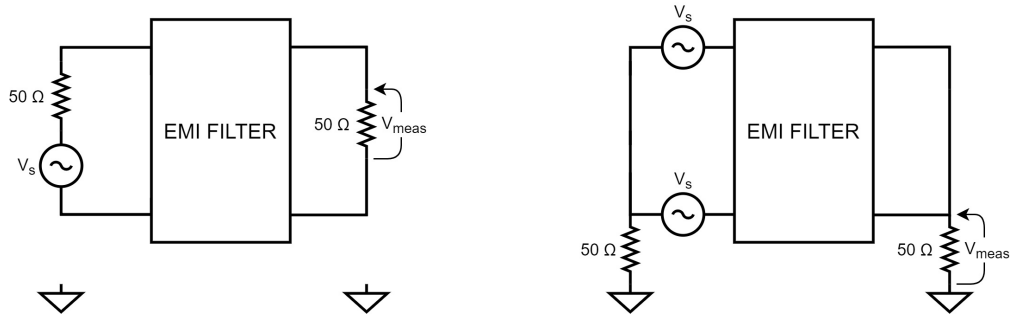


Figure 2.12. Setup for the EMI filter characterization in DM (left) and CM (right). [2]

The Insertion Losses are then compared between the two filters and removing the input capacitors in figure 2.13 and figure 2.14. The emission spectra resulted from the simulation on the systems with the filter added are displayed in figure 2.15 for the tedder inverter and in figure 2.16 for the ditcher inverter.

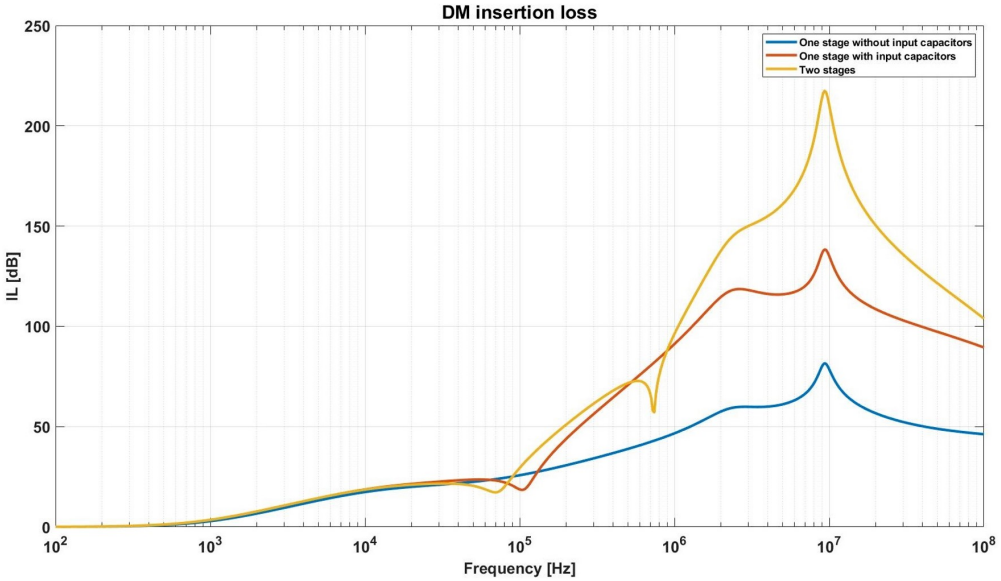


Figure 2.13. Comparison of the DM insertion losses measured on a generic 50 Ω/50 Ω system. [2]

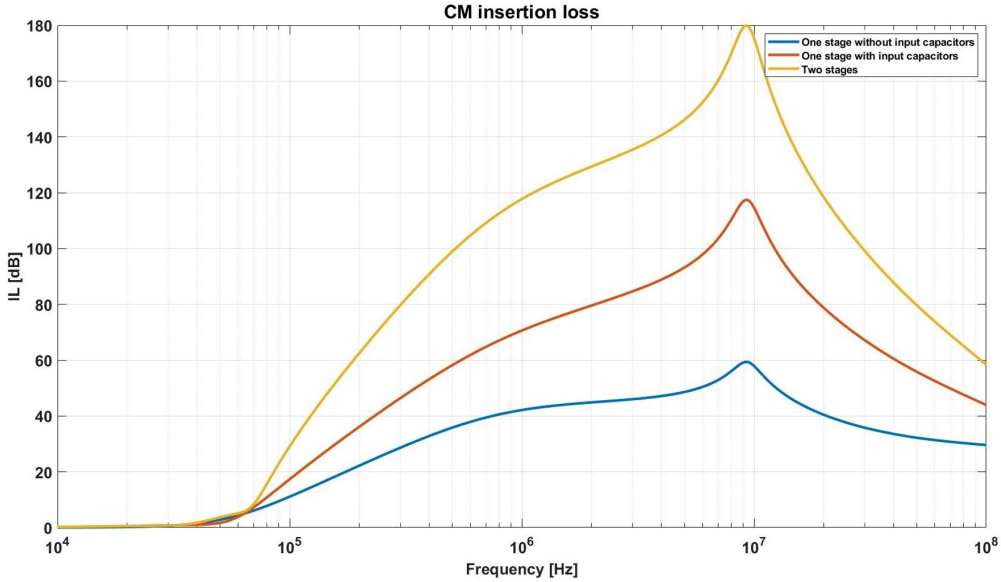


Figure 2.14. Comparison of the CM insertion losses measured on a generic 50 Ω/50 Ω system. [2]

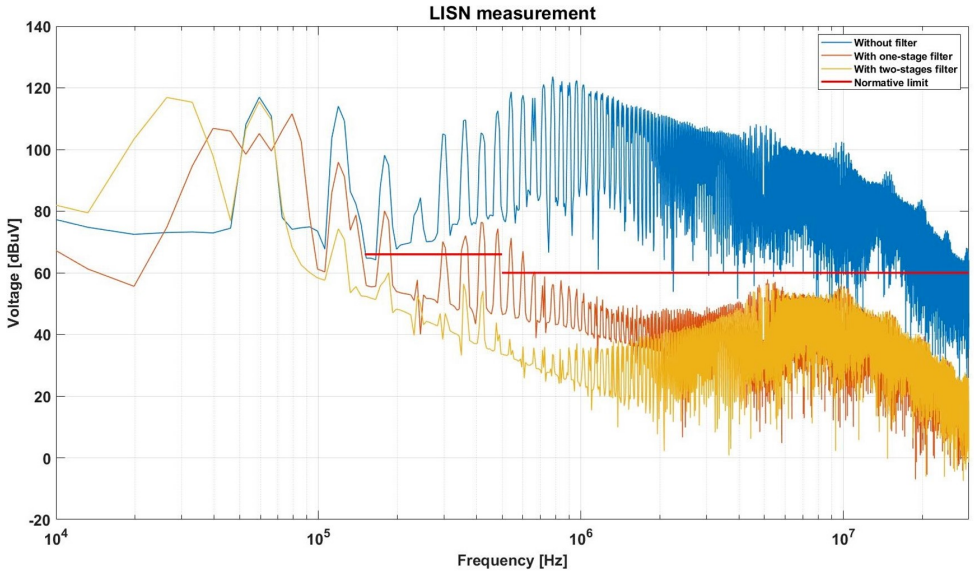


Figure 2.15. Comparison between the LISN measurement without filter and with a two stage filter on the tedder inverter [2]

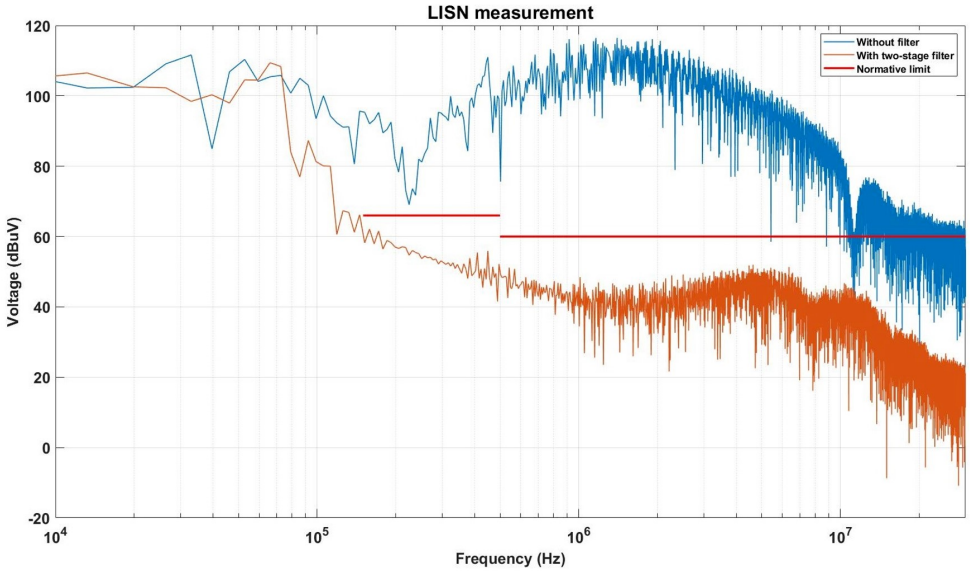


Figure 2.16. LISN measurements without and with two-stage filter on ditcher system. [2]

Chapter 3

Redesign of the EMI filter

Due to the shortage of components some of them have been changed with the ones available at the time of purchase. In some cases their value is different from the previous design, thus a comparison is mandatory.

These are the components used in both filters:

OLD Part Number	**Value**	**NEW Part Number**	**Value**
B32914A5105M	1 μF	BFC233814105	1 μF
B32022A3473M	47 nF	same	same
B3291651A5475M	4.7 μF	EZP-V1B475LTB	4.7 μF
CRCW20101R50FNEF	1.5 Ω	same	same
CM-161U-60A	160 μH	B82726S3543N040	95 μH

Table 3.1. New components compared to old ones

3.1 Component models

To obtain a result, in the simulations, as similar as possible to what will be measured it is necessary to have a good model of the components used in the circuit and to understand how each component behaves in a different frequency range. A detailed description of the components follows.

3.1.1 X-capacitor

The Vishay capacitor BFC233814105 is a class X1 film capacitor and no Spice library is available so it has been characterized using the impedance

curve provided in the datasheet in figure 3.1.

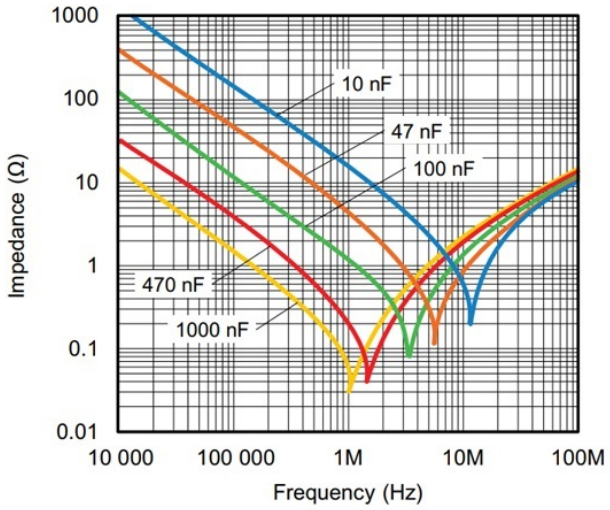


Figure 3.1. Impedance as a function of frequency (typical curve) [14]

Looking at the yellow curve (1 μF) it is possible to extract the values of the Equivalent Series Resistance (ESR) and of the Equivalent Series Inductance (ESL): the minimum of the curve is the ESR, whereas the ESL can be computed from a point after the minimum using equation 3.1.

$$L = \frac{Z}{2\pi f} \tag{3.1}$$

The values obtained are reported in table 3.2 where they are also compared with the previous component. The graph in figure 3.2 compares the two impedance curves with respect to frequency.

	C	**ESR**	**ESL**
NEW	1 μF	30 mΩ	25 nH
OLD	1 μF	45 mΩ	4.8 nH

Table 3.2.

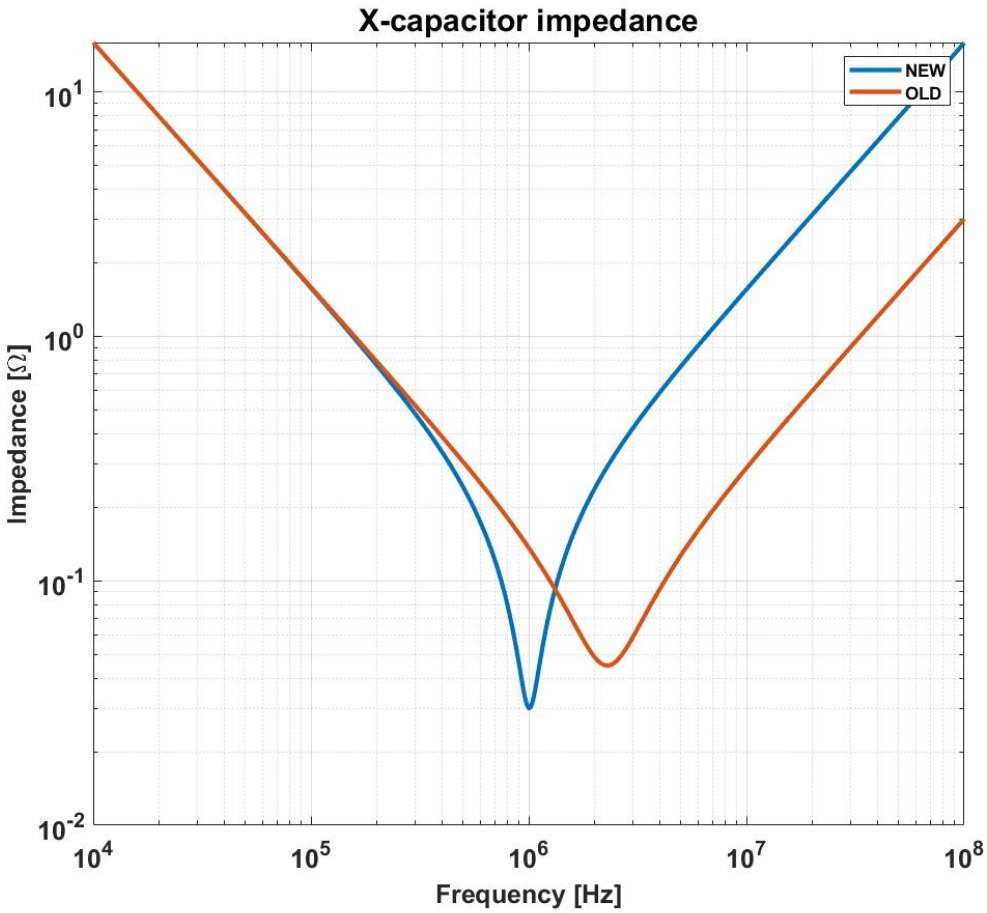


Figure 3.2. X-capacitor impedance comparison

3.1.2 Y-capacitor

The capacitor B32022A3473M made by TDK is a class Y2 Metallized Polypropylene capacitor. The datasheet does not provide an impedance curve, but TDK supplies an LTspice library. The circuit in figure 3.3, simulated in LTspice, allows to trace the impedance curve and using the procedure described in the previous paragraph its parasitic values are evaluated.

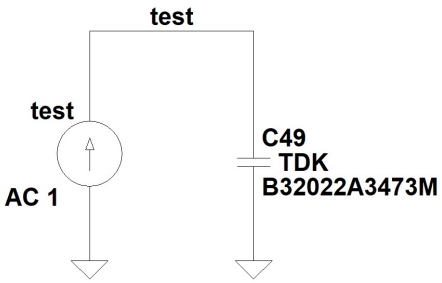


Figure 3.3. Simulation setup for the measurement of the capacitor impedance

The results of the characterization are shown in figure 3.4.

In the Printed Circuit Board B32022A3473M003 are used: the three last digit refer to the length of the terminals (3.2 ± 0.3) mm.

C	ESR	ESL
47 nF	89 mΩ	4.6 nH

Table 3.3. Capacitor B32022A3473M parasitics value

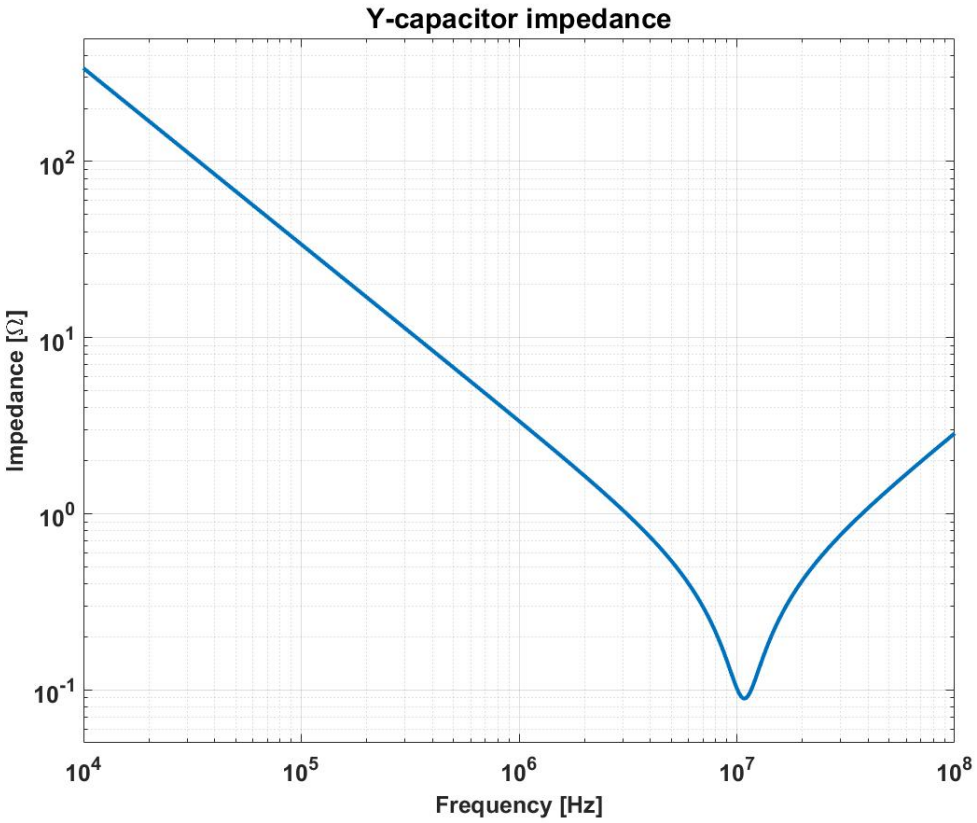


Figure 3.4. Y-capacitor impedance

3.1.3 Common Mode Choke

The model of the Common Mode Choke B82726S3543N040 made by TDK has been manually extracted from the netlist of the spice library provided by the vendor with the result shown in figure 3.5.

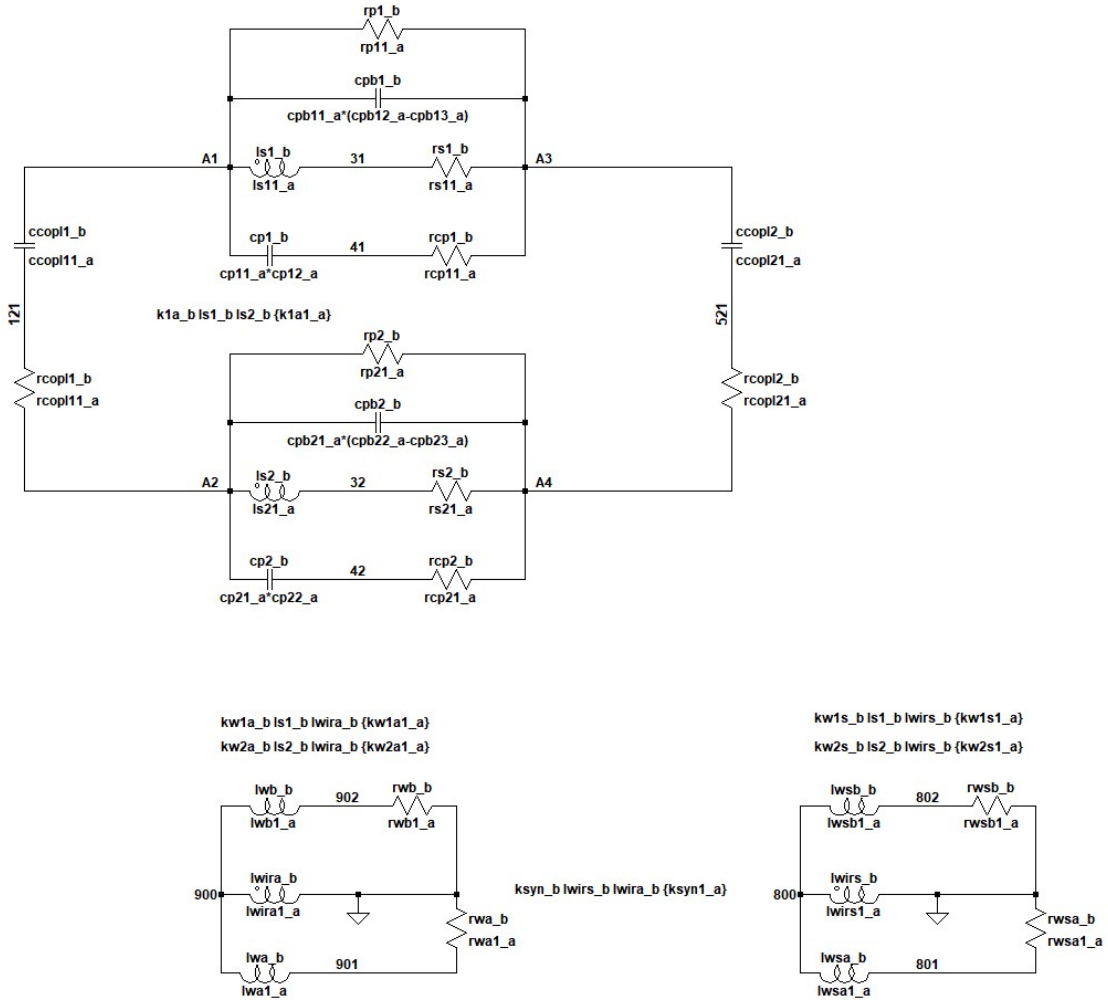


Figure 3.5. Model of the CMC from TDK library

The model has then been simplified to speed up simulations: since many components are small and contribute to the frequency response at high frequency with respect to the 30 MHz upper limit of the normative E-ECE-324-Add.9-Rev.6 [7] they are neglected. The datasheet isn't clear about the value of the inductance so it has been measured by FLAG-MS as 180 μH at 100 kHz per winding. The component has a 54 A current rating with

the windings connected in parallel so they must be connected in this way to satisfy the requirements of around 57 A. Since the inductance tolerance is -30/+50% the two inductances of 196.4593 μH from the library have been halved to 98.2297 μH. The model used in this project is shown in figure 3.6.

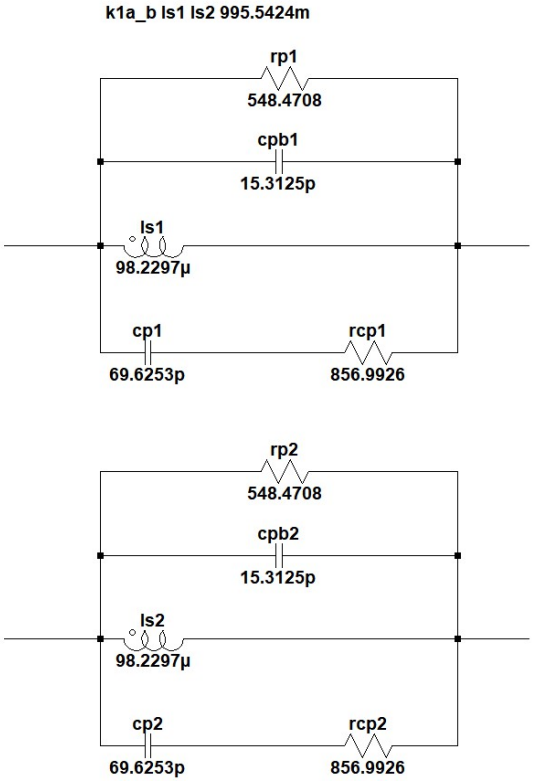


Figure 3.6. Simplified model of the choke

A comparison between the old and the new CMC main parameters is shown in table 3.4.

Common Mode Choke values			
	L_{cm}	L_{leak}	*Rated current*
OLD	160 μH	2 μH	60 A
NEW	95 μH	1.3 μH	54 A

Table 3.4. CMC values

The common mode impedance of the choke used in this work is measured using the setup shown in figure 3.7 and first of all compared to the measured impedance from the datasheet in figure 3.8. Then it is compared to the one of the choke CM-161U-60A modeled in the previous project giving the result in figure 3.9.

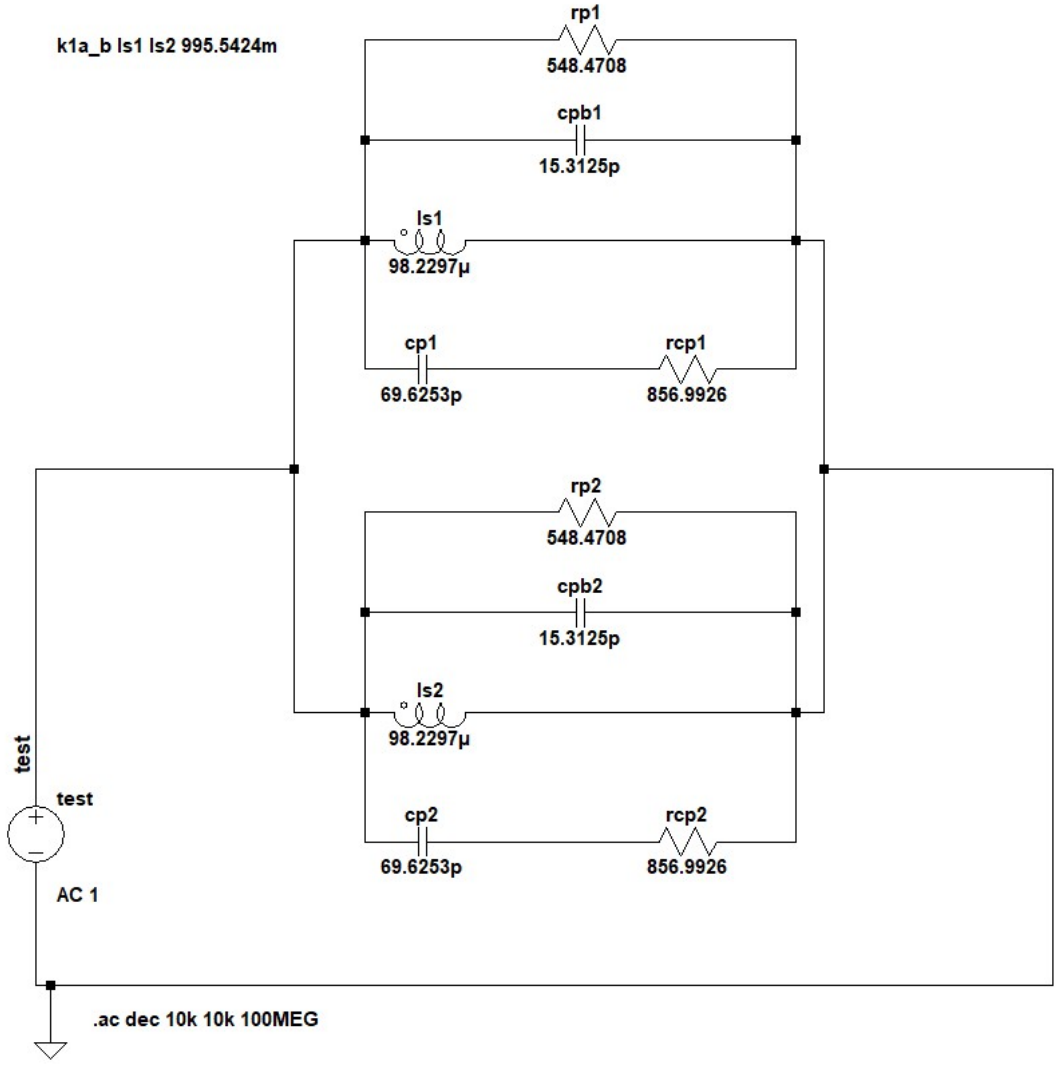


Figure 3.7. Setup for the simulation of the CMC CM impedance

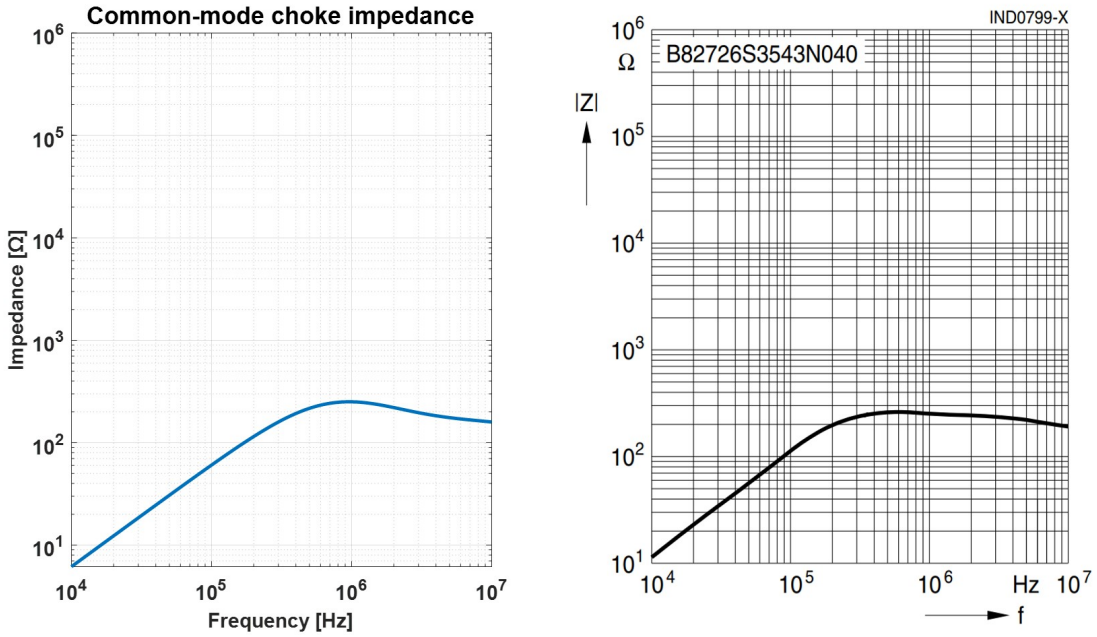


Figure 3.8. CMC impedance simulated from the LTspice model (on the left) compared to the datasheet [15] (on the right)

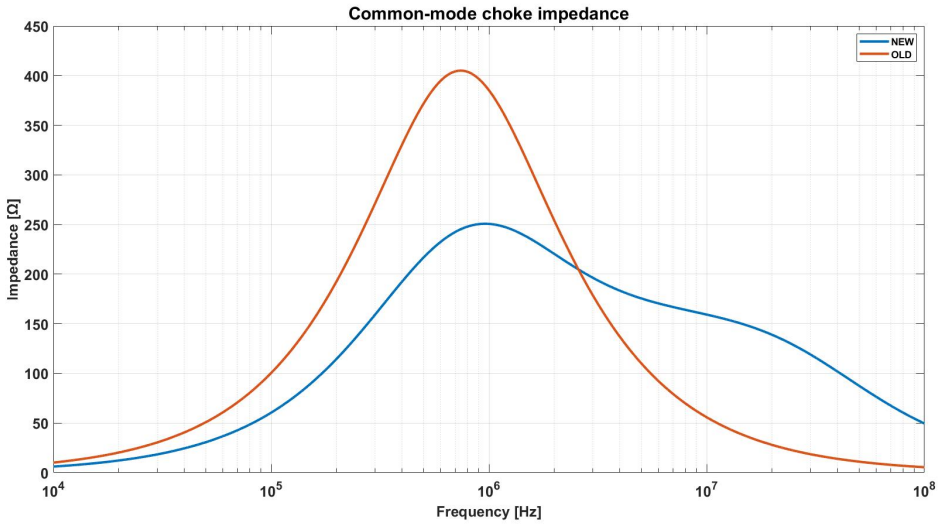


Figure 3.9. Comparison between the common mode impedances of the two CMCs

3.1.4 Damping capacitor

The Panasonic EZP-V1B475LTB is a metallized polypropylene film capacitor with a rated DC voltage of 1100 V. Since the datasheet provides an impedance curve shown in figure 3.10 the parameters have been extracted as demonstrated before.

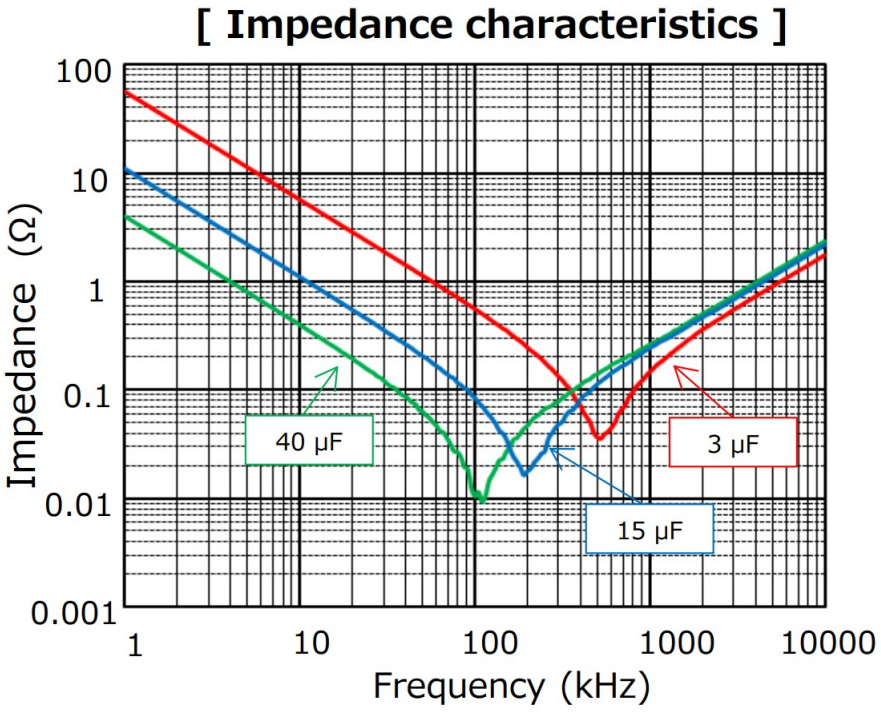


Figure 3.10. Impedance characteristics Panasonic EZP-V1B475LTB capacitor [16]

The main parasitic values compared to the old component are reported in table 3.5.

	C	**ESR**	**ESL**
NEW	4.7 μF	35 mΩ	32 nH
OLD	4.7 μF	10 mΩ	1.1 nH

Table 3.5. Parasitic values

In the following figure the impedance of the old and new capacitor are compared:

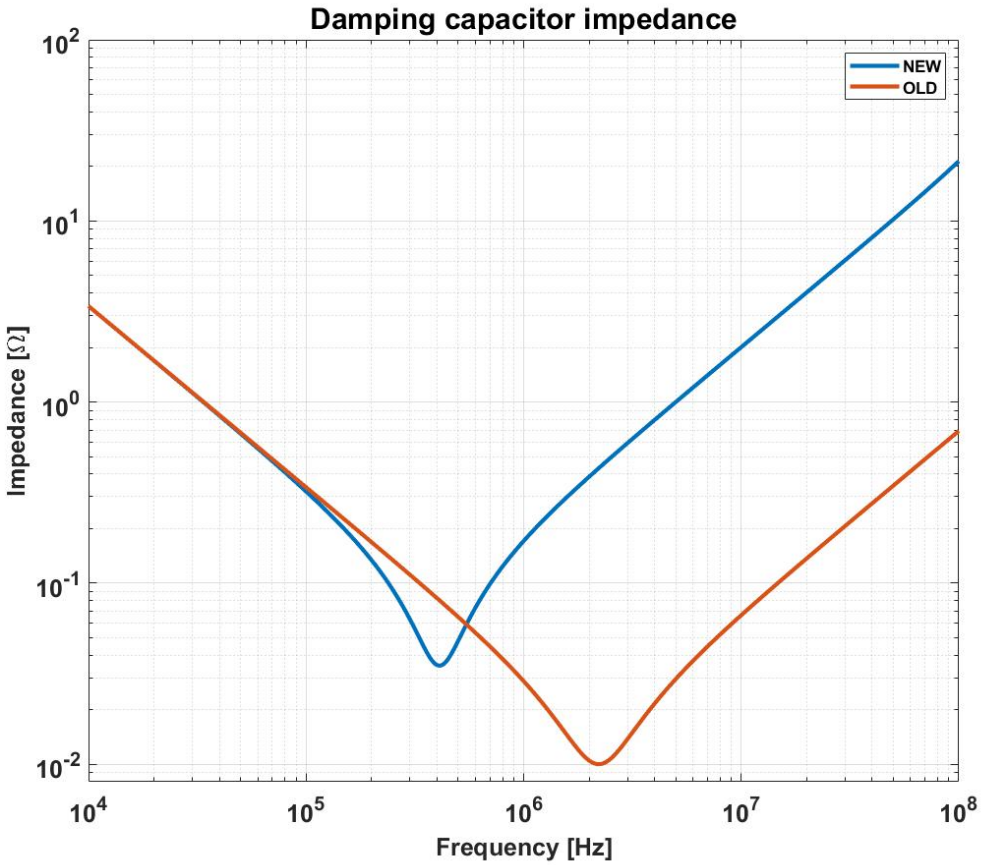


Figure 3.11. Impedance comparison

3.1.5 Damping resistor

In the implementation of the PCB it was decided to use a a single resistor instead of two in series; the component is maintained the same. Using the simulink model of the tedder inverter with switching frequency 15 kHz and without interleaving, worst condition, the peak power of the damping resistor has been measured:

$$P_{peak} = 18{,}5 \text{ mW} \tag{3.2}$$

This confirms that the 750 mW chosen resistor is more than capable of dissipating the power.

3.2 Filters schematic

This are the final schematics of the filters:

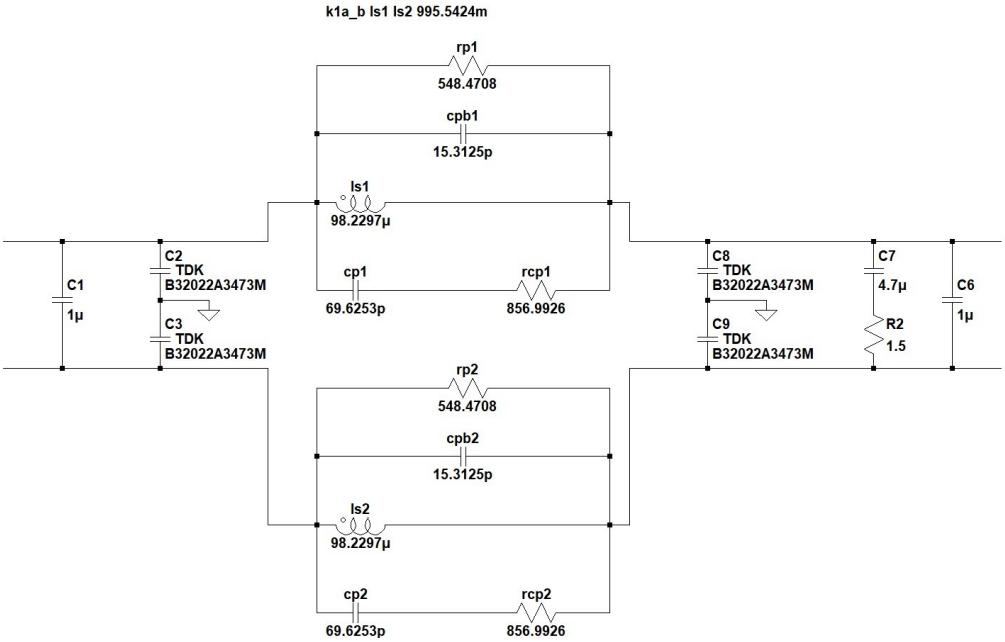


Figure 3.12. Schematic of the single stage filter

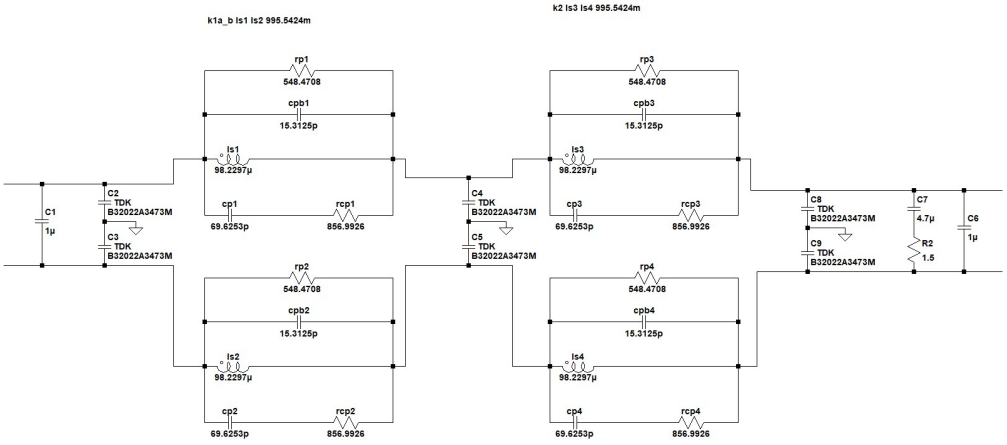


Figure 3.13. Schematic of the double stage filter

3.3 Filter re-design

The filter design started from the requirements in order to attenuate the emissions of the inverter. Given that the components are different from the ones chosen originally some considerations on the IL of the new filter need to be made. The poles were designed with a target frequency of $f_{CM} = 10$ kHz and $f_{DM} = 10$ kHz. Computing the values of the poles for the single stage filter using the components values we get:

$$f_{CM,new} = \frac{1}{2\pi\sqrt{L_{CM}2(2C_y)}} \simeq 38 \text{ kHz} \tag{3.3}$$

$$f_{DM,new} = \frac{1}{2\pi\sqrt{L_{DM}2(2C_x)}} \simeq 70 \text{ kHz} \tag{3.4}$$

Compared to the old single stage filter poles:

$$f_{CM,old} = \frac{1}{2\pi\sqrt{L_{CM}2(2C_y)}} \simeq 29 \text{ kHz} \tag{3.5}$$

$$f_{DM,old} = \frac{1}{2\pi\sqrt{L_{DM}2(2C_x)}} \simeq 56 \text{ kHz} \tag{3.6}$$

This results are confirmed by the simulations of the insertion loss of both filters, where it is clearly visible an increase of the poles frequency.

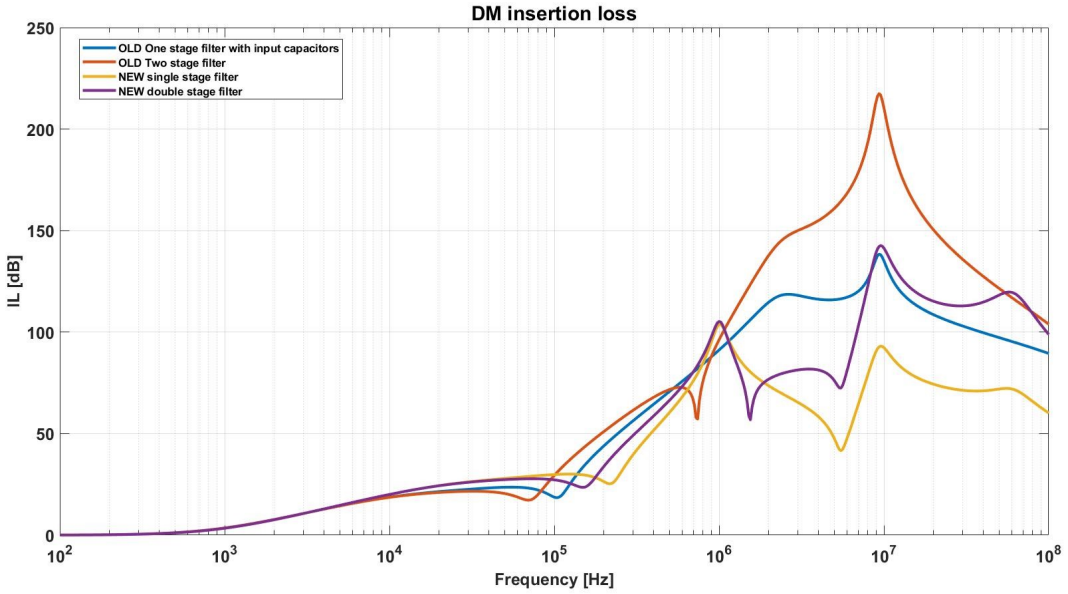


Figure 3.14. Comparison of the DM insertion losses of the two filters

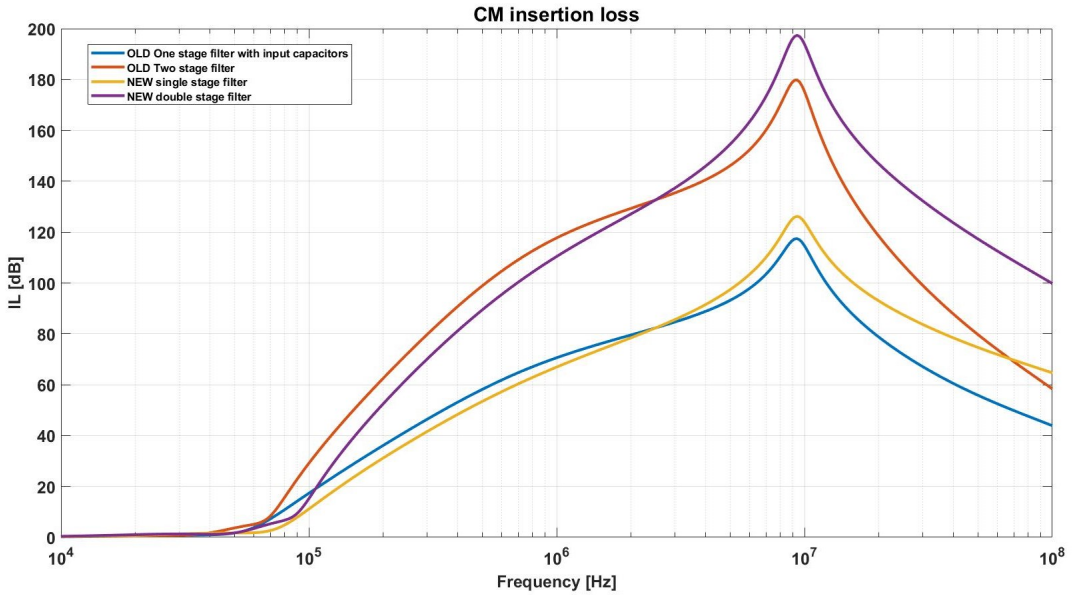


Figure 3.15. Comparison of the CM insertion losses of the two filters

3.4 Emission spectrum comparison

Because the poles are moved to higher frequencies due to a lower L_{cm} of the choke the emissions are a bit higher at lower frequency, especially in the tedder case, figure 3.17.

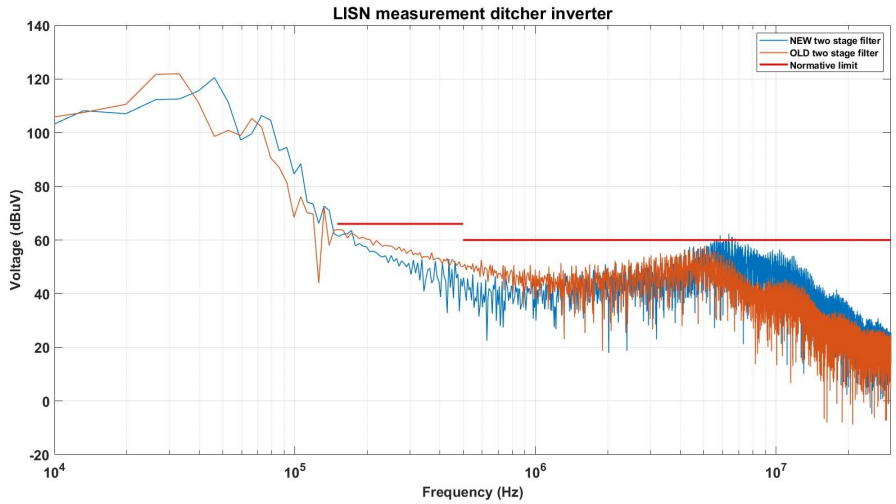


Figure 3.16. Comparison of the emissions between the old filter and the new one ditcher inverter

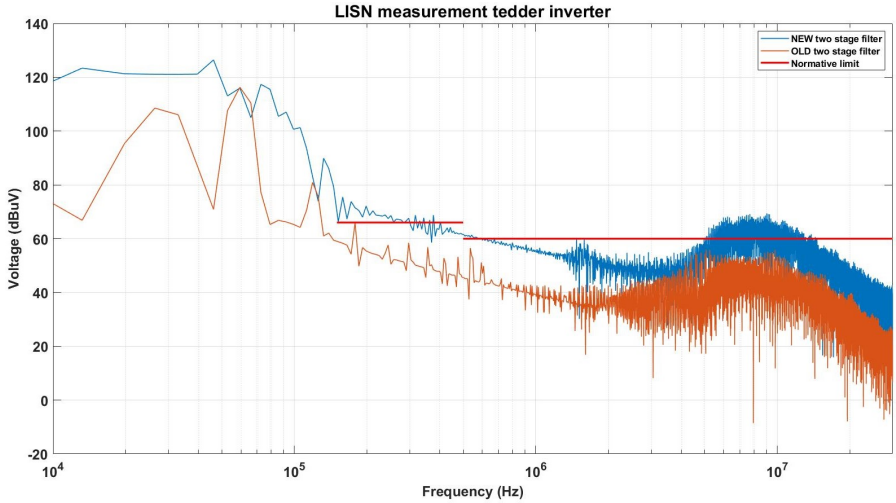


Figure 3.17. Comparison of the emissions between the old filter and the new one tedder inverter

Chapter 4

PCB design and measurement of the filter insertion loss

In this chapter will be discussed the procedure and results of the Insertion Loss measurements. First of all it is necessary to introduce the regulation that has been followed and the changes that have been made to the PCBs in order to make those measurements possible.

4.1 CISPR 17 regulation

The standard that will be used to characterize the filters is the CISPR 17 which specifies methods to measure the radio interference suppression characteristics of passive EMC filtering devices [8]. This work is focused on the Common Mode (CM) Insertion Loss (IL) and the Differential Mode (DM) IL measurements that are described in the following paragraphs. To measure the IL it is necessary to measure the Scattering parameters using a Network Analyzer.

4.1.1 Insertion Loss

In Annex E [8] the Insertion Loss (IL) is defined by:

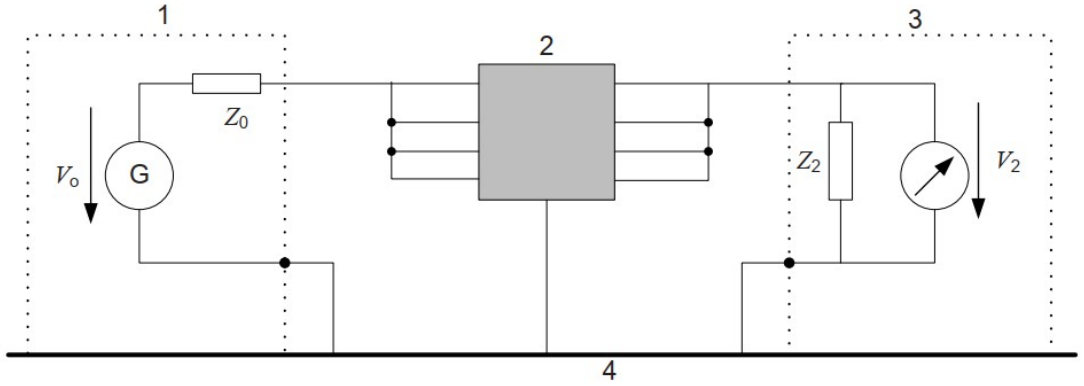
$$IL = 20log\frac{V_o}{2V_2} \tag{4.1}$$

Where V_o is the open circuit generator voltage and V_2 is the output voltage. In the standard configuration of a NA the reference impedance Z_0 is 50 Ω so $V_2 = \frac{V_o}{2}$. This corresponds to:

$$IL = -20log|S_{21}| \text{ dB} \tag{4.2}$$

4.1.2 CM measurement setup

To measure the CM IL the inputs of the filter shall be connected together to the port 1 of the VNA, whereas the outputs shall be connected in parallel to port 2 of the VNA as shown in the generic example in figure 4.1.



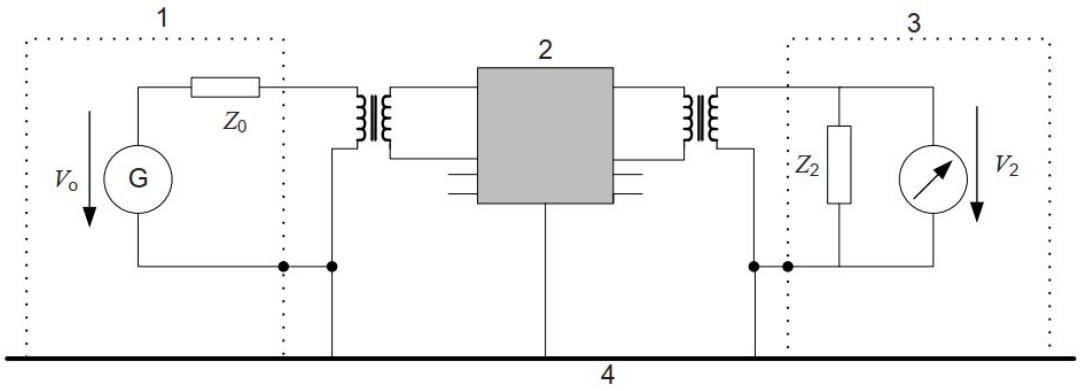
Key	
1	signal generator
2	EMC filtering (device under test)
3	measuring receiver
4	reference potential (metallic ground plane)
V_o	open circuit generator voltage
V_2	output voltage
Z_0	generator impedance
Z_2	receiver impedance

Figure 4.1. Common Mode test circuit (example: 4-line-filter) [8]

4.1.3 DM measurement setup

Each two input lines and the corresponding output lines shall be measured through isolating transformers, with a turn ratio of 1:1, leaving the unused

lines not terminated like shown in figure 4.2.



Key

1	signal generator
2	EMC filtering (device under test)
3	measuring receiver
4	reference potential (metallic ground plane)
V_o	open circuit generator voltage
V_2	output voltage
Z_0	generator impedance
Z_2	receiver impedance

Figure 4.2. Differential Mode test circuit (example: 4-line-filter) [8]

Balun de-embedding

As an isolation trasformer in this work will be used a balun with a turn ration 1:1 and 50 Ω impedance. Since the balun transformer introduces an error in the measurement a de-embedding procedure allows to remove it as shown in figure 4.3. Firstly the balun gets measured on a purposely made PCB then the filter with the balun is measured. The S-parameters are converted in T-parameters using the following formula:

$$\begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} = \frac{1}{S_{21}} \begin{pmatrix} S_{12}S_{21} - S_{11}S_{22} & S_{11} \\ -S_{22} & 1 \end{pmatrix} \tag{4.3}$$

Then the balun contribution can be removed:

$$T_{balun}^{-1} \cdot T_{balun} \cdot T_{DUT} \cdot T_{balun} \cdot T_{balun}^{-1} = T_{DUT} \tag{4.4}$$

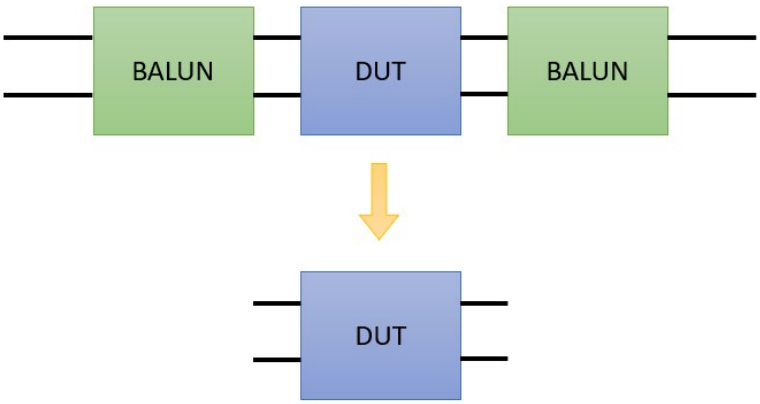


Figure 4.3. Balun de-embedding

Finally using equation 4.5 the Scattering matrix with only the filter can be found:

$$\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} = \frac{1}{T_{22}} \begin{pmatrix} T_{12} & T_{11}T_{22} - T_{12}T_{21} \\ 1 & -T_{21} \end{pmatrix} \tag{4.5}$$

Balun choice

A search was conducted in order to find a wideband transformer with low insertion loss and small package to be inserted on the PCB. The solutions found are reported in table 4.1.

Part Number	**Manufacturer**	**Frequency Range**
ADT1-1+	Mini-Circuits	150 kHz - 400 MHz
TC1-6X+	Mini-Circuits	150 kHz - 350 MHz
TC1-6+	Mini-Circuits	150 kHz - 300 MHz

Table 4.1. Available baluns

Since the ADT1-1+ has wider bandwidth it has been chosen.

4.2 Network Analyzer

There are two types of Network Analyzer: Scalar Network Analyzer (SNA) which measures only amplitude and Vector Network Analyzer (VNA) which measures amplitude and phase. The procedures described in the CISPR 17 regulation are about two port VNAs which allow to measure Scattering (S) parameters. As shown in figure 4.4 a signal is sent through a DUT and the Network Analyzer measures the incident, reflected, and transmitted signals to calculate the forward S-parameters [17]. Some of the key parameters of the VNA are described below.

- **Frequency range** The range of frequencies in which the measurements are performed. Since the normative [7] gives a limit of the emissions of the inverters considered in this work in the frequency range 150 kHz - 30 MHz the goal of this measurement campaign is to measure the IL of the filters at least in this range so the results can be used to evaluate the attenuation of the emissions.

- **Output power and trace noise** The power output is indicated by the instrument in dBm and refers to a 50 Ω impedance; increasing the power allows to reduce the trace noise.

- **Instrument calibration** The instrument needs calibration in order to remove the effects of the connectors and cables before the beginning of the measurement session. This can be done manually or using an electronic calibration kit: the procedure is to connect both ports to a 50 Ω load, a short, an open and connect them together. While doing this procedure the instrument performs the computations required.

- **IF filter** The Intermediate Frequency filter filters the RF signal that is down-converted using a mixer and a local oscillator. Decreasing its bandwidth the noise is greatly improved at the expense of a increase in measurement time.

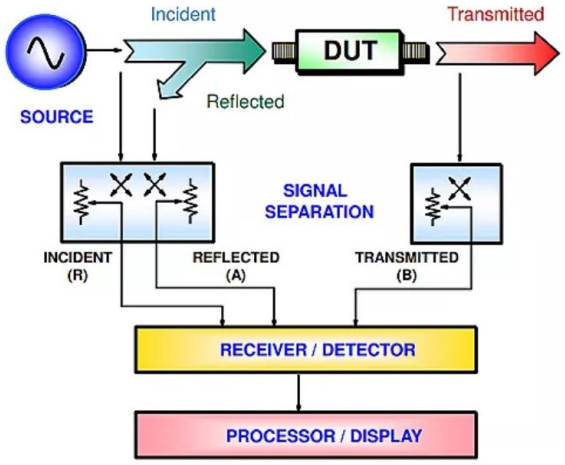


Figure 4.4. General Network Analyzer block diagram [17]

4.3 Filters PCB

The PCBs have been designed by FLAG-MS in order to follow the mechanical specifications required to place the filter on top of the driver board and into the inverter enclosure. Some design considerations are required in order to correctly measure the IL of the filter.

4.3.1 Connections to lab instruments

To connect the filter to the VNA it is necessary to use a coaxial RF connectors, which in this case consists of through-hole SMA connectors which are easy to connect to the instruments available in the lab directly or using adapters.

Four 0 Ω resistors allow to change between the CM and DM measurement configurations.

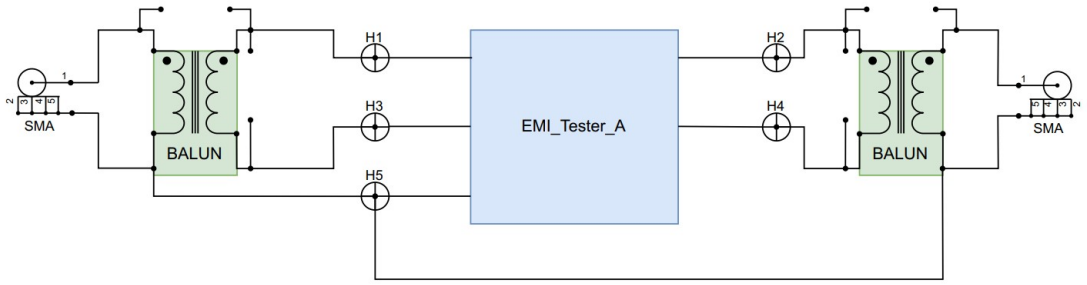


Figure 4.5. Connection diagram for DM IL measurement

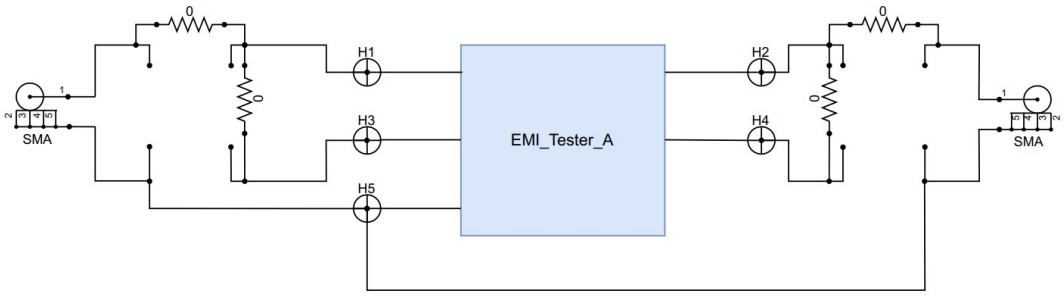


Figure 4.6. Connection diagram for CM IL measurement

Since the distances between the SMA (SubMiniature version A) connector and the plated holes for the connection to the inverter (as shown in figure 4.7) and the symmetrical for the connection to the battery are in the order of 3 cm, thus less than $\frac{\lambda}{20}$ it is not needed to design a microstrip with a characteristic impedance of 50 Ω.

$$\lambda = \frac{c}{f\sqrt{\varepsilon_{r,FR4}}} = \frac{3 \cdot 10^8}{30 \cdot 10^6 \cdot \sqrt{4}} = 5\ m \tag{4.6}$$

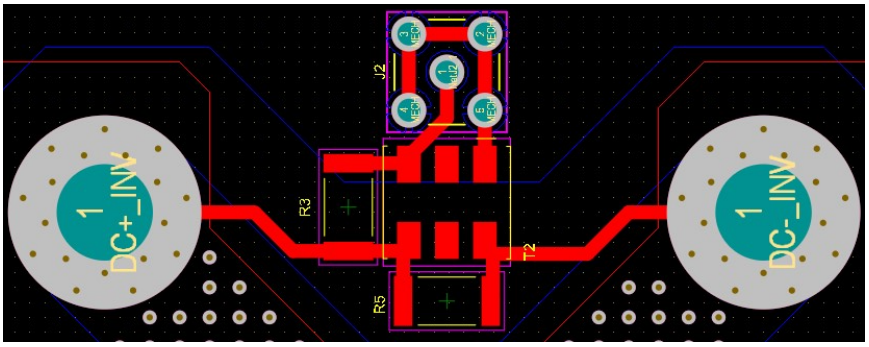


Figure 4.7. Close up view of the traces that connect the SMA connector to the board

4.3.2 Single stage filter: EMI Tester B

The single stage filter has been named EMI Tester B, sometimes shortened to EMI B. A 3D view of the filter is shown in figure 4.8 where is possible to see that the choke is the largest component in the circuit.

In figure 4.9 are highlighted in red the top layer traces while in figure 4.10 are highlighted in blue the bottom traces. The traces DC+_GEN, DC-_GEN, DC+_INV and DC-_INV are present of both layers and are connected with thermal vias allowing them to carry more current and to better dissipate the heat. The MECH trace is present only on the bottom layer and forms a loop around the perimeter of the board. Four 0 Ω resistors have been added to the bottom of the board and allow to short the windings of the choke or to leave only one wire connected; this configurations will be called respectively Parallel Wires (PW) and Single Wire (SW). This has been done to evaluate the value of the inductance of the choke.

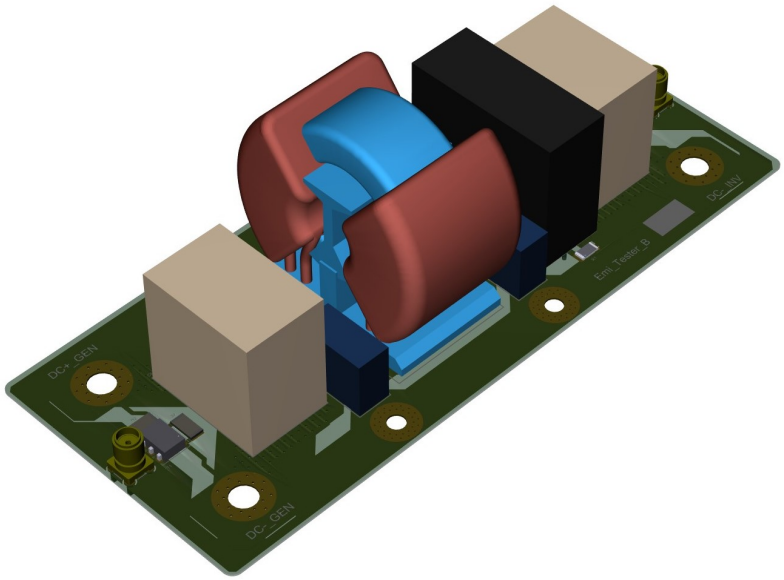


Figure 4.8. 3D view of the PCB EMI Tester B

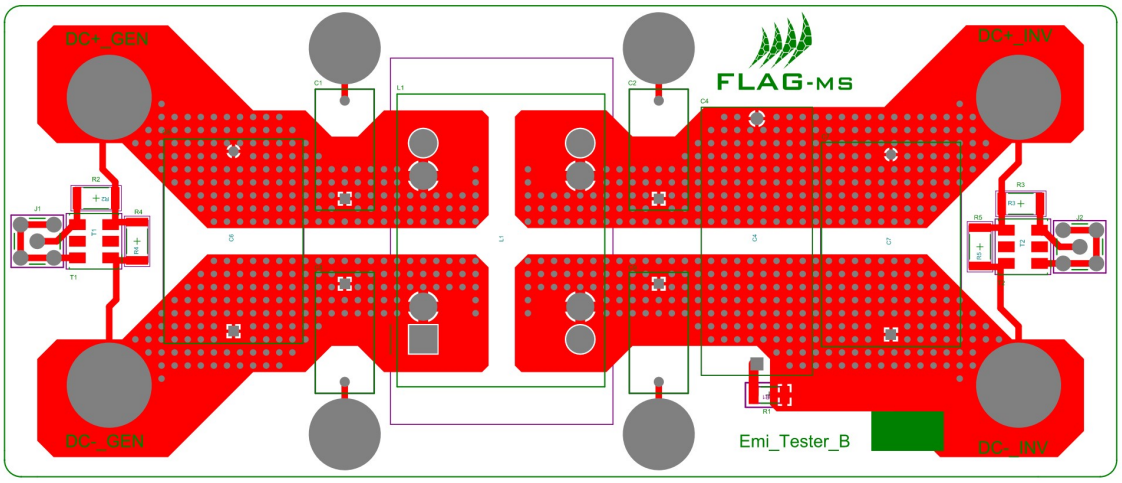


Figure 4.9. EMI B Top layer

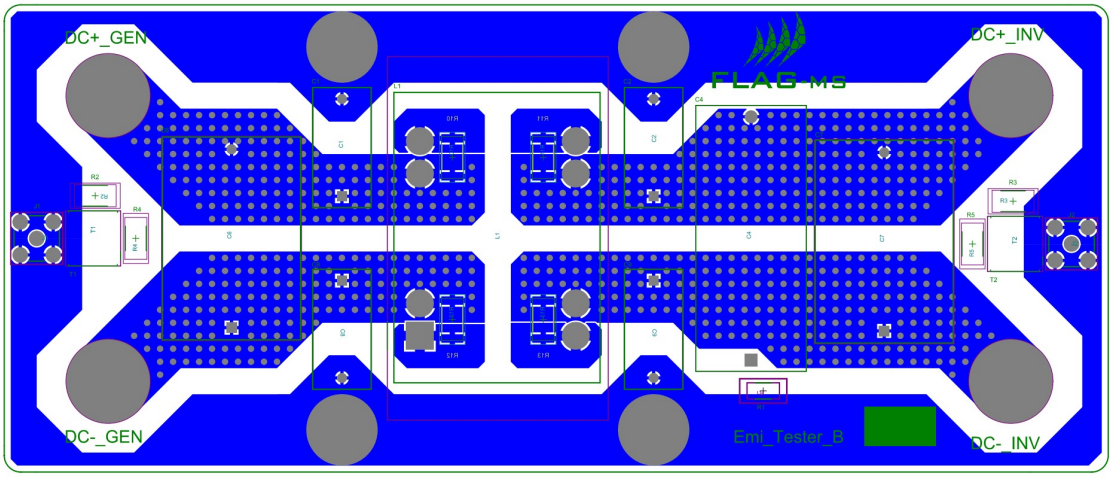


Figure 4.10. EMI B Bottom layer

4.3.3 Double stage filter: EMI Tester A

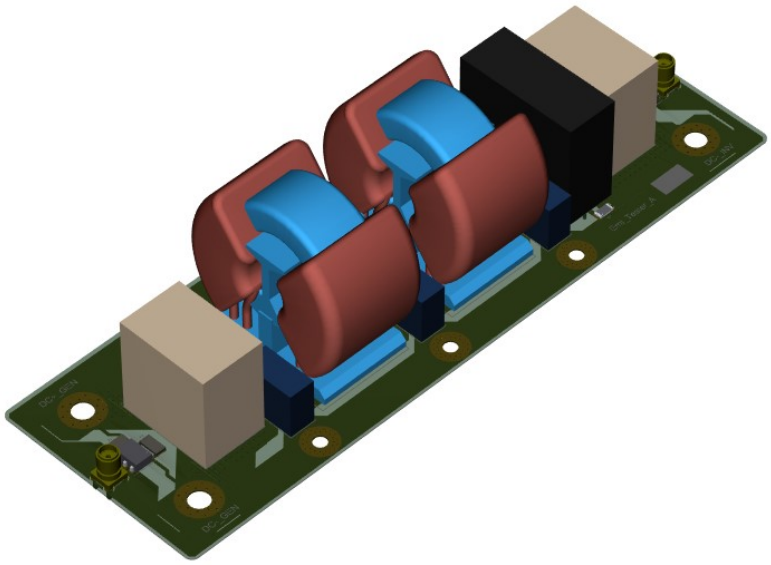


Figure 4.11. 3D view of the PCB EMI Tester A

The filter with two stages has been named EMI Tester A and will sometimes be called EMI A. The addition of a CMC and two Y-capacitor increases its length. The same design considerations of the single stage filter have been followed and are visible in the top layer view (figure 4.12) and bottom layer (figure 4.13).

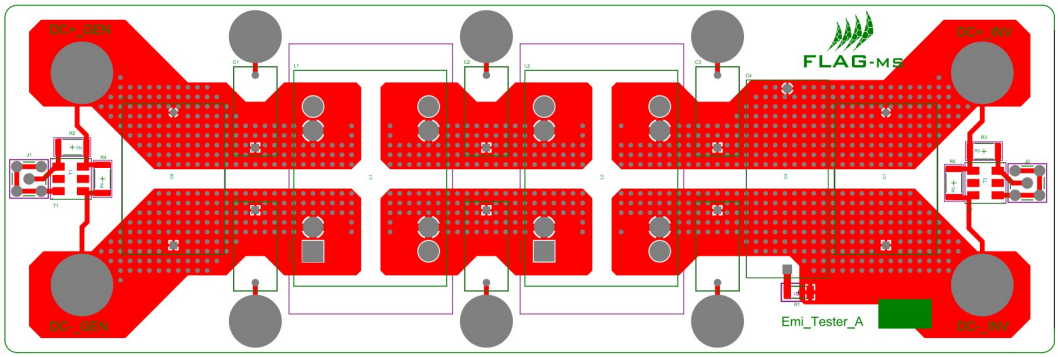


Figure 4.12. EMI A Top layer

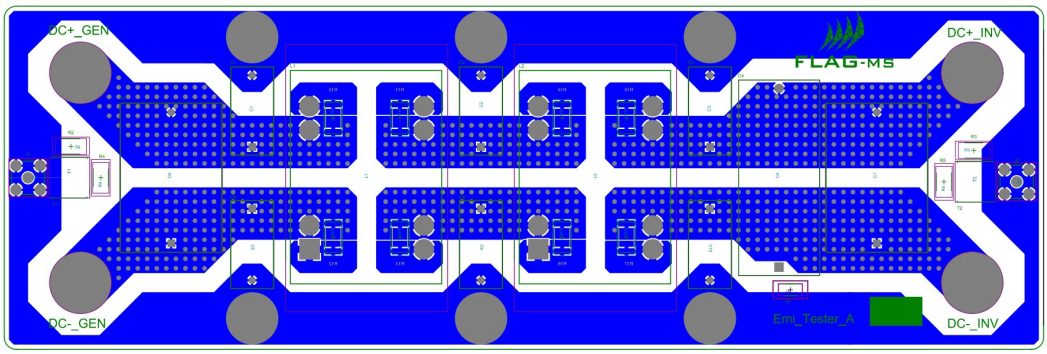


Figure 4.13. EMI A Bottom layer

4.3.4 PCB test balun

A PCB with a balun and two SMA connections has been designed to enable measurement of the insertion loss of the balun which will be considered the same as the ones in the EMI B and EMI A PCBs since they are from the same production batch.

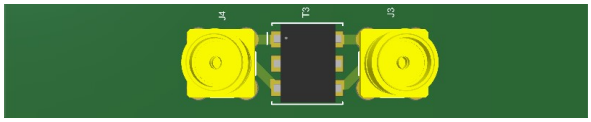


Figure 4.14. PCB balun to measure Insertion Loss

4.4 IL Lab measurements

In this section will be shown the final measurements obtained using two different VNAs. During the lab sessions different settings have been tried and at the end the measurements with the most accurate results have been accepted. The table in figure 4.15 explains the naming scheme that will be used to name the different measurements:

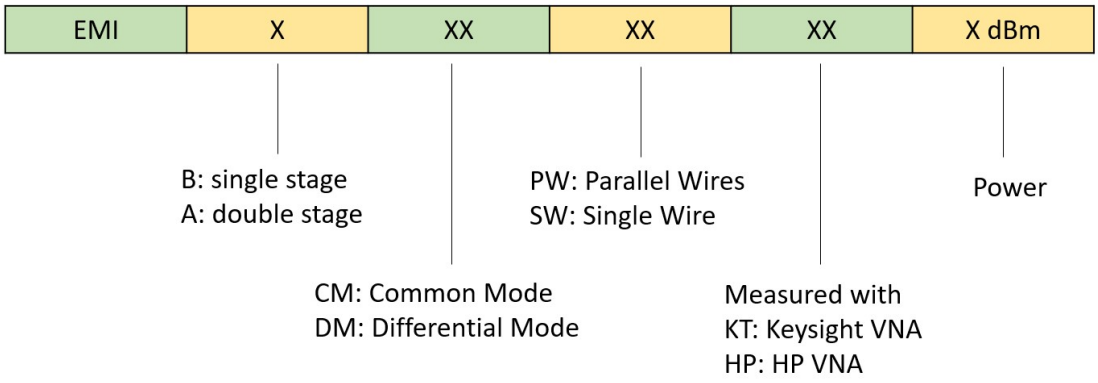


Figure 4.15. Explanation of simulation name

4.4.1 Measurements with NA Keysight P9371A

The calibration has been performed using the Keysight electronic calibration module N7551A.

Setup

Sweep type	Log Frequency
Sweep Properties	
Start	300 kHz
Stop	100 MHz
Power	-5 dBm
Points	1601
IF Bandwidth	100 Hz

Table 4.2. Keysight P9371A measurement settings

Balun measurement

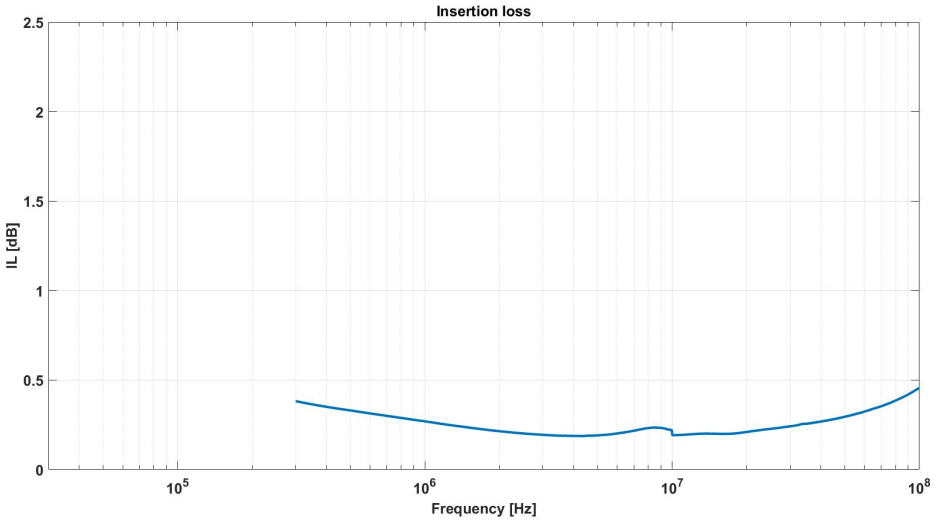


Figure 4.16. Measure of the IL of the balun

Figure 4.17. ADT1-1+ Typycal Performance Data [18]

The result of this measurement is comparable with the performances of the component described in the datasheet. This data will be used to de-embedd the balun from the circuit in the differential mode measurements.

De-embedding example

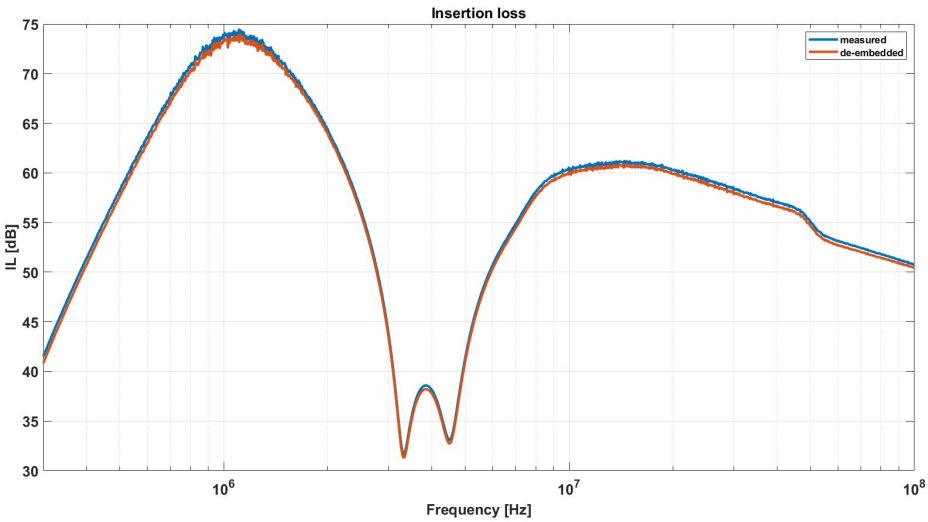


Figure 4.18. EMI B DM PW KT -5 dBm before and after de-embedding

An example of the de-embedding procedure is shown in figure 4.18 where the difference between the blue curve (measured data) and the red curve (after de-embedding) is due to the IL of the balun that is removed using the procedure described above.

Measurements with -5 dBm

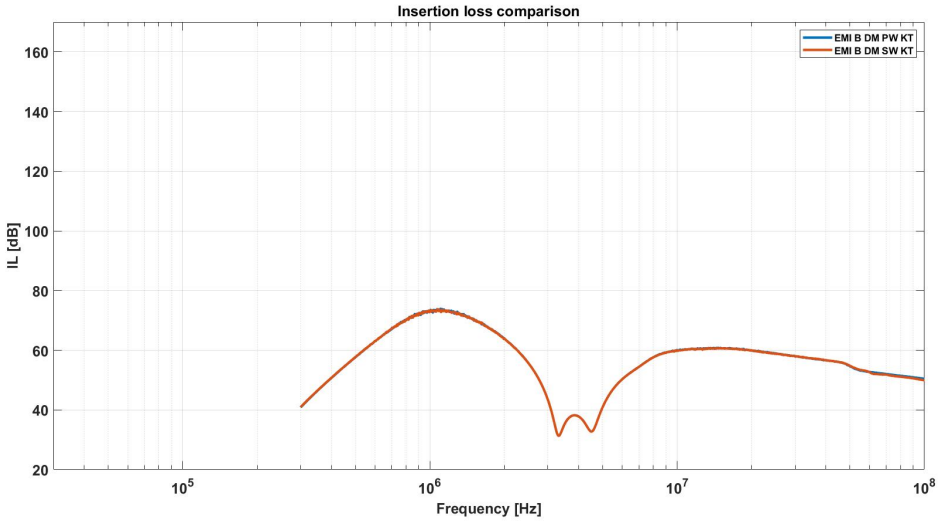


Figure 4.19. Comparison of insertion loss measurement with NA Keysight EMI B DM

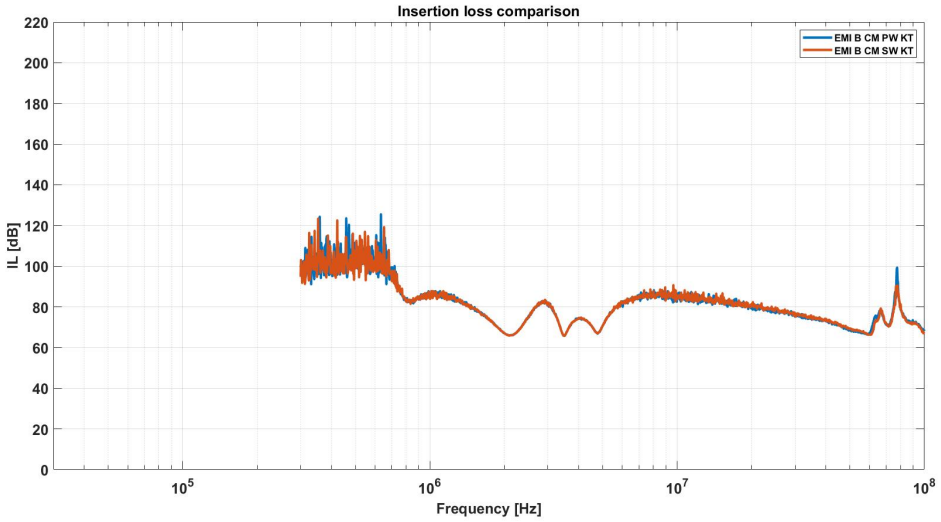


Figure 4.20. Comparison of insertion loss measurement with NA Keysight EMI B CM

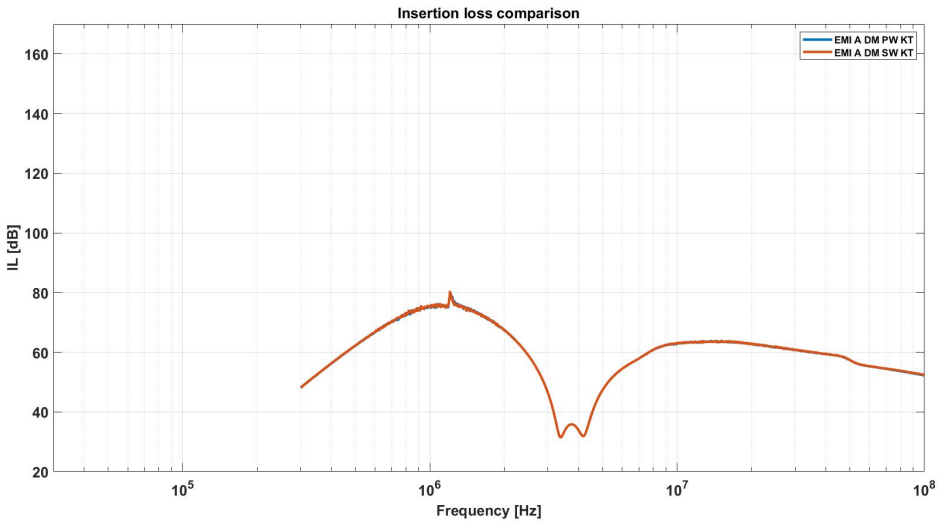


Figure 4.21. Comparison of insertion loss measurement with NA Keysight EMI A DM

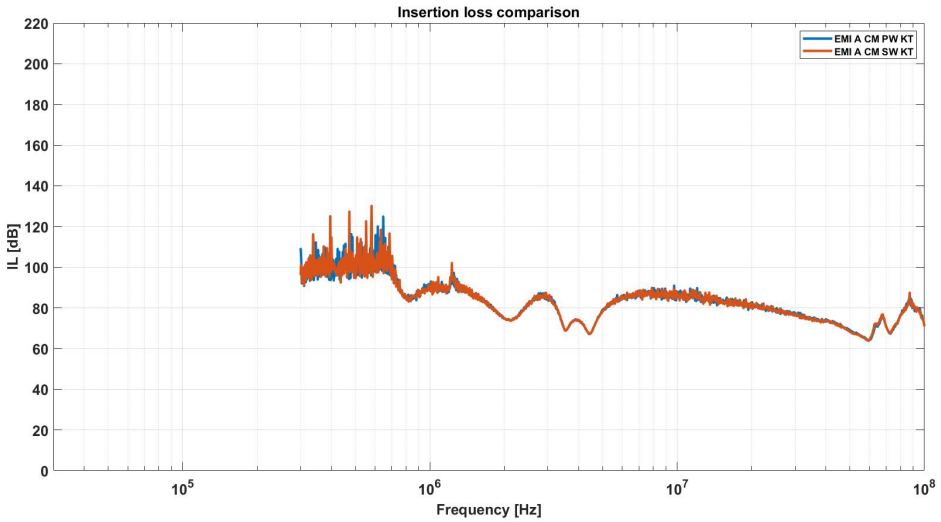


Figure 4.22. Comparison of insertion loss measurement with NA Keysight EMI A CM

In all of this measurements it is noticeable the presence of noise, to avoid that in the forthcoming measurements the power will be increased.

4.4.2 Measurements with NA HP 8753D

This instruments allows to measure the scattering parameters down to 30 kHz so it has been used for the final measurements in order to have data in the 150 kHz - 30 MHz frequency range. For the measurement of the Common Mode IL with the Keysight NA the balun was not removed since it was supposed that its effects were negligible. In practice the primary of the transformer in parallel with port 1 of the NA changed the behavior at low frequency so they will be removed in the measurement with the HP Network Analyzer.

Setup

Sweep type	Log Frequency
Sweep Properties	
Start	30 kHz
Stop	100 MHz
Power	+10 dBm
Points	1601
IF Bandwidth	100 Hz

Table 4.3. HP 8753D measurement settings

Measurements with +5 dBm

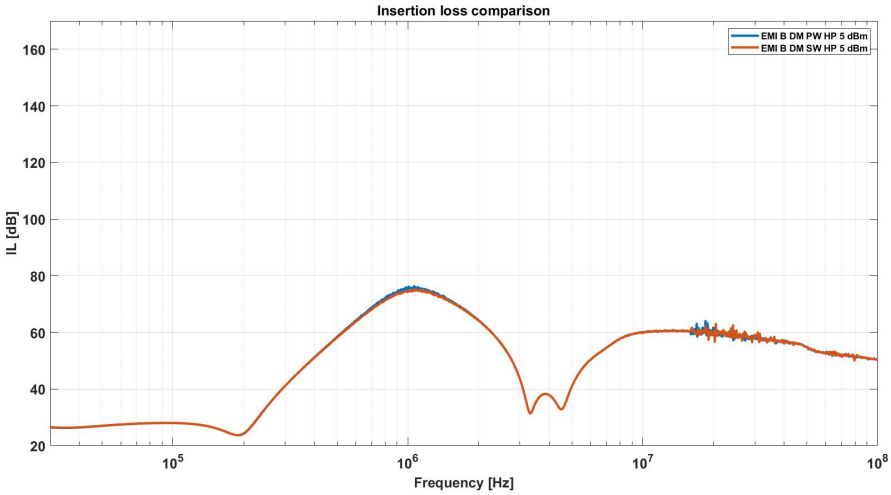


Figure 4.23. Comparison of insertion loss measurement with NA HP EMI B DM

Measurements with +10 dBm

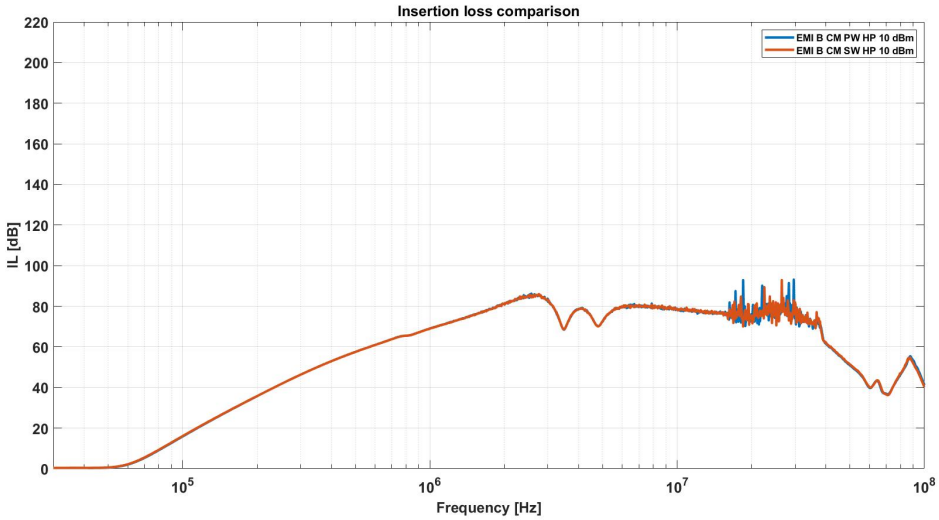


Figure 4.24. Comparison of insertion loss measurement with NA HP EMI B CM without balun

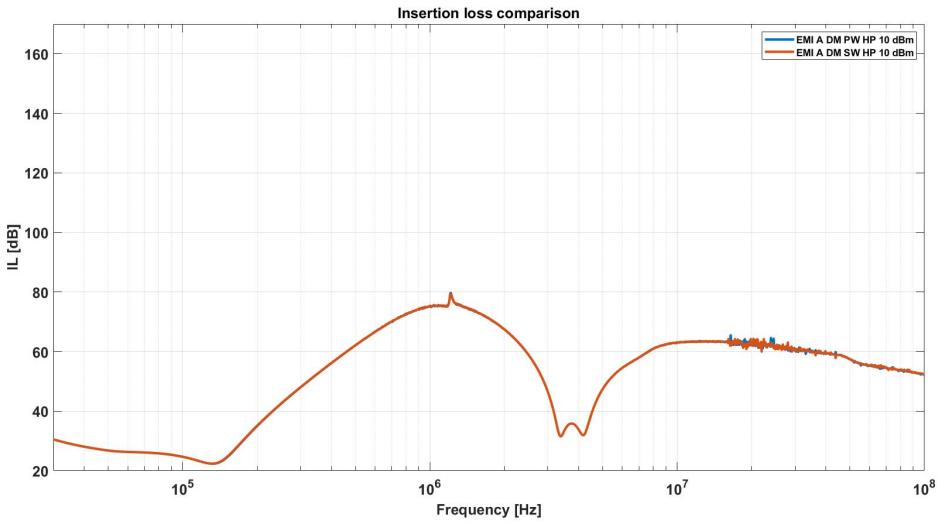


Figure 4.25. Comparison of insertion loss measurement with NA HP EMI A DM

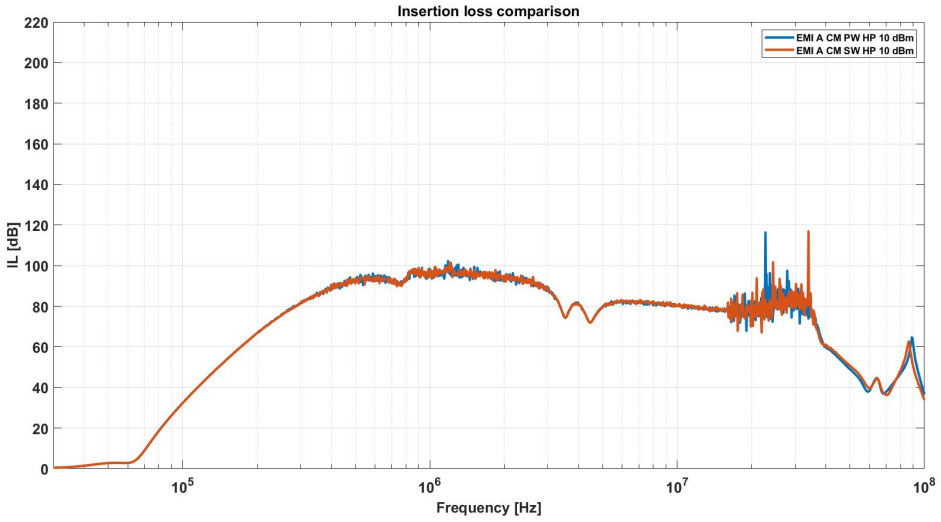


Figure 4.26. Comparison of insertion loss measurement with NA HP EMI A CM

4.4.3 Balun effect on the Common Mode insertion loss

Since the balun case is made of plastic intially the Common Mode IL measurements were performed without de-soldering the component to avoid destroying it. After comparing the measurement with the simulations it was found out that at low frequency (30 kHz - 3 MHz approximately) shown in

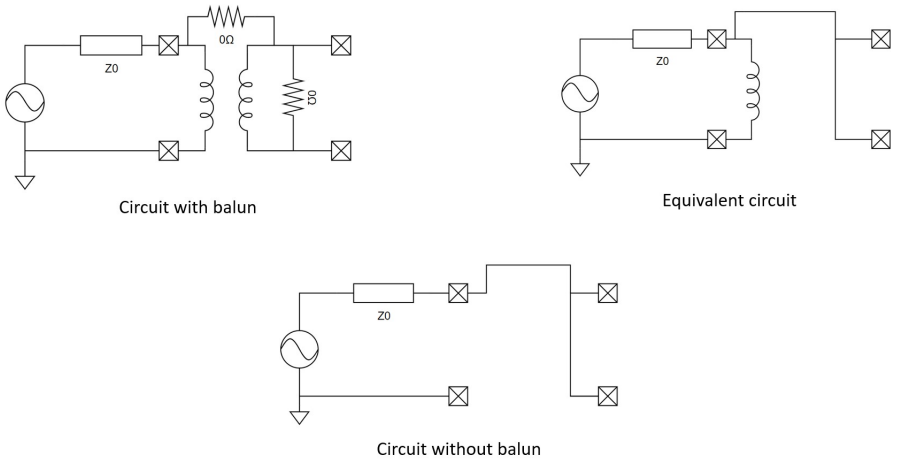


Figure 4.27. Equivalent circuit of port 1 with balun and resistors used to measure CM IL

figure 4.28 and 4.29 in blue there was up to 50 dB difference. It was assumed that the fault was due to the presence of the primary of the balun that in parallel with port 1 of the NA was behaving like a short circuit. Increasing the measurement frequency the balun starts to become an open circuit so the measurements are unaffected. In figure 4.27 are shown the equivalent circuits before and after the removal of the balun. The results of the IL measurements without the baluns are shown in red. Unfortunately the baluns were destroyed in the process of de-soldering.

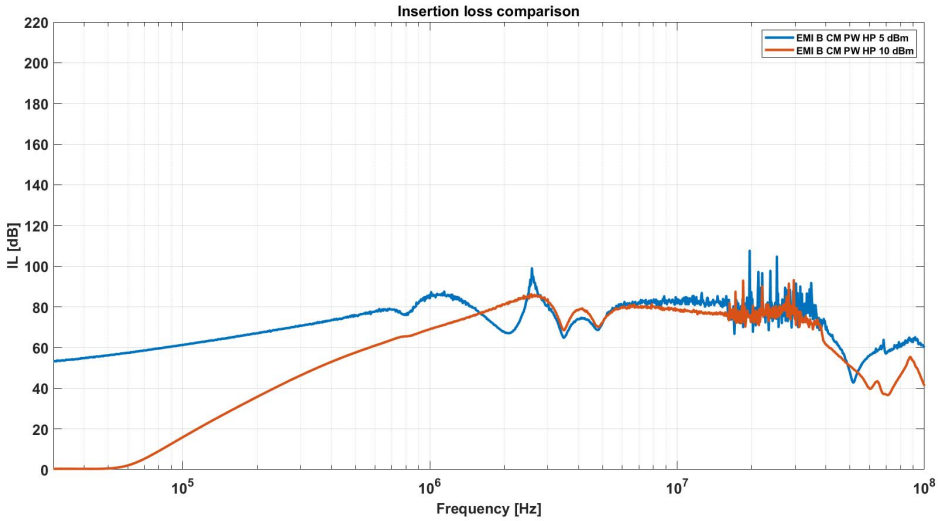


Figure 4.28. Common Mode Insertion Loss comparison measurement with balun an without balun EMI B

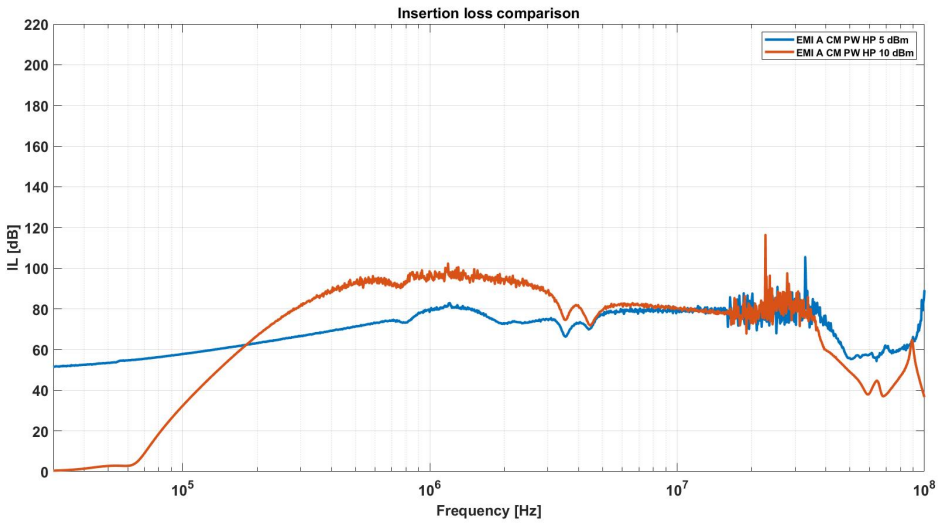


Figure 4.29. Common Mode Insertion Loss comparison measurement with balun an without balun EMI A

4.4.4 Comparison between single and double stage filters

As expected from the design of the filters for the common mode the double stage one has a slope of approximately 40 dB/dec and an higher IL at low frequency but after 3 MHz their value is roughly the same.

The Differential Mode IL is almost the same for both filters, but the pole is at lower frequency in the two stage filter case.

There is almost no difference between the single wire and parallel wire case. The resonances measured do not correspond to the simulated ones so further investigation on this behavior is needed.

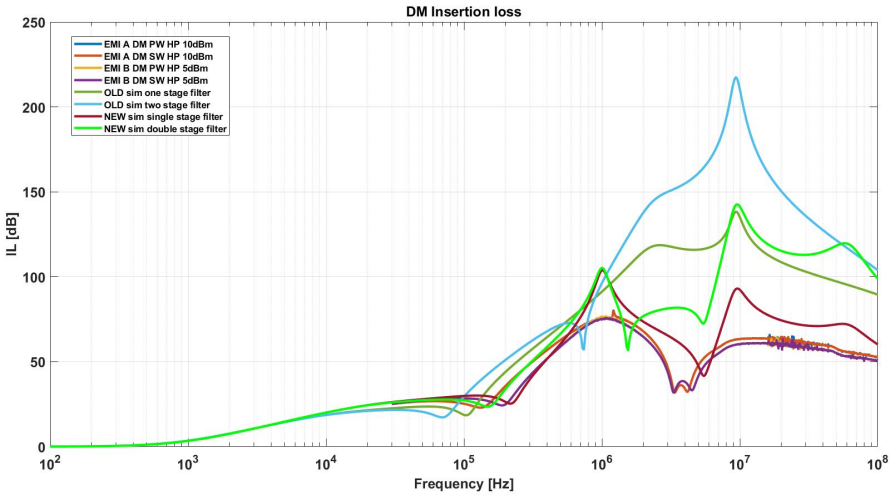


Figure 4.30. Differential Mode Insertion Loss comparison measurement between single stage filter and double stage filter

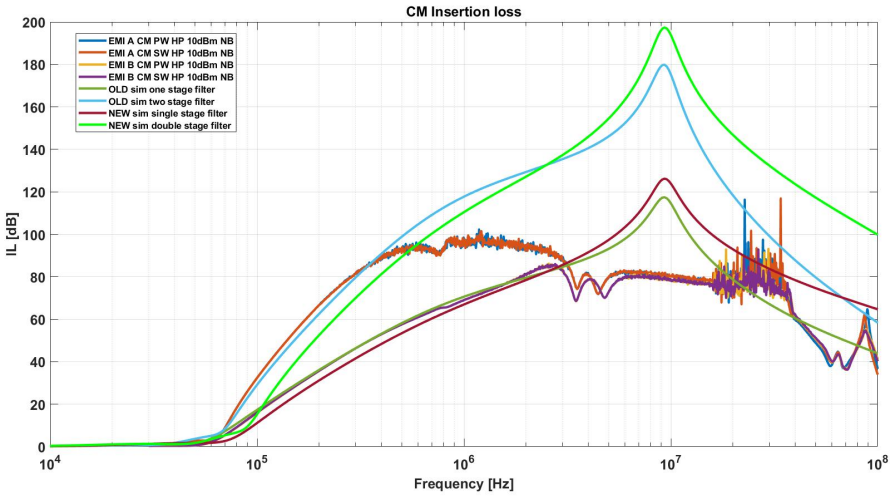


Figure 4.31. Common Mode Insertion Loss comparison measurement between single stage filter and double stage filter

Chapter 5

Circuital and EM simulations

In this chapter a study on the causes of the resonances is carried out, then more advanced simulation techniques are used to take in account the contribution of the PCB traces and finally these techniques are used to simulate the filter connected to the ditcher inverter to obtain the conducted emissions spectrum.

5.1 Circuital simulations

An initial study has been conducted using LTspice and manually introducing components to model the resonances.

5.1.1 EMI Tester B resonances

Starting from the IL measurements in figure 4.23 and 4.24 it is clear that some unidentified resonances are present at about 4 MHz, not identified with the ideal circuit in figure 5.1. Taking a look at the circuit (figure 4.9 and figure 4.10) seems possible that exists a parasitic capacitance between the MECH traces on the bottom of the PCB and the upper traces used to carry power. The area of the bottom traces is about 4000 mm^2 and the FR4 thickness is 1.55 mm so they are used as a first estimate in equation 5.1.

$$C = \frac{\varepsilon_0 \varepsilon_r \text{Area}}{d} \simeq 88 \text{ pF} \tag{5.1}$$

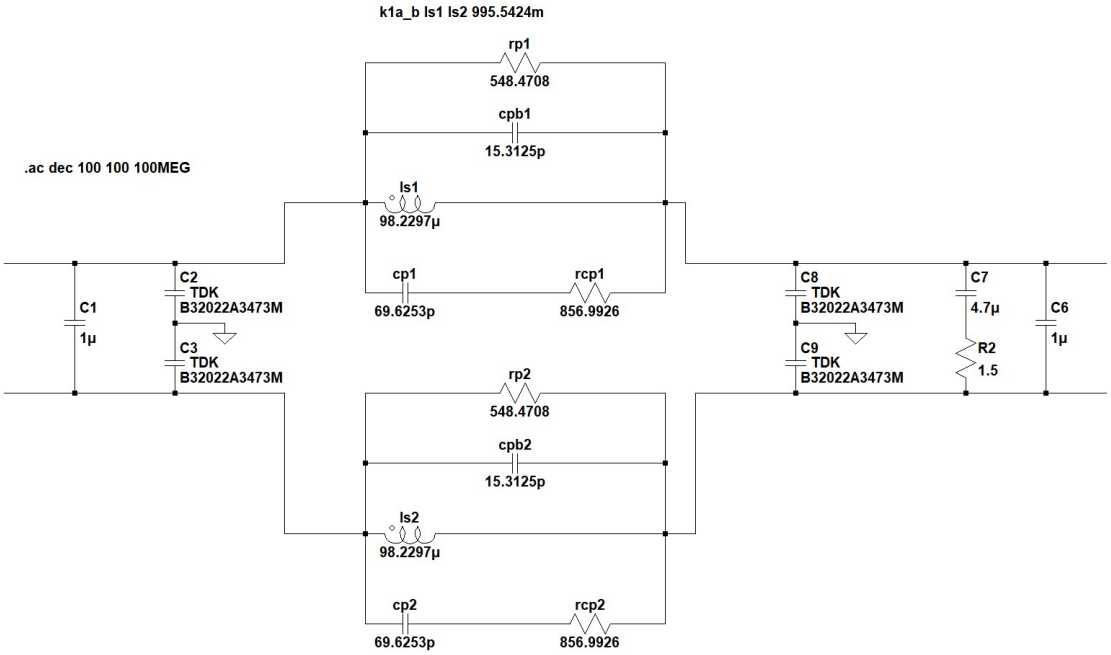


Figure 5.1. EMI B original circuit

Using these parasitic values in the LTspice simulation shows that the parasitic capacity exists but only when greater values, with respect to that obtained in equation 5.1, are used the IL results become similar to the measurements.

Differential Mode resonances

The values of C15 and C16 in figure 5.2 are chosen to get two resonances at approximately 4 MHz according to equation 5.2 and shown with the measurement in figure 5.3 (in red). The added resistors in series with the C_x and C_y capacitors reduce the peaks of the resonances. With the result obtained shown in blue in figure 5.3. The choke's parasitic capacitors are removed since they introduce a peak in the simulated IL at around 60 MHz which is not present in the measurement.

$$\mathrm{f} = \frac{1}{2\pi\sqrt{\mathrm{ESL} \cdot \mathrm{C}}} \tag{5.2}$$

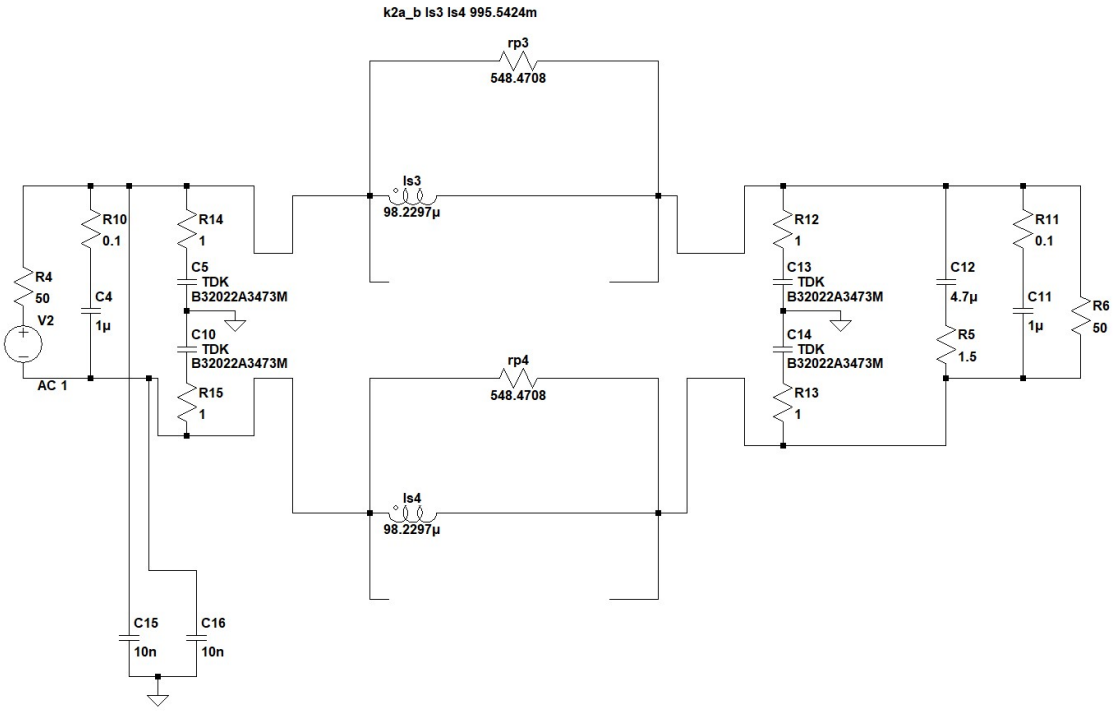


Figure 5.2. EMI B Differential Mode IL parasitic components

Parasitic capacitors value			
Capacitor	Capacitance	ESL	ESR
C15	10 nF	150 nH	0 Ω
C16	10 nF	150 nH	0 Ω

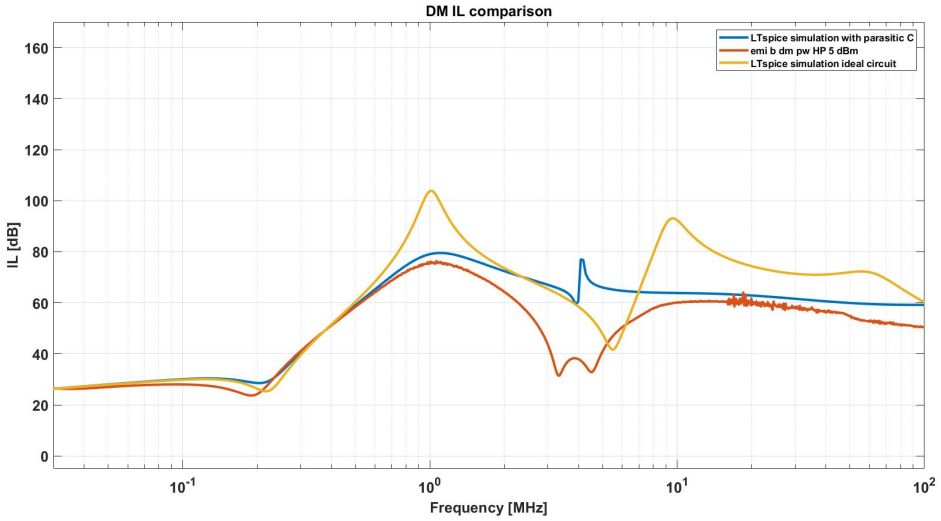


Figure 5.3. EMI B Differential Mode Insertion Loss

Common Mode resonances

As in the DM case two capacitors are used to get the the resonances at 3.5 MHz and 4.8 MHz obtained with the measurement (red curve in figure 5.5) but in this case with different values. The resistors in series with the C_y capacitors reduce the amplitude of the peak of the IL. The results are in blue in the same figure.

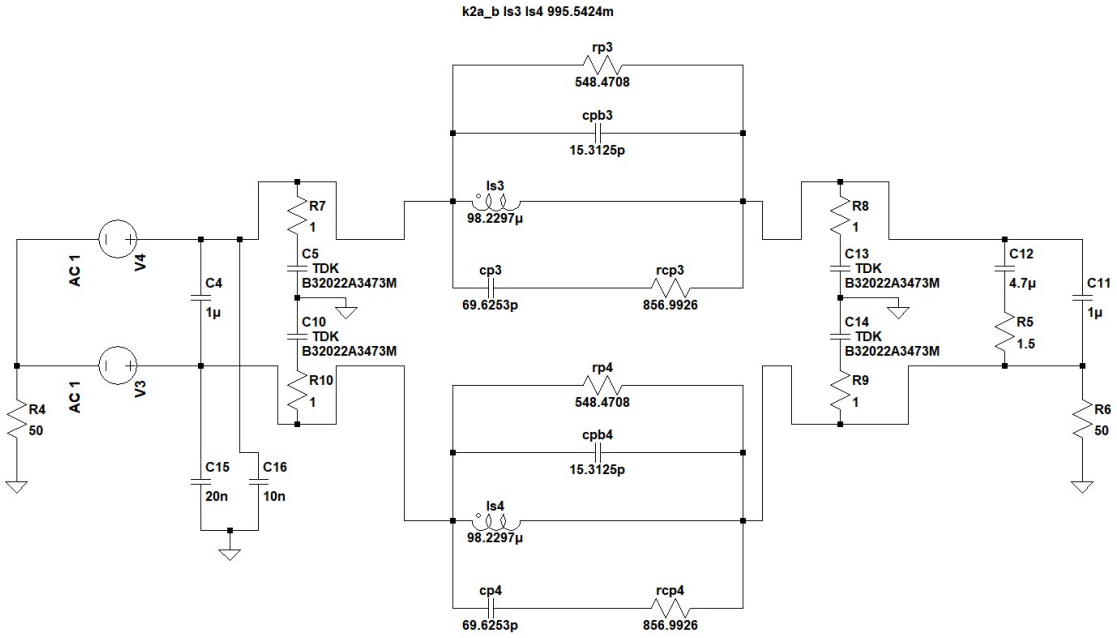


Figure 5.4. EMI B Common Mode IL parasitic components

Parasitic capacitors value			
Capacitor	Capacitance	ESL	ESR
C15	20 nF	150 nH	0.3 Ω
C16	10 nF	150 nH	0.3 Ω

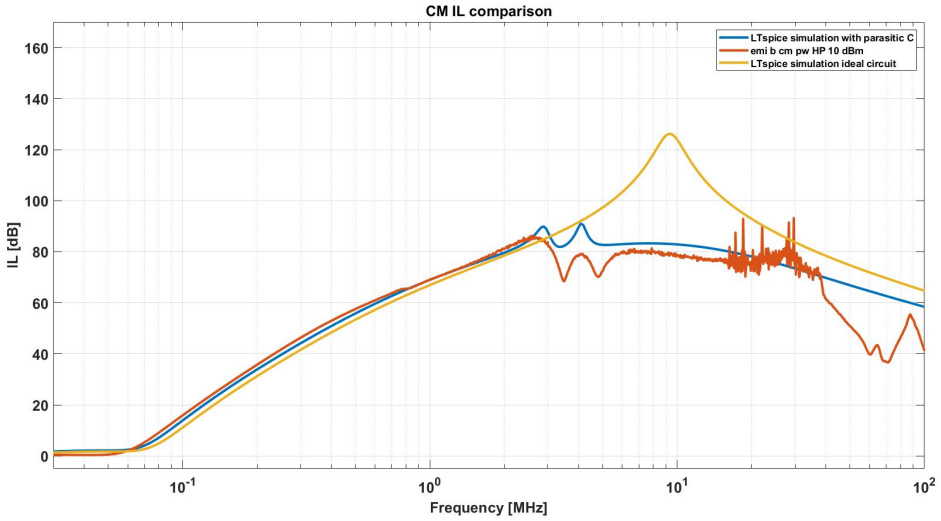


Figure 5.5. EMI B Common Mode Insertion Loss

5.1.2 EMI Tester A resonances

The analysis of the resonances in the circuit is conducted also for the two stage filter starting from the ideal circuit in figure 5.6.

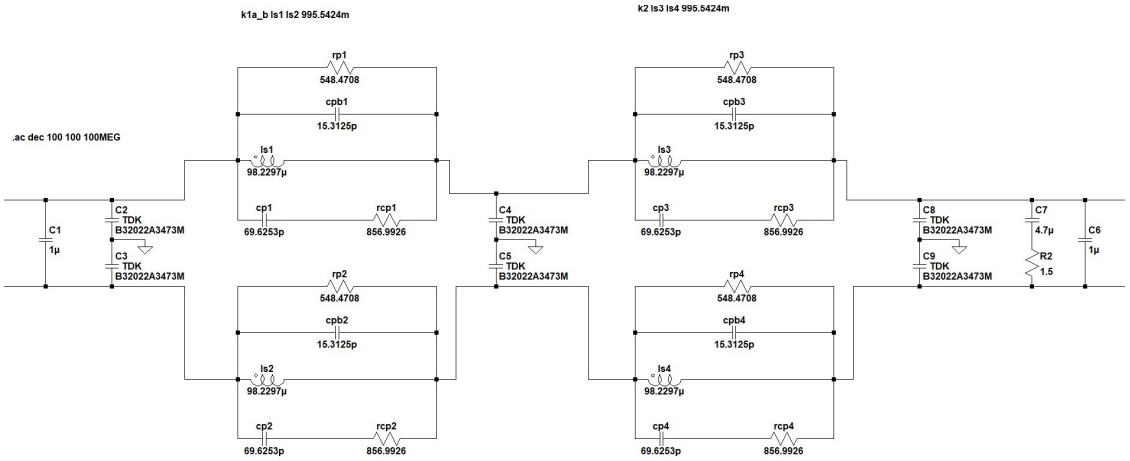


Figure 5.6. EMI A original circuit

Differential Mode resonances

Capacitors C19 and C20 in the schematic in figure 5.7 contribute to the resonances at around 4 MHz, while the resistors in series with the C_x and C_y capacitor reduce the amplitude of the peaks of IL in figure 5.8. The parasitic capacitors in the choke model are removed since they introduce a peak at around 60 MHz which is not present in the measurement.

Parasitic capacitors value			
Capacitor	Capacitance	ESL	ESR
C19	10 nF	150 nH	0 Ω
C20	10 nF	150 nH	0 Ω

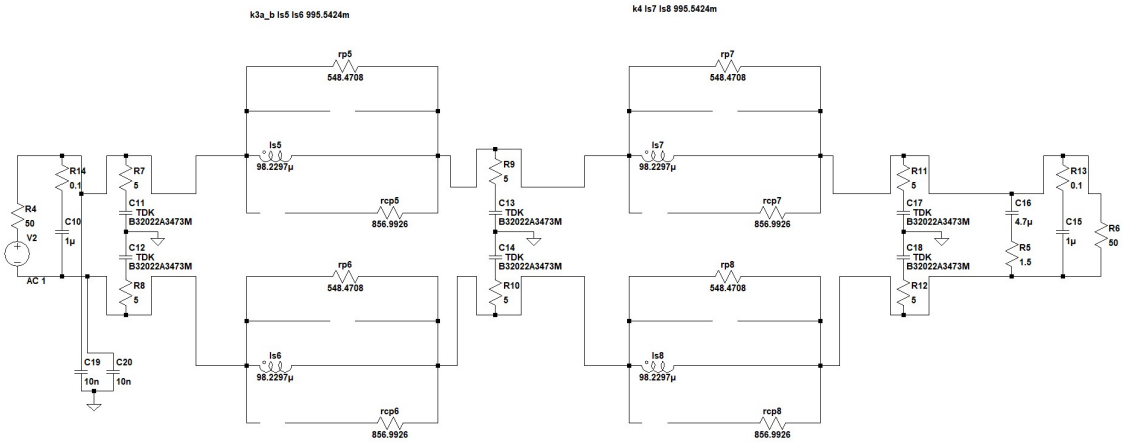


Figure 5.7. EMI A Differential Mode IL parasitic components

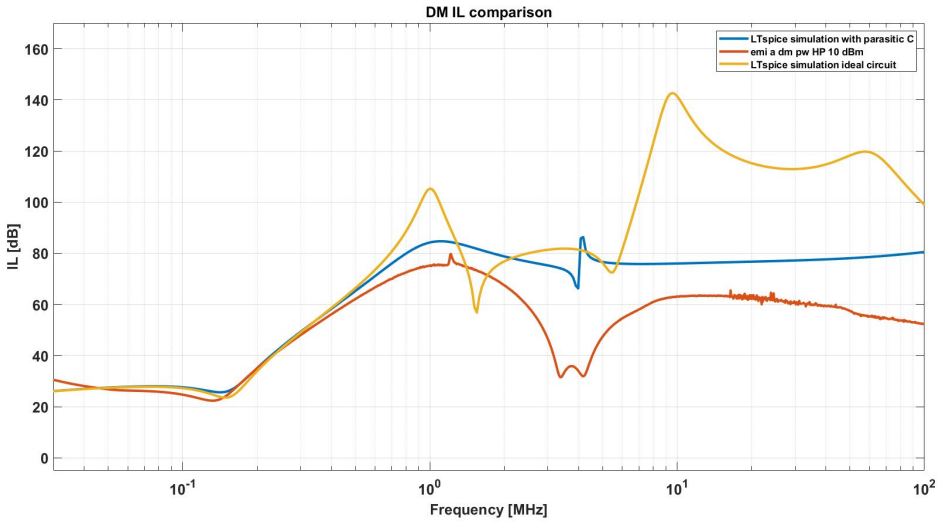


Figure 5.8. EMI A Differential Mode Insertion Loss

Common Mode resonances

As in the single stage filter the capacitors C19 and C20 in figure 5.9 introduce resonances at 3.5 MHz and 4.8 MHz respectively. As before the resistors in series with the C_y capacitors are used to reduce the amplitude of the Insertion Loss. The comparison of measurements and simulations is in figure 5.10.

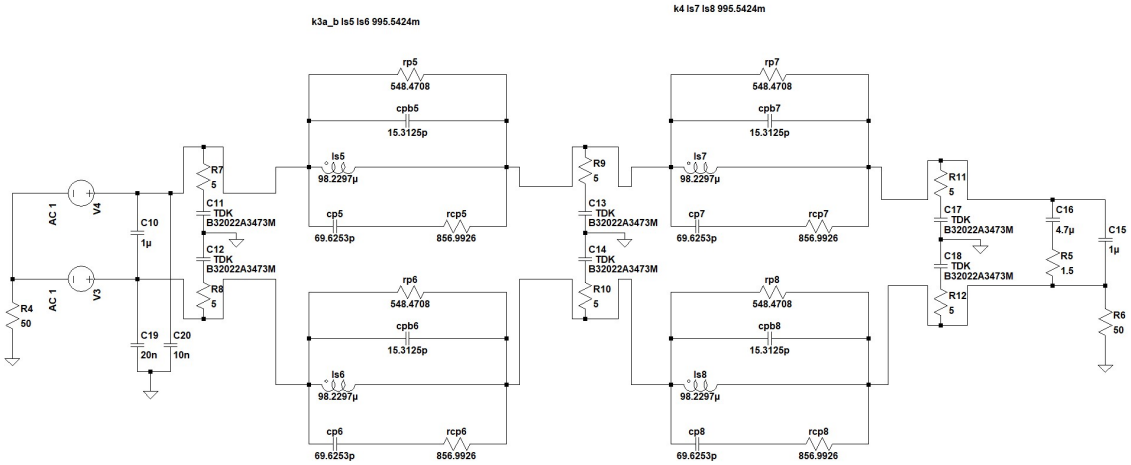


Figure 5.9. EMI A Common Mode IL parasitic components

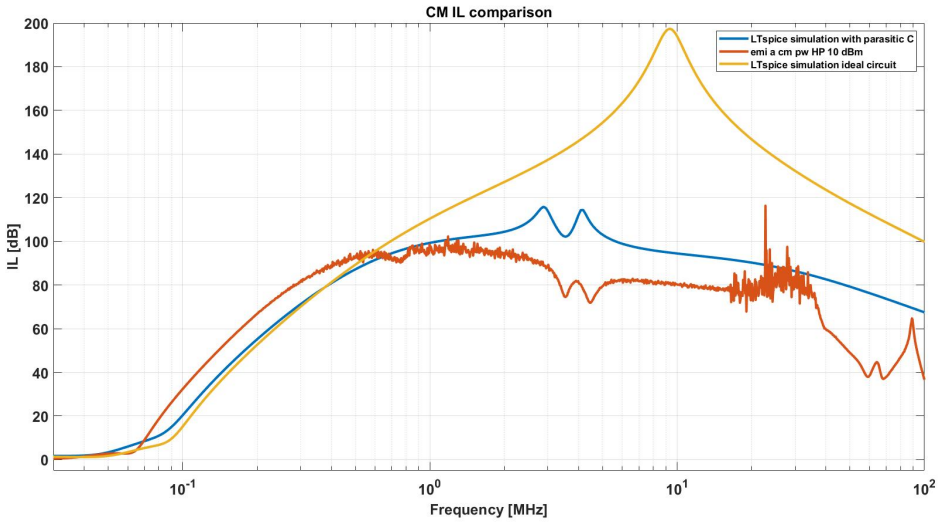


Figure 5.10. EMI A Common Mode Insertion Loss

The value of the components used to replicate the effect of the PCB traces

are too large and do not have a physical meaning, they are just used to replicate the effect of the measurements.

Parasitic capacitors value			
Capacitor	Capacitance	ESL	ESR
C19	20 nF	150 nH	0.3 Ω
C20	10 nF	150 nH	0.3 Ω

5.2 EM field simulations

The software used for this simulations is Keysight Pathwave Advanced Design System (ADS). A built in tool called PEPro allows to take in account all the geometries of the traces, vias and connectors on the board and convert the circuit in a scattering parameter matrix. The simulated S_{21} is then converted in IL using equation 4.2. The procedure that has been followed and the results obtained are described below.

5.2.1 PCB import and layer stackup definition

As the first step, the data from the Altium PCB design tool are transformed to ADS using the ODB++ file format which allows to bring all the PCB data including the layer stackup and the components. Then the layer thickness and material type are checked if they match the designed PCB. In figure 5.11 it is displayed the layer stackup and in figure 5.12 the thickness of the layers.

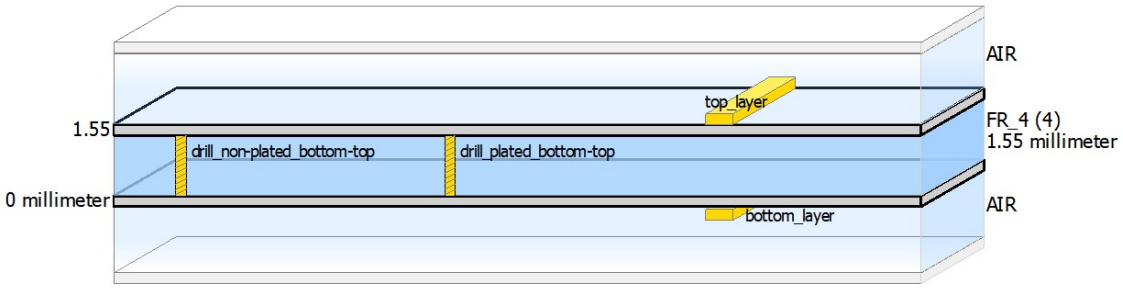


Figure 5.11. Substrate view in ADS

The FR4 material specifications are provided by the manufacturer and are: dielectric constant $\varepsilon_r = 4$ and loss tangent $\tan\delta = 0.02$.

	Type	Name	Material	Thickness
	Dielectric		AIR	
1	Conductor ...	top_layer ...	Copper	0.03556 mm
	Dielectric		FR_4	1.55 mm
2	Conductor ...	bottom_lay...	Copper	0.03556 mm
	Dielectric		AIR	

Figure 5.12. Substrate layer stackup values

A schematic needs to be created for each component in order for the simulation to work.

The comparison between the layout in Altium Designer and the layout imported in ADS, using the EMI B filter as an example, is displayed respectively in figure 5.13 and figure 5.14.

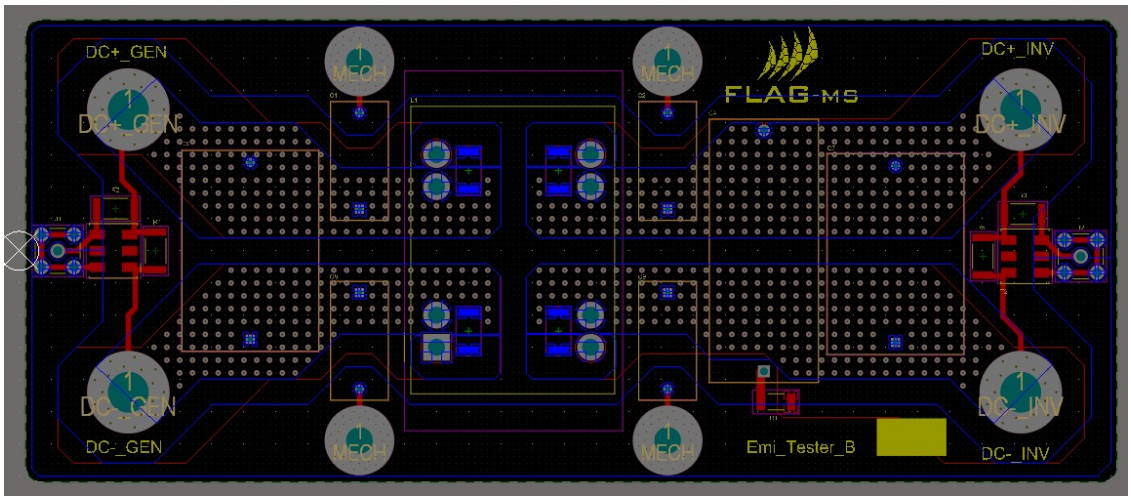


Figure 5.13. Layout view of the EMI B filter in Altium Designer

5.2.2 IL simulations

The analysis used for this simulation is the "Parasitic Extraction-All Nets" available in the PEPro tool. The first step is to define the ports, that have a "+" symbol for the signal and a "-" symbol for the reference terminal. The "Component Models" field needs to be loaded with the components that will be used for the specific simulation. The software automatically chooses the

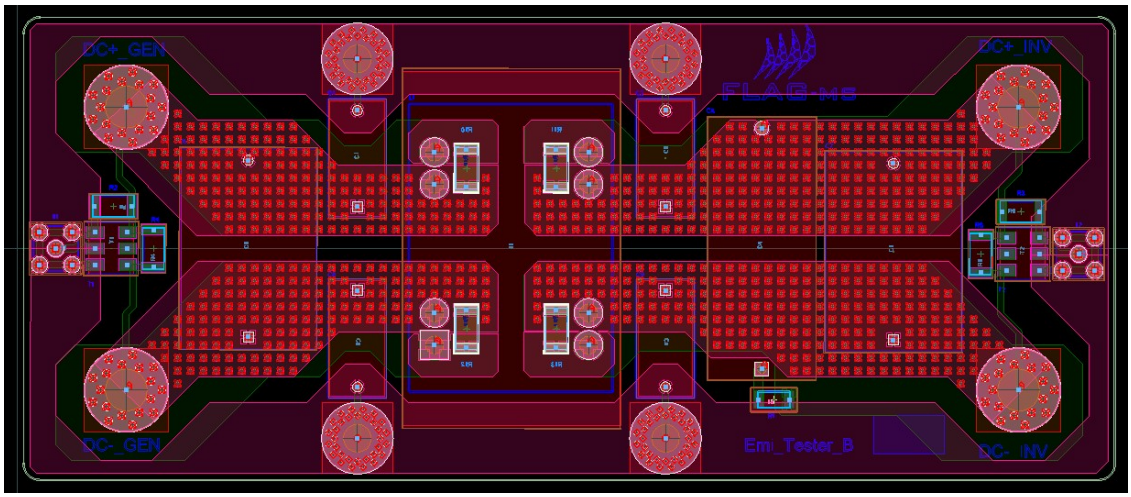


Figure 5.14. Layout view of the EMI B filter in ADS

model from the library previously imported, and the schematic of the components is defined manually ,but it is also possible to measure a component with a NA and use the results instead of an ideal model. This second option was not used. It is important to mention that the balun has been defined as an ideal 1:1 transformer, so there isn't the need to carry out the de-embedding procedure with these simulations. The simulation type and frequency points need to be defined, along with the simulator and its settings. The simulation can be run on the local machine or on a server and, when the simulation is complete, it is possible to generate a sub circuit that will be used to extract the scattering parameters and subsequently get the IL.

Setup

In the PEPro simulation the ports are connected to the bottom layer because a shorter distance between the "+" and "-" lowers the parasitic port inductance eliminating the shunt effect of the vias. An example of port 1 setup is shown in figure 5.15 whereas figure 5.16 shows a top view of the layout with the connections for port 1 and port 2. The connections used for the DM and CM IL measurements are the same used for the lab measurements and the balun and 0 Ω resistor are easily added/removed if needed, as explained before, following the schematic in figure 5.17 and figure 5.18.

With preliminary simulations it has been demonstrated that there is no difference between the results obtained using Momentum RF with respect to

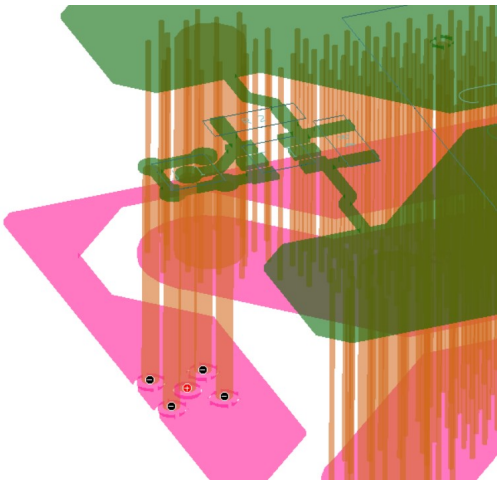


Figure 5.15. Port setup for PEPro simulation used to obtain IL

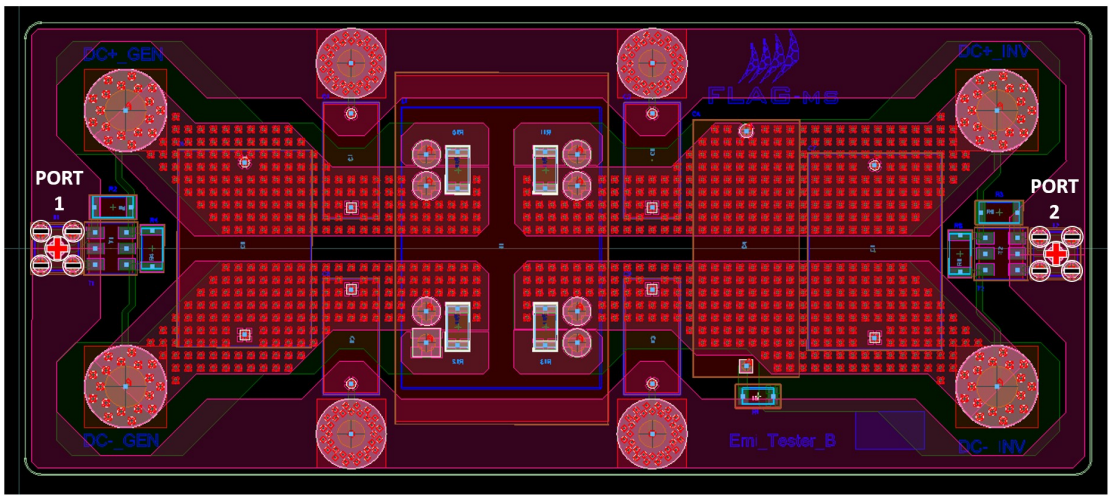


Figure 5.16. View of the ports connections EMI B

the Momentum Microwave simulator, so momentum RF has been used since it is faster. Momentum Microwave improves the results at higher frequencies that are not reached in this work.

The worst case condition for the emissions is obtained using the switching frequency f_{sw}=15 kHz so this value has been used in the simulations. The rise and fall times are the same of the gate driver's.

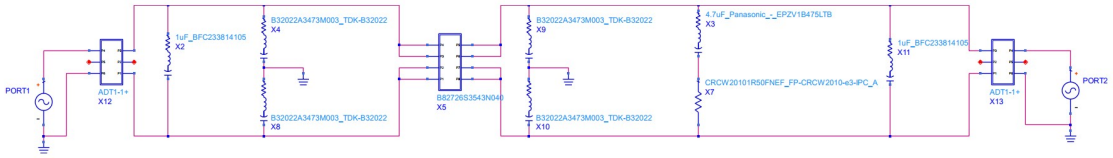


Figure 5.17. Schematic of the port setup EMI B DM

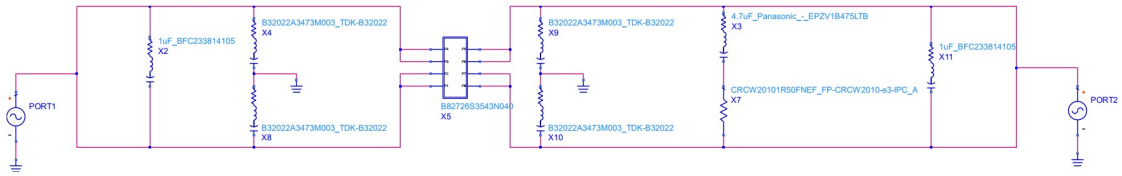


Figure 5.18. Schematic of the port setup EMI B CM

Type	Switching Freq	AC(Ripple) Freq	Rise Time	Fall Time
SMPS	15 kHz	Optional	50 ns	50 ns

Table 5.1. Frequency plan PEPro simulation

The SMPS frequency sweep automatically creates different sweep types in different frequency bands with a focus on the most important frequency points taking into account the switching frequency and the rise and fall times. The setup used provides the following frequency plans:

Sweep Type	Start Frequency	Stop Frequency	# points	Step
Linear	0 Hz	1 kHz	6	200 Hz
Linear	1 kHz	10 kHz	10	1 kHz
Logarithmic	10 kHz	15 kHz	2	5 points/dec
Linear	15 kHz	600 kHz	40	15 kHz
Logarithmic	600 kHz	100 MHz	46	20 points/dec

Table 5.2. Frequency plan points PEPro simulation

The settings used for this simulations are the ones in figure 5.19 that will be discussed in more detail in a following paragraph.

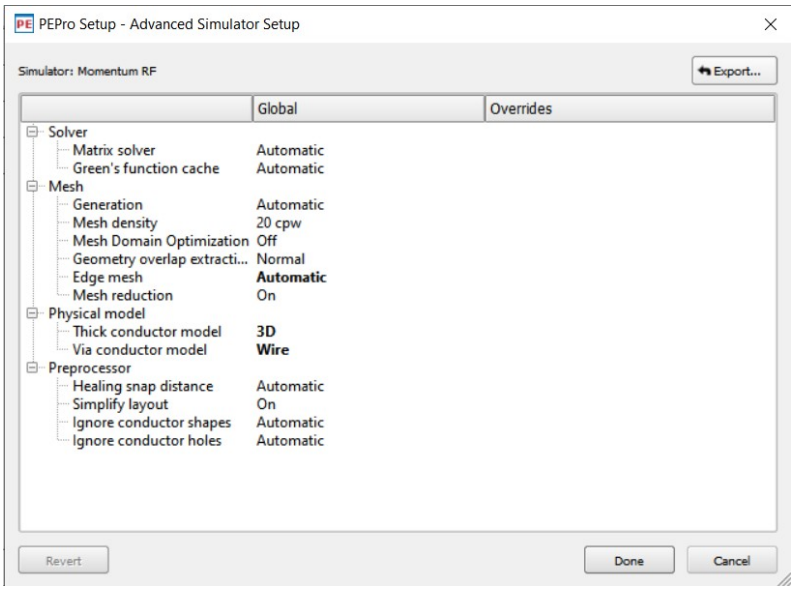


Figure 5.19. Advanced Simulator Setup settings used in this work

The far field data has been disabled since it is not needed thus reducing the dataset.

After running the simulation the results are exported using the "Generate Sub Circuit..." function creating a result like in figure 5.20.

This circuits can then be simulated using the ADS circuit simulator and the S_{21} can be simulated using the circuit in figure 5.21.

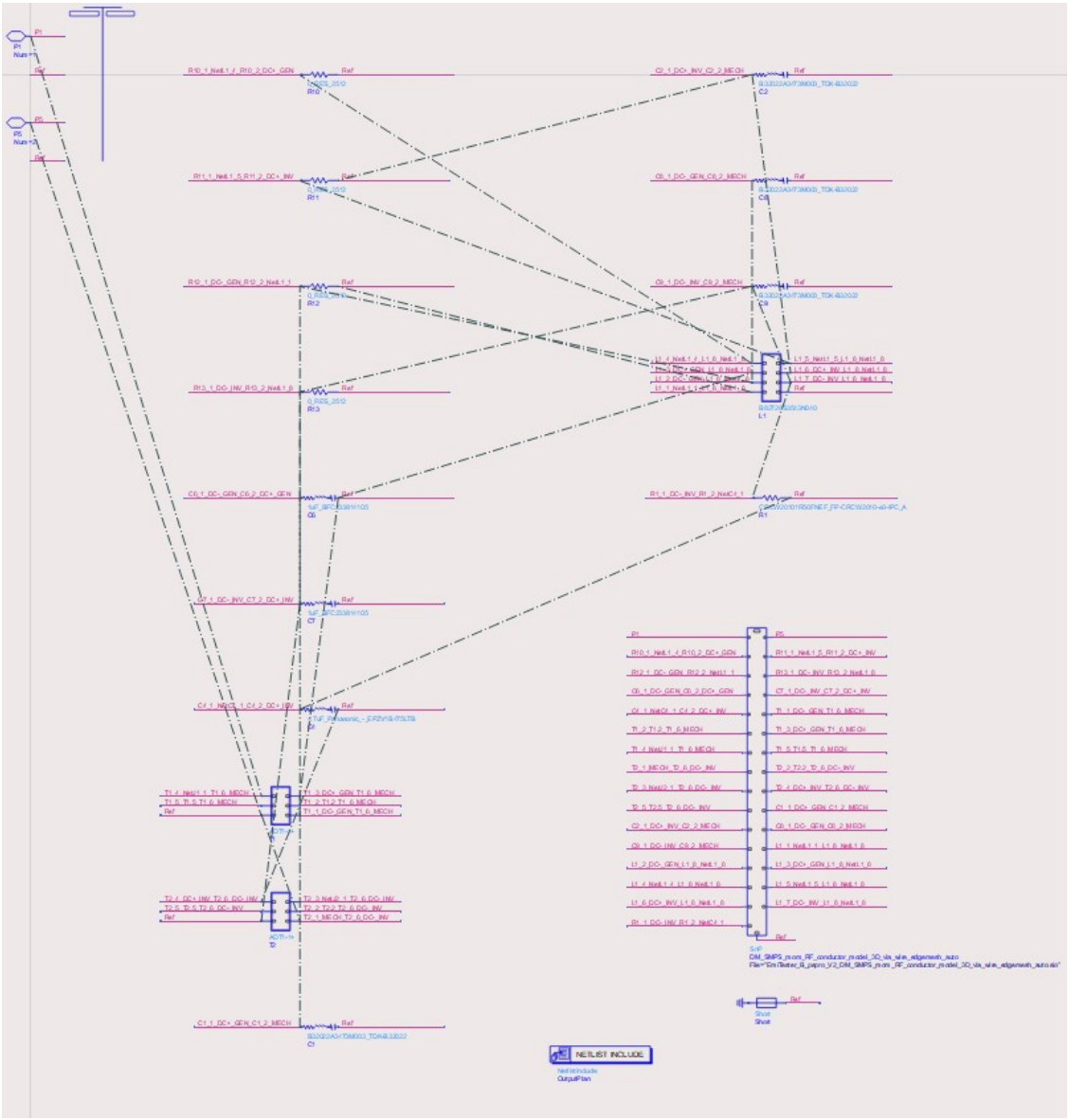


Figure 5.20. Example of Sub Circuit output from PEPro EMI B DM

The data is then saved in a touchstone .s2p file using the Data File Tool in the Data Display Window so that it can be further processed in Matlab. In the Data Display Window it is possible to process the data directly, for example in figure 5.22 it is shown the CM IL of the EMI B filter.

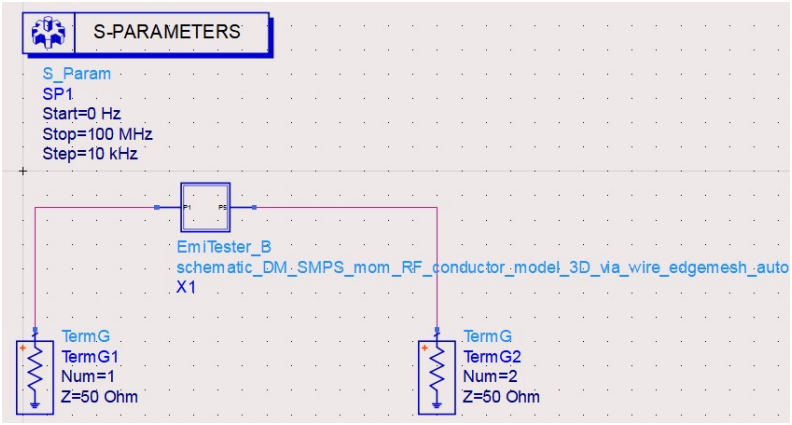


Figure 5.21. Example of simulation of S parameters from PEPro extracted Sub Circuit

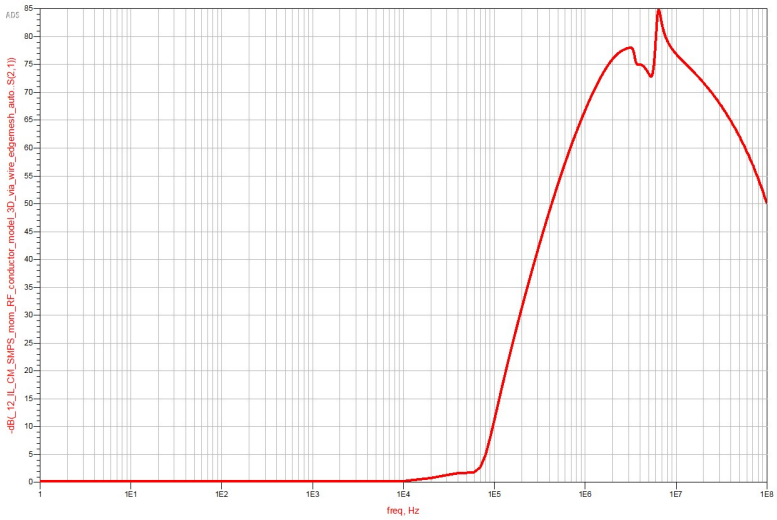


Figure 5.22. Example of CM IL result EMI B filter

EMI B

The simulations started from the EMI B filter because they run faster with respect to the EMI A since it has one stage less.

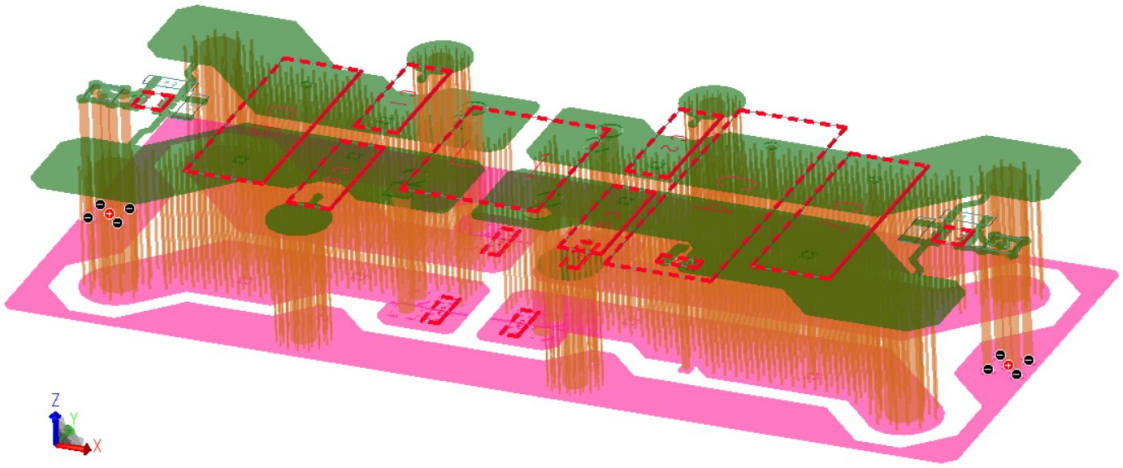


Figure 5.23. Port and components setup for DM IL EMI B

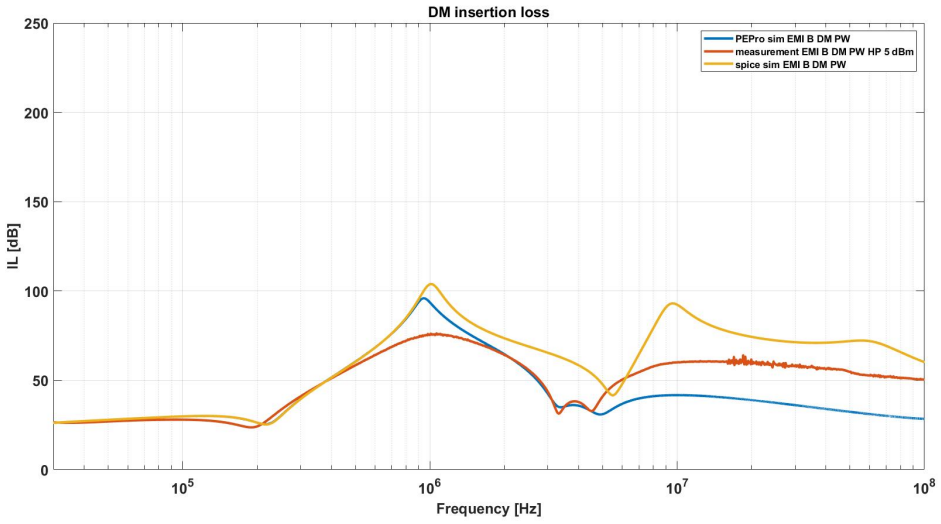


Figure 5.24. Simulation of differential mode IL EMI B filter comparison

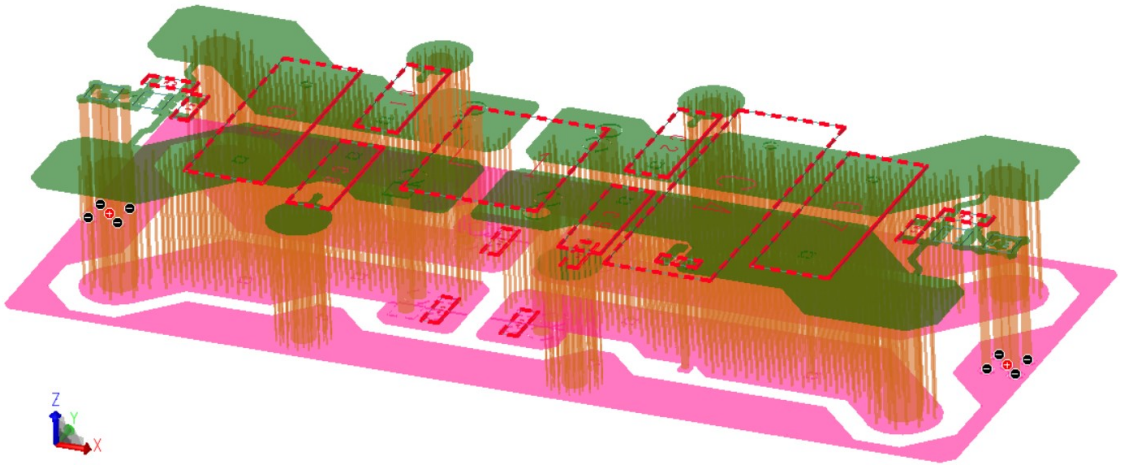


Figure 5.25. Port and component setup for CM IL EMI B

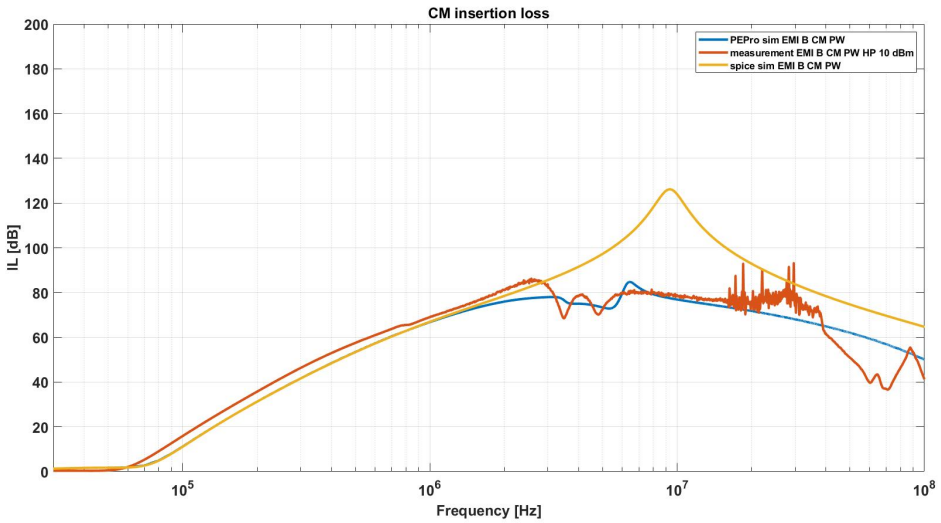


Figure 5.26. Simulation of common mode IL EMI B filter comparison

EMI A

The steps followed are the same as for the EMI B filter.

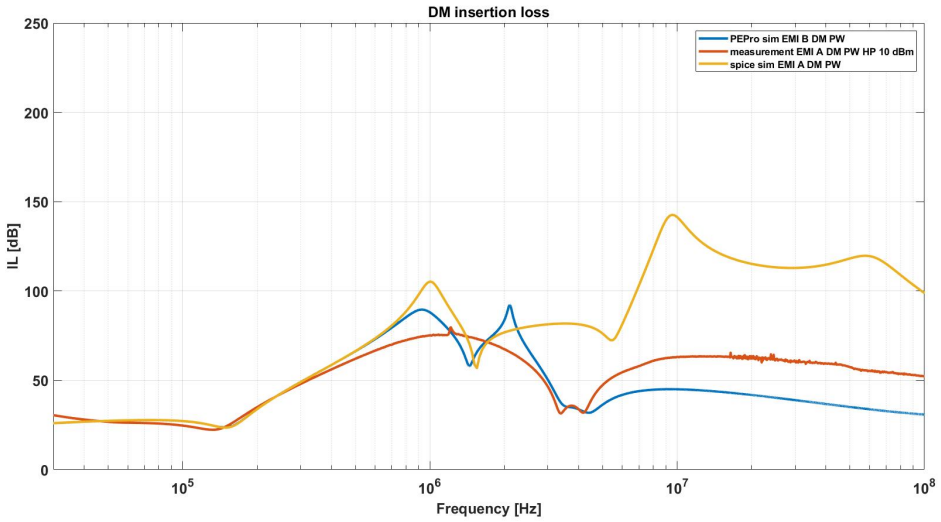


Figure 5.27. Simulation of differential mode IL EMI A filter comparison

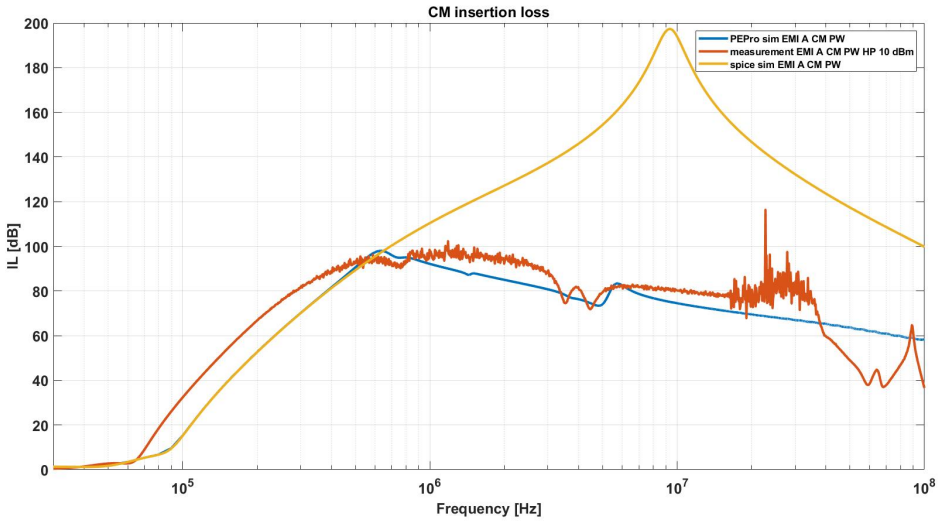


Figure 5.28. Simulation of common mode IL EMI A filter comparison

The results of these simulations are better than the ones before since the values are almost the same except from some resonances.

Results with proper hardware

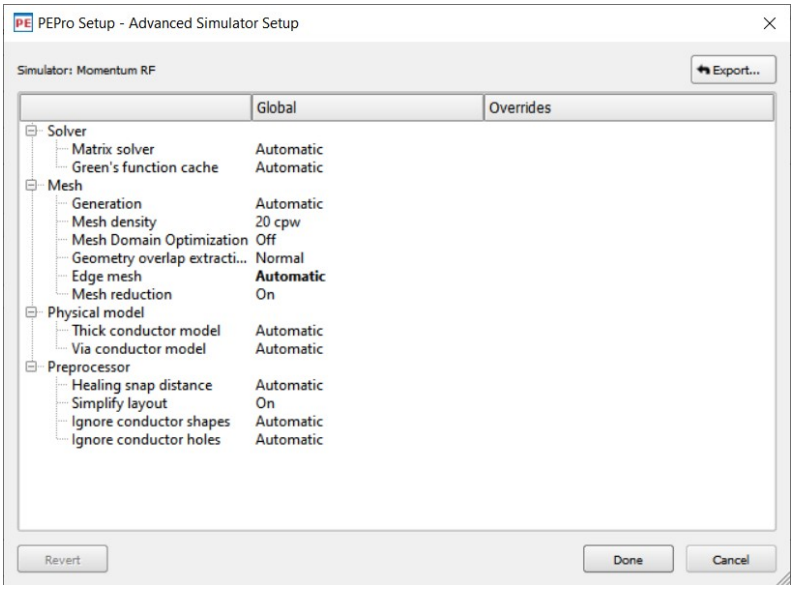


Figure 5.29. Advanced Simulator Setup settings suggested by the support

The hardware used for this simulations, a notebook with an Intel® Core™ i7-7700HQ processor with 8 threads, 16 GB of RAM and 1 TB mechanical hard disk, is not capable of running the software at its full potential due to the lack of RAM. Ideally the Advanced Simulator Setup should be set all to auto providing the results in figure 5.30 and figure 5.31. The peak obtained in the DM IL at roughly 1 MHz in the previous simulations is reduced and is comparable to the one measured in the lab. The CM IL simulation is not much different form the the previous one. Unfortunately this hardware, a server with 72 threads, is not available.

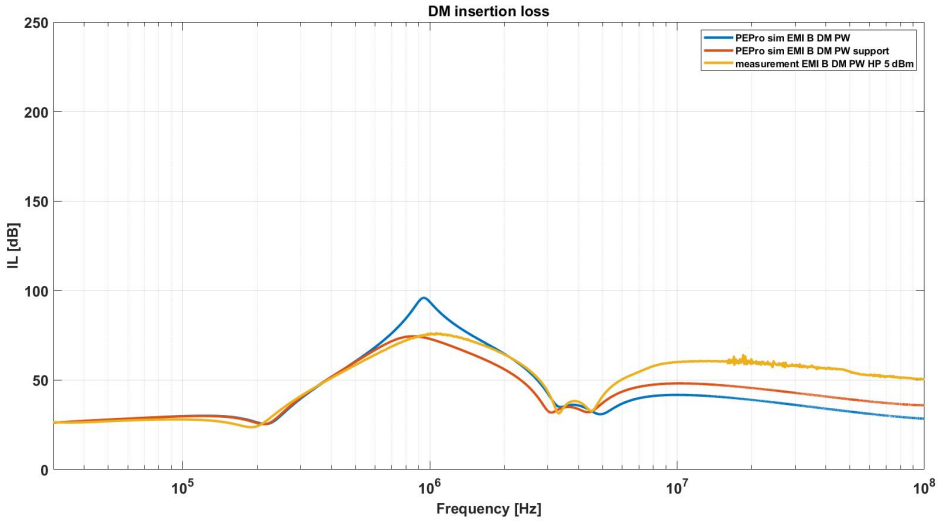


Figure 5.30. Comparison simulations and measurement

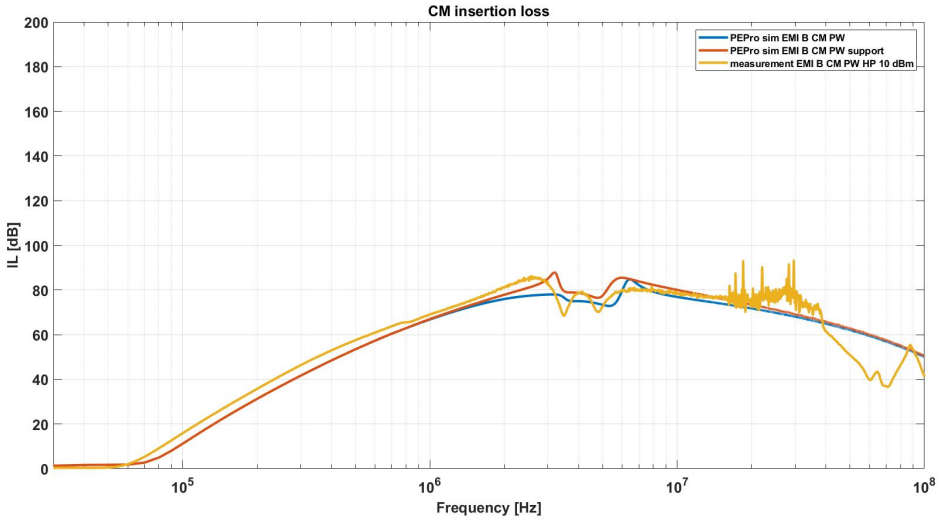


Figure 5.31. Comparison simulations and measurement

5.2.3 Ditcher inverter emissions

ADS allows the co-simulation between EM simulations in PEPro and circuital simulations. The PEPro tool has many predefined analyzes templates including the "Conducted EMI Analysis" which also contains a Data Dispay template for the CISPR-25 standard. This have been modified in this work to meet the requirements of the E-ECE-324-Add.9-Rev.6 and CISPR-17 normatives.

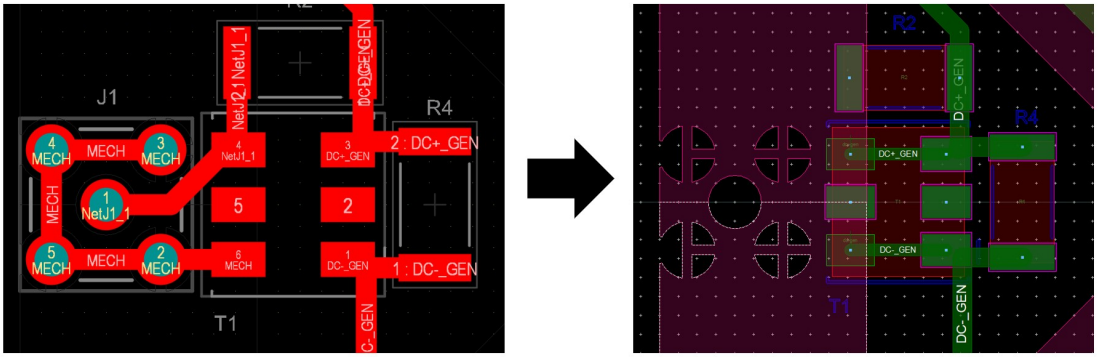


Figure 5.32. Layout modification for the 4 port setup

It is possible to include the result of the simulation from the PEPro tool in the ADS simulation environment. To do so it is needed to change the setup to create a four port analysis. On the battery side the SMA connectors and baluns are deleted and pin 1 and 6, pin 3 and 4 of the balun footprint are respectively connected together to provide the "+" of port 1 and 2 as shown in figure 5.32. Then virtual pins are created on the bottom layer defining the "-" of the two ports. The 0 Ω resistors R2 and R4 are de-soldered. This configuration is the repeated for the inverter side of the filters to define port 3 and 4. A screenshot of the setup for port 1 and 2 is shown in figure 5.34.

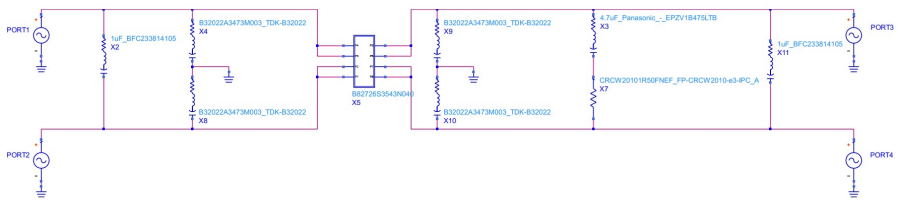


Figure 5.33. Schematic for the 4 port connection EMI B filter

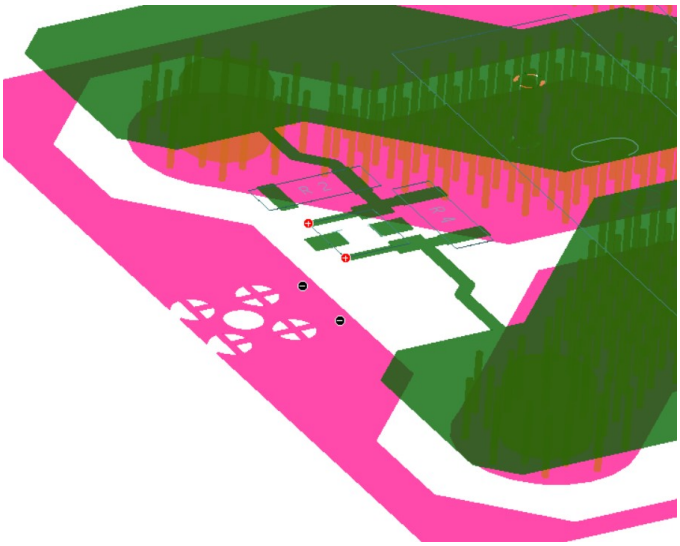


Figure 5.34. Example of four port setup in PEPro EMI B filter

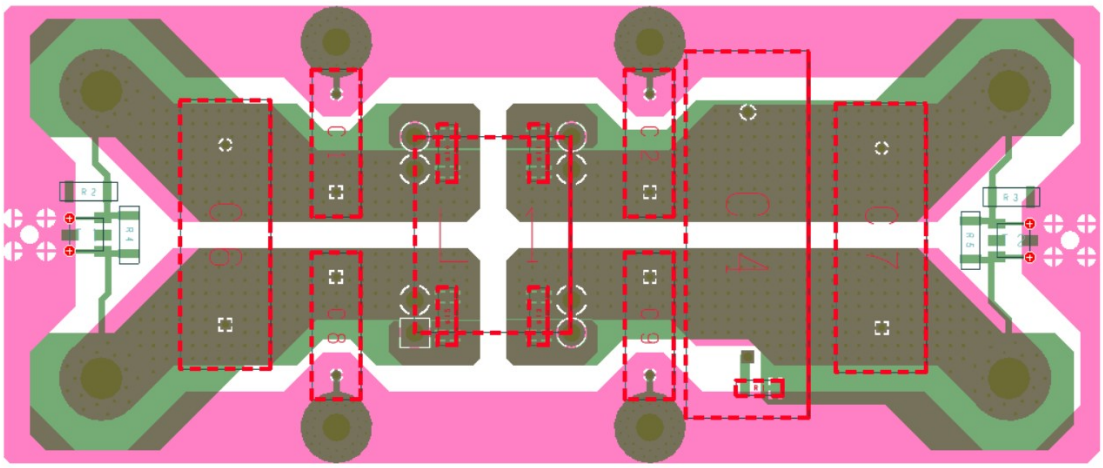


Figure 5.35. Top view of the port and components in PEPro EMI B filter

Setup

The controller used for the simulation is the Transient PE controller, which simplified the settings for the user with respect to the standard Transient simulation controller, and is dedicated to power electronics simulations. The timestep is variable and is computed by the controller from the rise time and fall time:

$$\text{Maximum Time Step} \;=\; 100 \cdot \text{minimum(Rise time,\ Fall time)} \;=\; 5\ \mu\text{s} \tag{5.3}$$

The maximum frequency is defined as:

$$\text{Maximum Frequency} = \frac{5}{\text{minimum(Rise time,\ Fall time)}} = 100\ \text{MHz} \tag{5.4}$$

Output window	
Start time	0 ms
Stop time	60 ms
Switched loop rise/fall times	
Rise time	50 ns
Fall time	50 ns

Table 5.3. TransientPE settings

Simulation options tolerances used:

Simulation Options: Tolerances	
Voltage relative tolerance	1 mV
Current relative tolerance	1 mA
Voltage absolute tolerance	1 mV
Current absolute tolerance	10 μA

Table 5.4. ADS simulation tolerances

Capacitors are precharged to 700 V and the option "UseInitCond" is checked to reach the regime condition faster.

MOS capacitances

	Datasheet	Simulation
C_{gs}	14.588 nF	14.588 nF
C_{gd}	112 pF	112 pF
C_{ds}	768 pF	100 pF

Table 5.5. Mosfet capacitances used

The parasitic capacitances used for the mosfets are listed in table 5.5 and are different from the ones in the datasheet since setting the C_{ds} to an higher value crashes the simulator.

All the other parameters are kept the same as the simulation of the previous work.

Time-to-frequency conversion

Following the template provided with the "Conducted EMI Test Bench" designed for the CISPR 25 standard the time-to-frequency conversion is performed. The equations parameters are changed to comply with the CISPR 16-2-1 regulation. It has been decided to convert into frequency a integer number of periods of the output waveform when the inverter reaches the regime condition, choosing 30 ms to 60 ms as they achieve a good balance between simulation time and result. This differs from the previous Simulink simulations since they were using the built in spectrum analyzer.

Simulation tolerances

Changing the simulation options tolerances can dramatically increase or decrease the time duration of the simulation. Unfortunately the tolerances have a big impact on the spectrum, for example in figure 5.36 the red curve with more strict tolerances is under the normative limit at higher frequencies.

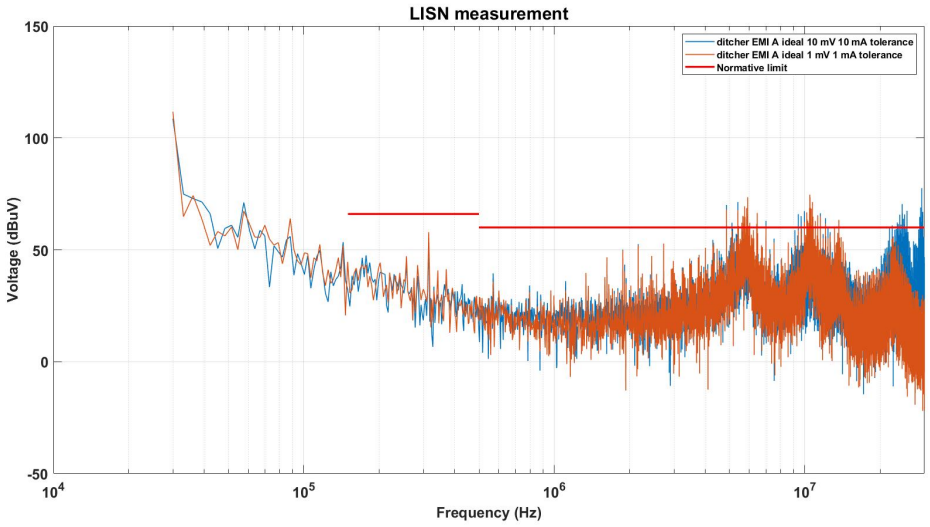


Figure 5.36. Effect of the change of tolerances on the spectrum

Simulation duration for 1 mV 1 mA tolerances: about 37 minutes
Simulation duration for 10 mV 10 mA tolerances: about 9 minutes

It is not possible to run all the simulations needed with tighter tolerances since the simulation duration increases too much.

Modulation effect

It was not possible to use the Space Vector PWM modulation used in the previous work in ADS. This might lead to different result regarding the emissions measured at the LISN.

Cable length effect

Increasing the length of the DC cables increases the total emissions, as shown in the example in figure 5.37 where using the EMI A ideal filter the emissions are compared between the DC cables with a 1 m and 2 m length. This effect

was expected but not with this much increase, so probably the simulation is not accurate enough.

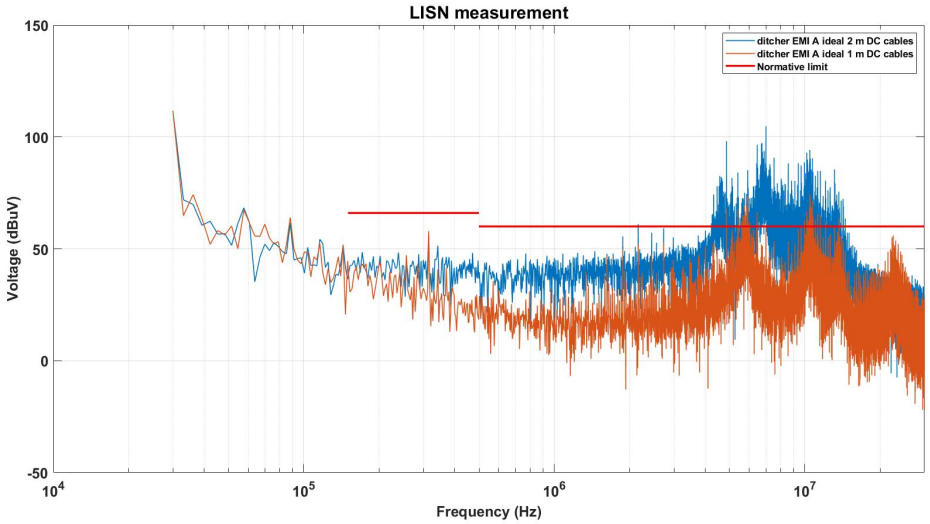


Figure 5.37. Effect of the DC cable length on the emission spectrum

EMI B

The results of the simulations with the single stage filter show that an higher insertion loss is needed both at low and at high frequency.

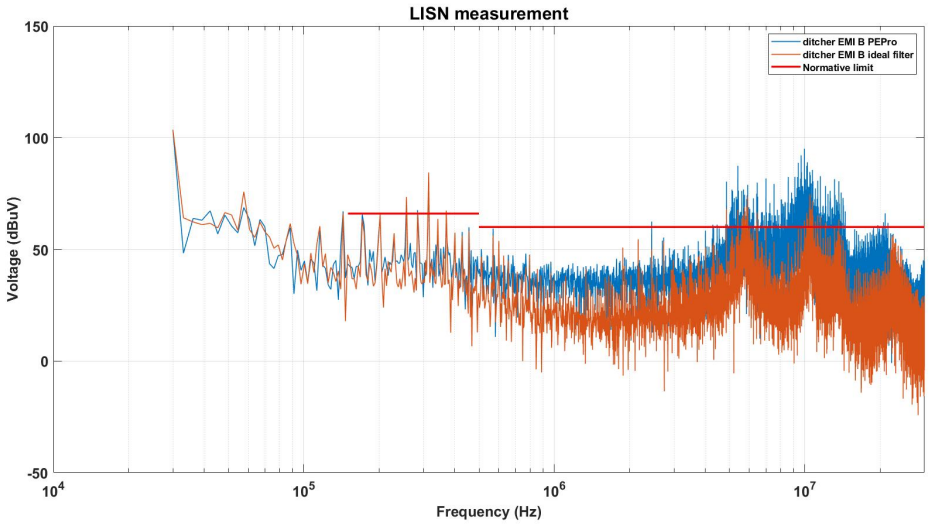


Figure 5.38. LISN measurement simulation with EMI B filter

EMI A

The emissions in the frequency range 150 kHz - 500 kHz are lower that the normative limit with the double stage filter, but there are still resonances at higher frequencies that exceed the limits.

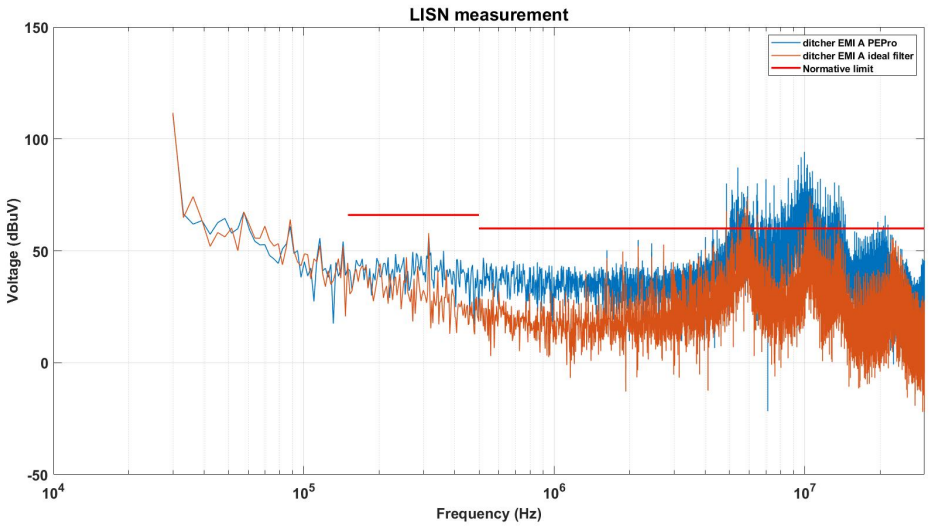


Figure 5.39. LISN measurement simulation with EMI A filter

Comparison with previous results

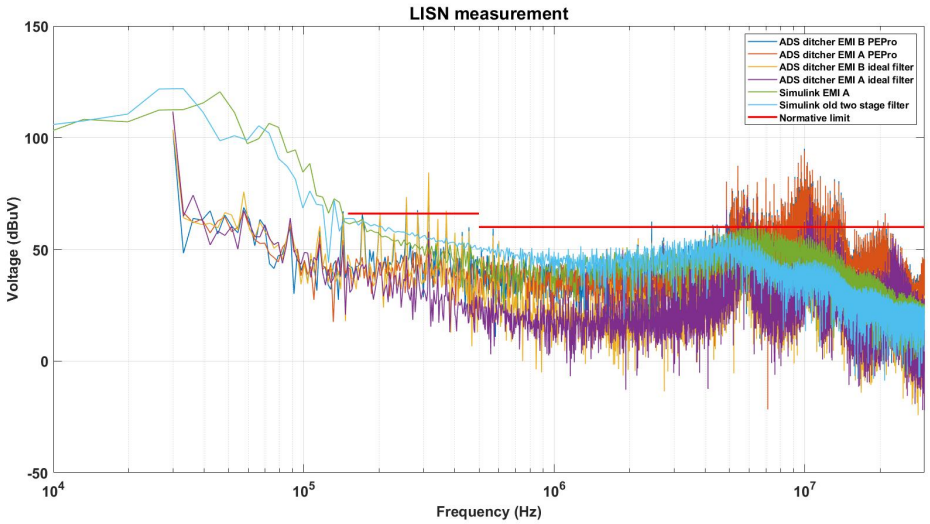


Figure 5.40. Comparison of the emissions

In figure 5.40 the new double stage filter simulated with Simulink (green curve) satisfies the normative limits, whereas the same ideal filter simulated in ADS (purple curve) exceeds them due to some resonances; the emissions with the filter simulated in PEPro (in orange) are worse. The new simulations differ from the previous ones due to the resonances and this effect has not been understood.

Chapter 6

Conclusion

This project started from the review of the preliminary filter design that was made in a previous work. Then, the filter fabricated with the specification derived from that previous work has been characterized in this thesis in terms of its insertion loss. The insertion loss of the filters has then been measured in the lab providing, during these measurements, some unexpected results. To understand the resonances identified, simulations were carried out to explain the filter behavior that was discovered. Then simulations were conducted to better understand the behavior of the designed filter and also estimate the generated conducted emissions. First of all the EM field simulations of the filters allowed to achieve the IL measurement results in the simulations. This certified the followed procedure, although the results are not perfect, and allowed to use the obtained sub-circuit, now simulated with 4 ports, with the circuital simulator available in ADS to simulate the ditcher system and its conducted emissions. The results achieved exceed the normative limits after 5 MHz and their trend is characterized by resonances that were not present in the Simulink model. This results need to be confirmed by the measurements in the lab that are planned in the coming weeks. The correct placement of the filter in the inverter case is still to be investigated as any parasitic effect that would arise could affect the effectiveness of the filter.

Future simulations
A future work might complete the simulations by focusing on the tedder inverter which was not thoroughly studied due to time constrains caused by the length of the simulations due to the lack of powerful computing hardware.

Planned laboratory measurements

Laboratory measurements are planned to evaluate the work done using the ditcher inverter that will drive a stator instead of the motor employed till now since it is not available. The specifications of the stator are: 157 μH phase inductance and 8 mΩ phase resistance. The simulations were conducted with the setting described in the previous chapter with the two filters in their ideal versions and in the one that takes in account the parasitic effects of the PCB.

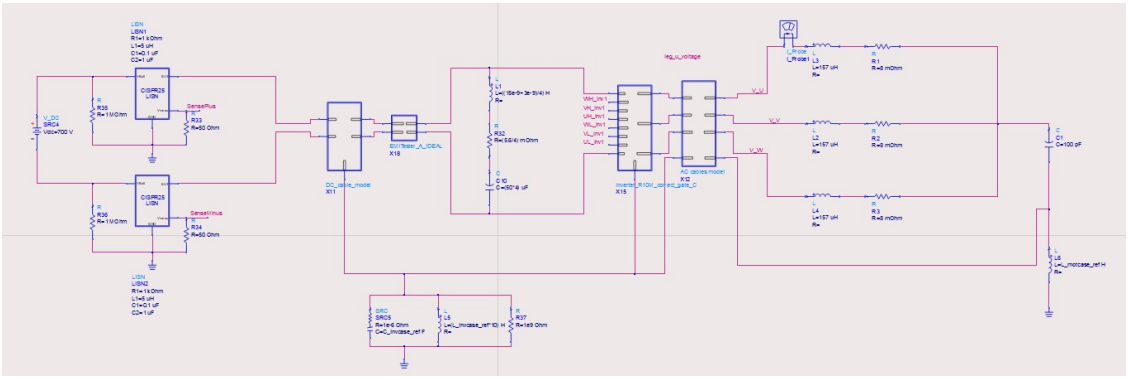


Figure 6.1. Model of the ditcher system connected to the stator and using the ideal EMI A filter

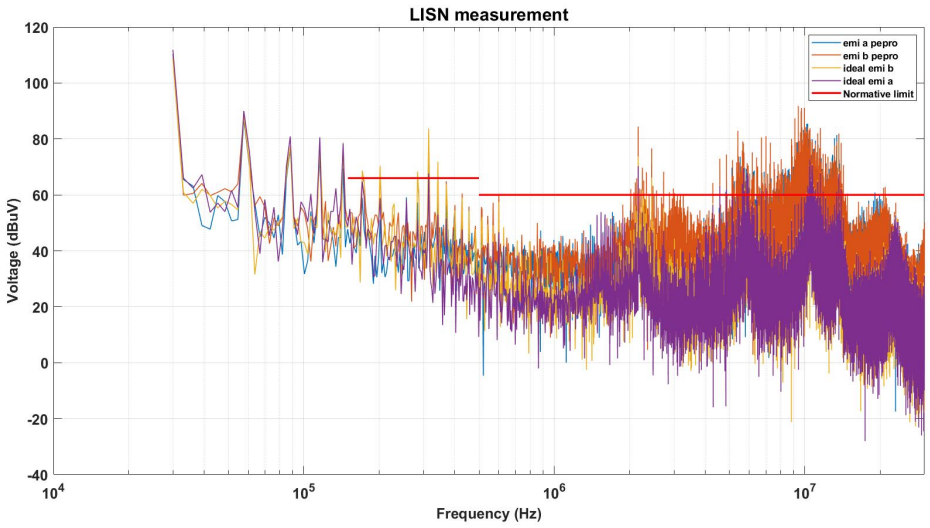


Figure 6.2. Comparison with the simulations made with the stator

Appendix A

Ditcher system

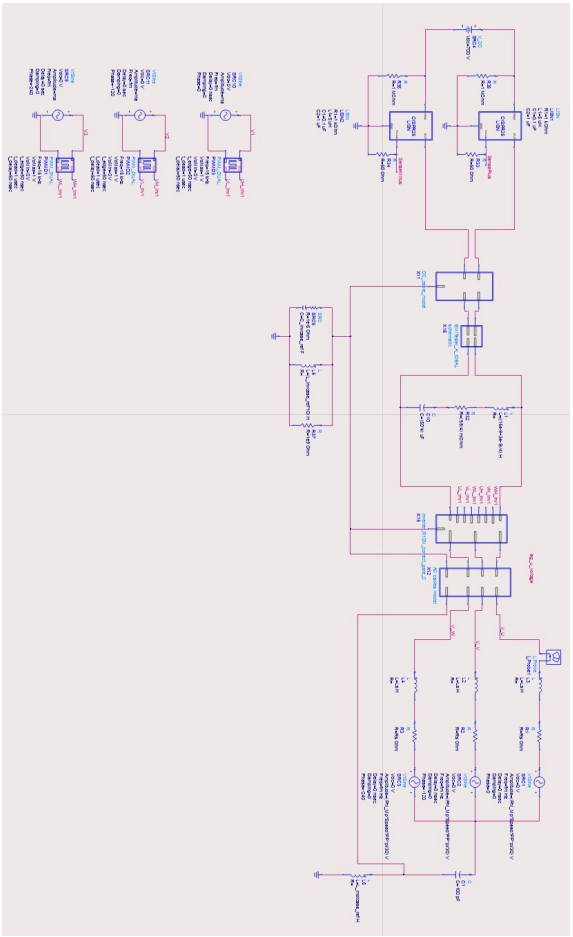


Figure A.1. Model of the ditcher system in ADS

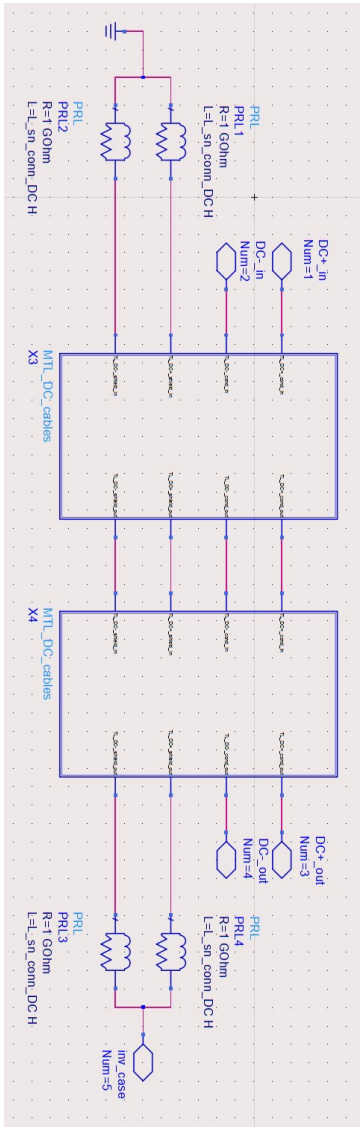


Figure A.2. Model of the DC cables

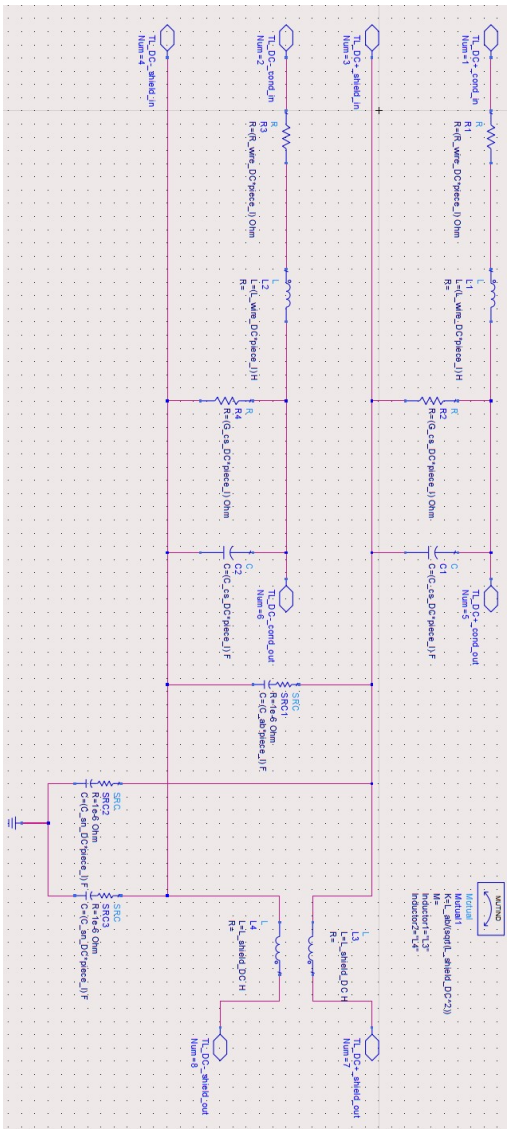


Figure A.3. Push into DC cable segment

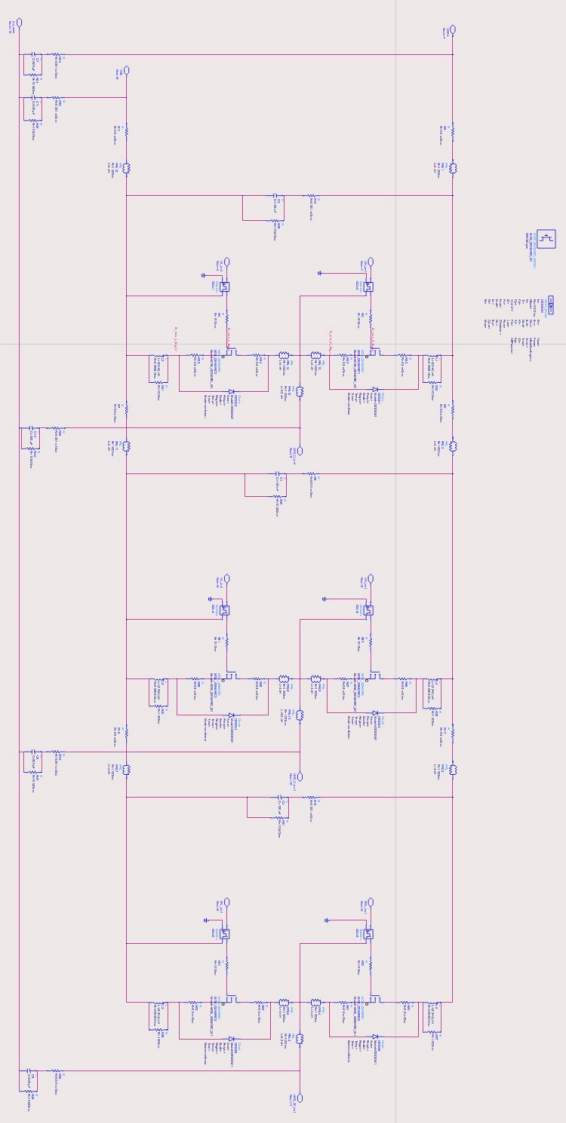


Figure A.4. Ditcher inverter

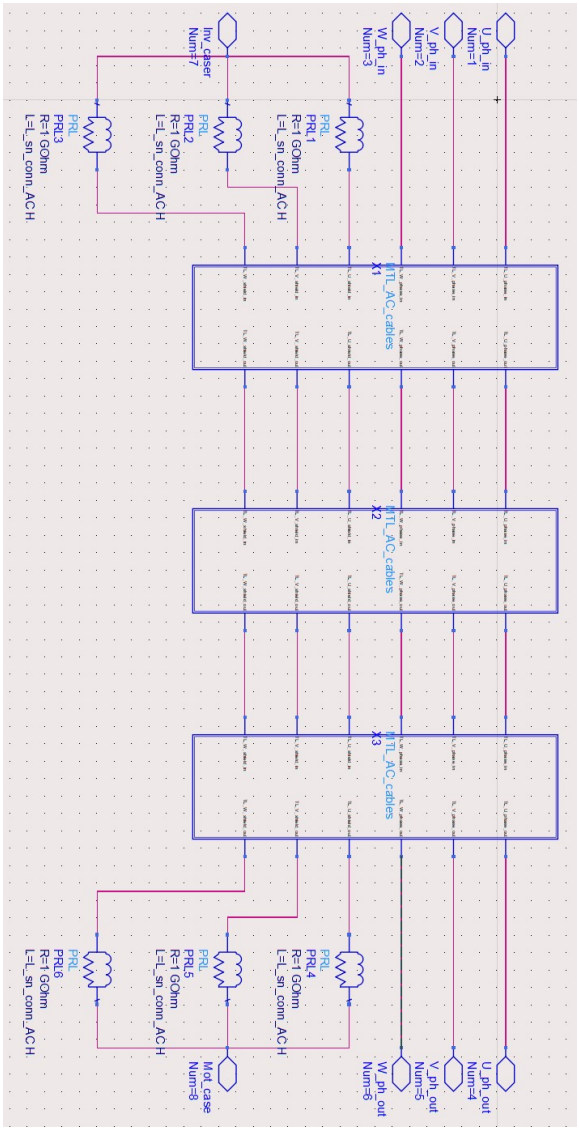


Figure A.5. Model of the AC cables

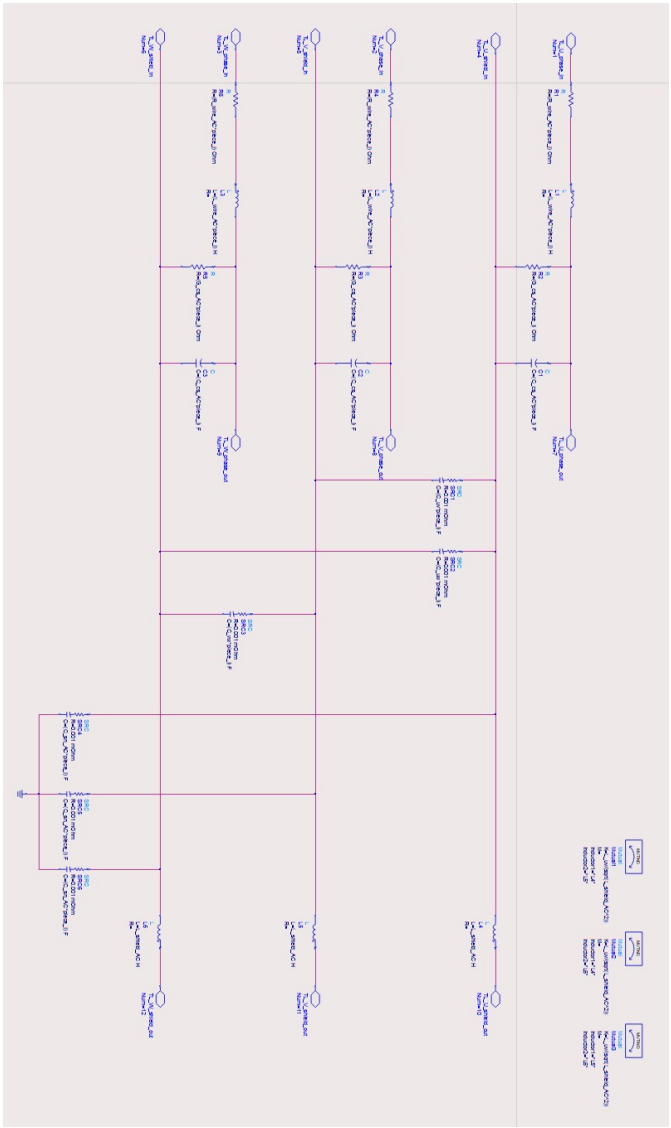


Figure A.6. Push into AC cable segment

Appendix B

Emissions code

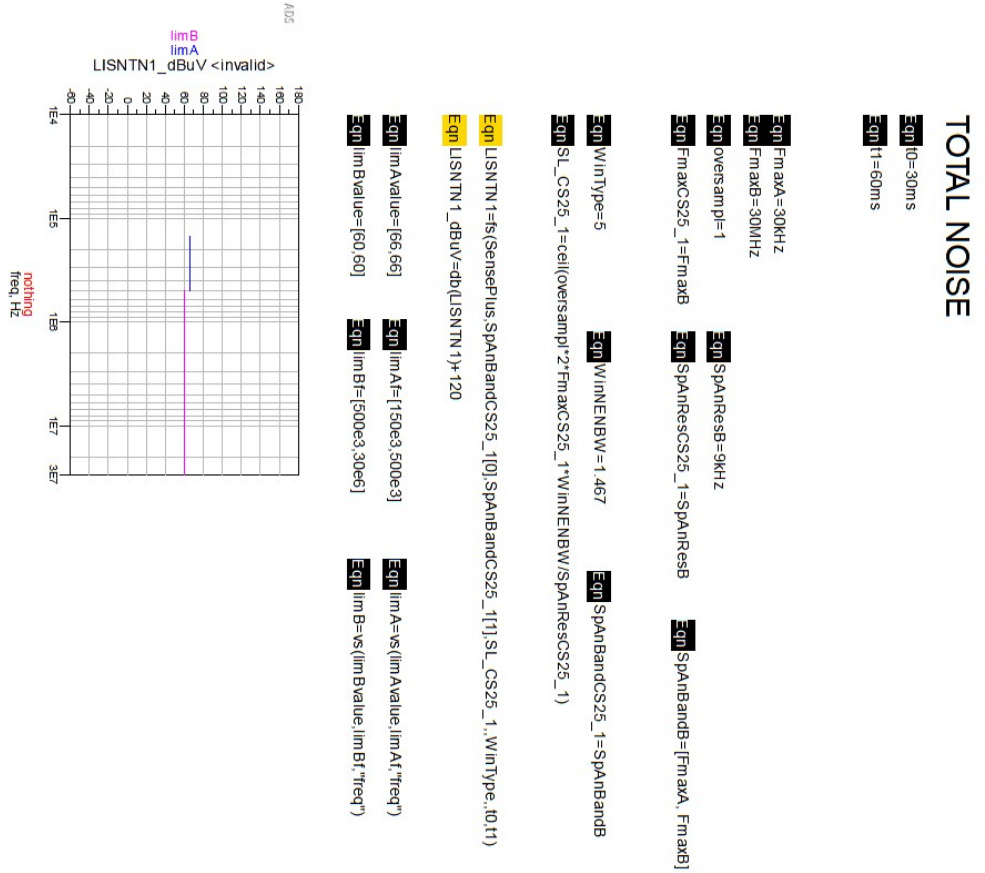


Figure B.1. Total emissions

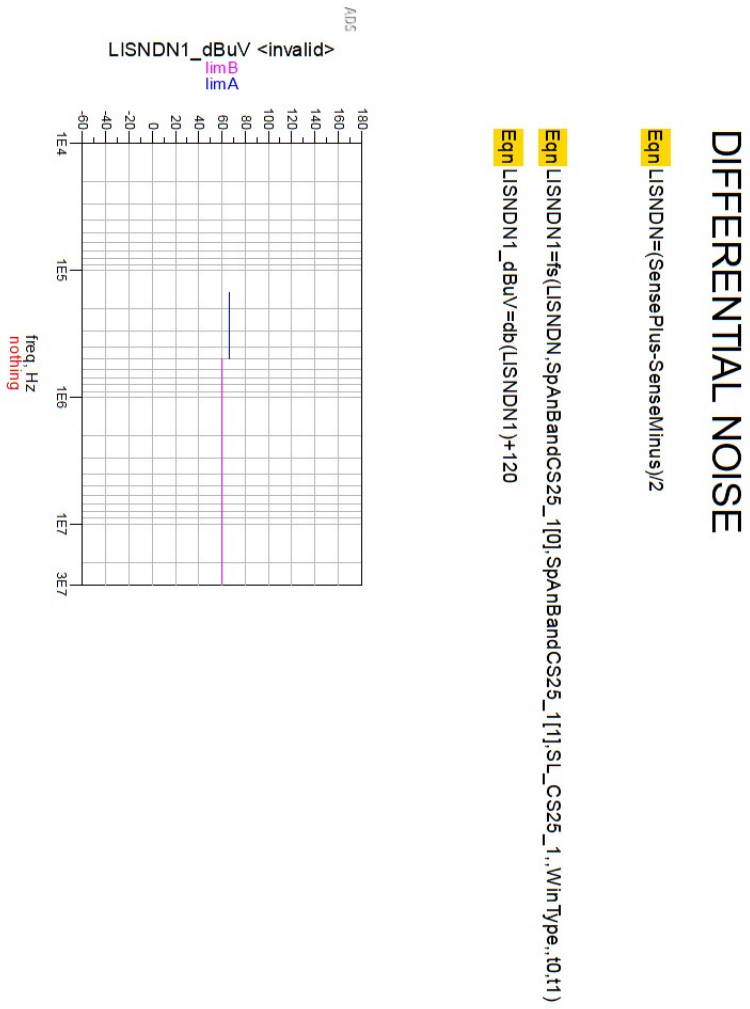


Figure B.2. DM emissions

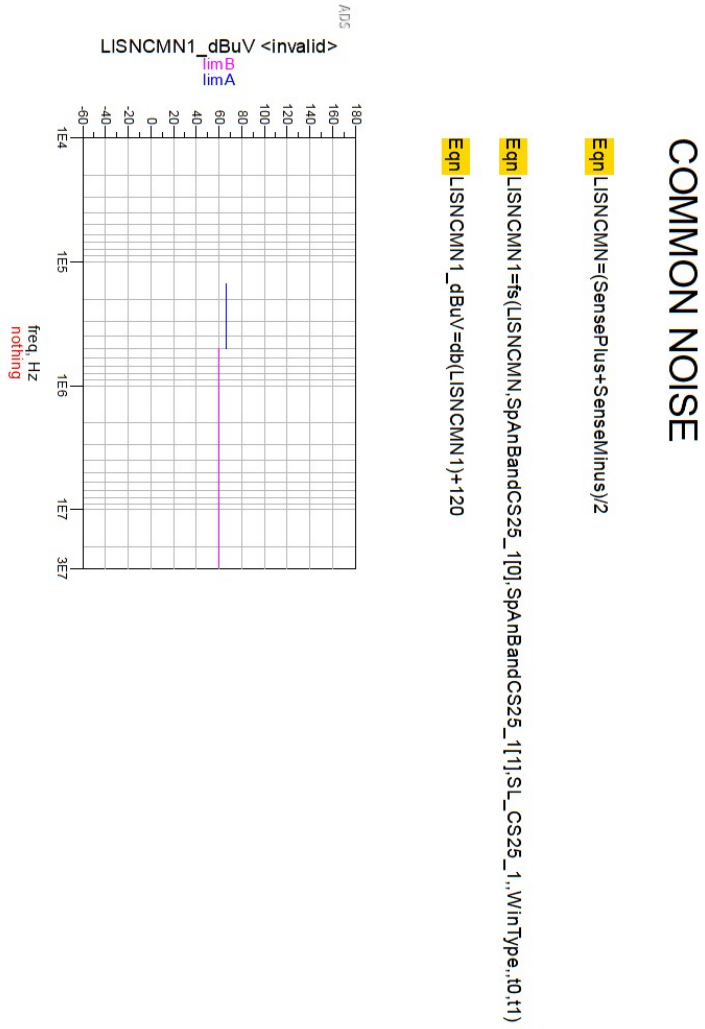


Figure B.3. CM emissions

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