POLITECNICO DI TORINO

MASTER'S DEGREE THESIS

Development of linear and highly efficient GaN power amplifiers for 5G applications

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Summary

In the last decade, mobile communication traffic has been rapidly increasing because of the growing popularity of smart devices. The 5th generation communication standard (5G) aims to cope with the explosive and ever increasing capacity demand. On one side, the mm-wave frequency bands (FR2) are being explored, since operating at higher frequencies allows wider channel bandwidths. However, a very strong interest is currently maintained both by the industrial and academic communities on the lower frequency bands (FR1). These are currently more crowded, but pose fewer challenges for the development of the complete infrastructure, and are therefore being further exploited. Power amplifiers operating in the FR1 5G bands are required to operate with high efficiency and linearity over wide bandwidths, in order to minimize power consumption, increase data rates, and minimize interference.

This thesis focuses on the design, fabrication, and experimental characterization of a single-stage class AB power amplifier operating in the 5G FR1 frequency range of around 3.5 GHz. The amplifier design strategy is based on the optimum trade-off between efficiency and linearity, and it has been developed in the framework of the "High Efficiency Power Amplifier" student design competition of the major conference of the field, the International Microwave Symposium. The designed amplifier should satisfy two main requirements, namely achieve output power in the range 4–40 W for a single-carrier drive with input power not higher than 24 dBm, and maintain the highest inter-modulation product below -30 dBc in a two-tone linearity measurement with 20 MHz tone spacing. At the same time, the designer is required to boost power-added efficiency as much as possible.

The realized prototype has qualified as a finalist in the 2022 competition that was held in Denver in June. Although outperformed by other designs, some of which were presented by more experienced designers on non-commercial advanced technologies, this amplifier has demonstrated to provide the required output power and gain, while achieving a power-added efficiency of 73% at maximum power and of 33% at the minimum required linearity. These results have been summarized in a scientific paper, which has been accepted for publication at the upcoming 2023 Radio and Wireless Week conference. However, further work is planned for a future post-graduation research activity, such as the attempt of applying different topologies or the investigation of more effective design strategies, aiming to improve the performance of the power amplifier and compete again in the student design competition that is going to be held in 2023.

Contents

List of Tables

List of Figures

1 Introduction

1.1 Overview

In the last decade, mobile communication traffics have been rapidly increasing because of the spread of smartphones and tablet devices. The demand for data continues to grow as the number of devices connected to the internet grows. Therefore, the high data rate 5^{th} generation mobile communication system (5G) is introduced to cope with the explosive capacity demand for the networks [4, 17, 18]. The 5G communication system is enabled by mm-Wave technology, which operates at higher frequencies allowing wider channel bandwidths. However, a very strong interest is currently maintained both by the industrial and academic communities on the lower frequency bands (FR1) [4]. These are currently more crowded, but pose fewer challenges for the development of the complete infrastructure, and are therefore being further exploited. Power amplifiers (PAs) operating in the frequency range1 (FR1) 5G bands are required to operate with high efficiency and linearity over wide bandwidths, in order to minimize power consumption, increase data rates, and minimize interference [14, 16].

1.2 Thesis Target

In this thesis, a PA targeting 5G FR1 operation is designed, manufactured, and characterized, with the further aim of participating in the High-efficiency power amplifier (HEPA) student design competition (SDC). The HEPA SDC primarily focuses on PAs having both high efficiency and linearity over a relatively narrow bandwidth, and with a design frequency that can be selected within a broad range. The specifications proposed by this competition are described below. The PA should:

1. Operate at a frequency between 1 GHz and 10 GHz.
2. Achieve an output power (P_{out,f_0}) in the range 4–40 W for a single-carrier drive at frequency f_0 with input power (P_{in,f_0}) not higher than 24 dBm.
3. Maintain the highest inter-modulation product below -30 dBc in a two-tone measurement with 20 MHz tone spacing and maximum input power ($P_{in,2t}$) of 21 dBm per tone, while achieving a PAE as high as possible.

The challenging specification restrictions in such a framework called for a design that compromises efficiency and linearity while keeping sufficient output power.

The competition has followed the same rules and had similar design constraints during the past years. A review of the former competition winners, which are invited

to publish their work in the Microwave Magazine, has allowed identifying some strategies and trends. The main difference is the tone spacing in the two-tone linearity test. This has been increased in accordance with the increasing instantaneous bandwidths of the signals adopted by modern communication standards. The winning entries from the past competitions adopt the Doherty power amplifier (DPA) architectures [11, 13], which takes the beneficial effect of the auxiliary amplifier in compensating the distortion. However, improving on the previous performance, which is well exploited and optimized in previous winning cases, is thus not an easy task. Other than this, a Class-AB PA extending the linearity through exploiting "sweet spots" won HEPA 2016 [6]. Compared to a linear DPA solution, this type of single-stage design is simpler to implement, and with less extensive biasing and matching circuitry. Inspired by this, the Class-AB is considered the design option for this work.

1.3 Thesis Work

In the thesis work, a single-ended deep Class-AB PA operated at a 3.5 GHz center frequency with a 500MHz bandwidth compatible with the 5G FR1 n78 band is designed and fabricated. The PA is intended to fulfill the above-mentioned requirements.

At the initial design phase, the design strategy focuses on determining the optimum source and load terminations, at base-band, fundamental, and harmonic frequencies through simulations in the Keysight Advanced Design System (ADS) CAD simulation software. As a second step, matching networks are designed in micro-strip technology to present to the active device the desired terminations. Finally, electromagnetic simulations are set up to evaluate the practical performance.

The prototype of PA is realized in a hybrid circuit i.e., by assembling the packaged active device and the Printed Circuit Board (PCB) containing the matching networks on a metal carrier, to provide both heat dissipation and mechanical stability. In a later measurement work, a real-time vector test bench is adopted to experimentally characterize the manufactured PA demonstrator.

2 PA theory

2.1 PA in Wireless Communication system

In any wireless communication system, the transmitter is a necessary component to enable the communication of information over a distance. The electrical signal carrying the information is modulated and amplified to a certain power level by the transmitter. Lately, an antenna transfers the signal into electromagnetic waveform towards the nearby designated receiver [15].

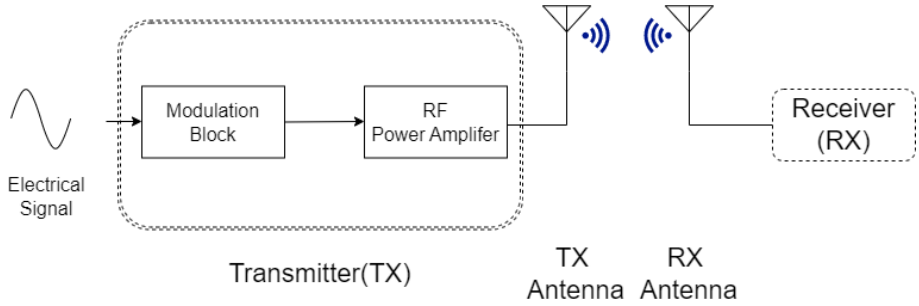

Figure 2.1: Transmitter and Receiver in Communication System.

The radio frequency (RF) PAs are constructed in the transmitter to magnify the signal. The PA outputs signal with a sufficient power level ensures the signals emitted by the antenna could be identified and received by the receiver after propagation. However, as the last block in the transmitter, the PA has a critical impact on the power consumption of the system [3]. The system expects the PA to have high converting efficiency. Additionally, as the communication system advances, the other performance criteria (such as linearity) become more demanding [12].

2.2 PA Figures of Merit

The RF PA is an active device-based power system that converts DC power and low-level RF signals into a relatively higher level RF signal delivering to a load (Fig. 2.11). Both the input and output signals operate at the fundamental frequency f_0.

The behavior of PA is described by Figures of Merit (FoMs), some of the most important from a design standpoint is the major behavior, such as gain, and efficiency, which refers to the continuous wave (CW) single-tone simulation. Other significant FoMs such as linearity can be evaluated by the two-tone or modulated signal test.

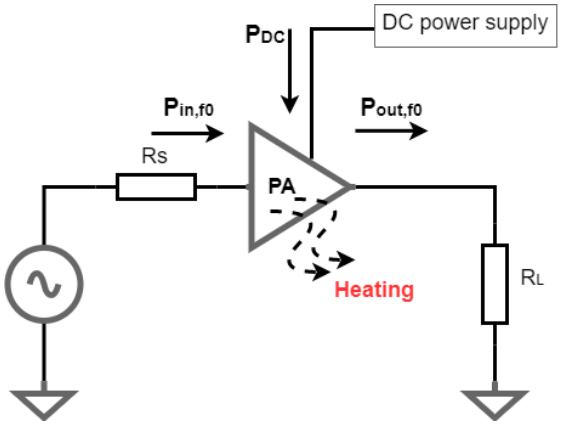

Figure 2.2: Conceptual scheme of an RF PA highlighting the power flows.

Continuous Wave (CW) Single-tone test

The PA is a system composed of input/output matching networks and the active device. In the single-tone test, the input signal is provided by an AC source with a constant power level $P_{in,av}$. The signal flows through an input matching network, entering the active device as a signal operating at f_0 with power P_{in}. The available power $P_{out,av}$ output by the active device is amplified at the fundamental frequency f_0 and partially distributed to harmonics nf_0. The power P_{out} is delivered to the load after the output matching network. The gain and efficiency are described to evaluate the performance in view of power transfer. In addition, the $P_{in} - P_{out}$ characteristic graph is used to quantify the P_{out} distributed on both fundamental and harmonics to assess the power behavior related to frequency [8].

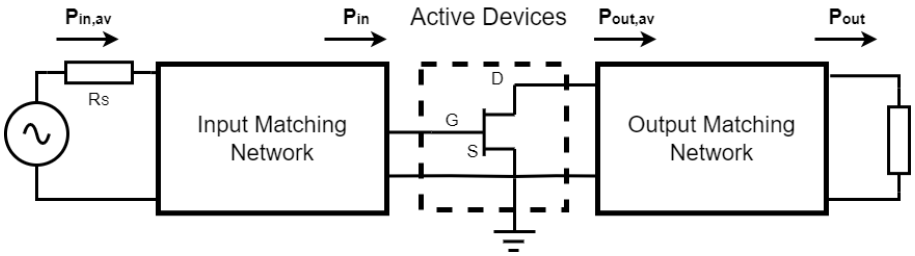

Figure 2.3: Block diagram of a generic single-transistor amplifier.

A. Operational gain G_{op} and Transducer gain G_{tr}

In general, the power gain is the ratio between output and input power at the fundamental frequency. It is however possible to define different gains, according to the powers that are considered and as a consequence, the possible mismatch of the different parts of the entire system. They are operational gain G_{op} and transducer gain G_{tr}

respectively. Transducer gain G_{tr} is defined as,

$$G_{tr} = \frac{P_{out}(f_0)}{P_{in,av}(f_0)}$$

where the $P_{in,av}$ is the input available power, and the P_{out} is the output power on the load.
Operational gain G_{op} is defined as,

$$G_{op} = \frac{P_{out}(f_0)}{P_{in}(f_0)}.$$

where P_{in} is the power entering the input port of the active device (i.e., transistor).

As the block diagram illustrated in (Fig. 2.3), G_{tr} depends both on the input and output matching, while G_{op} only depends on the output matching.

Maximum Power Transfer

The maximum power transfer in the PA occurs when two conditions are both satisfied, a) the input power P_{in} equals the available power $P_{in,av}$ generated by RF source; b) the power on the load P_{out} is the load (output) available power $P_{out,av}$ [8]. Hence, the input/output reflection coefficient presented to the transistor should be determined for conjugate matching. The equation for describing conjugate match provided in [2], is shown in the following.

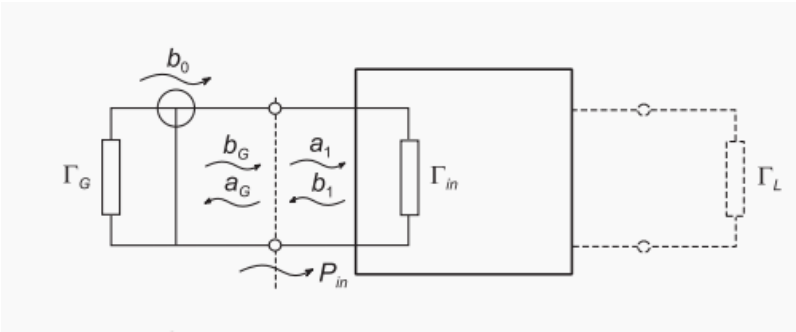

Figure 2.4: Two-port network analysis [8].

Input match:

$$\Gamma_{in} = S_{11} + \frac{S_{21} S_{12} \Gamma_L}{1 - S_{22} \Gamma_L}$$

Output match:

$$\Gamma_{out} = S_{22} + \frac{S_{21} S_{12} \Gamma_G}{1 - S_{11} \Gamma_G}$$

so for a conjugate match, one can set as below.

$$\Gamma_{out} = \Gamma_L^*; \Gamma_{in} = \Gamma_G^*$$

B. Efficiency η and PAE

The efficiency is the ratio between the output power at fundamental $P_{out}(f_0)$ and the DC power required from the DC power supply P_{DC} (see Fig. 2.11):

$$\eta = \frac{P_{out}(f_0)}{P_{DC}}.$$

Another important FOM related to the efficiency of the PA is the power-added-efficiency (PAE), describing the effective RF power converts from the DC source, the effective RF power here refers to the difference between $P_{in,f0}$ and $P_{out,f0}$, the equation is presented following:

$$PAE = \frac{P_{out}(f_0) - P_{in}(f_0)}{P_{DC}} = \eta(1 - \frac{1}{G_{op}}).$$

The PAE and η get close when the G_{op} is high. Practically, for gain larger than approximately 15 dB to 20 dB the difference between η and PAE are negligible [3].

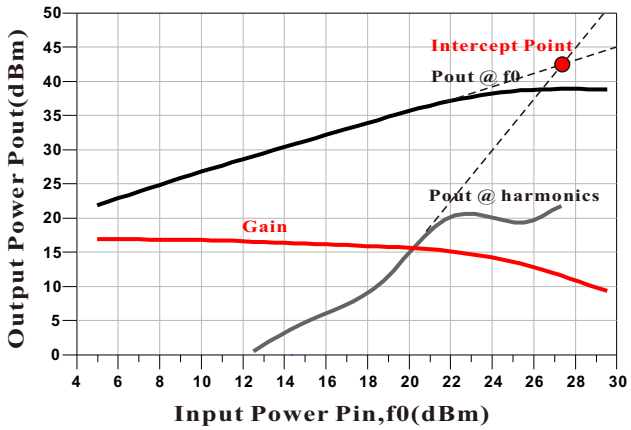

Figure 2.5: $P_{in} - P_{out}$ characteristics.

C. Third harmonic intercept point

With the aid of PA case simulation in ADS, the $P_{in} - P_{out}$ characteristic is shown. In the small signal regime, only the P_{out} at fundamental generated by the PA. However, as the P_{in} increases, the P_{out} at harmonics increases and $P_{out}(f_0)$ comes to saturate. The G_{op} in red illustrates that gain remaining constant in the small signal regime (see Fig. 2.5). As the signal strength grows, the gain is compressed. $P_{in} - P_{out}$ characteristics enable us

to get the third harmonic intercept point, which can be used as a linearity FoM since it is the result of an extrapolation from the small-signal [8].

Two-tone test - Carrier Power to Inter-modulation Power Ratio (CIMR)

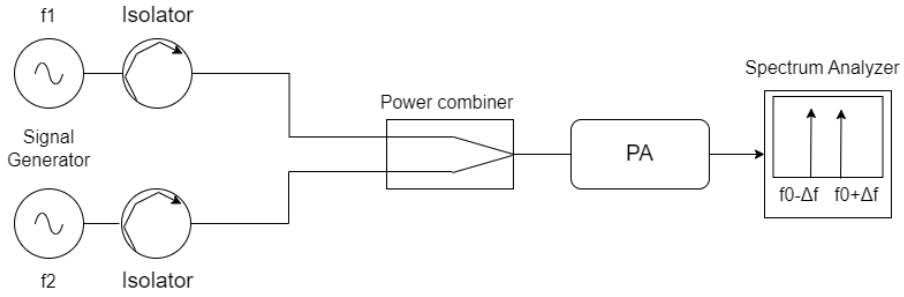

Figure 2.6: Simulation/measurement setup for a two-tone test on a PA.

The two-tone test is conducted to investigate the inter-modulation effect of the PA. The input of two-tone measurement is a set of two signals spacing with Δf and centered around f_1, located on frequencies f_1 and f_2. The signals are input to the PA after being processed by a 3 dB power combiner. The output is collected by the spectrum analyzer, which displays a series of intermodulation products at frequencies $m f_1 - n f_2$ with m, n integers, centered around f_0 (Fig. 2.6). The carrier power to 3rd order intermodulation power ratio ($CIMR_3$) is the significant criteria of linearity, shown in Fig. 2.7 [3].

$$CIMR_3 = \frac{P_{out}(f_1, f_2)}{P_{out}(2f_1 - f_2, 2f_2 - f_1)}$$

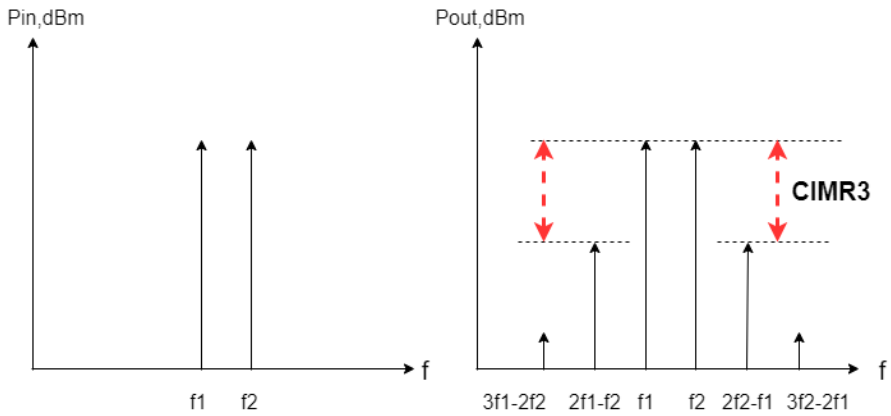

Figure 2.7: Input (left) and output (right) spectrum for two-tone test.

Adjacent Channel Power Ratio in Modulated signal test

The modulated signal test is a numerical measurement of the interference on an adjacent channel caused by spectral regrowth while there are input signals present. In

a modulated signal test, the input signal has a continuous spectrum that is often constrained to a small band around f_0. Besides, spectral regrowth appears in the adjacent channel due to the generation of odd-order inter-modulation products. (see Fig. 2.8) The adjacent channel power ratio (ACPR) is the linearity criteria, defined as:

$$\mathrm{ACPR}_3 = \frac{\int_{\mathrm{MC}} P_{\mathrm{out}}(f)\,df}{\int_{C_k} P_{\mathrm{out}}(f)\,df}$$

where MC stands for main channel f_c and C_k is k – th adjacent channel.

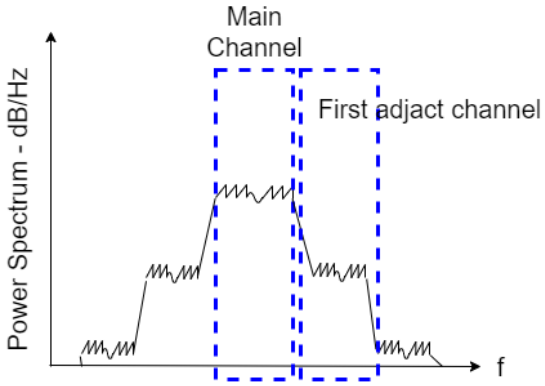

Figure 2.8: Output power spectrum after amplification, affected by spectral regrowth.

Stability

Stability is a key consideration when designing amplifiers. It is desirable that non-oscillation operation is maintained even in the presence of noise [8]. For instance, the PA should not produce an output signal at a frequency different from that of the main excitation, even though the spectral purity of the input source is limited, the power supply injects low-frequency disturbances, or there are undesired external signals. To evaluate the stability, some criteria are defined to determine if a two-port is unconditionally stable or potentially stable. It is known that a two-port loaded with generator and load impedance with positive real part is unconditionally stable if, (1) for any load impedance value, the input impedance has a positive real component (expressed through reflectance $|\Gamma_{in}| < 1$), and (2) For any value of the generator impedance has a positive real part in the output impedance.($|\Gamma_{out}| < 1$) [2]. Furthermore, stability is frequency dependent since the two-port characteristics are generally frequency dependent.

In the following is reported the two port stability criteria – stability factor K [8], which is a set of necessary and sufficient conditions:

$$K = \frac{1 - |S_{22}|^2 - |S_{11}|^2 + |\Delta|^2}{2|S_{21}\,S_{12}|} > 1$$

Together with,

$$|\Delta| < 1$$

where $\Delta = |S_{11}S_{22} - S_{12}S_{21}|$. By this set of criteria, if 1) K < 1, or 2) K > 1 but Δ > 1, the two-port is potentially unstable.

Another stability parameter for demonstrating the stable condition of linear 2-port circuits is "μ". $\mu > 1$ is both necessary and sufficient for being unconditionally stable [5]. This stability factor μ is well exploited by CAD tools. The equation is defined below,

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^{*}\Delta| + |S_{11}\,S_{22}|}$$

where the S_{11}, S_{22} are the scattering parameter of S-matrix, which is applied to describe the electrical behavior of the two-port network (see in Fig. 2.9).

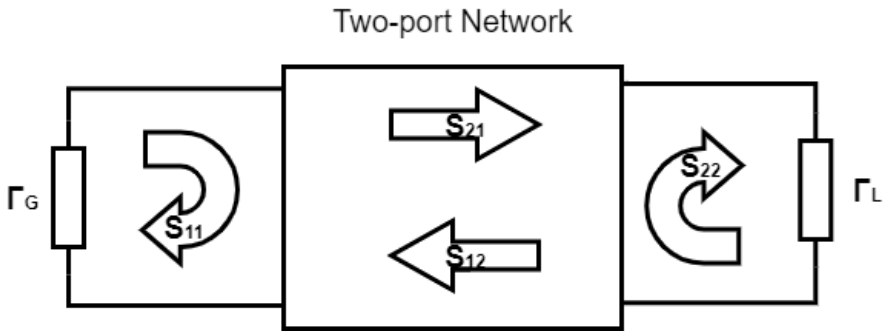

Figure 2.9: Scattering representation of a generic two-port network.

Maximum Available Gain

The maximum available (MAG) gain is the device's theoretically achievable power gain when the maximum power transfer is realized in the PA.

$$\mathrm{MAG} = \frac{|S_{21}|}{S_{12}}(K - \sqrt{K^2 - 1})$$

2.3 PA Classes

A typical single-ended power amplifier includes input and output bias T, active devices, and possible resonators. In detail, the bias T is built by DC capacitive block and RF inductive block, to avoid mutual interference. Meanwhile, the resonators are usually designed to filter undesired harmonics out to boost efficiency. The configuration of the single-ended power amplifier is illustrated in Fig. 2.10.

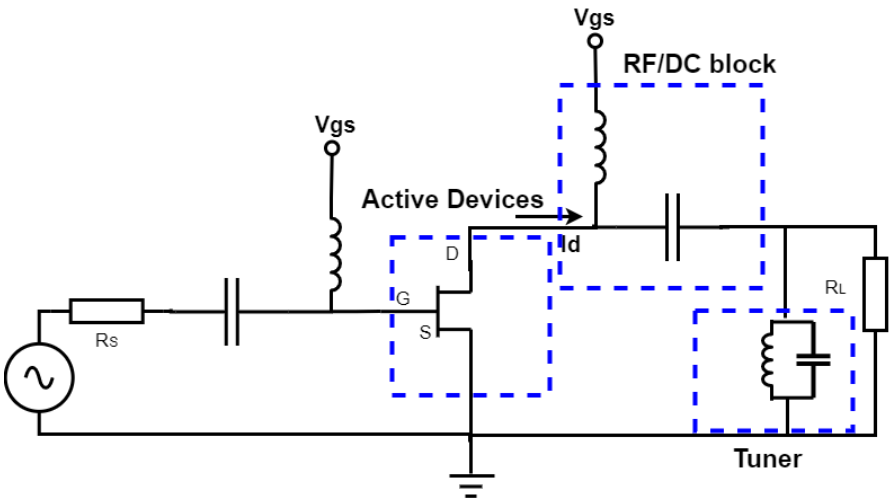

Figure 2.10: Power amplifier in single-ended configuration with the tuned load.

Active devices like transistors are commonly applied to amplify the input power in the PA design. The input signal imported from the gate alters the conductivity between the drain and source, controlling the drain current value. Based on the selection of bias voltage at the input, PA can be classified into different classes with corresponding property (Fig. 2.11) [8].

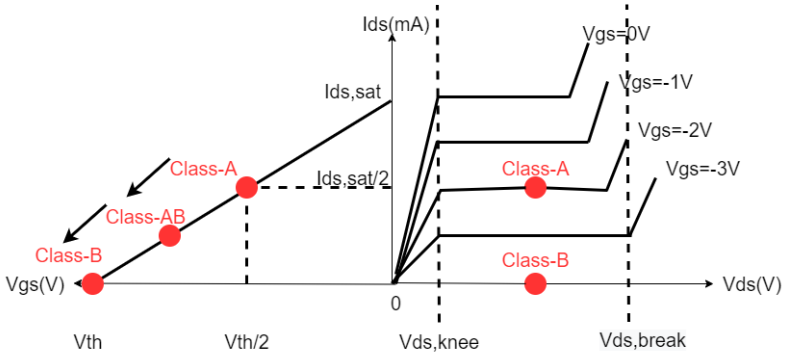

Figure 2.11: Trans-characteristics (left) and output characteristics (right) of the ideal device used in the analysis, with bias points of different PA classes.

Linear PA Class-A

In a class-A amplifier, the bias voltage at the gate V_{gs} and drain voltage V_{ds} is set to half of the threshold voltage $V_{th}/2$ and half of the breakdown voltage $V_{br}/2$ respectively, generating half of the maximum drain current $I_{ds,sat}/2$ at the drain. In terms of dynamic range, the maximum range of gate voltage is $[0, 2V_{dc}]$, meanwhile for output current it is $[0, I_{dss}]$. The corresponding optimum load R_{opt} is V_{br}/I_{dss} approximately. Therefore, the

maximum efficiency is

$$\eta = \frac{V_{br} * I_{dss}/4}{V_{br} * I_{dss}/2} = 50\%.$$

Considering the waveform of output current and voltage is almost sinusoidal (Fig. 2.12), the class-A amplifiers operate with minimal distortion but also with relatively low efficiency.

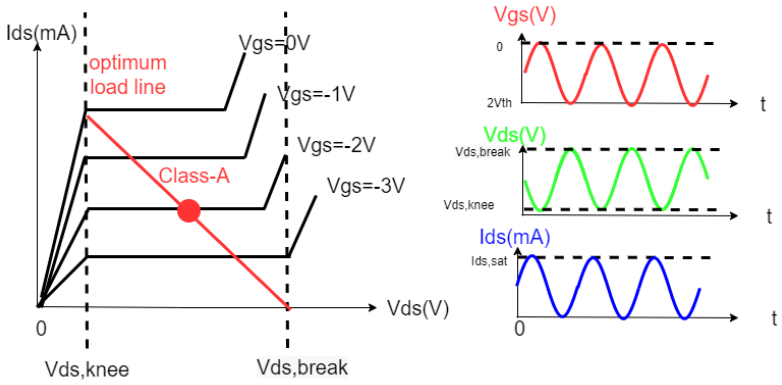

Figure 2.12: Class A: Output characteristics with dynamic load line (left) and time domain waveforms (right).

Nonlinear PA Classes: A, AB, C

Class-B

For a class-B amplifier, V_{gs} is equal to $V_{th}/2$ and V_{ds} is set to $V_{br}/2$. The corresponding optimum load R_{opt} is $V_{br}/(2I_{dss})$ approximately. The dynamic range of the Class-B amplifier is similar to the Class-A amplifier. As a consequence, the output current is approximately a half-wave rectified sinusoidal (Fig. 2.13) which leads to high non-linearity of the amplifier. Class-B amplifiers have a lower gain than Class-A amplifiers, but they are more efficient. In theory, a Class-B amplifier with a tuned load has the maximum efficiency.

$$\eta = \frac{1}{2} * \frac{V_{br} * I_{dss}/2}{V_{br} * I_{dss}/\pi} \approx 78\%$$

Class-AB

Class-AB is an intermediate case between class-A and class-B, which means the input voltage is below the threshold for less than half a period. In this class, efficiency improved while maintaining a certain amount of linearity.

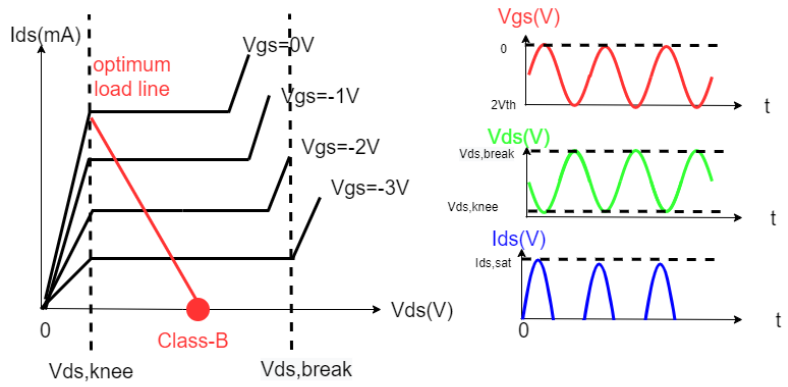

Figure 2.13: Class B: Output characteristics with dynamic load line (left) and time domain waveforms (right).

Class-C

In Class-C amplifiers, the output current deviates from zero for a longer period of time and the input bias is below the threshold. In comparison to class-B, class-C has higher distortion and lower gain, but also higher efficiency. However, at the limit, zero gain is required to achieve 100% efficiency. As a result, the practical value of class-C amplifiers is constrained.

From Class-A to Class-C

The conventional PA classification is determined by the drain current conduction angle α. The drain current circulation angle α clearly determines the amplifier class, according to conventional classification, presented as:

$$\frac{\alpha}{2\pi} = \frac{t_{on}}{T}$$

where t_{on} stands for the "on" state time of the PA. Therefore, conduction angles for PA are shown in table 2.1. Observe that class-A and class-B relate to conduction angles that are clearly defined, whereas class-C (and class-AB) correspond to an interval where the conduction angle may fluctuate depending on the applied RF stimulation.

In contrast to class-A amplifiers, class-AB, B, and C devices are driven below the threshold for a growing percentage of the time. The fundamental benefit of switching from class-A to class-AB amplifiers is an increase in efficiency in two areas (see in Fig. 2.14): not only is the peak efficiency higher than 50%, but the efficiency decline due to signal back-off is also less severe than in class-A amplifiers. However, both in terms of linearity and gain, nonlinear amplifiers fall short of class-A amplifiers.

Conduction angles of Classical PA		
PA Class	On-period t_{on}	Conduction angle α
A	T	2π
AB	$\frac{T}{2} < t_{on} < T$	$\pi - 2\pi$
B	$\frac{T}{2}$	π
C	$< \frac{T}{2}$	$< \pi$

Table 2.1: Summary of conduction angle characteristics for different PA classes.

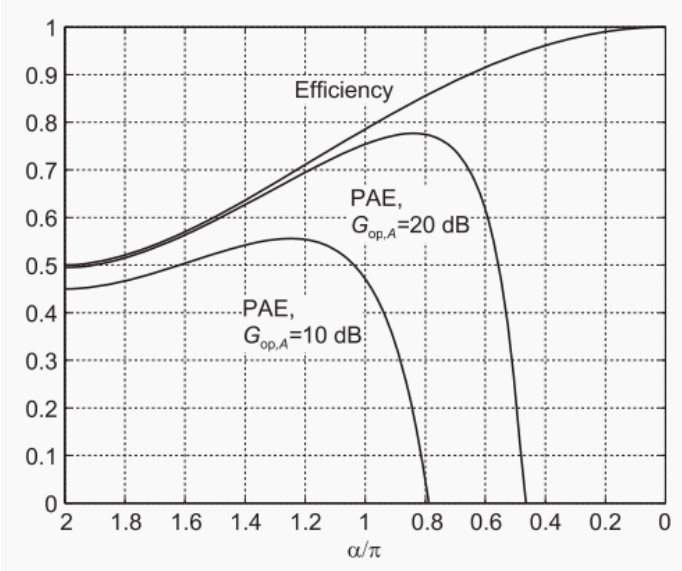

Figure 2.14: Efficiency and power added efficiency as a function of the circulation angle for several values of the class-A operational gain [8].

The behaviour of PAE and efficiency as the function of conduction angle is analysed mathematically [8](see Fig. 2.14). Efficiency rises monotonically from class-A to deep class-C, but the maximum efficiency of 100 percent attained in class C is essentially meaningless because it equates to no gain. According to the PAE behaviour, very high class-A gains are the only ones that allow for huge circulation angles to operate at their full efficiency.

Class-AB, B, and C amplifier inter-modulation product behavior cannot be as easily explained as class A amplifier inter-modulation product behavior. The usual behavior of inter-modulation products as a function of input power is depicted in Fig. 2.15, and it is crucial to note that this figure also illustrates the so-called ”sweet spots” where the IMD3 experience cancellation rather than the third-power law seen in class-A. Although there is only one sweet spot illustrated, practical amplifiers can potentially detect several sweet spots.

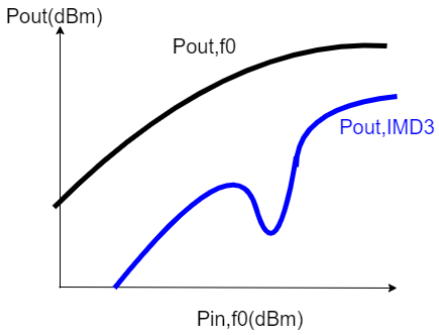

Figure 2.15: Example of two-tone test of a class-AB amplifier. The intermodulation product behavior vs. the input power does not follow a third-power law and sweet spots are present.

High efficiency PA: class-F and class-E

In some high efficiency PA designs, the active device operates in a specific operating mode, aiming to maximize the useful output power and simultaneously diminish the dc power consumption. Since they won't be used in this design, they are merely briefly stated here.

Class-F

The class-F amplifier applies the strategy of controlling the harmonics generated by the nonlinear stages to boost the amplifier efficiency. The bias is the same as the class B amplifier, which means the drain current will have a half-wave rectified sinusoidal. Besides, the resonators of class-F PA are designed to short at even harmonics and open at odd harmonics. In such conditions, the drain voltage waveform is a square wave, and the instantaneous power dissipated by the device is zero. (See Fig. 2.16) Therefore the power from the DC source is completely converted into RF, with 100 percent efficiency [15].

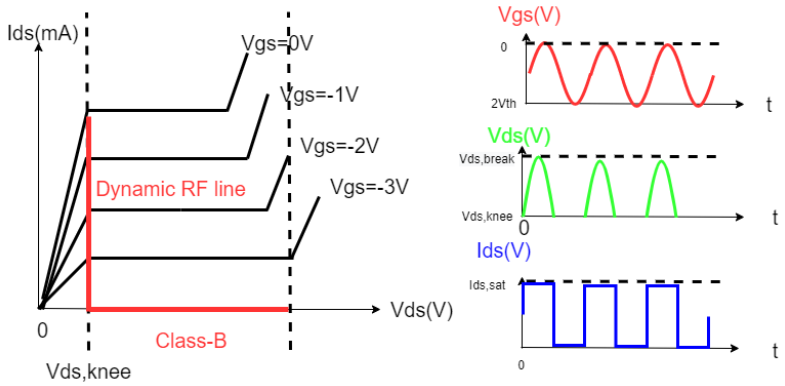

Figure 2.16: Class F: Output characteristics with dynamic load line (left) and time domain waveforms (right).

Class-E

The class-E amplifier is a highly efficient tuned switching power amplifier. The single-pole switching element and a tuned reactive network are applied between the switch and the load. The high efficiency performance is obtained by only operating the switching device either at points of zero current or zero voltage, which minimizes power lost in the switch [15].

3 Circuit Design

A gallium nitride (GaN) high electron mobility transistor (HEMT) is adopted to meet the output power requirements in this thesis while achieving high efficiency and relatively linear performance. The selected packaged device is manufactured and commercialized by Wolfspeed Inc. and corresponds to the model code CGH40006P. The DC characteristics and stability of CGH40006P are analyzed during the pre-design stage. The simulations shown in the following Chapters refer to the non-linear model of the packaged device, provided by the manufacturer for the adopted CAD tool (Keysight ADS).

3.1 DC Characteristics

Before designing the PA, it is necessary to evaluate the DC characteristics of the active device since it serves as the foundation for selecting the DC working point. They are defined in terms of trans-characteristics and output characteristics. Output characteristic reveals the relation between V_{ds} and I_{ds} for each V_{gs}, while the trans-characteristics display the I_{ds} changes as the V_{gs} varies at each V_{ds}.

The DC characteristics reported in Fig. 3.1, the output characteristic is obtained by sweeping the V_{ds} from 0 V to 150 V for a series of V_{gs} ranged from -4 V to 0.5 V. Inversely, the trans-characteristics is acquired by sweeping the V_{gs} from -4 V to 0.5 V for each V_{ds} between 0 V to 150 V.

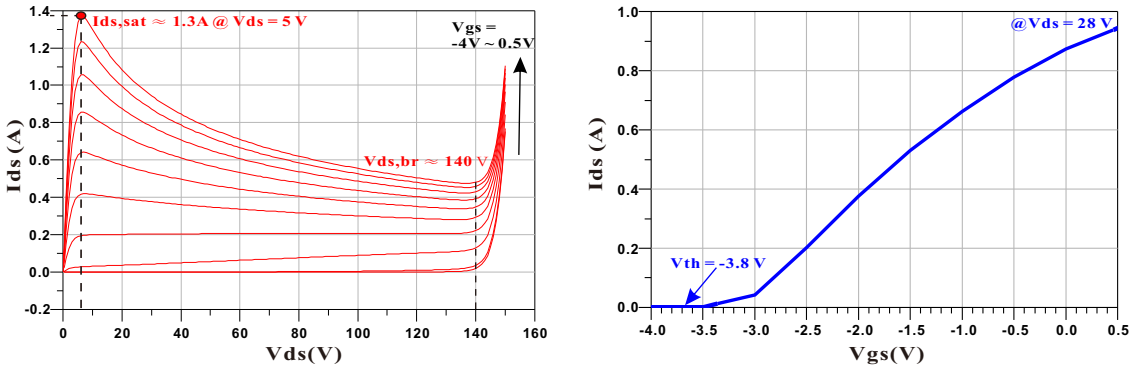

Figure 3.1: Analysis of transistor: output characteristics (left) and trans-characteristics applying V_{ds} = 28 V (nominal) (right).

The parameters required for design are the saturated current $O_{ds,sat}$ threshold voltage V_{th} and breakdown voltage $V_{ds,br}$, etc., which are determined by the output and trans-characteristics, listed below:

- Knee voltage $V_{ds,knee}$: 5 V

- Breakdown voltage $V_{ds,br}$: 140 V
- Threshold voltage V_{th}: -3.8 V
- Saturated current $I_{ds,sat}$: 1.4 A

On the basis of the PA theory introduced in the last chapter, a set of DC working points of HEMT located in the deep class-AB region is selected. As a result, the device is applied with V_{gs} = -2.6 V to -3.2 V and V_{ds} operates at a nominal 28 V.

3.2 Stabilization Network

In and out-of-band stabilization is mandatory to avoid oscillations, typically low-frequency oscillations that would saturate the amplifier [8]. Hence, a stabilizing network is designed to stabilize the PA. The stability condition of a transistor biased in deep class-AB region (V_{gs} = -2.6 V to -3.2 V) on frequencies 1 to 30 GHz is evaluated by FoM stability factor μ, simulated in Keysight ADS.

According to the simulation's findings (Fig. 3.2), the device biased in deep class-AB working point is potentially stable in both low frequency and above 8 GHz. Nevertheless, unconditional stability prevails in the upper frequencies.

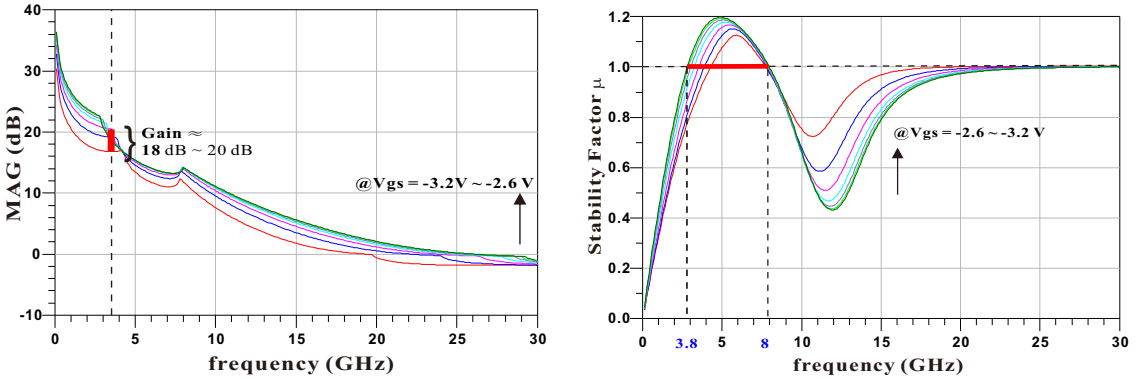

Figure 3.2: Small signal stability analysis of the CGH40006P device: MAG (left) and stability factor (right) versus frequency.

However, the device would become unconditionally stable if the negative input/output resistance or conductance for any passive output/input termination can be compensated respectively [8]. Furthermore, a stability factor K can be represented in terms of impedance to give the idea of stabilization. The equation reads as follows:

$$K = \frac{2\mathrm{Re}[Z_{11}]\mathrm{Re}[Z_{22}] - \mathrm{Re}[Z_{12}]\mathrm{Re}[Z_{21}]}{Z_{12}Z_{21}}$$

where $Z_{11} = V_1/I_1$ is the ratio of input voltage and current when the output port is open, and the subscript number illustrates the corresponding port.

A closer look reveals that adding the impedance at input/output to modify Z_{11}/Z_{22} does not affect the Z_{21} and Z_{12}. Because of that, the stability factor K would rise above 1, transistor stabilized correspondingly. This point serves as the foundation for the design of the stabilization network. Therefore, some resistive stabilization networks are proposed (Fig. 3.3).

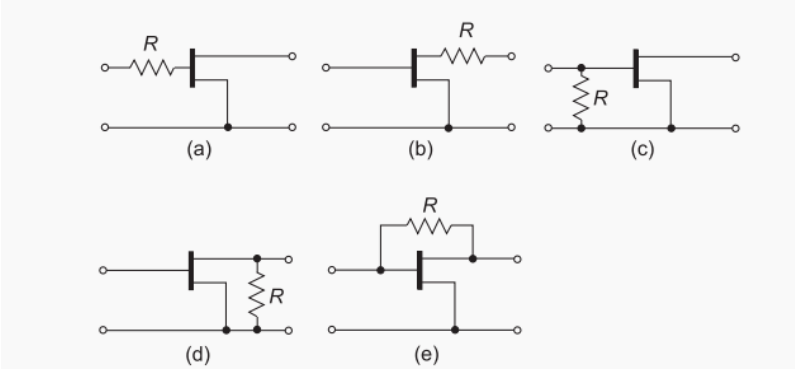

Figure 3.3: Resistive stabilization of a transistor [8].

In order to stabilize the network at both low and high frequencies, the simulation used the resistance combination of topologies (a) and (c). A 150 Ω resistance in series and a 120 Ω one in shunt are connected to the transistor's gate.

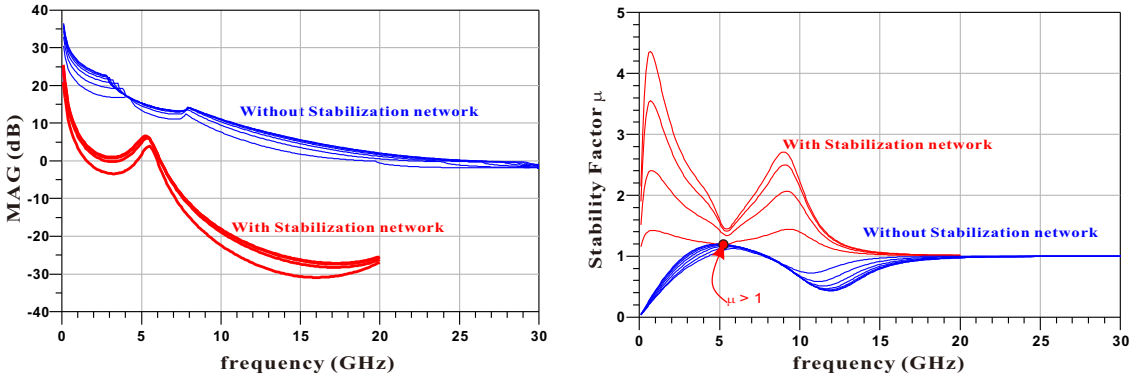

Figure 3.4: Small signal stability analysis of the CGH40006P device, without (blue) and with resistive (red) stabilization network.

The simulation result (Fig. 3.4) illustrates that the resistive network would stabilize the transistor, but the MAG is reduced due to the dissipative components in the circuit. However, for PA design case, the MAG should be improved to enable the PA to provide

sufficient gain. Therefore, a stabilization network including passive elements are applied in this design (Fig. 3.5).

The stabilization network is constructed utilizing RC parallel blocks in series and RL series blocks in parallel. RC block in series is in charge of the stability on low frequencies, but less affects the high frequencies since the capacitance is seen as "short" in high frequencies. The RL block is in parallel charges with high-frequency stability. The MAG could be improved in such topology due to the presence of passive elements.

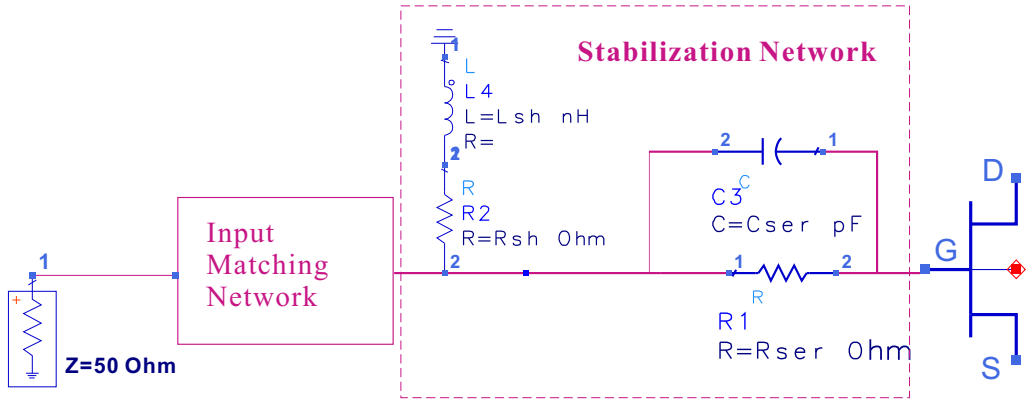

Figure 3.5: Circuit diagram of the topology adopted for the input stabilization network.

The stabilization network shown in Fig. 3.5 is simulated in Keysight ADS. The value of components is available for tuning. In this design, the parameters of the stabilization network are: Rser = 150 Ω, Cser = 1.8 pF, Rsh = 120 Ω, the Lsh is neglected. Consequently, the unstable issue is solved. And the MAG for the device biased with the DC operating points located in the deep-AB region is improved to more than 17 dB peaking at 3.5 GHz (Fig. 3.6).

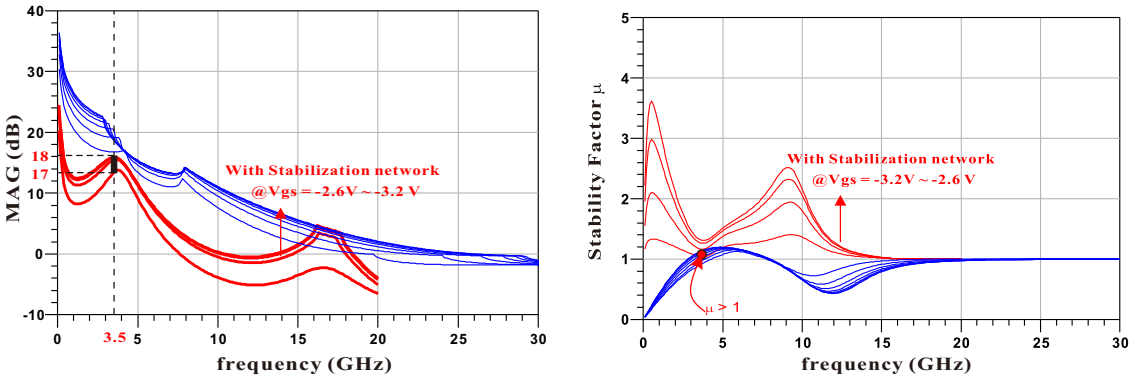

Figure 3.6: Small signal stability analysis of the CGH40006P device, without (blue) and with frequency-dependent resistive-reactive (red) stabilization network.

3.2.1 DC biasing Network

In PA design, the DC biasing network is requested to decouple the DC source supply from the RF circuit through proper circuit blocks, hence reducing the likelihood of mutual interference. Further explained, mutual interference mainly accounts for (a) possible power dissipation and damage if DC flow in the passive part of the RF circuit; (b) unpredictable electrical behaviour at electrical when the RF circuit is loaded on the DC bias one [2].

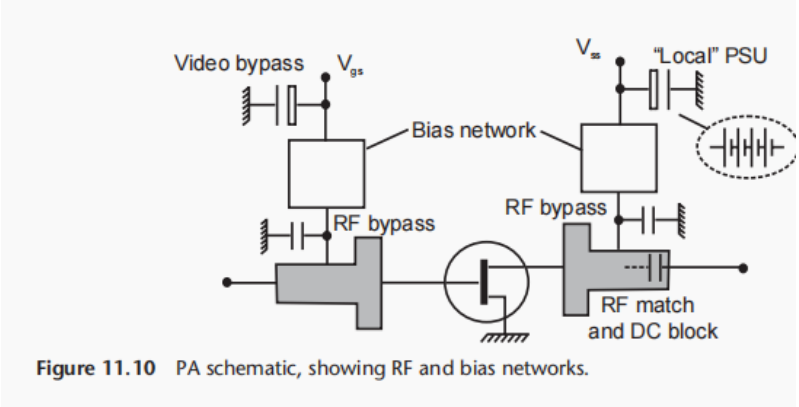

Figure 11.10 PA schematic, showing RF and bias networks.

Figure 3.7: PA schematic with biasing network [2].

Biasing network is designed at both input and output in the FET-like device-based PA (see Fig. 3.7). On the input side, since the DC source supply has a significant effect on the current generated from the output, the biasing network is requested to appear as a near-short circuit over the whole signal bandwidth. On the output side, there will be an intermediate biasing network that connects the RF decoupling point and a local voltage supply in the form of a suitably large capacitor, as a current reservoir [2].

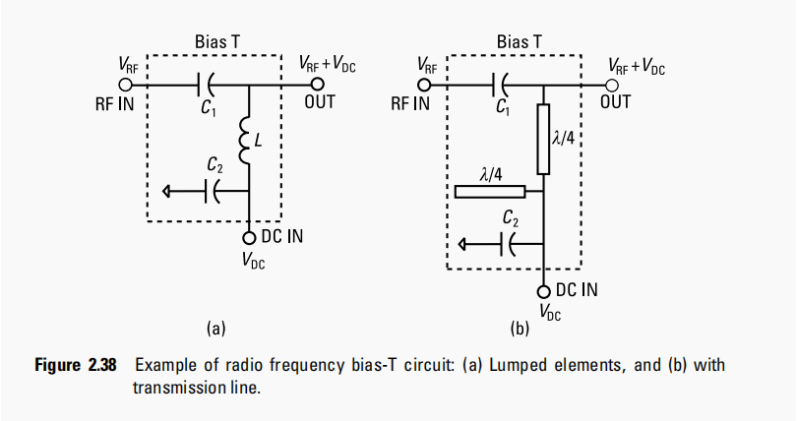

Figure 2.38 Example of radio frequency bias-T circuit: (a) Lumped elements, and (b) with transmission line.

Figure 3.8: Biasing network topologies [2].

Two different topologies of DC biasing block are depicted in Fig. 3.9. For each topology, the lumped C1 serves as a DC block and exhibits low resistance to the RF signal. Separately speaking, the inductor L is a DC short but nearly an open circuit at RF for the topology in (a). In such a topology, the short in the DC circuit would be worse since inductors would be harder to deploy at high frequencies. The open $\lambda/4$ stub RF and blocking capacitor C2 will work together to create a high-quality "short" for the topology in (b) [2]. By applying topology (b) in practice, the biasing circuit functions as a close approximation to an ideal short due to the recursion of numerous pairs of big capacitors and $\lambda/4$ stub.

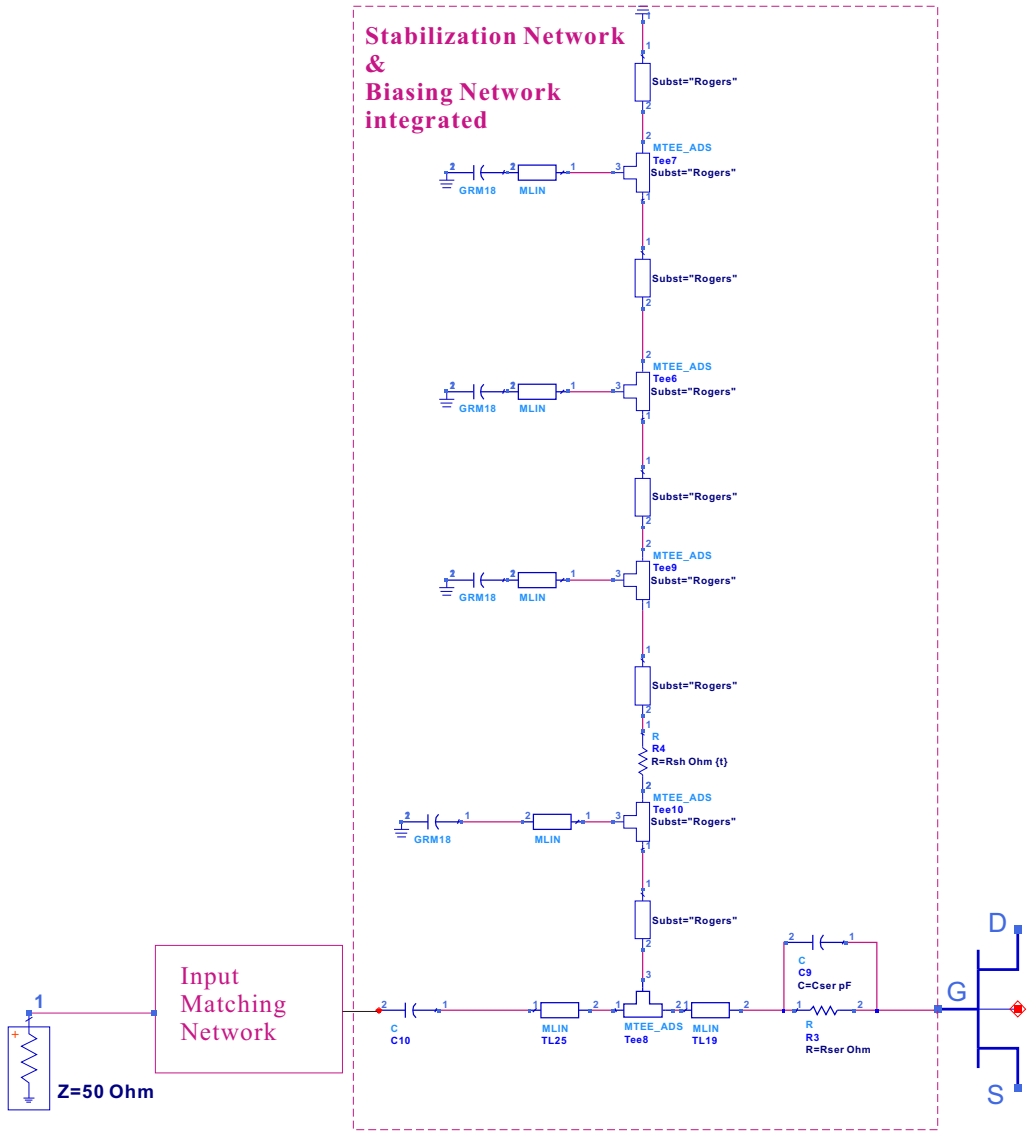

Figure 3.9: Realized biasing network integrated with stabilization block.

The design uses several pairings of the blocks that are depicted in Fig. 3.8 (b). The

biasing network is implemented by the micro-strip fabricated on Roger435b. The existing ideal ”short” in the stabilization network is replaced by biasing block which presents a high-quality ”short” in practice. Consequently, the stabilization and biasing network are integrated (Fig. 3.9).

However, the integration would modify the stability condition of the circuit on frequencies. Despite this, the possible fluctuation in the ground node would be seen as the source leading to potential stable conditions. Based on that, the designed circuit operating with the deep-class-AB biasing is simulated. As a result, shown in Fig. 3.10, the circuit maintains unconditional stability on all frequencies. And the MAG would increase to 18 dB at the center frequency of 3.5 GHz.

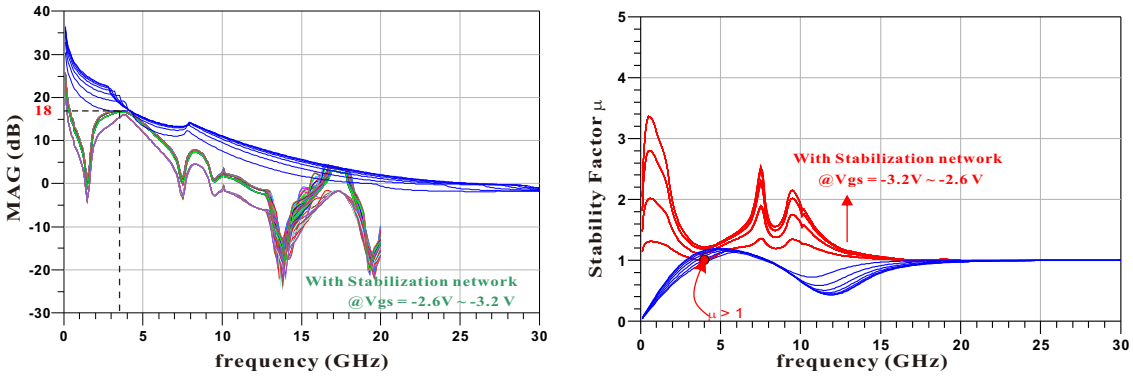

Figure 3.10: Small signal stability analysis of the CGH40006P device, without (blue) and with final stabilization network integrated with the gate biasing network (red).

3.3 Determination of Optimum Terminations

In this section, simultaneous optimization of source and load terminations is designed to satisfy the aforementioned requirements. It is assumed that the performance in both CW one-tone and two-tone measurements should be achieved with the same biasing setting.

3.3.1 Optimization for Power

Since $P_{out,f0}$ is the main prerequisite of PA to qualify for the linearity test, the simultaneous optimization of source and load terminations targets on maximizing the $P_{out,f0}$ firstly. In this design, the source/load termination is expressed as the reflection coefficient Γ_S and Γ_L present to the transistor. The design order for the optimization of Γ_S and Γ_L simultaneously is explained by the equation shown below [2],

$$\Gamma_{in} = \frac{S_{11} - \Delta\,\Gamma_L}{1 - S_{22}\,\Gamma_L}$$

as the equation presents, for a two-port network, Γ_L and Γ_{in} are related. Meanwhile, the maximized P_{out} is related to the match condition of Γ_L and Γ_{in} on related input power level. Hence, Γ_L should be primarily determined to select the suitable Γ_G for input matching at specific power conditions.

Load-pull Simulation

Based on load-line theory [2], the corresponding optimum load impedance is considered as an initial selection for fundamental load termination of PA design for realizing maximum power swing. However, the optimum load computed based on load line considerations is the one at the current source plane of the transistor and does not account for all parasitic and extrinsic effects. Different from the ideal one, the parasitic effect exists in the packaged device adopted in this design. Since the optimum load impedance is not able to compensate for the parasitic parts inside the device, it would not be selected as the load termination in this design. Instead, the load impedance is searched by the load-pull simulation to realize power maximization.

A load-pull simulation is introduced to determine which load impedance presents to a device to achieve a particular power delivered, PAE, IMD level and other specifications. Such measurement is available to simulate in Keysight ADS. The intended circuit is measured in the provided load-pull template, with a 50 Ω at source termination under the biasing condition V_{ds} = 30V and V_{gs} = −2.8V. The relevant outcome when P_{in} =

24 dBm is depicted in Fig. 3.11.

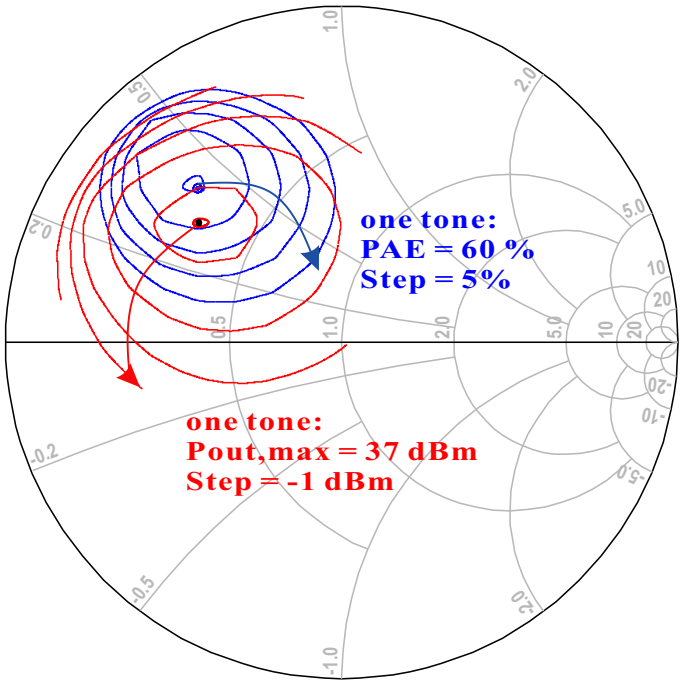

Figure 3.11: Load-pull in one-tone simulation when P_{in} = 24 dBm (V_{gs} = -2.8 V and V_{ds} = 30 V).

As the plot shows, the contours of the PAE and P_{out} in this plot heavily overlap, indicating that the PAE would remain at a high level while P_{out} optimized. At this step, the Γ on the position where $P_{out,f0}$ optimized, is selected as load reflection coefficient $\Gamma_{L,f0}$, with a coordinate of $0.555e^{-j140}$ in the Smith Chart. In the one-tone simulation, it is anticipated that $P_{out,f0}$ optimized to 37.27 dBm, leaving enough margin for P_{out} the possible loss. Nevertheless, expected PAE results of 60%.

The sweep of $\Gamma_{L,f0}$ is explored to reach output matching, maximizing the G_{op} and thus optimising the P_{out}. In the simulation, the $\Gamma_{L,f0}$ is configured to sweep using the previously chosen value. Consequently, the parameter sweep yields a set of curves encompassing the particular range in terms of PAE and P_{out}. $\Gamma_{L,f0}$ is chosen to be $0.54e^{-j120}$ in order to maximize P_{out} to 36.8 dBm when a single carrier with 24 dBm $P_{in,f0}$ injects. The PAE reaches 56.1%. The associated performance is displayed in Fig. 3.12. Additionally, the S_{22} proves that the PA is well-match at the output (Fig. 3.13).

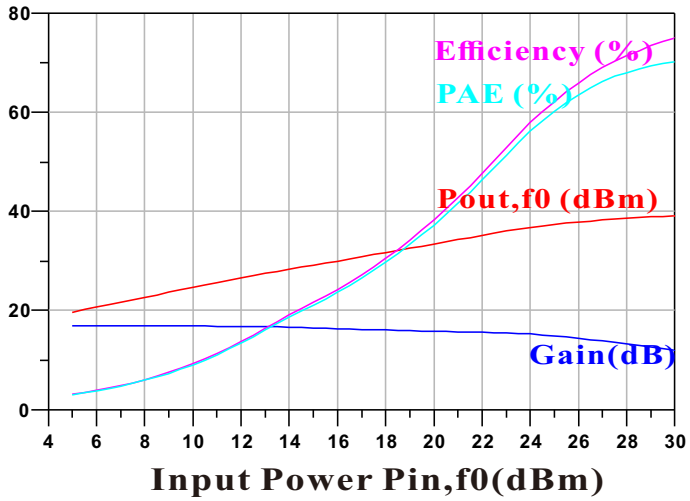

Figure 3.12: Optimized performance in one-tone simulation after adopted load-pull.

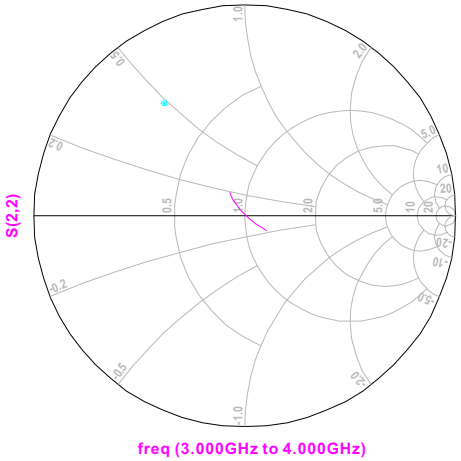

Figure 3.13: After load-pull: matching condition at load illustrated by S_{22}.

Source-pull Simulation

The source pull is performed for In this part, the $\Gamma_{S,f0}$ sweeps for reaching input matching at relative power level, aiming to maximize the G_{tr} for the whole PA chain thus maximizing the P_{out}. As the result shows, a collection of curves encompassing the specific range in terms of PAE and P_{out} are produced by the parameter sweep. $\Gamma_{S,f0}$ is selected as $0.615e^{-j220}$ to obtain maximum P_{out} to 38.2 dBm when a single carrier with 24 dBm $P_{in,f0}$ injects (Fig. 3.14). The PAE reaches 63.3%. The related performance is shown in the section below. The S_{11} further demonstrates that the PA is well-matched at the input (Fig. 3.15).

The PA optimized in terms of power provides a margin above the required P_{out} in one-tone simulation. The P_{out} criteria is thus fully met. However, it is essential to per-

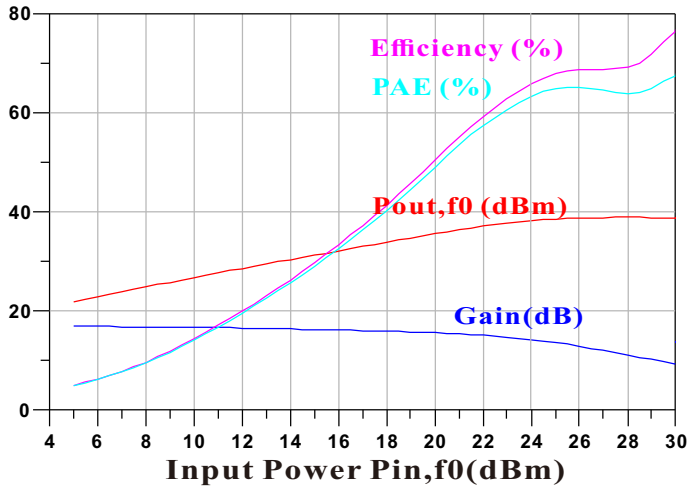

Figure 3.14: Optimized performance in one-tone simulation after adopted both load-pull and source-pull.

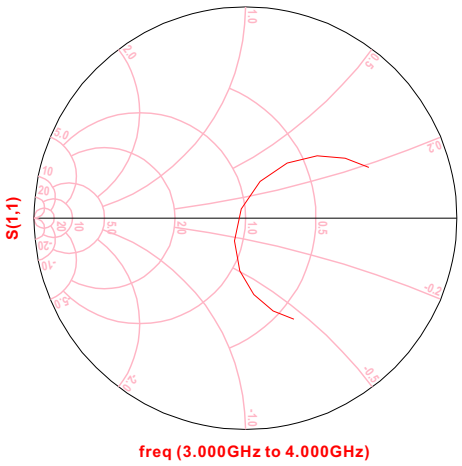

Figure 3.15: Matching condition at source illustrated by S_{11}.

form well in terms of PAE and IMD3 as well. Especially, the IMD3 criteria could be the toughest requirement among them. To assess the linearity of the PA, a two-tone simulation is used here.

In the two-tone simulation, source and load reflection coefficients are $0.615e^{-j220}$ and $0.54e^{-j120}$, respectively. The same biasing point V_{ds} = 30V and V_{gs} = −2.8V as CW simulation is set. The outcome is shown in Fig. 3.16, illustrating the IMD3 is seen to sustain a high linear level in a restricted small signal region. However, it exceeds -30 dBc when the $P_{in,f0}$ comes to 11 dBm (Fig. 3.16), the PAE reaches 15%.

Therefore, IMD3 should be optimized for maintaining below -30 dBc until the PA is injected with a maximum of 24 dBm $P_{in,f0}$. Meanwhile, the PA should be optimized for trading-off between PAE, IMD3, and P_{out}.

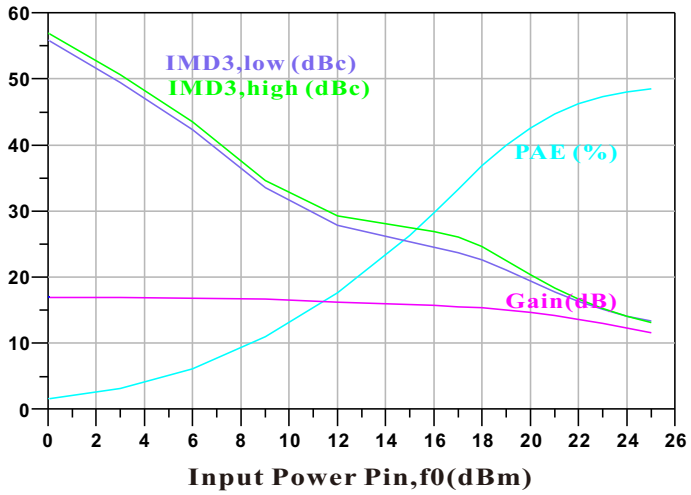

Figure 3.16: Performance of PA with power optimized in two-tone simulation.

3.3.2 Optimization for IMD3

There are a variety of ways to enhance IMD3. a) The biasing point adjustment is the easiest to perform. The equivalent linear behavior would differ because the change in biasing would lead PA to display different linear behavior. b) Modifying the source and load termination at baseband is another option to consider. Through this approach, it is anticipated that base-band control will have an impact on the IMD3 [1]. c) Additionally, the match condition adjustments would have an impact on the linearity behavior as well [9].

It is vital to verify the P_{out} again to confirm if it still gives margin to the requirement after modification, since each modification made will more or less have an impact on the P_{out}.

Adjustment of Biasing

Both V_{gs} and V_{ds} have been adjusted. The linearity behavior differs in small signals when the gate voltage changes from 2.8 V to -3.15 V. However the trend of IMD3 in higher power ranges tends to flatten out, slower the increasing speed of the IMD3. The V_{gs} is selected as -3.15 V. The IMD3 trend was little affected by the fluctuation of the V_{ds}, which remained at 30 V. Such that option was chosen, the simulation displays the IMD3 starts at a relatively higher value of roughly -40 dBc. As the input power increases, the slope declines more slowly than it did in the previous biasing (Fig. 3.17).

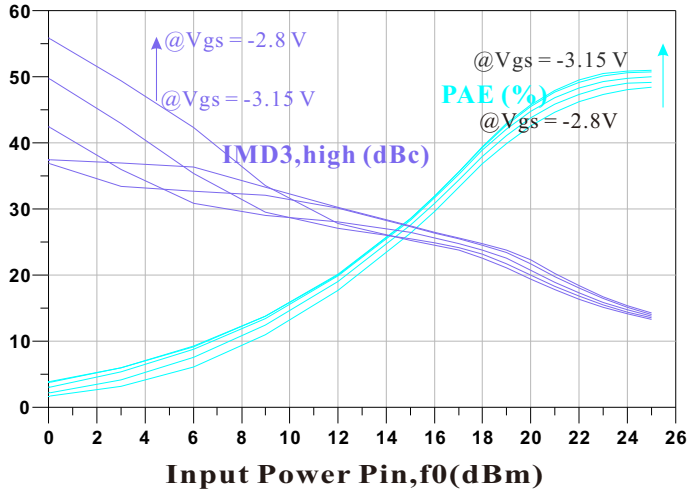

Figure 3.17: Adjustment of biasing to optimize the IMD3: two-tone simulation (V_{gs} ranger from -2.8 V to -3.15 V).

Modification of Source/Load Termination at Base-band

IMD3 performance is intended to be improved via base-band regulating. To test whether changing the termination of the source or load to a lower impedance could optimize IMD3, a straightforward experiment is conducted. The termination impedance range in this instance is 10Ω to 100Ω.

According to the graph (see Fig. 3.18), the IMD3 moves toward a greater linearity value throughout the entire power range when the load impedance at baseband $Z_{L,bb}$ lowers. Comparatively speaking, IMD3 is not benefited by changing the source impedance at baseband $Z_{S,bb}$. As a result, the $Z_{L,bb}$ is set to 10Ω, while the $Z_{S,bb}$ is as previous.

By utilizing the selected baseband, the IMD3 maintains below -30 dBc until the input RF power reaches 16 dBm (see Fig. 3.19). The decreasing trend of the IMD3 became flat in comparison to the one without change, and the PAE is significantly better since the IMD3 performs better in the higher P_{out} region (see Fig. 3.19).

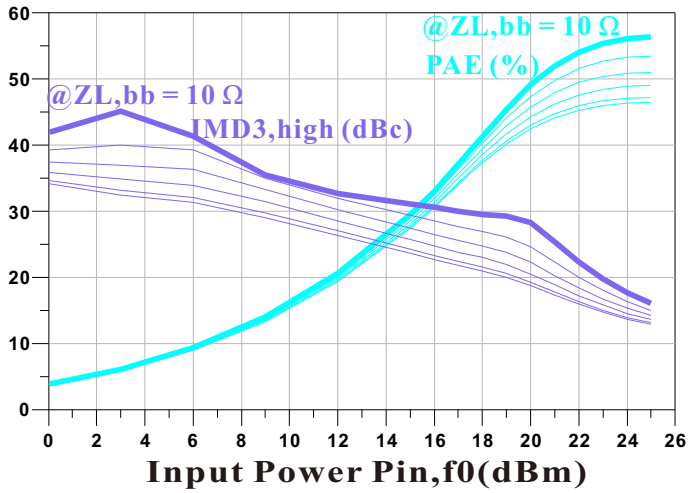

Figure 3.18: Modification of Load termination at base-band: two-tone simulation ($Z_{L,bb}$ ranger from 10 Ω to 100 Ω).

Mismatch Source/Load

The mismatch at both source and load is adjusted manually. With the mismatch applied, the IMD3 maintains 30 dBc until input RF power reaches 22 dBm.

The PAE overall lowered when compared to the ”match” one, but the goal PAE is increased since the IMD3 maintains over 30 dBc till a further input power level. In this case, $\Gamma_{L,fo} = 0.493e^{-j139.7}$ and $\Gamma_{S,fo} = 0.571e^{-j174.1}$ is select for the termination respectively. When used with these terminations, the IMD3 maintains a value above 30 dBc until the input RF power reaches a value of 22 dBm, with a corresponding PAE of about 45.64% (Fig. 3.20).

It is vital to confirm the P_{out} in one-tone simulation after modification since the match condition changes. The target P_{out} still provides a margin above the requested, as shown in the graph (Fig. 3.21).

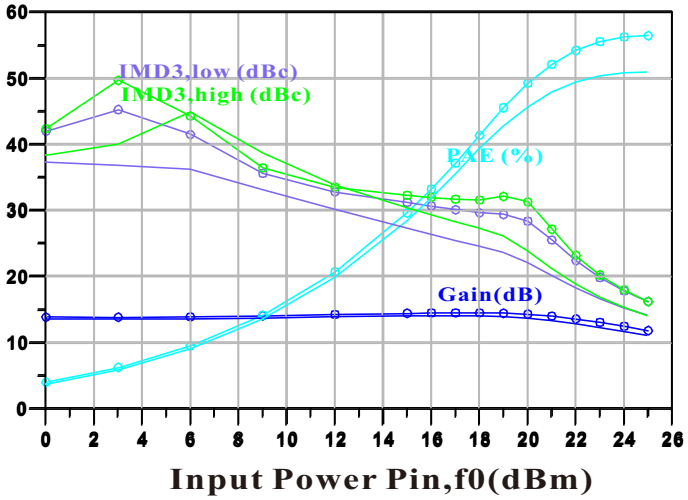

Figure 3.19: Comparison: Modification of Load termination at base-band (symbols) vs Without modification at base-band (solid): PA in two-tone simulation.

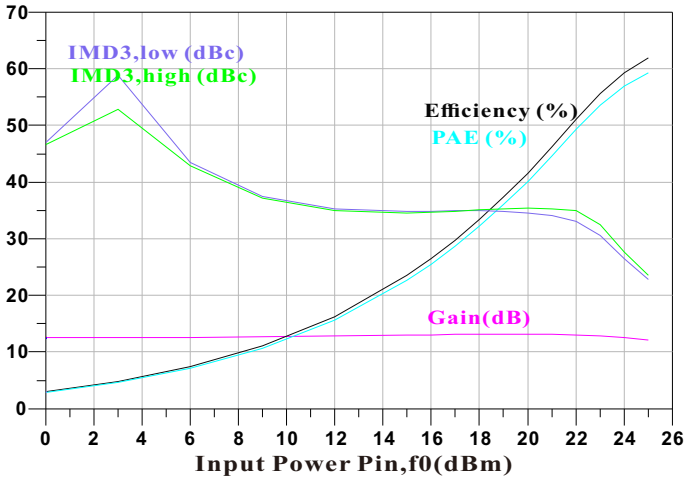

Figure 3.20: Mismatch for Improving IMD3: PA in two-tone simulation.

3.3.3 Boosting Efficiency

The PA is optimized in terms of P_{out} and IMD3 in the preceding section. In order to increase efficiency, second harmonic tuning is also used at the source and load. As a result, the second harmonic tuning has little impact on IMD3, notably not in the region of a strong signal. The intended PAE is raised to 48% in the meantime (Fig. 3.22). The equivalent value for $\Gamma_{L,2fo}$ is $0.99e^{-j60}$.

In conclusion, identifying the source/load at the base-band, fundamental, and second harmonics provides a target for executing the subsequent practice. The terminations are chosen as follows: $Z_{L,bb} = 10\Omega$, $\Gamma_{L,2fo} = 0.99e^{-j60}$, $\Gamma_{L,fo} = 0.493e^{-j139.7}$, $\Gamma_{S,fo} = 0.571e^{-j174.1}$.

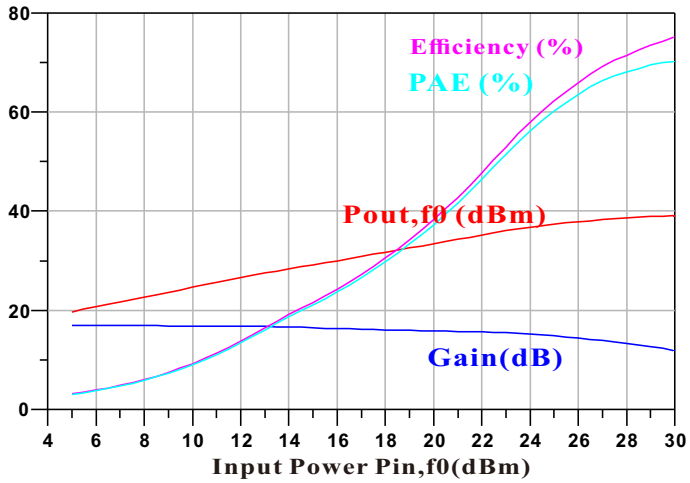

Figure 3.21: One-tone simulation of the PA optimized for IMD3.

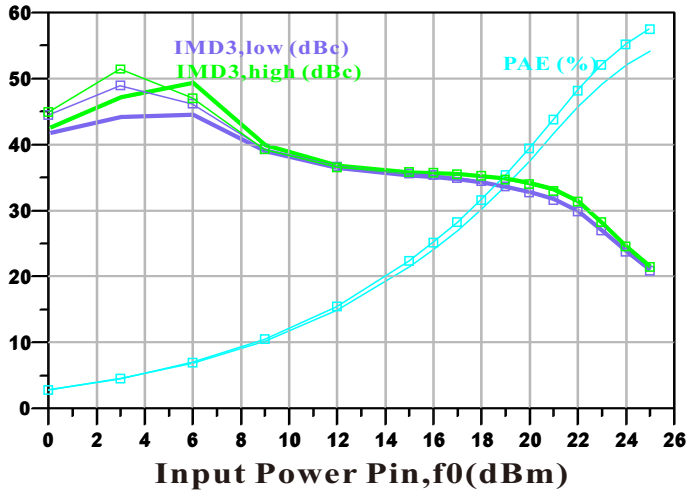

Figure 3.22: Boost efficiency by second harmonics control: PA performance in two-tone simulation.

3.4 Ideal Matching Networks Design

The input and output impedances for the PA integrated into the RF front-end are 50 Ω [10], which is different from the determined optimum impedance. Hence, the matching networks should be designed to transfer 50 Ω to the determined optimum one. In this design, ideal transmission lines (TLs) are adopted to build such a matching network. The design of the matching network is described in the following.

3.4.1 Output Matching Network

The optimization load involves controlling baseband, second harmonics, as well as the fundamental frequency. The matching should be designed for the match-determined termination on desired frequencies in order to realize optimization. Every corresponding matching block controls its own frequency range separately. The order of blocks illustrated in Fig. 3.23. The second harmonics matching is tuned as the first block along the power transfer channel, boosting PAE. The fundamental matching network is built at the following place to achieve optimal performance in terms of P_{out} and PAE at the fundamental frequency.

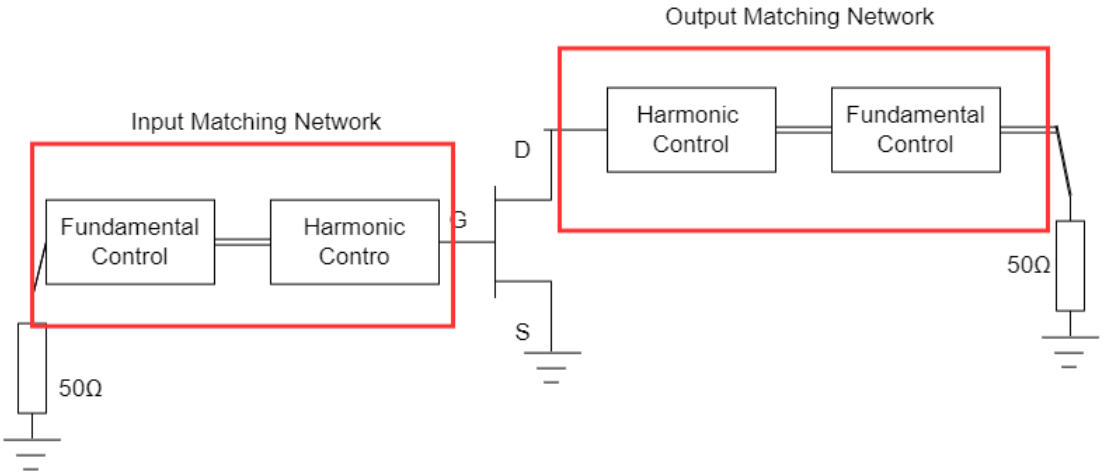

Figure 3.23: Block schematic of single-ended PA.

Shorts at Harmonics

In theory, the harmonics matching network should not consume any power because the reflection coefficient for second harmonics is reactive. The topology is therefore introduced. In this topology (Fig. 3.24), a transmission line in series is used primarily to modify the phase of $\Gamma_{L,2f0}$, whereas a transmission line in shunt is used to introduce a ”short” node into the network. This ”short” node is made in two different ways: ”short” could be created by duplicating the ”short” on another port of the transfer path. In another way, it can be obtained by converting the ”open” to the ”short” state. Both of these conversions take place at the second harmonic.

The S_{11} can be located in the designed $\Gamma_{L,2f0}$ region by employing this topology with the correct length of the TL in series (see Fig. 3.25).

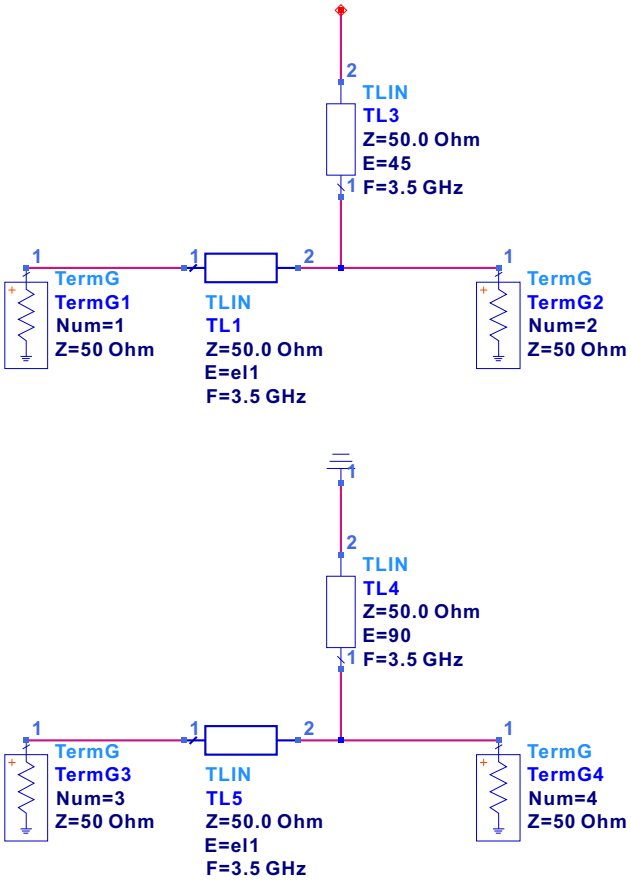

Figure 3.24: Topology of harmonics matching block.

Fundamental Control at Load

the fundamental control at the load target on realizing the chosen fundamental load. The topology uses a tunable transmission line to present the determined $\Gamma_{L,f0}$ at the load. The corresponding topology is the same as the one suggested above. In Fig. 3.26, the S_{11} provides an illustration of the match condition. As a result, the S_{11} reaches below -34 dB on frequency 3.5 GHz with relative 100 MHz in the plot, demonstrating the network is well-matched the $\Gamma_{L,f0}$ over the band.

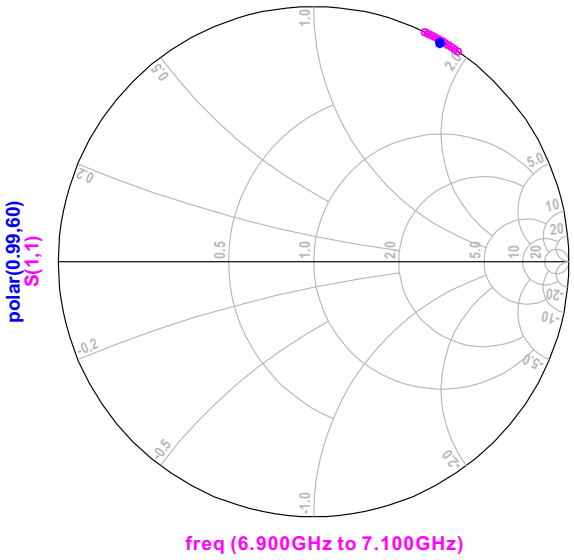

Figure 3.25: Second harmonics reflection coefficient.

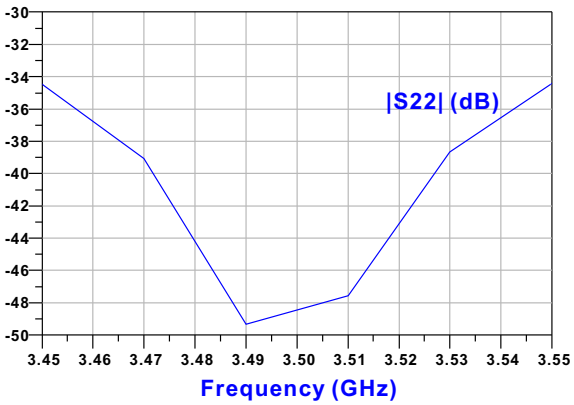

Figure 3.26: Fundamental matching condition illustrated by S_{22}.

Base-band Control at Load

The base-band matching block should be established after the fundamental one. However, the fundamental matching might have already narrowed the $\Gamma_{L,bb}$. Therefore, the prior action would be to investigate the base-band control posed by the constructed matching network. Additionally, the performance of two-tone simulation should be examined based on the existing base-band control.

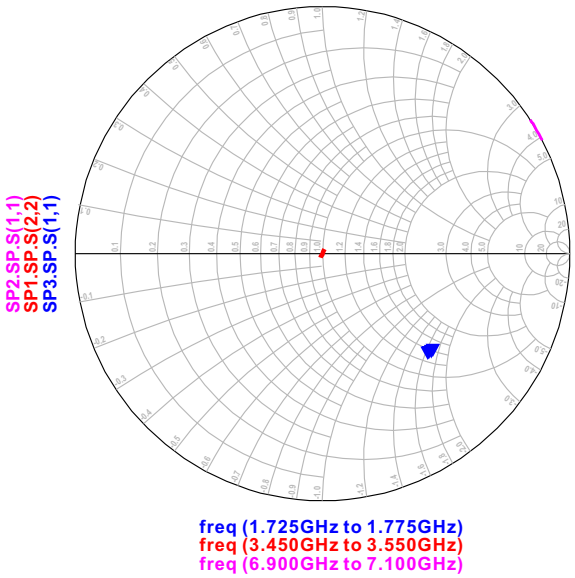

Figure 3.27: Matching condition at fundamental illustrated by S_{22}, and reflection coefficients for base-band and second harmonics illustrated by S_{11}.

In the two-tone simulation, the constructed output matching networks (OMN) are applied to the active device, with the source termination set as the determined value. The matching condition is depicted in the figure using the S-parameter (Fig. 3.27). And Figure 3.28 illustrates the pertinent performance.

The S-parameter demonstrates that the fundamental is properly matched, and the second harmonics are tuned to the chosen region. The $\Gamma_{L,bb}$ is situated at $0.55e^{-j41}$ in the meantime. When used with such a matching block, the performance is much in line with the desired results (Fig. 3.28). It confirms that the IMD3 benefits from the result $\Gamma_{L,bb}$. An extra matching block for base-band matching is not required.

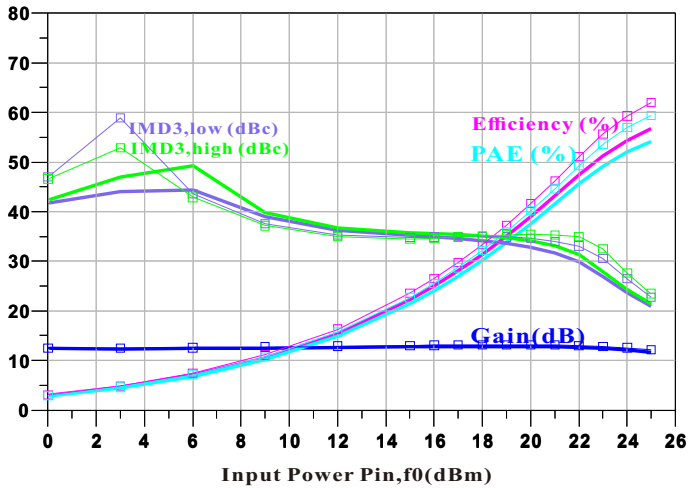

Figure 3.28: PA implemented with constructed OMN: two-tone simulation.

3.4.2 Input Matching Network

Only the fundamental control was optimized in the preceding section for source termination. Therefore, the input matching consists of just one block - fundamental matching. The technique used in output matching is the same. The identical topology is chosen, and the adjustable transmission line is used to achieve the desired $\Gamma_{S,f0}$ match condition. Consequently, the S_{22} in Fig. 3.29 shows the corresponding condition. The S_{11} maintains a good match at center frequency 3.5 GHz and stays below -32 dB in the band.

Figure 3.29: Fundamental matching condition illustrated by S_{11}.

Consequently, the PA is constructed with a matching network at the input and out separately connected to 50 Ω at the termination. The appropriate performance is shown below in Fig. 3.30. The outcome demonstrates that the implementation of the transmission line has enhanced performance in terms of IMD3 and PAE. As soon as the input RF strength hits 23 dBm, the IMD3 rise above -30 dBc. The improvement would be due to the better base-band control applied The target PAE is optimized to 56%.

3.5 Micro-strip Implementation

The circuit is built in hybrid technology on a Roger4350b PCB with a dielectric constant of 3.66. To fabricate the PA, the transmission line should be changed from ideal to microstrip. The design in this section is primarily focused on optimizing the input and output matching network to ensure it is coherent with the ideal one. And EM simulation is set up to evaluate the practical performance.

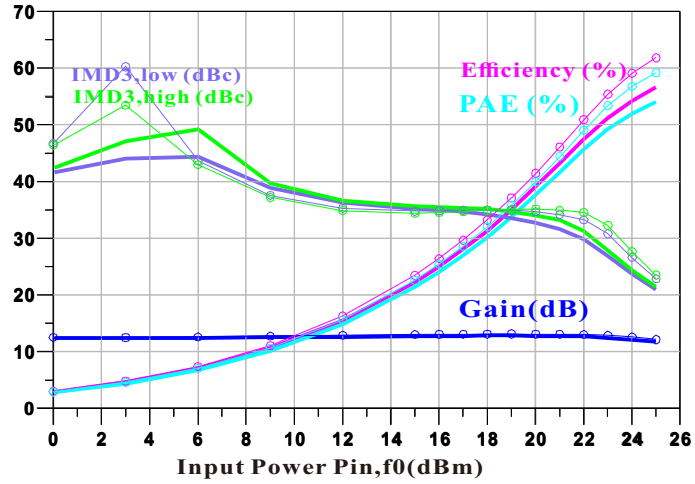

Figure 3.30: PA implemented in ideal TL: two-tone simulation.

3.5.1 Matching Networks Design in Micro-strip

The micro-strip is a type of electrical transmission line made up of a conductor, a dielectric layer, and a ground plane. In the structure of the microstrip, the conductor is separated from a ground plane by a dielectric layer. The described structure shows in Fig. 3.31. The corresponding line parameter is provided in Keysight ADS.

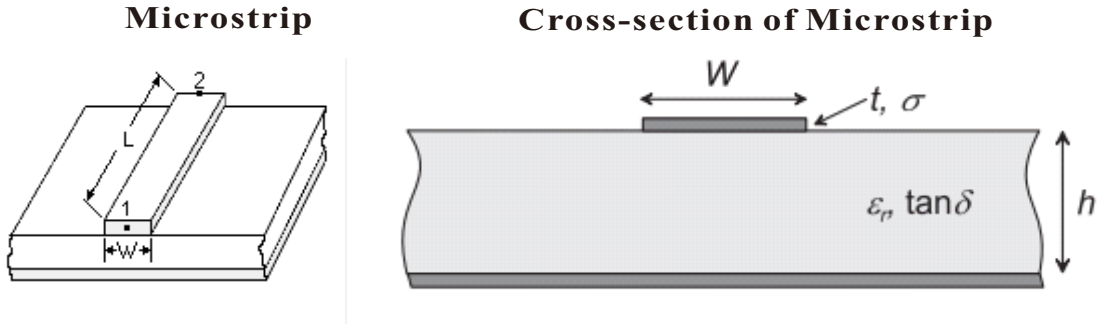

Figure 3.31: Physical structure of a microstrip line [8].

Unlike ideal transmission lines (TL), the microstrips are not completely lossless. There are some losses induced by microstrips. Unavoidable losses are classified into two types: conductor loss and dielectric loss. In theory, the losses are related to the impedance width. It is well known that the microstrip's ohmic losses decrease for increasing strip width, and are therefore large for high-impedance, narrow-strip lines [2]. Also, high impedance would lead to great electromagnetic radiation which could affect the PA's performance. Thus, to reduce potential losses, a wide transmission line should be avoided in the design.

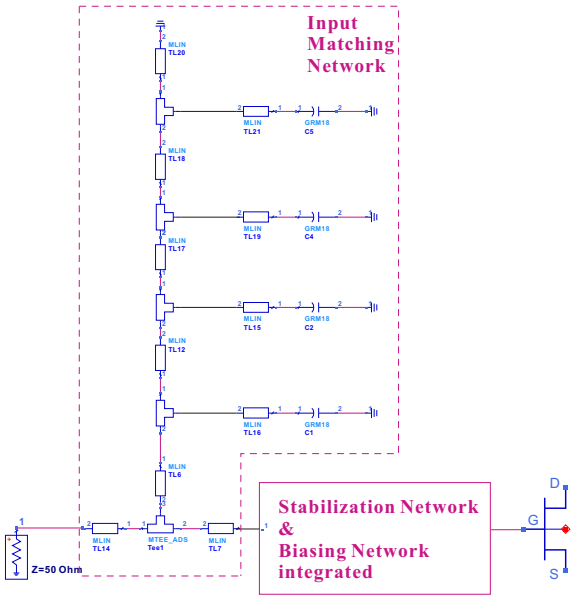

Figure 3.32: IMN implemented with microstrips.

The matching networks implemented in ideal TL are well optimized to realize the designed termination and reach the target performance. Based on that, the matching networks implemented in microstrip lines are applied the same topology (see Fig. 3.32 and Fig. 3.33) and define the dimension of microstrip lines based on the ideal one.

Different from the ideal one, the simple "short" in practice may have some impedance part existing, which is not ideal. A high-quality "short" in this network is realized by the recursion of the combination of TL and capacitor in this network. In this PA, this type of "short" implementation replaces the ideal one in the fundamental matching block of OMN, and also plays the role of the biasing block. Apart from this, microstrip T-Junctions are included in this schematic, which is introducing the effect of the parasitic on the PA. Therefore, the matching networks should be optimized.

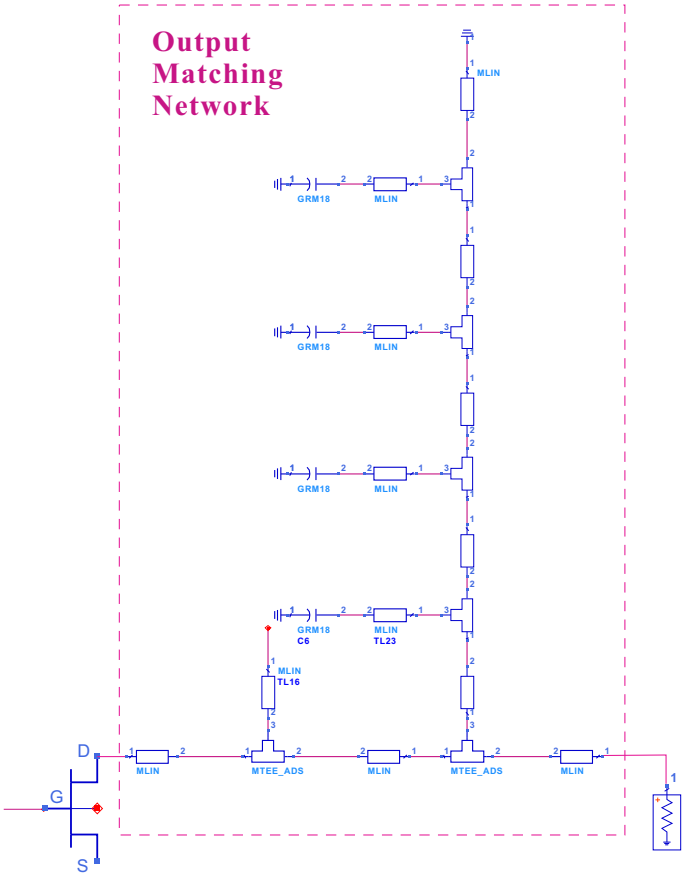

Figure 3.33: OMN implemented with microstrips.

The optimization results of IMN and OMN are shown in Fig 3.34 and Fig. 3.35, respectively.

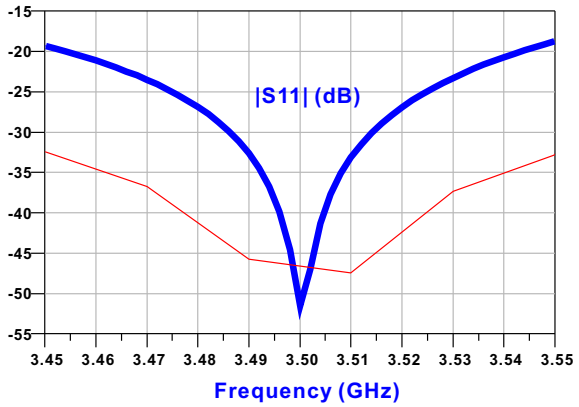

Figure 3.34: Comparison: IMN implemented with microstrip (blue) vs implemented with ideal TLs (red).

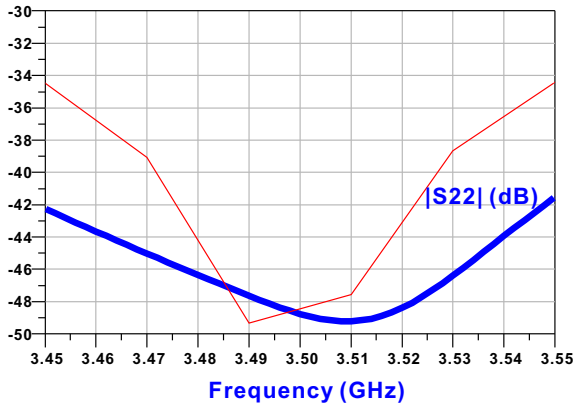

Figure 3.35: Comparison: OMN implemented with microstrip (blue) vs implemented with ideal TLs (red).

The S11 stays below -30 dB in the IMN simulation over the 3.45 GHz to 3.55 GHz band, and reaches below -45 dB in the center frequency. In comparison to the ideal, it is less match because of the loss and parasitic effect in the microstrips. However, after optimization, it performs well in that band. In the OMN simulation, the S22 maintains a level of less than -45 dB. The match from 3.45 GHz to 3.55 GHz is even better than the optimized one in the ideal TL.

Combining the optimized matching networks, the performance in one-tone and two-tone simulation is presented in Fig. 3.36 and Fig 3.37. respectively. These performances

are compared to the PA implemented with ideal TLs. Both of the circuits are biased, with V_{gs} = -3.15 V and V_{ds} = 30 V.

In the one-tone simulation, the Pout decreased by 1 dBm, this is expected due to the loss induced by the microstrips. And for the two-tone simulation, IMD3 keeps below -30 dBc, even the Pin increases to 24 dBm, which is better performed than the ideal one. The better linearity may account for better base-band control or the IMD3 cancellation in the circuit.

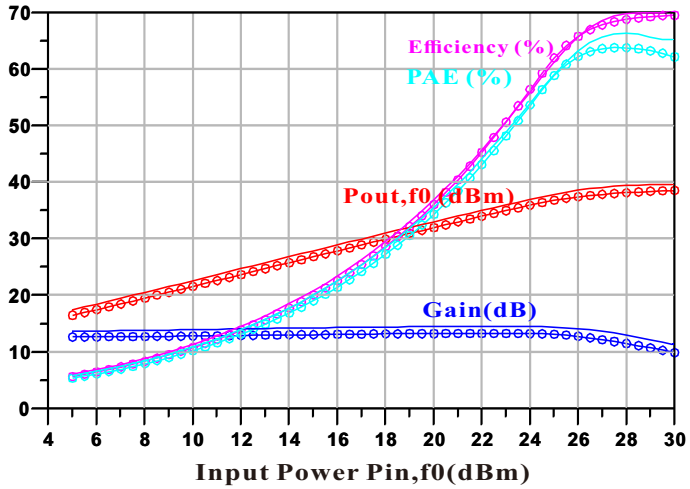

Figure 3.36: Comparison: the PA implemented with microstrips (symbols) vs implemented with ideal TLs (solid): one-tone simulation (biased with V_{gs} = -3.15 V and V_{ds} = 30 V).

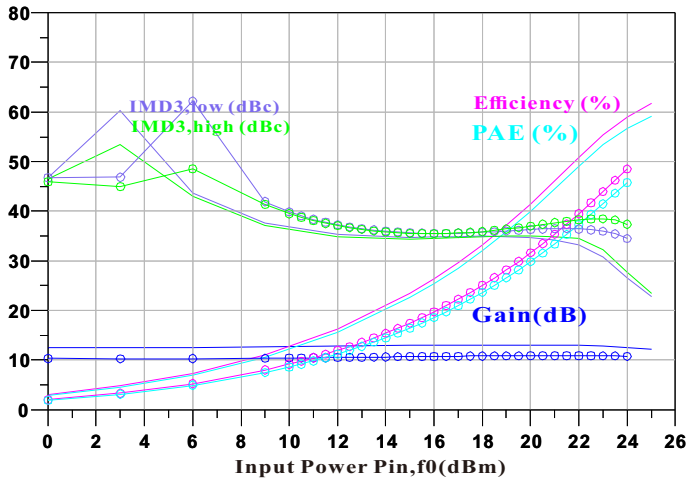

Figure 3.37: Comparison: the PA implemented with microstrips (symbols) vs implemented with ideal TLs (solid): two-tone simulation (biased with V_{gs} = -3.15 V and V_{ds} = 30 V).

However, as shown in Fig. 3.36, the Pout does not reach 36 dBm when the Pin is at 24 dBm. As a result, the biasing is adjusted to a higher V_{gs} = -2.8 V, resulting in a higher drain current and P_{out}.

Fig. 3.38 and Fig. 3.39 present the performance of the designed circuit after the biasing has been modified. In one simulation, the P_{out} exceeds 36 dBm. In the two-tone test, the target PAE is 41%.

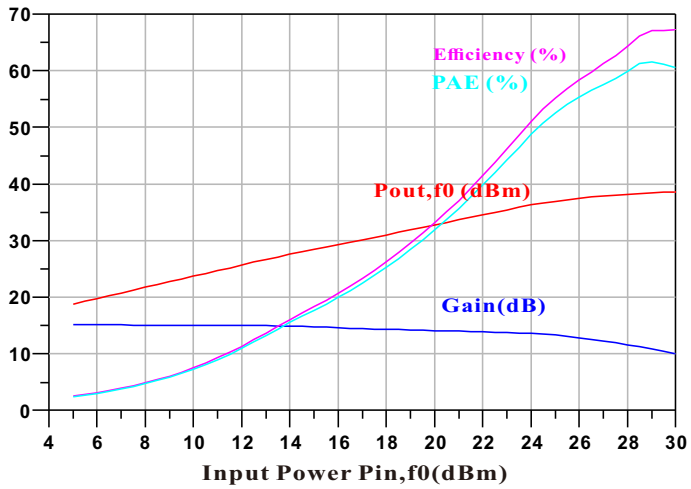

Figure 3.38: Biasing adjusted for satisfying P_{out} requirement: one-tone simulation (biased with V_{gs} = -2.8 V and V_{ds} = 30 V).

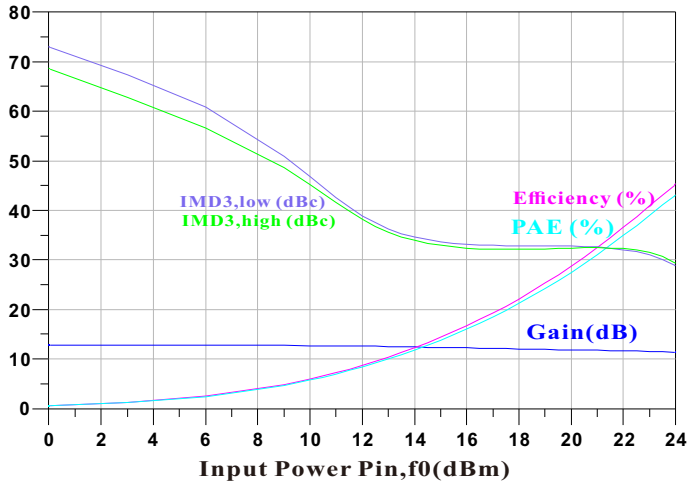

Figure 3.39: Biasing adjusted for satisfying P_{out} requirement: two-tone simulation (biased with V_{gs} = -2.8 V and V_{ds} = 30 V).

3.5.2 Layout and Electromagnetic Simulations

The layout is generated based on the schematic (Fig. 3.40). After the layout is created, an electromagnetic (EM) simulation of the circuit is conducted to obtain more precise results for the behavior of all amplifier parameters. EM includes and simulates electric and magnetic fields on circuits in order to provide results of interactions between different parts of the circuit that can change the predicted behavior.

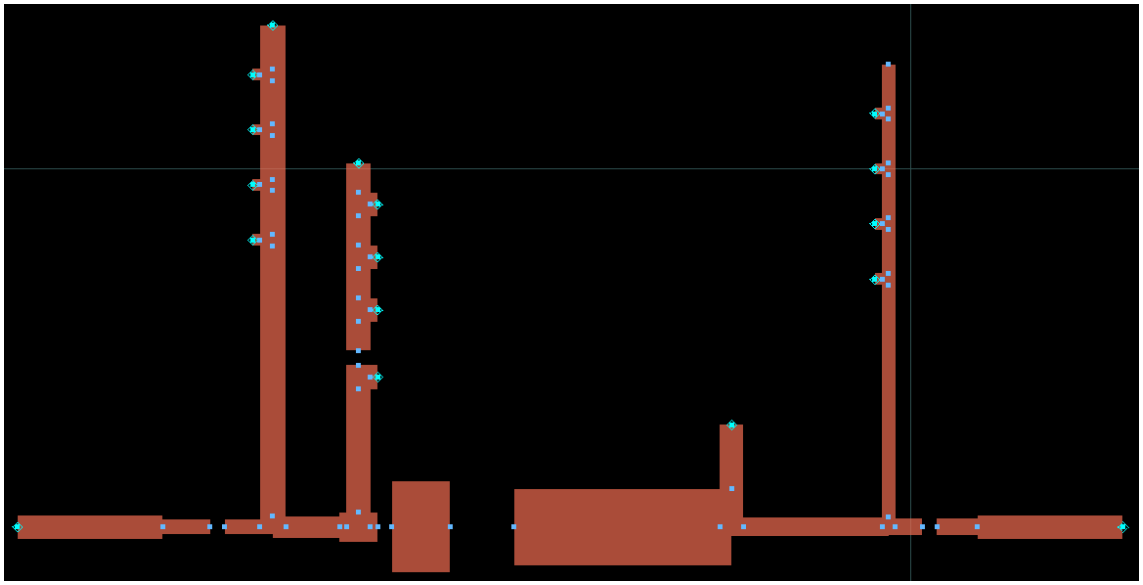

Figure 3.40: Layout of the input and output passive circuits, including matching, stabilization, and biasing networks.

Firstly, it is better to divide the problem by dividing the circuits into different parts and simulating each of them to fix any problems that may exist. EM simulation produces results for various parts that are simulated in terms of S-parameters, and this S-parameters network will be used in the circuit nonlinear simulation after the devices and lumped elements have been added. A final verification of the layout is made after PA optimized in EM simulation, achieving the desired results. The relevant performance of the designed PA, one with and one without the EM effect, is shown in Fig. 3.41 and 3.42.

In one tone simulation (Fig. 3.41), it can be observed that although the gain is compressed more after EM simulation, the P_{out} is in line with the performance of the one implemented in microstrip, reaches above 36 dBm when P_{in} = 24 dBm, satisfying the target P_{out}.

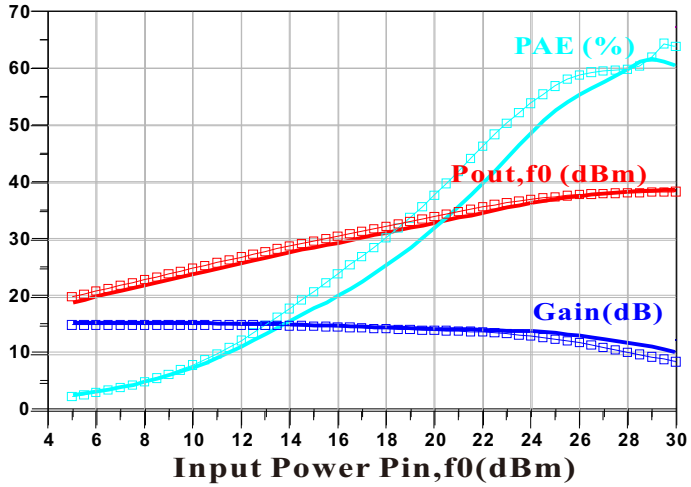

Figure 3.41: Comparison of one-tone performance simulated on the PA implemented in microstrip, without EM efforts (solid) with EM efforts (symbols) at 3.5 GHz.

For the comparison of two-tone performance in (Fig. 3.42), the PA optimized after EM simulation presents a bit better PAE, corresponding to the position where IMD3 is about to rise above -30 dBc. The fabricated PA is expected to have a PAE of 47%.

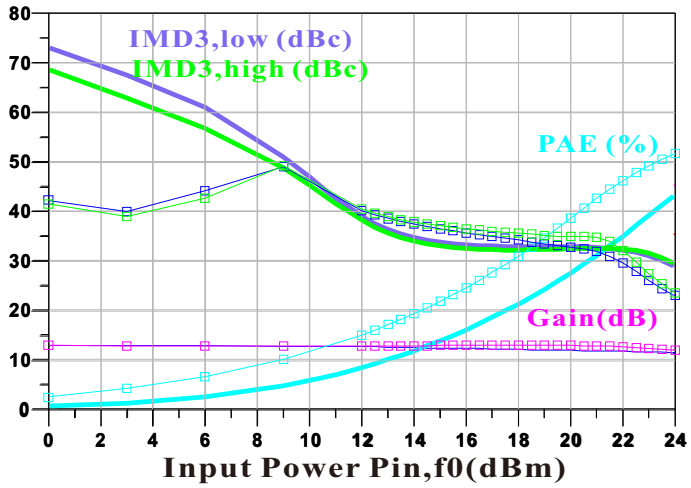

Figure 3.42: Comparison of two-tone performance simulated on the PA implemented in microstrip, without EM efforts (solid) with EM efforts (symbols) at 3.5 GHz.

The final layout is shown in Fig. 3.43

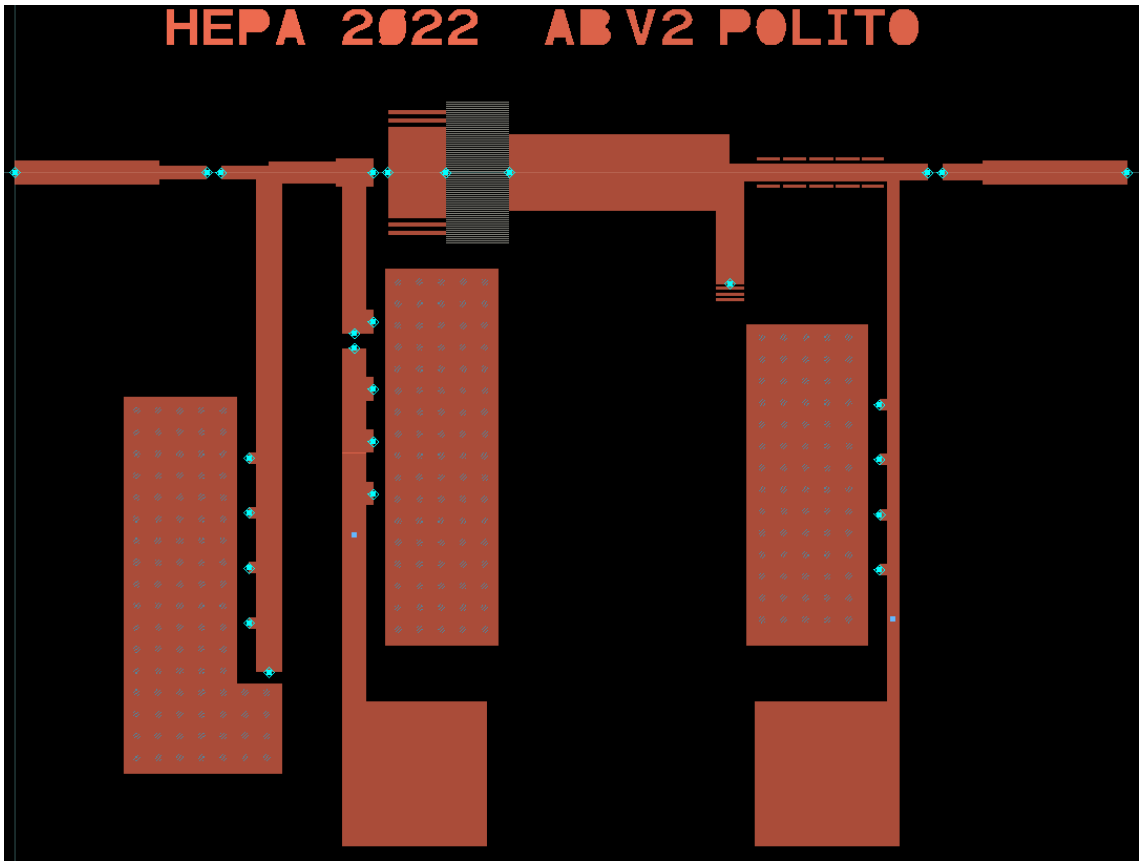

Figure 3.43: Final layout of the designed PA ready for manufacturing.

4 Measurements

The measurements are conducted to evaluate the practical performance of the fabricated PA. The amplifier has been characterized in small and large signal conditions. In the measurement, the selected bias point is V_{DS} = 30V, V_{GS} = −2.84V corresponding to I_{DS} = 35mA. In the simulation, the same drain current is obtained for V_{GS} = −3.1V.

4.1 Small Signal Measurements

The small signal performance is measured by adopting a bench based on a vector network analyzer (Keysight E8361A) in the frequency range 1 GHz to 6 GHz. The measurement result is illustrated in Fig. 4.1, where measured results (symbols) are compared to simulated ones (solid). The agreement is good apart from a 200 MHz shift towards lower frequency; S_{21} peaks at 3.3 GHz while input (S_{11}) and output S_{22} matching results better than 7 dB and 10 dB in a 500 MHz bandwidth, between 3 GHz and 3.5 GHz respectively.

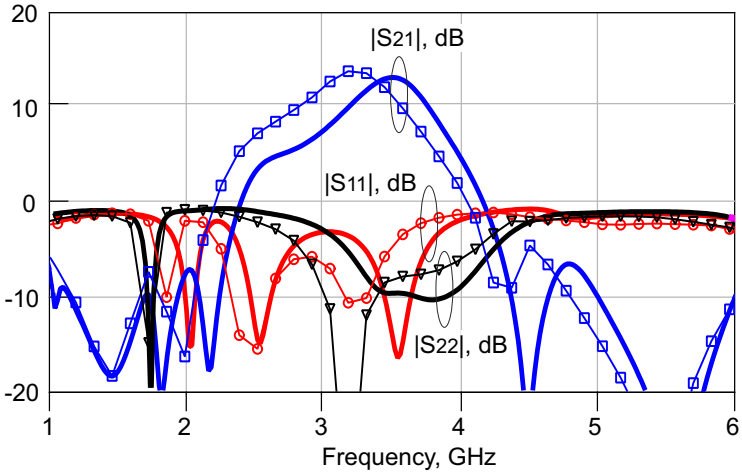

Figure 4.1: Simulated (solid) and measured (symbols) scattering parameters.

4.2 Large Signal Measurements

The large signal measurement is performed by a real-time vector test bench, calibrated using a 2-port Short-Open-Load-Thru (SOLT) routine, plus an SOL additional calibration at an extended output port connected to a power meter for the absolute power calibration [7]. The scheme of the measurement setup of the test-bench is illustrated in Fig. 4.2.

The simulated and measured continuous wave (CW) performance at the respective center frequencies is reported in Fig. 4.3. The comparison, once accounting for the center

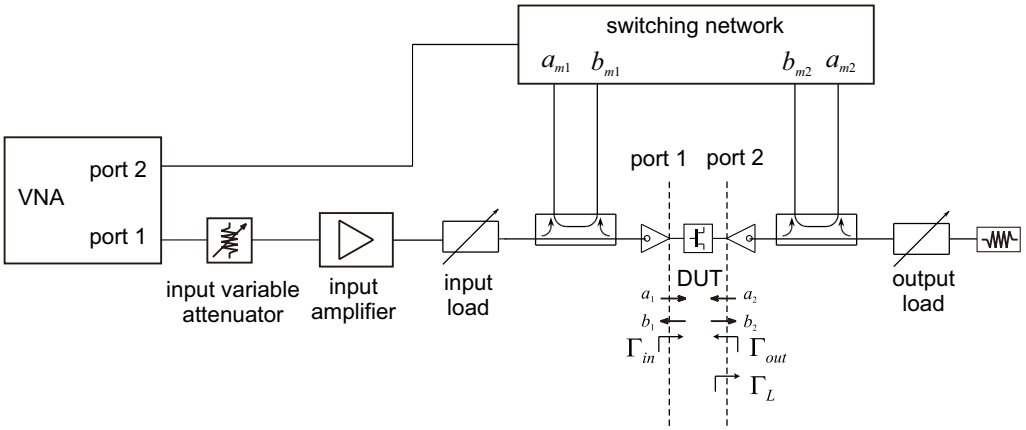

Figure 4.2: The scheme of the measurement setup of the test-bench.

frequency shift, highlights a very good agreement in terms of gain and output power, with a small difference only in terms of PAE, slightly higher in measurements (around 3%), due to a lower DC consumption. This may be due to the joint effect of a difference in the $2f_0$ termination and of lower losses in measurements as a result of the lower absolute frequency. At saturation (3 dB compression), the amplifier presents a power gain in excess of 10 dB, output power in excess of 38 dBm, and a PAE of 73%. At the target 24 dBm input power, the gain, output power, and power-added efficiency are 12 dB, 36 dBm and 60%, respectively.

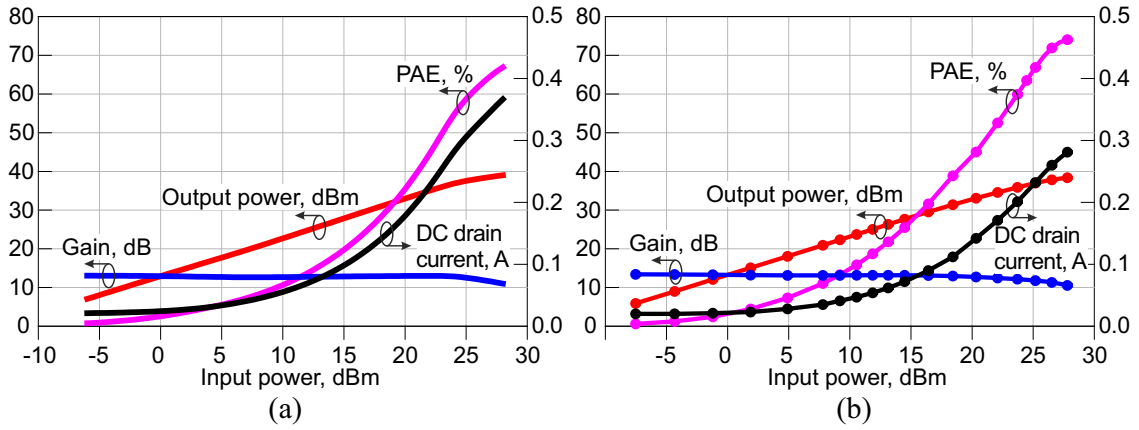

Figure 4.3: Comparison of CW single-tone performance at respective center frequencies: (a) simulated (solid) at 3.45 GHz and (b) measured (symbols) at 3.25 GHz.

The agreement over a 500 MHz band remains very well captured, as evidenced in Fig. 4.4. From 3 GHz to 3.5 GHz, the measured output power, gain, and PAE at saturation are higher than 36.5 dBm, 10 dB and 40%, respectively.

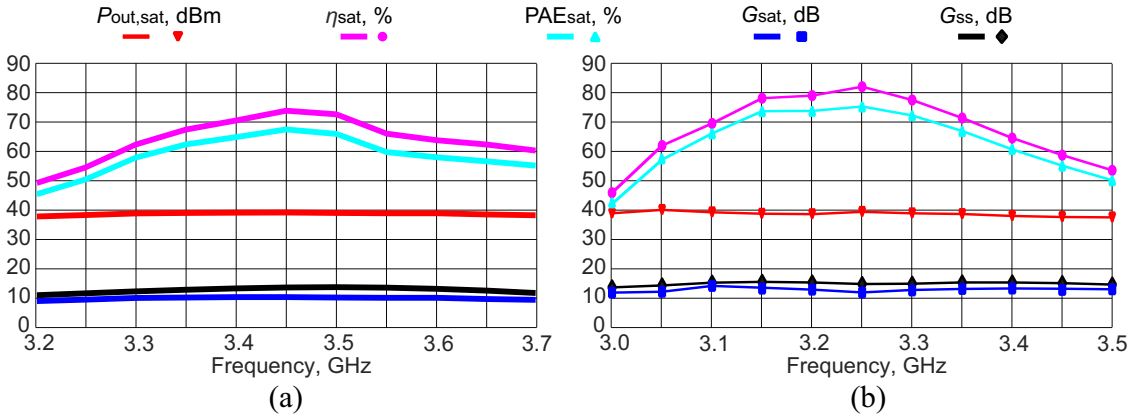

Figure 4.4: Comparison of CW single-tone performance versus frequency: (a) simulated from 3.2 GHz to 3.7 GHz and (b) measured from 3 GHz to 3.5 GHz.

4.3 Two-tone Measurement

Two-tone measurement is performed by adopting the bend described in the previous section, with the addition of a second microwave source frequency locked with the primary one. The absolute power is measured at the output with a spectrum analyzer, as shown in the scheme of Fig. 4.5.

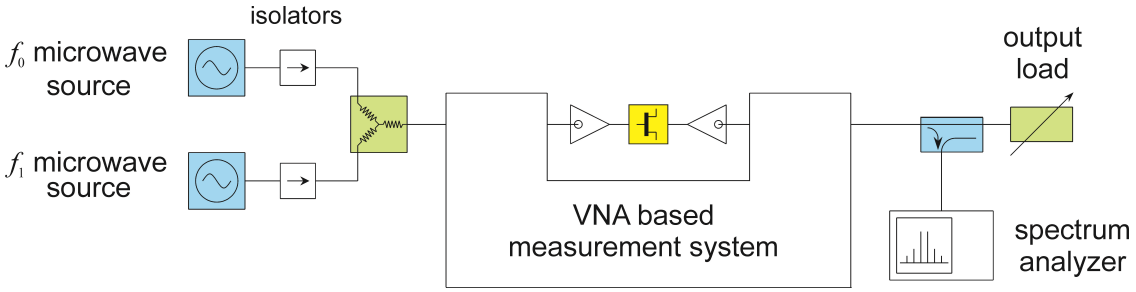

Figure 4.5: Scheme of principle of the characterization bench adopted for two-tone measurements.

Two-tone measurements with 20 MHz spacing have been performed in the range 3–3.5 GHz. The comparison between simulated and measured results at the respective center frequencies is reported in Fig. 4.6. Also in this case, the agreement is rather good. The output power, gain and PAE are accurately captured, as well as the IMD3 up to the position of the sweet spot (around 12 dBm input power). The main difference is visible in the IMD3 slope in the non-linear region, causing a faster drop in measurement than in simulation, which could not be fully compensated by adopting post-tuning of either bias point or matching networks. Around 3.25 GHz, the PA demonstrates a measured PAE of 33% at -30 dBc IMD3, while simulations predict a PAE of 45%. This, in turn, is

lower than the one observed in the load pull, due to the losses of the OMN as well as a slightly sub-optimal synthesis of the baseband and second harmonic terminations after bias point adjustments.

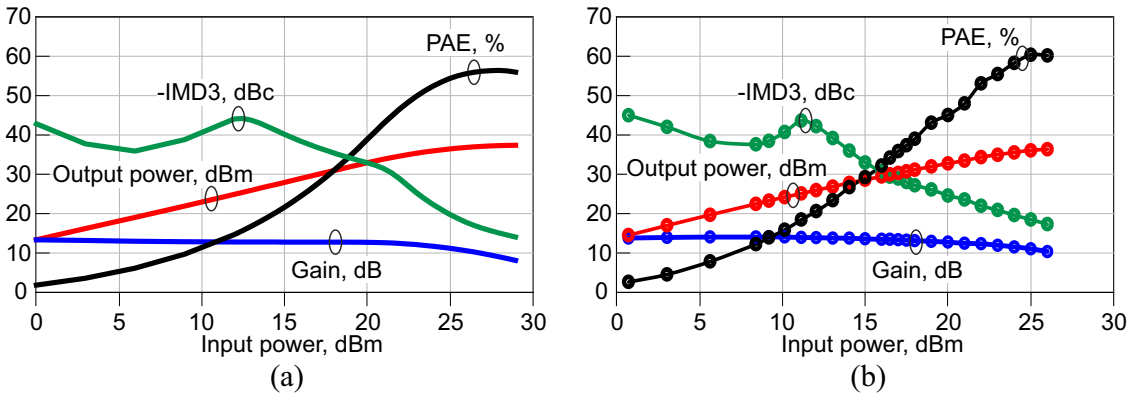

Figure 4.6: Comparison of two-tone performance at respective center frequencies: (a) simulated (solid) at 3.45 GHz and (b) measured (symbols) at 3.25 GHz.

5 Conclusion

This thesis presented the design, fabrication and experimental characterization of a medium-power single stage class-AB amplifier working around 3.5 GHz. The PA is optimized to maximize the performance of the HEPA competition of MTTs conference. In particular, the minimum output power to respect the competition requirements, the gain and the two-tone requirements are simultaneously controlled to achieve the best trade-off among them. In order to achieve the design goal proposed by HEPA, the optimum source and load terminations at base-band, fundamental, and harmonic frequencies are carefully selected. Considering the impact of electromagnetic effects not fully modeled at circuit level, full EM simulations are carried out on all the passive structures, evaluating the PA's expected performance. A prototype is manufactured based on a 6 W packaged GaN device.

The experimental results, in good agreement with their corresponding simulations, demonstrate the validity of the approach. The measured PA demonstrates a saturated PAE of 73% and 33% when satisfying the linearity target of -30 dBc highest IMDs.

As the follow-up work, different topologies, more effective design strategies and other possible advanced PA topologies would be investigated, with the goal of improving the performance of the PA and competing again in the student design competition of 2023.

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