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Investigation of retention and disturb of the BEOL engineered ferroelectric field effect transistors

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A mamma Antonella e
papà Carmine
a mio fratello Nicolò
a mio nonno Aldo
ai miei zii Giancarlo e
Angela
a mia cugina Chiara
e a chi ha creduto in me

Summary

Caused by the imperfect screening of polarization the Front end of line (FEOL) ferroelectric field effect transistor (FeFET) as non-volatile memory suffers from low data retention. The main mechanism behind is the depolarization field which counteracts the ferroelectric generated internal field and the back-switches ferroelectric dipoles degrading the memory performance. The FEOL FeFET gate stack is made of metal-ferroelectric-insulator-semiconductor (MFIS) and because of the absence of the metal electrode from semiconductor side it will provide an incomplete charge compensation and thus generating a finite depolarization field. An engineering of FeFET stack is proposed where the back end of line (BEOL) is suggested in which a floating conductive layer is sandwiched between the ferroelectric and insulator. In this thesis, specifically, the analysis of retention in the BEOL FeFET is simulated with GINESTRA modeling platform where metal-ferroelectric-metal-insulator semiconductor (MFMIS) gate stack is introduce to overcome the retention issue of the FEOL equivalent. The operation principles as well as the impact of ferroelectric layer's thickness and of the MFM and MFIS area ratio is investigated in order to optimize the advantage of combining a MFM capacitor on top of MIS FET to improve the memory performance of the device.

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Nothing great in the world was accomplished without passion

[Georg Wilhelm Friedrich Hegel]

Part I

First Part

Chapter 1

Introduction to the ferroelectric memories and its state of the art

1.1 Beyond CMOS

In 1965 Moore astonished the world of semiconductor technologies by showing a simple statistical and forethought law. The number of transistor in an integrated circuit doubles every $1.5 - 2$ years. For more than 50 years a new technological node come out to the market featured by the reduction of device dimensions, which benefits the integration density and enhance the performance of the device. As we're looking to the memory the concept of integration density is of relative importance. The more we could shrink down the device dimension the more the amount of data we could store in the memory. The performance of the device, indeed, was drastically influenced by the end of the Dennard scaling, often called constant-field scaling. Before 2006 the improvement of integration density, cost per device and clock frequency were in the same direction: *exponentially increasing*. From the 65nm node due to the reduction of dimension the current leakage and as a consequence the higher power dissipation, thermal runaway, limited the amount of frequency operation repressing the scaling trend. In the meanwhile the transistor went to geometrical scaling (1975-2000s) toward the equivalent scaling (2000s-2025) in which new materials where introduce like the replacement in the metal-oxide-semiconductor field effect transitor (MOSFET) of the silicon oxide with high κ dielectric, the substitution of polySilicon with a metal gate and the improvement of mobility with strained Si. Last but not least starting from the 22nm node (2011) the 3D MOSFET (FinFET), not a planar transistor but a vertical structure which benefits a better electrostatic control of the channel at reduce gate length, revolutionaries the manufacturing process of the semiconductor industry. Few years later in 2013 the International Road-map for Devices and Systems (IRDS) introduced for the first time the concept of *Beyond CMOS* as the next road in which the semiconductor technologies is going to face once the CMOS scaling comes to an

end. The *Beyond CMOS* explores emerging architecture, devices, technological processes, material with the scope of providing a completely new computational paradigms. Memories devices are in these sense the most studied due to scaling limit of NAND FLASH memory and DRAM, the two most predominant type of memory on the Semiconductor Memory Market. Both of them are charge storage devices which suffer from the related scaling. By shrinking down the dimension the amount of charge stored is reduced impacting the retention capability and in case of memory array the sensing of data due to the electrostatic interference of neighbouring cell and/or the leakage current when performing a reading operation. The requirement of new computational model far from the charge based rise the technological and physical study towards the new emerging memory, fig.1.1. The most investigated in the literature are the magnetic memory, oxide-based resistive

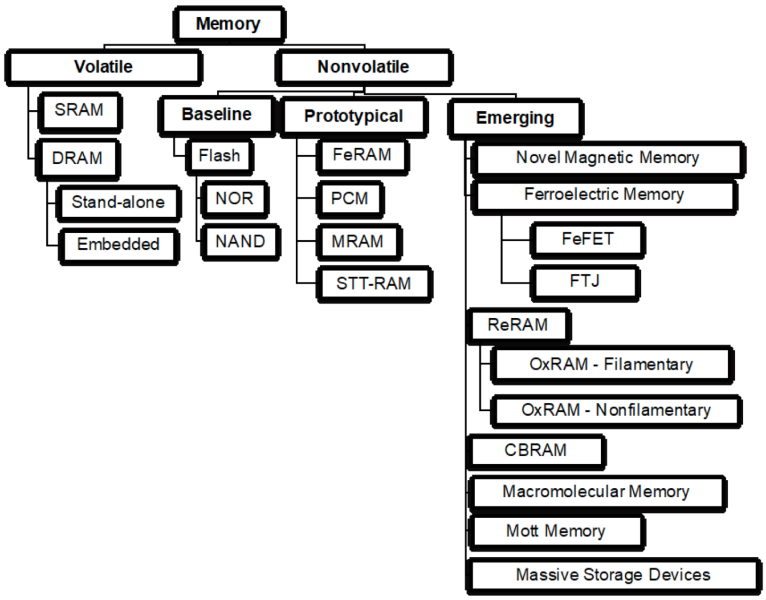


Figure 1.1: Taxonomy of emerging memories devices

memory, phase change memory and ferroelectric memory.

- Magnetic memories are based on the *giant magnetoresistance effect* (GMR), a change in electrical resistance observed when measuring the current flows between two magnetic layers (fixed and free layers) separated by a thin dielectric. According to the magnetization of the free layer with respect to the fixed one a change of tunneling current is retrieve, in particular, higher when parallel magnetization and lower if anti-parallel. The advantages are the non-destructive reading, long data retention and high endurance while the large cell size and the small current ratio are the two major drawbacks.

- In the oxide-based resisistive memory the oxygen ion transport modulates the formation of a conductive path modifying the resistance of the material. The drawback

is the current in the off (reset) state, once the filament is broken, which could different due to cell to cell variability and due to an increase of cycling condition with respect to the initial I_{OFF}. The pro is in the switching behavior as either uni-polar switching, set and reset on the same polarity, or bipolar switching, set and reset of different polarity, exist. Their main application is on high density data storage.

- Another resistive based memory device is the phase change memory where the material modify its phase from amorphous, high resistance state, toward its crystalline phase, low resistance, due to the increase of temperature. The main drawback is the highly temperature dependence and the related thermal disturb among neighbour cells. The advantage resides in the unipolar feature by which a high voltage for a sufficient short time lead the device to the set state (crystalline phase) and small amount of voltage in a long time range toward a reset state (amorphous phase).

- Ferroelectric (FE) memories use the polarization of the ferroelectric material induced by the application of an external field to store data. Three different kind of ferroelectric memory are under investigation as a feasible replacement to the Flash memory: ferroelectric RAM (FERAM), ferroelectric field effect transistor (FeFET) and ferroelectric tunnel junction (FTJ). Before the discovery of ferroelectricity in HfO_2 the major limit of the ferroelectric memory was in terms of scaling. Ferroelectric RAM, the first FE memory to be commercialized in the late 1990s, suffers from scaling due to the reduced amount of charge that the FE material could stored and going beyond the 100nm node was barely feasible.

Having define the key features of each emerging memory a significant aspect is on the technological process which are need to be careful evaluated such that the new material and/or process condition in which the devices work is compatible with the CMOS platform technology. A huge and intensive study is held in order to establish and develop the electrical behavior of the device. Once the comparison of the emerging memory properties with the benchmark Flash memory are measured, specifically the energy consumption, writing/reading time, cell area, the endurance and data retention (to cite one of the most relevant), it becomes than feasible or not the introduction to the memory market.

1.2 Ferroelectricity in hafnium oxide

1.2.1 The introduction of hafnium oxide in the CMOS fabrication process

Before introducing the ferroelectric memory in details a brief introduction to the role of hafnium oxide is needed. In 2007 Intel introduced for the first time ever a high κ dielectric material as a technological solution for the minimization of the leakage current encountered when scaling down the transistor. Starting from the 45nm node (2010) HfO_2 replaced the Silicon oxide in the MOS structure. The reduction of gate oxide increases the gate current in an exponential way degrading the performance of the transistor. The solution was found in HfO_2 characterized by a high dielectric constant (almost 6 times

higher than SiO_2) and at given oxide capacitance it could guarantee an equivalent oxide thickness higher than the SiO_2. This will mitigate the problem of gate tunneling current while scaling: reducing the power consumption and increasing the performance of the device.

1.2.2 The advent of ferroelectrics

Before 2011 in the field of material science the inorganic compound HfO_2 was known to exist, at normal pressure, in three different crystal structure: monoclinic (at room temperature), tetragonal (above $2050K$) and cubic (above $2803K$). In addition when the material decreases its dimension from bulk toward thin film, and the size-dependent and surface effect became more significant as we're dealing with nano-scale dimension, it was reported the stabilization at room temperature of the tetragonal phase in spite of the monoclinic one. As the polymorphs of HfO_2 are not characterized by a non-centrosymmetric phase it sounds like a big deal the discovery of ferroelectricity in hafnium oxide. We can start by considering a simple structure made of HfO_2 sandwiched by two metal electrode. The turning point in the scientific community as we have already mentioned comes from *Boscke*[7] which demonstrate for the first time ever the stabilization in hafnium oxide of a non-centrosymmetric phase with a formation of permanent polarization dictated by the displacement of atoms from their symmetric position. Two dominant feature brings its formation: doping content (Si is favoured as it help to stabilize the tetragonal phase in thin film hafnia) and capping mechanism. The first hallmark is achieved by metal organic atomic layer deposition process (Tetrakis-(ethylmethylamino)-hafnium also called TEMA-Hf, Tetrakis-dimethylamino-silane also named 4DMAS, metalorganic precursors and ozone are the material selected) in which the concentration of Silicon is varied by adjusting the cycle ratio of 4DMAS and metalorganic precursors. The second distinctive feature regards the capping mechanism and compare with the doping concentration it's the most dominant in terms of formation of ferroelectricity. It was reported that if the deposition of top metal electrode (by chemical vapor deposition) is implemented before the crystallization of the $Si-HfO_2$ then the hafnia diffraction pattern, acquire by the Grazing Incident X-Ray Diffractograms (GI-XRD), report peaks which best fit with the diffraction patter of a meta-stable orthorhombic phase responsible for the ferroelectricity behavior of the HfO_2. How is conceivable to have a new stable phase when the metal electrode is deposited after (capped sample) and not before (uncapped sample) the crystallization of hafnia? In the uncapped sample the dielectric undergo a transition from tetragonal toward monoclinic phase but this transition seems to be suppressed in the capped sample. The reason is related to the presence of the top metal electrode which inhibit the shearing of the unit cell and make attainable the formation of a meta-stable orthorhombic phase, hence ferroelectricity in hafnium oxide is observed. It's indeed relevant to properly emphasize the role of Silicon as changing the composition, molecular percentage ($mol\%$), inside the dielectric lead to a modification of the polarization hysteresis curve. The P-V characteristic shows a gradual transition from a ferroelectric (FE) phase toward antiferroelectric (AFE) phase hafnium oxide, specifically considering a $8.5nm$ of hafnia and a depostion temperature ofTiN electrode of $500°C$ and a post-metallization-anneal (PMA) of $1000°C$ for $20s$, above $2.6mol\%$ FE behavior is observed whereas above $4.3mol\%$ AFE

behavior dominates.

1.2.3 The key aspects that stabilize the ferroelectricity in hafnium oxide

Three main factor influence the stabilization of ferroelectricity in hafnia: the post-metallization-annealing, the thickness of hafnium oxide and the dopant concentration (common element are Silicon, Gadolinium and Zirconium), fig.1.2. It's verified in [8] that an increase in tem-

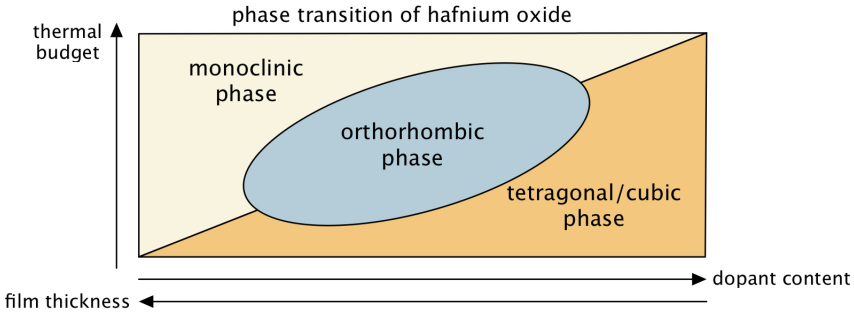


Figure 1.2: Phase transition of hafnium oxide influenced by the post metallization annealing, film thickness and doping concentration

perature in the PMA lead to a transition towards a monoclinic phase; same trend if the thickness of the dielectric increases. It is demonstrated that crystallization temperature drops for thicker film as less orthorhombic phase and more monoclinic phase are presented. Increasing dopant content may lead to the formation of ferroelectric film but the kind of dopant element used and the size of film are critical factors which could bring the hafnium oxide toward the cubic and/or tetragonal phase if the dopant concentration increases. In fig.1.3 it's illustrated the decreasing of remnant polarization when the film thickness increases for different dopant. Different factors need to be included like the increase of monoclinic phase with thickness, the deposition temperature of top metal electrode which could be closer to the crystallization temperature of the doped hafnia or the crystallization of thicker film which start during the electrode deposition process. Recalling fig.1.2 there is a trade-off concerning the stabilization of the orthorhombic phase from doping content and the type of dopant element toward the film thickness and last but not least to the annealing temperature providing substantial structural changes and/or chemical reaction leading to the formation of monoclinic phase and or the formation of interfacial layer due to oxygen scavenging in the TiN electrode. This last process can poses several issue regarding the endurance test of FE based HfO_2 devices since the material requires an initial cycling step before entering into the wake-up phase (10^3 cycles) where an opening of the pinched hysteresis loop is observed. For further analysis on the field cycling behavior of hafnia see the appendixA.

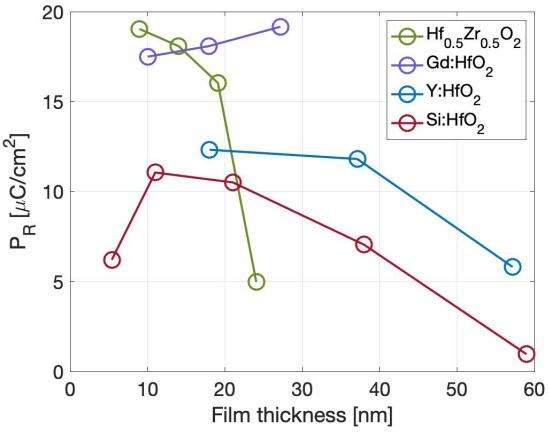


Figure 1.3: Remnant polarization as a function of film thickness for different dopants. Data taken from [3]

1.2.4 Hafnium oxide vs common perovskite material

We can know be question why the hafnium oxide has altered dramatically the scientific community on the role of ferroelectric memories. To answer we report in the table1.1 a comparison between the two old common perovskite material, knowing for their ferroelectric properties since 1990s, and the HfO_2. The low film thickness compared with PZT and SBT make it suitable for scaling with a stable atomic layer deposition capability and CMOS and BEOL compatible beside the controllable thermal budget require to stabilize the orthorhombic phase. Beside the remnant polarization the role of the coercive and breakdown field is critical for the reliability of the ferroelectric based devices. A notable figure of merit in ferroelectric devices is the concept of memory window (MW). When discussing the FeFET we will associate the MW to the threshold voltage of the transistor when subject to different writing voltage. Despite that another method to evaluate the MW accounting simply on geometrical and material properties is described in(1.1)

$$MW = 2 \times E_C \times t_{FE} \tag{1.1}$$

with E_C indicating the coercive field and t_{FE} the thickness of ferroelectric material. To achieve a memory window closer to the ferroelectric HfO_2 the perovskites which have a lower E_C necessitate higher film thickness make them not suitable for the nano-meter range integration. Let's make an example: in order to achieve a $MW = 2V$ in FE HfO_2 considering a $E_c = 1MV/cm$ a $10nm$ thickness is required whereas for SBT, considering the best case of $E_c = 100kV/cm$, then $100nm$ is the requirement. It might be relevant to point out that before its advent the application of ferroelectric as memory devices was limited toward the 90nm process node which means reach a death end point for the industry. The introduction of hafnium oxide has completely reshaped the evolution of the ferroelectric devices in the last decades. Anyway the advantage of high E_c field for HfO_2 is counterbalanced by the breakdown field (E_{BD}) which is characterized by the same order of magnitude of the coercive field. Despite for the perovskite where the ratio E_c/E_{BD} is

	$SrBi_2Ta_2O_9$ (SBT)	$Pb(Zr_xTi_{1-x})O_3$ (PZT)	FE-HfO_2
Film Thickness	$> 25nm$	$> 70nm$	$5 - 30nm$
Annealing Temperature	$> 750°C$	$> 600°C$	$450°C - 1000°C$
P_r	$< 10\mu C/cm^2$	$20 - 40\mu C/cm^2$	$1 - 40\mu C/cm^2$
E_c	$10 - 100kV/cm$	$\sim 50kV/cm$	$1 - 2MV/cm$
E_{BD}	$\sim 2MV/cm$	$0.5 - 2MV/cm$	$4 - 8MV/cm$
$E_C/E_{BD} \times 100$	$0.5 - 5\%$	$2.5 - 10\%$	$12.5 - 50\%$
κ	$150 - 250$	~ 1300	~ 30
ALD capability	limited	limited	mature
CMOS compatibility	Bi and O_2 diffusion	Pb and O_2 diffusion	stable
BEOL compatibility	H_2 damage	H_2 damage	stable

Table 1.1: Comparison of FE HfO_2 and the common perovskite ferroelectric from[1]

lower than 10% in hafnium oxide can even reach 50% indicating the limited endurance for the HfO_2 based devices.

1.3 Ferroelectric memories

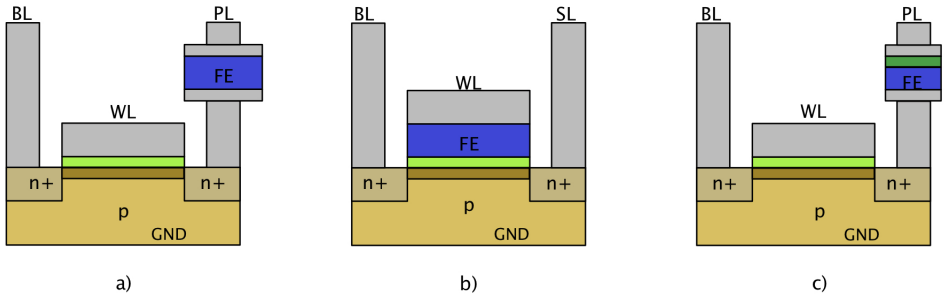


Figure 1.4: Device cross-section of the three different ferroelectric memory devices: FeRAM, FeFET and FTJ

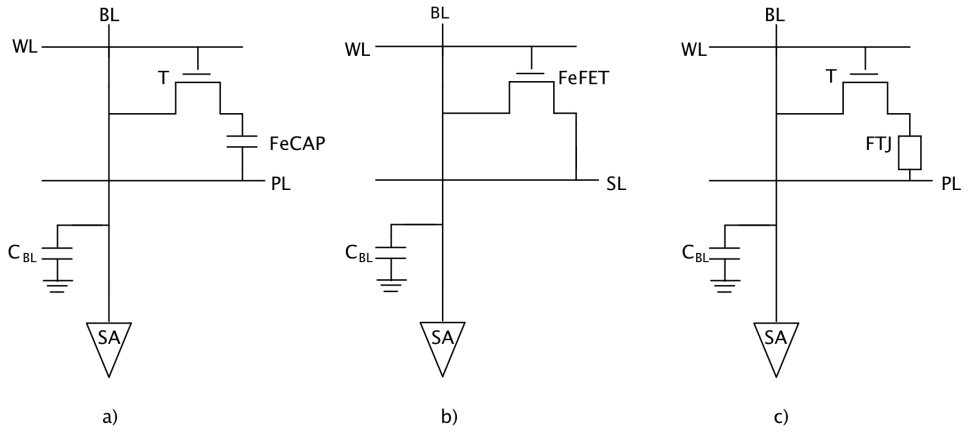


Figure 1.5: Equivalent circuit of the three different ferroelectric memory devices: FeRAM, FeFET and FTJ

1.3.1 Ferroelectric Random Access Memory

Ferroelectric RAM, device and circuit model in fig.1.4a and fig.1.5a, was the first to be commercialized in the late 1990s. A ferroelectric capacitor (FECap) and a transistor are connected in series in what is called 1T1C storage cell design. To write a logic 1/0 or to read the cell both the word line (WL) and the pulse line (PL) are pulsed simultaneously. As in the DRAM case the read is destructive as it can either leaves the polarization unchanged or flip partially the ferroelectric dipoles which result into a transient current that charges the bit line capacitance. The sense amplifier is used to amplify the change of voltage detected. In eq(1.2) the difference of the bitline voltage when the state is 0 and 1 is evaluated.

$$\Delta V_{BL} = \frac{2 \cdot P_R \cdot A_{FE}}{C_{BL}} \tag{1.2}$$

The remnant polarization P_R play a significant role in modifying the amount of bitline voltage that is amplified by the SA. The major concerns in terms of reliability of the devices comes from endurance test as the field cycling behavior of HfO_2 is featured by a wake-up phase and fatigue condition which limit to 10^9 number of cycles. A 2T2C cell can potentially mitigate the previous effect where not only the signal is double but also the degradation in terms of cycling is very alike; the main disadvantage is the increase of cell size: twice with respect to 1T1C.

1.3.2 Ferroelectric tunnel junction

The operation principle of the ferroelectric tunnel junction (FTJ) is the modulation of the tunneling current through the polarization direction of the ferroelectric material. Once the polarization is assessed the different potential profile of the device can either inhibit or enhance the tunneling current providing respectively the "0" and "1" state. Differently to the ferroelectric RAM the reading can be detected non-destructively due to the tunneling

current which identifies the direction of the polarization. Beside the similar structure with the FeRAM, fig.1.4 c, the first demonstration of the FTJ was in 2009, almost 20 years later than the first commercialization of FeRAM. The limiting factor which confines the FTJ at research level is the complexity in obtaining ferroelectric thin film beside a well-know understanding of the physics behind the switching of the polarization and of tunneling electroresistance effect (TER). The last term indicate the modification of the tunneling current dictated by the polarization reversal of the ferroelectric layer whose understanding is still under debate.

1.3.3 Ferroelectric field effect transistor

In 1974[9] the first ferroelectric transistor based on perovskite material (SBT) was made of. The gate stack was a little bit different to the modern FeFETs as it lack of the insulating layer between the ferroelectric and semiconductor. The operation principles indeed remain unchanged: the conductivity of the semiconductor region is modulated by the polarization charge present in the ferroelectric region. Why this structure metal-ferroelectric-semiconductor (MFS) was abandoned? Mainly for technological issue as inter-diffusion of element and chemical reaction at the ferroelectric-semiconductor interface are common. As shown in table1.1 lead and oxygen for PZT diffuse in the Silicon substrate as well as bismuth and oxygen for SBT. Their inclusion will modify the surface channel as the presence of heavy metal alters the properties of the device with the alternative drawback of creating a thin layer at F-S interface of poor electrical quality.

What happens for the hafnium oxide replacement of perovskite material? Beside the high band gap and bad offset which enable low leakage current even for nm size film thickness the formation of silicides and silicates(down to 800° annealing)[10] at the F-S interface is the one of the two main issue which have limited the fabrication of MFSFETs. Nowadays the FeFET is made of metal-ferroelectric-insulator-semiconductor gate stack and in 2016 GlobalFoundries has successfully carried out the implementation of hafnium-oxide FeFET embedded non-volatile-memory (NVM) into a 28nm gate first super low power CMOS technology platform[11].In fig.1.4b the device cross section and fig.1.5b the circuit level of the MFIS FeFET. By applying high voltage on the gate electrode the direction of the polarization can either promote the inversion region or the accumulation region. In such a way the threshold voltage is controlled by the polarization inside the ferroelectric material. Specifically considering a p-type channel when the device is set to program (PRG) the positive potential on the gate generate a polarization pointing downward which attract minority carriers close to the semiconductor-insulator interface, fig.1.6. Due to the action of the polarization the threshold voltage is at low potential, low-V_{th} ($V_{th_{PRG}}$). Contrarily when the polarization points upward the accumulation region (holes) is favoured shifting the threshold voltage at higher potential, high-V_{th} ($V_{th_{ERS}}$). The memory window, a powerful figure of merit in ferroelectric field effect transistor, is defined by the difference of the two threshold values

$$MW = V_{th_{ERS}} - V_{th_{PRG}} \tag{1.3}$$

Another simplified version is found between the memory window and the flat band voltage. Let's consider an ideal MFIS gate stack with work-function of metal equals to the

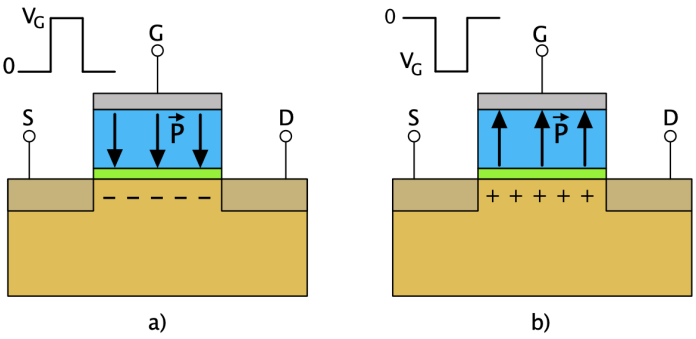


Figure 1.6: Write operation for the FeFET. a) for positive gate voltage the polarization of the ferroelectric is providing the attraction of minority carriers (electrons): low-V_{th}. b) for negative gate voltage the ferroelectric polarization points upward attracting majority carriers (holes): high-V_{th}

semiconductor and look at the flat band condition. In this condition the conduction and valence band are flat whit the consequence that the charge carriers are not influenced by any electric field, meaning that the every capacitor charges of the stack is zero. In ferroelectric the state in which the charge is 0 is verified only when the voltage is equal to the coercive field $V_{C\pm}$ values.

$$MW = V_{C+} - V_{C-} \approx 2 \cdot V_C = 2 \cdot E_C t_{FE} \approx \Delta V_{FB} \approx \Delta V_{th} \tag{1.4}$$

The result shown in eq(1.4) justify the eq(1.1) used to highlight the role of hafnium oxide in enabling a higher memory window due to the higher coercive field values (1.2.4).

1.4 Toward the BEOL FeFET

When dealing with memory devices the main concern is related to endurance and retention test. Considering the FEOL FeFET the charge trapping and dielectric breakdown field are responsible for the low endurance of the device in the range of $10^4 - 10^6$ cycles [12]. The impact of the charge trapping is correlated to the polarization switching which can substantially modify the trans-characteristic of the FeFET[13]. For instance as the negative gate voltage provide the polarization to point downward this can promote the hole injection through the ferroelectric layer. As a consequence a shifting of the threshold voltage is obtained with the results of shrinking the memory window by increasing the number of cycles. The second cause is related to the high electric field across the dielectric layer when the device is either in program or erase condition. This provokes the band bending of the interlayer which could enhance the injection of electrons and holes from the channel through the gate stack. The outcome is the screening of the modulation of the surface potential by the ferroelectric polarization because of the reduce amount of switching domains dictated by the increasing of trap density. On the other side when dealing with the ability of retain data the ferroelectric FET suffers from the same charge trapping

as described before and the depolarization field [14]. Because the depolarization field is present due to the partially (not fully) compensation of the polarization charge due to the neighbour dielectric and semiconductor layer in the MFIS gate stack, we propose a new architecture in which the ferroelectric is sand-witched between two metal layers in what is called: the back end of line FeFET. The metal-ferroelectric-metal-insulator-semiconductor gate stack (MFMIS) featured by the top and bottom metal layer between the ferroelectric material can guarantee the complete compensation of the polarization charge improving the retention of the device. Moreover the following structure could be beneficial for providing an increase of endurance cycles as well. By inspecting the Metal-Ferroelectric-Metal stack it was verified in [15] a switching cycles endurance up to $4 \cdot 10^{10}$. In the thesis we provide the *investigation of retention and disturb of the BEOL engineered ferroelectric field effect transistors*. As two different model at simulation level are employed to simulate ferroelectricity we discuss in chapter2 the Preisach and Ginzburg-Landau theory. Ginestra simulation software, chapter3 is our modeling framework where we're going to analyse the behavior of the BEOL FeFET and compare it with the FEOL FeFET. Chapter4 will be dedicate to the study of the depolarization field when the ferroelectric and dielectric layer are featured by different area and finally chapter5 where we highlight the main outcomes from Ginestra software.

Chapter 2

Modeling ferroelectricity

In this section a detail analysis of ferroelectric model is given with some mathematical formulation used to simulate the hysteresis behavior. We start with the Preisach model and given the value of coercive field, remnant polarization and saturation polarization, easily acquired from experimental result, it's possible to characterised the polarization vs electric field curve. We move then to the Landau theory describing the behavior of a system in equilibrium near phase transition. We will introduce the concept of Landau coefficient and link them to the Preisach parameter in order to draw the hysteresis curve. At the end we will introduce the ferroelectric model used in GINESTRA software: Preisach and Landau but a detail analysis will be given to account for physical aspects not mentioned before.

2.1 Preisach model

Preisach hysteresis introduced in 1935 by *Ferenc Preisach* was suggested to describe hysteresis behavior observed in the magnetization versus magnetic field of a magnetic material. It was expanded towards other field where the hysteresis behavior was defined including the case of ferroelectric material. The mathematical model is discussed considering the articles of [16] and [17]. Eq(2.1) describe the hysteresis operator with P value set to ± 1 once E overcome the two limit β and α defining the negative and positive coercive field values. The k parameter keep track of the history behavior which means that if E was previously lower than α than is set equal to -1 (set to 1 if it was previously higher than β). As Preisach model considers macroscopic system then we could think of dividing our entire ferroelectric material into parallel and independent unit each features by an hysteresis operator with different values of negative and positive coercive fields.

$$P(E) = \begin{cases} 1 & \text{if } E > \beta \\ -1 & \text{if } E < \alpha \\ k & \text{if } \alpha < E < \beta \end{cases} \tag{2.1}$$

Having define the first building block of Preisach model, usually defined as $\hat{\gamma}_{\alpha\beta}$, it remains to consider the distribution of coercive fields as a second parameter $\mu(\alpha, \beta)$ determined

by experimental data. The total polarization is given by eq.(2.2)

$$P(t) = \iint \mu(\alpha, \beta)\hat{\gamma}_{\alpha\beta}E(t)\mathrm{d}\alpha\mathrm{d}\beta \tag{2.2}$$

Because of its double integral evaluation with the determination of $\mu(\alpha, \beta)$ and its consequence evaluation of parameters at microscopic level makes it hard to correctly employ at least computationally. A correct fitting between the experimental result and the model was achieved by the hyperbolic tangent which involve just few parameters to model the hysteresis behavior of the ferroelectric material. Defining by $P^+(E)$ the positive branch of the hysteresis curve and with $P^-(E)$ the negative branch then an easy-going mathematical model for hysteresis curve is shown in eq.(2.3)

$$P^{\pm}(V) = P_S \tanh\left[a(E - E_{C^{\pm}})\right] \tag{2.3}$$

with P_S indicating the saturation polarization and E_C the coercive field. In [4] an almost similar expression was derived to simulate the polarization versus electrical field (P-E) behavior with the parameter a defined in eq.(2.3) which is now dependent on the saturation polarization and remnant polarization (P_R), making the following equation more easily to implement. The dipole polarization (P_d) as a function of the electrical field is expressed as

$$P_d^+(V) = P_S \tanh\left[\frac{(E - E_C)}{2\delta}\right] \tag{2.4}$$

with the parameter δ which is defined by setting $P_d^+(0) = -P_R$

$$-P_R = P_S \tanh\left[\frac{-E_C}{2\delta}\right] \tag{2.5}$$

From eq.(2.5) it follows

$$\frac{E_C}{2\delta} = \operatorname{arctanh}\left[\frac{P_R}{P_S}\right] \tag{2.6}$$

Recalling that $\operatorname{arctanh}(x) = \frac{1}{2}\left(\frac{1+x}{1-x}\right)$ then it follows

$$\delta = E_C\left[ln\left(\frac{1 + P_R/P_S}{1 - P_R/P_S}\right)\right] \tag{2.7}$$

For the negative branch in [4] it is assumed to be symmetric with respect to the positive branch such that

$$P_d^-(E) = -P_d^+(-E) \tag{2.8}$$

In fig.2.1 the behavior of the polarization as a function of the electrical field is described. The intercepts of the upper and lower branch with the Electric field axis ($P = 0$), red line, indicate the values of coercive field set to $E_C = \pm 2MV/cm$. The upper/lower violet line corresponds to the intercept of the lower/upper branch with the Polarization axis ($E = 0$) and gives the value of the remnant polarization $P_R = \pm 20\mu C/cm^2$. The yellow line represent the saturated value of the polarization as both curves approach to it at higher field $P_S = \pm 25\mu C/cm^2$.

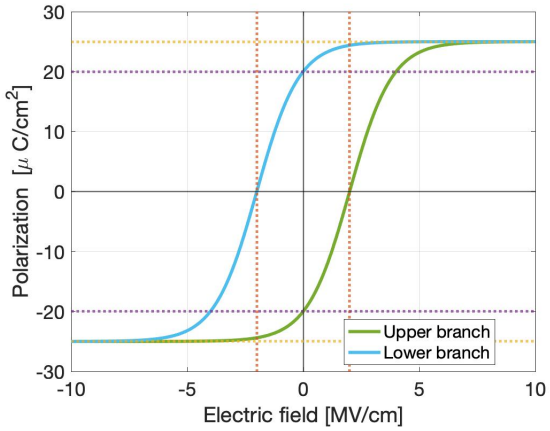


Figure 2.1: Hysteresis curve performing the mathematical model introduce by [4]. The green curve include the trend of the polarization for positive going field whereas the blue curve for negative going field

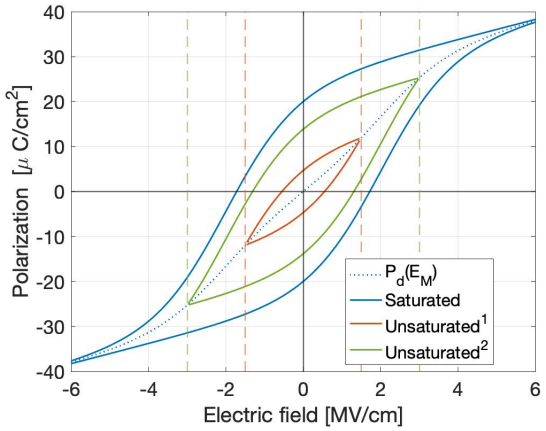


Figure 2.2: Simulated hysteresis curve considering saturated and minor loop according to eq.(2.9), eq.(2.10) and eq.(2.11). The unsatured hysteresis (red and green curve) are featured by a maximum electrical field of $1.5MV/cm$ and $3MV/cm$

Eq(2.4) is however only suitable for saturated hysteresis loop. As every P-E point is either on or within the saturated loop, a new expression for the case of minor loop should be defined [18]. The new variable which enters in play is E_M and is defined as the maximum electrical field that experience the ferroelectric in non-saturated hysteresis curve. The minor upper and lower branch are defined as

$$P_d^+(E, E_M) = P_S \tanh\left[\frac{(E - E_C)}{2\delta}\right] + \epsilon_{FE}\epsilon_0 E + \frac{1}{2}\left(P_S \tanh\left(\frac{E_M + E_C}{2\delta}\right) - P_S \tanh\left(\frac{E_M + E_C}{2\delta}\right)\right) \tag{2.9}$$

$$P_d^+(E, E_M) = P_S \tanh\left[\frac{(E + E_C)}{2\delta}\right] + \epsilon_{FE}\epsilon_0 E - \frac{1}{2}\left(P_S \tanh\left(\frac{E_M + E_C}{2\delta}\right) - P_S \tanh\left(\frac{E_M + E_C}{2\delta}\right)\right) \tag{2.10}$$

whereas the dipole polarization versus the maximum electrical field, dotted blue curve in fig.2.2, is given by

$$P_d(E_M) = \epsilon_{FE}\epsilon_0 E_M + \frac{1}{2}\left(P_S \tanh\left(\frac{E_M + E_C}{2\delta}\right) + P_S \tanh\left(\frac{E_M - E_C}{2\delta}\right)\right) \tag{2.11}$$

Fig.2.2 illustrates the mathematical model introduced by [18] to simulate the P-E characteristic of ferroelectric material. Due to the requirement of few parameters: remnant and saturated polarization, coercive field and the maximum electric field experienced by the ferroelectric when is in minor hysteresis loop it gives to this model a simple analytic way to describe the polarization behavior as a function of the electric field.

2.2 Landau Theory

For bulk ferroelectric the thermodynamic state of a system is a function of 5 different variables: polarization, electric field, stress, strain and temperature [19]. It has been reported that for temperature above the so called Curie temperature T_C (each material has its own T_C) a loss of spontaneous polarization is observed. Having defined the role of temperature, it's possible to distinguish between external variable and internal one from the 4 variables defined above. Electric field E and elastic stress σ are applied external to the material and can therefore introduce changes in polarization P and strain η (internal variables). As the ferroelectric material can undergo a transition from paraelectric toward ferroelectric phase, Landau in its model defines that close to a transition the free energy can be expanded in power series of internal variables (T, P, ν) with coefficients determined by experimental microscopic calculation. It links microscopic parameters with experimental result with the macroscopic world, in our case ferroelectric material. The total free energy considering an unstrained bulk ferroelectric with spatially uniform polarization can be expressed as

$$\mathcal{F} = \frac{\alpha}{2}P^2 + \frac{\beta}{4}P^4 + \frac{\gamma}{6}P^6 - E\,P \tag{2.12}$$

Eq(2.12) is the ferroelectric free energy according to the Landau-Devonshire theory where the coefficient α, β and γ are the ferroelectric anisotropy constant and E indicates the electric field. Embedded in α is the dependence of temperature as:

$$\alpha = \alpha_0\,(T - T_0) \tag{2.13}$$

with temperature T_0 the Curie-Weiss temperature of a material. The eq.(2.12) can be formulated as follow:

$$\mathcal{F} = \frac{\alpha_0}{2}(T - T_0)P^2 + \frac{\beta}{4}P^4 + \frac{\gamma}{6}P^6 - E\,P \tag{2.14}$$

Ferroelectric materials are feature by positive value of the α_0 and γ parameter. The value of the quartic term indicates the second order transition case when $\beta > 0$ and first order discontinuous case when $\beta < 0$.

2.2.1 First order transition

Starting from eq.(2.14) with $\beta < 0$ the behavior of the free energy at different temperature is illustrated in fig.2.3. To properly analyse how the temperature influences the free energy-polarization curve, the minima of the free energy is evaluated as reported in eq.(2.15)

$$\frac{\mathrm{d}F}{\mathrm{d}P} = \alpha(T - T_0)P + \beta P^3 + \gamma P^5 = 0 \tag{2.15}$$

Apart from the solution $P = 0$ from eq.(2.15):

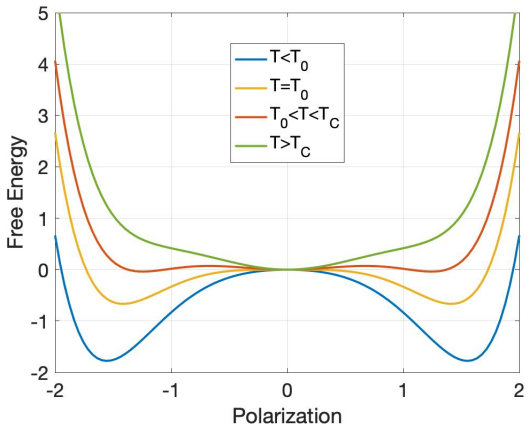


Figure 2.3: First order transition with $\alpha_0 = 0.1\,[m/(F\,K)]$, $\beta = -2\,[m^5/(F\,C^2)]$, $\gamma = 1\,[m^9/(F\,C^4)]$ and $T_0 = 100\,[K]$. The Curie temperature defined in eq.(2.18) is equal to $T_C = 110\,[K]$

$$P^2 = \frac{-\beta \pm \sqrt{\beta^2 - 4\gamma\alpha_0(T - T_0)}}{2\gamma} \tag{2.16}$$

The minima of free energy as a function of polarization at different temperature is expressed in eq.(2.17)

$$P = \begin{cases} \pm\sqrt{\frac{-\beta\pm\sqrt{\beta^2-4\gamma\alpha_0(T-T_0)}}{2\gamma}} & \text{for } T < T_0 \\ 0, \pm\sqrt{\frac{-\beta\pm\sqrt{\beta^2-4\gamma\alpha_0(T-T_0)}}{2\gamma}} & \text{for } T_0 < T < T_C \\ 0 & \text{for } T > T_C \end{cases} \tag{2.17}$$

with

$$T_C = \frac{\beta^2}{4\gamma\alpha} + T_0 \tag{2.18}$$

the Curie temperature. The discontinuous transition is dictated by the suddenly jumps from two non-zero stable state towards $P = 0$ as illustrated in fig.2.3. Specifically the jump coincides when temperature overcomes the Curie temperature, $T > T_C$, and the polarization inside the material drops to 0.

2.2.2 Second order phase transition

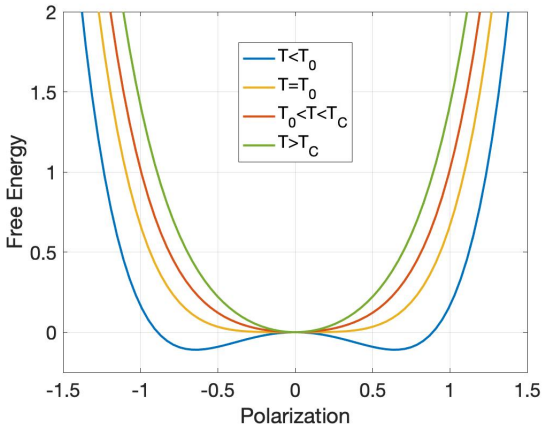


Figure 2.4: Second order transition with $\alpha_0 = 0.1\,[m/(F\,K)]$, $\beta = +2\,[m^5/(F\,C^2)]$, $\gamma = 1\,[m^9/(F\,C^4)]$ and $T_0 = 100\,[K]$

The second order phase transition is involved when the parameter $\beta > 0$ and the behavior of the polarization vs free energy is entirely influenced by T_0 as shown in fig.2.4. As the quadratic term α increases its value, from negative to positive, by increasing the temperature T the minimum of polarization move toward the two stable non-zero polarization toward the value of $P = 0$. What differentiatesì the two transitions is the temperature T which invoke this passage from ferroelectric material toward paraelectric material. It's the Curie temperature in the first order transition and the value of T_0 in the second order transition. Because our study is mainly focus on material featured by the parameter $\beta > 0$ we will give an analysis of the polarization vs electric field exclusively for the second order transition.

2.2.3 Hysteresis performed with Landau theory

When tracing the ferroelectric hysteresis at least three relevant points are inspected to evaluate the behavior of the ferroelectric polarization as a function of the electric field. Saturation polarization, the maximum polarization induced in the material at higher field, remnant polarization indicating the amount of polarization when the field is removed ($E = 0$) and the coercive field defines as the electric field bringing the polarization back to 0. The question could be how to link them with the Landau ferroelectric anisotropy constant[20]. Before introducing some mathematical formula we slightly modify the free energy formula describe in eq.(2.14). As the coefficient $\alpha_0(T - T_0)$ in ferroelectric material is negative we set equals to α as for the simulation we set the temperature $T < T_0$; in addition it's quite common to set $\gamma = 0$ for second order transition phase. Given the free energy in eq.(2.19)

$$\mathcal{F} = \frac{\alpha}{2}P^2 + \frac{\beta}{4}P^4 - E\,P \tag{2.19}$$

the electric field as a function of the polarization can be defined by setting $\frac{\mathrm{d}F}{\mathrm{d}P} = 0$ (in other word by finding the minima of the free energy), fig2.5.

$$E(P) = \alpha P + \beta P^3 \tag{2.20}$$

From the zeros of eq.(2.20) the value of remnant polarization is given:

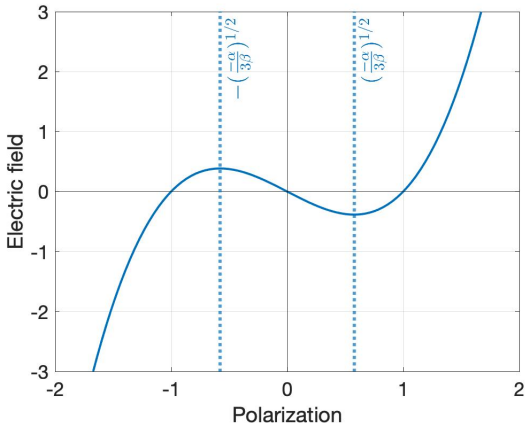


Figure 2.5: Electric field vs Polarization with $\alpha = -1\,[m/(F)]$, $\beta = +1\,[m^5/(F\,C^2)]$. The two vertical blue line indicate the P value, eq.(2.23) for the local minima and maximum of the electric field

$$\pm P_r = \left(\frac{-\alpha}{\beta}\right)^{1/2} \tag{2.21}$$

The coercive field is determined by the value of the electric field at local minimum and maximum. From eq.(2.20) by computing the derivative with respect to polarization and set to 0:

$$\frac{\mathrm{d}E}{\mathrm{d}P} = \alpha + 3\beta P^2 = 0 \tag{2.22}$$

it follows that

$$P = \pm \left(\frac{-\alpha}{3\beta}\right)^{1/2} \tag{2.23}$$

By combining eq.(2.23) with eq.(2.20) the coercive field as a function of Landau coefficient can be expressed as:

$$\pm E_C = \alpha \left(\frac{-\alpha}{3\beta}\right)^{\frac{1}{2}} + \beta \left(\frac{-\alpha}{3\beta}\right)^{\frac{1}{2}} \tag{2.24}$$

Recalling the relationship between the remnant polarization with α and β, then merging eq.(2.21) with eq.(2.24) the parameter β can be expressed as a function of coercive field and remanent polarization

$$\beta = -\frac{3\sqrt{3}E_C}{2P_R^3} \tag{2.25}$$

Having defined the relationship between the Landau parameters with the coercive field and saturation polarization in eq.(2.21) and eq.(2.25) our next step is to simulate the ferroelectric hysteresis loop (P-E curve). It's defined by finding the inverse roots of the $E(P)$ function, starting from eq.(2.20), [20]. The solutions are given in eq.(2.26)

$$\begin{cases} P1(E) = S + T \\ P2(E) = -\frac{1}{2}(S+T) + \frac{1}{2}j\sqrt{3}(S-T) \\ P3(E) = -\frac{1}{2}(S+T) - \frac{1}{2}j\sqrt{3}(S-T) \end{cases} \tag{2.26}$$

with

$$\begin{cases} S = \sqrt[3]{R + \sqrt{Q^3 + R^2}} \\ T = \sqrt[3]{R - \sqrt{Q^3 + R^2}} \\ R = \frac{E}{2\beta} \\ Q = \frac{\alpha}{3\beta} \end{cases} \tag{2.27}$$

The simulation of the hysteresis function is reported in fig2.6 with the simulated asterisk points chosen from the real valued root $P_m(E_i)$, with m indicating one of the three solution in eq.(2.26) and i the i-component of the electric field vector, which is closest in value to the previous point $P_m(E_{i-1})$. As the applied field increases we should expect a constant

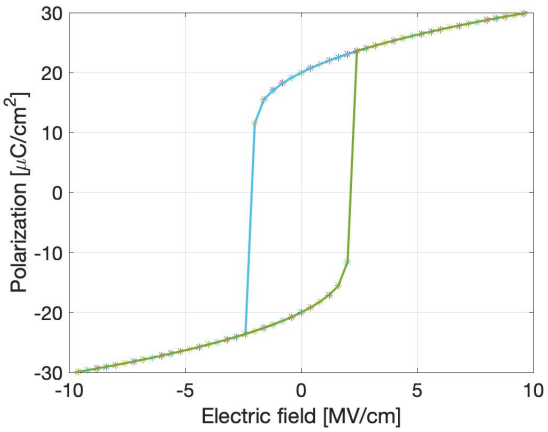


Figure 2.6: Ferroelectric hysteresis performed with the Landau model. The E_C and P_R parameter are first determined and set to $2MV/cm$ and $20\mu C/cm^2$ which defines the Landau coefficient to be $\alpha = 2.59 \cdot 10^{11}\,[cm/F]$ and $\beta = 6.49 \cdot 10^{20}\,[cm^5/(FC^2)]$

polarization to be set up due to the completely alignment of dipoles inside the material. Indeed as shown in fig.2.6 the maximum value of polarization P_S is not retrieved. The comparison of the two models is illustrated in fig.2.7 The difference between the Landau model and Preisach model is mostly dictated by the saturation polarization. In Preisach P_S is one of the parameter used inside the $\tanh(x)$ function, eq.(2.4) but in Landau the coefficient α and β have no dependencies on P_S despite having a relationship with E_C and P_R. Another pertinent point to highlight is the slope of the two models. In fig.2.7

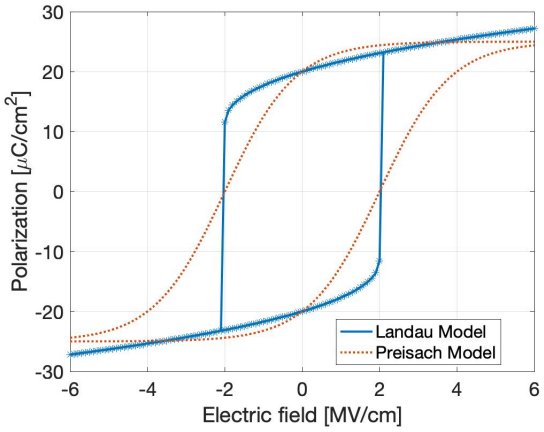


Figure 2.7: Ferroelectric hysteresis comparison. Landau model, blue curve, and Preisach model, red curve, with $E_C = 2MV/cm$ and $P_R = 20\mu C/cm^2$

the Landau curve shows a fast transition from a negative polarization toward positive and vice-versa. In Preisach model keeping the same value of E_C and P_R a different slope is observed which indicate a slow transition of the polarization as a function of the electric field. Beside their difference these two models are the most used one to describe the behavior of ferroelectric material.

2.3 Ferroelectricity model in GINESTRA simulation software

Ginestra software is employed, throughout the thesis, to simulate the behavior of ferroelectric field effect transistor as well as understand the physics of ferroelectric material when is sandwiched between two metal electrodes or a metal and insulator and so on. To carry out these simulation we need firstly to introduce the ferroelectric model implemented in *Ginestra* and understand when one model is convenient over the other (its pros and cons). Before entering in the discussion we should anticipate that Preisach and Landau model are used in *Ginestra* but we need some insight on how the simulation software define them.

2.3.1 *Ginestra* Preisach model

It's a one-dimensional model where the polarization direction can be defined either on one of the three Cartesian axis or on a custom direction defined by the user. The coercive field, saturation polarization and remnant polarization can be set to be symmetric or asymmetric (in that case, for instance, we need to define both E_C^+ as E_C^-). Last but not least this model is not time dependent which means that studying the ferroelectric polarization over time is not allowed. Mathematically the polarization is defined according

to eq.(2.28).

$$P = c \cdot P_S \cdot \tanh\left[\frac{1}{2E_C} \ln \frac{P_S + P_R}{P_S - P_R}(E \pm E_C)\right] + P_{off} \tag{2.28}$$

It looks like very similar to eq.(2.4) beside the parameter P_{off} which offer the possibility to set an initial value of polarization.

2.3.2 *Ginestra* Landau model

This model introduces new relevant parameter with respect to section2.2.3. Starting from the polarization of ferroelectric which follows the Ginzburg-Landau dynamic equation

$$\rho \frac{\mathrm{d}P}{\mathrm{d}t} + \nabla_P u = 0 \tag{2.29}$$

with ρ indicating the viscosity term influencing the transition toward the two stable polarized state. At physical level the viscosity term indicates the internal resistivity of ferroelectric material as fast transition is characterized by low value of ρ. The free energy is defined in eq.(2.30)

$$u = \alpha(T)P^2 + \beta P^4 + \gamma P^6 - E \cdot P + g(\nabla P)^2 + \frac{\epsilon_0 \epsilon_{FE}}{2} E^2 \tag{2.30}$$

with

$$\alpha(T) = \alpha + \alpha_T(T - T_C) \tag{2.31}$$

Two additional terms are defined with respect to eq.(2.12): the domain coupling term and the electrostatic self-energy (depolarization) term. The parameter g is the domain wall coupling factor which can be either isotropic or anisotropic; in the last case g is a tensor with a longitudinal component along the preferential direction (defined by the user) and a transverse component along the perpendicular direction. Not only the parameter α, T_C, α_T, β, γ can be defined by the user but also the viscosity ρ, and the longitudinal and transverse domain wall component g_L and g_T by using the Ginzburg-Landau (G-L) model can now be edit to shown the behavior of the ferroelectric material. A final remark about the model is it only works when transient simulations are performed.

Chapter 3

GINESTRA modeling platform

Once the models for ferroelectricity have been acquired it's now essential to present how practically the P-E hysteresis loop results are obtained in *Ginestra* showing both the device and the test section. We introduce firstly how the device is created either using a template or defining it by custom geometry and after how the test is set by specifying the electrical and physical parameters. We conclude the chapter with the analysis of the FeFET test focusing on the different gate voltage waveform which will be used in the evaluation of retention test as describe in final chapter5.

3.1 *Ginestra* Device section

We start with a simple structure of metal-ferroelectric-metal (MFM) as illustrated in fig.3.1. TiN is the metal electrode used while the ferroelectric material is HZO ($Hf_{0.5}Zr_{0.5}O_2$)

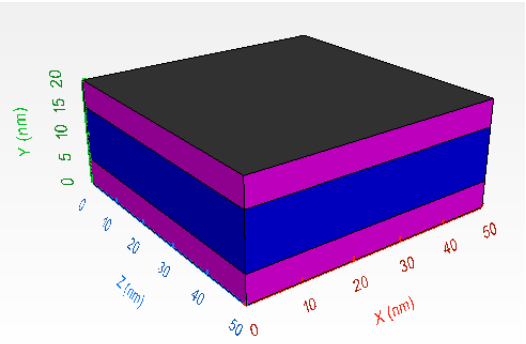


Figure 3.1: Metal-Ferroelectric-Metal (MFM) structure. The top and bottom electrode are defined respectively at the top and bottom of x − y plane. The blue cuboid indicates the ferroelectric HfO_2 material while violet bottom and top cuboid the TiN layer

compatible with the Complementary Metal Oxide Semiconductor (CMOS) flows and showing large remnant polarization, close to $20\mu C/cm^2$, even at thickness lower than $10nm$. It is considered to be one of the most promising ferroelectric material for memory application. In fig.3.2 is shown the dielectric behavior of $Hf_{1-x}Zr_xO_2$ by varying the Zr ratio and

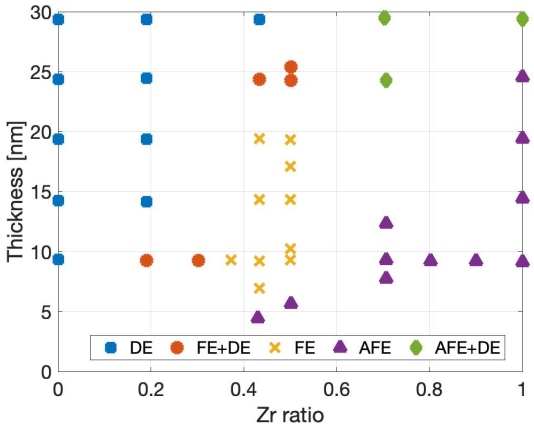


Figure 3.2: Behavior of $Hf_{1-x}Zr_xO_2$ film as a function of Zr_x ratio and film thickness. Data taken from[5]

film thickness. The results are for the same annealing and atomic layer deposition condition and reveal that only close to 0.5 of Zr ratio the ferroelectric behavior is obtained. As described above even for film thickness $t < 10nm$ the ferroelectric behavior is preserved. Decreasing the Zr ratio an increase of monoclinic phase is reported with the consequence of dielectric behavior while increasing Zr ratio up to 1 (ZrO_2) the tetragonal phase dominates over the orthorhombic phase and the antiferroelectric behavior is observed.
Once the structure is properly set by defining its geometry, electrodes position and the different regions composing our device the device section is ended.

3.2 *Ginestra* Test section

Ginestra Test is by far the main part of our simulation program. It's mainly divided into three different sections: *simulation*, *statistics* and *design of experiments*. We will introduce deeply the first one as it provides electrical parameters and physical options which need to be properly design to the kind of simulation we want to performed. Statistics and design of experiments will be elucidated as well.

3.2.1 Simulation section

It accounts for different aspects that are encountered when performing simulation. It's the main part, the key component and is worth to pointing out how it works specifically because DC, Kinetic Monte Carlo and Transient simulation requires different input and/or physical model which should be either enable or disable before running the test. Transient

simulation are mostly performed when discussing ferroelectric devices. As a consequence of that the time stepping part is a relevant section in which the minimum and maximum time step together with the total simulation time can be defined by the user. Nonetheless it's possible to set the applied voltage on each electrodes either using a constant signal or triangular or square or even a user defined signal in which time-voltage points are specified in order to properly fit a specific kind of signal. Inside the Physics Options it's possible to define the Ginzburg-Landau physics for ferroelectric material, solve in 1D,2D and 3D (the last one will increase drastically the amount of running time), enable or disable a specific transport mechanism through the material (e.g. enable/disable the tunneling of electrons between the conduction bands of two material or enable/disable electrons transitions between electrodes and traps or between conduction band and traps). In addition of solving the Poisson equation accounting for defect charges and/or for doping charge, it's manageable to enable the movements of species within a region accounting for Coulomb interaction between ions and/or accounting for ion empty state charge. Practically it's the heart of the simulation program and the correct choice of parameters along with the enable of different physical tab make our test result very close to the one performed in the fab.

3.2.2 Statistic, Design of experiments and sequence section

As the name suggest the statistic section is allowed when we want to study devices whose parameters are randomly generated. For instance considering the RRAM (resistive random access memory) it is possible to vary the distribution of oxygen vacancies which can be randomized and a statistical device will be created. The design of experiments is performed when a given parameter (it could be more than one) of the material like its dielectric constant or the value of Landau coefficient or its geometry is varied according to the user specifications. We will use design of experiments in the next section to illustrate how the Ginzburg-Landau coefficients modify the P-V hysteresis curve while the statistic will be employed when a statistical study of devices made of defects is performed (it will not be employed in our thesis project). Lastly the sequence section is performed when an endurance study of the device is held. Because of the need of performing test in sequence and repeating them for one cycle or more than one than the second test is included in the project and it can be enqueued and by saving the state of the first test a sequence tests is enabled. As we're looking on retention test we will skip both statistic and sequence section. Design of experiments will be used when the evaluation of retention at different ferroelectric thickness is investigated.

3.3 Ferroelectric Capacitor Test

Keeping in mind the same structure illustrated in fig.3.1 we define two different tests with *Ginestra* simulator whose target is the investigation of the ferroelectric polarization.

3.3.1 Positive-Up-Negative-Down (PUND) test

The PUND test is a transient test and is one of the method used to characterize the ferroelectric response. In fig.3.3 the red dashed line illustrates the signal waveform with the maximum positive and negative voltage set to $\pm 4V$ and a total simulation time of $250\mu s$. Beside the first negative pulse, named pre-polarization pulse, whose goal is to switch the dipoles into a positive polarization state we aim to discuss the role of *Positive* and *Up* pulse on the behavior of the polarization inside the material. As shown in fig.3.3 the first

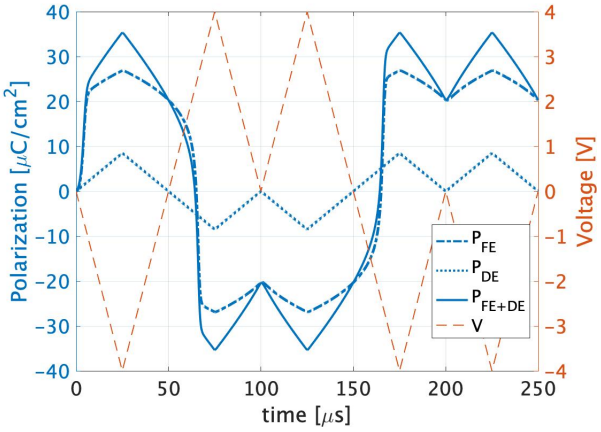


Figure 3.3: Polarization as a function of time using PUND test. Blue curve indicates the polarization inside the material, specifically the dashdot curve is for the ferroelectric polarization P_{FE}, the dotted curve stands for the dielectric polarization P_{DE} while the solid curve indicates the total polarization of the device P_{FE+DE}. The red dashed curve marks the PUND testwaveform

positive pulse is related to the response of the ferroelectric and dielectric component. To be specific the ferroelectric component switches from a positive state into a negative one and governs the total polarization inside the ferroelectric till the application of *Negative* pulse. The second positive pulse influences mostly the paraelectric component of the material, as P_{DE} increases in magnitude once the voltage is applied and returns back to 0 when the electric field is removed. The ferroelectric components, instead, retains its polarization over time. Furthermore by performing the difference of the two pulses response, fig.3.4, the amount of remnant polarization is obtained. Precisely we isolate the dielectric component by shifting the second pulse in order to align with the polarization axis at $t = 0s$. The difference between the first pulse, ferroelectric and dielectric response, and the second pulse, uniquely dielectric response results into the remnant polarization of the material, solid blue line in fig.3.4, equal to $20\mu C/cm^2$. We will double-check the remnant polarization value when illustrating the hysteresis loop, fig.3.7, but for now on we will move our discussion on the (displacement) current behavior of the MFM structure, fig.3.5. Before inspecting the role of the ferroelectric component and the dielectric one,

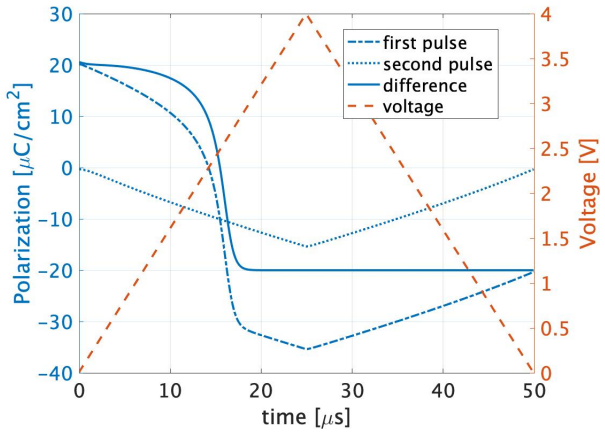


Figure 3.4: Analysis of the polarization switching over time as a function of the *Positive* pulse, dashdot line, and *Up* pulse, dotted line. The difference indicated by the solid line measures the amount of remnant polarization inside the material

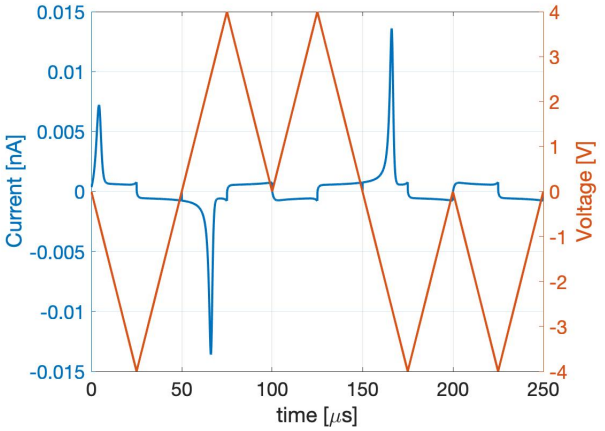


Figure 3.5: Transient current, blue curve, and signal waveform, red curve, using PUND test

we recall the formula of the displacement current in eq(3.1)

$$I_D = \iint_S J_D \cdot \mathrm{d}S \tag{3.1}$$

with J_D indicating the displacement current density, eq(3.2)

$$J_D = \frac{\partial D}{\partial t} = \epsilon_0 \frac{\partial E}{\partial t} + \frac{\partial P}{\partial t} \tag{3.2}$$

with D the electric displacement field. The large peaks shown in fig.3.5 are related to changes in ferroelectric polarization over time, once the dipoles switches from positive to

negative state and vice-versa, and small-scale peaks are related to the rate of change of electric field over time. We conclude the PUND section by showing the ferroelectric hysteresis behavior, P-V, and the current-voltage, I-V curve in fig.3.6. The two double peaks

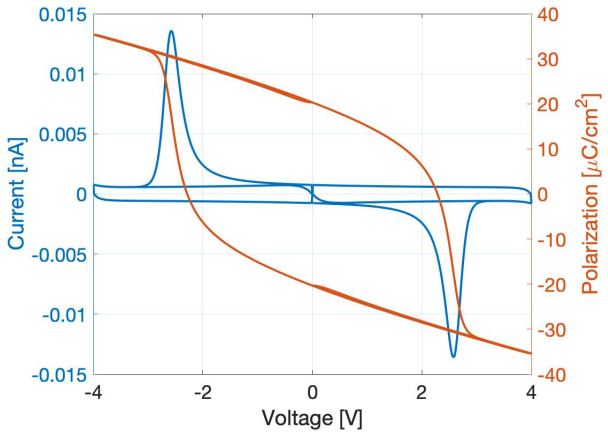


Figure 3.6: Polarization-Voltage, blue curve and Current-Voltage, red curve using PUND test

correlates the changes of ferroelectric polarization direction while the almost rectangular shape is dictated by the first term of the eq.(3.2) ($\propto \frac{\partial E}{\partial t} = const.$) related to the dielectric component. As a final step the evaluation of the ferroelectric capacitance is made and compared with the dielectric one. We will start firstly by showing the polarization-voltage characteristic considering both the ferroelectric and dielectric component and separately, fig.3.7. How does the capacitance look like for the ferroelectric component and for the

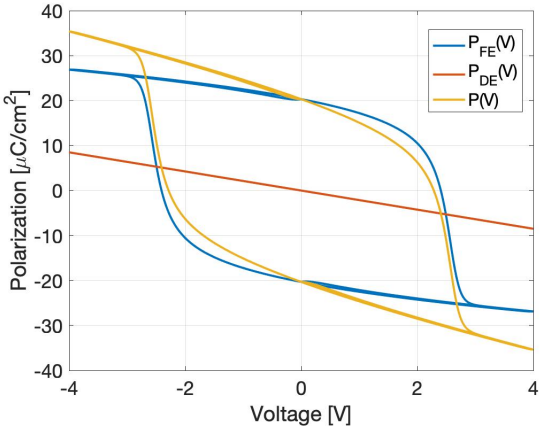


Figure 3.7: Polarization-Voltage characteristic considering the ferroelectric polarization, blue curve, dielectric polarization, red curve and the sum of them, yellow curve

dielectric one?

Let's consider the electric displacement field:

$$D = \epsilon_0 E + P_{TOT} \tag{3.3}$$

with P_{TOT} indicating the sum of the polarization due to the ferroelectric switching dipoles and due to the linear displacement (dielectric component).

$$P_{TOT} = P_{FE} + P_{DE} = P_{FE} + \epsilon_0 \chi E \tag{3.4}$$

with the electric susceptibility correlated to the dielectric constant by

$$\epsilon_R = 1 + \chi \tag{3.5}$$

Combining eq.(3.3) with eq.(3.4) and eq.(3.5) the electric displacement field can be expressed as

$$D = \epsilon_0 E + P_{FE} + \epsilon_0 \chi E = \epsilon_0 \epsilon_R E + P_{FE} \tag{3.6}$$

Because the displacement field, in a capacitor structure, is equal to the surface charge density, that is to say the charge per unit of area

$$D = \frac{Q}{A} = \frac{\epsilon_0 \epsilon_R E + P_{FE}}{A} \tag{3.7}$$

then the capacitance can be defined as

$$C = \frac{\mathrm{d}Q}{\mathrm{d}V} = \frac{1}{t}\frac{\mathrm{d}Q}{\mathrm{d}E} = \frac{A}{t}\left(\epsilon_0 \epsilon_R + \frac{\mathrm{d}P}{\mathrm{d}E}\right) \tag{3.8}$$

The first term of eq.(3.8) is the well-know capacitance formula of the parallel plate capacitor. It indicates the dielectric component terms. What is new is the ferroelectric component, second term of eq.(3.8). Because of the hysteresis nature of the polarization with voltage the second term results into a non-linear capacitance behavior, [21], as shown in fig.3.8. The hysteresis behavior of the capacitance as a function of the applied voltage is a consequence of the orientation of the polarization. Specifically closer to the coercive field the two maximum peaks are observed. The reason is because of the relatively small change of electric field, near $V_C = \pm 2V$, which bring the polarization to drastically changes from positive to negative state in the first condition, *Positive* pulse, and from negative to positive state in *Negative* pulse. We conclude this section by remark the role of ferroelectric polarization, due to the switching dipoles, and the polarization due to the linear displacement. In ferroelectric devices the dominant feature is the ferroelectric component as both the P-V curve and C-V one shown the characteristic hysteresis behavior properly dictated by the non-linearity of polarization which at the end is a characteristic of ferroelectrics.

3.3.2 Polarization-Voltage test

The last test, called polarization-voltage test, still provides the investigation of dielectric and ferroelectric response but as a total response. Meaning that the splitting of

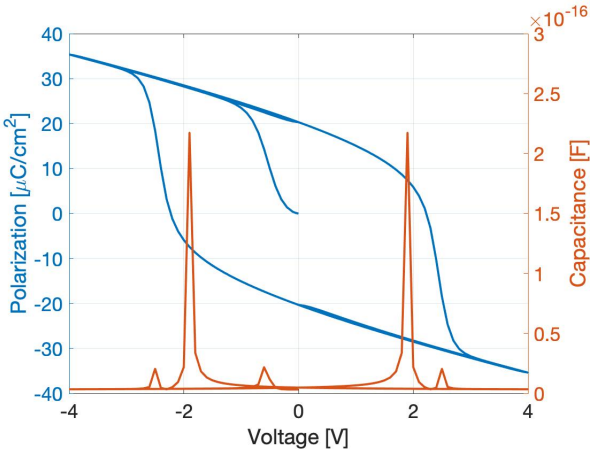
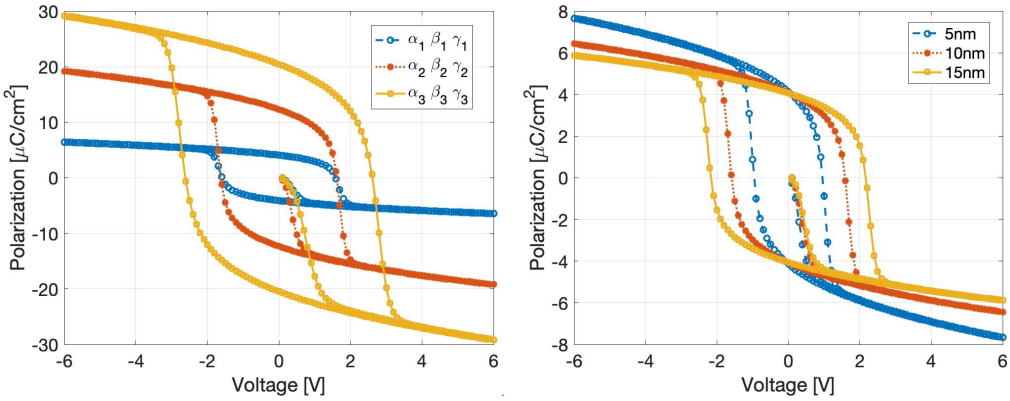
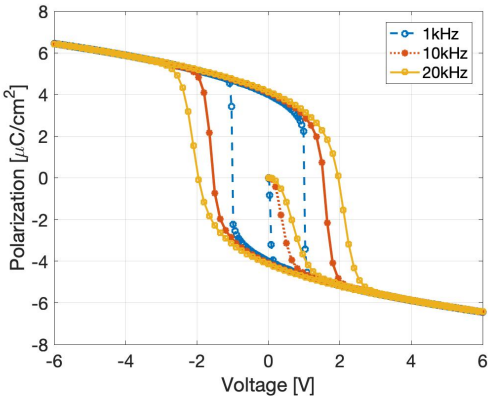


Figure 3.8: Small signal Capacitance measurement showing the C-V hysteresis characteristic. The small signal capacitance is evaluated at frequency $f = 1.2kHz$ of AC signal

two component: paraelectric and ferroelectric is disabled. Which kind of waveform is used? Keeping as a reference the positive-up-negative-down waveform signal, the voltage signal waveform is obtained by removing the *Up* and *Down* pulse (the total simulation time is set to $250\mu s$). We dedicate this section to understand the impact of the Landau parameter on the polarization-voltage curve by both modifying (recalling the equation2.29 and equation2.30) the first and second Landau coefficient (α, β) and the frequency of the applied signal (which acts like the viscosity term ρ in the P-V behavior). Starting from the Ginzburg-Landau parameter, fig.3.9a, we simulate three different set of α and β values. Two of them corresponds to the default ones used in Ginestra $\alpha_1 = -2.922e9[m/F]\,\beta_1 = 9.1339e11[m^5/(FC^2)]$ and $\alpha_2 = -9.0933e8[m/F]\,\beta_2 = 1.13e10[m^5/(FC^2)]$ whereas the third one correspond to the result obtain by [22] $\alpha_3 = -1.03e9[m/F]\,\beta_3 = 3.5e10[m^5/(FC^2)]$. Despite the difference in terms of remnant polarization as the $P_{R_1} = 4\mu C/cm^2$ and $P_{R_3} = 20\mu C/cm^2$ we may interpret as the best choice to work with the G-L coefficient defined in [22]. As we discuss in the second part of the thesis having a high value of remnant polarization does not indicate a better performance of the device which for the memory indicates is high capability of retain data over time. In fig.3.9b the thickness of the HZO t_{FE} material is varied from $5nm$ toward $15nm$ considering the G-L parameter $\alpha_1\,\beta_1$. What is interesting to notice is the potential value corresponding to the disappear of the ferroelectric polarization. By taking the potential value from the intercept of the P-V curve with the x axis and divide by the t_{FE} the coercive field value is recovered. According to eq.(2.24) the E_C value should only depend on the first and second Landau parameter which indicates a strong discrepancies with the result reported in table3.1. What is missing with the previous analysis? The dependence of time as it's mostly remarked in fig.3.9c and eq(2.29). By performing a triangular signal test at different frequencies, keeping the $t_{FE} = 10nm$, we observe how the switching of the polarization is influenced over time. Increasing the frequency will induce a lower



(a) P-V as a function of α and β coefficient (b) P-V as a function of HZO thickness



(c) P-V as a function of the applied signal frequency

Figure 3.9: Polarization-Voltage hysteresis

t_{FE}	E_{FE}
$5nm$	$1.9072\,MV/cm$
$10nm$	$1.5883\,MV/cm$
$20nm$	$1.4429\,MV/cm$

Table 3.1: Evaluation of coercive field value of HZO at different ferroelectric thickness

response time for the dipoles to switch from negative to positive polarization and vice-versa. The direct consequence involves the dependencies of the coercive field alteration as higher voltage is required to completely switch the ferroelectric dipoles when high frequency signal are applied. For a better analysis on the ferroelectric switching behavior we suggest the appendixB. In conclusion the viscosity term ρ defined in (2.29) influences the

polarization-voltage curve as well. The term influences the speed of the transition as for lower value a fast switching toward the opposite polarization is derived. Lastly we have to claim that the G-L parameter are only valid for a given ferroelectric thickness and at a given frequency of the signal applied. Beside we keep them fix in the simulation section is the proper choice to point out that their validity is limited and can not be considered as an identity document for that specific kind of ferroelectric material. The correct choice is to fabricate a MFM capacitor and evaluate the experimental P-V loop. By fitting with the G-L loop, section2.2.3, is possible to define the α, β, γ, ρ parameters.

3.4 Ferroelectric field effect transistor test

3.4.1 Device inspection

In this section we're going to investigate the retention test. Prior to that we will provide a brief analysis on how the device is made of by showing an example of the FeFET in fig.3.10. The bottom layer and the following one correspond respectively to the SiO_2 and Si material layers. The buried oxide layer, orange cuboid, is included to emulate the FDSOI (fully-depleted-silicon-on-insulator) FeFET implemented in the 22nm node by GlobalFoundries (semiconductor manufacturing company) as reported in [23] and [11]. We

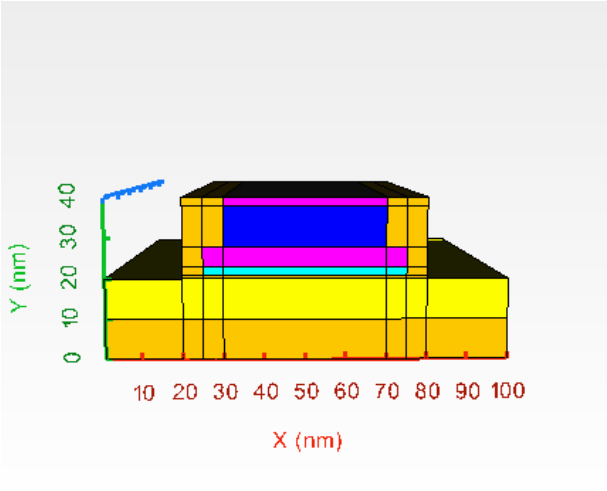


Figure 3.10: BEOL FeFET device with area ratio 0.8 simulated in GINESTRA

set the thickness of the bottom oxide layer and the silicon layer to $10nm$ (y direction) while the length is $100nm$ (x direction). The gate oxide stack is made of $0.8nm$ of SiO_2 thickness (the dielectric constant is $\epsilon_{INS} = 6.6$), orange cuboid, and $2nm$ of HfO_2 thickness, celestial cuboid. The reason of including the silicon oxide between the semiconductor and the high-κ material is to properly mimic the problem of interface which is overcome by placing a thin layer of SiO_2 on top of Si. The FEOL is ended by adding the metal layer made of TiN, pink cuboid, with $5nm$ of film thickness and $50nm$ of gate length. The area ratio of 0.8

implies that the area of the ferroelectric material need to be modified. In our simulation the width, z direction, is preserved and equals to $100nm$. The only choice is to act on the x direction by reducing the length from $50nm$ toward $40nm$. A decreasing of the ferroelectric length is responsible for the formation of different area ratio and so different BEOL FeFET devices. In our study the AR is varied from 1.0 to 0.4, corresponding to ferroelectric length of $50nm$ and $20nm$. The last correspond to the maximum achievable resolution for the optical lithography which limited the inspection of different AR BEOL FeFET devices if 28nm and 22nm gate length are used. The FEOL FeFET is obtained by removing the floating metal layer and the high-κ dielectric layer while constrain the gate oxide length to be the same (SiO_2 and HZO length of $50nm$).

Doping

In this paragraph we're going to illustrate the doping concentration inside the semiconductor layer. In fig.3.11 a two-dimensional plot investigates the doping concentration inside the Silicon material. By cutting along the y axis a one-dimensional plot is obtained

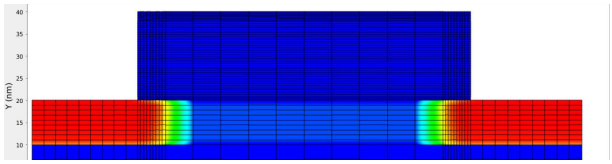


Figure 3.11: 2D plot of the doping concentration inside the semiconductor

to evaluate the amount of doping concentration in the channel and at source and drain region. The source and drain are n-type doped with the peak density of $10^{20}\,cm^{-3}$ while

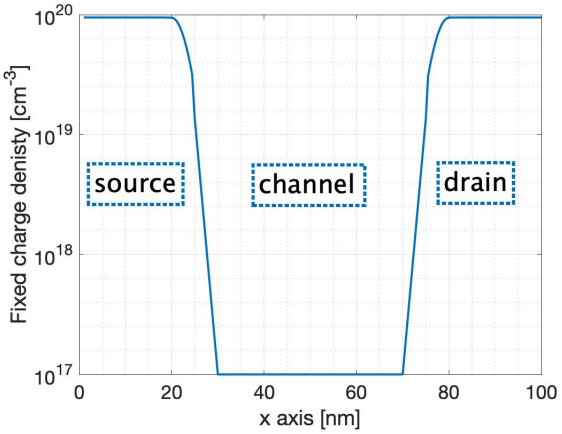


Figure 3.12: Fixed charge density along the x direction by performing a cutting at $y = 16nm$ (Silicon side)

the channel is p-type uniformly doped with concentration of $10^{17}\,cm^{-3}$, fig.3.12.

3.4.2 Ginestra test

We dedicate this part to properly analyse the writing and reading operation of the ferroelectric memory devices. As the core result will be present in chapter5 we will highlight the main aspect concerning to the single pulse waveform and try to elucidate the ideal-close behavior of the ferroelectric FeFET. In fig.3.13 the waveform scheme of the gate

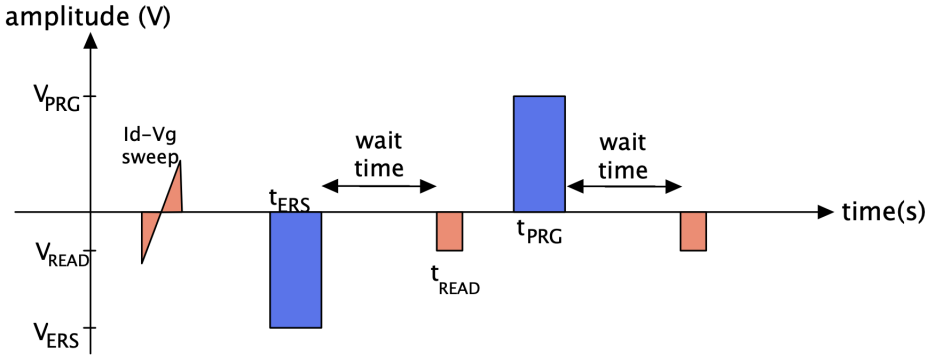


Figure 3.13: Gate voltage waveform scheme apply for the evaluation of retention for the ferroelectric FET

voltage is shown in order to study the behavior of the n-type FeFET memory device when retention test is applied. In the following a brief study of the single pulse signal of fig.3.13 is carried out.

1. Small sweep $I_D - V_G$ read. The initial read of the device is exclusively performed to check the behavior of the transistor. What does it mean? By inspecting the trans-characteristic curve we should get result closer to an ideal MOSFET device as the ferroelectric is oriented neither upward nor downward since in this phase the ferroelectric dipoles are randomly oriented. The outcome of the first test should guarantee that the device is "alive" which indicates that it's working as a transistor. For the electrical standpoint we will ramp up the gate voltage from $-1.5V$ to $2.5V$ in a time interval of $100ns$ while the drain voltage is keep fix at $0.1V$.

2. ERS pulse voltage. During the applied negative potential on the gate the ferroelectric polarization start pointing upwards providing the condition of the attraction of positive charges close to the semiconductor-insulator interface. The result will give a high threshold voltage which can be read into the "0" state of a memory device. It should be mentioned that the applied signal on the gate has to provide the proper switching of the ferroelectric dipoles, meaning that the electric field across the ferroelectric need to be higher than the coercive field in order to insure a correct write operation. Inside our simulation framework we vary the write voltage on the gate as a function of ferroelectric thickness. The time interval is set to $20\mu s$ while the applied gate voltage is $V_G = -5V$.

3. Wait time. To evaluate the behavior of the ferroelectric field effect transistor in retain data we slightly increase the amount of wait time before the read operation.

In spite of that an *instant reading* (wait time set to 0s) has been initially tested to verify the behavior of the memory device. Once certify the high-V_{th} state and low-V_{th} state the wait time has been varied from $1ns$ toward $1s$ inside the design of experiment panel. Within the simulation test we simulate the condition of open circuit in which the current in each terminals is set to $0A$. Two different motivation can justify the following operation: if the gate voltage is set to 0 we will still have the influence of the work-function difference between the semiconductor and the metal with the consequence of providing an effect on the ferroelectric polarization which could benefit one state over the other. Secondly the retention test are performed by putting the device in an oven and evaluating the ability of retain data at different temperature values. This implies that the device is not connect to any terminals which indicates the proper choice used.

4. Small pulse voltage read. The requirement of the point reading instead of the sweep reading will be highlight in chapter5. We could anticipate that no matter the amount of voltage on the gate is applied we will influence the ferroelectric polarization as well as the trans-characteristic curve. The memory window describe in section1.3.3 is generally evaluated using the constant-current-method, that is the value of the gate voltage when the drain current is equal to $10\mu A$. Nonetheless by providing a sweep reading we will show a strong disturb of the ferroelectric state which has bring us to transfer toward the point reading. The time interval remains the same as the previous sweep read while the gate voltage is kept at $-0.2V$.

5. Program pulse voltage. In order to avoid any redundant concepts already discussed for the ERS pulse voltage we have only to claim that a positive voltage is applied on the gate terminals to provide the reversal of the ferroelectric dipoles, $V_G = 5V$. The direction of the polarization is now pointing downward with the attraction of minority carrier leading to the low threshold voltage or "1" state of the memory device. Point 3 and point 4 remain unchanged as the wait time and the amount of pulse voltage have not been modify in the retention study.

With the previous analysis we conclude the first part of the thesis. In the next section we will demonstrate the reduction of the depolarization field when the ferroelectric area is reduced and the results obtained with Ginestra of the retention test for both the FEOL FeFET and of the engineered BEOL FeFET.

Part II

Secon Part

Chapter 4

Depolarization field

Having examine how the simulations are performed with the use of *Ginestra* simulator software, we're now discussing the main issue concerning the ferroelectric memory devices: its low data retention [14]. The phenomenon is dictated by the switching of the polarization and as a consequence the loss of memory state when the power has been switched off. Let's look at fig.4.1 where a metal-ferroelectric-metal structure is illustrated. The

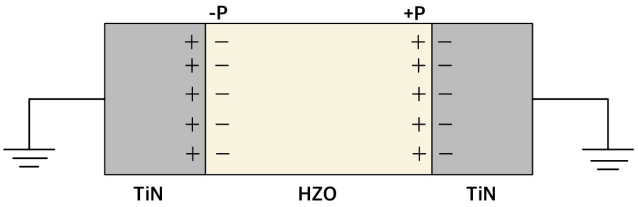


Figure 4.1: MFM structure where ideal electrodes are considered, $l_s \approx 0$, and no depolarization field is resulted due to the perfect balance of compensation and polarization charge

polarization charge attracts compensation charges from the metal electrode as they tends to be in close proximity with the ferroelectric surface. Providing the complete charge compensation no electric field is evaluated in short circuit condition, hence depolarization field is null. However, in reality either the screening length of the metal electrodes or the formation of a dielectric layer during the fabrication process has to be taken into account. It's not uncommon, in addition, during the deposition process of the ferroelectric layer the combination of different phases which means that the HfO_2 based material can be found in a mixed of paraelectric phase with the ferroelectric one. As mention in fig.3.2 one of the main aspect responsible for the formation of monoclinic and tetragonal phase (responsible for the paraelectric behavior) is the role of the thickness as by increasing it the probability of losing the ferroelectric behavior rises. The above mention cases are responsible for the formation of the depolarization field as the ferroelectric charge is not fully compensated by the screening charge. What need to be mention is that the depolarization field can not be

confined as the main factor which influences the nucleation and switching of domains but is the relationship with the coercive field and the depolarization field itself which impacts the performance of ferroelectric devices. When the depolarization field exceeds the coercive field a reduction of ferroelectric polarization is observed as the polarization reversal occurs, meaning that the number of switched domain into an opposite state is occurring due to the non-vanishing field inside the ferroelectric material. In this chapter a detail analysis on the depolarization field is held considering different kind of structure: from the metal-ferroelectric-metal (MFM) structure toward the metal-ferroelectric-insulator-metal (MFIM) to the metal-ferroelectric-metal-insulator-metal (MFMIM) with different area ratio. Concurrently the investigation of a semiconductor substrate instead of the metal one is held. We firstly built a circuit model where we analyse the parameter which influence the raising of the depolarization field and secondly we move our attention to the Landau free energy and see how the depolarization field could benefit the stabilization of negative capacitance state, one of the crucial aspect in the negative capacitance field effect transistor (NC FEFET). In appendixC we leave to the reader the impact of the depolarization field on the transition temperature of the ferroelectric layer while we neglect in the whole thesis project the influence on the temperature on the ferroelectric Landau free energy expression (eq(2.30) and eq(2.31) with $\alpha_T = 0$).

4.1 Circuit model for the evaluation of the depolarization field in MFIM structure

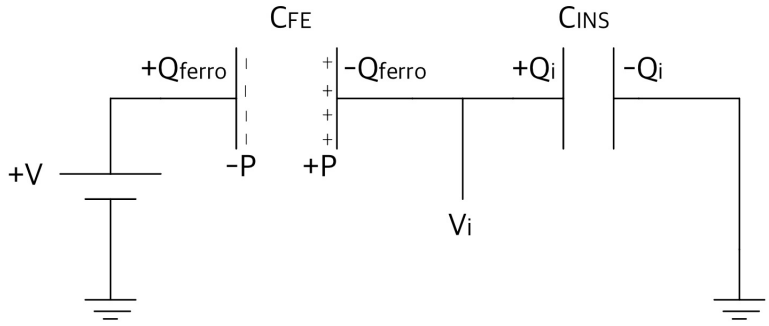


Figure 4.2: Circuit model of MFIM structure with ferroelectric capacitor in series with a dielectric capacitor. The depolarization field is evaluated by finding the field in the ferroelectric when $V = 0$

In fig.4.2 a simple circuit model is implemented in order to evaluate the depolarization field. Because of the formation of a passive layer, in the literature is usually called dead layer, due to imperfection in the fabrication process or dictated by the formation after the thermal annealing step of a dielectric phase the structure metal-ferroelectric-metal

(MFM) turns into metal-ferroelectric-insulator-metal (MFIM) structure. What is relevant to notice is that the dielectric in series with the ferroelectric layer is responsible of the depolarization field formation. It comes naturally that our scope is to define the parameters that influence its behavior and since it's one of the major drawbacks encountered in ferroelectric devices try to reduce as much as the ratio with the coercive field is lower than 1. According to fig.4.2 we define with C_{FE} the ferroelectric capacitance per unit of area and C_{INS} the dielectric capacitance per unit of area and we impose the continuity of the electric displacement field at the interface between the dielectric and the ferroelectric layer

$$D_{FE} = \epsilon_0 \epsilon_{FE} E_{FE} + P = D_{INS} = \epsilon_0 \epsilon_{INS} E_{INS} \tag{4.1}$$

By adding to (4.1) the condition

$$V = t_{FE} E_{FE} + t_{INS} E_{INS} = V_{FE} + V_{INS} \tag{4.2}$$

we can define the electric field in the ferroelectric E_{FE} and insulator electric field E_{DE}, eq(4.3) and eq(4.4)

$$E_{FE} = \frac{1}{t_{FE} C_0}(-P + C_{DE} V) \tag{4.3}$$

$$E_{DE} = \frac{1}{t_{DE} C_0}(P + C_{FE} V) \tag{4.4}$$

where the total capacitance per unit of area C_0 is defines as

$$C_0 = \epsilon_0 \left(\frac{\epsilon_{DE}}{t_{DE}} + \frac{\epsilon_{FE}}{t_{FE}} \right) = C_{FE} + C_{INS} \tag{4.5}$$

with ϵ_{DE} and ϵ_{FE} the dielectric constant of dielectric and ferroelectric layer and t_{DE} and t_{FE} the thickness of dielectric and ferroelectric region. In short circuit condition ($V = 0V$) from (4.3) the evaluation of the depolarization field is expressed as

$$E_{FE} = -P \left(\epsilon_0 \epsilon_{FE} \left(\frac{C_{INS}}{C_{FE}} + 1 \right) \right)^{-1} \tag{4.6}$$

As shown in eq(4.6) the field is in the opposite direction to the polarization inside the material which indicates the reduction of polarization when no bias is applied. This lead to the low data retention problem which degrade the performance of the device as it tends to reduce the memory time. In addition it increases its value for larger P. A possible solution is to work with minor loop where as a pros we impact on the remnant polarization by reducing its value but the reduction of coercive field clearly counterbalance the previous effect. As remark in the previous section the depolarization field per se is not a crucial factor but is the ratio between the depolarization field and coercive field which influence the switching of ferroelectric domains and as a consequence the memory behavior. What we left is the possibility to vary the capacitance ratio and it could be beneficial since by increasing the dead layer capacitance a reduction of the depolarization field is acquired. In fig.4.3 the effect of the capacitance ratio ($C_{FE} \propto 1/t_{FE}$) and of the polarization is illustrated. How the retention is influenced by E_{dep}? Considering the highest coercive

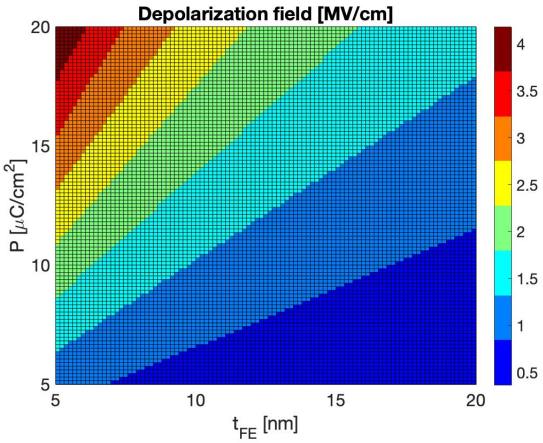


Figure 4.3: Depolarization field evaluated by varying the ferroelectric thickness from 5nm to 20nm and the ferroelectric polarization from $5\mu C/cm^2$ to $20\mu C/cm^2$. The dielectric thickness is set to $t_{INS} = 1nm$, whereas the dielectric constant of ferroelectric and oxide are respectively $\epsilon_{FE} = 21$ and $\epsilon_{INS} = 6.6$

field for hafnia-based ferroelectric $E_C \approx 2MV/cm$ then by looking at fig.4.3 the decay of polarization state and as a consequence the lose of memory data is assessed even for ferroelectric film thickness lower than $15nm$ when the remnant polarization is set to $P = 20\mu C/cm^2$. Let's thinking about the P-E curve of the ferroelectric (fig.2.7). When the electric field is double the coercive field ($E \approx 2E_C$) almost the entire polarization is either pointing upward or downward, indicating the stabilization of the ferroelectric state. From fig.4.2 the direction of the polarization is pointing from left to right. We may ask if the direction still remains the same when considering $t_{FE} = 5nm$ and $P = 20\mu C/cm^2$. By inspecting fig.4.3 the value of depolarization field is twice the value of E_C meaning that the majority of ferroelectric dipoles have switched toward the opposite state due to the effect of E_{dep}. To better explain explains the drawback of ferroelectricity in retain data we can evaluate the amount of compensation charge, defined by setting

$$Q_{FE} = Q_i \tag{4.7}$$

as the central node Q_i is electrically neutral from fig.4.2. When the bias voltage is zero the voltage across the ferroelectric is equal and opposite to the voltage across the dead layer (4.8)

$$V_{FE} + V_{INS} = \frac{Q_{FE} - P}{C_{FE}} + \frac{Q_i}{C_{INS}} = 0 \tag{4.8}$$

By merging (4.7) with (4.8) it follows

$$Q_i = \frac{C_{INS}}{C_{INS} + C_{FE}} P \tag{4.9}$$

The balance of the polarization across the ferroelectric layer and the compensation charge takes place only when the dead layer capacitance $C_{INS} \to \infty$. In fig.4.4 we report the

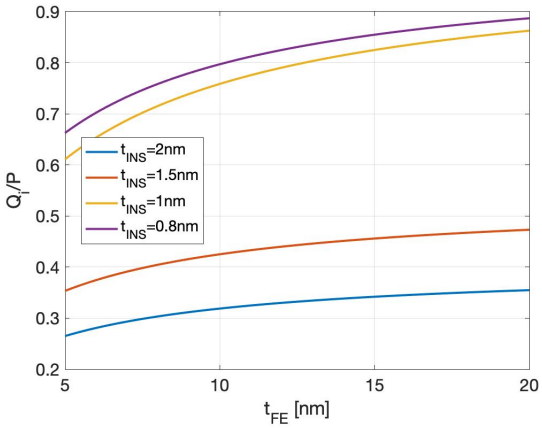


Figure 4.4: Fraction of P compensated by the electrodes as a function of ferroelectric thickness and at different value of t_{INS}

result of (4.9), specifically the fraction of polarization charge compensated by the metal electrodes is evaluated considering different dielectric thickness while varying the ferroelectric thin film from 5nm to 20nm. An almost 90% of compensation is reported for $t_{DE} = 0.8nm$ and $t_{FE} = 20nm$ indicating the road of reducing the dielectric thickness and concurrently introduce thicker ferroelectric material in order to reduce the changes on ferroelectric polarization when $V = 0$.

4.2 How the floating gate and the area ratio impact the depolarization field

In fig.4.5 we suggested four different structure for the evaluation of the depolarization field. Having already defined the MFIM stack, case a, we may discuss how the MFMIM stack and the role of the area ratio could potentially be beneficial to the reduction of the depolarization field and hence to the increase of data retention. By adding a floating metal between the ferroelectric and insulator as proposed in case b could influence the depolarization field as the ferroelectric material is now sandwiched between two conductive layers. This indicate that the complete compensation charge can be achieved despite the screening length contribution which still provide a non-negligible depolarization field. It is relevant to claim that the following conclusion we derive does not take care of the charging of the floating conductive layer. For such a reason and by neglecting gate leakage current through the layers the electrostatic boundary condition for the MFIM and MFMIM stack with the same area between the ferroelectric and the dielectric remains unchanged. Consequently we inspect the case c in details recalling that the formula will conduct to the case a and b respectively when ferroelectric area is equal to the insulator area ($A_{FE} = A_{INS}$). The electrical boundary conditions for the MFMIM stack with different

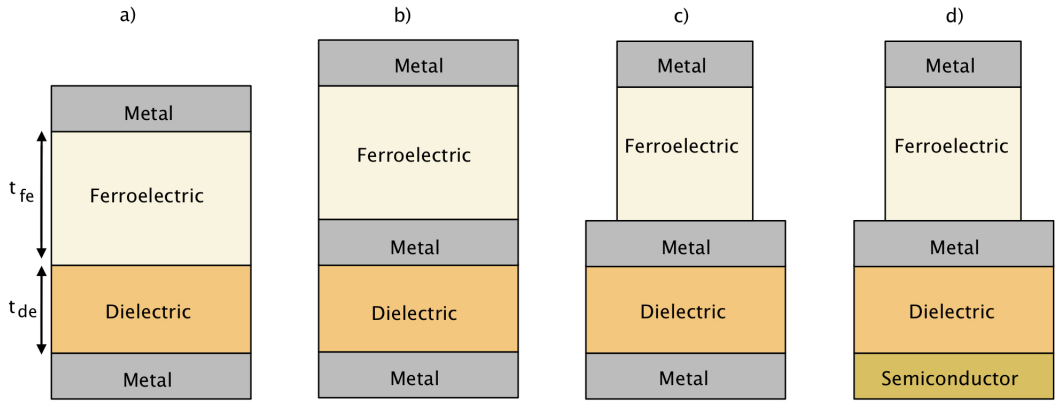


Figure 4.5: Four different structure employed for the evaluation of the depolarization field: (a) MFIM stack, (b) MFMIM stack and (c-d) MFMIM and MFMIS stack with different area ratio

area between the ferroelectric and dielectric is defined in eq.(4.10) and eq.(4.11)

$$D_{FE} = A_{FE}(\epsilon_0 \epsilon_{FE} E_{FE} + P) = D_{INS} = A_{INS} \epsilon_0 \epsilon_{INS} E_{INS} \tag{4.10}$$

$$V = t_{FE} E_{FE} + t_{INS} E_{INS} = V_{FE} + V_{INS} \tag{4.11}$$

It is convenient for the following analysis to define a new parameter called area ratio (AR)

$$AR = \frac{A_{FE}}{A_{INS}} \tag{4.12}$$

which gives the impact of the shrinking of the ferroelectric area with respect to the insulator area or vice-versa. By solving eq(4.10) and eq(4.11) we can evaluate the ferroelectric and insulator field

$$E_{FE} = \frac{1}{t_{FE} C_T}(-P \cdot AR + C_{DE} V) \tag{4.13}$$

$$E_{DE} = \frac{1}{t_{DE} C_T}(P \cdot AR + C_{FE} \cdot ARV) \tag{4.14}$$

with

$$C_T = C_{INS} + C_{FE} \cdot AR \tag{4.15}$$

By setting V=0, short circuit condition, the field across the ferroelectric layer becomes

$$E_{FE} = -P \left(\epsilon_0 \epsilon_{FE} \left(\frac{C_{INS}}{AR \cdot C_{FE}} + 1 \right) \right)^{-1} \tag{4.16}$$

This new formula of the depolarization field suggests three different degree of freedom: the polarization P, the ratio between the ferroelectric and insulator capacitance per unit of area

and the ratio between the ferroelectric and insulator area embedded in AR. Despite the first two of them has been already found in the MFIM and MFMIM stack, the role of the AR is inspected in this section. In fig.4.6 the depolarization field is evaluated considering insulator thickness $t_{INS} = 1nm$ while ferroelectric thickness ranging from $5nm$ to $20nm$ and insulator and ferroelectric relative permittivity of $\epsilon_{INS} = 6.6$ and $\epsilon_{FE} = 21$. Lastly the polarization is fixed to $P = -8\mu C/cm^2$. Before inspecting the result we recall that

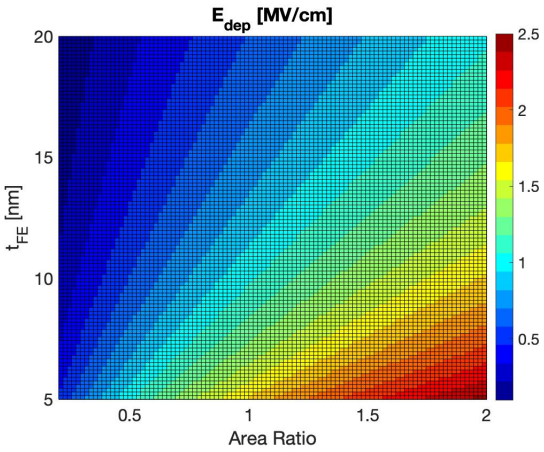


Figure 4.6: Depolarization field as a function of the ferroelectric thickness and AR, according to eq.4.16

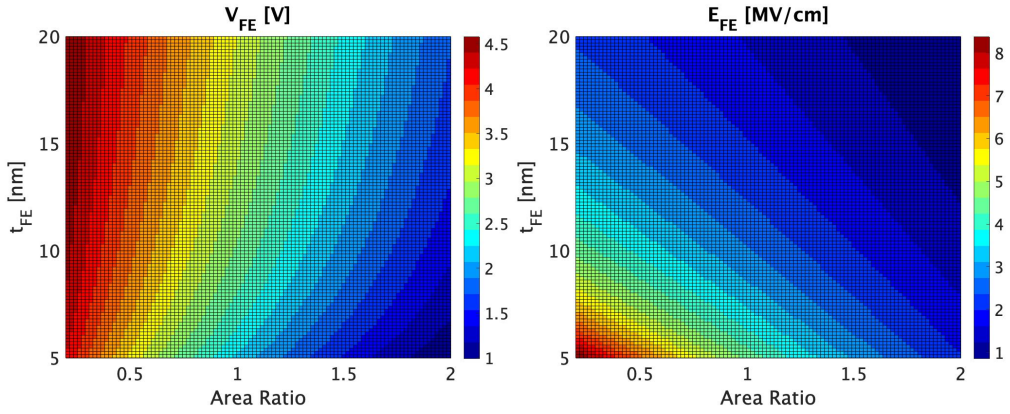
the coercive field of ferroelectric materials based on doped-hafnium oxide ranges from $E_C = [1,2]MV/cm$ and that we need to keep the ratio E_{dep}/E_C lower than 1 in order to ensure that only a small portion of the ferroelectric dipoles to flip. The following condition is encountered when considering AR lower than 1 as shown in fig.4.6. The area of the ferroelectric material has to be reduced with respect to the dielectric area as shown in case c of fig.4.5 where a shrink on the lateral direction of the ferroelectric material guarantee the condition $AR < 1$. A further analysis is the evaluation of the amount of voltage drop across the ferroelectric material when the applied voltage is different from 0. In fig.4.7 we demonstrate that the reduction of ferroelectric area lead to an increasing of voltage drop over the ferroelectric material. What happens is that by reducing A_{FE} the ferroelectric capacitance C_{FE} reduces as well as

$$C_{FE} = \frac{\epsilon_0 \epsilon_{FE} A_{FE}}{t_{FE}} \tag{4.17}$$

Because of the charge and voltage are related by

$$Q = C \cdot V \tag{4.18}$$

this cause that the voltage drop over the ferroelectric increases when the $AR < 1$ whereas tends to reduce to the case of $A_{INS} < A_{FE}$. The last condition indicates the reduction of the electric field across the ferroelectric which reduces the amount of polarization as the ferroelectric dipoles experience a lower field. The analysis performed in this section



(a) Voltage drop across FE (b) Electric field over FE

Figure 4.7: Voltage and electric field across the ferroelectric material when the applied gate voltage is set to 5V. The ferroelectric thickness as well as the area ratio has been varied to defined the coupling between the control gate and the ferroelectric layer

suggest to reduce the ferroelectric area compared to the dielectric area in order to reduce the depolarization field and increase the amount of voltage drop across the ferroelectric layer. This will imply that at lower AR the electric field over the ferroelectric layer increases and hence the remnant saturation. As a consequence a higher memory window is achieved for the BEOL FeFET with lower area ratio (the result is reported in fig.5.16).

4.3 Single-domain Landau Free Energy potential in the MFMIM stack

In this section a thermodynamic analysis of the MFMIM stack is presented where we define the overall free energy of the MFMIM stacks by showing how the stabilization of the ferroelectric domains become more pronounced at reducing area of ferroelectric and increasing the ferroelectric thickness. To start off the analysis we require the knowledge of Ginzburg-Landau theory reported in section2.2 and section2.3. The ferroelectric anisotropy constant α and β ($\gamma = 0$ as we deal with a second-order phase transition material) are determined by inverting eq.(2.21) and eq.(2.24) such that the coercive field and the remnant polarization of the ferroelectric material are $E_C = 1.5MV/cm$ and $P_R = 15\mu C/cm^2$. Furthermore because of the single-domain case the value of the domain wall coupling constant in eq.(2.30) is set to $\kappa = 0$. The overall free energy density of the ferroelectric is defined as

$$u_{FE} = \alpha P^2 + \beta P^4 + \frac{\epsilon_0 \epsilon_{FE}}{2} E_{FE}^2 \tag{4.19}$$

with the last term indicates the electrostatic self-energy contribution. The free energy density of the dielectric material is

$$u_{DE} = \frac{\epsilon_0 \epsilon_{DE}}{2} E_{DE}^2 \tag{4.20}$$

where we assume a linear and isotropic dielectric. We can now build up the total free energy of the system by considering two different cases: the first involves the study of the MFIM and MFMIM $AR = 1$ whereas the second the behavior of the free energy when the ferroelectric area is lower then the dielectric one MFMIM with $AR < 1$.

4.3.1 MFIM and MFMIM free energy and the depolarization effect

To evaluate the free energy of the system we need to sum up the ferroelectric free energy eq(4.19) and the dielectric free energy eq(4.20). Despite that we miss the evaluation of the electric field across the ferroelectric and dielectric layer. How they are defined? We need to use the same boundary condition as reported in section4.1. To avoid any redundant formalism we substitute eq.(4.3) into eq.(4.19) which gives the ferroelectric free energy as

$$u_{FE} = \left(\alpha + \frac{C_{FE}}{2t_{FE}C_T^2}\right) P^2 + \beta P^4 \tag{4.21}$$

with $C_T = C_{FE} + C_{DE}$ the sum of the ferroelectric and dielectric capacitance per unit of area. With the same procedure we substitute eq.(4.4) into eq.(4.20) so to get the free energy density of the dielectric

$$u_{DE} = \frac{C_{DE}}{2t_{DE}C_T^2} P^2 \tag{4.22}$$

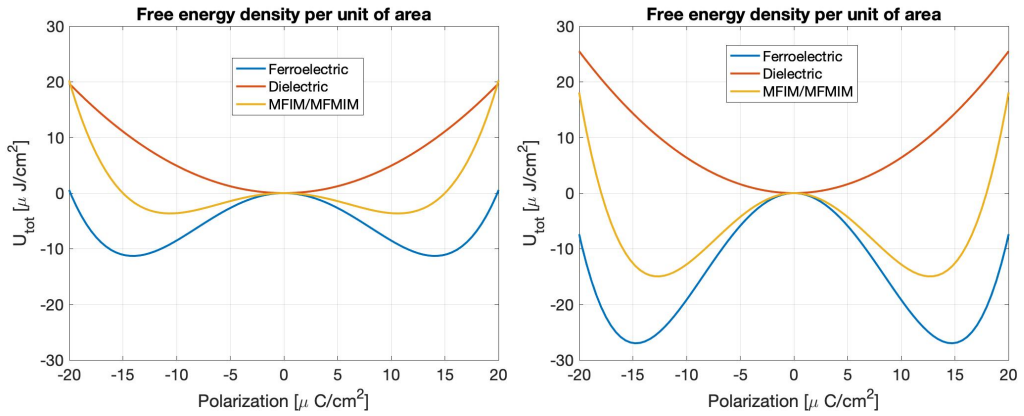
We can define the total free energy of the system per unit of area

$$U_{MFIM} = u_{FE} \cdot t_{FE} + u_{DE} \cdot t_{DE} \tag{4.23}$$

and replacing eq.(4.21) and eq.(4.22) into eq.(4.23) yields

$$U_{MFIM} = \left(\alpha t_{FE} + \frac{1}{2C_T}\right) P^2 + \beta P^4 \tag{4.24}$$

In fig.4.8 the evaluation of the free energy is reported considering two cases of ferroelectric thickness. In our research we're interested in calculating the barrier between the two minimum and the local maxima at $P = 0$. This can be explained by considering that for high depolarization field the free energy minimum stands at $P = 0$ which coincide with the creation of negative capacitance state where the ferroelectric need to operate in the negative-capacitance FET[24]. To ensure that the FeFET works as a memory we need to stabilize the two minimum in such a way that the energy difference, Δ, with respect to local maxima at $U_{MFIM} = 0$ is $\Delta > 0$. This indicates that by evaluating Δ we're simultaneously inspecting the impact of the depolarization field over the system [25]. As shown in fig.4.8a and in fig.4.8b the effect of the ferroelectric thickness is such that by increasing t_{FE} the total free energy gets closer to the ferroelectric one. Furthermore the free energy at the two local minima gets down with respect to the $U = 0$ meaning a better stability of the two states. The higher the barrier the better the stability of the system as we're dealing with memory this implicate that the switching from one state over the other is mostly influenced by the applied voltage and less by the effort of the depolarization field.



(a) Ferroelectric thickness $t_{FE} = 10nm$ (b) Ferroelectric thickness $t_{FE} = 20nm$

Figure 4.8: Free energy density per unit of area for the MFIM and MFMIM stack.

4.3.2 Free energy and the depolarization effect of the MFMIM with different area ratio

In this subsection the effect of the area ratio with respect to the total free energy is given. Because of the electrostatic boundary condition which defines the electric field over the ferroelectric and dielectric according to eq(4.13) and eq(4.14) the ferroelectric free energy and dielectric field energy are

$$u_{FE} = \left(\alpha + \frac{AR^2 \cdot C_{FE}}{2t_{FE}C_T^2}\right) P^2 + \beta P^4 \tag{4.25}$$

$$u_{DE} = \frac{AR^2 \cdot C_{DE}}{2t_{DE}C_T^2} P^2 \tag{4.26}$$

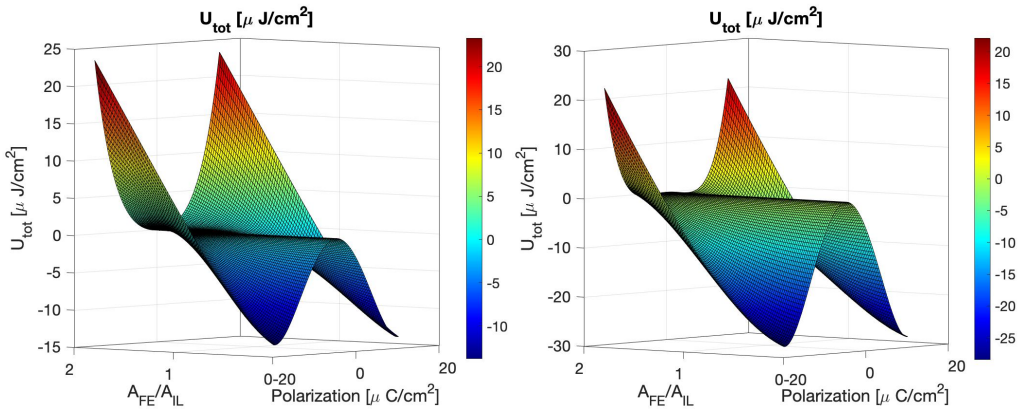
with

$$C_T = C_{DE} + AR \cdot C_{FE} \tag{4.27}$$

The total free energy density per unit of area accounting for the different area between ferroelectric and dielectric layer is evaluated in eq(4.28)

$$U_{MFMIM-AR} = \left(\alpha t_{FE} + AR^2 \frac{C_{FE} + C_{DE}}{2C_T}\right) P^2 + \beta P^4 \tag{4.28}$$

In fig.4.9 the total free energy of the system is evaluated at different AR. It's clearly visible that reducing the ferroelectric area will bring to the formation of the two energy minima at higher in magnitude energy values. This imply the increase of stability of the system as the difference from the free energy at the saddle point $P = 0$ increases in magnitude in agreement with the reduction of the depolarization field at reducing AR as shown in fig.4.6. In conclusion the Δ parameter defines as $\Delta = U_T(P = 0) - U_T(P = P_{min})$ is evaluated and shown in fig.4.10. For AR close to 1 and low ferroelectric thickness is



(a) Ferroelectric thickness $t_{FE} = 10nm$ (b) Ferroelectric thickness $t_{FE} = 20nm$

Figure 4.9: Free energy density per unit of area for the MFMIM stack at different area ratio

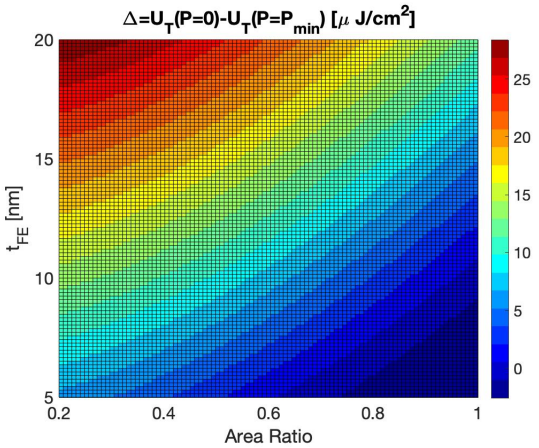


Figure 4.10: Variation of the free energy minima at different AR and ferroelectric thickness $\Delta = U_T(P = 0) - U_T(P = P_{min})$

reported a low value of Δ parameter which provides a further check on the role of the depolarization field. Specifically the higher is the Δ parameter the lower is depolarization field and hence the better we gain in terms of retention. In this study we claim that to ensure the stability of a ferroelectric state in short circuit condition a higher thickness of ferroelectric layer and low AR could be beneficial to limit the effect of the depolarization field. In the next section we explore the consequence of substituting the bottom metal electrode with a semiconductor layer. Our question could be: this entire formalism is gonna to drop when considering semiconductor instead of a metal layer?

4.4 The impact of semiconductor substrate

4.4.1 The depolarization field in the MFMIS structure at different area ratio

When substituting the bottom metal electrode with the semiconductor substrate what we could expect is to define a higher depolarization field as the presence of a non conductive layer provides less screening charges to the ferroelectric polarization. As a consequence a high chance of destabilization of the ferroelectric polarization is acquired indicating that a larger depolarization field will cause the formation of opposite polarization charge inside the ferroelectric material. In spite of that we need to contrast the behavior of semiconductor when is either in accumulation region or in strong inversion region. For the following analysis a p-type semiconductor substrate is chosen. In fig.4.11 we report

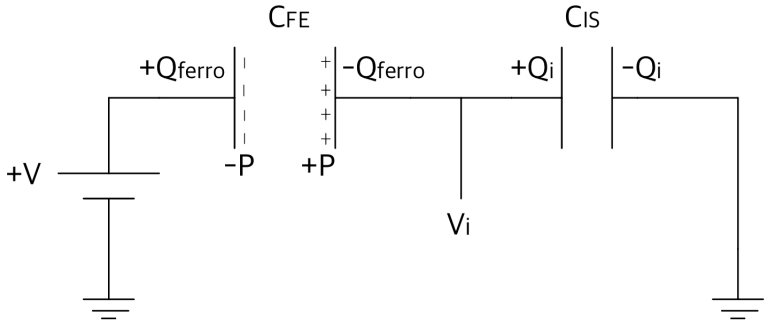


Figure 4.11: Circuit model of MFIM structure with ferroelectric capacitor in series with a dielectric capacitor.

the circuit model to evaluate the depolarization field when considering the MFIS and MFMIS stack. The main difference with respect to the MFIM case, fig.4.2, consists in the computation of the capacitance C_{IS} that is the series combination of the dielectric capacitance and the capacitance of the semiconductor layer:

$$C_{IS} = \frac{C_{SMC} + C_{INS}}{C_{SMC} C_{INS}} \tag{4.29}$$

Because the semiconductor capacitance is influenced by the semiconductor surface potential which varies according to the operating condition we defines two extreme case of C_{SMC} [26]. In accumulation region the $C_{SMC} \gg C_{INS}$ leading to

$$C_{IS} \approx C_{INS} \tag{4.30}$$

These because we have a large number of holes close or near the surface which cause to neglect the semiconductor surface potential ($V_S \approx 0$). Due to the surface accumulation we can look at the semiconductor like a metal which brings back the derivation found in

section4.1 and 4.2 for the depolarization field. In strong inversion region the formation of an inversion layer provides that the surface potential

$$V_S \approx 2\phi_B = 2V_T \log \frac{Na}{ni} \tag{4.31}$$

with ϕ_B the semiconductor bulk potential. Due to the dependence of the depletion region width with the surface potential

$$W_{SMC}(V_S) = \sqrt{\frac{2\epsilon_0 \epsilon_{SMC} V_S}{qN_A}} \tag{4.32}$$

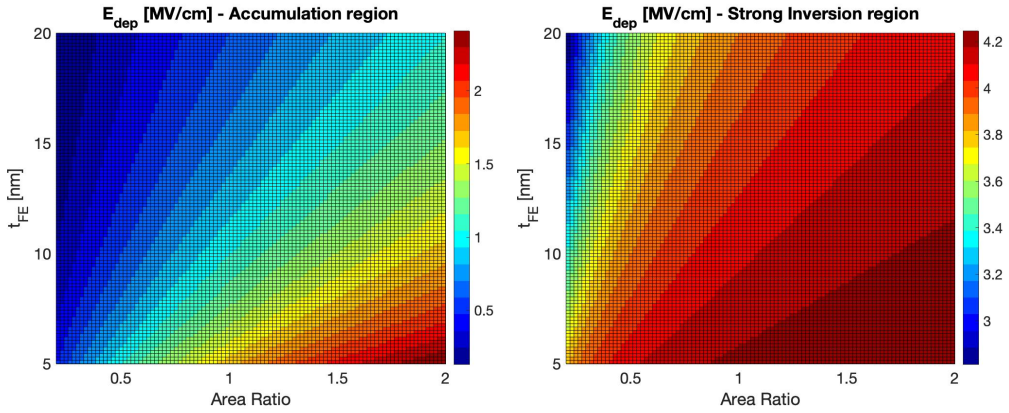
the minimum semiconductor capacitance is defined by substituting the surface potential in inversion region eq(4.31) in eq(4.32)

$$C_{SMC_{min}} = \frac{\epsilon_0 \epsilon_{SMC}}{W_{SMC}(V_S = 2\phi_B)} = \sqrt{\frac{\epsilon_0 \epsilon_{SMC} q N_A}{4V_T \log(N_A/n_i)}} \tag{4.33}$$

The series capacitance when in strong inversion region is

$$C_{IS} = \frac{C_{SMC_{min}} + C_{INS}}{C_{SMC_{min}} C_{INS}} \tag{4.34}$$

Having defined the two extreme cases for the evaluation of the series capacitance of the semiconductor layer and the dielectric layer we can now substitute eq.(4.30) and eq.(4.34) into eq(4.16) where C_{INS} is replaced by C_{IS}. The depolarization field shown in fig.4.12 highlight the behavior of the structure when the semiconductor channel has an accumulation layer, fig.4.12a or an inversion layer fig4.12b. At first glance the depolarization field



(a) Accumulation region (b) Strong inversion region

Figure 4.12: Depolarization field for the MFMIS stack when the semiconductor is in accumulation region and strong inversion region

when in accumulation region shows a different sign with respect to the inversion region.

This is justified by the changing of sign of the ferroelectric polarization P since when in accumulation the P points upwards, positive, whereas in strong inversion is negative. Because the depolarization field is the electric field whose direction is opposite to the polarization, as it tends to reduce P over time, this implies that when in accumulation, as the semiconductor behaves like a metal, a lower depolarization field is expected. Differently when the semiconductor is in inversion region as a non-negligible voltage drop across the semiconductor substrate will be generated in view of the fact that we need to create an inversion layer. The semiconductor capacitance is responsible for the higher depolarization field which could drastically impact the retention of the device when the semiconductor is in the inversion region.

4.4.2 A deep analysis on the depolarization field when considering a semiconductor substrate

What we miss in the investigation of the depolarization field in the MFMIS stack is the voltage distribution across the capacitor stacks. This need to be modified accounting for the semiconductor surface potential V_S and the work-function difference ϕ_{MS} between the top metal layer and semiconductor substrate [27].

$$V = V_{FE} + V_{INS} + V_S + \phi_{MS} \tag{4.35}$$

Because the depolarization field is evaluated in short circuit condition, $V = 0$, we can simply eq(4.35) by considering only the voltage across the ferroelectric and insulator layer

$$\hat{V} = V - V_S - \phi_{MS} = V_{FE} + V_{INS} \tag{4.36}$$

This procedure is compatible when the semiconductor substrate is both in the accumulation region and inversion region. Specifically when in accumulation the surface potential is negligible and

$$\hat{V}_{acc} = -\phi_{MS} = V_{FE} + V_{INS} \tag{4.37}$$

whereas in strong inversion by recalling eq.4.31 the voltage drop across the ferroelectric and insulator becomes

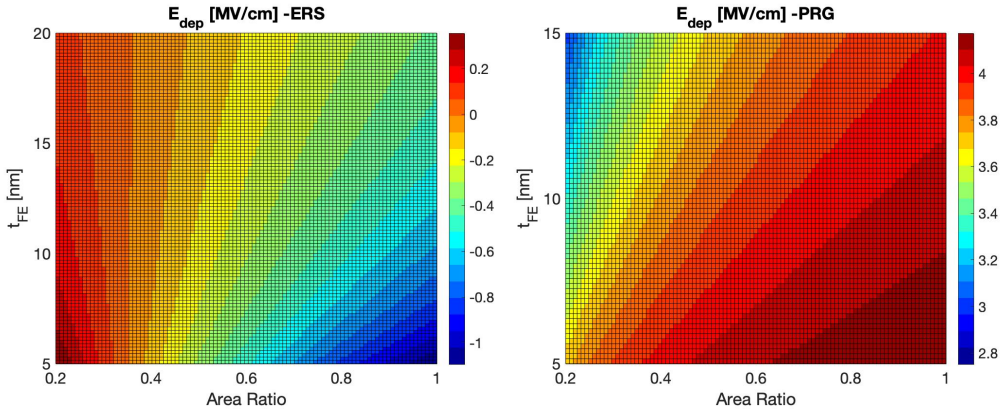
$$\hat{V}_{inv} = -\phi_{MS} - 2\phi_B = V_{FE} + V_{INS} \tag{4.38}$$

By adding the continuity of the electric displacement field eq(4.10) the depolarization field in accumulation and strong inversion yields to

$$E_{FE} = \frac{1}{t_{FE}C_T}(C_{DE} \cdot (-\phi_{MS}) - P \cdot AR) \tag{4.39}$$

$$E_{FE} = \frac{1}{t_{FE}C_T}(C_{DE} \cdot (-\phi_{MS} - 2\phi_B) - P \cdot AR) \tag{4.40}$$

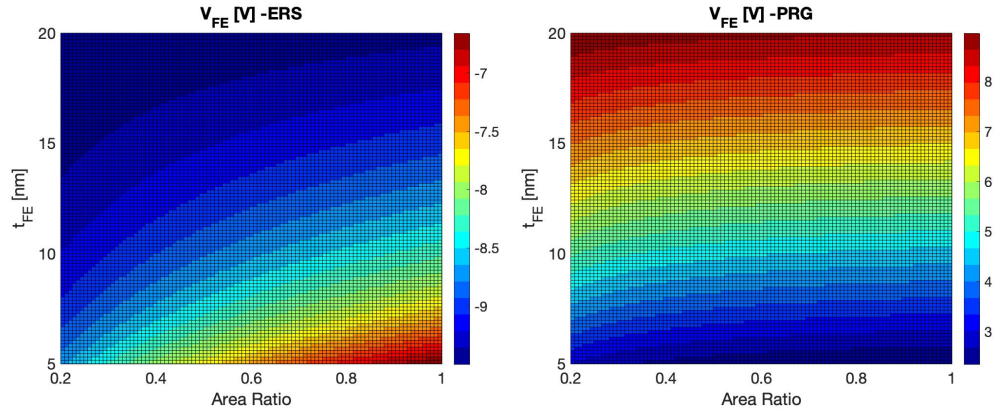
In fig.4.13 the depolarization field is presented where we claim with the program (PRG) condition the case in which the semiconductor substrate is in strong inversion condition whereas the erase (ERS) condition when in accumulation. PRG and ERS are well know



(a) Erase condition (b) Program condition

Figure 4.13: Depolarization field for the MFMIS stack when erase and program condition are applied

formalism in the FeFET devices. PRG indicates the condition where the potential applied on the gate is such that the ferroelectric polarization points downward attracting minority carrier close to the channel, strong inversion condition. In ERS the upward polarization of the ferroelectric genereted by a lower bias applied on the gate is responsible for the attraction of positive charge, accumulation condition, toward the semiconductor-insulator interface. Beside the PRG condition described in fig.4.13b where the depolarization field gets increase toward positive value at reduce ferroelectric thickness and increase AR the ERS condition need to be briefly investigated. In fig.4.13a is reported the change of sign of the depolarization field as we tends to lower area ratio. This lead to an increase of the ferroelectric polarization as the direction of E_{dep} is in the same as P. This will justify the trends when performing FeFET retention test which estimate a losing of PRG state despite the high stability in ERS condition. In 5.7 and 5.8 the retention result are obtained for the MFIS and MFMIS. In conclusion we evaluate the amount of voltage drop across the ferroelectric layer when the applied voltage $V_G = 10V$. This result will give us an idea on how much the area ratio can potentially increase the the amount of ferroelectric polarization since most of the gate voltage is gonna drop across the FE thin film and lower on the semiconductor and insulator layer. This is beneficial when performing endurance test as the dielectric is less stressed and less charge injection from the channel can result due to the lower field across it. From the endurance point of view the inter-layer dielectric breakdown can be mitigated when most of the field is across the FE [28] and according to fig.4.14 this justify the MFMIS structure with lower area ratio. What is the main drawback encountered when we both increase the ferroelectric thickness and reduce the AR? It's the poor coupling between the gate and the channel which hinders the main mechanism able to provide the formation of an inversion or accumulation region: the internal field over the ferroelectric, in substance the ferroelectric polarization. If the Coulomb coupling is increased instead we could guarantee a low operation voltage on the device beside the fast switching and low power operation and its CMOS compatibility which have been gained



(a) V_{FE} in ERS condition (b) V_{FE} in PRG condition

Figure 4.14: The amount of voltage drop across the ferroelectric layer when the applied gate voltage is $V_G = 10V$ for the MFMIS stack when ERS and PRG condition are applied

on the FeFET a strong attention as a memory device.

Chapter 5

Results and analysis

In this last chapter we aim to discuss the results obtained with Ginestra simulator in order to provide a complete understanding on the behavior of the ferroelectric FET for both the front end of line and back end of line gate stacks. Before introducing the device and the analysis of the transistor we dedicate a brief section on the ferroelectric capacitor (FeCap) structure in which a 1D problem is performed to investigate the role of the floating metal layer and the impact on the dielectric layer when in close proximity to the FE material, section5.1. As the crucial point is to focus on the retention trend of the device we firstly introduce varies combination of FeCap structure which could give a hint on the future outcome when discussing ferroelectric transistor. A complete analysis on the retention test is deeply carried out. The impact of reading is intensively describe as the main source of disturb of the polarization state and to properly minimize it a new reading is implemented. We conclude the chapter by showing the retention test for FEOL and BEOL FeFET where the last device is studied under different area ratio value ranging from 1 to 0.4. Two different set of Ginzburg-Landau parameter taken from the literature are implemented in the ferroelectric material in order to analyse the retention behavior of the device when different ferroelectric properties are presented. In the end the same test is run for different ferroelectric thickness ranging from $5nm$ to $20nm$.

5.1 Ferroelectric capacitor and the impact of screening

When dealing with ferroelectric devices an important figure of merit is the evaluation of the polarization-voltage (P-V) characteristics. From that measurement we can extract the two key parameters which enable to exploit the behavior and the working principles of the ferroelectric material: the remnant polarization and the coercive field. However because when dealing with FEOL FeFET the gate stack is made of meta-ferroelectric-insulator-semiconductor the influence of the dead layer (insulator) and the silicon (semiconductor) can drastically modify the functionality of the ferroelectric material and as a consequence a different P-V loop is obtained. In fig.5.1 the polarization-voltage characteristic is shown by using the P-V test describe in 3.3.2. The maximum and minimum gate voltage is set to

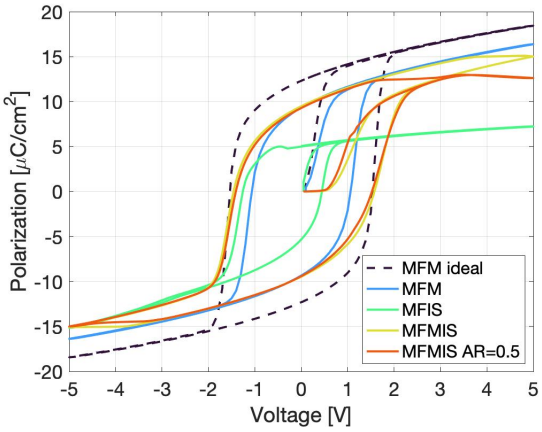


Figure 5.1: P-V characteristic for different FeCap structure: MFM with ideal contact, MFM when the screening length is considered, MFIS and MFMIS for different area ratio between the ferroelectric and dielectric area, respectively $A_{FE} = A_{DE}$ (yellow curve) and $A_{FE} = 0.5 \cdot A_{DE}$ (red curve)

$\pm 5V$ while the frequency is set to 10kHz. By inspecting the black and blue curve which correspond respectively to the exclusion of the screening lengths (ideal electrodes) and the inclusion of the screening charge, concentration gradient of electron density, inside the electrodes (close to the the metal and ferroelectric interface) we can provide a different value of remnant polarization as well as coercive field. This changes can be explain by defining the depolarization field when the ferroelectric capacitor is sandwiched between two metal layers as reported in [29] and in eq(5.1)

$$E_{dep} = -P\left(\epsilon_0 \epsilon_{FE}\left(\frac{C_{scr}}{2 \cdot C_{FE}} + 1\right)\right)^{-1} \tag{5.1}$$

where the C_{scr} indicates the capacitance of the finite screening length of the metal electrode

$$C_{scr} = \frac{\epsilon_0 \epsilon_m}{l_s} \tag{5.2}$$

with l_s the screening length and ϵ_m the dielectric constant of bound electron in the metal. Let's investigate the two cases where the screening length is finite and when it approaches to zero. In the first condition the l_s provide a non negligible depolarization field which results into a slightly reduction of the remnant polarization inside the ferroelectric material when the applied voltage is zero. This means that in the real case, when considering the MFM structure (e.g. ferroelectric tunnel junction devices) the depolarization field can repress the stability of the ferroelectric states due to imperfect screening charges between the metal-ferroelectric interface. When the $l_s \to 0$ the value of the depolarization field, according to eq(5.1), $E_{dep} \to 0$ which justify the fact that the polarization charges are perfectly compensated by the metal electrodes. This justify the higher value for the P_R as the polarization is entirely screened and no internal field is presented inside the ferroelectric layer.

Having discuss the Metal-Ferroelectric-Metal structure we will focus our attention on the Metal-Ferroelectric-Insulator-Semiconductor (MFIS) structure, fig.5.1 green curve. Two major differences are need to be highlight:

1. The different work function between the semiconductor and the top metal layer (ψ_{sm}). The effect is to generate a shift of the P-V curve by the same amount of ψ_{sm} along the x axis (the center is 0 for the MFM case).

2. The semiconductor capacitance, fig.5.2. As we doped the Silicon to be a p-type semiconductor substrate when the gate voltage is at negative potential the accumulation region is held. Due to the high numbers of holes, the free carriers will move close the semiconductor-insulator interface where they will provide a partial compensation charge from the polarization of the ferroelectric layer. When the applied voltage is

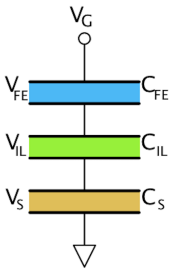


Figure 5.2: Capacitive voltage divider of the metal-ferroelectric-insulator-semiconductor structure

increases toward positive value the semiconductor is in depletion region and because the semiconductor capacitance is now compared or lower than the dielectric capacitance a drop of voltage on the Silicon substrate is provided to properly build up depletion charges. This imply that the P-V loop is asymmetric as the coercive field $E_C^+ \neq E_C-$ due to the different condition inside the semiconductor layer when is in accumulation and in depletion region.

3. The Source and Drain make easier the creation of the inversion region due to the lowering of the barrier which enhance the formation of minority carriers in close proximity to the inter-layer material. Because of the absence of them when the top metal electrode is at higher potential the P-V loop shows an almost line which indicates that the semiconductor is not able to provide enough minority carriers. In addition the voltage drop across the semiconductor layer reduces the electric field across the ferroelectric material providing a pinch of the hysteresis curve in the right portion of the P-V characteristic. The consequence of the following trend provide, as for the coercive field, a different and asymmetric value of the remnant polarization $P_R^+ \neq P_R-$.

How the floating gate can mitigate the criticalities of the MFIS structure? In fig.5.3 we inspect the value of the polarization that is preserved when no voltage is applied on

the FeCap and the loss of the polarization when the device reaches $\pm 5V$ and then go back to $0V$. The last parameter is a relevant figure of merit as it reveals how much the ferroelectric material is inclined to lose memory. The floating metal layer between the

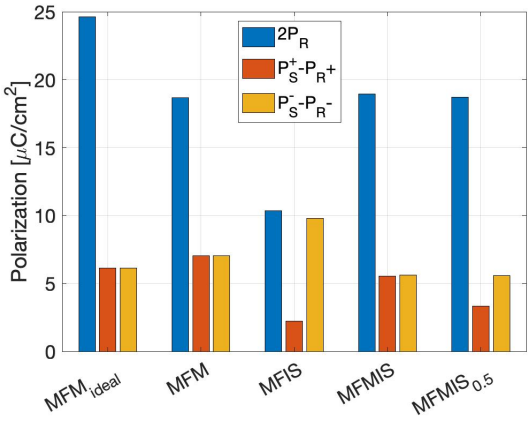


Figure 5.3: Remnant polarization, P_R and the difference between the saturation polarization P_S at $V_G = \pm 5V$ and the remnant polarization P_R at $V_G = 0V$

ferroelectric and the dielectric layer provides both a higher value of remnant polarization and a lower polarization loss with respect to the MFIS structure. Because the loss of polarization is associated to an increase of depolarization field this justify the role of the floating metal layer in stabilizing the ferroelectric state. In fig.5.4 the coercive

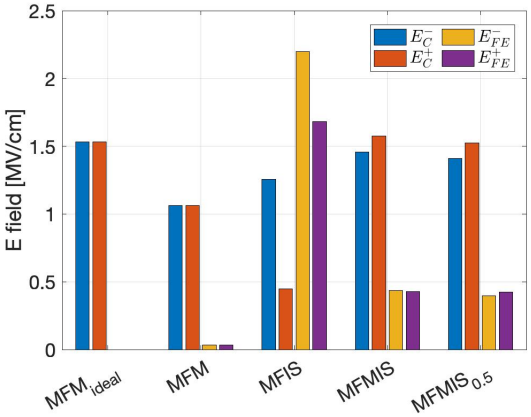


Figure 5.4: Coercive field, E_C and the electric field across the ferroelectric material, E_{FE}, when the applied voltage $V_G = 0V$

field and the depolarization field are sketched. As the ratio E_{dep}/E_C, fig5.5, provides an estimation of the capabilities of the ferroelectric material to retain data, it's clearly visible how the MFIS is effortlessly prone to lose the ferroelectric polarization over time.

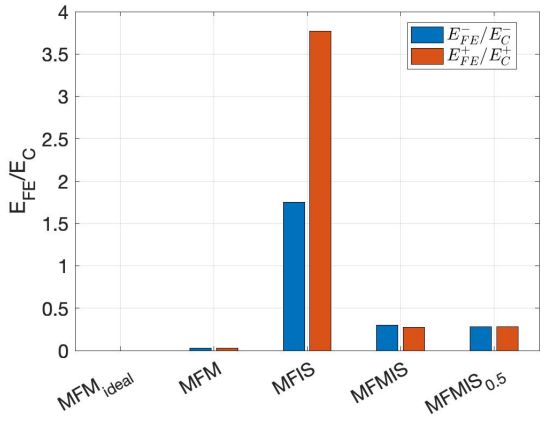


Figure 5.5: Coercive field and the electric field ratio. Higher values indicates the tendency of the memory state to be modified over time as the back-switching of the ferroelectric dipoles is provoked

On the other side the MFMIS structure has a less tendency on degrading the memory states of the ferroelectric devices as the floating gate guarantee an almost complete charge compensation reducing the internal field across the ferroelectric material. Having analysed the FeCap we will investigate how the presence of the floating metal layer can increase the retention time of the ferroelectric FET. In the meanwhile the retention study performed in GINESTRA is studied as the impact of reading and the polarization state on the writing operation will conduct to the main goal of the thesis project.

5.2 The role of the neutral reading and the impact of the ferroelectric thickness

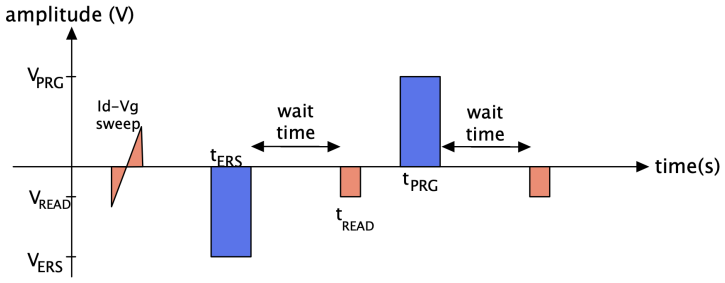


Figure 5.6: Gate voltage waveform scheme apply for the evaluation of retention for the ferroelectric FET

We're now ready to study the retention test describe in 3.4.2. Let's recall the gate voltage waveform scheme used in order to emulate the retention in the ferroelectric field

effect transistor, fig.5.6. The initial reading is used to verify if the device work correctly; once the fabrication process are completed the priority is to check if the transistor is active. As each die inside the wafer could be subjected to contamination it's critical to firstly prove the behavior of the device. The $I_D - V_G$ curve gives an absolute image of the state of the transistor. In fig.5.7 the trans-characteristic of the BEOL FeFET is shown for

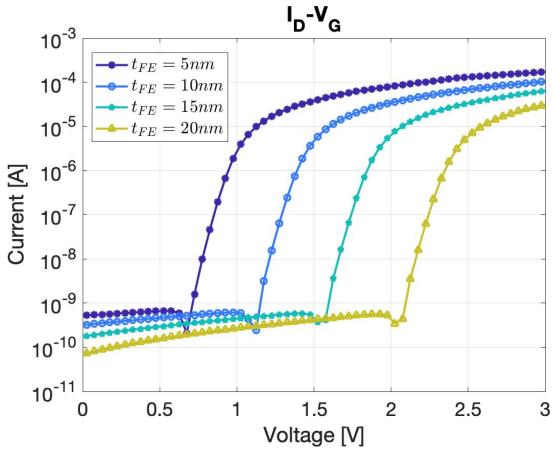


Figure 5.7: Transcharacteristic $I_D - V_G$ of the BEOL FeFET for different ferroelectric thickness

ferroelectric thickness ranging from $5nm$ to $20nm$. An increase of the threshold voltage (evaluated using the Constant Current Method) is notability visible. What is the feature which link the shift of the V_{th} with the t_{FE}? Let's consider the case when the $t_{FE} = 20nm$. By increasing the ferroelectric thickness the capacitance is getting smaller which means that more voltage is gonna drop across the material

$$t_{FE} \uparrow \implies C_{FE} \downarrow \implies V_{FE} \uparrow \tag{5.3}$$

As a consequence based on the voltage distribution across the different capacitor stacks a reduction of voltage is over the semiconductor channel.

$$V_G = V_{FE} + V_{IL} + \psi_S \implies \psi_S \downarrow \implies V_{th} \uparrow \tag{5.4}$$

As less voltage is dropping over the channel then we need to provide higher gate voltage in order to switch the device from the OFF to the ON state. What we miss is the inclusion of the polarization charge inside the ferroelectric material which through Coulomb coupling is able to modulate the conductivity of the semiconductor channel. Because neither erase nor program condition is provided to the device the polarization charge can be disregarded. By looking at fig.5.7 we exhibit the behavior of the transistor when is at the initial stage. Even so we could claim that the increase of the ferroelectric thickness implicates a fall of the gate-semiconductor coupling which result into the right shifting of the threshold voltage. Pushing to higher gate voltage will generate a disturb inside the ferroelectric state while performing the read operation. An alternative solution is the use of pulse

reading where the gate voltage is maintained fixed during the reading time. We still feed the ferroelectric state to a non negligible disturb but compared to the sweep reading it's by far the most reliable one.

5.3 Ferroelectric polarization in erase and program condition

Having defined the role of the sweep reading we move our attention on the program and erase state of the FeFET. As discuss in 1.3.3 the two write operation correspond respectively for the erase to the formation of HVT state (high-V_{th}) while LVT state (low-V_{th}) when the program operation is applied. They differ from the direction of the polarization inside the ferroelectric material dictated by the positive/negative value of the gate voltage applied. Using Ginestra we're able to inspect how the mean value of the polarization inside the ferroelectric HZO material behaves. This could give us a comparison on how the floating metal layer could properly stabilize the ferroelectric polarization due to the complete charge compensation provided by the bottom and top metal film. In fig.5.8 the applied voltage and the transient time, discussed in 3.4.2, are illustrated. Because tran-

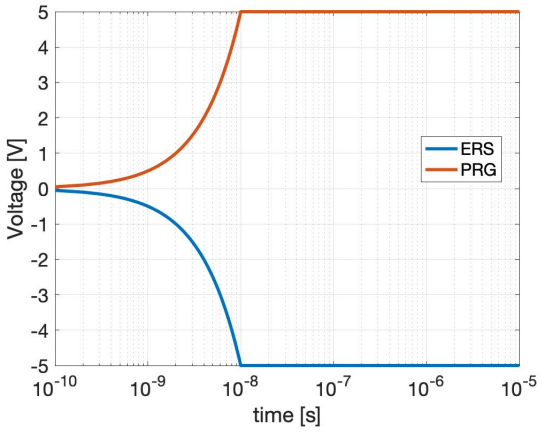


Figure 5.8: Erase and Program gate voltage waveform for the write operation of the FeFET device

sient simulation are performed a ramp up of the gate voltage is observed from $0.1ns$ and $10ns$ followed by the hold phase where the write voltage is preserve at high/low voltage over the time. As we are focused on the polarization trend when the device is set to either PRG or ERS condition we will show the polarization state of the ferroelectric in the time interval from $10ns$ to $10\mu s$. The polarization in ERS condition, fig.5.9, and in PRG condition, fig.5.10, makes clear the impact of the floating layer in increasing the amount of ferroelectric polarization due to the complete charge compensation. The imperfect screening in the FEOL FeFET enhance the depolarization field and is responsible for the loss of polarization. Both PRG and ERS condition spotlight the necessity to introduce

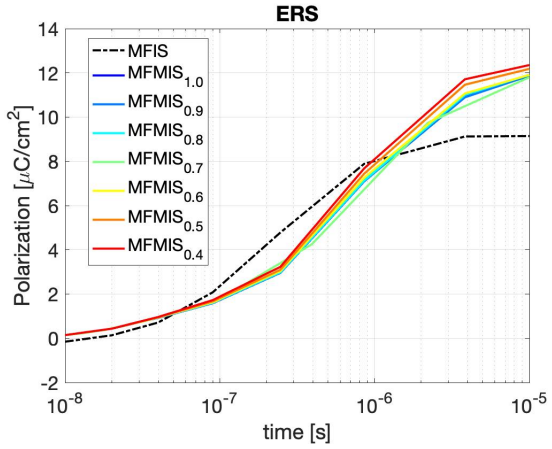


Figure 5.9: Mean value of the ferroelectric polarization along the y axis when the device is in erase condition

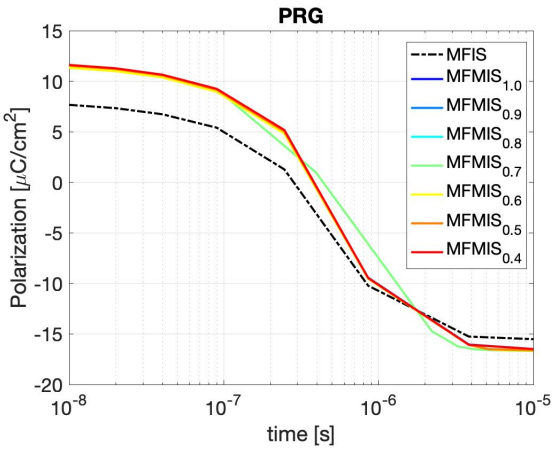


Figure 5.10: Mean value of the ferroelectric polarization along the y axis when the device is in program condition

the BEOL FeFET as a higher ferroelectric stability is acquired. As the area ratio is varied from $AR = 1.0 \implies l_{FE} = 50nm$ to $AR = 0.4 \implies l_{FE} = 20nm$ the slope of the ferroelectric polarization increases, red curve of fig.5.9 and fig.5.10. This behavior means that by reducing the area, enhancing the voltage drop across the ferroelectric layer and so the electric field, the speed of switching grows as well. Having characterized the trend of the polarization during the write operation our next step is the investigation of the ferroelectric polarization over time during the "wait-time" test. Preliminary to that we need to analyse how the test has been characterized as to mimic the physical study of retention performed in the laboratory.

5.4 Retention analysis

As we're interested in memory devices an important figure of merit is the study of retention. We dedicate this section to analyse how at simulation level the FEOL and BEOL FeFET behave by inspecting the polarization loss over the time. As discussed in 1.3.3 there are two relevant players which are responsible for the contribution of retention loss: the depolarization field and the charge trapping. We neglect in the entire thesis project the contribution of charge trapping as no defects in both semiconductor and ferroelectric layer are provided. By adding them we will mostly impact the ferroelectric polarization due to the screening of the trapped charge inside the FE. The main consequence is a decreasing of the coupling between the electric field across the ferroelectric and the semiconductor conductivity, [13] [30] [31]. The depolarization field investigated in chapter4 is therefore the main responsible for the low data retention of the ferroelectric devices we're going to examine, [14]. Having described the criticalities of the FeFET to retain data we move our focus on the retention study. Let's pose a simple question: how to mimic the real retention test inside Ginestra? From the experiment point of view, when the ferroelectric transistor is tested for the evaluation of the stability of the two memory states, the device is placed physically inside an oven at different temperature (usually $300\,K$ and $360\,K$ [28]). By doing so the device is not connected to any voltage sources: it's floating. To be consistent with the real test on each terminals (gate, source and drain) an ideal current generator (with infinite impedance) is attached and $0A$ is applied. In spite of that we will simultaneously compared the retention test when the device terminals are attached to voltage sources; specifically we ground the gate and the source/drain terminals. We will label by GND the previous test and with Floating the simulation using the true retention experiment. In fig.5.11 the polarization vs time is illustrate for the BEOL FeFET for two

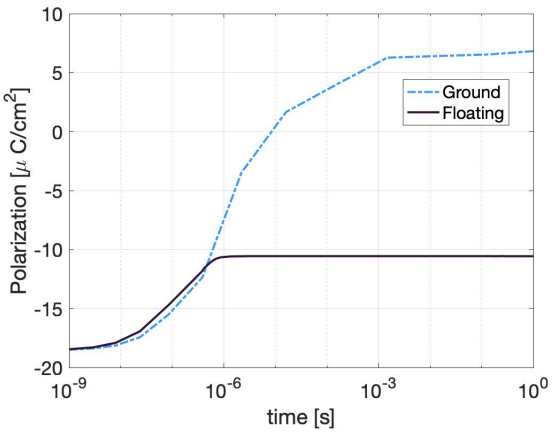


Figure 5.11: Mean value of the ferroelectric polarization at different wait time after PRG for the BEOL FeFET with area ratio $AR = 1$

different wait time tests

- GND: the terminals are set at $0V$

- Floating: an ideal current generator is attached at each terminals and $0A$ is applied

What is the principle effect in forcing the electrode to $0V$? Fig.5.11 clearly shows a loss of polarization over time when the terminals are grounded; moreover the sign of polarization is changed too. This phenomenon is dictated by the creation of a counteracting field since when the $V_G = 0V$ we still perturb the polarization state as the contribution of the different work function between the semiconductor and the metal enable the strong retention lost. In fig.5.12 by showing the band diagram we can further highlight the

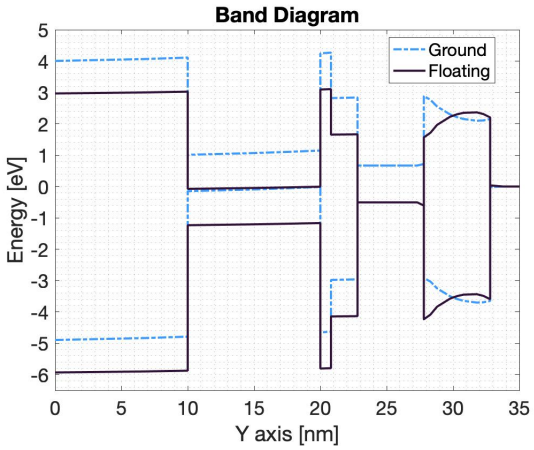


Figure 5.12: Band diagram for the BEOL FeFET with area ratio $AR = 1$ after $1s$ of waiting time

two different approach when performing retention. By looking at the ferroelectric region $27.8nm < y < 32.8nm$ is possible to notice the change of potential inside the material derived from the distinct value of the polarization at $t = 1s$ of waiting time reported in fig.5.11. Additionally the semiconductor surface potential is modified as well. The GND condition will lead the semiconductor to reduce the number of electrons inside the channel. As the retention test results are performed after the program condition where a high concentration of electrons close to the interface is present due to the coupling with the ferroelectric polarization what the ground enable is a substantially deprivation of minority carriers. The following analysis makes clear the need to move toward the floating retention test which are close, from the simulation point of view, to resemble the real retention operation. We conclude the retention analysis by reporting in fig.5.13 the evolution of the band diagram when different waiting time are performed, specifically from $t = 1ns$ to $t = 1s$. The blue curve, waiting time set to $1ns$, indicates a higher field across the ferroelectric material, hence a better stability of the ferroelectric polarization. The reason is because the ferroelectric material per se generates dipoles and so electric field. The more we're capable in storing the field the higher the retention of the device. As discussed previously the depolarization field, opposing to the direction of polarization, will tend to hammer the storing field leading to a reduction of data storage over time. In fig.5.13 when the time of wait after the reading operation is set to $1\mu s$ the slope of the ferroelectric band diagram is less sharp because of the contribution of the depolarization

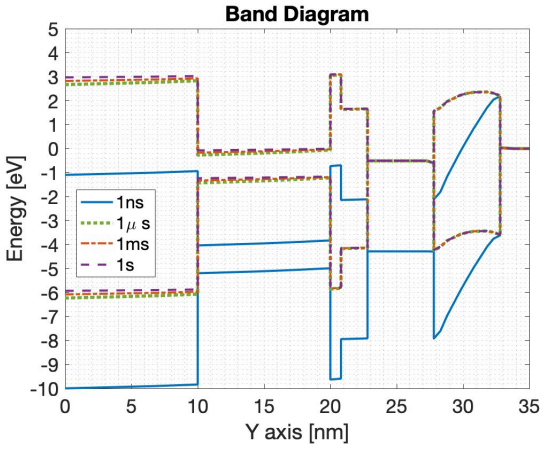


Figure 5.13: Band diagram evolution as a function of different waiting time for the BEOL FeFET with area ratio $AR = 1$

field that diminish the internally-generated voltage on the ferroelectric material and lower the coupling between the channel. How the band diagram in the FEOL FeFET changes as a function of waiting time? Due to the presence of an insulating layer in close contact

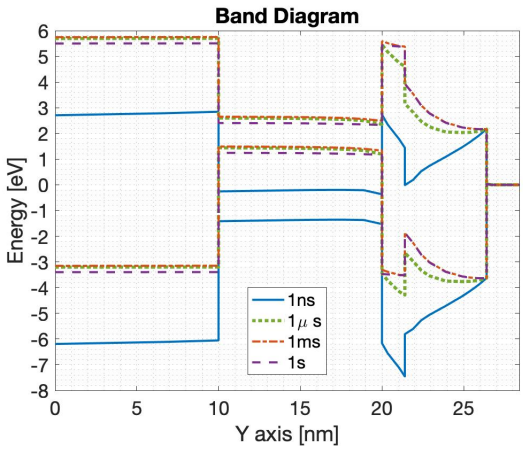


Figure 5.14: Band diagram evolution as a function of different waiting time for the FEOL FeFET

with the ferroelectric material we expect higher loss of polarization as the depolarization field will tend to reduce the memory retention time. In fig.5.14 we find out that the semiconductor channel is exited from the inversion region when the wait time is $1\mu s$. Moreover the slope of the potential inside the ferroelectric has changed sign. This indicates that the depolarization field has provided a switching of the ferroelectric dipoles. A loss of polarization and hence of the memory state is obtained for the FEOL FeFET device while the device is in the "wait condition" after the program operation.

5.5 Sweep Reading and the perturbation of the memory state

In this section we explore the reading operating, specifically we will inspect the condition when the gate voltage is swept from $-V_R$ to V_R (by V_R we indicate the maximum absolute value of the voltage applied) in order to evaluate the memory state of the device [32]. Furthermore the introduction of disturb reading is studied as well since this kind of operation can potentially lead the state to be ruin by the same reading voltage applied. Before discussing the concept of disturb we will show how the memory window of the ferroelectric FET is evaluated by showing the trans-characterisitic of the transistor when the device is read after program and after erase operation. In fig5.15 the $I_D - V_G$ behavior of the BEOL FeFET with area ratio 0.6 is reported using a sweep reading on the gate from $-3.5V$ to $3.5V$ during a time interval of $100ns$ while the drain voltage is fixed at $0.1V$. In 1.3.3 we report the concept of the memory window which is defined by the different

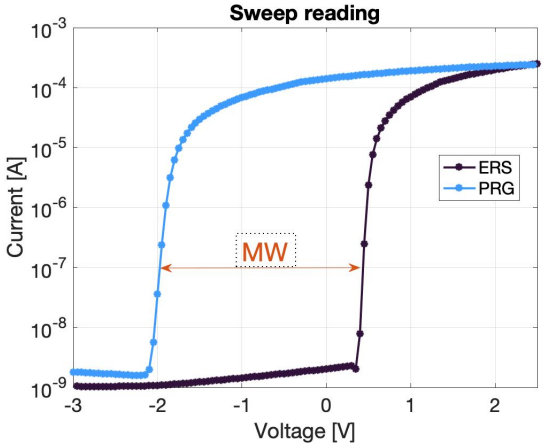


Figure 5.15: Memory window for the BEOL FeFET with area ratio $AR = 0.6$ considering a wait time of $1ns$

threshold voltage of the two memory state:

$$MW = V_{th_{ERS}} - V_{th_{PRG}} \tag{5.5}$$

A simplified version for the definition of the threshold voltage is through the use of the constant current (CC) method, [33]. It's mostly employed for its easy of evaluation as it defines V_{th} as the voltage corresponding to a constant drain current values, typically set to $10^{-7} \times W/L(A)$ with W and L indicating the width and length of the channel. The drawback of this approach which is at the same time its main advantage is the dependence of the chosen value of the drain current. Here for ease of convenience the drain current for the evaluation of program and erase threshold is set to $0.1\mu A$ which defines $MW \approx 2.5V$. We re-run the same test for different area ratio as we will expect an increase of the MW when the area of the ferroelectric is by far lower compared to the MOS gate stack. The cause is related to the higher voltage drop across the ferroelectric material which enables

a complete switching of ferroelectric domain for the same gate voltage applied. In fig.5.16 we report the memory window as a function of different area ratio between the ferroelectric and the FEOL gate stack. The following result are in good agreement with [34] and [35]. Both articles claim the increase of memory window value in the BEOL FeFET due to the higher field across the MFM capacitor. Furthermore in fig.5.17 we report the evaluation

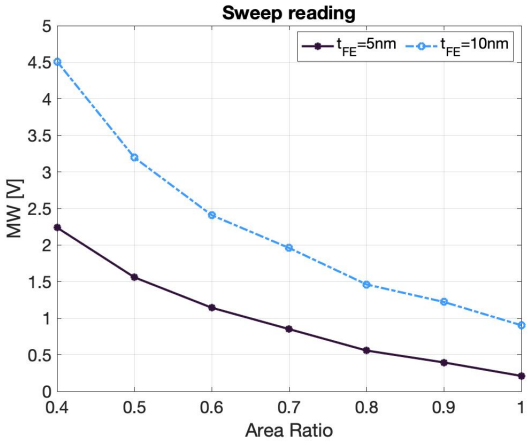


Figure 5.16: Memory window for the BEOL FeFET with ferroelectric thickness $t_{FE} = 5nm$ and $t_{FE} = 10nm$

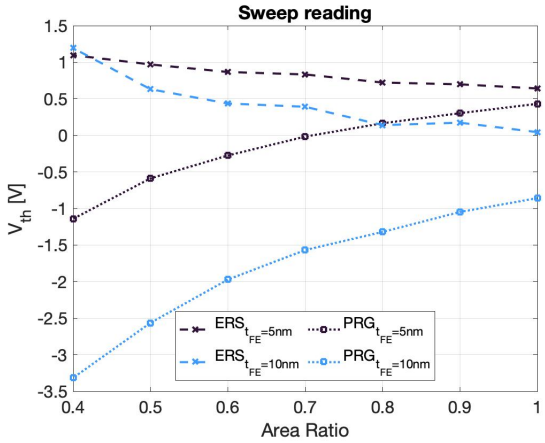


Figure 5.17: Erase and Program threshold voltage for the BEOL FeFET with ferroelectric thickness $t_{FE} = 5nm$ and $t_{FE} = 10nm$

of the threshold voltage when the device is read after being in ERS or PRG condition. The trends highlight a high change for the PRG state as for the $t_{FE} = 10nm$ the threshold voltage ranges from $1V$ ($AR = 1.0$) to $\approx 3.5V$ ($AR = 0.4$) indicating that for the low area ratio the reading should be performed by ramping the gate voltage at higher values in order to properly reach the $0.1\mu A$ for collecting the V_{th} data. The following outcome

implies that by performing the sweep reading we inevitably stress the stored memory state. A disturb of the cell during the reading operation will inevitably lead the device to a poor data retention as the probability of reversing the ferroelectric state when ramping between a negative and positive voltage is drastically favourable. Furthermore by recalling the second definition given in 1.2.4 for the memory window:

$$MW = 2 \times E_C \times t_{FE} \tag{5.6}$$

we point out that for ferroelectric thickness higher than the one reported in fig.5.16 higher reading voltage are gonna to be selected which makes unavoidable the risk of disturbing the cell. Let's consider for instance $t_{FE} = 20nm$ and a value of coercive field of $1.5MV/cm$ (HfO_2 coercive field ranges from $1MV/cm$ to $2MV/cm$). According to eq(5.6) the theoretical memory window is $MW = 6V$ which intimate the need of applying after the PRG/ERS condition a large voltage on the gate terminals if we want to read the high memory window of the device. This turns to the concept of perturbation of the memory state which is further enhance when the theoretical memory increases. For this reason we will discuss in the next section the use of pulse reading instead of the sweep reading as it can provide less stress on the ferroelectric polarization. We conclude the sweep reading discussion by showing the memory window result for the BEOL FeFET device when different sweep reading are applied:

- TEST1: Gate voltage in Read after ERS from $-3.5V$ to $3.5V$ while for Read after PRG $3.5V$ to $-3.5V$
- TEST2: Gate voltage in Read after ERS from $-2V$ to $2V$ while for Read after PRG $2V$ to $-2V$

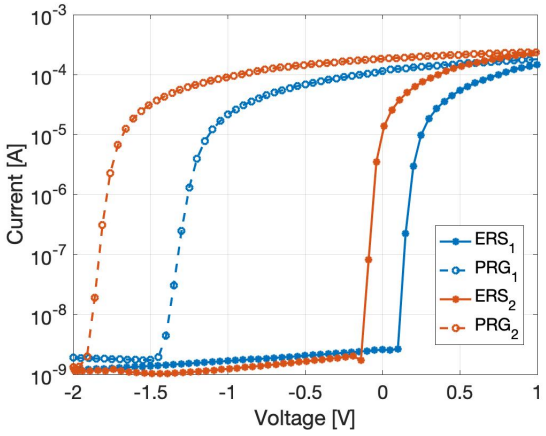


Figure 5.18: MW comparison when different reading voltage are applied in the BEOL FeFET with $AR = 0.8$

The $I_D - V_G$ characteristic for the two different tests is reported in fig.5.18 while the memory window is reported below:

- MW TEST1 1.46V
- MW TEST2 1.74V

The dissimilar memory window obtained through the modification of the maximum voltage applied when reading further justify the use of pulse reading. When we applied high voltage on the gate terminal to read the state we inevitably disturb the ferroelectric polarization and the impact of it is further enhance by increasing V_R. Moreover the read after program has been modified in order to reduce as much as possibile the stress on the ferroelectric state. As the PRG condition is held when the positive gate voltage is applied which lead to switch the ferroelectric dipoles by pointing them downward, it seems natural to reverse the reading by ramping the gate from the higher positive voltage to the higher (in absolute value) negative voltage (e.g $3.5V$ to $-3.5V$). If we kept the same gate waveform scheme for the Read after PRG we could provide to the ferroelectric polarization a high perturbation. The reason is because the negative potential on the gate will be responsible to the partially back-switching of the ferroelectric dipoles with the consequence of shifting the V_{th} toward positive values. The effect will be the formation of a small memory window and a loss of polarization state over time. In order to overcome the previous issue correlated to the gate voltage ramping from $\mp V_R$ to $\pm V_R$, a selected gate voltage value is applied.

5.6 Point Reading

The point reading is performed in our thesis project for the evaluation of the retention comparison between the FEOL and BEOL FeFET. As the name suggest we simply provide a gate voltage pulse on the device while drain voltage remains unchanged with respect to the sweep reading approach. In fig.5.19 we report the value of the gate voltage used

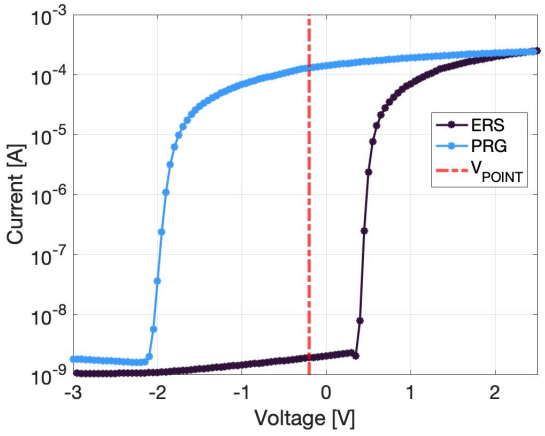


Figure 5.19: $I_D - V_G$ characteristic for the BEOL FeFET obtained using the sweep reading vs the point reading approach

throughout the retention analysis toghether with the $I_D - V_G$ curve (the last obtained

with the use of sweep reading). A value of $V_R = -0.2V$ on the gate is set inside the simulation tool to reduce the disturb of the cell. Specifically by comparing the trans-characteristic of the two states choosing a gate pulse voltage close to zero could guarantee a higher resolution for the comparison of the ON and OFF current. Furthermore during experimental test the point reading is implemented because of the detection of the current, drain current, is evaluated. Having explain how the point reading is performed we may ask if the device can still be perturb while a single gate voltage is applied. In fig.5.20 the

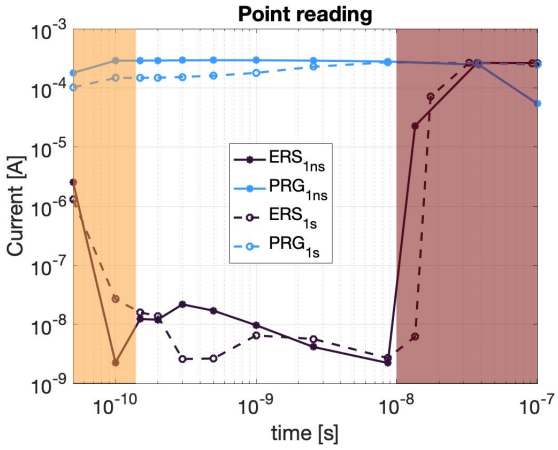


Figure 5.20: Drain current when the device, BEOL FeFET $AR = 0.8$, is read after been in PRG and ERS condition for two different waiting time: $1ns$ and $1s$

drain current of the BEOL FeFET has been evaluated using a read voltage of $-0.2V$ for a time of $100ns$. Let's inspect the whole time interval included in fig.5.20:

- time $[0\,s; 10^{-10}\,s]$: we will neglect the first two points as the numerical methods used could generate not truthful results. For this reason we disregard the orange region because of the non optimal convergence of the simulator.

- time $[10^{-9}\,s; 10^{-8}\,s]$: *free disturb window*. This time interval is the one which enable to extract the ON and OFF current as no perturbation of the device is presented. The experiments are conducted in these regime; specifically we extract a single value of ERS and PRG current at a specific time where we collect the data used in the retention analysis.

- time $[10^{-8}\,s; 10^{-7}\,s]$: long pulse on the device lead to perturb the ferroelectric state. This unexpected disturb in the ERS current is the effect of the *accumulative switching* [36]. The main cause is dictate by the fact that the memory state is influenced by both the applied voltage as well as the amount of time the signal is held. As a low amplitude voltage is applied on the gate we need a repetitive number of pulses or an high reading time to provide a complete switching of the ferroelectric state. High voltage and small pulses or low voltage and long pulses creates the condition of accumulation of the ferroelectric dipoles with the consequence of providing a

complete FE switching. The previous effect is elucidated in the read after ERS, red rectangle, for both waiting time considered. This demonstrate that the studied reading operation still provide disturb on the ferroelectric device.

Before discussing the retention results we point out the role of disturb reading which should be critically considered for the ferroelectric devices. As the applied voltage can impact the ferroelectric internal field a trade off between the two previous reading technique should be regarded. If sweep reading is applied we could damage the cell as higher gate voltage need to be applied for the detection of the two different threshold voltage. This means that the two states are both perturbed during the operation. The second technique which involve the use of point reading can generate less stress to the cell as a single value of gate voltage close to zero is applied. In spite of that we still observe the disturb of the memory state as the accumulative switching can flip the ferroelectric polarization when long time interval and short pulse are used. How to get rid of the disturb phenomenon? By the evaluation of a disturb free window where the ferroelectric polarization is stable and is not altered by the signal applied. Hence we will collect the drain current data by intersect the I_D vs t, fig.5.20, by selecting a time $t = 5ns$ (within the free disturb window) for the retention outcome.

5.7 Retention results

In the final section we will report the retention result obtained for the FEOL and BEOL (area ratio varying from 1.0 to 0.4) FeFET with waiting time of $1ns$, $1\mu s$, $1ms$ and $1s$. The Ginzburg-Landau parameters used are [22] $\alpha_1 = -1.03e9[m/F]$, $\beta_1 = 3.5e10[m^5/(FC^2)]$ and $\rho_1 = 1750\Omega m$ (TEST1) and [37] $\alpha_2 = -5.31e8[m/F]$, $\beta_2 = 5.22e9[m^5/(FC^2)]$ and $\rho_2 = 100\Omega m$ (TEST2) with ferroelectric thickness of $5nm$, $10nm$, $15nm$ and $20nm$. The result for the G-L of [37] are reported in fig.5.21,fig.5.23,fig.5.25 and fig.5.27. To properly investigate which of the two state is more prone to decay over time we illustrate the program and erase current in fig.5.22a and fig.5.22b for the $t_{FE} = 5nm$; fig.5.24a and fig.5.24b for $t_{FE} = 10nm$ and so forth. The same approach is given in TEST2 where in fig.5.29,fig.5.31,fig.5.33 and fig.5.35 the retention results using the G-L of [37] is provided.

5.7.1 TEST 1: Ferroelectric thickness 5nm

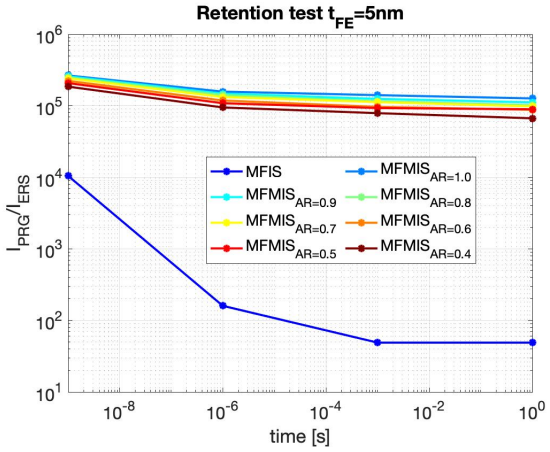
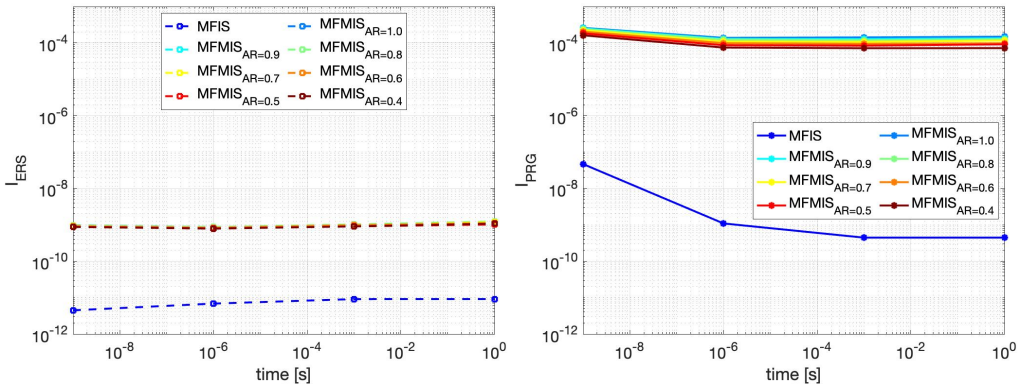


Figure 5.21: Retention result for the BEOL and FEOL FeFET with $t_{FE} = 5nm$



(a) ERS current (b) PRG current

Figure 5.22: Erase and Program current as a function of the waiting time for the BEOL and FEOL FeFET with $t_{FE} = 5nm$

5.7.2 TEST 1: Ferroelectric thickness 10nm

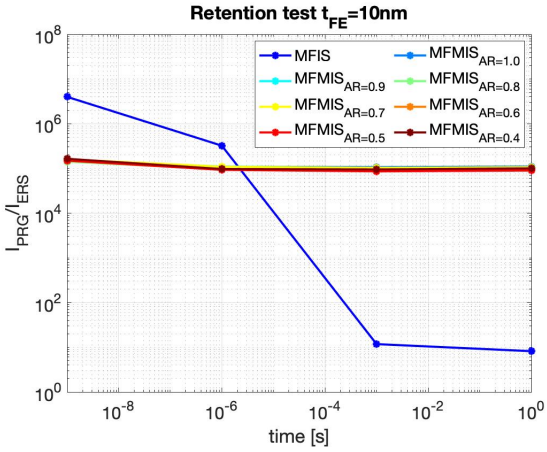
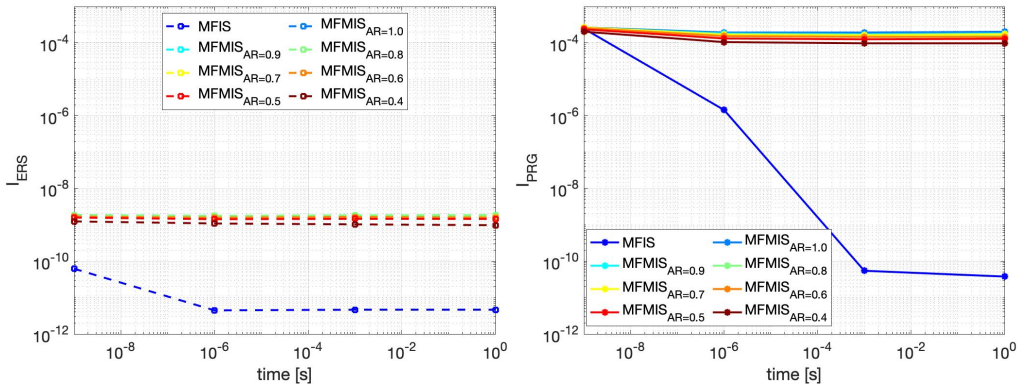


Figure 5.23: Retention result for the BEOL and FEOL FeFET with $t_{FE} = 10nm$



(a) ERS current (b) PRG current

Figure 5.24: Erase and Program current as a function of the waiting time for the BEOL and FEOL FeFET with $t_{FE} = 10nm$

5.7.3 TEST 1: Ferroelectric thickness 15nm

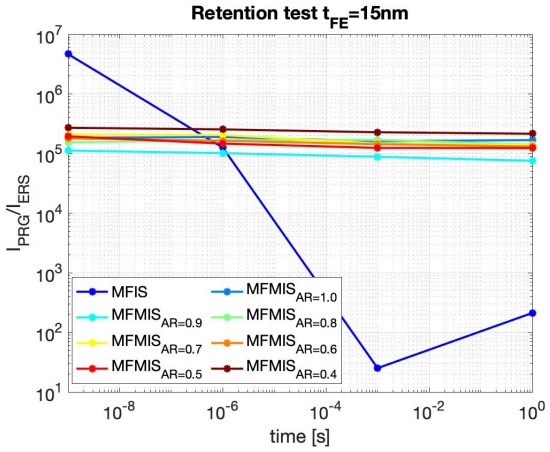
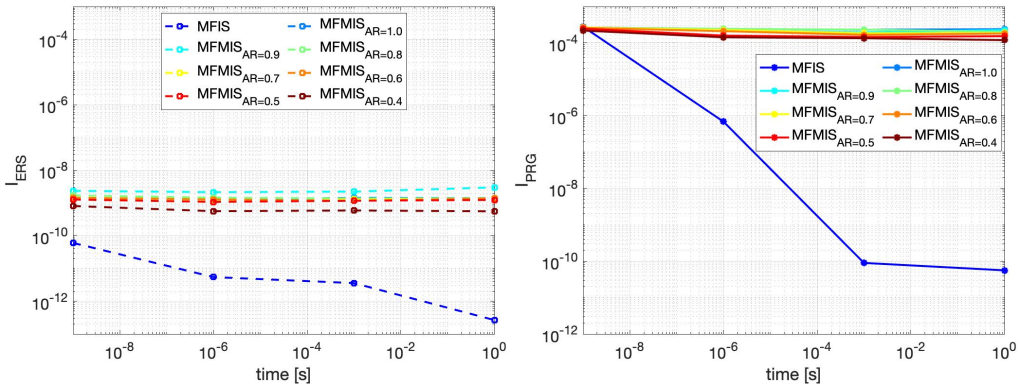


Figure 5.25: Retention result for the BEOL and FEOL FeFET with $t_{FE} = 15nm$



(a) ERS current (b) PRG current

Figure 5.26: Erase and Program current as a function of the waiting time for the BEOL and FEOL FeFET with $t_{FE} = 15nm$

5.7.4 TEST 1: Ferroelectric thickness 20nm

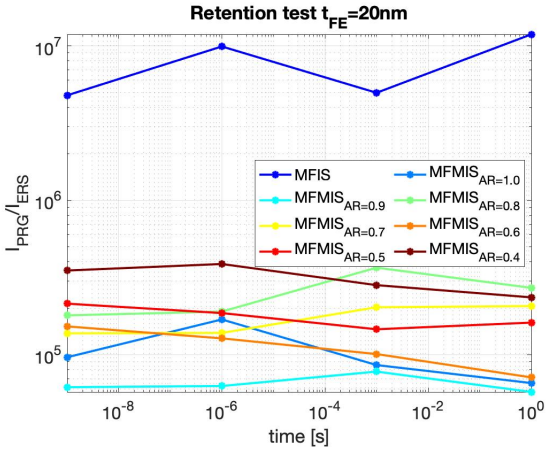
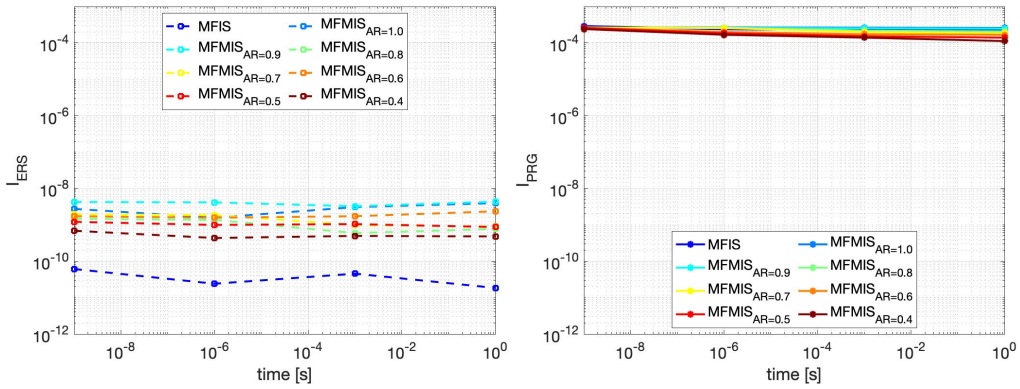


Figure 5.27: Retention result for the BEOL and FEOL FeFET with $t_{FE} = 20nm$



(a) ERS current (b) PRG current

Figure 5.28: Erase and Program current as a function of the waiting time for the BEOL and FEOL FeFET with $t_{FE} = 20nm$

5.7.5 TEST 2: Ferroelectric thickness 5nm

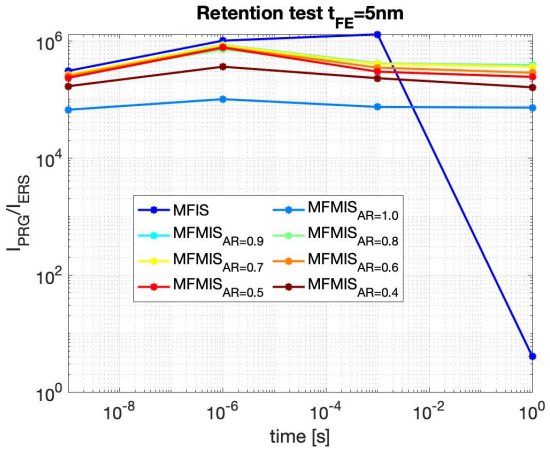
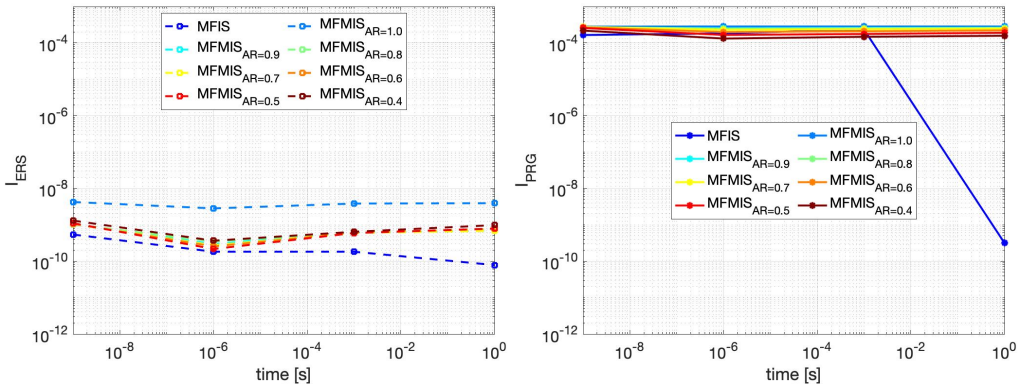


Figure 5.29: Retention result for the BEOL and FEOL FeFET with $t_{FE} = 5nm$



(a) ERS current (b) PRG current

Figure 5.30: Erase and Program current as a function of the waiting time for the BEOL and FEOL FeFET with $t_{FE} = 5nm$

5.7.6 TEST 2: Ferroelectric thickness 10nm

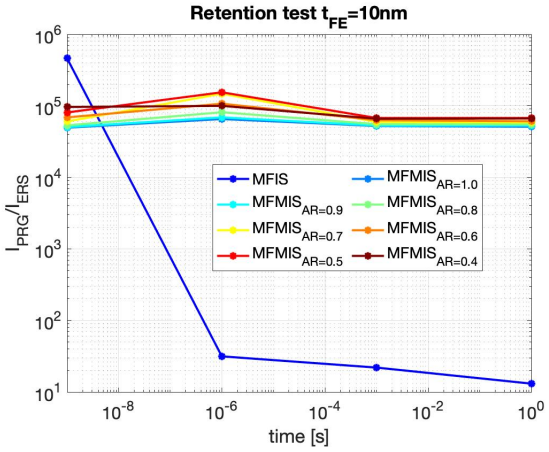
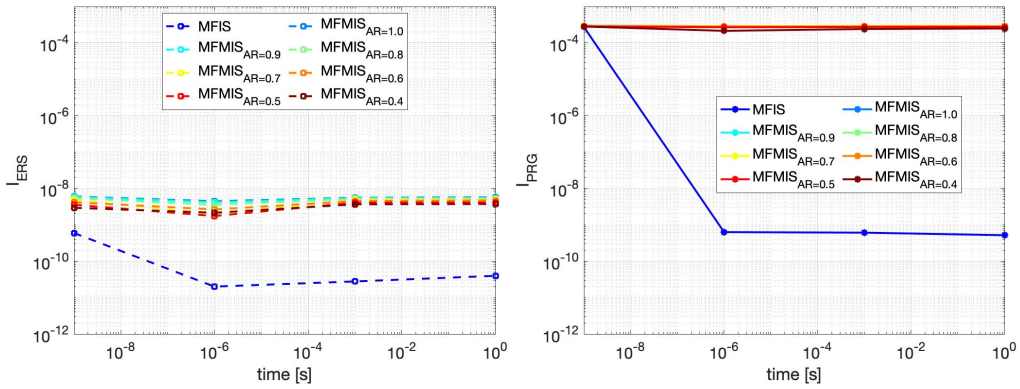


Figure 5.31: Retention result for the BEOL and FEOL FeFET with $t_{FE} = 10nm$



(a) ERS current (b) PRG current

Figure 5.32: Erase and Program current as a function of the waiting time for the BEOL and FEOL FeFET with $t_{FE} = 10nm$

5.7.7 TEST 2: Ferroelectric thickness 15nm

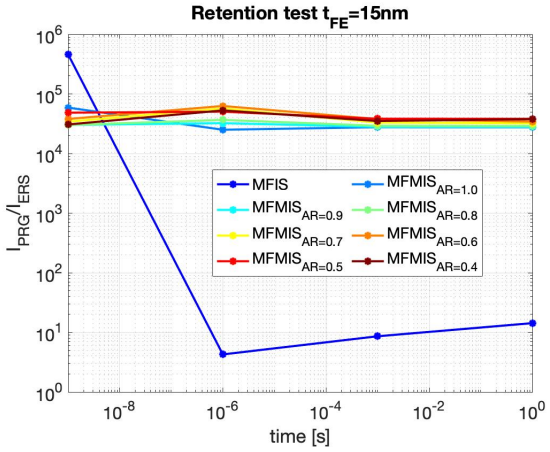
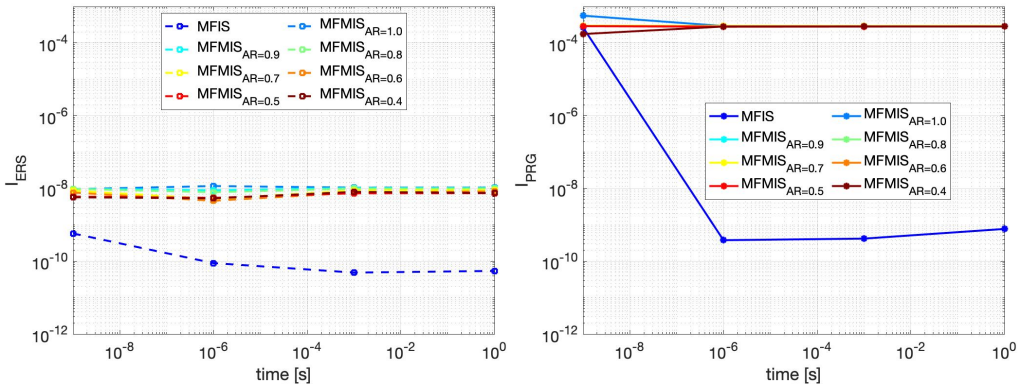


Figure 5.33: Retention result for the BEOL and FEOL FeFET with $t_{FE} = 15nm$



(a) ERS current (b) PRG current

Figure 5.34: Erase and Program current as a function of the waiting time for the BEOL and FEOL FeFET with $t_{FE} = 15nm$

5.7.8 TEST 2: Ferroelectric thickness 20nm

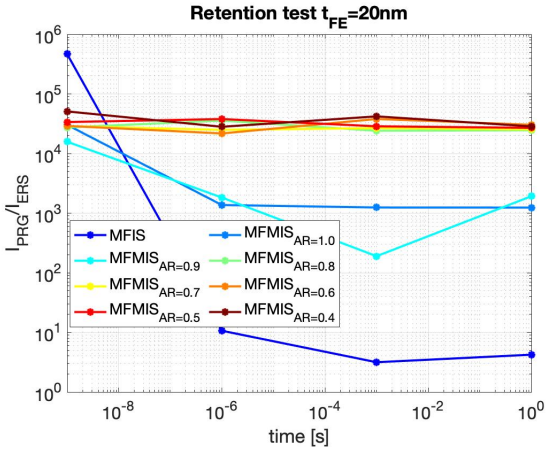
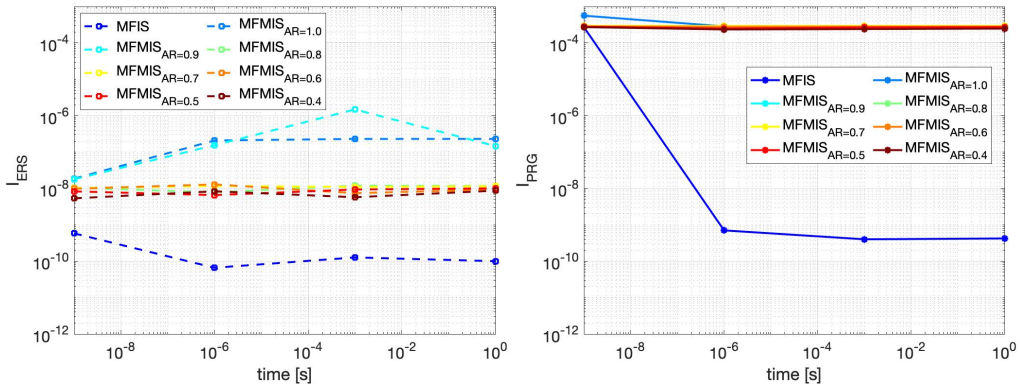


Figure 5.35: Retention result for the BEOL and FEOL FeFET with $t_{FE} = 20nm$



(a) ERS current (b) PRG current

Figure 5.36: Erase and Program current as a function of the waiting time for the BEOL and FEOL FeFET with $t_{FE} = 20nm$

5.8 Conclusions

The final section is devoted to summarize (briefly) the result obtained through the master thesis project. We start with the analysis of the depolarization field by inspecting the free energy landscape of the metal-ferroelectric-metal-insultor-metal structure by showing how an increase of the area ratio between the ferroelectric and the dielectric could make possible the transition from a double well potential shape toward a parabola shape. The main responsible of such change is the depolarization field which due to the opposite direction of the ferroelectric polarization tends to cause an hysteresis free device (negative capacitance FeFET). The circuit model is inspected as well since we measure the value of the depolarization field in order to compare it to the coercive field of the ferroelectric material. It's their ratio, E_{dep}/E_C, which need to be constantly be account for when discussing the study of retention of any ferroelectric device. From the theoretical model we move inside Ginestra modeling platform by comparing the FEOL vs BEOL FeFET transistor. The operation of the device, specifically the writing and reading operation has been intensively explain with the concept of disturb that lead to modify the sweep reading approach into a point reading one. In the end we report the retention study by considering the same device featured by two different G-L parameters (both taken from the literature) and we demonstrate that the retention in the BEOL FeFET is higher compared to the FEOL FeFET as the ferroelectric in the first device is sandwiched by two metal layers which enables a complete charge screening reducing considerably the effect of the depolarization field. In fig.5.37 the ferroelectric decay of the polarization in the

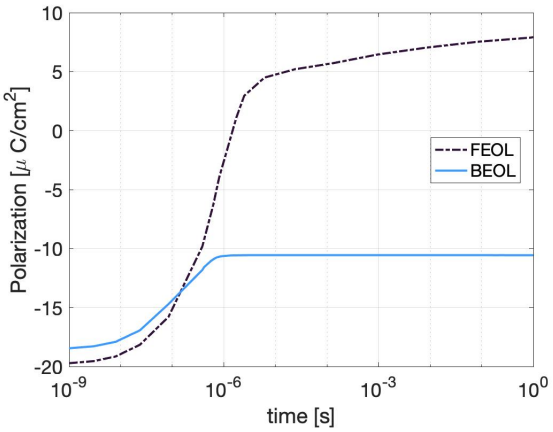


Figure 5.37: Ferroelectric polarization over time after PRG for the FEOL and BEOL FeFET

FEOL further justify the need of the floating metal layer in order to increase the data retention of the memory device.

5.9 Future works

In our thesis we neglect two important phenomenon, described below:

- the inclusion of trapping which plays a strong role in both endurance and retention of the FeFETs
- the consideration of the different equivalent oxide thickness due to the modification of the area ratio between the ferroelectric and the MOS gate stack. A proper adjustment on the gate voltage should be provided for the BEOL FeFET in order to compare the behavior of them when the same voltage is dropped over the ferroelectric material

This future works could further ameliorate the retention result reported in 5.7 beside giving a proper evaluation of the two different causes of retention loss: charge trapping (outlook) and depolarization field (current thesis project).

Appendix A

Field cycling behavior in hafnium oxide FECap

By far we have considered only variability concerning the fabrication level but we need to understand the consequence of a field cycling behavior, which means what happens when the FeCAP is subjected to a high field bipolar stress cycling, is the remnant polarization stable or does it change? It's very likely the measurement that one could perform in order to evaluate the endurance behavior (capability of material to face a given number of switching cycles) of the device and performing this investigation before reaching the FeFETs concept is crucial since it elucidate several aspects which are hidden in the MFM structure. The endurance characteristics with an alternating positive and negative pulse

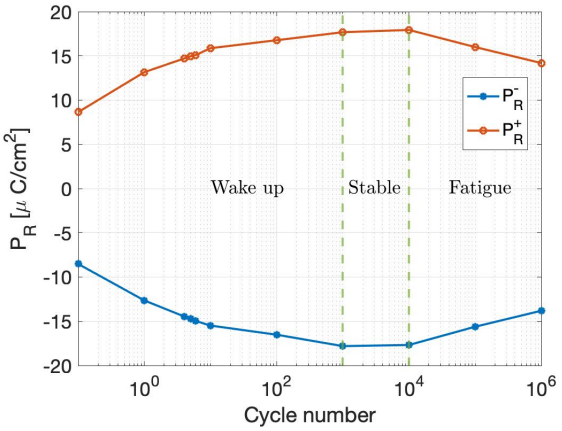


Figure A.1: Remnant polarization as a function of the number of bipolar cycling (10kHz) for a Sr:HfO_2 FeCAP

($\pm 4V$) is shown in fig.A.1. Two distinct trend can be observable:

1. wake-up: the remnant polarization P_r^+ (P_r^-) increases (decreases) the value up to 10^3 cycles. It corrospond to a de-penching of the pristine pinched hysteresis loop.

2. aging or fatigue: contrary to the wake-up behavior it shows a decreasing of the remnant polarization starting from 10^4 cycles. It is responsible of the low endurance behavior in ferroelectric capacitor beside for FeFETs other main factors are responsible for it.

In[3][38][39] the reason of such phenomenon is deeply examined and is entirely based on the two following features:

- ferroelectric: domain orientation, granular morphology, grain boundary, phase stability of the orthorhombic non-centrosymmetric phase, phase transition induce by field-cycling condition

- dielectric: generation, activation and distribution of defect (oxygen vacancies, oxygen ion), charge injection and trapping

We can start to describe the behavior of the structure in the pristine state by performing an analysis on the current-voltage characteristic. The result shows the presence of a double current peak in the dynamically measured transient current and recalling that the polarization is the integral of the transient current the trend is the cause of the pinched hysteresis loop in the P-V curve. During cycling the merge of the double peaks into one in correspondence of the wake-up state is the source of the open hysteresis loop. Why a double peak is observed in the pristine state? It originates from the different built-in bias field inside the insulator due to:

1. non uniform distribution of oxygen vacancies: recalling that HfO_2 is a high-k material which is featured by a high number of defects like dislocation or impurities acting as electron/hole trap (due to the high coordination number and electrons from the d shell). The oxygen vacancies distribution at least in the pristine sample maybe dictated by the fabrication process. The MFM structure $TiN-HfO_2-TiN$ can in turn be made of $TiO_xN_y-TMHfO_x-HfO_2-TMHfO_x-TiO_xN_y$ where the $TMHfO_x$ (also called dead-layer or passive layer) is an interface region non switchable generated by the diffusion of N into the insulator and O into the electrodes.

2. variability of grains: as the insulator is made of grains of different sizes and domain orientation. Oxygen vacancies are mostly localized at the grain boundaries while the granular morphology can also have an effect on the relative number of defects which can impact the domain pinning/de-pinning responsible for the pinched/open hysteresis loop

3. the relative difference of $\epsilon_r(\kappa)$ relative permittivity[8] (cubic $\kappa = [40,50]$, tetragonal $\kappa = [32,40]$, monoclinic $\kappa = [17,20]$, orthorhombic $\kappa \approx 30$) responsible of a non-uniform κ due to the co-presence of non FE phases beside the orthorhombic non-centrosymmetric ferroelectric one

The built in bias field, evaluated with the first order reversal curve (FORC) method in[40], drastically drops down to zero once reaching the 10^3 cycling and coincide with the increase of the remnant polarization which dictate the presence of a wider number of switchable domain. Focusing on the material no generation of defects is observable in the wake-up phase in good agreement with the flat behavior of the DC leakage current. During these stage the oxygen vacancies defects redistribute in the material(assisted by the high oxygen mobility of HfO_2 based device[41]), change their charge state and can provide a partial transformation toward the FE phase as less monoclinic and tetragonal phase is recorded by the High-Angle Annular Dark Field STEM during field cycling. In the fatigue stage a degradation of the insulator cause by the generation of defects, which means an increase of oxygen vacancies, result in an increase of leakage current. Where these defects originate? At the interface between the electrode and passive layer since the latter is characterize by low-κ a high field drop is the outcome which lead to a easily-broken bond and a further reduction of the electrical field in the ferroelectric region. It was revealed that an increase of leakage intra-grain current is the main factor beside the leakage current through the grain boundaries (already present in the wake-up state). Furthermore the charge trapping through the trap assisted tunneling (TAT) will lower the P_r^+ and $|P_r^-|$ as an increase number of pinned domain. The fatigue stage is not reported in case of uni-polar stress cycling as both the remnant polarization $P_r^{+/-}$ and leakage current do not deviate their trend by increasing the number of cycles. Let's make a summary:

- Up to 10^3 field cycling the constant DC leakage current is dictated by the redistribution of oxygen vacancies within the bulk grains which reduce the build-in bias field (present in pristine state). A transformation from the monoclinic to orthorhombic and tetragonal to orthorhombic with field cycling can facilitate the uniform distribution of the field and increase the remnant polarization.

- Further cycling can induce the generation of new defects and an increase of leakage current. The injection of charges into vacancies lead to creation of dipoles which hinder the reversal polarization of domains.

The effect of the temperature on the FeCAP during the endurance test can be beneficial as a rapid diffusion of oxygen vacancies and redistribution of them is obtained. Specifically at the start of the field cycling stress, as reported in[38], by performing 2 cycling field at $425K(\approx 150C^\circ)$ it can lower the number of wake-up cycles down to zero. A uniform field inside the HfO_2 is so reach immediately.

Appendix B

Domain switching kinetics

We introduce this chapter by analysing the reversal domain switching kinetics in ferroelectric material. As our approach is to study FE with nanometers dimension we may be question if the switching kinetics of ferroelectric domain is preserved when passing from a single bulk crystal FE toward a thin film poly-crystalline FE? The Kolmogorov-Avrami-Ishibashi (KAI) model[42] was by far the most appreciated model develop to describe the behavior of the domain switching in a bulk ferroelectric material. As shown in fig.B.1 once a creation of domain of opposite polarization is created by the formation of independent nucleation center, letter a, it unboundly growths due to the motion of domain wall after the nucleation, letter b and c indicating that the switching time is basiclly determined by the expansion of domains. While expanding another nucleation of domain can take place

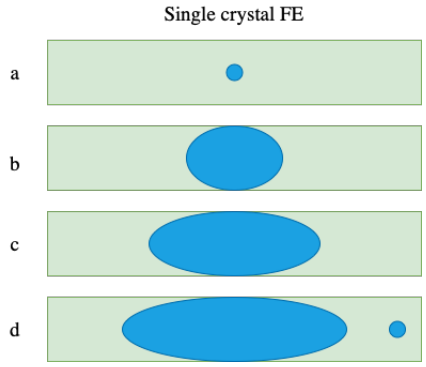


Figure B.1: Evolution of FE switching domain in a bulk single crystal at different time step

in the material, letter d contributing to the further transition toward the opposite state. According to KAI model the fraction of switched volume (p) at time t is:

$$p(t) = 1 - e^{-A(t)} \tag{B.1}$$

with $A(t)$ indicating the Avrami's extended volume. At constant nucleation rate and domain wall velocity is equal to

$$A(t) = (t/\tau(E))^n \tag{B.2}$$

where $\tau(E)$ is a characteristic switching time inversely proportional to the electric field and n is the dimension of domain growth (either one-dimensional which indicate $n = 1$ or two-dimensional, $n = 2$ where the last one consider that after the creation of circular-shape nuclei the boundary moves in a 2D fashion as reported in fig.B.1). In fig.B.2 the fraction of

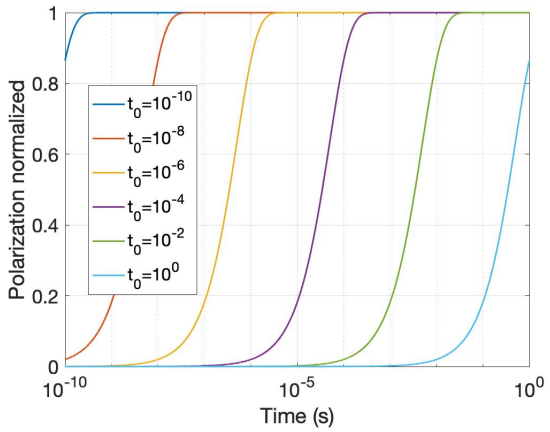


Figure B.2: KAI model for switching domain

switched polarization according to KAI model is illustrated considering $n = 2$ and different characteristic switching time. Since τ is related to the electrical field, a variation of the latter results in just a shifting of the curve along the logarithmic axis. Nevertheless when dealing with a thin film ferroelectric material the switching polarization shows different trend. As reported in[43] after the application of two pulses of the same polarity $(-5V)$ the FeCap was subjected to pulse of different amplitude and time width. The experimental result reported in fig.B.3 demonstrate that only above the $1V$ applied a complete switching of the polarization is obtained. Not only as we increase the applied voltage the time to complete the switching is reduced. It seems clear that the Kolmogorov-Avrami-Ishibashi model fails to predict the behavior of the switching of ferroelectric domains when dealing with thin film. A new model need to be inspected. It's called nucleation-limited-switching and is constitute of four main hypothesis:

1. the material is composed of elementary regions
2. the switching of a region happens once a domain of opposite polarization is nucleated in that region
3. The time for the switching corresponds to the waiting times of the first nucleation (is negligible the time to fill the region with reversed domain
4. The waiting times are distributed for each region and exponentially broad

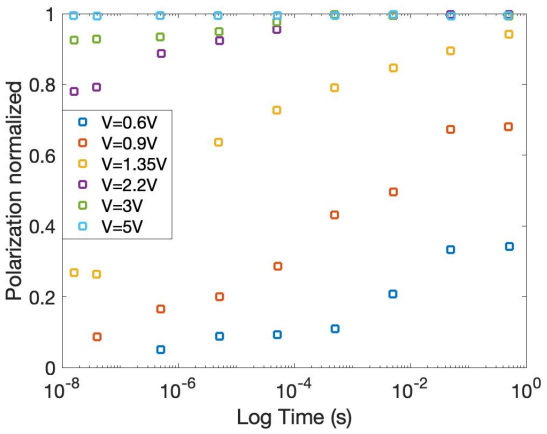


Figure B.3: Polarization switching for a FeCAP with 135nm PZT film

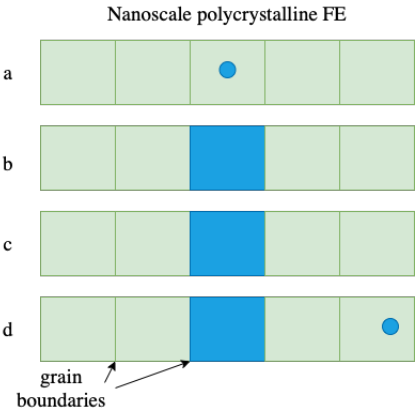


Figure B.4: Evolution of FE switching domain in a polycristalline thin film at different time step

The first three assumption can be well represent in fig.B.4. As for the bulk case in letter a the nucleation of domain of reversed polarization is created. In letter b and c the domain growth is confined by the grain boundaries which hinder its expansion towards the neighbour grains. This justify the name of the NLS model as the reversal of polarization is limited by the nucleation of domains. In letter d a second nucleation center is formed characterised by a different switching time (waiting time). Assuming $z_0 = logt$ and a distribution of the waiting times flat for the lower and upper limits of the switching time spectrum ($\tau_{min} = 10^{z_1}$ and $\tau_{max} = 10^{z_2}$) which decays as $1/z^2$ outside those boundaries[44]

we can define the fraction of the switched volume at time t by:

$$p(t) = \begin{cases} \Gamma h\left(\pi/2 - \arctan\frac{z_1 - z_0}{\Gamma}\right) & \text{for } z_0 < z_1 \\ \Gamma h\left(\pi/2 + \frac{z_0 - z_1}{\Gamma}\right) & \text{for } z_1 < z_0 < z_2 \\ \Gamma h\left(\pi/2 + \frac{z_2 - z_1}{\Gamma} + \arctan\frac{z_0 - z_2}{\Gamma}\right) & \text{for } z_2 < z_0 \end{cases} \tag{B.3}$$

where $h = (z2 - z1 + \Gamma\pi)^{-1}$ and Γ is a parameter controlling the rate of decay of the distribution function of the waiting times. Base on eq.(B.3) the switching of polarization is illustrated in fig.B.5 with the square indicating the experimental result. The value of

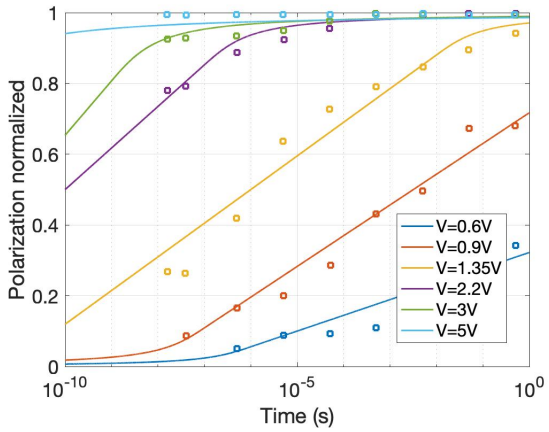


Figure B.5: NLS model for switching domain

z_1 and z_2 and of consequence τ_{min} and τ_{max} are evaluated by an empirical relationship which correlate the characteristic switching time with the voltage applied

$$\tau_{max/min} = \tau_0 10^{(V_{0_{max/min}}/V)^n} \tag{B.4}$$

with τ_0, n and $V_{0_{max/min}}$ are the parameters used to fit the data.

By far we have seen that the switching of the polarization as a function of time, from $-P_s$ to $+P_s$, can be expressed with the KAI model in the form of

$$P(t) = -P_s + 2P_s(1 - e^{-t/\tau}) \tag{B.5}$$

What we can say for the NLS model? As the characteristic switching time is not uniform in polycristalline thin film and is strongly related to the local field applied a new way to fit the experimental data was reported for the first time in [6]. The fraction of switched volume is slightly modified by introducing an exponential fitting parameter β:

$$p(t) = (1 - (exp(-t/\tau)^{\beta}) \tag{B.6}$$

The switching time τ is dependent on the local field and by the activation field E_a by

$$\tau = \tau_\infty exp\left(\frac{E_a}{E}\right)^{\alpha} \tag{B.7}$$

with τ_∞ the minimum nucleation time constant and α an empirical parameter. The last pieces is the definition of the distribution of switching times. As this phenomenon is dictated by the local field variation due to impurities/defect in the FE thin film, we define $E = \eta E_{FE}$ with E_{FE} the field applied in the ferroelectric layer ($E_{FE} = V/t_{FE}$) and η a random variable with probability density function corresponding to the generalized beta distribution of type 2:

$$f(\eta) = \frac{(|a|/b)(\eta/b)^{ap-1}}{B(p,q)(1+(\eta/b)^a)^{p+q}} \tag{B.8}$$

with $B(p,q)$ the beta function. Finally the evolution of the switching polarization considering the NLS model is:

$$P(E_{FE},t) = -Ps + 2Ps\int_0^\infty p(t,\tau(E_a,\eta E_{FE}))f(\eta)d\eta \tag{B.9}$$

The switching behavior is defined by 4 parameters corraleted to the FE switching dynamics: P_s, τ_∞,β and α and 4 parameters a, b, p, q describing the distribution function. An example of behavior is reported in fig.B.6.

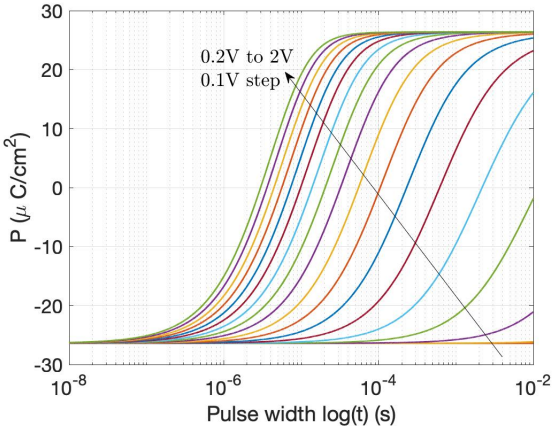


Figure B.6: Polarization reversal as a function of the pulse amplitude and pulse width with fitting parameter taken from[6]

Appendix C

The depolarization field due to the metal screening length on the ferroelectric transition temperature

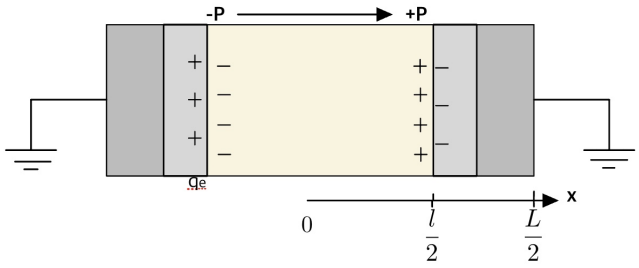


Figure C.1: MFM geometry used to evaluate the effect of depolarization field on the ferroelectric free energy

In fig.C.1 is reported the metal-ferroelectric-metal geometry used considering l to be the thickness of ferroelectric and $\frac{1}{2}(L-l)$ the metal electrode thickness. Furthermore the compensation charges $\pm q_e$ present in the metal electrodes are such that the polarization charge in the ferroelectric material is not fully neutralized. The ferroelectric free energy, according to Landau-Devonshire theory 2.2, is shown in (C.1)

$$\mathcal{F} = \alpha_0(T - T_0)P^2 + \beta P^4 + \gamma P^6 - E\,P \tag{C.1}$$

Because we consider ferroelectric material which exhibit a second order phase transition then higher order term can be neglected and we set the third Landau coefficient $\gamma = 0$. From (C.1) it's possible to derive the ferroelectric electric field and remnant polarization,

(C.2) and (C.3):

$$E_{FE} = 2\alpha_0(T - T_0)P + 4\beta P^3 \tag{C.2}$$

$$P_R = \sqrt{\frac{\alpha_0(T_0 - T)}{2\beta}} \tag{C.3}$$

Having recall the definition of electric field and remnant polarization for the ferroelectric material we can move on to discuss how the electric field in the electrode, E_M is evaluated. Setting the polarization inside the metal electrode to zero and the condition that the total current density is zero, from (C.4) and (C.5)

$$\frac{\mathrm{d}D}{\mathrm{d}x} = -\rho(x) \tag{C.4}$$

$$D = \epsilon_m E_M + P \tag{C.5}$$

it follows that

$$\frac{\mathrm{d}^2 E_M}{\mathrm{d}x^2} = \frac{1}{l_s^2} E_M(x) \tag{C.6}$$

with l_s the screening length defines as the length of concentration gradient of electron density in the electrode at the metal-ferroelectric interface[29]

$$l_s = \frac{h}{q}\left(\frac{3}{8\pi}\right)^{\frac{1}{3}}\left(\frac{1}{n}\right)^{\frac{1}{6}}\left(\frac{\epsilon_0\epsilon_m}{3m_e^*}\right)^{\frac{1}{2}} \tag{C.7}$$

It strongly depends on the electron density within the material as for higher electron density ($l_s \propto n^{1/6}$) the *Thomas-Fermi screening length* is of the order of interparticle spacing indicating that the electrons are very effective at shielding external charges. Taking as a reference the TiN metal electrode we can define its screening length by evaluating the carrier density (Hall measurements), the effective mass (Ultraviolet Photoelectron Spectroscopy) and the dielectric constant of bound electrons (through optical measurements). In tableC.1 we report the result obtained for TiN. Imposing the boundary condition,

ϵ_m	m_e^*	$n[1/cm^3]$	l_s
4	$2.3\,m_0$	$4 \cdot 10^{22}$	$0.826\,nm$

Table C.1: Material properties of TiN according to [2]

(C.8)

$$\begin{cases} E_M = 0 & x = \frac{1}{2}L \\ E_M = -\frac{q_e}{\epsilon_m} & x = \frac{1}{2}l \end{cases} \tag{C.8}$$

the electric field in the metal electrode is

$$E_M(x) = \frac{q_e}{\epsilon_m \sinh\left[(L-l)/2l_s\right]} \sinh\left(\frac{x - 1/2L}{l_s}\right) \tag{C.9}$$

For the ferroelectric material the electric field is assumed to be constant and is given in (C.10)

$$E_{FE} = -\frac{q_e + P}{\epsilon_{FE}} \tag{C.10}$$

Because no bias is applied to the circuit, we're under short circuit condition, by setting (C.11)

$$\int_0^{l/2} E_{FE}(x)\mathrm{d}x + \int_{l/2}^{L/2} E_M(x)\mathrm{d}x = 0 \tag{C.11}$$

then a linear relationship between the polarization and the compensation charge is found

$$q_e = -P\frac{\frac{l}{2\epsilon_{FE}}}{\frac{l_s}{\epsilon_m}\left[\coth\left(\frac{L-l}{2l_s}\right) - \operatorname{csch}\left(\frac{L-l}{2l_s}\right)\right] + \frac{l}{2\epsilon_{FE}}} \tag{C.12}$$

Due to the smaller screening length compared to the electrode thickness which satisfy the following condition $(L-l) \gg 2l_s$ (C.12) can be rewritten as

$$q_e = -P \cdot \theta(l_s, l) = -P\frac{l/2\epsilon_{FE}}{l_s/\epsilon_m + l/2\epsilon_{FE}} \tag{C.13}$$

By combining (C.13) with (C.10) the depolarization field is given as

$$E_{FE} = -\frac{P}{\epsilon_{FE}}(1-\theta) \tag{C.14}$$

Let's see how the depolarization field affects the remnant polarization (C.3). Combining (C.14) with (C.2) we can define a new transition temperature which now depends on the ferroelectric thickness and screening length as well.

$$T_0^* = T_0 - \left(\frac{1-\theta(l_s,l)}{\epsilon_{FE}2\alpha_0}\right) \tag{C.15}$$

By (C.15), the remnant polarization is given by:

$$P_R = \sqrt{\frac{\alpha_0(T_0^* - T)}{2\beta}} \tag{C.16}$$

indicating that the value of P_R is drastically influenced by the depolarization field which tends to switch dipoles into the opposite state, lowering as a consequence the polarization of the material when no bias is applied. In fig.C.2 is shown how by varying the thickness of the ferroelectric material the transition temperature and the remnant polarization are affected [45]. The first one is evaluated by $\Delta T = T_0 - T_0^*$ and display how by lowering the film thickness the ferroelectric stability is met at temperature much lower than the ideal case. The remnant polarization $P_R - t_{FE}$ is a monotonically increasing function that saturates when reaching a certain thickness value. It's relevant to notice the dotted red line which represent the value of P_R in the case where the compensation charge counterbalance the polarization of the ferroelectric material. An interesting trend is observed in fig.C.3 where the depolarization field reaches a peak value close to $t_{FE} = 3nm$. This can be explain by looking at (C.14) where $E_{dep} \propto \Delta T \cdot P_R$ and because of their trends ΔT monotonically decreasing and P_R monotonically increasing then a maximum value is obtained.

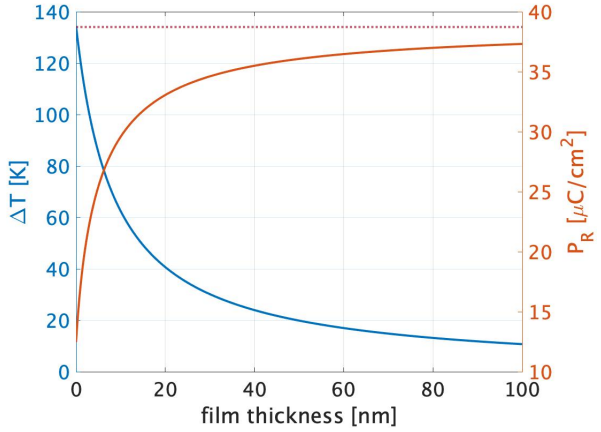


Figure C.2: Shift of the remnant polarization and transition temperature as a function of ferroelectric thickness. The Landau coefficient $\alpha_0 = 1e7[m/(F\,K)]$, $\beta = 1e10[m^5/(F\,C^2)]$, the Curie-Weiss temperature $T_0 = 450[K]$ and the screening length value is the one reported in the tableC.1

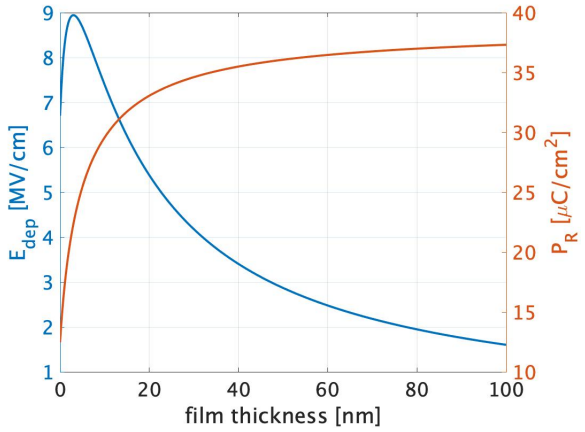


Figure C.3: Depolarization field behavior as a function of ferroelectric thickness. The Landau coefficient $\alpha_0 = 1e7[m/(F\,K)]$, $\beta = 1e10[m^5/(F\,C^2)]$, the Curie-Weiss temperature $T_0 = 450[K]$ and the screening length value is the one reported in the tableC.1

Bibliography

[1] J. Müller, P. Polakowski, S. Mueller, and T. Mikolajick, "Ferroelectric hafnium oxide based materials and devices: Assessment of current status and future prospects," *ECS Journal of Solid State Science and Technology*, vol. 4, no. 5, p. N30, 2015.

[2] P. D. Lomenzo, C. Richter, T. Mikolajick, and U. Schroeder, "Depolarization as driving force in antiferroelectric hafnia and ferroelectric wake-up," *ACS Applied Electronic Materials*, vol. 2, no. 6, pp. 1583–1595, 2020.

[3] M. Pešić, C. Künneth, M. Hoffmann, H. Mulaosmanovic, S. Müller, E. T. Breyer, U. Schroeder, A. Kersch, T. Mikolajick, and S. Slesazeck, "A computational study of hafnia-based ferroelectric memories: From ab initio via physical modeling to circuit models of ferroelectric device," *Journal of computational Electronics*, vol. 16, no. 4, pp. 1236–1256, 2017.

[4] S. Miller, R. Nasby, J. Schwank, M. Rodgers, and P. Dressendorfer, "Device modeling of ferroelectric capacitors," *Journal of applied physics*, vol. 68, no. 12, pp. 6463–6471, 1990.

[5] M. H. Park, H. J. Kim, K. Do Kim, Y. H. Lee, S. D. Hyun, and C. S. Hwang, "Impact of zr content in atomic layer deposited hf1- xzrxo2 thin films," in *Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices*. Elsevier, 2019, pp. 75–101.

[6] C. Alessandri, P. Pandey, A. Abusleme, and A. Seabaugh, "Switching dynamics of ferroelectric zr-doped hfo 2," *IEEE Electron Device Letters*, vol. 39, no. 11, pp. 1780–1783, 2018.

[7] T. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, "Ferroelectricity in hafnium oxide thin films," *Applied Physics Letters*, vol. 99, no. 10, p. 102903, 2011.

[8] M. Hoffmann, U. Schroeder, T. Schenk, T. Shimizu, H. Funakubo, O. Sakata, D. Pohl, M. Drescher, C. Adelmann, R. Materlik *et al.*, "Stabilizing the ferroelectric phase in doped hafnium oxide," *Journal of Applied Physics*, vol. 118, no. 7, p. 072006, 2015.

[9] S.-Y. Wu, "A new ferroelectric memory device, metal-ferroelectric-semiconductor transistor," *IEEE Transactions on Electron Devices*, vol. 21, no. 8, pp. 499–504, 1974.

[10] G. He, M. Liu, L. Zhu, M. Chang, Q. Fang, and L. Zhang, "Effect of postdeposition annealing on the thermal stability and structural characteristics of sputtered hfo2 films on si (1 0 0)," *Surface Science*, vol. 576, no. 1-3, pp. 67–75, 2005.

[11] M. Trentzsch, S. Flachowsky, R. Richter, J. Paul, B. Reimer, D. Utess, S. Jansen, H. Mulaosmanovic, S. Müller, S. Slesazeck *et al.*, "A 28nm hkmg super low power

embedded nvm technology based on ferroelectric fets," in *2016 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2016, pp. 11–5.

[12] H. Mulaosmanovic, E. T. Breyer, T. Mikolajick, and S. Slesazeck, "Ferroelectric fets with 20-nm-thick hfo 2 layer for large memory window and high performance," *IEEE Transactions on Electron Devices*, vol. 66, no. 9, pp. 3828–3833, 2019.

[13] E. Yurchuk, J. Müller, S. Müller, J. Paul, M. Pešić, R. van Bentum, U. Schroeder, and T. Mikolajick, "Charge-trapping phenomena in hfo 2-based fefet-type nonvolatile memories," *IEEE Transactions on Electron Devices*, vol. 63, no. 9, pp. 3501–3507, 2016.

[14] T. Ma and J.-P. Han, "Why is nonvolatile ferroelectric memory field-effect transistor still elusive?" *IEEE Electron Device Letters*, vol. 23, no. 7, pp. 386–388, 2002.

[15] A. G. Chernikova, M. G. Kozodaev, D. V. Negrov, E. V. Korostylev, M. H. Park, U. Schroeder, C. S. Hwang, and A. M. Markeev, "Improved ferroelectric switching endurance of la-doped hf0. 5zr0. 5o2 thin films," *ACS applied materials & interfaces*, vol. 10, no. 3, pp. 2701–2708, 2018.

[16] I. Mayergoyz, "Mathematical models of hysteresis," *IEEE Transactions on magnetics*, vol. 22, no. 5, pp. 603–608, 1986.

[17] B. Jiang *et al.*, "Computationally efficient ferroelectric capacitor model for circuit simulation," in *1997 Symposium on VLSI Technology*. IEEE, 1997, pp. 141–142.

[18] H.-T. Lue, C.-J. Wu, and T.-Y. Tseng, "Device modeling of ferroelectric memory field-effect transistor (femfet)," *IEEE transactions on electron devices*, vol. 49, no. 10, pp. 1790–1798, 2002.

[19] P. Chandra and P. B. Littlewood, "A landau primer for ferroelectrics," in *Physics of ferroelectrics*. Springer, 2007, pp. 69–116.

[20] C. J. Brennan, "A physical model for the electrical hysteresis of thin-film ferroelectric capacitors," *Ferroelectrics*, vol. 132, no. 1, pp. 245–257, 1992.

[21] J. T. Evans, "Characterizing ferroelectric materials," *Proc. IEEE ISAF*, pp. 1–123, 2011.

[22] E. Breyer, H. Mulaosmanovic, T. Mikolajick, and S. Slesazeck, "Reconfigurable nand/nor logic gates in 28 nm hkmg and 22 nm fd-soi fefet technology," in *2017 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2017, pp. 28–5.

[23] S. Dünkel, M. Trentzsch, R. Richter, P. Moll, C. Fuchs, O. Gehring, M. Majer, S. Wittek, B. Müller, T. Melde *et al.*, "A fefet based super-low-power ultra-fast embedded nvm technology for 22nm fdsoi and beyond," in *2017 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2017, pp. 19–7.

[24] M. Hoffmann, M. Pešić, S. Slesazeck, U. Schroeder, and T. Mikolajick, "Modeling and design considerations for negative capacitance field-effect transistors," in *2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*. IEEE, 2017, pp. 1–4.

[25] ——, "On the stabilization of ferroelectric negative capacitance in nanoscale devices," *Nanoscale*, vol. 10, no. 23, pp. 10 891–10 899, 2018.

[26] N. Gong and T.-P. Ma, "Why is fe–hfo 2 more suitable than pzt or sbt for scaled nonvolatile 1-t memory cell? a retention perspective," *IEEE Electron Device Letters*, vol. 37, no. 9, pp. 1123–1126, 2016.

[27] T. Ali, P. Polakowski, T. Büttner, T. Kämpfe, M. Rudolph, B. Pätzold, R. Hoffmann, M. Czernohorsky, K. Kühnel, P. Steinke *et al.*, "Theory and experiment of antiferroelectric (afe) si-doped hafnium oxide (hso) enhanced floating-gate memory," *IEEE Transactions on Electron Devices*, vol. 66, no. 8, pp. 3356–3364, 2019.

[28] K. Ni, P. Sharma, J. Zhang, M. Jerry, J. A. Smith, K. Tapily, R. Clark, S. Mahapatra, and S. Datta, "Critical role of interlayer in hf 0.5 zr 0.5 o 2 ferroelectric fet nonvolatile memory performance," *IEEE Transactions on Electron Devices*, vol. 65, no. 6, pp. 2461–2469, 2018.

[29] R. Mehta, B. Silverman, and J. Jacobs, "Depolarization fields in thin ferroelectric films," *Journal of Applied Physics*, vol. 44, no. 8, pp. 3379–3385, 1973.

[30] N. Gong and T.-P. Ma, "A study of endurance issues in hfo 2-based ferroelectric field effect transistors: Charge trapping and trap generation," *IEEE Electron Device Letters*, vol. 39, no. 1, pp. 15–18, 2017.

[31] M. Pesic, A. Padovani, S. Slcsazeck, T. Mikolajick, and L. Larcher, "Deconvoluting charge trapping and nucleation interplay in fefets: Kinetics and reliability," in *2018 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2018, pp. 25–1.

[32] H. Mulaosmanovic, S. Dünkel, J. Müller, M. Trentzsch, S. Beyer, E. T. Breyer, T. Mikolajick, and S. Slesazeck, "Impact of read operation on the performance of hfo 2-based ferroelectric fets," *IEEE Electron Device Letters*, vol. 41, no. 9, pp. 1420–1423, 2020.

[33] A. Ortiz-Conde, F. G. Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent mosfet threshold voltage extraction methods," *Microelectronics reliability*, vol. 42, no. 4-5, pp. 583–596, 2002.

[34] D. Lehninger, R. Hoffmann, A. Sünbül, H. Mähne, T. Kämpfe, K. Bernert, S. Thiem, and K. Seidel, "Ferroelectric fets with separated capacitor in the back-end-of-line: Role of the capacitance ratio," *IEEE Electron Device Letters*, vol. 43, no. 11, pp. 1866–1869, 2022.

[35] K. Seidel, D. Lehninger, R. Hoffmann, T. Ali, M. Lederer, R. Revello, K. Mertens, K. Biedermann, Y. Shen, D. Wang *et al.*, "Memory array demonstration of fully integrated 1t-1c fefet concept with separated ferroelectric mfm device in interconnect layer," in *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*. IEEE, 2022, pp. 355–356.

[36] H. Mulaosmanovic, S. Dünkel, M. Trentzsch, S. Beyer, E. T. Breyer, T. Mikolajick, and S. Slesazeck, "Investigation of accumulative switching in ferroelectric fets: Enabling universal modeling of the switching behavior," *IEEE Transactions on Electron Devices*, vol. 67, no. 12, pp. 5804–5809, 2020.

[37] P. Chang, Y. Zhang, G. Du, and X. Liu, "Experiment and modeling of dynamical hysteresis in thin film ferroelectrics," *Japanese Journal of Applied Physics*, vol. 59, no. SG, p. SGGA07, 2020.

[38] M. Pešić, F. P. G. Fengler, L. Larcher, A. Padovani, T. Schenk, E. D. Grimley, X. Sang, J. M. LeBeau, S. Slesazeck, U. Schroeder *et al.*, "Physical mechanisms behind the field-cycling behavior of hfo2-based ferroelectric capacitors," *Advanced Functional Materials*, vol. 26, no. 25, pp. 4601–4612, 2016.

[39] M. Pesic, F. P. Fengler, S. Slesazeck, U. Schroeder, T. Mikolajick, L. Larcher, and A. Padovani, "Root cause of degradation in novel hfo 2-based ferroelectric memories,"

in *2016 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, 2016, pp. MY–3.

[40] T. Schenk, M. Hoffmann, J. Ocker, M. Pešić, T. Mikolajick, and U. Schroeder, "Complex internal bias fields in ferroelectric hafnium oxide," *ACS applied materials & interfaces*, vol. 7, no. 36, pp. 20 224–20 233, 2015.

[41] T. Schenk, E. Yurchuk, S. Mueller, U. Schroeder, S. Starschich, U. Böttger, and T. Mikolajick, "About the deformation of ferroelectric hystereses," *Applied physics reviews*, vol. 1, no. 4, p. 041103, 2014.

[42] Y. Ishibashi and Y. Takagi, "Note on ferroelectric domain switching," *Journal of the Physical Society of Japan*, vol. 31, no. 2, pp. 506–510, 1971.

[43] A. K. Tagantsev, I. Stolichnov, N. Setter, J. S. Cross, and M. Tsukada, "Non-kolmogorov-avrami switching kinetics in ferroelectric thin films," *Physical Review B*, vol. 66, no. 21, p. 214109, 2002.

[44] N. Gong, X. Sun, H. Jiang, K. Chang-Liao, Q. Xia, and T. Ma, "Nucleation limited switching (nls) model for hfo2-based metal-ferroelectric-metal (mfm) capacitors: Switching kinetics and retention characteristics," *Applied Physics Letters*, vol. 112, no. 26, p. 262903, 2018.

[45] I. P. Batra and B. Silverman, "Thermodynamic stability of thin ferroelectric films," *Solid state communications*, vol. 11, no. 1, pp. 291–294, 1972.