Master of Science in Micro and Nanotechnologies for Integrated Systems

Master Thesis

DESIGN OF RAD-HARD ANALOG BLOCKS FOR A FULLY INTEGRATED DC-DC CONVERTER

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Abstract - ENGLISH

The main activity of CERN (the European Organization for Nuclear Research) consists of collecting and analysing data generated from high energy particle collisions to study the fundamental constituents of matter and their interactions. This is done by using sophisticated particle detectors that include various electronic circuits. As any electronic system, efficient power delivery to the detector is crucial. However, extra requirements are imposed by the highly radioactive environment, where radiation doses can reach 1 Grad of Total Ionizing Dose (TID) across the lifetime of the circuit. The lack of commercial solutions necessitates the design of radiation-hard power circuits such as DC-DC converters in order to properly operate in such environment.

The powering network to be used in the future LHC (Large Hadron Collider) upgrade will consist of two stages of DC-to-DC conversion. The first stage (48V $\rightarrow$ 5V) has already been designed while the second stage (5V $\rightarrow$ 0.9V) is currently under development. This thesis will revolve around the design of analog blocks that are to be used in the second stage of this powering network.

The chosen topology for the second stage is a stacked tank converter. It is being implemented in a commercial 28nm CMOS technology and utilizes only core transistors rated for 0.9V. Such devices exhibit a strong tolerance against TID, and therefore no specific radiation hardening is required at the schematic level to mitigate TID effects. In order to properly operate this converter, several blocks have to be designed. In this thesis, five blocks were designed using core transistors and with supply voltages ranging from 0.9V to 1.8V. Over-voltage and single event effects were taken into account and appropriate protections have been implemented.

The designed blocks consist of a capacitor-based level shifter with a range of 0.9V $\rightarrow$ 5V (max), a resistor-less beta multiplier made up of core transistors (rated for 0.9V) with a supply voltage of 0.9V $\rightarrow$ 1.8V, along with various over-voltage protections, an error amplifier with a GBW of 238 MHz and a DC gain of 94 dB, and a ramp generator along with a current generator sub-block, which constitute an integral part in the control loop of the converter.

Abstract - ITALIAN

L'attività principale del CERN (l'Organizzazione Europea per la Ricerca Nucleare) consiste nel raccogliere e analizzare i dati generati dalle collisioni di particelle ad alta energia per studiare i costituenti fondamentali della materia e le loro interazioni. A questo scopo vengono utilizzati sofisticati rivelatori di particelle che comprendono vari circuiti elettronici. Come per ogni sistema elettronico, un'alimentazione efficiente del rivelatore è fondamentale. Tuttavia, ulteriori requisiti sono imposti dall'ambiente altamente radioattivo, dove le dosi di radiazioni possono raggiungere 1 G rad di Total Ionizing Dose (TID) durante la vita del circuito. La mancanza di soluzioni commerciali rende necessaria la progettazione di circuiti di potenza resistenti alle radiazioni, come i convertitori DC-DC, per operare correttamente in questo ambiente. ,1 cm La rete di alimentazione che verrà utilizzata nel futuro upgrade dell'LHC (Large Hadron Collider) sarà costituita da due stadi di conversione DC-to-DC. Questa tesi riguarda la progettazione dei blocchi analogici da utilizzare nel secondo stadio di questa rete di alimentazione. La topologia scelta per il secondo stadio è un convertitore switched tank, che e' progettato utilizzando una tecnologia CMOS commerciale a 28 nm e utilizza solo transistor core con un rating di tensione di 0,9 V. Tali dispositivi presentano una forte tolleranza alla TID e pertanto non è necessario utilizzare specifiche tecniche a livello di schematico per mitigare gli effetti della TID. Per far funzionare correttamente questo convertitore, è necessario progettare diversi blocchi. In questo lavoro di tesi, sono stati progettati cinque blocchi utilizzando transistor core e con tensioni di alimentazione comprese tra 0,9V e 1,8V. Sono stati presi in considerazione gli effetti di sovratensione e i single event effects e sono state implementate le opportune protezioni.

I blocchi progettati consistono in un level shifter capacitivo che opera nel range di tensioni 0,9V $\rightarrow$ 5 V (max), un generatore di corrente senza resistenze composto da transistor core (con una tensione nominale di 0,9V) con una tensione di alimentazione di 0,9V $\rightarrow$ 1,8V, il quale utilizza varie protezioni contro le sovratensioni, un error amplifier con un GBW di 238 MHz e un guadagno DC di 94 dB e un generatore di rampe con un sottoblocco di generazione di corrente, che costituiscono parte integrante dell'anello di controllo del convertitore.

Abstract - FRENCH

L'activité principale du CERN (Organisation européenne pour la recherche nucléaire) consiste à collecter et à analyser les données générées par les collisions de particules à haute énergie afin d'étudier les constituants fondamentaux de la matière et leurs interactions. Pour ce faire, on utilise des détecteurs de particules sophistiqués qui comprennent divers circuits électroniques. Comme pour tout système électronique, l'alimentation efficace du détecteur est cruciale. Cependant, des exigences supplémentaires sont imposées par l'environnement hautement radioactif, où les doses de radiations peuvent atteindre 1 Grad de dose ionisante totale (DIT) pendant la durée de vie du circuit. L'absence de solutions commerciales nécessite la conception de circuits d'alimentation résistants aux radiations, tels que les convertisseurs DC-DC, afin de pouvoir fonctionner correctement dans un tel environnement.

Le réseau d'alimentation qui sera utilisé dans la future mise à niveau du LHC (Large Hadron Collider) sera composé de deux stades de conversion DC-DC. Le premier stade (48V $\rightarrow$ 5V) a déjà été conçu tandis que le second stade (5V $\rightarrow$ 0.9V) est actuellement en cours de développement. Cette thèse s'articulera autour de la conception des blocs analogiques qui seront utilisés dans le deuxième stade de ce réseau d'alimentation.

La topologie choisie pour le deuxième stade est un convertisseur switched tank. Il est conçu dans une technologie CMOS commerciale 28 nm et utilise uniquement des transistors core qui tolerent 0,9 V. Ces dispositifs présentent une forte tolérance à la TID et, par conséquent, aucun technique spécifique n'est nécessaire au niveau du schéma pour atténuer les effets de la TID. Afin de faire fonctionner correctement ce convertisseur, plusieurs blocs doivent être conçus. Dans cette thèse, cinq blocs ont été conçus en utilisant des transistors core et avec des tensions d'alimentation allant de 0,9V à 1,8V. Les effets de surtension et des Single Event Efffects ont été pris en compte et des protections appropriées ont été implémentées.

Les blocs conçus sont constitués d'un level shifter basé sur un condensateur qui fonctionne entre 0,9V et 5V (max), d'un générateur de courant sans résistances composé de transistors core avec une tension d'alimentation de 0,9V $\rightarrow$ 1. 8V, ainsi que diverses protections contre les surtensions, un amplificateur d'erreur avec une largeur de bande de 238 MHz et un gain DC de 94 dB, et un générateur de rampe ainsi qu'un sous-bloc de générateur de courant, qui sont partie intégrante de la boucle de contrôle du convertisseur.

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Chapter 1

Introduction

1.1 CERN

The Conseil européen pour la recherche nucléaire, better known by its acronym CERN is the largest particle physics research facility in the world. It was established in 1954 after the second world in Meyrin, a Swiss city located at the border with France. Switzerland was chosen as the host country due to its stability, neutrality and its location in the heart of Europe. CERN's mission consists of creating a collaborative environment where people contribute to science by treading into unexplored areas through the utilization of the unique particle accelerators maintained by CERN. The fundamental components of matter and their interactions are investigated at CERN with the primary goal of advancing our understanding of the underlying rules of nature. Built in 2008, the Large Hadron Collider (LHC) is the largest and most potent particle accelerator in the world. It is made up of a 27-kilometer ring of superconducting magnets and other accelerating elements that serve to increase the energy of the particles as they travel through the accelerator. Proton beams are formed through the injection and acceleration of a bunch (each packet of protons is referred to as a bunch) of protons. After reaching a certain energy two counter rotating beams are made to collide at one of CERN's LHC experiments : ALICE, ATLAS, CMS and LHCb. The generated particles resulting from the beam collision and other byproducts are studied by first gathering data obtained from a detector (present in all CERN experiments along with its required infrastructure) and then processing it in a data center. Each collision site is surrounded by detectors that collect data on the position, charge, speed, mass, and energy of the particles created by the collisions. In order to provide these functionalities the detectors are made up of complex devices which can be categorized in two categories :

- Tracking devices : The majority of the tracking devices in a detector are positioned near to the collision site, whereas muon detectors are located in the exterior layer of the detector (since muons are highly energetic particles and can travel much deeper in materials compared to other particles). These

tracking devices operate based on detecting charged particles by exploiting a magnetic field and studying the curvature of the particle's trajectory.

- Calorimeters : Neutral charges cannot be detected by tracking devices, instead they are identified by their energy which is absorbed by calorimeters.

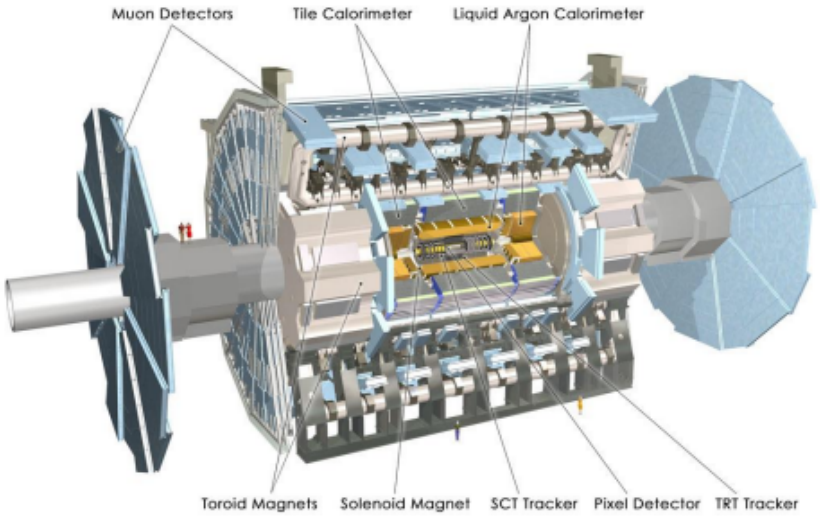


Figure 1.1: A cross-section of the Atlas experiment

The mentioned devices contain complex circuits which are present in a highly radioactive area filled with very high energy particles. Consequently, a stable and radiation tolerant power supply is required for all the circuitry. Providing these supplies while maintaining a low power consumption through the minimization of the cable number and length is achieved by developing a powering network with different DC-DC converters that supply various voltages required for optimal circuit operation. In this work, several radiation hard analog blocks for a point of load DC-DC converter with an input voltage of 5V are designed.

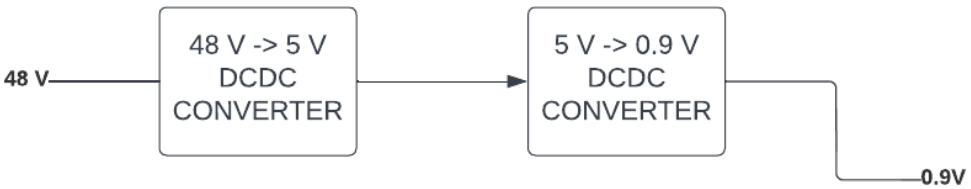


Figure 1.2: The proposed two stage powering network

In view of the future LHC experiment upgrades, a powering network based on two stages of DC-to-DC conversion has been proposed. The 48V $\rightarrow$ 5V step down

converter will provide an output power greater than 100W, while reaching high conversion efficiencies thanks to the use of Gallium Nitride (GaN) power switches. The radiation tolerance of such first stage converter is not enough to allow its deployment in close vicinity to the collision points. The next stage is a 5V $\rightarrow$ 0.9V fully integrated converter, which is being developed in a 28nm CMOS technology with the aim of reaching an increased radiation tolerance (up to 1 Grad of Total Ionizing Dose, TID). This device could be placed close to the collision point, thus allowing the power distribution at 5V until the location where the read-out electronics of the subdetectors is placed. This leads to reduced losses in the cables or conversely allows the usage of thinner cables. It is important to note that while the 5V step down DCDC converter will typically output 0.9V to power most circuits, this value can be tuned and thus the output voltage can be allowed to vary from 0.8V up to 1V.

As a final remark, this 5V DCDC converter project is being developed by five people including myself belonging to the microelectronics section at CERN. Subsequently, a significant number of blocks were designed by other team members. In this work, the focus will be on the analog blocks designed by me. A brief overview will be given to introduce the operating principle and the system level view of the converter.

1.2 Converter Type and Purpose

The main goal of the project of which this thesis revolves around is to design a fully integrated DC-DC converter to be inserted in the powering network for several chips. This converter is to receive a 5V input and output a stepped down voltage in the 0.8-1V range. DC-DC step down converters can be realized in different typologies and are operated based on several working principles, however due to the restricting specifications and radiation tolerance requirements, an STC (Switch Tank Converter) was adopted.
Before diving into the topology of the STC, it is worth to make some arguments as to why the relatively simplest step down converter, the Buck was not considered in this project.

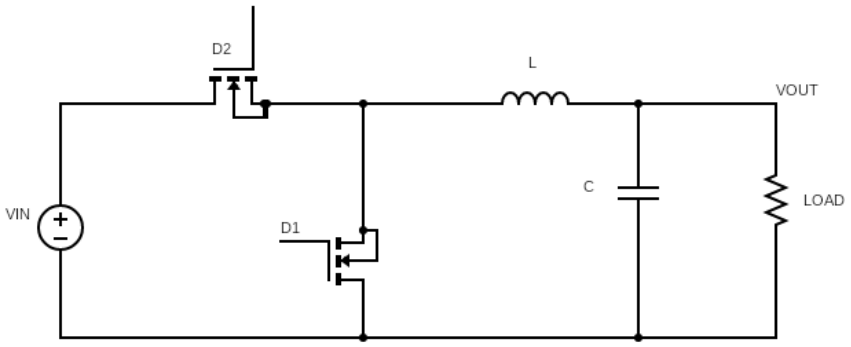
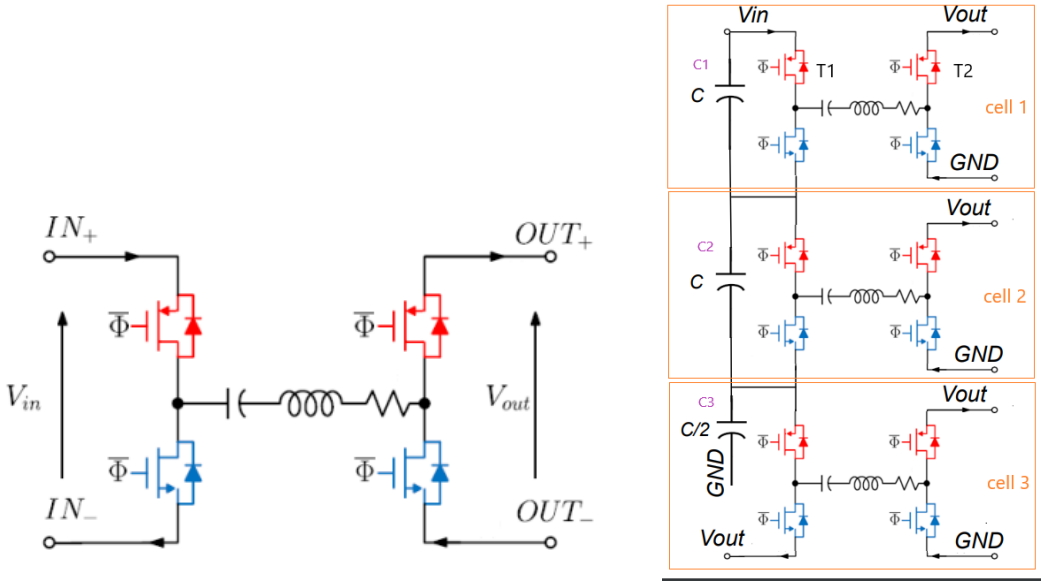


Figure 1.3: A simple representation of a Buck converter

Although the buck functions based on a different operating principle, the main reason it was not considered is that core transistors rated for 0.9 V could not be used with a 5V input: in a buck configuration, these transistors which operate as switches experience the total input voltage drop across them, and would therefore break.
What makes the use of FETs with a voltage rating lower that the input voltage desirable is their increased FoM (Figure of Merit) over their higher voltage counterparts. For FETs used as power switches, the most commonly used FoM is the product of their on resistance and the gate charge needed to turn them on, accounting for both the conduction and the switches losses. In fact, core transistors are often characterized by a smaller gate length and thinner gate oxide. The shorter length leads to a lower on resistance thus decreasing the conduction losses, while as the gate charge needed to turn on the device decreases compared to higher voltage solutions, leading to lower frequency-dependent losses. In addition, a shorter length leads to a better radiation tolerance according to a CERN internal report based on experimental data on the 28nm CMOS technology used in this work [1]. Furthermore, a thinner gate oxide leads to less accumulated charge due to TID and

therefore exhibits a smaller threshold voltage shift i.e. a better tolerance to radiation, enabling applications exceeding a TID of 1 Grad.
Coming back to the original topic, the converter adopted in this project is a modified STC which was originally designed for data center applications [2]. One of the reasons this converter was chosen is that it can be fully integrated, therefore it is more lightweight, and interferes less with the physics performance. The basic cell consists of two pairs of switches connected by an LC tank. Several stacking methods were introduced in the original paper, but the one used is depicted on the right part of Fig. 1.4.



(a) The basic cell.

(b) The stacked topology.

Figure 1.4: The basic cell and the stacked circuit.[2]

As depicted in Fig. 1.4, the full converter can be seen as a stack of three basic cells sharing the same resonance frequency, which achieves an ideal conversion ratio $\frac{V_{out}}{V_{in}}$ of $\frac{1}{4}$ (in any practical application, such ratio is lower due to the conduction losses). The capacitors connected vertically are used as dc filtering capacitors that behave as dc voltage sources which effectively clamp the voltage across transistors [2]. This circuit goes through two different switching phases during a switching period. During the first phase, $\bar{\phi}$ is low and the PMOS switches (depicted in red in Fig. 1.4) are on. In such phase, current flows from Vin to Vout in the case of section 1 (marked in the figure) through the transistors T1 and T2. This discharges capacitor C1 slightly. In the second phase, $\bar{\phi}$ is high and all the NMOS transistors (in blue in Fig. 1.4) are switched on, and in section 1 current flows from GND to C2, thus charging it.
The output voltage can be regulated by modifying the duty cycle of the driving signal $\bar{\phi}$ while maintaining the same period of the signal. The duty cycle control will be introduced and elaborated upon in a following section and chapter. Besides

the modified mode of operation (with respect to the original paper), the switches in the basic cell have been doubled. This has been done in order to protect the 0.9V rated switches from any voltage stress that may occur as ideally the 5V input should be divided across the 3 stages, any parasitics and non idealities might also lead to a voltage exceeding the rating. The added switches can be seen as protection elements that serve to lessen the voltage stress (voltage drop) across the main switches. Additionally, these switches are biased with a constant gate voltage and therefore are always on. This can be seen in Fig. 1.5 below.

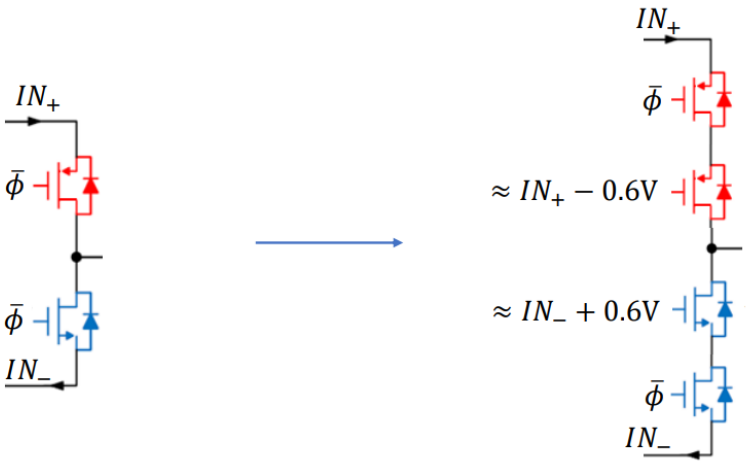


Figure 1.5: The original design (left) and the modified design with added protections (right)

As a final remark it is important to mention that on top of the previously mentioned advantages that this circuit entails, it will also exhibit :

- **A lower area due to the elimination of external passives.**
- **Due to the ability of exploiting a capacitor for energy storage, the resonant architecture reduces the size of the inductor compared to a buck converter, thus making it possible to use integrated inductors.**

Further details concerning the mode of operation and working principle of the STC are out of the scope of this work.

1.3 Block Level Description

During the duration of this thesis, I have worked on several blocks that are needed to both properly drive the switches and provide an accurate control signal, which consequentially sets the output voltage or the step down factor.
In this section, the block-level schematic of the DC-DC converter will be introduced

and its operation will be briefly explained, while a more detailed discussion of each block will be presented in the relative chapter.

1.3.1 Power Blocks

As mentioned in the previous section, the main converter consists of a stack of three basic cells having a 5V input voltage drop across them all. Consequently, each stage in the stack lies in a different voltage domain compared to the other two cells. This necessitates a unique powering stage for every stage in order to properly drive the main switches.

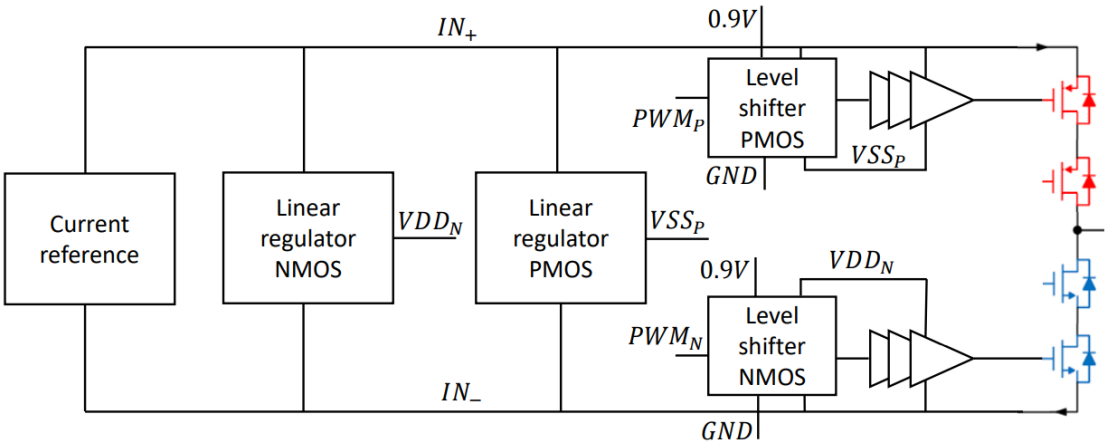


Figure 1.6: The power stage block view

The powering stage shown in Fig. 1.6 above consists of four main blocks: a current reference, level shifters, linear regulators and gate drivers.
The power supply voltage of each stage ($IN_+ - IN_-$) exceeds the 0.9V rating of the power switches. In order to ensure that the driving voltage of the switches does not exceed their voltage rating, each gate driver is powered by a 0.9V voltage generated by a linear regulator. The current reference provides a constant current of $2\mu A$ to the linear regulator. Level shifters are responsible for translating a PWM (Pulse Width Modulated) signal from the control voltage domain (GND $\rightarrow$ 0.9V) to the required domain belonging to each stage.
The blocks belonging to the powering section that have been developed in this work will be presented and discussed in independent chapters, and they consist of the level shifter and current reference.

1.3.2 Control Blocks

The second set of blocks that are integral to the converter's operation is the control block.
The control circuitry is needed to regulate the output voltage to the desired values, regardless of variations in the input voltage or output load. This is achieved by

generating a PWM (Pulse width modulated signal) that can vary in duty cycle while maintaining the same frequency of 200 MHz. This signal is first generated, then phase shifted and supplied to the relative level shifters which will drive the main switches as discussed in the previous section.

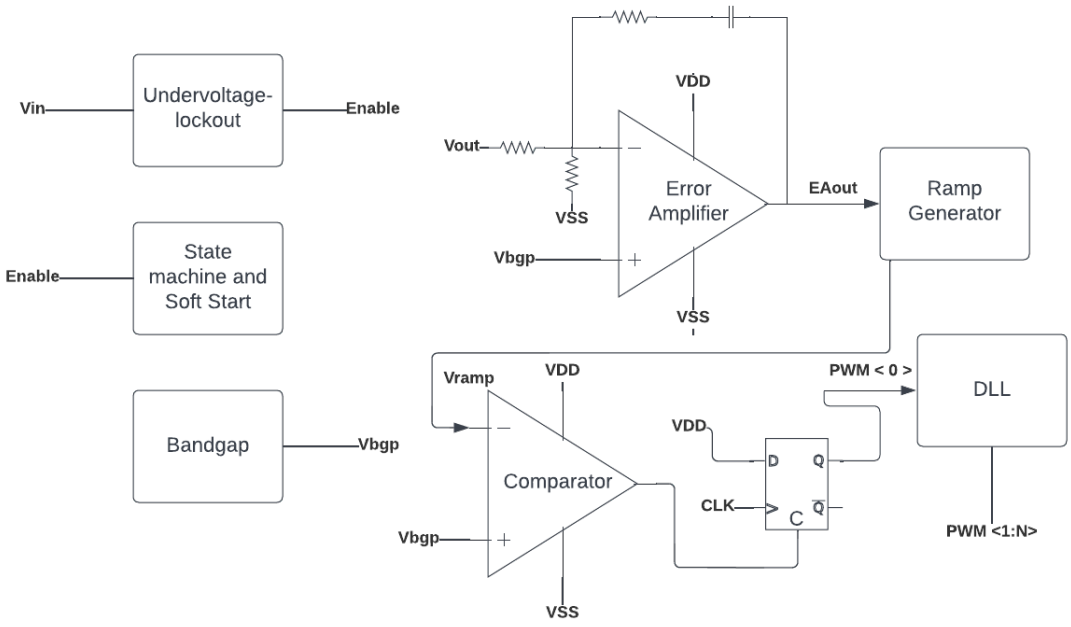


Figure 1.7: The control block view

This control is achieved by interconnecting the blocks shown above in Fig. 1.7. Briefly, a state machine governs the status of the circuit, defining whether the circuit is idle or in operation and managing the start-up phase. The enabling of the DC-DC converter operation is made based on an enable signal generated by the under-voltage lockout block, which detects when the supply, reference and input voltages have risen to around their steady state value. In the normal operating mode, an error amplifier compares a fraction of the output voltage (achieved with a variable resistive divider, which allows the tuning of this ratio, which in turns allows the adjustment of the output voltage) to a 300mV reference voltage generated by the bandgap circuit. The output of the error amplifier *EAout* is used to tune the duty cycle of the PWM signal, thus adjusting the output voltage of the converter to the desired value. The PWM is always set at the rising edge of the clock signal, while its duty cycle is tuned in the following way: *EAout* is inputted to a ramp generator (will be discussed in depth in a further chapter). Such block outputs a ramp signal that starts from *EAout* and goes downwards with a constant slope. As soon as the ramp voltage falls below the bandgap voltage, the comparator output goes high and the PWM signal (the flip flop output) is reset. In this way, a higher value of *EAout* is translated to a larger duty cycle of the PWM signal.
It is important to note that the representation shown above is a simplified diagram,

and does not illustrate all the intricacies of such blocks as some peripheral circuits have been omitted among other things. Out of the blocks presented above, I have worked on the error amplifier and the ramp generator. Therefore these blocks will be discussed in depth in their relative chapters in this work.

1.4 Radiation Effects and Hardening

The power converter will be placed in a region where highly energetic particles generated from particle collisions in one of CERN's colliders are present. Therefore, radiation types and effects on MOS ICs have to be well understood, and methods to mitigate them have to be implemented as they can be detrimental to the operation of a circuit in highly radiated regions. In this section, a mainly qualitative explanation and elaboration will be given. For a quantitative and more complete view the reader is encouraged to go through the relative PHD thesis which is the main reference of this section.[3]

1.4.1 Radiation Types and Effects

Generally, radiation effects can be associated to incident particles that can either be neutral such as a neutron or possess a charge as a proton. Radiation effects can be grouped into two sets, ionizing and nuclear displacement effects. In most cases, neutral particles such as neutrons are responsible for the latter, while charged particles tend to ionize the material. Nuclear displacement is when a particle impinges on a nucleus of an atom and forces it to shift thus creating a vacancy and a neighboring interstitial atom (a Frenkel pair). In modern CMOS technologies, Frenkel pairs recombine quickly at room temperature, and the nuclear displacement has therefore a negligible effect on the performance of the circuit. The following will instead focus on ionizing effects, which lead to the creation of electron hole pairs in a material. The amount of generated free carries is directly proportional to the amount of energy deposited in the material. The cumulative ionization effects are expressed in terms of TID (Total Ionizing Dose). The errors in an integrated circuit that are caused by ionization effects due to a single highly energetic particle are instead referred to as Single Event Effects (SEE).

1.4.2 Total Ionizing Dose Effects on MOS devices

TID effects are quite detrimental for MOS type devices as they have several effects that come into play. It is important to note that the main part that is affected by TID is silicon dioxide that serves as an insulating layer both under the gate and between devices.
Most electron and hole pairs generated in the silicon bulk and other conductive materials have minimal consequences as these materials are characterized by a low resistance and therefore the electron hole pairs are quickly removed. On the other hand, in silicon dioxide charges are trapped and can significantly affect the performance of the device. In the upcoming discussion, the effect of trapped electrons in the dioxide will be neglected as it is negligible compared to the effect of holes mainly

due to the electron mobility which is several orders of magnitudes higher than that of holes (electrons are therefore evacuated from the oxides in a much shorter time and do not accumulate). Additionally, the number of electron hole pairs can be calculated from the amount of energy deposited by the impinging particle. This energy amount is proportional to the LET (Linear Energy Transfer) of the particle and it varies with the material of the absorbing material and energy of the initial impinging particle.

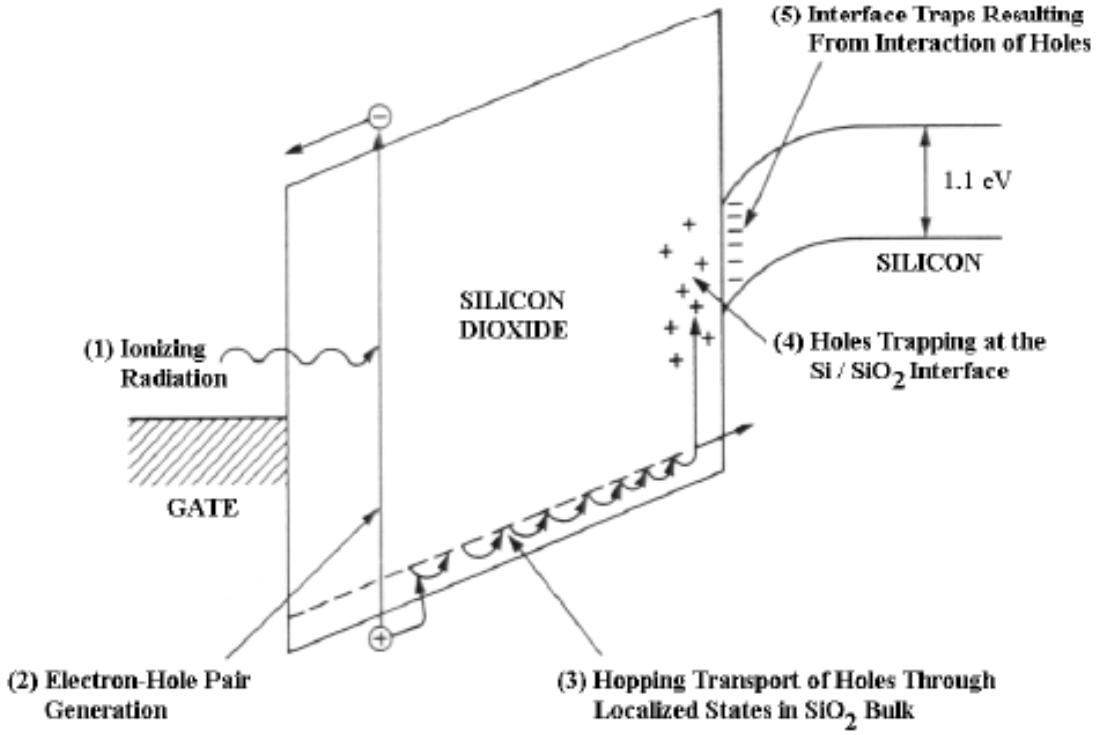


Figure 1.8: Ionizing radiation effects in gate SiO2 (assuming a positive bias on the gate)[3]

1.4.2.1 Gate Oxide Effects

Out of the electron hole pairs generated in the gate oxide, holes tend to cause issues and modification while as the effect that electrons induce is negligible in comparison. Generated holes in the gate dioxide can lead two two different outcomes.
Depending on the amount of defects in the oxide layer, a proportional number of holes are trapped and constitute a fixed positive charge that can take a variable amount of time to get neutralized. This time depends on several factors such as the spacial distribution of traps in the oxide, since one of the ways these trapped charges are neutralized is through tunnel annealing by electrons from the Si-SiO2 interface.
On the other hand, radiation generated holes can interact with hydrogen atom

impurities already present in the oxide and set hydrogen ions free. These ions drift towards the Si-SiO2 interface (in the case of a positive potential applied on the gate contact) and they give rise to new states around the SiO2-Si interface. In case of a negatively biased gate, the number of generated traps is decreased as the only thing generating them are hydrogen ions generated very close to the interface. Most modern CMOS technologies are characterized by a thin gate oxide. Therefore, the amount of TID-generated charge in such oxides is limited, and the Gate Oxide effects are less relevant than the STI Effects.

1.4.2.2 STI Effects

STI (Shallow Trench Isolation) is a thick layer of oxide that is mainly used to separate adjacent devices electrically from each other. Due to its thickness, the effect of trapped holes plays a very significant role compared to induced surface traps. These positive charges attract electrons and in the case the STI is placed between two n-type diffusions set at different voltages, a parasitic channel is created and current is allowed to leak through it.

The following paragraphs will detail the effects of TID on the electrical characteristics of MOSFETs.

1.4.2.3 Threshold voltage Shift

As mentioned in one of the previous sections (see Gate Oxide Effects 1.4.2.1), generated holes in the gate oxide lead to two different effects.
First, holes can be trapped in the gate oxide defects and constitute a positive charge. This positive charge has an opposite effect on Nmos and Pmos threshold voltages. In the case of an Nmos, it decreases the threshold voltage, while as it is increased in the case of a Pmos. This is obvious as the positive charges attract electrons towards the oxide interface in an Nmos and repels holes in the case of a Pmos. The effects of these trapped charges in the oxide are exacerbated as the oxide thickness increases. On the other hand, generated holes in the gate oxide lead to the rise of new states at the SiO2-Si interface. These induced traps affect both the N and P Mos device thresholds, as they are increased in both cases (in absolute values). In Fig. 1.9 below acceptor and donor like traps were assumed to be above mid-gap and below mid-gap relatively. Having made this assumption, in the case of an Nmos, the acceptor states which lie under the Fermi level next to the SiO2-Si interface become negatively charged thus positively shifting the threshold voltage. Similarly in the case of a Pmos, the donors above the Fermi level become positively charged and lead to a negative threshold voltage shift (increase in absolute value).

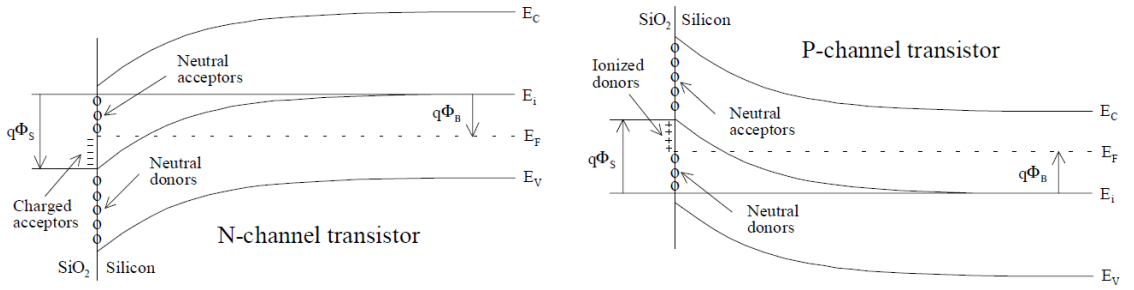


Figure 1.9: The effect of induced interface traps in the case of both an N and P transistors.[3]

It is important to note that in the case of an Nmos, the sign of the threshold voltage shift induced by radiation cannot be easily predicted as both effects counteract each other, and depending on the setting and time, one effect might dominate over the other.

Summing up, charges generated in the gate oxide lead to two contributions when it comes to the threshold voltage, these contributions being the trapped holes in the dioxide ΔV_{TR} and the generation of traps at the SiO2-Si interface ΔV_{INT} .
As for the case of trapped charges, the equation governing the threshold voltage is the following :

$$\Delta V_{TR} = -\frac{1}{C_{OX}} \int_0^{t_{OX}} \frac{x}{t_{OX}} \rho(x)\, dx \tag{1.1}$$

- ρ : Charge distribution inside SiO2
- C_{OX} : Oxide capacitance per unit area
- t_{OX} : Oxide thickness
- x : Distance from the gate-oxide interface

As qualitatively explained before, due to the polarity of the charge, the threshold voltage shift for both P and N type MOS devices is negative. In other words, the threshold of the N type device decreases while the threshold of the P type increases in absolute value. This can be understood by positive charges attracting electrons in the case of an N-type device and repelling holes in the P-type.
To quantify the contribution given by the generation of traps at the SiO2-Si interface ΔV_{INT} equation 1.1 can be used :

$$\Delta V_{INT} = -\frac{1}{C_{OX}} \frac{Q_{INT}}{t_{OX}} \tag{1.2}$$

The contribution effects on the threshold voltage shift have already been introduced and elaborated upon previously.

1.4.2.4 Increase in the sub-threshold and parasitic currents

It can be shown that the interface traps also lead to a decrease in the sub-threshold slope of NMOS devices, which leads to an increase in the leakage current.
On the other hand, the rise of the parasitic currents is mainly due to the formation of parasitic channels under the STI due to a significant amount of trapped charge in the thick oxide. Since, when an STI is placed between two n-type diffusions biased at different voltages, electrons are pulled towards the interface and form a channel that allows current to leak from the device. (see 1.4.2.2)

1.4.2.5 Mobility and Trans-conductance Degradation

The operation of the regular MOS devices is based on the flow of electric current very close to the oxide-silicon interface under the gate. As discussed in previous sections, exposing the device to radiation leads to trapped holes in the oxide which can then drift towards the Oxide-Silicon interface and induce traps. In fact, these traps are responsible for the mobility degradation as they result in rapid trapping and detrapping of carriers, thus degrading the mobility. This can be seen in the following equation :

$$\mu = \frac{\mu_0}{1 + \alpha(\Delta N_{it})} \tag{1.3}$$

Where :

- μ : The mobility after irradiation
- μ_0 : The mobility before irradiation
- α : A technology dependant factor
- ΔN_{it} : The induced surface traps

As a consequence of the decrease in carrier mobility, the trans-conductance of the transistor is also degraded as it is proportional to the mobility. Therefore, the current driving capability of the transistor is reduced.

1.4.3 Single Event Effects

In the previous section, radiation effects relating to mainly TID (Total ionizing Doze) were discussed. In this work, these effects were not tested for nor considered in the design phase as it was concluded that the used technology was robust against TID up to the target TID = 1Grad.
On the other hand, SE (Single Events) were detrimental towards the proper operation of the circuit and therefore they were modeled and tested at the design stage. SE effects and modeling will be discussed in the following subsections.

1.4.3.1 Single Events Effects

A highly energetic particle such as a heavy ion impinging on an integrated circuit, thus generating free carriers is called a single event. The generated carriers can lead to two different categories of effects. The first being reversible errors (does not destroy the device/IC) and non reversible errors (damage/destroy the device/IC).

1.4.3.2 Reversible Errors

Reversible errors are also called soft errors where the operation of the device/IC is momentarily disturbed, but can be brought back to its proper operation with or without external stimulus.
In the case of SEUs (Single Event Upsets), an impinging particle having an LET corresponding to the generation of a certain amount of charge greater than the critical charge of the device can change the stored information in a memory cell (a bit). This change in the stored bit can be rectified by rewriting the correct information in the memory. As the frequency of these errors is increased, the performance of the system is degraded. In the case when a SE affects one memory cell the phenomenon is called SEU, otherwise if it affects several cells it is called MBU.
The last soft error to be discussed is SEFI (Single Event Functional Interrupt). This issue can alternatively be seen as a specific instance of SEU. In complex memories, the peripheral circuits and memory cells are linked to other circuits that have extra functions, such as error detection and correction (EDAC). If an energetic particle affects one of these circuits, the inaccuracy will have an impact on how well the circuit functions as a whole.

1.4.3.3 Non-Reversible Errors

In this section, the most relevant destructive effect of SEs will be elaborated upon. Other destructive effects that mainly concern outdated technologies and high voltages will be listed briefly.

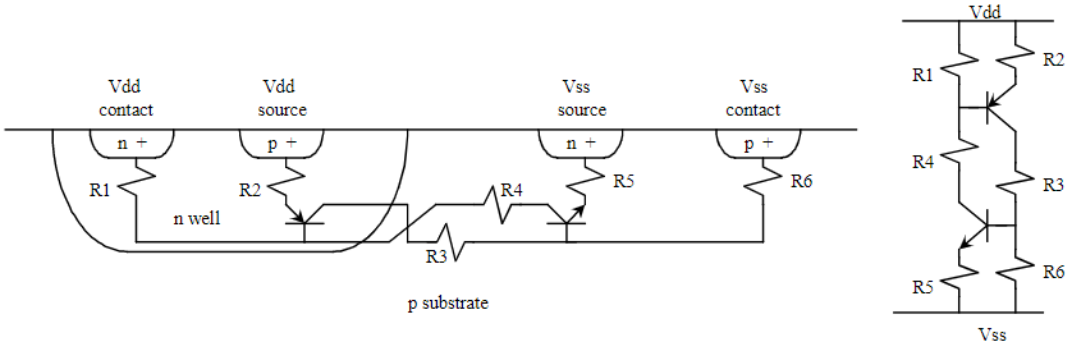


Figure 1.10: The parasitic thyristor in an n-well CMOS technology depicted graphically.[3]

The most detrimental effect for modern technologies is SEL (Single event latch-up). Latch-ups are possible only if certain conditions are met: the presence of a parasitic thyristor, the two parasitic bipolar junctions constituting the thyristor being forward biased, the gain product of the two bipolar junctions being greater than one, and a sufficient current supply taken from the source. If these conditions are met, then the parasitic thyristor is turned on and can constitute a short between two nodes, mainly the supplies. The formation of a short leads to a large sudden current that can irreversibly damage or even destroy the device if no action is taken. The other effects with brief explanations are listed below :

- SES (Single Event Snapback) : An impinging ionizing particle can trigger an avalanche process which turns on a parasitic NPN junction (in the case of an Nmos), thus injecting holes underneath the gate which effectively constitutes a base current for this junction. The base current is then amplified and reinforces the avalanche process initially triggered by the SE.

- SHE (Single Hard Error) : A threshold voltage shift caused by the generation of a large amount of charge in the gate oxide of a MOS transistor. This shift can make a memory device inoperable.

- SEGR (Single Event Gate Rupture) : A SE (ionizing particle) passing through the gate oxide during the presence of a high electric field can lead to the destruction of the gate oxide. For example high electric fields can be observed in power Mosfets and in EEPROMs (Electrically Erasable Programmable Read-Only Memory) during the erasing or writing phases.

- SEBO (Single Event Burn Out) : In some biasing conditions, a parasitic bipolar junction (present in both power Mosfets and bipolar transistors) can be turned on by an impinging particle. If sufficient current conducts through this parasitic junction, the generated heat due to power dissipation can lead to the destruction of the device.

1.4.3.4 Single Event Modeling on the Schematic Level

Single events are generated by highly energetic particles that can be emitted from a collision, and they interfere with the normal operation of the circuit. According to the particle's LET (Linear Energy Transfer, which represents the amount of deposited energy per unit distance and is usually expressed in $\frac{MeV \cdot cm^2}{mg}$ when normalized by the density of the target material), it is able to generate a proportional number of electron hole pairs that can cause the circuit to malfunction. This effect can be modeled by a current source that injects/sinks current from specific nodes.

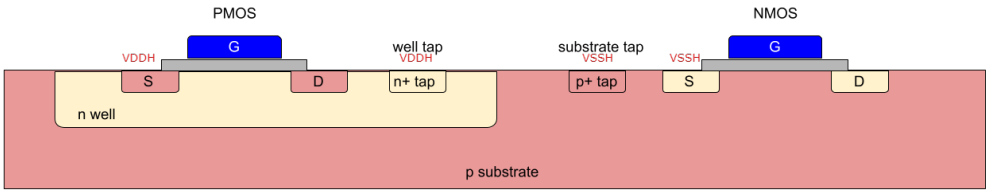


Figure 1.11: NMOS (right) and PMOS (left) layout.

In order to better present the reasoning behind modeling single events as current sources, an example is given. Assume a circuit connected as in Fig. 1.11. Looking at the NMOS, assume a highly energetic particle impinges the device and generates a certain number of electron hole pairs according to its LET. Some positive charges recombine in the substrate and most go to the p+ contact, and since this contact is connected to VSSH then the potential will not vary, as VSSH is a power rail and is therefore characterized by a very low resistance, so a current variation will not lead to a changing potential at that node. As for the negative charges, they are attracted to the positively biased node which will be the drain in this case. This can be seen as a discharging current flowing between the drain and the bulk (p+ tap), which leads to a decrease in potential at the drain since its parasitic capacitance is effectively being discharged. After some time the device that was already pulling up the node will charge back the parasitic capacitance and return the voltage to its normal level. As for the PMOS, a similar phenomenon occurs, but it leads to an increase in the drain voltage rather than a decrease such that in the case of an NMOS, and it is followed by a current discharge which brings back the node voltage to its normal value. It is important to note that the also source is susceptible to discharging/charging, it was not the case here since the source of the PMOS and NMOS were connected to VDDH and VSSH respectively, but in other typologies/circuits where the sources are connected to a certain node other than the power rails then an effect similar to that discussed above takes place, where the source is discharged (charged) to the bulk which is typically connected to VSSH (VDDH) in the case of an NMOS (PMOS). Additionally, as it will be introduced later on, the bulk is sometimes tied to the source, with Vsource > VSSH , then SE effects occurring on the source are not to be considered. In this case, the drain is charged/discharged to the bulk as always, but since it is tied to the source then the drain is charged and discharged to the source in the case of a PMOS and NMOS respectively.
The charge injection due to single events can be modeled in simulations by means of current pulses. For an NMOS, a current source between the drain/source and VSSH (the bulk) is used in simulations, while a current source between VDDH (bulk) and the drain/source is employed for PMOS devices. In a previous work [4], it was highlighted that the injected charge per unit LET (expressed in $\frac{MeV \cdot cm^2}{mg}$) in a CMOS technology can be estimated to be 10 fC. The circuits designed in this Master project must be tolerant to an LET up to 40 $\frac{MeV \cdot cm^2}{mg}$ (which translates into

a charge deposition of 400 fC), which is the typical maximum LET that can be found in CERN experiments. The charge injection has been modeled in simulations by means of a triangular current pulse, with the following parameters:

- **4 mA current amplitude with a 50 ps rise time and 150ps fall time**
- **400 ua current amplitude with 500ps rise time and 1500ps fall time**

These cases represent a fast and slow charge injection. Both types lead to an observable effect, therefore sometimes the respective circuit has to be made more robust (will be dealt with in every circuit as different methods are used). It is assumed that no single events occur during the power up or start-up phase of the circuits. The placement of these current sources modeling SE depends on the connections and the steady state value of a node. In fact, nodes that are already high (low) in steady state are not modeled to be charged (discharged) by single effects as they have no effect on them.
As for other cases, it is important to make the distinction of what nodes the current sources are placed between. In the case of an NMOS with its bulk connected to VSS, the SE is modeled by a current source connected between VSS and the drain thus discharging it and therefore decreasing the drain voltage (this is done as well for the source in case it is not connected to VSS). While as in the case of a PMOS with its bulk connected to VDD, the SE is modeled by a current source connected between VDD and its drain thus charging it and therefore increasing the drain voltage (this is done as well for the source in case it is not connected to VDD).
On the other hand, for devices that have their bulk connected to the source. such as driven clamps (introduced in chapter 3), then the highest (lowest) potential terminal for a PMOS (NMOS) which is the bulk, now corresponds as well to the source. Therefore, the current source is placed in between the source and drain in these cases. Current flows from source to drain in the PMOS case while it flows from drain to source in the Nmos case in comparison.

1.4.4 Radiation Hardening - Process, Layout, and Design

Generally, there are three methods of radiation hardening. These methods can summarized as hardening by process, layout, and system architecture or design.

1.4.4.1 Process

A possible approach to obtain radiation-hard circuits is using a radiation-hardened CMOS process. This can nevertheless be too expensive, and therefore commercial CMOS technologies are used at CERN to design radiation-tolerant ASICs. As mentioned several times in previous sections, a critical region of MOSFETs for TID tolerance is the thickness of the gate oxide, which is susceptible to the generation of charges within it. Additionally, it was also noted that thinner gate oxides are less affected by radiation due to the narrower space where charges can be trapped.

This fact inherently makes more advanced technologies and processes that are often characterized by a thinner gate oxide thickness less susceptible to radiation effects. Having a thinner gate oxide is one of the parameters that allow a better electrical performance in MOSFETs, and therefore there is an economical drive for its adoption into modern processes. This intrinsic increased radiation tolerance of more advanced commercial CMOS processes can be exploited to meet the increasing TID targets of CERN experiments. Nevertheless, the usage of a commercial process requires the adoption of layout and design methods to limit radiation effects, as detailed in the following subsections.

1.4.4.2 Layout

There are several possible ways to limit radiation effects by means of layout techniques. The first method addresses the inter-device leakage current between n-type diffusions/implants. As mentioned before, devices are usually separated by STI which is a thick oxide layer. This oxide layer can thus trap a significant amount of positive charge that can attract electrons from the substrate and create a parasitic channel between two neighboring n-type diffusions/implants. STI separating two p-type diffusion/implants does not create a parasitic channel since the trapped positive charge repels holes, which are the main carriers responsible for current conduction in these devices. One way to approach this issue is to separate the n-type diffusions/implants by a p + guard ring, which cuts any parasitic channels under the STI.
An Enclosed Layout can be instead adopted to suppress radiation-induced drain-to-source leakage current in NMOS devices.

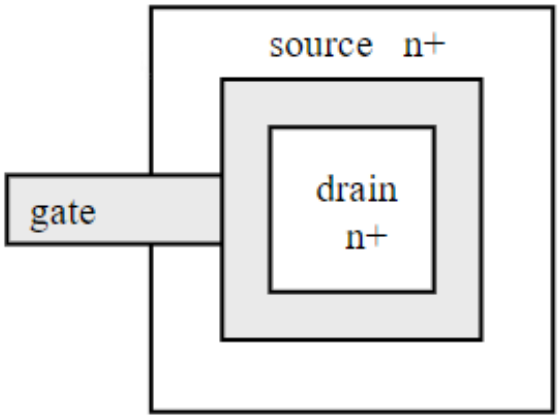


Figure 1.12: The proposed enclosed layout for an n channel device.

As depicted in Fig. 1.12, the gate surrounds the drain completely and effectively cuts all parasitic paths in between the drain and source diffusions. However, this layout technique comes with its own challenges such as :

- A larger area occupation, thus decreasing the density significantly.

- Obtaining a larger gate and source or drain capacitance.
- Modeling challenges with the W/L ratio.
- Asymmetrical design.
- The presence of constraints in selecting the W/L ratio.

A third issue that can be solved with layout methods is the SEL introduced previously. In fact, several approaches and recommendations are made (referring to Fig. 1.10) which are constituted by the following :

- Increase the distance between the n+ diffusion in the substrate and the p+ diffusion in the well.
- Reduce the resistances of R1 and R6 by utilizing many substrate and well contacts along with positioning them as close as possible to the latch-up loop.
- Surround n channel and p channel devices by a p+ and n+ guard ring respectively. The p+ guard rings introduce a heavily doped p region into the base of the NPN parasitic bipolar transistor, thus lowering the gain while maintaining the base around the ground level. The PNP parasitic bipolar junction is affected similarly by the n+ guard rings.

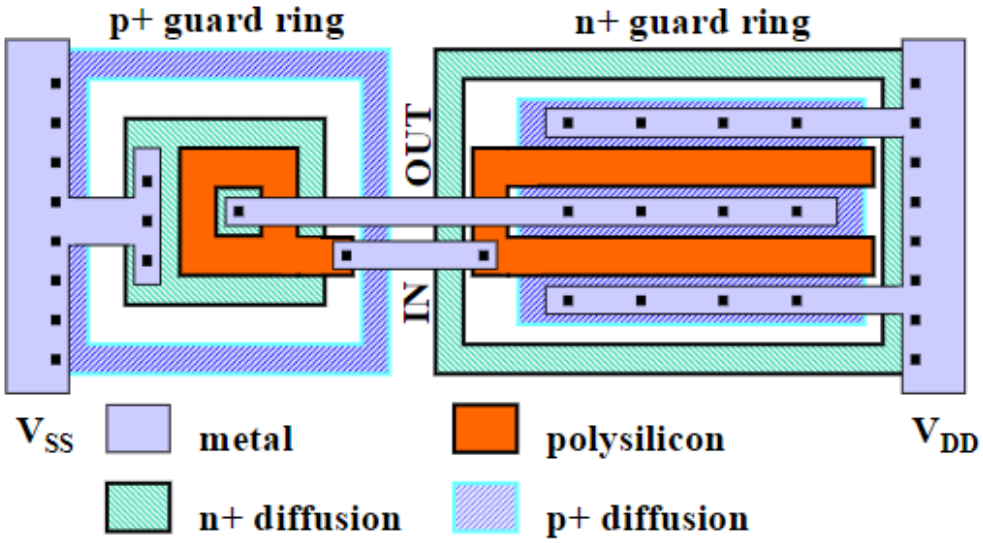


Figure 1.13: An inverter layout adopting the introduced approaches and recommendations for radiation tolerance.[3]

1.4.4.3 Design

A circuit can be made radiation tolerant also by using specific circuit architectures. This section will only focus on the techniques adopted in this work. It is worth

mentioning again that TID effects were not taken into account in this work, as the used 28nm CMOS technology did not warrant such an investigation. The main effects that were taken into account at the design level were limited to SEs (Single Events) and the disruptions they caused. Initially, no standard approach was taken to mitigate SEE (Single Event Effects), instead charge injections and sinking (modeled by a current source) were simulated at all sensitive nodes in the designed blocks. The effects were observed and conclusions on how to mitigate their effects were drawn. Through this, a standard approach concerning biasing transistors and networks was discovered and adopted. This standard consists of a clamp and an RC filter. In order to elaborate on the rise of this standard, it is important to recall that SEs are short charge injections/sinks in time but high in amplitude (up to 4mA), thus they cause large voltage fluctuations. On biasing branches and some biasing transistors where voltages should remain constant in steady state, clamps consisting of transistors biased to be around 100mV below the threshold voltage i.e. off in the normal operation of the circuit are utilized. In the case a SE occurs at the sensitive biasing node, the voltage either increases or decreases and that activates the respective clamp which counteracts this increase or decrease. Therefore, the voltage increase/decrease at that sensitive node is reduced significantly in time, and consequently it becomes of a higher frequency. Then, the RC filter kicks in and filters out this large but short amplitude fluctuation and maintains almost the same steady state voltage with slight variations.
However, this approach cannot be used in all nodes, since some of them (such as in an operational amplifier) need to be able to react quickly to input signal variations and adding an RC filter would degrade the performance significantly.
It is worth mentioning that several other design approaches are available but they were not implemented in this work, thus the reader is encouraged to go through the reference of this section for supplementary information.

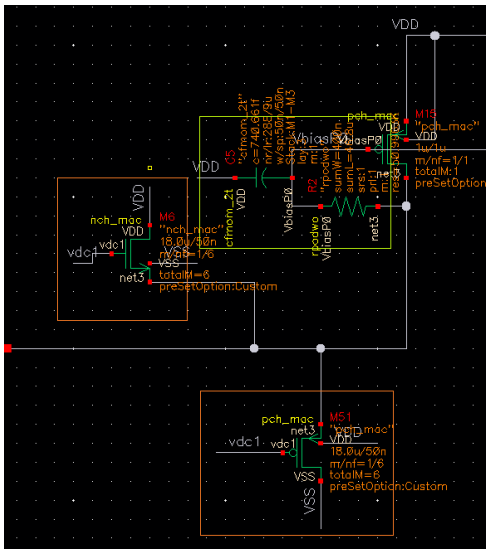


Figure 1.14: A section of a schematic showing the voltage clamps (orange rectangles) and the RC filter (green rectangle) for SE robustness.

Chapter 2

The Level Shifter

2.1 Circuit Overview

One of the peripherals required to operate the DCDC converter is the level shifter, which translates voltage pulses/signals from one domain to another. The two voltage domains studied are $4.1V \rightarrow 5V$ (the highest potential domain) and $0V \rightarrow 0.9V$ (The lowest potential domain). As a reminder, several voltage domains are needed to operate the switching transistors introduced in the converter powering block section, therefore for the sake of efficiency the PWM driving signal domain (lowest) along with the highest voltage domain are studied.
A capacitive floating level shifter inspired by [5] was designed and used to achieve the required functionality.

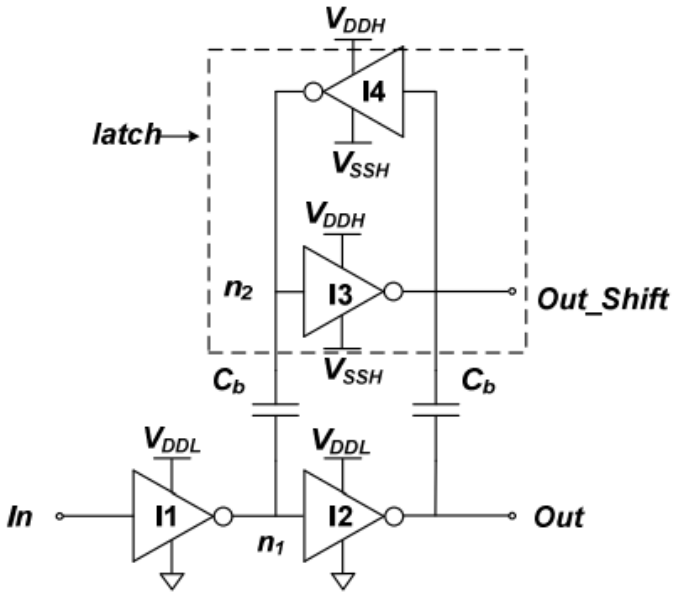


Figure 2.1: The Capacitive floating level shifter. [5]

Referring to Fig. 2.1 above, assume an initial condition where In is zero (low state) then n1 , and n2 are high while out and out_shift will be low. In the case when In moves from low to high, then consequently n1 is pulled down and Out is pulled up. Given that that the capacitor Cb and the R_{on} of the inverters I4 and I3 are high, then lost charge will be minimal and the voltage across the capacitor will be maintained thus node n2 and Out_Shift will follow nodes n1 and Out respectively and consequently their voltages will change by VDDL. This change is guaranteed when the voltages of n2 and Out overcome the inverter switching threshold: in this case, the state of the memory element (the latch) will change due to the characteristic positive feedback of back to back connected inverters. In the case where the capacitance of Cb and/or the on resistance of I3 and I4 are low, then the capacitor is allowed to lose a relatively significant amount of charge, thus discharging or charging the capacitor, and this may prevent the signals n2 and Out_Shift from reaching the inverter switching threshold, thus compromising the circuit functionality.

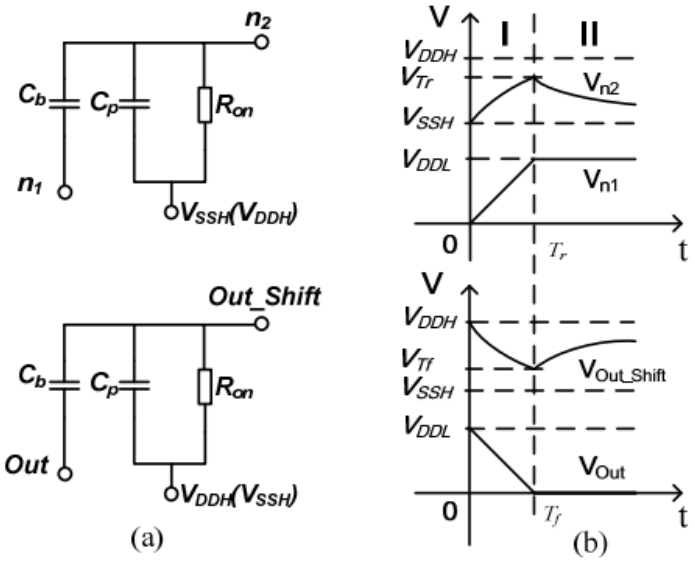


Figure 2.2: (a) A simplified representation of the circuit, (b) the corresponding waveforms. [5]

In order to better understand the main operation of this circuit, it is useful to first simplify it. The simplified circuit is presented in Fig. 4.5a. The top and bottom stacked schematics represent the left side and right sides of the latch presented in Fig. 2.1 respectively. Taking the top schematic :

- Cp : Represents the total parasitic capacitance of the node;
- Ron : Represents the on resistance of both inverter's (I3 and I4) transistors.

Taking the top circuit, and assuming the starting condition is with node n1 being low, then as soon as n1 starts to rise (due to the presence of a pulse for example) then node n2 starts to rise accordingly as well. Node n2 keeps on rising until node

n1 reaches its steady state value (Part I in Fig. 4.5). After n1 ceases to rise, n2 starts to fall again, mainly due to the Ron resistance that connects it to VSSH and therefore discharges the node. This discharge is lower than the charging of the node by the current incoming from node n1 when it's varying, and that is why we observe an increase when the slope of n1 is positive and a decrease when the slope of n1 is zero. Generally speaking, the increase in the potential of node n2 should be sufficient to turn on the nmos of the following inverter and thus this should reinforce node n2 to a high level. In this discussion, only the qualitative functioning of this type of circuit is studied. A more quantitative view and explanation is given below by solving the differential equations of the circuit. At first, we assume Vn1 rises linearly and then we apply KCL on the circuit and obtain the following :

$$C_p\frac{dV_{n2}(t)}{dt} + \frac{V_{n2}(t) - V_{SSH}}{R_{on}} = C_b\frac{d[V_{n1}(t) - V_{n2}(t)]}{dt} \tag{2.1}$$

Solving the equation leads us to the following :

$$V_{n2}(t) = R_{on}C_b\frac{dV_{n1}(t)}{dt} \cdot [1 - \exp\left\{\frac{-t}{R_{on}(C_b + C_p)}\right\}] + V_{SSH} for (0 < t < T_r) \tag{2.2}$$

Looking at equation 2.2 it is clear that for very large inverter R_{on} the node voltage of n2 follows the rising voltage of n1 which is what is intended.
However, when the node voltage n1 stops increasing it's slope becomes zero therefore equation 2.1 is modified by removing the term $\frac{dV_{n1}}{dt}$. The following is obtained :

$$V_{n2}(t) = (V_{tr} - V_{SSH}) \cdot \exp\left\{\frac{-T_r}{R_{on}(C_b + C_p)}\right\} + V_{SSH} for (T_r \leq t) \tag{2.3}$$

According to the equations presented above, the node voltage n2 rises when the potential of node n1 is rising (Region 1). n2 starts to fall when the potential of node n1 stops to vary since it reached its steady state value. Substituting R_{on} with a very high value, it is concluded according to the equations above that node voltage n2 will follow and stabilize according to the nodal voltage of n1. As a final remark, it is important to recall that the discussion given concerning figure 4.5 does not take into account the dynamics of the inverter and therefore the positive feedback characteristic of the loop. In reality, R_{on} is not infinitely large, and the potential of node n2 behaves similarly to what is presented in region 1 in figure 4.5 b. Then, as the potential of node n2 rises, it crosses the switching threshold of the following inverter before it starts to fall again as depicted above. This threshold crossing reinforces the rise of V_{n2} and therefore it continues on rising even after V_{n1} reaches its steady state value.
A similar discussion can be made in the opposite case (a transition from high to low) but this is left to the reader in order to avoid redundancy.

2.2 Circuit Implementation and Design

According to the discussion and points made above, relatively large capacitors are utilized due to their ability to store a large amount of charge. In addition, the inverter sizing, specifically the inverters constituting the latch have been chosen to impose a high resistance at the terminals of the capacitor to minimize charge loss. During operation, the capacitor loses a small amount of charge compared to its total stored charge, i.e. we can ideally assume the stored charge to be constant. Therefore, according to the basic equation $Q = CV$ the voltage drop across the capacitor is now a constant since the other two parameters are constants as-well. Due to that, the voltage pulse amplitude on one terminal will be effectively translated to the other one, i.e. to the other voltage domain.

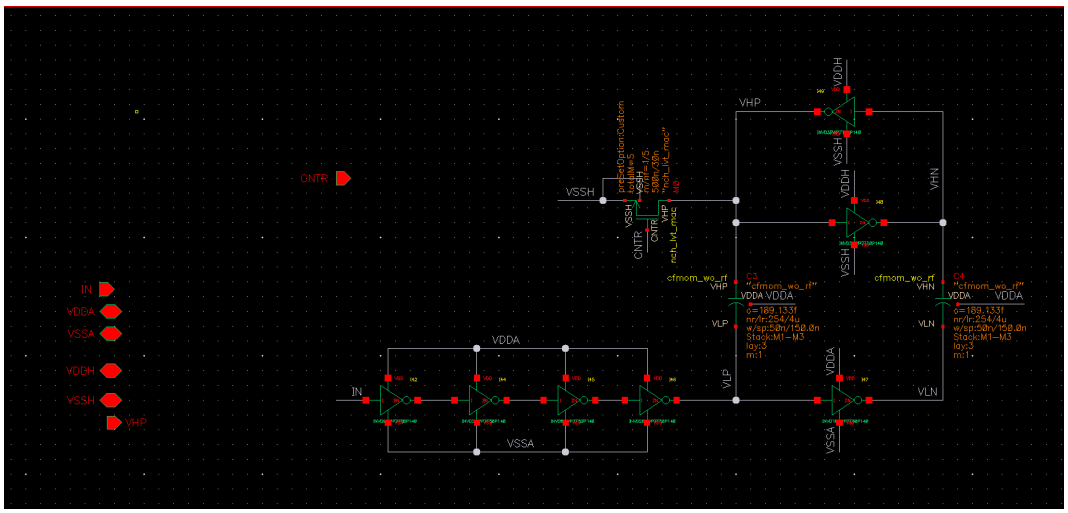


Figure 2.3: The Level-Shifter circuit implementation

Along with introducing a large resistance seen by the capacitors, the inverters constituting the latch increase the circuit robustness by continuously refreshing the signal and sensing changes on both sides of the circuit (VHN and VHP). On the other hand, the circuit is driven by a series of buffers sized in order to decrease the delay of the circuit. The sizings of these buffers have been chosen based on the logical effort model which takes into account the driving gate input capacitance, its size and current driving capabilities, and the capacitive load which has to be driven.

Starting with the inverters constituting the memory latch, a high resistance is needed. As for the inverter between VLP and VLN, its size has been decided on through the logical effort model. The exact sizings are listed below :

Identifier	**NMOS**	**PMOS**	**FINGERS**
Buffer Chain (1)	W = 0.1μ	W = 0.11μ	1
Buffer Chain (2)	W = 0.4μ	W= 0.44μ	2
Buffer Chain (3)	W = 1.6μ	W = 1.76μ	8
Buffer Chain (4)	W = 4μ	W = 4.4μ	20
Inverter between VHN and VHP	W = 3.2μ	W = 3.52μ	16
Both Latch Inverters	W = 0.6μ	W = 0.66μ	3
Clamp Transistor	W = 0.5μ	**NA**	5

Table 2.1: Transistor sizings presented in the level shifter main block with a common length equal to the minimum value allowed by the technology ($L_{min} = 30nm$). The total widths are presented and the number of fingers (which is the same for the NMOS and PMOS devices when applicable in this case) is also indicated. The width per finger can be obtained by the division of the written width by the number of fingers.

Referring to table 2.1, the Buffer Chain inverters are numbered from left to right corresponding to Fig. 2.3. Additionally a 189.133 fF main capacitor value has been used on both sides of the circuit. On the other hand, it is worth mentioning that in order to balance the inverter and set the switching threshold in the middle of the voltage range, the PMOS width is 10% bigger than that of the NMOS. As for the clamping transistor, a low threshold flavor (the same transistor but characterized with a lower threshold voltage) was utilized. This choice was made due to the operation of the startup circuit and the need to properly set the initial state of the memory latch. The gate voltage signal CNTR of this transistor increases with VDD, turning it on and allowing the device to set the memory state as its source is connected to VSSH (see Fig. 2.3). Above a certain VDD value the CNTR signal drops quickly to zero (this will be elaborated upon in the next section), then the clamping transistor is turned off. In order to benefit and guarantee a proper initialization, a lower threshold is desired so that the transistor is turned on earlier in time and therefore conducts for a longer duration. A lower threshold voltage is also beneficial for Process, Voltage, and Temperature (PVT) variations as the transistor is guaranteed to sufficiently conduct in these conditions.
The generation of the CNTR signal (the clamping/initializing signal) will be discussed in the next section along with the operating principle of the startup circuit.

2.3 The Startup Circuit

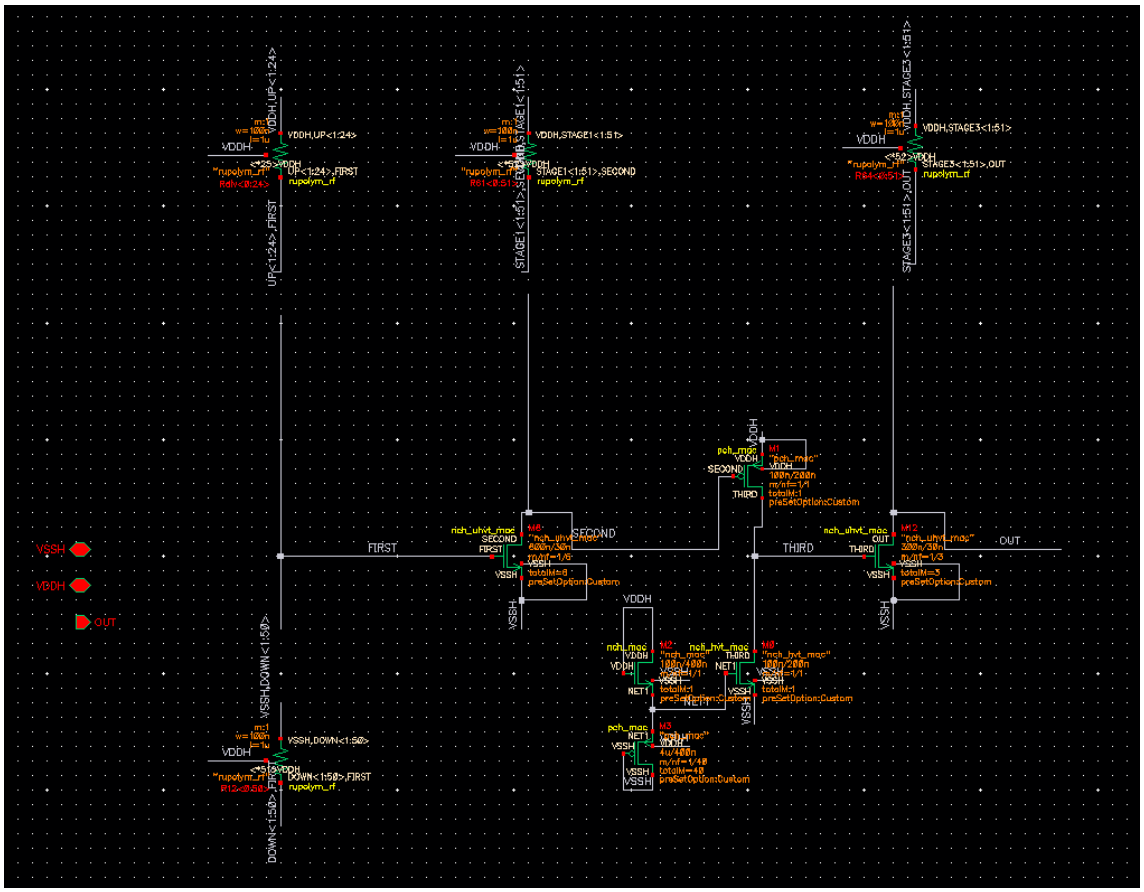


Figure 2.4: The Level-Shifter circuit implementation

In this section, the design approach and methodology used to design the startup circuit will be discussed along with simulations performed across process, voltage, temperature, and statistical mismatch variations.

2.3.1 Working Principle & Design approach

2.3.1.1 Working Principle

The power supply signals VDDH and VSSH (shown above in Fig. 2.4) need a finite time to rise to their steady-state value. The voltage ramp is set to be 1ms long (the full rise time of the power signals i.e. to 100 % of their steady state value), the circuit was also tested for a rising voltage ramp of $100\mu s$. The two ramp durations can be seen as the maximum and minimum durations respectively. Only VSSH and VDDH were mentioned since they constitute the power rails of the latch memory which is initialized by the startup circuit. As mentioned before, the values of VDDH

and VSSH will correspond to the highest voltage domain the level shifter is used to set, therefore VDDH is 5 V while as VSSH is 4.1 V at steady state.
Referring to Fig. 2.4, initially:

- **FIRST : is zero and it steadily increases as the voltage difference between VDDH and VSSH increases**
- **SECOND: is zero and it steadily increases as it is being pulled up by the resistor connected to it**
- **THIRD : is zero and it is being pulled down by the transistor biased by nmos and pmos pair, since the pull-up pmos M1 is initially off**
- **OUT : is zero and it steadily increases as it is being pulled up by the resistor connected to it, turning on the clamping transistor**

The main goal of this circuit is to activate the clamped transistor previously discussed in the level shifter and properly initialize the latch state. Therefore, it is important that the OUT signal goes to a voltage level that is able to properly activate the clamp. FIRST initially steadily increases from zero to a certain value determined by the voltage divider. At a certain value the FIRST voltage level is enough to turn on transistor (M8), and therefore a significant current will flow in the second stage of the branch which will cause the voltage to drop across the resistor, so the NMOS (M8) effectively pulls down the node SECOND down to zero. Due to that, PMOS (M1) is activated and manages to pull up the signal THIRD which was initially at zero and sets it to VDDH, since the PMOS is significantly more powerful than the NMOS which is responsible for initially pulling down the circuit. Finally, OUT which was steadily increasing with (VDDH-VSSH) gets pulled down to around zero volts since THIRD activates transistor (M12) and therefore the voltage is made to drop across the resistor. This mechanism guarantees that the clamping transistor is initially turned on to initialize the output of the level shifter, while it is switched off after a certain value of VDDH-VSSH is reached.

2.3.1.2 Design Approach

The main goal of this circuit is to manage to effectively clamp the latch to a proper/predictable state, therefore OUT needs to reach a value which is sufficient to turn on the clamp and then go down to zero. In order to achieve that, the voltage divider resistor values were chosen in order to delay the increase of FIRST, in order to delay OUT being pulled down. In addition to that, ultra high threshold voltage transistor flavors were used in order to achieve the same goal (allow OUT to be maximized). The third stage was designed in a different way due to the presence of the self biased transistor (the self biased transistor was only used here and not in the other branches because the trade offs it imposed in other branches were very difficult to balance, and it ended up degrading the waveforms). It is important to note that the third branch can be designed as a transistor with a pull down resistor, but this

has been avoided in order to save space on the chip, and the proposed design works well. Transistor sizes were selected based on having the proper capability to pull up or down a node while decreasing the steady state current to the lowest achievable value. Three stages were used in order to amplify the varying waveform and make it look like a digital signal that goes from rail to rail. Less stages lead to performance issues while more stages are redundant and lead to extra power consumption.

Transistor	**Sizing**	**Flavor**
M6	W = 600n L = 30n	UHVT
M2	W = 100n L = 400n	Standard
M3	W = 4μ L = 400n	Standard
M1	W = 100n L = 200n	Standard
M12	W = 300n L = 30n	UHVT
M0	W = 100n L = 200n	UHVT

Table 2.2: Transistor sizings in the Startup circuit. UHVT stands for the Ultra High Threshold Voltage flavor.

The values presented in Table 3.2 were obtained by satisfying the control signal (Output, OUT in Fig. 2.4, and CNTR in Fig. 2.3) waveform characteristics through simulation.

2.3.2 Startup Circuit Simulation Results

Hundreds of simulations were conducted on this circuit as achieving a balance between performance and consumption (drawn branch current) was not a trivial task. The final simulations will be shown, and they will consist of FIRST, SECOND, THIRD, and OUT for a 1 ms (VDDH/VSSH) voltage ramp. There will be several similarly behaving waveforms, this is due to simulating process and temperature variations and outputting them on the same figure. As for voltage variations, the ideal level is 4.1 V for VSSH, 5V for VDDH and 0.9V for the input pulses. Taking into account a 10% voltage variation, the circuit has to function for the voltage range of $(0.8 \rightarrow 1)$V for the input pulses.
The most critical value is 0.8V, therefore VSSH, VDDH, and the pulse amplitude will be 4.1V,4.9V,and 0.8V respectively. The circuit operates exactly the same in all voltage ranges if it operates properly at a 0.8V input pulse amplitude. Finally, only three temperatures were simulated, (-30,27(room temp),100) $^{\circ}$**C** these temperatures represent the minimum, typical and maximum temperatures respectively.

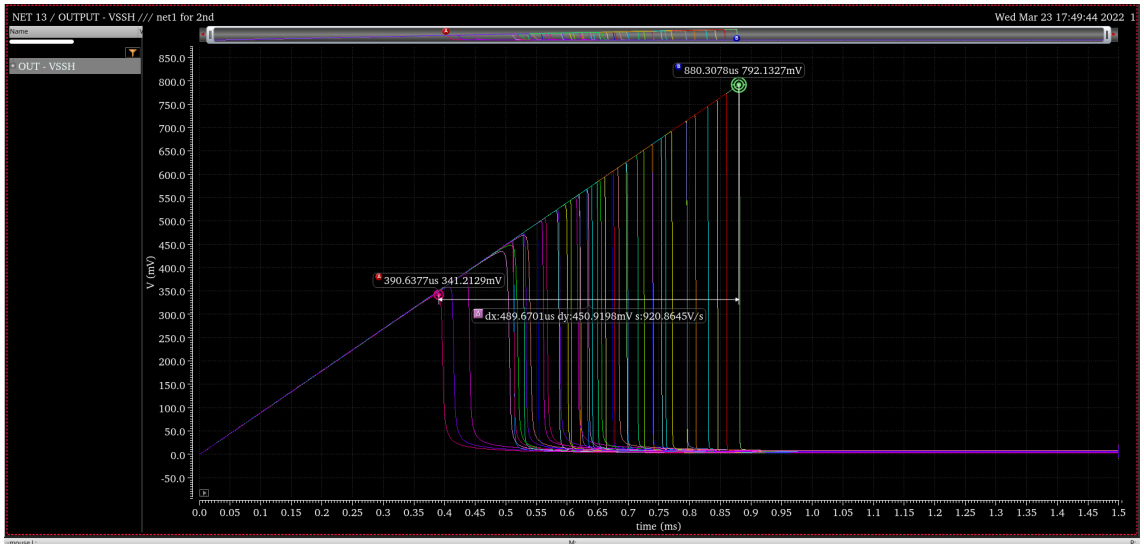


Figure 2.5: OUT-VSSH, represents VGS of the clamping transistor.

It is important to note the effect of temperature. As it increases, the devices can be seen as if they are sped up at low VGS as more current flows through them due to the thermal generation of carriers thus lowering the threshold voltage and increasing leakage current. At high VGS this is no longer true since the mobility degradation effectively leads to a lower current conduction at a higher temperature. The main operation of this circuit takes place when the power rails are rising in potential (startup phase) , consequently the gate voltages that determine when the control signal i.e. the output goes to VSSH are inherently low (around the threshold voltage). Steady state conduction is not important for this circuit as it should only work at startup when the power supply voltages are rising. The dual of this effect can be applied at low temperatures as well. Due to the arguments given above, the control signal OUT goes to VSSH at a significantly lower value of (VDDH-VSSH) in high temperature conditions than in the nominal case (room temperature $27°\mathbf{C}$), and much later (slower) than that at lower temperatures. This can be seen in Fig. 2.5, where the pink and green points represent the signal at 80 $°\mathbf{C}$ and -30 $°\mathbf{C}$ respectively.
The flavor of the used clamp is low Vth (threshold voltage) also indicated by lvt, therefore it is turned on sufficiently and is actually able to initialize the latch state properly before the CNTRL signal drops to VSSH in all PVT corners.

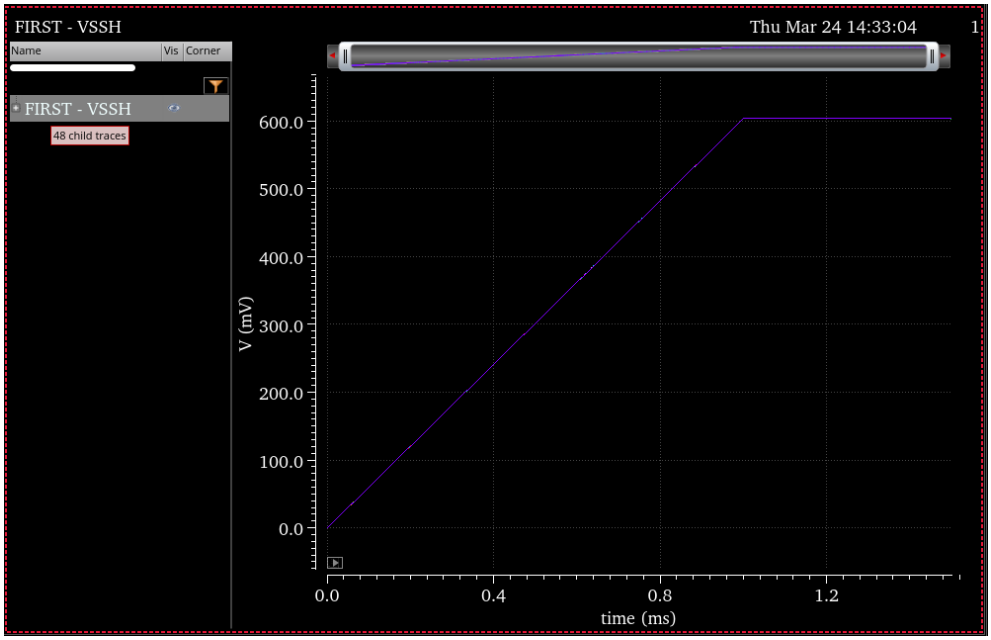


Figure 2.6: First-VSSH, represents VGS of transistor M8.

As expected, the "FIRST" signal does not change around process corners since it is set by a resistive voltage divider and the ratio between the resistors is always the same since they are affected by corners equally. The same cannot be said about signals "SECOND" and "THIRD" which are significantly affected as shown in Fig. 2.7 and 2.8 respectively.

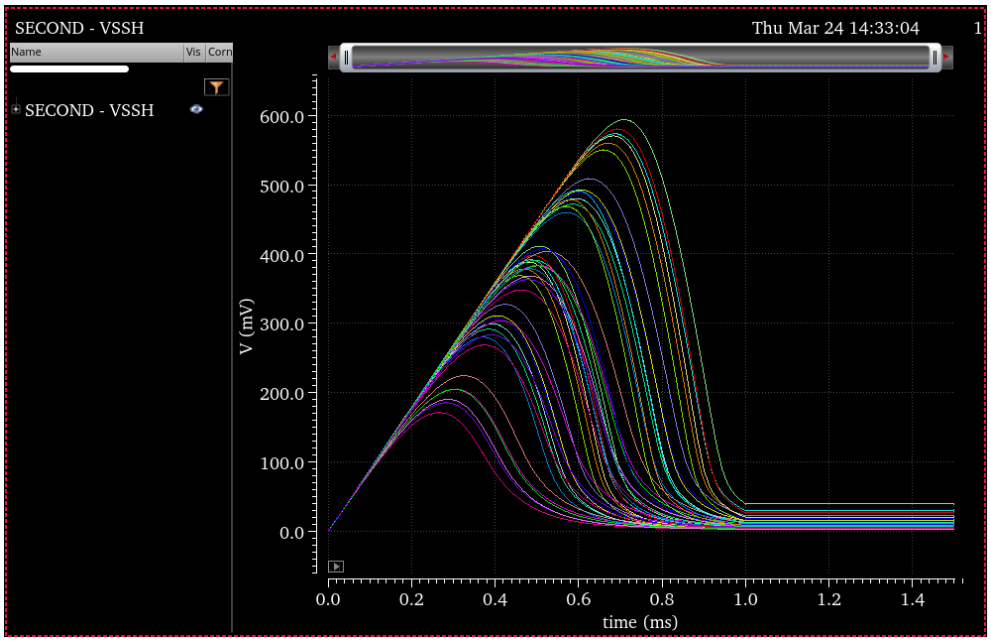


Figure 2.7: Second-VSSH.

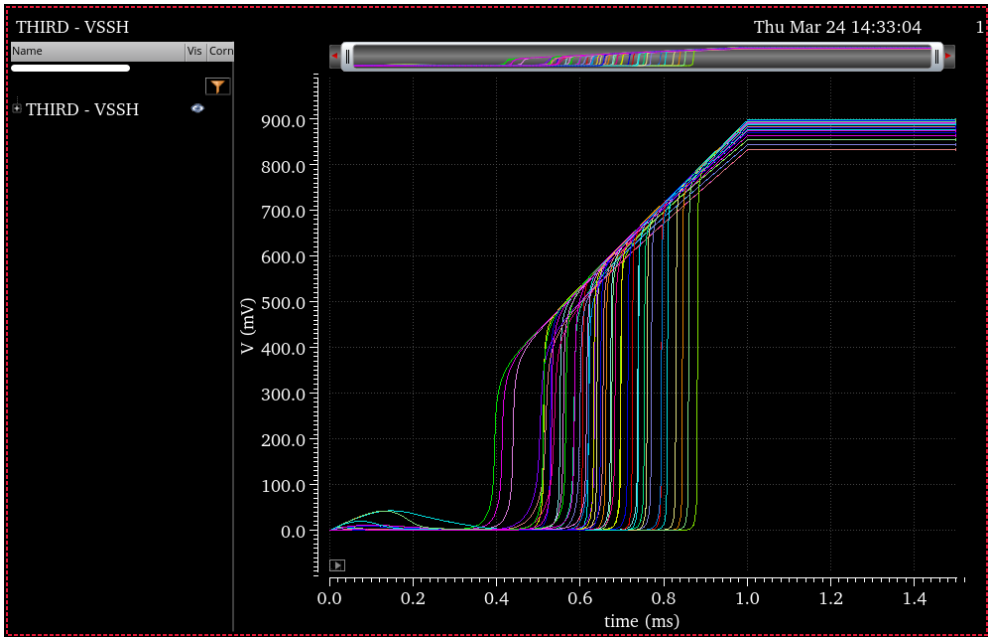


Figure 2.8: Third-VSSH, represents VGS of transistor M12.

Even with the signal variation with PVT corners, the circuit operated properly and correctly set the latch to the required state.

2.4 Single Event Effects and Measures Taken to Minimize them

As discussed in the previous chapter, single event effects can be modeled by current sources that inject/sink current from specific nodes. In order to avoid errors caused by single events such as the modification of the latch state, triplicating the circuit and utilizing a successive voting circuit is the best approach.

2.4.1 Single Event Testing Schematics

In this section, single events were modeled as ideal current sources, and both of the current injection/sinking characteristics shown below were tested (representing the maximum value of Linear Energy Transfer that is present in the application, 40 $\frac{MeVcm^2}{mg}$).

- **4 mA current amplitude with a 50 ps rise time and 150ps fall time**
- **400 uA current amplitude with 500ps rise time and 1500ps fall time**

Both injection types have similar effects, therefore in order to avoid any redundancy the faster and bigger amplitude injection/sink is presented. Both types of injections lead to a change in state of the latch, therefore the circuit has to be made more robust. As a final remark, nodes which are continuously low or high in steady state were not simulated for discharges, and injections respectively since discharging a low node or charging a high node will not change the logic state of the node. In addition, it is assumed that no single events occur during the 1ms power up phase.

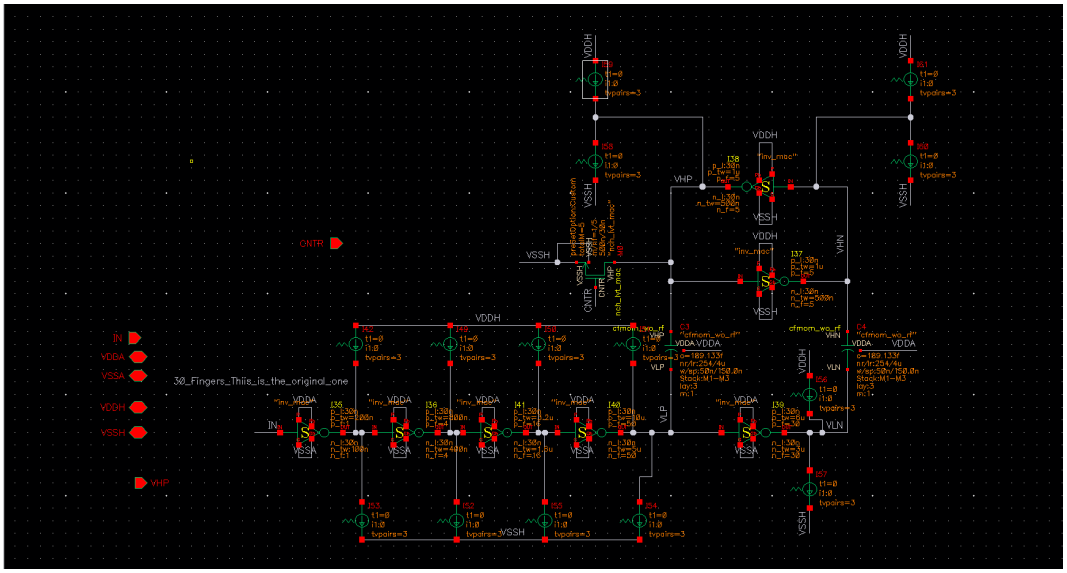


Figure 2.9: The level shifter schematic with the current sources modeling single events.

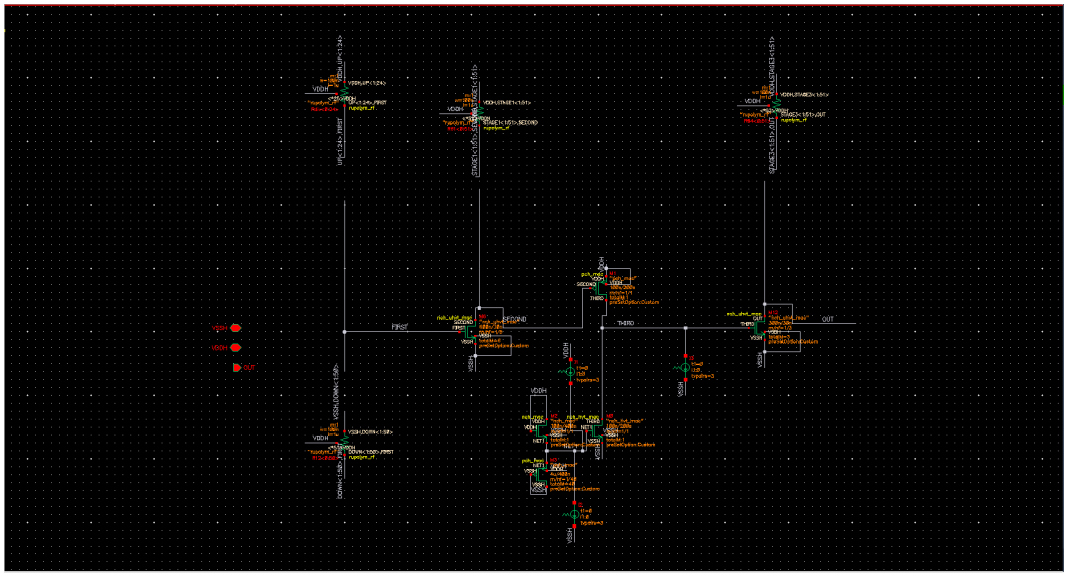


Figure 2.10: The start-up schematic with the current sources modeling single events.

It is crucial to specify that no two current sources conduct at the same time in the complete circuit (start-up + level shifter). This is due to the fact that single events can typically only affect one node/device at a time in the target application. Therefore, all of sensitive nodes are studied individually for single events. This is reflected in simulations by defining a certain delay time between each of the current sources, in a way that after the circuit recovers from a single event at a sensitive node the successive single event is simulated by a current injection at the next sensitive node.

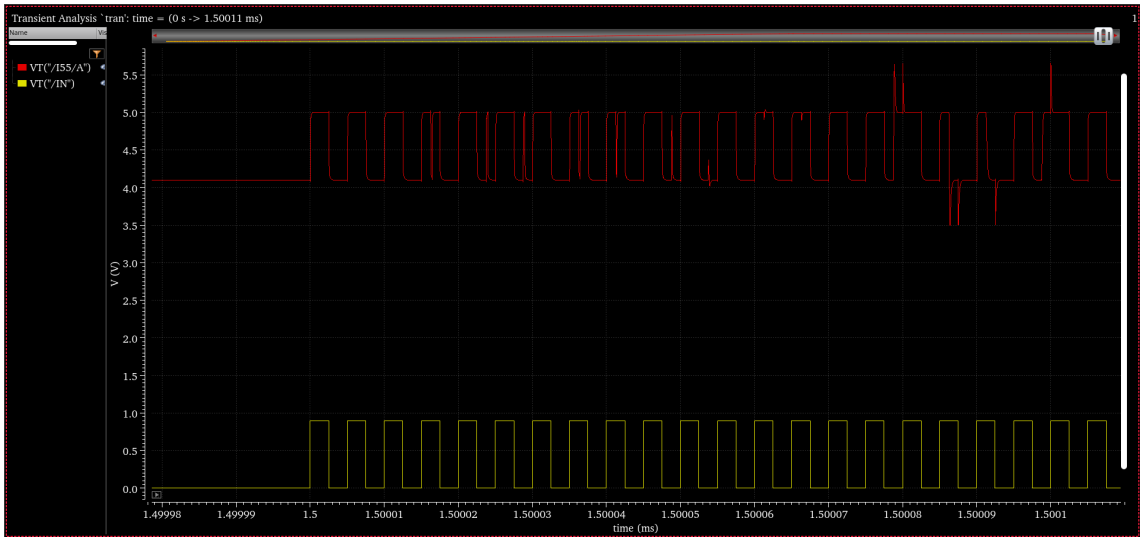


Figure 2.11: Single Event Effects leading to a state change.

As what is observed in Fig. 2.11 above, some single events affect the state of the latch and lead to an incorrect output. This is detrimental for the proper operation

of the circuit, therefore the circuit has to be made robust to single event effects.

2.4.2 Immunizing the Circuit to Single Events

Single events can only effect one node/device at a time, therefore one of the simplest approaches to address single events is to triplicate the circuit and route all outputs to voters which will set the output to the majority (2/3) state (this approach can be only used in digital circuits, the level shifter output is indeed digital). Therefore, an error on one level shifter will not propagate to the output of the circuit. The three voters which were instantiated have their outputs shorted together, such that if one outputs the wrong value due to a single event affecting it (the voter itself), the two other voters can either pull it up or down since they have double the driving capability.

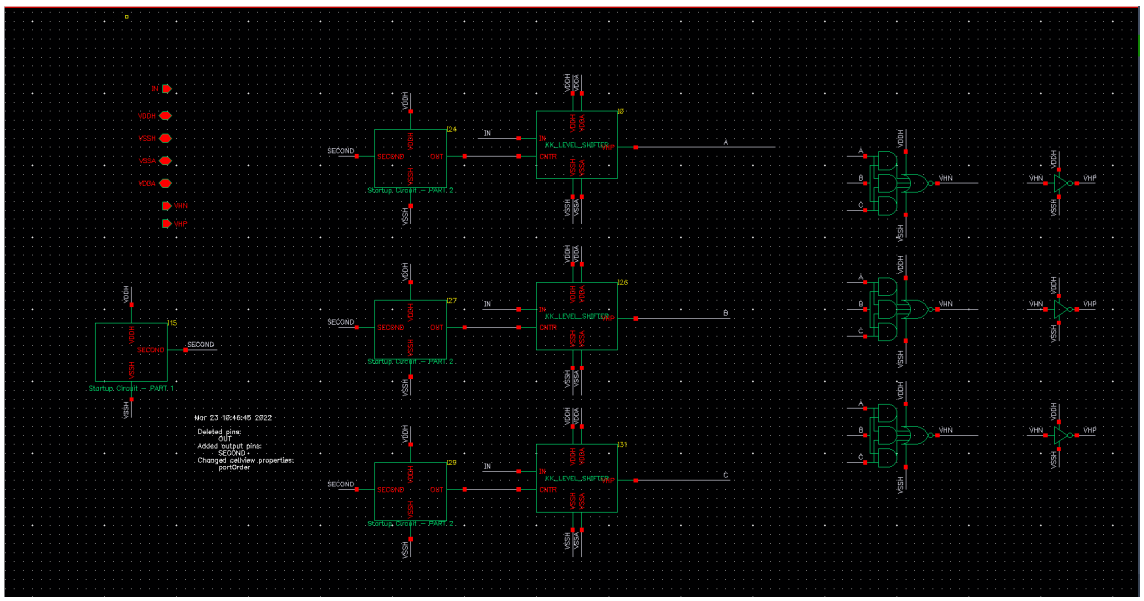


Figure 2.12: The triplicated circuit.

It is important to highlight that the startup circuit only needs to be triplicated partially since the first two stages of the circuit are practically immune to any single events as discussed in the previous section (in steady-state, their logic value is such that it cannot be modified by a single event), therefore only two stages are triplicated, thus saving a lot of area due to the reduced number of resistors. This can be observed in Fig. 2.12. In addition, the complementary signal to VHN, which is VHP is now generated by simply inverting the output of the inverting voting circuit. All of the inverter outputs are shorted together due to the same reasoning introduced above.

2.5 Final Simulation & Monte Carlo Sampling

The total delay of the triplicated level shifter changes with temperature, voltage and process corners. Nominally at 27 °C and at a 0.9 V input pulse amplitude, the delay is 32.63 ps. Fig. 2.16 presents a summary of the total rise and fall delays of both VHN and VHP.

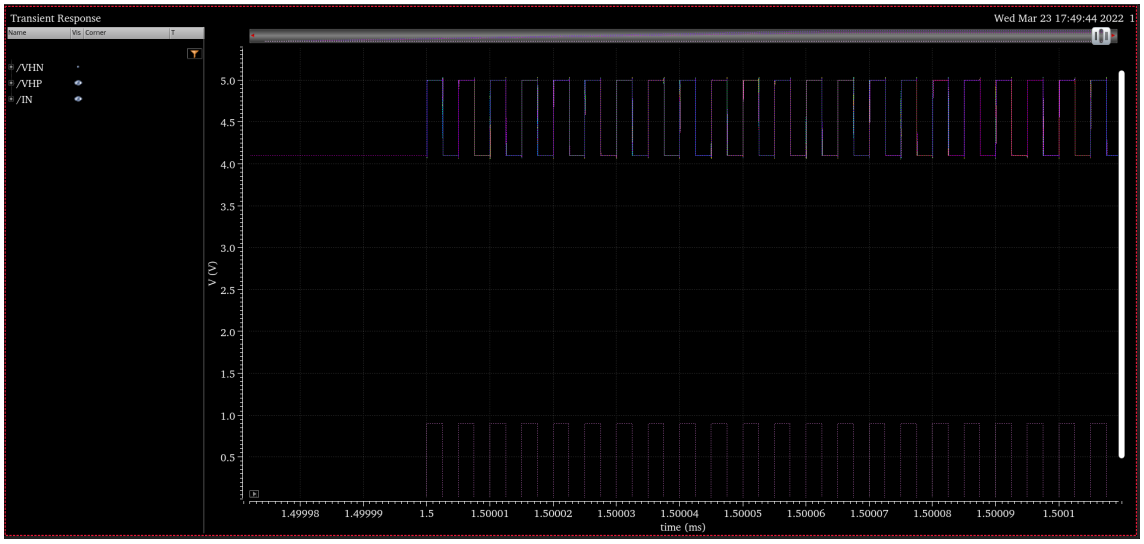


Figure 2.13: The final simulation, with VHN hidden for better visibility.

As for the Monte Carlo sampling, two simulations consisting of 200 points each were performed, the first with a statistical variation covering process and mismatch and the other covering mismatch only.

Test	Name	Yield	Min	Target	Max	Mean	Std Dev	Cpk	Errors
Yield Estimate: 100 %(200 passed/200 pts)	Confidence Level: <not set>	Filter: <not set>							
KK_StackedTank28:KK_LEVEL_SHIFTER_TB:1									
	IN/VHN rising falling(summary)	100% (200/2...	29.28p		38.1p	32.81p	1.592p		0
	IN/VHN rising falling_MC-GENERAL	100% (200/2...	29.28p	info	38.1p	32.81p	1.592p		0
	IN/VHN falling rising(summary)	100% (200/2...	29.63p		37.82p	33.43p	1.562p		0
	IN/VHN falling rising_MC-GENERAL	100% (200/2...	29.63p	info	37.82p	33.43p	1.562p		0
	IN/VHP falling falling(summary)	100% (200/2...	31.94p		41.18p	36.12p	1.768p		0
	IN/VHP falling falling_MC-GENERAL	100% (200/2...	31.94p	info	41.18p	36.12p	1.768p		0
	IN/VHP rising rising (summary)	100% (200/2...	32.1p		41.83p	35.97p	1.776p		0
	IN/VHP rising rising _MC-GENERAL	100% (200/2...	32.1p	info	41.83p	35.97p	1.776p		0
	Delay between A and VHN(summary)	100% (200/2...	8.35p		13.32p	10.83p	856.2f		0
	Delay between A and VHN_MC-GENERAL	100% (200/2...	8.35p	info	13.32p	10.83p	856.2f		0
	Delay between B and VHN(summary)	100% (200/2...	8.928p		13.25p	10.79p	905f		0
	Delay between B and VHN_MC-GENERAL	100% (200/2...	8.928p	info	13.25p	10.79p	905f		0

Figure 2.14: Monte Carlo simulations covering process and mismatch statistical variation.

Test	Name	Yield	Min	Target	Max	Mean	Std Dev	Cpk	Errors
Yield Estimate: 100 %(200 passed/200 pts)	Confidence Level: <not set>	Filter: <not set>							
KK_StackedTank28:KK_LEVEL_SHIFTER_TB:1									
	IN/VHN rising falling(summary)	100% (200/2...	31.69p		34.25p	32.76p	416.4f		0
	IN/VHN rising falling	100% (200/2...	31.69p	info	34.25p	32.76p	416.4f		0
	IN/VHN rising falling_MC-GENERAL	100% (200/2...	31.69p	info	34.25p	32.76p	416.4f		0
	IN/VHN falling rising(summary)	100% (200/2...	32.08p		34.8p	33.37p	433.2f		0
	IN/VHN falling rising	100% (200/2...	32.08p	info	34.8p	33.37p	433.2f		0
	IN/VHN falling rising_MC-GENERAL	100% (200/2...	32.08p	info	34.8p	33.37p	433.2f		0
	IN/VHP falling falling(summary)	100% (200/2...	34.44p		37.66p	36.05p	485.5f		0
	IN/VHP falling falling	100% (200/2...	34.44p	info	37.66p	36.05p	485.5f		0
	IN/VHP falling falling_MC-GENERAL	100% (200/2...	34.44p	info	37.66p	36.05p	485.5f		0
	IN/VHP rising rising (summary)	100% (200/2...	34.73p		37.29p	35.9p	456.4f		0
	IN/VHP rising rising	100% (200/2...	34.73p	info	37.29p	35.9p	456.4f		0
	IN/VHP rising rising _MC-GENERAL	100% (200/2...	34.73p	info	37.29p	35.9p	456.4f		0
	Delay between A and VHN(summary)	100% (200/2...	9.479p		12.76p	10.79p	502.6f		0
	Delay between A and VHN	100% (200/2...	9.479p	info	12.76p	10.79p	502.6f		0
	Delay between A and VHN_MC-GENERAL	100% (200/2...	9.479p	info	12.76p	10.79p	502.6f		0
	Delay between B and VHN(summary)	100% (200/2...	8.958p		12.28p	10.75p	524.1f		0
	Delay between B and VHN	100% (200/2...	8.958p	info	12.28p	10.75p	524.1f		0
	Delay between B and VHN_MC-GENERAL	100% (200/2...	8.958p	info	12.28p	10.75p	524.1f		0

Figure 2.15: Monte Carlo simulations covering mismatch statistical variation only.

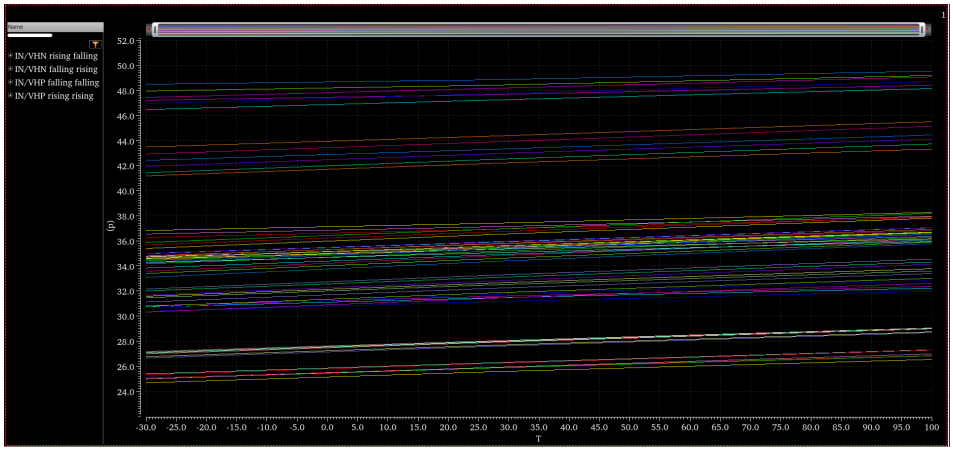


Figure 2.16: Delay Overview across process/voltage/temperature corner simulations.

In Fig. 2.16, the resulting input-to-output delay of the designed level shifter across process, voltage and temperature simulations is presented. A trend of increasing delays can be observed with increasing temperature. According to what was explained previously, transistors with high gate voltages (high VGS) output less current compared to their operation at low temperatures with the same biasing conditions. This is due to the mobility degradation of the main carriers which are responsible for conduction. In this case, transistors are switched with a VGS of ($0.8V \rightarrow 1V$) where as the switching in the startup circuit took place at around ($0.3V \rightarrow 0.5V$). An undesirable faster behaviour was observed due to the lowered threshold voltage and increased leakage current in the startup circuit. The delay of the circuit is measured as the delay in time between the rise (fall) of the input pulse and the subsequent rise (fall) of the level shifter output pulse. This is applied to both VHN and VHP. Given that, the worst case delay of this circuit is around 49 ps.

Chapter 3

The Beta Multiplier

3.1 Introduction & Circuit Overview

The switched tank topology shown below in Fig. 3.1 consists of several basic cells stacked on top of each other. One of the consequences of this topology is that every basic cell of the tank belongs to a different voltage domain.

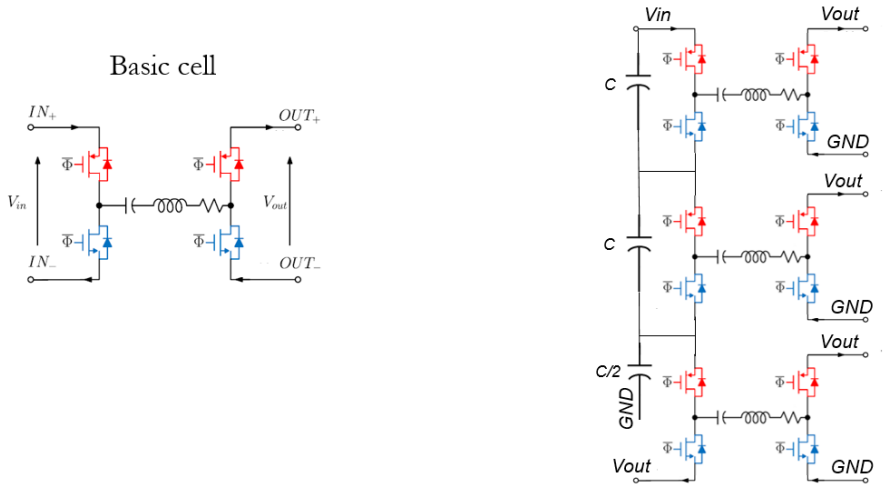


Figure 3.1: The basic (left) and stacked cell (right) representations

In order to properly drive the basic cell's transistors using a pulse width modulated signal several components were designed (shown below in Fig. 3.2). These blocks consist of current references, linear regulators and level shifters. This chapter concerns the Beta multiplier which is used to provide somewhat of a constant current (independent of supply voltages) to the linear regulator, which in turn produces the required voltages that belong to the correct ranges for driving the transistors without stressing them with over-voltages.

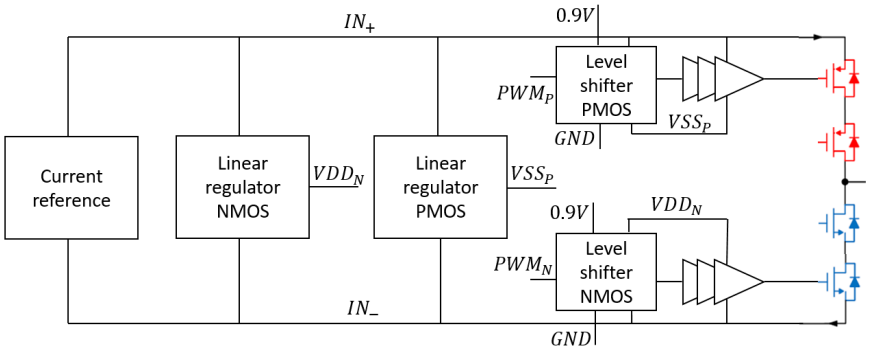


Figure 3.2: The basic (left) and stacked cell (right) representations

The designed block consists mainly of two parts, the main current reference (the beta multiplier itself) and a startup circuit. The role of the startup circuit is to inject current into one or several branches of the multiplier in order to kick-start the proper operation and set the circuit to the correct operating point.

This block's main challenge is constituted by the wide range of the supply voltage (0.9 $\rightarrow$ 1.8)V, which significantly exceeds the voltage rating of the used transistors (0.9V). The other challenging aspect of this design is to achieve a relatively low variability with temperature, process , mismatch and voltage variations. Several techniques (addressed in the following section) have been used to meet these requirements.

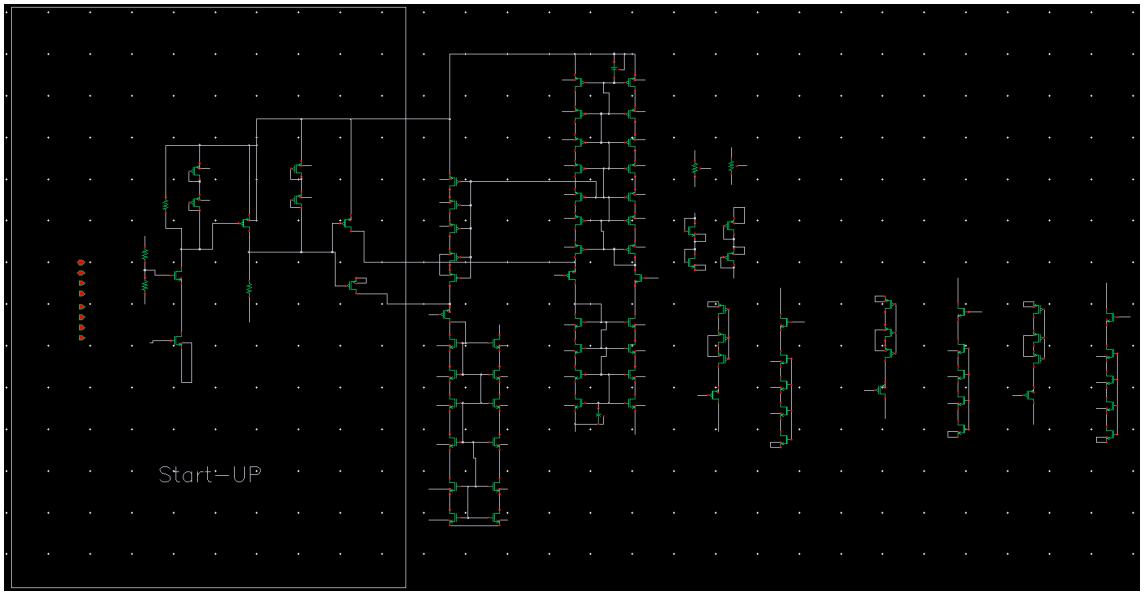


Figure 3.3: The complete Beta Multiplier circuit implementation

The annotated image shown in Fig. 3.3 shows the complete circuit that consists of a startup circuit on the left, the main current reference in the middle and the

copy branches along with voltage generating branches on the right. An in depth explanation on these branches will follow.

3.2 The Design Approach

In this section, the general approach and methodology used to design the circuit in a way to make it conform to the specifications while protecting all core transistors from over-voltages will be discussed. Initially, voltage stress (over-voltage) protections will be elaborated upon and their use will be explained.

3.2.1 Over-Voltage Protection

As mentioned in the introduction of this chapter, core transistors are not able to withstand voltages exceeding 0.99V (the voltage rating of 0.9V plus a 10% tolerance). This is not an issue at the minimum operating voltage (0.9V), while it poses a risk at the higher end of the voltage range presented above (0.9 $\rightarrow$ 1.8)V. In order to guarantee the proper operation of the circuit, two types of clamps have been implemented. A driven clamp and an un-driven clamp, with the latter consisting of two or more diode connected transistors.

3.2.1.1 Driven Clamps

As the name suggests, driven clamps are controlled by a fixed gate voltage set by either a resistive voltage divider or a series of diode connected transistors and a resistor. The latter can be seen in Fig. 3.4.

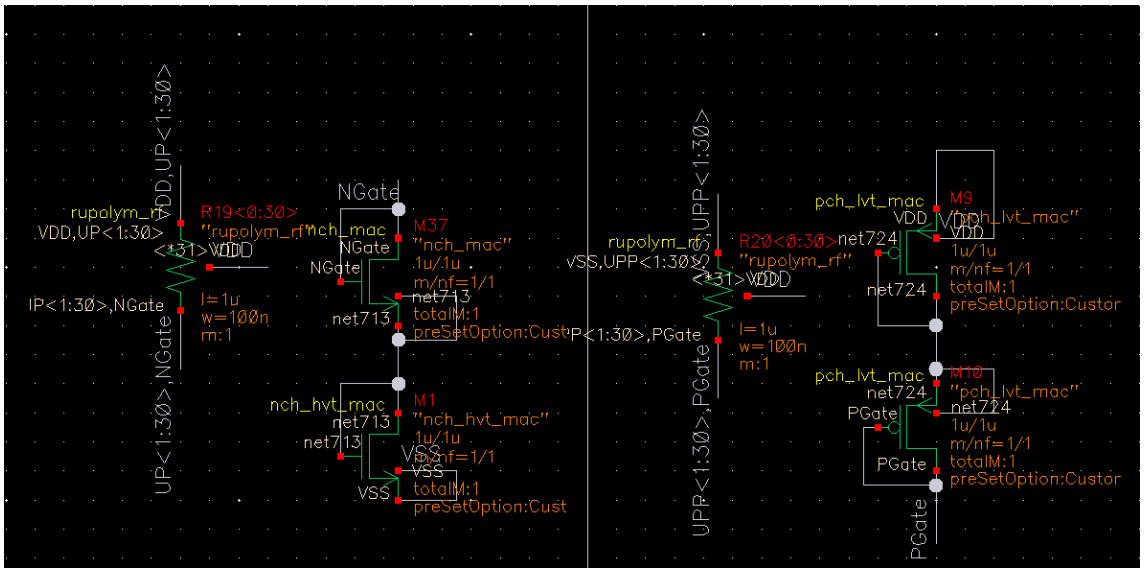


Figure 3.4: The driving voltage generator.

The operating principle of this (Fig. 3.4) small circuit is the following: at startup, as VDD increases the drop across the resistor remains initially zero since no current is flowing yet in the circuit, while the diode connected transistors starts to have a voltage drop across them. After VDD exceeds the threshold voltage of the transistors, current starts to conduct through the transistors and is then limited by the resistors, which will have a significant drop across them. Due to the square law that links the transistor's current and its voltage, the drain voltage changes only moderately with VDD. Since VD = VG then the transistor is always in saturation since VDS > VGS - Vth, the characteristic of the device is described in the following equation (assuming strong inversion and neglecting the early and body effects) :

$$I_D = \mu C_{OX} \frac{W}{2L}((V_G - V_S) - V_{th})^2 \tag{3.1}$$

Applying $V_G = V_D$ and the Ohm law :

$$\frac{V_{DD} - V_D}{R} = \frac{\beta}{2}(V_D - V_{th})^2 \tag{3.2}$$

where $\beta = \mu C_{OX} \frac{W}{L}$, solving for V_D :

$$V_D = \frac{\beta R V_{th} - 1 + \sqrt{1 + 2\beta R(V_{DD} - V_{th})}}{\beta R} \tag{3.3}$$

In other words, changing the supply voltage while maintaining the resistance value only leads to a different current which does not greatly affect the generated voltage. Since the driven clamps do not require a very accurate voltage, this small variation does not cause any issues. The obtained voltage depends directly on the number of diode connected transistors in series, in fact it can be approximated by the threshold voltage on one transistor multiplied by the total number of diode connected transistors in series. In this, for the Nside (left of Fig. 3.4) the voltage, Ngate is around 600mv above VSS. On the other hand, the Pside generated voltage Pgate is around 600mv less than VDD (Right of Fig. 3.4).

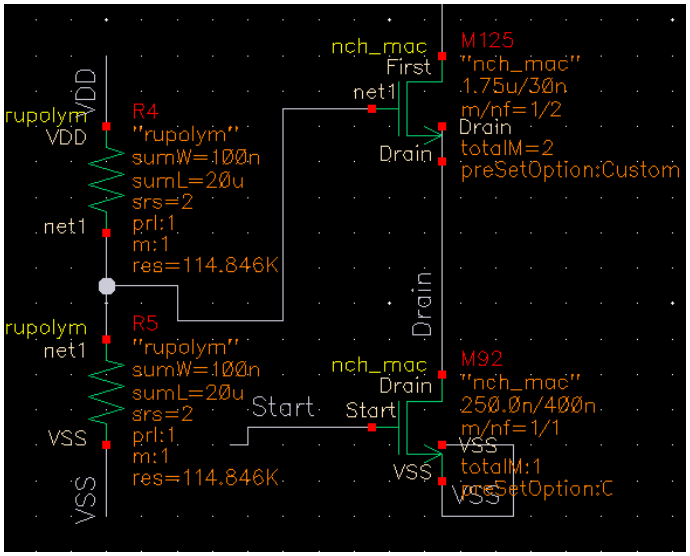


Figure 3.5: A driven clamp.

Fig. 3.5 shows a driven clamp which is implemented throughout the circuit, but in this case it is driven by a voltage divider rather than using diode connected transistors as discussed earlier. Regardless of the driving voltage generation method, the driven clamps behave in the same way. In fact they possess a constant gate voltage, in addition to a constant current that flows across them, and since they are operated in saturation, their source voltage is determined by their W/L ratio. This is apparent in the Mosfet saturation equations below.

$$I_{NMOS} = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - VT)^2 \tag{3.4}$$

$$I_{PMOS} = \frac{1}{2}\mu_p C_{OX}\frac{W}{L}(V_{SG} - VT)^2 \tag{3.5}$$

Therefore, by changing the conductive capability of the transistor, the source voltage increases or decreases in a way to compensate that change. Using this method, voltages across transistors can be manipulated in order to never go over the 0.99V limit. For example, if an NMOS clamp was increased in width with a constant length, such that W/L increases, the source voltage increases in order to maintain the same current which is set by other parts of the circuit. The opposite can be said for the source voltage of a Pmos in the same setting/conditions.

3.2.1.2 Un-Driven Clamps

In some situations, mostly at startup some node voltages increase/decrease a lot in amplitude and thus lead to over voltages on some devices, therefore the undriven clamps automatically pull up/down the node back to acceptable values.

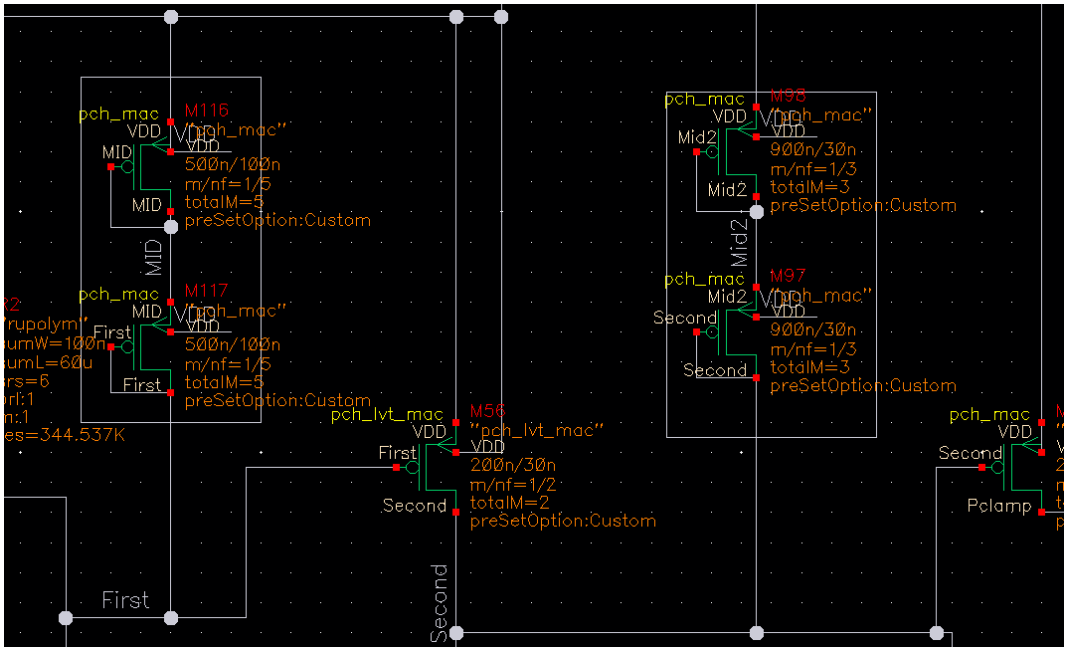


Figure 3.6: Un-driven clamps.

Two undriven clamps can be observed in Fig. 3.6 (enclosed by rectangles). Similarly to what was mentioned before, the transistors with gates connected to drains as shown above can be treated as diodes. Therefore, since these clamps are connected between a voltage node and VDD, they are activated only when the node voltage falls to a value such that VDD - VNode (node voltage) is greater than two times the threshold voltage of one transistor, since there are two connected in series in this case. When activated, the transistors pull up the node to a higher voltage thus preventing the voltage to fall too low and risk damaging the transistors by the induced over-voltage.
At least one protection clamp is placed on every branch of the circuit. In other words, the clamps are fundamental for guaranteeing the proper operation of the current reference for the operating voltage range.

3.2.2 Used Typology and Variability Minimization

As a first approach, a current reference based on a beta multiplier topology was implemented. The schematic [6] is presented in Fig. 3.7. Furthermore, a brief discussion will be made on the operating principle along with expanding on the reason this circuit fails to meet variability specifications, and thus the need to move to a different topology.

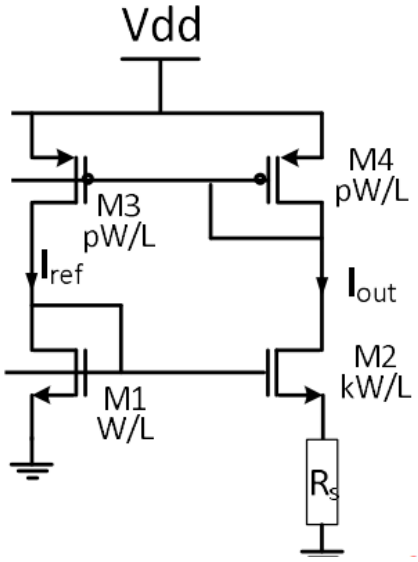


Figure 3.7: The Beta multiplier topology/circuit introduced at EPFL [6].

A beta multiplier is a circuit that is used to provide a supply independent current. It is typically a circuit that has a constraint imposed on it in order to uniquely define the constant current. This constraint can be introduced by the resistor presented in Fig. 3.7. The output current of the beta multiplier topology can be shown to be:

$$I_{out} = I_{ref} = \frac{2}{n\beta Rs^2}(1 - \frac{1}{\sqrt{k}})^2 \tag{3.6}$$

Where, n is the body factor, $\beta = \mu_n C_{OX} \frac{W}{L}$, Rs is the resistor, and k is the multiplication factor of the $\frac{W}{L}$ ratio of transistor M2 compared to that of M1. The equation governing this circuit has multiple solutions, in fact the circuit can either produce $I_{OUT} = I_{REF} = 0$ or the unique current defined in equation 3.6 above. This imposes the need for having a startup circuit that injects some current into one or several branches of the circuit and jump starts its proper operation by pushing it towards the desired operating point.
This topology utilizes a resistor to set the current, due to its relative simplicity it was the first topology to be explored. This has been later dropped due to the presence of a very high variability with process corners and temperature, which mainly arises from the process corner effects on the resistance. In the used technology, process corners can change the resistance by +- 20%. Looking at equation 3.6, it can be seen that such a variation on the constraining resistor (Rs) would lead to significant variations that lie outside the acceptable ranges for the generated current.

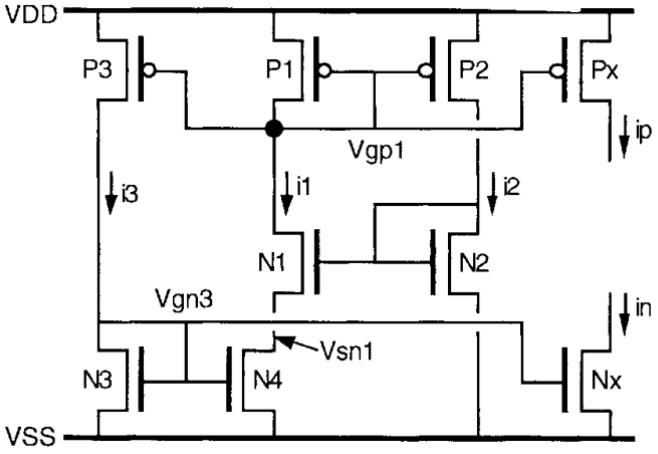


Figure 3.8: The Adopted Resistor-less Beta multiplier topology/circuit[7].

Due to the reasons mentioned above, a new topology was adopted based on [7]. The new topology can be found in Fig. 3.8 where the resistor is replaced by a transistor operating in the triode region. According to the figure presented above, the resistance effect is achieved by creating a copy branch that copies the current through P3 by using the gate voltage of P1 and P2. Then transistors N3 and N4 are sized in a way to push them in strong inversion while N1 and N2 are sized in order to be in the weak inversion region.
Given that the circuit components are properly sized then referring to Fig. 3.8 the overall operation i.e. the generated current (i1) can be calculated as follows:

$$i_3 = \frac{1}{2}\beta_{n3}(V_{gn3} - V_{Tn})^2 \tag{3.7}$$

$$i_1 = n\beta_{n4}V_{sn1}(V_{gn3} - V_{Tn} - \frac{n}{2}V_{sn1}) \tag{3.8}$$

These equations have been obtained since it was assumed that transistor P3 is in saturation while transistor N4 is in triode and strong inversion. Since N1 and N2 are assumed to be in weak inversion, their source voltage is given by the following :

$$V_{sn1} = U_T \ln \frac{Z_{N1}Z_{P2}}{Z_{N2}Z_{P1}} \tag{3.9}$$

Where $U_T = KT/q$ is the thermal voltage and Z represents the $\frac{W}{L}$ ratio for the transistors. Looking at transistor P3 which copies current from transistor, P1 $V_{gn3} - V_{Tn}$ can be replaced by using the governing equation of P3, and the following is obtained:

$$\bar{i_1} = n\beta_{n4}V_{sn1}\left(\sqrt{\frac{2i_iS_{P3}}{\beta_{n3}S_{P1}}} - \frac{n}{2}V_{sn1}\right) \tag{3.10}$$

Taking the crossing point between $\bar{i_1}$ and i_1, two points can be identified, only one is non zero. Solving the equations above, the generated current equation is obtained:

$$i_1 = (n^2\beta_{n4})U_T^2K_{eff} \tag{3.11}$$

With K_{eff} given as follows :

$$K_{eff} = [K_2 - 0.5 + \sqrt{K_2(K_2 - 1)}] \ln {K_1}^2 \tag{3.12}$$

$$K_1 = \frac{Z_{N1}Z_{P2}}{Z_{N2}Z_{P1}} \qquad K_2 = \frac{Z_{N4}Z_{P3}}{Z_{N3}Z_{P1}} \tag{3.13}$$

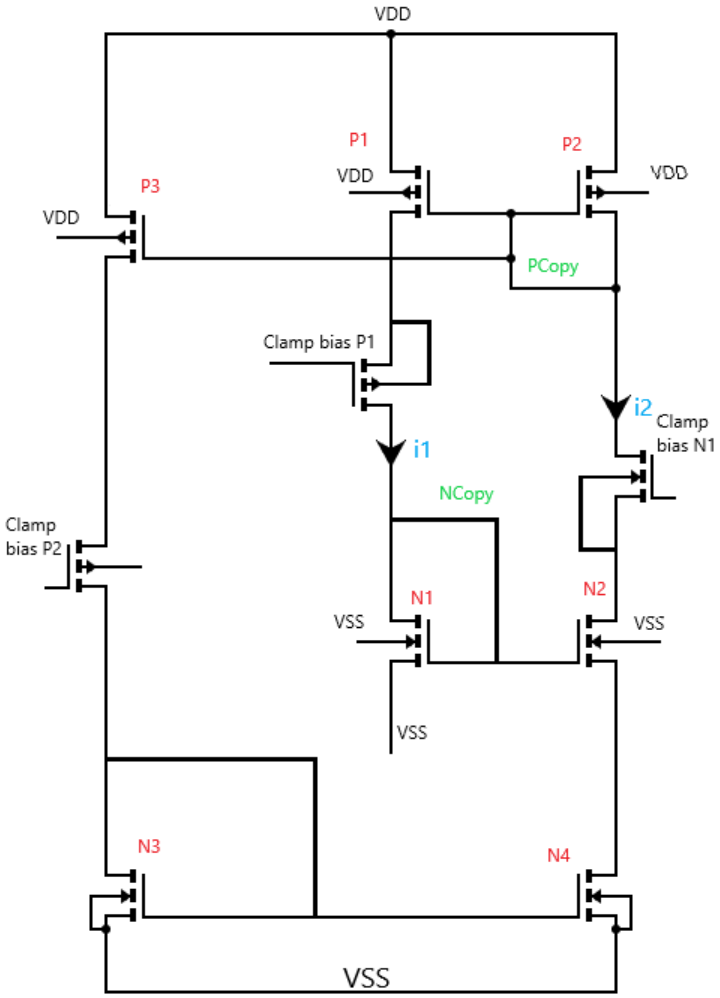


Figure 3.9: A simplified view of the implemented current reference (beta multiplier) with the over-voltage protection clamps.

As for transistor sizings (Referring to Fig. 3.9), several things have to be taken into account. The most important consideration is ensuring that transistors N2 and N1 are in weak inversion while transistors N3 and N4 are in strong inversion. Initially, the desired current to be generated is set to be $i1 = i2 = 2\mu A$, then the inversion coefficients (I_F) of the transistors are studied and the sizings are chosen in such a way to guarantee the proper operating region for each transistor. In fact

the inversion factor defined as

$$I_F = \frac{I_D}{I_S} = \frac{I_D}{2n\mu C_{OX}\frac{W}{L}U_T^2} \tag{3.14}$$

identifies the type of inversion undergoing in the transistor. For :

- $I_F < 0.1$ The transistor is in weak inversion.
- $0.1 < I_F < 10$ The transistor is in moderate inversion.
- $I_F > 10$ The transistor is in strong inversion.

Since not all technological parameters are given by the fab, an exact calculation is challenging to obtain. The only parameter that can be easily manipulated in the inversion factor equation was the $\frac{W}{L}$ ratio, therefore it was the main design variable used to size the transistors. Generally, the larger the W/L ratio the more the transistor goes into weak inversion and vice versa, this can be seen in the inversion factor equation. Setting the W/L ratios was the only degree of freedom used for the sizings. For the sake of completeness, transistors P2, P1, and P3 operate as a current mirror therefore they were sized in order to operate in the strong inversion region.

Transistor	**Sizing**	**W/L Ratio**
P1	W = $1\mu m$ * 8 L = $1\mu m$ * 8	1
P2	W = $1\mu m$ * 8 L = $1\mu m$ * 8	1
P3	W = $1\mu m$ * 10 L = $1\mu m$ * 5	2
N1	W = $2\mu m$ * 8 L = $1\mu m$ * 4	4
N2	W = $2\mu m$ * 32 L = $1\mu m$ * 4	16
N3	W = $1.25\mu m$ * 6 L = $1\mu m$ * 6	1.25
N4	W = $1.125\mu m$ * 6 L = $1\mu m$ * 6	1.125

Table 3.1: Transistor sizings in the Beta Multiplier. [Multiplication factors with widths correspond to the number of transistors connected in parallel with the same gate, source and drain (equivalent to the number of fingers). Multiplication factors with lengths correspond to the number of transistors connected in series, this is done to increase the effective length since the maximum value is $1\mu m$ in this technology. Several transistors connected in parallel can be seen as one device with an equivalent width equal to the sum of all individual widths. Several transistors connected in series can be seen as a single transistor with an equivalent length equal to the sum of all individual lengths.]

Although adopting this circuit topology has reduced the overall variability by removing the process dependent resistor, upon performing Monte Carlo simulations which introduce mismatch between transistors, a significant variability was still obtained as well. The main method to address this issue is to increase the total width and length of the transistors while maintaining the same $\frac{W}{L}$ ratio. Since in 28 nm

technology the maximum transistor length is $1\mu m$, several transistors have been connected in series while increasing the individual transistor width, thus effectively maintaining the same $\frac{W}{L}$ ratio.
In addition to that, instead of utilizing transistors with several fingers, transistors were connected in parallel in order to achieve the same effect as an increased number of fingers, in other words the number of fingers was made to be the number of transistors with the base width connected in parallel. In order to understand why this was done, one has to understand how the simulator views devices with several fingers. The outer fingers of an array of devices experience a different mechanical stress compared to the central devices, and therefore behave differently. The simulator accounts for that by changing the electrical parameters of the outer fingers compared to to inner ones. However, these stresses on outer fingers are usually avoided by placing dummy transistors in the layout phase that have no function other than absorbing these stresses so that they do not affect the operational transistors. Using this connection method, all transistor fingers are equivalent (according to the simulator) and the results are more accurate.
Going back to the the sizing table 3.1, N2 had a a larger W/L ratio compared to N1 (factor of four larger). This factor of four is arbitrary, but it should be noted that since the source of N2 is not connected to VSS as N1, but instead it is connected to a certain voltage while having the same gate voltage as N1, then its W/L ratio should be higher than that of N1 in order to be able to drive the same current. After setting all of the transistor values, according to simulation results the width of N4 was modified (i.e. W/L was modified) until a satisfactory current of $2\mu A$ was achieved. As a final remark, it is important to note that the copy branch transistors (branches with current setting transistors connected to the gate of the P or N side of the beta multiplier) should be equal in number and size to the transistors in the respective n or p side. In this case the P side contained a lot of transistors and after adding all the output copy branches, the circuit stopped working properly at startup due to the greatly increased capacitive load on the internal nodes of the beta multiplier structure. In order to mitigate this, the current was copied to 4*4 transistors (4 transistors in series, each consisting of 4 transistors in parallel) with $(W = L = 1\mu m)$. Although this is not ideal, maintaining the same overall W/L ratio, a quite accurate current is obtained. As for the N side, the copy branches contained transistors identical in width and size to N1 (since their sources were connected to VSS as N1).

3.2.3 The Startup Circuit

As mentioned before, both of the introduced circuits required some sort of current injection into one or more of their branches. This is due to the presence of several operating points for the circuit, and the need to force the circuit to operate in the correct one thus allowing it to produce the desired current. In order to satisfy these requirements, a startup circuit was designed and implemented as follows in Fig. 3.10.

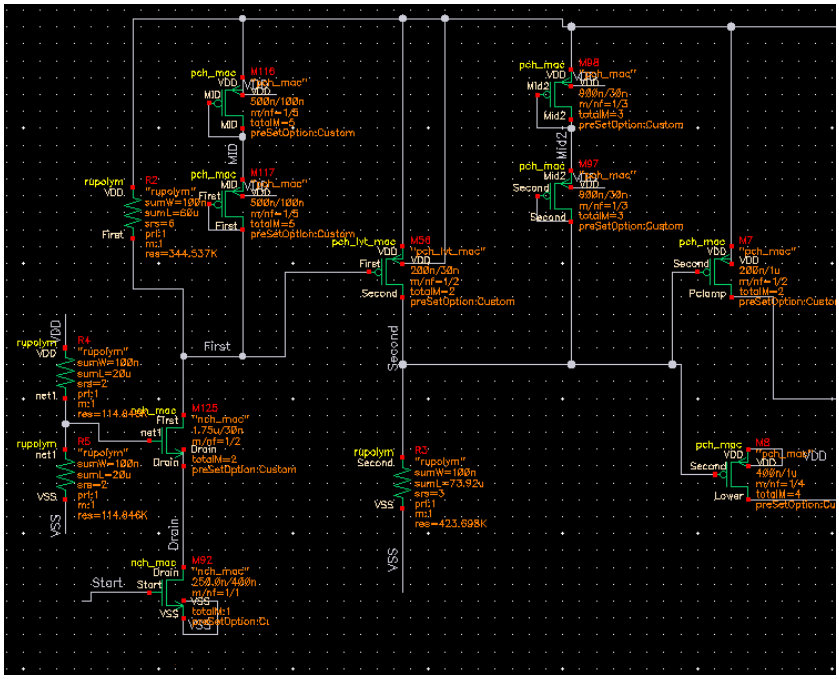


Figure 3.10: The Startup circuit.

Before diving into the startup operation, acknowledging the fact that VDD does not go immediately to its nominal value is very important in order to understand the operation of this circuit. The increasing ramp of VDD affects the whole circuit and all of its nodes. The *start* node in particular rises once some current has been established in the beta multiplier, so it is used as a signal to drive the initial branch current which allows the startup circuit to work.

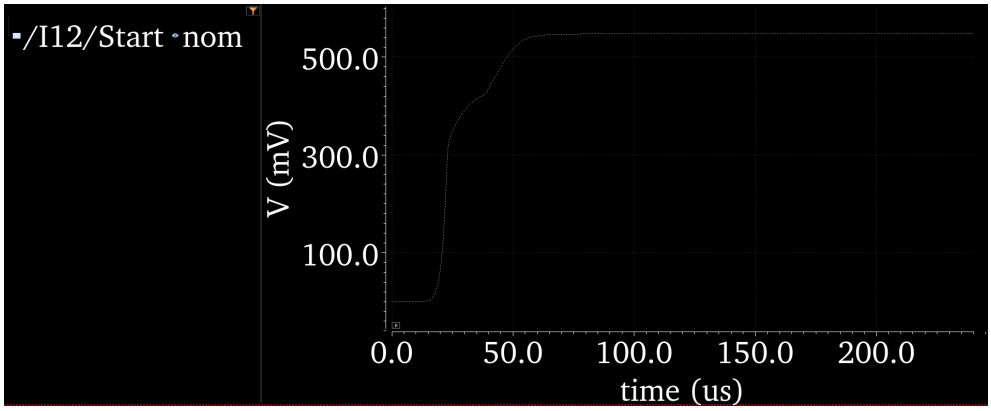


Figure 3.11: The Start signal.

The order of events that lead to a time limited current injection is explained below and is referenced to Fig. 3.10:

- **FIRST : Initially FIRST rises with VDD as no current flows in the branch yet, but when the Start signal reaches a sufficiently high**

value to turn on M92(transistor whose gate is connected to Start) current starts to flow in the branch and therefore First node voltage drops to a level that will create a sufficient VSG on transistor M56 whose gate is connected to FIRST, thus turning it on and allowing it to conduct.

- **SECOND: Initially Second remains zero since no current is flowing in the branch, and as VDD rises transistors M7 and M8 activate due to a sufficient VSG and therefore, inject current into two branches of the circuit in order to jump start it (see Fig. 3.3 for the injection locations). Meanwhile, as transistor M56 is activated by First dropping in potential, current flows through M56 and therefore pulls node Second up to VDD thus turning off both transistors M7 and M8. This has been designed to occur after they have injected a significant current, thus achieving the desired effect of forcing the circuit into the correct operating point.**

Transistor	**Sizing**	**Flavor**
M92	W = $0.25\mu m$ L = $0.4\mu m$	Standard
M56	W = $0.2\mu m$ L = $0.03\mu m$	Low VT (LVT)
M7	W = $0.2\mu m$ L = $1\mu m$	Standard
M8	W = $0.4\mu m$ L = $1\mu m$	Standard

Table 3.2: Transistor sizings in the Beta Multiplier Startup circuit referring to Fig. 3.11. Protection clamps sizings are not reported as they do not affect normal operation.

Startup transistor sizings and flavors were chosen according to simulation results. Transistor M8 has two times the driving capability of transistor M7 due to the fact that the branch it is injecting current into has double the current found in the branch being injected by M7, however the choice remains arbitrary as long as sufficient current is injected in the reference branch to start it up.

3.3 Simulation Results & Discussion

In this section, simulation results regarding the circuit will be presented and a short discussion/elaboration will follow. It is important to note that all simulations in this section have been conducted for VDD equal 1 and 1.8 Volts at a temperature of -30, 27 and finally 80 °C. Two types of simulations have been conducted, the first being across all process corners (along with temperature and voltage, PVT) and the second being a Monte Carlo simulation which introduced mismatch and process corners at the various temperatures and voltages mentioned before.

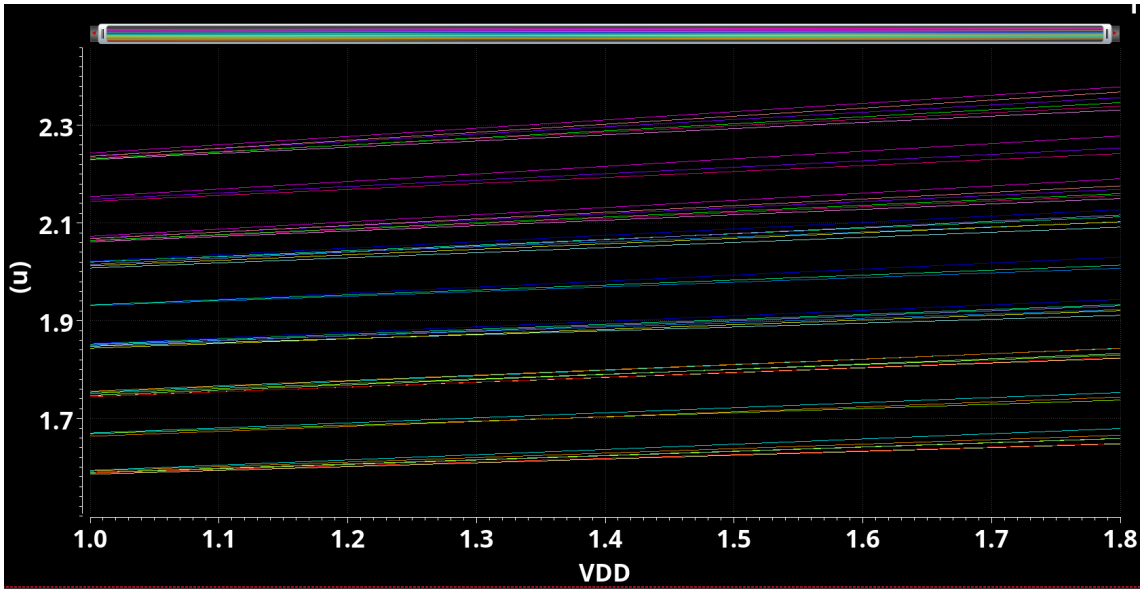


Figure 3.12: Generated current across all process corners, temperatures and voltages.

As shown in Figure 3.12, the current varies by around 20 % from it's nominal value of 2μA with PVT corners. This is an acceptable variation as it still falls in the specifications of the circuit.

Yield Estimate: 75.5 %(151 passed/200 pts) | Parameters: T=-30,VDD=1							
KK_StackedTank28_KK_Beta_Mult_TB_2							
Branch Curre...	83% (166/200)	1.349u	2.097u	1.676u	177.6n	0.331	0
Copy Branch c...	84.5% (169/200)	1.322u	2.189u	1.678u	161.3n	0.368	0
Branch Curre...	87% (174/200)	1.24u	2.151u	1.689u	173.7n	0.363	0
Copy Branch c...	88% (176/200)	1.33u	2.191u	1.692u	154.8n	0.414	0
Yield Estimate: 85 %(170 passed/200 pts) | Parameters: T=-30,VDD=1.8							
KK_StackedTank28_KK_Beta_Mult_TB_2							
Branch Curre...	91% (182/200)	1.418u	2.178u	1.754u	183.8n	0.46	0
Copy Branch c...	94% (188/200)	1.39u	2.294u	1.759u	166.8n	0.518	0
Branch Curre...	91% (182/200)	1.301u	2.23u	1.764u	179.5n	0.49	0
Copy Branch c...	97% (194/200)	1.396u	2.292u	1.772u	160n	0.567	0
Yield Estimate: 100 %(200 passed/200 pts) | Parameters: T=27,VDD=1							
KK_StackedTank28_KK_Beta_Mult_TB_2							
Branch Curre...	100% (200/200)	1.616u	2.329u	1.939u	170.5n	0.858	0
Copy Branch c...	100% (200/200)	1.594u	2.424u	1.941u	154.3n	0.954	0
Branch Curre...	100% (200/200)	1.508u	2.379u	1.953u	166.2n	0.908	0
Copy Branch c...	100% (200/200)	1.605u	2.43u	1.959u	148.4n	1.03	0
Yield Estimate: 99.5 %(199 passed/200 pts) | Parameters: T=27,VDD=1.8							
KK_StackedTank28_KK_Beta_Mult_TB_2							
Branch Curre...	100% (200/200)	1.697u	2.415u	2.021u	175.6n	0.909	0
Copy Branch c...	99.5% (199/200)	1.665u	2.526u	2.027u	158.7n	0.993	0
Branch Curre...	100% (200/200)	1.581u	2.461u	2.033u	171.2n	0.91	0
Copy Branch c...	99.5% (199/200)	1.675u	2.53u	2.044u	152.6n	0.995	0
Yield Estimate: 98.5 %(197 passed/200 pts) | Parameters: T=80,VDD=1							
KK_StackedTank28_KK_Beta_Mult_TB_2							
Branch Curre...	99% (198/200)	1.85u	2.53u	2.154u	160.2n	0.72	0
Copy Branch c...	99.5% (199/200)	1.83u	2.597u	2.157u	143.3n	0.797	0
Branch Curre...	99% (198/200)	1.744u	2.552u	2.169u	155.7n	0.709	0
Copy Branch c...	99.5% (199/200)	1.844u	2.607u	2.179u	138.1n	0.776	0
Yield Estimate: 85.5 %(171 passed/200 pts) | Parameters: T=80,VDD=1.8							
KK_StackedTank28_KK_Beta_Mult_TB_2							
Branch Curre...	91% (182/200)	1.946u	2.649u	2.262u	165.6n	0.48	0
Copy Branch c...	95% (190/200)	1.932u	2.723u	2.268u	148n	0.522	0
Branch Curre...	92% (184/200)	1.832u	2.663u	2.274u	161.3n	0.468	0
Copy Branch c...	94.5% (189/200)	1.945u	2.731u	2.289u	142.4n	0.494	0

Figure 3.13: Monte Carlo simulation summary across all temperature and voltage corners along with the introduction of mismatches between transistors. Columns from left to right refer to : Current Name, % Yield (referred to an arbitrary current range of $1.5\mu A \rightarrow 2.5\mu A$), minimum value, maximum value, mean value, standard deviation, process capability index (Cpk), and the number of simulation errors.

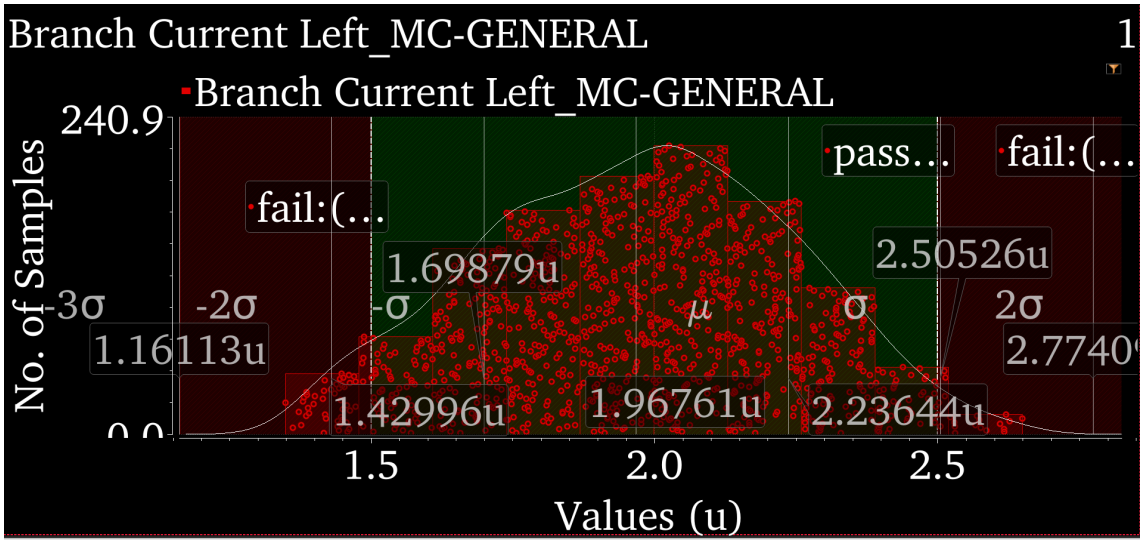


Figure 3.14: Monte Carlo simulation histogram across all process corners, temperatures and voltages along with the introduction of mismatches between transistors.

The reader might be intrigued as to why some Monte Carlo simulations appear to have failed, in fact the simulations have succeeded but they did not conform to the initial specifications of $1.5\mu A \rightarrow 2.5\mu A$. After performing hundreds of simulations it has been concluded that a technology limitation has been reached. As a consequence, in order to satisfy the initial requirements, the circuit area explodes to a very large value (to mitigate mismatch effects), therefore this is not an effective solution. Nevertheless, extreme cases in current variations are presented at two or three standard deviations from the mean (see Fig. 3.14). This corresponds to a 5% to 0.3% occurrence probability which is quite low and indicates a very rare possibility of this extreme case to be present on a fabricated chip. However, after testing the current reference along with the linear regulator (the main block it has to supply) it has been observed that the performance is very good and the variability range of the output voltage of the linear regulator is acceptable.

3.4 Single Event Testing & Reasoning

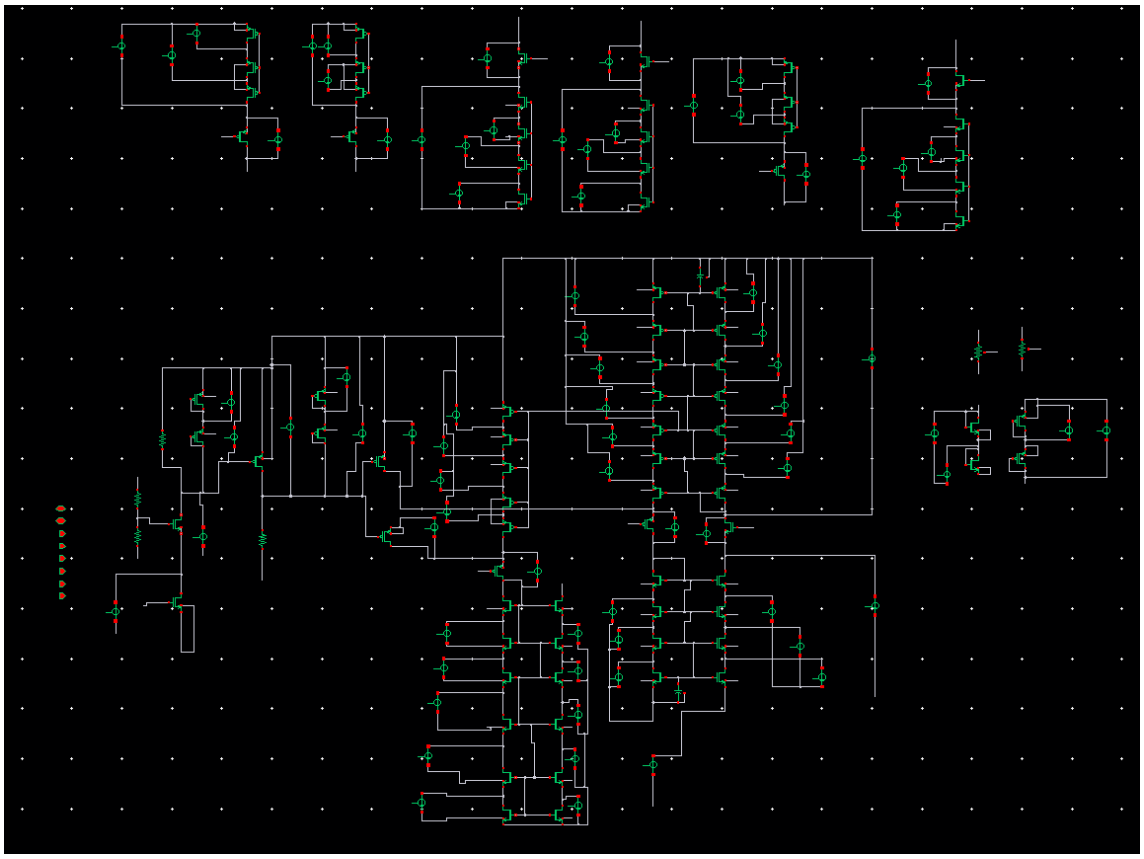


Figure 3.15: The modified circuit for single event testing.

The current sources modeling SEs (in Fig. 6.12) supply a **4 mA current amplitude with a 50 ps rise time and 150ps fall time** (corresponding to the worst case LET in the application 40 $\frac{MeV \cdot cm^2}{mg}$) to either charge or discharge a sensitive node of a Pmos or Nmos respectively.
After performing SE tests, over voltages appeared all over the circuit, but they were not critical due to two things.

- **1 : The time duration where the over voltages occur are in the order of a hundred pico seconds therefore long term transistor damage is very unlikely**
- **2: The modeled case is the absolute worse, where a very energetic particle impinges the circuit, and this event is very rare**

In addition to testing the isolated beta multiplier, it was also connected to the linear regulator and tested for the issues that might propagate to the voltage generated by

the linear regulator. In fact the output voltage of the regulator slightly exceeded 1V (nominal value is around 0.9V), even if this was acceptable for a short duration of time, a 2pF capacitor was placed between VDD and PCopy, and another between VSS and NCopy. By doing so, the voltage variation was allowed to be slightly reduced by making the SE generated over voltage marginally better.
It is important to note that studying SE effects at the block level does not show the full extent of issues that can arise. Therefore, a system level simulation is crucial to observe SEE propagation from the initial block to the system output. This is done for the control loop which utilizes the 0.9V version (introduced in 3.6) of this current reference.

3.5 Brief Comment

The current produced by the reference (beta multiplier) increases with temperature according to simulation results. This current is fed into a diode connected transistor in the linear regulator in order to generate a stable voltage (which is used as a reference voltage to determine the output of the regulator), but as temperature increases, the threshold voltage of the transistor decreases. Therefore, the voltage obtained by this method decreases, but since the current coming from the reference increases with temperature, then this effect mitigates the decrease in threshold and increases the drain voltage of the diode connected transistor in the linear regulator, thus making it behave better with temperature variations.

3.6 The 0.9V Version of the Current Reference

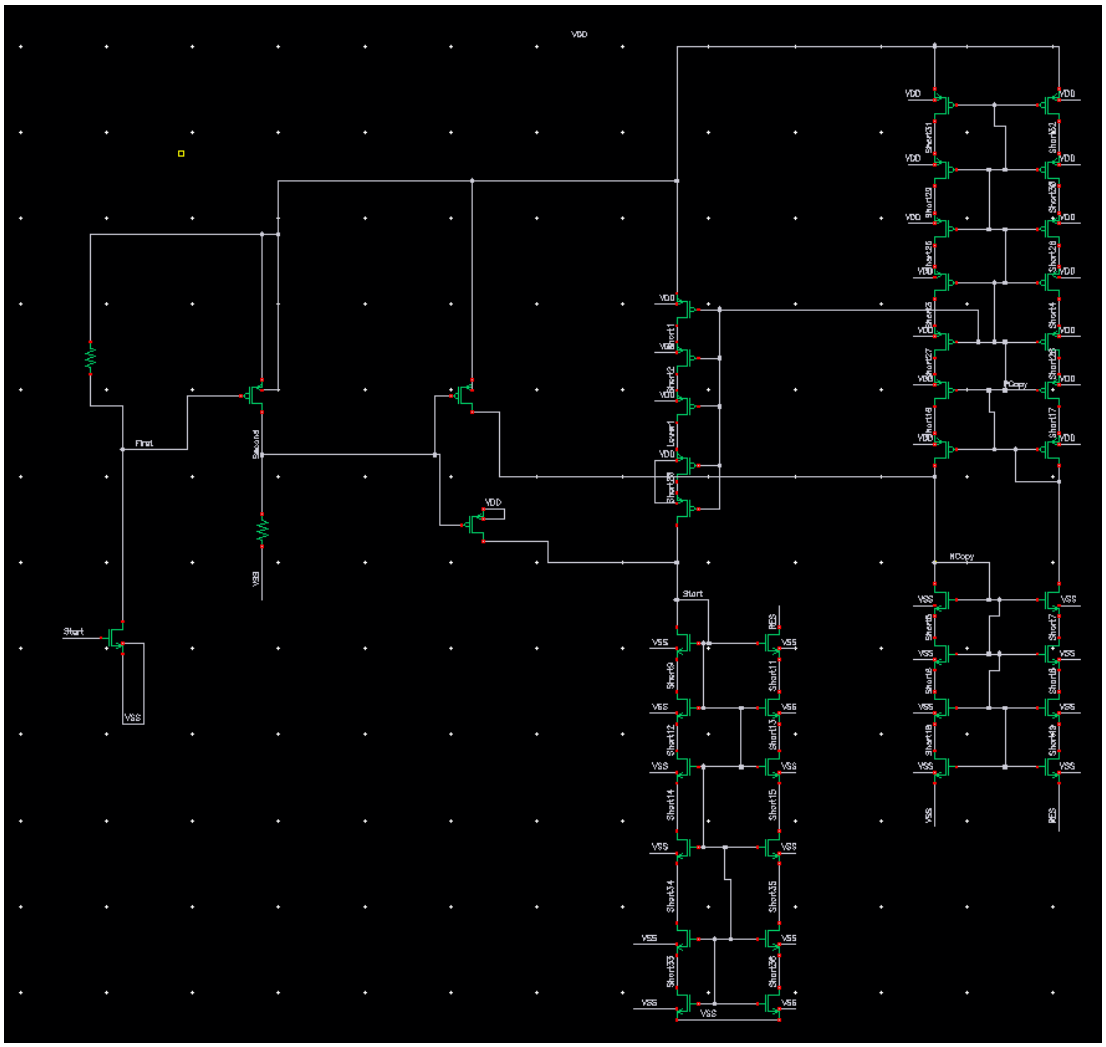


Figure 3.16: The simplified circuit.

Due to the need of a current reference that would work in the nominal voltage domain of a 0.9 V difference between VDD and VSS, the original circuit was simplified. This simplification came in the form of removing all the over-voltage protections which consisted of driven and undriven clamps along with the branches generating the voltages for the driven clamps, as over voltages would never happen at this nominal voltage during operation. The simplified circuit can be found in Fig. 4.5. A system level (control loop) SE testing will be conducted for this 0.9V current reference in Chapter 6.

Chapter 4

The Error Amplifier

4.1 Introduction & Circuit Overview

In the DC-DC converter under design, the on time (Ton) of the power switches (Mosfets) sets the conversion function. In order to maintain a stable output voltage regardless of variations in the input voltage or output load, some sort of control system is needed.

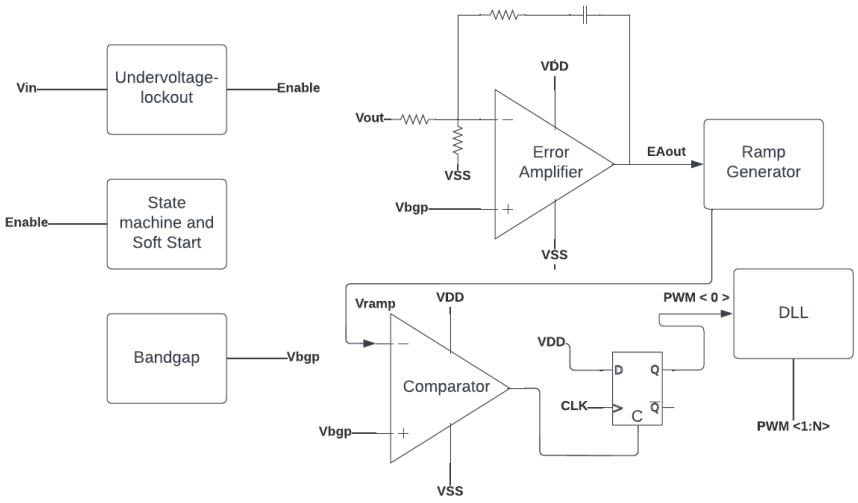


Figure 4.1: A block diagram of some required circuits for the converter

As shown in Fig. 4.1, this control circuit is composed of several blocks. This chapter will consider arguably one of the most important blocks, the error amplifier. The reference voltage that is fed into this amplifier is a temperature invariant voltage generated by a bandgap reference. Additionally, an enable signal is used along with its inverted version to switch the amplifier from operating mode to idle and vice versa. An external current is needed in order to properly bias the amplifier. The

previously discussed beta multiplier is used to provide a current of 2uA into the amplifier. This current is later used to design a biasing network which properly biases the whole amplifier.

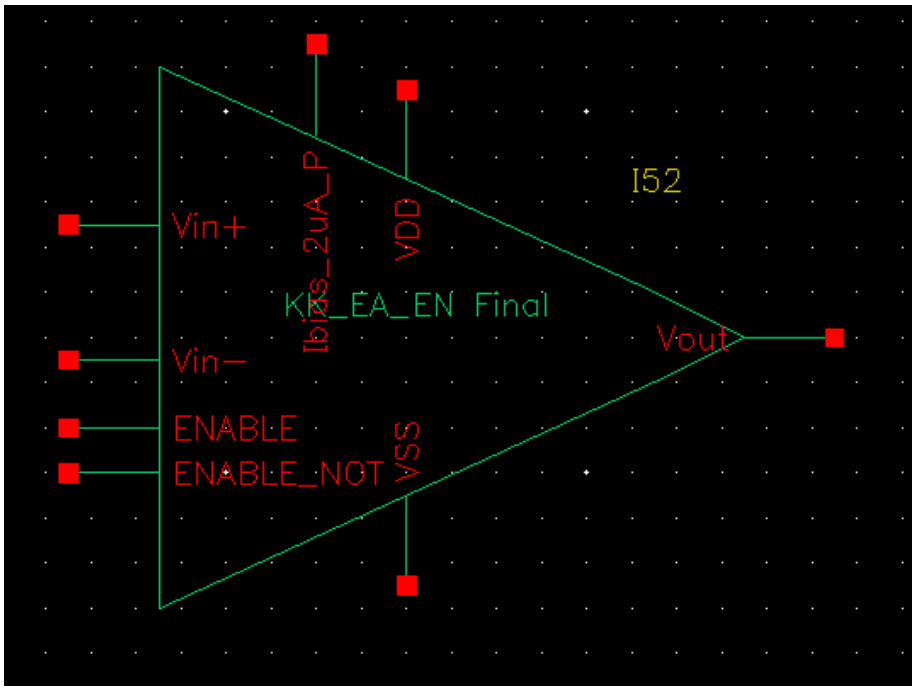


Figure 4.2: The amplifier symbol which includes all input/output pins

The error amplifier has to sense the output voltage and generate a control signal which feeds into the Ton generator and sets the output voltage to the required/desired value. In particular, the amplifier is used to generate the PI (Proportion-Integral) compensation filter that is needed to set the dynamic performance of the DC-DC converter control loop and to guarantee a high DC gain and the stability of the system. For this application, an amplifier with a GBW that is significantly larger than the bandwidth of the control loop of the converter (which is 20MHz) is needed. In addition, a high DC gain is required to ensure a high DC gain of the full control loop, while any offset is reflected by an inaccuracy in the output voltage. These considerations drive the definition of the specifications, which are GBW = 200MHz , DC Gain = 80dB, standard deviation < 1 mV for the input offset.

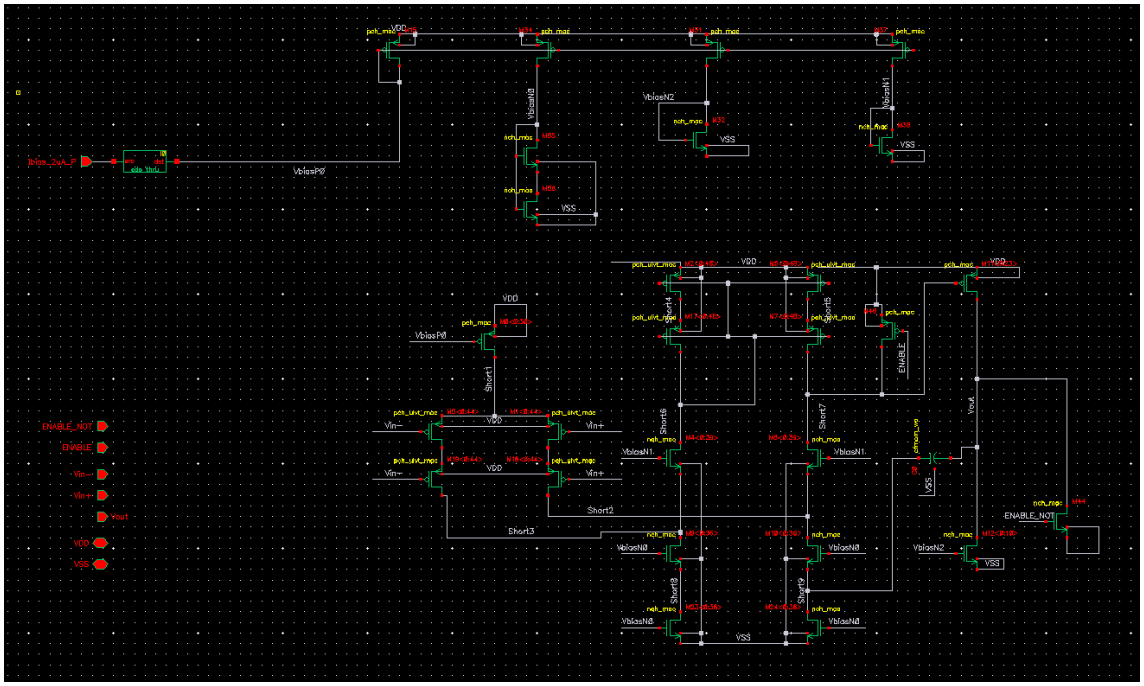


Figure 4.3: The complete Error Amplifier circuit implementation

In order to meet specifications and achieve proper operation, a folded cascode OTA topology was implemented [6]. This topology allows for a drastically improved dynamic output range over a conventional OTA and makes it easier to introduce an N and P cascode which increase the output resistance and therefore the gain. Usually, the addition of a cascode in a regular operational amplifier is possible but since the supply voltage is only 0.9 volts, it is very difficult to keep all the transistors in the saturation operating region. This issue is made less severe in the case of the folded cascode topology, since the differential pair are removed from the main branches. In addition, a second common source stage was added in order to further increase the gain. The necessity to add a second stage implies the addition of a second pole to the circuit. This non-dominant pole can cause the circuit to be unstable, and consequently a compensation capacitor was added in between the output and the N-cascode. This connection splits the two poles using the Miller effect, which moves the dominant pole to lower frequencies, while the non dominant pole is pushed towards higher frequencies. Therefore at the GBW frequency i.e. the frequency where the gain is unity, the phase is significantly above than -180°(assuming the circuit starts at a phase of 0°).

All of the mentioned points will be individually discussed and elaborated upon in the following sections.

4.2 The Design Approach

Before diving deep into this section, it is important to properly define the two terms, Gain Bandwidth Product (GBW) and Phase Margin (PM). The PM, represents the difference between the phase at unity gain and the phase which makes the feedback become positive (usually -180°assuming a start from 0°), while as the GBW is the frequency where the gain is unity as mentioned above. In Fig. 4.4 below, the PM can be visualized at the GBW frequency, a start from 0°phase with a gain of around 90dB is taken.

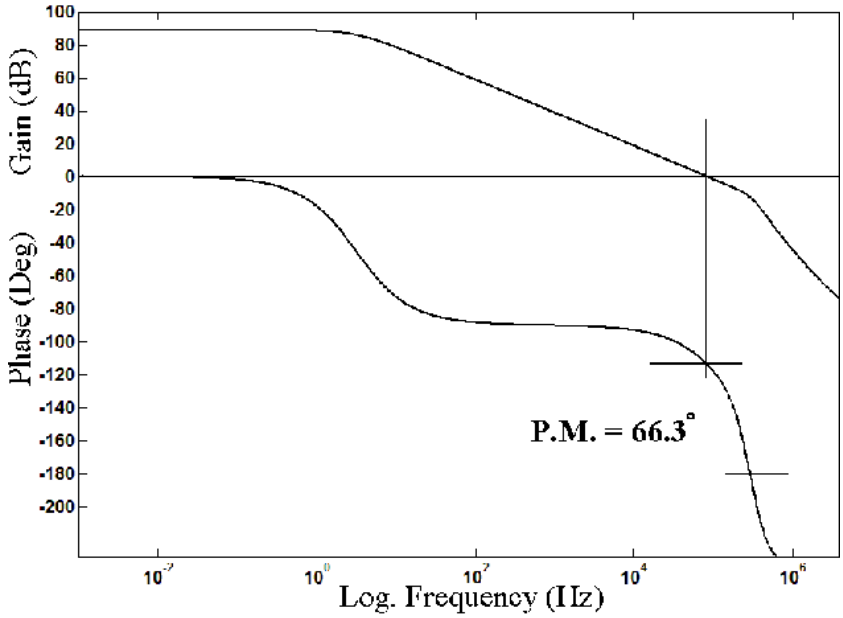


Figure 4.4: A visualization of the PM and GBW. [8]

4.2.1 Preliminary Design

The amplifier under study is a two stage amplifier, which implies the necessity of some sort of compensation network for stability reasons. In fact, after performing a circuit analysis, it can be proved that the values of gm2 and gm7 (trans-conductance of the differential pair and 2nd stage common source respectively) are the most important along with the value of the compensation capacitor Cc and node capacitance Cn1 to define the pole frequencies. These values and stages are represented in the simplified circuit schematic in Fig. 4.5.

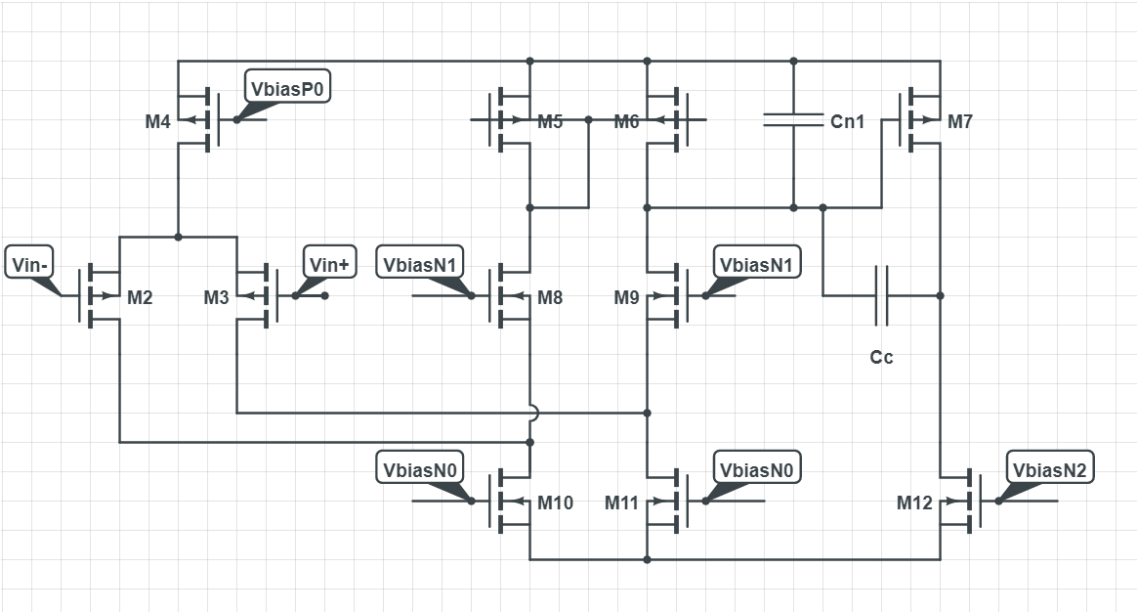


Figure 4.5: The initial two stage folded cascode circuit schematic.

The preliminary design was done through a script utilizing Murmann's approach to obtain the technology parameters. For starters, the non-dominant pole frequency was chosen to be three times the GBW in order to have a sufficient phase margin. In addition to that, the value of the compensation capacitance Cc was chosen to be 3 times the node capacitance Cn1. Cn1 is the node capacitance, but as an approximation its value can be considered to be that of the gate capacitance of transistor M7.
It can be shown that for a generic 2-stage op-amp, the following is true (referring to Fig. 4.5, noting that M2 and M3 are identical transistors):

$$F_{nondom} = \frac{g_{m7}}{2\pi C_L} \frac{1}{1 + \frac{C_{n1}}{C_c}} \tag{4.1}$$

$$gm_2 = 2\pi GBW \cdot C_c \tag{4.2}$$

Where C_L is the load capacitance that is being driven by the amplifier, and C_C is the compensation capacitor. As mentioned before, the non dominant pole frequency is set to be three times the frequency of the dominant pole due to stability requirements. In addition, the correction term $\frac{C_{n1}}{C_c}$ is set to be around 1/3. After setting these values, the trans-conductance of the differential pair transistors along with the second stage transistor (M7) are obtained.
After obtaining the numeric solutions for $gm2$ and $gm7$ from the above equations, the values are plugged into a script and other transistor parameters are outputted (using the method by Boris Murmann). Obtaining these values, the designer is then mainly tasked to choose the proper length of the transistors that determine the output resistance of each stage. The length values are integral for meeting the gain specification as the gain of each stage is proportional to the transconductance

of the input devices multiplied by the output node resistance of the stage. The L of the differential pair can be kept relatively low, as the differential pair does not contribute to the output resistance in a folded cascode topology.

The Matlab script developed by Boris Murmann from Stanford University[9] utilizes lookup tables consisting of tens of automatically performed simulations that contain DC operating points for P and N channel devices. Such lookup tables include the parameters of the devices (e.g. threshold voltage, gm, output resistance, ...) for various VDS, W , L and VGS values. These tables capture the variations of these parameters with the transistor size (e.g. they already include the decrease in threshold voltage due to the short channel effect) and allow a one-step accurate calculation of the needed sizing to obtain the desired gm or output resistance. After calculating $gm2$ and $gm7$ using the above equations, the user can set several design parameters such as the gm/ID (useful to guarantee that the differential pair in moderate inversion and the current mirrors in strong inversion) and the transistor length, and utilize the script to obtain the remaining transistor parameters (namely bias currents and W). This method presents a faster way to reach an initial solution of the circuit. However, circuit manipulations are still needed as the script does not encompass the gain requirement of the circuit along with all the parasitics and effects that can take place. Therefore, tweaking the circuit parameters according to simulation iterations is unavoidable.
The design procedure for obtaining transistor parameter values is listed below :

1. Calculating $gm2$ and $gm7$ from the above equations

2. Setting a reasonable value for the length of transistor M7 along with a gm/I_D factor (a higher value corresponds to the transistor operating in the weak inversion region, this value is relatively high so the transistor can be seen as operating in the weak inversion region) allows us to obtain the drain current though the following : $I_{D7} = \frac{gm_7}{\frac{gm_7}{I_{D7}}}$

3. Utilizing the lookup tables (provided by Boris Murmann's lookup table generation script) the value of I_{D7}/W_7 can be obtained and therefore the width of that transistor can be concluded.

4. Providing the DC operating point along with the length of transistor M7, the lookup table is used to obtain the gate capacitance of M7 which is approximated to be Cn1. Then the compensation capacitor is taken to be three times the value of the obtained Cn1.

5. Moving on to the differential pair, a similar approach is followed. The transistor length is set along with the gm/I_D factor (set to 14 i.e. weak inversion). The drain current is obtained through $I_{D2,3} = \frac{gm_{2,3}}{\frac{gm_{2,3}}{I_{D2,3}}}$

6. Computing the width of the differential pair through $I_{D2,3}/W_{2,3}$ which is obtained through the lookup table.

7. Tweaking the cascode transistor lengths (also M7 and M12) to meet gain requirements, along with increased the total area of transistors in order to meet input offset requirements. This tweaking can lead to a deviation from the original sizing values.

The gain of the amplifier mainly depends on the resistance observed at the outputs of each stage, for example the first stage's resistance is the parallel of the drain of M9 and the drain of M6, while as in the second stage it is the parallel of the drain resistances of M7 and M12. It is important to note that increasing the length of transistor M7 degrades g_{m7} as it is proportional to W/L and the drain current, this necessitates an increase in the branch current. In order to keep power consumption at a reasonable value, instead of extensively increasing the length of M7, the cascode transistor lengths are increased.

In this work, the script was utilized to reach initial sizing values then an iterative simulation approach was adopted to reach the final solution.

Before presenting the transistor sizes, the reader should note that the implemented compensation capacitor connection was modified from what can be seen from the general two stage folded cascode topology (Fig. 4.5) to what is presented in Fig. 4.3. The reasoning behind this will be introduced in section 4.2.3. Simulation iterations were used after this change to guarantee that the amplifier meets the specifications.

Transistor	**Sizing**	**Flavor**
M4	W = $1\mu m$*31 L = $1\mu m$	Standard
M2,M3	W = $2\mu m$*45 L = $0.1\mu m$	Ultra Low VT (ULVT)
M5,M6	W = $2.835\mu m$ * 49 L = $1\mu m$*2	Ultra Low VT (ULVT)
M8,M9	W = $1\mu m$*40 L = $0.1\mu m$	Standard
M10,M11	W = $1\mu m$*37 L = $1\mu m$*2	Standard
M7	W = $2\mu m$*24 L = $0.4\mu m$	Standard
M12	W = $2\mu m$*11 L = $0.3\mu m$*2	Standard

Table 4.1: The final transistor sizings referring to FIG 4.5. The general transistor placement remains the same, even if the compensation capacitance connection is modified

The ULVT flavor was used for transistors M2 and M3 in order to increase their transconductance, while as it was used for transistors M5 and M6 in order to have a voltage at their sources which is sufficient to place all of the transistors below in saturation.

4.2.2 Biasing Network

As observed in Fig. 4.5 and 4.3, the amplifier needs several biasing voltages in order to operate properly. As mentioned previously, a $2\mu A$ current is used to generate all

the bias voltages. In fact, this current is fed into a biasing network that generates the proper voltages that are used to obtain a wide range of currents throughout the circuit. Though obvious to an analog designer, it is important to note that using different widths and lengths while maintaining the same $\frac{W}{L}$ ratio between a biasing and copying transistor does not lead to an accurate copied current. That is due to the transistor model changing, and among the changed parameters is the threshold voltage that greatly impacts the copied current. The transistor length plays a greater role in this parameter change compared to the transistor width which has a lesser effect on these models. It is a good practice to use the exact same values of transistor widths and lengths in the current mirror branches.

On the other hand, large values of currents were needed compared to the input current of $2\mu A$. Therefore in order to avoid having a large number of transistor fingers, the multiplication of the current was split between generating and copying branches instead of keeping it all in the copying branch. In this case, a current of $100\mu A$ was needed in the second stage of the amplifier, which translates to 50 times the width (50 times the fingers) of the generating transistor (with a drain current of $2\mu A$). This leads to a complicated layout, therefore a better approach is to generate a $10\mu A$ current in the biasing branch (5 times larger than the initial transistor with $2\mu A$) and copy it to a transistor which is only 10 times larger than the generating transistor, thus saving tens of transistor fingers.

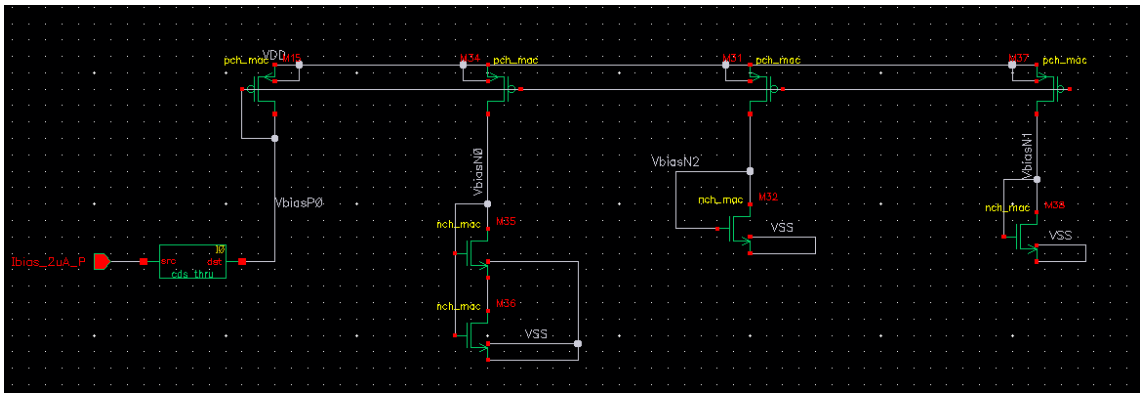


Figure 4.6: The Bias Network.

Finally, it is worth mentioning that transistors with more than 1 finger are represented by single finger transistors connected in parallel. This produces a more accurate model, and a more realistic Monte Carlo mismatch simulation (See 3.2.2).

Transistor	**Sizing**
M15	W = $1\mu m$ L = $1\mu m$
M34	W = $1\mu m$ L = $1\mu m$
M31	W = $1\mu m$ * 5 L = $1\mu m$
M37	W = $1\mu m$ L = $1\mu m$
M35/M36	W = $1\mu m$ L = $1\mu m$*2
M32	W = $2\mu m$ L = $0.3\mu m$
M12	W = $0.15\mu m$ L = $1\mu m$

Table 4.2: Transistor sizings (Referring to Fig. 4.6) for the biasing network. Transistors M35 and M36 are considered to be a single transistor with double the individual length. This transistor is named M35/M36 in the table.

4.2.3 Modifications and Trade offs

As mentioned in section 4.2.1, the preliminary design which was reached a Matlab script that utilizes a lookup table is insufficient to meet specifications, specifically in terms of gain and mismatch. Therefore, some modifications have been made in terms of transistor length and compensation feedback node. Initially, an N and P cascode were utilized in order to boost the gain significantly, but that became an issue since saturation was difficult to achieve for all transistors due to the low supply voltage (VDD =0.9V). To that effect, one of the P-side cascode levels was removed. In order to compensate for a decreased gain, the output resistance of the first stage had to be boosted, so the transistor lengths were drastically increased to 2um, which can be achieved by placing two transistors in series as the maximum length provided by the 28nm technology is 1um.
Based on simulation results, increasing the length of the transistors had an effect on the frequency behaviour of the amplifier. In fact, this introduced an additional pole at low frequency, thus causing the system to turn into a positive feedback network i.e. an unstable system below the required GBW of 200 MHz. A very good solution to this issue was discovered, it consisted of connecting the compensation capacitor feedback in between the bottom N-cascode rather than the way it was shown in Fig. 4.5. One can see transistor M11 (referring to Fig. 4.5) to consist of 2 transistors in series (due to the length limitation discussed before) and the compensation capacitor to be connected in between the two series transistors that form M11. This can be observed in Fig. 4.3.

4.2.4 Amplifier Enable

Another feature of the amplifier is the possibility to switch it from operation to idle mode using an input enable signal accompanied by its inverted version. The amplifier is to operate normally when the enable signal is 1 and it should be idle when enable is 0. In other words, the output voltage is pulled to zero when enable is 0. This is achieved by adding two transistors, the first being a pmos that pulls the output of the first stage to VDD thus cutting off the second stage common source amplifier. The second transistor being an Nmos connected to the output of the second stage (output of the whole amplifier) that pulls it to zero when enable is zero. The added transistors can be seen bordered by red squares in Fig. 4.7 below.

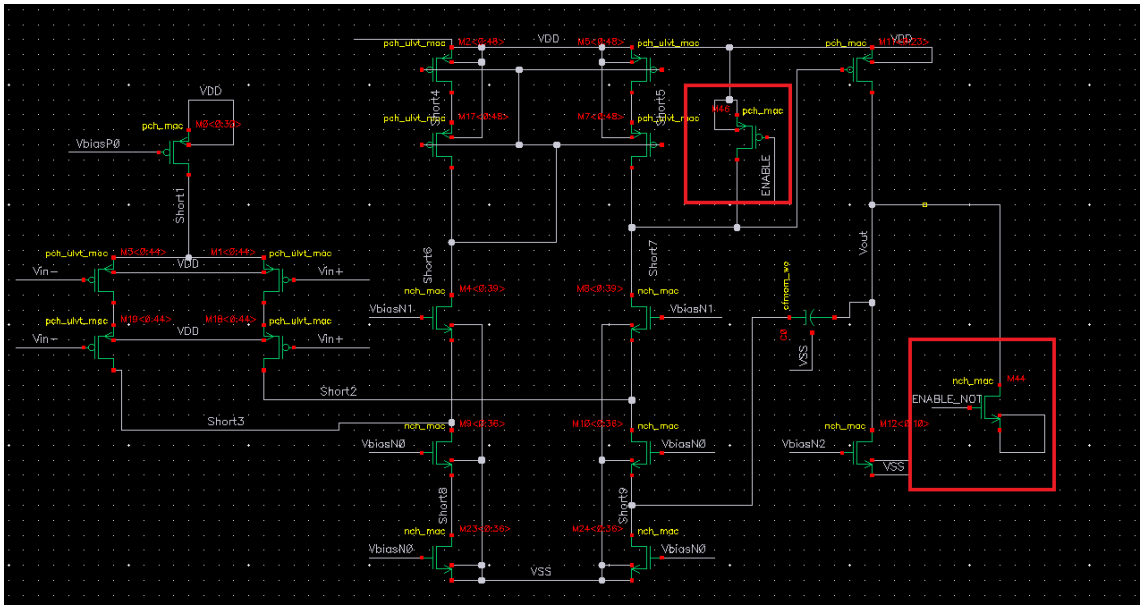


Figure 4.7: The added transistors.

4.3 Simulation Results

In this section, simulation results will be presented concerning the complete and finalized circuit.

4.3.1 Phase Margin and Gain Bandwidth

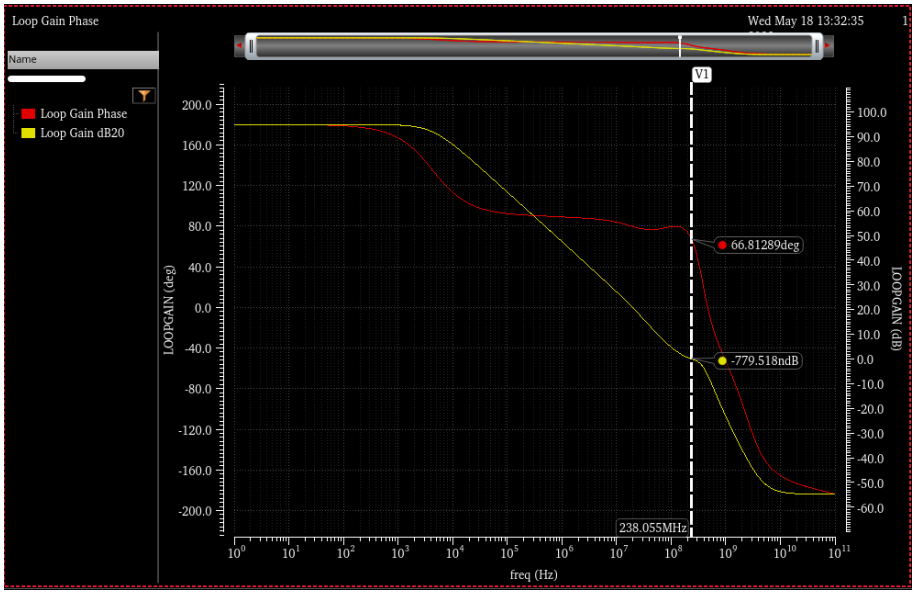


Figure 4.8: The frequency behaviour of the amplifier.

As observed in Fig. 4.8 above, the circuit exhibits a **Phase Margin = 66.82°** along with a **Gain Bandwidth Product (GBW) = 238 MHz** and **DC Gain = 94.915dB**. All of the mentioned values meet specifications, and stability requirements.
The reader is encouraged to observe the increase in phase around the Gain bandwidth frequency. Generally, a standard feedback connection for the compensation capacitor leads to a right half plane zero (a positive zero) which degrades the phase margin and therefore, the stability of the circuit. There exist several solutions to this problem, but what is used here is connecting the compensation capacitor in between the N cascode (see Fig. 4.3). One can see that as introducing a large resistance between the the feedback node and the output of the first stage due to the presence of two transistors in between them. In this effect, the positive zero becomes a negative zero and instead of degrading the phase margin it ends up improving it. The effect of this zero is shown at the GBW frequency where a phase "bump" can be seen.
Another comment worth mentioning is that the compensation capacitor is connected to a node that has a good PSRR (Power Supply Rejection Ratio). This improves the PSRR of the output of the error amplifier at high frequencies.

4.3.2 Mismatch and Variability (PVT & Monte Carlo)

Three different 500 point Monte Carlo simulations were performed across different temperatures [-30,27,80]°C. Mismatch and process corners were taken into account. Since the amplifier was placed in a voltage follower topology, the input offset was

measured as the difference between the fixed input of the amplifier and the output voltage which is connected to the other input. The summary and the histograms of these simulations can be found below in Fig. 4.9 and 4.10

Yield Estimate: 73.2 %(366 passed/500 pts) | Parameters: T=-30								
DC_Test								
(VDC("/VDC") - VDC("/Vout"))(summary)	100% (500/500)	-2.66m		1.911m	8.808u	715.5u		0
(VDC("/VDC") - VDC("/Vout"))_MC-GENERAL	100% (500/500)	-2.66m	info	1.911m	8.808u	715.5u		0
KK_StackedTank28_KK_EA_TB_1								
Phase Margin(summary)	82.6% (413/500)	48.15		80.33	66.35	6.256	0.338	0
Phase Margin_MC-GENERAL	82.6% (413/500)	48.15	> 60	80.33	66.35	6.256	0.338	0
Phase Margin Frequency(summary)	90.6% (453/500)	156.8M		343.2M	238M	31.01M	0.408	0
Phase Margin Frequency_MC-GENERAL	90.6% (453/500)	156.8M	> 200M	343.2M	238M	31.01M	0.408	0
Yield Estimate: 73.2 %(366 passed/500 pts) | Parameters: T=27								
DC_Test								
(VDC("/VDC") - VDC("/Vout"))(summary)	100% (500/500)	-2.586m		1.951m	14.93u	708.1u		0
(VDC("/VDC") - VDC("/Vout"))_MC-GENERAL	100% (500/500)	-2.586m	info	1.951m	14.93u	708.1u		0
KK_StackedTank28_KK_EA_TB_1								
Phase Margin(summary)	82.6% (413/500)	48.15		80.33	66.35	6.256	0.338	0
Phase Margin_MC-GENERAL	82.6% (413/500)	48.15	> 60	80.33	66.35	6.256	0.338	0
Phase Margin Frequency(summary)	90.6% (453/500)	156.8M		343.2M	238M	31.01M	0.408	0
Phase Margin Frequency_MC-GENERAL	90.6% (453/500)	156.8M	> 200M	343.2M	238M	31.01M	0.408	0
Yield Estimate: 73.2 %(366 passed/500 pts) | Parameters: T=80								
DC_Test								
(VDC("/VDC") - VDC("/Vout"))(summary)	100% (500/500)	-2.512m		1.997m	26.83u	703.7u		0
(VDC("/VDC") - VDC("/Vout"))_MC-GENERAL	100% (500/500)	-2.512m	info	1.997m	26.83u	703.7u		0
KK_StackedTank28_KK_EA_TB_1								
Phase Margin(summary)	82.6% (413/500)	48.15		80.33	66.35	6.256	0.338	0
Phase Margin_MC-GENERAL	82.6% (413/500)	48.15	> 60	80.33	66.35	6.256	0.338	0
Phase Margin Frequency(summary)	90.6% (453/500)	156.8M		343.2M	238M	31.01M	0.408	0
Phase Margin Frequency_MC-GENERAL	90.6% (453/500)	156.8M	> 200M	343.2M	238M	31.01M	0.408	0

Figure 4.9: Monte Carlo result summary.

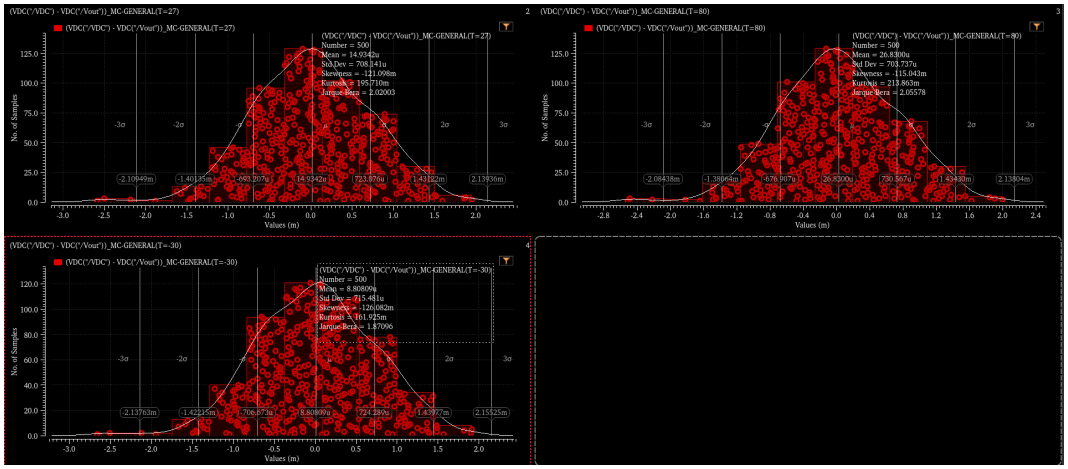
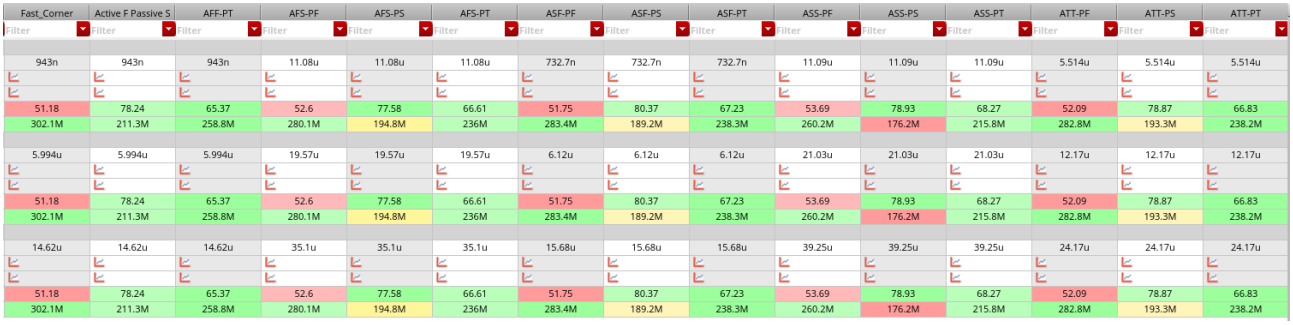


Figure 4.10: Monte Carlo histograms.

The standard deviation of the input offset being < 1mV, the specifications are met.

4.3.3 Process Corners



Fast_Corner	Active F Passive S	AFF-PT	AFS-PF	AFS-PS	AFS-PT	ASF-PF	ASF-PS	ASF-PT	ASS-PF	ASS-PS	ASS-PT	ATT-PF	ATT-PS	ATT-PT
943n	943n	943n	11.08u	11.08u	11.08u	732.7n	732.7n	732.7n	11.09u	11.09u	11.09u	5.514u	5.514u	5.514u
51.18	78.24	65.37	52.6	77.58	66.61	51.75	80.37	67.23	53.69	78.93	68.27	52.09	78.87	66.83
302.1M	211.3M	258.8M	280.1M	194.8M	236M	283.4M	189.2M	238.3M	260.2M	176.2M	215.8M	282.8M	193.3M	238.2M
5.994u	5.994u	5.994u	19.57u	19.57u	19.57u	6.12u	6.12u	6.12u	21.03u	21.03u	21.03u	12.17u	12.17u	12.17u
51.18	78.24	65.37	52.6	77.58	66.61	51.75	80.37	67.23	53.69	78.93	68.27	52.09	78.87	66.83
302.1M	211.3M	258.8M	280.1M	194.8M	236M	283.4M	189.2M	238.3M	260.2M	176.2M	215.8M	282.8M	193.3M	238.2M
14.62u	14.62u	14.62u	35.1u	35.1u	35.1u	15.68u	15.68u	15.68u	39.25u	39.25u	39.25u	24.17u	24.17u	24.17u
51.18	78.24	65.37	52.6	77.58	66.61	51.75	80.37	67.23	53.69	78.93	68.27	52.09	78.87	66.83
302.1M	211.3M	258.8M	280.1M	194.8M	236M	283.4M	189.2M	238.3M	260.2M	176.2M	215.8M	282.8M	193.3M	238.2M

Figure 4.11: Process corner values. (Legend below)

LEGEND (ONLY RELATED TO NUMERICAL VALUES): The first row exhibits the mismatch between Vout and Vref (amplifier is connected in a voltage follower topology) the fourth and fifth rows exhibit the PM and the GBW relatively. This is repeated for each temperature (-30,27,80)°C, where the first set of rows (from the top) correspond to -30, then 27 and finally the last set of rows corresponds to 80

The circuit characteristics across the process corners exhibit a certain pattern.

- **Input offset increases with temperature for the same process corner.**
- **Corners with changes to passive components drastically change the circuit's stability performance.**

The second point is consistent with theory. PS (PF) corners refer to slow (fast) passives i.e. bigger (smaller) effective passive component values, and it is known that a bigger (smaller) capacitor value decreases (increases) the GBW and increases (decreases) the PM (in this case the passive component is the compensation capacitor). This logic can be extended to all process corners shown in Fig. 4.11, where passive components are increased or decreased in effective value.

4.3.4 Output Range

In order to study the output range, the circuit test bench and connections have to be changed from the voltage follower topology to the one presented in Fig. 4.12 below.

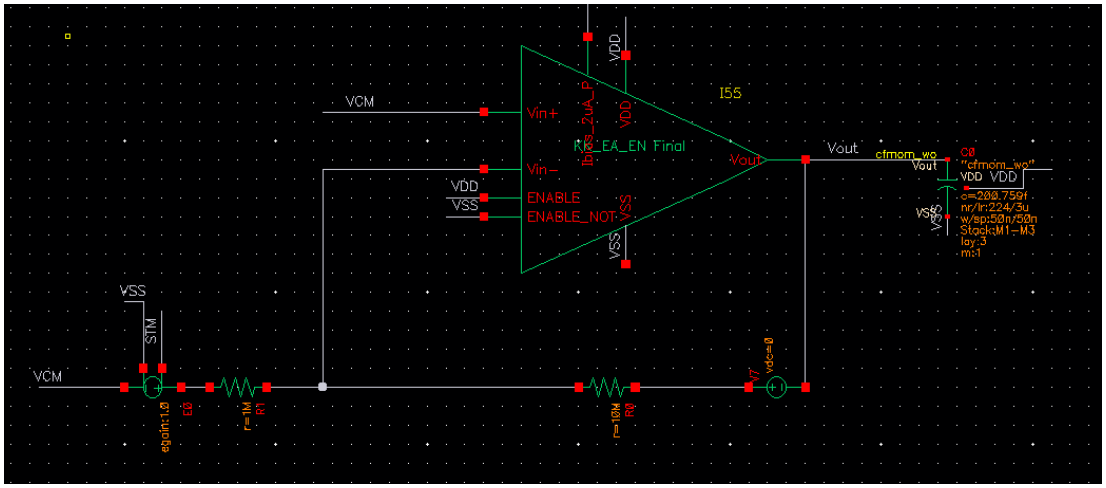


Figure 4.12: Circuit Topology to Test the Output Range.

A DC sweep has been performed on VCM and the circuit response has been studied. In order to better understand the response, a simple circuit study has to be made. The equation (referring to Fig. 4.12) relating input to output is the following :

$$Vout = \frac{VCM - VCM - STM}{1M} \cdot 10M + VCM \tag{4.3}$$

This equation assumes that the amplifier is working properly. Assuming that STM is a dc voltage and it is swept across several values, then the proper operation of the circuit can be identified in the range where a slope of -10 appears in the voltage sweep. Therefore, the presence of a -10 slope will be used to indicate the two extremities of the output voltage swing.

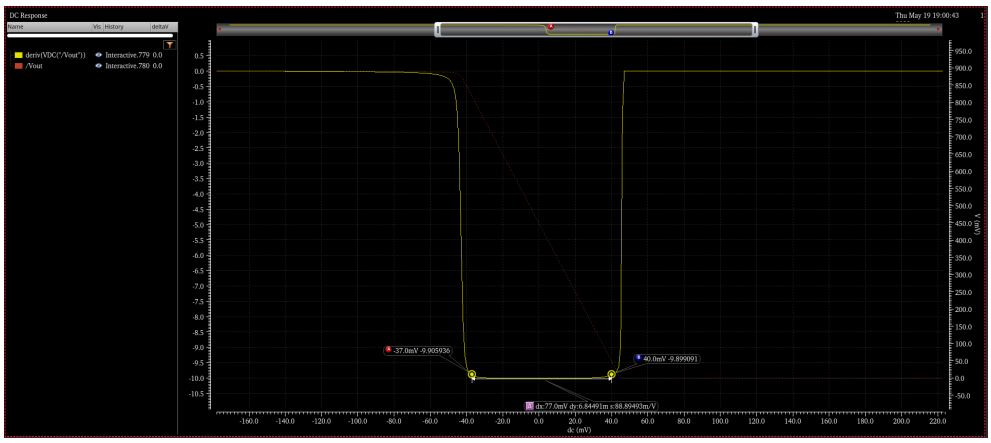


Figure 4.13: Vout and it's derivative vs the STM(dc) voltage sweep.

The points to be taken on the derivative plot are within +-1% variation, i.e. -9.9 slope. The two points are shown in the figure above and they lie at -37mV at the lowest extremity and 40mV at the highest extremity. Plugging in these values

in the equation presented above indicates an output voltage range ranging from **(50→820)mV**. It is important to bring to the reader's attention that the value of VCM is VDD/2 which corresponds to 450mv.

Chapter 5

The Ramp and Current Generators

5.1 Introduction and Circuit Overview

As introduced in the first chapter, in order to control the duty cycle (Ton/Period) two signals are compared through a comparator. These signals are the ramp voltage and the bandgap voltage which is always fixed at 300mV. The output of the comparator goes to logic state 1 when the ramp voltage drops below the bandgap voltage. The amplifier output is the starting point for the ramp voltage that starts to decrease with a constant slope when the clock signal CLK goes high, while it goes back to the amplifier output voltage level when CLK is low. The decrease in slope is always constant as it depends on a fixed current discharging a fixed capacitor (will be seen later on). Therefore, the main impact on the duty cycle (which determines the conversion ratio of the DC-DC converter) arises from the initial voltage value of the ramp voltage i.e. the error amplifier output.

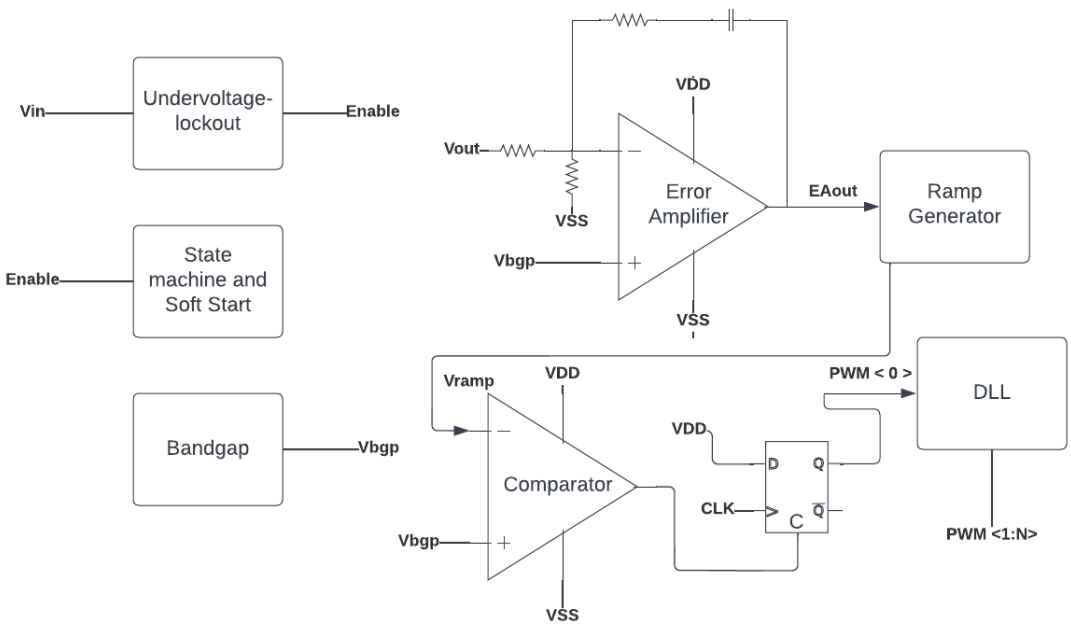


Figure 5.1: The control block view

In this chapter, the ramp generator including the current generator which supplies it will be presented.

5.2 The Ramp generator Design Methodology

In order to generate a voltage that decreases with a constant slope, a fixed current and capacitor are needed in the general case. According to the following equation $C = i\frac{dv}{dt}$, one can infer that a constant voltage slope can be achieved by fixing the current and capacitance. In fact this is the operating principle of the ramp generator shown below in Fig. 5.2.

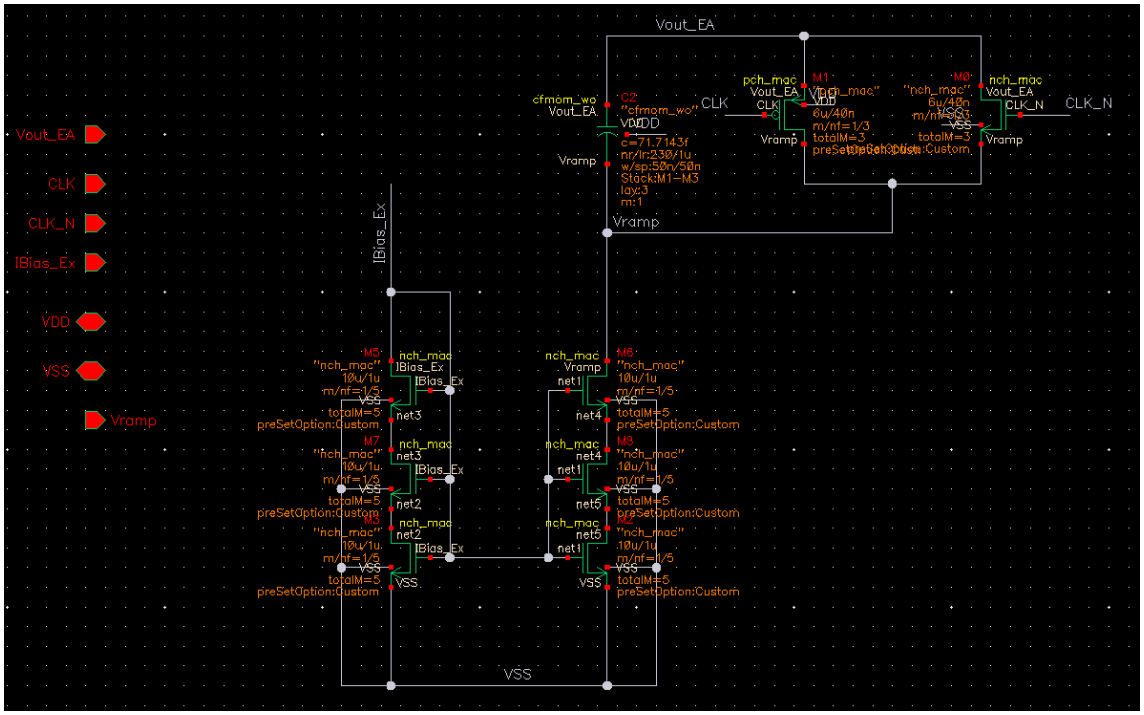


Figure 5.2: The ramp generator schematic

The first decision to be made by the designer in this block is to choose the current that will discharge the capacitance. Since a small capacitance is desirable (the used capacitance is $71fF$), then the main parameter to be modified in order to control the discharge slope is the current.
This decision is made based on the fact that the generated ramp voltage will be always compared to a fixed 300mV bandgap reference voltage, and the current has to be chosen in a way that at a maximum error amplifier output of 800mV (see 4.3.4), the ramp voltage does not cross the 300mV threshold. Since a very high error amplifier output voltage implies a converter output that is lower than the target, then the maximum duty cycle has to be set. Summing up, a maximum error signal voltage is assumed, then a discharging current is set in a way to prevent crossing the 300mV switching threshold which causes the Ton (Duty cycle) to not reach its maximal value. A minimum margin of around 30-50mV above the bandgap voltage was chosen across all corners and temperatures. According to the setup and the imposed conditions mentioned previously, a $10\mu A$ current was chosen to discharge the capacitor. This current will be originating from the current generator which will be discussed in the next section.
In order to properly copy this current, a current mirror with a relatively large effective length should be used. This is done in order to mitigate the Early effect which induces a change in the drain current of the transistor based on the value of the drain to source voltage that is very different between the two transistors in this case. Three transistors are stacked with a length of $1\mu m$ each in order to achieve a total effective length of $3\mu m$. Setting this mirror will allow the capacitor to dis-

charge with an accurate current. However, in order to charge the capacitor back to the error amplifier output voltage, a pass transistor is utilized. This pass transistor is sized in a way to allow the flow of large currents such that the voltage Vramp can quickly reach its steady state voltage before the next rising clock.

Transistor	**Sizing**
M0	W = $6\mu m$ L = $0.04\mu m$
M1	W = $6\mu m$ L = $0.04\mu m$
M5/M7/M3	W = $10\mu m$ L = $1\mu m$ *3
M6/M8/M2	W = $10\mu m$ L = $1\mu m$ *3

Table 5.1: Transistor sizings (Referring to Fig. 5.2) for the ramp generator. Transistors M5,M7,M3 and M6,M8,M2 are considered to be two single transistors with triple the individual length, since they are three individual transistors in series. All the transistors presented here are of the standard flavor.

Summing up, this circuit operates based on the CLK (clock) signal and its inverted version. In fact, when clock is high the capacitor is being discharged by the $10\mu A$ current discussed before. However, when CLK is low, the strong pass transistor is activated and pulls up the ramp voltage to the error amplifier output. This can be clearly seen in the simulated signals.

5.3 The Current Generator Design Methodology

As mentioned previously, for the ramp generator to function properly, its capacitor has to be discharged by a constant current which sets the decrease in slope of the ramp voltage signal. This current is generated from the circuit found in Fig. 5.3 below.

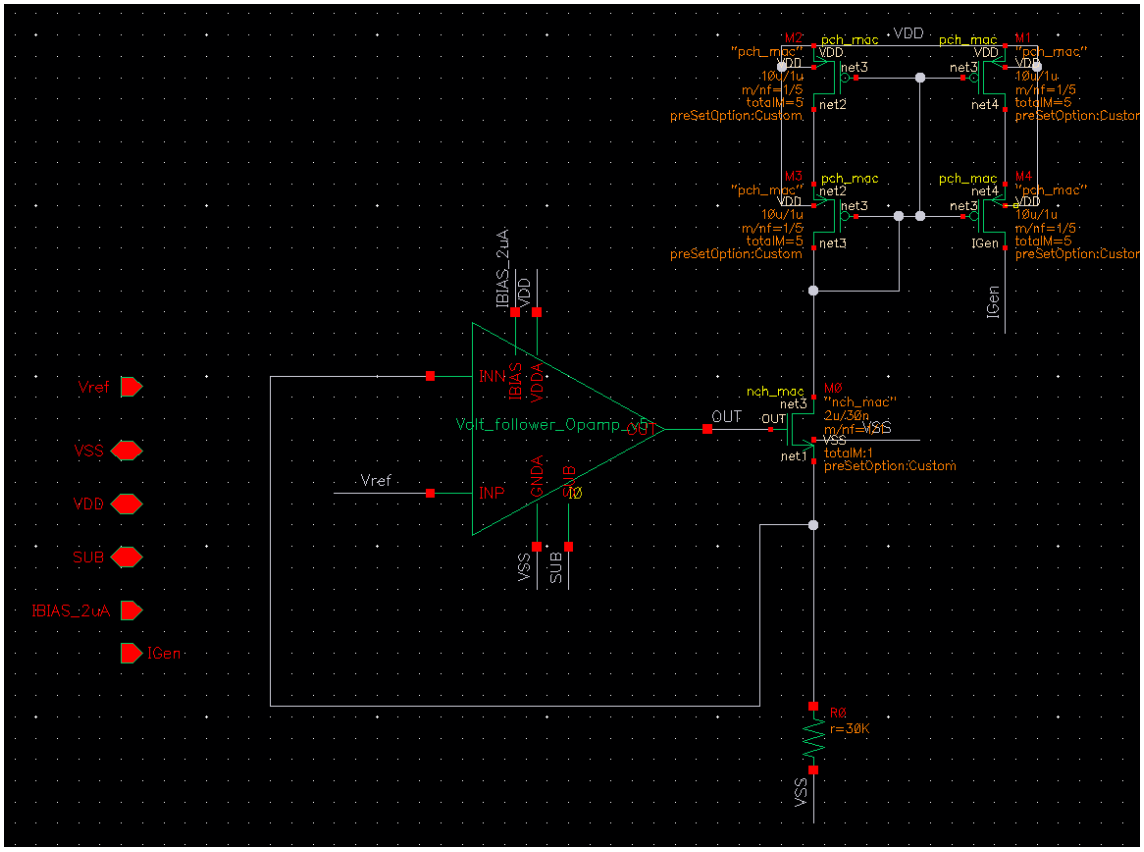


Figure 5.3: The current generator initial schematic

This circuit (a very well known voltage to current converter) consists of a pre-designed amplifier optimized for voltage follower applications, a current mirror and an external resistor. An external resistance is needed since a very accurate current is required, and integrated resistors can vary a lot with process corners as discussed before. Looking closely at the schematic, one can see that the amplifier output is not directly connected to its negative input, but it drives an NMOS. This is done in order to avoid reducing the gain of the amplifier since it is directly proportional to the output impedance. If a transistor was not used and the output was connected to the external resistance then the total resistance (the parallel of both the high amplifier output impedance and the relatively low resistance of the external resistor) is significantly decreased thus the gain is reduced as well. This can be critical for the proper operation of the circuit, therefore it is avoided by making the amplifier drive a capacitive load instead of a resistive one. Another issue that arises from connecting the amplifier output to the resistance is that current can flow from the amplifier to the resistor, thus making the current inaccurate.
In this topology, the operational amplifier is made to equalize both of its inputs to the same value, consequently the circuit operates in a way where the voltage drop across the resistor is exactly Vref. In this case Vref is the voltage from the bandgap i.e. 300mV, thus the current can be set by choosing the resistance value. In order to generate the $10\mu A$ current needed to supply the ramp generator, an ideal

resistance of $30K\Omega$ is used (this is possible since an external resistance is used). Applying Ohm's law, one can easily verify that the generated current is indeed what is required. Additionally it is worth noting that the operational amplifier is supplied by a $2\mu A$ current coming from the previously discussed 0.9V version of the beta multiplier. However, this simple design is very susceptible to noise. Given that a pin is needed in order to connected the external resistance, noise coupling from that pin can be problematic. Therefore, in order to see the effects of noise on this circuit a sinusoidal wave with an amplitude of 100mV and frequency of 200MHz (the switching frequency of the converter) is coupled through a capacitor to the susceptible node (see Fig. 5.4).

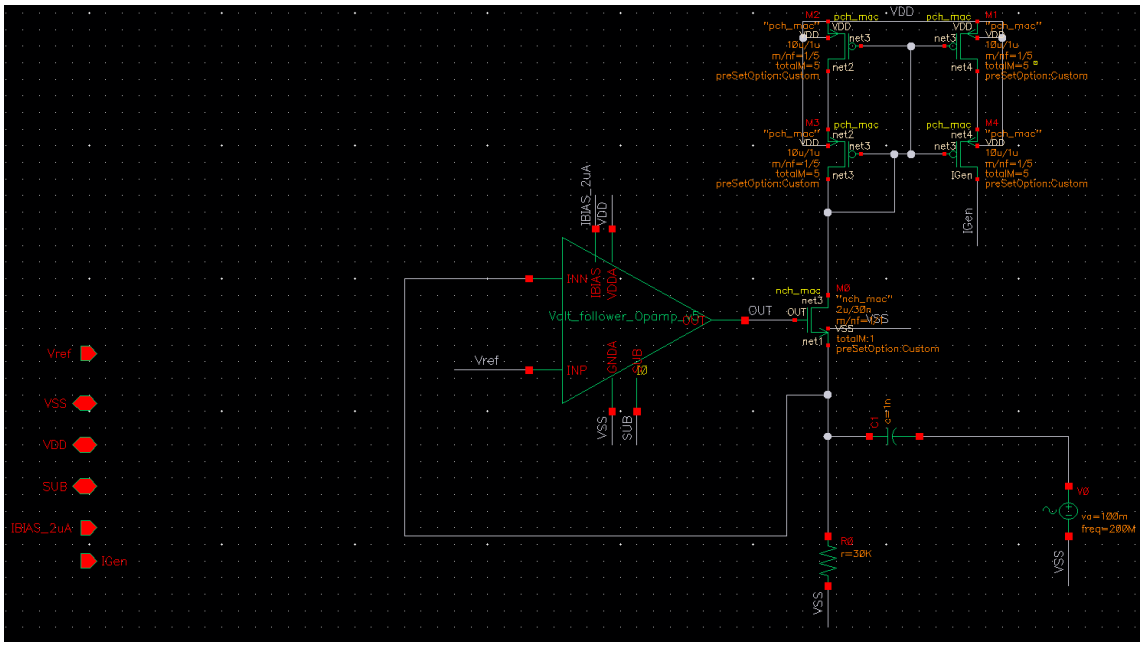


Figure 5.4: The initial current generator noise test schematic

Simulating this leads to a degraded behaviour as the current is not stable and fluctuates to very high, and low values. This will lead to the critical effect of varying slopes in the ramp voltage which is not acceptable.

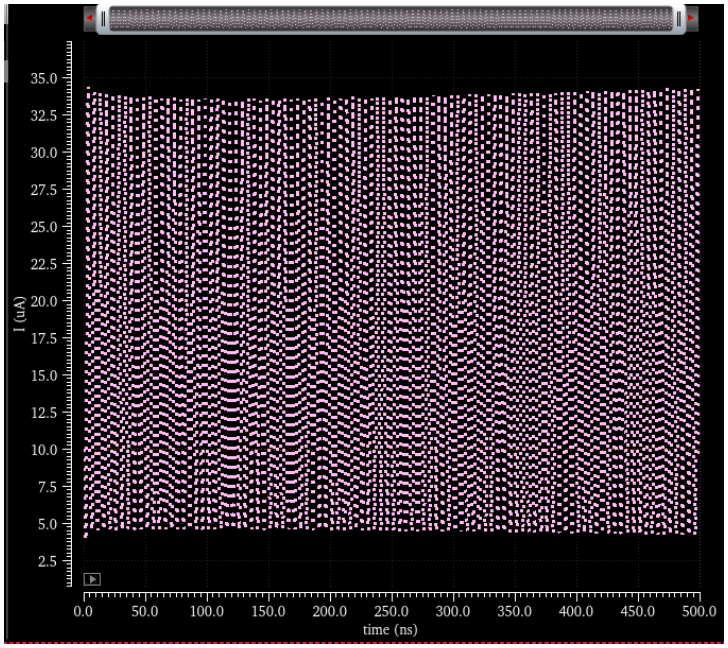


Figure 5.5: The current after noise injection for the first topology.

However, another promising typology (see Fig. 5.6) consists of a slightly more complex version of the circuit presented initially. One can see that the amplifier output connection is no longer in the same branch where the external resistance is present, and an RC circuit was added between the susceptible node and the negative input of the amplifier. The RC cutoff frequency was chosen to be around 100MHz in order to have a significant gain reduction at the expected noise frequency which is about 200MHz.

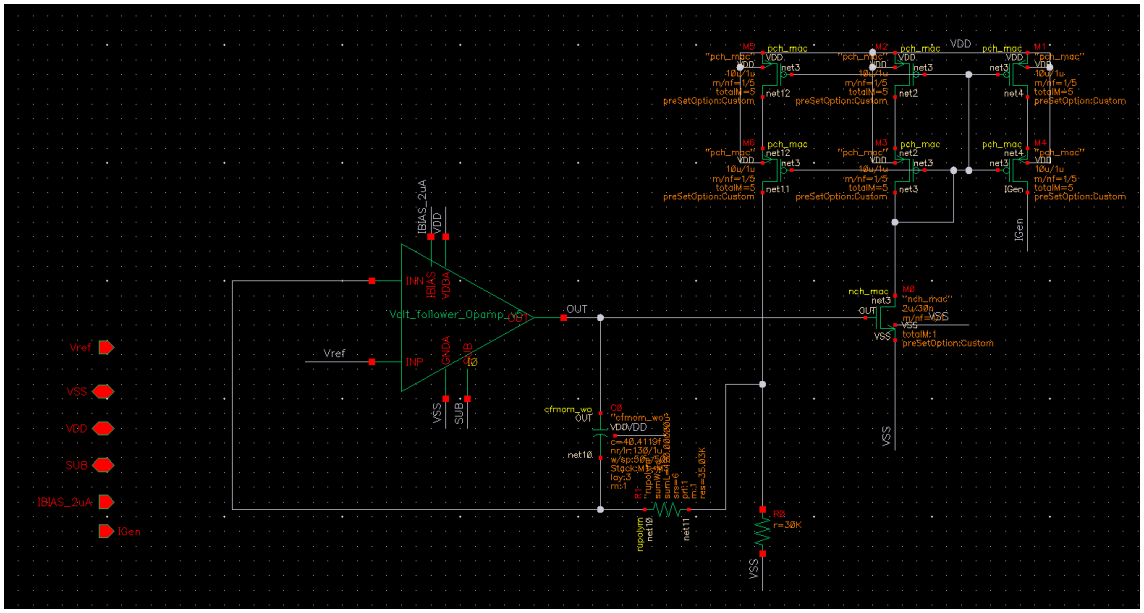


Figure 5.6: The noise tolerant current generator schematic

Coupling the same noise (as the first topology) at the susceptible node for the improved circuit leads to a drastically different result. The current in this case remained almost constant. This is presented below in Fig. 5.7.

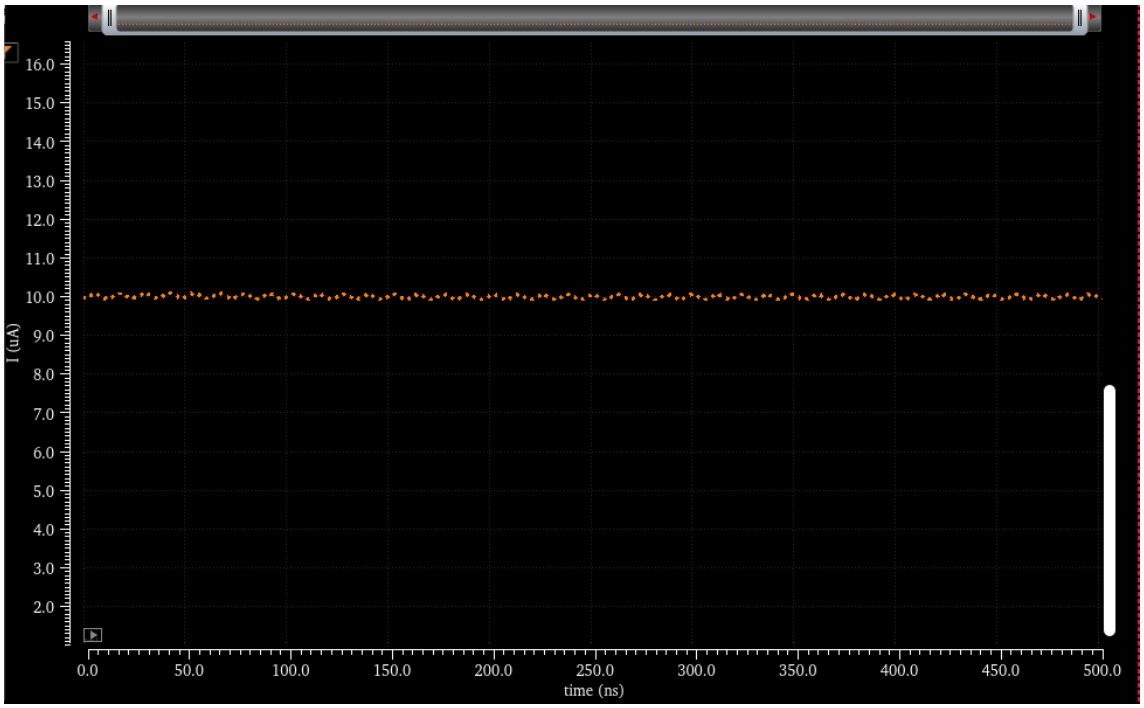


Figure 5.7: The current after noise injection for the improved topology.

The sizing of the transistor directly biased by the output of the amplifier was chosen in order to guarantee a driving capability that is sufficient for this circuit's operation. In addition, the transistors in the current mirror were sized in order to have a large effective length (stacking two transistors in series) which is needed to mitigate the early effect. Finally, the RC circuit consisted of a capacitance $C = 40fF$ and a resistance $R = 35K\Omega$. The external resistance and the reference voltage along with the operating principle of this topology are the same compared to the initial circuit.

Transistor	**Sizing**
M5/M6,M2/M3 and M1/M4	W = $10\mu m$ L = $1\mu m$ *2
M0	W = $2\mu m$ L = $0.03\mu m$

Table 5.2: Transistor sizings (Referring to Fig. 5.6) for the current generator. Transistor names separated by a '/' are considered to be single transistors due to the serial connection used to achieve a high effective length. All the transistors presented here are of the standard flavor.

5.4 Simulation Results

In this section, all the real blocks will be used in order to properly test the ramp generation. In fact, the error amplifier fixed to an output voltage of 800mV, along with the other real components such as the bandgap, the current reference, and the current generator were all added. This can be seen as a system level view as all of the blocks interact with one another. This interaction is of particular interest for the propagation of SEs and their effects on the output (mainly the ramp signal). The SE test on the system level will be presented in the final chapter of this work.

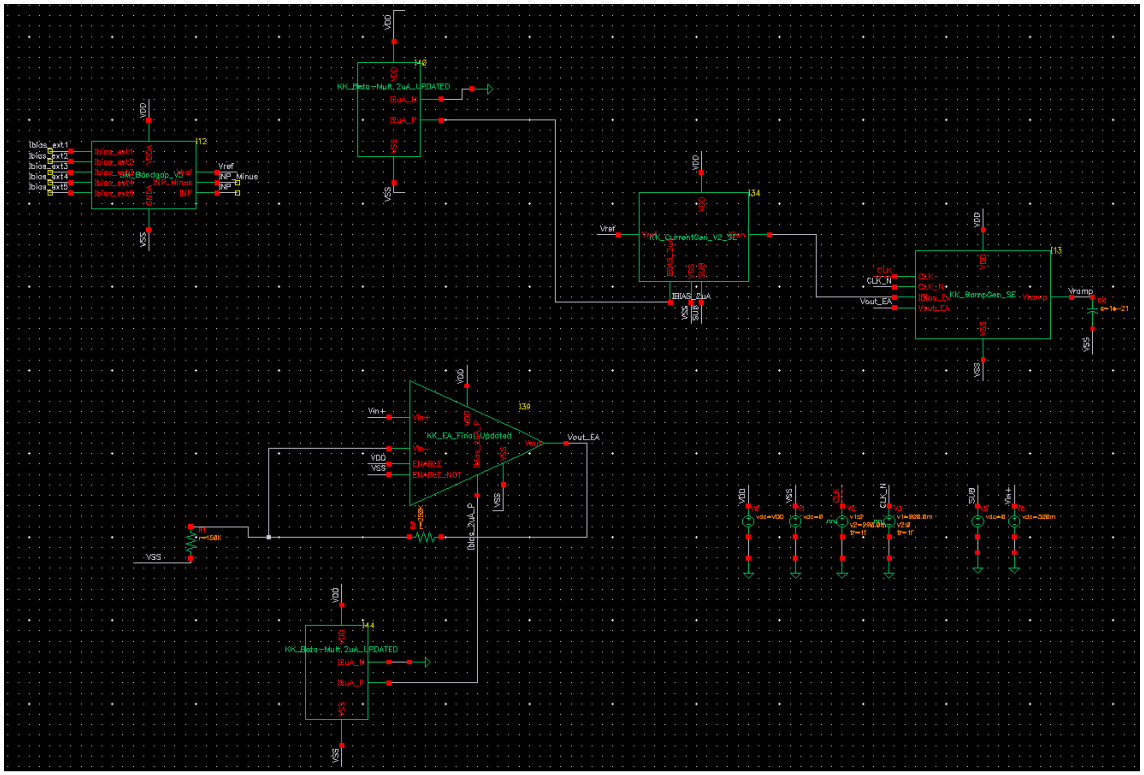


Figure 5.8: The system level view of the ramp generator

Some of the signals were ideally generated, such as the clock and supply voltages. The use of real generators of these signals is out of the scope of this study.

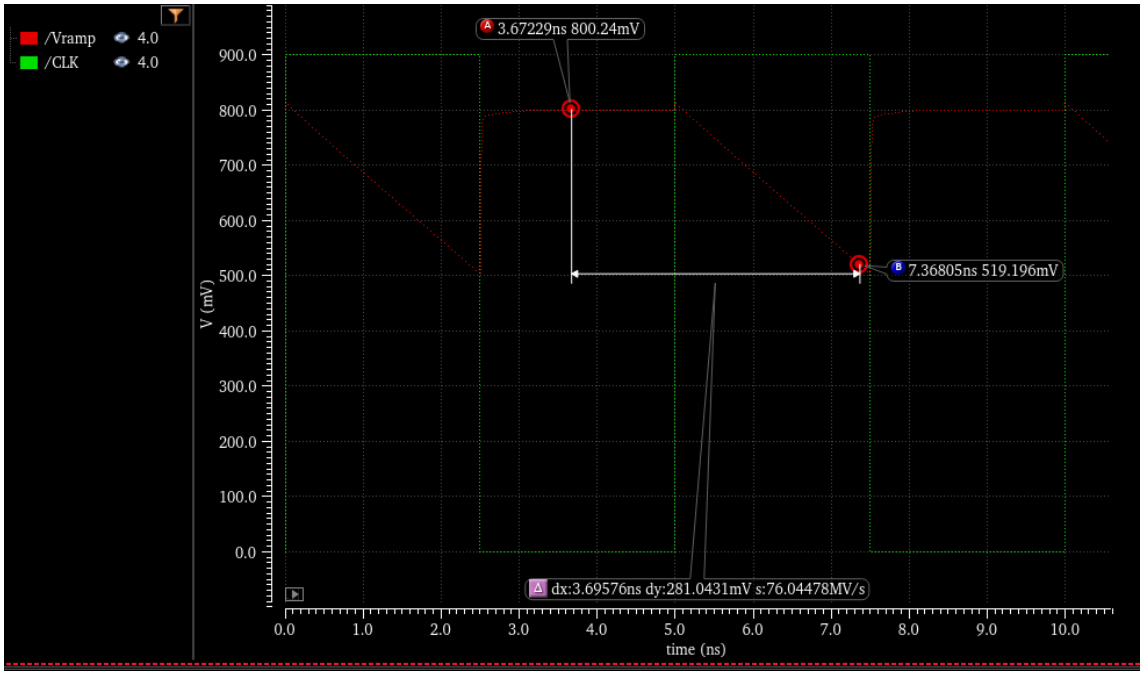


Figure 5.9: The ramp and clock signals.

As mentioned before, the ramp signal decreases with a constant slope when CLK is high and then is set back to the voltage of the error amplifier (set to be 800mV) when CLK is low. It is important to note that in the ramp signal presented in Fig. 5.9 is in the nominal corner at room temperature, and thus the lowest value it can reach is around 200mV above the bandgap voltage which is 300mV. In other critical corners, the difference between these two signals goes down to around 30-50mV. This worst case margin is acceptable as discussed before.

Chapter 6

SE Critical Nodes and Hardening Approach

In this chapter, the schematic used for SEE testing along with the general approach towards SE hardening will be discussed. Accordingly, the modified circuits will be shown with the proposed solutions.

6.1 General Approach

Making a circuit robust towards Single Event Effects is not an easy task. It is specifically challenging to completely filter out an SE-induced voltage spike in nodes that are inherently fast in reacting to voltage or current variations. For example in the case of the error amplifier differential pair, adding components whether active or passive will usually lead to a decrease in the bandwidth of the system, therefore SE mitigating solutions are limited. Nevertheless, in many cases the transient perturbations occurring on these nodes have a very limited duration (due to the reaction speed of the node) and can be accepted. On the other hand, biasing networks and stable nodes (constant steady state voltage/current) can be made more robust to single events through the use of both a voltage clamp and an RC filter.
Single events effects are generated by highly-energetic particles that inject charge at a specific node, this injection is directly proportional to the particle's LET (Linear Energy Transfer, which represents the amount of deposited energy per unit distance and is usually expressed in $\frac{MeV \cdot cm^2}{mg}$ when normalized by the density of the target material). The maximum LET reached in CERN experiments is 40 $\frac{MeV \cdot cm^2}{mg}$, therefore all SEs will be modeled using an injected/sinked current proportional to this worst case value of the LET. This is done to guarantee the proper operation of the circuit in all cases. The charge injection has been modeled in simulations by means of a triangular current pulse, with the following parameters:

- **4 mA current amplitude with a 50 ps rise time and 150ps fall time**

Charge injection in a susceptible node creates a positive or negative spike in the node voltage. This is due to capacitances and/or resistances present at that node. The voltage increase/decrease lasts as long as it takes to sink the excess charge or recuperate the charge that has been lost. The duration of this process depends on the used bias current and some events can take much more than a 5ns clock cycle to resolve (see Fig. 6.2). Clamps (transistors) connected in between VDD or VSS and the node itself are utilized. These clamps are usually biased with a certain gate voltage such that at steady state they do not conduct. Usually the gate voltage is chosen to have a VGS (Nmos) = VSG (Pmos) = - 100mV or lower, so that it remains in cutoff in all PVT conditions. Although not the only option, resistor dividers that are not impacted by SE can be used to set these voltages.
The direct result of the clamp addition is the improvement of the circuit recovery time, since any voltage peak or valley in a critical node will lead to the activation of the respective clamp/s connected to that node, thus providing a direct path to sink or supply charge which has been injected or lost. This faster recovery entails a higher frequency voltage variation, which can be easily filtered by an RC filter.
The used filter resistance and capacitance are fixed across all the used circuits $R = 50K\Omega$ & $C = 740fF$, which exhibit a cutoff frequency of around 4MHz. The combination of both clamps and RC filters in biasing nodes (which are the most critical nodes according to simulation results) leads to a greatly improved behaviour.

A detailed explanation will be shown in the case of the ramp generator sub-block in order to prove the remarks through simulation. As for the error amplifier and the beta multiplier, the modified circuit schematics and supplementary information will be given.

As a final comment, circuit modifications have been made and tested in the system level simulation showed in Fig. 5.8 since SEEs cannot be studied in depth at the block level. In fact SEs were modeled to occur at all the sensitive nodes in each block consecutively and their effect on the ramp voltage (the system output) was studied. The circuit modifications adapted to mitigate the effects on the ramp voltage can be extended to the general case. The system level simulation just highlighted the most critical events.

6.2 The Ramp Generator Sub-block

6.2.1 SE Testing

As will be the case in all the following blocks, the schematic used to test for SEs will be introduced. Then the modified schematic adopting the SE hardening techniques will be presented.

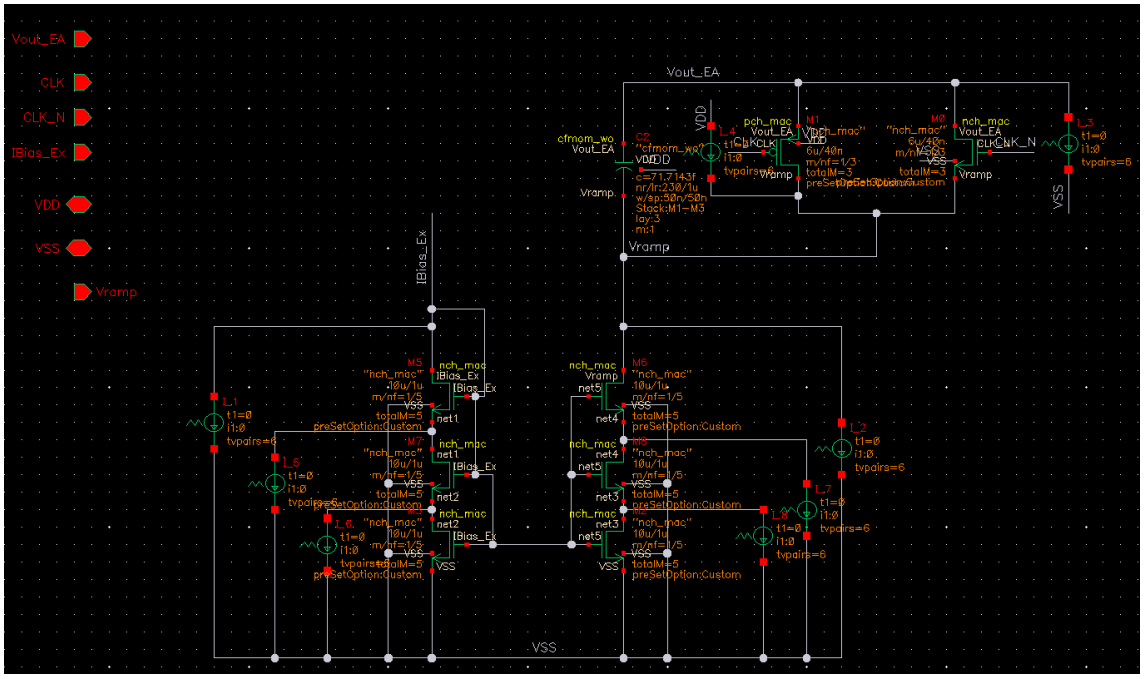


Figure 6.1: The modified ramp generator for single event testing.

Injecting the charges starting from I_1 up to I_8 in the ramp generator (Fig. 6.1) leads to a very large variation in the ramp voltage. This effect can be seen in the following figure where each current injection is represented by two pulses respectively injected on the same node when the clock is high and low.

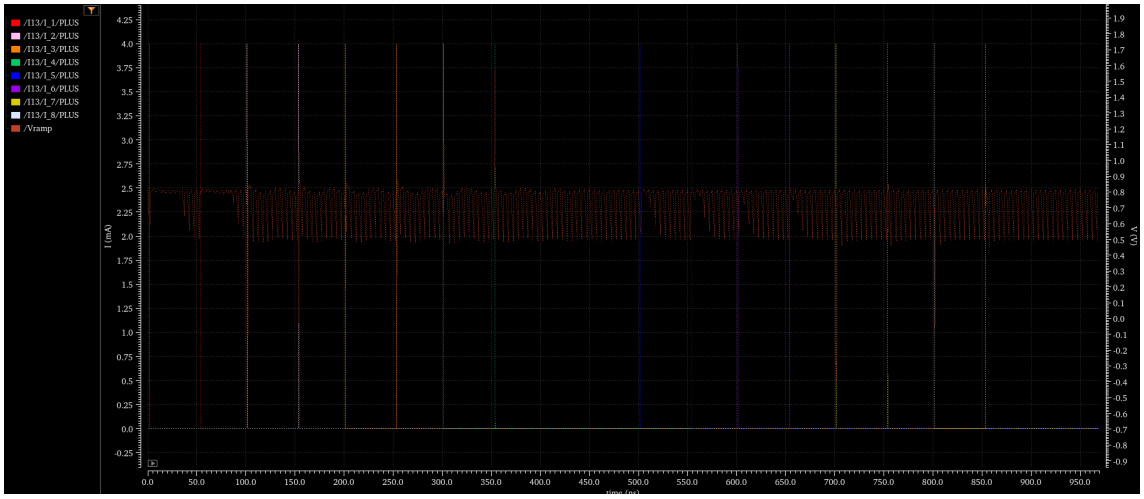


Figure 6.2: Single event induced ramp voltage variations.

Each pair of peaks represents a current injected by I_1 from the leftmost pair to I_8 at the right. It is important to note that the most critical nodes for single events according to simulations are biasing branches where a diode connected transistor is present. However, the modified network dictated by the general approach mentioned

(addition of a clamp and of an RC filter) before makes SEEs in these cases much less critical.

6.2.2 SE hardening

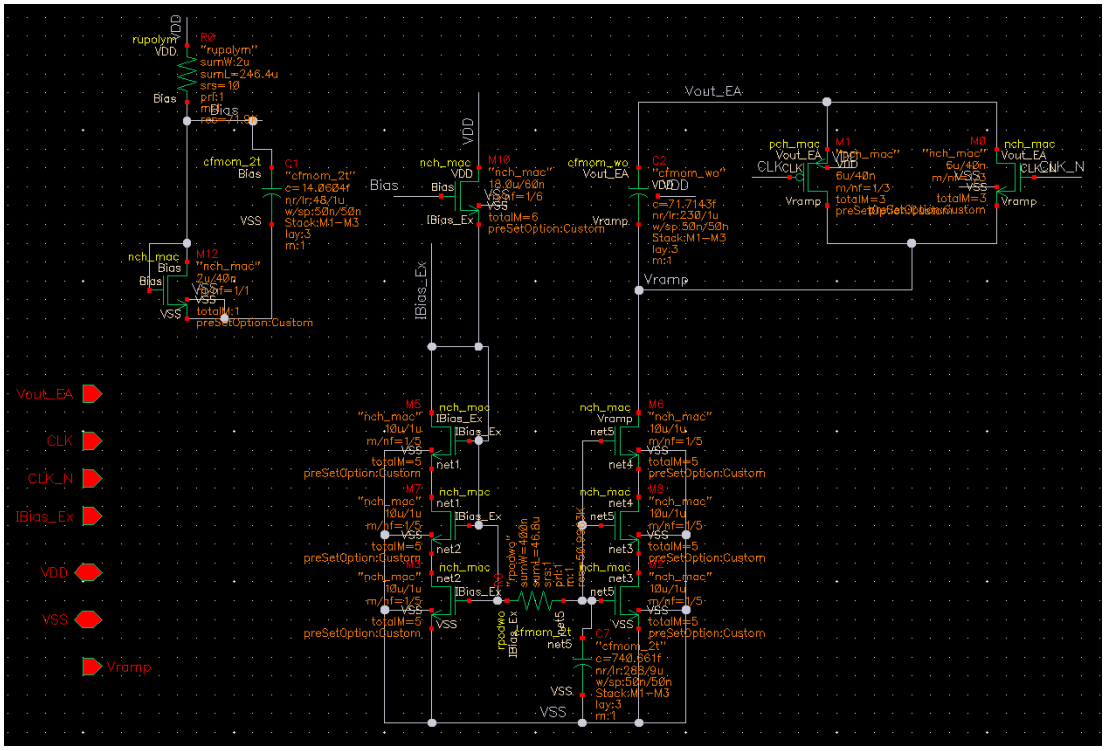


Figure 6.3: The modified ramp generator sub-block

Compared to Fig. 5.2, Fig. 6.3 features an RC circuit in between the gates of the Nmos current mirror along with a clamping transistor M10 and its respective biasing branch. It was mentioned previously that biasing voltages are usually generated by resistor dividers, but in this case it is done using a diode connected transistor (see 3.2.1.1), with an added capacitor in order to introduce a coupling to VSS at high frequencies. It is important to mention that the added biasing branch is susceptible to SEs, but since the generated voltage is connected to an Nmos drain then the SE charge sink will just lower the voltage level of "Bias", thus driving transistor M10 (the clamp) deeper into cutoff, which is not an issue since it is to be off in steady state operation. Obviously after some time "Bias" goes back to its steady state value and the clamp operates as it was initially designed to.
Going back, simulations with the addition of only a clamp were conducted. In order to avoid redundancy, the only current injection that will be studied in this sub-block is the most detrimental one which is I_1 (see Fig. 6.2). The results proved that just by adding a clamp, a much better performance can be achieved.

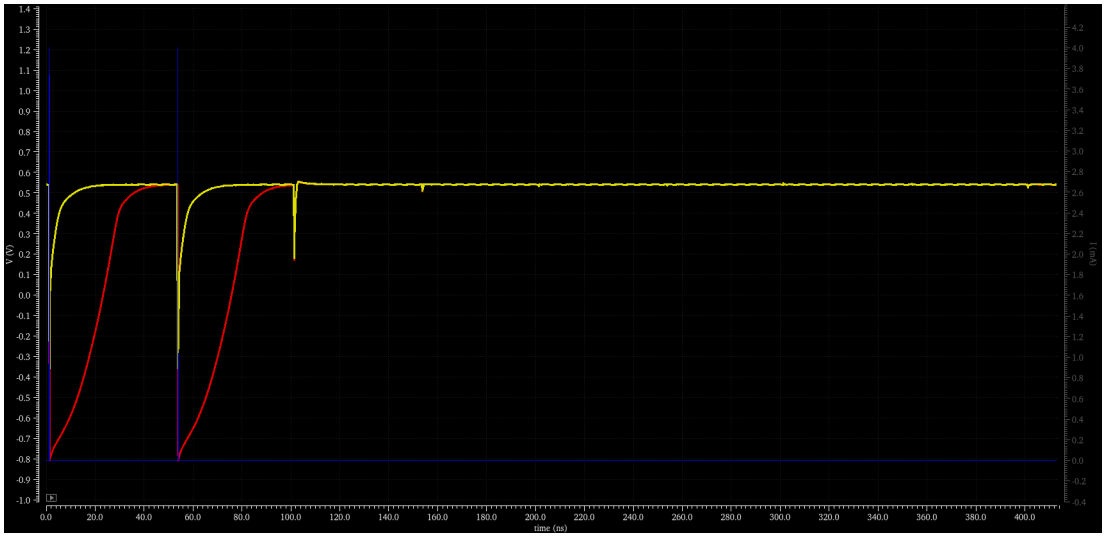


Figure 6.4: VGS of the diode connected transistor (M5,M7, and M3 in series). Yellow : VGS after adding a clamp , Red : VGS before adding a clamp, Blue : the injected current

In Fig. 6.4 above, it is clear that the addition of a clamp alone significantly decreases the circuit recovery time and therefore improves SE robustness. This improvement is translated to the ramp voltage which is shown below.

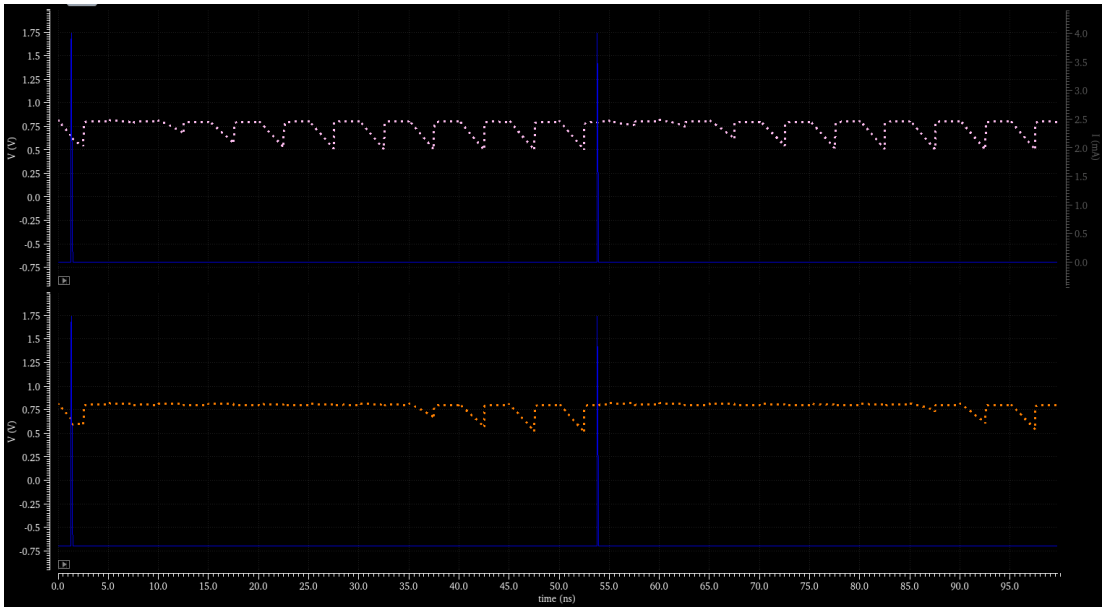


Figure 6.5: The ramp voltage before (bottom) and after (top) the addition of a clamp.

Furthermore, the addition of an RC filter almost completely removes any high frequency voltage fluctuations, therefore SEs no longer have significant effects on the node under study. This is shown in Fig. 6.6.

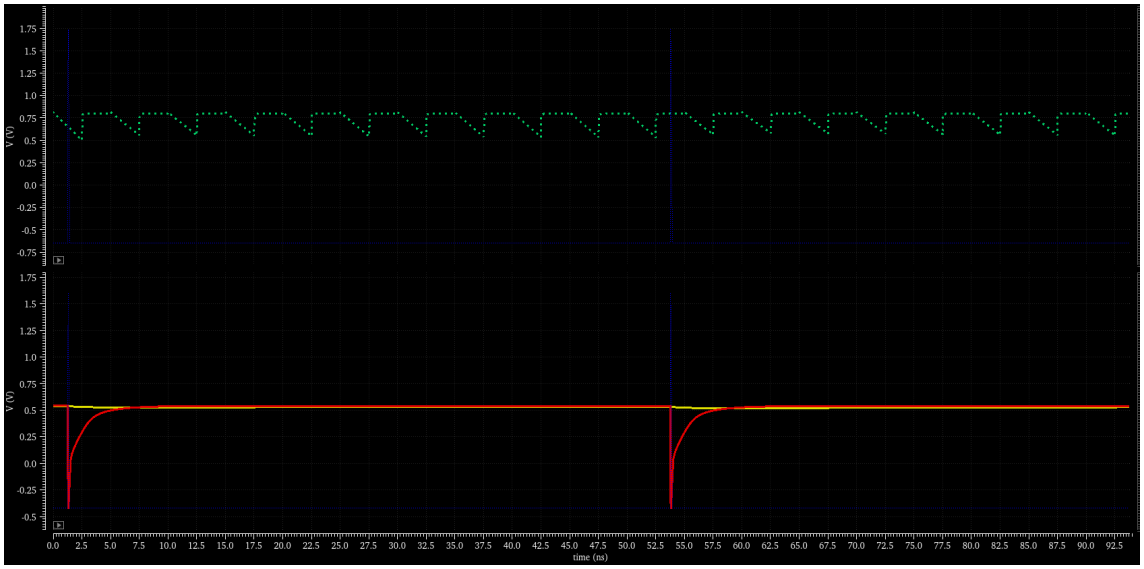


Figure 6.6: The full circuit behaviour after the addition of both a clamp and an RC filter. Green : Final Vramp / Red : VGS before the RC filter/ Yellow : VGS after RC filter / Blue : SE current injection

As observed above, the used method almost eliminated any effects of the SE. This is observed in all biasing transistors/networks and nodes that have a stable steady state voltage. Therefore, in the next sections repeating the analysis given above will be omitted to avoid redundancy.

As a final comment, SEs in the blocks connected to the ramp generator usually propagate to the output in the form of voltage variations. The most detrimental being effects originating from SEs at biasing nodes (in the EA, current generator), and in the beta multiplier. These SEs lead to a significant and long degradation of the output ramp voltage. In other cases, SEs can translate to various effects. In the case of the EA, SEs at non biasing nodes lead to a varying starting voltage of the ramp, or brief spikes and valleys in the ramp voltage. Additionally in the case of the current generator, the ramp slope can be decreased or increased and therefore the ending voltage of the ramp (ramp voltage at the falling edge of the CLK) is temporarily changed (this also occurs in the previous case concerning the EA).

An analysis of SE propagation from specific blocks to the output will not be conducted since the induced effects are very similar, and they are effectively mitigated by the adopted method.

6.3 The Beta Multiplier - 0.9V Version

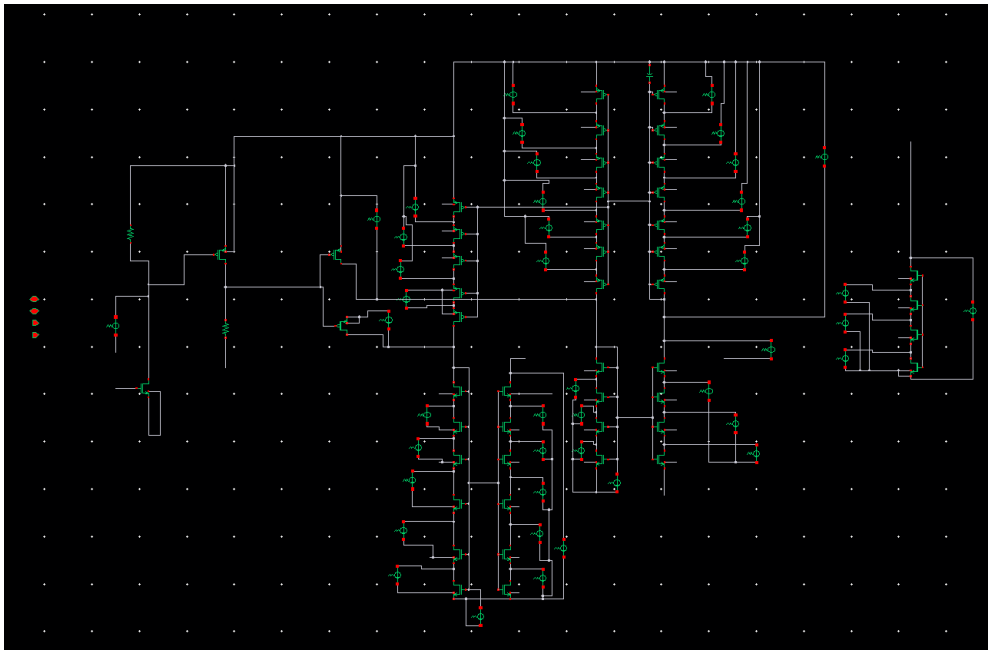


Figure 6.7: The circuit with modeled SE locations.

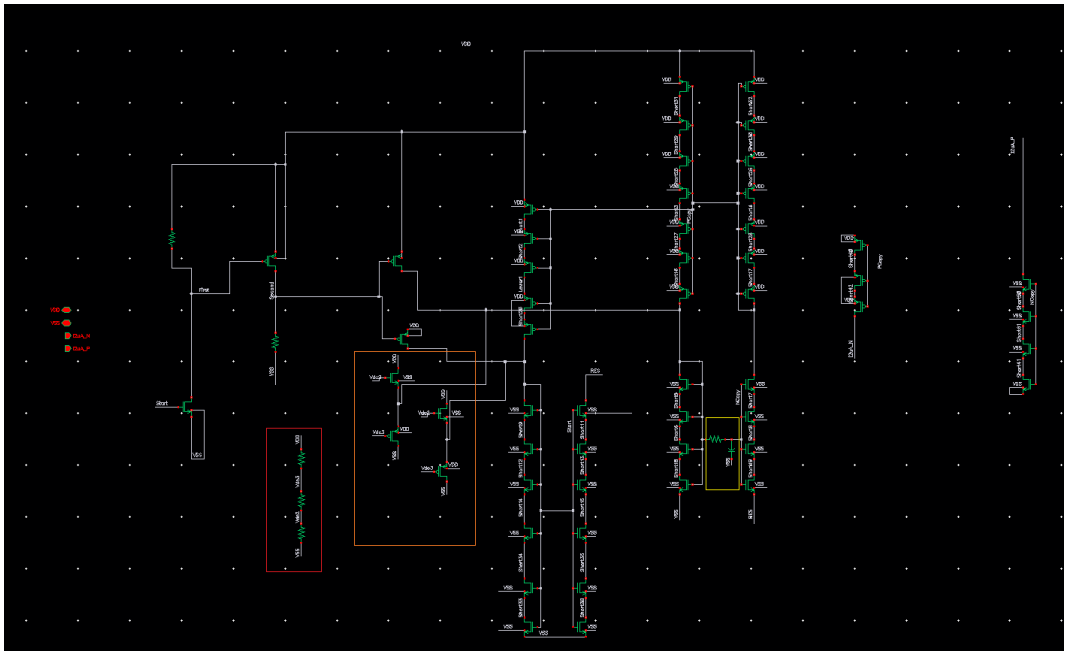


Figure 6.8: The modified Beta Multiplier schematic

As shown in Fig. 6.8, clamps (orange rectangle) were added along with a resistive divider to properly bias them (red rectangle) and an RC filter was added at the N stage (yellow rectangle). The filter was added only on the Nstage since most of the uses for this multiplier consist of utilizing the Ncopy signal originating from the Nside. Additionally, two clamps were used (see orange rectangle) since the voltage of the node they are connected to can vary greatly bidirectionally. Therefore, it is necessary to use two transistors to properly clamp the signal.

The most important SE modification regarding the current reference (the beta multiplier) does not actually lie inside the circuit itself, but in the blocks that it supplies. More specifically, the diode connected transistor that is used to set the voltages. For example, in the current generator sub-block, an OTA supplied by the beta multiplier is used. SEs impacting this biasing diode lead to very drastic variations that last for tens of cycles. Therefore, every transistor receiving current from the reference has to be clamped bidirectionally and have its gate voltage filtered by an RC filter as done before in order to be robust against SEs. As a final comment, the clamp gate biasing voltage has to be adapted to all cases in order to maintain a VGS (Nmos) or VSG (Pmos) of -100mV to guarantee that the clamp is in cutoff during normal operation of the circuit.

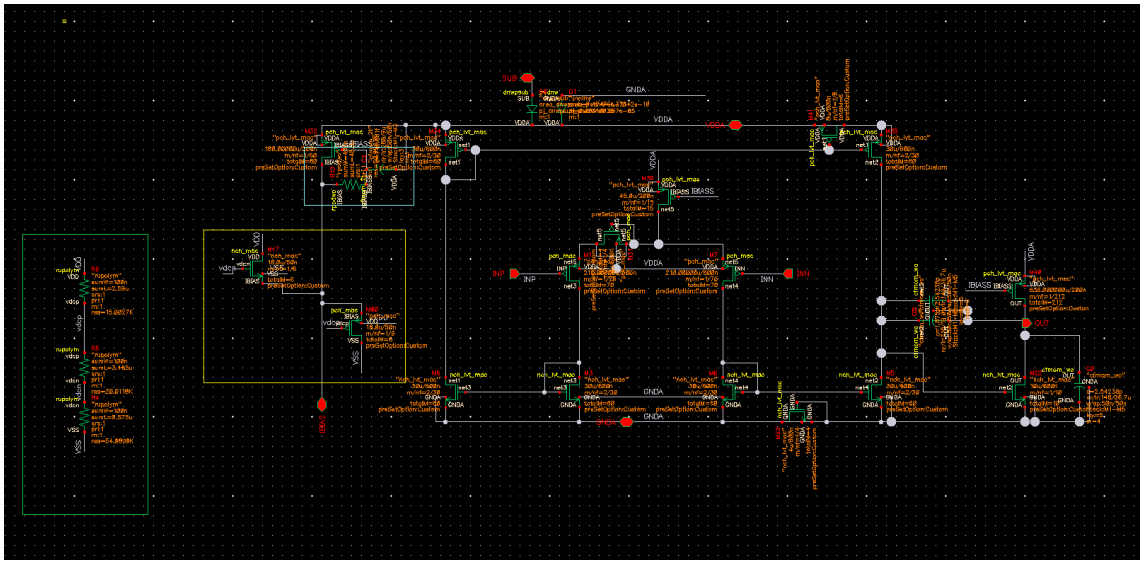


Figure 6.9: The Added protections to the biasing transistor of the current generator OTA.

As shown above in Fig. 6.9, these protections (RC filter in the blue rectangle, bidirectional clamps in the yellow rectangle, and the biasing branch which can be designed in several ways in the green rectangle) have to be present in all diode connected transistors connected to the beta multiplier.

6.4 The Current Generator sub-block

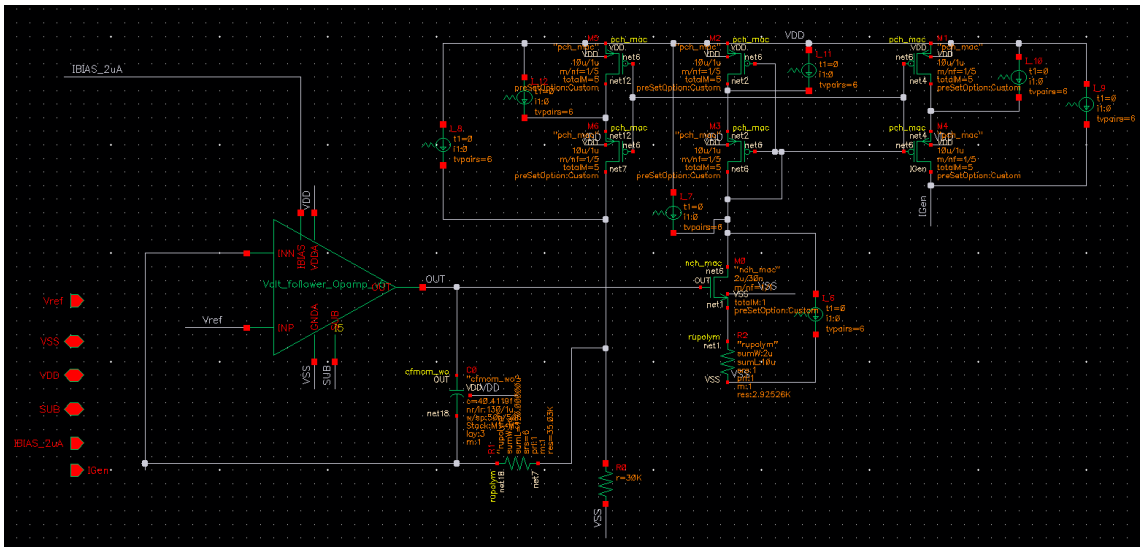


Figure 6.10: The circuit with modeled SE locations.

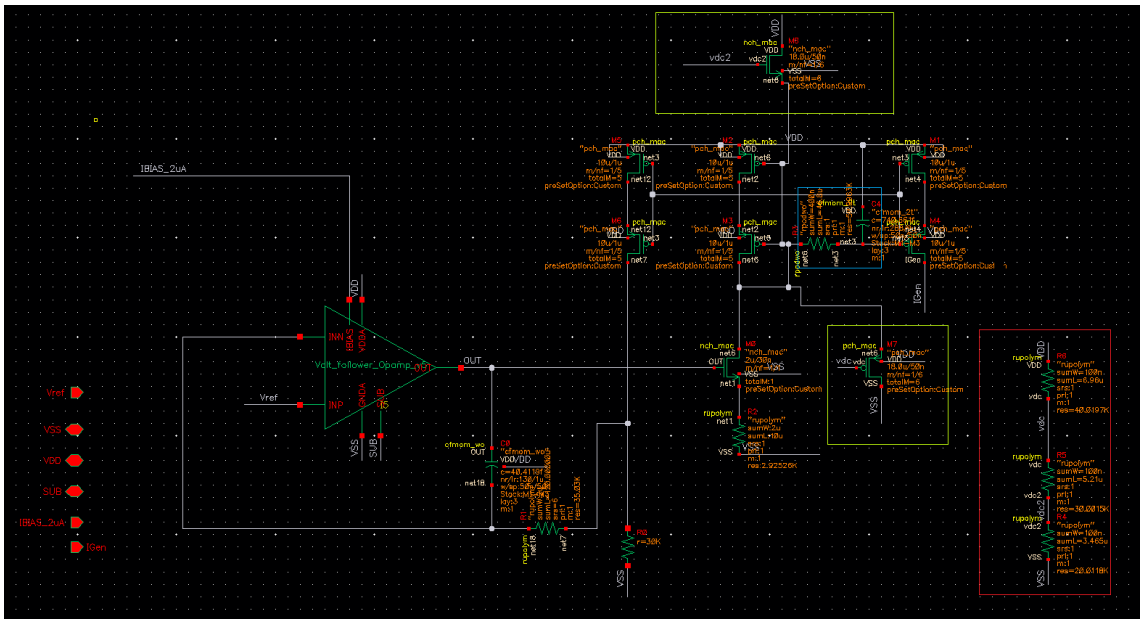


Figure 6.11: The modified Current Generator sub-block.

Other than the protections added inside the voltage follower (discussed in the previous section), two transistors (bidirectional clamp), their biasing branch, and an RC filter have been added. As mentioned before, the most detrimental node in biasing networks, current mirrors etc.. is the diode connected transistor. Therefore

all of the efforts were made mainly on these branches. In addition, simulation results confirm the effectiveness of this approach.

6.5 The Error Amplifier

The output voltage due to current injections (SEs) at certain nodes can increase to reach above 1V, but this is no reason to be concerned as the circuit recovers back to proper operation quickly and the high voltages last for a very short time.
In fact, the most important single events are the ones that impact the biasing network mainly or the beta multiplier that is providing the constant current to it as mentioned before.

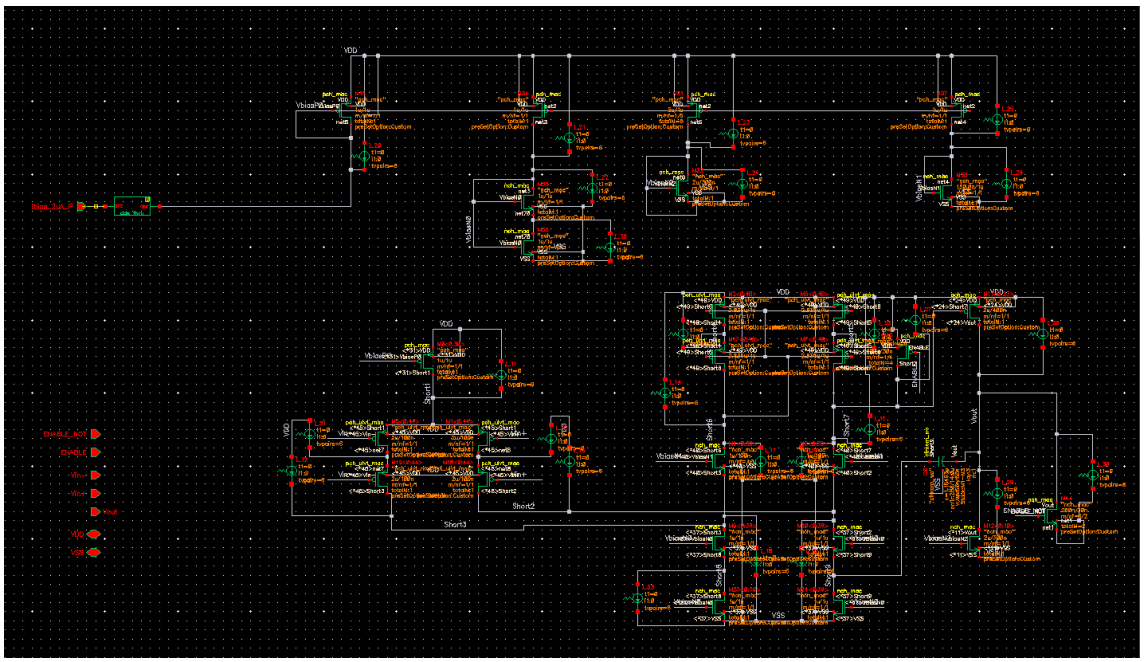


Figure 6.12: The circuit with modeled SE locations.

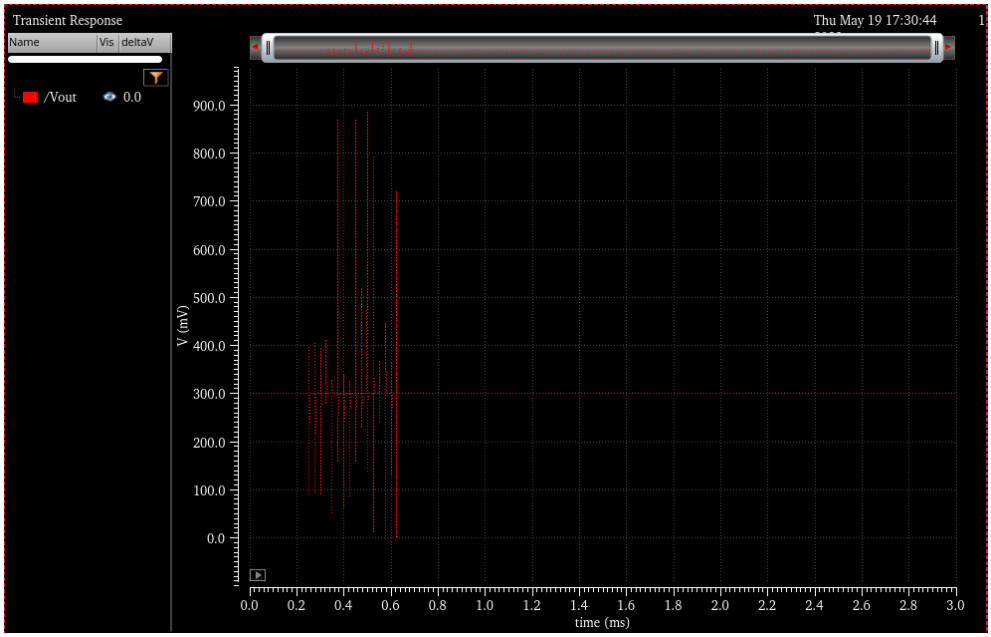


Figure 6.13: The output voltage fluctuations according to SE charge injection at various nodes in the circuit.

Finally, the simulation where the circuit returns to a proper operating point after several SEs can be observed in Fig. 6.13 above. Each positive or negative peak usually represents a SE injection at a node somewhere in the circuit.

As discussed before, the general method of using clamps combined with an RC filter can be only used on nodes that have an invariable voltage. This is not the case for the error amplifier, as its voltages are required to change quickly and it has to react in a matter of nanoseconds. Due to that, protection components cannot be inserted in the amplifier circuit itself. However, since the amplifier is designed to be fast, then SEEs on these fast nodes are not detrimental since they are able to recuperate quickly. This is not the case for the biasing network as its voltages are stable in normal operation.

Since the biasing network is supplied by the beta multiplier, then the bidirectional clamp and RC filter are added initially. Additionally, RC filters are added to all biasing transistor gates in order to filter any perturbation that may occur and prevent it from affecting the amplifier operation. Finally, clamps were added at the nodes which exhibited the need for them. Clamps can be added to all the biasing nodes/branches as it would not cause any issues. However, in this specific biasing network, some branches showed little to no variation before and after adding the clamps, so only the RC filter was added in these cases.

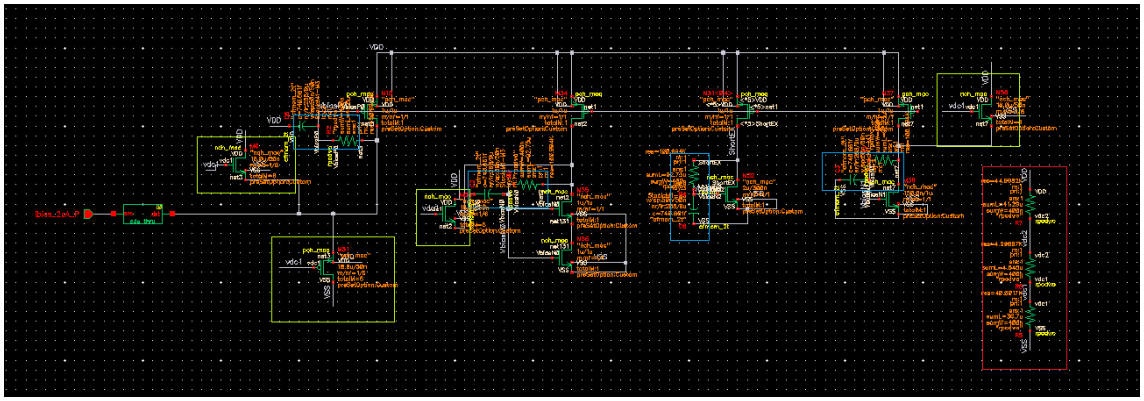


Figure 6.14: The modified EA biasing network.

Referring to the biasing network above in Fig. 6.14. The added components are bordered by rectangles with different colors.

- Blue : RC filter
- Light Green : Clamping transistor
- Red : Biasing branch

Chapter 7

Conclusion

In this work, the schematic level design of five analog blocks belonging to a DC-DC converter was presented. The converter under development represents the second stage in a two stage radiation-tolerant DC-DC powering network to be deployed in CERN's experiments. The first stage steps down a 48V input to a 5V output while as the second stage steps down 5 volts to 0.9 volts. The chosen topology for the second stage is a switched tank converter where only core transistors rated for 0.9V were utilized. Given that this converter is placed near the high energy collisions which inherently create a highly radioactive environment, several radiation hardening techniques were implemented. Radiation effects include TID (Total Ionizing Dose), SE (Single Event), and Displacement Damage (DD) effects. However only SEEs (Single Event Effects) were taken into account at the schematic level, since the used technology (commercial 28nm CMOS) is robust against TID and DD effects up to the target radiation levels for the application.

The developed blocks fit into the two main groups employed in the converter, the powering/biasing section, and the control loop. The blocks belonging to the powering section are the level shifter and the beta multiplier that are used to drive the switching transistors and provide a constant biasing current respectively. On the other hand, the designed error amplifier, along with the ramp and current generators belong to the control loop of the converter.

The first designed block is a capacitor based level shifter that is used to shift Pulse Width Modulated (PWM) signals into several voltage domains where the switches driven by it are located. This circuit employs a memory latch, which necessitates the development of a startup circuit in order to properly initialize the memory state to a desirable value. In addition, the level shifter exhibits a relatively short delay of 35ps for both rising and falling edges of the PWM signal. However, in order to mitigate the effect of single effects, the circuit along with its startup circuit have been triplicated and an output voter was implemented. Thus, in the case where a level shifter is compromised, the voter output remains correct as it is set by the two other unimpacted shifters. The total delay of the circuit after the addition of the voter is around 49ps.

The second designed block is a beta multiplier or a current reference that is used to provide a voltage independent current of $2\mu A$, along with its startup circuit that is needed to set the proper operating point. Instead of using a resistor to set the current value, a transistor in triode was utilized instead. This is done in order to achieve a better performance with process corners. In addition, the circuit was designed with core transistors rated for 0.9V while being operated with supply voltages ranging from 0.9V up-to 1.8V. Consequently, several over-voltage protections were adopted in the form of driven and undriven clamps. Furthermore, a 0.9V version of this circuit was developed for application in the control circuitry, therefore the over-voltage protections were removed as they were not necessary.

The third designed block is the Error Amplifier (EA) which belongs to the control loop of the converter. A folded cascode topology was adopted in order to have a large output voltage swing and guarantee that all transistors are in saturation for a supply voltage of 0.9V. The EA has a Gain Bandwidth Product (GBW) of 238 MHz and a Phase Margin (PM) of 66.82 °.

The final two blocks are the ramp and current generators. These blocks also belong to the control loop of the converter. In fact, they can be seen as a single block since the current generator directly supplies the ramp generator with a fixed current of $10\mu A$. The generated ramp voltage is characterized by a fixed decreasing slope with a starting potential (voltage) value set by the EA. The decreasing slope of the ramp voltage is chosen in order to properly set the on time of the power switches Ton, which in turn sets the conversion ratio of the DC-DC converter.

The project is still under development, and the layouts of the discussed blocks among others are currently being designed.

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