Politecnico di Torino

Master's degree in Nanotechnologies for ICTs

Self-heating in cryogenic HEMTs for quantum computing readout applications

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Abstract

Quantum computers are becoming more and more relevant in today's world to compete with traditional computing solutions. To achieve such performance levels it is necessary to integrate the bulky control, bias, and readout electronics inside the dilution fridge to scale the number of qubits inside the quantum computer. Low noise amplifiers realized with InAlAs and InGaAs HEMTs are a viable option to transfer the readout amplification to the $4\,\mathrm{K}$ stage. Self-heating of these devices in this operating condition is not fully characterized yet and this work wants to understand how this affects the area around the HEMT to evaluate future on-wafer integration.

Novel sensing structures are proposed to build in-situ temperature monitoring with high versatility and integration possibilities. HEMTS and Schottky diodes temperature dependent electrical characteristics are used to assess the temperature of the substrate. This ensures high possibilities of integration, using the same processes to fabricate the device to be characterized and the ones used to sense. HEMT sensing devices show crosstalk problems and low sensitivity whereas the Schottky diodes provide linear and reliable results. Multiple arrays of devices are fabricated to gather a complete 2D heatmap around the device under test. Vertical temperature profiles show to be complementary with gate thermometry values performed on the same devices. Measurements at $300\,\mathrm{K}$ prove that this approach represents a working methodology that may be integrated with other technologies.

The sensing structure was used to obtain substrate heat dissipation at cryogenic temperature. Higher or compared self-heating has been reported in the literature on the device level but this work shows how this does not affect the area around the device. Measurements at $4\,\mathrm{K}$ display values under the resolution of the sensing element at all locations characterized. This represents the possibility to position temperature sensitive devices (e.g. qubit) close to the amplifier, resulting in higher integration density.

Acknowledgement

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Contents

1

Introduction

1.1. Sequence project

With advancements in CMOS technology computing power continues to increase and this trend does not seem to saturate soon. At the same time, these traditional computing architectures are not able to efficiently solve complex problems (i.e. new drug development, accurate weather forecast ecc.), if not able to solve them at all. A new paradigm of computing is needed to address these issues in a completely different way. Here quantum computing can play a role. Harnessing the quantum physics principles it is possible to perform calculations much more efficiently and this opens the door to possibilities that were never considered before.

Multiple qubits technologies exist today[1], but in every case, they need to be operated at really low temperatures (below $4.2\,\mathrm{K}$). Each qubit requires a bias, readout, and control electronics to complete the computations. For now, given the limited number of qubits connected, it is possible to implement all of these electronics with bulky equipment positioned outside the cooling stage and connected with long cables to the qubits. To scale up this system to the dimensions necessary to compete and overcome supercomputers novel electronics solutions to be cooled down and positioned close to the qubits are fundamental. Thus, the development of electronic devices with a wide span of functionalities needs to be accomplished. The main features are compatibility with cryogenic temperature operation, very low noise, and negligible power dissipation to guarantee the correct performance of the sensitive qubits. To achieve this, it is necessary to expand our understanding of existing transistor behaviors at low temperatures that are now only used at room temperature. The development of new integrated systems and the use of innovative low-temperature effects in electronic devices would be crucial to succeed in this effort.

The European project SEQUENCE (Sense and Readout Electronics Cryogenically Integrated for QUantum ENhanced Computation and Evolving Communication) was established to unite research institutes,company and universities from all over Europe to make them collaborate on this challenging task. The main partners are IBM Research, Lund University, Fraunhofer Institute for Applied Solid State Physics, Grenoble INP, CEA Leti, Tyndall National Institute and Ecole polytechnique fédérale de Lausanne. The objective is to combine Si CMOS, III-V, and 3D integration technology to further accelerate the scaling

of superconducting and spin qubit-based quantum computers and to provide an electronic platform to drive scalability performance and reduce costs. Device design and fabrication can be tuned to make the stringent operation requirements an advantage from a performance point of view. RF circuits such as low noise amplifiers, digital-to-analog converters, mixers, oscillators, multiplexers, and RF switches are the final goal of this European project. These operate at extremely low power levels and benefit from the cryogenic temperature to achieve high performance.

1.2. Quantum readout framework

If the computational power scales linearly with the number of transistors, in the case of quantum computing it increases exponentially with the number of qubits. This implies that if it is possible to reach a high number of qubits that are connected all with each other it is then possible to overcome the computational limit imposed by the classical linear scaling.

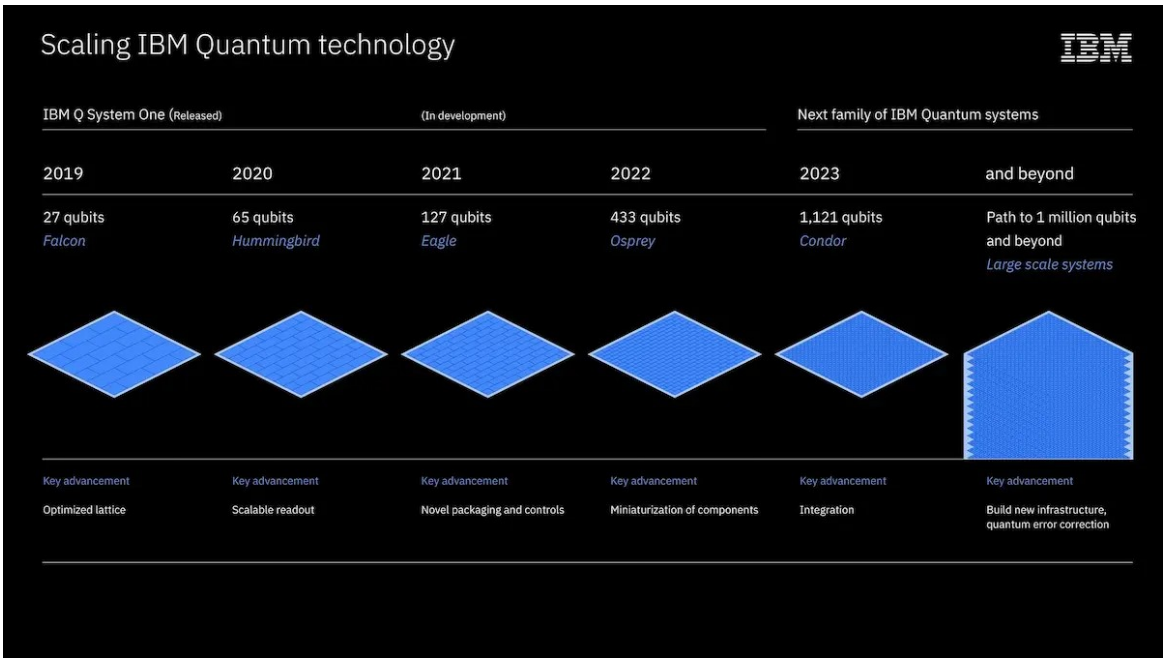


Figure 1.1: IBM quantum computer roadmap [2].

How this technology can be disruptive depends on the ways this can be used. Starting from machine learning and artificial intelligence quantum computers can help to speed up the development of new models and applications. Another crucial example is computational chemistry. In this case, the complexity of simulations required to understand the structure and the behavior of a molecule or compound is a critical point in developing new chemical processes. This includes not only new material development but also new drug research. This can enhance the effectiveness of this kind of discovery projects both in terms of money and in terms of time. Also, the financial market can benefit from quantum computers. Many simulations are often involved in the definition of an investment strategy with accurate and time-consuming backtesting. The use of a faster and more efficient technology implies ben-

efits for both quality and timings of investing solutions. Since the money volume is high a little improvement may represent a large increase in the profit margin of these operations. In addition to this, logistics and weather forecasts could benefit from a more powerful computing paradigm. This technology may enable to solve challenges that could not be tackled before, such as a new way of optimizing the supply chain or predicting the weather with accurate time predictions. To accomplish these transformations in so many sectors IBM has a clear roadmap to scale this technology to the necessary level to be competitive. It is represented in Fig.1.1. The idea is to increase the number of qubits per chip and then develop an architecture that allows to put together multiple chips. Multi-chip processors would rely on real-time chip-to-chip couplers to realize communication across numerous chips. This would enable to increase the computing power achievable.

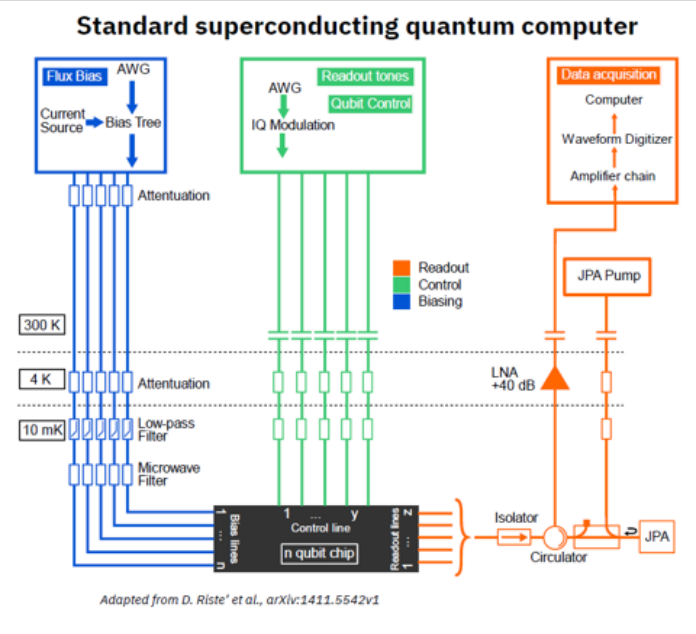


Figure 1.2: IBM quantum computer architecture [3].

All these qubits will require in any case to be controlled and read during operation time. Both in terms of space and in terms of cost all the electronics that is now used cannot be scaled up with the qubis number. In this sense, the project SEQUENCE helps to build the tools to bring this technology to reality. Each qubit needs to be biased, to be controlled, and to be read after the computation. All of these are obtained through RF signals that need to be generated and driven to the qubit. The thermal noise needs to be attenuated until it reaches a level that does not perturb its operation. There is high activity to bring CMOS technology to the $4\,\mathrm{K}$ stage to get rid of heavy and bulky room temperature electronics. The same is happening to bring the readout to a lower temperature and enable accelerated

scaling.

In today's framework, the signal needs to be thermalized, in order to analyze it at room temperature. The integration of amplifiers at lower temperatures stages, together with in-situ signal processing may be the solution to solve some of the technical bottlenecks. After a first amplification, thanks to TWPA (Travelling Wave parametric amplifier) the signal requires at least 40 dB of additional amplification. Extreme low noise and operation frequency in the range of GHz for both superconducting and spin qubits are the requirements needed to guarantee the correct operation of these devices. III-V materials have been identified as a promising candidate to realize HEMT (high electron mobility transistor), delivering low noise and high-frequency operation range performance. It is also crucial that these amplifiers are extremely low power since they will be positioned inside one stage of the dilution refrigerator, which has fairly low dissipation power. In addition to that, multiplexers to limit the number of effective amplifiers to be integrated are a viable option. This would allow to increase the total number of devices that can be inserted in the refrigerator and therefore the number of possible qubits that can be integrated within the same quantum chip for the same power and area.

1.3. Thesis outline

As described in the previous section integrated III-V amplifiers are crucial to scale quantum computers and make quantum supremacy a reality. The behavior of these devices is not completely understood and characterized at low temperatures. They have been used for other applications such as satellites and telescopes, but their behavior at cryogenic temperatures was not fully investigated. In particular, quantum applications require to understand better how the physics of the transistor changes in the case of extremely low temperatures. Other studies sum up the electrical characteristics of CMOS and SOI technology at cryogenic temperature, but a comprehensive study about III-V HEMT is not available to this date. Subthreshold swing and threshold voltage are some of the most important parameters to study. In addition to that, the project to integrate the HEMTS with other devices requires getting a deep understanding of self-heating and heat dissipation in the substrate to understand its limits and find new tailored solutions for this specific application. The benefits of this study are related to improvements in the device performance and integration limits. This is related to an increased understanding of the self-heating of the device and in dissipation mechanism in the area close to the device. Due to the high sensitivity of the qubits to temperature, these pieces of information represent a crucial step to further scaling. To achieve this, the work of the thesis will be focused on realizing a sensing structure to sense temperature directly in-situ with high spatial resolution and high integration possibilities.

Below is a short description of the content of each chapter:

- **Chapter 2**: the main theoretical concepts necessary to understand the following experimental work are analyzed. This includes device physics, a description of materials thermal properties and how these change with temperature.
- **Chapter 3** the first generation characterization results are presented and the limitation, together with the ways employed to overcome them are explained. This entails the description of the new design, and all the different elements presented in the secodn generation devices.

- **Chapter 4** reports the fabrication process flow needed to realize the HEMT and the additional sensing structures that are characterized in the following sections. The results of the fabricated devices is also presented.
- **Chapter 5** describes the different electrical characteristics considered to extract the temperature of the substrate, providing experimental data with advantages and limitations for all of them, to motivate the choice made for the full characterization.
- **Chapter 6** aims to gather the experimental results of the characterization both at room and cryogenic temperature, to give an overview of substrate heat dissipation for these devices and structures in different environmental conditions.
- **Chapter 7** draws the relevant conclusion of this work highlighting the main accomplishments and the issues encountered, laying the foundation for future work.

2

Fundamentals

2.1. High electron mobility transistor

As previously mentioned the main objective of this thesis is to study the behavior of high electron mobility transistors. These are field effect transistors realized by a heterostructure of materials with different bandgaps. Since the qubits control and readout uses millimeter wave signals their low noise and high-frequency performance make these devices the ideal candidate to be used in quantum computer applications.

2.1.1. Structure

To ensure good performance of the device the two semiconductor layers must have the largest bandgap difference with the lowest lattice mismatch. For this reason, it is possible to fabricate HEMT in AlGaN/GaN or AlGaAs/GaAs. Nitride ones have much wider bandgaps (from 3.4 to 6.1 eV) which makes them more suitable for power application. Instead, the second class of materials is used in low-power, low-noise applications. The bandgap difference, that can be obtained is limited by the transition of AlGaAs to indirect bandgap [4]. A solution to this problem consists in introducing a lower bandgap material, such as InAs, and being able to engineer the lattice growth to avoid defects coming come lattice mismatch. It is possible to grow a layer of InAlAs over an InP substrate and to create a channel of strained InGaAs under the critical thickness. This allows to avoid dislocation but at the same time enhances the performance of the device. In particular, this allows to obtain a lower effective mass for the channel electrons and a higher bandgap difference (until 0.5 eV). This results in higher carrier concentration, higher velocity saturation, and higher electron mobility[5]. These characteristics are responsible for the low noise and low power performance of the device. The HEMTs studied in this project are based on InP technology. The optimization of the semiconductor stack was performed by E.Cha and the wafer used to fabricate the devices used in this thesis was supplied by an external company, responsible for MBE deposition of thin films. The epitaxial structure is represented in fig.2.3.

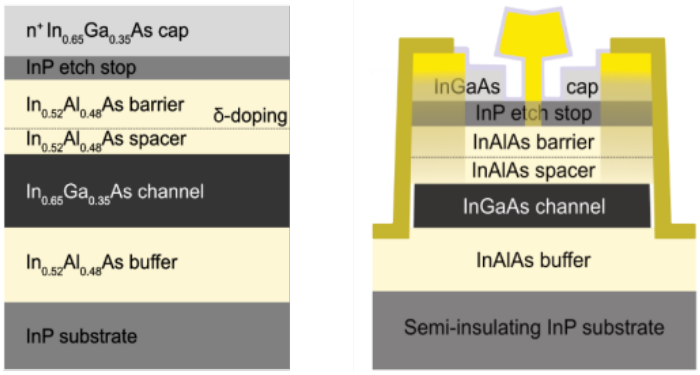


Figure 2.1: HEMT epitaxial structure from wafer (left) to device level (right) [6].

From top to bottom it is possible to identify the following layers:

- **Cap layer:** highly doped InGaAs layer with the aim to reduce the contact resistance between the source and drain metal lines and the semiconductor.
- **InP etch stop:** this allows to increase the selectivity of the cap layer etching and induces passivation of deep-level defects of the layer beneath. These are responsible for unwanted kinks and depletion of the channel carrier concentration which can be therefore eliminated. [7]
- **Barrier layer:** responsible for the rectifying behavior of the gate contact, limiting large currents to flow across and tunneling to the channel. The thickness of this layer is what determines the threshold voltage and the gate control over the channel.
- δ **doping:** the doping is limited to a few nanometers layers of silicon atoms that provide the electrons to the channel.
- **Spacer layer:** this layer keeps the dopants physically separated from the channel and limits the coulomb interaction with the electron flowing, preserving the high mobility of the channel.
- **Channel layer:** the conduction happens in this layer. Here is where the electron concentration is maximum and the mobility is the highest. This guarantees the high performance of the device.
- **Buffer layer:** a pseudomorphic layer is deposited on top of the InP substrate. This allows to obtain an epitaxial quality of the interface to the channel and limits the lattice mismatch through the pseudomorphic layer.

2.1.2. HEMT operation

The structure previously described allows to realize two important technological elements. The first one is to separate physically the dopants from the conduction channel. This is crucial to exploit fully the high mobility of the III-V compound, that makes the channel. The dopants are responsible for the perturbation of the crystalline structure that causes the scattering inside the channel for other field effect transistors. In particular, the delta doping chosen for these devices has the additional advantage to confine the doping in a region of few nanometers. It is important that the donor atoms are also distant from the channel to limit electrical interaction with the electrons which still give rise to scattering. The second one is to exploit the bandgap difference to confine the electrons in a triangular-shaped well. In this way, a 2D electron gas can be formed and the electrons are transferred from the barrier layer to lower energy states present in the channel. If that layer is strongly doped, this allows to obtain a high carrier concentration inside the channel.

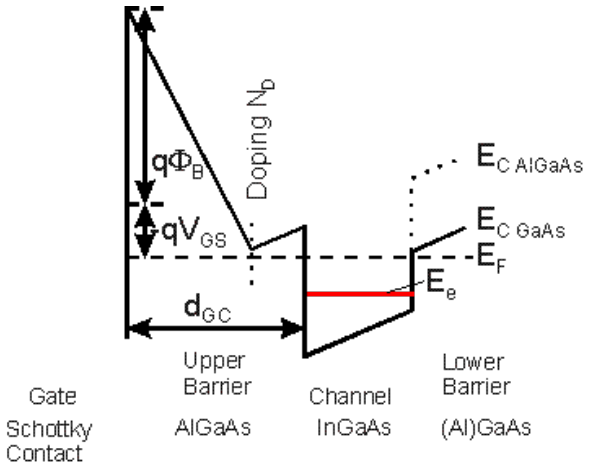


Figure 2.2: Band diagram of III-V HEMT with delta doping [8].

2.1.3. Cryogenic performance

In the framework of quantum readout application, it is also important to understand the performance of the device under cryogenic temperature. In particular, the decrease in temperature induces a reduction in the scattering frequency. It is shown in Fig.2.3 that the mobility increase until the main responsible for collision are the defects of the crystal itself and not anymore the atom thermal agitation. At the same time, it is possible to notice that the carrier concentration is kept almost constant for the wide temperature range considered. Therefore the device can still operate at 4.2K showing no sign of carrier freeze-out.

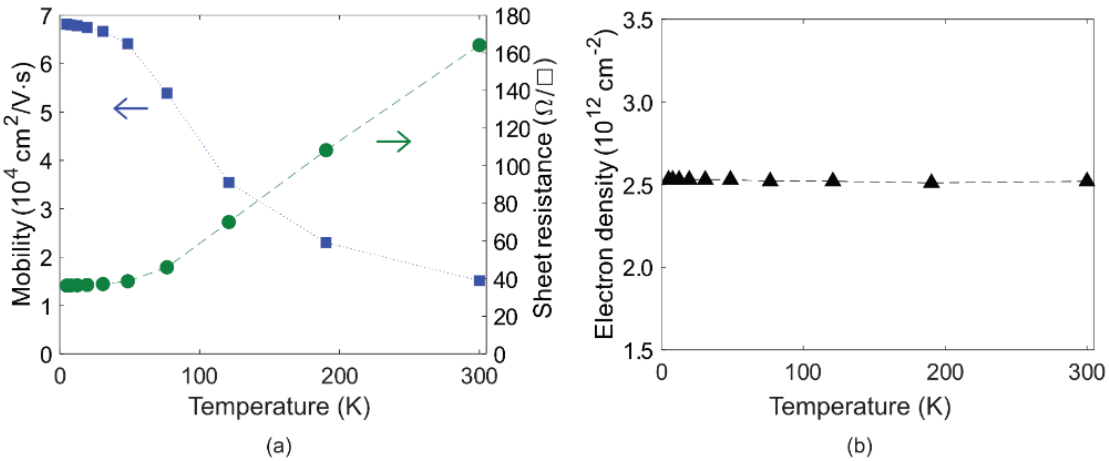


Figure 2.3: (a) Electron mobility (left) and sheet resistance (right) and (b) electron sheet density in the channel as a function of the temperature [6].

2.2. Thermal characteristics

The heat dissipation of the device is also related to the thermal properties that characterize its structure. Understanding the main figures of merit that are relevant in this dissertation is fundamental to describe correctly the phenomena observed. In this section, this topic will be explored, in relation to both performance and sensing points of view.

2.2.1. Thermal conductivity

In the case of the HEMT, the main heat dissipation mechanism is heat transfer. Both irradiation and convection are not relevant in this case. Irradiation dis not contributing because it starts to play a role when the temperature is much higher, although it can have an indirect impact in the cryogenic probestation where the environment heat radiation can limit the cooling of the substrate. The second one is not relevant since the operation conditions are under a high vacuum, which makes it completely negligible. For these reasons the only equation that describes the heat transfer in our case is Fourier's law:

$$q(r,t) = -\kappa(r,T)\Delta T(r,t)$$

where q $(\mathrm{W/m^2})$ is the heat flux, $\kappa(\mathrm{W/mK})$ is the thermal conductivity and ΔT is the temperature gradient. All material properties are entailed in the thermal conductivity. Concerning semiconductor crystal, this means that anisotropy can be measured along different crystal orientations and the temperature has an effect on the magnitude. If in the case of metals the main heat carriers are electrons, phonons play a big role when semiconductors are considered [9]. The scattering of electrons with the crystal can involve dissipative processes that are responsible for heat dissipation, generating phonons. The way the latter travel in the crystal determines how the semiconductor dissipates the heat. It is important to note that these phenomena are temperature-dependent, as shown in Fig.2.5.

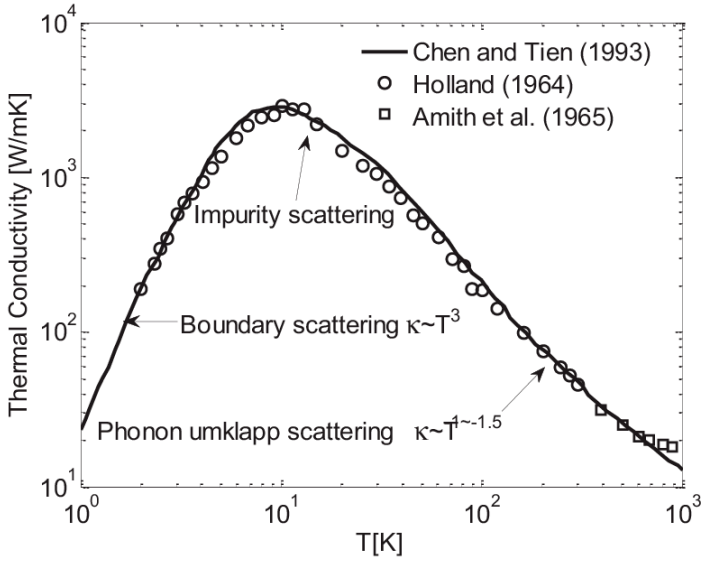


Figure 2.4: Calculated thermal conductivity of GaAs, based on a model that considers phonon dispersion and contributions from different phonon branches (solid line) compared with two sets of experimental data (symbols) [10]

It is possible to identify three main mechanisms that are widely responsible for this dependency:

- **Phonon umklapp scattering**: these are the dissipative phenomena involving three phonons through inelastic scattering, which do not conserve energy. They are linked mainly to the phonon density and therefore the lattice vibration, that perturbs the field inside the crystal.
- **Impurity scattering**: when the crystal vibrations are drastically reduced due to low temperature, the biggest perturbation to the crystal is represented by the impurities. These are not any more related to thermal agitation but are fixed modifications of the crystal structure which are responsible for scattering.
- **Boundary scattering**: when the phonons in the crystal are low in energy and have large wavelengths the boundaries start to dominate the dissipation mechanism.

These three processes are not the only factors to determine thermal conductivity. The interface between materials plays also a role. The phonon diffusion is impacted by the acoustic mismatch between materials and this can lead to temperature drop across interface not only in liquid to solid [11] but also to solid-to-solid ones[12]. There is experimental evidence that this effect shows strong temperature dependence and at low temperature can become the dominant factor in multilayered structure [13][14][15]. Another important element of this discussion is the effect of thickness in thermal transport and how this can change the thermal response of the structure. The thermal conductivity can decrease if the layers becomes thin enough, as shown by *Mei et Al.* [16] and *Kim et Al.* [17]. There is no clear and unique explanation for this but is evident also in superlattices of many materials [18].

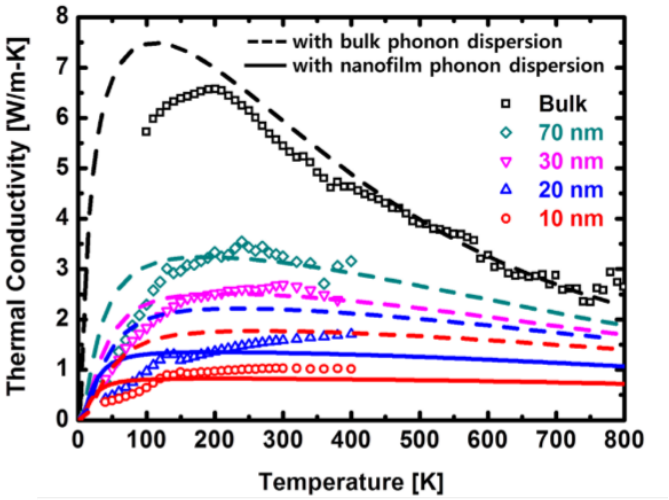


Figure 2.5: Thermal conductivity of $In_{0.53}Ga_{0.47}As$ at $300\,\mathrm{K}$ versus thickness [17].

Concerning the III-V compounds used in this thesis, there is no complete agreement in the literature regarding thermal properties, especially for InAlAs. Cryogenic characterization of thermal conductivity is not available to the author's knowledge of both materials. A convergence around $4.8\,\mathrm{W/mK}$ for InGaAs [15][19][18] and $2.7\,\mathrm{W/mK}$ [16] [18][20] for InAlAs at room temperature can be found, although some authors provide much lower values for InAlAs, reaching $1\,\mathrm{W/mK}$ [15]. The semiconductor stack used to realize the HEMT for this thesis shows all the characteristics above mentioned: multiple layers with many boundaries separating the channel from the substrate,very low thickness (from a few to tens of nanometers) operated at really low temperature. All of these together make the correct assessment of the self-heating in these devices complex and require experimental techniques to gather information about heat dissipation. For this reason, the purpose of this thesis is to overcome the theoretical struggle to correctly parametrize these types of complex structures and provide a comprehensive method to investigate the temperature of operating devices.

2.2.2. Thermal characterization techniques

In this section the collection of state-of-art thermal characterization techniques is presented to show how this project helps to overcome some limitations, offering useful benefits for specific applications. Conventional thermometry is not sufficient anymore to gather specific data regarding temperature profiles when the spatial resolution required is decreased to the micron range. For these reasons numerous non-contact techniques have been developed, that use light to extract temperature data.

Infrared thermography

One of the simplest techniques to use is to measure the infrared emission spectra of the surface of the device. The black body emission equation relates the temperature of the emitting device with the radiation emitted. In practice, no material has an ideal response, but instead the material properties affect the emission through their specific emissivity. The

radiation is characterized by wavelength and intensity. The relationship between them can be easily obtained. The wavelength of maximum emission has an inverse relation with the temperature and to measure objects in the range of $300\,\mathrm{K}$ the most appropriate wavelength is around $10\,\mu\mathrm{m}$, i.e. the infrared region [21]. Therefore the IR emission can be converted into a temperature signal. Different sensors can be employed to measure the radiation, from a CCD camera to microbolometers. Spatial resolution and accuracy depend on the camera used to take the measurements. In the case of CCD, it can be cooled down cryogenically to remove the thermal noise that limits the temperature resolution [22]. The result is in any case an actual image of the device with false colors, corresponding to different temperatures. Spatial resolution less than 3-$10\,\mu\mathrm{m}$ can be achieved with this method and temperature resolution of $1\,\mathrm{K}$ is typically available, with the possibility to reach $20\,\mathrm{mK}$ if it is a perfect black body. For the interest of this research, the main limiting factor is the spatial resolution and the possibility to integrate this technique for cryogenic temperature. Sensor operating range and sensitivity at these conditions are not sufficient to provide reliable data. Black body emission at $4\,\mathrm{K}$ is too low (at least two orders of magnitude less [22]) to be sensed with an IR camera.

Thermoreflectance thermal imaging

Another non-contact technique is thermoreflectance thermal imaging (TTI) which provides temperature contrast by analyzing the optical reflectance of the inspected surface. Amplitude, phase, and polarization carry information about the thermomechanical response of the device under test. A temperature variation ΔT creates a reflectivity variation ΔR :

$$\frac{\Delta R}{R} = \frac{1}{R}\frac{\delta R}{\delta T}\Delta T = \kappa \Delta T$$

where κ is the thermoreflectance coefficient. This factor is strongly dependent on the material and on the incoming light wavelength [23]. This means that calibration is necessary to extract temperature values from the measurements. This method allows to use light with much smaller wavelengths compared to infrared thermography, with a consistent improvement in resolution [24].

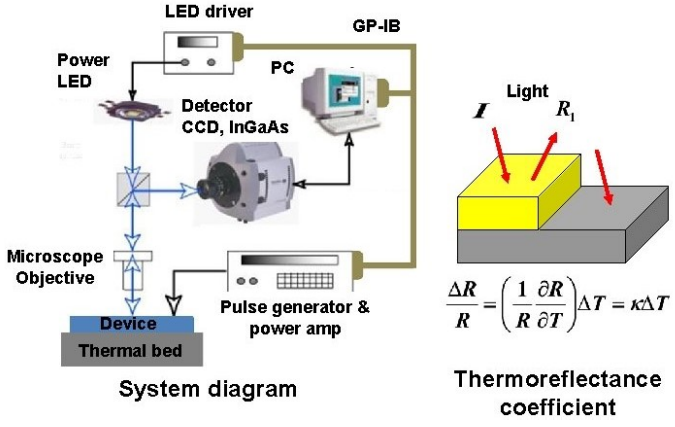


Figure 2.6: Thermoreflectance thermal imaging setup scheme [25]

The usual setup is composed of a led light, whose intensity can be modulated and polarized, and a CCD camera that can sense the intensity variation coming from the reflection. The spatial resolution can reach 0.3-0.5 µm whereas resolution of 0.01 K are possible. Nevertheless, this technique is not easily integrable inside a cryostat due to its high volume and it requires a special setup to operate also for cryogenic measurements [26].

Raman thermal spectroscopy

Another technique that uses the optical response of the material to gather information about its temperature is the Raman thermal spectroscopy. Raman spectroscopy technique is a common method to study chemical compounds and characterize chemical bonding but it can be also used to determine the temperature. There are two methods to determine the temperature. The first one relies on the peak position of the Stokes signal. The latter shifts with the temperature due to a change in the bond lengths among atoms and can be related to a temperature change value. The second method relates the intensity of the Stokes and anti-Stokes resonance peaks to the Boltzmann distribution. In this way, the temperature can be easily related to their ratio [27]. In both cases, a laser source is needed to stimulate the Raman scattering. An optical sensor is needed to detect the photons emitted by the substrate and its resolution and accuracy are responsible for the sensitivity of the measurement setup. In the case of the Stokes and anti-Stokes ratio method, the sensor should provide high performances both at higher and lower wavelengths than the emitting laser. Another important aspect is that both techniques interact not only with the surface but with a small volume of material beneath. Lateral resolution can reach values less than 0.5 µm and vertical resolution can be more challenging (even more for transparent material) and be limited to few µms [28]. Also in this case the integration with a cryogenic setup can be difficult and need a specific arrangement.

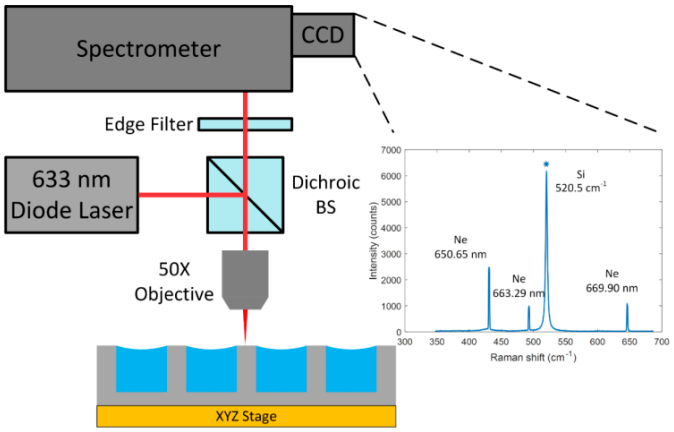


Figure 2.7: Raman setup scheme [29]

Scanning thermal microscopy

To achieve the best spatial resolution AFM techniques can be tailored to sense surface temperature in addition to topography. Most often temperature sensitive resistor at the end of the tip are used [30]. Sensing the change in the resistance value is is possible to obtain temperature maps with much higher resolution than other techniques (around 10 nm).

On the other hand, this comes with other difficulties. The relation between the actual signal measured and the investigated parameter is not simple, due to the complex interaction between the tip and the sample. Topographic artifacts, wear, and tear, can lead to inaccurate results if the thermal exchange is assumed by the heat transfer model. This means that effective calibration techniques are required to obtain reliable results[31]. There are numerous thermal methods developed in the years that use different thermosensitive phenomena: change in electrical resistance or thermovoltage method are the most used [32]. Thermovoltage-based methods are realized using a junction between two electrodes. Usually, this is established between the tip and the sample and therefore requires a conducting sample or a metallic film covering the sample. Resistance methods exploit metallic or doped silicon probes and are used in passive mode for thermometry purposes. This means that a small current is passed through the probes to sense the resistance value but at the same time to limit the self-heating of the device the magnitude is small. The voltage applied can be a combination of AC and DC components that can be used together with a lock-in amplifier to increase accuracy and reduce noise impact on the measurement. This technique is also used to perform cryogenic measurements but requires a specific instrument built exactly for this purpose. The SThM needs to be mounted inside a high vacuum chamber connected with a cryogenic cooler.

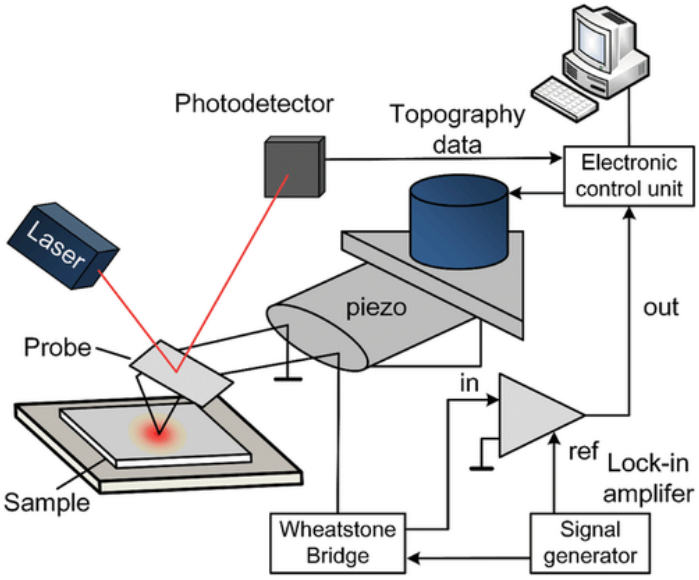


Figure 2.8: SThM setup scheme [31]

Gate resistance thermometry

All the previous techniques allow to obtain thermal maps on various devices exploiting different physical phenomena. In any case, metal is always difficult to characterize due to high reflectivity and the absence of crystal structure in most cases. In the particular framework of this project, the metal gate covers the region where the actual conduction happens. Therefore is more difficult to obtain direct observations of the channel temperature. To obtain complementary information with respect to the previous techniques is possible to use

the metal gate as a temperature sensor itself. This technique is called gate resistance thermometry and exploits the temperature-dependent resistance of the gate to obtain the value of the temperature of the beneath channel. The result is the mean temperature of the active region if thermal equilibrium between the channel and the gate is assumed. This is true if the TBR (thermal boundary resistance) is considered negligible. The latter assumption holds in most cases, but it shows to have a bigger impact at low temperatures [14]. This technique is widely used to assess temperature in power devices that work with much higher voltages. The optimal configuration exploits 4 probes measurements to reduce the impact of access resistances and improve accuracy. In this way is possible to bias the device and at the same time measure the resistance value of the gate.

This project aims to assess in-situ self-heating and heat propagation on the substrate. This requires high spatial resolution and thermal sensitivity. All the techniques above mentioned require special instrumentation to be operated. For this reason, a more accessible sensing method is evaluated, that can provide easy integration and versatility in the operating environment. For this reason, local integration of the sensing device is studied to include the sensing element directly during the fabrication process. Compared to other thermography techniques this would simplify the measurement setup at the cost of data points available. In the following chapter, the solution is discussed in greater detail to explain the solution proposed.

2.3. HEMT temperature behavior

Another important aspect to study self-heating is how the HEMT changes its characteristics with respect to temperature. Two different behaviors are observed depending on the bias point. The measured transcharacteristics are displayed in Fig. 2.9.

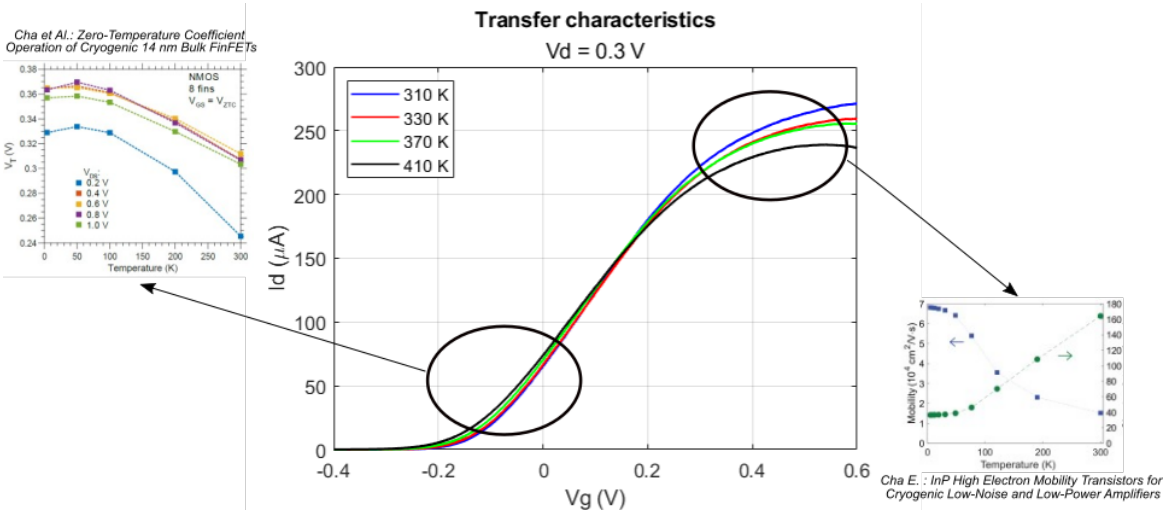


Figure 2.9: HEMT transcharacteristics at different temperature values ($300\,\mathrm{K}$, $330\,\mathrm{K}$,$370\,\mathrm{K}$, $410\,\mathrm{K}$)

Deep in the linear region (i.e. for high V_g) the current is decreasing with respect to temperature increase. The reason for that is the change in mobility. The scattering rate of the electrons is higher and this limits the current flowing in the channel. The electrical

mobility in InAlAs is very high compared to other semiconductors but is strongly temperature-dependent, affecting the performance of the device. In the quadratic region (i.e. for lower V_g) the opposite happens and the current increase with the temperature. This can be linked to a change in V_{th} of the device. This variation is observed among many transconductance devices. MOSFET on Silicon and FDSOI shows the same trend in threshold voltage. The change in the Fermi potential of the channel is responsible for this kind of phenomenon. At first approximation the relation for the MOSFET can be expressed as follows:

$$\phi_f = U_t ln \frac{N_a}{n_i}$$

where ϕ_f is the Fermi potential, N_a is the dopant concentration anf n_i is the intrinsic concentration of the substrate. These two phenomena exist together but are more or less evident in different operating regions. For this reason, there is a bias point where the temperature dependence is negligible and this is called ZTC (zero temperature coefficient). Another important aspect to consider is the behavior in the weak inversion region (i.e for V_g under the threshold voltage). A useful parameter to characterize device performances in this region is the subthreshold swing which is defined as follows:

$$SS = \frac{dV_g}{d(log_{10} I_d)} = m \frac{kT}{q} ln10$$

where V_g is the gate voltage, I_d is the drain current and m is the body factor, which takes into account the control of the gate to the channel. This is strongly temperature dependent and this affects very much the performance of the device. This FOM is an indicator of the slope of the logarithmic plot in the subthreshold region. In Fig. 2.10 it is possible to see how the increase of the temperature leads to an increase in the current and to a higher off-current of the overall device.

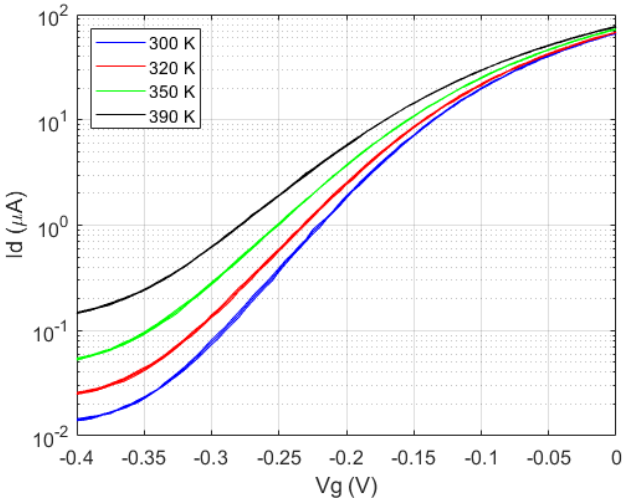


Figure 2.10: HEMT log-transcharacteristics at different temperature values (300 K, 320 K ,350 K, 390 K)

3

I generation devices

A previous attempt was made to measure the temperature of the substrate. For this reason, a first-generation sensing structure was realized. In this chapter, the analysis and conclusion coming from this device generation are presented. From the results and understanding gathered from these measurements, a new generation of devices was developed.

3.1. Measurement method

The structure was composed of a wider HEMT device, that for this thesis will be called the power device. This is the one to be characterized. A high current is passed through to induce self-heating in a controlled manner. Through bias parameters (i.e. V_g and V_d) the power dissipated from the device varies and it is possible to estimate the substrate temperature thanks to an array of HEMTS with a smaller width. These are called sensing devices. In Fig.3.1 the latter structure is shown.

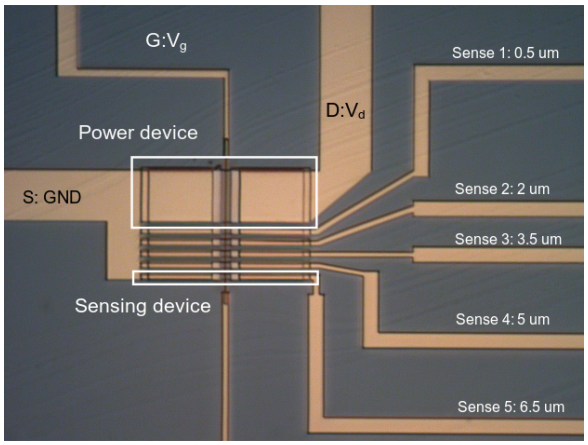


Figure 3.1: Optical microscope image of first generation sensing structure

To extract more information from the structure, multiple sensing devices are fabricated at different distances from the power device. In this way, it is possible to understand information about the heat spread across the sample, in addition to the substrate thermal

properties. The spacing between two adjacent devices is 1.5 µm starting at 0.5 µm from the power device. The total number of devices is five, being able to probe until 6.5 µm distance from the heating source. The width of the power device is 7 µm whereas the sensing device is just 1 µm wide. Both devices are 200 nm. This means that the measured temperature is the mean value across an area of 0.2 µm^2. As it is possible to observe, both source and gate are shared among all devices, power, and sensing. This allows using only 4 probes to bias the power and one sensing device. One probe is used for the common source, one for the gate bias, one for the power device drain, and the last one is used for the drain of the selected sensing device.

To obtain information about substrate temperature the following operations are needed:

- Common source is connected to ground
- Sensing drain bias is fixed
- Common gate bias is fixed
- Power drain bias is swept across a voltage range

With this configuration is possible to measure temperature dissipation at different power levels, achieved by different power drain voltage, which is the only variable parameter.

3.2. Calibration curves

The definition of the bias point of the sensing device is not a trivial question. Two main factors must be considered: sensitivity and self-heating of the sensing device itself. Ideally, an operation point with maximum sensitivity and minimum power dissipation (i.e sensing drain voltage) would be the best condition where to operate the sensing device. In Fig. 3.2 transfer characteristics of a sensing device are shown for different temperatures and different drain voltages.

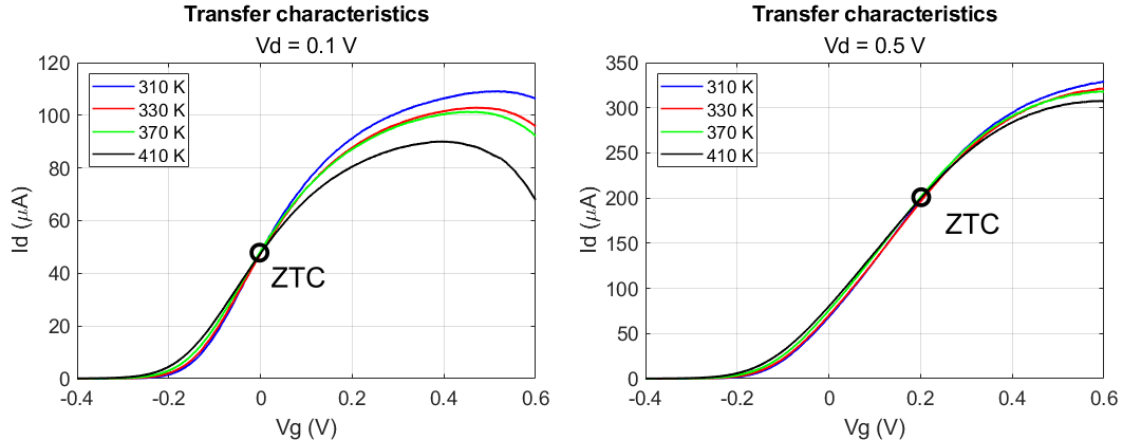


Figure 3.2: Transfer characteristics of sensing HEMT at different drain voltages for different temperatures

As previously explained the HEMT shows a positive and a negative temperature dependence changing the bias of the device. In Fig.3.2 the zero temperature coefficient (ZTC) is also highlighted. It is possible to see that this is shifting to higher gate voltages, while we

are increasing the drain bias. To limit the power dissipation of the sensing device it is important to use the HEMT at gate voltages lower than the ZTC, but at the same time to achieve high sensitivity to detect small temperature variations the device must be operated far away from this point without turning off the transistor. From these measurements, it is possible to extract the current change for different V_g and V_d to assess the temperature coefficient.

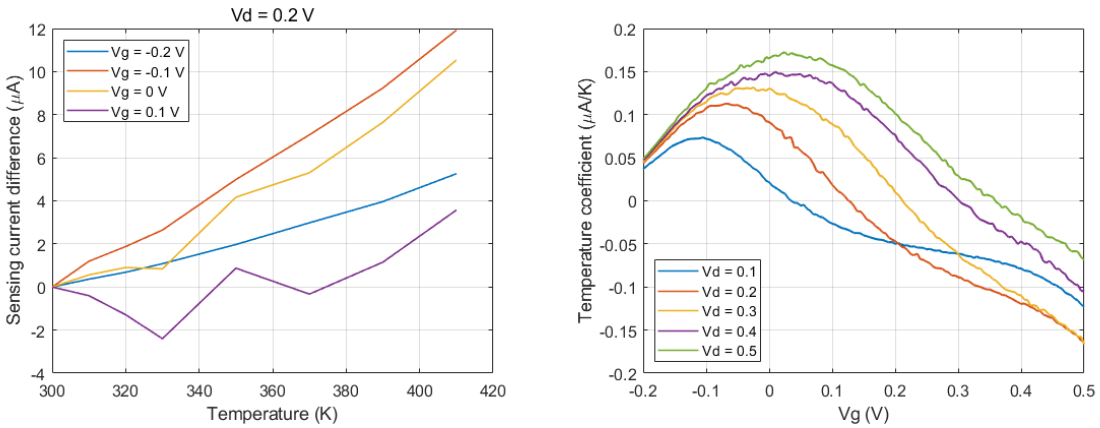


Figure 3.3: (a) Current variation for different temperatures at different operating points. (b) Linear temperature coefficient extrapolated from experimental data for different drain bias

In Fig.3.3 an extract of the experimental data is shown. It is possible to see that both the linearity and the magnitude of the sensitivity are changing along with the operating point. In addition to this, it is important to note that with higher bias the measurements are noisier than at lower values of V_g. The temperature coefficient can be extracted, performing a linear fit of current variation with respect to temperature. The angular coefficient can be defined as the temperature sensitivity of that particular device at that particular operating point. Doing a more comprehensive analysis the current temperature sensitivity shows a maximum before inverting its polarity. The gate voltage corresponding to this value and the actual maximum increase together with the drain voltage. This corresponds to the shift in ZTC that was possible to observe before. In Fig. 3.4a the sensitivity is shown together with the standard deviation of the linear fit. It can be seen that for higher V_g the dependence on temperature loses linearity, and the fit is no longer accurate. This can be attributed to the non-linearity of the threshold shift with temperature which is more relevant for these operation points. In conclusion, if a higher sensitivity is desired, the power dissipated from the same device needs to be higher and a lower degree of linearity needs to be expected. For these reasons, the selected operation point would correspond to the maximum for drain voltage equals to $0.3\,\mathrm{V}$, i.e $V_g = 0\,\mathrm{V}$.

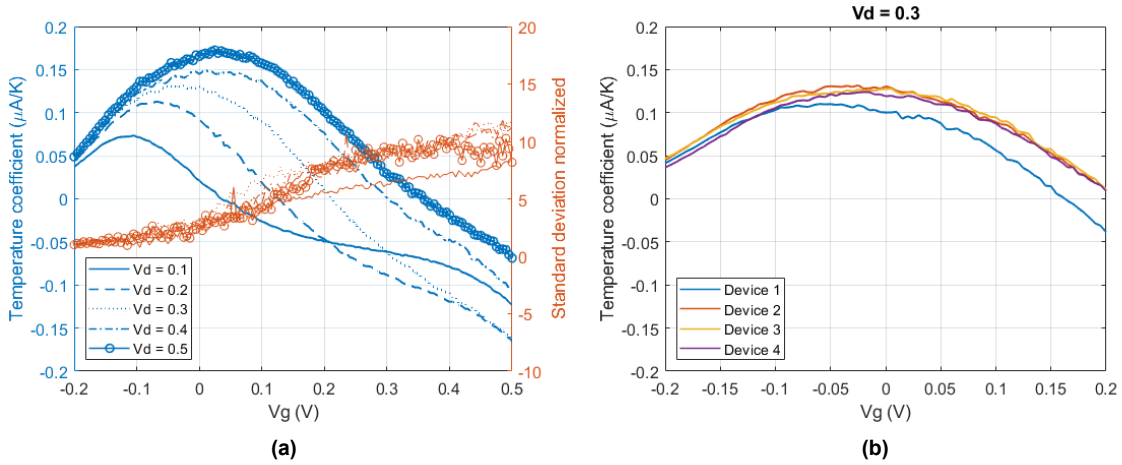


Figure 3.4: (a) Temperature sensitivity and standard deviation of the linear fit. (b) Temperature sensitivity for selected bias points of different devices

The different device of the sensing structure differs slightly due to process variation. E-beam patterning and etching are affected by the different environments of a single device. If the devices in the middle are exposed to the same surrounding, the top and bottom are processed under slightly different conditions. This can give rise not only to different transfer characteristics but also to different temperature sensitivity. In Fig. 3.4b it is possible to notice that this intrinsic variability increases with higher gate voltages, but at the selected bias point its maximum change is limited to around 20%. For this reason, a single calibration is necessary for each device to obtain reliable temperature values.

3.3. Parasitic effects

To assess correctly the operation of the sensing structure is important to check that the two devices operating, one sensing and one power, are not interfering with each other. In this perspective, a detailed analysis of the effect of common source contact is presented here. It is important to note that the access resistances in this structure are not completely negligible, due to the presence of the probes and the lines connecting the actual source of every device with the grounded pad. The voltage of the common source contact is monitored during the switching of the power device through an additional probe used as a voltmeter.

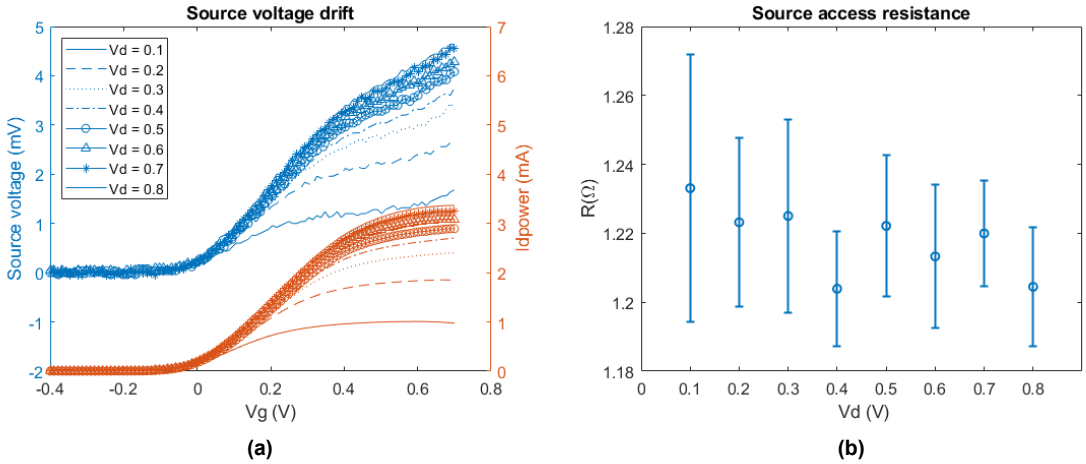


Figure 3.5: (a) source voltage drift and power drain current of the same device. (b) Access resistance estimation for different drain voltage

In Fig. 3.5a the difference in the source voltage is shown together with the current from the power drain that flows through it. The difference reaches the maximum at $4.8\,\mathrm{mV}$ which can be negligible for the transfer characteristics. However, this is no longer true for the sensing device. Since the latter is working at a fixed operating point the result is that a small variation can influence the temperature measurement. To exclude this from the data, the access resistance is calculated. The source voltage continues to increase steeply even after the drain current saturates. This is related to the effect of gate leakage which adds to the total current flowing to the source. If this is also taken into account is possible to define the access resistance as the ratio between the source voltage and the source current. In Fig. 3.5b the results for different drain voltages show consistency in resistance value, supporting the hypothesis that the cause is the access resistance. The value considered is obtained as the mean of the displayed values$1.22\,\Omega$. To correctly assess the impact on the sensing current is necessary to obtain the source transconductance. In Fig. 3.6 the values of the extracted transconductance at $V_g = 0\,\mathrm{V}$ are shown. With increasing drain voltage the maximum absolute transconductance decreases. Biasing the sensing device at a higher gate bias would also increase the effect on the sensing current. In addition to this, it is possible to note that the gate voltage corresponding to the maximum is decreasing.

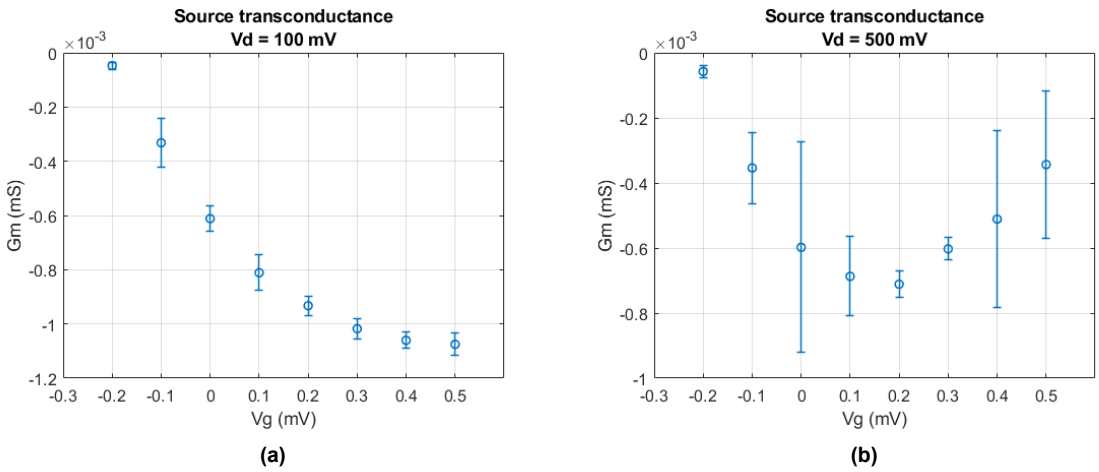


Figure 3.6: Source transconductance for 100 mV and 500 mV drain voltage

All these considerations allow one to counterbalance these effects considering that the drain current of the power device induces a change in the sensing current corresponding to the product between the current magnitude and the gain. The latter is simply obtained as the product between access resistance R_s and the source transconductance G_{ms}. This additional contribution can be removed from the measurement to eliminate this effect and obtain the correct measurement. In Fig. 3.7 the access resistance repercussion are evident and make a difference of more than 60% for higher power dissipation. For this reason, it is crucial to take this into account when obtaining temperature values from the sensing current.

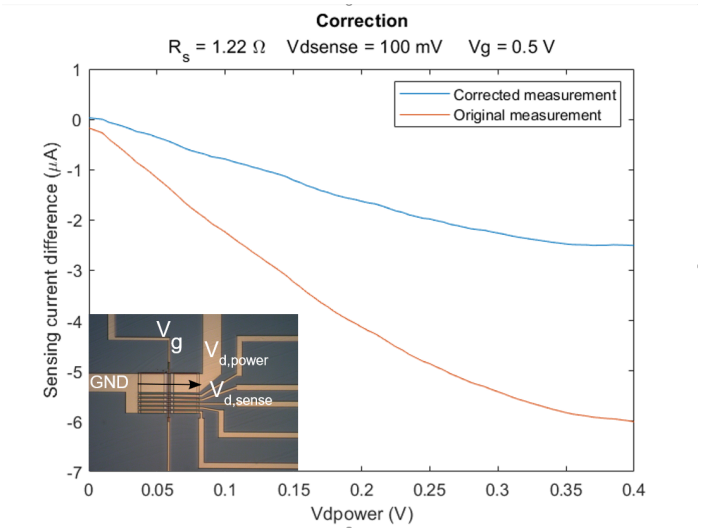


Figure 3.7: Sensing current with and without correction applied for common source effect

3.4. Preliminary results

These previous considerations allow to consider different aspects of the sensing structure and to understand how to operate correctly the measurement. The latter follows the description in Section 3.1. In this way, the current of the sensing device is measured, and from the calibration curves with the help of the correction, it is possible to estimate the temperature of the substrate. The results are presented in Fig. 3.8.

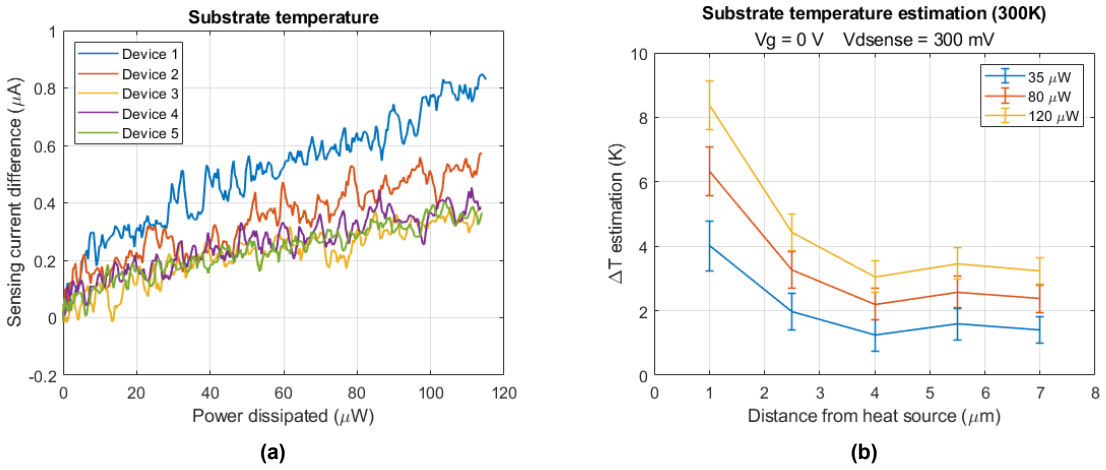


Figure 3.8: Sensing current variation with respect to power dissipated (a) and substrate temperature estimation with respect to distance from the power device for three different power levels(b). Devices are numerated from the closest one to the most distant

From these measurements, it is possible to observe an initial abrupt jump in the temperature, and only after that, a linear trend is established. This effect is most evident for the device closest to the heating source, i.e. the power device. The trend agrees with other measurements reported in the literature [33] [34] although heating is two to three times higher than CMOS technology on silicon substrates, considering the power levels that are possible to reach. At this temperature range as shown also by Choi[14] in almost identical devices, the self-heating has not such a huge impact and the trend stays linear with respect to power at $300\,\mathrm{K}$. Deviations from linearity are observed only under $60\,\mathrm{K}$, probably due to temperature-dependent thermal properties and boundary resistance. Therefore it is not possible to ensure that this is an actual thermal signal. Residual crosstalk between devices limits the possibility of extrapolating only thermal effects from the sensing device current. Even correcting for the source voltage shift is limited by the estimation of the parameters needed. This can entail intrinsic errors, because the measurement is not direct anymore, and estimating correctly the operating point can induce additional uncertainties.

3.5. New mask design

This design was not ideal for sensing the temperature of the substrate. For this reason, a new mask design was necessary to fabricate new devices, that can overcome the main limits that this first important characterization highlighted. The main limitations that arose are:

- **4 probes measurements**: the number of probes available to characterize the devices was only four due to the experimental setup. This caused suboptimal design choices.
- **Common source**: the source is shared across all sensing devices and power devices, causing crosstalk between them, for high power current values.
- **Common gate**: the gate is shared also among all devices and this defines the gate bias both for power and sensing devices.

Due to these elements, the possibilities to design experiment is limited to set low power dissipation and optimal sensitivity or high power dissipation but not useful sensitivity. In addition to that other possible temperature-dependent characteristics can be used (e.g sub-threshold swing and threshold voltage) with an additional degree of freedom as the gate voltage.

3.5.1. Sensing structure

To do so, a modified sensing structure has been designed to increase the isolation of the single device. Additional pads for the gate and source of the sensing devices have been added. To increase the spatial resolution the length of the sensing device has been reduced to 150 nm and the width remained fixed to 1 µm. The number of sensing devices was increased to six, and spread not uniformly to optimize density with respect to temperature gradient.

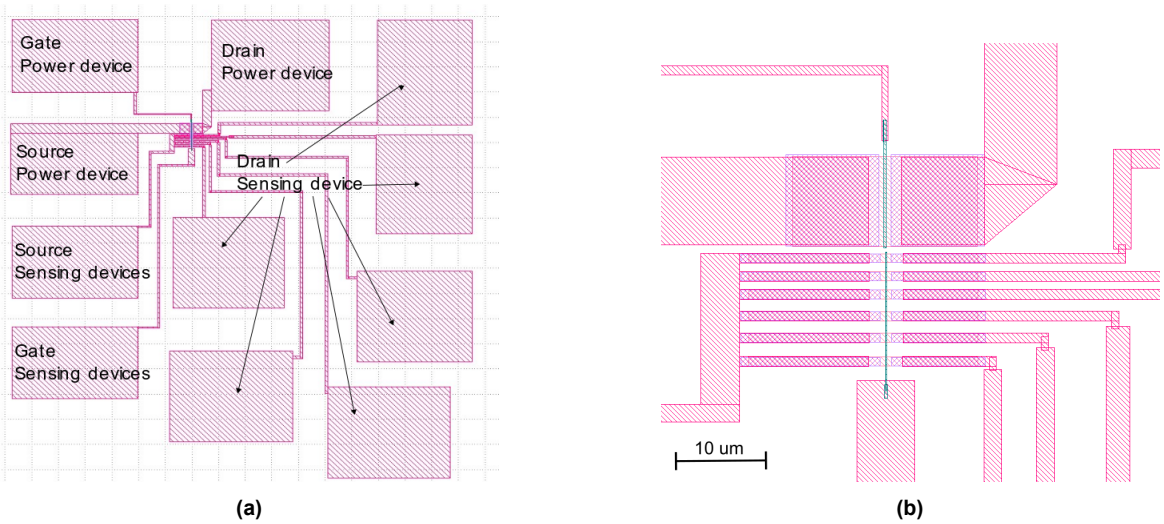


Figure 3.9: Layout of new sensing structure with pads (a) and with only active parts (b)

In Fig. 3.9 the new layout is presented together with a closer look only at the sensitive area. The complete design occupies an area of 570 µmx570 µm. The 4 pads to the right are

equally spaced with a 100 µm pitch to allow a multiprobe wedge to access the four metal covered area at the same time.

In Tab.3.1 the distances from the power HEMT are reported for the six devices. For the first three devices, the minimum distance is used, whereas for the other ones it has been relaxed, since the expected variation of temperature will be lower.

Device number	1	2	3	4	5	6
Distance (µm)	0.75	2.75	4.75	7.15	9.5	12.2

Table 3.1: Layout distances of different devices in the HEMT sensing structure

Another objective of this thesis was to understand heat spreading in the substrate around the device to estimate the influence of one single HEMT on close temperature-sensitive devices (e.g. qubits) to better position them in further architecture. For this reason, multiple copies are designed in which the sensing structure is shifted laterally by a fixed value. The exact location is presented in Tab. 3.2. It is, therefore, possible to extract a 2D heatmap of the substrate. The center device is aligned with the drain border of the gate where the highest heating is expected. It is important to highlight that for each lateral position a different device is designed to be able to characterize them. Therefore, the complete set of sensing structures is made up of 9 devices similar to the one in Fig. 3.9. In addition to that, the impact of the gate length on self-heating is investigated. Three gate lengths for the power device are considered: 150 nm, 250 nm and, 400 nm. The array cited above is replicated for these different power device gate lengths. Concerning the gate width for all power devices, it has been set to 10 µm.

Device label	L4	L3	L2	L1	C	R1	R2	R3	R4
Lateral distance (µm)	-2.12	-1.12	-0.42	-0.2	0	0.2	0.42	1.12	2.12

Table 3.2: Lateral distance from the center position

3.5.2. Single point measurement

The sensing structure is composed not only of the active area of the gate but also of the metal interconnections. Although this effect can be neglected at first instance, this may alter the temperature distribution. Therefore new structures composed of only one sensing device are designed to assess the contribution of the metal to substrate heat dissipation. To recall, the realization of a single device for each sensing device would imply fabricating 54 devices. To find a compromise between the area on the chip and the completeness of the data set, only two lateral positions, the central (C) and rightmost (R4), but all vertical positions for each one have been considered. In Fig. 3.10 the layout of both center and lateral positions is presented.

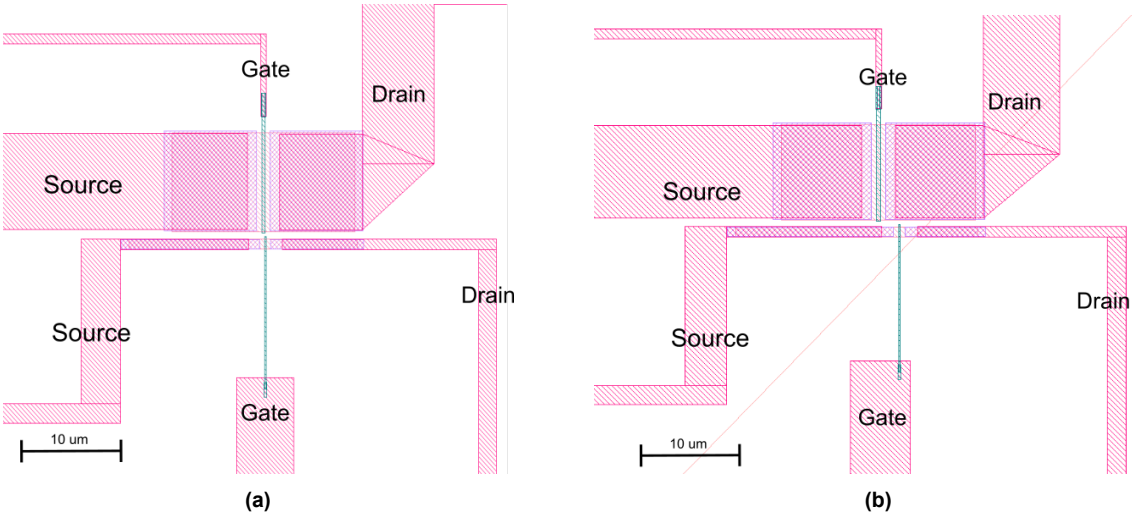


Figure 3.10: Layout of new single point measurement on centered position (a) and lateral position (b)

3.5.3. Drain to gate variable distance

Another interesting feature to investigate is the effect of the gate-to-drain distance on self-heating. In power applications HEMT usually the drain and source contact are not symmetric with respect to the gate. Instead, the drain is located more distant. This helps to limit capacitance values that can lower the cutoff frequency, and the noise performance and to control the electric field in the channel [35]. Therefore modulated drain to gate distance power devices are studied to understand better the relationship with the self-heating through electric field modulation in the channel. The standard distance used for all the devices previously mentioned is $1.6\,\mu$m for both drain- and source-to-gate distance. In Tab 3.3 the effective distances are presented for the four different versions of the power devices.

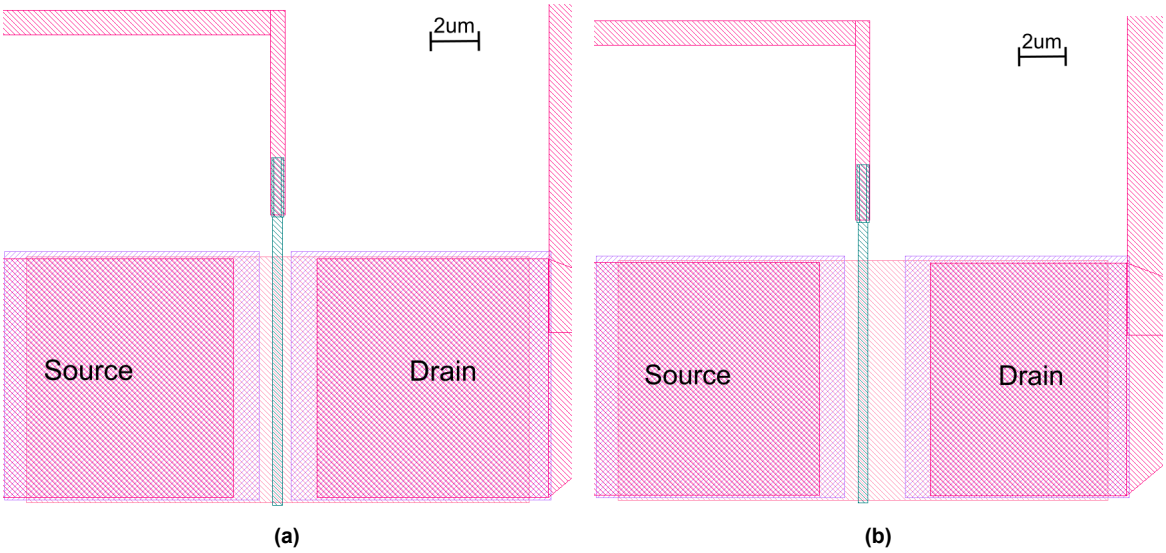


Figure 3.11: Layout of XS power device (a) and XL power device (b)

XS	M	L	XL
1.4 µm	1.8 µm	2 µm	2.6 µm

Table 3.3: Gate-to-drain distance

3.5.4. Schottky diodes

To improve the accuracy and reliability of the results using another device that relies on different physics principles is a suitable option. To maintain the same simplicity of integration and to use the established processes, Schottky diodes were chosen. They are realized as leaky gates to source junctions. Compared to MOSFET technology, the gate is a Schottky junction with higher gate leakage. This allows to easily integrate diodes in the design removing the drain contact. In this way, it is possible to obtain the following main benefits:

- simpler device with rich literature as a temperature sensor
- simpler characterization method with only 5 probes
- easy integration with well-developed process flow

In Fig. 3.12 the layout of a single diode device is presented. The green mask is the metal gate and the light red is the mesa of III-V compounds. Due to anisotropic etching with respect to crystal orientation, the diode junction is oriented vertically. Otherwise, the mesa structure cannot guarantee good enough performance due to the extreme thinning of the bottom layers. In addition to that, keeping a similar layout of the complete sensing structure ensures that different methods can be compared with more accuracy. The active area of both HEMT and Schottky devices is the same, given the same length and width. Metal connections to the gate are realized with higher width to limit problems in the liftoff processing.

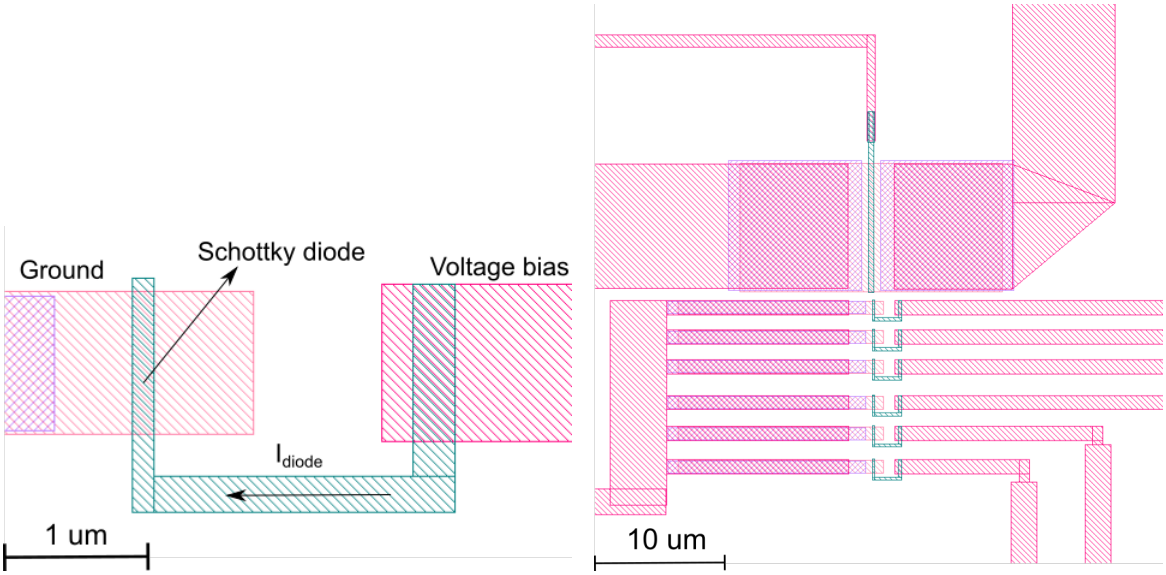


Figure 3.12: Layout of Schottky diode (a) and sensing structure together with diode array (b)

Regarding the sensing structure, the multiple versions are the same as the one described in Section 3.5.1, only with a different sensing device. This includes different positions and gate lengths. Given the additional constraints coming from the bigger vertical footprint of the new device, the vertical dimension has been modified to ensure that critical dimensions are respected. The vertical displacements from the power devices, in this case, are the ones depicted in Tab. 3.4.

Device number	1	2	3	4	5	6
Distance (µm)	0.75	3.05	5.35	8.15	10.55	13.15

Table 3.4: Layout distances of different devices in the diode sensing structure

4

Device fabrication

4.1. Fabrication techniques

In this section, the instrumentation used to fabricate the devices are briefly explained with the specification of the tools used in the case of this thesis. Basic principles and motivation of the latter are also shortly explained to give a clear overview of the process flow definition.

Electron beam lithography

There are multiple ways to transfer a pattern to the wafer surface. A polymer layer called photoresist is normally exposed to photons or particles changing its properties. Therefore it is possible to selectively eliminate part of the photoresist to let the wafer surface be exposed to additional processes, while the rest of the substrate is protected. Electron beam lithography makes use of a beam of electrons to modify the photoresist. The beam is generated from a source and then focused by multiple magnetic lenses. These are able to modify the beam shape and trajectory. Compared to photons, the electron can show orders of magnitude smaller wavelength (0.5 - 0.1 Å) compared to advanced photolithography techniques such as DUV ($193\,$nm) and EUV ($13.5\,$nm). This allows EBL to reach a much higher spatial resolution. In addition to that, traditional photolithography needs a mask to block the incoming light and transfer the correct pattern. This allows to realize a much faster process since the whole wafer or smaller parts can be exposed simultaneously but this requires the fabrication of a mask, which is also time-consuming and costly. On the other hand, EBL versatility and resolution come at the cost of a much more time-consuming process. There are two main ways to expose the photoresist: raster scan and vector scan. With the first one, the e-beam is moved across the entire wafer and it is shut on and off according to the required exposure layout, whereas the second exposes only the required region and jumps from one feature to the other. In case of quicker but less reliable pattern exposure, vector one is the preferred solution. In the case accuracy is the priority, the raster scan is the most used. For the purpose of this project, the use of EBL is motivated by smaller features that require a higher degree of accuracy in terms of alignment and patterning. In addition to that, the sensing structure has a dense structure that requires precise positioning. In this thesis, the EBL tool of the BRNC cleanroom has been used. The model is Vistec EBPG 5200+ and can reach sub-8 nm resolution.

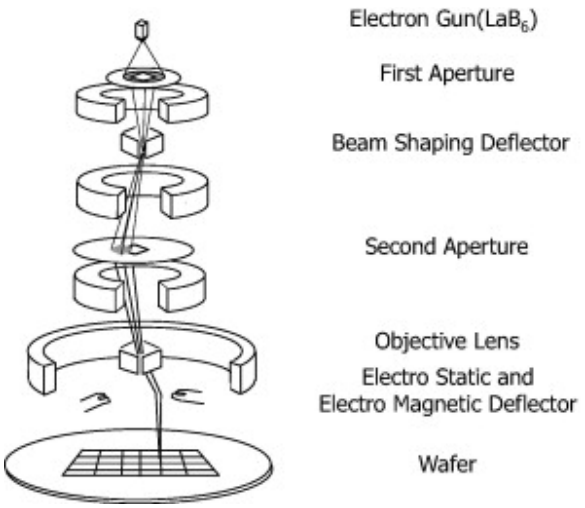


Figure 4.1: E-beam lithography schematics [36].

Lift-off

To deposit the metal stacks that form the contacts and the metal lines, one of the main techniques is the lift-off. The latter is realized using two different photoresists with different properties. The first one is normally the thicker and the one more susceptible to the developer's solution, whereas the second one is thinner and more reluctant to be etched by the developer. This implies that when fully processed, the feature in the bottom layer is larger than the one on top.

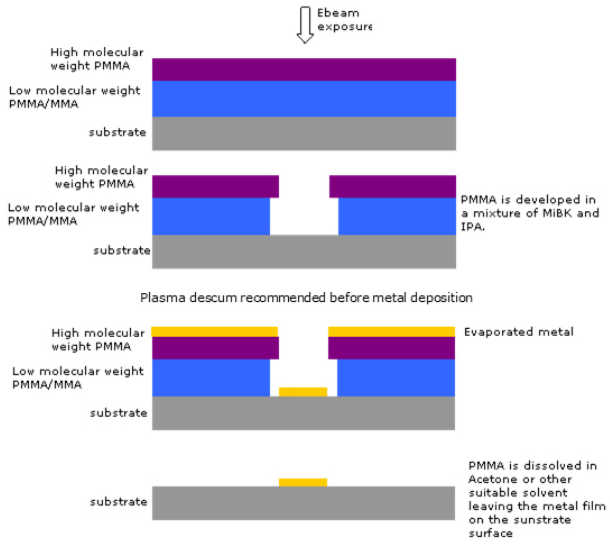


Figure 4.2: Lift-off process flow schematics [37].

This feature can be used to create a discontinuity of the deposited layer. The principal advantage is that once the resist is removed the deposited material is already patterned.

With that, a multilayered feature can be obtained without the need for multiple patterning and multiple selective and specific etching. In order to fully exploit the benefits of this technique, the deposition method should be less conformal possible to realize the physical separation between the layers deposited on top of the resist stack and the ones directly on the wafer. For the purpose of this project, a stack of metal layers is used to realize ohmic contacts and metal connections. For this reason, this technique was the best solution in terms of efficiency and ease of implementation.

E-beam evaporation

To ensure a successful lift-off procedure e-beam evaporator is chosen as the deposition technique. It consists of a physical deposition method that involves the condensation of the evaporated materials onto the substrate without chemical reactions. The material to be deposited, usually metal, is normally kept inside crucibles that are water cooled to eliminate contamination and thermal cross-talk. Multiple metals can be therefore sputtered without breaking the vacuum inside the chamber, loading various crucibles that can be interchanged. In the case of an e-beam evaporator, the heating source is a collimated e-beam deflected through a magnetic field to the surface of the crucible. In this way, it is possible to heat the material to reach the evaporation point, without introducing impurities. A flux of particles of the vaporized material is generated and the sample is positioned in the line of sight. The distance between the sample and the crucible is the factor determining the variability of the direction of the incoming particles: the more distant the substrate the more aligned and perpendicular to the surface the particle trajectory will be. To reach a nonconformal deposition like the one needed for this project the substrate was positioned far away to obtain an orthogonal flux with respect to the surface. Additional advantages of this deposition technique are higher deposition rate and lower temperature operation compared to other CVD techniques. The tool used in this project is the Evatec BAK501 LL.

Rapid thermal annealing

The rapid thermal annealing allows to increase the temperature of the substrate for a small fraction of time to stimulate specific processes. The heating is normally obtained through high-intensity lamps or lasers. It is most commonly used for dopant activation, thermal oxidation, or more in general to trigger thermally activated processes. It is difficult to have full control of the temperature ramp-up due to the non-equilibrium of the sample with the heating chamber. To realize alloyed ohmic contact RTA is used after evaporation of the metal stacks to realize the metal alloy necessary for a good contact quality. The furnace adopted for this thesis is the Annealsys AS-one 150.

Atomic layer deposition

Atomic layer deposition, also known as ALD, enables thin film deposition with single layer control. This is realized through a sequence of nonoverlapping exposure to gaseous chemicals, called precursors. The deposition of a single layer is accomplished through multiple separated exposures to different precursors. This allows to deposit one single layer per complete cycle. The reaction between the precursors is responsible for the formation of the wanted thin film, but the different precursors are always kept separated in the chamber to

finely control the deposition rate. The first precursors prepare the surface of the sample and the following one reacts only on the surface to form a single layer of the chosen material. The advantages of this technique are the high control of the thickness of the material and the high conformality of the deposited layer. This is enabled by the chemical nature of this deposition technique that does not involve flux of direct particles impinging the substrate but instead is a self-limiting process. This feature together with the possibility to heat the substrate allows to reach single layer control of the deposition. On the opposite, this method is really slow, depositing one single layer per cycle. This means that is most suitable to deposit highly conformal very thin film.

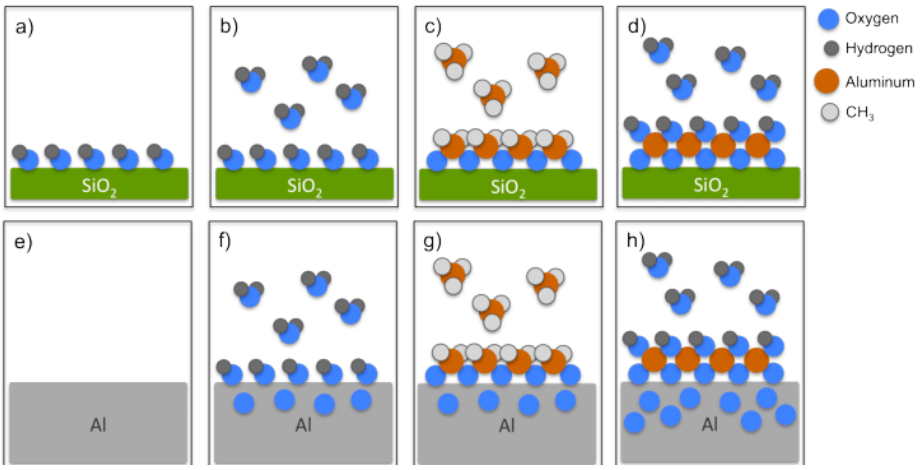


Figure 4.3: ALD processing scheme [38].

4.2. Process flow

In this section, the process flow used to realize the device is summarized and presented. Multiple e-beams steps have been used to pattern the photoresist and transfer the design to the substrate. This involves resist spinning, exposure, and development in addition to various bake, fundamental to guarantee both uniformity and structural stability to the photoactive compound. The substrate is supplied by a third-party vendor by exact specifications. This was chosen to obtain a fast and versatile substrate within a short period. These are the principal steps:

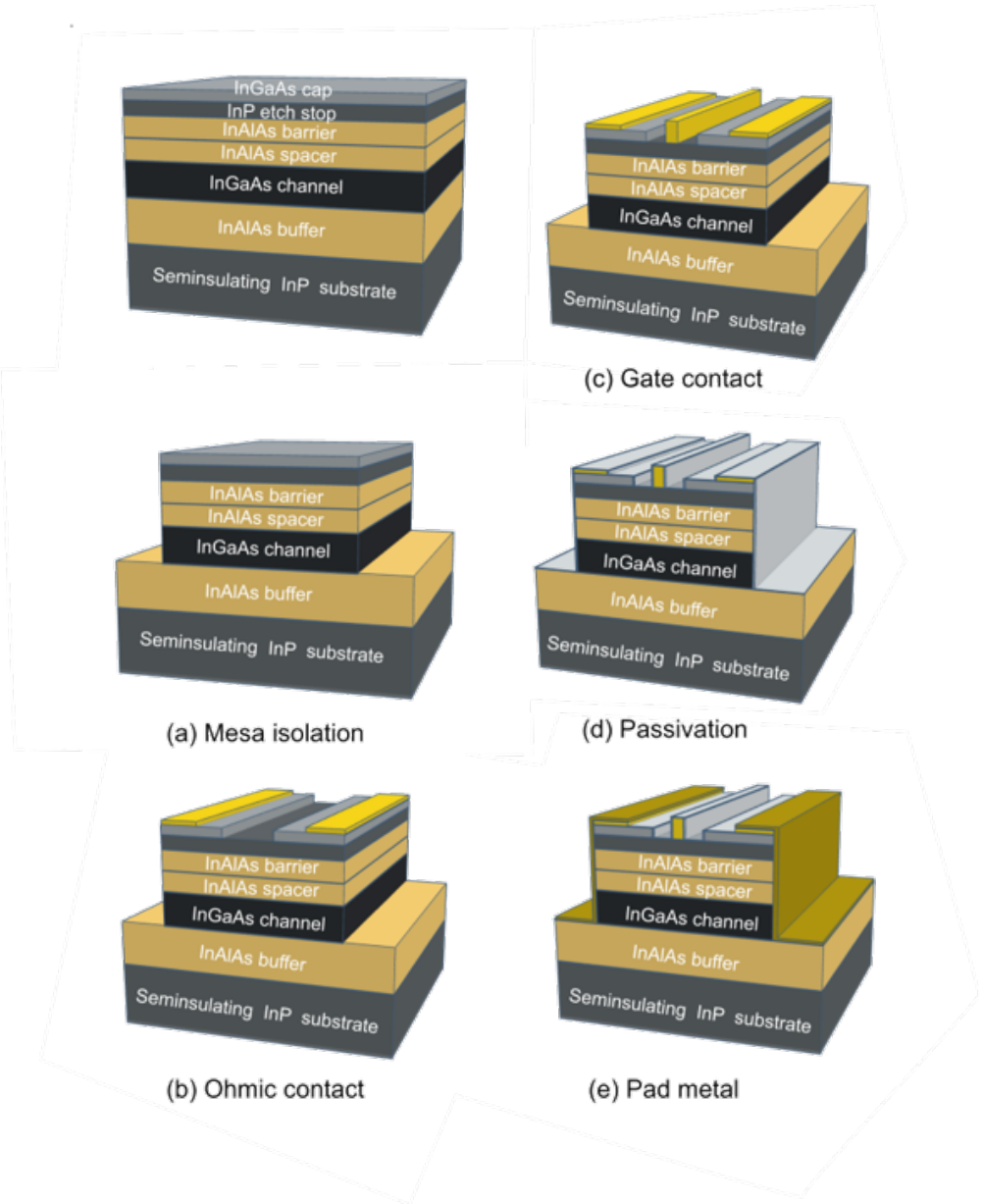


Figure 4.4: Process flow scheme from substrate to device.

(a) **Mesa etching**: at first it is necessary to isolate the device one from the other. To do so, mesa structures are realized by etching the substrate until reaching the InAlAs bottom layer. This is realized through wet etching with $H_2O_2 : H_3PO_4 : H_2O$ (1:1:25) solution for InAlAs and InGaAs, whereas $HCl : H_20$ (1.5:1) solution for the InP cap layer on top. This step defines the actual dimension, width, and length of the HEMT and therefore the time is critical to limit underetch. Wet etching is isotropic and requires particular attention while establishing a functioning workflow.

(b) **Ohmic contact deposition**: Ohmic contact is needed to have a good connection between the metal and the channel. Alloyed NiGeAu is the one chosen for this thesis. A stack of these three materials is deposited through e-beam evaporation and patterned through lift-off.

- **Contact annealing** after the deposition the metal layers are alloyed by means of a rapid thermal annealing procedure. This allows to decrease the contact resistance and achieve better device performance.

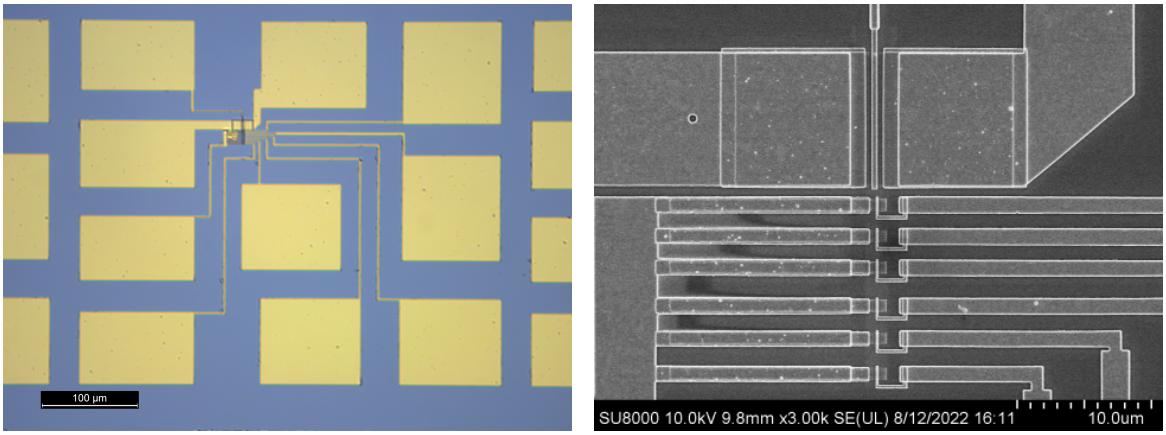
(c) **Gate formation**: to be able to realize the gate structure is necessary to eliminate the InGaAs cap layer which is highly doped to realize a Schottky gate contact with low reverse current. The control of the semiconductor stack below the gate is crucial to determine many device parameters, such as threshold voltage, gate leakage, and transconductance. Therefore is crucial to have fine control over etching processes. To do so highly selective wet etching with citric acid/H_2O_2 (7:1) solution is used. This ensures selectivity greater than 400:1 [39] and allows to realize the recess etch with high control. The metals used to fabricate the gate itself are also critical to have control over the barrier height. The stack used in this case is made of Pt/Ti/Pt/Au through e-beam evaporation. Pt is responsible to reduce the leakage with a higher barrier voltage whereas the other layer makes sure the gate resistance is low.

(d) **Passivation**: after the liftoff of the gate a passivation layer of Al_2O_3 is deposited through ALD to selectively protect the active area and isolate them electrically. The passivation layer is therefore realized only on the gate stack. The ALD process heats the sample to 250 degrees, making it possible to obtain the diffusion of the Pt into the InP layer which limits the gate leakage. The oxide etching is obtained through $HF : H_2O$ solution to remove it when not needed.

(e) **Metal pads patterning**: the last step is to realize the metal stack that builds the pads and the metal interconnection. In this case, a Ti/Au metal stack is used to connect external pads to the source, drain ohmic contact layer, and the gate metal stack.

4.3. Fabrication results

The layout designed in the previous chapter was successfully fabricated in the BRNC cleanroom. Periodic optical controls on the transferred e-beam pattern were performed to guarantee the success of the process flow. The final metalization for the pads resulted in some faulty devices, creating shorts between the power device and the sensing device. Nevertheless, the yield was high enough to guarantee a comprehensive characterization. In Fig.4.5 both optical microscope and SEM images of the fabricated diode arrays are shown.

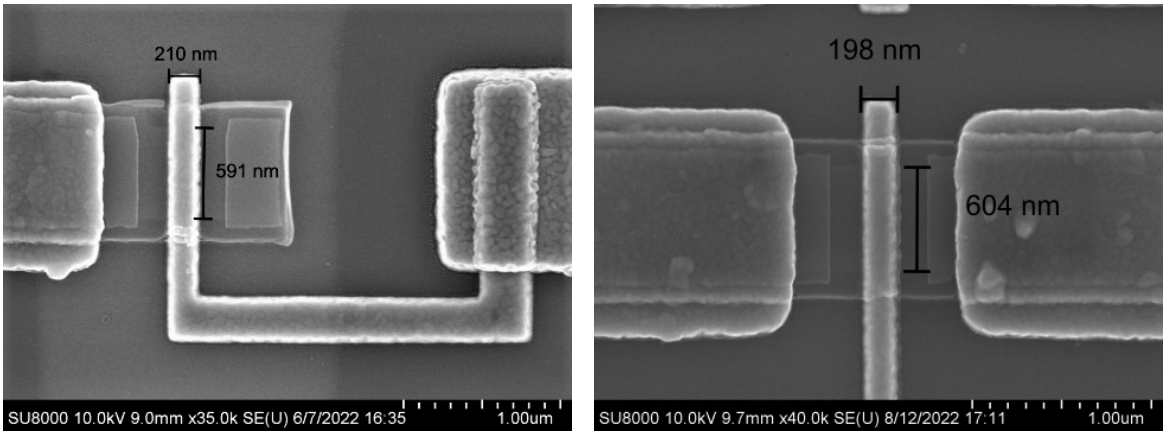


(a) **(b)**

Figure 4.5: Optical image (a) and SEM micrograph (b) of diode sensing structure.

Effective dimensions

Regarding the functioning devices, the effective dimensions are investigated to assess correctly electrical parameters. In Fig.4.6 the SEM images of the two different sensing devices are presented. It is important to remember that the targeted dimensions were $1\,\mu$m width and $150\,$nm length. Firstly the mesa definition experienced overetch for about $75\,$nm on both upper and lower sides reducing the width of the mesa by at least $150\,$nm. In addition to this, a light underetch can be seen under mesa edges in correspondence with the gate metal. This can be linked to the recess etch which is performed once the resist is exposed with the gate mask. In fact, during this step, the wet etchant has much less selectivity with the InAlAs compared to InP. Therefore the layers beneath the etch stopper are also etched, causing a reduction in the effective width of the device. The underetch has been estimated as $115\,$nm. Concerning the gate length, overexposure is responsible for $45\,$nm increase with respect to nominal values. All combined these effects allow to increase our spatial resolution of temperature data, but also cause a decrease in the SNR across all devices.



(a) **(b)**

Figure 4.6: SEM image of diode sensing device (a) and single sensing HEMT (b).

These effects are also present for power devices, but on a much wider device, the impact is much more limited. The effective distances from the power device are within 150 nm from the designed positions. In the following tables, the values extracted from the SEM images are presented. Possible variations for different devices should still be considered.

Expected distance (µm)	0.75	3.05	5.35	8.15	10.55	13.15
Measured distance (µm)	0.83	3.18	5.47	8.25	10.63	13.22

Table 4.1: Distance from the power device to the diode sensing device.

Nominal L_g	Fabricated L_g	Expected W_g	Fabricated W_g
150 nm	202 nm	10 µm	9.55 µm
250 nm	296 nm	10 µm	9.56 µm
400 nm	447 nm	10 µm	9.61 µm

Table 4.2: Effective dimensions of the power gate.

	Nominal Width	Fabricated width	Nominal Length	Fabricated length
Diodes	1 µm	590 nm	150 nm	210 nm
HEMT	1 µm	606 nm	150 nm	195 nm

Table 4.3: Sensing devices effective dimensions.

5

II generation devices

5.1. Measurements methods

In this section, different measurement methods are presented for the HEMT structure and for Schottky devices to highlight their strengths and limitations. Preliminary results and initial assessments are shown to select the best technique to develop a comprehensive analysis of the substrate temperature. At first, the structures are measured at room temperature to develop a working workflow. After that cryogenic measurements are performed to understand the heat dissipation in these particular conditions.

5.1.1. HEMTS current

With the new design is possible to bias independently the sensing and the power device. This implies that 6 probes are necessary to perform the measurement. The current flowing through the sensing device is monitored to detect any changes due to temperature variation. The bias of the device is set as the following:

- Power source is connected to ground
- Sensing source is connected to ground
- Sensing drain bias is fixed
- Sensing gate bias is fixed
- Power gate bias is fixed
- Power drain bias is swept across a voltage range

The variation in the power drain voltage allows to modulate the power dissipated from the device. The maximum drain voltage used is $0.8\,\mathrm{V}$, whereas the gate bias is kept at values lower than $0.6\,\mathrm{V}$ to limit the leakage current and protect the junction from breakdown.

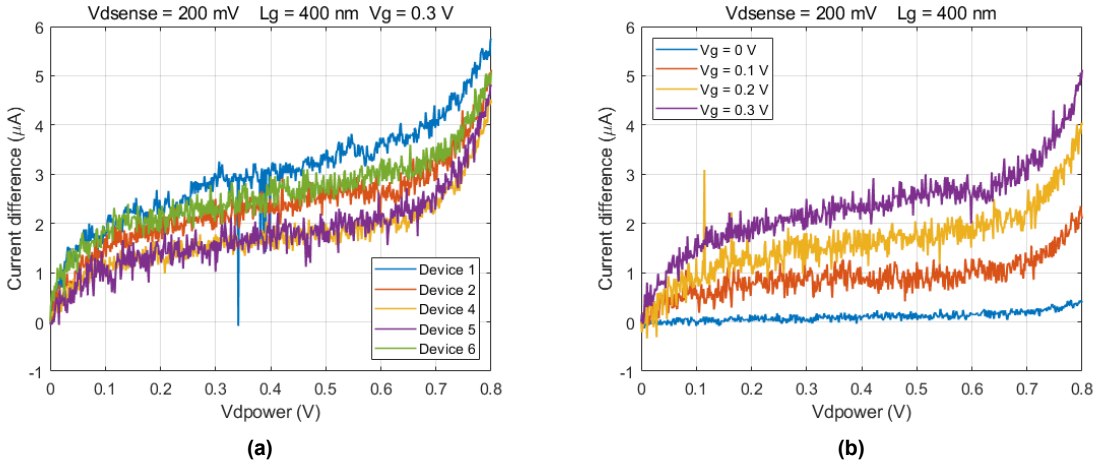


Figure 5.1: (a) Current variation for different devices with respect to the power drain voltage. (b) Current variation at different bias points with respect to the power drain voltage.

In Fig.5.1 the results of the measurements are shown. The current presents a similar behavior to that measured with the old generation, with a fast transition for the lowest value of drain voltage. In addition to that, there is no trend among devices. The further the device from the heat source is, the smaller the expected signal. But in this case, the magnitude of the most distant sensing device is smaller than the closest one. The change in gate bias of the sensing device is expected to change the magnitude of the sensitivity. As described in Section 3.2 it is expected that the ZTC point should be crossed and the sensitivity should become negative. In this case, this is not happening, and instead, the current difference is only increasing with higher gate values. This indicates that crosstalk between the power and the sensing device is still present.

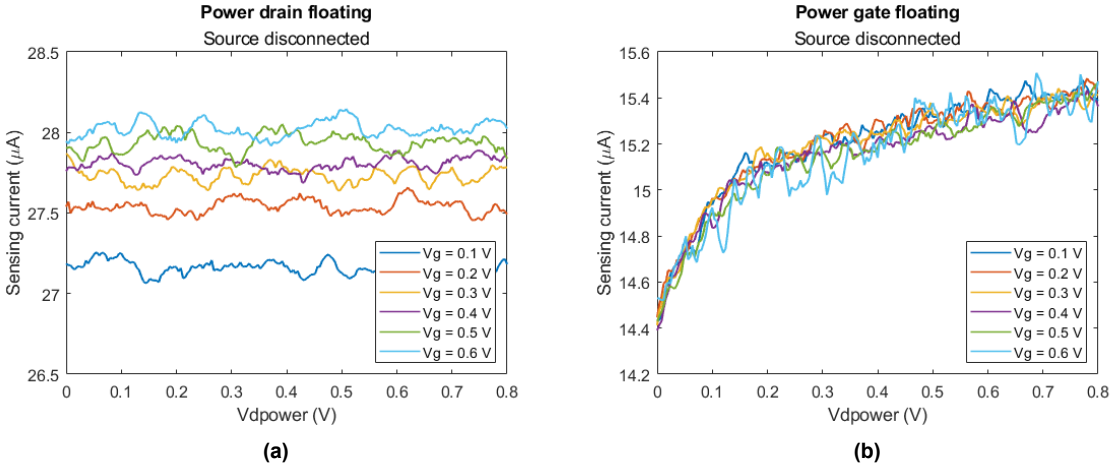


Figure 5.2: (a) Current in the sensing device with source and drain of the power device floating. (b) Current in the sensing device with source and gate of the power device floating.

To assess the responsibility for these effects we measured the current in the sensing device while no current is flowing through the power device biasing either the drain or the

gate but keeping the source floating. In this way, it is possible to see the effect of power biasing with respect to the characteristics of the sensing device. The results are reported in Fig.5.2. It is important to note that no current is floating in the power device. Therefore no power dissipation is happening in the device. The measurement setup is always the same, but what changes is the probe in contact with the metal pads. In the case the gate bias is changing it is possible to observe an increase of the current for higher biases. Instead, when only the drain is changing, a parabolic increase is observed in the sensing current. These combined effects can explain the trend shown in Fig.5.1. These experiments revealed that the two different devices cannot be operated simultaneously to detect temperature.

5.1.2. HEMTS threshold shift

Other parameters can be used to assess the temperature. In particular, the sensing device can be used in weak inversion to limit the crosstalk. As previously discussed in Section 6.11b the threshold voltage V_{th} change with respect to temperature. In this thesis, the latter is calculated as the voltage at a fixed current. It is possible to consider different current levels and obtain different sensitivities. In Fig.5.3 the change in the threshold voltage of I generation power HEMT is presented. Due to a change in the subthreshold swing the sensitivity increase for lower current, but the trend can still be considered linear. We can expect to obtain a sensitivity as high as $8\,\mathrm{mV/K}$ for $25\,\mathrm{nA}$ current in the II generation sensing HEMT.

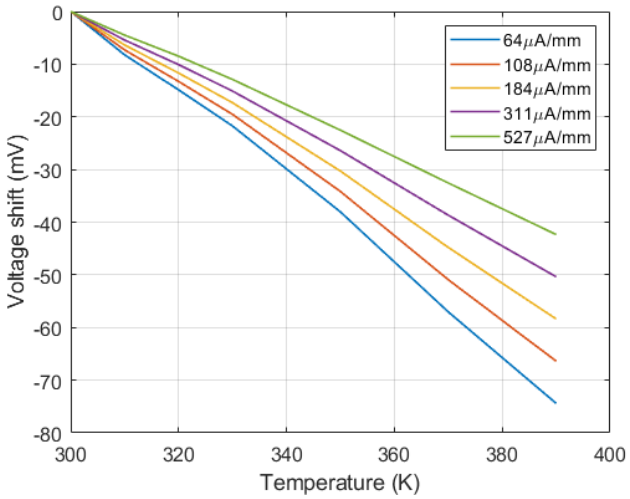


Figure 5.3: Threshold voltage shift at different temperatures for different current values.

This method has been evaluated through a different measurement method. Eight values of the power drain voltage have been considered. For each, the sensing device gate has been swept in the subthreshold region to collect information about the sensing device response at this operating point. The results are showed in Fig.5.4a. Compared to the simple current method it is possible to acknowledge a trend among devices, with a shift that decreases in intensity with the increase of the distance. On the other hand, the threshold voltage shift does not seem to be linear with the power. Instead, for Device 1 after $1.5\,\mathrm{mW}$

there is an abrupt change and for Device 5 the threshold voltage difference is even positive. To better assess the reliability of these results, additional measurements have been performed. A negative drain has been applied to the power device, with the same magnitude as the previous measurement. This causes the current to flow from the source to the drain. Assuming a discrepancy in the power dissipation due to a different band configuration, self-heating is still expected. In Fig.5.4b the results are presented. One can note that the trend inverts and even shows a positive shift for enough high dissipated power. This implies that also the threshold voltage shift suffers from the crosstalk between the power device and the sensing device, although the effects are less critical.

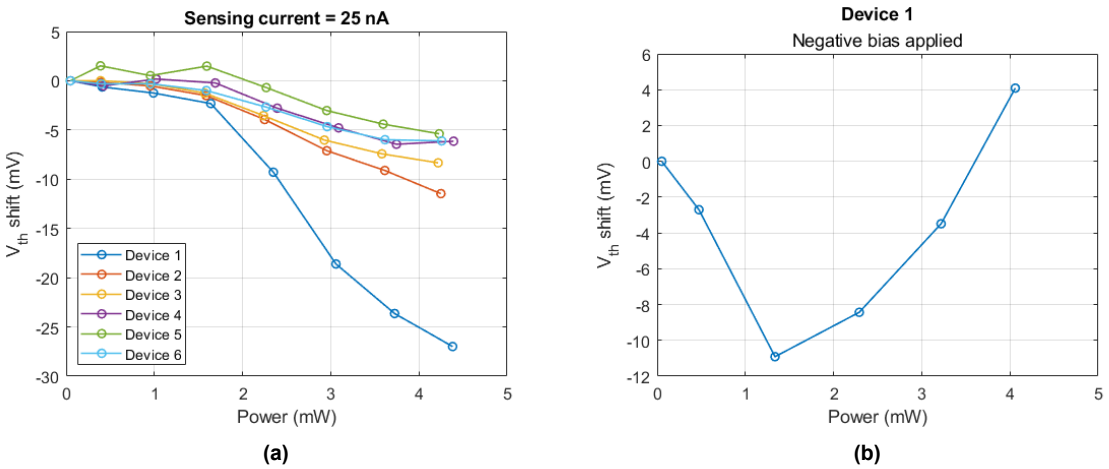


Figure 5.4: (a) Threshold shift with respect to power dissipation in the power device. (b) Threshold shift in the case of negative bias applied to the drain.

5.1.3. HEMTS subthreshold swing

In addition to the threshold voltage, the subthreshold swing is also linear with temperature. Given the structure of the device, the SS is in principle only dependent on temperature, making this parameter more resilient to crosstalk. In Fig.5.5 the trend with the substrate temperature is presented. The values for the room temperature values are close to the limit of $60\,\mathrm{mV/dec}$ but a slight effect of the drain bias is noticeable. In addition to that, for higher temperatures, the trend is superlinear due to other parasitic effects that are responsible for the deviation from theoretical models. Therefore, the expected temperature sensitivity is around $0.4\,\mathrm{mV/dec}$.

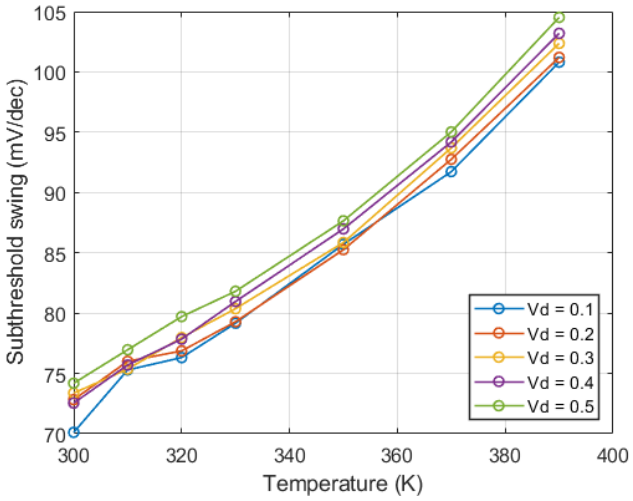
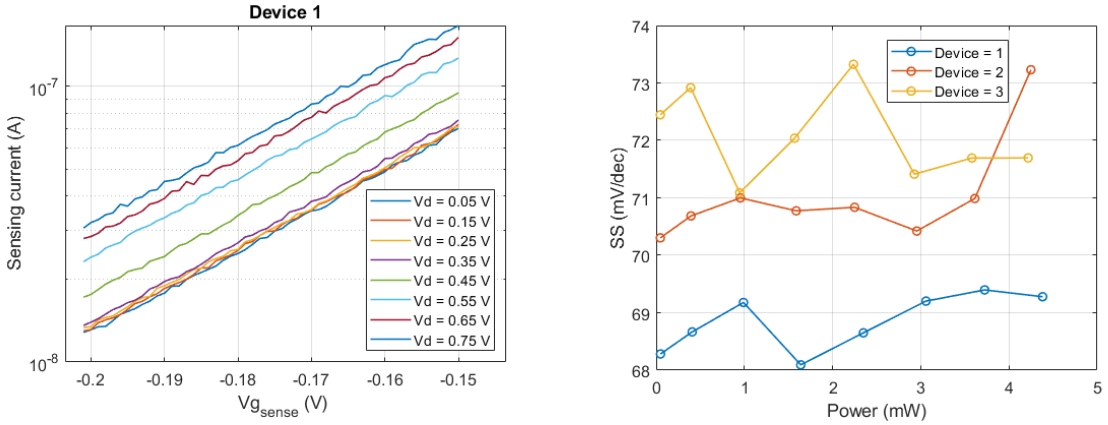


Figure 5.5: Subthreshold swing temperature dependence of a HEMT at different drain biases.

Measurements are performed as in the case of the threshold voltage. This means the transfer characteristics are recorded for limited and fixed drain voltage values, to be able to change the sensing gate voltage at determined power levels. In Fig.5.6a the sensing current is plotted for different power drain voltages (i.e. different power levels) in the weak inversion regions. From these curves, it is possible to extract the SS with respect to power, depicted in Fig.5.6b. The accuracy of the measurement is not high enough to detect the temperature variation induced by the power device. No clear trend is evident and values have a too high variability for the sensitivity provided by this measurement method. The measurement of the SS is, in fact, indirect, through a linear fitting of the curve, and a lock-in amplifier would be necessary to measure directly in a particular bias point.



(a) **(b)**

Figure 5.6: (a) Threshold shift with respect to power dissipation in the power device. (b) Threshold shift in case of negative bias applied to the drain.

5.1.4. Schottky diodes

In addition to the HEMT, the Schottky diodes represent another way to probe the temperature. The use of a simple two-probe bias, one for the ground and one for the other terminal, allows a simple characterization. As explained in the Appendix A this device can be biased at constant current and a temperature change corresponds linearly to a change in the voltage of the diode. In Fig.5.7 the diode characteristics measured at different temperatures are shown. The devices realized as gate-to-channel junctions indeed behave as Schottky diodes, presenting an exponential trend with respect to the voltage applied. A voltage of $750\,\text{mV}$ is considered, to set the limit of the electric field across the spacer and not let the device undergo breakdown. To avoid device failure, the maximum voltage for the temperature calibration was set to $600\,\text{mV}$ to restrict the maximum current through the device at temperatures higher than RT.

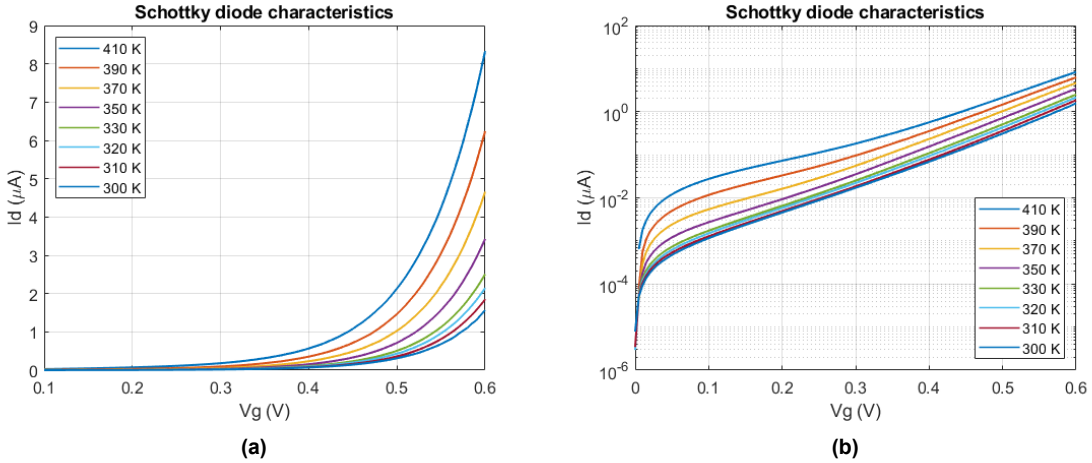
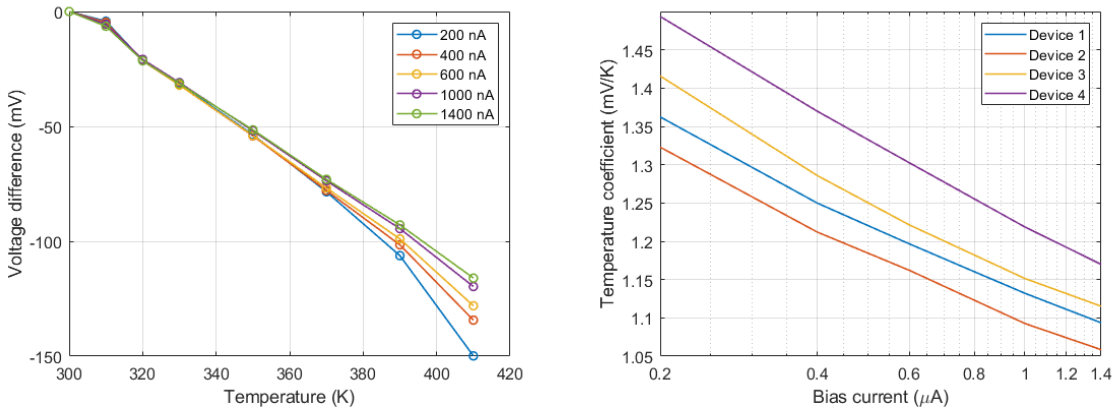


Figure 5.7: (a) Linear and (b) logarithmic plot of the diode characteristics with respect to different temperatures.

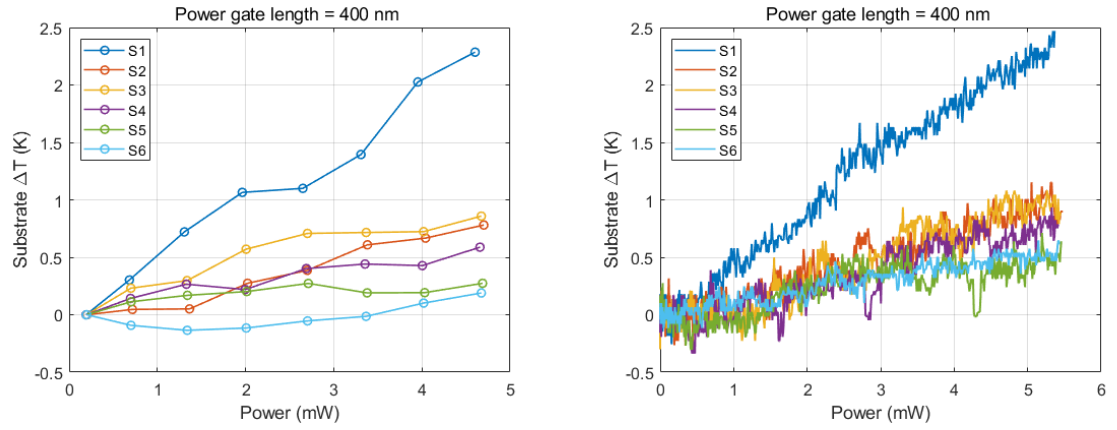
On the other hand, an increase in temperature induces an increase in current and a shift in the diode voltage for the same current value. This effect is depicted in Fig.5.8a. Using a higher bias current, the linearity increases for higher temperatures, where the trend is no longer linear for values below $1\,\mu\text{A}$. As it is possible to extract from a simple diode equation the sensitivity reduces as the logarithm of the bias current. This confirms that the devices fabricated match the theoretical model correctly. From Fig.5.8b the sensitivity is different from device to device. Therefore a calibration of every single device is crucial to achieve the correct temperature values. To achieve high sensitivity and linearity, the diodes are biased at a constant $2\,\mu\text{A}$ current. This also corresponds to a power density of $10\,\mu\text{W}/\mu\text{m}^2$, which is two orders of magnitude less than the maximum power density dissipated by the power device. This ensures that the diode self-heating is limited and does not affect the temperature sensing.



(a) (b)

Figure 5.8: (a) Diode voltage difference with respect to temperature at different current levels. (b) Logarithmic plot of the extracted temperature coefficient with respect to bias current.

The diode can be used to sense the substrate temperature in two different ways: static and dynamic. In the static mode, the power device is biased at a fixed point and the diode voltage is recorded for a short period. This means that the current flowing through the power device and the corresponding power is stable during measurement. The mean value of the voltage during the sample time is considered the value of the voltage at that particular power level. This ensures the possibility to eliminate some noise from the instrumentation. On the other hand, it is possible to vary continuously the power drain voltage and record the change in diode voltage. In this way, a more precise trend with the dissipated power can be observed, although the noise needs to be treated in a more sophisticated way. Fig.5.9 shows the results of the measurement, comparing the two methods.



(a) (b)

Figure 5.9: (a) Static and (b) dynamic measurements for 400 nm gate length power device for the central sensing device array.

Compared to the results of the HEMTs the response of the diode is linear with power and the trend among devices is consistent with the expectations. The temperature is increasing

less and less, the longer the distance from the power device. The two plots show the same trend and almost the same temperature values. This allows to determine that the thermal response of the substrate is faster than the measurement time in both methods. This means that the dynamic measurement can be a reliable method, to sense the temperature for all the power levels. In both cases, an intrinsic uncertainty is to be considered due to the noise and the setup used which can explain the difference between the two measurement methods. Some deviations from linearity are present in the case of the static data, more evident for Device S1, S3, and S6. On the other hand in the dynamic data, residual high-frequency noise is present combined with little oscillations, less impactful than in the static case. The dynamic one incorporates more information since the number of points available is two orders of magnitude higher, but it is not possible to remove the noise as in the static case. Therefore is more difficult to assess the voltage at zero power with high accuracy and define the temperature along the curve due to the perturbation of the signal. However, it is possible to process the data with more sophisticated data treatment techniques that take into account the physics of the phenomena. For these reasons the chosen method is the dynamic one.

6

Temperature measurements

The most accurate and reliable sensing structure has been identified as the diode array, through dynamic measurements. Localization and versatile temperature assessment are the best advantages of this technology. The integration on the same substrate and with the same processes make it suitable to characterize the heating dissipation around devices.

6.1. Data treatment

The dynamic method can be further enhanced through the use of post-processing. In particular, it is possible to use the physical understanding of the heating diffusion to elaborate the data and eliminate noise and interference. The temperature of the substrate is determined by the heat flux and thermal resistance. Since one can assume that the thermal resistance is constant for the variation considered, the temperature is linearly proportional to the power dissipated from the device. Therefore, a linear increase in the temperature is expected. In addition to that, some low-frequency oscillations are observed in the signal, due to the setup environment that can alter the correct definition of the zero power voltage.

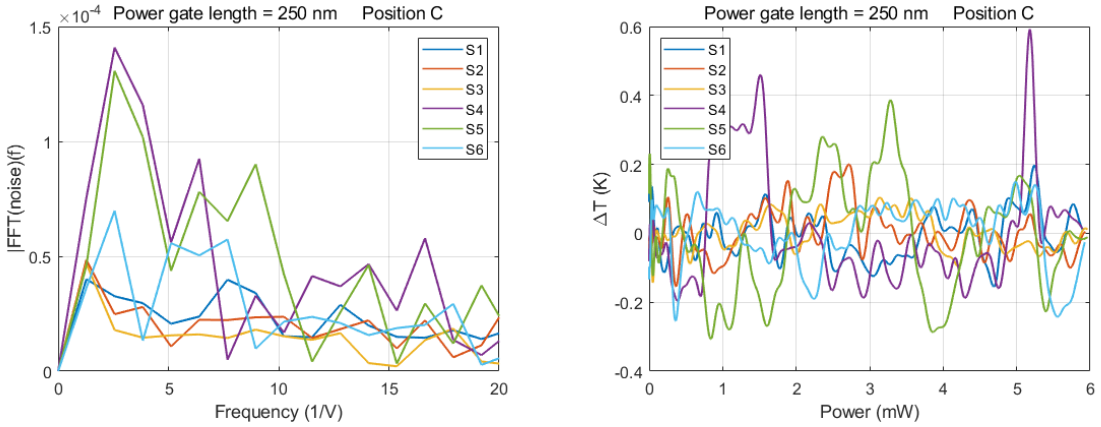


Figure 6.1: (a) FFT of the noise, once removed the linear trend. (b) Magnitude of low-frequency noise extracted from the measurement.

In Fig.6.1a the noise is extracted from the raw measurement in Fig.5.9 subtracting the main linear trend that is possible to identify. The Fourier analysis clearly shows that there is a bigger component at lower frequencies that is added to the signal. The filtered noise is represented in Fig.6.1b where big oscillations are visible, especially for Device S4 and S5. Due to the high periodicity of the signal, the source is most likely the instrument or environment noise. Therefore, it is reasonable to eliminate it. This allows the zero power voltage to be defined with higher accuracy. The script used to perform this analysis can be found in Appendix B. The following steps are followed to eliminate these effects and extract only the effective thermal signal:

- Extraction of main linear trend
- Low pass filter to select the low-frequency noise
- Subtraction of the selected noise from the signal
- Linear fit of the filtered signal
- Elimination of residual vertical shift
- Mean of multiple curves taken in the same bias condition

In Fig.6.2 the results of the post-processing are shown. The post-treatment data are more consistent with each other and the reference at zero power looks more reliable, due to lower oscillation around that region. This data processing helps to separate the thermal signal from the noise or interference. The data have been processed using this algorithm and from the measurements taken is possible to gather information on the self-heating and how this affects the temperature around the device.

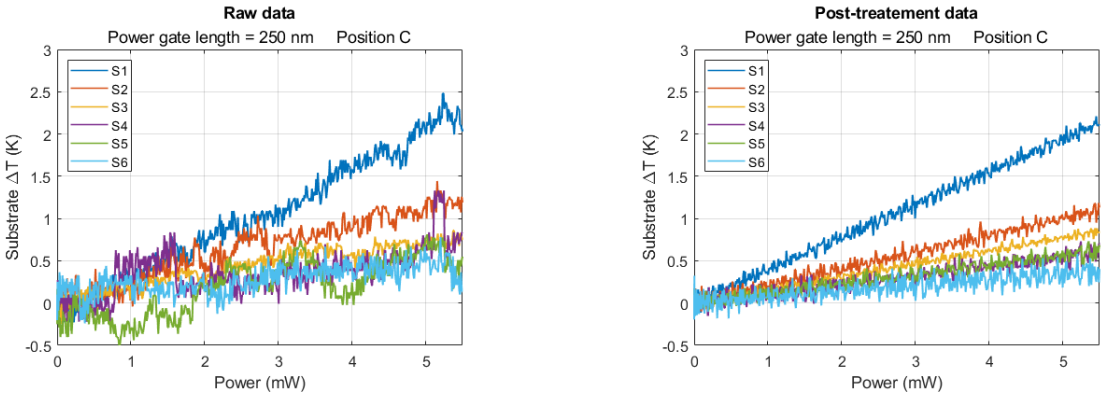


Figure 6.2: (a) Raw and (b) processed data of the substrate temperature for the central position of the array.

6.2. Temperature map

Using this method, the full array of diodes fabricated has been characterized. Due to the variability of the devices, a single-device calibration procedure was necessary to assess the temperature with enough accuracy. Characterization was performed at room temperature to verify the performance of this technique and to assess its potential in localized integrated temperature evaluation.

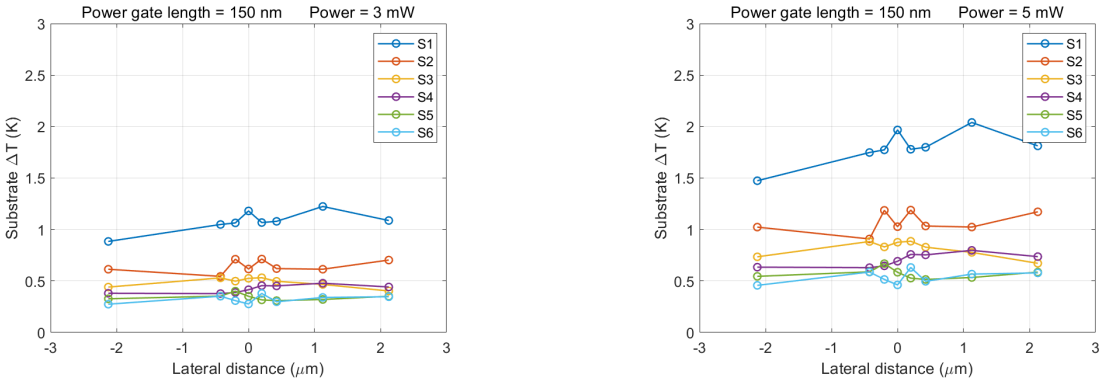


Figure 6.3: Substrate temperature along lateral distance for multiple devices at 3 mW and 5 mW of power dissipated from a 150 nm gate length device.

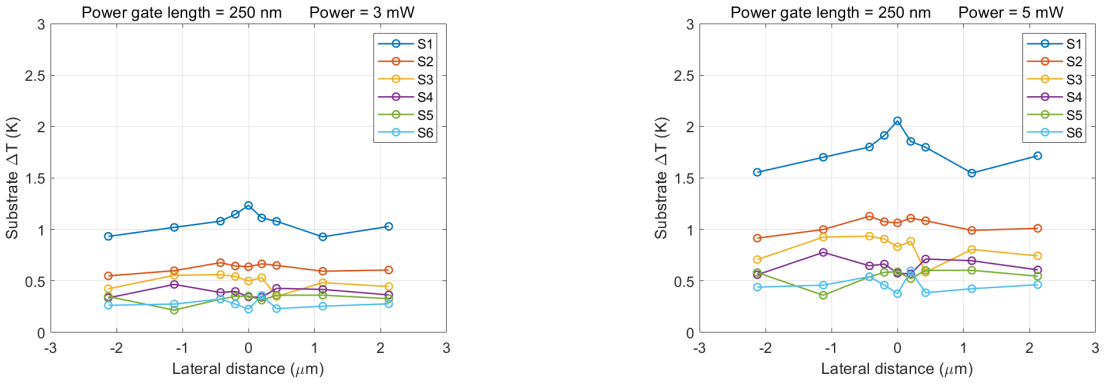


Figure 6.4: Substrate temperature along lateral distance for multiple devices at 3 mW and 5 mW of power dissipated from a 250 nm gate length device.

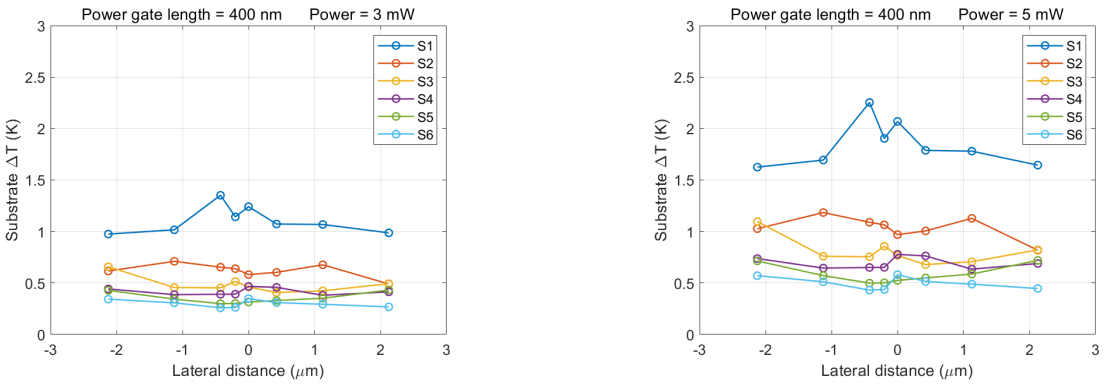


Figure 6.5: Substrate temperature along lateral distance for multiple devices at 3 mW and 5 mW of power dissipated from a 400 nm gate length device.

In Fig.6.3, 6.4, 6.5 the results for the three different gate lengths are presented. The lateral distance is taken from the center position, located at the drain side of the power device. There is not a relevant difference compared to the accuracy of the measurement among them if we consider the maximum temperature for the same power level. The substrate reaches almost 2 K of temperature increase for all gate length in the center array dor 5 mW of power dissipation. The 400 nm device has additional lateral peaks at 2.27 K and 2.07 K at R1 and L1 device. The heat distribution peaks in the center position, but the temperature is high also next to the power device. This implies that the source and drain metal pads play a role in heat dissipation. The closest device to the heat source shows the highest increase in temperature and the peak value is the center top most device which is aligned to the gate side facing the drain. This confirms the assumption that the heating occurs closer to the drain side. This behavior is observed for all gate lengths except for the devices of 400 nm. Calibration and measurement error can be accounted for this deviation or the bigger gate metal stack impacted the heat dissipation. In the smallest gate length, the drain side shows a higher temperature than the source side also for larger distances. This would imply that the electrons have a higher mean free path in the drain. This may be related to the higher energy of the electrons traveling in the channel. Therefore the electrons would travel over a longer distance. However, the accuracy is not enough to conclude with certainty that this is an actual signal, but it is worth further investigation.

6.3. 2D heatmap

From the previous data, it is possible to build a graphical representation on two dimensions to represent the substrate heating around the device. in Fig.6.6 the plot is attached on top of an SEM image of one of the structures used to build the complete map. This result is crucial since it demonstrates the possibility to gather information on heat diffusion and give insightful information to the possible integration of other devices, that are highly temperature sensitive, such as the qubits.

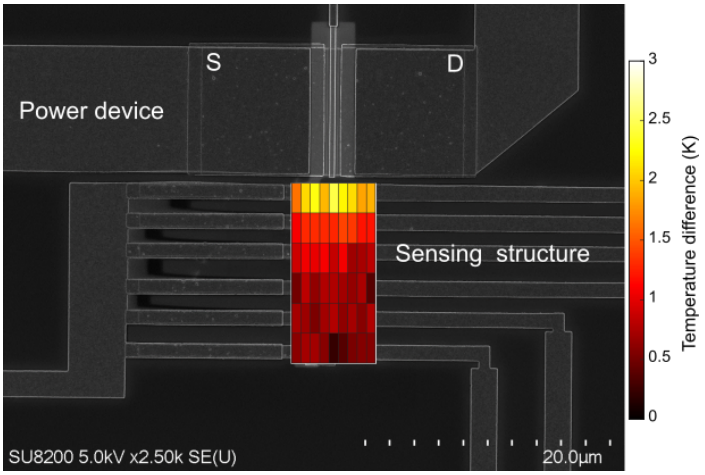


Figure 6.6: Heatmap of the substrate temperature attached to the SEM image of one of the structures measured at 5 mW power dissipation.

At room temperature, it is possible to extract some important characteristics. The temperature near the metal connections to the source and drain stays high even going $2\,\mu$m far away from the active region. This means that these structures play a fundamental role in heat dissipation. However, the center of the structure is hotter than the more lateral ones. This difference is no more evident if the vertical distance considered is higher. This means that the actual heat source is localized, but at larger distances, the metal starts to play a role in the temperature distribution.

6.4. Vertical temperature distribution

In addition to the overview of all devices, it is possible to focus only on the vertical temperature distribution. In Fig.6.7 the graph of the increase in substrate temperature with respect to the vertical distance from the power device is shown. The different gate lengths do not have a noticeable impact on the substrate heating, according to these measurements. Both the temperature and the overall trend agree for the different devices. In the case of the $250\,$nm power device, the most distant devices show some deviation from the other gate lengths.

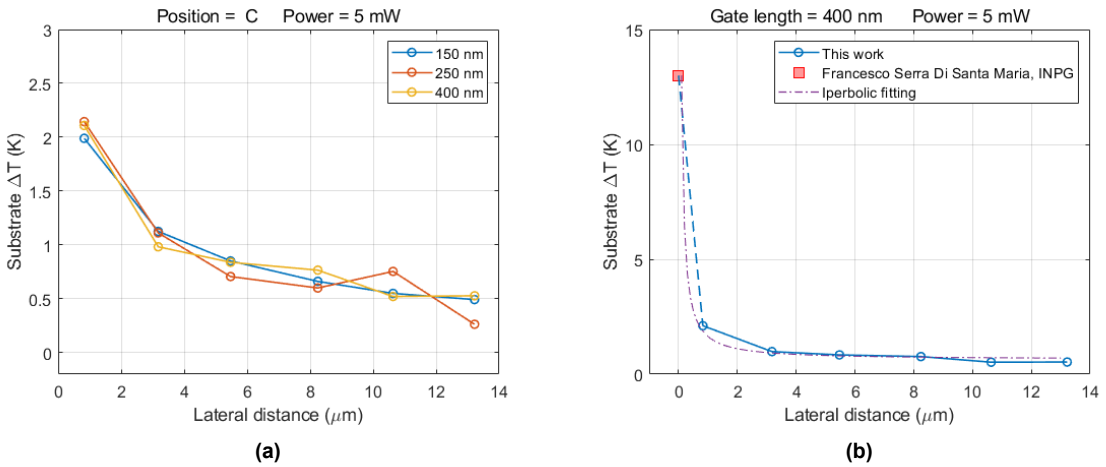


Figure 6.7: (a) Vertical temperature distribution for three gate lengths at $5\,$mW power dissipation. (b) Fitting and complete representation of the vertical temperature distribution with gate thermometry data.

The temperature reaches an increase of more than $2\,$K at $0.8\,\mu$m from the power device and saturates at around $0.5\,$K at larger distances. This behavior is qualitatively similar to [33] and [34], following a $1/d^n$ law (where d is the distance and n is a factor between 1.09 and 1.10 at $5\,$mW). Gate thermometry has been performed on the same devices and the combination of the two datasets is fitted and shown in Fig.6.7. At room temperature, the channel temperature reaches $13\,$K which agrees with our measurements with high accuracy. This represents an additional reliability proof of this methodology to assess the temperature of the substrate correctly, providing accurate values in agreement with both the literature and different techniques.

6.5. Cryogenic measurements

Once the setup has been validated at room temperature, the integration of the sensing structure is used to understand and compare self-heating and dissipation at cryogenic temperatures. For this reason, a cryogenic probestation has been used to perform the characterization of the devices at temperatures from $300\,\mathrm{K}$ to $4.2\,\mathrm{K}$.

6.5.1. Cryogenic probestation setup

For the purpose of this work, a helium cryostat has been used. Compared to a dilution refrigerator, it is much more versatile and easy to operate. There exist two main versions: the open-loop and the closed-loop. In the first case, the helium is lost during the refrigeration after being evaporated. In the second case, the helium is reused. The sample holder is put in contact with a liquid helium bath at $4.2\,\mathrm{K}$ that removes heat from the stage. During this step, it becomes vapor and can be either discarded (open-loop) or cooled down again (closed-loop). The biggest advantage of the closed-loop cryostat is the possibility to run continuously and that there is no need to be refilled. This saves time and money when an experiment requires this type of cooling. A pump and a cooler are responsible for keeping the system stable, whereas a heater is used to change the temperature to a set value and to keep it constant with time.

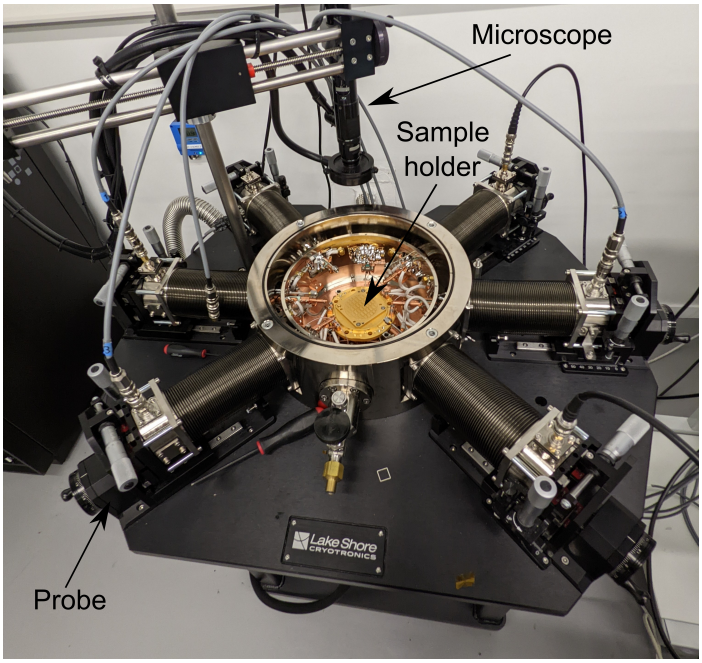


Figure 6.8: Cryogenic probestation used to perform the measurement in this section. The six probes are located at the border and a microscope allows to operate the probes on the sample.

In the chamber where the sample is situated the pressure needs to be in the order of $1 \times 10^{-6}\,\mathrm{mbar}$ to avoid the condensation of molecules dispersed in the air, i.e water and nitrogen that has a boiling point well above the targeted temperature (respectively $273\,\mathrm{K}$ and $77\,\mathrm{K}$). This limits the convective heat transfer. In addition to that, a shield is mounted

inside the chamber to avoid irradiation to heat the sample. At the same time, it is crucial to cool down also the probes to avoid that they heat the device once they are positioned on the sample. It is really difficult to bring them to $4.2\,\mathrm{K}$ but they are thermalized when they are in contact, due to their low thermal capacity. Another important part of this setup is the antivibration precautions, due to high mechanical oscillation induced by both the void pump and the helium compressor. The cryogenic probestation used for this work is provided by the IC Lab, in Neuchatel and it is shown in Fig.6.11b. The possibility to finely control the temperature and its stability were crucialaspects to be able to perform the experiment, together with the possibility to use up to six probes.

6.5.2. Experimental results

To use this structure is essential to know how the Schottky devices behave at cryogenic temperatures. This setup allows to extend the calibration to lower temperatures. It is important to remember that the carrier concentration in the 2DEG is stable even at cryogenic temperature. Therefore the electronic emission is still dominated by thermionic effects. In Fig.6.9a the measurements both from the RT and from the cryogenic probestation are reported in the same graph to provide a complete overview. A quadratic fitting is provided with the data, to extract the sensitivity. The latter matches closely with the values calculated at RT. The diode voltage is saturating at around $50\,\mathrm{K}$ and shows a maximum around $10\,\mathrm{K}$. At even lower temperatures, the voltage starts to decrease. This kind of trend has also been identified in the threshold voltage of the HEMT. In addition to that, mobility also saturates in this temperature region.

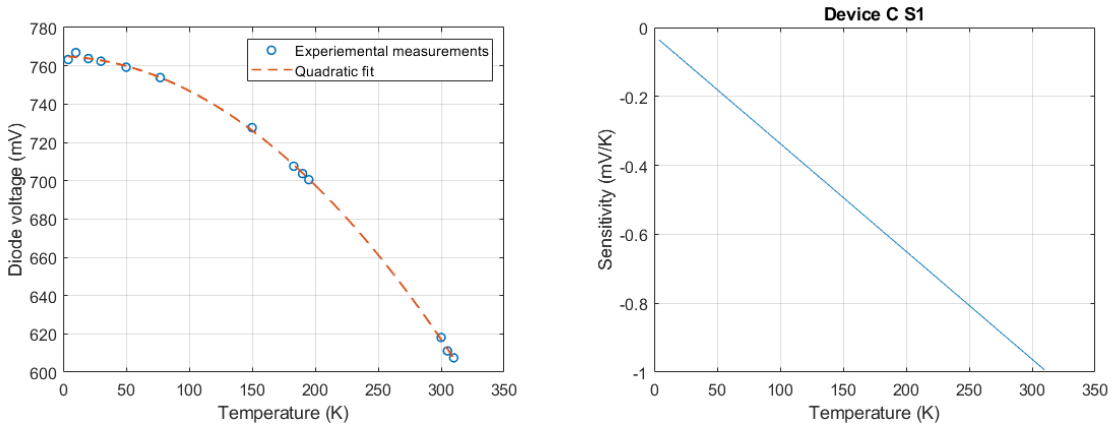


Figure 6.9: (a) Diode voltage with respect to temperature, fitted with a parabolic equation. (b) Extracted sensitivity at different temperatures.

Silicon diodes, on the contrary, are usually characterized by a kink at the lowest end of the temperature range, attributed to carrier freeze-out [40]. The doping necessary to reach a degenerate state (such as the one in the HEMT) removes this anomaly, and the silicon diode shows also behaviors similar to the one presented here. Instead, from a theoretical investigation of the threshold voltage in a CMOS transistor, the freeze out of the carrier would not be sufficient to explain the kink [41]. However, this effect remains unclear in pMOS de-

vices, where additional effects must be considered to explain the phenomena. Concerning the diodes in this thesis, the carrier concentration is kept stable even at cryogenic temperature and therefore the freeze out is avoided and no kink is visible. In addition to that, in multiple devices the behavior at temperatures below 30 K is variable. Interface traps and defects play an important role in defining how the Fermi level is positioned within the band gap [41]. Since the active area of these devices is small, the variability induced by a single trap or defect may be relevant. For all these reasons, the sensitivity in the lowest temperature region requires an analysis on single devices. The measurements have been performed for the 250 nm on C and R2 devices at different temperatures. In Fig.6.10 two graphs are reported on the measurements made at the lowest temperature (4.2 K). The diode voltage is represented with respect to the power dissipation of the HEMT. It is clearly noticeable that for the three different values of temperature, the signal oscillates, but no trend is visible. The signal is almost stable if we interpret the oscillation only as noise. Therefore the evidence is that the system is sensitive to temperature variation even in a cryogenic environment, but no heating of the substrate is measurable at 4 K. However, self-heating expected is greater than at room temperature for these devices from both simulation [42][43] and experimental evidence [14][44]. The results shown here do not mean necessarily that no self-heating is happening in the device, but that there may be very little thermal crosstalk between the power device and the surrounding area.

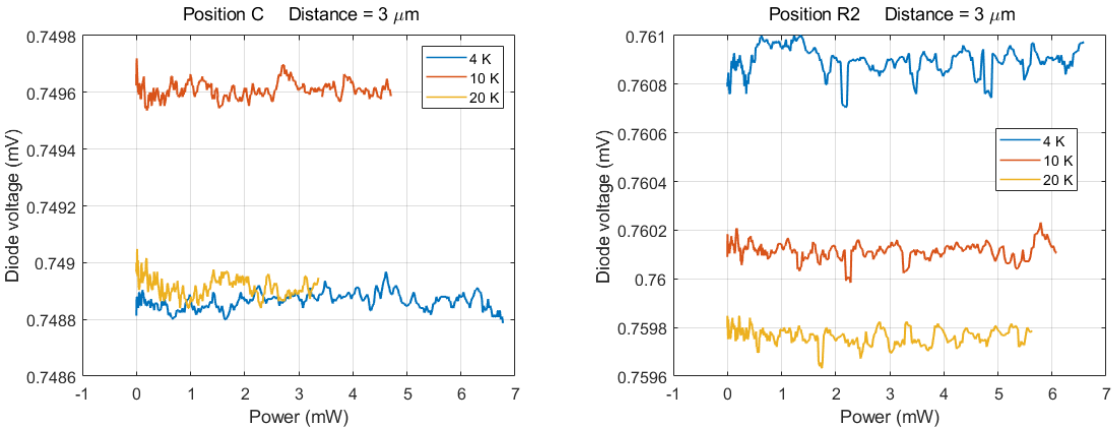


Figure 6.10: Diode voltage measurement with respect to power dissipation for the center device (a) and the second right device (b).

With the same algorithm shown in Section 6.1 the temperature difference of the substrate is extracted. From 4 K until reaching 150 K no thermal signal is detected by the diode sensing array. In Fig.6.11a the change in the diode voltage for the latter temperature is represented. It is noticeable a linear trend which is related to a temperature effect on the device. A comparison for different temperature values is also shown. The increase in the substrate temperature is still small even at 150 K and is lower than the uncertainty of the measurement (0.5 K) for even lower temperatures. In the case of CMOS, silicon behaves differently from a thermal point of view. The thermal properties of III-V materials nanostructure are not fully characterised and these can have a huge impact in the heat spreading in the substrate.

This shows that the heat distribution at cryogenic temperature around the device is much lower than expected compared to the results obtained directly on the device temperature with gate thermometry [14][44].

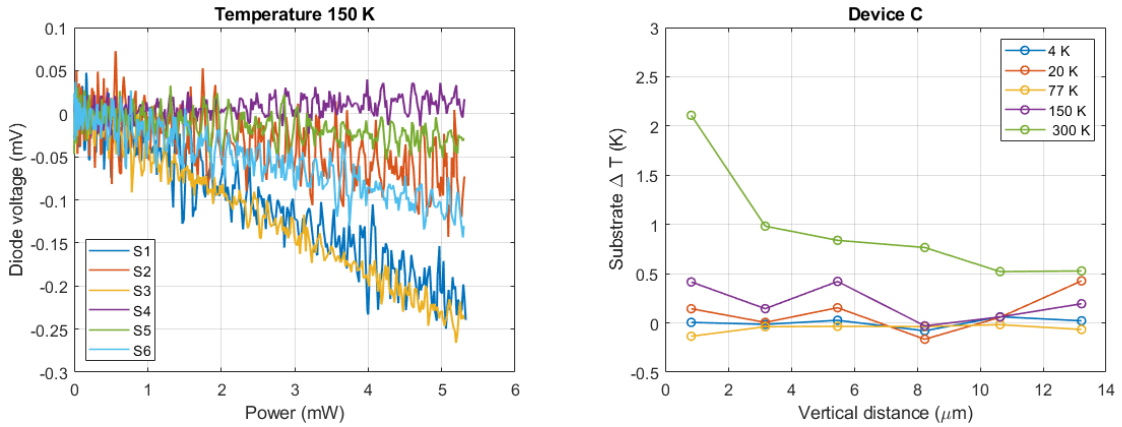


Figure 6.11: Diode voltage measurement with respect to power dissipation for the center device at $150\,\mathrm{K}$ (a). Substrate temperature extracted values for different substrate temperatures with respect to vertical distance from the power device (b).

To conclude, at lower temperatures the sensitivity and the signal-to-noise ratio represent the biggest obstacle to perform more accurate measurements, but it is possible to gather information about the heat spreading around the device. If at room temperature the self-heating of the device induces the increase of the substrate temperature for a large distance, at $4\,\mathrm{K}$ the thermal crosstalk with the surrounding area is strongly limited. The combination of the temperature-dependent thermal resistance and the heat transport mechanism may isolate the device and induce higher self-heating, as in the case of Ziabari [34].

7

Conclusion

In this chapter the summary of this work is presented, together with the main results and a prospect of future work and outlook. Attention has been given to address the most fundamental problems solved and the possible challenges for future development and improvement of this technology.

7.1. Summary

The principal objective of this thesis was to characterize heat dissipation and self-heating in the substrate of cryogenic HEMTS to enable further integration in quantum computers. Through a new design and new devices, an integrated sensing structure was obtained that showed the possibility not only to gather information on heat diffusion over a large area but also to provide flexibility in the measurement conditions, from room to cryogenic temperature. This was possible through a integrated sensing structure, processed together with the device to study. Firstly, the first-generation structure was characterized to understand the main limitations. The limited setup forced to have access only to four probes. This introduced built-in crosstalk between the power device and the sensing structure which was affecting the possibility to obtain reliable measurements. The high current flowing in the source and its access resistance caused a shift in the effective ground voltage applied. The gain provided by the sensing HEMT was responsible for an additional contribution that covered the actual thermal signal.

For this reason, a new design with more flexibility in biasing the devices was introduced in order to avoid this effect and Schottky diodes were considered to evaluate different device physics as sensing principle. A separate gate and source between the two classes of devices were realized to try to remove the crosstalk and additional structure were realized to obtain a full 2D map in the close area of the device. This means designing multiple versions of the design with different positions with respect to the power device to characterize a bigger area of the substrate. With 54 devices it was possible to characterize more than $60\,\mu m^2$ around the DUT, with temperature gradient-dependent spatial resolution. In this way, the data points were positioned to obtain the maximum information possible for a fixed number of sensing devices.

This approach was applied to the following structures:

- 6 probes sensing structure
- Single point sensing structure
- Drain to gate variable distance sensing structure
- Schottky diodes sensing structure

These devices have been fabricated with the process flow described in Chapter 4 inside the cleanroom of IBM Research Lab Zurich. Starting from an epitaxially grown wafer it was possible to obtain working devices and sensing structures that have been characterized. The effective dimensions of the fabricated devices have been evaluated through SEM imaging to assess the distances and dimensions of the active areas of the devices.

Different methods have been evaluated to assess the temperature of the substrate. Multiple control parameters were monitored with respect to the power dissipated by the DUT. Here are the physical quantities that were studied in this work:

- HEMT current at fixed bias
- HEMT threshold voltage shift
- HEMT subthreshold swing
- Schottky diodes voltage

All the methods involving the HEMT showed lowering signs of crosstalk but it was not possible to eliminate it completely. The highest accuracy and reliability of the measurement were achieved with the Schottky diodes voltage methods. This comes also with a simpler measurement routine and lower setup requirements (5 probes). The data acquisition was also evaluated and a static and dynamic method has been studied. The first one is based on fewer power values with higher acquisition time and the second one relies on a much denser power dataset with punctual voltage sampling. Additional physics-based data treatment allowed to reduce noise and improve the accuracy of the extracted data. The dynamic method was the most suitable for this technique and provided reliable measurements in agreement with the literature.

This technique was used to obtain information on the substrate temperature. At first, the characterization of the full sensing matrix was performed at room temperature. This included the calibration of every single device to overcome the intra-device variability. The result was a full 2D map of the substrate heating around the DUT. This represented the proof that this methodology can be used to gather information and that is competitive with other techniques. The temperature is monitored for different power levels and different gate lengths. This showed little dependency of substrate heating on geometrical parameters of the HEMT but highlight the impact of the source and drain metal pads in the heat dissipation. With the gathered data it was possible to integrate gate resistance thermometry data collected on the same sample and fit the extended dataset, providing evidence of the reliability of this method.

After the room temperature measurements, the sample has been measured at cryogenic temperatures. It was possible to conclude that the substrate heating at low temperatures is decreasing. If at room temperature the substrate reached $2\,\mathrm{K}$ increase, the variation at $4\,\mathrm{K}$ is

under the detection limit of the sensing structure ($0.5\,\mathrm{K}$). The important consequence of this result is the possibility of integration of thermal-sensitive devices in a much more compact way without compromising performances. This opens up possibilities of qubits integration directly on-chip to further aggressively scale quantum computers. To conclude, this work proves the possibility to use an in-situ sensing structure to characterize the heat dissipation on the substrate with versatility and easy integration possibilities. With that, device self-heating has been characterized both at room temperature and at cryogenic temperature, showing new perspective on heat dissipation at cryogenic temperature, completing the characterization of these devices in these operating condition.

7.2. Future work and outlook

Self-heating in these devices is not fully explained and understood, due to complex heating dissipation phenomena. A lot of factors are influenced by the specific structure and the material properties of these devices, as explained in Chapter 2. This work represent a step in gathering crucial information on how the heating propagates but is not sufficient to answer all questions.

Improvements regarding the sensing devices can still be obtained and can help to gather more data. One way would be to increase the dimension of the active area of the devices. They suffer from different noise sources and telegraph noise was observed, together with high variability issues at low temperatures. Acting on the dimension can be an easy solution to improve SNR and obtain more accurate results. This can be beneficial, especially at low temperatures where accuracy is most critical.

In addition to that much information has been collected regarding material properties that can be used to provide a model to verify and explain the experimental data. This would be interesting to establish the main responsible for the results at low temperatures and to increase the speed of assessing the performance of different designs. This would include also the possibility to evaluate the impact of the metal pads in heat dissipation and act on that to improve performances.

To conclude, some aspects not covered in this work are worth to be investigated. Papers have been published regarding GaN power HEMTs to improve their performances, actively reducing the self-heating. Simpler ones rely on additional thin film coatings of high thermal conductivity materials like diamond [45][46]. Other possibilities rely on changing the InP substrate with high thermal conductivity materials like diamond or SiC. This would require complex wafer bonding and reverse epitaxial growth on the wafer [47][48]. For these kinds of applications, interesting results have been shown, but cryogenic performances have not been evaluated. This represents an opportunity for further improvements of key performance indicators also for quantum readout applications.

A

Diode temperature characteristics

Schottky diodes are meta-semiconductor junctions and thanks to the energy barrier at the interface the contact is not ohmic anymore. In this work, the metal is represented by the gate stack and the semiconductor is the $InAlAs$ layer beneath. Although the doping mechanism is not the same as in traditional Schottky devices, the junction behaves still in the same way. These devices are optimized to minimize the leakage with the addition of a Pt thin layer to increase the barrier but can provide the necessary performance to be used as a temperature sensor.

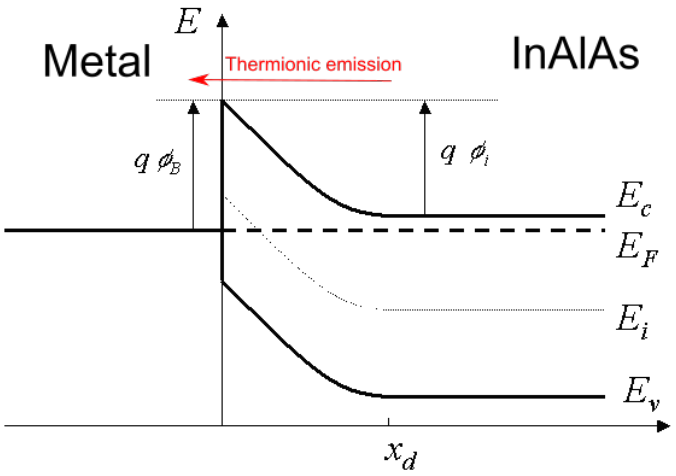


Figure A.1: Band diagram of a Schottky diode.

Multiple conduction mechanisms in Schottky diodes are possible: thermionic emission, diffusion current, and tunneling. In the case of Schottky devices, at room temperature, the tunneling is negligible, whereas thermionic and diffusion are the main responsible. Thermionic emission implies that there is a net flux of electrons with higher energy than the barrier that moves from one side to the other. The applied bias changes the height of the barrier seen by the electrons and this change the magnitude of the current. Temperature affects elec-

tronic concentration at fixed energies changing the net flux of electrons flowing above the barrier. It is possible to obtain an analytical formula for the current:

$$I = ART^2 \exp -\frac{\phi_b}{k_b T} \exp \frac{qV_b}{k_b T}$$

where A is the area of the active region, R is the Richardson's constant, ϕ_b is the barrier potential and V_b is the applied bias to the metal. The temperature dependency of the current is complex and depends on both a quadratic term and an exponential term. On the other hand, the voltage for a fixed current value is equal to:

$$V_b = ln(\frac{I}{AR})\frac{k_b T}{q} - 2\frac{k_b T}{q} ln(T) + \frac{\phi_b}{q}$$

This means that at first approximation the voltage is linearly dependent on the temperature if the diode is biased with a fixed current.

$$V_b \simeq ln(\frac{I}{AR})\frac{k_b T}{q} \simeq CT$$

The temperature coefficient is dependent on geometrical parameters (active area) but also on the chosen bias current. The logarithm ensures a lower impact of current noise on the effective accuracy of the temperature measurement.

B

Post processing script

To post process the data, the algorithm below was used to carefully remove low frequency noise coming from external source and to provide a more accurate dataset to work with. It was essential to discriminate better the zero power voltage with more reliability, excluding big oscillation that were related to high uncertainty.

The noise analysis allowed to determine the correct paramaters to identify the cut off frequency of the low pass filter. The data treatment was performed with Matlab and the script is presented below:

```
1
2  clc,clear all
3
4  meas_name  = 'dynamic_complete\5P_DIODE_TEMP';
5  power_w = ["150" "250" "400" ];
6  power_tab = [ 'w150' "w250" 'w400' ];
7  device = [ "S1" "S2" "S3" "S4" "S5" "S6" ];
8  diode.(power_tab(2)).position = ["L4",'L3', 'L2' ,'L1', 'C', 'R1','R2', 'R3', '
       R4'];
9  diode.(power_tab(3)).position = ["L4",'L3', 'L2' ,'L1', 'C' ,'R2', 'R3' 'R4'];
10 diode.(power_tab(1)).position = ["L4", 'L2' ,'L1', 'C', 'R1','R2', "R3" ,'R4'];
11
12 load('sensitivity.mat')
13 v_distance =
14 [0.826719577 3.17680776 5.473985891 8.242945326 10.63271605 13.21869489] ;
15
16 diode.(power_tab(1)).distance=
17 [-2.125 -0.425 -0.2 0 0.2   0.425 1.125  2.125];
18 diode.(power_tab(2)).distance=
19 [-2.125 -1.125 -0.425 -0.2 0  0.2 0.425 1.125 2.125];
20 diode.(power_tab(3)).distance=
21 [-2.125 -1.125 -0.425 -0.2 0    0.425 1.125  2.125];
22
23 % filter parameters
24 dv = 0.0013;
25 Fs = 1/dv;
26
27 for w = 1:length(power_w)
```

```
28      subfile = append(meas_name,'_','D',power_w(w), '_');
29      for dev = 1: length(device)
30          subsubfile = append(subfile,device(dev),'_');
31          for pos = 1:length(diode.(power_tab(w)).position)
32
33              filename = append(subsubfile,diode.(power_tab(w)).position(pos),".
                    csv")
34              % diode voltage values
35              [tension, vd_p, leg] = IVmatrix(filename,3,3);
36              % power device curret values
37              [Id_pow, vd_p, leg] = IVmatrix(filename,3,2);
38
39              % outlier elimination
40              dut.voltage = filloutliers(tension, 'nearest', 'movmean',10);
41              dut.current = Id_pow;
42
43              dut.power = dut.current.*vd_p;
44
45              % second outlier modification
46              dut.var = filloutliers(dut.voltage-mean(dut.voltage(1:20,:)), '
                    nearest', 'movmedian' , 30);
47
48              diode.(power_tab(w)).(device(dev)).(diode.(power_tab(w)).position(
                    pos)) = dut;
49
50              for vd = 1 : length(leg)
51
52                  % first linear fit
53                  dut.p(:,vd) = polyfit(dut.power(:,vd),dut.var(:,vd),1);
54                  dut.fitpow = [0:0.01:5]*1e-3;
55
56                  %%fit to eliminate the principal component
57                  dut.fft_fit(:,vd) = polyval(dut.p(:,vd), dut.power(:,vd));
58
59                  %%Fourier analysis
60                  dut.noise(:,vd) = dut.var(:,vd)-dut.fft_fit(:,vd);
61                   dut.fft_noise(:,vd) = fft(dut.noise(:,vd));
62                  dut.noise_filtered(:,vd) = lowpass(dut.noise(:,vd),10,Fs);
63                  dut.var_filt(:,vd) = dut.var(:,vd)-dut.noise_filtered(:,vd);
64
65                  %%fit over the same power values
66                  dut.p_fft(:,vd) = polyfit(dut.power(:,vd),dut.var_filt(:,vd),1)
                        ;
67                  dut.fit(:,vd)  = polyval(dut.p_fft(:,vd), dut.fitpow);
68
69                  %%subtract the intercept
70                  dut.var_filt(:,vd)  = dut.var_filt(:,vd) - dut.p_fft(2,vd);
71
72                  %%reobtain the fit  to excluede all sort of noise
73                  dut.p_final(:,vd) = polyfit(dut.power(:,vd),dut.var_filt(:,vd)
                        ,1);
74                  dut.fit_final(:,vd) = polyval(dut.p_final(:,vd), dut.fitpow);
75
76                  sens = sensitivity.(power_tab(w))(dev,pos);
77                  dut.temp = dut.fit/sens;
78
```

```
79              end
80
81              % mean value extraction
82              dut.var_mean = mean(dut.var_filt(:,end-1:end),2);
83              dut.fit_mean = mean(dut.fit_final(:,end-1:end),2)
84
85              diode.(power_tab(w)).(device(dev)).(diode.(power_tab(w)).position(
                    pos)) = dut;
86          end
87      end
88  end
```

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