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High-frequency characterization of GaN buffer losses

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It is my duty to leave this space of my thesis to the people who have contributed to its realization with their support.

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Gioacchino Giffoni

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Acronyms

DUT
Device Under Test

FOM
Figure of Merit

HEMT
High Electron Mobility Transistor

NLR
Non Linear Resonance

NLS
New Large Signal

ESR
External Series Resistance

NLESR
Non Linear External Series Resistance

PCB
Printed Circuit Board

Q
Quality Factor

RF
Radio Frequency

RHS

Right Hand Side

RMS

Root Mean Square

SJ

Super-Junction

SPT

Scattering Parameter Technique

ST

Sawyer-Tower

VNA

Vector Network Analyzer

WBG

Wide Bandgap

Chapter 1

Introduction

The Gallium Nitride (GaN) is the principal material for power electronics applications due to its outstanding properties: High Breakdown Voltage, Wide Bandgap and Large Mobility of the Electrons. Unlikely unexpected losses in GaN technology due to trap defects in the Buffer limit its performance and development as Silicon substitute. In this thesis, I am going to characterize at high frequencies (up to 100 MHz) these effects, finding a physical explanation and a solution to avoid their presence in the normal operation of the device. The first part will be focused on the field of study: The Power Electronics, only after this, I will pass to GaN, its advantages and devices; at the end of the chapter these loss effects will presented.

1.1 Power Electronics

Before of starting with more specific and complex concepts, it is better to understand what is the field to which my thesis refers: Power Electronics. Power Electronics is the branch of electrical engineering focused in the conversion and manipulation of electrical power through the use of semiconductor power switches like diodes, power transistors and in our case GaN High-Electron Mobility Transistors (HEMTs).

Always more applications are found that need a power system like automotive, battery charges, electronic devices, etc; in general the raw power supplied at 50 Hz from the common plugs have to be converted to provide the suitable power for the system considered.

The power conversion systems can be classified in four types according to the kind o power:

1. AC to DC (rectifier),
2. DC to AC (inverter),
3. DC to DC (chopper),

4. AC to AC (Cycloconverter or AC voltage controller).

So, why this power converters are so important, it has been estimated that now at least half of the USA power flows through power converters and in the future this trend will reach the 100% [1].

In order not to dwell too much, I will not discuss how all types of power converters work and are made, the most curios reader can read the book of A. M. Trzynadlowski, Introduction to Modern Power Electronics [1], where I have taken some information presented in this chapter.

I want to talk about the evolution and the problems that these systems are finding in the current technology; in the last years a constant increase about the power consumption and volume reduction has required an improvement in the power losses (lower) and switching frequencies (higher) (remember that the power converters can be schematized with several switches that should be turned on or off as fast as possible [1]) that were limited by the Silicon and so a new material have to be used for the future power electronics.

An important parameter of these systems is the output power density that is defined as the output power divided by the total volume so an higher value means a smaller system, the Fig. 1.1 [2] shows an exponential increase over the last 30 years.

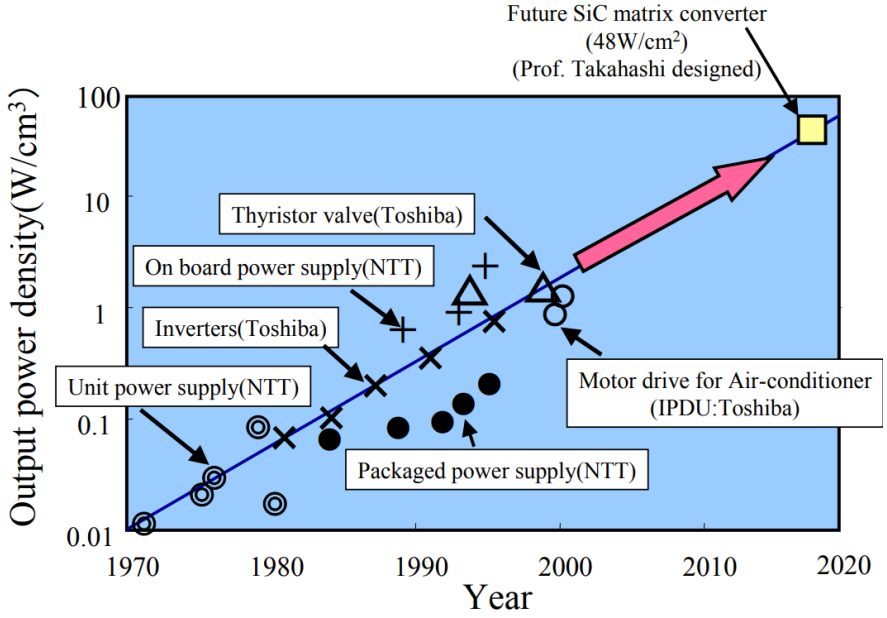


Figure 1.1: Output power density improvement [2]

Another important aspect to be considered is the fact that the larger part of these systems is occupied by heat sink, magnetic components and capacitors, so

for having an effective reduction of the volume we need before to reduce the power losses in order to use smaller heat sink and so in this way increasing the switching frequency enabling the use of smaller passive components.

Furthermore it has been shown from the data by NTT a relation between output power density and power loss, the former increases when the second one decreases (Fig. 1.2).

Similarly also from the switching frequency operation, we have an effective reduction of the volume, in [2] it has been shown the same relation for frequency and output power density; to finally achieve the higher frequency and lower loss, we need to improve the power semiconductor device because practically the half of the total losses in these systems come from their operations and increasing the frequency leads to an unwanted increase of its loss so limiting their use to an upper bound.

Why we cannot continue to use the Silicon as main material for high power devices, to show its main problem we need to refer to the its switching speed limit that has been computed analytically in [2] and it is limited by the square of the critical electric field, the mobility of the majority carriers and the drain-source voltage.

The limitation of these parameters have shown the need of a new material for the future electronic power applications that has been identified in the Gallium-Nitride (GaN).

1.2 Why is GaN so important in Power Electronics?

Gallium Nitride is a wide bandgap (3.4 eV, three times the Si one) semiconductor with an hexagonal crystal structure.

The bandgap determines the quantity of electric field that a device can support before breaking, so the GaN one allows the development of devices with a really narrow depletion region, obtaining structures with high carrier density while reducing the energy loss and the volume.

The main difference with the Si technology, it the possibility with the GaN to have higher electric field in smaller regions, resulting in faster switching; moreover, GaN devices can work also at higher temperature (melting point of 1600°).

Another important aspect that has been shown it is the possibility with the correct GaN design to have power transistors with also ten times lower carbon footprint than the Si ones. In the future, it has been estimated that the Si-on-GaN integration will reduce the energy loss also up to 40% which is translated in much less CO_2 emission.

Then the GaN manufacturing in clean room can save up to 80% of energy and

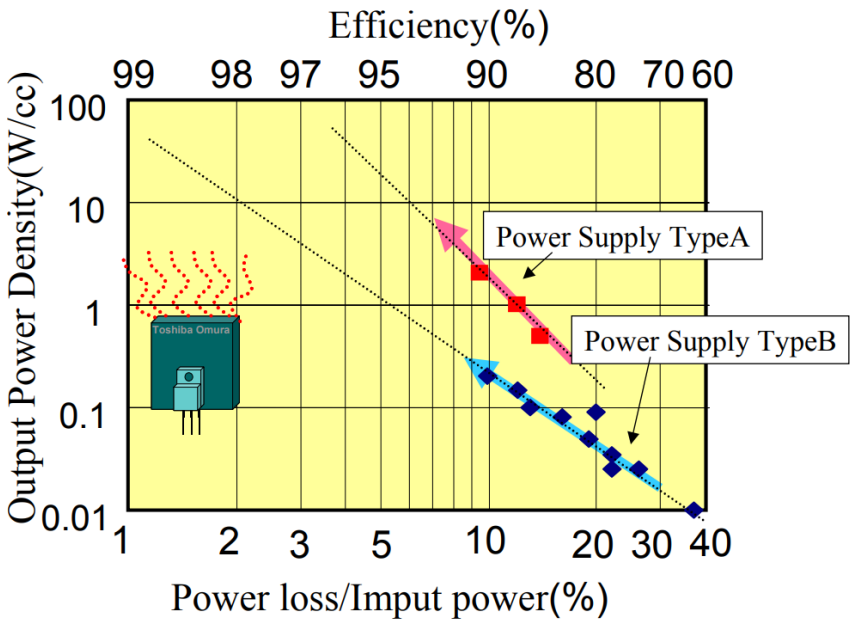


Figure 1.2: Relation between output power density and power loss of converters [2]

chemicals used and more than 50% in packaging, so the GaN has a clear eco friendly advantage with respect the Si.

The GaN has been mainly used in the manufacturing of LEDs and RF component but now it is moving towards more power switching and conversion applications for example GaN can enable three times faster mobile charging having a much smaller adaptors than Si ones (more power to the battery due to lower Resistance and Capacitance).

Finally, considering all these aspects together the GaN power High Electron Mobility Transistors (HEMTs) present at least 10 times higher switching frequency of the Silicon devices, another important figure of merit is the product of the on-resistance and the gate charge that can be up to 20 times better than Si one (smaller transistors) but parasitic elements that will be the main topic of these thesis can unexpectedly limit the total performance.

1.3 GaN High Electron Mobility Transistor

Before explaining the technology limitations and the parasitic effects of GaN HEMT, I wanted to give a brief explanation about the design and main advantage of this device.

For the substrate, we can have several possibilities like Si, SiC or *sapphire*, each with different characteristic and advantages. On top of the substrate, it is deposited a buffer layer made typically by GaN or AlN that works as the seed for the epitaxial growth of the GaN layer that will be the channel where electrons flow and on top there will is an AlGaN layer that works as a physical barrier and creates the 2 dimensional electron gas (2DEG) in the GaN interface, the device design is presented in the Fig. 1.3.

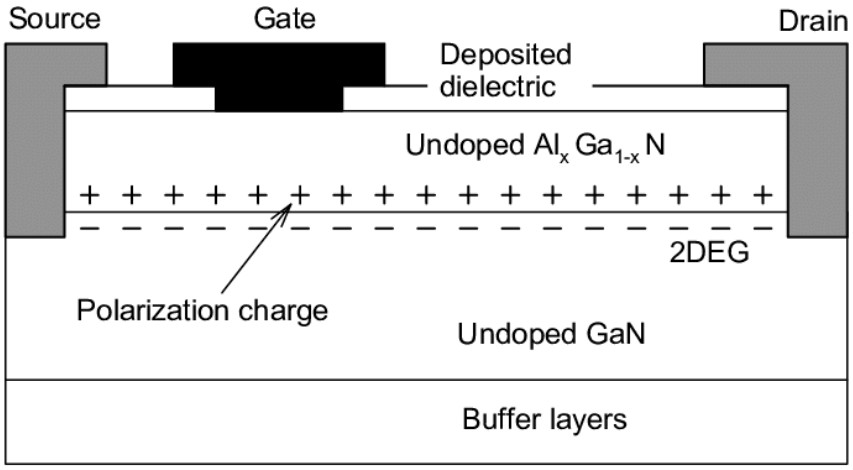


Figure 1.3: Cross Section of an HEMT

Finally, we deposit the Source, Gate and Drain electrodes, they can have several configurations and geometries, the more common is the field plate structure (not represented in the Fig. 1.3) that is characterized by a deposition of an insulator (SiN) above the electrodes and on top the same metal but only up to the gate. This configuration is used to decrease the electric field maximum inside the device that allows the increase of the breakdown voltage and so the raising of the output power density. The gate is usually characterized by Metal-Insulator(SiN)-Semiconductor structure that is characterized by a deposition of a thin layer of an insulating material (SiN) under the gate electrode, this design reduces the leakage current through the drain during the off state and so lower power loss.

This device presents several advantages with respect the Si MOSFET there at least five parameters that are optimized with this technology:

1. Smaller On-Resistance
2. Higher Drain Current
3. Higher Switching frequency

4. Lower Gate (Leakage) Current
5. Higher Breakdown Voltage
6. High 2D electron gas density with high mobility
7. Lower Output Charges

which leads to have outstanding performance comparing with the state-of-the-art Si devices.

These kind of device is far from perfection, there are several issues that must be overcome, for example:

1. Larger chip area, for kW power application we need a size $> 10\,\mathrm{mm}^2$.
2. Higher interconnection resistance due to the large current to be driven between Source and Drain that can cause a large voltage drop.
3. Normally on characteristic that presents higher power consumption with respect the more suitable normally off device, the ration of the leakage current to the conduction one is not small enough.
4. Low Reliability that denotes a high risk for the total system and also for the companies.

Moreover, some unexpected losses are present during the normal operation, that will be analyzed in the remaining chapter.

1.4 Power loss in GaN

The GaN HEMT, with its incredible properties, allows an almost lossless conduction and a very high switching frequency; these results entail the lowering of filtering (less passive components) and cooling (smaller heat sink) implying an outstanding power density.

One of the most hard part of the manufacturing was the epitaxial growth of the GaN on Si to overcame the large mismatch of their lattice constant, for this reason several others layers are deposited in the between, at the end a large amount of buffer traps are present.

GaN has several loss mechanisms not completely understood, the main ones are the dynamic $R_{ds,on}$ phenomena and the output capacitance, C_{oss}, losses that limit the potential of these devices.

The first effect is related to the dynamic on-resistance (R_{ON}) that is constituted by channel resistance, the source/drain access region resistance and the contacts.

In static condition R_{ON} is low due to the 2DEG but when we switch from a high voltage off state to the conduction one, we observe an increase of the resistance, this phenomenon is called Dynamic R_{ON} degradation.

It is explained by trapped charges in the buffer or in the passivation layer that entail a depletion of the 2DEG, so a diminution of the density of majority carriers, leading to an increase of the resistivity [3]. Why happens this phenomenon? The physical explanation of this effect includes two main points:

1. At off state with high drain bias, the V_{GD} is so negative that electrons can be scattered in the traps of the Buffer.

2. At High Voltage during hard switching, the electrons can be generated in the 2DEG and then injected in the Buffer, going back to the one state, the trapped charges cannot be released instantaneously.

Other possible causes of the increase of the RON exist and are described in [4]. Despite this phenomenon has not been completely solved by the manufacturers (the field plate was one of the solutions that was found for limiting hot electrons), it is well characterized in [3] and [4].

The second mechanism is more complicated, it describes the losses due to the charging and discharging of the output capacitance C_{oss} of the transistor, so affecting the performance of the soft-switching operation. Soft switching ideally means that during the on or off state of the operation of our device, we should have zero loss, this should be also the case for the GaN but recently this behavior failed and also its soft switching is pretty lossy, compromising its efficiency and working principle. There are many evidence of this phenomenon in literature like in [5] or [6] but only not proved hypotheses have been made on the origin of this phenomenon. This kind of Loss is the main subject of my thesis and more details are present in the next chapters.

1.5 Defects in GaN HEMTs Buffer

The reason behind the losses in GaN HEMTs is the non ideality of the several depositions for having a good GaN interface with almost no leakage. These processes cause the formation of the parasitic capacitance that will be present in our final device, see Fig. 1.4 for the schematic.

In total we have three capacitors, the drain-source capacitance, C_{d-s} is defined as the capacitance between the source and the drain metal including the field plate and the 2DEG then in parallel there is the gate-drain capacitance, C_{g-d}. In my thesis, the DUT was always PTO so these elements are in general considered lossless as long as the dielectric can be assumed nearly ideal and there is no potential drop applied across the gate that could cause the injection of holes.

Differently from the two others capacitors, the third one is constituted between source or drain and the substrate in which the dielectric is the buffer itself which can show intrinsic losses, indeed the 95% of the losses of the device, when is PTO, are due to this element.

The main role of the buffer is to provide an electrical insulation between the substrate and the GaN channel when a non zero V_{DS} is applied to the DUT. This epitaxial layer forms a vertical capacitance with ideally a zero leakage current (I_{leak}), actually I_{leak} increases with V_{DS} but for typical static conditions, its contribution to the losses can be neglected.

However the losses related to dynamic condition can be more significant depending on the structure of the buffer. Usually it is constituted by several layers: an aluminium nitride on the bottom that has a very good interface match with the Si substrate, then several layers for compensating the thermal expansion mismatch between Si and the remaining III-N buffer, obtaining a sufficient good quality base for the GaN channel.

Moreover for increasing the insulating of these layers, some deep traps are introduced during their growth; the most common is carbon (C), that beyond to be fully compatible with the Si-CMOS technology, it has been shown that an increase concentration of carbon leads to a significant lowering of the leakage current, the reason is not still clear. Other advantages concern the dynamic conduction, allowing a fast discharge of the GaN channel and the buffer from the trapped or stored charges, decreasing the $R_{DS,on}$ phenomena.

Then recently it has been hypothesized ([6]) that C atoms also isolate the structural defects of the buffer so that the distance between these defects could become so small to enable defect-to-defect interaction; thanks to several electrical measurements, the existence of this defect band has been proven so it must be considered for the transport mechanism.

We can conclude that the resistive behavior of the C-band is responsible for a fraction of the losses in addition to the presence of others traps mechanism in the buffer that can cause the hysteresis behavior of C_{OSS} with the resulting losses.

1.6 Conclusion

This quick summary of Losses in GaN HEMTs finishes this part of the introduction but the next chapters will be characterized by more insights. I started with a short preface about the field of study of my thesis: "The Power Electronics" and after I presented the major material for application in this branch of Engineering: the GaN with all its advantages with respect the Si. Then a short description of the main device based on GaN: the HEMT, its physical design with its main aspects, showing also the better performance comparing to the Si MOSFET. Finally, some

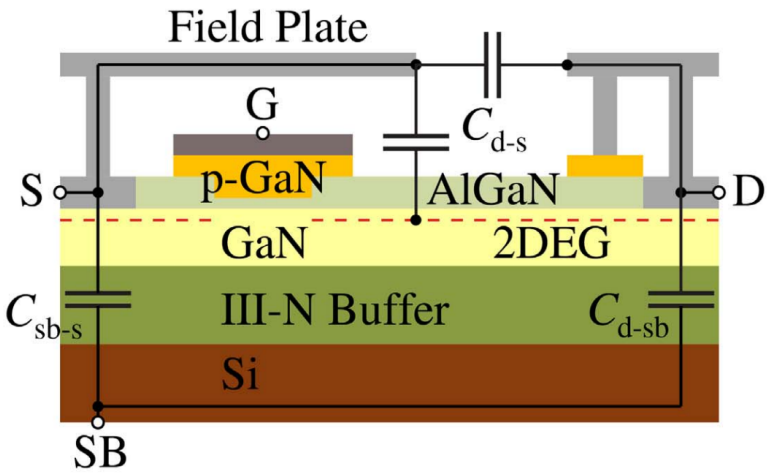


Figure 1.4: Cross Section of a GaN HEMT showing the main parasitic capacitors [6]

unexpected losses are presented with a major focus on the degradation of the on-resistance, since its effects have been fully understood; and the C_{OSS} Losses on which my work is based, so the investigation on defects in GaN HEMT Buffer are fundamental for understanding the physical reasons behind these kind of losses that limit the performance of this device and cause the Hysteresis in the charge and discharge of the Output Capacitance. Before of that, in the next chapter, some theory about this phenomenon and the main methods used for its evaluation have been reported.

Chapter 2

State of the Art

The identification on the physical phenomenon behind the C_{OSS} Losses is a really important achievement that this thesis aims to have, but before the continuation of the analysis of this effect, we need two important points: the mathematical theory behind this effect, since we need to understand the physical parameters that can affect it, and the main methods used for its evaluation nowadays in the more modern labs.

This chapter will cover these points, I will start with an easy theory on C_{OSS} losses, called "Linear ESR", reaching more complicated ones.

After, I will start my state of the art presentation of the more used techniques for the measurement of C_{OSS} hysteresis, dividing in large and small signal that are present also in the future analysis in the next chapters.

At the end, together with these methods, I will briefly describe a new technique developed during my studies that I compared with the others already present.

2.1 Mathematical Description of losses in GaN HEMTs

The investigation on the Output Capacitance Loss of soft-switching power converters has showed a relation with the voltage-swing, the frequency and dV/dt, in general these hysteresis losses can be expressed by the Steinmetz equation:

$$E_{DISS} = k \cdot f^{\alpha} \cdot V^{\beta}$$

So the dissipation energy is related to the frequency (f) and the voltage (V) instead k is a constant and α and β are two experimental exponents. IN the most of cases, the device gets permanently turned off by shorting the source and gate, so that the device can be schematized by a simple capacitor.

Actually for the evaluation of the losses, the device is modelled in a different way; one of the easiest way is to consider the series of an output capacitance (C_{OSS}) with an external serial resistance (ESR) to obtain the asymmetry of the charging discharging behavior, in this way the corresponding energy dissipation can be measured by analyzing the root mean square (rms) current $i_{ac(rms)}$ of a sinusoidal large signal voltage applied between the drain and source (V_{DS}), the result is as following:

$$E_{DISS} = \frac{i^2_{ac(rms)} \cdot ESR}{f_{sine}}.$$

Another way for analyzing the lossy behavior of our device is to consider the power dissipated (P_{DISS}) through the ESR that can be expressed considering the current equal to $i_{AC} = C_{OSS}\frac{dV_{DS}}{dt}$, obtaining:

$$P_{DISS}(t) = ESR(C_{OSS}\frac{dV_{DS}}{dt})^2.$$

Integrating both sides from t = 0 to some arbitrary time, we get:

$$E_{DISS}(t') = \int_0^{t'} ESR \cdot C^2_{OSS} \cdot (\frac{dV_{DS}}{dt})^2 \, dt.$$

By taking t' = T , the time period of the input waveform and replacing in the integral, we can separate the energy in two additive terms (constant ESR for simplicity):

$$E_{DISS} = ESR[(\int_0^{V_{peak}} (\frac{dV_{DS_c}}{dt} \cdot C^2_{OSS}\, dV_{DS_c}) + \int_{V_{peak}}^0 (\frac{dV_{DS_d}}{dt} \cdot C^2_{OSS}\, dV_{DS_d})]$$

from this equation we can observe the dependence of the dissipated energy from the rate of change of voltage across the C_{OSS} during the charge and discharge periods. Moreover we can observe that for a perfectly symmetrical behavior of the V_{DS} across the capacitance, the value of ESR must be equal to zero which leads to zero the Right hand side (RHS) of the previous equation and so having a perfectly lossless behavior of the output capacitance.

2.2 Linear Model

Based on how we model the ESR we have two different methods: the linear model and the non linear one. This section is dedicated to the former which considers the ESR as a constant, trying to develop a real model that can be used for measuring the actual losses.

Let's consider a special case, in which we approximate a sinusoidal waveform by a triangular one with equal rising and falling time, t_{SW}, in this way $\frac{dV_{DS}}{dt}$ is constant and can be taken out of the integral; the dissipation energy can be computed as:

$$E_{DISS} \approx 2 \cdot ESR(\frac{dV_{DS}}{dt}) \int_0^{V_{peak}} C_{OSS}^2 \, dV_{DS}.$$

This equation can be rewritten as

$$E_{DISS} = 2 \cdot ESR(\frac{dV_{DS}}{dt}) \cdot V_{peak} C_{OSS}^{eff2}$$

in which we introduced the new term C_{OSS}^{eff} which is the rms of C_{OSS} from 0 to V_{peak}

$$C_{oss}^{eff} = \sqrt{\frac{1}{V_{peak}} \int_0^{V_{peak}} C_{oss}^2 \, dV_{DS}}.$$

We can still simplify the dissipation energy using $f = \frac{1}{2t_{SW}}$, obtaining:

$$E_{DISS} = 4 \cdot ESR \cdot f \cdot V_{peak}^2 \cdot C_{OSS}^{eff2}.$$

Linking this equation to the Steinmetz (the first one of this chapter), we get $\alpha = 1$ and $\beta = 2$. So for a fixed value of ESR, we get $\alpha = 1$ but in general how it has been reported in [7], α is lower than 1, this leads to a ESR that must be frequency dependent; also for β we have the same observation, indeed the C_{OSS} related term leads to a value lower than 2 since it decreases when the voltage increases.

This method is exploited for small signal analysis and it is less powerful of any large signal ones but much simpler, indeed we start with the extraction of the effective C_{OSS}, using data reported in datasheets, obtaining also an equation dependent on the voltage then with an impedance analyzer (small signal measurement), we measure the ESR as a function of the frequency (it is almost constant in function of the voltage and on the contrary for the capacitance).

Putting all together we have a closed equation in function of the frequency and voltage of the energy dissipation. This method is very easy and it is used to compare different Wide Band Gap (WBG) semiconductors.

There are several problems using this method: we do not capture the total shape of V_{DS} versus Q_{OSS} unlike of the next methods and so do not model the energy losses correctly and it is invalid for modeling the large signal measurements. Moreover if we do not work in the hysteresis region, we can never capture the essence of this phenomenon, since this region is not stable, we cannot trust blindly on the gathered data.

2.3 Non linear Model

A more exact but hard model is the non linear one in which we assume in the equations two addictions:

- Non-linearity of C_{OSS} indeed we know at this point that the output capacitance depends on the drain source voltage

  $$C_{OSS} = C_{OSS_0} - CDOL \cdot V_{DS}$$

  where C_{OSS_0} is the drain to source OFF-state capacitance and CDOL is the first order voltage coefficient

- Non-linearity of ESR (NLESR), also the ESR has a dependence on the drain source voltage and can be approximated as

  $$NLESR(V_{DS}) = \alpha \cdot V_{DS}^2$$

  where α is a coefficient, since the exponent on the last equation is 2 we can say that NLESR is proportional to the power content of the applied signal.

Experimentally it has been shown that α is not a constant and change with V_{peak} so we need to compute an average NLESR:

$$NLESR_{avg} = \frac{\int_0^{\pi} \alpha \cdot V_{peak}^2 sin(\frac{\omega t}{2}) \frac{d\omega t}{2}}{\pi} = \frac{\alpha \cdot V_{peak}^2}{4}.$$

Here we supposed that the charging and discharging period of the sinusoidal voltage are symmetric so we can perform the integral just in half the period. Moreover considering that the average of NLESR is the average resistance that the DUT encounters during the hysteretic cycle and by assuming that $NLESR_{avg}$ is a linear function of the maximum of $\frac{dV_{DS}}{dt}$ so $NLESR_{avg} = m \cdot \frac{dV_{DS}}{dt}_{max} + C$, we can calculate the energy dissipated per switching cycle as:

$$E_{DISS(AVG)} \approx \int_0^{V_{peak}} [m \cdot \frac{\frac{dV_{DS_c}}{dt}^2}{cos(\frac{\omega t}{2})}$$

$$+C \cdot (\frac{dV_{DS_c}}{dt})] \cdot C_{OSS}^2 \, dV_{DS_c}$$

$$+ \int_{V_{peak}}^{0} [m \cdot \frac{\frac{dV_{DS_d}}{dt}^2}{cos(\frac{\omega t}{2})}$$

$$+C \cdot (\frac{dV_{DS_d}}{dt})] \cdot C_{OSS}^2 \, dV_{DS_d}.$$

In conclusion the NLESR model predicts a dependence of the energy dissipated both on the $(dV/dt)^2$ and dV/dt of the drain to source waveform, it is more accurate in the calculation but also more complex. Unlike the linear ESR model, NLESR model lacks of a physical explanation because does not fit the theory on dielectric absorption or any other established theory.

These two models have tried to prove the physical relations of the output capacitance losses, relating to several parameters, now it is time to present the main techniques used for the correct evaluation of this effect.

2.4 Sawyer-Tower Analysis

The main method for the evaluation of the C_{OSS} loss mechanism is the so called Sawyer-Tower (ST) technique (Fig. 2.1), in which we keep the DUT permanently OFF, short between source and gate, in series with a reference linear capacitance (C_{REF}) then we apply a large signal sinusoidal voltage thanks to a signal generator and an high voltage amplifier through its drain and source, since the current is the same, the stored charge in C_{REF} and in C_{oss} is supposed to be equal, this is valid only if the leakage current in the DUT is smaller than the drain current (I_D), if not we can observe a fake hysteresis.

By measuring the charge (voltage across C_{REF}) in function of the voltage across the DUT during the charge and discharge process, we can note an hysteresis that gives us a direct measure of the total losses in one cycle.

In more details, if we consider the circuit of the ST method (Fig. 2.1) and apply a large signal to the drain, the charge Q_{OSS} across the non linear capacitance and the charge stored in the ideally loss-less linear capacitance C_{REF} are the same since the series connection, so:

$$Q_{OSS} = V_S \cdot C_{REF},$$

&

$$V_{DS} = V_{YX}.$$

The asymmetry due to the charge and discharge of C_{OSS} is the principal cause of the power dissipation. By measuring two distinct voltages V_X and V_Y, we can plot V_{DS} in function of Q_{OSS} and compute in an entire cycle the hysteresis and evaluate the losses.

Mathematically speaking if we define V_{DS_c} and V_{DS_d} as the charging and discharging voltages across the capacitor C_{OSS} and E_{OSS_c} and E_{OSS_d} the corresponding charging and discharging energies per switching cycle, we have:

$$E_{DISS} = E_{OSS_c} - E_{OSS_d} = \int_{Q_i}^{Q_f} V_{DS_c}\, dQ_{OSS} - \int_{Q_i}^{Q_f} V_{DS_d}\, dQ_{OSS},$$

where Q_i is the initial charge on the capacitor which is zero and Q_f is the final charge corresponding to the peak of an eventual sinusoidal voltage applied. From this equation and the two at the beginning, we can easily compute the dissipated energy by just measuring two voltages and solving two integrals, this is the way in which the ST method works.

One problem that concerns C_{OSS} is its not linearity in function of the drain and source voltage (varying also some orders of magnitude), the choice of C_{REF} is fundamental since it limits the maximum charge stored, moreover the heat during the losses can significantly affect our measurements, for example the leakage current increase with the temperature and can become comparable to the displacement current, leading to wrong measurements. Another limitation is related to the voltage swing/frequency applied before the thermal runaway of the DUT [8].

This method was originally used for the superjunction (SJ) Silicon (Si) MOSFET but in that case how has been explained by [9], the losses are due to stranded charges in the p-columns that during the depletion that can no longer flow as majority carriers. Differently from SJ, GaN HEMTs have to be a completely different loss mechanism since dopant charges are practically absent (see Chapter 4).

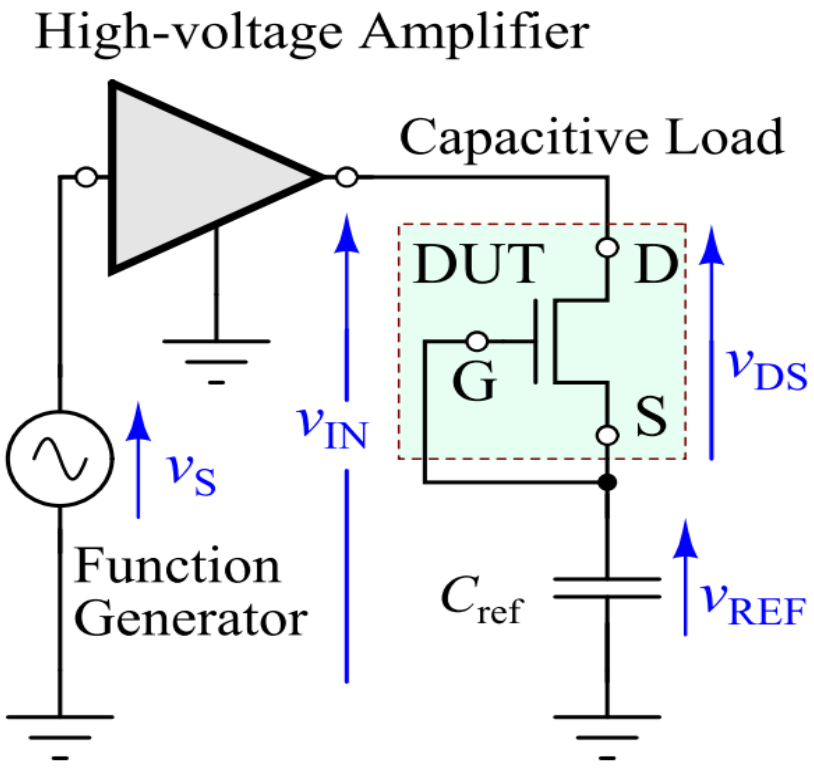


Figure 2.1: Sawyer–Tower circuit [5]

2.5 Non Linear Resonance Large Signal Method (NLR)

We have explained the Sawyer Tower method to evaluate the large signal output capacitance of HEMTs in which we basically turn off the device (short gate source) and apply a high amplitude sinusoidal waveform to our DUT and a reference capacitor. This method presents some limitations as the dependence of C_{OSS} on the choice of C_{ref} and the steady state regime measurement indeed during the analysis the device can heat up due to the losses and affect the accuracy like an increase in the leakage current that can become comparable to the displacement one obtaining an incorrect C_{OSS} hysteresis.

Another limitation concerns the maximum voltage-swing and frequency before thermal runaway, the need of high amplitude sinusoidal voltage limits the maximum frequency that can be applied, so the typical value of dV/dt for our DUT can only achieve the tens of MHz range.

For these problems, another technique has been developed [10], more robust and simple, to analyze the large signal C_{OSS} loss and the energy dissipation. This method is based on the nonlinear resonance between a known inductor and the output capacitance of the DUT, in this way the C_{OSS} and E_{DISS} can be measured under a single pulse condition which eliminates the effect of self-heating and there is no thermal limit to the maximum voltage swing or frequency applied to the DUT.

The Fig. 2.2 shows the proposed circuit for the large signal measurement, the transistor remains on for t lower than t start, charging the inductor, then by turning off, the inductor resonates with C_{OSS} and the parasitic capacitance C_{PAR}, generating a voltage pulse at the output (drain-source voltage), at this point knowing the value of L and C_{PAR}, we can extract the value of C_{OSS} and E_{DISS}.

Let's suppose that the internal resistance losses and the resistance of the gate driver are negligible; the equation that controls this process is:

$$LC(V_{DS})\frac{dv_{DS}}{dt} = LI_0 - \int_{t_0}^{t} v_{DS}(t)\,dt$$

where C = C_{OSS} + C_{PAR} is the total capacitance at the output node. At the peak of the voltage, the inductor has zero current, so we can evaluate its flux by integration of its voltage:

$$LI_0 = \int_{t_0}^{0} v_{DS}(t)\,dt.$$

Replacing in the first equation, we can evaluate the capacitance as:

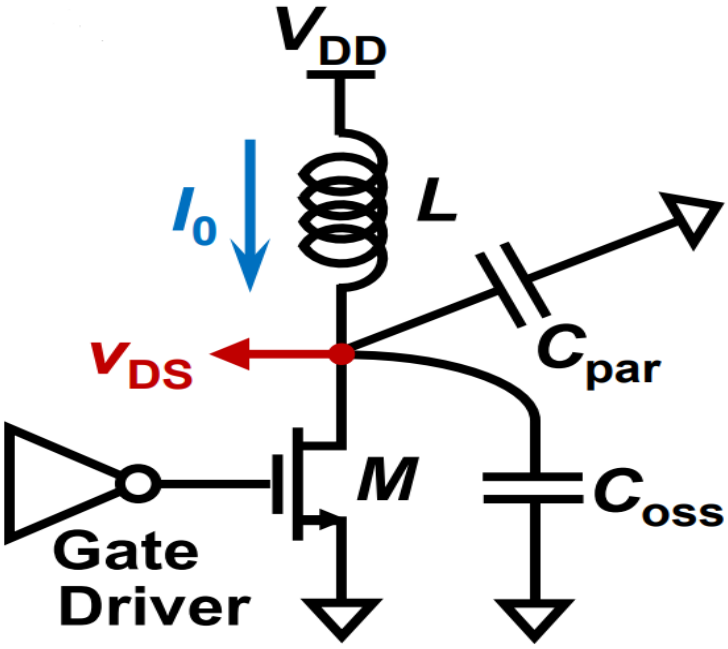


Figure 2.2: Circuit for Non Linear Resonance Large Signal C_{OSS} Analysis [10]

$$C(V_{DS}) = \frac{\int_{t_0}^{0} v_{DS}(t)\,dt - \int_{t_0}^{t} v_{DS}(t)\,dt}{L\frac{dv_{DS}}{dt}}.$$

This equation shows that the capacitance is a function exclusively of V_{DS}.

Before discussing the energy loss, we have to note that the output voltage starts from 0 at t = t_0, increases to a maximum V_{max} at t = 0 and then again decreases to 0; in the case of a symmetrical behavior the device does not present any C_{oss} hysteresis that characterize only asymmetrical behavior.

Starting from the last equation, we can calculate the energy exchanged by C_{oss} during a time interval T:

$$E_T = \int_T v_{DS} C(v_{DS})\,dv_{DS}.$$

After replacing in the equation and considering the charging time as T = [t_0,0] and discharging time as T = [0,t_1], we can easily extract the energy to charge the capacitor and then released as:

$$E_{OSS}^{ch} = \frac{1}{2L}(\int_{t_0}^{0} v_{DS}(t)\,dt)^2$$

&

$$E_{OSS}^{disch} = \frac{1}{2L}(\int_0^{t_1} v_{DS}(t)\,dt)^2.$$

Their difference gives the energy dissipated in C_{OSS}:

$$E_{DISS} = \frac{1}{2L}\,((\int_{t_0}^{0} v_{DS}(t)\,dt)^2 - \frac{1}{2L}(\int_0^{t_1} v_{DS}(t)\,dt)^2)).$$

This method relies only in the integration of a single voltage signal that can be measured also at ultra-fast cycles (below 10 ns). If we use a large value of the inductor L we can get small resonance frequencies, however with small value of L we can use larger value for the frequency and dv/dt.

2.6 Scattering Parameters Small Signal Analysis (SPT)

All these methods are large Signal so really precise but due to the circuit, they cannot be applied directly on wafer, in the previous chapter we found that one of the source of losses on GaN HEMTs concerns the epitaxial structure, so the Scattering Parameters Small Signal Method can be used for a direct analysis [11].

The frequency limit of the examinations on commercial devices is typically less than 40 MHz, farther the packaging and external connections do not allow an accurate measurement of C_{OSS}. This method can characterize the dissipated energy at high switching frequencies, ideally we can work also at value well beyond 100 MHz.

This method uses a small signal model by considering the approximation that at high voltage, C_{OSS} becomes constant and approximately equal to C_{epi} that is the drain-substrate capacitance (through the Buffer) that represents the main source of loss.

This capacitance is sandwiched between drain pad and Si substrate, so it depends on the area of the drain pad that will be where we apply the signal, we have also a ground pad all around with dimensions such that the effect of the fringing fields can be neglected and forming a giant capacitance with the substrate which practically ground the Si substrate at radio frequencies (RF).

The schematic of our DUT is shown in the Fig. 2.3, where it is approximated by a capacitor of value C_{epi}, by applying an incident wave from a Vector Network Analyzer (VNA) with amplitude V_{inc} and measuring the reflected wave V_{ref}, we can extract the gamma factor as $\Gamma = V_{ref}/V_{inc}$ in function of the frequency. We expect that a lossless device shows the total reflection of the incident wave and so $|\Gamma| = 0\,\text{dB}$ while a lossy capacitor results in a partial reflection and so $|\Gamma| < 0\,\text{dB}$. At this point, we can extract the impedance of the DUT:

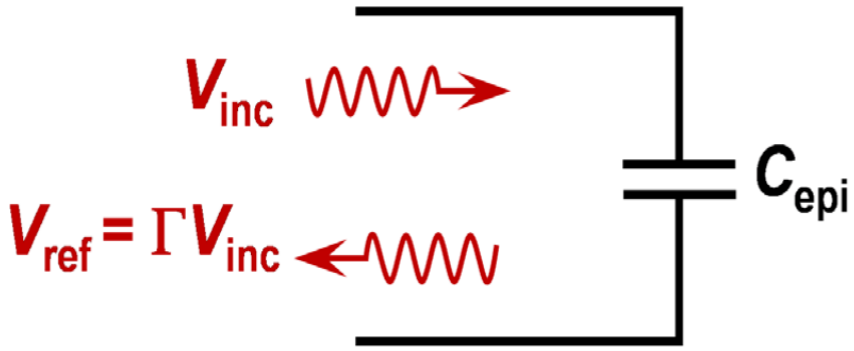


Figure 2.3: Measurement Method of Scattering Parameters Analysis Of C_{OSS} Losses [11].

$$Z = Z_0 \frac{1+\Gamma}{1-\Gamma}$$

where $Z_0 = 50\,\Omega$ is the measurement port characteristic impedance. The quality factor Q of the capacitor is obtained as $Q = Im(Z)/Re(Z)$ where Im(Z) and Re(Z) represents the imaginary and real part of the impedance. For a capacitive element, the amount of charging and discharging losses can be expressed with the equation:

$$E_{DISS} = \frac{\pi}{2Q} E_{tot}$$

where $E_{tot} = 1/2CV^2$ is the total energy stored in the capacitor when charged to the voltage V; so $\pi/2Q$ represents the percentage of energy losses.

In [11], this method was used to measure several test structures and has highlighted the presence of two lossy peaks at 17 MHz and at 90 MHz, showing the importance to test our devices for frequency normally higher than the usual one. For this reason, for large signal measurement, it is better to use the pulse excitation instead of ST method. Therefore this method has also the potential to reveal other types of power dissipation, including resonant and leakage losses, confirming this is the ability to show $1-2\%$ loss over a wide range of frequencies, which indicates the possibility to capture the background losses caused by other phenomena as substrate resistivity.

2.7 New Large Signal Method: Schematic (NLS)

Until now I have explained two large signal methods and one small signal one with their pros and cons, but at the beginning of my thesis, my group noticed the need to have a new large signal method, more general, that includes the ST and the Non Linear method but that allowed to overcome them, indeed we wanted to be able to perform a large voltage measurement directly on wafer to be able to characterize completely the C_{OSS} loss of GaN HEMT.

For this reason we started thinking a new way in which we could perform the measurement, avoiding the series reference capacitance or inductor that is the cause of the strict limitations of these methods; at the end we come up with a new type of measure.

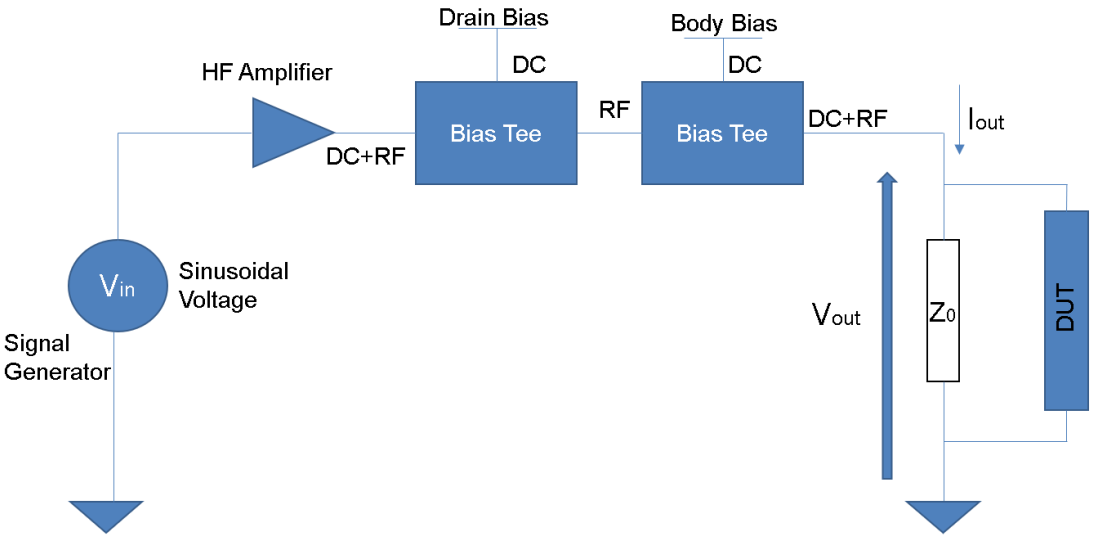


Figure 2.4: Schematic of the New Large Signal Technique.

This method has been schematized in the Fig. 2.4, in the next chapter I will show a real implementation and use; we start from a signal generator that corresponds to the sinusoidal input, this signal passes through an high frequency class A amplifier which is biased by a voltage supplier (Drain Bias) thanks to a Bias Tee. The amplified signal passes through another bias tee that increases its mean value by superimposing a DC voltage equal to the amplitude of the signal through another voltage supplier (Body Bias). Finally we supply this signal to the output that is constituted by our DUT and a reference impedance due to the setup (connectors and adaptors) that must be evaluated and considered in the successive analysis.

The measure is based on the evaluation of both signals: voltage and current at the output with two different probes, these will add the need of a calibration to

our analysis.

The final results are extracted by the following equations:

$$Q_{OSS} = \int_0^T i(t)\,dt$$

&

$$E_{DISS} = \int_0^t i(t) * v(t)\,dt$$

more details and explanations about these equations are reported in the next chapter.

This method is revolutionary for some incredible characteristics, it allows to measure on-wafer chip, possibility to apply a signal different from a sinusoidal voltage that allows the possibility of partial hysteresis analysis in which the applications of sinusoidal voltages with different minimum and mean are considered and the not need of reference capacitor or inductor for the setup.

All these advantages are summarized in the table 2.1 in which all the methods presented in these thesis are compared.

Comparisons of Methods for C_{OSS} Losses measurement						
Methods	Large Signal	T Ind.	Partial Hysteresis	On-Chip	No Cal.	No Ext. Elements
ST	✓	X	X	X	✓	X
NLR	✓	✓	X	X	✓	X
SPT	X	✓	X	✓	X	✓
NLS	✓	X	✓	✓	X	✓

Table 2.1: Advantages and Disadvantages of the reported methods for Output Capacitance Hysteresis Losses Measurement

2.8 Conclusion

The main focus of this chapter is the Output Capacitance Hysteresis Loss theory and practice; I have analyzed the mathematical aspect with the equations that control this phenomenon (Linear and Non-Linear ESR) with different approximations, after I preferred to present some of the more used methods like ST, NLR and SPT for the measuring of this effect, their schematic and use are explained and some of these will be present in the future chapters of the thesis.

The most relevant part is the presentation of a new large signal method, developed by me and my group during my studies, here i have just shown how it works and the schematic with its advantages with respect the other techniques.

The next chapter is completely focused on this method, more information is given and a real implementation with the successive use are described.

Chapter 3

New Large Signal Method

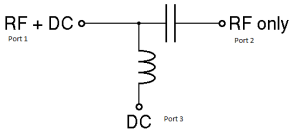
After the State of the Art about the main methods that are used to evaluate losses in power devices, here I will present a real implementation of the new large signal technique. After understanding all the tools present and how they work, I will explain how to calibrate, important step in the measurement analysis and finally I will show the first results of this method by measuring the main parameters of an RC system and its energy analysis, comparing its losses with a Spice simulation.

3.1 Prerequisites

From the last chapter, we understood the main methods used to evaluate C_{OSS} losses in power devices and also how the new method was developed and used during my thesis. Before the validation, I want to explain some elements and concepts used later in this chapter. Let's start from the bias tee, a bias tee is a three port electronic element that works as a diplexer, from the port 1 we have a signal composed by an AC and a DC component, that are divided and supplied respectively to the port 2 and 3, my Bias tee is represented in the Fig. 3.1a with also a circuit schematic Fig. 3.1b; the only difference is that in my case we used it in the opposite way, we supplied a DC signal to the port 3 that was used or to bias an amplifier or to have a only positive voltage, then the Input Signal goes from port 1 to 2 in the first case and 2 to 1 in the second case.

When it is used in the first configuration, its task was to bias a class A amplifier, Fig. 3.2 its working principle is really simple since it can use just a single device (like in my case) that is biased and amplifies the signal over the entire range of the input cycle, they have better high frequency performance indeed I needed to use it up to 100 MHz but they are generally inefficient, usually only the 25% of the input power is exploited, this means expensive power supply and heat sink, moreover we cannot expect high time life since device is always on but to overcome this problem

(a) BT-A17-S1 from Taylor Microwave, it works from 100 kHz to 500 MHz



(b) Circuit schematic

Figure 3.1: Bias Tee

our measurements were usually performed in Burst mode in which the device was active for just few µs in usually a ms period (Duty cycle lower than 1%).

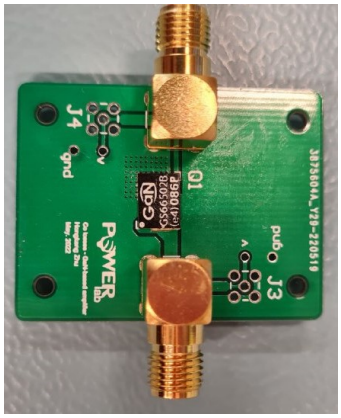


Figure 3.2: My class A amplifier, GS66502B: a GaN on SI power MOSFET

For the second configuration, I said in the previous chapter that we need to supply only positive voltage to permanently off transistors, the reason is the body diode effect: because of the doping, the source and drain form a pn-junction with the body of the transistor that is generally grounded, so during the normal polarization, applying a negative voltage to the drain or source makes sure that the voltage between them and the body polarizes positively the presented diode allowing the vertical conduction. In this way it is not possible the correct analysis of a permanently off transistors, to better understand this problem, during this thesis, the transistors analyzed in this configuration are schematized by capacitors connected to really small parasitic resistors, our task is to understand the reasons of why we have the higher than expected energy losses but having conduction means adding dominant elements that overshadows the output capacitance losses,

creating a conduction channel along the side of the device with the effect that the output capacitance is completely shorted by the diode.

Finally, the last element that is present in this new method, focus of this chapter, is a Printed Circuit Board (PCB), a structure made by a conductive and insulating layers in which electronic component are properly welded, my PCB was designed precisely for this method, showed in the Fig. 3.3. It is characterized by two SMA connectors for input and output, 2 MMCX voltage connectors for a stable ground in which we connect the Voltage Probe (Tektronix TPP1000) and an hole in the center where a wire with the signal passes through the Current Probe (Tektronix CT-1). For all the measurements, the voltage is always measured before the current so that the current probe does not measure the parasitic current inside the voltage probe, effect more dominant that measuring the additional voltage that is developed across the wire passing in the current probe (small also compared to the hundreds of Volts reached in the future analysis).

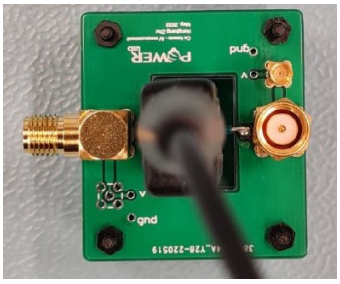


Figure 3.3: PCB with the Current Probe already connected

3.2 New Large Signal Method: Implementation

IN the previous chapter, I presented the schematic of the new large signal method, very general that includes and allows more sophisticated measurements than the others large signal techniques.

Now I want to describe a real implementation, Fig. 3.4: starting from the top part, we have the signal generator (KeySight 33600A) that corresponds to the input characterized by a sinusoidal voltage, this signal passes through a class A amplifier which is biased by a voltage supplier (MicroLab Power Supply) not present in the picture thanks to the port 3 of a Bias Tee. The amplified signal passes through another bias tee that raises it to only positive values by superimposing a DC signal (EX354 Power Supply) equal to the amplitude of the sin wave through another voltage supplier not present in the figure.

Finally, we apply this signal to input of the PCB where we measure the voltage, the sin wave passes through a wire inside the current probe and goes to the DUT

connected through a SMA port. The Voltage and Current Output measured on the PCB are then visualized thanks to an oscilloscope (Tektronix MDO3104), averaged 512 times, saved and analyzed with the Software Matlab.

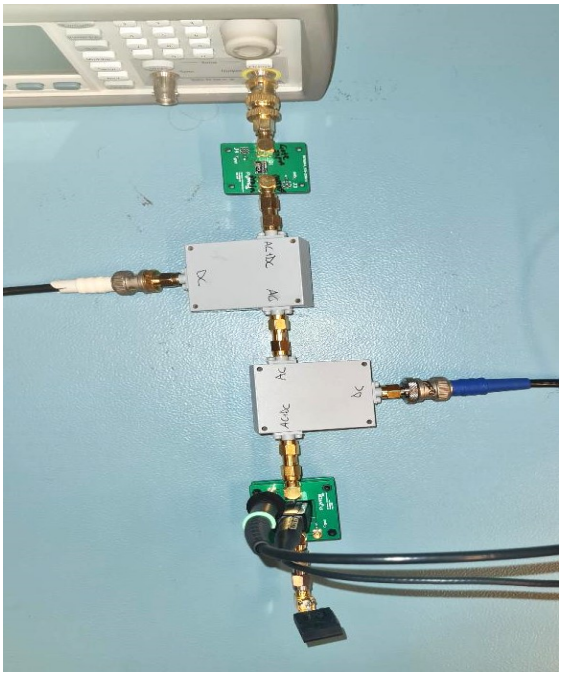


Figure 3.4: Implementation of the new Large Signal Technique

3.3 Calibration

The measure is performed with two different probes: one that measures the current and another one the voltage; our signal will be always a sinusoidal one so not constant in time; for this reason the velocity response of the two probes will not be the same, it depends on their specifications so we will have a delay in order to refer the two signals to the same time moment.

The first step was the calibration of this delay, evaluating it in function of several parameters like frequency, amplitude and bias to see how it changed. How can we evaluate this delay? The method we used was quite simple but to better understand it we need to schematize all the measurement setup.

The simplified model of our method is schematized in the Fig.3.5, at the output we have a reference impedance Z_0, by connecting in parallel an high quality factor (Q) impedance,Z , the equivalent impedance will also have an high Q since it is increased by the imaginary part of Z, moreover Q_0 is already a large value (higher

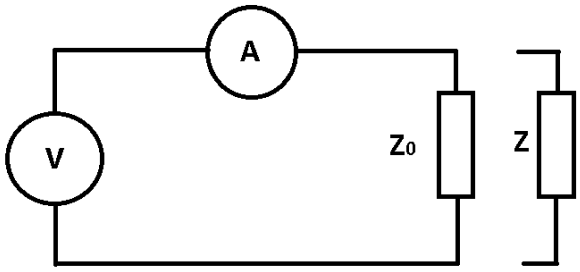


Figure 3.5: Circuit Model of the Large Signal Method

than 50 up to 100 MHz where C_0 is the maximum and is equal to 17 pF):

$$Q_{out} \approx Q_0 * (1 + \frac{C}{C_0}).$$

At this point before staring, we need to have an idea about Z_0, we used an Impedance Analyzer (KeySight E4990A), the extracted output capacitance was about 6 pF, so we just needed to choose an appropriate Z to obtain a $Q > 100$ for the entire frequency range: a 470 pF up to 2 MHz then it was not ideal anymore and I had to change reference and chose a 47 pF up to 100 MHz.

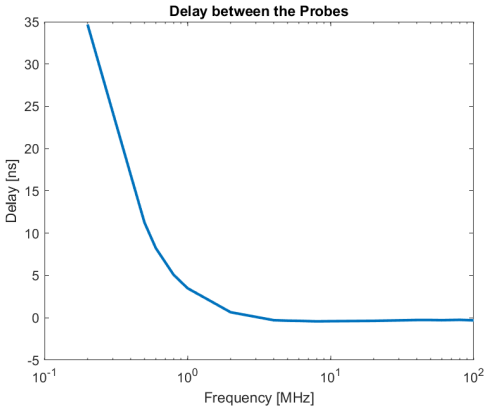
All this preparation in order to have an high Q output impedance, in this way we can consider the system lossless and so by measuring the voltage and current we can identify the mutual delay in order to minimize the energy loss of the system, mathematically speaking we want to compute the shift i with respect N points per a period of the vector Current in order that

$$E \cong \Big| \int_{-\infty}^{+\infty} v(t) * i(t - \Delta t) dt \Big|$$

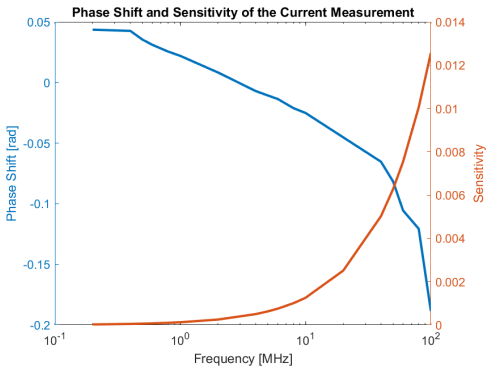
is minimum.

Applying 5 V Amplitude sinusoidal Voltage as input I measured the following results, these are not so obvious as one can think, indeed in the Fig.3.6a, we can see that the delay is not constant with the frequency and neither have a remarkable function, it decreases fast up to 5 MHz and then looks constant, around -0 4ns.

This can be considered a sort of disadvantage with respect the ST since it increases the complexity of the analysis but it is a small price to pay indeed each



(a) Delay of the Current with respect the Voltage Signal



(b) Sensitivity of the Large Signal Analysis

Figure 3.6: Calibration Results

saved data from the oscilloscope needs to be shifted by a certain value corresponding to this delay, this is also the reason why I could not measure in function of the frequency in the KHz range.

Luckily there is an important aspect: the constant region, that can simplify the computation (just by adding this delay as a deskew in the oscilloscope, if we need only frequencies higher than 5 MHz), we can consider the delay fixed in this region; this approximation may not always be true, since in the Fig. 3.6b, I have measured the phase shift,ϕ , of the vector when the delay is considered and the corresponding sensitivity,S ,of the measure that evaluates the amount of variation of the results when the delay is increased by one, both expressed as

$$\phi = \frac{delay}{Period} * 2 * \pi$$

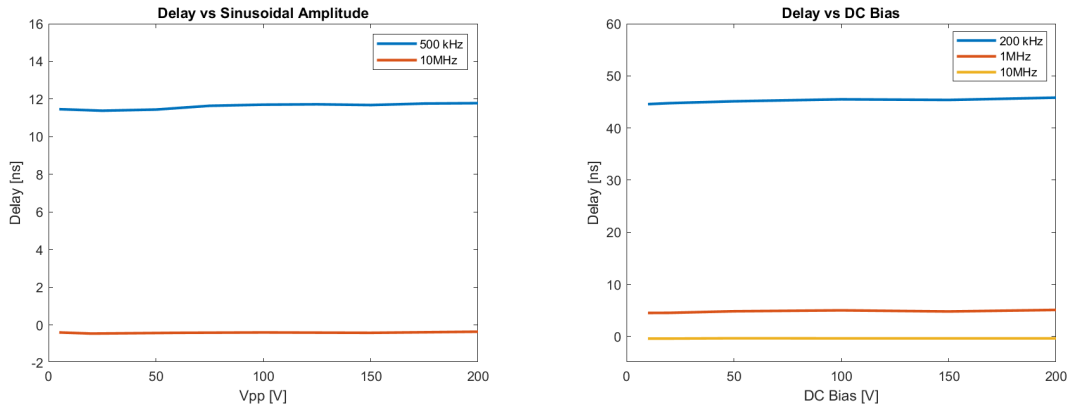
&

$$S = \phi(delay = n + 1) - \phi(delay = n)$$

they increase in absolute value with the frequency, for this reason for frequencies higher than 50 MHz, the constant delay approximation cannot hold anymore and it is needed to consider a more accurate calibration however this always depends on the amount of accuracy that we need for our results.

We have a frequency dependence of the delay between the probes, one can ask if there are others unwanted dependencies, for example if the delay changes with the amplitude of the sinusoidal voltage or with DC bias (average value over a period of the sin wave); these two analysis have been performed in the Fig. 3.7a and Fig. 3.7b and luckily there is no dependence, this saves this method because allows to

apply any kind of sinusoidal signal at a fixed frequency and the delay is determined uniquely.



(a) Constant Delay in function of the sinusoidal input amplitude

(b) Constant Delay in function of the DC bias for 10 Vpp Sinusoidal voltage

Figure 3.7: Delay Analysis

3.4 Validation

At this point, we have calibrated the method, the next step is the validation; the objective is to check if our setup can properly measure energy losses and gives us correct results. The Validation was performed by measuring and analyzing an RC system; this DUT was connected to the output in parallel to Z0. The total impedance (Z_T)was the result of a parallel combination between the DUT impedance and the setup itself so we need to reverse the formula (see Fig. 3.5):

$$Z_T^{-1} = Z^{-1} + Z0^{-1}$$

so

$$Z^{-1} = Z_T^{-1} - Z0^{-1}.$$

The first step was to model the setup impedance, just by measuring the open circuit condition of the PCB, the results are in the Fig. 3.8,this shunt element is the combination of a Capacitance of about 13 pF that increases at high frequency up 17 pF and a Resistance of 450 Ω at 200 kHz that decreases to zero at higher frequency, analyzed by an Impedance Analyzer (KeySight E4990A) from 200 kHz at 100 MHz that is also the maximum operating voltage of this method.

Knowing Z_0, after, we have connected in parallel our DUT constituted by a Capacitor (102S42E120JU3S) of 12 pF nominal and a resistor of 600 Ω in DC condition, we measured the large signals at the output by applying a 20 Vpp

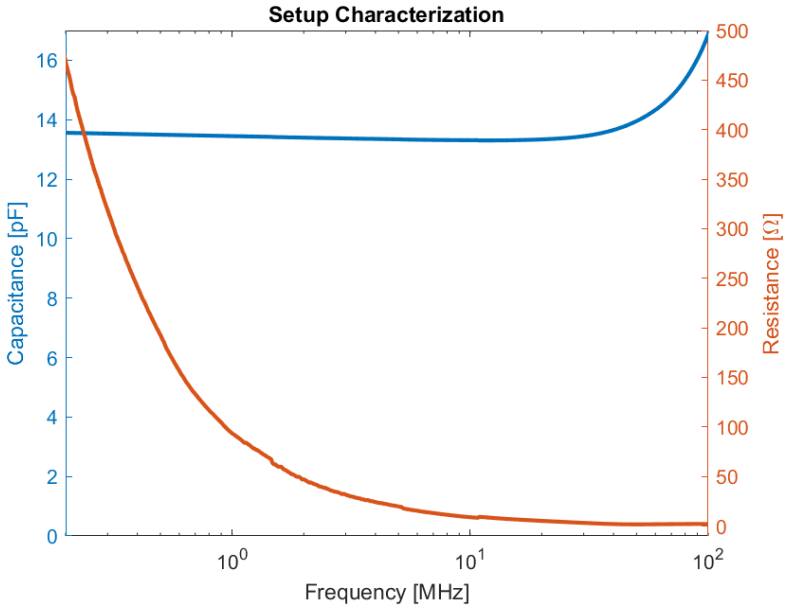


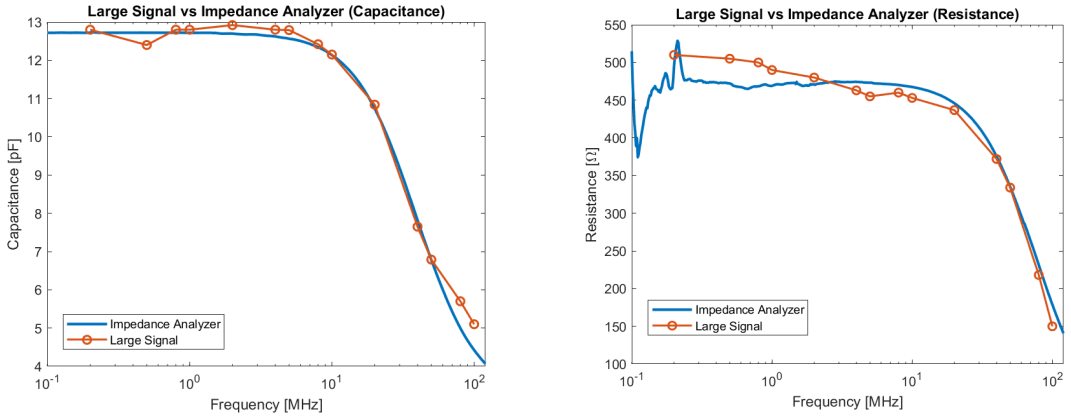
Figure 3.8: Capacitance and Resistance of Z_0

sinusoidal voltage from the signal generator, saved the output of the PCB and extracted the amplitude and phase of the total impedance thanks to the Voltage and Current: the former was measured by dividing the mean between the difference of maximum and minimum of the voltage and current, the last by measuring the shift of the normalized current (division by its amplitude) in order that the absolute difference with the normalized voltage is minimum.

Then I computed the resistance and capacitance and compared with an Impedance Spectroscopy of this device, the results are summarized in the Fig. 3.9a and Fig. 3.9b.

The match is quite good, the error is always limited around the 10% of the absolute values of the two elements, the main differences are in the Capacitance for high frequencies, likely due to the high sensitivity of the measure and to the really small value instead for the resistance, we have a larger difference at low frequencies likely due to the smaller value compared with the imaginary part of the total impedance that makes it more sensitive to the phase between the voltage and current signal (its value was really close to 90° so the cosine has its maximum derivative and so maximum sensitivity), the error could be computed by shifting the current of one point.

This method passed the RC validation by extrapolating its parameters but it was not designed for this, indeed it is not efficient since we need to know the effects of the setup and make one measure for all the single frequencies (problem solved in the last chapter) we are interested, this analysis could be really long and after



(a) Capacitance Match

(b) Resistance Match

Figure 3.9: RC Analysis

all the computations the error on the final results is affected by several steps like delay, Z_0 measure, phase measure, all these steps are not exact and can change dramatically our results overall at high frequencies.

A more stable measure and it is also the reason why we designed this method was to directly analyze the total energy of the system; that can be expressed as:

$$E = \int_{t_0}^{t_f} v(t) \cdot i(t - \Delta t), dt$$

where Δt is the delay computed during the calibration. This perfectly fits the main advantage of this method since we directly measure the current and the voltage; one can note that the measured current is the combination of two contributions (Fig.3.5), the setup one and the DUT one:

$$E = \int_{t_0}^{t_f} v(t) \cdot (i_s(t - \Delta t) + i_D UT(t - \Delta t)), dt$$

in many cases, the former is several order of magnitude lower than the second one and so to evaluate the energy dissipated and energy stored, one can consider the total current not making a significant error. The reason behind this difference is that R_{DUT} is much higher of R_0 in many devices that goes to zero quite fast (Fig.3.8), usually also the C_{DUT} has the same relation with C_0 and so the power on the DUT branch is much higher:

$$E = \int_{t_0}^{t_f} P_{DUT} + P_0, dt \approx \int_{t_0}^{t_f} P_{DUT}$$

but how from the energy in function of the time we technically measure the energy loss and stored it is a fundamental step of this method and so I wrote a specific paragraph.

3.4.1 Energy Validation

The energy analysis is really important since it will be repeated many times during the remaining chapters.

First of all we need to model our DUT, in my general cases at a fixed frequency I had an RC series connection with inductive effects that play a role only at high frequencies (>10 MHz) and so can be neglected in this first stage; what we get is a simple RC circuit.

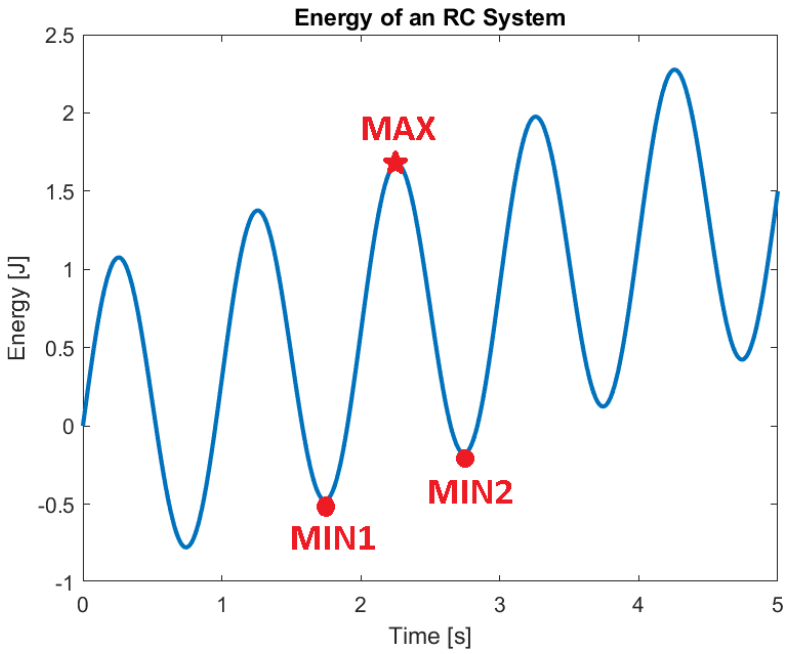


Figure 3.10: Typical Time-Energy Shape

By applying a sinusoidal voltage to this circuit, the typical response is depicted in the Fig. 3.10; how we can see, the energy is made of two contributions: a sinusoidal waveform that describe the charge and discharge process of the capacitor and a positive line that describes the dissipated energy (passive elements), the slope of this line describes the dissipated power (P_DISS) that can be computed just considering the period time (T) and so we can easily compute the loss per cycle (E_{DISS}) as:

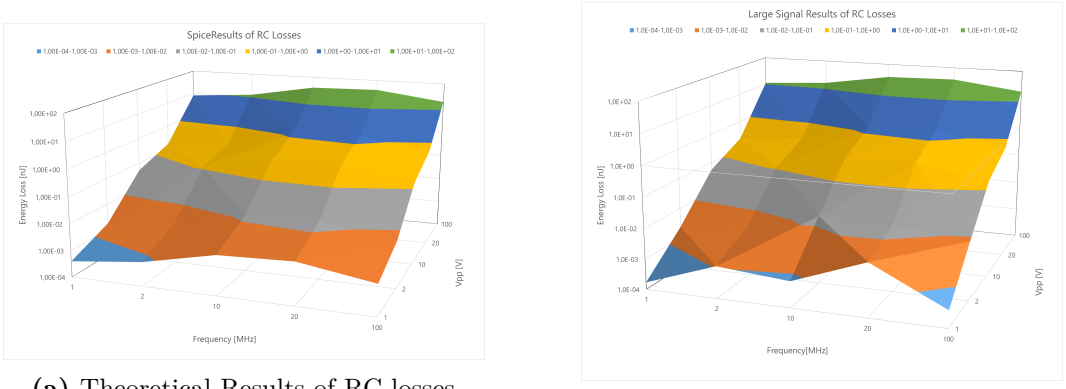
$$E_{DISS} = P_{DISS} * T$$

.

In my case, I considered the proper differences between maximum and minimum of the waveform to deduce the charging and dissipated energy, extending the notation of the Fig. 3.10 to all the plot, we have:

$$E_{DISS} = MEAN(MIN2 - MIN1)$$
$$E_{CH} = MEAN(MAX - MIN1).$$

At this point, we are ready for the last validation in which I have measured the losses with my new Large signal technique and compared them to a Spice simulation in which the parameters were found with an Impedance Analysis. The results are shown in the Fig. 3.11a and Fig. 3.11b; to interpret these plots, we have on the x axis the frequency of the sinusoidal wave and on the y axis the peak-to-peak voltage. For each combination of frequency and voltage I have plotted the energy loss, the results are comparable, in all the case i got the same order of magnitude and an error always lower than 10%, the main differences are present in the low voltage case where the loss are in the order of the pJ and so really small and hard to measure with all the large signal methods presented in the chapter 2. Finally we have validated the method, now it is time to use it, for this purpose in the next chapter I am going to analyze two important devices: Super-junctions and Power MOSFET and trying to give some explanations for the losses that are present.



(a) Theoretical Results of RC losses

(b) Large Signal Results of RC Losses

Figure 3.11: Energy Analysis

3.5 Conclusion

The calibration and validation of the new method were successful, both shown good results with respect the Impedance Analyzer and Spice. This passage, although not important for the purposes of this thesis, was useful to have an idea of the power of the method and if it was possible to get coherent results with the theory, without them I could not consider the future analysis correctly since all the results

could be affected by intrinsic error of the setup. Taking away all doubts about this problem, the next steps are the application of the Large signal method on commercial devices with the ultimate goal the understanding of the phenomenon behind the losses that I will find during the analysis.

Chapter 4

Off-Chip Analysis of GaN Buffer Losses

Now, I am ready for the application part, I have calibrated the new Large Signal Method and verified it, that was the introductory but mandatory part; in this chapter I am going to present some results about the output capacitance losses for two types of devices: Super-Junctions (SJs) and High Electron Mobility Transistors (HEMTs). For analyzing them, I needed to permanently turn off them by shorting the source and gate welding them together at the same pin of an SMA connector. I reported all the implications that I got in all the measurements, I performed on these two device, starting from a classic sinusoidal voltage input, confirming the theory, up to more complicated cases that resulted in new insights and characteristics concerning the losses in GaN Buffers. Before reaching that point, I will start from an easier part that is the complete understanding of output capacitance losses in SJs.

4.1 Super-Junctions

Before analyzing the loss in some SJ devices, we need to explain how it is designed to better understand the future results [9]. The SJ MOSFET is a type of power MOSFET that is designed to work with really high level of voltages. The idea is to expand the depletion region of a normal MOSFET (just Oxide-Semiconductor Interface) and so reducing the on-resistance; it is made by alternating n-p semiconductor stripes with really high but equal doping, Fig. 4.1 shows one possible structure.

These stripes are really narrow and can be depleted by a small gate voltage, after they appear as intrinsic layers and so an uniform electric field is spread inside the device, resulting in a really high breakdown voltage. With the presence

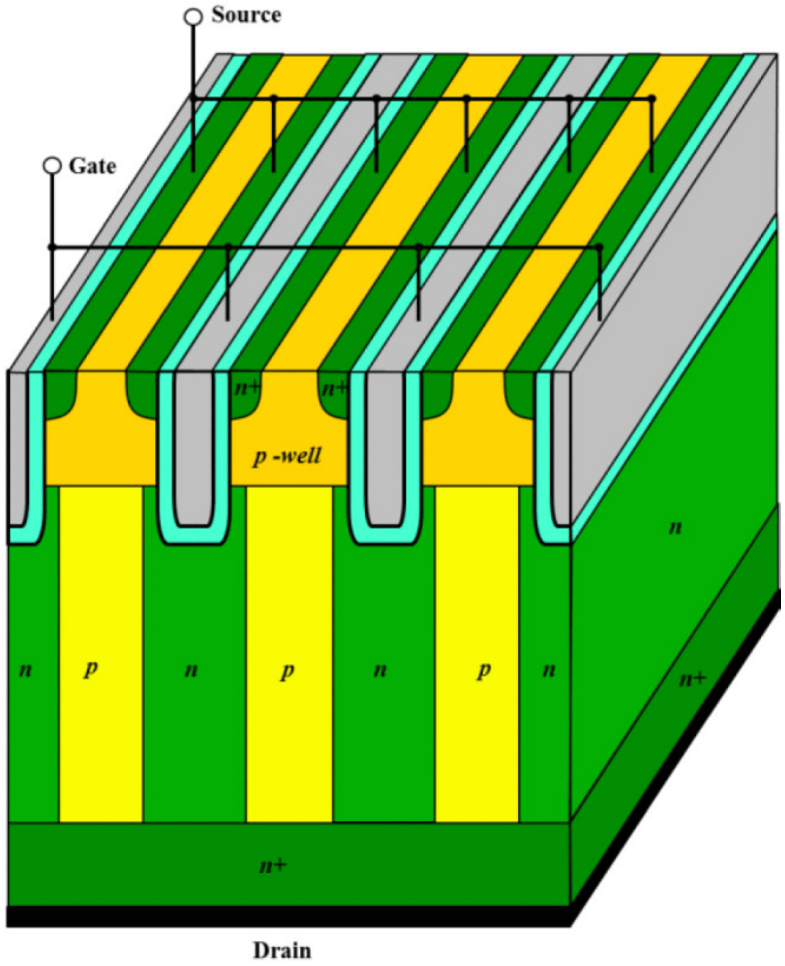


Figure 4.1: 3-D schematic layout of a vertical superjunction trench MOSFET [9].

of the stripes it is possible to have doping also order of magnitude higher than the conventional case, this entails an higher conduction area (A) and so these devices break the Si limit for the Specific on Resistance (R_on) and this limit can be continuously exceeded just by shrinking the stripes and increasing the doping, indeed it is possible to proof that for SJ we have:

$$R_{on} \cdot A \propto \frac{w}{l} \cdot \frac{V_B^2}{\mu \cdot \epsilon \cdot E_C^3}$$

where w and l are the dimensions of the trenches, μ is the mobility, ϵ is the permittivity, V_B is the breakdown voltage and E_C is critical electric field.

By decreasing w, we can overcame the Si limit as shown in [9], so $R_{on} \cdot A$ is called the conduction Figure of Merit (FOM) of SJs; in my case for switching

applications, another really relevant parameter is the charge stored (Q_{SW}/A) in the output capacitance but unlikely the product between them, $R_{on} \cdot Q_{SW}$, depends only on the material and doping and so have no improvement at high frequency. This is proportional to:

$$R_{on} \cdot Q_{SW} \propto \frac{V_B^2}{\mu \cdot E_C^2}.$$

Dividing the low frequency and high frequency case, in the former one the conduction loss are dominant and the switching loss is negligible so it is $R_{on} \cdot A$ that limits the total loss, here we have a net improvements from the conventional case, [9].

For improving the second case we need to develop wide band gap semiconductors.

Typically SJs are used in hard and soft-switched applications and increasing their performance by lowering w or increasing the doping have met some problems, unexpected losses from charging and discharging the output capacitance are appeared and in the next section I will analyze them and giving an explanation of why they are present and how to avoid them.

4.2 Super-Junctions: Hysteresis in QV curves.

In a normal operation mode, when the SJs are in off state (source and gate shorted), the output capacitance, C_0, is charged and discharged continuously, ideally incurring zero switching losses but some dissipating effects are present as hysteresis in the QV curve. The SJ analyzed in my thesis is the STW38N65M5 by ST-Microelectronics, the results are been compared with an ST Analysis in [5].

I started the analysis by applying to a permanently off ($v_{gs} = 0V$) DUT a sinusoidal voltage at 200 kHz with different amplitude, max 300 V, the experimental setup is shown in the Fig. 4.2, where we see the presence of the DUT at the output of the PCB, the GaN Amplifier and the 2 Bias-Tees connected to 2 Voltage Suppliers.

The typical QV pattern for a 300 V sinusoidal wave is shown in the Fig. 4.3, where i plotted the charge, found by integrating over time the current, in function of the V_{DS} voltage that varies between 0 and 300 V at 200 kHz.

This pattern is the same found in [5] with the ST method, we see a really large hysteresis loss, the charging process is smoother like an exponential increase but at some points gets constant instead the discharging is sharper, the charge remains constant up to really small voltage and then drops to zero but after around 200 V the two processes coincide.

The next step is to change some parameters to identify what causes the hysteresis pattern, the first analysis was to change the amplitude to verify if exists a threshold voltage, the results are similar to what was measured in [5], the hysteresis showed

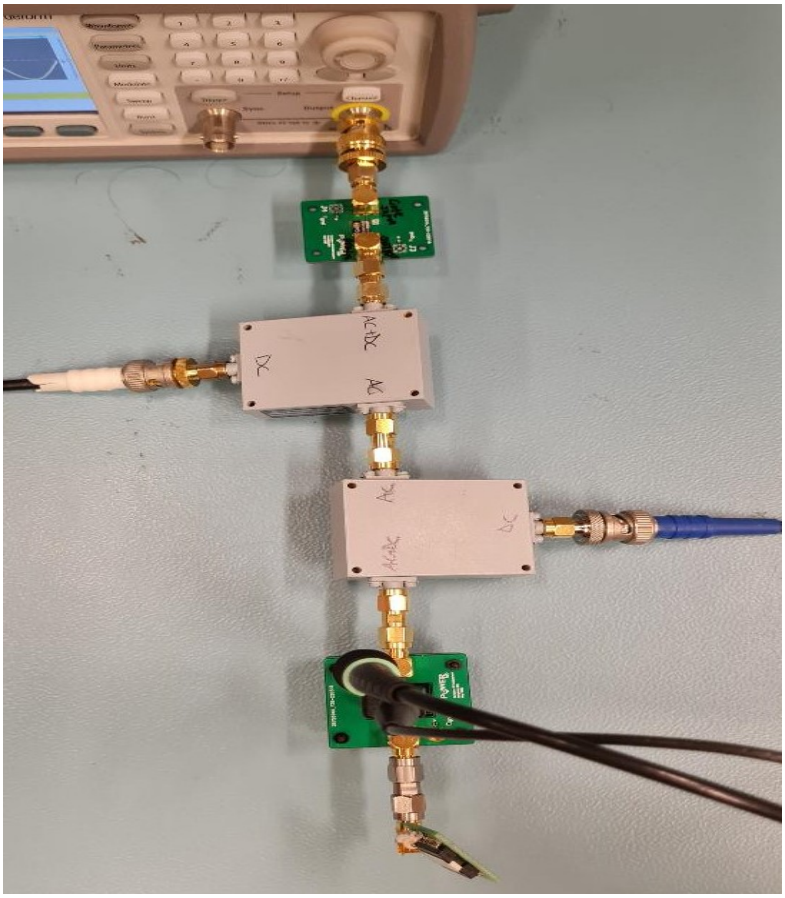


Figure 4.2: Setup of the new Large Signal Method on the STM device.

the same shape and the dissipated energy was comparable, Fig. 4.4, in which I compared the results with the new method for different voltages with the ST ones, this analysis was performed at 200 kHz (due to the bias-tee) so I also had to rebuild the same setup presented in [5] to do the same analysis at the same frequency (in the paper the results were at 100 kHz), it is possible to observe a clear saturation of E_{diss} at high voltage due to the match of the charging and discharging path, Fig. 4.3 resulting in no hysteresis.

The hysteresis is present also at 100 V, naturally with lower area, this suggests a low-voltage phenomenon, the next step is to verify if it depends on the frequency while keeping the excitation voltage fixed at 100 V.

The results are shown in the Fig. 4.5, as demonstrated also from [5], these devices did not have a significant frequency dependence, the losses have a small increase but the charging energy remains constant, due to the really high losses this device is not a good candidate for high frequency regime, indeed in [12], the

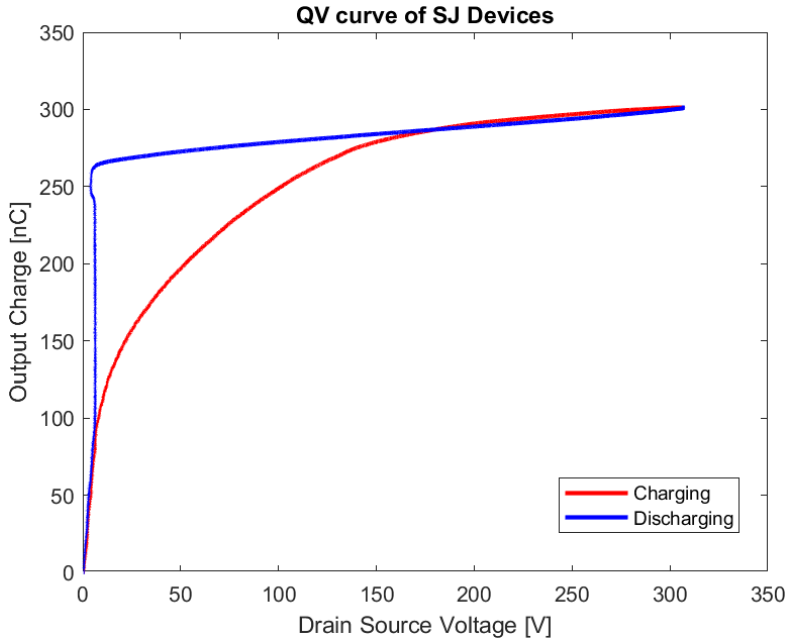


Figure 4.3: Charging and Discharging Process of C_0 in SJ devices.

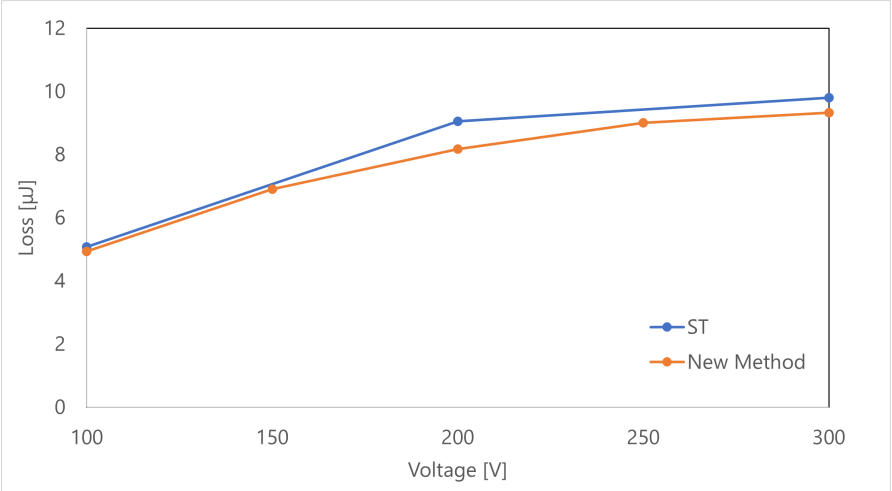


Figure 4.4: ST and New Method Comparison on DUT Losses.

analysis on frequency has shown always a positive slope and in the MHz regime the losses reached few Watts moreover analyzing in function of the voltage, they were not constant anymore after 200 V but higher so showing a frequency dependence only above 2 MHz.

So for SJs, two hysteresis component have been reported: a low frequency

component (with no frequency dependence) and an high frequency component. I could not measure this phenomenon due to the really high loss of my DUT, this is due to the design of the SJ indeed as reported in [12], the pitch dimension is inversely proportional to the C_{OSS} losses so to better analyze this effect is better to work with large pitch SJ as it was done in [12] but this also involves smaller R_{on} so losing the small conduction losses that characterize these devices.

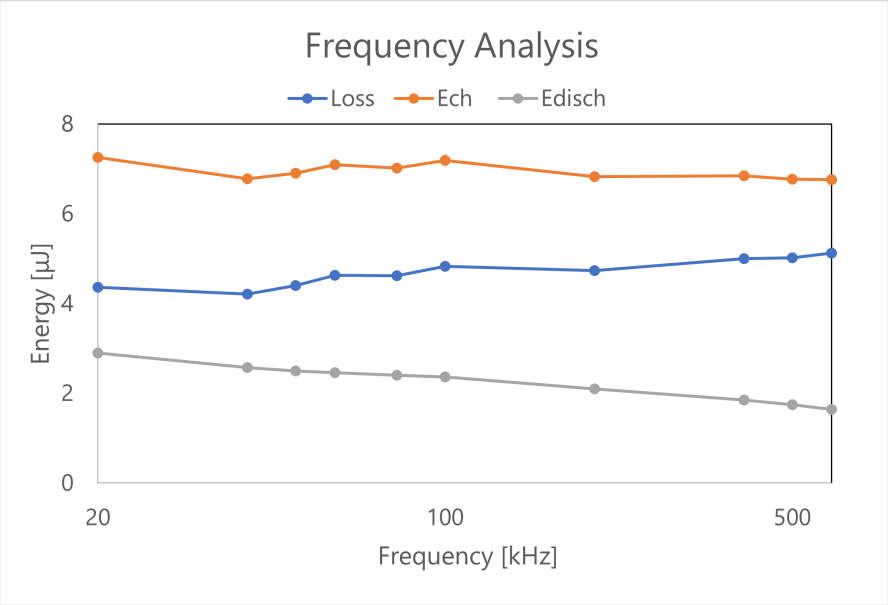


Figure 4.5: SJ Losses in function of the frequency.

4.3 Physical Explanation of C_{OSS} Losses in SJ

This hysteresis losses are really significant for these devices since they happens in soft-switching applications in which we cannot have anymore the recycling of the energy stored, for this reason the output capacitance, C_0, in power converters is an important selection component since its energy stored, E_0, determines the thermal operation and efficiency. In the literature and also in this thesis (to not use many names) this capacitance is called C_{oss}, since it is characterized by small signal methods, that integrated across V_DS gives E_{OSS} despite in this section I used a large signal method for the characterization.

In the previous analysis, I have applied a large signal to characterize C_{oss} losses to better replicate the normal working mode of power converters, since (from chapter 2) the quasi static approximation that allows the extrapolation from small signal measurement to large signal one is not valid; leading to under prediction of

the effective stored energy and resulting in much higher than expected losses, like in [5] where E_0 was under-predicted by over 100% when comparing the ST results with the small signal ones of datasheets.

Let's consider one device characterized by one gate connection, Fig. 4.1, it has been shown in [9] that this hysteresis occurs only during the pinch-off of the SJ high doped columns.

During the ramp up of the voltage (charging), we deplete the pn-junction always more and there is the formation of trapped holes in the center of the p-pillar but no electrons in the n-side however in ramp down, they observed holes pockets alternated with electron pockets (not present previously), showing a non equilibrium condition. These trapped majority carriers must recombine with the minority carriers in that side of the column or reach the contacts which are separated or by an high resistive layer or by a depleted region, this process is so slow that the time constant for SJs can also reach several hours (for the recombination of the majority carriers). So the root cause of the observed dc hysteresis anomaly is charge trapped by asymmetrical depletion of the SJ columns and this effect is proportional to the settling time of the trapped charges (in another words, the finite velocities of the carriers in the semiconductor are the root cause for C_0 hysteresis).

Another phenomenon that was observed in the SJ behavior in [9] was the shift of the output capacitance where it significantly decreases with increasing the frequency but happening only close to the full depletion; it does not change with the frequency, the difference is in the transient response. In this case, the author considered the SJ cell as a distributed RC network and compare with a classical pn cell, this last network produce a capacitance proportional to the term $(1/\omega/ImZ)$ that makes it independent on the frequency, instead for the SJ we have $\omega \cdot \Im Z$ that increases with the frequency one decade below the RC time constant that for reasonable values of Resistance and Capacitance is on the order of MHz. The frequency shift is fundamental of the SJ structure and so must be present in all the measurements.

The loss measured does not only consist of hysteresis effects but also by heat that is generated during the charging and discharging process, this is reasonable since we explained the reasons of losses are not recombined charges that moving towards the electrodes, generating Joule heating flowing through lightly doped regions (charging and discharging currents), this effects is superimposed to the hysteresis and it is measured at the same time, it is always needed to measure the variation of temperature of the device to see if it is negligible.

4.4 GaN Power Transistor

The next device to be analyzed was a Gallium Nitride enhancement-mode power Transistor, IGO60R070D1, a commercial device from Infineon. The GaN Mosfet

exploits the 2DEG so that electrons have high velocity, its importance is due to the high critical electric field in addiction to small on-resistance and capacitance of Si Mosfet. Another important feature of this device is its reverse recovery performance, the used GaN have no minority carriers and no body diode, this makes the measure more stable. This kind of devices are characterized by a substrate that can be Si usually Boron-doped with a doping concentration between 10^{14} and 10^{15} cm^{-3} (lower leakage current with respect the n-type case) or for a better isolation Sapphire in which is deposited an epitaxial buffer (III-N: usually GaN properly doped) to electrically isolate the active area (GaN channel) and the substrate, deep acceptors, like Carbon, are usually introduced inside to suppress off-state leakage current. Then we have an AlGaN layer on top for the formation of 2DEG at the interface, p-GaN to make the device normally-off and finally the three contacts:gate, source and drain.

This device is called HEMT and can operate at higher frequency than ordinary transistors, possibly because the main charge carriers are the majority ones that diffuse from the wide band gap material (AlGaN) to the adjacent narrow material conduction states (no doping so free states) until the equilibrium is reached (developing of a potential at the interface) and the channel called 2DEG is formed, this presents no donor atoms to cause scattering so higher mobility, so higher velocity of the majority carriers.

Another important aspect of the device analyzed in this section is the presence of a field plate, a metal contact to the source that extend up above the gate which main function is to reshape the electric field in the channel reducing its peak to the drain side and so increasing the breakdown voltage. At this point, our device can be characterized by several parasitic capacitors: a drain source capacitor defined by inter-metal contacts as 2DEG and field plate, in addiction also the drain gate capacitor considered in parallel; these elements are considered lossless. Differently there other two other capacitors from drain and source to the conductive substrate with the buffer as relevant dielectric, which in principle could show losses.

As for the SJs, analyzing permanently off HEMTs at high voltage result in hysteresis losses, the problem is that the structure is completely different and there are no dopant charges and so the origin of this phenomenon must be found in a different loss mechanism.

4.5 GaN HEMTs: Hysteresis in QV curves

This section is analogous (same measurement setup) at the SJ one, the first part consists in just the application of a 400 V sinusoidal voltage and measuring the charging and discharging of the output capacitance, C_0, at 1 MHz.

The results are shown in the Fig. 4.6, the effect is completely different with

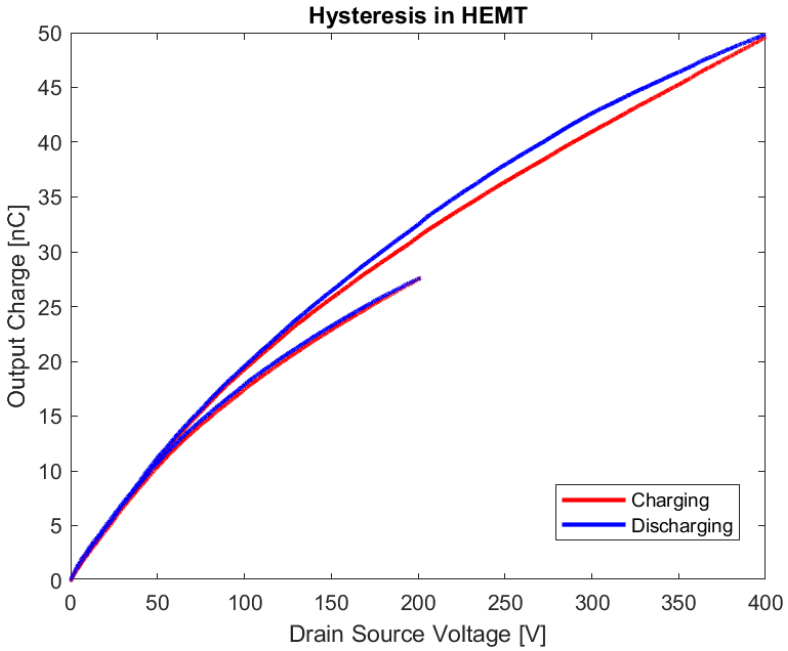


Figure 4.6: HEMT Hysteresis Losses.

respect the SJ as confirmed also by the ST method in [5], for low voltages there are no losses, the only differences is for the high voltage part. In the next section I will try to give some hint about the physical reason of this effect, in the literature it has been observed an increasing effect with the voltage (differently from the SJs) though the loss values are much smaller compared to SJs ones; it looks like there is a threshold voltage for this effect (no effect under 100 V). In the same figure it is plotted also another hysteresis but for lower Voltage (200 V), this is used to show the superimposition of the two QV curves, showing that the charge path is not the same for the two sinusoidal excitation signals and so we can conclude a non uniform dependence of QV patterns on the Voltage.

Then I preferred to check my method as i did with the SJ and ST analysis, this time the quasi-linear approximation holds for these devices and so i could use the datasheet for the control that showed a really good match with the Large Signal Analysis, Fig. 4.7, both for the charging energy,E_0, and the charge stored in the output Capacitance, Q_{OSS}.

The datasheet analysis usually are measured by a small signal technique since they are much faster but for the SJ as demonstrated in [9], the results are different with respect a large Signal technique but in this case for GaN HEMTs, also if the QV patterns depend on the amplitude voltage, the main parameters can be established by a small signal method and then extended to the large case and so the SS subscript loses its significance. For obtaining clean results, I had to consider

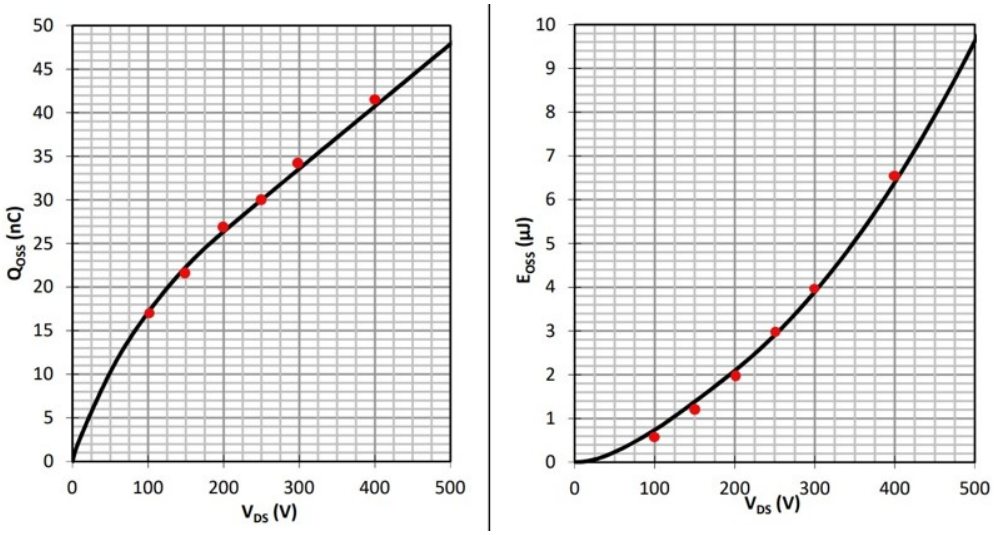


Figure 4.7: Large Signal (Red Dots) vs Datasheet (Black Line) of the DUT.

the setup configuration that is also constituted by a capacitance (C_S) in series with a resistance (see Chapter 3) and so I needed to evaluate the charging energy and charge stored in C_S and then subtract to the complete case to get the results in Fig. 4.7.

How this hysteresis changes with the frequency? For this analysis I just applied a 100 V sinusoidal voltage from 1 to 10 MHz, the results are shown in the Fig. 4.8, the charging energy is almost constant when we increase the frequency, instead what drastically changes is the energy loss that has a huge variation in function of the frequency, there are more dissipating effects at larger frequencies, the approximation of perfect capacitors for the active region is not anymore valid, the shape of the QV plot is much wider and for this reason the hysteresis is completely different and other phenomena become dominant; this frequency dependence was also predicted in [5] but not measured since the ST cannot work at so high frequencies.

4.6 Physical Reason of Hysteresis Losses in GaN HEMTs

GaN power HEMTs are generally grown hetero-epitaxially on a Si-substrate for lower cost that allows large scale production and high reliability. The first source of losses are generally resistance, in my case the most important is the substrate one (R_{SUB}) that depends on the doping concentration, the thickness and the device active area. Unlikely these parameters affect also the Breakdown Voltage, current collapse and power losses, often we cannot optimize everyone at the same time. For

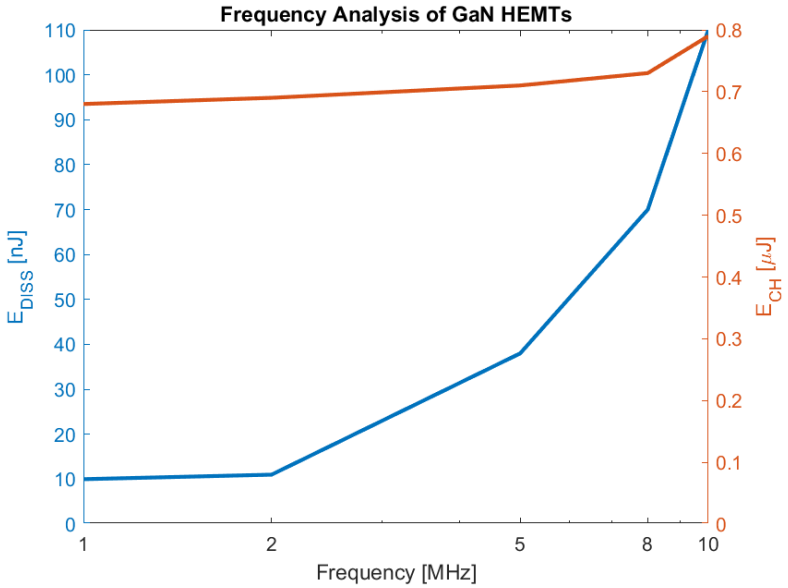


Figure 4.8: Frequency Analysis of GaN HEMT.

example, high resistive (low doping) substrate gives a better breakdown voltage since the depletion region will extend in the substrate, creating an additional region for the voltage drop but this phenomenon also results in stronger trapping effects. This Resistance is dominant for the devices with small active area, in [13], the current through the Si substrate (that is dissipated) has been measured for different frequencies and amplitude, they showed a clear increase with both of these parameters, this effect is in accordance with the theory that proves the raising of the C_{OSS} losses with higher dV/dt, going also to confirm my previous results concerning the frequency analysis. To suppress this phenomenon, the idea of different device manufactures is to change the stack design, in particular the GaN layers that may be able in the future to completely block the vertical leakage current through the substrate.

The resistive losses just counts for a small portion of the total C_{OSS} losses, there are other important effects that are analyzed in the rest of this section.

One of the main hypothesis about the physical reasons behind these others hysteresis losses have to be found in the vertical stack of HEMT. The complete structure of the buffer consists of several layers, at the bottom an aluminum nitride layer for better nucleation on the Si substrate, then several layers to compensate the thermal expansion mismatch between the substrate and the remaining buffer, this also provide a sufficiently good quality seed for the active GaN channel but all these layers are not intrinsic insulating but usually doped and during their growth some deep traps are introduced that can capture charged carriers and keep

them localized. Their purpose is to increase the dynamic conduction performance, allowing a fast discharging of the GaN channel but these traps can also segregate the structure defects making the distance between atoms smaller and enabling direct defect-to-defect interactions, suggesting the existence of a defect band that transport charge (leakage current higher) but as observed in [6] this is not the only effect that causes leakage, other effects are present and their origin have to be found in the combination of layers within the buffer

Trap levels in the GaN buffer have a long trap/detrap time which makes electrons trapped in these states unable to follow the high frequency V_{DS} change, contributing to the hysteresis in $C_{OSS}losses$. These trap sites are mainly due to dislocations caused by a really different lattice between GaN and Si; so when a large voltage is applied between source and drain, electrons are accelerated in the channel and gain enough kinetic energy to be scattered in the buffer layer traps, reducing the drain current and increasing the dynamic on-resistance.

These losses reach a peak at around room temperature but the total charge stored is approximately the same [13], this is the first fact confirming that the reduction of C_{OSS} is mainly due to a decrease in trapping effects indeed increasing the temperature leads in fast de trapping time, in the limit of high temperature this trapping effects become negligible. What is the physical mechanism of this loss phenomenon? This is primarily attributed to the charge imbalance during the charging/discharging of acceptor traps in the buffer, the process is as following:

- Increasing the V_{DS}, the depletion region expands and the electrons in the 2DEG accelerated closest to the drain gets injected in the traps in the buffer,
- Decreasing the V_{DS}, the depletion region shrinks, the decelerated electrons gets injected much closer to the gate side, then these electrons are also responsible of the current collapse during the initial on transient (effect not visible with my analysis).
- Then after some time the electrons gets discharged and according to the time can get recovered or contribute to the energy dissipation.

This hypothesis can model also the threshold voltage characterized in the hysteresis C_{OSS} losses of GaN HEMTs which effect was visible only for voltage higher than 200 V, that can be considered as the minimum value for having an electron velocity in order to scatter them in the buffer traps. Over this effect others have been identified that add to C_{OSS} loss mechanisms like resistive losses in the GaN stack; but additional investigations from the manufacturing company are required to have a complete knowledge on the device and related loss phenomena. Now that we have an idea of what can be the physical reasons behind these losses, I am going to analyze how GaN devices behave for different input condition.

4.7 Partial Hysteresis in GaN HEMTs: Fixed Amplitude

The rest of the chapter is left to some new insights about C_{OSS} hysteresis losses, the next analysis was performed on the Infineon Device, IGOT60R070D1, the idea is to check if we use the device around the hysteresis region (over 200 V) we observe the same losses. What I did, it was to apply a small amplitude sinusoidal voltage (10 V) at 1 MHz but increasing the DC bias; some example of the input is presented in the Fig. 4.9, where I plotted only the first three sinusoidal input Voltage.

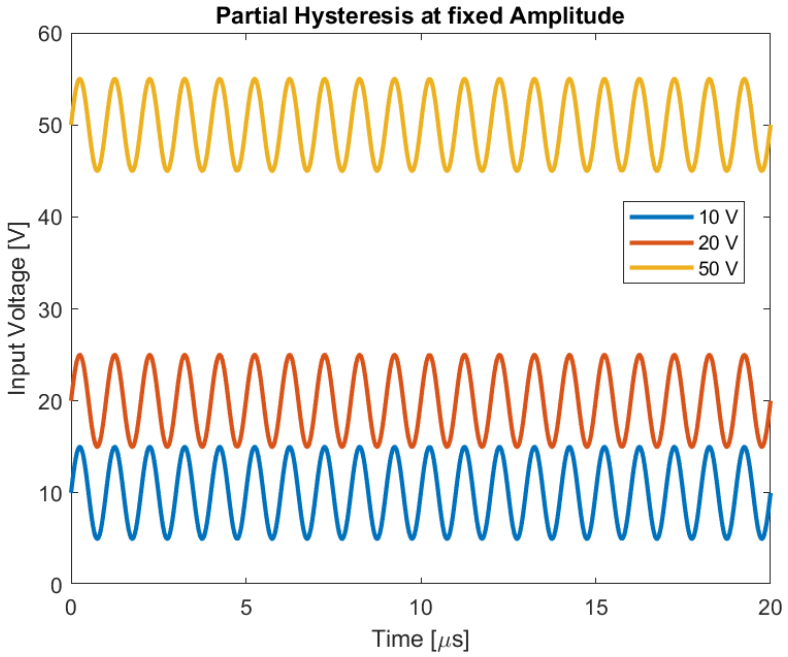


Figure 4.9: Input Signal for Partial Hysteresis Analysis.

The resulting QV curves are presented in the Fig. 4.10, contrary of what one can image the larger losses are presented for lower DC Bias where before with the 300 V sinusoidal voltage there was no hysteresis, instead for higher bias the loss are almost zero, the discharge and charge curve are coincident, in this range it is like if trap states loss are not activated, only for low voltage we have this effect.

This can be proven by considering the velocity of the electrons, we need low voltage so small velocity to activate the trap states that are visible only at the discharge moment where the electrons cannot be recovered indeed at high voltage, we do not have the charging of these states ans so this effect is not present.

These results are shown in the Fig. 4.11a, the losses decrease in function of the Bias with a hyperbolic shape and gets almost constant at high voltage, the

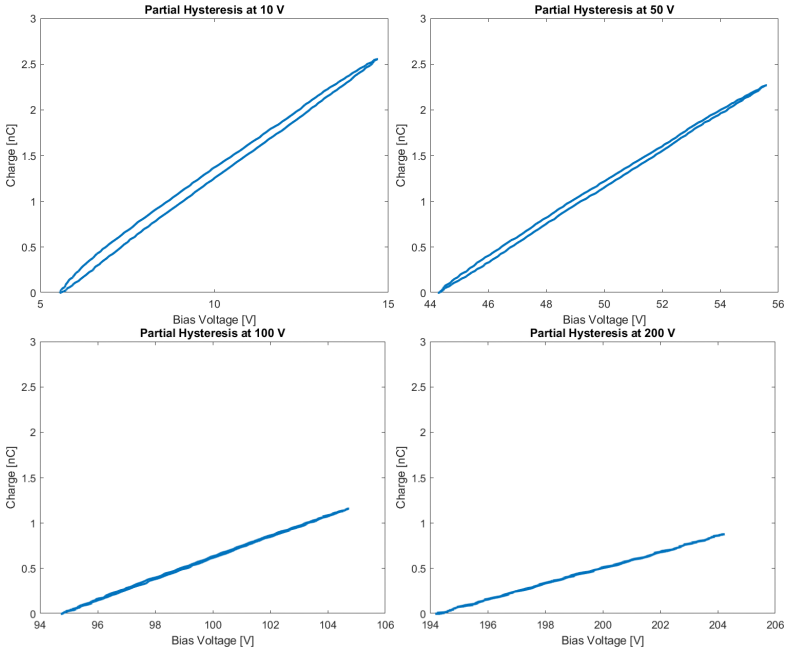


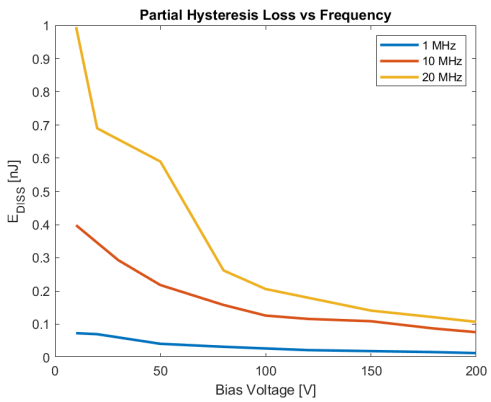
Figure 4.10: QV results of the Partial Hysteresis Analysis.

concavity drastically changes with the voltage, indeed at 1 MHz there is no effect and the hysteresis is not present as showed in the Fig. 4.11b, where increasing the frequency not only increase the hysteresis area and so the losses but the charge follows different path so different slope implying a not linear dependence on the frequency of this trap states loss effect.

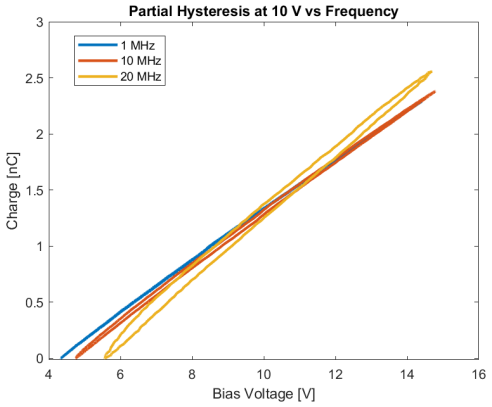
Summarizing to active this loss effect, we need to apply a small voltage and this depends on the frequency and the DUT; for small frequency this effect is less visible, likely charging and discharging the capacitance at small frequency is possible since the charges can stabilize also if they get trapped in the buffer instead at high voltage the velocity is so high that the scattering in these trap states is less likely moreover the detrapping time can be conditioned by the high voltage so the electrons can be recovered during the normal cycle of the output capacitance C_0.ù The next question and so the next analysis on these losses was to verify if the high voltage hysteresis is always present also if we change only the starting voltage.

4.8 Partial Hysteresis in GaN HEMTs: Fixed Maximum

The next part consists in the analysis of partial hysteresis in which I fixed the maximum Voltage, also in this case the applied sinusoidal voltage are presented in



(a) Hysteresis Losses for different Bias and Frequency.



(b) Hysteresis Shape at 10 V for different Frequencies.

Figure 4.11: Partial Hysteresis Results.

the Fig. 4.12, in which I just worked with the amplification of the amplifier and the dc bias to fix the maximum voltage at 300 V.

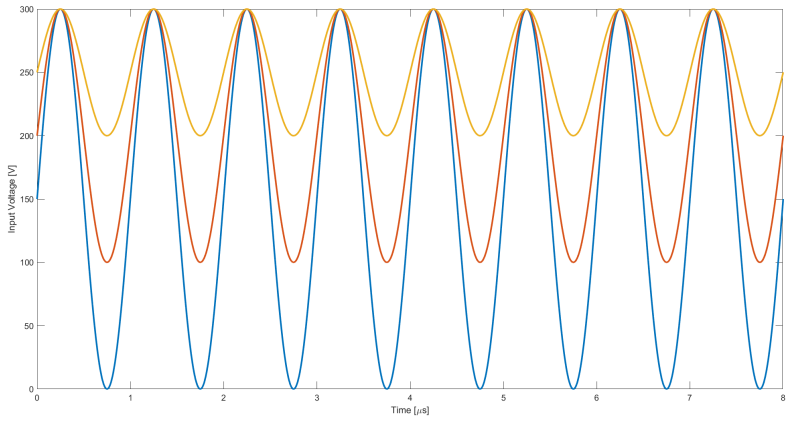


Figure 4.12: Input Signal for Partial Hysteresis Analysis.

The analysis consists in starting from the normal case, the 300 V peak-to-peak sinusoidal voltage and then increase the DC and decrease the amplitude reaching the partial high voltage hysteresis case. The results on the Infineon GaN HEMT device are shown in the Fig. 4.13, I have divided the behavior of the device losses in three regions:

- For Vpp $\leq$ 50 V, the C_{OSS} losses are really low, indeed in this region computing the quality factor,

$$Q = \frac{\pi}{2} \frac{E_{CH}}{E_{DISS}}$$

, where E_{CH} is the charging energy and E_{DISS} is the dissipated energy, has a value higher than 100 so we can consider the system behaving like a good capacitor;

- For 50 < Vpp ≤ 250, the losses increase linearly but more important is Q that is almost constant in this region, the system in this range behaves like a RC system with a quality factor of 70, but interestingly the losses in this region are not hysteresis like but affected by resistive effects of the device like contacts, substrate, buffer and active region;
- For Vpp > 250, the losses undergo a huge increase, the slope of the linear increases immediately raises up, in this region we find again the hysteresis losses with the high voltage effect that generates an higher variation between the charging and discharging curve, here the quality factor is reduced up to 40, meaning in a decrease of the quality of the DUT, only for high peak-to-peak voltage, starting from low values, we observed the presence of the trap states that are charged for low voltage and create an increase on the losses that are superimposed to the normal resistive effects.

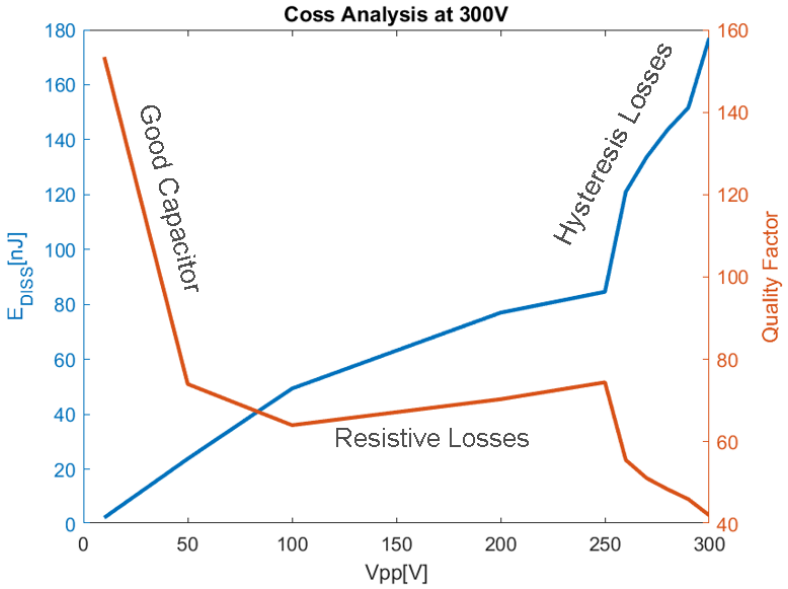


Figure 4.13: Partial Hysteresis Results on Infineon DUT.

In this Analysis, we observed a huge change in the losses staring from 40 or 50 V and going up to 300 V, like there is another effect that plays a significant role only for the 260 Vpp case.

Analyzing in the detail these two cases, I presented the Fig. 4.14, the comparisons between them, in the left part we have the 40-300 V case, where we see the hysteresis

at high voltage, so the trap states have been activated instead in the right part there is the 50-300 V case where the difference between the charging and discharging curve is constant for all the voltage range, so for this reason I called this region 'resistive' because this effect is typical for resistors. In the bottom part there is a zoom of the starting zone of the curves, we see that the difference is higher for the second case that for the first one, so the effects that determine the losses for this device change with the staring voltage, the hysteresis is dominant in the total losses of the DUT but it needs low voltage to be activated and present in the normal behavior of the DUT, instead normally the device behaves like a classic RC system and the only sources of losses are due to resistive effects of the several layers.

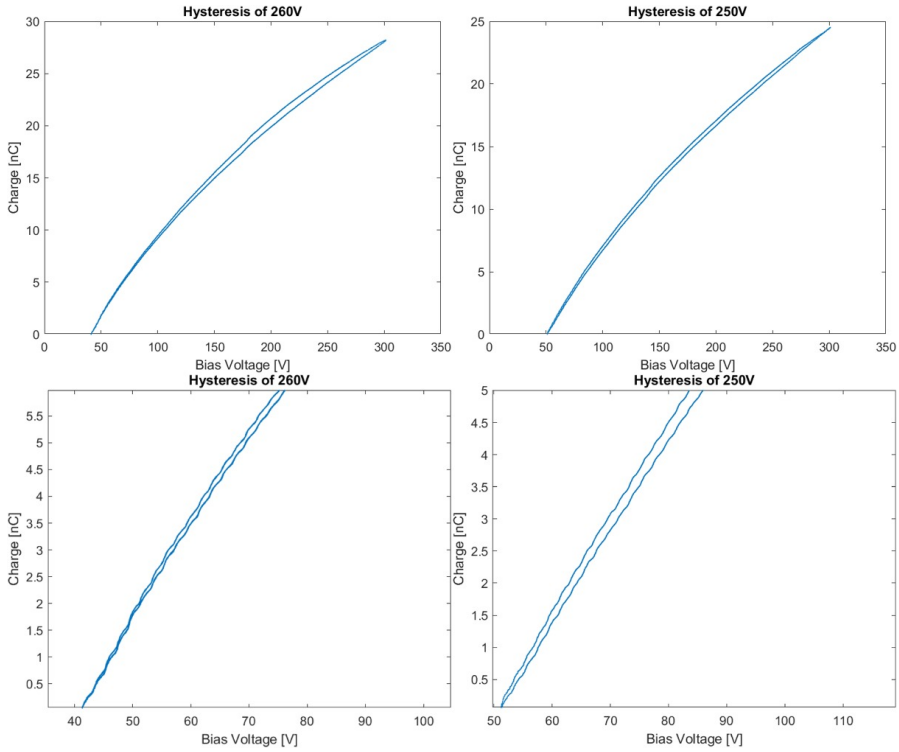


Figure 4.14: Difference between the hysteresis for the 40-300V and 50-300V case.

This analysis looked very interesting and so I decided to analyze another GaN HEMT Device, the PGA26E07BA from Panasonic, a GaN Normally Off Power Transistor that in [5] showed the same behavior of the Infineon GaN Transistor but with a slightly higher hysteresis losses. Unlikely I could not have the single device but it was bonded in a PCB used for ST Analysis, so I used crocodile inter-connectors for connecting it to my PCB, the results are presented in the Fig. 4.15, the main differences with the previous device that I found was a better capacitor behavior up to 150 Vpp (the complete analysis showed a continuous

increase on the quality factor that reached also the value of 500 for small amplitude voltage but this forced me to plot only for 150 Vpp to show the slope in the second part of the analysis).

For peak-to-peak voltage higher than 150 V, the results are similar to the previous case, we have a linear increase on the Loss associated to resistive effects and a positive transition of the slope between the 250 Vpp and 260 Vpp but in this case probably due to the connections that worsened the results, this shift is less visible.

Also for this device, this transition effect of the losses causes is present that modifies the behavior of the device; at this point we can hypothesize that these trap states to be activated they need that the voltage across the DUT should be lower than 50 V, in this case the velocity of the electrons is smaller enough to activate the trap states, obtaining the hysteresis effect. The question at this point is why there is this dependence on the minimum of voltage or also why if we start the analysis for high voltage it is like that this effect is not present and what we have is only resistive losses due to the layer stack of the DUT. I will try to give an hypothesis about this effect: the electrons in the channel are accelerated and due to scattering effects, they get trapped in these buffer states, at this point if they are not recovered before of the end of the charging curve, they are lost and are found in the hysteresis part of QV plot, if we start from $V \geq 50$ V, the electrons trapped in these states are completely recovered before of the discharging path and the loss are generated by Joule effect; instead for $V < 50$ V, the electrons trapped in these states are not recovered in time and so generating the hysteresis effect. The main cause of this effect may be a dependence on the voltage or on (dV/dt) of the detrapping time:

- For a starting Voltage ≥ 50, the higher velocity of the electrons is translated in a shorter time for them to cross the active layer so a lower total probability that they get trapped moreover this is confirmed also by the previous analysis where for high voltages there were no hysteresis losses;

- For a starting Voltage < 50, the lower velocity of the electrons is translated in a longer time for them to cross the active layer so an higher total probability that they get trapped, like for the other case, the previous analysis is coherent also with these results. At this point the de-trapping time is much higher and not enough to be able to recover these electrons before of the discharging path.

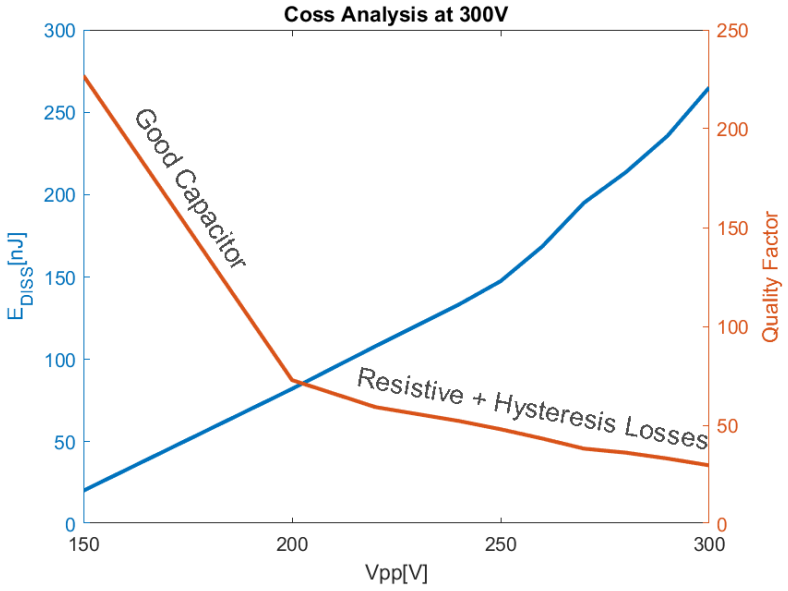


Figure 4.15: Partial Hysteresis Results on the Panasonic Device

4.9 Burst Analysis

Until now all the analysis have been performed in continuous way but normally these devices are not used continuously but only for a certain time that means that it is impossible that the sinusoidal voltage have a total duty cycle of 100% or that a continuous charging/discharging have been applied with no rest for the DUT.

The question at this point is if we apply the excitation sinusoidal signal at the output of the Panasonic GaN HEMT only for a short time and then leave the DUT rest to be sure that it will be in equilibrium for the second cycle what kind of hysteresis loss we have to expect.

For this measure, I always applied a sinusoidal signal at 400 kHz with peak-to-peak voltage of 300 V, with a duty cycle of 1 ms that means I can apply from 1 to 400 cycles before reaching the continuous case. The results QV hysteresis are presented in the Fig. 4.16, I started from only 10 cycles and going up to 399 cycles that is practically the continuous case; we can quickly see that the shape of the QV curves change going from the discrete to a more continuous signal; for few cycles, the hysteresis is almost no present and the difference between the charging and discharging curve looks constant like if the causes of the losses are only resistive and not due to trap states instead going to the continuous case we find the classic result. At this point we can hypothesize a threshold Duty Cycle for which for the last cycles, if we analyze the QV curves, we have the high voltage hysteresis losses, to better show this I have analyzed the losses and the quality factor of the DUT

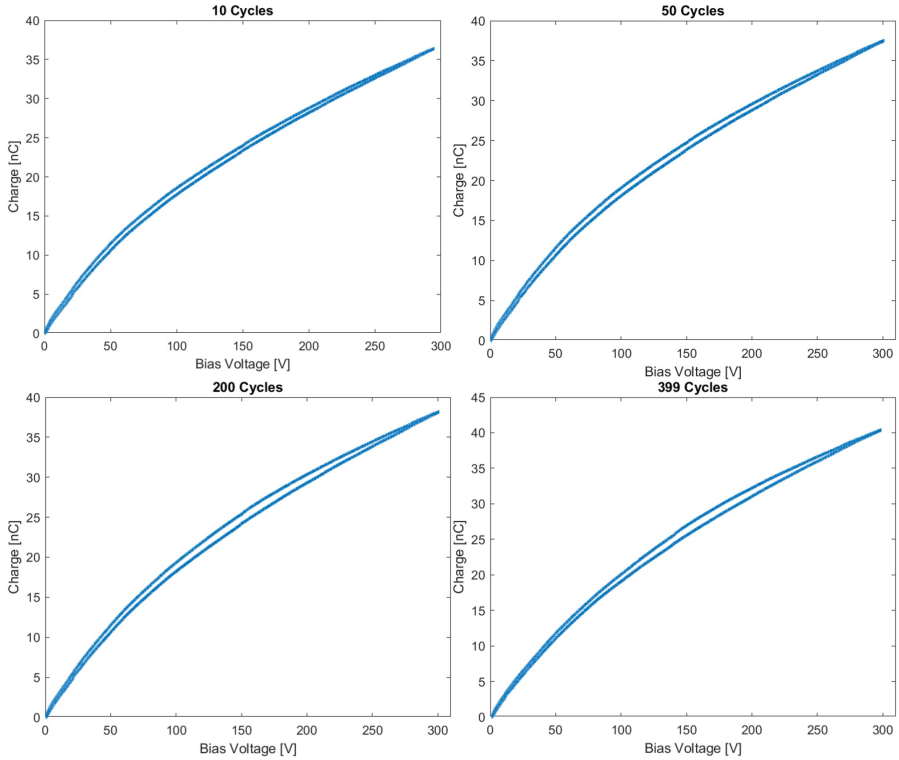


Figure 4.16: QV Results for the Burst Analysis of Panasonic Device.

for the different number of cycles and the results are shown in the Fig. 4.17, we find the same conclusions of the analysis of the QV plot.

For few cycles the total losses are small, 50% smaller than the continuous case and also the quality factor is higher meaning that the output capacitance has a better behavior than the continuous case but after 100 cycles (Duty cycle of 25%) the losses gets constant meaning that the hysteresis present is analogous of the continuous case and increasing or decreasing the cycles have no effect in the Output capacitance losses, the quality factor gets constant and smaller than the few cycle one.

With this analysis, we can conclude that makes sense to use the DUT with a Duty cycle smaller than 20%, naturally this number can change with the operating frequency and the DUT so it would be better to perform a quick analysis before deciding these parameters so that the device presents no high voltage hysteresis losses.

But why there is this dependence; my hypothesis is that for few cycles the total number of trapped electrons is small due also at a probability effect for a scattering event to happen and have as result an electron blocked in these trap states, in this way we can consider these states practically empty and filled with only few

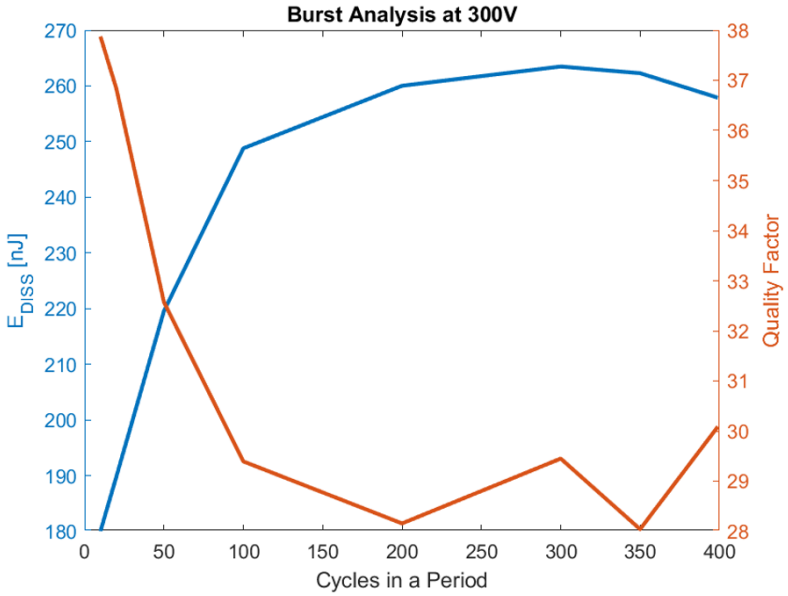


Figure 4.17: C_{OSS} Losses and Q of the Panasonic GaN HEMT.

electrons that have no effect in the discharging path. They are recovered only in the burst time where we have a constant 0 V and so it does not participate as hysteresis loss but only resistive losses are present and so the difference between the charging and discharging curve looks constant instead for enough cycles, we practically recover electrons during the discharge path at high voltage and so we get the classical high voltage hysteresis shape of the QV plot.

This effect can be summarized by hypothesizing that the detrapping time is equal to: $t_{DT} = \frac{NCC}{f}$, where NCC is the maximum number of cycles having constant loss and f is the frequency; in this way if we apply more cycles of NCC, the electrons are de-trapped in time to be recovered in the discharging curve and so obtaining the hysteresis otherwise we just charge these states and the electrons can be considered lost, like happens for resistive effects in the contact or substrate.

4.10 DC Bias Affecting Hysteresis Losses

The last analysis of this chapter was the answer of a question if there is any kind of influence of the hysteresis losses on a DC bias stress.

The signal designed properly for this analysis is represented in the Fig. 4.18, the signal is applied in Burst mode with a rest time of over 100 ms to be sure that the Device is in equilibrium after each application of the signal, this excitation consists in three parts, a relax AC sinusoidal signal with amplitude of 75 V at 400 kHz then a stress DC voltage at 150 V for the same time of the input signal and finally

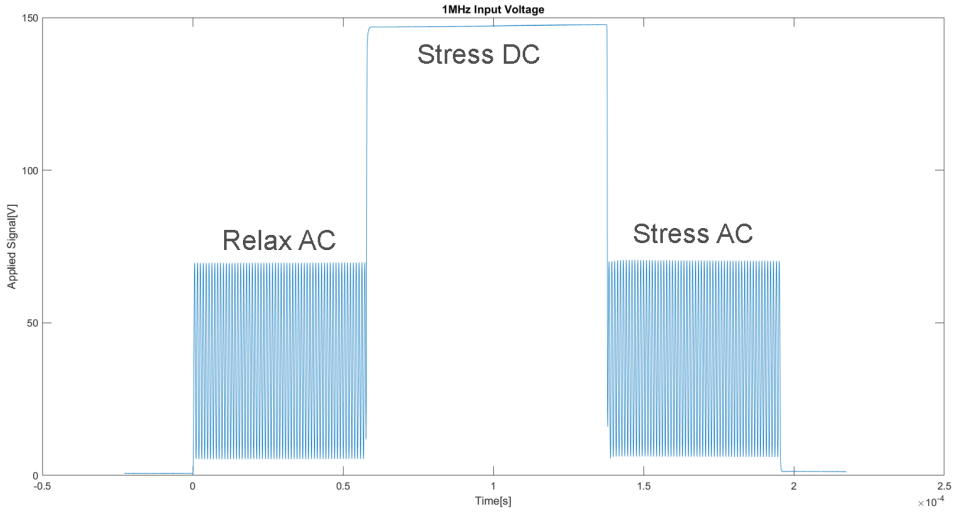


Figure 4.18: Input Voltage of DC Affecting Losses Analysis for the Panasonic GaN HEMT.

the same sinusoidal signal to measure if there are any kind of difference in the $C_{OSS}losses$between the Relax and Stress case, The hope of this analysis is observe any modification on the energy of the system, looking both at the dissipated and charging energy.

The best way to analyze both is to plot the total energy that will have the classic increasing sinusoidal shape before and after the stress DC Voltage. The results are shown in the Fig. 4.19; for what concerns the Panasonic Device, we have on the top part the total energy before the stress, after a certain stabilization time due to the non linearity on the current that makes the calibration useless in this range, we have that the energy increase linearly, after the stress, we have the same stabilization time due to the same reason but completely different with respect the Relax case and then the energy increases linearly and the losses are constant. Unlikely I performed this analysis several times with different stress time and sinusoidal amplitude but never exceeding 150 V, for technological limits it was the maximum reachable with the amplifier that I had, for all the cases after the stabilization time the value of the charging and dissipated energy was practically equal so with this kind of analysis I showed no influence on the Losses on a DC Bias. The only open question was the stabilization region were there was a substantial difference between the two cases; to check if this behavior was intrinsic of the measure, always in the Fig. 4.19, in the bottom part I presented the results when I applied the same excitation signal to a High Quality Factor Capacitor that was used in the calibration part and for this reason it should not present any kind of losses; this device had the same stabilization time and behavior so the strange

shape that characterizes the HEMT for the first part of the measure was normal and intrinsic of the measure and I cannot conclude on any kind of dependence of the Losses on a DC Bias stress.

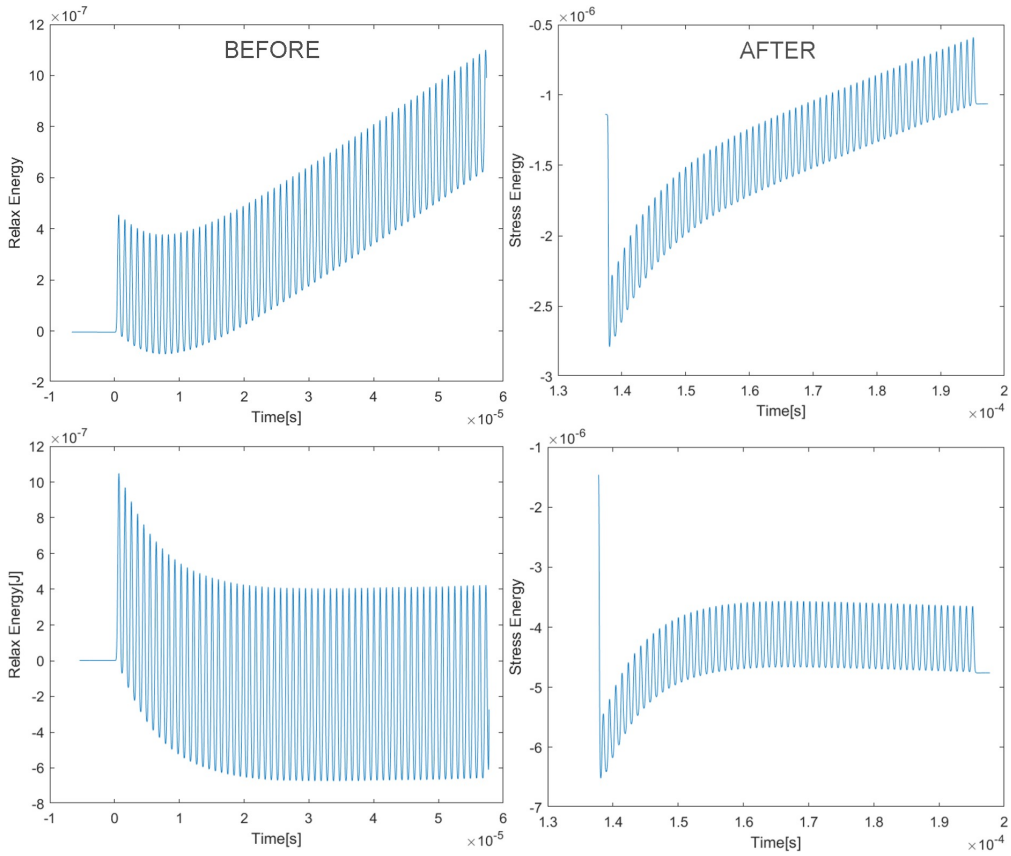


Figure 4.19: Total Energy Results of the DC Affecting Losses Analysis for the Panasonic DUT (up) and an High Q Capacitor (down).

At the end, this analysis did not confirm our suspicion, at the same way I cannot conclude that there is no dependence of trap states losses on a DC Bias, I just applied small amplitude sinusoidal voltage (up to 100 V) and a stress of (150 V) for just one kind of device, If I had the possibility to go higher there are good possibility to have some differences in the output capacitance response since in the reality, I measured a very small difference on the dissipated energy but too low with my parameters (less than 10%) and so I copuld not confirm this effect but with the possibility to apply a 200 Vpp sinusoidal voltage and a 300 V stress Bias there are good chances to obtain a dependence on the hysteresis effect. For time reason, I had to go further with the Loss Analysis of GaN buffer and I finish here this part with only a suggestion for future analysis.

4.11 Conclusion

In this chapter, the output capacitance losses have been analyzed for two important commercial devices: Super-Junctions and GaN High Electron Mobility Transistors. For the former, the losses have been analyzed for one commercial device and an explanation have been found also in accordance with the literature results; for the last one, there is no a demonstrated explanation of the physical reason of the Output Capacitance Losses but just a really accredited hypothesis, I have measured the same results of the literature that used the Sawyer-Tower technique and so confirming the results but thanks to the exploitation of a new more flexible method I could perform more sophisticated analysis giving extra insights on the physical phenomenon that characterizes the losses of this kind of devices. I linked the output capacitance losses to a dependence on the bias voltage, showing a correlations with partial hysteresis analysis when the amplitude was fixed but just the DC bias was increased, a dependence on the starting voltage, obtaining a relation for a threshold voltage for having hysteresis losses at the output and finally a dependence on the duty cycle of the applied sinusoidal signal, showing also in this case a threshold time after that we have the normal hysteresis losses. Finally I also tried to relate these losses to a dependence on a stress DC voltage applied on the DUT but unlikely I could not get any positive results about this, just supposing an hypothetical dependence that can be analyzed by future measurement. At this point, for time reason I had to finish the Off-Chip Analysis and passing in the second and last part of this thesis the On-Chip analysis so exploiting this method for on-wafer analysis that is another advantage with respect the ST method.

Chapter 5

On-Wafer Analysis of GaN Buffer Losses

Another important aspect of this new large signal method was the ability to be applied also for on.wafer analysis, differently from all the reported methods in the Chapter 2, this possibility opened new opportunities in the characterization of GaN Buffer Losses.

In this chapter, I am going to measure and analyze High Frequency losses directly on GaN-on-Si Buffer thanks to a probe station and some devices already available in the Lab.

The analysis will not be so straightforward, also if the device can be schematized by an RC system, some non linear effects as resonances characterize the spectrum of losses in the MHz range of these kind of devices.

The complete understanding of these effects was really hard but some hypothesis and checks have been proposed. Before of this, I will start with the presentation of the problem.

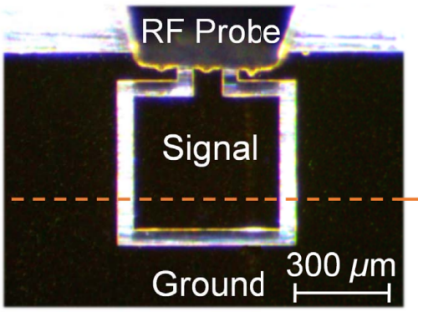
5.1 Introduction

In the previous chapter, I highlighted lower than expected efficiency of GaN HEMTs, showing energy dissipation in charging and discharging of the output capacitance and the investigation of this phenomenon has found the origin of these losses in the GaN-on-Si epitaxial structure.

In [11], a precise small signal on-wafer method, that was explained in the State of Art Chapter, was used to evaluate C_{OSS} losses in the MHz range and some unexpected resonant lossy peaks were revealed in GaN-on-Si epitaxies.

The test structures analyzed in [11], that will be subject also of my analysis in the following chapter is pictured in the Fig. 5.1a with a photo of the GaN-on-Si

(a) Picture of the GaN on Si Buffer.



(b) Optical image of the test structure measured with an RF probe [11].

Figure 5.1: Test Structures.

wafer analyzed in my thesis.

In the Fig. 5.1b, there is an optical image of the measured device with in the top part also the RF probe used for all the future analysis performed in these devices, it is the Infinity Probe GSG 150.

The test structure is divided in a ground and a signal pad which is used to extract the C_{OSS} losses. The ground pad is considerably larger than the signal one, forming a giant capacitance with the substrate which ground the doped Silicon substrate at the radio frequency (in our operating frequency, we have an excellent ground connection), the cross section is presented in the Fig. 5.2, in which the two capacitance are showed, the large ground pad, that ground the substrate, and the epitaxial pad at which the wave is applied and the reflection is measured, then it is possible to extract the impedance and the losses (See Chapter 2).

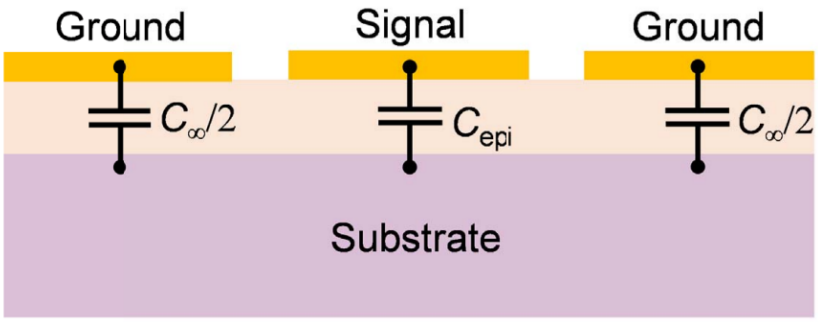


Figure 5.2: Cross-section illustration of the proposed test structure [11].

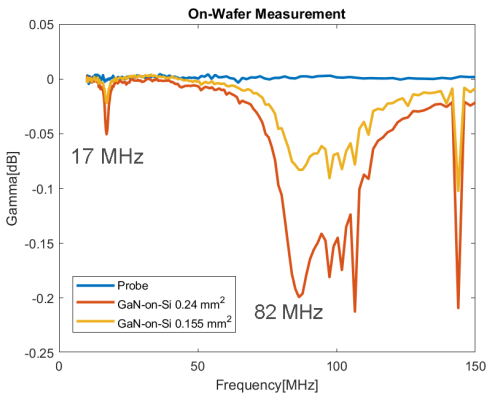
The area of the signal and ground pads are 0.24 mm^2 and 3.7 mm^2, respectively,

and the thickness of the pads is 300 nm (270 nm of gold with 30 nm of titanium adhesion layer). The measured reflection coefficient and the extracted losses are plotted in the Fig. 5.3a and Fig. 5.3b for different devices in the same wafer; in the first image, it is shown the reflection coefficient for three test structure: the open condition in which I measured only the reflection from the probe and the results for two different pad area Devices, both are characterized by considerably higher losses with two pronounced peaks at around 17 MHz and 82 MHz; in [11] these loss peaks have been analyzed also for a SiO_2-on-Si sample, suggesting that the Si substrate is a potential origin of C_{OSS} lossy peaks in GaN-on-Si HEMTs.

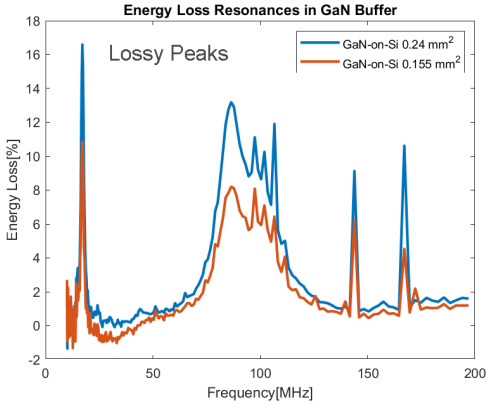
These peaks in the gamma coefficient are translated with the appropriate equations to peak in the percentage of dissipated energy for this reason this effect can limit the maximum operating frequency and also the performance for these kind of devices.

At the correspondence of the peaks, two phenomenon are observed: a peak on the resistance and an abrupt change on the capacitance also of the 25% like observed in [11]; moreover this energy dissipation depends on the switching time and so it may limit the performance of the Device. Since these resonances are very close, the idea about their origin is focuses on a strong material dependence.

This effect shows the importance to characterize C_{OSS} losses at high frequencies and one of the main reason of why I developed a new large signal method to characterize them also for on-wafer measurements.



(a) Reflection Coefficient results for the probe (Open) with two different signal pad area GaN-on-Si Buffers.



(b) Energy Loss results for the probe (Open) with two different signal pad area GaN-on-Si Buffers.

Figure 5.3: Small Signal Analysis of the Test Structures.

5.2 Measurement Setup and New Calibration

Before starting with the analysis, I need to present briefly the new setup used for the Large Signal Analysis of GaN-on-Si Buffer. The picture of the proposed new setup is presented in the Fig. 5.4, starting from the right we have an orange cable from which the input signal was injected, it starts from a signal generator that creates the sinusoidal voltage that is then amplified by the High frequency Amplifier. After the input signal goes through the input of the PCB, connected to the Probe station thanks to SMA connectors, always characterized by the voltage and current probes. The PCB terminates with the Infinity Probe (the same used for the Scattering Parameter Small Signal Method in the previous chapter). Finally we have the chuck on which there is the DUT kept fixed by vacuum made by some holes on the chuck itself.

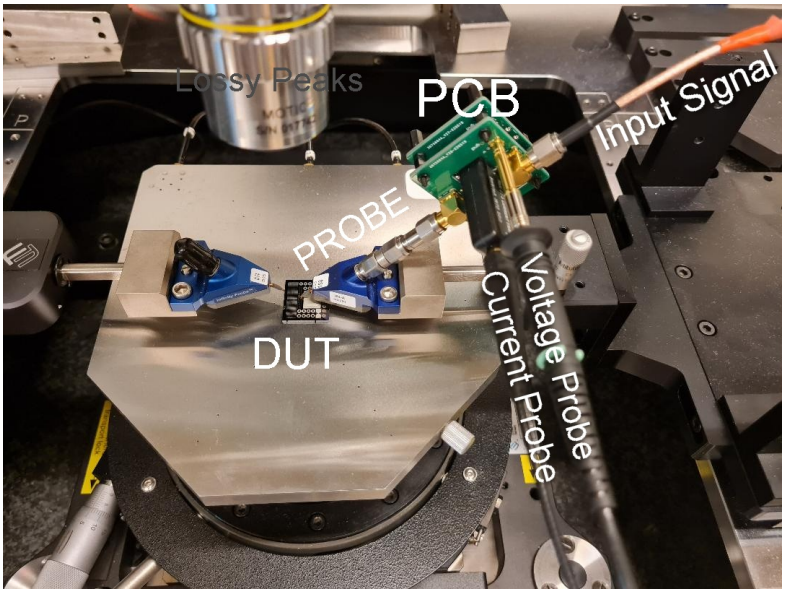


Figure 5.4: Measurement Setup of the Large Signal Method for On-Chip Analysis.

Due to the probe connections with respect the direct SMA connection to the DUT for off-chip analysis, the extra elements forced me to complex the calibration, the delay was found to be almost identical to the previous case but for better accuracy in the results I added an extra impedance in the circuit model; previously it was based only on parallel lumped element Z_0, for these analysis I have added a series element after the parallel one, Z_S. At this point, we need to measure it and compensate in all the analysis, for example if I measure an impedance Z, the actual Z_{DUT} is given by de-embedding the setup, so obtaining: $Z_{DUT} = \frac{Z \cdot Z_0}{Z_0 - Z} - Z_S$ The calibration was performed by applying a 10 Vpp sinusoidal voltage from 10 MHz up

to 100 MHz to the open circuit condition (Z_{open}) and to the short circuit condition (Z_{short}), then due to the kind of connections I could suppose that $Z_{short} \ll Z_{open}$ and so after measured these two conditions I have just assigned the following calibration:

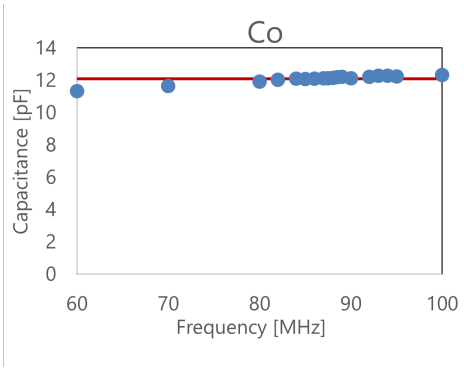
$$Z_0 \approx Z_{open}$$

&

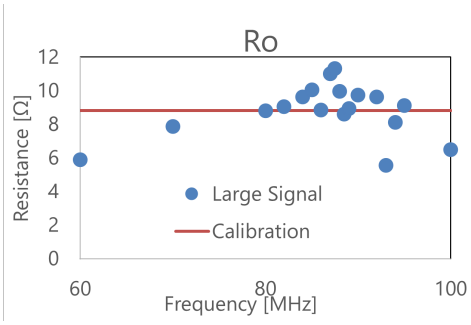
$$Z_S \approx Z_{short}.$$

The results of these calibration are shown in the Fig. 5.5, the blue dots are the results I got by the above approximation, in particular I got the following mean values: $C_0 = 12\,08$ pF, $R_0 = 8.9\,\Omega$, $L_S = 31\,5$ nH and $R_S = 1.93\,\Omega$; at this point it is possible to compute the impedance Z_0 and Z_S in the MHz range and have the confirmation of the previous approximation.

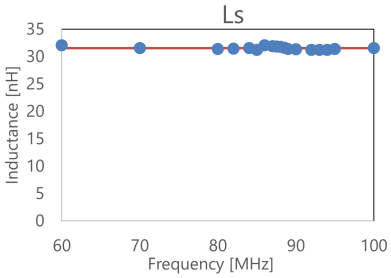
The first step on the analysis, performed also for checking the quality of this calibration, was the measure of another kind of device, similar to the GaN-on-Si Buffer but with an addiction of another layer on top: the AlGaN.



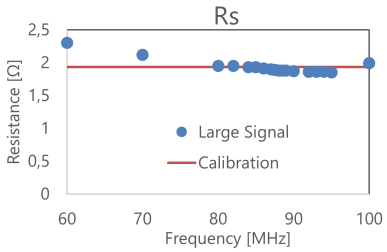
(a) Calibration pf the Parallel Output Capacitance of Z_0.



(b) Calibration pf the Parallel Output Resistance of Z_0.



(c) Calibration pf the Series Output Inductance of Z_S.



(d) Calibration pf the Series Output Resistance of Z_S.

Figure 5.5: New Setup Calibration.

5.3 Analysis of 2DEG Buffer

The analysis of losses on GaN-on-Si Buffer starts with a different kind of device always present in the Fig. 5.1a, the set of five devices in the below part of the picture. These devices are characterized by the addiction of a top layer made of AlGaN that acts as Barrier Layer and creates at the interface with the GaN the 2DEG, an active layer that will behave as a dominant impedance in the analysis indeed by charging the signal pad we are going to deplete the 2DEG that will dominates the energy analysis.

Since we need just to deplete the 2DEG, the applied sinusoidal voltage had an peak-to-peak voltage really small considering all the previous analysis, only 1 Vpp, from this we can expect a good match with the VNA measurement.

The resulting impedance in plotted in the Fig. 5.6a and Fig. 5.6b, the blue dots are the results I got with the large signal method and with the new calibration compared with the Scattering parameter method.

The capacitance of this device decreases with the frequency starting from a relatively high value with respect the simple GaN-on-Si Buffer as shown in [11], at least one order of magnitude; the same for the resistance that can be considered analogous to energy losses (same trend) decreases with the frequency almost linearly.

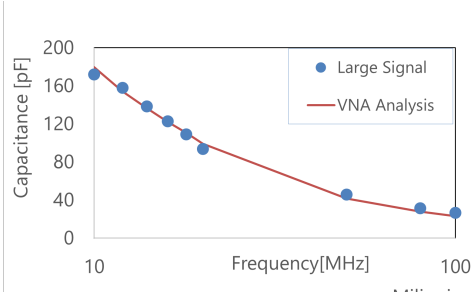
The match with the small signal method is really good, this also confirms the validity of the VNA analysis for energy loss measurements, this is also given by the relatively small signal applied with my method but necessary for the correct evaluation of the device.

The main reason of why these results are coherent with the theory is the presence of the 2DEG that entails an acceleration of Joule heating (higher scattering density) so higher Resistance and Energy Loss; the decreasing with the frequency is related to the charge and discharge of the 2DEG, at some value the electrons can no longer follow the frequency switch and the electrons remains at the interface, this effect generates the diminution of the capacitance and the resistance.

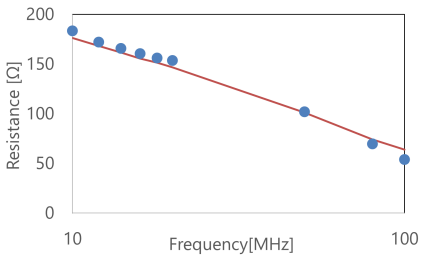
This was only an introductory part, just confirming the calibration and the setup, if it was possible to apply the method for on-wafer measurement, being able to extrapolate good results, from here we can move to the GaN-on-Si Buffer, being sure of the correct operation of the method.

5.4 Large Signal Analysis of GaN-on-Si Buffer Losses

At this point, we can come back to the GaN-on-Si Buffer, starting my analysis by measuring the losses with my large signal method, trying to understand new insights about their origin.



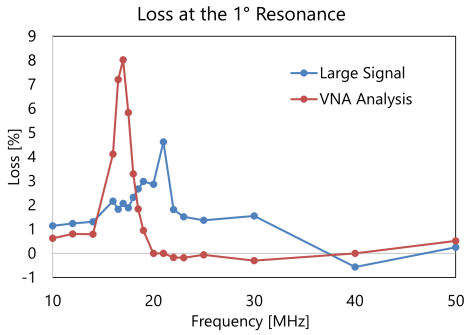
(a) Capacitance Results for the 2DEG Buffer.



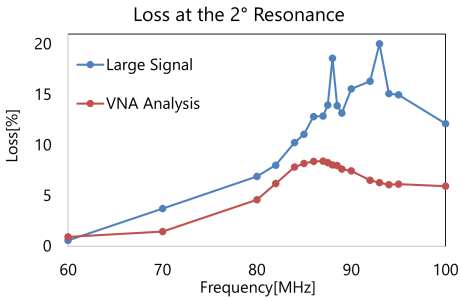
(b) Resistance Results for the 2DEG Buffer.

Figure 5.6: Impedance Analysis of 2DEG Buffers.

For convenience, I divided the analysis in the two range; 10 MHz - 50 MHz and 60 MHz - 100 MHz, analyzing the two peaks separately, then I applied in the first range a 15 Vpp sinusoidal voltage (note that there is no more the bias tee to make the signal positive since the body diode is not present and so the DUT does not conduct for negative voltage), for a single frequency at a time; the results are shown in the Fig. 5.7a, there are two important differences between the two measures; the different shape of the peak and a slight shift on the frequency. When we noticed this, we started reasoning about these two facts, also after repeating the same measure multiple times, the results were always the same; the first step to understand what was happening inside the device, it was to perform the same measurement at the second peak and check if the same phenomenon was observed.



(a) Comparisons between the Large Signal and the VNA Analysis at the 1° Peak.



(b) Comparisons between the Large Signal and the VNA Analysis at the 2° Peak.

Figure 5.7: Match between the Small and Large Signal Analysis on GaN-on-Si Buffer.

The results for the second peak are shown in the Fig. 5.7b, we can observe the same two phenomenon: a change in the amplitude and the same shift of about 3

MHz.

The first idea that came up to us was to associate the shift to a mechanical nature indeed the large signal and the VNA analysis were performed in two different but close probe stations (same infinity probe) and the change in the chuck and the different mechanical structure could cause the shift on the resonances; this mechanical association on the resonance peaks was an interesting idea and we also got two ways to try to verify this idea: dicing of the device so changing the mechanical structure and observing the same phenomenon (for time reason I could not analyze this idea and decided to choose the second one) or simultaneous analysis on different VNAs, changing continuously the probe station.

For the sake of simplicity, I have just tried the second idea also due to the presence of a second VNA in the lab characterized by four ports (Agilent Technologies N5230A). The starting strategy is to perform the same Scattering Parameters Analysis (same setup conditions) on the two VNAs (same probe station) and observe any differences in the results. This analysis is shown in the Fig. 5.8, we can observe one important point, the 17 MHz peak is not present in the second VNA analysis, at its place there are smaller peaks, around 2%, negligible for the energy losses analysis of the Buffers. This measurement was performed several times, repeating the calibration of the tool in different time moments.

From the shift question, we changed our mind, the point was if the 17 MHz peak was real and not given by some weird effects of the first VNA; for the second peak no differences were found in the analysis and so its presence and effects on the performance of the GaN devices have to be taken into account.

At this point, we needed to understand the effective presence of the 17 MHz peak, with just the VNA analysis it was no clear its presence, we needed to exploit the large signal analysis but in this moment of the time there was a problem of this method: the Single frequency Analysis.

The possibility to measure only one frequency by time did not allow us to have the continuity of the analysis and so some incoherence in the results can be found, for example in the Fig. 5.7a, the peak was just identified as one single point and so the incorrectness of this value can be taken in consideration.

The next step was to generalize the large signal method so that a frequency continuous analysis can be a possible measurement; the type of signal that we needed for a better accuracy of this measure is a modulated frequency one, that means by keeping the amplitude fixed we have to change the frequency starting from 10 MHz up to 100 MHz.

To generate this signal, I could not use the internal function of the signal generator since the output was not synchronized with the trigger so not being able to average on more cycles (one cycle is not enough for accuracy), the idea was to use the arbitrary function generator of the tool trying to create the signal shown in Fig. 5.9.

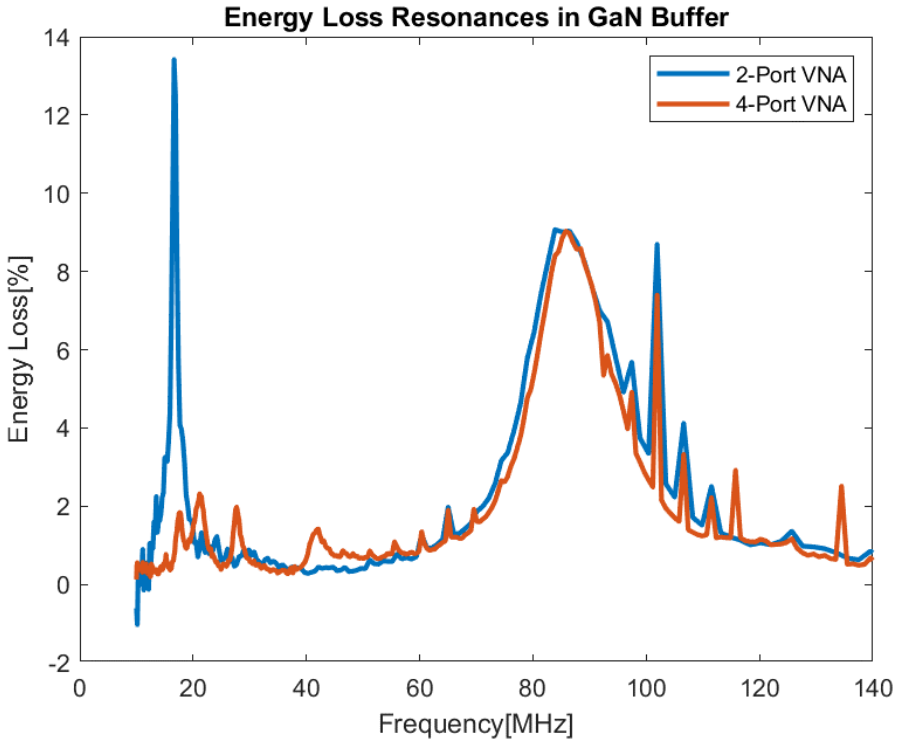


Figure 5.8: Comparisons between two VNAs Analysis at the same conditions.

The next step was to solve some problems that this analysis has reported intrinsically, the first point is the calibration, indeed we know that our method is based on a delay that is constant only on Voltage but not on Frequency, luckily in the Chapter 3, the calibration showed an almost constant delay after 10 MHz (reason of why I chose this value as starting frequency), this is the first approximation that I had to consider for the analysis. The next point was the high number of data and the huge dimension of the file (5 million points) that did not allow me to interpolate and so increasing the quality of the measure, this is the second approximation for the results I got.

My objective in this case is to find the impedance, expressed in function of its amplitude and phase, the idea was to divide the 5 millions points for the voltage and also for the current in fixed parts and analyzing separately, extrapolating for each section the respective amplitude and phase.

The first time I tried to extrapolate this parameters, for the amplitude I have just divided the average between the local maximums and minimums of the voltage and current in the respective section (I found the peaks of the signals for each part) and for the phase, what I did also for previous measurements, was to find the shift between the current and voltage in order that the difference in absolute value

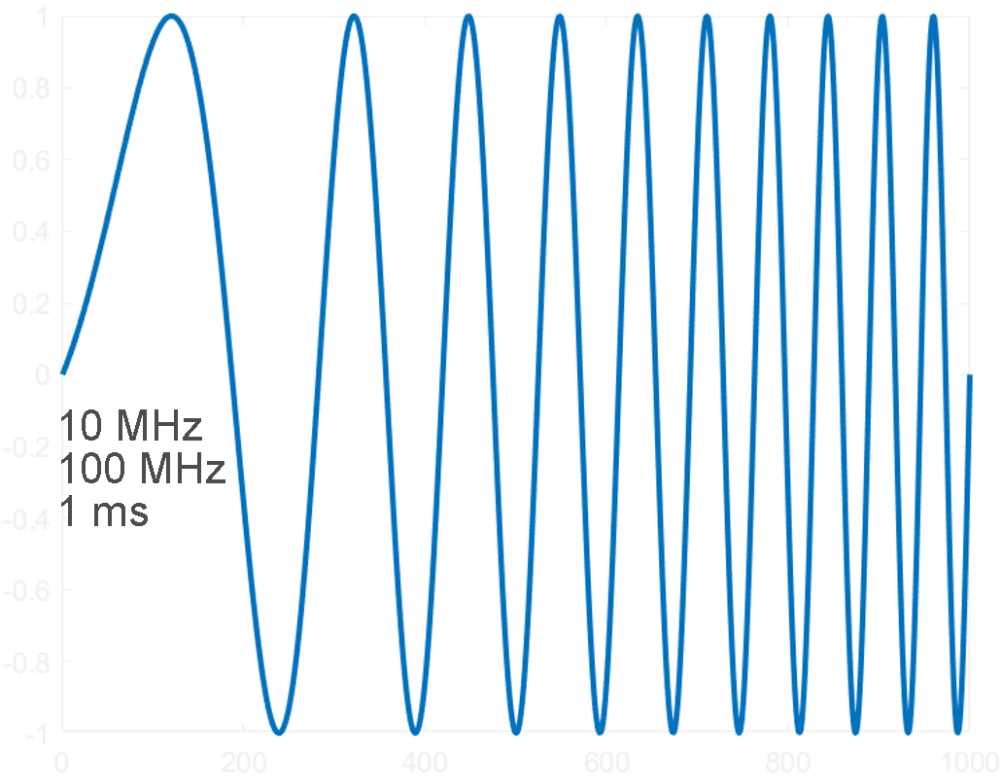


Figure 5.9: Input Signal Generated for Frequency analysis with the large signal method.

is minimum, the first results of this kind of strategy were unsuccessful because of errors in the amplitude and phase. Indeed considering the final results, they were incomprehensible, the total impedance was characterized by a clear shape but made by huge oscillations that made the resonances impossible to observe.

For solving this problem, we had to think at what at the end we want to compute that is not the impedance (from it measuring the quality factor and then the energy loss) but the percentage of energy loss that is directly related to the quality factor. Our system based on the GaN-on-Si Buffer can be generalized by an RC system, the total impedance, Z, is:

$$Z = R + \frac{1}{j\omega C}$$

$$Z = \frac{1}{\omega C}(-j + R\omega C).$$

But the quality factor is the ratio between the imaginary and real part, so:

$$Q = \frac{1}{\omega C R}$$

$$Z = \frac{1}{\omega C}(-j + Q^{-1})$$

the phase, ϕ, is;

$$\phi = tan^{-1}(-Q)$$

and so the quality factor Q is;

$$Q = tan(-\phi).$$

This last equation confirms a very important aspect, we do not need to compute the amplitude of the impedance but only its phase for obtaining the quality factor and, after, extrapolating the energy losses. This is the main simplification of this analysis, then we had to change also the method of how we measure the phase, previously i just subtracted the voltage and the shifted current signal and found the minimum. The problem of this method is due to the non linearity of the current signal that is not anymore a pure sinusoidal signal and so finding the phase in this way can give in wrong values.

The idea to solve this problem was to find the phase considering separately the two signals, I found the respective delay of the two output with respect a pure sinusoidal signal, $sin(\omega t + \phi)$, where for the frequency I computed the inverse of the difference of time between the first two peaks of the voltage signal (that is more linear), and I proceeded at the same way, finding the minimum of the difference between the pure sinusoidal signal and the outputs of the PCB. Finally I subtracted the two phases that I found, obtaining a more clean and linear result.

At the end of the day, I analyzed the frequency behavior of the Buffer with the large signal method and my results are shown in the Fig. 5.10, we see that the 17 MHz peak is actually not present but there is, with a smaller amplitude, another peak at around 28 MHz that looks matching the same small peak in the Agilent VNA analysis, instead the second one presents the same characteristics of the VNA analysis but with higher percentage of losses.

In general in this plot it is like the Large signal analysis presents a sort of background loss, resulting from the constant delay approximation and the missing interpolation of the data that forced me to consider a delay approximated up for the total range, in this way there is a positive energy loss common for all the analysis, this can explain also the much higher losses with respect the VNA case of the Large signal for the second peak. In conclusion the 17 MHz peak is sensitive to the VNA, the large signal showed the presence of a peak but with small amplitude, likely it can resonate with the setup itself, the higher frequency instead is much more stable.

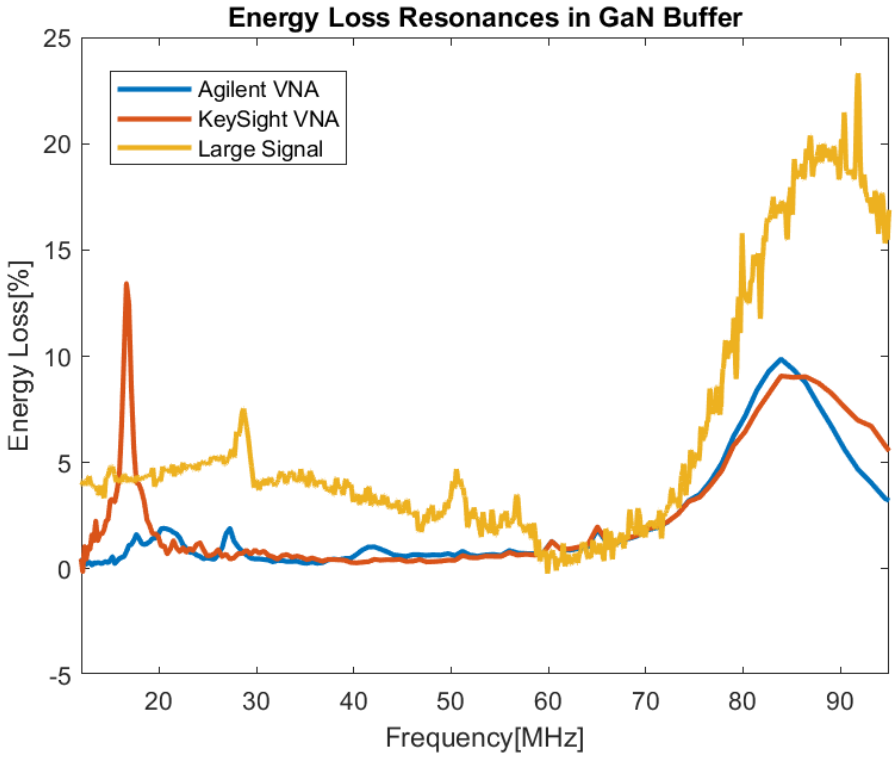


Figure 5.10: Energy Loss Comparison of two VNA Analysis and the Large Signal one on the GaN-on-Si Buffer.

5.5 Large Signal Analysis of GaN-on-Si Buffer Losses: Up to 100 Vpp

Until this moment, I always called large signal method but in all the previous analysis the maximum peak-to-peak voltage was 15 V (not a real large signal analysis compared to the 400 V of the off chip analysis); due to the high frequency i could not reach the 400 V of the off chip analysis, the maximum was 100 Vpp.

For accomplishing this task, I have exploited all the previous advances, same frequency modulated input signal with a burst period of 100 ms but due to the high voltage I added the same high frequency amplifier presented in the previous chapter made by a GaN transistor and so by just increasing the amplitude of the input and increasing the minimum to 0 V to not have negative values that are not amplified and, at the same time, activating the gate with a internal DC bias voltage of the input FM signal I started from 10 V and reached up to 100 V considered the maximum for the setup and technology used.

The results are shown in the Fig. 5.11, the problem of this analysis was the non linearity of the current that was not sinusoidal for the first part of the analysis and

so the results were coherent only for the high frequency part (higher than 60 MHz), for time reason I could not solve the problem for the low frequency part.

For the high frequency part, we observe the increase of the loss where there is the resonance but increasing the voltage does not entail an increase in the percentage of loss rather the loss decreases, the resonance is less 'strong', the loss goes down up to 10% and in general the total trend is constant, the effect of the resonances may change on the voltage and depends on it, this also can be observed looking at the differences between the small and large signal results in the previous section.

This concludes for now this analysis, for timing reason I could not investigate more about this phenomenon. At the end, the high voltage, at which is related also an higher temperature of the device, can reduce possible Silicon defects effects in the substrate that generates the resonance, like for the hysteresis losses in the commercial device, the temperature, affecting trapping/de-trapping time, can decrease resonance lossy peaks, leaving only constant resistive losses.

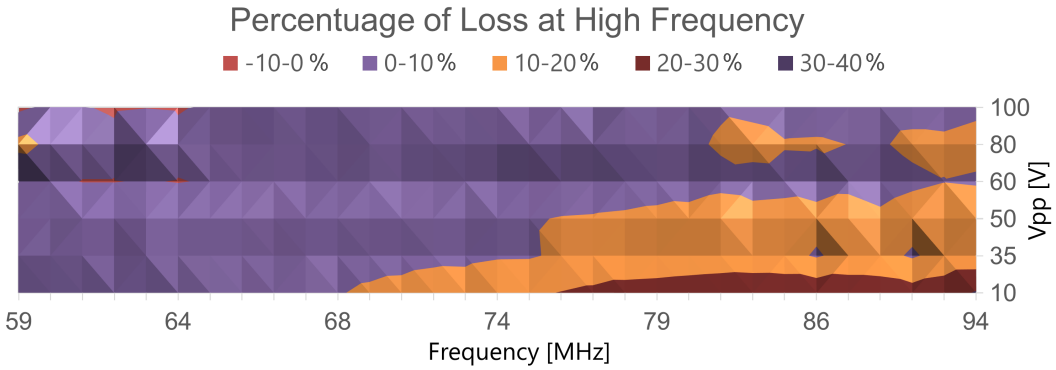


Figure 5.11: Frequency-Voltage Table of the percentage of Loss at high frequency for GaN-on-Si Buffer.

5.6 Conclusion

The Large Signal analysis on the GaN-on-Si Buffer ends the characterization of the resonance lossy peaks, with the possibility for future measurements to go further with the voltage or Temperature, observing any reduction of the high frequency losses, so confirming the defect nature of the 82 MHz peak.

For the lower frequency part, the time and the impossibility to extract coherent results in the large signal analysis could not allow me to understand if there are any modification in voltage but the 17 MHz has been characterized with many techniques multiple times, its existence is not still clear since the large signal analysis

confirmed the presence of an 28 MHz lossy peak coherently with the Small Signal Analysis with the Agilent VNA, the question is if it the 17 MHz peak coincides with this second peak or they are different and their presence depends on the measurement setup and type of analysis. Another effect is its real effectiveness, the percentage of loss measured was smaller compared to that reported at the beginning of the chapter.

It would be really weird if the physical phenomenon inside the two resonances is not related to the same material of the Buffer, indeed if both have been determined also in $Si - on - SiO_2$ buffer, the possibilities of their origins concern only the Silicon layer and defects at the interface.

I am quite sure about the 82 MHz (explained above), the open question, due also at strange behavior with the different analysis, was the nature of the first peak, different VNAs showed different spectrum and the large signal just a small peak (almost negligible), this multiple nature can be given by different interactions of the Si-on-GaN Buffer with the instruments used for the analysis or with the probe station.

This phenomenon requires further characterizations to be fully understood and more sophisticated measurements with this new large signal method can lead to a more deep understanding of the physics behind these effects.

Chapter 6

Conclusion

The most important material in Power Electronics is the Gallium Nitride (GaN) due to its outstanding properties: High Breakdown Voltage, Wide Bandgap and Large Mobility of the Electrons. Unlikely unexpected losses in GaN technology due to trap defects in the Buffer limit its performance and development as Silicon substitute. The main device based on GaN is the High Electron Mobility Transistor (HEMT) that exploiting the 2 Degree Electron Gas (2DEG) presents higher mobility of the charges and lower on-resistance so showing better performance comparing to the Si MOSFET especially at high frequencies. This device presents some unexpected losses, the most relevant are the degradation of the on-resistance and the Output Capacitance Hysteresis Losses indeed it has been shown that, charging and discharging the Output capacitance, an hysteresis is present which area is the energy loss. The cause of this phenomenon has been identified on buffer defects of GaN HEMT like threading dislocations which act as trap states, these defects are due to the large lattice mismatch of GaN and Si, so several depositions and doping are needed for having a good GaN-on-Si layer with low leakage current but inducing a high concentration of defects inside the Buffer. The mathematical theory on this type of effect proves that the physical parameters that can affect the C_{OSS} Losses are the frequency, the voltage and dv/dt (slew rate), considering the Output capacitance in series with a (approximation) linear Resistance (ESR). The main methods used for the measurement of C_{OSS} hysteresis can be divided in large signal like Sawyer-Tower and Non Linear Resonance and small signal like Linear ESR or Scattering Parameters. The working principle is completely different each other and have different advantages and accuracy. I noticed right away that for a deeper analysis of C_{OSS} Losses, I needed a new method with less limits. This new method is based on the generation of a sinusoidal signal that gets correctly amplified and superimposed to a DC bias for not having negative voltage (body diode), then it is supplied to a Printed Circuit Board (PCB) at which output is connected our Device under test (DUT). Then, I measure with two different probes

the voltage and current across the DUT and can extrapolate the stored charge, the C_{OSS} and the energy dissipated. This method needs a calibration since the two signals have a different delay according to their probe, this delay was proved having only a dependence on the frequency of the sinusoidal voltage. After I have validated the model by measuring the main parameters of an RC system and its energy analysis and compared the results with an Impedance Analysis and a Spice simulation. In this way, I could have an idea of the power of the method and if it was possible to get coherent results with the theory, avoiding the presence of an intrinsic error of the setup.

After the verification, I have applied this method at two types of devices: Super-Junctions (SJs) and High Electron Mobility Transistors (HEMTs) for the analysis of their output capacitance losses which are unexpectedly different. For the characterization, I needed to permanently turn off the devices by shorting the source and gate. I started with the application of a classic sinusoidal voltage to check if the curves were coherent with the literature, reaching more complicated cases that resulted in new insights and characteristics concerning the losses in GaN Buffers. For the SJs, the losses have been analysed for one commercial device, the new method showed correct behaviour of the QV curves and the analysis of losses was comparable to what the ST method has got for the same device. After I have explained the reason why the C_{OSS} hysteresis happens for this kind of device. The hysteresis is dominant for low voltages, but after 200 V, the charge and discharge curve match, the reasons behind this phenomenon are the stranded charges in the depleted doped column that need much time for recombining or reaching the contacts. For the GaN HEMTs, there is not a demonstrated explanation on the physical reason of the Output Capacitance Losses but just a really accredited hypothesis. In this case, the hysteresis presents a complete opposite behaviour: almost zero loss for V lower than 200 V then the charge and discharge curve starts to mismatch; the reasons behind this effect must be different since in this type of device there are no doping regions that depleting can cause the blocking of majority carriers. I have measured the same results of the literature in which the Sawyer-Tower technique was used, so confirming this effect but thanks to the exploitation of a new more flexible method I could perform more sophisticated analysis giving extra insights on the physical phenomenon that characterizes the losses of this kind of devices. The more accredited hypothesis concerns defect states in the GaN buffer that can trap the electrons from the substrate or the active region because of their high energy and scattering effects, due to the high de-trapping time, these charges cannot be recovered, resulting in a charge imbalance during one cycle of the sinusoidal input, causing the hysteresis in the QV curve. At this point, I have exploited my method to perform more complex measurements; with the application of a fixed amplitude sinusoidal wave, I showed that the output capacitance losses have a dependence on the bias voltage, proving a reduction of

the losses when we increase the mean of the partial hysteresis. After I fixed the maximum voltage and increased the starting one, proving another more complex dependence, in this case I have obtained a relation for a threshold (starting) voltage for having hysteresis losses at the output. Finally, I found a dependence on the duty cycle of the applied sinusoidal signal, proving also in this case that exists a threshold time after that we have the normal hysteresis behaviour. This part finishes my Off-Chip Analysis and I started the second and last part of my studies: the On-Chip analysis, exploiting this new method for on-wafer measurements, an advantage with respect the other large signal techniques; this possibility opened new opportunities in the characterization of GaN Buffer Losses. I changed setup for the on-wafer analysis, I used a probe station and GaN-on-Si wafer, then I performed the measurement with the scattering parameter technique and some non-linear effects as resonances at 17 MHz and 82 MHz were present in the spectrum of losses in the MHz range for these kinds of devices. The complete understanding of these effects was really hard, but some hypothesis have been proposed. I started with a Large Signal analysis on these Buffers, the objective was to observe any modification on the resonance lossy peaks at high voltage. The 17 MHz has been characterized multiple times with small and large signals methods but its existence is not still clear since the large signal analysis confirmed the presence of a 28 MHz lossy peak coherently with the Scattering Parameter Analysis performed with another Vector Network Analyzer (VNA), the question is if the 17 MHz reported peak coincides with this second one or they are different and their effect depends on the measurement setup and type of analysis. The 82 MHz peak instead was identified by multiple VNA analysis, also the large signal found the same behaviour of the percentage of losses. At this point, I increased the voltage up to 100 V and measured the loss: for the low frequency part I could not extract coherent results, at high frequency, I observed a reduction on the effect of the resonance, this can be explained considering that at this voltage, the device has an higher temperature so reducing any kind of defect trapping effect that can cause the resonance (like C_{OSS} losses in commercial devices). It would be really weird if the physical phenomenon behind the two resonances is not related to the same material of the Buffer due to their proximity in frequency, furthermore these lossy peaks have been determined also in the Si-on-SiO2 buffer, the possibilities of their origins concern only the Silicon layer and defects at the interface. The 82 MHz peak nature is related to defects inside the Si substrate or at the interface with the GaN, the open question is the 17 MHz one that showed a different behaviour with the same analysis; different VNAs showed different spectrum and the large signal just a small peak (almost negligible), this multiple nature can be given by different interactions of the Si-on-GaN Buffer with the instruments used for the analysis or with the probe station. This phenomenon requires further characterizations to be fully understood, more sophisticated measurements with this new large signal

method, like increasing further the Temperature and Voltage, can lead to a deeper understanding of the physics behind these effects.

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