POLITECNICO DI TORINO

Master's Degree in Nanotechnologies for ICTs

Master's Degree Thesis

Design and Benchmarking of Low Power, Low Noise and Rad-Hard Comparators for Hybrid Pixel Detector for the Large Hadron Collider Upgrade

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Abstract

Hybrid pixel detectors allow to optimize separately the sensor matrix and the readout Application Specific Integrated Circuit (ASIC). Although the use of this type of detectors was extended to other fields of science by the Medipix collaboration, it is still employed at CERN (the European Organization for Nuclear Research) to assemble trackers for the Large Hadron Collider (LHC) experiments. The electronics associated to CERN detectors operates in a harsh environment, because of high levels of radiation and high magnetic field.

LHC detecting systems are constantly object of upgrades to improve their performances in terms of speed, resolution and power consumption. To this end, CERN microelectronics section recently choose a 28 nm bulk CMOS technology replacing older nodes in order to develop the next generations of read out ASIC. Thanks to the advantages of miniaturized transistors, a new prototype chip named PicoPix is under development with the aim to achieve a time resolution lower than 30 ps for large input charges.

A continuous-time discriminator is one of the key blocks of the hybrid pixel detector analog front end. It compares the signal originating from the sensor and amplified by the charge sensitive amplifier, with a threshold set above the intrinsic electronic noise. The output of the comparison must be a logic signal since it will be fed to the digital pixel. Four different topology were explored and compared, through simulations, to fulfil the requirement concerning time, mismatch, area and power consumption. Particular attention was given to the optimization of the jitter, which represents the switching uncertainty in the time domain. Some expedients were employed to make the circuits radiation tolerant. Moreover, a layout was developed for two of the topology considered, to evaluate the effects of parasitics on the jitter performance.

Acknowledgements

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Acronyms

ADC

Analog to Digital Converter

ASIC

Application Specific Integrated Circuit

CERN

Conseil Européen pour la Recherche Nucléaire

CMOS

Complementary Metal-Oxide Semiconductor

CSA

Charge Sensitive Amplifier

DAC

Digital to Analog Converter

FD-SOI

Fully Depleted - Silicon On Insulator

LEP

Large Electron-Positron collider

LHC

Large Hadron Collider

HL-LHC

High Luminosity Large Hadron Collider

IC

Inversion Coefficient

IP

Intellectual Property

MOSFET

Metal-Oxide Semiconductor Field Effect Transistor

OTA

Operational Transconductance Amplifier

PS

Proton Synchrotron

PVT

Process, Voltage and Temperature

SC

Synchrocyclotron

SPS

Super Proton Synchrotron

SR

Slew Rate

STI

Shallow Trench Isolation

TID

Total Ionizing Dose

TOA

Time Of Arrival

TOT

Time Over Threshold

TSV

Through-Silicon Via

VELO

VErtex LOcator

Chapter 1

Introduction

1.1 CERN

The Conseil Européen pour la Recherche Nucléaire (CERN) was the provisional council founded in 1952 by 12 European countries to build a first-class physics research facility with two fundamental objectives: to limit the phenomenon of brain drain towards America begun during the second world war and to create a sense of community in post war-Europe. The acronym CERN was then maintained to identify the European Organization for Nuclear Research, officially established in 1954 at the border between France and Switzerland. Geneva was selected among several proposals for its geographic centrality, military neutrality and because the city already hosted several international organizations. CERN currently counts 23 member states and around 2500 staff members but over 12200 scientists of 110 nationalities, from institutes in more than 70 countries are involved in projects related to the organization.

Initially, the laboratory was founded to deeply study the atomic nuclei but soon the main area of research became particle physics and that is why, throughout the years, CERN has developed and built state-of-the-art particle accelerators and colliders. The first accelerator, the 600 MeV Synchrocyclotron (SC), was turned on in 1957. In 1959 the Proton Synchrotron (PS) reached a beam energy of 28 GeV, a new record at that time; this facility has been upgraded in the course of history and is still active as beam provider for more powerful accelerators. The Super Proton Synchrotron (SPS) built in 1976 was the first underground accelerator with a diameter of 2 km; protons were accelerated up to 400 GeV investigating matter-antimatter phenomena. From 1989 and for 11 years the Large Electron–Positron (LEP) collider, 27 km of circumference, was operative researching on electroweak interaction. The same tunnel, 100 m underground, was then exploited for the construction of the Large Hadron Collider (LHC), started up in 2008 [1].

In April 2022, LHC has restarted for *Run 3* after three years of stop needed for maintenance, consolidation and upgrade work. Another long shutdown is foreseen in 2026 to allow the installation of the High Luminosity LHC (HL-LHC) project upgrades [2]. The R&D projects that will make the performance improvements possible are already in place for several years. Nevertheless, LHC is already the world's largest and most powerful particle accelerator.

During normal functioning, protons are firstly extracted from hydrogen. Once the proton beam is formed, its energy is gradually increased through a series of accelerators until a velocity closed to the speed of light is reached. Two counter-rotating beams are then fed into the LHC; they travel in ultra-high vacuum guided by superconducting magnets and collide in four different sites called experiments (ALICE, ATLAS, CMS and LHCb). From the collisions, that can reach energies up to 13.6 TeV, particles are generated and observed by the detectors which can give information about energy, mass, charge, velocity and position.

As it can be expected, the environment in which the detectors, and the relative electronics, have to operate, is extremely harsh because of the unusually high radiation level and the large value of the magnetic field (up to 8 T).

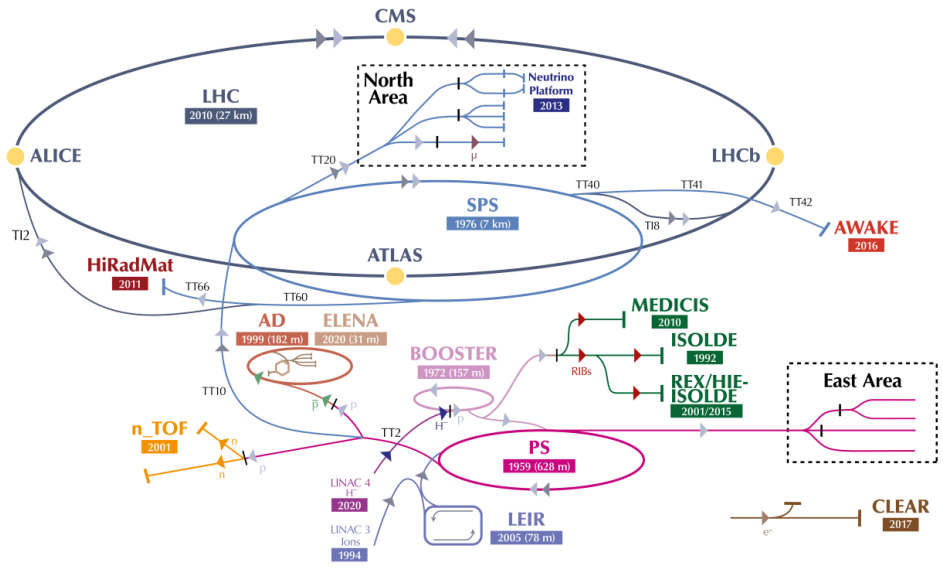
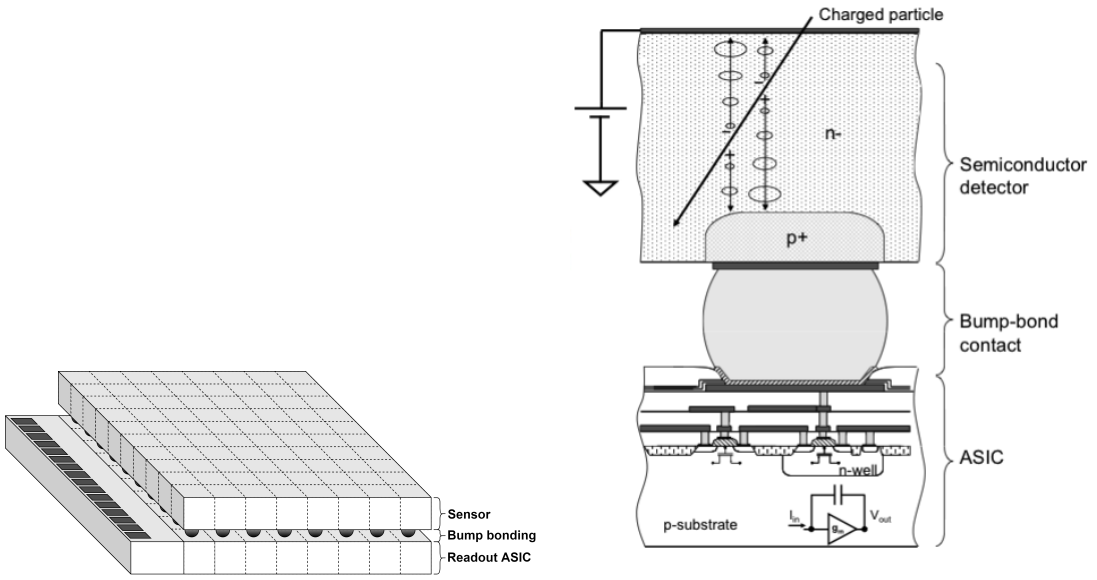


Figure 1.1: CERN accelerator complex [1].



(a) 3D view. **(b)** Schematic (not in scale) [3].

Figure 1.2: Hybrid pixel detector.

1.2 Hybrid pixel detectors and Medipix collaboration

The first hybrid pixel detectors were developed in the 1980s at CERN to deal with the challenging requirements of tracking detectors, such as spatial resolution, granularity and speed [4][5]. The peculiarity of this type of detector lies in the fact that the 2 dimensional sensor matrix and the corresponding readout electronics are manufactured in different substrates and then bonded together using flip-chip technology (figure 1.2). The main advantage is represented by the possibility of optimizing the sensitive element and the processing Application Specific Integrated Circuit (ASIC) separately. For example, depending on the targeted application, different materials, with different thicknesses, can be used for the sensor such as Si, GaAs, CdTe and CdZnTe. On the other hand, different designs of the readout electronics allow to measure various characteristics of the incoming radiation such as time of arrival, energy information and number of particles deposited during a given exposure.

In the framework of the LHC, hybrid pixel detectors are usually employed in the experiments as trackers, located in close proximity to the collisions site and able to record the trajectory of charged particles. For this purpose, the spatial resolution must be in the order of few micrometers. Moreover, the amount of data

sent out from the detectors has to be reduced as much as possible and its readout electronics must be fast enough to deal with the collision rate (up to 40 MHz).

Based on the experience accumulated in high energy physics, four European research institutes, including CERN, formed the Medipix1 collaboration in the 1990s with the aim of exploring the possibility to extend the use of hybrid pixel detectors to other fields of science involving X-ray imaging, in particular in the medical sector. After a series of encouraging results, the collaboration has been renewed and extended throughout the years to many other institutes, developing four families of readout ASIC [6][7]. The standard functionality of the Medipix chips is to register and count the number of hits above a threshold in each pixel. In this way, single photons can be detected and false hits due to electronic noise can be avoided. The aim is to provide noise-free images from X-ray and gamma-ray sources. Some characteristics of this family of ASICs are presented below.

- Medipix1 is the first chip developed by the collaboration and it was manufactured in 1997 [8]. It consists of a matrix of 64 x 64 square pixels with 170 µm pitch; the technology used for the design is the SACMOS1, with a minimum feature size of 1 µm and two metal layers available. Each cell has a Charge Sensitive Amplifier (CSA), a comparator with a 3 bits tuning Digital to Analog Converter (DAC) and a 15 bits counter that acts as shift register during readout.

- The Medipix2 chip was developed from 1999 to 2005 [9]. The main improvement compared to the previous ASIC concerns the spatial resolution: the pixel pitch is in fact reduced to 55 µm thanks to the use of a 250 nm CMOS process technology. The total number of pixels is also increased to 256 x 256. Another novelty introduced is the possibility of tiling the chip to three sides, allowing multiple units to be connected to a single sensor.

- The Medipix3 chip is designed using a 130 nm CMOS process but keeping the same pitch and the same total number of pixels as Medipix2 [10]. It introduces a sharing correction algorithm to correct the effect of charge sharing among pixels in the detector that negatively affected the spectroscopic imaging performance of Medipix2. Moreover, the chip can be configured in order to simultaneously collect hits and deliver data. The final version, called Medipix3RX, was fabricated in 2013 after seven years of development.

- The Medipix4 chip was submitted for fabrication in March 2022. It can be configured with 320 x 320 pixels with a pitch of 75 µm or 160 x 160 with a pitch of 150 µm [11]. The main novelty is the possibility of tiling the chip on all its four sides: this is achieved by moving the input and output pads and the peripheral circuits from one lateral edge to beneath the sensor pixels using Through-Silicon via (TSV) [12].

In parallel to the development of the Medipix family of chips, another family of ASICs, called Timepix, have been designed starting from 2005. These chips extend the functionality of the Medipix ones by introducing the possibility to measure the Time Of Arrival (TOA) and the energy of the hit, by recording the Time Over Threshold (TOT). For this purpose a clock is distributed to all the pixels. A summary of the characteristics of the Timepix ASICs is shown in table 1.1.

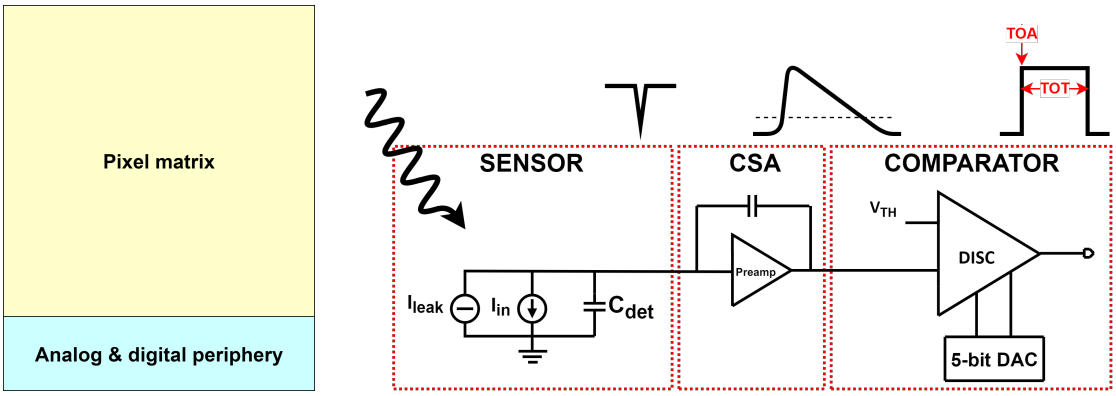
Table 1.1: Summary of Timepix chips characteristics.

	Timepix [13]	Timepix2 [14]	Timepix3 [15]	Timepix4 [16]
Year of production	2005	2018	2014	2019
CMOS process	250 nm	130 nm	130 nm	65 nm
Pixel pitch	55 µm	55 µm	55 µm	55 µm
Pixel matrix	256 x 256	256 x 256	256 x 256	448 x 512
Tiling sides	3	3	3	4
Time resolution	10 ns	10 ns	1.6 ns	200 ps
Readout architecture	Frame-based	Frame-based	Data-driven or frame-based	Data-driven or frame-based
Read/Write	Sequential	Sequential or continuous	Sequential	Sequential or continuous

The families of chips mentioned above have been exploited in many different fields: medical imaging, in particular computed tomography imaging [17], space dosimetry [18], electron microscopy [19], synchrotron application [20] and others. It also exists an educational kit, where a detector is installed on a USB stick that can be easily connected to a PC and allows to observe incoming particles: this is used, for instance, in partner high school to teach students about effects of radiation and to inspire the next generation of physicists and engineers [21].

1.3 PicoPix chip

The technology developed by the Medipix collaboration came back to CERN and LHC with the VeloPix ASIC [22]. This chip is based on Timepix3, but it is designed to be radiation tolerant and the data throughput is increased by a factor 10. It was used for the readout of the VErtex LOcator (VELO) in the LHCb experiment that was installed during the *long shutdown 2* (2018 - 2022). It is foreseen to further upgrade the VELO for *Run 5*, that will start in 2035. To this end a VeloPix2 ASIC will be developed based on previous chips but exploiting a 28 nm CMOS technology. PicoPix is the name of the demonstrator chip that is starting to be designed as first step in the VeloPix2 development.



(a) Floorplan. **(b)** Analog front end of one pixel.

Figure 1.3: Concept of PicoPix chip and its analog front end.

Figure 1.3a shows the floorplan concept for this ASIC. The analog structure of the PicoPix pixel is depicted instead in figure 1.3b. The sensor is modeled by the sensed current I_{in}, the capacitance C_{det} and the leakage current I_{leak}. The input charge is integrated by a charge sensitive amplifier, with a gain of 40 mV/ke$^-$, that also implements a compensation for the DC leakage current in the sensor. The CSA output signal is fed to a comparator, usually called discriminator in the radiation sensor field. This allows noise hit-free measurements by setting the global threshold above the intrinsic electronic noise. A 5 bits digital to analog converter is employed to adjust locally the threshold, compensating the pixel-to-pixel mismatch so to have a uniform voltage reference across the entire chip. The discriminator output must be digitally reconstructable because it is fed to the digital circuitry of the pixel. Counters and latches in the digital front end allow to measure the number of hitting particles, TOT and TOA on pixel. All the DC biasing needed in the analog front end are provided by global DACs implemented in the analog periphery. This area also contains a bandgap reference circuit and end-of-columns

circuits to configure the pixels. The digital periphery includes instead some control logic and the input/output interfaces.

The VeloPix2 (and PicoPix consequently) is still at an early stage of development, where the design team is exploring different solutions because the 28 nm CMOS technology is a novelty in the high energy physics community. For example, the sensor type is yet to be chosen; also two different pixel pitches are being considered, 42 µm and 55 µm. Moreover, the power density budget of this ASIC is under evaluation: for room temperature operation without active cooling the maximum is $1.0\,\mathrm{W\,cm^{-2}}$ but if active cooling is introduced it is possible to go up to $2\,\mathrm{W\,cm^{-2}}$, bringing benefits to the performance of the chip. A clear objective is to design an ASIC with a time resolution lower than 30 ps rms for an input charge of $10\,\mathrm{ke^{-}}$, that is equivalent to a 400 mV amplitude input signal fed to the discriminator. To this end a study of different topology for the comparator is carried out in this work optimizing the jitter with constraint on area and power consumption.

Chapter 2

Discriminator

2.1 Overview: static and dynamic characteristics

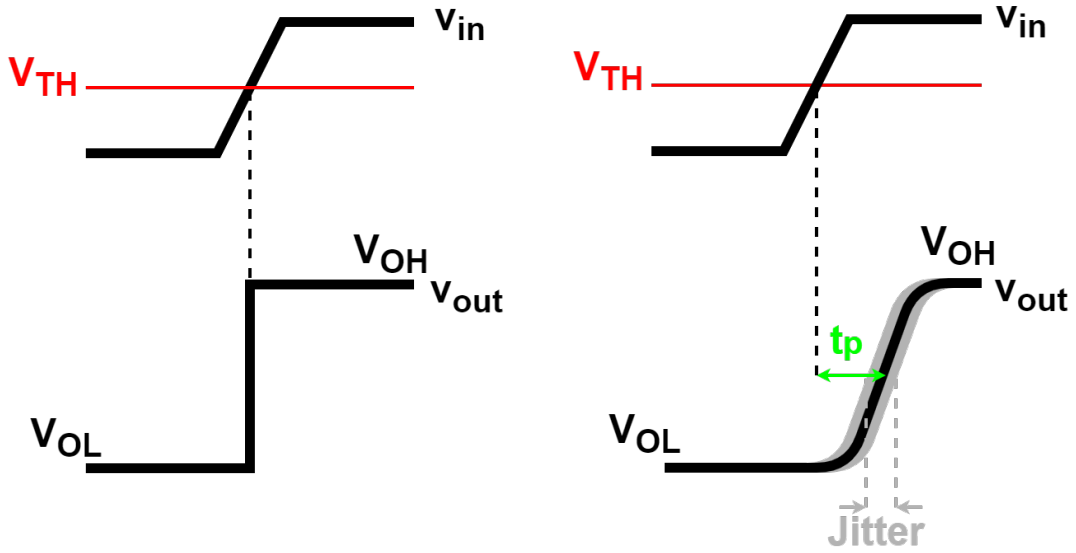
In general, the aim of a discriminator is to compare two analog signals and to provide as output a logic signal based on the result of the comparison. In this particular case, one input is the voltage signal originating from the sensor while the other input is a fixed voltage: if the CSA signal is above the set threshold, the discriminator output will be at the logic "one" (V_{OH}) otherwise it will be at the low logic level (V_{OL}).

Synchronous comparators are widely used in building Analog to Digital Converters (ADC) because of their good performances in terms of speed and accuracy. Nevertheless, in radiation sensors, continuous-time comparators are required to be developed for two main reasons: the first is the time unpredictability of the event to be detected; the second is to avoid the distribution of an accurate and high speed clock to a large number of analog pixels which could affect the behaviour of those sensitive blocks.

Ideally, the comparator should be able to resolve any slight difference between the two inputs and it should be able to switch instantaneously between the two output states when the threshold is crossed. However, this implies having a circuit with infinite gain and bandwidth. Real discriminators have finite gain and bandwidth, which result in a finite resolution and propagation delay. Moreover, transistor mismatch and random noise in the front-end electronics also affect the switching performances (figure 2.1).

The *resolution* of the comparator is defined as the minimum input signal above the threshold that can be detected correctly, delivering a clear binary signal to the digital pixel; it can be mathematically represented as follows:

$$V_{IN_{min}} = \frac{\Delta V_{O,\,HL}}{A_{v0}} = \frac{V_{OH} - V_{OL}}{A_{v0}}\,, \tag{2.1}$$



(a) Ideal. **(b)** Non-ideal.

Figure 2.1: Discriminator behaviour in time.

where A_{v0} is the static gain of the circuit [23].

The study of the dynamic characteristics of the discriminator is not trivial because it is intrinsically a highly non-linear component. The small signal approximation is only partially valid since the input signal amplitude is often large enough, making the comparator work in different operating region with respect to the linearization point. In this case they say that the comparator operates in slewing (or slew rate) mode. Also, the boundary between the slewing and the small signal operation modes is not clearly defined and that makes difficult to predict the dynamic behaviour of this circuit.

The discriminator *propagation delay* (t_p) refers to the time delay between the input crossing the threshold and the output responding to this excitation, by reaching 50% of the supply voltage. If a comparator completely limited by the slew rate (SR) is being considered, then the propagation delay can be expressed by the following [24]:

$$t_p = \frac{V_{OH} - V_{OL}}{2\,SR}\,. \tag{2.2}$$

If the input signal amplitude V_{IN} is comparable with minimum value detectable, $V_{IN_{min}}$, then a small signal analysis can be performed. Assuming a single pole

system with time constant τ_p, the transfer function is

$$A_v(s) = \frac{A_{v0}}{1 + s\tau_p}\,. \tag{2.3}$$

The output response to a rectangular step input with amplitude V_{IN} results to be

$$v_{out}(t) = V_{IN} A_{v0}\,(1 - e^{-\frac{t}{\tau_p}})\,. \tag{2.4}$$

Now defining $\alpha = {}^{V_{IN}}/_{V_{IN_{min}}}$ and considering the switching point corresponding to $v_{out}(t_p) = {}^{\Delta V_{O,HL}}/_2$, the propagation delay can be represented as follows [25]:

$$t_p = \tau_p \cdot \ln \frac{2\alpha}{2\alpha - 1}\,. \tag{2.5}$$

From equation (2.5), the graph in figure 2.2 is gathered, where the normalized propagation delay, ${}^{t_p}/_{\tau_p}$, is plotted as a function of α. It is easy to notice that an increase in the input signal amplitude causes a logarithmic decrease in the comparator time delay, which reaches asymptotically zero when α tends to infinity.

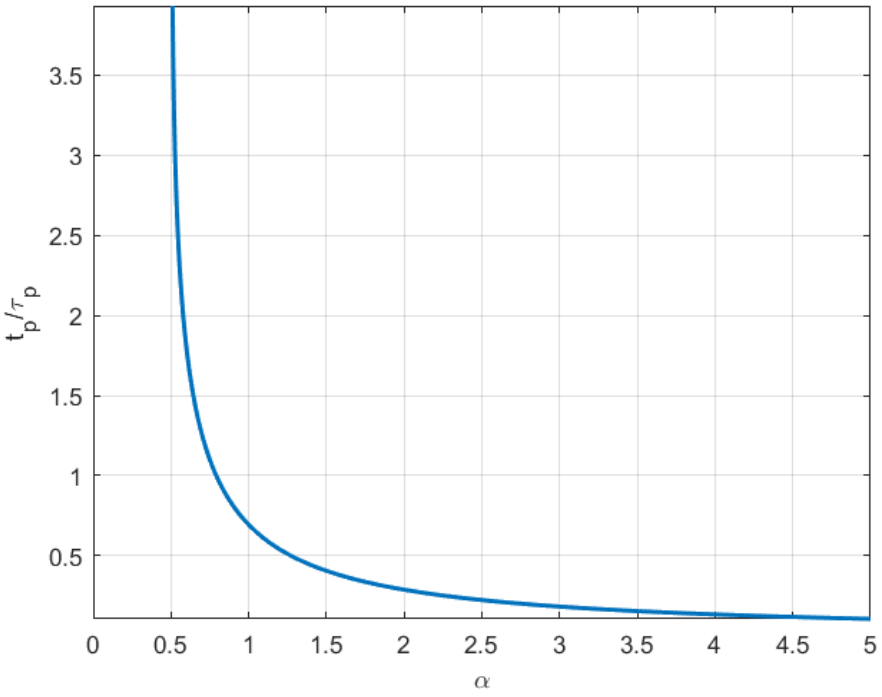


Figure 2.2: Normalized propagation delay.

2.1.1 Timing jitter

When the discriminator is fed repeatedly with identical input pulses, a time variability in the switching point around an average value can be noticed: this phenomenon is defined as *timing jitter* and it is due to the electronic noise intrinsically introduced by the transistors of the front end. Jitter can be interpreted as the transposition of voltage noise in the time domain and can be mathematically formulated as the ratio between the output rms noise and the output signal slope at the threshold crossing point:

$$\sigma_t = \frac{\sigma_v}{\frac{dv}{dt}|_{t=t_0}} \,. \tag{2.6}$$

It is straightforward to point out that a lower jitter is achievable by reducing the noise sources in the circuit for example by limiting the number of transistors. Moreover, fast discriminator is usually synonymous of low jitter discriminator. Indeed, the jitter is overall inversely proportional to the square root of the bandwidth since the noise is proportional to the square root of the bandwidth while the slope is directly proportional to it [25].

As stated in the previous chapter, minimizing the jitter is the primary motivation of this study on different comparator topology since the PicoPix chip has the goal of having a time resolution under 30 ps rms.

An example of jitter calculation for the single-ended Operational Transconductance Amplifier (OTA) in figure 2.3 is reported below. The OTA is approximated as a single pole system with static gain $A_{v0} = g_{m_1} R_{out}$ and dominant pole $\tau_p = R_{out} C_{out}$, being g_{m_1} the transconductance of $M1$, R_{out} the output resistance and C_{out} the output capacitance. Replacing these two quantities in equation (2.4), the maximum slope of the output signal can be computed as

$$\left.\frac{dv_{out}}{dt}\right|_{max} = \frac{V_{IN} g_{m_1}}{C_{out}} \,. \tag{2.7}$$

For what concerns the noise contributions, only the thermal component is considered. Flicker noise is neglected for two main reasons: the first is that the bandwidth of the front end is very wide and therefore, when integrated, white noise is dominant over $1/f$ noise. The second is that, as it will be further explored in the next chapter, the dimensions of the transistors in the treated designs are quite larger than the minimum size and flicker noise is inversely proportional to the area of the MOSFETs. Thermal noise in a MOS transistor is due to the resistance of the conductive channel and, assuming the MOS operating in saturation, it can be modeled as a drain to source current with a spectral density of:

$$I^2_{n_{th}} = 4 k_B T \gamma g_m \,, \tag{2.8}$$

where k_B is the Boltzmann constant, T is the temperature and γ is a transistor parameter depending on the Inversion Coefficient (IC) that swings from $1/2$ in weak

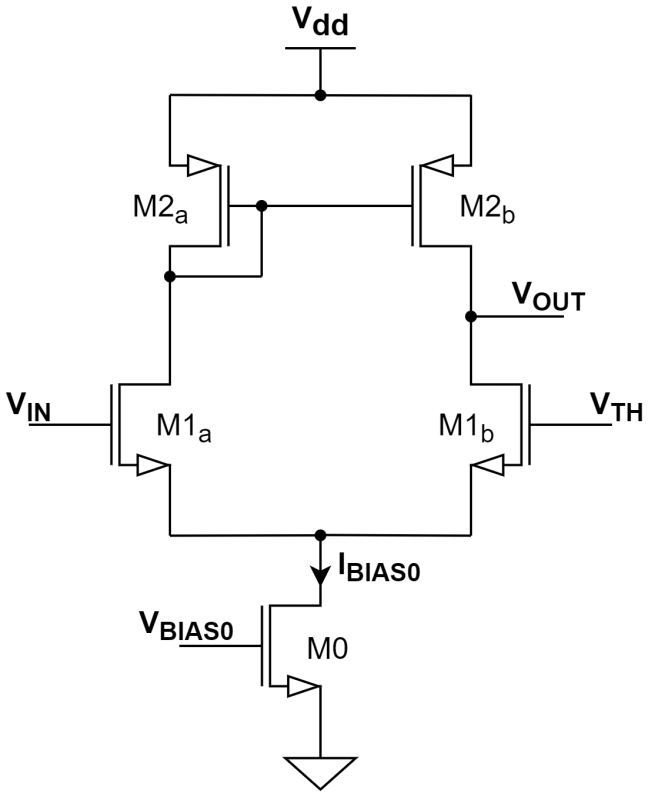


Figure 2.3: Single-ended OTA.

inversion region to 2/3 in strong inversion region. Assuming transistors $M1_a$ and $M2_a$ respectively identical to $M1_b$ and $M2_b$ and considering that the contribution of the bias transistor $M0$ is completely negligible, the total noise output current spectral density is

$$I^2_{n_{th},\,out} = 2 \cdot 4k_B T(\gamma_1 g_{m_1} + \gamma_2 g_{m_2})\,. \tag{2.9}$$

From that the output voltage spectral density can be expressed as

$$V^2_{n_{th},\,out}(f) = 8k_B T(\gamma_1 g_{m_1} + \gamma_2 g_{m_2})\left|\frac{R_{out}}{1 + sR_{out}C_{out}}\right|^2. \tag{2.10}$$

Therefore the rms output voltage noise results to be:

$$\sigma_{V_{n_{th},\,out}} = \sqrt{\int_0^\infty V^2_{n_{th},\,out}(f)\,df} = \sqrt{\frac{2k_B T R_{out}}{C_{out}}(\gamma_1 g_{m_1} + \gamma_2 g_{m_2})}\,. \tag{2.11}$$

By substituting equations (2.7) and (2.11) in (2.6), the final expression for the jitter of a single-ended OTA is derived as:

$$\sigma_t = \frac{1}{V_{IN}}\sqrt{2k_B T R_{out} C_{out}\Big(\frac{\gamma_1}{g_{m_1}} + \frac{\gamma_2 g_{m_2}}{g^2_{m_1}}\Big)}\,. \tag{2.12}$$

The first thing to observe is that, as it happens for the propagation delay, the jitter decreases if a larger overdrive voltage is applied, meant to be the amplitude of the input signal above the threshold level. In addition, this relation shows already some guidelines in designing a low jitter optimized comparator. The jitter performance improves if the input transistor transconductance (g_{m_1}) is maximized: this can be achieved by pushing the transistor to operate in weak inversion but also by increasing the biasing current, entailing obviously a penalty in the power consumption. In the opposite way, a decrease of g_{m_2} is desirable. However, it is important to highlight that in this simplified analysis the input capacitance, which affects the slope of the output signal, is omitted. For this reason, increasing excessively the width of the differential pair, to move it into deep weak inversion, can be counter-productive. Furthermore, the parasitic capacitance should be minimized as well as the output resistance, paying attention to not lower the gain below the specification.

This jitter model can be tailed for different schematics, as it will be shown in the next section, and can provide interesting indications in the design phase. The model is, however, based on several simplifications, such as a single pole system or the dominance of thermal noise. As soon as some of these hypotheses are dropped, the analysis gets immediately very complicated. Moreover, as already highlighted in the discussion about the propagation delay, the comparator is likely working in a region of operation incompatible with the small signal equivalent circuit, and this is the main limitation in developing an exhaustive mathematical model of the jitter.

2.2 Design challenges

Table 2.1: Discriminator specifications.

Static gain	$> 50\,\mathrm{dB}$
Jitter at $10\,\mathrm{ke}^-$	$\ll 30\,\mathrm{ps}$ rms
Threshold dispersion (without DAC)	$< 5\,\mathrm{mV}$ rms
Maximum current consumption	$\sim 5\,\mu\mathrm{A}$
Area	$< 10\%$ of pixel size
Radiation hardness	Yes
Technology	CMOS 28 nm - 9 metals
Supply voltage	900 mV

Table 2.1 reports the targeted specification of the discriminator. The static gain is required to have a minimum resolution of around 1.5 mV, calculated from

equation (2.1) assuming V_{OH} and V_{OL} respectively equivalent to 75% and 25% of the supply voltage. An increase of the gain has likely a cost in terms of power consumption or speed and, therefore, jitter.

Regarding the time resolution, to reach the system goal of 30 ps rms, the comparator should be designed to have a jitter well below this value. This because it must be considered that discriminator jitter has to be quadratically added to the jitter components originating from the CSA, the digital pixel and from the sensor itself.

Threshold dispersion represents the uncertainty on the firing point of the comparator: it means that the discriminator switches when the input signal is in the neighbourhood of the nominal threshold value. This phenomenon is caused by transistor mismatch in differential pairs and current mirrors and impacts differently each pixel of the chip. It can be simulated by means of a statistical analysis, such as Monte Carlo simulation. As stated above, the front end system includes a DAC with the purpose of equalizing the threshold of the entire pixel matrix. Even if, in principle, whatever offset spread can be corrected using a DAC, the required number of bits and therefore the area depend on the threshold dispersion value. For this reason, transistor mismatch must be kept in any case as low as possible: it can be mitigated during the design and layout phases and, in general, it is minimized by increasing the area of critical transistors.

For what concerns power consumption and area, the specifications for the discriminator are generic because they are strongly dependent on the integration of this component in the whole system. Indeed, the design of other blocks and other choices that must be made at high level, such as power density and pixel pitch, play a role in the definition of these requirements. Considering, for example, a power budget of $1\,\mathrm{W\,cm^{-2}}$ and assuming that the power is distributed equally between the analog and the digital part of the pixel, the maximum analog current consumption is 16.8 µA for 55 µm pixel pitch and 9.8 µA for 42 µm pixel pitch. This current has to be allocated to CSA, comparator and tuning DAC. 5 µA of maximum current consumption is then a reasonable value set to compare different comparator topology. Concerning the area, around 10% of the pixel surface will be reserved for the discriminator.

2.2.1 Radiation hardness

The Velopix2 final application will be LHC-related and hence the pixel comparator needs to be radiation hardened; that is probably the main challenge to be faced in the design but also what makes chips developed at CERN unique. Both neutral and charged incident particles can affect the performances of CMOS technology-based devices, and the entity of the damages is strongly related to different factors such as impinging energy, impinging mass, but also impinged mass and material

density. There are several ways to categorize radiation effects; one is for example to distinguish between single event and cumulative effects. Single event effects are caused by ionizing particles which, generating electron-hole pairs in the substrate, can introduce current spikes in certain nodes of the circuit: this particularly affects DC-DC converters and digital blocks, since the radiation may cause glitches, memory failures and clock disruptions [26]. Regarding cumulative effects, two subgroups can be identified: displacement damage and Total Ionizing Dose (TID). Displacement damage is related to the formation of traps and vacancies in a crystalline lattice, but the technology used in this work results to be almost insensitive to this effect. TID is instead related to the accumulation of positive charges in the oxides of CMOS such as gate oxide, spacers and Shallow Trench Isolation (STI), used to separate contiguous devices. This accumulation causes transistor threshold voltage variations, an increase of the leakage current in nMOS and a decrease of the ON current in pMOS. It is worth noting that TID effects have dependencies on width and length of the transistors but also that they are related to the CMOS process technology employed. The effects of the ultra-high TID expected to be reached in the HL-LHC upgrade have been extensively studied for the 28 nm CMOS technology adopted by CERN [27]. Constraints in choosing the dimensions of single transistors were identified to limit the radiation-related degradation: the minimum width allowed is 800 nm while the length should not exceed 250 nm. In the cases where longer devices are advantageous, for instance in improving the matching of current mirrors, several transistors are stacked one over the other with the gates connected together (Appendix A). Nevertheless, this technique entails a small penalty in terms of area, because of the devices physical separation, and parasitics because of the additional interconnects required.

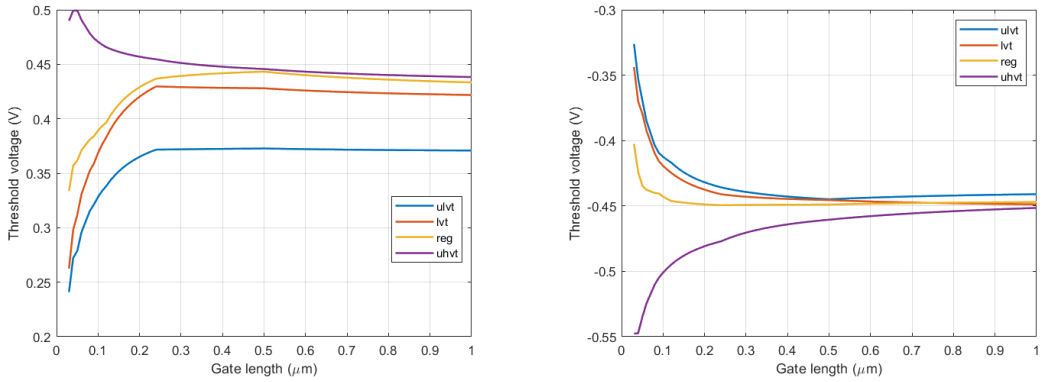
2.2.2 CMOS 28nm bulk technology

The latest integrated circuits developed at CERN and installed in its facilities were designed in 130 nm and 65 nm. In 2020, an important research and development programme was launched to think and realize the infrastructures for the future upgrades of the LHC: one of the work packages, WP5, has been focused on selecting the new CMOS technology for ASIC development and in designing IP blocks in the selected process [28]. There are two main reasons for which CERN microelectronics development should follow the downscaling of CMOS processes: the first is to ensure that the in-use technology will be available and supported in the long term by foundries, which tend to dismiss older processes gradually; the second is to exploit the advantages of miniaturized transistors such as higher speed, lower power and smaller area. The 28 nm technology is the last bulk CMOS node before moving to advanced processes such as Fully Depleted Silicon On Insulator (FD-SOI) and FinFET. It was selected as the technology for the next generation of ASIC at

CERN primarily for its good performances in terms of radiation tolerance and for its contained production and design costs.

While in digital design, the benefits of speed, power consumption and area are undeniable and evident, in analog design, the new technology brings several challenges in the development of IP blocks. For example, the intrinsic gain of transistors results to be quite limited, forcing the designer to introduce gain boosting technique in the schematics. The low supply voltage (900 mV) makes difficult to stack several transistors operating in saturation and forces to design MOSFETs working in weak or moderate inversion. In addition, in the layout phase, it is possible to draw the polysilicon only in the vertical direction. This has two consequences: the necessity for some IP blocks to have two layout versions, one vertical and one horizontal, to be more flexible; the impossibility of exploiting the enclosed layout transistor [29] to limit radiation-related degradation.

Four different flavours of both p and n-type MOS can be employed in the schematics: ultra-low V_t (ulvt), low V_t (lvt), regular (reg) and ultra-high V_t (uhvt). These flavours were selected after technical discussions based both on implications in analog design and on availability of digital libraries. In figure 2.4 the threshold voltage is plotted as a function of the gate length for the four different transistor flavours. Both n and p-type MOS are considered. As it can be seen, transistors should be designed with a short length ($\ll 400$ nm) to fully benefit of these flavours; that is actually in accordance with the constraints for radiation tolerance.



(a) nMOS. **(b)** pMOS.

Figure 2.4: Threshold voltage variation with gate length.

Chapter 3

Discriminator topology

In this chapter, the topology of discriminator explored and designed are presented. Even though a basic continuous-time comparator can be easily realized as an open-loop OTA without compensation capacitor, the stringent requirements on jitter and power consumption of this application make it necessary to adopt more advanced solution [25]. Furthermore, the literature mainly focuses on synchronous comparators, because they are massively employed in building ADC, while continuous-time comparator are generally used in radiation detectors and time-domain imaging. For this reason, the following topology are originated from discriminators implemented in detectors readout ASICs.

The transistors sizes reported in this chapter result to be the best optimization enabling each topology to fulfill the specifications of table 2.1, keeping all the transistor in the saturation region of operation and ensuring the correct functioning of the comparator also in all the Process, Voltage and Temperature (PVT) corners considered, as it will be better shown in the next chapter. For the topology comparison purpose, the threshold voltage is fixed to be half of the supply voltage (i. e. 450 mV). This value is considered as the common mode input voltage of all the examined discriminators.

Moreover, it must be noted that the following schematics do not show the connection of the bulk since it is assumed that it is connected to the negative rail, in the case of an nMOS, and to the positive rail, in the case of a pMOS.

3.1 CLAMPed folded cascode discriminator (CLAMP)

In figure 3.1 it is illustrated the schematic of the CLAMP with the relative sizing reported in table 3.1. The inversion coefficient is also shown in the table. Based on the value of IC, the transistor region of operation can be defined. If $IC < 0.1$,

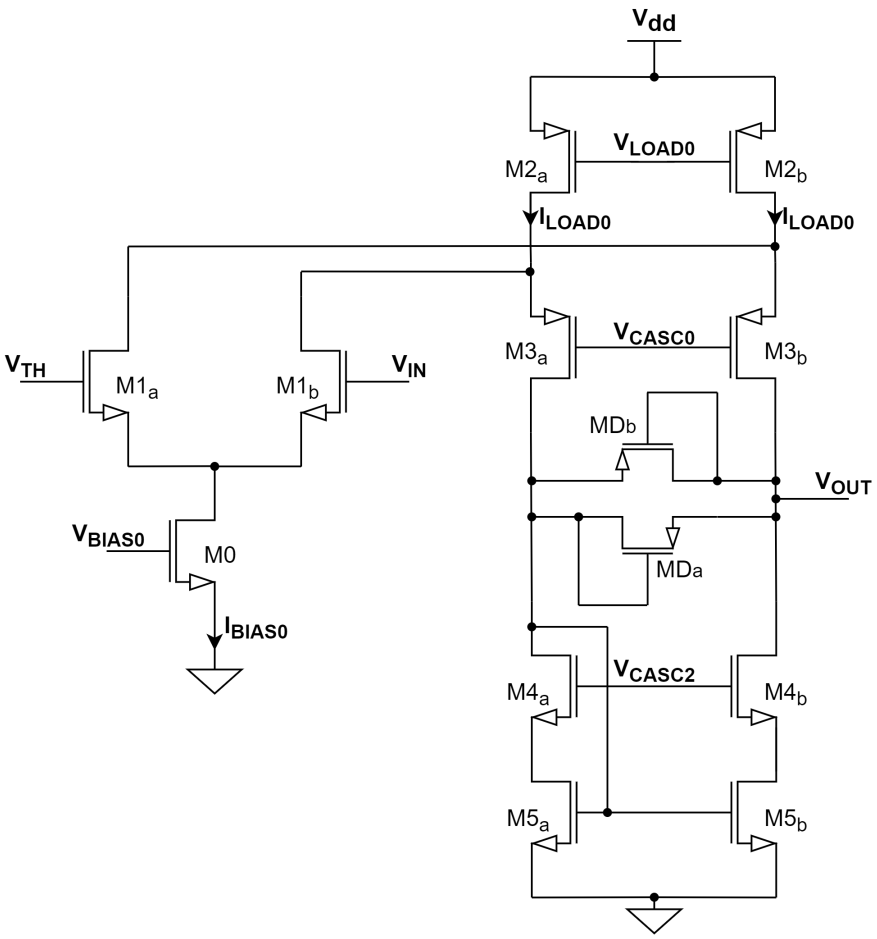


Figure 3.1: Schematic of the clamped folded cascode discriminator.

Table 3.1: Transistor dimensions of the clamped folded cascode discriminator.

	M0	M1	M2	M3	M4	M5	MD
Width (µm)	2	12	2	0.8	0.8	1	1
Length (µm)	1	0.12	1	0.06	0.06	1	0.06
IC	1.67	0.07	2.64	0.43	0.43	2.75	0.22

the transistor is in weak inversion; if $0.1 < IC < 10$, it is in moderate inversion; if $IC > 10$, the transistor is in strong inversion. All the transistors are ulvt flavour, to cope with the low supply voltage, except for $M5$ that are uhvt. In fact, the gate-source voltage of $M5$ must be enough to fit both $M4$ and $M5$ in saturation. I_{LOAD0} is set to 50% of the total current consumption, i. e. 2.5 µA for 5 µA of total current, while I_{BIAS0} is 46% of the current budget. Overall, this comparator will draw a maximum current equal to $2I_{LOAD0}$.

This topology is based on a folded cascode OTA which guarantees a sufficient DC gain, a decent input voltage swing and allows an easier placement of saturated transistors compared to the telescopic version. Still because of the low V_{DD}, a low-voltage cascode current mirror is implemented ($M4-M5$) instead of a standard cascode current mirror at the cost of an addition bias voltage (V_{CASC2}). Furthermore, two diode-connected transistors, MD, are added to limit the output voltage swing and, therefore, to have a faster switching between the two possible states. The tighter the output swing, the faster the discriminator, and the better the jitter is. Nevertheless the signal at V_{OUT} has to be logically interpreted; consequently, this mechanism cannot be pushed too far.

The static gain is

$$\begin{aligned} A_{v0} &= g_{m_1} R_{out} \\ &= g_{m_1} \Big\{ \Big[r_{o_3} + r_{o_1} // r_{o_2} + g_{ms_3} r_{o_3} (r_{o_1} // r_{o_2}) \Big] // \Big(r_{o_4} + r_{o_5} + g_{ms_4} r_{o_4} r_{o_5} \Big) \Big\} \\ &\approx g_{m_1} \Big(g_{ms_3} r_{o_1} r_{o_3} // g_{ms_4} r_{o_4} r_{o_5} \Big) , \end{aligned} \tag{3.1}$$

where g_m is the gate transconductance, g_{ms} is the source transconductance and r_o is the output resistance in saturation of the single transistor (EKV model [30]).

The jitter can be calculated as presented for equation 2.12, assuming the noise contribution of cascode transistors, $M3$ and $M4$, negligible [31]:

$$\sigma_t = \frac{1}{V_{in}} \sqrt{2 k_B T R_{out} C_{out} \Big(\frac{\gamma_1}{g_{m_1}} + \frac{\gamma_2 g_{m_2}}{g_{m_1}^2} + \frac{\gamma_5 g_{m_5}}{g_{m_1}^2} \Big)} . \tag{3.2}$$

The following trade-offs were considered during the design phase of this comparator.

- It is desirable to have the differential pair biased in deep weak inversion to maximize the gate transconductance in order to improve DC gain and jitter, and to enhance the gate-source voltage matching. This is achieved by increasing the aspect ratio of $M1$ transistors. The cost is an increase of both area and input capacitance, that has to be limited to not affect negatively the preceding block.

- Dimensions of MD can be adjusted to reduce their V_{gs} and so the output voltage swing of the discriminator. However, the correct functioning of the comparator must be preserved in all the simulated PVT corners, meaning that the output signal has to be digitally reconstructable in all condition, as already stated above.

- $M5$ transistors should be pushed in strong inversion to improve the current matching of the low-voltage current mirror, but this means a large saturation voltage that is not compatible with the low voltage supply of this technology. Furthermore, the accuracy of the current mirror improves with the length of $M5$ (channel length modulation effect [25]). Nevertheless, this has a negative effect on the jitter because parasitic capacitances are increased. The same is true for $M0$ and $M2$ to get an accurate current from the biasing DAC.

- Cascode transistors, $M3$ and $M4$, are fundamental to boost the gain and to suppress the Miller multiplication effect. They are designed small to limit the parasitic output capacitance, while ensuring that all the devices in the stack, $M2$, $M3$, $M4$ and $M5$, operate in saturation.

3.1.1 Layout

Table 3.2: Transistor dimensions of clamped folded cascode discriminator (new). Updates highlighted in bold.

	M0	M1	M2	M3	M4	M5	MD
Width (µm)	2	**24**	2	**1.2**	0.8	1	1
Length (µm)	1	**0.06**	1	**0.12**	0.06	1	0.06

The layout of the CLAMP topology is presented in figure 3.2. The total area is 6.46 µm × 7.72 µm. To integrate this discriminator in the complete front end, some small modifications to the sizing were necessary, since the operating value of the threshold voltage turned out to be 350 mV. The new dimensions are reported in table 3.2; thus, it is ensured that transistors operate in saturation and that the specifications are fulfilled, even with a lower common mode input voltage.

Good matching between transistors is required for some analog structures, such as differential pairs and current mirrors, so that they can operate correctly. Therefore, the layout is developed by placing the devices in a symmetrical configuration and following the general rule of fingers interdigitization [31]. Also, dummy transistors are added to keep the same environment for the fingers at the periphery. By doing so, linear variations due to process, stress and temperature gradients are minimized.

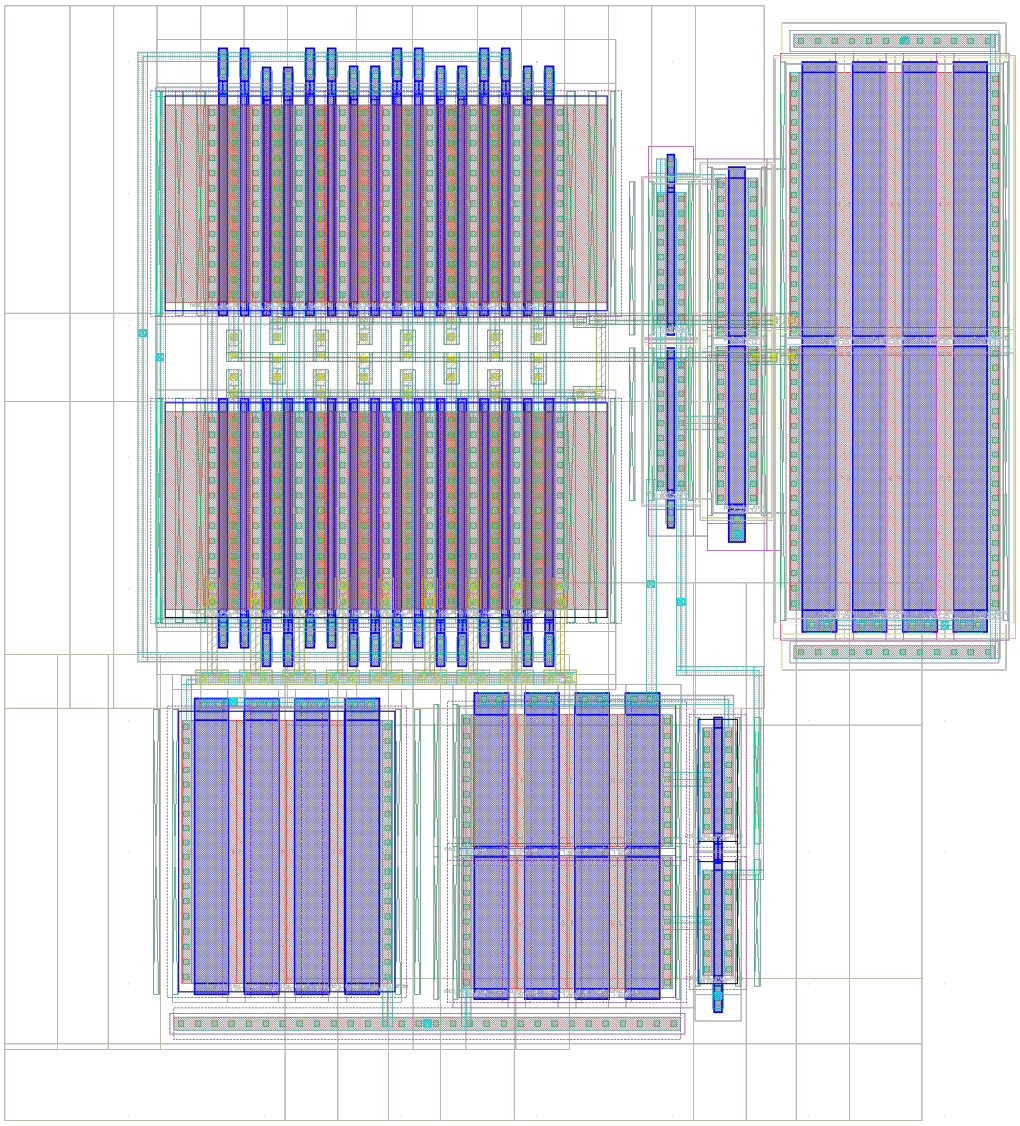


Figure 3.2: Layout of clamped folded cascode discriminator (6.46 µm × 7.72 µm).

Regarding the interconnections, only the first three metal layers are employed; the width of metal lines is at least 50% larger than the minimum allowed and multiple vias are used to minimize the parasitic resistances. It is important to recall that the polysilicon gate layer can be drawn only vertically.

In addition, it is worth highlighting that a triple-well process is used for nMOS transistors. As depicted in figure 3.3, this technique implies the fabrication of a nMOS, not directly in the p-type substrate, but in a p-well surrounded by an n-well, called deep n-well. The triple-well structure is exploited to avoid the coupling with the significant substrate noise generated by the switching of the digital logic.

Lastly, it must be noted that this preliminary layout was developed mainly to evaluate the impact of the parasitic resistances and capacitances on the comparator performances, above all on the jitter. The final layout of the discriminator will be realized simultaneously with the other blocks of the analog front end, in order to further optimize the area, that is a critical aspect of the pixel development.

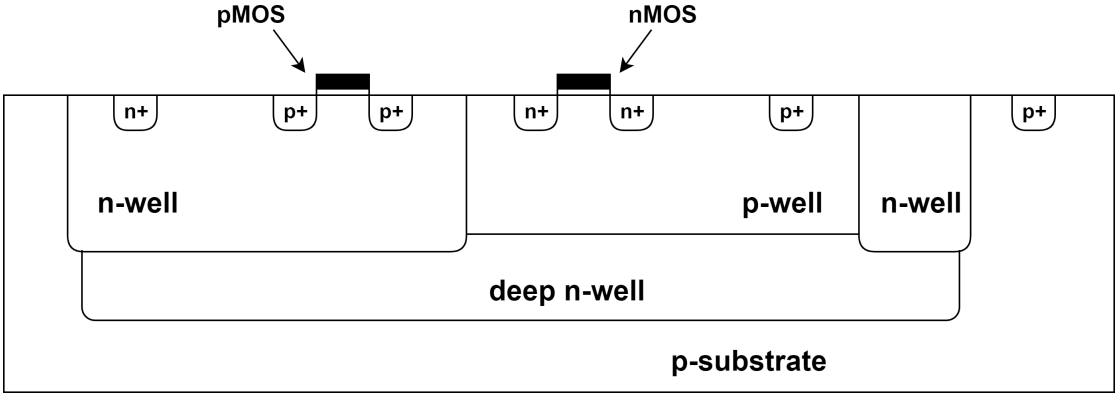


Figure 3.3: Triple-well structure.

3.2 CURRent based discriminator (CURR)

Table 3.3: Transistor dimensions of current based discriminator.

	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
Width (µm)	2	12	2	0.8	0.8	1	0.8	3	3	1	1
Length (µm)	1	0.12	4	0.06	0.06	1	0.2	0.2	0.06	0.08	2
IC	0.69	0.06	2.44	0.32	0.33	1.67	1.39	0.29	0.20	0.11	4.37

The schematic of the CURR is depicted in figure 3.4; this topology is derived from the analog front end of other chips of the Medipix family [3]. The sizing

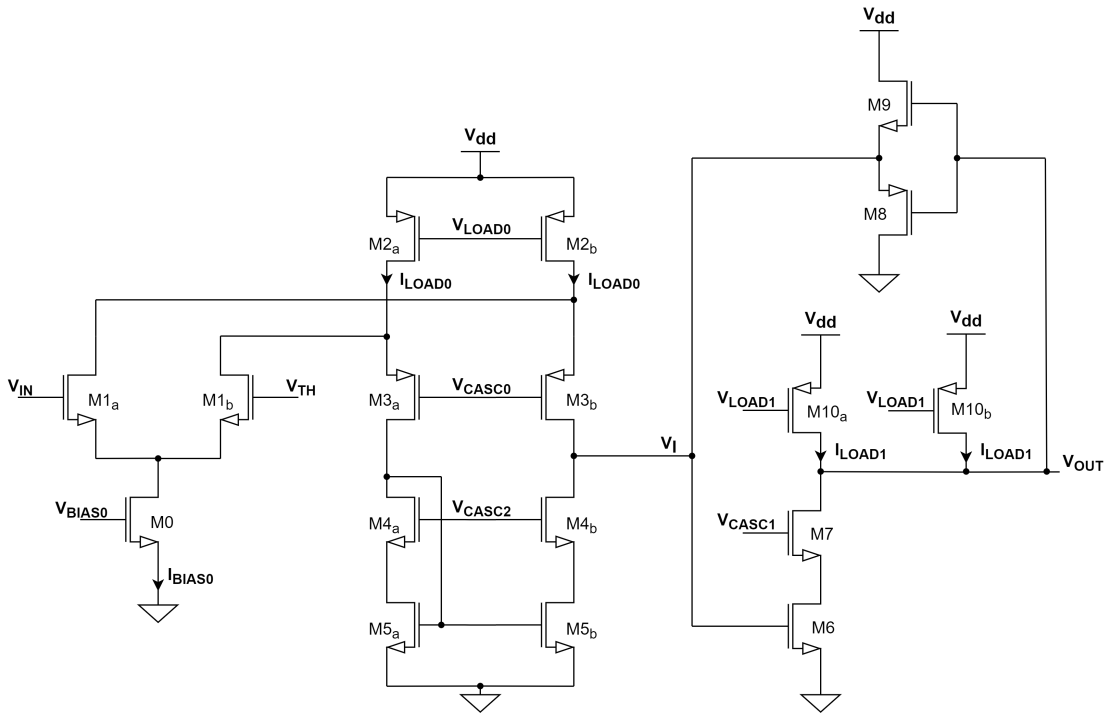


Figure 3.4: Schematic of current based discriminator.

is shown in table 3.3. $M5$ and $M6$ are uhvt, $M9$ is standard while all the other transistors are ulvt flavour. With respect to the total current budget, I_{BIAS0} is set at 16% while I_{LOAD0} and I_{LOAD1} at 22% each.

This discriminator is again based on a folded cascode OTA, here followed by a second stage ($M6$ - $M10$) that is a high speed current comparator [32]. A cascoded common source amplifying stage has replaced the CMOS inverter originally presented in [32] for two reasons: the necessity to control precisely the current flowing in the comparator and the will to improve the decoupling with the power supply. The feedback introduced by $M8$ and $M9$ allows fast switching between the two possible output states.

The principle of operation is now briefly described. At the equilibrium, for $V_{IN} = V_{TH}$, the current flowing in $M5_a$ and $M5_b$ is the same and corresponds to $I_{LOAD0} - {}^{I_{BIAS0}}/_2$; in this state, the feedback network is off and V_{OUT} matches V_I. If, for instance, the input voltage is above the threshold ($V_{IN} > V_{TH}$), then $I(M1_a)$ is larger than $I(M1_b)$. Consequently, the current in $M3_b$ is smaller than the one in $M3_a$. The latter is mirrored by $M4$ and $M5$, generating a current unbalance at the node V_I, with $I(M5_b) > I(M3_b)$. This excess current is drawn from $M9$, causing the rise of V_{OUT} to $V_I + V_{gs}(M9)$. On the other hand, when the input voltage is below the threshold, an excess current is injected in $M8$ making the output voltage fall to $V_I - V_{gs}(M8)$.

A mathematical formulation of the jitter is not straightforward because of the feedback network. However, it can be approximated to (3.2), assuming that the noise arising from the second stage can be neglected and, therefore, the first stage is dominating in the jitter calculation. Equation (3.3) shows the output thermal noise as the sum of the contribution from the first and the second amplifying stages:

$$\sigma_{V_{n_{th},\,out}} = \sigma_{V_{n_{th},\,I}} A_{v0_I}^2 + \sigma_{V_{n_{th},\,II}} \,. \tag{3.3}$$

Regarding the design of this discriminator, some of the trade-offs identified are similar to those described for the CLAMP topology. A compromise between jitter performance, mismatch, area and input capacitance is found in sizing $M1$. Dimensions of $M0$, $M2$, $M10$ and in particular $M5$ are set in order to optimize jitter, area and mismatch. In addition to that, it is important to match the voltage at node V_I with the voltage at the drain of $M4_a$ to have a well-behaving current mirror. This can be done by adjusting the sizing or changing the flavour of $M6$, which fixes the voltage V_I given the I_{LOAD1} current. It must be taken into account also that, to have a fast current comparison, the capacitive load of the first amplifying stage has to be kept low. $M6$, $M8$ and $M9$ should be as small as possible to reduce parasitic capacitances. $M8$ and $M9$ are also significant because, as stated above, they set the lower and the upper value of the output voltage, which must be fed to the digital pixel.

3.2.1 Layout

The layout of this topology view is shown in figure 3.5. The total area is 11.98 µm × 7.26 µm, as expected larger than the CLAMP but still within the specifications. The same guidelines, already described for the layout of the CLAMP, are followed. Also in this case some small adjustment to the transistors sizing were necessary and the updated dimensions are reported in table 3.4.

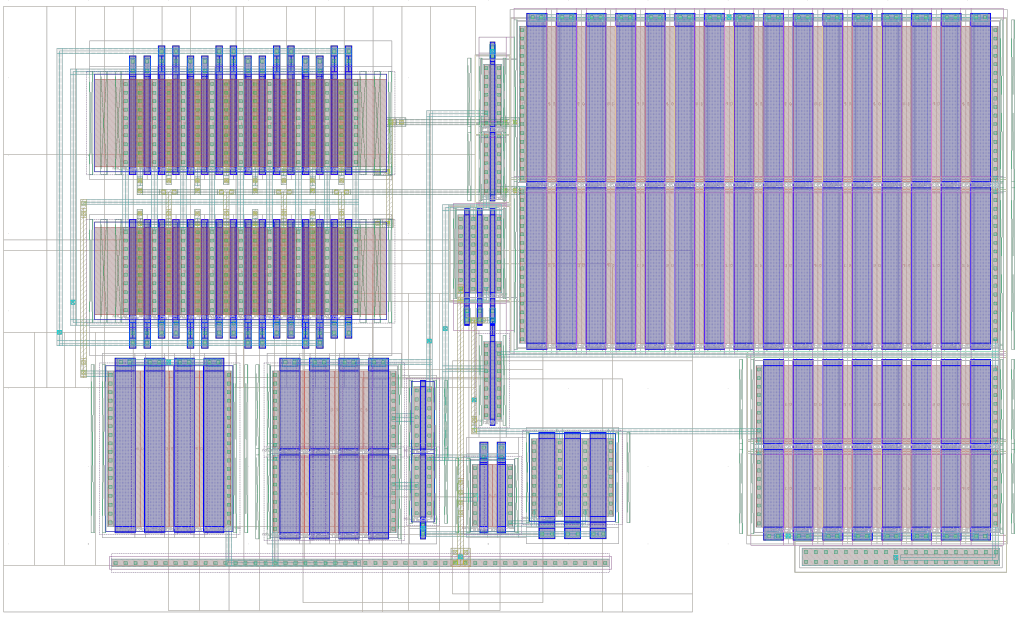


Figure 3.5: Layout of current based discriminator (11.98 µm × 7.26 µm).

Table 3.4: Transistor dimensions of current based discriminator (new). Updates highlighted in bold.

	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10
Width (µm)	2	**18**	2	0.8	0.8	1	0.8	3	3	1	1
Length (µm)	1	**0.08**	4	0.06	0.06	1	0.2	0.2	0.06	0.08	2

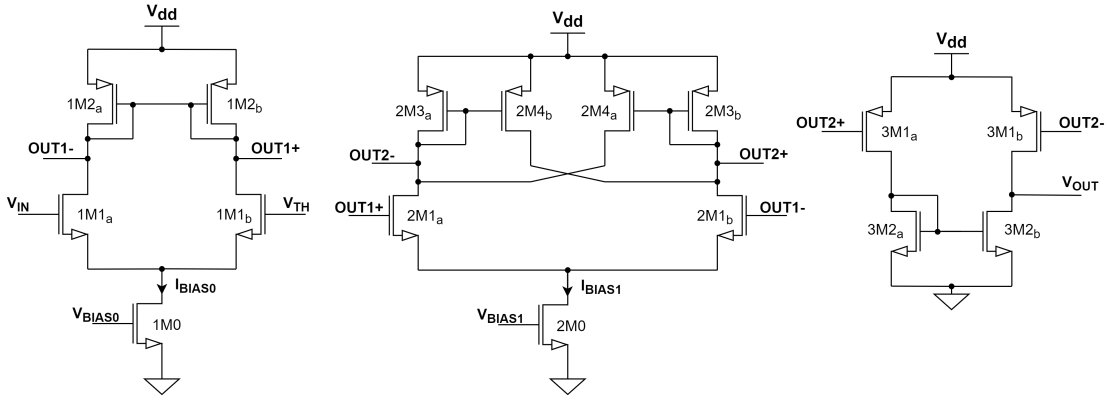


Figure 3.6: Schematic of cross-coupled positive feedback discriminator.

Table 3.5: Transistor dimensions of cross-coupled positive feedback discriminator.

	1M0	1M1	1M2	2M0	2M1	2M3	2M4	3M1	3M2
Width (µm)	2	12	1	2	3	1	1	1	1
Length (µm)	1	0.12	0.75	1	0.12	0.44	0.38	0.3	0.16
IC	1.27	0.07	1.53	1.28	0.11	0.33	0.33	0.33	0.28

3.3 CROSS-Coupled positive feedback discriminator (CROSSC)

The CROSSC topology, shown in figure 3.6, is derived from the discriminator implemented for the Dosepix ASIC [33], a chip developed at CERN for active personal dosimetry. The idea is to introduce a positive feedback amplifying stage, an OTA with cross-coupled loads ($2M0$ - $2M4$), to speed up the comparator flipping. A first very low gain stage ($1M0$ - $1M2$) is added to permit the local tuning of the threshold voltage. The last stage converts the differential output of the cross-coupled cell into a digital-interpretable signal. The transistors sizing is reported in table 3.5. Only the ulvt transistor flavour is employed in this design. I_{BIAS0} and I_{BIAS1} are both set to 34% of the total current budget.

The mathematical formula of the jitter is very hard to derive for such a positive feedback multi-pole system. However, a jitter-mismatch trade-off is spotted for $2M3$ and $2M4$: the larger these transistors are, the better the matching is. On the other hand if $2M3$ and $2M4$ are designed smaller, the jitter improves. The aspect ratio of $2M4$ is greater than the one of $2M3$ to introduce the internal positive feedback, as it will be described in the following subsection (3.3.1). Moreover, transistors $3M1$ are sized to control the maximum current in the last stage, since they mirror the current flowing in $2M3$.

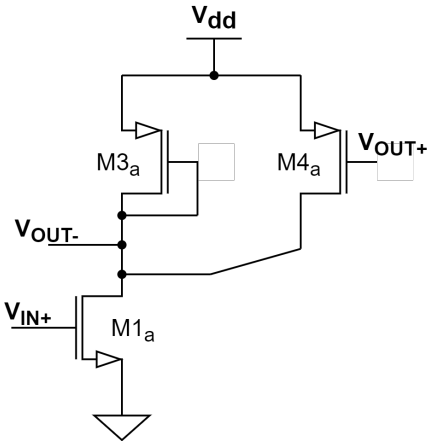
Related to this, one drawback of this topology is the large variation of the current flowing in it, depending on the state in which the discriminator is. In fact, if the input voltage is below the threshold ($V_{IN} < V_{TH}$), the output level is low and the branch $3M1_b$ - $3M2_b$ is off. On the contrary, for an input above the threshold ($V_{IN} > V_{TH}$), the output voltage is high, thus the current flowing in the last stage is doubled. Such fluctuation in the supply current should be limited to avoid disruptions in the pixel matrix due to coupling.

3.3.1 Cross-coupled loads OTA

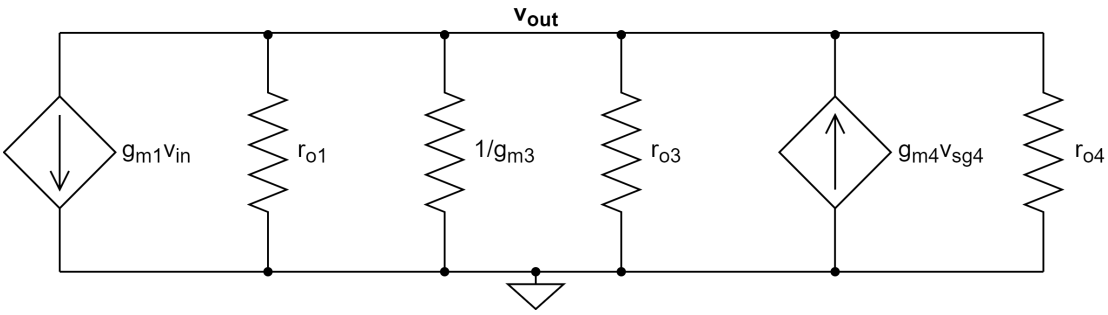
The small signal equivalent circuit for half of the OTA with cross-coupled load is depicted in figure 3.7b, where a pure differential input signal is considered. The signal v_{out} is referred to the node V_{OUT-} in figure 3.7a. v_{sg4} is then equal to $-v_{out}$ because voltages at nodes V_{OUT-} and V_{OUT+} swing in opposite directions by the same amount for a pure differential input. Therefore, the gain v_{out}/v_{in} is easily calculated as follows:

$$A_{v0} = -g_{m_1}\left[r_{o_1} // r_{o_3} // r_{o_4} // \frac{1}{g_{m_3}} // \left(-\frac{1}{g_{m_4}}\right)\right]. \tag{3.4}$$

From this, three possible cases can be distinguished depending on the sizing of transistors $M3$ and $M4$.



(a) Half circuit schematic.



(b) Small signal equivalent circuit.

Figure 3.7: Small signal model of cross-coupled OTA (half circuit).

- If $M3$ and $M4$ are exactly congruent, their transconductances are the same and their contribution cancels each other. Hence equation (3.4) becomes $A_{v0} = -g_{m_1}(r_{o_1}//r_{o_3}//r_{o_4})$. In this case, the cross-coupled OTA has a quite high gain which is comparable to the one of a single ended OTA. Nevertheless this configuration is too sensitive to mismatch, since a slight difference in $M3$ and $M4$ dimensions results in a significant gain drop.

- In the case where the aspect ratio of $M4$ is greater than the one of $M3$, g_{m_4} is larger than g_{m_3}. Therefore (3.4) is reduced to $A_{v0} \approx {}^{g_{m_1}}/_{g_{m_4}}$. Internal positive feedback is introduced in the cell; this is the mechanism exploited above in 3.3.

- The last possibility is to design $\left(\frac{W}{L}\right)_3$ greater than $\left(\frac{W}{L}\right)_4$. As a consequence $M3$ transconductance is larger than $M4$ transconductance and (3.4) can be approximated to $A_{v0} \approx -{}^{g_{m_1}}/_{g_{m_3}}$. This configuration is employed as an amplifying stage without hysteresis in the topology presented in the next section.

3.4 MULTI-low-gain-stage discriminator (MULTI)

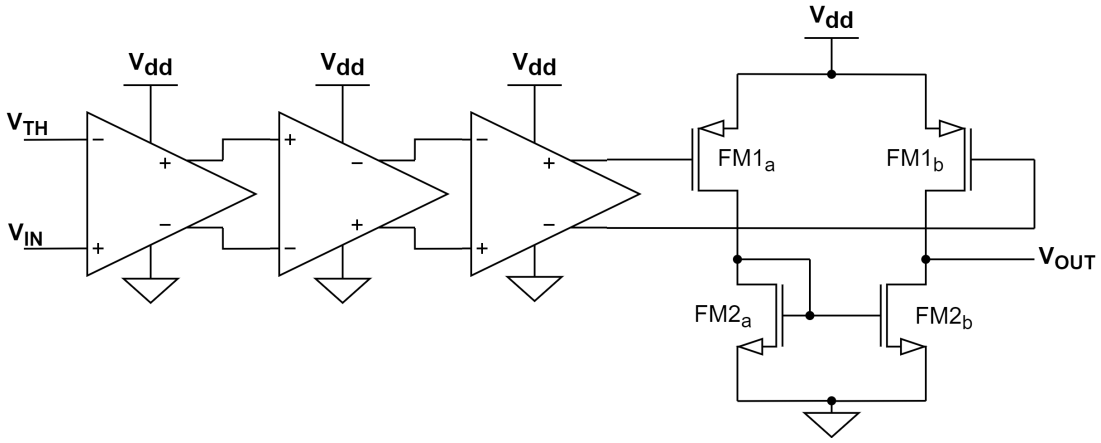


Figure 3.8: Schematic of multi-low-gain-stage discriminator.

Figure 3.8 shows the concept of the MULTI topology. A sequence of low gain differential amplifiers is followed by a final stage, which performs the conversion from differential to single-ended signal. The idea is to build up the required total gain by cascading several low gain and large bandwidth OTA [25]. Large bandwidth means small time constant and this benefits the discriminator in terms of speed, and therefore jitter. In fact, assuming n equal stages cascaded, the overall propagation

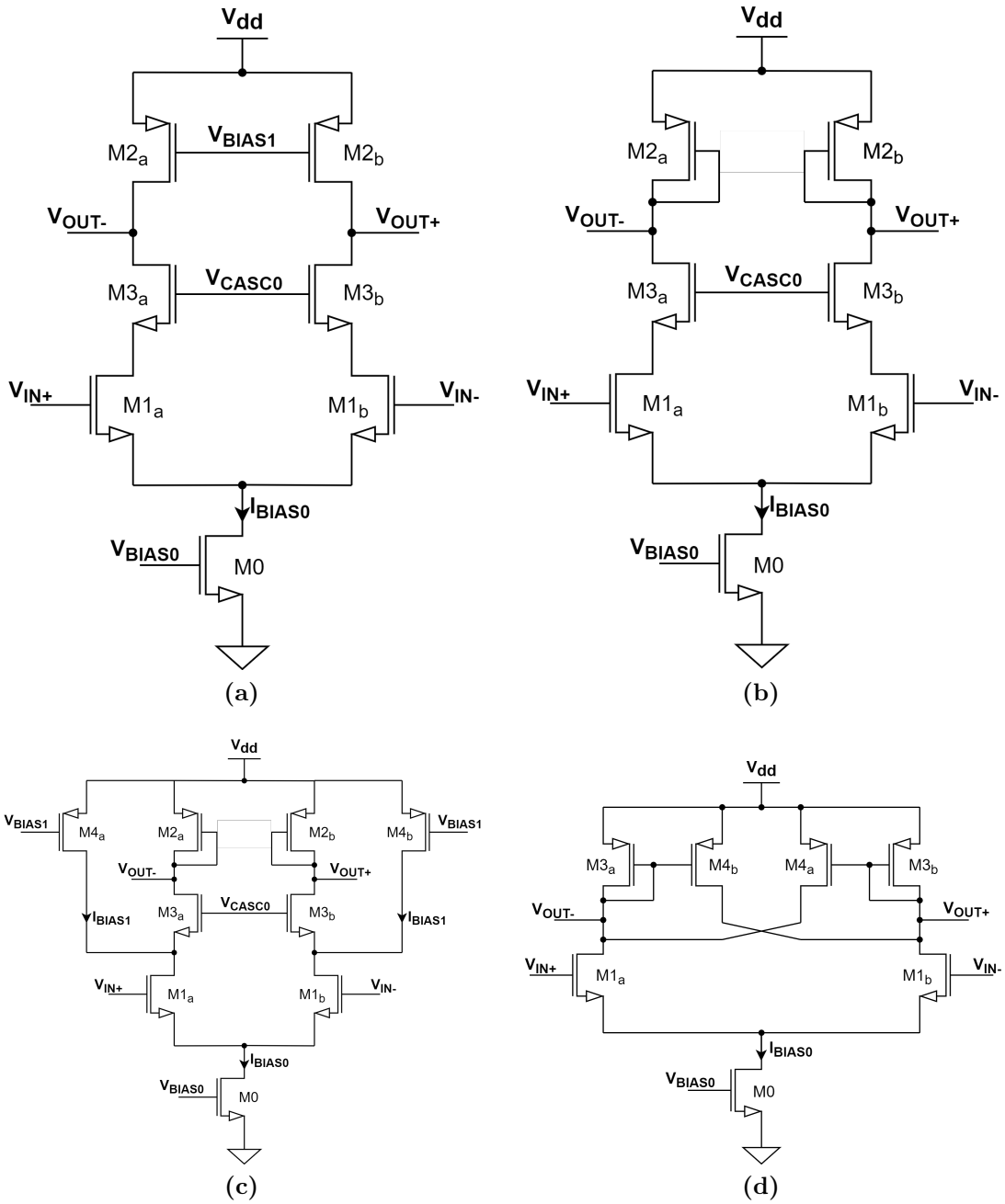


Figure 3.9: Topology options for fully differential OTA.

delay can be approximated as

$$t_p \approx \sqrt{\sum_{i=1}^{n} \tau_{p_i}^2}\,. \tag{3.5}$$

This topology gives the designer several degrees of freedom in developing an optimized comparator. For example, it can be chosen the number of differential amplifiers to place (the three shown in figure 3.8 are only illustrative), but also how to implement these cells and how to distribute the current among the different stages.

Recalling that the minimum required discriminator gain is $50\,\mathrm{dB} \approx 316\,\mathrm{V\,V^{-1}}$, from [34] the optimal number of stages is determined to be 5. By referring to [25] instead, this value is calculated to be 11. The second analysis, however, does not take into account any limit on power dissipation. In general, because of the strict constraints on power consumption and area, a maximum of 5 differential cells is considered.

Concerning the single stage implementation, figure 3.9 gives an overview of the options that can be employed. The first possibility (figure 3.9a) is a basic fully differential OTA, with an external bias for the active loads $M2$. Even though it allows to have a sufficient DC gain, this topology suffers from a high mismatch due to the two current mirror setting the same: any small discrepancy between the two biasing voltages V_{BIAS0} and V_{BIAS1} will push either $M0$ or $M2$ in triode region and cause a drop in OTA performances. The problem could be addressed by implementing a common mode feedback network which would require additional area and power. This solution is therefore not compatible with the target application. The second option, in figure 3.9b, employs two diode-connected transistors ($M2$) as active loads. The static gain is $A_{v0} = -{}^{g_{m_1}}\!/_{g_{m_2}}$. Because of the technology and the low supply voltage, the transistors mainly operate in moderate and weak inversion; hence it is not possible to achieve the required gain. A solution is shown in figure 3.9c: two current sources ($M4$) are used to "starve" the loads ($M2$), so that the current flowing in them is smaller with respect to the one flowing in the differential pair ($M1$). In this way the gain can be controlled by tuning the I_{BIAS1} current. The same strategy is adopted in the last option (figure 3.9d), where the cross-coupled branches $M4$ act as internal starving current sources. Here the aspect ratio of transistors $M3$ is greater than the one of transistors $M4$ to have an amplifying stage without positive feedback, as already described in subsection 3.3.1.

Table 3.6 shows the sizing of the discriminator using the basic cell in figure 3.9c. Table 3.7 refers instead to a comparator built with the differential OTA in figure 3.9d. All the transistors considered are ulvt flavour. The current is equally distributed in each stage and depends obviously on the number of stages placed.

Table 3.6: Transistor dimensions of multi-low-gain-stage discriminator c.

	First stage					Inner stage (if any)				Final stage	
	M0	M1	M2	M3	M4	M0	M1	M2	M4	FM1	FM2
Width (µm)	2	12	0.8	1	0.8	2	3	0.8	0.8	0.8	0.8
Length (µm)	1	0.12	0.4	0.06	0.4	1	0.12	0.4	0.4	0.2	0.2
IC (3 stages)	1.4	0.07	0.29	0.23	0.58	1.4	0.12	0.3	0.58	0.32	0.35

Table 3.7: Transistor dimensions of multi-low-gain-stage discriminator d.

	First stage				Inner stage (if any)				Final stage	
	M0	M1	M3	M4	M0	M1	M3	M4	FM1	FM2
Width (µm)	2	12	1	1	2	3	1	1	1	1
Length (µm)	1	0.12	0.38	0.44	1	0.12	0.38	0.44	0.3	0.16
IC (3 stages)	1.27	0.09	0.33	0.33	1.27	0.11	0.33	0.33	0.33	0.32

The total gain for a discriminator with n stages is

$$A_{v0_{tot}} = \prod_{i=1}^{n} A_{v0_i} \,. \tag{3.6}$$

The output thermal noise is dominated by the first stages of the chain because their contribution must be multiplied by the squared gain of the following stages (equation (3.7)).

$$\sigma_{V_{n_{th},\,out}} = \sum_{i=1}^{n} \sigma_{V_{n_{th},\,i}} \, \frac{A_{v0_{tot}}^2}{\prod_{k=1}^{i} A_{v0_k}^2} \,. \tag{3.7}$$

Regarding the threshold dispersion effect, the mismatch is dominated by the input differential pair. This explains why the differential pairs ($M1$) of the inner stages can be made smaller. The advantage is a reduced capacitance load to the preceding stage. Moreover, the cascode transistor $M3$ in the inner stages of MULTIc can be removed because Miller effect is not relevant.

In both the configurations, two diode-connected transistors (not shown in the schematic) are inserted between the two branches of the differential pair to limit the maximum voltage swing and, consequently, to improve the switching speed of the comparator [25]. The mechanism was already explained in section 3.1.

This topology has the same drawback of the CROSSC concerning the large variation of the supply current. Another negative aspect is that the "starving" currents, that are used to boost the gain of the cells, reduce the slew rate and, therefore, the speed and the jitter of the discriminator for large input signals.

Chapter 4

Simulation results

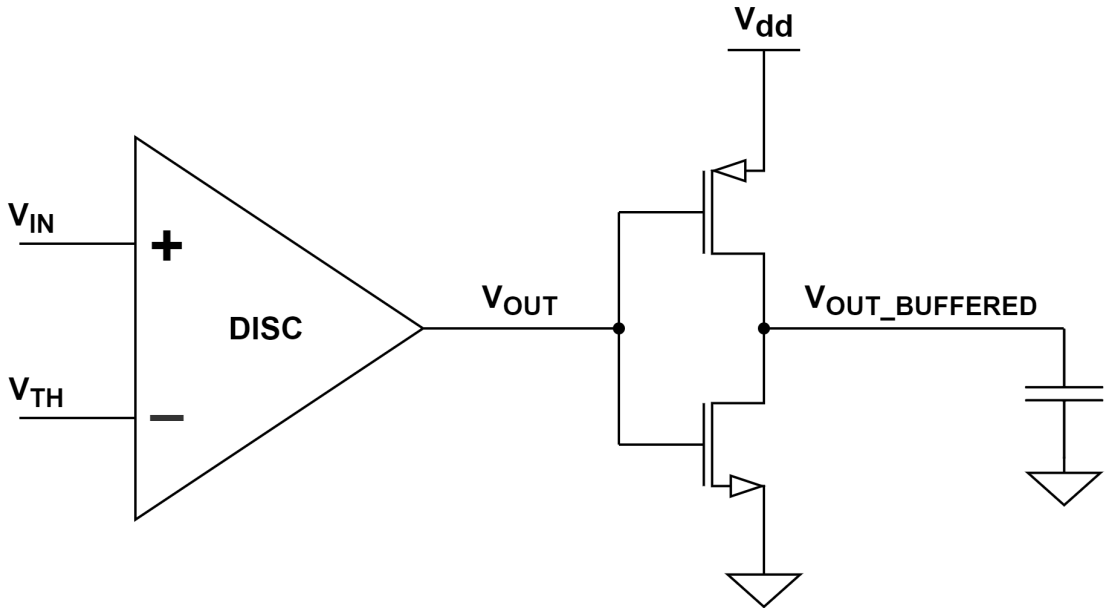


Figure 4.1: Simulation setup.

In this chapter, the simulation results for the topology described above are presented. The simulation setup is shown in figure 4.1. The discriminator under test is followed by a standard library inverter. This allows to have a load capacitance that mirrors the one in the pixel implementation, where a logic gate will come after the comparator. Also, looking at the output voltage of the inverter enables to check if the discriminator delivers a digitally reconstructable signal. The DAC exploited to correct the pixel-to-pixel mismatch is not included and it must be considered that it may impact the discriminator performance.

The threshold voltage is fixed at 450 mV. The input signal in the transient simulation, performed to measure the jitter, is an ideal step voltage. The baseline of this signal is 420 mV, with the amplitude varying from 50 mV to 430 mV. The comparator input voltage amplitude can be linked to the input charge, considering that the CSA gain is 40 mV/ke$^-$. For the DC sweep simulation, the input voltage ranges from 0 V to V_{DD}.

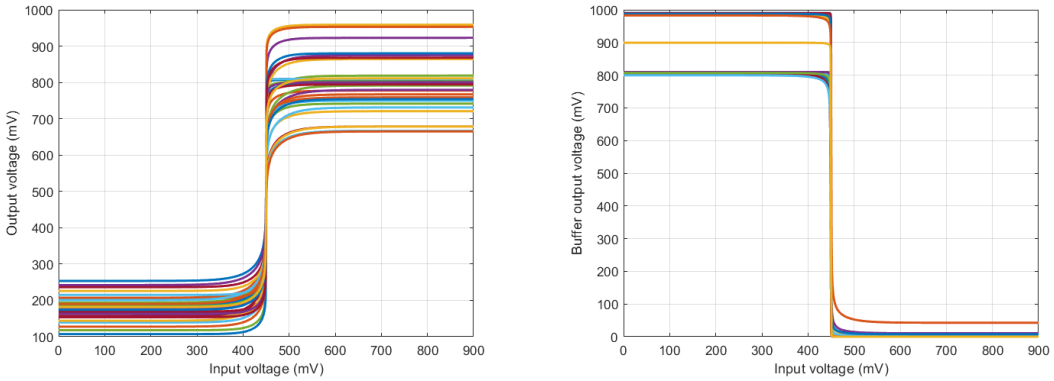
4.1 PVT corners and mismatch simulations

Corners simulation is the technique used in ASIC design to model the extreme cases of variation of fabrication parameters, supply voltage and temperature. Because of fabrication inaccuracy, some process-dependent parameters such as oxide thickness, diffusion depths, dopant concentrations and transistor dimensions may vary. Consequently, carrier mobility, threshold voltage and other metrics can deviate from their predicted values and the transistors can behave differently compared to the ideal case. Moreover, supply voltage fluctuations, caused for instance by the parasitics of the interconnects, affect the functioning of the design. Lastly, the chip temperature also impacts the circuit performances. A total of 45 corners are taken into account, as a result of the combination of the following:

- 5 process corners for active components. These are typical-typical, fast-fast, slow-slow, fast-slow, slow-fast, where the first term corresponds to nMOS and the second one to pMOS.
- A deviation of ±10% of the supply voltage (0.81 V, 0.9 V and 0.99 V).
- 3 temperature cases, −40 °C, 25 °C and 80 °C.

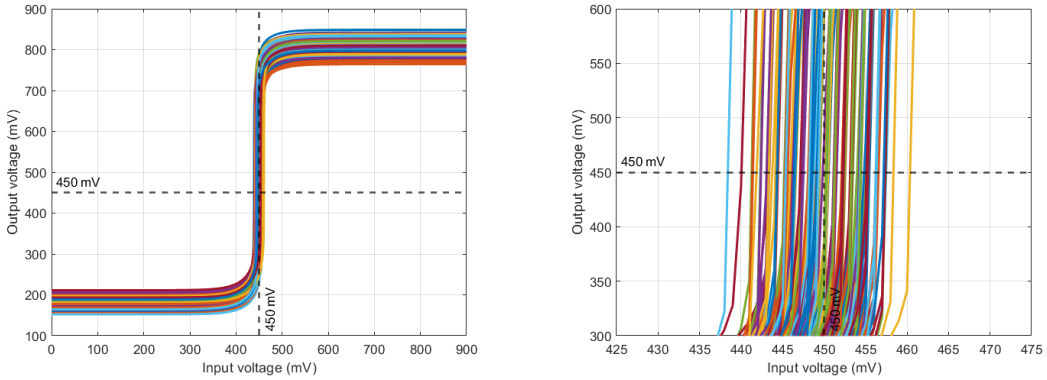
All the topology presented operate properly for the PVT corners considered. Figure 4.2 shows the DC sweep simulation results for the CURR discriminator. The comparator output is displayed in 4.2a, while the inverted signal is depicted in 4.2b. This confirms that the discriminator delivers a logically interpretable voltage to the digital pixel in all the extreme conditions simulated.

While corner simulations can be very pessimistic (or optimistic), because they cover only extreme cases, a Monte Carlo analysis allows to consider a statistical distribution of the fabrication-dependent parameters. At each run, the simulation is performed with parameters calculated randomly according to a statistical distribution model. Monte Carlo analysis is here exploited to verify how the mismatch affects the discriminator performance, in particular to estimate the value of the threshold dispersion. Figure 4.3 shows the comparator output of the CURR topology in response to a DC input sweep; 400 iterations are performed to get significant results.



(a) Discriminator output. **(b)** Buffer output.

Figure 4.2: PVT corners DC sweep simulation (CURR).



(a) Discriminator output. **(b)** Detail of threshold dispersion.

Figure 4.3: Monte Carlo DC sweep simulation (CURR).

In figure 4.3b threshold dispersion can be observed clearly. Ideally, the discriminator output crosses half of the supply voltage when the input signal corresponds to the nominal threshold value, i. e. 450 mV ($V_{OUT} = V_{DD}/2$, when $V_{IN} = V_{TH}$). Because of mismatch, the comparator fires for input voltages slightly smaller or larger than the expected. Figure 4.4 shows the threshold voltage distribution, obtained by looking at the input voltage value corresponding to $V_{OUT} = 450$ mV. Threshold dispersion coincides with the standard deviation of this Gaussian distribution.

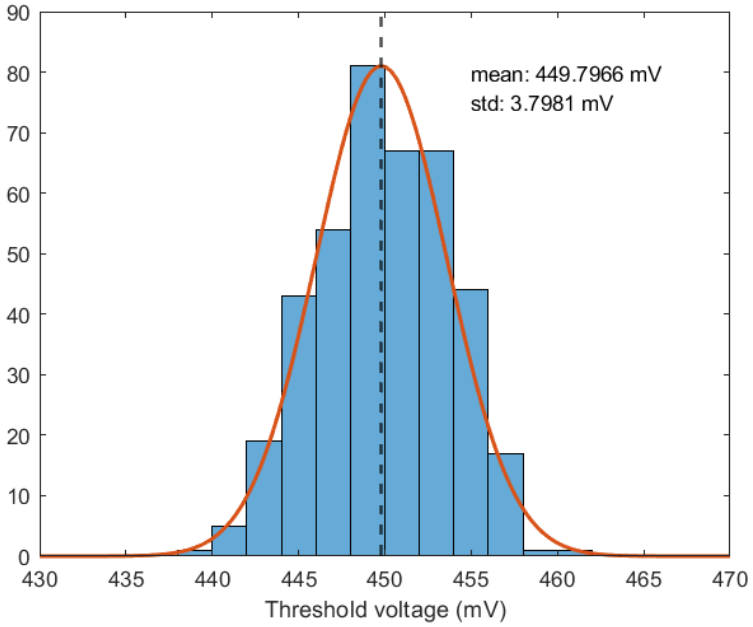


Figure 4.4: Threshold voltage distribution (CURR).

4.2 Topology comparison

Jitter is simulated through a transient noise analysis; 100 iterations are performed to have meaningful results. It is worth saying that transient noise simulation are very demanding in terms of time and computing resources. As an example, figure 4.5 reports the CURR discriminator output as a function of time for an input charge of 10 ke$^-$. Jitter is defined as the standard deviation of the time at which the signal crosses 450 mV.

Figure 4.6 compares the jitter performance for the MULTI discriminator (section 3.4). A number of stages varying from 2 to 5 for both the two possible differential cell is considered. The first thing worth to notice is that the MULTId topology has a lower jitter with respect to the MULTIc, considering the same

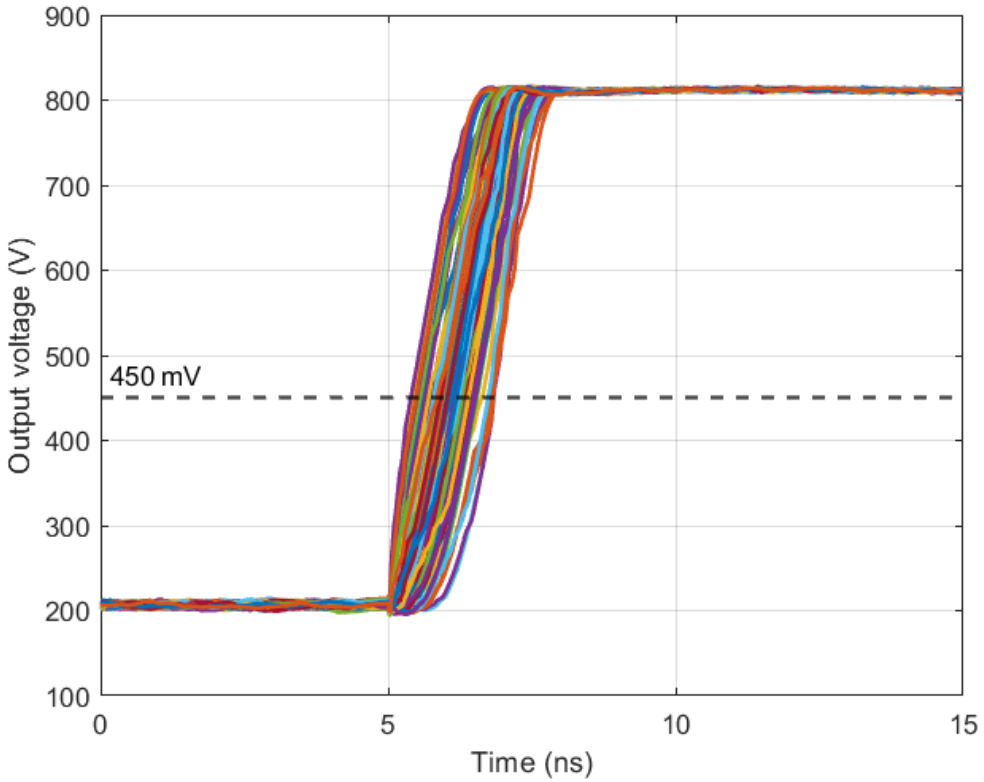


Figure 4.5: Jitter simulation output voltage at 10 ke$^-$ (CURR).

number of stages. Moreover, it is clear that the less the stages are, the better the jitter is. Therefore, it seems that the comparator does not take advantage of a larger bandwidth. This is probably due to the fact that, at the input voltage considered, the comparator is already slewing. If this assumption is true, then the jitter degradation is justified by the worsening of the slew rate, because the same amount of current is distributed to an increasing number of stages.

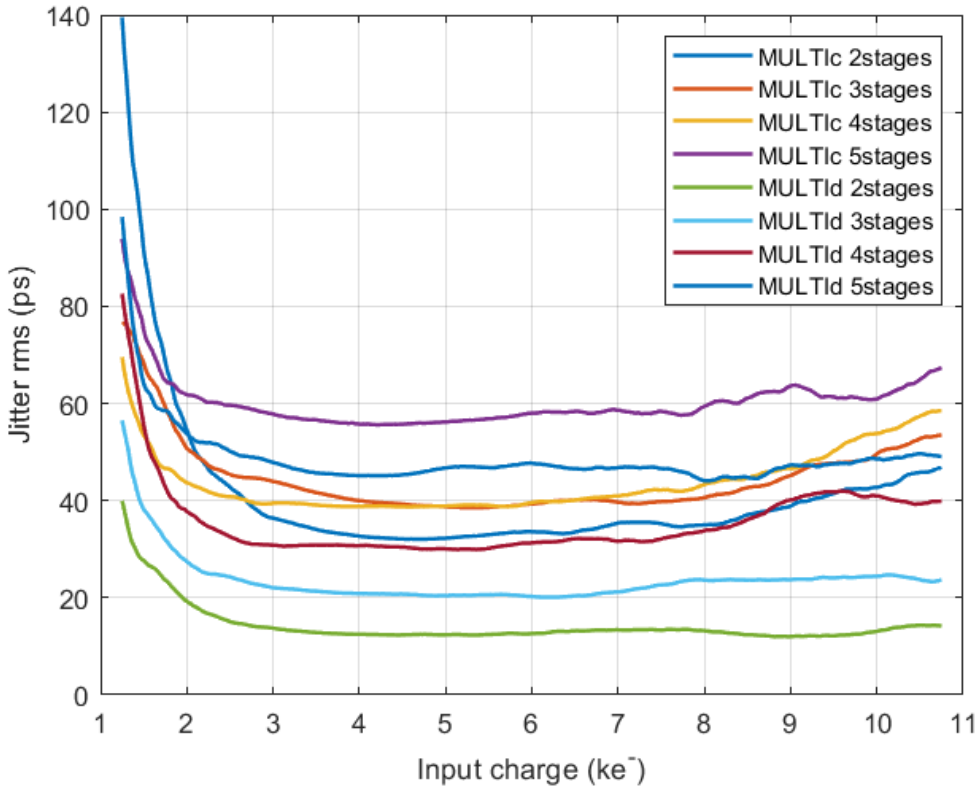
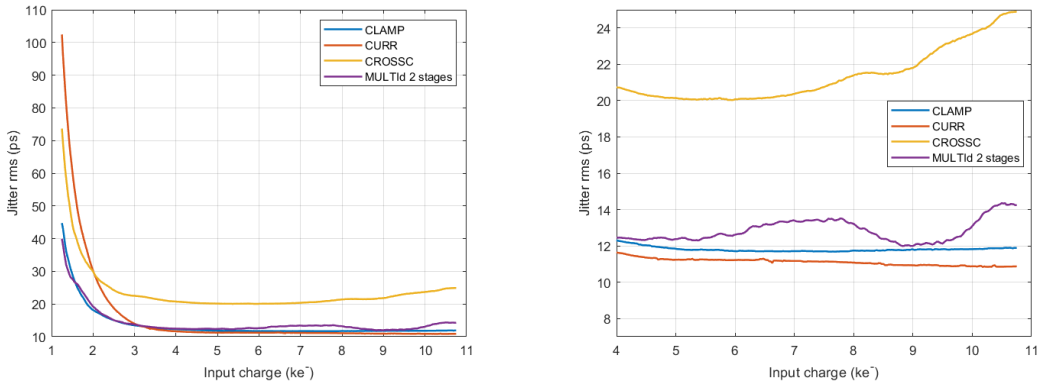


Figure 4.6: Jitter comparison for MULTI topology.

The comparison in terms of jitter between the four main discriminator topology explored in this work is shown in figure 4.7. From figure 4.7a it is possible to observe that CLAMP and MULTId 2 stages are the best for a low input charge. This is not a result of great interest since the target jitter of 30 ps is for an input charge of 10 ke^- and in most of the cases the input charge will be comparable to this value. At 10 ke^-, the CURR comparator results to be the best topology, with a jitter of 10.202 ps. It is not trivial to explain the behaviour of the CROSSC and MULTId 2 stages curves for high input charges. The unexpected increase of the jitter for high input charge can be due to the ideal step voltage input.

Figure 4.8 shows the supply current flowing in each topology of discriminator as



(a) Overview. **(b)** Detail for large input charge.

Figure 4.7: Jitter comparison.

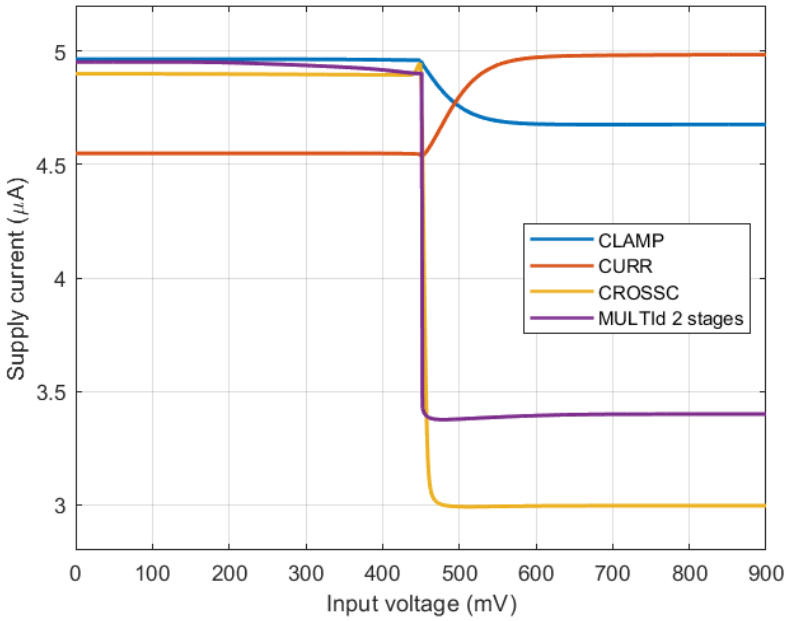


Figure 4.8: DC sweep current comparison.

a function of the input voltage. Current variation is defined as the difference of the currents in the two possible states, input low or input high. A lower fluctuation in the supply current is preferable to avoid coupling with other pixels through the power supply distribution network. Table 4.1 compares the four topology for threshold dispersion and current variation. All the mismatch values are within the

specification and therefore it will be possible to equalize all the pixel thresholds thanks to the 5 bits tuning DAC.

Table 4.1: Topology comparison.

	CLAMP	CURR	CROSSC	MULTId 2 stages
Threshold dispersion (mV)	3.445	3.798	4.385	3.164
Current variation (µA)	0.288	0.434	1.552	1.903

4.3 Power sweep

In chapter 2 it was already highlighted that timing jitter improves if more power is delivered to the discriminator. This has been verified by sweeping on the current supplied to the comparator. In figure 4.9, discriminator jitter is plotted as a function of the current consumption for the CURR topology, with the input charge fixed at 10 ke^-. The trend reflects the expectations: the larger is the comparator power consumption, the better is the jitter performance. This occurs even if the schematic is designed to operate with 5 µA and it may need further adjustments to be fully optimized for different values of supply current.

Nevertheless, it is important to manage the power distribution at pixel level in order to get similar contributions of the jitter from all the components, that have to be quadratically added together. If, for instance, the jitter arising from the discriminator is much smaller than the one due to the CSA, then the latter component is dominant and the over-optimized comparator is not crucial in achieving a good time resolution.

4.4 Post-layout simulations

Parasitic resistances and capacitances are extracted from the layout developed for the CLAMP and CURR topology. Post-layout simulations of jitter, together with schematic simulations, are depicted in figure 4.10, for the CLAMP discriminator, and in figure 4.11, for the CURR discriminator. For 10 ke^- input charge, in the first case, the performance is deteriorated by 43.9%; in the second case post-layout jitter is 37.8% worst with respect to the schematic.

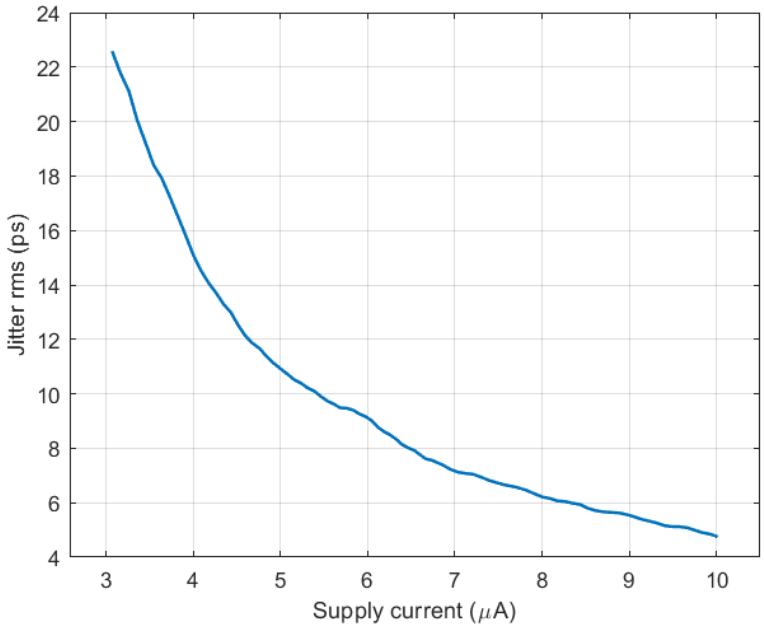


Figure 4.9: Jitter vs supply current for 10 ke$^-$ input (CURR).

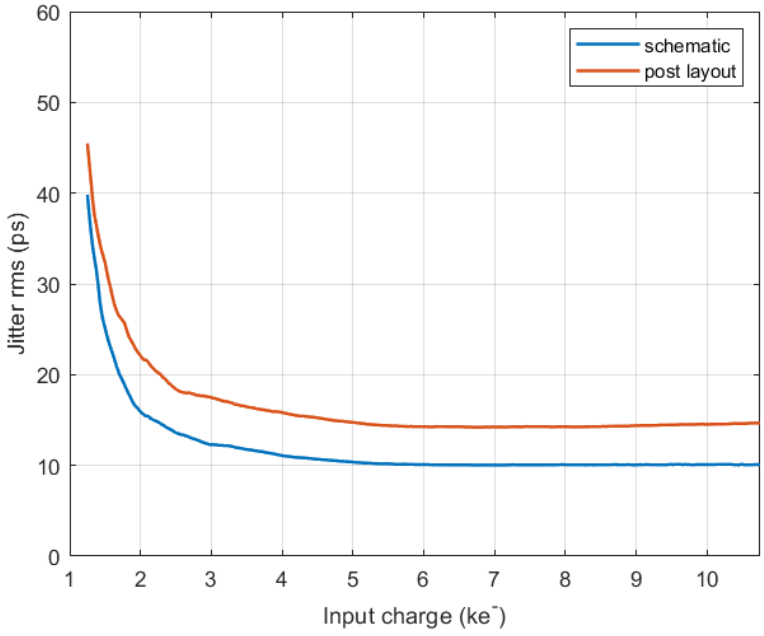


Figure 4.10: Post-layout simulation (CLAMP).

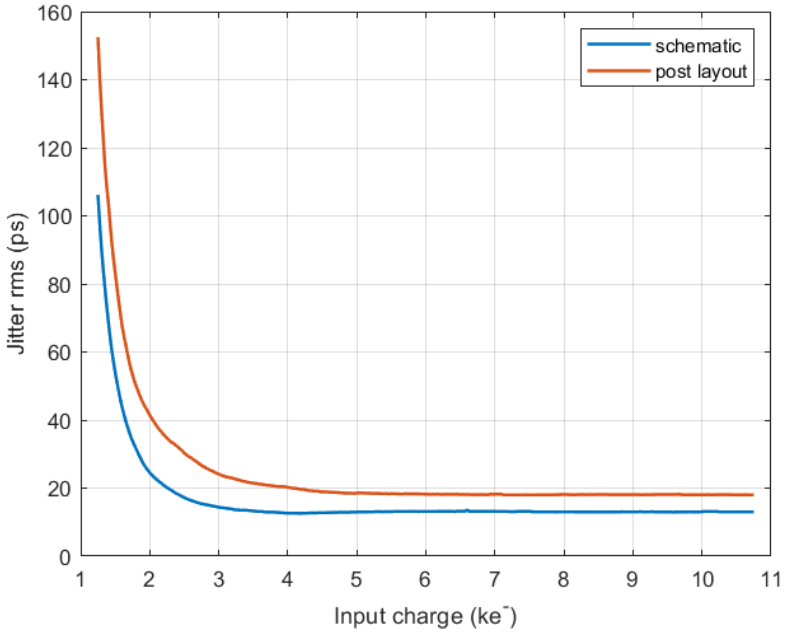
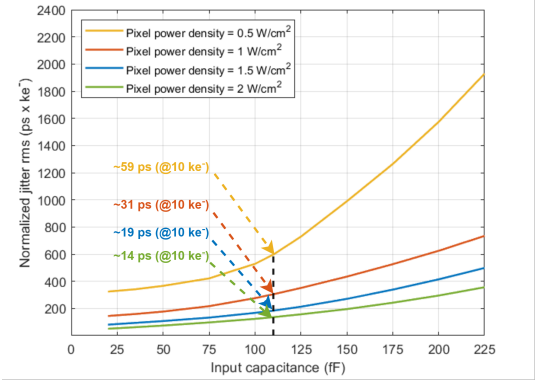


Figure 4.11: Post-layout simulation (CURR).

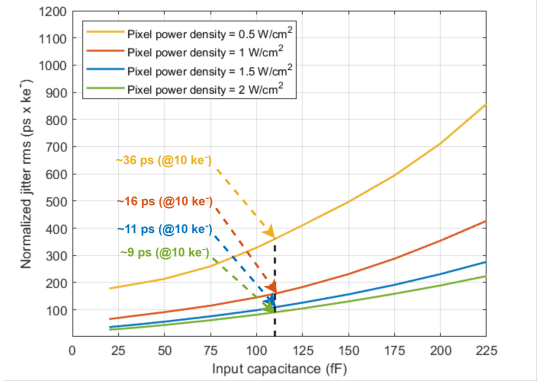
4.5 Integration with CSA

Figure 4.12 shows the jitter simulation of the CSA followed by the CURR discriminator. For both the blocks the schematic views are considered; the tuning DAC is still not taken into account. Figure 4.12a refers to a pixel pitch of 42 µm while figure 4.12b refers to a pixel pitch of 55 µm. Four pixel power density are considered: 0.5 W cm^{-2} and 1 W cm^{-2} for which active cooling is not necessary, 1.5 W cm^{-2} and 2 W cm^{-2} that require implementing an active heat dissipation system. It is assumed that the power is equally divided to the analog and the digital pixel. The current is then distributed between the CSA and the comparator in such a way the jitter components of the two blocks match. The input capacitance reported on the x axis is mainly dominated by the sensor capacitance, which is for example 110 fF for a 3D-trench sensor [35]; the jitter normalized with respect to the input charge is represented on the y axis. On both the plots, the values for the jitter related to an input charge of 10 ke$^-$, for an input capacitance of 110 fF, are highlighted.

As it is displayed in the figures, considering a pixel pitch of 55 µm, a pixel power density of 1 W cm^{-2} could be enough to reach the objective of 30 ps rms jitter. On the other hand, in the case of a 42 µm pixel pitch, it is necessary to add an active cooling system to achieve the expected time resolution. Anyway, it must be also considered that the performances will degrade of about 40% when post-layout simulations will be performed. This leads to think that a pixel pitch of 55 µm would be preferable to cope with the strict time resolution goal.



(a) 42 µm pixel pitch.



(b) 55 µm pixel pitch.

Figure 4.12: Jitter at the output of CSA and discriminator chain versus the input capacitance.

Chapter 5

Conclusion

CERN upgrades continuously the electronic systems of LHC and its experiments to increase the number of collisions, their energy and the amount of data collected. The detectors placed closer to the collision sites, called trackers, are usually based on hybrid pixel detectors, which have the sensor matrix and the readout ASIC manufactured separately. A new demonstrator chip for the LHCb VELO, PicoPix, is under development to reach a time resolution below 30 ps for an input charge above 10 ke^-. One of the key factors to design such a fast and precise ASIC is the employment of a 28 nm CMOS technology, which is gradually replacing older nodes (130 nm and 65 nm) in the high energy physics community. The new CMOS technology is particularly interesting because it showed encouraging results regarding the performances degradation due to the LHC radiation levels.

Each electronic pixel has an analog and a digital circuitry. In the analog part, the charge deposited on the sensor is amplified and transformed in a logic signal. In the digital side, TOA, TOT and number of hitting particles are measured. The link between the analog and the digital pixel is represented by a continuous-time discriminator. This block compares the signal generated by the CSA with a reference voltage set above the intrinsic electronic noise in order to have noise hit-free measurements.

In this work, four different discriminator topology, derived from existing readout ASIC, were designed and optimized to achieve the best performance in terms of jitter with constraints on power consumption, area and threshold dispersion. The development of these circuits was complicated by the difficulty in modelling mathematically the jitter, because of the non-linear comparator behaviour, and by the low voltage supply of the 28 nm technology.

Simulations showed that all the discriminators were designed to deliver a binary signal, correctly interpreted by an inverter, in the PVT corners considered (process variations, $\pm 10\%$ of V_{DD}, three environmental temperatures). A Monte Carlo analysis was also performed to evaluate the threshold dispersion phenomenon, due

to transistors mismatch. Mismatch must be kept below certain values to limit the area of the tuning DAC employed in correcting the threshold fluctuation along the pixel matrix.

The different topology were compared for jitter at the same power consumption; the best discriminator, at $10\,\mathrm{ke}^-$, resulted to be the one composed by a folded cascode OTA followed by a current comparator. It was shown also that the jitter improves if the current supplied to the discriminator is increased.

Furthermore, the layout of two comparators were developed. The parasitics effect on jitter were evaluated with post-extraction simulations. A degradation of around 40% of the performance was observed.

Lastly, the most promising discriminator topology (CURR) was simulated together with the CSA, showing that to achieve the desired time resolution it will be probably necessary to adopt the 55 µm pixel pitch instead of the 42 µm one.

Appendix A

Stacked transistors sharing the same gate voltage

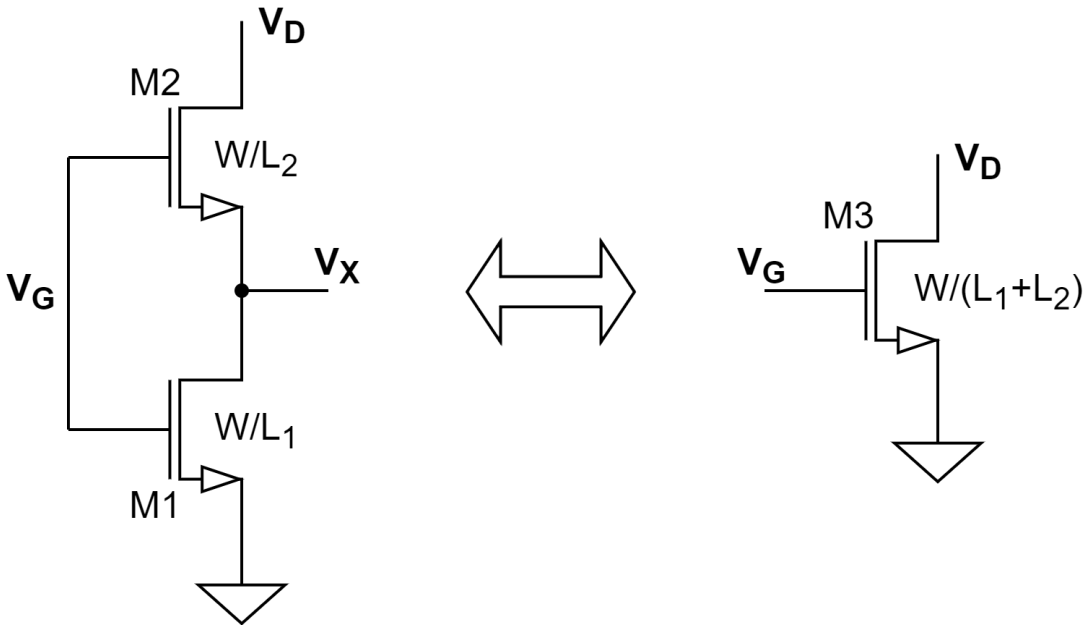


Figure A.1: Representation of the equivalence between two stacked transistors and a single transistor.

When two transistors are stacked one over each other, having lengths L_1 and L_2, identical widths W and sharing a common gate voltage V_G, they are equivalent to a single transistor with the same width W and length $L_1 + L_2$. Figure A.1 gives an image representation of this equivalence. The current flowing through $M1$ and

$M2$ is identical. The equivalence is proved using the EKV model in both weak and strong inversion.

Weak inversion

Let us assume that both $M1$ and $M2$ are in weak inversion. The drain current can be expressed as:

$$I_D = 2n\mu C_{ox}\frac{W}{L}U_T^2\, e^{\frac{V_G-V_T}{nU_T}}\left(e^{-\frac{V_S}{U_T}} - e^{-\frac{V_D}{U_T}}\right). \tag{A.1}$$

The current flowing through the two transistors is then given by:

$$I_{D_1} = 2n\mu C_{ox}\frac{W}{L_1}U_T^2\, e^{\frac{V_G-V_T}{nU_T}}\left(1 - e^{-\frac{V_X}{U_T}}\right), \tag{A.2}$$

$$I_{D_2} = 2n\mu C_{ox}\frac{W}{L_2}U_T^2\, e^{\frac{V_G-V_T}{nU_T}}\left(e^{-\frac{V_X}{U_T}} - e^{-\frac{V_D}{U_T}}\right). \tag{A.3}$$

Considering $I_{D1} = I_{D2}$,

$$\frac{1}{L_1}\left(1 - e^{-\frac{V_X}{U_T}}\right) = \frac{1}{L_2}\left(e^{-\frac{V_X}{U_T}} - e^{-\frac{V_D}{U_T}}\right). \tag{A.4}$$

From this an expression for V_X is gathered:

$$V_X = -U_T \ln\frac{L_1 e^{-\frac{V_D}{U_T}} + L_2}{L_1 + L_2}. \tag{A.5}$$

By substituting equation (A.5) in one of the expressions for the current, (A.2) or (A.3), the following is obtained:

$$I_{D_{1,2,3}} = 2n\mu C_{ox}\frac{W}{L_1 + L_2}U_T^2\, e^{\frac{V_G-V_T}{nU_T}}\left(1 - e^{-\frac{V_D}{U_T}}\right). \tag{A.6}$$

This equation expresses the current going through a transistor in weak inversion with width W, length $L_1 + L_2$, source voltage (V_S) equal to zero, gate voltage V_G and drain voltage V_D.

Strong inversion

Here, transistors $M1$ and $M2$ are assumed to operate in strong inversion. Since they share the same gate voltage, also their pinch-off voltage, $V_P = \frac{V_G-V_T}{n}$, is identical. V_D is considered larger than the pinch-off and therefore $M2$ is saturated.

Supposing $M1$ to be in saturation, V_X is larger than V_P. This implies $M2$ to be turned off, because it has both the source and the drain voltages above the pinch-off. The condition of no current flowing in the two transistors is not acceptable and therefore $M1$ must operate in linear region. Hence,

$$I_{D_1} = \frac{n}{2}\mu C_{ox}\frac{W}{L_1}\Big(\frac{V_G - V_T}{n} - \frac{V_X}{2}\Big)V_X\,, \tag{A.7}$$

$$I_{D_2} = \frac{n}{2}\mu C_{ox}\frac{W}{L_2}\Big(\frac{V_G - V_T}{n} - V_X\Big)^2. \tag{A.8}$$

Considering $I_{D1} = I_{D2}$,

$$\frac{1}{L_1}\left[\Big(\frac{V_G - V_T}{n}\Big)^2 - \Big(\frac{V_G - V_T}{n} - V_X\Big)^2\right] = \frac{1}{L_2}\Big(\frac{V_G - V_T}{n} - V_X\Big)^2. \tag{A.9}$$

Consequently, an expression for V_X is obtained:

$$V_X = \frac{V_G - V_T}{n}\Big(1 - \sqrt{\frac{L_2}{L_1 + L_2}}\Big)\,. \tag{A.10}$$

Replacing equation (A.10) in equation (A.7) or (A.8), the expression for the current becomes:

$$I_{D_{1,2,3}} = \frac{n}{2}\mu C_{ox}\frac{W}{L_1 + L_2}\Big(\frac{V_G - V_T}{n} - V_X\Big)^2. \tag{A.11}$$

Equation (A.11) refers to the current of a MOS biased in strong inversion and operating in saturation, having width W, length $L_1 + L_2$ and gate voltage V_G.

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