Building Blocks for Nanocryotron Logic

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Abstract

Nanocryotrons have emerged in recent years as a candidate for superconducting electronics. Their inherent spiking behavior and robustness against magnetic fields make them suitable devices for implementing reliable low-power systems at cryogenic temperatures. Although some proof-of-concept devices based on nanocryotrons have been demonstrated, the lack of reliable standard cells that combine memory and logic functions has hindered the design of larger circuits.

In this work, a logic family based on this technology is proposed. This family constitutes a complete set of cells that combine sequential and combinatorial functions. In particular, the set of gates and memory cells offers a sound basis for the design of any finite state machine.

All the gates share the same structure, consisting of a superconducting loop, in which the information is stored, and a number of nanocryotrons that can modify the state of the cell. The elementary building block is a destructive readout memory cell, containing two input nanocryotrons, for writing and reading operations. The other devices derive directly from the memory: by adding an input nanocryotron, an OR gate can be made, while swapping the positions of read and write terminals produces inverting logic functions such as NOT and NOR, necessary to create a functionally complete set.

The devices were designed, simulated with SPICE, and fabricated out of a single niobium nitride thin film. All the single-cell circuits were experimentally demonstrated and characterized at 4.2 K, in liquid helium. Moreover, two memory cells have been combined to make an equivalent delay flip-flop. The proper operation of this device shows the possibility of combining multiple cells to make larger systems.

This work paves the way for the design of large-scale systems based on nanocryotrons. Diverse applications may benefit from the development of such systems. The possibility of coupling these devices could make them suitable for integrated control and processing of superconducting nanowire single-photon detectors. Moreover, thanks to their structural and operational robustness, standalone systems based on nanocryotrons can be envisioned as low-power digital technology in harsh environments such as deep space.

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Table of Contents

List of Figures

Acronyms

AWG

arbitrary waveform generator

BER

bit error rate

CMOS

complementary metal-oxide semiconductor

DFF

delay flip-flop

DRO

destructive readout

DUT

device under test

EBL

electron beam lithography

FSM

finite state machine

IPA

isopropanol

JJ

Josephson junction

MOSFET

metal–oxide–semiconductor field-effect transistor

NMP

n-methyl-2-pyrrolidone

PCB

printer circuit board

RF

radio frequency

RIE

reactive ion etching

RSFQ

rapid single flux quantum

SEM

scanning electron microscope

SFQ

single flux quantum

SNSPD

superconducting nanowire single photon detector

SPICE

simulation program with integrated circuit emphasis

SQUID

superconducting quantum interference device

Introduction

Low-temperature electronics are drawing increasing attention. The exotic properties offered by superconducting materials and the low thermal noise environment enable technologies that are not available at room temperature. Single photon detectors [1], quantum computers [2], and extremely low-power digital logics [3] are just examples of the possibilities risen from electronics at cryogenic temperatures.

Although the promising advantages, the scaling up of these systems is hindered. An issue of particular concern is the increasing number of lines that connect the low-temperature environment to the room temperature control electronics. A large number of interconnections between the two systems leads to additional complexity and creates a significant heat load on the cryocooler due to heat conduction [4, 5].

Different strategies have been tried to address this problem, either changing the way of transmitting the information from the device to the room temperature environment, by encoding it in frequency [6] or transmitting the signals through optical fibers [7, 8], or directly integrating part of the electronics at low temperature [5, 9, 10]. The latter approach can also improve the overall speed of the system, avoiding transferring data from outside to inside the cryostat and vice versa.

The electronics at cryogenic temperatures usually employ either complementary metal-oxide-semiconductor (CMOS) technology or Josephson junctions (JJs) as core components. These technologies exhibit different strengths and limits. In particular, CMOS represent the state-of-the-art technology for electronics, but their usage at cryogenic temperatures is limited by the cryostat cooling power, due to the high power consumption [11]. On the other side, JJs exhibit an energetic cost per operation over two orders of magnitude smaller than CMOS [12]. However, the high sensitivity to electrical and magnetic noises can make their integration into superconducting systems challenging [13].

Recently an alternative device, the *nanocryotron*, has been proposed as a candidate for low-power electronics at cryogenic temperatures [14]. The nanocryotron (or nTron) is a three-terminal device composed of a superconducting nanowire (the channel) and a gate terminal. If a bias current is flowing in the nanowire, the channel can be switched to the normal state by injecting a current pulse into the gate terminal. Therefore, the device behaves as a current controllable normally-closed switch. This superconducting component shares some key properties of both CMOS and JJ. It allows driving high impedance loads and operating in ambient magnetic fields, as

CMOS technology, at switching energies closer to Josephson junctions in single flux quantum (SFQ) circuits. Moreover, the nanocryotrons' versatility allows them to be coupled with different technologies. In fact, the possibility of integrating them with superconducting nanowire single-photon detectors (SNSPDs) or interfacing with CMOS and SFQ has already been demonstrated [15].

Despite the nTron attractive properties, this device has never been employed as the core technology of large-scale circuits. Only a few proof-of-concept devices based on nanocryotrons were designed and fabricated [16, 17]. The main obstacle to designing larger circuits is the lack of reliable standard cells that can be employed. This absence forces the designers to adopt an *ad hoc* approach for every new circuit, wasting time and limiting the system to a modest complexity.

The work reported in this thesis proposes a set of building blocks based on nanocryotrons, capable of performing sequential and combinatorial operations. These devices compose a logic family for spiking computing, which can be employed in the design of any finite state machine based on nTrons. Moreover, the blocks can be configured and combined to produce larger circuits.

The thesis will start by introducing the fundamental electronic components employed in the circuits. Afterward, an explanation of the devices' design process will be provided, focusing on the implementation of the elementary cell and the logic gates that can be derived from it. The design description will be followed by an overview of the fabrication processes and the characterization procedures. Then, the experimental results of each circuit will be presented and discussed. Lastly, the figures of merit of the devices, namely the essential features' values to evaluate their performance, will be displayed to determine the possible applications of this set of cells and the potential future work on the technology.

Chapter 1

Technical background

A particular set of materials, when cooled down under a certain temperature T_C (known as *critical temperature*), exhibit peculiar properties. Among the most interesting of these properties are the vanishing of the electrical resistance [18] and the expulsion of magnetic fields [19]. Materials that behave according to these physical effects are called superconductors.

These phenomena are caused by the formation of Cooper pairs in the material. These couples of electrons attracted by electron-phonon interaction act as bosonic charge carriers, which flow without electrical resistance and thus a related ohmic loss. This quantum effect was first explained in 1957 by Bardeen, Cooper, and Schrieffe [20].

The application of a strong enough magnetic field (greater than the *critical field*) will cause the superconductivity in the material to break. The same effect can be obtained by applying a current through the superconductor. If the current density inside the material exceeds its relative critical current density J_C, that portion of the superconductor turns to the normal (resistive) state [21]. The portion of the material that no longer superconducts is called *hotspot*. As will be clearer later, the generation and evolution of these hotspots play a crucial role in the operation of devices based on superconducting nanowires.

The unique characteristics of superconductivity make it interesting for several electronic applications, ranging from high-resolution sensors, such as superconducting nanowire single-photon detectors (SNSPDs) [1] or superconducting quantum interference devices (SQUIDs) for magnetometry [22]., to quantum computers [2]. Superconducting devices exploit different physical properties compared to traditional room-temperature electronics, thus offering the designers novel tools [23]. These devices can give substantial advantages to superconducting electronics, for instance in terms of speed or power consumption, which is drastically reduced by the absence of ohmic losses related to the conduction in superconductors [24].

To describe the standard cells proposed in this work, it is necessary to introduce the main electrical components that are used in the circuits. Precisely, the following

description will include kinetic inductors, superconducting nanowires, nanocryotrons, and superconducting loops.

1.1 Kinetic inductance

The inductance of each conductor is composed of two terms: a magnetic and a kinetic one. These two contributions arise from different physical effects. In particular, the first one is related to the energy storage in the magnetic field induced by the current. In contrast, the other refers to the kinetic energy of the charge carriers.

Room-temperature electronics make use of magnetic inductance. One example is solenoids. The energy E_M stored inside these components is in the form:

$$E_M = \frac{1}{2} L_M I^2 \tag{1.1}$$

where L_M is the magnetic inductance, and I is the current passing through the device. A similar formula can be derived for the kinetic inductance [25], starting from the relation between current and charge-carriers velocity.

The current passing through a conductor is defined as the charge crossing its section in the time interval, that is $I = \Delta Q/\Delta t$. Specifically, the number of carriers crossing the section is the Cooper pair volumic density n_s times the actual volume, which is equal to hwl, as illustrated in Fig. 1.1. The length of the volume crossing the section can be expressed as a function of the particles' mean velocity $l = v\Delta t$. Each Cooper pair carries a charge equal to $2e$. Therefore, the total charge ΔQ is:

$$\Delta Q = 2e\, n_s\, hw\, v\Delta t$$

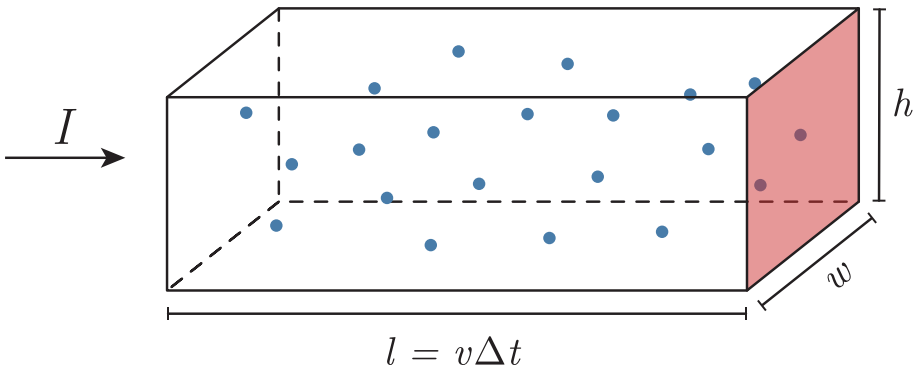

Figure 1.1: Schematic of a conductor showing the relation between current and charge carriers velocity. The current is defined by the charge passing through the cross-section of the conductor in the time interval. Thus, it is equal to the density of charge carriers n_s, times their charge ($2e$ for Cooper pairs), times the volume crossing the surface in the time interval ($hw\, l = hw\, v\Delta t$), divided by the time interval itself.

From the charge, the relation between current and particles velocity can be obtained:

$$I = \frac{\Delta Q}{\Delta t} = (2e\, n_s\, hw)\, v$$

Therefore:

$$v = \frac{I}{2e\, n_s\, hw} \tag{1.2}$$

Each Cooper pair is composed of two electrons; thus, its kinetic energy equals $m_e v^2$, where m_e is the electron mass. When summing the contribution of all the carriers in the volume (multiplying by the number of particles N), E_K can be expressed as:

$$E_K = N\, m_e v^2 = n_s\, hw\ell\, m_e v^2 \tag{1.3}$$

Where ℓ is the length of the whole conductor.

Substituting the velocity v from Eq. 1.2 into Eq. 1.3, the kinetic energy can be expressed as a function of the current I:

$$E_K = (n_s\, hw\ell\, m_e)\left(\frac{I}{2e\, n_s\, hw}\right)^2 = \frac{1}{2}\left(\frac{m_e\, \ell}{2e^2\, n_s\, hw}\right) I^2 = \frac{1}{2} L_K I^2 \tag{1.4}$$

The expression is analogous to Eq. 1.1. Consequently, the kinetic inductance can be defined as:

$$L_K = \left(\frac{m_e}{2e^2}\right)\left(\frac{\ell}{hw}\right)\left(\frac{1}{n_s}\right) \tag{1.5}$$

In addition, the density of Cooper pairs n_s is a function of the operating temperature, and its dependency can be approximated as $n_s(T) \approx n_s(0)(1 - T/T_C)$ within Ginzburg–Landau theory [26]. This dependency causes the kinetic inductance to be non-linear with temperature [27]. Indeed, it can be expressed as:

$$L_K(T) = L_K(0)\, \frac{1}{n_s(0)\,(1 - T/T_C)}$$

It is worth noting that, contrary to the electrical resistance, L_K does not depend on carriers' relaxation time (i.e., the mean time between two scattering events). In a superconductor, the relaxation time tends to infinity, causing the electrical resistance to vanish. Therefore, the kinetic inductance becomes the dominant term of the superconductor's impedance.

Furthermore, the crystalline structure has a significant influence on the properties of a superconductor. Precisely, higher values of kinetic inductance are found in strongly disordered thin films [28][29].

Superconducting resonators at microwave frequencies are the main application for kinetic inductors [30]. Nevertheless, this kind of inductance represents a fundamental parameter for all the devices based on superconducting nanowires. As will be discussed later on, the kinetic inductor is a key component for the functioning and scaling of the circuits presented in this work too.

1.2 Superconducting nanowire

Superconducting nanowires are non-linear components that have drawn particular attention in cryogenic electronics. In Fig. 1.2 the current versus voltage (I-V) curve of these devices is shown. From the curve, three main regions of operation can be identified: the superconducting state, the expansion of the hotspot, and the resistive (or normal) state [31].

In the superconducting state (labeled with (a) in Fig. 1.2), the current flows with no ohmic resistance and thus produces no voltage across the device. This condition occurs until the current I exceeds the switching current value I_{SW}. Above this threshold current, the superconductivity is suppressed in a region of the nanowire. In this region, the material behaves as a normal conductor, exhibiting an ohmic

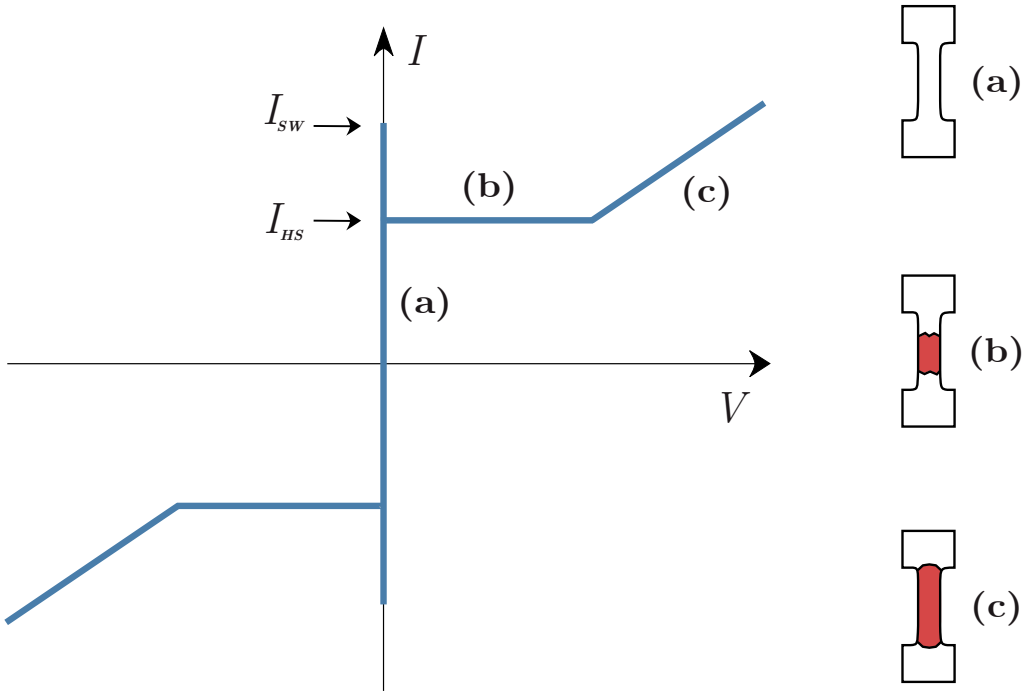

Figure 1.2: Superconducting nanowire I-V curve. **(a)** The nanowire is in the superconducting state. No potential difference is produced at the terminals if current is sent in this regime. **(b)** When the current exceeds the nanowire switching (or critical) current I_{SW}, the superconductivity is suppressed in part of the component, generating a hotspot. In this state, the current drops to I_{HS}. Applying a larger voltage increases the hotspot size, and thus the resistance, linearly, causing the current to plateau. **(c)** The whole nanowire is in the normal state at a large enough voltage. The resistance can not increase anymore, producing a linear voltage-current relation. Figure from [31].

resistance. Under these conditions, a voltage increase does not produce any variation in the current value (shown in the (b) section of the graph). This effect is caused by a linear growth of the hotspot size (and relative resistance) with voltage, which keeps the current at the I_{HS} value [32]. Lastly, if the voltage is further increased, all the nanowire eventually turns into the normal state (Fig. 1.2c). Under this circumstance, the wire behaves as an ohmic resistor (typically in the kΩ range).

Superconducting nanowires have been proposed for single-photon detection in 2001 by Gol'tsman *et al.* [34]. In recent years, superconducting nanowire single-photon detectors (SNSPDs) have gathered increasing attention due to the small jitter, low dark counts rate, and high detection efficiency [1].

An SNSPD is composed of a superconducting nanowire biased with a current slightly lower than the critical current of the device. In Fig. 1.3 the photon detection mechanism is depicted. If the current is close enough to the critical current (Fig. 1.3a), the absorption of a single photon can lead to the generation of a hotspot (Fig. 1.3b). This normal state area expands following an avalanche effect: the more the hotspot grows, the more the current crowds in the superconductive parts of the wire, causing those areas to switch to the normal state too (Fig. 1.3c). When the lateral expansion of the hotspot reaches the wire edges (Fig. 1.3d), the superconducting path is interrupted, and the voltage increases. The current is diverted to the shunt resistance (e.g., the 50 Ω input impedance of the amplifier). The decrease of current in the nanowire and the thermal dissipation of the hotspot help recover the superconducting state (Fig. 1.3e). Once the superconducting state of the nanowire is restored, the bias current moves back to the detector (Fig. 1.3a). The initial conditions are reestablished so the nanowire can collect photons again.

The detection of a photon generates a voltage pulse, which characteristic shape is shown in the center of Fig. 1.3. This voltage curve is strongly asymmetrical, with a rise time much shorter than the fall time: the first in the order of picoseconds, the latter in the nanoseconds range. Therefore, the fast rise time, given by the avalanche effect of hotspot expansion, is responsible for the low jitter, while the slow fall time, necessary to recover the superconducting state, limits the maximum speed of operation.

For high bias current values, the shunt resistance R_s and the nanowire's intrinsic kinetic inductance L_K are crucial parameters for the functioning of the device. In particular, different operating conditions can lead to two alternative behaviors of the nanowire. The first unusual behavior is named *latching*. When the electrical time constant, determined by the ratio L_K/R_s, is smaller than the thermal time constant, the hotspot does not recover when the current is removed. If the device is over-biased (i.e., the bias current is higher than the switching current), the electrical circuit is fast enough to reach an equilibrium point in which the current is split between the resistor and the nanowire, in the normal state [32]. Thus, the superconducting state is not recovered, and the voltage latches to a constant value. Once an SNSPD latches, it can not detect other photons until the superconducting state is externally restored, turning off the bias current.

High-valued shunt resistors cause an over-biased nanowire to latch. On the contrary, a small shunt resistance makes the device oscillate. This effect was first

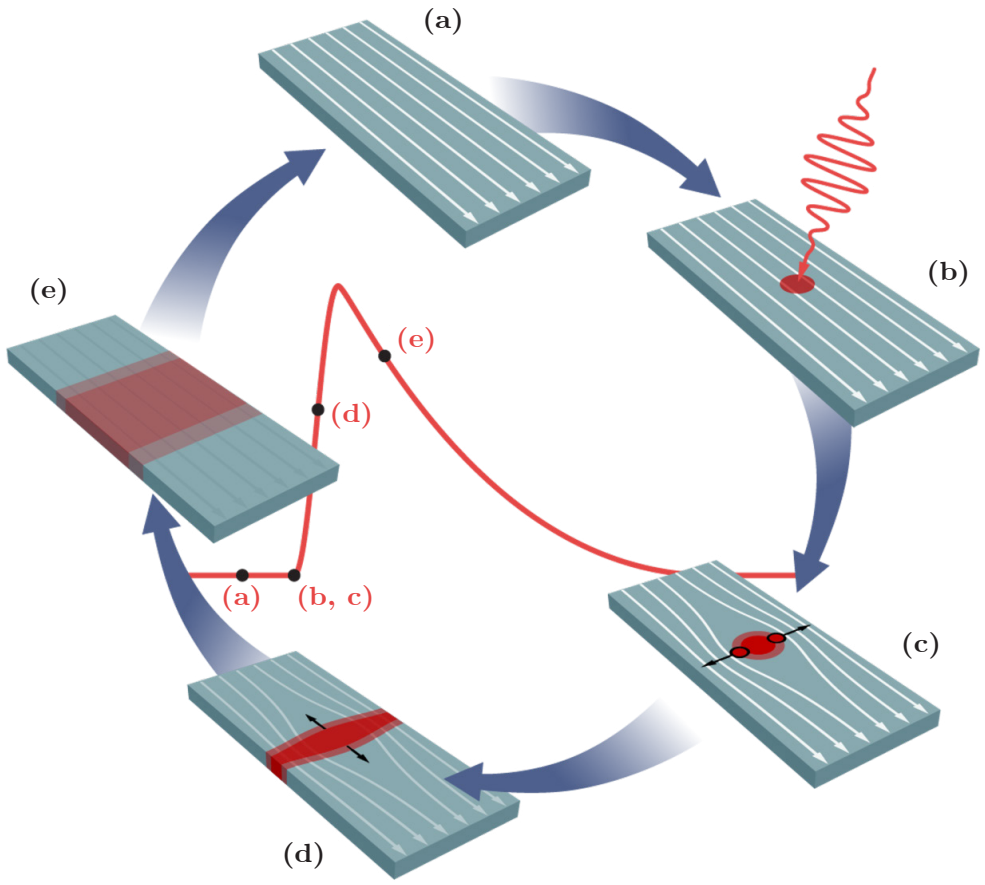

Figure 1.3: Superconducting nanowire single-photon detector (SNSPD) principle of operation. **(a)** The nanowire is biased below its critical current. The voltage at the terminals is null. **(b)** A photon impinges on the detector. If its energy is sufficient, some Cooper pairs are broken into electrons. The thermalization of the electrons forms a hotspot in which the superconducting state is suppressed. **(c)** The supercurrent is diverted from the hotspot region. The current crowds and exceeds the critical current density around the hotspot, switching a larger area to the normal state. **(d)** The hotspot expands to the whole width of the nanowire. No superconducting path between the terminals is present anymore. This condition results in a voltage increase. The current causes the hotspot to expand longitudinally. **(e)** The current is diverted from the nanowire to the shunt resistor. The lowering of the nanowire's current and the hotspot's dissipation allow the recovery of the superconducting state. Figure from [33].

observed in [35]. Under these circumstances, when the device is over-biased, the current is periodically transferred from the nanowire to the shunt resistor and vice versa, forming and dissipating the hotspot. The result is in the generation of a train of spikes whose frequency depends on the bias current [32].

The presence of these behaviors can be exploited for specific applications, such as neuromorphic computing [36]. However, it negatively affects the range of operation of the devices presented in the following. For this reason, they were taken carefully into account during the design process.

1.3 Nanocryotron

As the previous section shows, an SNSPD can generate a voltage pulse when a photon is impinging on the nanowire. A similar voltage pulse can be generated electrically, suppressing the nanowire switching current by injecting a current pulse into a third terminal. A device working likewise was proposed in 2014 by McCaughan and Berggren [14]. This device was named *nanocrytron* (shorten to nTron) after the cryotron, a superconducting switch developed by Dudley Buck in 1956 which used a magnetic field induced by a solenoid to suppress the superconductivity in a channel,

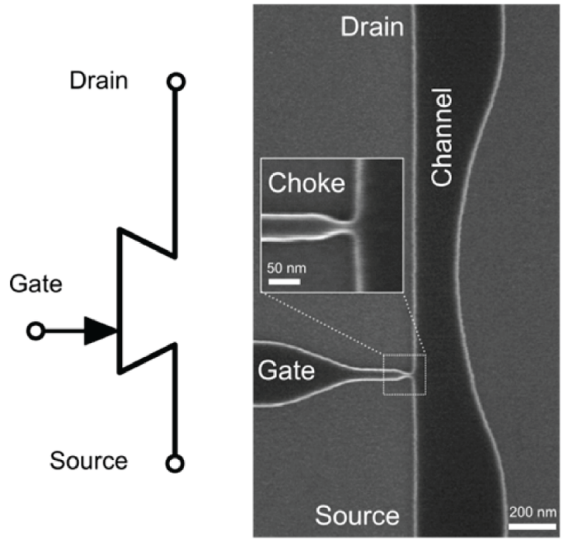

Figure 1.4: Schematic and scanning electron micrograph of a nanocryotron. **(a)** The schematic shows the terminals of the device, which follow the general transistor nomenclature. In particular, the nanowire lies between the drain and source contacts, with the gate connected perpendicularly. **(b)** In the scanning electron microscope (SEM) picture, the choke connecting the gate and the nanowire is shown. This feature is critical for the correct operation of the nTron. Figure from [14].

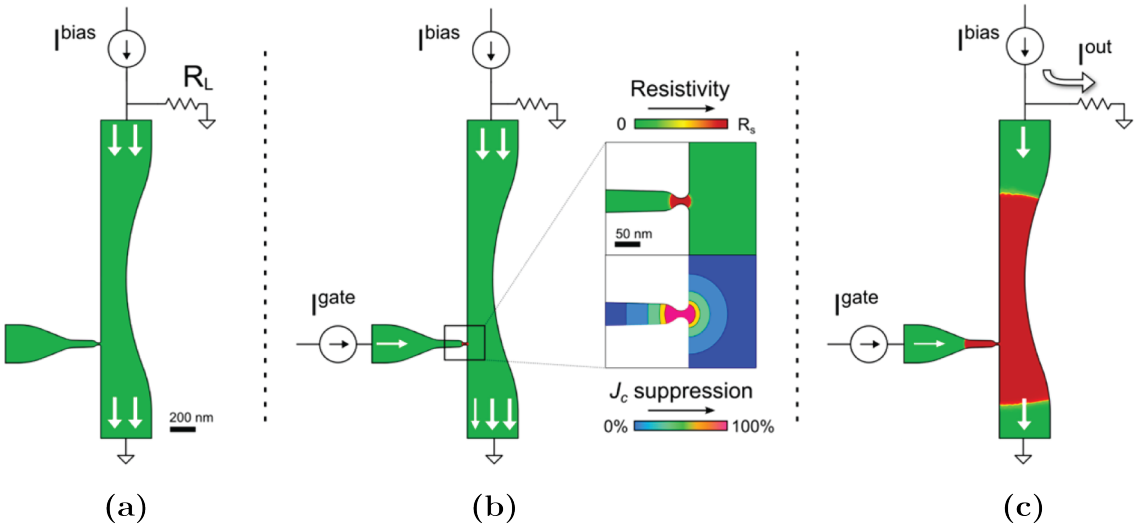

Figure 1.5: Nanocryotron principle of operation. **(a)** Current flows along the nanowire, no current is injected from the gate. The whole device is in the superconducting state (in green). **(b)** Current is injected into the gate terminal. This current exceeds the choke's critical current, generating a localized hotspot at the intersection of the gate and the main channel. This hotspot suppresses the critical current in the intersection's proximity, decreasing the effective critical current of the nanowire. **(c)** If the bias current is large enough, the hotspot expands along the whole nanowire's section. The normal state (in red) interrupts the superconductive path to ground, raising the voltage on the nTron drain and diverting the current to the shunt resistor. Figure from [14].

creating a resistive state [37].

In Fig. 1.4 a schematic and an electron micrograph of the device are shown. In the schematic, the transistor-like structure, with the three distrinctive terminals, is illustrated. Analogously to metal-oxide-semiconductor field effect transistors (MOSFET), the device is composed of a main channel (connecting drain and source terminals), whose conduction properties are controlled by the gate terminal.

The main channel is normally in the superconducting state, as shown in Fig. 1.5a. Under these circumstances, no difference in potential is present between source and drain terminals; therefore, the entire bias current flows in the nanocryotron channel and not in the shunt resistor. When an intense current pulse is injected into the gate terminal (Fig. 1.5b), the current density inside the choke, the narrow connection between the gate and the channel, exceeds the critical current density generating a localized hotspot. The hotspot partially expands into the main channel, causing the effective channel switching current to decrease. If the bias current value is greater than the suppressed channel critical current, the whole channel switches to the normal state (Fig. 1.5c). In this condition, the current split between the channel

and the shunt resistor, generating a potential difference between source and drain of the nanocryotron. Depending on the kinetic inductance of the channel and the shunt resistance, the superconducting state is recovered, generating just a voltage pulse, or not. In the second case, the channel latches in the normal state, producing a constant voltage at the output (the drain terminal).

The nTron has gathered attention thanks to its uncommon properties, compared to the Josephson junction. JJs offer better performances in terms of speed and power consumption. However, the low voltage pulses generated by these devices limit their fanout (i.e., the number of devices that a junction's output can drive). In addition, the sensitivity to stray magnetic fields can largely affect the functioning of Josephson junctions, which thus require proper magnetic shielding. On the contrary, the possibility of operation in magnetic fields and the capability of driving high-impedance are intrinsic properties of a nanocryotron [14], making it a unique device in the field of superconducting electronics.

Another attractive characteristic of the nTron lie in its geometric structure and fabrication. Indeed, as shown in section 2.4, a nanocryotron can be patterned on a thin film in a single lithographic step. The simplicity of its structure makes it easy to reproduce and robust against process variations. Additionally, the device is fairly small (between tens and hundreds of nanometers), especially compared to Josephson junctions, which have micrometric dimensions [38].

The aforementioned properties raised some interest in employing this technology for different applications. A current comparator can be made by biasing an nTron with the proper channel current. If an input pulse has sufficient current to create a hotspot in the choke, this suppresses the channel critical current causing it to switch. Designing the nTron to have a large ratio between the channel and the choke, an input-output current gain can be obtained [39]. In this work, the nanocryotron is mostly operated as a normally-closed switch. In order to better understand the digital circuits presented in the following is convenient to conceive the device this way.

Given the evident affinity, the nTron was first devised to be coupled with SNSPDs as an amplifier [14]. Nevertheless, the nanocryotron was shown to be able to interface with other superconducting technologies, such as SFQ, and CMOS, in [15]. It has also been proposed to connect JJs and light emitting diodes (LED) in a heterogeneous neuromorphic system [40].

The advantages offered by nanocryotrons, such as the robustness against magnetic fields and compact dimensions, can be exploited in systems completely based on this technology. Some effort was put in this direction. Two examples are the superconducting nanowire encoder proposed in [16] and the memory cell developed in [17], which is based on a variation of the nTron.

However, a way to move from these proof-of-concept circuits to larger modular systems employing nanocryotrons has not been proposed yet. The absence of a set of reliable standard cells able to operate combinatorial and sequential elementary functions prevented the complexity of nTron circuits from increasing. This work

intends to address this problem, trying to shift the design paradigm of nanocryotron circuits from specific design approaches to a more general purpose strategy, which may favor the scaling up.

1.4 Superconducting loop

The last component to be introduced is the superconducting loop. This element is employed in this work as a memory element. Indeed, thanks to the absence of ohmic losses, the current can flow around a superconducting loop indefinitely. The current flowing in a superconducting loop is named *persistent current*. According to a fit of experimental data, the persistent current can be stored in a loop for over 100 000 years [41].

In Fig. 1.6 a simplified circuit schematic is used to show how the current can be stored in a superconducting loop. When a loop branch is open, the current is forced to flow in the other branch (Fig. 1.6a). When the loop is closed (Fig. 1.6b), the

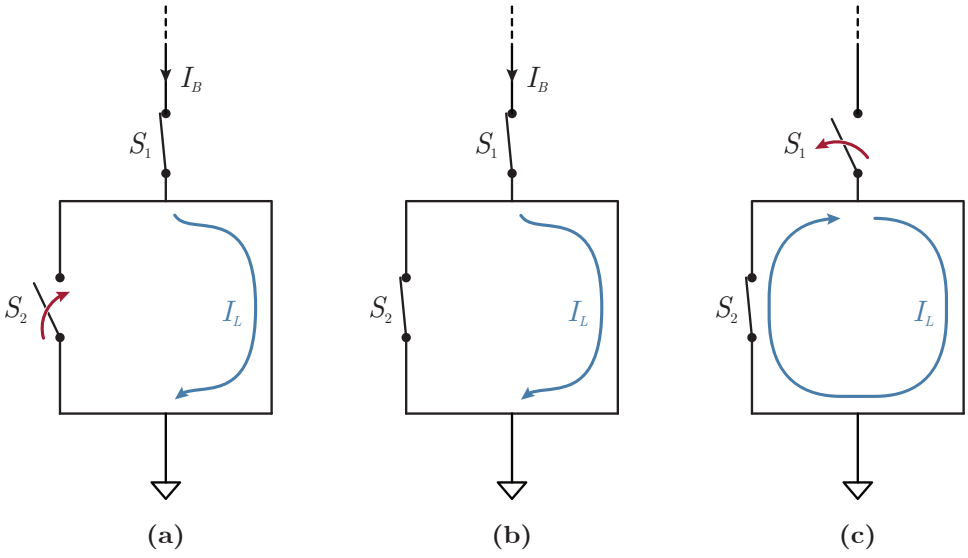

Figure 1.6: Circuit schematic showing the persistent current storage in a superconducting loop. **(a)** Direct current I_B is injected into a superconducting loop. The switch S_2 is open, making the whole current flow in the other branch, thus $I_L = I_B$. **(b)** The closing the S_2 switch forms the superconducting loop. Due to the kinetic inductance of the wires and the absence of resistance, the current keeps flowing in the right branch of the loop. **(c)** If the switch S_1 is opened, the loop is disconnected from the bias. The current can not flow anywhere but in the other branch of the loop now. Being the whole loop superconducting, the current keeps flowing with no ohmic loss around it. A persistent current is stored in the loop.

current keeps flowing in the same branch. This behavior is not found in a normal conductor, which exhibits an ohmic resistance (causing the current to split between the two branches). Even if the two branches are equal and both superconducting, the kinetic inductance keeps the current flowing in the right branch if no electrical resistance forces the current into the left one. As soon as the loop is disconnected from the bias line, the current has no direction in which to flow but the other branch of the loop (Fig. 1.6c). The result is a persistent current flowing along the loop without resistive losses.

Thanks to its stability, the persistent current along a superconducting loop can be used to implement a memory function. Loops as information storage elements are employed in many superconducting electronics technologies. For example, this component has been employed both in the thermal nanocryotron-based memory proposed by Butters *et al.* in [17], and in the rapid single flux quantum (RSFQ) flip-flop, which can be found in [42].

All the elements composing the superconducting circuits proposed in this work have been introduced. As it will be explained in the followings, each of these components plays a key role in the functioning of the standard cells: the loop stores the information, which is modified by the nTrons, while the inductor directs it properly within and between the cells.

Chapter 2

Methods

Once the necessary technical background has been introduced, the discussion is moved to the steps that have been performed to allow the experimental demonstration of the circuits. Specifically, starting from the superconducting components analyzed, the design process of the circuits will be presented and justified. Afterward, the details of the circuit simulation, sizing, and layout will be illustrated. Lastly, the description will focus on the fabrication and characterization of the devices.

For the sake of clarity, the steps conducted in this work will be presented linearly, showing each task after the preceding one. Although this method allows a better comprehension of the whole process, it is necessary to notice that the actual workflow that led to the fabrication and testing of the final devices is composed of many feedbacks. The design has been influenced by the results of the simulations and by the preliminary experimental results obtained from the circuits' single components; similarly, the layout was affected by the fabrication process. Albeit this clarification could be considered trivial, the continuous improvements based on the results of every step significantly affect the development of this work.

2.1 Design

The first part of the work involved the design and possible implementation of the nanocryotron logic building blocks. A bottom-up approach is applied to the description of the logic cells design process. Specifically, the presentation of the process will start from the initial concept of the building block, its circuital implementation, and the principle of operation. Afterward, the discussion will focus on the logic cells derived from the initial one and how these can be combined to obtain more complex devices.

2.1.1 Concept

The goal of the design process was to create a building block for sequential and combinatorial logic. The configuration and combination of this elementary block were intended to form a complete basis for the design of any finite state machine (FSM) based on nanocryotrons.

The block representation of the elementary cell is shown in Fig. 2.1. Its structure includes a storage element powered by a bias line and three terminals: an input (IN), a read (READ), and an output (OUT). The block works as a destructive readout (DRO) memory: an input signal arriving at the IN terminal gets stored by the block (one-state). If the cell is read, an output signal is generated, and the cell is reset to the initial (zero) state.

An efficient implementation of this block, and of the ones derived from it, should exhibit some favorable properties in terms of power consumption. This quantity affects the required energy per operation; additionally, the overall device power consumption is limited by the power dissipation of the cooling system. Therefore, a lower power consumption allows the integration of larger circuits [43].

Two design choices have been made to reduce the block's energetic cost: avoiding

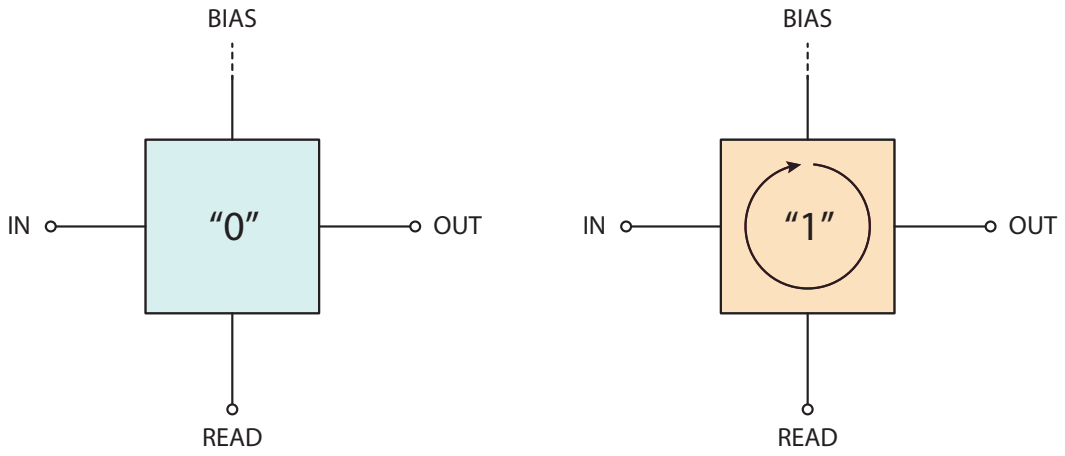

Figure 2.1: Memory cell block scheme. The three terminals are shown: input (IN), read (READ), and output (OUT). The block is powered by a bias line (BIAS), which in the scheme includes the grounding too. The two boolean states of the memory are depicted. **(a)** The memory cell is in the zero-state ("0"), no persistent current is stored. If a read signal is sent, no output signal is generated. If an input signal arrives, the cell transitions to the one-state ("1"). **(b)** The memory cell is in the one-state. The information is stored in a loop's persistence current. If an input signal arrives, the cell remains in the one-state. If a read signal is sent, an output signal is generated, and the cell is reset to the zero-state, erasing the persistent current.

static power consumption and employing spikes for encoding the information. While the absence of static power consumption is clearly advantageous, the utilization of spikes needs further clarification. The use of spikes for efficient computing has recently gathered interest [44] for its ability to concentrate all of the energy in short time pulses and not in direct voltage signals, such as in CMOS technology, which can increase leakage-related energetic losses. Moreover, the hotspot formation, at the basis of the nanocryotron working principle, is a threshold effect since the hotspot is generated above a certain critical current. Concentrating the information in short pulses allows for exceeding the critical current with a lower energy per switch and faster. Due to the hotspot formation and recovery process, the superconducting nanowires are naturally suited to work with spikes. In the devices developed in this work, the information was digitally encoded in spikes, with the absence and the presence of one of those corresponding to a "0" and "1", respectively.

When the nTron was designed, a set of logic gates based on it was proposed too [14]. However, these building blocks does not include any storage element, exploit different principles for different logic functions, and in some cases exhibit static power consumption, which prevented their further development.

The memory cell was implemented by combining the power requirements and the building block concept previously discussed. The superconducting circuit is shown in Fig. 2.2. From the figure, the correspondence between the block diagram's terminals and the circuit schematic ones can be noticed. The circuit is exclusively composed of components presented in the previous chapter: a superconducting loop, fed by a bias

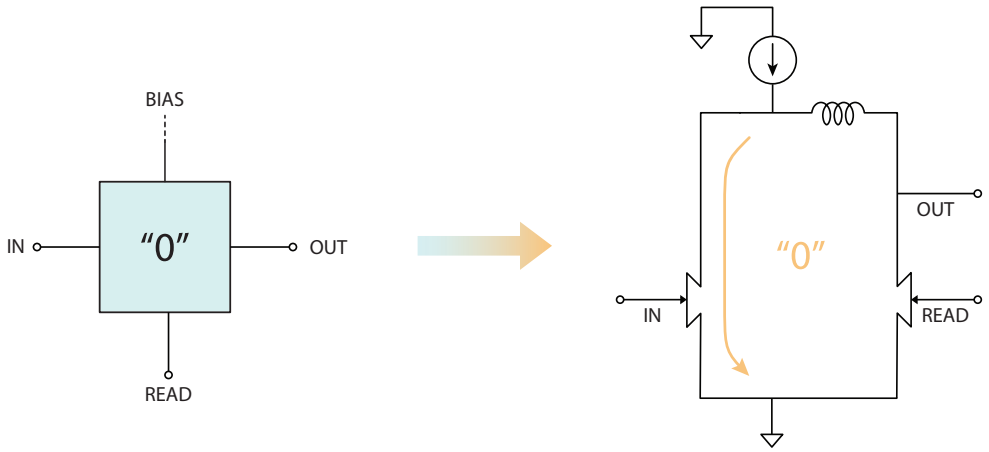

Figure 2.2: Block diagram and corresponding circuital implementation. On the left, the previously-shown block diagram of the memory cell is depicted. On the right, the circuital implementation is shown. In the circuit, the superconducting components (nanocryotrons, kinetic inductor, and superconducting loop) and the terminals' correspondence with the block diagram can be noticed.

line, which includes a kinetic inductor in the right branch and two nanocryotrons, one for the input, the other for the read signal. In the following, the role of these components and the device principle of operation are described.

2.1.2 Principle of operation

The information in the circuit is stored in the current flowing in one or the other branch of the loop. Precisely, the current flowing in the left branch corresponds to the zero-state, and flowing in the right branch to the one-state. The memory cell state can be modified by firing one of the nTrons, which diverts the current to the opposite branch, changing the boolean state.

When the bias is turned on, the kinetic inductor prevents the current from flowing in the right branch. Therefore, the bias current is entirely sent to the left branch. The cell is initialized in the zero-state, ready to store an input value.

The procedure for writing a one ("1") in the memory is shown in Fig. 2.3. Starting from the zero-state (Fig. 2.3a), a current pulse can be injected into the IN terminal. This pulse generates a local hotspot at the choke of the input nTron. Due to the bias current flowing in the left branch, the hotspot expands throughout the nanocryotron's main channel, causing the whole device to switch to the normal state. The current is diverted to the right branch superconducting path (Fig. 2.3b), changing the memory state from "0" to "1". The hotspot in the loop's left branch recovers, but the bias current keeps flowing in the right branch (Fig. 2.3c). The cell is now in the one-state.

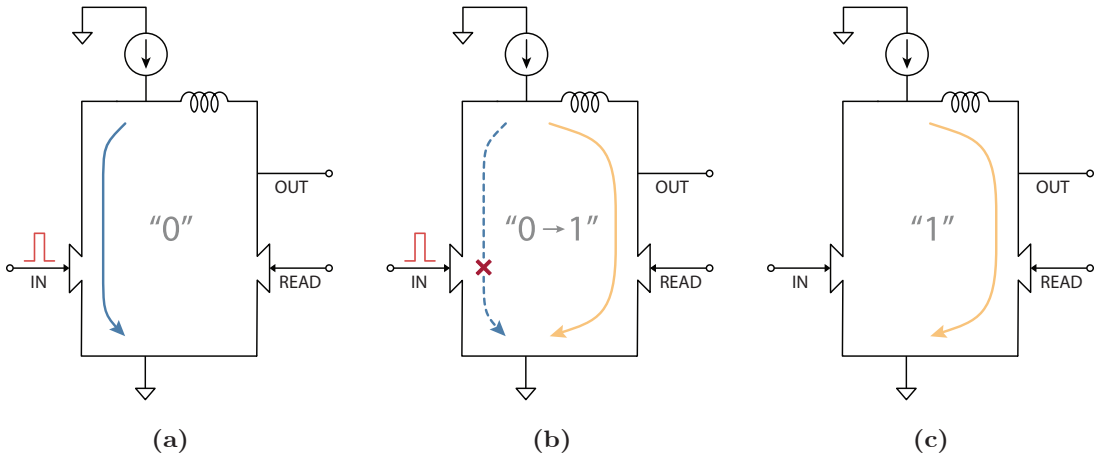

Figure 2.3: Procedure for writing a "1" in the memory cell. **(a)** The memory is in the zero-state "0". The current flows in the left branch. An input pulse is injected. **(b)** Since the current is flowing in the input branch, the pulse causes a hotspot to form and expand. The current is diverted to the right branch, causing the cell to transition from the zero-state to the one-state "1". **(c)** The current now flows in the right branch of the loop. The cell is in the one-state.

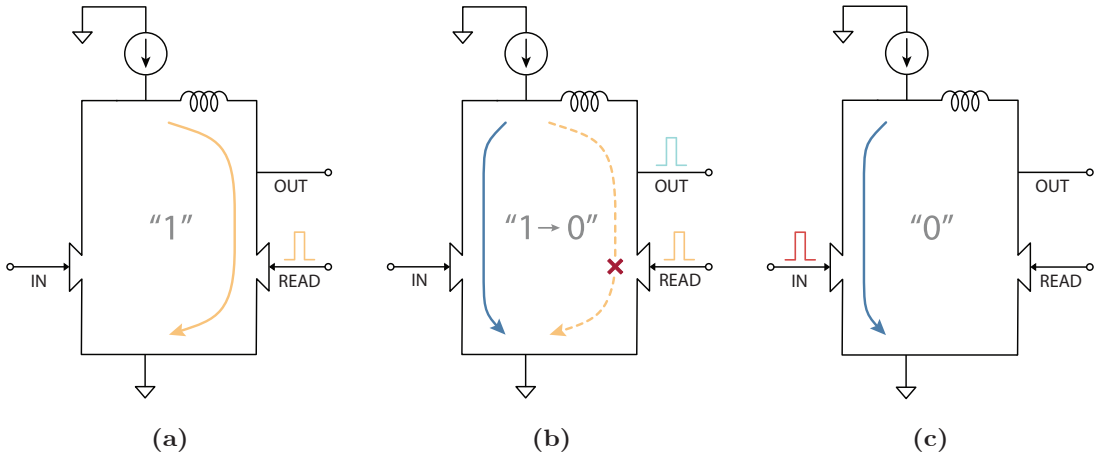

Figure 2.4: Procedure for reading a "1" in the memory cell. **(a)** The memory is in the one-state "1". The current flows in the right branch. A read pulse is sent. **(b)** Since the current is flowing in the read (right) branch, the read pulse causes a hotspot to be generated and expand. The current is restored in the left branch, causing the cell to transition from the one-state to the zero-state "0". Moreover, the normal state generated in the channel of the read nTron gives rise to a voltage pulse, which can be observed at the output (OUT) terminal. **(c)** The current now flows in the left branch of the loop. The cell is reset in the zero-state.

If an additional pulse is sent at the input, nothing happens. A hotspot is generated at the input nTron choke, but the absence of bias current in the left branch prevents the hotspot from expanding in the main channel.

For the same reason, when a read signal is sent to a memory cell in the zero-state, no hotspot, and thus no output signal, is generated. Conversely, an output signal is produced when a cell in the one-state is read. The corresponding procedure is shown in Fig. 2.4. This process mirrors the one described for the writing. The current pulse is now sent to the left (READ) nTron, where the bias current is flowing. The hotspot expands and diverts the current, resetting the cell to the zero-state.

The main difference between the two processes lies in the output generation. When an input pulse causes an nTron to switch, a voltage pulse is generated at the drain terminal. However, thanks to the presence of the kinetic inductor, the voltage pulses generated on the left nTron's drain are filtered by the inductor, while the ones generated on the right nTron's drain are sent to the output and not to the left branch of the loop. Therefore, the kinetic inductor does not only divert the current setting the cell to the initial state but allows for generating output pulses at the OUT terminal and filtering the unwanted pulses generated in the other branch.

The operation of the cell can be efficiently visualized through the diagram of a Mealy machine (i.e., a finite state machine (FSM) whose output depends both on the state and the input of the system). The corresponding schematic is illustrated

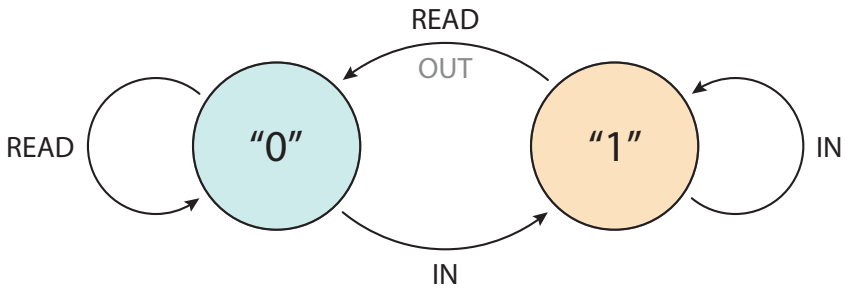

Figure 2.5: Mealy finite state machine representation of the memory cell. The diagram represents the two possible states of the memory and the state transitions induced by the input and read signals. The circuit behaves like a Mealy machine; therefore, its output depends on both the state and the input signals. An output signal is produced only during the transition from "1" to "0" when a READ signal occurs.

in 2.5. The diagram shows the two memory states and the transitions between them. Specifically, the writing procedure, which corresponds to the transition from "0" to "1", and the reading procedure, represented by the "1" to "0" transition, which is the only one generating an output signal, are illustrated. From the diagram, it can also be noticed that no change of state is performed to the cell when read while in "0" or written while in "1".

Particular attention has to be paid when dealing with simultaneous inputs. If both branches are switched to the resistive state, the current is split between the two paths of the loop. This condition causes the cell to end up in an uncontrolled state, in which the correct functioning is not guaranteed. This malfunctioning can also lead the cell to a latching state. To avoid this undesired behavior, it is sufficient to read the cell only when it has reached a stable state. The same requirement is found in sequential circuits based on CMOS: the input of a flip-flop needs to be stable for at least a certain time interval before the following clock edge. This time interval is commonly named *setup time*.

The cell was described as a DRO memory. Introducing the circuit in this way helps to clarify the device's functional behavior. However, to better understand the usage of this block for designing larger systems, it is convenient to look at the device from different perspectives. Particularly, the cell can be considered as a buffer gate, which is the natural way to consider it when compared to the other logic gates presented in the following, or a set-reset latch (SR latch), convenient when two of these cells are combined to form an equivalent delay flip-flop (DFF). The cell can even be thought of as a first-arrival detector. If the IN pulse arrives before the READ one, an output spike is generated, while if the read signal arrives before the input one, no output is produced. The latter function could be used to design elementary

first-arrival photon detectors.

The device principle of operation is reminiscent of the RSFQ flip-flop [42], in which, analogously, the current in the loop stores the information, which is modified by the switching of two Josephson junctions. However, the nanocryotron has got an extra terminal compared to the two terminals of a JJ. The nTron three-terminal structure allows for obtaining other logic functions by slightly modifying the superconducting loop configuration. These different configurations, presented in the following subsection, do not have an analogous RSFQ design.

2.1.3 Configuration

A destructive readout memory cell on its own does not constitute a complete basis for designing finite state machines. However, the cell configuration can be modified to obtain an OR gate, a NOT gate, and a NOR gate. These three gates' schematics are shown in Fig. 2.6.

The first device that can be obtained by modifying the memory cell is the OR gate. An additional nTron can be placed in the left branch of the cell (Fig. 2.6a). In this configuration, if any of the two inputs fires, the current is diverted in the right

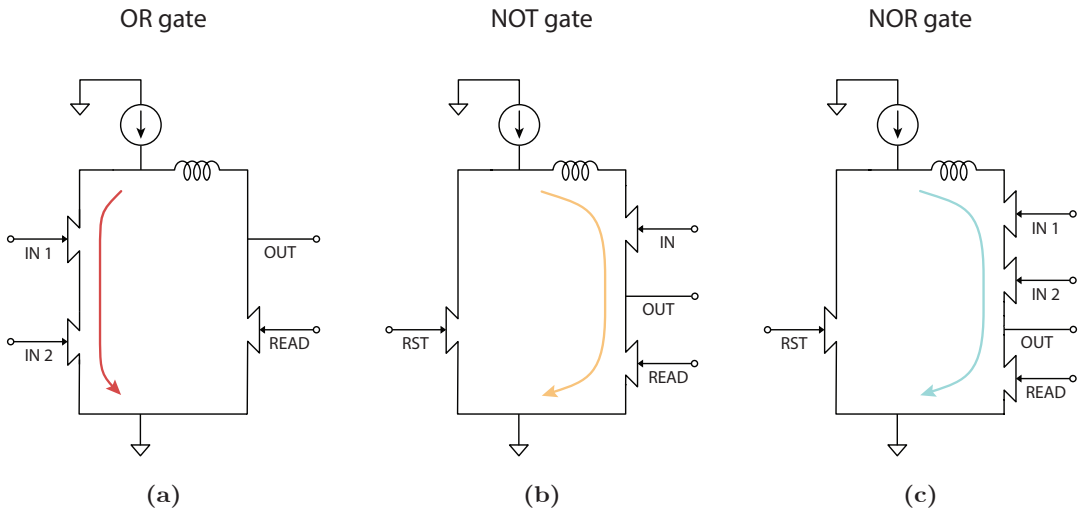

Figure 2.6: Sequential logic gates circuits derived from the memory cell. **(a)** An OR gate can be obtained by adding an extra input nTron. In this configuration, the cell can be set to the logic value "1" if one *or* the other input fires. **(b)** Inverting functions can be produced by setting the cell to "1", firing the reset (RST) nTron. If an input (IN) pulse is injected, the cell is set to "0". Thus, the circuit behaves as a NOT gate. **(c)** Adding an extra input to the NOT gate, as done from the memory cell to the OR gate, a NOR gate is produced. The cell remains in the one-state if neither one input *nor* the other is injected.

branch, switching the state to "1". If none of the inputs receives a current pulse, the zero-state is preserved. No output is generated by a reading of the cell in this case. Therefore, the device behaves as an OR gate.

Inverting gates can be obtained from the elementary cell too. An additional step is necessary to implement this type of functions. Specifically, the loop has to be reset to the "1" state, by firing an additional left-branch nTron (RST terminal). The input IN is now placed in the right branch (Fig. 2.6b). If a current spike is sent at this input, the cell is set to the zero-state. Otherwise, it remains in the one-state. The operation performed in this case is equivalent to a NOT gate.

Adding another input terminal to the NOT gate allows for producing a NOR gate (Fig. 2.6c), analogously to what was done moving from the buffer gate (memory cell) to the OR gate. Among the four gates, the NOR gate is particularly interesting since it is the only *functionally complete* one [45], that is, every boolean function can be expressed just using this operation. This property, along with the memory function, guarantees the completeness of the set of gates for designing finite state machines.

When an input nTron is added to the right branch of the loop, its positioning is relevant. The nanocryotron can not be added underneath the output terminal. If that is the case, every time the right branch input is fired, the superconducting path between the output and the ground is interrupted, generating a spurious voltage pulse at the output. Positioning the additional nanocryotron above the OUT terminal, instead, avoids the generation of unwanted output signals. When the input nanocryotron switches to the normal state, the output is kept at the ground voltage due to the superconducting channel of the read nTron.

In the schematics, only two-input gates were shown. However, as an input nTron was added to the buffer gate to obtain an OR gate, another nTron could be placed in the same branch to make a three-input OR gate. The timing of the cell is not affected by the relative arrival times of the different inputs, since only the first one generates a hotspot that changes the state. The absence of strict constraints on the inputs' timing could be helpful for applications in which the spike's arrival time is not known *a priori*, such as event detection. Additional inputs do not affect considerably the footprint and the electrical characteristics of the circuits too. Therefore, the increase in fan-in (i.e., the number of inputs) of the gates comes with minimal drawbacks in terms of area and timing. This is not the case for other technologies such as RSFQ and CMOS, whose gates fan-in directly affects the footprint and the speed of the devices [46]. Multiple input gates are particularly useful for the design of two-level logic circuits [47]. Moreover, as it will be discussed in section 2.3, high fan-in gates are promising for downscaling the overall system.

A single loop cell can be used to implement more complex logic functions too. An example is shown in Fig. 2.7. In this case, both branches are used for producing the logic function. The overall logic function of the cell will be the AND between the OR of the left branch inputs and the NOR of the right branch inputs. Operating the cell with this approach, additional attention with respect to the timing is required.

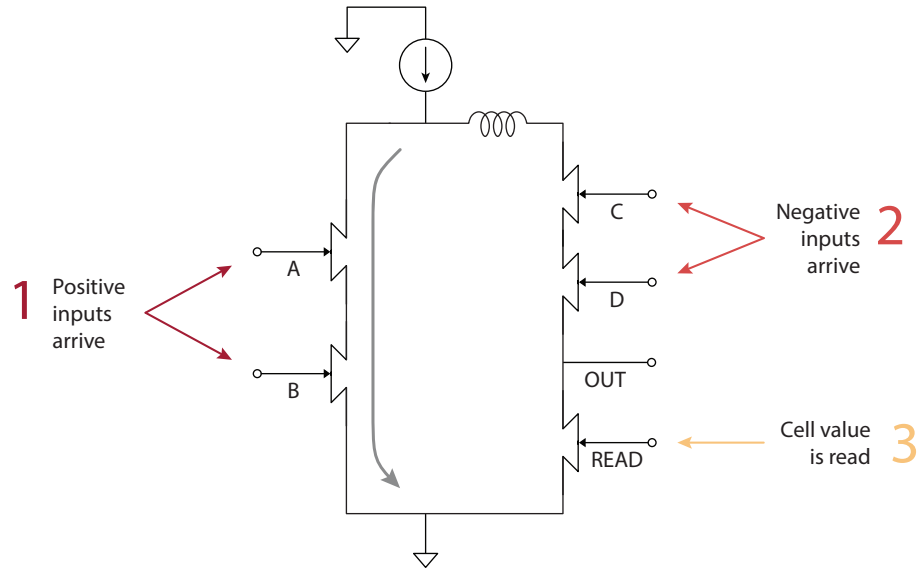

Figure 2.7: Schematic of a generic multiple-input logic gate. In this configuration, the operation is performed in three moments. First, the positive inputs are sent, then the negative ones, and finally, the cell is read. Specifically, the cell reaches the one state, if either A or B fires and none of C and D do. Therefore the circuit performs the function $f = (A + B) \cdot \overline{(C + D)}$, where the plus represents the OR, the dot represents the AND, and the logical inversion is expressed by the overline.

The correct output is obtained only if the right inputs are sent first, then the ones in the right branch, and lastly, the cell is read. Nevertheless, not every logic function can be implemented by means of a single loop. For this reason, the cells need to be easily combined and concatenated. The way to achieve the proper cell combination is discussed in the next subsection.

2.1.4 Combination

A set of building blocks requires the possibility of combining more of them together into larger systems. For this purpose, the output signals generated by a cell should be indistinguishable from the signals received by the inputs. In particular, the current value of an output pulse should be high enough to cause a switching event in the input nTron of the next cell.

The simpler circuit involving multiple cells connected together is shown in Fig. 2.8. This circuit can be thought of as a flip-flop. Specifically, if each memory cell is considered as an SR latch, the circuit structure corresponds to the one of a master-slave flip-flop. Analogously to it, the two memory cells perform different tasks. The first cell gets the input spikes. When it is read, its value is transferred to the second loop, which stores it until the second cell is read too. By concatenating more of

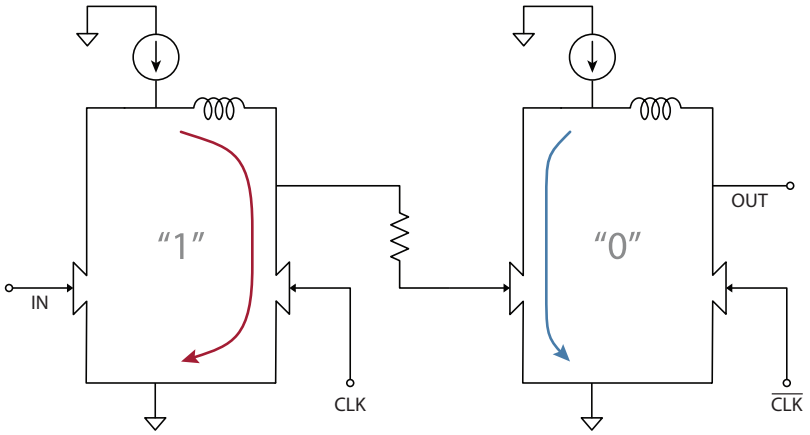

Figure 2.8: Combination of two memory cells to produce an equivalent flip-flop. The output of the first cell is connected with a resistor to the second cell input. The two cells are read at different times. In particular, if a spike is injected at the input, a "1" is stored in the first cell, resulting in the configuration of the figure. A clock pulse (CLK) can shift the "1" from the first to the second cell. The value is stored until the second cell is read by a $\overline{\text{CLK}}$ pulse.

these blocks, the input values can be transferred all along this flip-flop chain. This operation is equivalent to the one of a shift register.

As can be noticed from Fig. 2.8, the connection between two cells contains a resistor. The resistor makes an electrical connection avoiding the presence of any superconducting path between different cells. Such paths could end up storing unwanted persistent currents passing through the gate terminals. These currents would sum up to the signal currents, causing uncontrolled switching events. Conversely, a resistive connection allows the signals to move between the cells but blocks constant (bias) currents, which flow in the superconducting paths to ground found in the loops. The resistor value is not crucial for preventing direct current from flowing in the connection. A smaller resistor will allow a greater current to be injected from one cell to the next. However, small resistances will increase the electrical time constant, slowing down the circuit. Therefore, the resistor value gives rise to a design trade-off.

The amount of current sent from a cell to the successive one is a crucial parameter. A higher output current can more reliably drive the following cell or even drive more than one gate. The number of cells driven by the same output is named fan-out. A small fan-out can limit the application of the device in multi-cell circuits. This problem affects other superconducting technologies such as RSFQ [48]. On the contrary, the nanocryotron's capability to drive high loads is promising for obtaining larger fan-out values. For increasing the fan-out, another solution can be applied, leveraging the nTron's gain. The output pulse of a cell could be amplified by a

single nanocryotron stage before injecting it into the following cell's input. If the signal is large enough, the current could be split into different cells, increasing the fan-out. In order to drive an even larger number of devices from a single output signal, more complex structures have been proposed, such as tree-like structures of nanocryotrons [49], which could exponentially increase the number of output lines.

2.2 Simulation

All the circuits were verified by means of SPICE simulations. In order to simulate the nanocryotron dynamics an LTspice nTron model developed by Castellani in [49] was employed. This model was, in turn, based on the superconducting nanowire electrical model implemented in [31].

Fig. 2.9 shows the results from the simulation of a memory cell with a 60 nH kinetic inductor. The signal traces reported in the plot demonstrate two correct reading operations (respectively, reading a "0" and a "1") and one writing process.

Performing electrical simulations was convenient for two main reasons. First of all, the simulations confirmed the proper logical behavior of the cells, proving the previously described principle of operation right. In the second instance, they allowed for carrying out parametric analyses on the circuit components' values, such as the

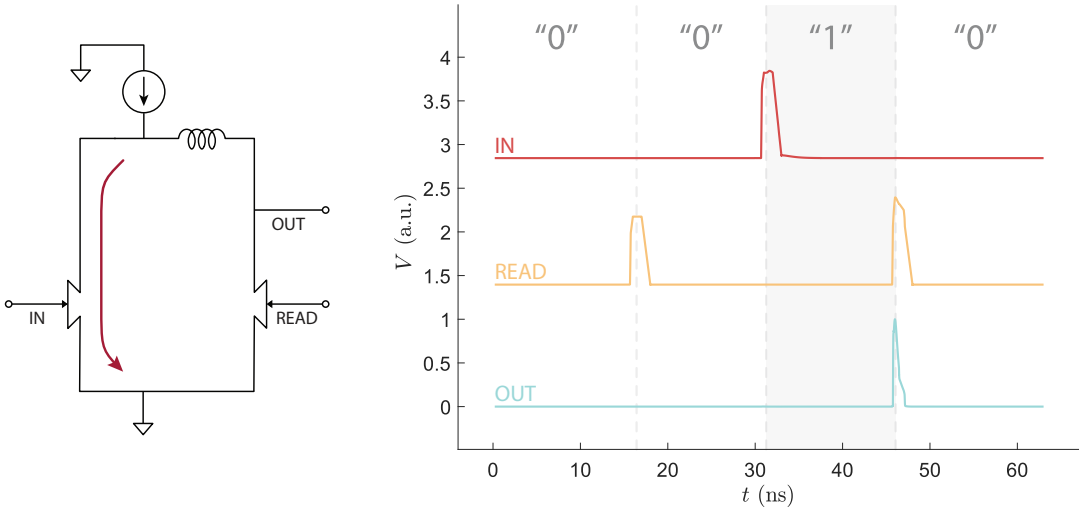

Figure 2.9: SPICE simulation of reading and writing procedures performed on a memory cell with 60 nH kinetic inductance. The time evolution of the three signals is shown. First, the cell, in zero-state, is read, producing no output and leaving the cell's state unchanged. When an input pulse is sent, no pulse is generated at the output, but the cell transitions to the one-state. Lastly, the cell is read, producing an output voltage pulse and resetting the state of the memory.

kinetic inductance, the shunt resistance, and the dimensions of the nanocryotrons.

The dimensions of the nanocryotrons' channel affect the operating point of the devices, that is, the bias and input currents. Three nTron parameters can be mainly tweaked during the design and fabrication: the thin film thickness, the width of the channel, and the width of the choke. Therefore, they were the nanocryotron's parameters of interest during the simulations. The values for each cell were 15 nm for the film thickness, 300 nm for the channel width, and 30 nm for the nTrons choke, which is the device critical feature.

Concurrently, the kinetic inductor and the shunt resistors were sized. Variations of these components' values affect the time constant, thus the dynamics of the system. As previously mentioned, the nanocryotron functioning depends on the hotspot generation and recovery processes, which, in turn, are influenced by the electrical impedance shunting the device. A small time constant (L/R) would cause the device to latch, preventing the cell from working properly. On the other hand, a large time constant reduces the speed of the system and its maximum frequency of operation. Moreover, high-valued resistances and, especially, high kinetic inductances take up a larger area of the chip. Therefore, the downscaling of the cells requires strict limitations on these parameters.

The simulations confirmed the fundamental role of the kinetic inductor in the circuit's operation. Specifically, the inductance is responsible for four different processes in each cell:

- Initializing the memory by sending the bias current to the opposite branch when the cell is turned on.
- Preventing latching by properly setting the circuit's time constant
- Filtering the voltage pulses coming from the left branch switchings.
- Directing the current to the output when a cell in the one-state is read by increasing the output impedance.

A large kinetic inductance favors all of these processes, but, as mentioned above, slows down the circuits and takes up a larger chip area.

Once the devices were tested, the results were compared to the electrical simulations. From the comparison, the main difference between experiments and simulations concerned the occurrence of latching in the devices. In particular, according to the simulations, no device should have worked with a loop kinetic inductance lower than 60 nH due to latching, occurring for every bias current able to switch the nanocryotrons. However, devices including smaller kinetic inductances were fabricated and tested. All of the devices worked properly for a specific operating point, including the one featuring the lowest value of kinetic inductance, equal to 5 nH. The discrepancy, although showing the model to be too sensitive to latching events, allowed for largely shrinking the device and made further scaling promising.

2.3 Layout

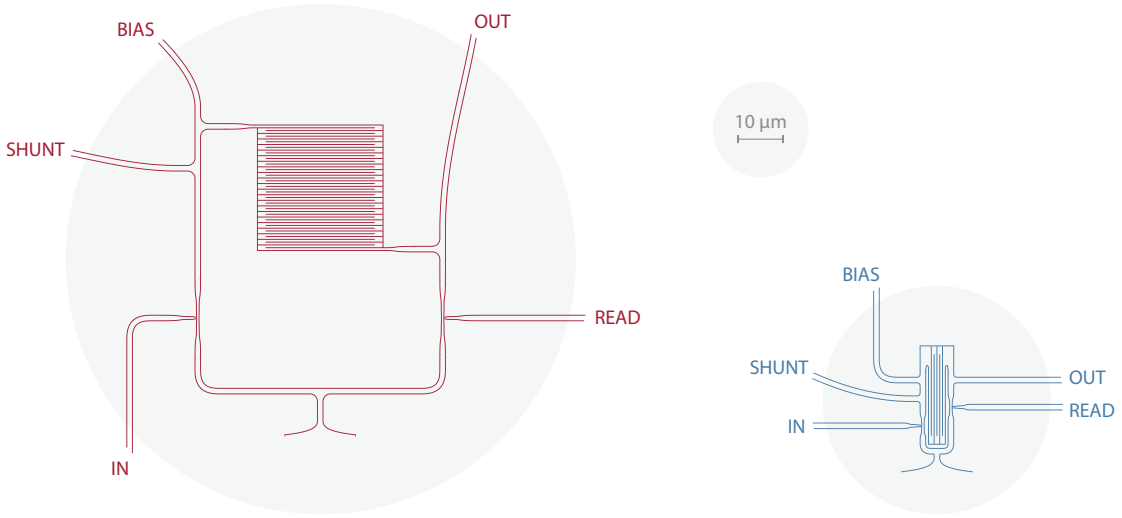

Figure 2.10: First and final cell layout. The first memory cell is shown on the left. In this layout, the correspondence with the schematic is clear: the two nTrons and, in particular, the big kinetic inductor 60 nH can be recognized. The second cell includes a considerably smaller inductor (5 nH), which is wrapped inside the superconducting loop to decrease the device area. The two devices are shown on the same scale to show the effective scaling achieved.

Once all the parameters of the circuits were determined, the circuit layout was developed. The layouts were created using PHIDL, a python package for automated design, optimized for 2D geometries, and developed for device design [50]. This package allowed for generating parametric designs of the circuits, which were used to easily generate chip layouts involving cells with different values of kinetic inductance.

During the development of the cells, different layouts have been devised. Fig. 2.10 shows the first and the final layout of the memory cell, respectively, on the left and right. Showing the initial design is useful for two reasons: making the correspondence to the circuit schematic more clear (in particular for the two nTrons and the 60 nH kinetic inductor), and giving a qualitative sense of the scaling achieved during the work. The final layout of the figure, has a remarkably smaller inductor, of around 5 nH, which is wedged into the superconducting loop, to decrease the total area of the device.

Notwithstanding, the size of the kinetic inductor still represents the main limit to the scaling of single-cell devices. Multiple input gates can be particularly attractive to shrink multi-cell systems dimensions since they allow for reducing the total number of gates needed for performing a logic function, with a limited overhead in area

footprint per cell. In fact, the size of this kind of gates does not scale linearly with the fan-in, since it mainly depends on the kinetic inductor size.

The devices are defined by the area within the two lines. As will be shown in the next section, the lines are etched during the fabrication process separating the inside (the device) and the outside, which acts as a ground plane. The ground plane extends all over the chip, providing proper grounding to the devices. Each cell is connected to ground by the broadening at the bottom of the circuits. The shape of the broadening is designed to prevent current crowding at the connection. It is worth noticing the simplicity and elegance of the devices, defined by just two lines that separate them from the ground plane.

2.4 Fabrication

The fabrication of the devices plays a crucial role in the correct functioning and reproducibility of the designed circuits. The process entailed three main steps: deposition, electron beam lithography, and dry etching. In Fig. 2.11 a cross-sectional view of the sample during the major fabrication steps is depicted. The devices were fabricated on 1 cm^2 silicon dioxide on silicon chips, with an oxide thickness of 300 nm (Fig. 2.11a). A cleaning procedure involving acetone, methanol, and isopropanol (IPA) was performed on all the chips to remove organic contaminants and improve the adhesion of the deposited layer.

The first fabrication step was the NbN sputtering deposition (Fig. 2.11b). This

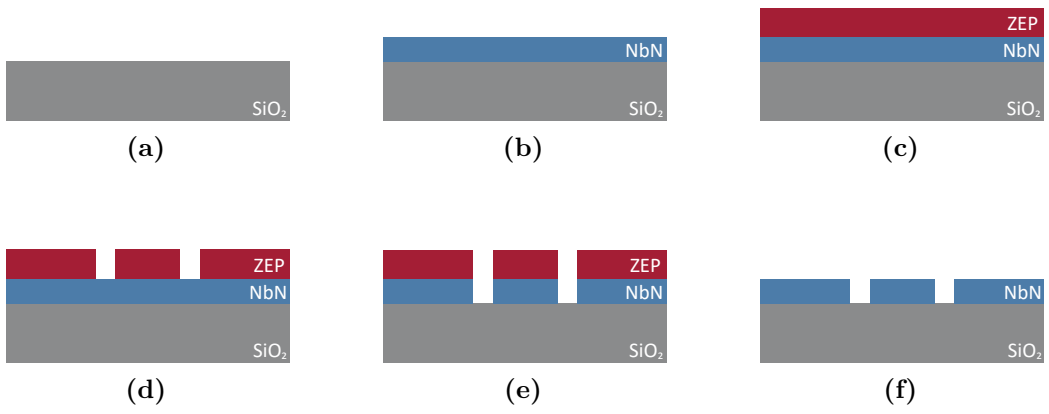

Figure 2.11: Cross-sectional view of a superconducting nanowire during the main fabrication steps. **(a)** Silicon dioxide (300 nm) on silicon substrate. **(b)** Sputtering of 15 nm NbN layer. **(c)** Spin coating of electron beam lithography resist (ZEP530). **(d)** Sample after exposure and cold development. **(e)** Reactive ion etching of the NbN layer, performed with CF_4 chemistry. **(f)** Cross section view of the final device.

process was performed by reactive magnetron sputtering with a niobium (Nb) target in a nitrogen atmosphere. The control of the nitrogen flow allows for adjusting the stoichiometry of the deposited layer. The thickness layer was not a critical factor for the correct functioning of the cells. Nevertheless, this parameter influences the critical temperature T_C [51]. The larger the critical temperature compared to the device operating temperature, the larger the noise margin for the switching events. The desired thickness for the NbN layer was 15 nm, which produced a film critical temperature around 8 K. More details about this deposition process can be found in [52].

After the deposition, a characterization step was introduced to analyze the sputtered film properties. Four-point resistance measurement was performed on the sample to extract the electrical properties of the thin film. Through this measurement, the sheet resistance was calculated using the proper thin-film correction factor [53]:

$$R_{\square} = \frac{\pi}{\ln(2)} \frac{V}{I} \tag{2.1}$$

A complete derivation of this formula is reported in the appendix A of this work. Secondly, the thickness of the film was measured employing ellipsometry [54]. The film thickness was an essential parameter for assessing the quality of the deposition process. Moreover, the film resistivity can be obtained from the ratio of sheet resistance and thickness. From those two parameters, combined with the critical temperature of the film, an estimate of the sheet inductance can be made too [27]. In particular, for a 15 nm NbN film, the expected parameters were around 170 Ω/□ for the sheet resistance, 2.5 µΩ m for the resistivity, and 20 pH/□ for the sheet inductance.

Once the NbN layer was deposited and characterized, the layout of the devices had to be transferred onto it. For this purpose, electron beam lithography (EBL) was employed. The higher resolution given by electron beam lithography, compared to photolithography, favored the reproducibility of the smallest feature, the 30 nm choke of the nTron, and thus the reproducibility of the devices. First, the sample was coated with ZEP530A (about 150 nm thick), a positive-tone resist, at a spinner velocity of 5 000 rpm and baked at 180 °C on a hotplate for 2 min (Fig. 2.11c). Subsequently, the electron beam exposure was performed using the Elionix ELS-F125 with a dose of 550 µC/cm^2. The last step of the electron beam lithographical process was the cold development: the chip was kept for 90 s in o-xylene at 5 °C and rinsed for 30 s in IPA at room temperature. In Fig. 2.11d the sample after development is depicted.

Finally, the NbN layer was etched through reactive ion etching (RIE) with CF_4 chemistry (Fig. 2.11e). The total etching time of 6 min was split into three successive 2 min intervals to avoid burning the resist and thus easing its removal. The resist stripping was performed by leaving the chip in *N*-methyl-2-pyrrolidone (NMP) at 70 °C for about 2 hours. In Fig. 2.11f, the final cross-section of the chip is depicted.

The devices were inspected using the scanning electron microscope (SEM), looking

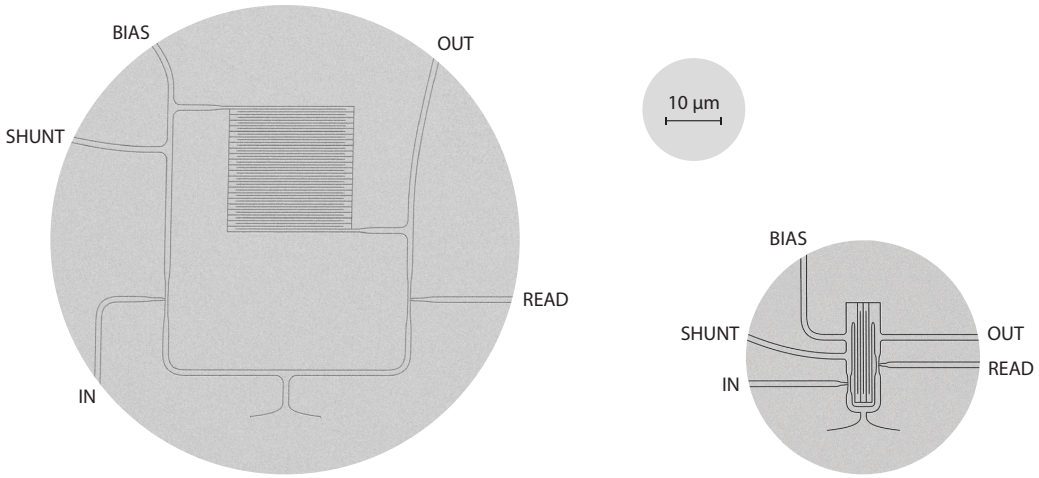

Figure 2.12: Scanning electron micrographs of the first and final cells. In correspondence to Fig. 2.10, on the left is shown the micrograph of the first device that was designed. On the right, the picture of the smallest fabricated and correctly tested cell is shown.

for possible defects and checking the dimensions of the critical features. The micrographs of the first and last fabricated cells are reported in Fig. 2.12. Analogously to the layouts in Fig. 2.10, the cells are shown on the same scale, to exhibit the achieved scaling. From the two SEM pictures, the overall quality of the fabrication process can be appreciated too. Once the devices were fabricated, the chip could be finally measured.

2.5 Characterization

The characterization of a device at cryogenic temperatures requires additional care regarding the whole experimental apparatus. The temperature at which the circuit is operated sets limitations on the materials and components employed. Moreover, particular attention has to be paid to the noise during the measurements. The injection of thermal noise from the experimental setup can perturb the correct functioning of the devices. Proper precautions need to be taken in order to decrease the impact of the external noise. The chip was glued on a printed circuit board (PCB) with GE varnish, an adhesive material for cryogenic applications. The board pads and the chip were electrically connected by wire bonding. On the PCB, shown in Fig. 2.13, surface-mounted resistors and capacitors were soldered. Placing the resistors on the PCB, at cryogenic temperatures, helps decrease the thermal noise produced by these components. The electrical components on the PCB were used

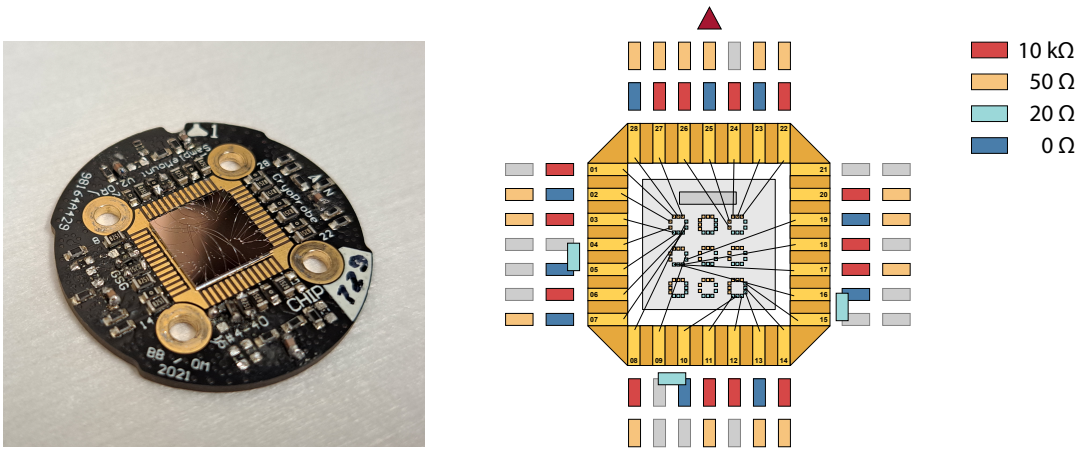

Figure 2.13: Chip mounted on the printed circuit board (PCB) and the corresponding diagram. The left picture shows the PCB to be inserted in the RF probe to test the circuits. In the diagram on the right, the resistances mounted on the PCB and the connections to the chip are shown.

as shunt resistors (50 Ω), resistive connections between loops (20 Ω), matching for signal lines, and circuitry for current biasing. To provide a stable bias current, a 10 kΩ resistor was used, in parallel to a 68 pF capacitance to filter the power supply noise. Analogously, the signals were sent through a 10 kΩ resistor to control the current injected, in parallel with 50 Ω to match the transmission line characteristic impedance. Surface-mounted resistors give an advantage compared to integrated on-chip resistors. After testing the circuit, surface-mounted resistors could be unsoldered and changed for successive measurements to test the effects of different resistance values or fix potential design errors. This degree of freedom can not be exploited when the resistors are integrated on-chip, limiting the possible tests of the chip.

The PCB interfaces the chip and the room temperature electronics. A diagram of the whole electrical apparatus is reported in Fig. 2.14. In the diagram, the connections between the chip's inputs and the arbitrary waveform generator (AWG) and between the circuits' outputs and the oscilloscope are shown. The inputs are split and sent to the devices and the oscilloscope. The outputs' direct current (DC) component is filtered by the bias tees, while the radio frequency (RF) signal is amplified and sent to the scope. The attenuator placed before the amplifier is intended to reduce the amplitude of outputs' reflections.

Fig. 2.15 illutrates the electrical and cryogenic experimental apparatus. The picture shows the previously described electrical setup and the liquid helium dewar. The sample PCB is mounted on the RF probe, developed by Butters [55], which is directly inserted in liquid helium. An exploded mechanical diagram of the probe

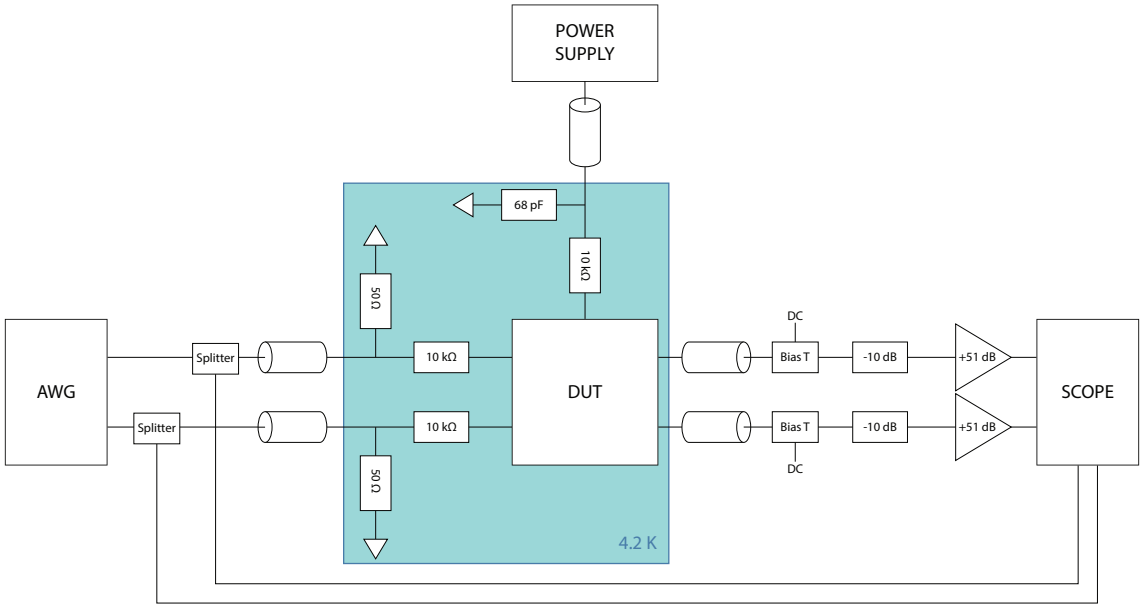

Figure 2.14: Scheme of the experimental electrical setup for measuring the memory cell. The signals from the arbitrary waveform generator (AWG) are split and sent to the device under test (DUT) and to the oscilloscope. The direct current components of the DUT output signals are filtered by the bias tees. The signals are then amplified at room temperature. An attenuator is placed before the amplifiers to reduce the impact of the reflections. The electrical components at 4.2 K are mounted on the PCB. On the bias line, the capacitor filters the power supply noise, while the signal lines are matched with 50 Ω to the generator. 10 kΩ resistors are placed on the lines to make the current pulses less sensitive to the impedance changes in the circuit.

is reported on the right of Fig. 2.15. The probe has 28 RF lines that connect the PCB, submerged in liquid helium at a temperature of 4.2 K(−268.93 °C), to the room temperature setup. Moreover, the probe has additional features. Among these features there is a sensor to record the chip's operating temperature, a fiber to shine a laser from an external source onto the chip, and a copper coil to apply a magnetic field to the sample. The RF probe was a key asset for the testing and development of the devices. Conversely to cryostats, measurements in liquid helium with the RF probe do not involve long cooldown periods. This advantage allowed for rapid testing of different chips, not only increasing the number of devices measured but also decreasing the time interval needed to get results. A shorter time interval between design and experimental results can enhance the development feedback, allowing for more frequent design and fabrication improvements.

In total, 34 devices were fabricated (18 memory cells, 10 OR gates, 2 NOT gates, and 4 NOR gates). Among these circuits, 9 were characterized experimentally, that

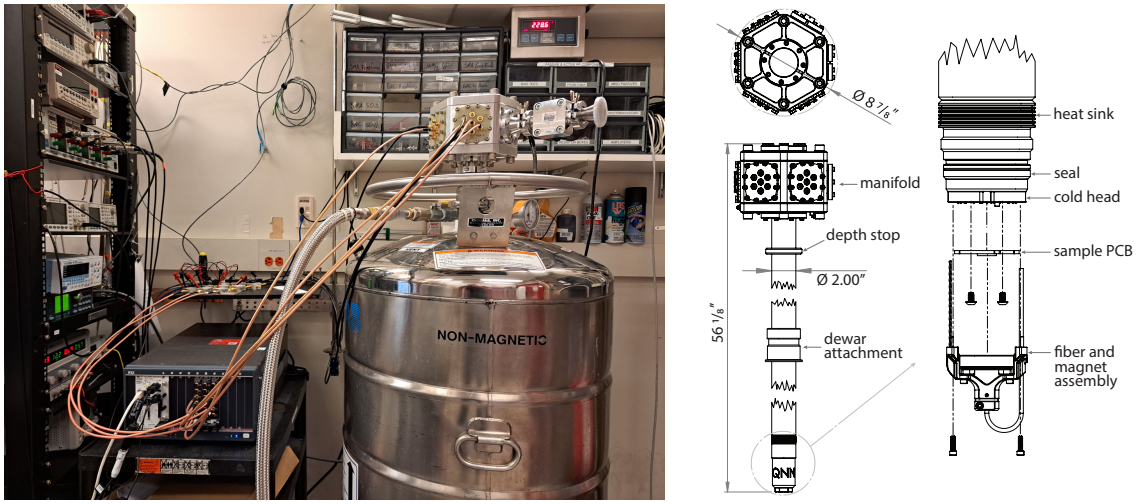

Figure 2.15: Picture of the electrical setup and scheme of the cryogenic probe. In the left picture, part of the experimental apparatus is shown: on the left are the generators and the digitizer, and on the right is the helium dewar with the cryogenic RF probe inserted in it. The mechanical scheme on the right shows the entire structure of the cryogenic RF probe. The upper part connects the room temperature setup and the PCB. The chip is mounted at the bottom of the probe, which is submerged in the liquid helium dewar. In addition, the probe allows for shining a laser on the chip through an optical fiber and applying an external magnetic field, generated by a coil at the probe tip. The probe's mechanical diagram is taken from [55].

are 5 memory cells (two with 60 nH inductances and the remaining three with 40 nH, 20 nH, and 5 nH), 2 OR gates (60 nH and 40 nH), 2 NOR gates (both with a 20 nH inductor) and a 20 nH NOR gate. A D flip-flop, made of two 60 nH memory cells, was characterized too.

Chapter 3

Results

In this section, the experimental results of the building blocks are presented. The discussion is divided into different sections, one for each of the circuits. First, the memory cell measurements are shown, followed by the ones of the OR gate, the NOT gate, the NOR gate, and finally, the D flip-flop. For the memory cell, further analysis has been performed regarding the variation of operating point margins at different frequencies, under the effect of a magnetic field and for decreasing values of kinetic inductance.

3.1 Memory cell

The first device that was characterized is the memory cell. A thorough analysis of this elementary cell gives insights into all the other single-cell devices, which share with it a great part of their structure.

Fig. 3.1 shows the voltage versus time traces measured from a memory cell with a 40 nH kinetic inductor. As can be noticed from the plot, the cell is read multiple times while in "0", leaving the state unaltered and producing no output. After the third read pulse, a signal is injected at the input, changing the state of the cell to "1". When the cell is read by the successive pulse sent to the READ terminal, an output spike is generated, and the cell is set back to "0". When the cell is read again no output is produced. The behavior is analogous to the one obtained with the corresponding SPICE simulation shown in the previous chapter in Fig. 2.9. The presence of a significant delay between the read pulse and the related output signal comes from the connections between the device and the room temperature setup. Indeed, as it will be shown in the following subsection, the device operation is not affected by this time interval, and it can be operated with a period shorter than this delay.

As stated previously, multiple devices have been tested with different values of kinetic inductance, the critical element of the circuit. In Fig. 3.2, the traces related to a smaller device are reported. In particular, this cell includes a kinetic inductor of

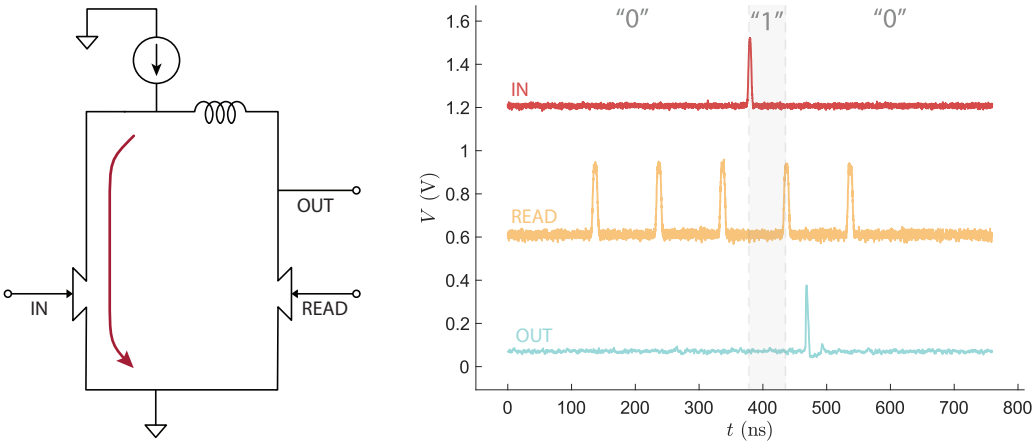

Figure 3.1: Experimental voltage versus time traces of a memory cell with a 40 nH inductor. On the left, the cell schematic is shown. On the right, the three main signals' traces of the cell are plotted. Specifically, the input (IN), the read signal (READ), and the output (OUT). In the operation cycle in the figure, the cell, while in the zero-state is read three times, and no output is produced. An input pulse is injected into the cell, switching the state to "1". When the fourth read spike arrives, the cell produces an output spike, and the state is reset to "0". If the cell is read again, by the fifth and last read signal, no output is produced.

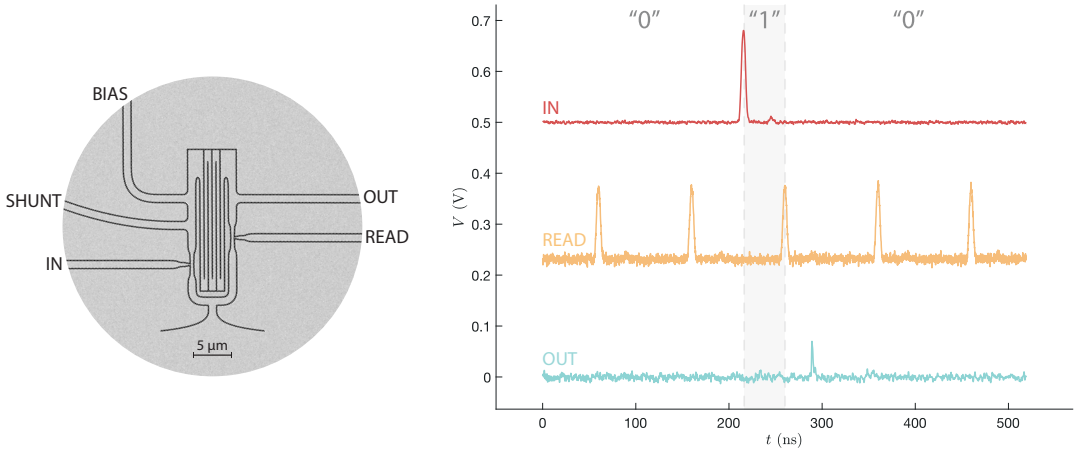

Figure 3.2: Experimental voltage versus time traces of a memory cell with a 5 nH inductor. On the left, a scanning electron micrograph of the memory cell is displayed. The plot on the right shows the memory operation cycle described in Fig. 3.1. In this case, the output signal appears to be smaller due to the lower output impedance of the cell.

5 nH, the lowest value among the cells fabricated and tested. The plot on the right of the figure shows the same memory operation discussed previously.

The graph shows that the cell works properly, analogously to the one with a 40 nH. Notwithstanding, the output signal appears to be smaller. The values reported in the plot are directly acquired from the experimental setup. Therefore, due to amplification and filtering, the output collected could be slightly distorted. Anyway, it is reasonable to think that the output signal generated by a cell containing a smaller kinetic inductance has a lower peak voltage. This decrease in the output signal voltage can be attributed to the smaller output impedance. The intensity of the output voltage does not directly affect the functioning of a single cell but could limit its applicability in a multi-cell system. In fact, a weaker output signal corresponds to a lower current injected into the input nTrons of the following cell. If the current is not high enough, the formation of a hotspot in the nanocryotron's choke could be inhibited, causing a fault in the transmission of the signal between the cells. To inject a larger amount of current the connection resistance could be decreased. Nevertheless, the electrical time constant would be decreased, slowing down the cell, thus resulting again in a trade-off between the device area and speed.

3.1.1 Operating point versus frequency

The operating conditions of the memory cell have been characterized to study its robustness against noise and variations in the bias and input (and read) currents. First of all, the analysis has been performed increasing the frequency of operation. Fig. 3.3 displays the bit error rate (BER) at different bias points (i.e., pairs of input

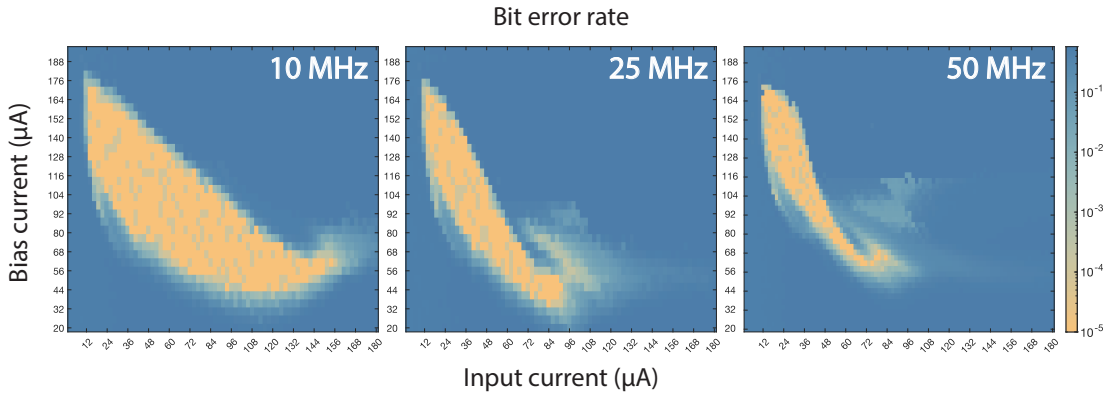

Figure 3.3: Cell bit error rate in logarithmic scale versus operating point currents at 10 MHz, 25 MHz, and 50 MHz. As it is possible to notice, the area of the valid operating point for bias and input currents shrinks with the increase of frequency. The correct functioning region does not narrow evenly but instead gets compressed to the left side of the plot. Each operating point was tested on 10^4 pseudorandomly generated bits.

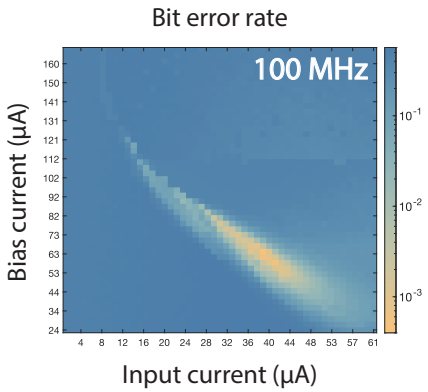

Figure 3.4: Cell bit error rate in logarithmic scale versus operating point currents at 100 MHz. Although a region of correct functioning can still be identified at this frequency, the margins on the operating point narrow significantly. Again, each operating point was tested on 10^4 bits.

and bias currents). This measurement has been performed equivalently at three different frequencies: 10 MHz, 25 MHz, and 50 MHz. Each bias point has been tested on a stream of 10^4 pseudorandomly generated bits. At first glance, it is possible to notice the shrinking of the yellow area corresponding to the correct functioning (characterized by low BER values) of the device with the increase in frequency. In particular, the margins at 10 MHz (around 50% for input currents and 40% for the bias current at the center of the area) decrease unevenly at 50 MHz. At high frequencies, the margins on the inputs current significantly decrease. This is not the case for the margins on the bias current, which are just slightly altered at the different frequencies.

The causes for the malfunctioning of the system are different. In the bottom left corner, the device is under-biased, and the currents are not sufficient to cause switching events, necessary for the operation of the cell. Conversely, the top right corner is characterized by the occurrence of latching. In this region, the nanocryotrons get stuck in the normal state, preventing proper operation. It is interesting to notice the transitions from under-biasing, to correct functioning, and then latching. The transition from correct functioning to latching is abrupt since the occurrence of this phenomenon causes the cell to fail multiple times, while stuck in this condition. Inside the correct functioning area, some single errors are found. These errors are attributed to external noise injected by the room temperature setup.

As shown, increasing the frequency decreases the operating point margins. When the frequency is raised up to 100 MHz the device can still be operated, but with very limited margins. The BER at this frequency versus the operating point is shown in Fig. 3.4.

3.1.2 Operating point versus magnetic field

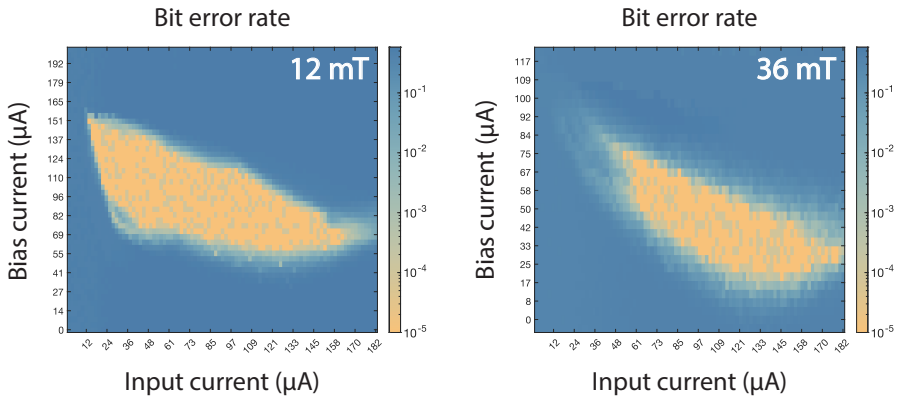

Figure 3.5: Cell bit error rate in logarithmic scale versus operating point currents when applying a magnetic field of 12 mT, and 36 mT. The application of a magnetic field influences the operation of the devices. In the plot on the left a magnetic field of 12 mT is applied. At this intensity, the operating point area does not shrink significantly. On the right, with a different scale, the bit error rate at 36 mT is shown. Under the effect of such a magnetic field, the device still operates correctly, with a moderate decrease in the operating point margins. Each operating point was tested on 10^4 pseudorandomly generated bits at 10 MHz.

In the presence of stray magnetic fields in the order of tens of µT, the superconducting technologies based on Josephson junctions fail [56, 57]. Therefore, the operation of such technologies needs proper magnetic shielding and careful design to avoid internal fields. The nanocryotron working principle is not directly influenced by the presence of a magnetic field. The robustness against high fields could be a valuable property for the application of the cells proposed in this work. For this purpose, the BER bias margin variation under the effect of a magnetic field was evaluated. The external field was applied using the coil included in the RF probe. More information on the field application can be found in [55].

The results of the analysis are reported in Fig. 3.5. The two plots show that the devices can be operated both under a magnetic field of 12 mT and 36 mT. At the lower magnetic field intensity (left plot), the bias margins are essentially unaltered from the case without the application of a field. When the 36 mT field is applied, the device can still be operated properly, but with a smaller low-BER area (the scale of the two plots is different). The analysis was performed at 10 MHz on 10^4 pseudorandomly generated bits.

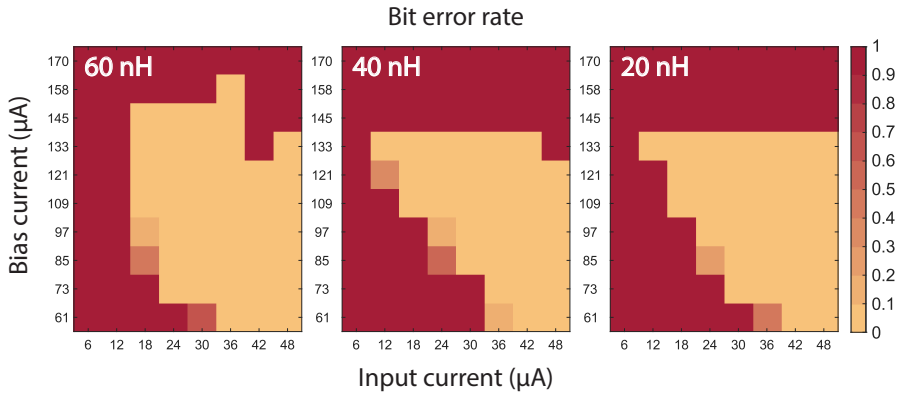

Figure 3.6: Preliminary results of cell bit error rate in linear scale versus operating point currents for kinetic inductors of 60 nH, 40 nH, and 20 nH. In the plots, from left to right, the inductor size decreases. In the limited range analyzed, the variation of margins appears to be small with the inductance. Each operating point was tested on 10^2 bits at 10 MHz.

3.1.3 Operating point versus kinetic inductance

As discussed previously, the kinetic inductor included in the memory cell plays a crucial role in the device's functioning. Some preliminary data were collected regarding the bit error rate at different operating points for cells with different kinetic inductors. Fig. 3.6 displays the bit error rate versus input and bias currents for three values of kinetic inductance, 60 nH, 40 nH, and 20 nH. Each operating point was tested on one hundred bits. Given the modest number of test bits, the BER is displayed on a linear scale.

Although the smaller range taken into account, the correct functioning area in the operating point space is fairly consistent for the three values of kinetic inductance. Having a weak dependence between the correct operating points and the inductor size can be useful. Specifically, a similar dependence is promising both for the robustness against the fabrication variability (which can lead to different sheet inductances) and for the scaling down of the device. The correct functioning of devices with inductor sizes lower than 60 nH was not possible due to the occurrence of latching, according to the SPICE simulations. The invariance of the correct operation areas displayed in the plots suggests that latching does not represent a tight constraint for the device's functioning.

3.2 OR gate

The second device that was experimentally measured was the OR gate. All four input configurations were tested. The different configurations' signals are reported in the graphs of Fig. 3.7 and Fig. 3.8. In the plot on the right of Fig. 3.7, the experimental

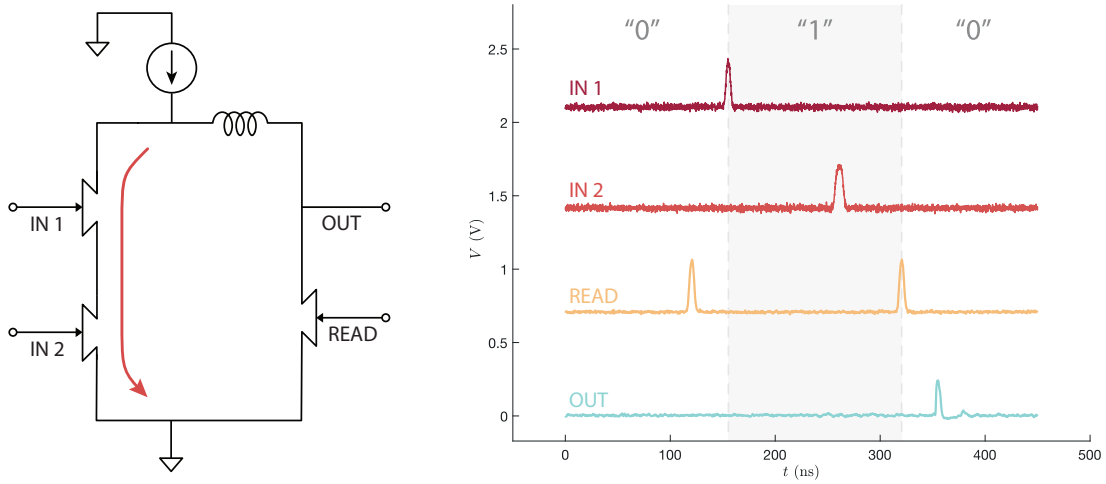

Figure 3.7: Experimental voltage versus time traces of an OR gate with a 40 nH inductor, for "00" and "11" input configurations. On the left, the schematic of the OR gate is shown. On the right, the traces of the main signals of the gate are plotted, the two inputs (IN 1 and IN 2), the read signal (READ), and the output (OUT). In the first part of the right graph, no input arrives before the read signal. When the cell is read, no output spike is generated. Before the second read signal arrival, both of the inputs receive a spike. The first arrived spike switches the state of the cell from "0" to "1". When the gate is read, a spike is produced, and the cell is reset as intended. The two above-mentioned cases correspond to the "00" and "11" input cases for the OR gate, which output "0" and "1", respectively.

voltage traces collected when measuring an OR gate with a 40 nH inductor are shown. As can be noticed from the figure, when the first read pulse arrives, no input has been injected into the gate, and thus no output is generated. Then, an input spike occurs. The state is switched to "1". When a second pulse is injected into the other input the state remains unaltered. The reading of the cell produces an output spike while resetting the gate. The other two input configurations ("10" and "01") of the OR gate are shown in the plot of Fig. 3.8. This graph illustrates that the arrival of one or the other input switches the gate state to "1". When the cell is read, an output spike is produced.

The schematic in Fig. 3.7 and the micrograph in Fig. 3.8 show that the structure of the circuit is the same as the memory cell one. From the micrograph, it can be appreciated the minor overhead in the device's area when another input is introduced. The possibility of increasing the number of inputs of the device and the related advantages are discussed in the next chapter.

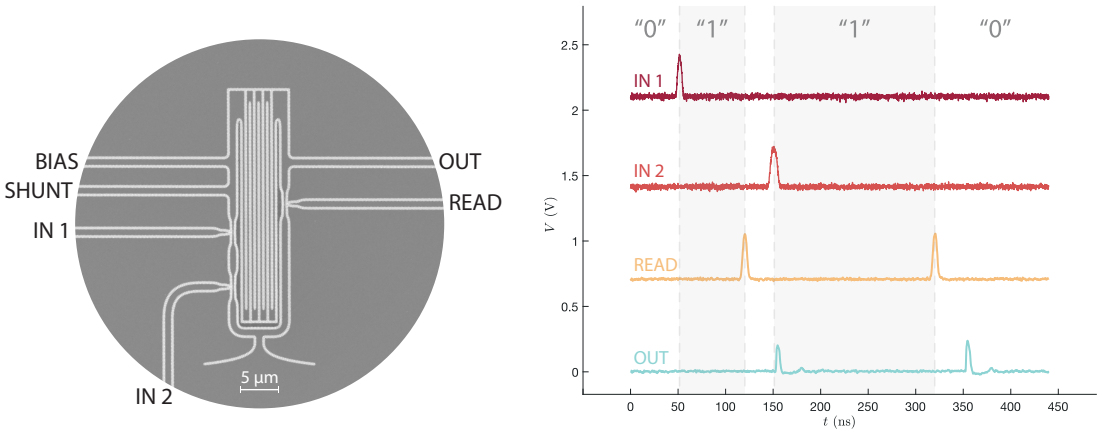

Figure 3.8: Experimental voltage versus time traces of an OR gate with a 40 nH inductor, for "10" and "01" input configurations. The scanning electron micrograph on the left shows an OR gate with a 20 nH inductor. In the plot on the right, the signals' traces are displayed. In this case, before each of the two read pulses, a spike arrives at one or the other input. Thus, both readings of the cell produce an output signal. These cases correspond to the "10" and "01" input cases for the OR gate, which both output "1".

3.3 NOT gate

An OR gate does not constitute a set of functionally complete logic gates if not complemented with inverting operations. Therefore, the development of a NOT gate was crucial for the logic family proposed in this work. As mentioned in the design section (Sec. 2.1), operating the cell as inverting gate requires a reset terminal (RST). This additional element has an impact mainly on the timing of the device, which needs to be reset before every cycle of operation.

In Fig. 3.9 the schematic and corresponding experimental voltage versus time traces of the NOT gate (with a 20 nH kinetic inductor) are reported. The cycle of operation of the plot shows the NOT gate receiving no input, thus generating a spike at the output terminal. In particular, the reset signal is sent, setting up the cell to the one-state. This state is read, producing an output since no input pulse switches the cell back to "0". Differently, in the plot of Fig. 3.10, an input signal is injected after the reset, switching the state to "0" before the read signal arrival. No output signal is generated in this case. Placing the input nTron above the OUT terminal prevents the output voltage to rise when an input pulse is injected. In this case, the hotspot is generated at the IN nTron, while the output is kept at zero voltage by the superconducting path to ground. Therefore, when the input spike arrives at the IN terminal, the state is switched, but no unwanted pulse is generated at the output.

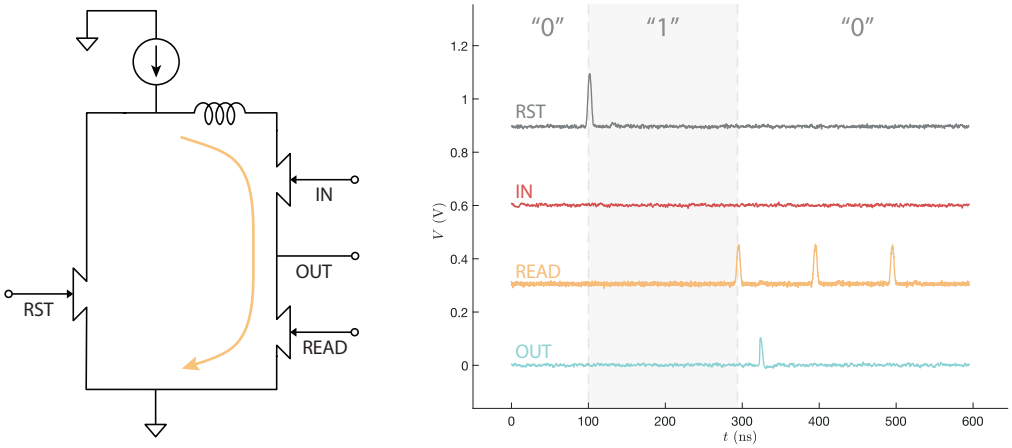

Figure 3.9: Experimental voltage versus time traces of a NOT gate with a 20 nH inductor when no spike is injected at the input ("0"). On the left, the schematic of the NOT gate is shown. On the right, the traces of the signals are plotted. To make inverted functions the cell has to be reset to the one-state, by sending a pulse at the RST terminal. In this case, no input spike arrives, then when the cell is read an output spike is produced, and the gate is set to the zero-state.

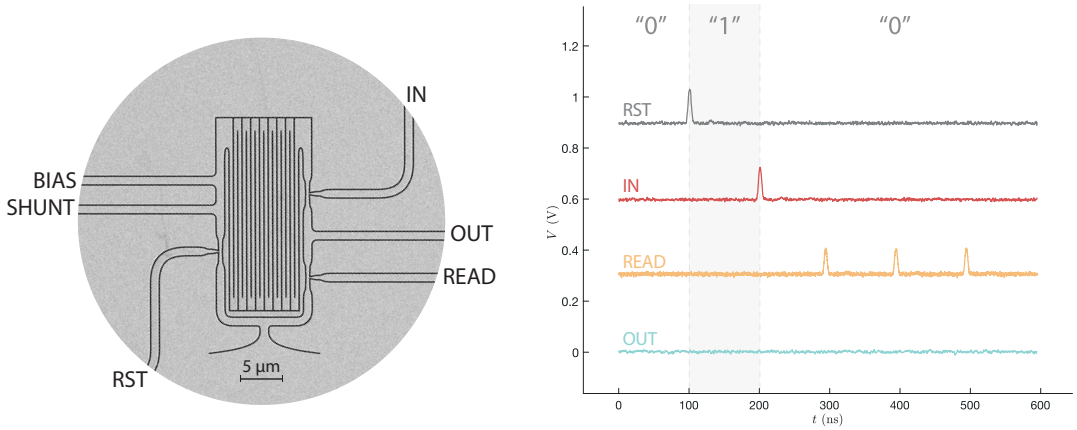

Figure 3.10: Experimental voltage versus time traces of a NOT gate with a 20 nH inductor when a spike is injected at the input ("1"). The figure is composed of a scanning electron micrograph of the circuit and a plot of the signals traces. In this case, in the plot, after the cell is reset to the one-state, an input signal arrives. This spike does not produce any output pulse while switching the state to "0". The reading does not generate any output signal.

3.4 NOR gate

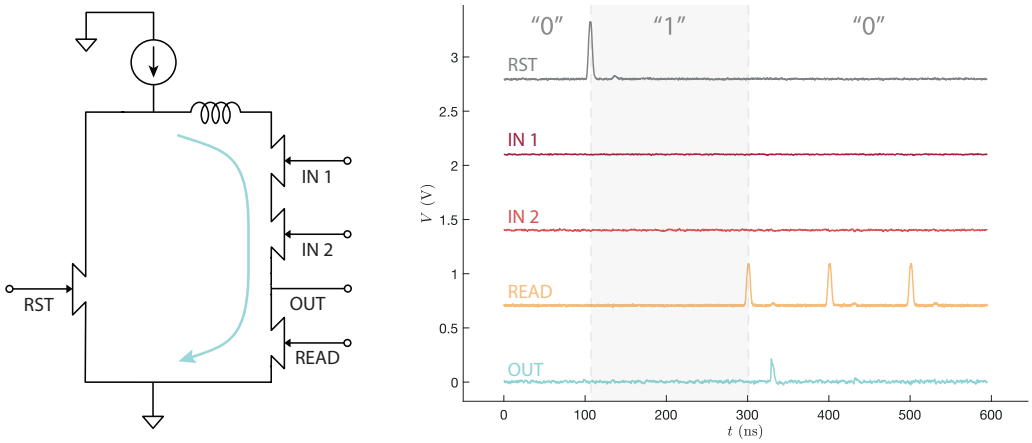

Figure 3.11: Experimental voltage versus time traces of a NOR gate with a 20 nH inductor when no spike is injected at any input ("00"). On the left, the schematic of the NOR gate is shown. On the right, the traces of the signals are plotted. As for the NOT gate, the cell is reset to the one-state by sending a pulse at the RST terminal. In this case, no input signals arrive at both terminals IN 1 and IN 2. Therefore, the one-state of the cell is preserved until the reading occurs, which produces an output spike and sets the cell back to "0".

The last single-cell gate that was characterized is the two-input NOR. The working principle of this gate is similar to the one of the NOT gate, but in this case, two inputs (IN 1 and IN 2) are placed in the right branch. The corresponding schematic is illustrated on the left of Fig. 3.11.

Analogously to what has been shown for the other logic gates, the traces of the different input configurations are displayed in Fig. 3.11 and Fig. 3.12. In the first figure, the plot shows the "00" input configuration. That is when no spike is injected in IN 1 and IN 2. As it was for the NOT gate, the cell is previously set to "1" by the reset signal. The absence of any input arrivals preserves the one-state until the reading, which thus produces an output spike.

On the contrary, when one or the other input arrives, the state is set back to "0", producing no output. The traces corresponding to these configurations are reported in Fig. 3.12. In both cases, after the reset pulse, an input spike is injected at the terminal IN 1. This input generates a hotspot in the right branch, above the output terminal, moving the bias current back to the left branch. Thus the cell is switched to the zero-state. When the device is read no output pulse is produced. In the right plot of the figure, another input signal arrives at the IN 2 terminal ("11" input configuration). This pulse leaves the state of the cell unaltered, leading to the same result when the device is read. The experimental results prove the correct functioning

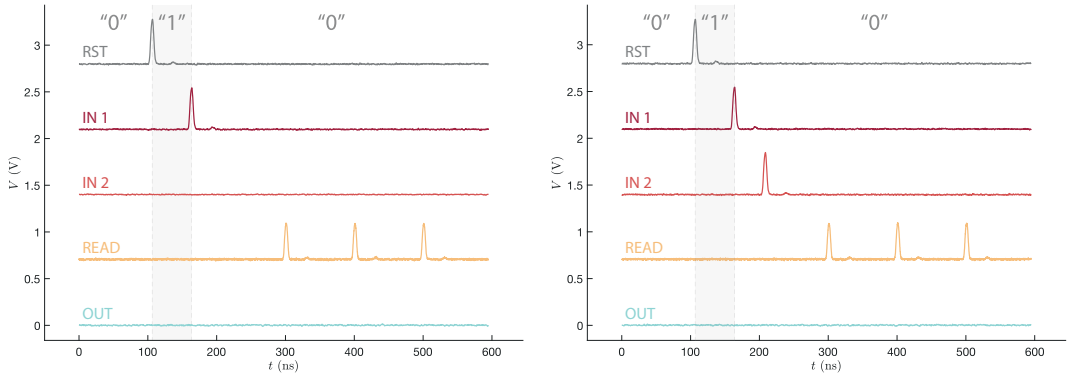

Figure 3.12: Experimental voltage versus time traces of a NOR gate with a 20 nH inductor when one or two spikes are injected at the inputs ("10" and "11"). In the plot on the left, after the reset of the cell, an input pulse arrives at the IN 1 terminal. This pulse switches the cell back to "0". When the cell is read, no current is flowing in the right branch, and no output spike is generated. In the plot on the right, the situation is similar. After the IN 1 pulse, a spike is injected at the IN 2 terminal. This second pulse does not affect the state of the cell (already in "0"). Therefore, in this case, no output is produced too.

of the logic gate for all the possible input configurations. The experimental results of the NOR gate were the last data, regarding a single cell, to be presented. The following section shows the experimental proof of the connections of two cells.

3.5 Flip-flop

Any standard cell of a system needs to be easily combined with the other building blocks. Therefore, the connection of multiple cells is a crucial demonstration for the future application of the devices in larger circuits. In this section, the experimental results regarding the connection of two memory cells are shown. As discussed in subsection 2.1.4, the out-of-phase reading of two connected memory cells produces an equivalent D flip-flop.

The experimental voltage traces of the flip-flop's signals are illustrated in the plot of Fig. 3.13. The slight increase in complexity makes it harder to follow the device evolution directly. Until no input has reached the flip-flop, the reading of one or the other cell produces no changes to the device. When an input signal is injected, the digital "1" is sampled by the first cell, which switches its state. The state of the two cells is now "10". When a clock pulse arrives at the CLK terminal the "1" is moved to the second cell (state "01"). This change happens when the output pulse of the first cell (OUT 1 signal) reaches the input nanocryotron of the second cell, generating a hotspot and diverting the current to the other branch. The state is

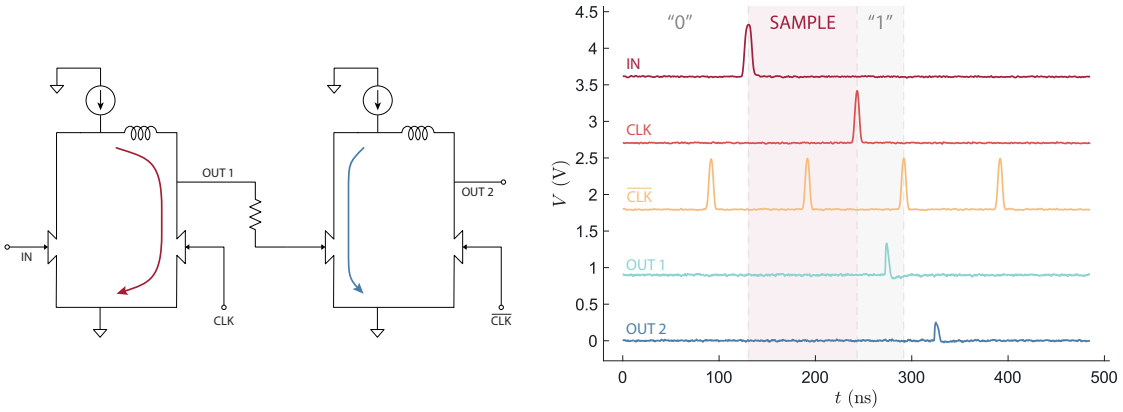

Figure 3.13: Experimental voltage versus time traces of a D flip-flop with a 60 nH inductor. On the left, the schematic of the DFF is shown. On the right, the main signals' traces of the device are plotted. In particular, the input (IN), the two clock signals (CLK and $\overline{\text{CLK}}$), and the first and second cells' outputs (OUT 1 and OUT 2). As long as no input is stored if the second cell is read ($\overline{\text{CLK}}$) no output is produced. When a signal arrives at the IN terminal, the input gets sampled and switches the first cell to "1" (this case is shown in the schematic on the left). When the first cell is read by a clock signal (CLK), the "1" is shifted to the second cell, while the first one is reset to "0". An OUT 1 spike is produced. When the second cell is read by a $\overline{\text{CLK}}$ signal, the cell is reset, and a pulse is generated at the output of the flip-flop.

stored in the second cell, the first cell is able to sample the input again. If the second clock pulse is sent, at the $\overline{\text{CLK}}$ terminal, the second cell is reset, and an output (at OUT 2) spike is generated.

Although the device is working properly, the output peak voltage of the second cell appears to be smaller than the one of the first. The two signals come from different nodes of the circuit and are collected at the scope through diverse amplifiers and cables. Nevertheless, the reduction of the signal intensity along a chain of cells could be concerning for the design of a larger scale system. Anyway, the first output signal was able to fire the following nTron, granting the proper operation of the DFF. A decrease in signal intensity could be remedied by adding an nTron amplifying stage between successive cells.

Chapter 4

Discussion

The experimental results proved the devices' operation and robustness. In the following, the characteristics and possible applications of the devices are examined. First, the figures of merit of the cells are analyzed to frame them in the context of low-temperature electronics. Starting from the properties of the device, some potential applications of this technology are proposed. Lastly, possible future developments of the devices are outlined, focusing on circuit and system scaling.

4.1 Figures of merit

To properly evaluate the logic family proposed in this work, it is necessary to consider its performance with respect to standard quantities. Fig. 4.1 summarizes some of the key parameters determined during the measurements.

The first parameter that has been considered is the area footprint of the cell. The device's area directly affects the number of cells that can be fabricated on a chip, limiting the complexity of a system. The downscaling from the first to the final layout, shown in section 2.3, allowed for shrinking the memory's area up to about $100\,\mu m^2$, resulting in a cell smaller than the equivalent RSFQ SR latch [12]. The difference in area between the two technologies increases when the logic gates are compared, particularly when the fan-in is increased. Thanks to the robustness against magnetic fields, the vertical stacking of these devices looks feasible. A similar 3D integration could increase the chip's density and the complexity of the system. Moreover, it is worth noticing how the total area is divided among the various electronic components. In particular, a large part of the area is occupied by the kinetic inductor and the routing, while the nanocryotrons themselves cover a very limited area, having a choke width of 30 nm and the main channel width equal to 300 nm. The small size of the core component of the cell allows for hypothesizing a possible further scaling.

During the characterization of the cells, a lower bound on the memory data retention has been set. The input and read pulse were performed at a temporal

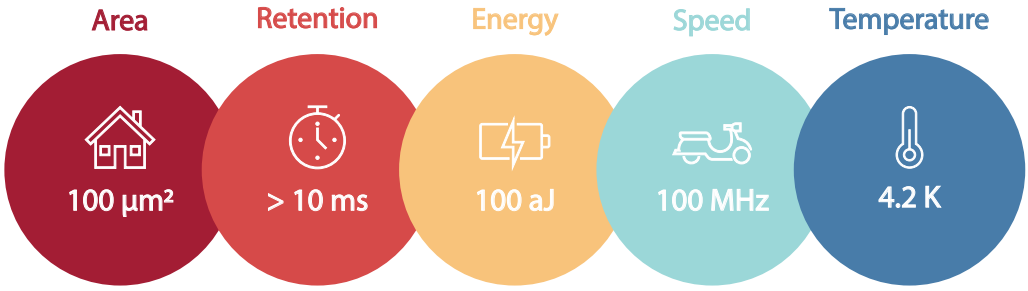

Figure 4.1: Summary of circuits figures of merit. In the diagram are reported the parameters of the final cell design, such as chip area per device, data retention of the current in the loop, energy per operation performed, maximum frequency, and operating temperature.

distance of 10 ms, the maximum value given the experimental setup. As mentioned, the information is stored in the persistent current of the superconducting loop. The same phenomenon is exploited in the RSFQ flip-flop and in the nanocryotron memory. Therefore, the maximum data retention time can be considered of the same order of magnitude, compared to these technologies, or even larger due to the higher kinetic inductance and the greater value of persistent current stored.

An essential parameter to evaluate a device's performance is the energetic cost per operation. In this work, the *operation* consists of both writing and reading a zero "1". During each of the procedures, the energy is dissipated during a single switching of the nanocryotron channel. The power consumption during each switching event depends quadratically on the bias current and linearly on the equivalent resistance. The equivalent resistance is determined by the parallel of the 50 Ω shunt resistor and the hotspot resistance. Due to its non-linearity, the hotspot resistance is hard to determine. However, an upper bound on the energy can be easily obtained considering the spikes as square pulses of 5 ns and power equal to the square of the bias current times the equivalent resistance, which is roughly approximated to the shunt resistor value. This estimation, depending on the bias current, results in an energy per operation that belongs to the range from 100 aJ to 1 fJ. This range of energy per operation places the cells bewteen CMOS and RSFQ. The first has an energetic consumption one order of magnitude higher than the cells proposed in this work, while RSFQ consumption is lower than both (about one order of magnitude from the cells) [12].

Albeit the power consumption of the cells might be decreased with the scaling, a different analysis is needed in the study of the device's maximum speed. The circuits presented in this work were successfully tested up to 100 MHz. The speed of the cells is limited by the speed of the nanocryotrons. Unlike the Josephson junction, which operation is based on Cooper pairs tunneling, the nanocryotron works by generating a hotspot in the main channel of the device. The latter is an electro-thermal process

fundamentally slower than the Cooper pairs tunneling. In particular, as discussed in section 1.2, the transitions from superconducting to normal and vice versa have different speeds, with a larger fall time compared to the rise one. The transitions' asymmetry causes the speed of the device to depend mainly on the recovery of the superconducting state once a hotspot is generated. Downscaling of the devices would result in a smaller thermal time constant. Shrinking this parameter would allow for decreasing the electrical time constant without running into latching phenomena, thus making faster devices, possibly up to several hundreds of megahertz.

The last figure of merit that was included in Fig. 4.1 is the operating temperature. The circuits can operate in liquid helium at 4.2 K, without strictly needing a cryocooler. In this work, the possibility of directly measuring the chips in liquid helium allowed for saving time, avoiding any cryocooler cooldown or warmup.

Some interesting properties of the designed cells are harder to fit into standard figures of merit. These characteristics are related to the simplicity of the geometry, its modularity, and the robustness of the device, and they could be leveraged to transition from a few cells to larger systems. Specifically, the possibility of making the circuits out of a single superconducting thin film could improve the yield of the fabrication process. The chip yield could benefit from the modularity and configurability of the cells too: the regularity in the different circuits could ease the optimization of the fabrication process. Lastly, the robustness of the devices to magnetic fields and noises on the operational currents could extend the correct functioning of the single cell to larger systems. All of these properties are crucial for determining the possible applications.

4.2 Applications

The characteristics of the cells proposed in this work make them suitable for diverse applications, either integrating them with other technologies or in standalone systems. As previously mentioned, the nanocryotron has been coupled with different devices. In particular, since its development, the nTron was devised to be integrated with superconducting nanowire single-photon detectors. The two technologies have similar fabrication processes, operating conditions, and maximum frequency of operation. These conditions suggest that the cells could be employed as building blocks for elementary control and readout of an SNSPD-based detector. Performing logic operations at the detector level would result in faster systems that do not need to exchange data and control signals across the cryostat. Other technologies had been employed for this purpose [58] but without any monolithic integration of detectors and electronics, which would enhance the scaling. The direct integration with SNSPDs could be the most interesting application for the developed devices.

These devices can be used as a standalone technology too. A field that could benefit from an nTron-based system could be deep space exploration. The robustness of the device's functioning and structure could allow for radiation-tolerant operation,

which is necessary for such an environment. Josephson junction-based technologies have also been shown capable of operation when irradiated [59]. However, radiation damages to the thin oxide barrier of the JJs can cause the device to fail. The absence of this fragile part of the device would probably favor the reliability of nTrons compared to the one of Josephson junctions. Additionally, deep space exploration requires small energetic costs per operation. Superconducting electronics can provide a platform for low-power computing but requires working at cryogenic temperatures. These temperatures can be reached more easily in deep space, where the system can be passively cooled down to tens of kelvins and actively at the nTrons operating temperatures, as reported in the study for the Origins Space Telescope [60]. Nevertheless, moving from the single cells to a complete nTron-based system requires further development of the devices and the choice of an adequate architecture.

4.3 Future work

The employment of the circuits in a large-scale system needs a more profound analysis of the capabilities of the circuits, specifically concerning the connection of multiple cells. A similar short-term examination would strengthen the choice of the cells as building blocks for the fabrication of reliable multi-cell devices. Once the robustness of the building blocks has been further proven, the research should focus on the scaling of the system. In this section, an outline of the longer-term possible work to be performed on the cells is proposed. Two complementary directions are taken into account. First, the scaling down of the devices will be discussed. The advantages of shrinking the size of the circuits will be considered. The corresponding limitations will be highlighted too. Successively, some observations on the development of larger systems employing the cells are made. The composition of these systems will be related to traditional electronic structures, and then to an alternative choice of architecture.

4.3.1 Scaling down

The employment of the technology proposed in this work in larger systems would need to scale down the device's size. The shrinking of these devices is mainly impeded by the need to have high kinetic inductances inside the loop to function. However, decreasing the width of the nanowires composing the cells could mitigate the problem. Indeed, narrower wires of constant length exhibit higher inductance values, since they are composed of more squares. Narrower wires could also be slightly faster since the hotspots to be recovered would be smaller in size. In addition, the power consumption of the devices would benefit from scaling. Since the critical current of a nanowire depends on its cross-section, smaller nanowires would work with lower currents, decreasing the energy dissipated in the switching events.

The advantages arising from scaling down are partially balanced by some minor

drawbacks, specifically regarding the lower operating currents of the circuits. The decrease of currents' intensity, would affect the pulses sent from one cell to the other. For instance, this decrease could limit the devices' fan-out. Moreover, the critical current of nTrons chokes, which defines the threshold current corresponding to a digital "1", would decrease accordingly. A device with a lower threshold current is more susceptible to the noise. Therefore, the scaling of the devices could cause the bit error rate to increase at the margins of the correct operation area, decreasing the cell robustness.

4.3.2 Building up

Shrinking the size of the devices could enhance the integration of a larger number of cells. Larger-scale integration requires the study of multi-cell structures that operate more complex functions. Some future work should be oriented toward the analysis of structures that benefit the most from the properties of the cells.

One of the most interesting properties of the cells is surely the negligible overhead in area and speed of high fan-in gates. The inductor size of two-input and multi-input gates is roughly the same, and this makes increasing the number of inputs favorable. High fan-in gates can enhance two-level logic synthesis. This kind of structure is composed of two levels of logic gates between inputs and outputs. Every logic function can be synthesized with this approach [47]. Moreover, this approach allows for having the lower possible number of gates from inputs to outputs, decreasing the latency.

Fig. 4.2 illustrates a possible hardware implementation of the two-level logic. The system depicted is a half adder, where A e B are the inputs, S is the sum (the XOR of the inputs), and C is the carry (the AND of the inputs). The whole circuit is composed of three different logic planes: a first one made of buffers and inverters and two NOR planes. The logic levels are wired together by a crossbar array, analogously to the one found in programmable logic arrays. This implementation shows some differences from CMOS two-level synthesis implementation. First, the two logic planes of the system are made of NOR gates. This is not usually the case for CMOS technology, in which NAND gates are preferred for speed reasons [46]. Nevertheless, the main difference lies in how the gates operate. CMOS logic gates are combinatorial elements, while the cells presented in this work exhibit a sequential behavior. The difference arises in the need to read (and reset) the designed gates when operated. The distribution of these signals can be done efficiently by sharing the controls among the three levels of cells. This distribution of signals results in a pipelined system in which every cell is reset (RST), then receives the inputs (IN), and it is finally read (READ), as shown in the top-right corner of Fig. 4.2. In the bottom plot of the same figure, the spiking signals are shown. The three out-of-phase pulse trains, corresponds to the three times of operation of the cells RST, IN, and READ. These times are interleaved in the pipeline: when a cell is read, the following plane receives the outputs.

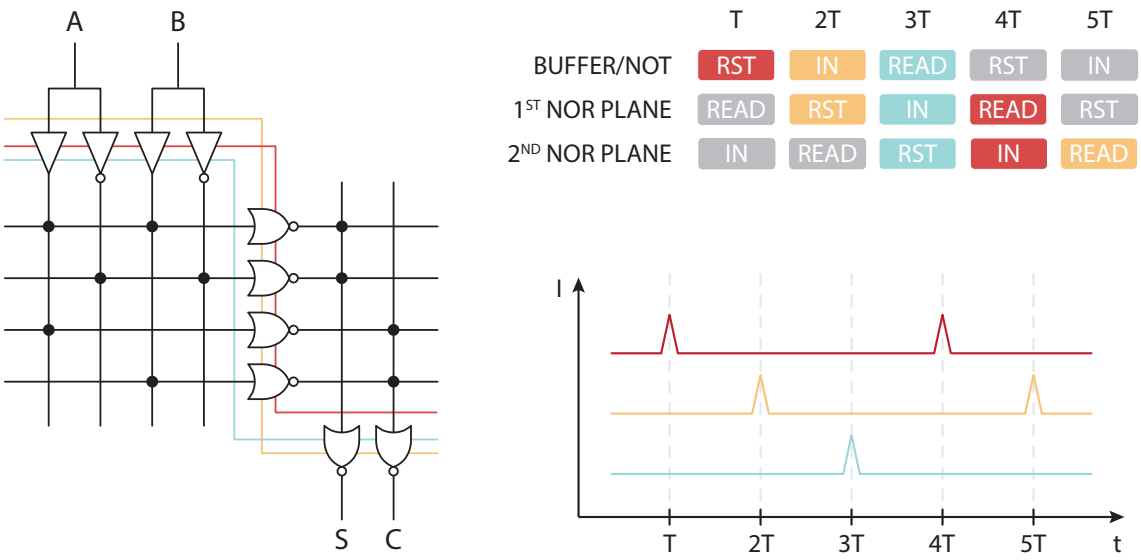

Figure 4.2: NOR-NOR plane implementation of a half adder. The structure is composed of three layers: the first layer of buffers and inverters and the two NOR planes. The control signals of the levels can be made out of three phases of spike trains, shown in the bottom right plot. The controls are pipelined, performing for every level resetting (RST), idling when waiting for the inputs (IN), and reading of the cell (READ), as shown in the top-right corner.

Distributing the control signals, such as the system clock, is challenging in superconducting electronics. Many strategies have been proposed. An example is a recent work on a resonator based on a metamaterial transmission line for clock distribution [61]. Nanocryotrons allow for distributing signals with equivalent clock trees with nTrons as buffers. However, large area and complexity overheads originate from these signal distributions. Alternative logic families, such as race logic in temporal computing [62], could help reduce the number of control lines per gate. Some of the race logic gates can be straightforwardly implemented with the proposed cells. Such a computing frame could better suit the technology.

The last problem that should be addressed in future works regards circuits' biasing. In CMOS technology, the cells are powered by a voltage source. The biasing is achieved by connecting all the standard cells in parallel between the power rails and the ground. Superconducting electronics typically need to be biased in current instead of voltage. Biasing all the cells in parallel starting from a single current source is inconvenient since it would need to send to the system an intense current. Injecting large amounts of current from outside the cryostat can result in static power dissipation [63] and a higher heat load due to ohmic losses [64].

A more reasonable way to power these circuits would be biasing them in series [64].

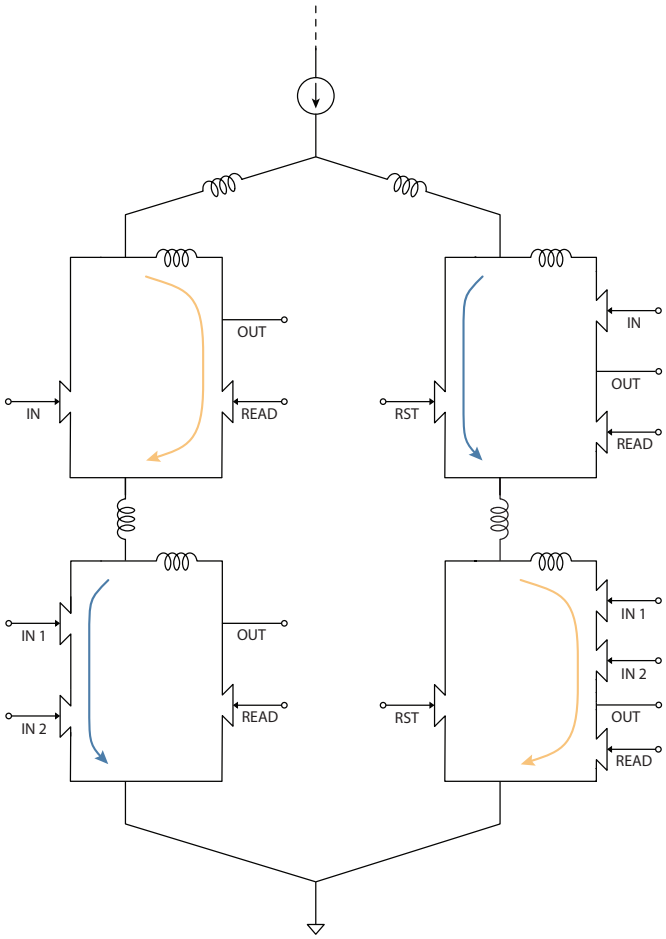

Figure 4.3: Simplified scheme for series-parallel biasing. Current biasing can be performed in parallel, splitting resistively or inductively a single current source. The cells could be also biased in series to reduce the total bias current sent to the cryostat and the cables' ohmic heating.

In this manner, the same current can bias more cells, decreasing the total current to be sent to the cryostat. In the specific case of the cells proposed in this work, SPICE simulations have been successfully performed for two cells biased in series. However, the current injected at the gate terminals of the cells' inputs and the transient voltage spikes generated could result in cross-talks between cells biased in series. To mitigate the propagation of these unwanted signals, high-valued kinetic inductors can be inserted between the cells. A hybrid biasing, having parallel strings of cells biased in series, could limit the cross-talks and avoid injecting into the cryostat too large currents. A simplified scheme for this hybrid biasing is shown in Fig. 4.3.

Conclusion

This work proposed and demonstrated the operation of a set of building blocks for digital logic based on nanocryotrons. Starting from the concept of a destructive readout memory cell, a functionally complete set of gates was designed and implemented. The implementation choices were made to fulfill the requirements of a reliable standard cell (such as no static power consumption and compatible input and output signals), making use of some of the valuable properties of the superconducting components, such as the spiking behavior of the nTrons and the possibility of storing information in a loop. The same structure has been used to implement a set of logic functions by just arranging the position of the input nanocryotrons.

The devices were fabricated using a single superconducting layer that was deposited by sputtering, patterned with electron beam lithography, and finally etched by means of reactive ion etching. The chips were measured at a temperature of 4.2 K employing a probe submerged in liquid helium.

The correct functioning of all cells has been experimentally demonstrated. An equivalent D flip-flop was experimentally proven too, by connecting two memory cells. This demonstration paved the way for the design of multi-cell devices. The memory cell has been characterized by taking into account the operating point margins against variations in the bias and input currents. The bias margins have been tested for increasing frequencies and also under the effect of an external magnetic field. A shrink of the area in the operating point space was encountered for higher frequencies and more intense magnetic fields. In particular, the possibility of operating the device under high magnetic fields represents one of the main advantages compared to other superconducting technologies.

The experimental work was necessary for determining the figures of merit of the devices. A discussion on these quantities has been presented, comparing the technology with CMOS and RSFQ. Regarding some of the figures of merit, the cells show advantages over one or the other existing technology. The main advantage of the devices, when compared to RSFQ, is the lower footprint area. Instead, regarding the energetic cost per operation, the technology has a lower consumption than the one of CMOS. Nevertheless, rapid single flux quantum has the best performance in terms of both power and speed. In addition, RSFQ and especially CMOS have a higher degree of maturity and dedicated infrastructure, which allows a designer to implement complex systems based on them. At the moment, the gap in maturity is

the main limit for the creation of nTron-based larger systems. The aim of this work is to reduce this gap.

Some possible applications for this technology have been proposed too. Leveraging either the inherent compatibility with SNSPDs for fabricating integrated detectors or the robustness of the operation for developing harsh-environment superconducting electronics. However, the horizon of large system integration based on such devices is still far. For this reason, some future works have been outlined too, underlining the need to shrink the size of the devices and discussing multi-cell structures that would benefit from the properties of these circuits (such as NOR-NOR planes logic and temporal computing).

In this work, a platform for combinatorial and sequential logic has been developed. The availability of this platform immediately offers the designers a set of devices to implement few-cells circuits. Moreover, it represents a step toward a standard design of nanocryotron-based circuits, which can enable all the applications that benefit from the compactness and robustness of these devices.

Appendix A

Thin film sheet resistance

When dealing with thin film resistances it is convenient to rely on the concept of sheet resistance $R_\square$. This quantity is defined by the ratio between the resistivity ρ and the thickness t of the film. Therefore, when a thin film is deposited, the sheet resistance is fixed. The value of patterned resistors on the same thin film will just depend on their geometrical shape. In particular, the essential geometrical parameter is the number of squares $N_\square$ that composes a microstrip (Fig. A.1), given by the ratio between the length L and the width W of the conductor. This relation can be derived from Ohm's law:

$$R = \frac{\rho}{t}\frac{L}{W} = R_\square\, N_\square$$

In this appendix, a proof for the formula (Eq. 2.1) used to derive a thin film sheet resistance from a four-point measurement is shown. The formula is the following:

$$R_\square = \frac{\pi}{\ln(2)}\frac{V}{I} \tag{A.1}$$

In the analysis made by Valdes [53], a general film case was taken into account. The formula for thin films was then obtained from the limit of infinitesimal film thickness. However, starting from the hypothesis of an infinitely thin film, Eq. A.1 can be

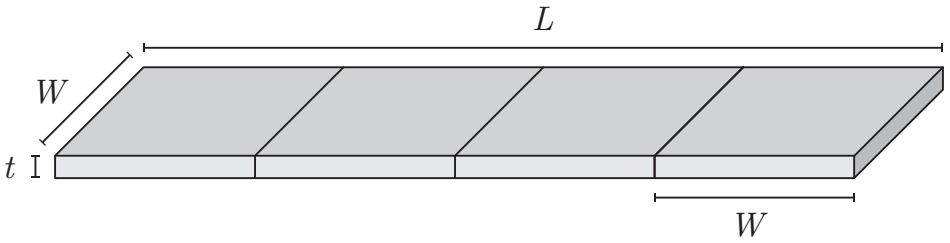

Figure A.1: Conductor strip with its geometrical dimensions. The conductor is composed of four squares (L/W) and has a thickness of t.

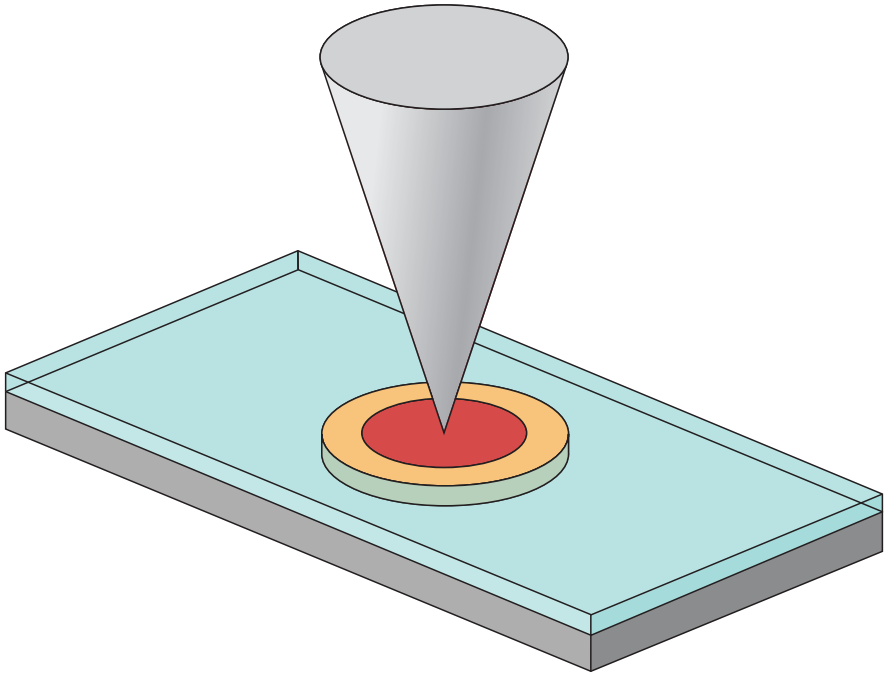

Figure A.2: Perspective view of a probe in contact with a thin film. The image shows a single probe of the four-point measurement setup. The thin film, in light blue, is uniform. The red and yellow areas have no physical meaning, they are just intended to show the cylindrical equipotential surfaces. The grey parallelepiped represents the insulating substrate.

directly derived from the analysis of the four-point measurement setup. The last part of the derivation can be also found in [65].

To prove Eq. A.1, the voltage distribution in the thin film, given by a single probe, is analyzed. This setup is shown in perspective view in Fig. A.2 and in cross-section in Fig. A.3. From the perspective view, it is possible to notice that, for an infinitely thin film, the equipotential surfaces have a cylindrical shape, since the voltage across the film thickness is constant and spreads radially for symmetry in the other directions. In both views, the coloring has no physical meaning. The film is uniform, and the red and yellow areas are just meant to show the shape of the equipotential surfaces. Due to the radial symmetry and the constant voltage across the vertical direction, the problem can be studied in a single dimension, in this case, in a radial direction r originating from the probe.

In the radial direction, the current density J can be obtained, according to the local Ohm's law, from the product of the electric field ε and the film conductivity σ, which is considered to be uniform across the whole film:

$$J(r) = \sigma\varepsilon(r) \tag{A.2}$$

By definition, the electric field can be expressed as the negative gradient of the voltage. In the one-dimensional case, the field will be defined by the negative derivative in the radial direction:

$$\varepsilon(r) = -\nabla V(r) = -\frac{dV(r)}{dr} \tag{A.3}$$

Substituting the electric field from Eq. A.3 into Eq. A.2:

$$J(r) = -\sigma \frac{dV(r)}{dr}$$

$$\frac{dV(r)}{dr} = -\rho J(r) \tag{A.4}$$

Where ρ is the resistivity of the film, or rather the inverse of the conductivity σ.

The current is injected from the tip, modeled as a point source, and spreads in all directions in the thin film. A voltage gradient is generated, which, as mentioned, has a cylindrical shape. A fine detail has to be cleared out. In this setup, the current is collected across the boundaries of the thin film, which is considered to expand across a whole plane. In a moment, a negative current source will be added, solving the problem of the current spreading at the film boundaries.

The current I spreads on a cylindrical surface of area A. The lateral surface of the cylinder is $A = 2\pi r\, t$, where t is the film thickness Therefore, the current density

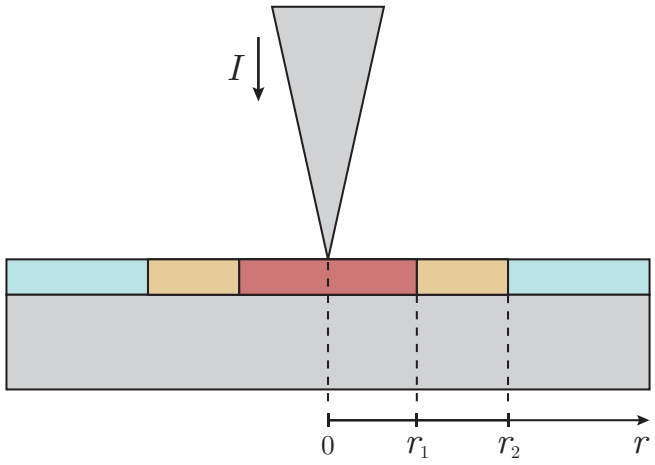

Figure A.3: Cross-sectional view of a single probe in contact with the thin film. The physical system is reduced to a single dimension, r, due to the circular symmetry. The current injected is modeled as a point source inside the thin film.

J can be expressed as:

$$J(r) = \frac{I}{A(r)} = \frac{I}{2\pi r\, t} \tag{A.5}$$

Finally, substituting the current density (Eq. A.5) into Eq. A.4, a separable variables differential equation in voltage and position is obtained:

$$\frac{dV(r)}{dr} = -\frac{\rho I}{2\pi t}\,\frac{1}{r} \tag{A.6}$$

The potential difference ($\Delta V = V_1 - V_2$) between the points at r_1 and r_2 can be derived by integrating both sides over r, changing the integration variable on the left side, and solving:

$$\int_{r_2}^{r_1} \frac{dV(r)}{dr}\, dr = -\int_{r_2}^{r_1} \frac{\rho I}{2\pi t}\,\frac{1}{r}\, dr$$

$$\int_{V_2}^{V_1} dV = -\frac{\rho I}{2\pi t}\int_{r_2}^{r_1} \frac{1}{r}\, dr$$

$$V_1 - V_2 = \frac{\rho}{t}\,\frac{I}{2\pi}\,\ln\left(\frac{r_2}{r_1}\right)$$

The equation can be rewritten by substituting the ρ/t with the sheet resistance:

$$\Delta V = R_{\square}\,\frac{I}{2\pi}\,\ln\left(\frac{r_2}{r_1}\right) \tag{A.7}$$

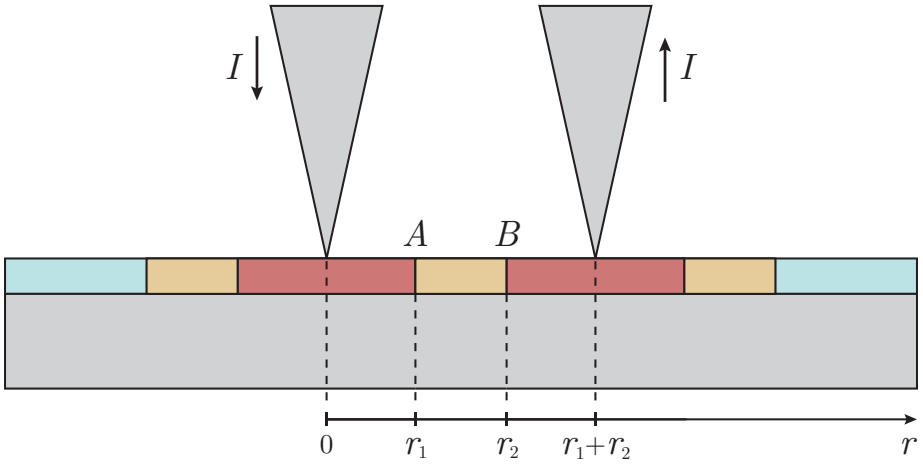

Figure A.4: Cross-sectional view of two probes in contact with the thin film. Starting from Fig. A.3, another probe, with current flowing in the opposite position, is added at a distance $r_1 + r_2$ from the first.

Eq. A.7 shows the radial voltage distribution.

If another probe, with an opposite current flowing through it, is added to the system (Fig. A.4), the voltage difference between the two points changes. The linearity of the physical setup allows for applying the superposition of effects, thus independently adding the contribution of the single probes. In particular, if the second probe is placed at a distance $r_1 + r_2$ from the first one, the system is symmetrical with respect to the two points. Oppositely to the previous case, point A is at a distance r_2 from the second probe while point B is at a distance r_1. Therefore, the amplitude of the voltage between the two points produced by the second probe only is equal to the one of the first. The sign of the contribution is also the same since the current is flowing in the opposite direction, and the voltage is measured between the further point A and the nearer B. The difference in potential between A and B will be doubled with respect to the one in Eq. A.7:

$$\Delta V = R_{\square} \frac{I}{\pi} \ln\left(\frac{r_2}{r_1}\right) \tag{A.8}$$

The four-point measurement setup, which cross-section is shown in Fig. A.5, is equivalent to the one analyzed in the derivation. Two more probes are added to the system to measure the potential difference V across two points of the thin film. A negligible amount of current flows in these two high-impedance probes.

The four probes are evenly spaced with a spacing s, and the two probes dedicated

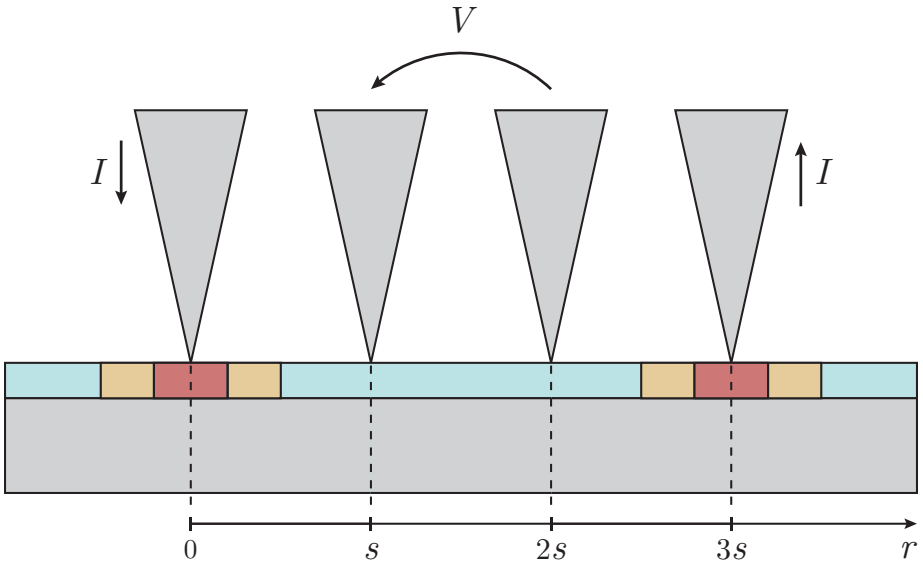

Figure A.5: Cross-sectional view of a four-point measurement setup for determining the sheet resistance of a thin film. The four probes are equally spaced with spacing s. In the two outer probes, the current I flows in opposite directions. The inner probes are used to measure the potential difference V across two points of the thin film.

to the voltage measurement are placed in r_1 and r_2. Therefore, the one placed in r_1 will be at a distance s from the origin while the other at a distance $2s$. Entering these geometrical information into Eq. A.8:

$$V = R_{\square}\,\frac{I}{\pi}\,\ln\left(\frac{2s}{s}\right) = R_{\square}\,\frac{I}{\pi}\,\ln\left(2\right)$$

Solving for the sheet resistance $R_{\square}$ the formula to be derived (Eq. A.1) is obtained:

$$R_{\square} = \frac{\pi}{\ln(2)}\,\frac{V}{I}$$

It is worth noticing the beauty of the formula itself, which has the form of Ohm's law, as expected, with a correction factor equal to the ratio between π and $\ln 2$.

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