Design of a Hardware-in-the-loop (HIL) e-Drive system based on FPGA and microprocessor

The aim of the thesis project, carried out at the company Kineton S.r.l., involves the design of a Hardware-in-the-loop (HIL) system, low voltage, consisting of an external control unit with sensorless FOC control (and CAN communication), that will perform the function of Device Under Test (DUT); a model of a permanent magnet synchronous motor developed on a processor and an inverter model (together with the Clarke & Park transformers) developed on FPGA, given the high frequency band.
In this project, the permanent magnet synchronous motor has an electric turbocharger as application, so that the additional objective is to achieve high speed and performance of the motor itself.

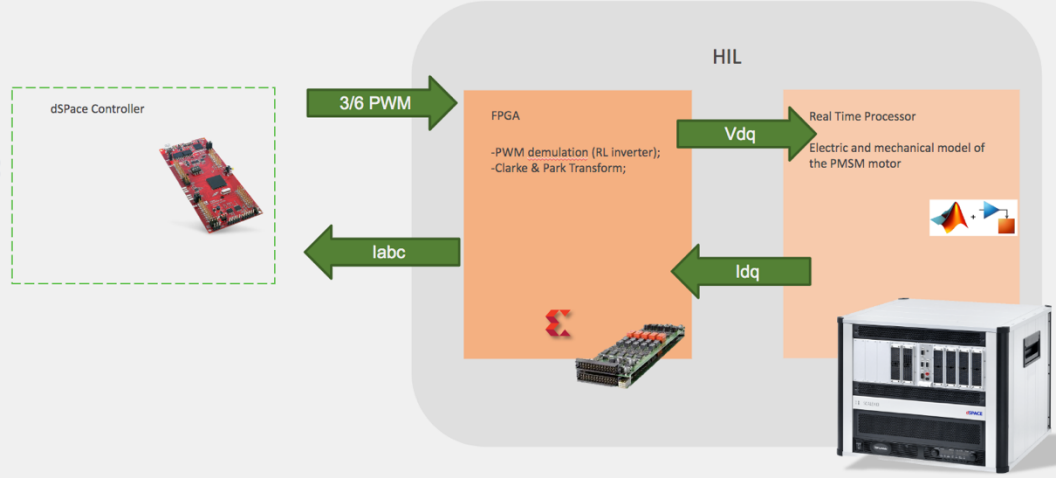

Figure 1 – Version 1.4

Hardware-in-the-loop simulations run at real time speed and perform I/O with the system or subsystem under test; in this way the test item believes it is operating as a component of a real system in its operational environment.
This type of simulation allows to test the system in its intended modes of operation as well as under dangerous or emergency situations without risking loss of life or valuable assets.
Moreover, critical or strange environmental conditions that may be almost impossible for system test, like outer space or icy roads in summer, can be simulated using computers and appropriate software algorithms.
Considered the complexity of the project itself, several models have been created with structures of increasing difficulty. In this way, it was possible to test one by one the electric and mechanical model of the Permanent Magnet Synchronous motor (PMSM) and the Clarke & Park transforms.
The approach was at first to create a simplified model, consisting of a simple speed control that I implemented on FPGA, in order to test the PMSM motor model implemented on the processor side (electrical + mechanical model).

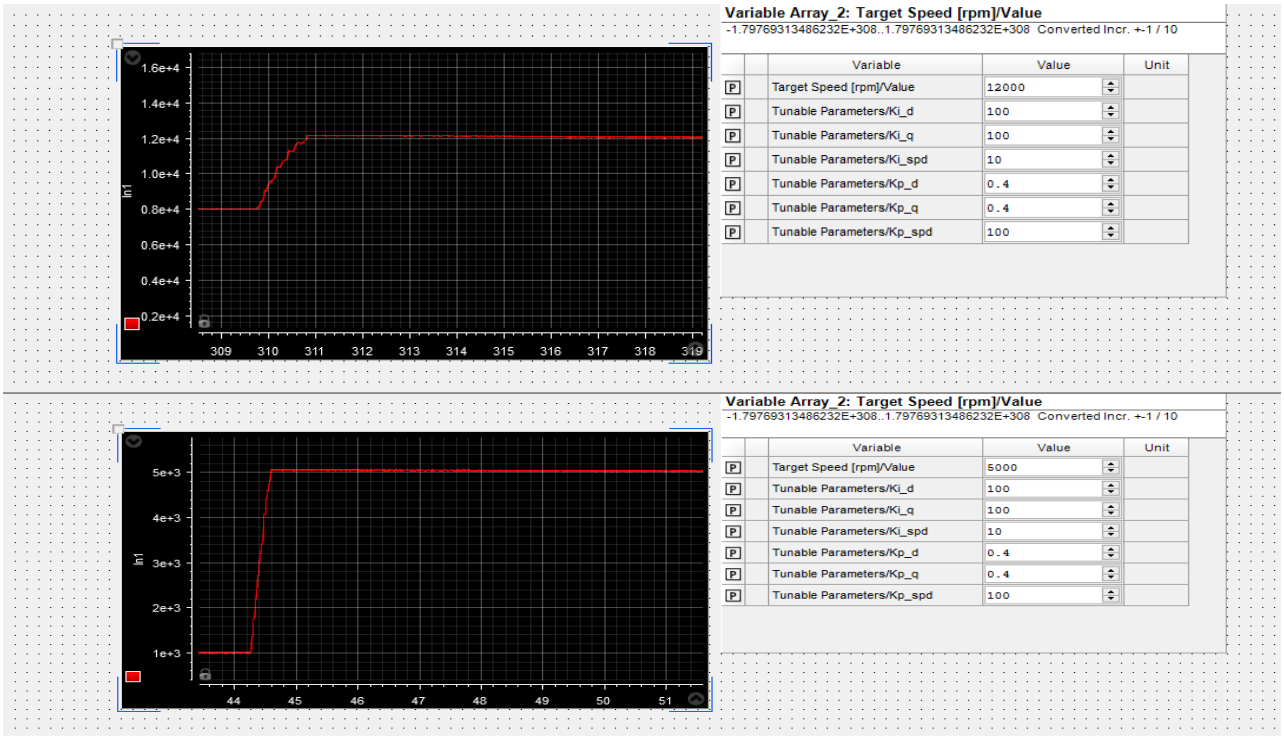

Figure 2 – Motor model at 12000 rpm (top) and 5000 rpm (bottom)

Then I moved on to a second and more articulated model, where the transforms of Clarke & Park were introduced in the FPGA part in such a way as to be able to test them or mainly to visualize the trend of voltages and currents in each phase.

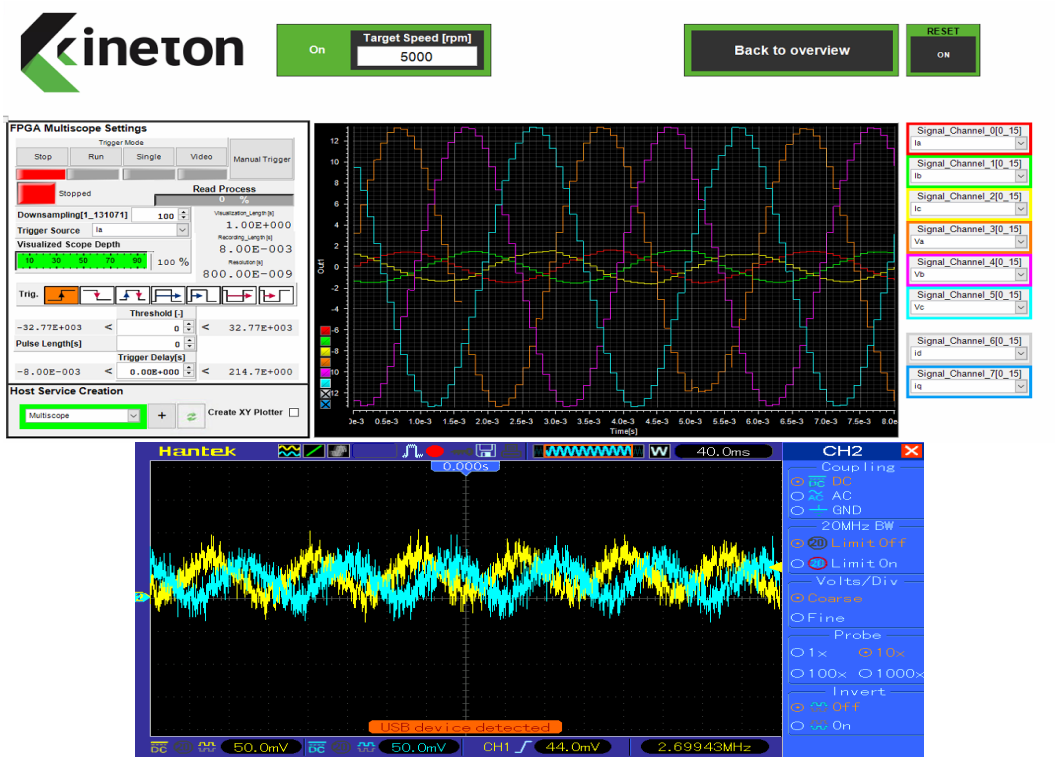

Figure 3 – Voltage and current trend through Oscilloscope (Bottom) and FPGA Scope (top)

In the end, the final and complete model of the project has been implemented, thus consisting of the PMSM motor, the inverter and the Clarke & Park transforms. Unfortunately, as we did not have the opportunity to test this model through the use of a real control unit, it was therefore decided to include a model of a controller present in the XSG libraries of the dSpace, in order to be able to view the complete operation of the project. Through an appropriate graphical interface, that has been utilized to make the simulation simpler and more intuitive, it is possible to visualize the following results of the model:

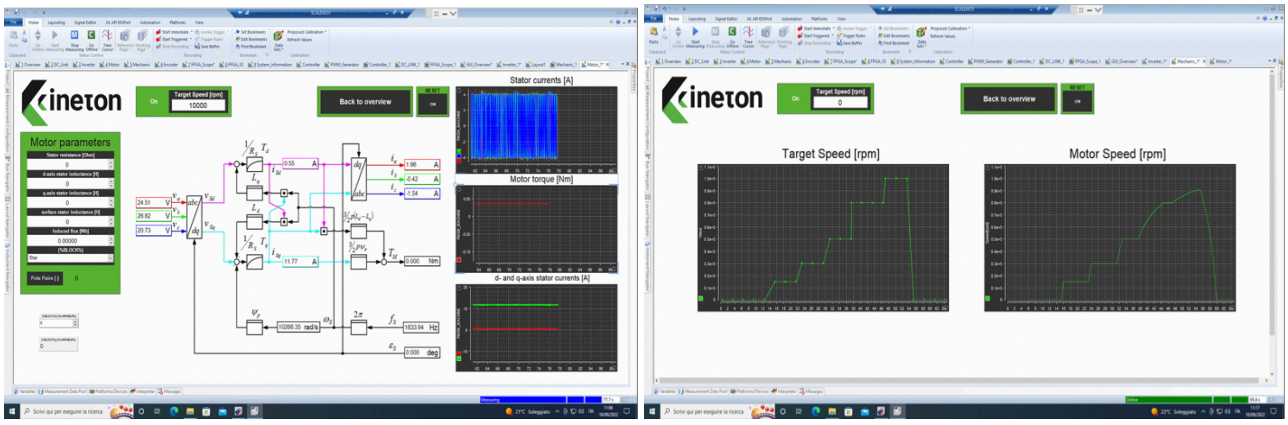

Figure 4 – Project result

Thanks to the implemented model and the parameterization used, it was possible to achieve excellent system performance both in response to noise and for the achievement of high speeds.

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CON.Kp_spd = 100;
CON.Ki_spd = 10;
CON.Kp_d = 0.4;
CON.Ki_d = 400;
CON.Kp_q = 0.4;
CON.Ki_q = 400;
MOT.Rs = 0.75;
MOT.Ld = 1.05e-3;
MOT.Lq = 1.05e-3;
MOT.I = 2.4018552467e-06;
MOT.P = 4;
MOT.Ke = 3.8;
MOT.phif = (MOT.Ke)/(sqrt(3)*2*pi*1000*MOT.P/60);
MOT.Bm = 11.603710493e-06;
MOT.I_max = 1.8;
MOT.configuration = 1;
MOT.FPGA_step = 8e-9;
```

Figure 5 – Parameters used

In particular, having operated outside the zone of flux-weakening has been possible to spin the motor until 13000 rpm approximately.
Therefore, considered the impossibility of having a real control unit to be used as a device under test, one of the next steps of my project will be then to replace the dSpace controller with a real control device.
In this way it will be possible to make a comparison with the model tested during my thesis and to visualize the differences both in terms of performance, speed achieved, parameters used and furthermore to adapt the model according to different and specific requirements.
Therefore, last but not least, a future job will be to verify and test the response of this model in such a way as to reach the same objectives even by using another device under test (DUT) different from the one used in this project.