POLITECNICO DI TORINO

Master's Degree in Electronics Engineering

Master's Degree Thesis

VOLATILE MEMRISTIVE SWITCHING DEVICES FOR NEUROMORPHIC COMPUTING

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Chapter 1

Introduction

Neuromorphic systems, which aim to mimic the function of the biological brain, are promising candidates to overcome the von Neumann architecture. Traditional architectures, where memory and processing unit are separated, cannot withstand the exponential growth of computation power and data transfer rate requirements. The attractiveness of biological neural networks is the ability to concurrently work both as computing and storage unit. In this context, memristors are increasingly gaining interest as artificial neurons or synaptic elements thanks to their low power consumption, scalability and complementary metal-oxide semiconductor (CMOS) technology compatibility. Memristors are two-terminal devices consisting of two electrodes sandwiching a switching layer. By applying a voltage across the two terminals, the resistance of the device can be changed from low (ON state) to high (OFF state) and vice-versa. Among memristive technologies, there are the electrochemical metallization memories (ECMs). In ECMs, one of the two electrodes is based on metals such as Cu or Ag which can easily diffuse into the switching layer. The transition to ON state (set) relies on the formation of a conducting filament inside a solid electrolyte: when a positive bias is applied, metal cations migrate from anode (active electrode) to cathode (inert electrode). In general, ECMs can be both volatile and non-volatile. In the first case, the transition to OFF state (reset) is achieved by the filament self-dissolution in absence of electric field, in the second, disrupting the metallic filament requires the application of a negative voltage on the active electrode. This thesis addresses the study of volatile and non-volatile functionality of ECM cells and how this dual regime can be controlled by engineering the materials stacks and the programming conditions.

The investigated devices in this thesis are based on Pt (bottom electrode) / switching layer / Ag (top active electrode) stacks. As switching layers, I first consider single dielectrics as 10 nm SiO_x and 10 nm Al_2O_3. The first device shows volatile behaviour, whereas the second one is non-volatile. To explore the coexistence of both volatile and non-volatile functionality, bi-layer stacks are

developed by engineering a thin Al_2O_3 layer positioned at the top or bottom electrode interfaces: 10 nm SiOx / 1 nm Al_2O_3 (top), 10 nm SiO_x / 2.5 nm Al_2O_3 (top), 2.5 nm Al_2O_3 (bottom) / 10 nm SiO_x. Devices are electrically characterized by performing quasi-static measurements.

The results discussed in this thesis illustrate how critical is the role of an interlayer at the metal/insulator interface, between different materials inside the switching layer, on the switching capabilities of the device.

The following chapters of this thesis are organized as follows:

Chapter 2. Memristive devices for neuromorphic applications
In this chapter I introduce the neuromorphic computing concept and the role of memristive device inside in-memory computing architectures, as well as the state of the art on memristive technoplogies and materials. Then, I focus on the class of ECMs and their working principles, highlighting the most important concepts that are discussed in my thesis.

Chapter 3. Device fabrication and experimental methodologies
In this chapter I describe the experimental and theoretical methodologies that I used to fabricate and characterize the ECM samples. I will focus on the fabrication procedure and techniques, and on the measurements methodologies for the memristors electrical characterization.

Chapter 4. Electrical characterization: Results and Discussion
This chapter describes the results of DC current-voltage measurements and statistical analysis. After a general overview on samples behaviour, I make a comparison among data and results obtained from different devices. Then, final considerations and hypothesis are provided about the influence of stack composition on the ECM cells performance.

Chapter 5: Conclusion and future work
I summarize the activity's main results and discuss the outlook and perspective.

Appendix A: Detailed analysis on bi-layered stacks
This appendix shows additional electrical characterization of the samples made of bi-layered SiO_2/Al_2O_3 insulating compound stacks. Results and plots reported in this section are supporting information for determined claims made in the body of the thesis.

Appendix B: MATLAB algorithm for automatic data analysis
This appendix addresses the explanation of the main routines implemented in MATLAB for the detection of the main figures of merit during data analysis.

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Chapter 2

Memristive devices for neuromorphic applications

A neural network consists of a set of neurons connected by weighted synaptic connections. The information transmitted by each synapse travels from the pre-synaptic neuron to the post-synaptic neuron. In between, the signal gets scaled by a synaptic weight, which has to be updated to train the entire network for the execution of a precise task [1]. To date, networks require the storage and training of a huge number of synaptic connections, but conventional hardware implementations encounter critical speed and energy consumption issues, because they rely on an off-chip memory for the storage of synaptic weights. The limiting process of constantly loading weights into the processing unit for the computation of the outputs to the next neurons, known as von-Neumann bottleneck, is overcome by in-memory computing architectures [2].

In-memory computing comprises hardware solutions that fulfill high throughput and low latency computational demands from machine learning and Artificial Intelligence (AI) algorithms such as Deep Neural Networks (DNNs) and Convolutional Neural Networks (CNNs) [3]. The implementation of these novel architectures is based on emerging beyond-CMOS devices that, exploiting diverse physical phenomena such as ionic transport, spin or phase transition ([4], [5], [6], [7]), are able to simultaneously store the synaptic weight and modulate the transmitted signal. Among these devices, memristors stand out as promising candidates for the hardware implementation of bio-inspired neural networks, that find a wide range of applications such as in speech recognition, autonomous vehicles, computer vision, robotics, to name just a few.

2.1 Memristive technology and materials

To date, memristive devices can be classified depending on the physical concept exploited and their structure: resistive switching random access memory (RRAM), phase change memory (PCM), spin-transfer torque magnetic random access memory (STT-MRAM), ferroelectric random access memory (FeRAM), ferroelectric field-effect transistor (FeFET), electro-chemical random access memory (ECRAM) and spin-orbit torque magnetic random access memory (SOT-MRAM) [8]. Under electrical stimulus, application of a voltage across the electrodes, these devices experience a change in the physical properties of the switching layer material. As an example, there is a change of the resistance for RRAM and PCM, magnetic polarization for STT-MRAM, and electrical polarization for FeRAM.

Depending on the switching mechanism, memristors can be nonvolatile, that is they maintain their previous resistance states without an applied electric field, or volatile, that return to their initial state over time in absence of bias. In particular, volatile memristors can be used in various applications such as selectors, synaptic devices (target application of this thesis) and integrate and fire neurons for neuromorphic computing, artificial nociceptors, devices for spiking encoded stochastic neural networks, to name some [9]. In this context, diverse materials have been explored in literature. To date, a large variety of conductive materials are being analysed, such as graphene, carbon nanotubes, conductive oxides like ITO, p- and n-type Si, and so on. Concerning the switching layer, recently, solutions like nanowires, 2D materials, 3D nanoarrays, etc, are investigated [10].

For RRAM, switching mechanisms can be classified mainly in two categories: electrochemical metallization (ECM), induced by redox reaction and migration of metal ions, and valence change mechanism (VCM), related to oxygen vacancies [9].

In my work I focus on the study of volatile memristive devices, and in particular I study electrochemical metallization (ECM) cells. Also known as conductive-bridge random access memory (CBRAM), they are a class of RRAM where a metallic conductive filament is created/disrupted between the electrodes, which has gained strong interest in recent years. Ag and Cu have been the most popular choice as active electrodes in ECMs, since they can easily dissolve in solid electrolytes under low electric field, thanks to their high ionic mobility. The switching layer is a thin film typically made of an insulating material or a semiconductor. Among the insulating materials, binary oxides are commonly studied, due to their good compatibility with CMOS process and good thermal stability.

2.2 Working principles of volatile ECMs

The principle of operation for the resistive switching inside a volatile ECM cell is based on an electrochemical metal deposition and dissolution [11]. As in RRAMs, in general, by applying a voltage across the two terminals, the resistance of the device can be changed from high resistance state (HRS), OFF state, to low resistance state (LRS), ON state, and vice-versa. Figure 2.1 shows a typical current-voltage characteristic of a $Pt/SiO_2/Ag$ ECM cell, highlighting the most important stages of the switching process in the insets A to E.

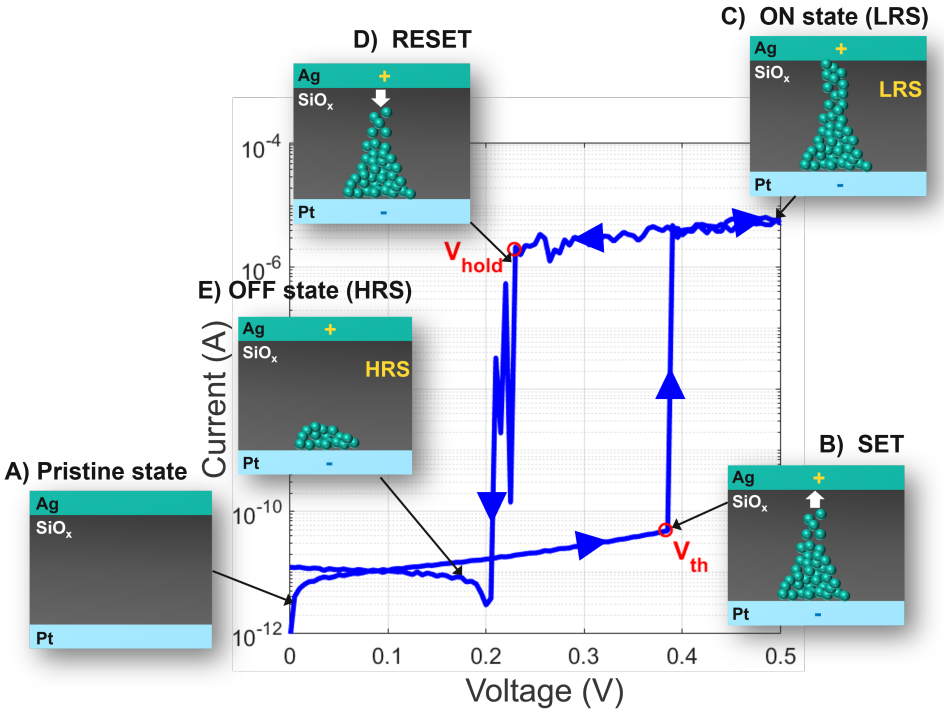


Figure 2.1: Typical current response to triangular voltage sweep of a $Pt/SiO_2/Ag$ ECM cell. The current compliance limits the conductance in ON state. The most important stages of the switching process are illustrated in the insets A to E.

The device is initially in the pristine HRS. The application of a sufficient positive bias voltage to the active Ag electrode leads to the injection of cations from the electrode into the SiO_2 switching layer. Under the driving force of an electric field, the migration of Ag ions across the solid-electrolyte, from top active Ag electrode to bottom inert Pt electrode, follows a mass transport process [12]. Once Ag ions reach the bottom interface, they are reduced and electrocrystallization (nucleation) occurs. Subsequent nucleation and growth, form a metal filament growing preferentially

toward of the active electrode, resulting in a cone shape pointing upwards [13]. The switching process ends when the Ag conductive filament makes a metallic contact to the opposite active electrode: the two electrodes are bridged and the memory cell goes to LRS. The cell retains the ON state unless the filament self-dissolves once the applied voltage falls below a hold value V_{hold}, with a given retention time. Driving forces of the self-relaxation process discussed in literature include surface tension or surface energy minimization effects ([14],[15],[16]), mechanical stress [17], steric repulsion [18] or thermo-diffusion effect [19], depending on the nature of the filament and the surrounding oxide matrix. A schematic representation of the physical mechanisms taking place inside a Pt/10nm SiO_2/Ag ECM cell for the Ag filament growth is depicted in Figure 2.2.

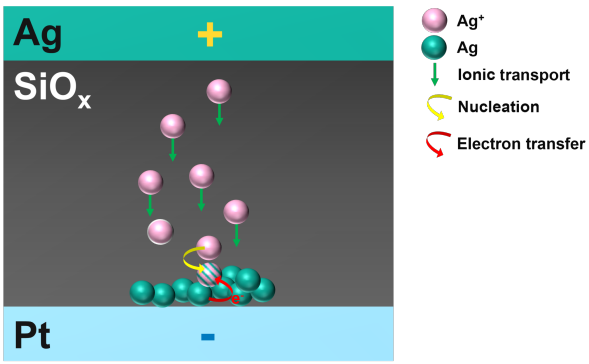


Figure 2.2: Schematic representation of the physical mechanisms for the filament growth inside a Pt/10nm SiO_2/Ag ECM cell, such as ionic transport and nucleation.

Figure 2.3, shows the influence of voltage on the limiting physical mechanisms, thus on the growth rate and morphology of the metallic filament.

At low voltages where nucleation is the limiting step, a homogeneous growth is expected as well as a relatively bulky filament. In the intermediate region a linear growth of a dendritic-shaped filament occurs, since electron transfer limits the filament's growth rate. At higher voltages where ion-migration also becomes the limiting factor, local depletion of Ag ion creates a field enhancement effect in the filament region. This causes a self-accelerated and anisotropic growth and eventually, a thin, fragile filament is formed [20].

Size and shape of the formed metallic filament are stated to have an important role in determining the volatile or nonvolatile characteristics of the memory cell. If the filament is large and thermodynamically stable, even in absence of electric field it does not dissolve, thus showing nonvolatile characteristics. On the other hand, if the size of the conductive filament is smaller than a certain critical size, the device shows volatile characteristics and dissolves without the electric field [21].

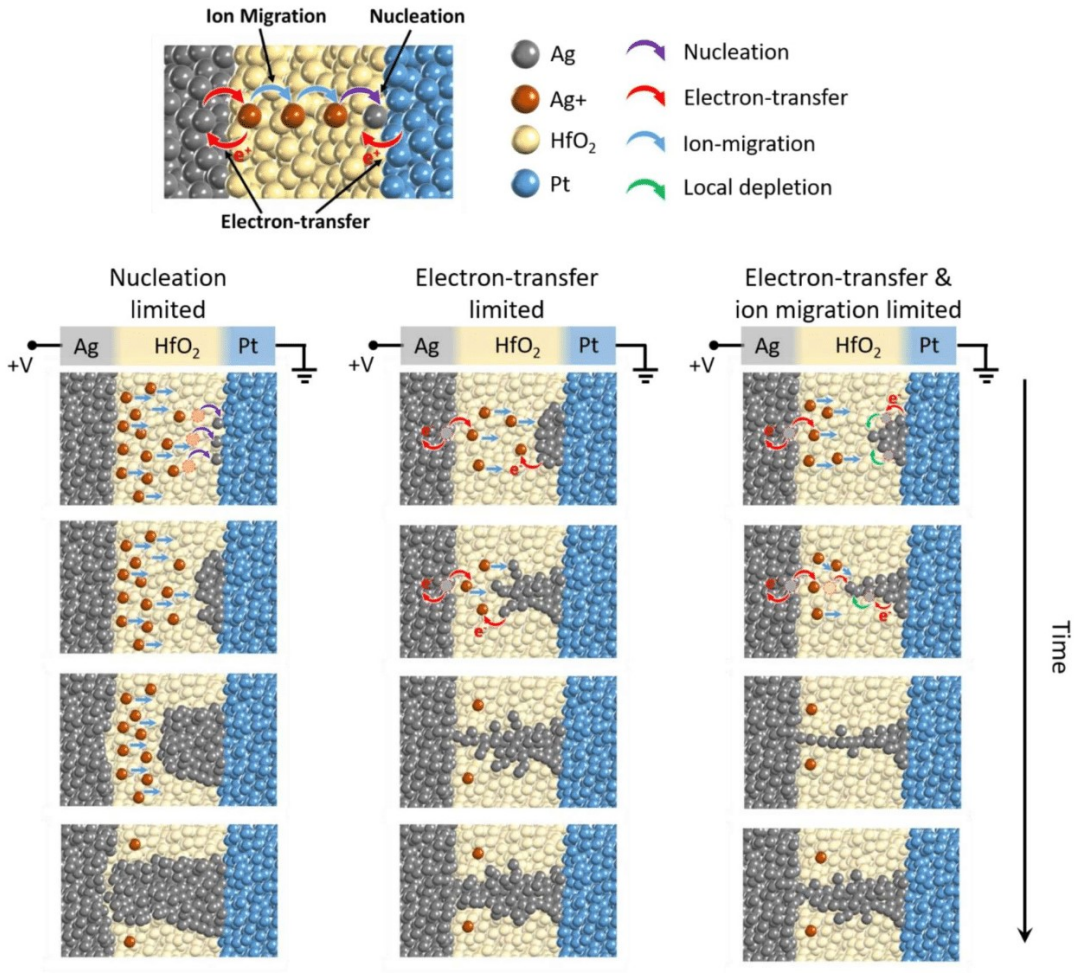


Figure 2.3: Voltage-dependent filament growth mechanisms. Reprint from [20].

2.3 Contribution of this work

Novel ECM structures proposed in this thesis have bi-layer switching stacks made of SiO_2 and Al_2O_3 with different thicknesses and arrangements. I found a coexistence of both volatile and non-volatile features within each of these samples. Both features can be attained by adjusting the current limitation during the forming process and switching cycling, thus controlling the strength of the conductive filament.

Chapter 3

Device fabrication and experimental methodologies

This chapter is divided into three sections. The first one is focused on the device fabrication flow. The second section shows the electrical setup and equipment used for the device characterization. The last section describes the measurement methodology used for the electrical testing.

3.1 Device fabrication

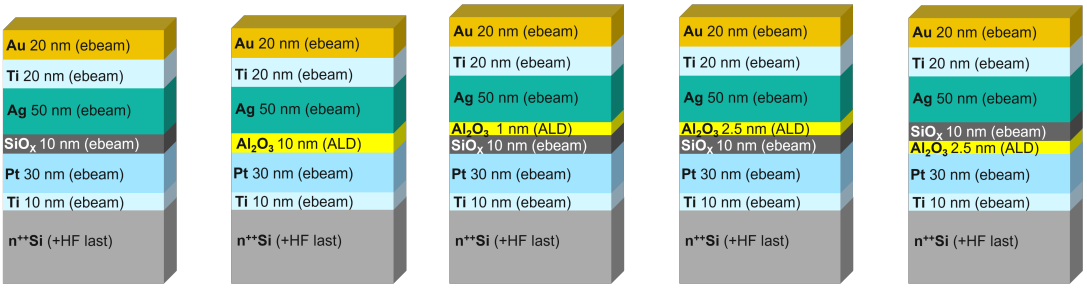
The fabrication process follows four macro steps which will be discussed in detail in the following subsections: deposition of bottom electrode, insulating stack, top electrode and back contact.

The final structure of the samples is reported in Figure 3.1. It depicts qualitatively the cross-section of the developed devices, which are fabricated according to the steps explained later. For the sake of brevity, a naming system is then defined. From now on, I will refer to the devices depicted in Figure 3.1 from left to right as *Si10*, *Alu10*, *Alu1T*, *Alu2T*, *Alu2B*, where *1T* and *2B* stand for "1 nm on Top" and "2.5 nm at Bottom", respectively.

In the following subsections, every step of the whole fabrication procedure, reported for samples *Si10* and *Alu10* in the following table (Table 3.1), is addressed. Other samples (*Alu1T*, *Alu2T* and *Alu2B*) only differ for the combination of materials, thus alternation of deposition techniques, in the switching stack.

3.1.1 Bottom electrode

The bottom electrode deposition is performed by electron beam evaporation (e-beam) on a 4-inches highly doped (n-type, $1 - 3 \cdot 10^{-3}$ Ω·cm) silicon wafer, after



(a) Sample Si10 **(b)** Sample Alu10 **(c)** Sample Alu1T **(d)** Sample Alu2T **(e)** Sample Alu2B

Figure 3.1: Schematic representation of the samples cross-sections, with same bottom and top electrodes (Pt and Ag), but different dielectric stacks. From left to right the stacks are made of 10 nm SiO_2, 10 nm Al_2O_3, 10 nm SiO_2 / 1 nm Al_2O_3 (top), 10 nm SiO_2 / 2.5 nm Al_2O_3 (top), 2.5 nm Al_2O_3 (bottom) / 10 nm SiO_2.

Fabrication step	**Si10**	**Alu10**
HF-last	500µm $n^{++}Si$	500µm $n^{++}Si$
Bottom electrode	10nm Ti/30nm Pt by e-beam	10nm Ti/30nm Pt by e-beam
Oxide	10nm SiO_2 by e-beam	10nm Al_2O_3 by ALD
Sample cut	2.2×2.2 cm^2	2.2×2.2 cm^2
Thermal treatment	RTP @400°C, 10min, 2000sccm N_2 flux	RTP @400°C, 10min, 2000sccm N_2 flux
Photolithography		
Top electrode/contact	50nm Ag/ 20nm Ti/ 20nm Au, by e-beam	50nm Ag/ 20nm Ti/ 20nm Au, by e-beam
Lift-off		
Back contact	150nm Al by e-beam	150nm Al by e-beam

Table 3.1: Name and description of each fabrication macro-step.

its native silicon dioxide is removed by using a 5% solution of hydrofluoric acid (HF). It consists of a 30nm-thick Pt layer grown successively to a 10nm-thick Ti layer, which is used to promote adhesion on silicon, without breaking vacuum.

3.1.2 Switching layer

The insulating stack is different in each sample. In samples *Si10*, *Alu1T* and *Alu2T* (Figure 3.1a,c,d) a 10 nm thick layer of SiO_2 is deposited by e-beam evaporation on the bottom Pt electrode. For the sample *Alu10* (Figure 3.1b), a 10 nm-thick layer of Al_2O_3 is deposited by atomic layer deposition (ALD) at 200°*C* employing the Trimethylaluminum (TMA) and H_2O as Al and oxygen precursors, respectively.

The schematic representation of one cycle of ALD for the Al_2O_3 deposition on SiO_2 substrate is reported in Figure 3.2. During each cycle, one atomic layer is deposited. One cycle consists of the sequence TMA dosing / purging / H_2O dosing / purging. This sequence is repeated 104 times to grow 10 nm thick alumina. To complete the switching stack in sample *Alu1T* (*Alu2T*), 1 nm (2.5 nm) of Al_2O_3 is grown by ALD. Twelve (26) cycles are required to grow 1 nm (2.5 nm) thick alumina. In *Alu2B* the two deposition techniques are applied in the reversed order. In this case the 2.5 nm thick alumina layer is between the Pt bottom electrode and the SiO_2 layer.
Once the oxide layers are deposited, the wafer is cut in 2.2×2.2 cm^2 squared samples and successively thermally treated by rapid thermal processing (RTP) @400°C for 10min under 2000sccm N_2 flux.

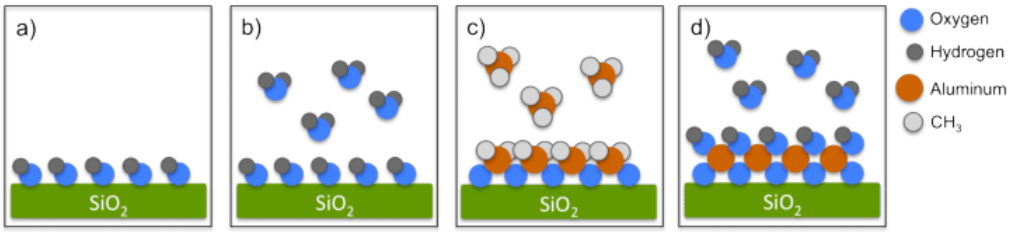


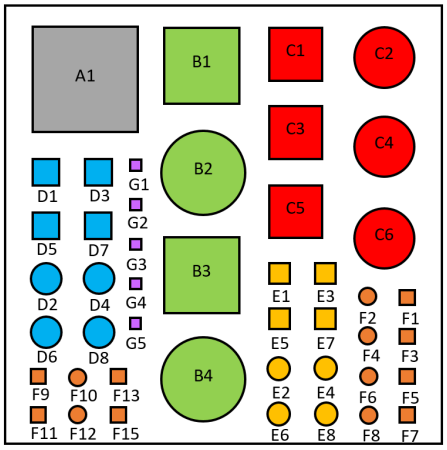
Figure 3.2: Al_2O_3 growth by ALD occurs by separately pulsing H_2O and TMA ($Al(CH_3)_3$) into the reaction chamber. The surface of SiO_2 is naturally hydroxylated, so the it satisfies the requirements for ALD processing (a). H_2O is introduced into the chamber to completely hydroxylate the surface of the substrate, (b). H_2O is evacuated from the chamber, then TMA is pulsed into the chamber to deposit one layer of Al (c). TMA is then evacuated form the chamber, and H_2O is reintroduced (d). Figure edited from [22].

3.1.3 Top electrode/contact

The top metal stack is made of Ag (50nm) and 20nm-thick Au contact layer on top. A 20nm-thick Ti layer is also required to promote Au adhesion on Ag. The top electrodes of devices are patterned by contact photolithography. The lithographic photomask (made of transparent fused silica covered with a chromium (Cr) pattern defined by electron beam lithography), used for the patterning of each sample, is composed of 12x12 squared dyes; in each dye, which is named like in Figure 3.3a, there are gates with specific sizes and shapes (Figure 3.3b-c). The tested devices on each sample are the ones in dyes located in the centre of the dye grid (3.3a), where less defects are statistically found (best device yield). Moreover, I focused on characterizing devices of type "G" (Figure 3.3b) which have the smallest area ($40\mu m \times 40\mu m$).

A1	B1	C1	D1	E1	F1	G1	H1	I1	J1	K1	L1
A2	B2	C2	D2	E2	F2	G2	H2	I2	J2	K2	L2
A3	B3	C3	D3	E3	F3	G3	H3	I3	J3	K3	L3
A4	B4	C4	D4	E4	F4	G4	H4	I4	J4	K4	L4
A5	B5	C5	D5	E5	F5	G5	H5	I5	J5	K5	L5
A6	B6	C6	D6	E6	F6	G6	H6	I6	J6	K6	L6
A7	B7	C7	D7	E7	F7	G7	H7	I7	J7	K7	L7
A8	B8	C8	D8	E8	F8	G8	H8	I8	J8	K8	L8
A9	B9	C9	D9	E9	F9	G9	H9	I9	J9	K9	L9
A10	B10	C10	D10	E10	F10	G10	H10	I10	J10	K10	L10
A11	B11	C11	D11	E11	F11	G11	H11	I11	J11	K11	L11
A12	B12	C12	D12	E12	F12	G12	H12	I12	J12	K12	L12

(a)



(b)

Square				Circle			
Gate	Side (mm)	Area (mm^2)	Area (cm^2)	Gate	Diam. (mm)	Area (mm^2)	Area (cm^2)
A_d	0.4	0.16	$16x10^{-4}$	-	-	-	-
B_d	0.283	0.08	$8x10^{-4}$	B_p	0.32	0.08	$8x10^{-4}$
C_d	0.2	0.04	$4x10^{-4}$	C_p	0.226	0.04	$4x10^{-4}$
D_d	0.1	0.01	$1x10^{-4}$	D_p	0.-113	0.01	$1x10^{-4}$
E_d	0.071	0.005	$5x10^{-5}$	E_p	0.08	0.005	$5x10^{-5}$
F_d	0.05	0.0025	$2.5x10^{-5}$	F_p	0.0565	0.0025	$2.5x10^{-5}$
G_d	0.04	0.0016	$1.6x10^{-5}$	-	-	-	-

(c)

Figure 3.3: (a) Each sample is organised in 12x12 dyes named with a letter, indicating the coloumn, and a number, indicating the row where they are located. (b) Gates of different sizes and shapes are present on each squared dye. (c) Table describing the geometry and the area of each device.

The photolithographic procedure is described in detail in the following list and each step is depicted in Figure 3.4.

1. **Dry-bake**: the specimens is heated on a hotplate at 120°C for 4 minutes to remove any trace of water from the oxide surface and promote resist adhesion;
2. **Spin-coating**: a uniform film of Photoresist (AZ 5214 E) is deposited on the oxide through spin-coating at 6000 RPM for 30s;
3. **Pre-bake**: heating at 110°C for 60s on the hotplate;
4. **Exposure**: exposure of the sample under UV light through the lithographic mask (previously cleaned using acetone (C_3H_6O) and isopropyl alcohol $(CH_3)_2CHOH$ and rinsed with nitrogen N_2) for 5 seconds. The contact photolithography method was exploited to improve features definition;

5. **Reversal bake**: heating at 110°C for 60s on the hotplate;

6. **Flood exposure**: exposure of the sample under UV light for 35s (without mask);

7. **Development**: removal of the unexposed resist by 1:6 solution of AK400K and deionized water for 50 seconds. Rinsing of the sample under N_2;

8. **E-beam evaporation**: deposition of top metal stack by e-beam (50nm Ag/20nm Ti/20nm Au);

9. **Lift-off**: removal of the residual photoresist and of the excess metal by acetone dipping and nitrogen jet enhanced acetone dipping. Then the sample is rinsed with deionized water and nitrogen.

Moreover, for the top metal processing, an image reversal resist (AZ 5214E) in negative mode is exploited (if used with 1:4 dilution ratio it works as positive resist), so that UV light enhances the cross-linking reaction in the area exposed to UV light. Doing so, the insoluble photoresist assumes a pattern which is complementary to that of the lithographic photomask.

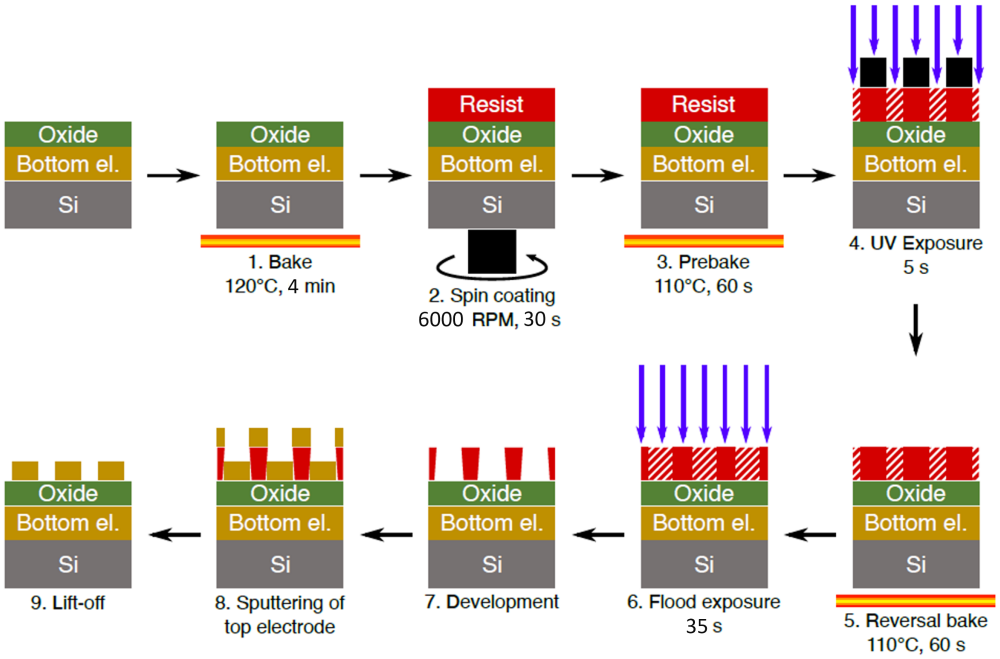


Figure 3.4: Schematic representation of photolithographic and lift-off steps for the Ag/Ti/Au top electrode patterning.

For demonstration purposes, the schematic cross-section representation of four gates, patterned during the fabrication steps photolithography/e-beam/lift-off, is schemed in Figure 3.5.

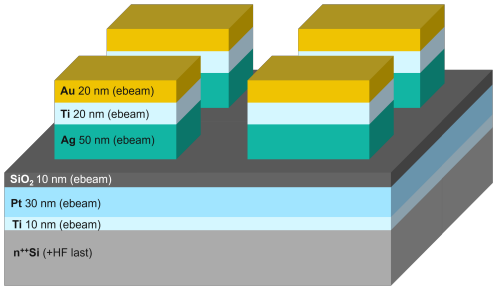


Figure 3.5: Schematic cross-section scheme of four patterned top electrodes/contacts belonging to sample *Si10*.

3.1.4 Back contact

As last step, a 150nm thick Al layer is deposited at the bottom of the silicon wafer to provide a back contact. This second contact will be used to ground the device during its electrical characterization (Figure 3.6). The solution of having two sides to be contacted, instead of having two pads (contacting top and bottom electrodes of the device) on the top of the sample, is much more practical for prototyping and electrical testing purposes. Furthermore, the process results cleaner and simpler (no vias needed, only one lithographic mask is required, few fabrication steps).

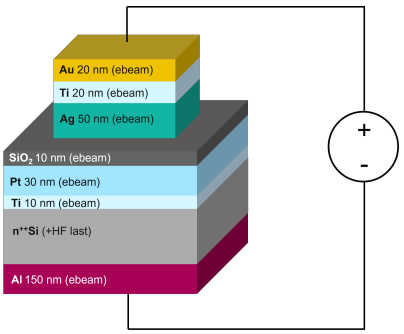


Figure 3.6: Electrical connection scheme showing top Au contact and back Al contact probed to the voltage supply.

3.2 Electrical measurement setup

In this section the measurement electrical setup, instruments and connection schemes used for the device electrical characterization are presented.

The experimental setup used to perform the electrical characterization of the device at room temperature consists of the following instrumentation:

- A probe station (Wentworth Labs) on which the chuck is embedded together with an optical microscope (MicroZoom II) and adjustable cursors with micrometric tungsten probes (tip $\varnothing 25\mu m$) to contact the top electrode of the device (Figure 3.7a).

- A metallic chuck (Figure 3.7b) that works both as sample sustain and as back contact (GND) directly connected to the rack panel via a coaxial cable. A vacuum valve at the center ensures the sample to be steady in place and to have a solid contact.

- Agilent B1500A Semiconductor Device Analyzer supported by the EasyExpert© which is the software of the B1500A (Figure 3.7(c-d)).

- Two Agilent B1531A remote-sense and switch units (RSUs) (Figure 3.8). The RSU is mounted on the wafer prober close to the device under test (DUT) to optimize measurement performance.

- A PC to control the Agilent B1500A operation through the EasyExpert© software. Some custom made and pre-made programs were used for the characterization of the device. The desktop communicates with the B1500A via General Purpose Interface Bus (GPIB) interface (IEEE-488).

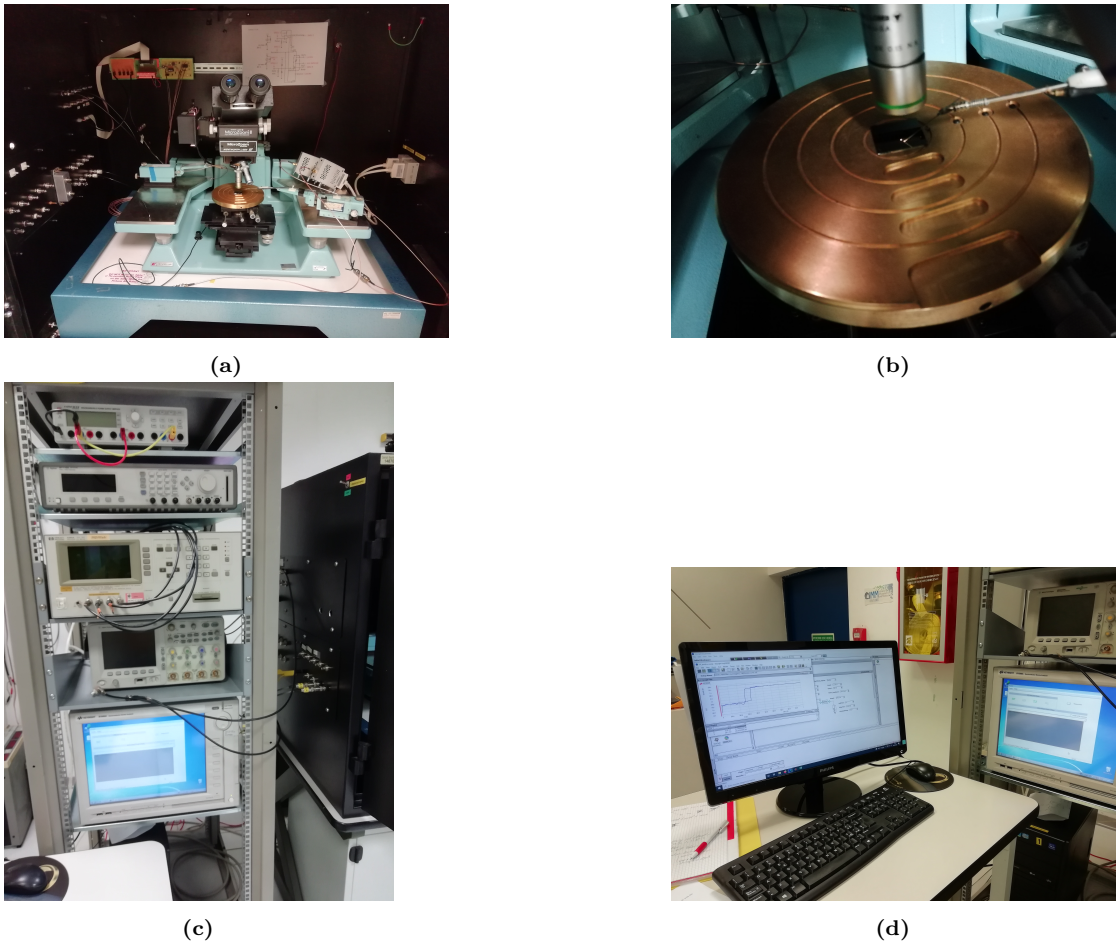


Figure 3.7: (a) Grounded metallic chuck with a sample placed on top with the tungsten probe. (b) Probing station inside the black metallic box working as a Faraday shield. Above the chuck there is the optical microscope for the manual probing of the devices. (c-d) Instrumentation rack with the B1500A Semiconductor Ananlyzer at the bottom. It is connected to the PC via GPIB to be controlled by the EasyExpert© software.

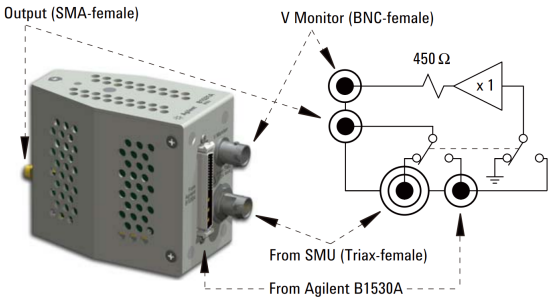


Figure 3.8: Agilent B1531A remote-sense and switch units (RSUs).

3.3 Measurement methodology

In this section the experimental technique for the devices electrical characterization are addressed. The tested samples are depicted in Figure 3.1.

The DC characterization of devices is mainly performed in two steps: Forming and threshold switching (TS).

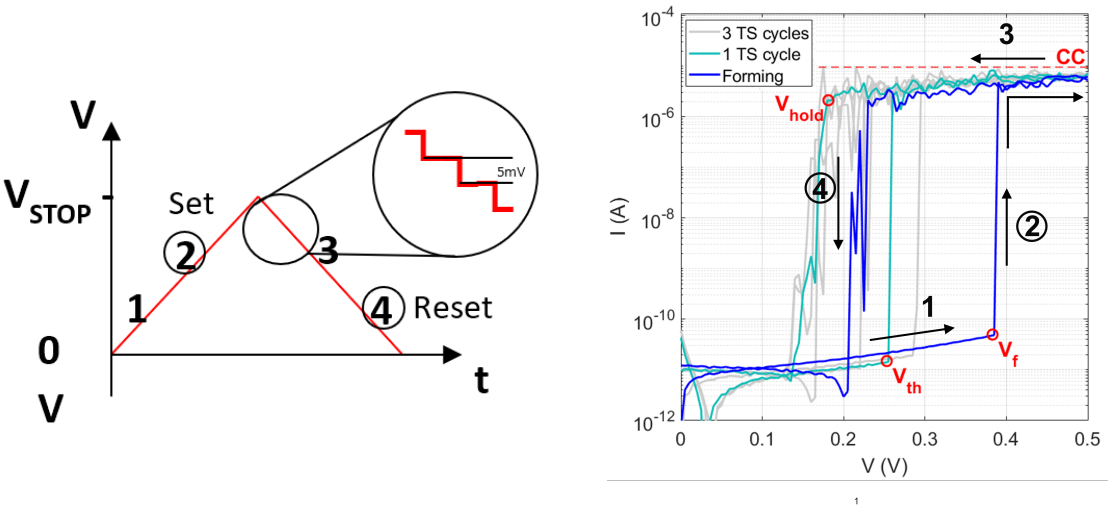
Forming

To characterize the forming process of a pristine device (first formation of a Ag conductive filament inside its switching layer), I apply a voltage across the two electrodes. Voltage is linearly swept from 0V up to V_{stop} (maximum voltage value reached during the quasi-static characterization) and then back to 0V. This forward and backward sweep cycle will be simply denoted *cycle*, and is schemed in Figure 3.9a. For the entire duration of the measurement I set a compliance current (CC), which define the maximum current allowed to flow in the measured device, to limit the current passing through the device, preventing it from breaking. A representative forming process of a pristine device for a CC of 100nA is shown in Figure 3.9b in dark blue. The arrows indicate the evolution of the current response during the linear voltage sweep, following the steps highlighted in Figure 3.9a. Initially, the current level is low in the range of tens of pA (I_{off}, current level when the device is in OFF state) and slightly increases proportionally to the applied voltage (1). In (2) an abrupt increment of the conductivity takes place, leading the current to reach the CC: this switching occurs when the Ag filament bridges bottom and top electrode, and happens when a sufficiently high voltage, called forming voltage V_f, is reached. Above V_f, the current response results in a plateau, since it is limited by the CC. When sweeping backward, from V_{stop} to 0V (3), a drop of the conductivity occurs, usually in correspondence of a voltage level that is lower than V_f: the current decreases back to the initial I_{OFF} value because of the disruption of the conductive filament inside the switching layer due to the insufficiently high electric field.

Threshold switching

After the pristine device is formed, the TS endurance test is performed to study the performance of the device under repeated stress: the electrical characterization of forming and TS endurance of one device is performed at the same CC. For the characterization of TS endurance on ECM cells, I apply a series of many (at least 100) cycles, that is linear voltage sweeps, similarly to the one used for the forming (Figure 3.9a). During the TS measurements the V_{stop} is usually set at a lower value than V_{stop} set for the forming. The switching (SET) of the device to the ON state during TS occurs when the increasing voltage overcomes a threshold value V_{th} (usually lower than V_f [13]). The cell retains the ON state unless the filament self-dissolves once the applied voltage falls below a hold value V_{hold}, with

a given retention time. V_{th} and V_{hold} points are depicted on a TS representative I-V characteristic in Figure 3.9b (light blue curve).



(a) (b)

Figure 3.9: (a) Sweeping scheme of the voltage with time. The 5mV step of the ramp dictates when the measured current will be sampled. Circled numbers highlight when SET and RESET of the device occur: numbers have correspondence with numbers and arrows to the sample forming on the right. (b) I-V curve of a sample forming process where arrows indicate the current dynamics in response to a voltage sweep stimulus.

The compliance current and other measurements settings, used for the characterization of the devices, are adjusted on the B1500A Semiconductor Analyzer through its software Keysight EasyExpert©. Typical forming and TS electrical conditions and settings for the characterization of volatile ECMs are reported in the following table (3.2).

Test type	$\mathbf{V_{stop}}$	$\mathbf{V_{step}}$	$\mathbf{t_{hold}}$	$\mathbf{t_{delay}}$
Forming	0.7V or 1.0V	5mV	0s	5ms
TS	0.5V or 0.7V	5mV	0s	5ms

Table 3.2

where:

- V_{stop} is the last reached voltage value before sweeping back to 0V.
- V_{step} is the ramp voltage resolution, which defines the points where the corresponding current values are acquired by the measuring system. A 5mV voltage step is represented in Figure 3.9a.

- t_{hold} is the time from beginning of channel output to beginning of t_{delay}: Figure 3.10.
- t_d is the delay time, from end of t_{hold} (start of the whole measurement routine) to beginning of measurement. Channels start the measurement as soon as the wait time elapses: Figure 3.10.

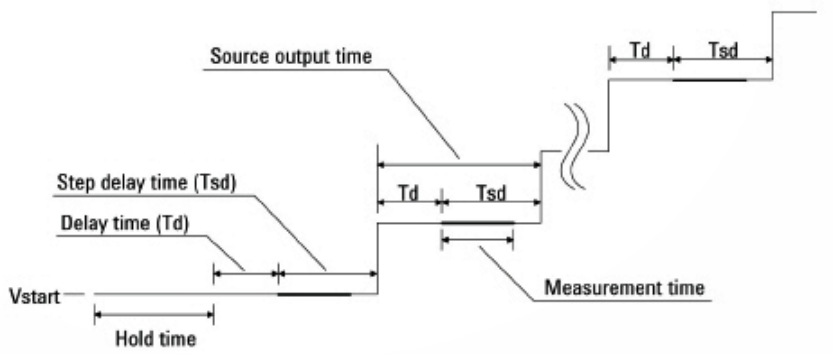


Figure 3.10: B1500A channel measurement timing diagram.

Chapter 4

Electrical characterization: Results and Discussion

In this chapter I report the results of DC measurements performed on the fabricated samples, following the measurement specifications discussed in the previous chapter. Firstly, an overview about the samples behaviour is provided. A device which has volatile memory characteristics, returns to its initial state over time in absence of bias. It can be electrically driven by many cycles in Threshold Switching (TS), where it is possible to achieve the filament formation (SET) and disruption (RESET) at the same voltage polarity in the forward and backward IV sweep, respectively. Non-volatile operation, instead, consists of performing cycling through positive and negative voltage polarity, called Bipolar Resistive Switching (BRS), to achieve the SET and RESET of the device, respectively.

In the second section a detailed analysis on volatile switching of the sample Pt/10nm SiO_2/Ag (sample Si10) is shown. The last section addresses the analysis of volatile switching on samples with SiO_2/Al_2O_3 compound stacks (10nm SiO_2/1nm Al_2O_3(top), 10nm SiO_2/2.5nm Al_2O_3(top), 2.5nm Al_2O_3(bottom)/10nm SiO_2) to illustrate their behaviour and give a final consideration about the influence of stack composition on the ECM cells performance.

4.1 Overview of sample behaviours: analysis of volatile and non-volatile switching

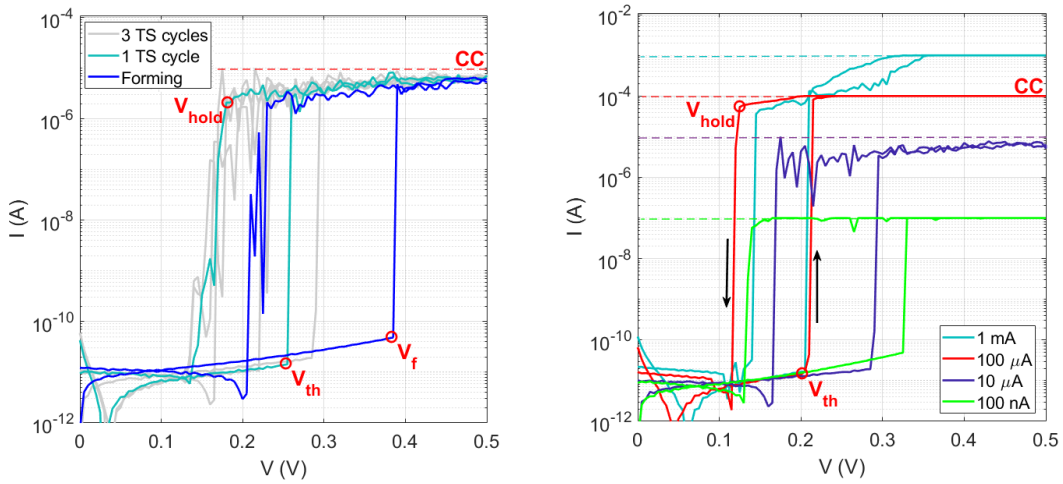
This section gives an overview on the electrical behaviour of the different fabricated samples. The structure of each sample is depicted in Figure 3.1 and is summed up in Table 4.1.

	Si10	**Alu10**	**Alu1T**	**Alu2T**	**Alu2B**
Bottom electrode	30nm Pt	30nm Pt	30nm Pt	30nm Pt	30nm Pt
Switching layer	10nm SiO_2	10nm Al_2O_3	10nm SiO_2/ 1nm Al_2O_3	10nm SiO_2/ 2.5nm Al_2O_3	2.5nm Al_2O_3/ 10nm SiO_2
Top electrode	50nm Ag	50nm Ag	50nm Ag	50nm Ag	50nm Ag

Table 4.1: Table listing the layers composition of the five fabricated samples.

$Pt/SiO_2/Ag$

From the characterization of forming and threshold switching of devices with Pt/ SiO_2/Ag structure, I plot the typical I-V characteristics in Figure 4.1a at the CC of 10 μA. In this picture, the I-V of the forming process is plotted in blue together with some representative TS cycles: the most important DC features, defined in Chapter 3.3, such as Forming Voltage (V_f), Threshold Voltage (V_{th}), Hold Voltage (V_{hold}) are indicated. Several TS cycles are performed at different compliance levels. Typical I-V responses of TS at different CC are plotted in Figure 4.1b. Devices show TS on a wide CC working range, from 100 nA to 1 mA.



(a) **(b)**

Figure 4.1: (a) Sample $Pt/SiO_2/Ag$. Current-Voltage response of the forming process (blue) and four representative TS cycles at 10 $\mu A_{(CC)}$. V_f, V_{th} and V_{hold} points are indicated. (b) Representative TS cycles at four different CCs, 100 nA, 10 μA,100 μA and 10 mA, respectively. Threshold and Hold voltages are indicated.

$Pt/Al_2O_3/Ag$

From the DC characterization of devices from sample Pt/10nm Al_2O_3/Ag

(*Alu10*), I find that they are non-volatile at every CC value from $100\,nA$ to $1\,mA$. Figure 4.2a shows the forming I-V curve of one device at $10\,\mu A_{(CC)}$ (blue) together with one representative BRS cycle at $1\,mA_{(CC)}$ (cyan). The current at the end of the forming process (during backward voltage sweep) does not fall back to I_{OFF}: this suggests that the ON state is stable (non-volatile behaviour). Therefore, the device needs to be reset with a negative V sweep before driving it through successive BRS. Figure 4.2b depicts four BRS cycles performed at $1\,mA_{(CC)}$ on one representative device from sample Alu10: the arrows follow the current response path, highlighting the SET (2) and RESET (4) of the device as response to bipolar voltage sweeping.

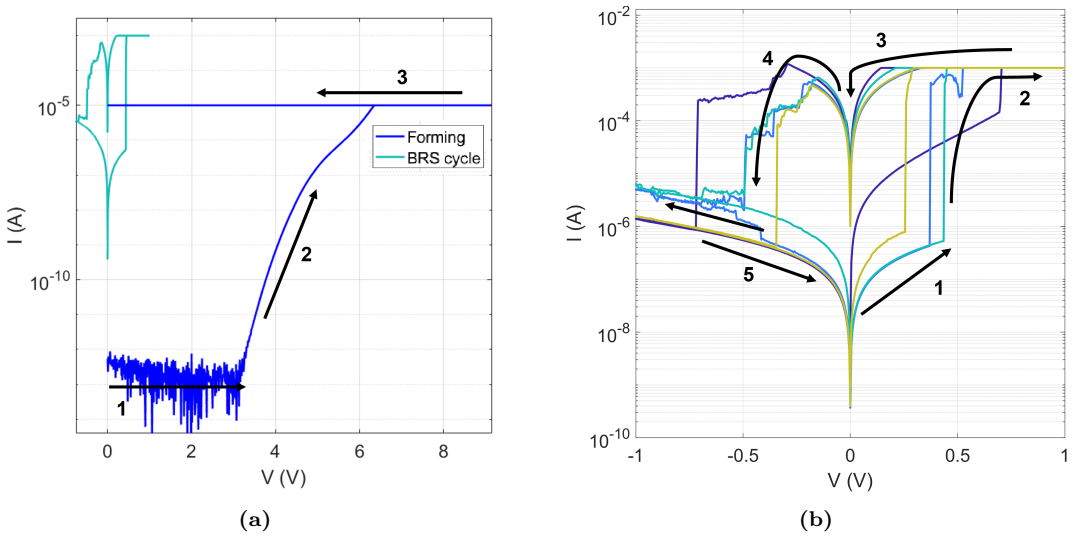


Figure 4.2: Sample $Pt/Al_2O_3/Ag$ (*Alu10*). (a) Forming of one device at $10\,\mu A_{(CC)}$ and one representative BRS cycle at $1\,mA_{(CC)}$. (b) Current-voltage response of four BRS cycles from sample *Alu10* at $1\,mA_{(CC)}$.

$Pt/SiO_2{+}Al_2O_3/Ag$ & $Pt/Al_2O_3{+}SiO_2/Ag$

The DC characterization of $SiO_2{+}Al_2O_3$(top) double-layer stacks shows volatile behaviour when operated at low CC However, when driven at high CC, such as 1 mA, TS is only possible for the first two TS cycles just after forming (see detailed data analysis in Appendix A about samples *Alu1T* (A.1) and *Alu2T* (A.2) in Figures A.3 and A.6). Moreover, sample *Alu2T* shows volatile switching at $I_{CC} = 100\,nA$, whereas its behaviour is mainly non-volatile already at $10\,\mu A_{(CC)}$.

A peculiar case, is the behaviour of sample *Alu2B* which can show both volatile and non-volatile behaviour at $I_{CC} = 100\,nA$ depending on the forming process conditions.

In Figure 4.3a, I report some representative I-V for the non-volatile operation: one forming process and nine BRS cycles at $10\,\mu A_{(CC)}$ are depicted. Arrows in Figure 4.3b indicate the steps of current response to the bipolar voltage sweep mode.

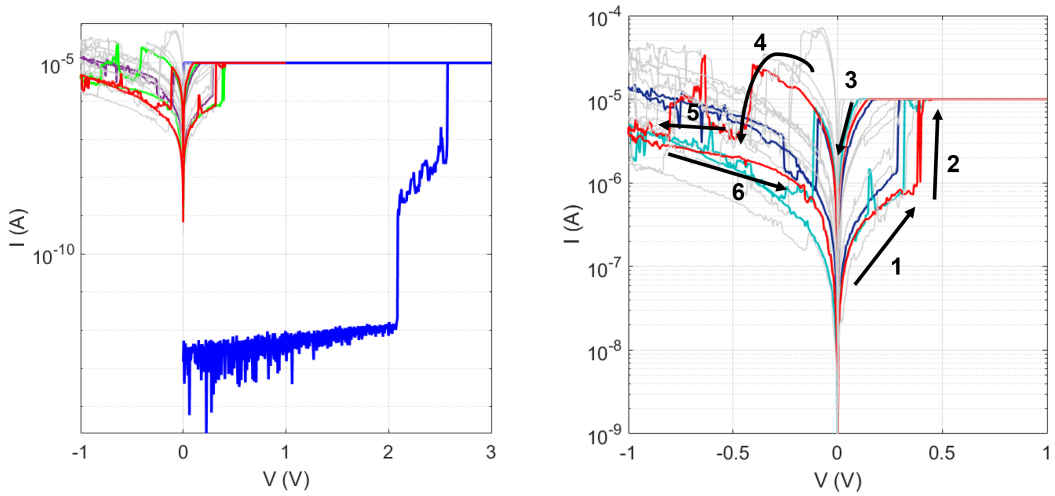


Figure 4.3: Sample Pt/2.5nm Al_2O_3/10nm SiO_2/Ag (*Alu2B*). (a) I-V response of a representative forming process (blue) and some BRS cycles of one device at $100\,nA_{(CC)}$. (b) Some representative bipolar resistive switching current responses at $100\,nA_{(CC)}$.

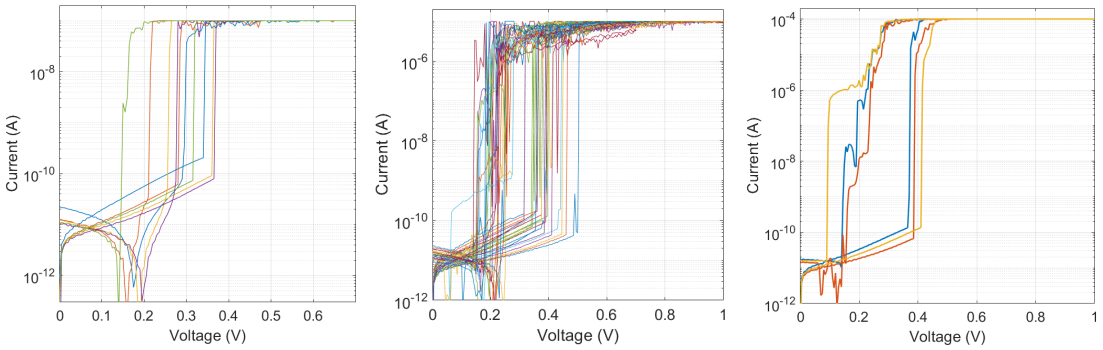
In the following chapters, I focus my attention on samples exhibiting volatile behaviour. I investigate forming characteristics and TS in all samples that can show a volatile operation.

4.2 Detailed analysis of volatile switching of Pt/SiO_2/Ag

In this chapter I show the results on the electrical characterization of sample *Si10*, made of a 10 nm SiO_2 dielectric layer (Pt/SiO_2/Ag): see Figure 3.1a. I consider CC values of $100\,nA$, $10\,\mu A$ and $100\,\mu A$. Statistical analysis on DC endurance and device-to-device variability is carried out.
For the threshold switching endurance test, 1 $mA_{(CC)}$ is also tested to check if the device can support this high value to operate in the volatile regime.

4.2.1 Forming

Figure 4.4 depicts the I-V curves of the forming process of different devices acquired setting $100\,nA_{(CC)}$, $10\,\mu A_{(CC)}$ and $100\,\mu A_{(CC)}$, respectively: each color corresponds to the forming of a different device.



(a) Forming @100 $nA_{(CC)}$ **(b)** Forming @10 $\mu A_{(CC)}$ **(c)** Forming @100 $\mu A_{(CC)}$

Figure 4.4: Sample $Pt/SiO_2/Ag$: the superposition of the forming process of a variable number of devices for CC 100nA (a), 10uA (b) and 100uA (c) is shown from left to right, respectively.

Each trace is characterized by a different value of V_f and leakage current ($I_{leakage}$), defined as the current value evaluated in the off-state in correspondence of 0.15 V before the device switches to the ON state. So, I consider the variability of the detected V_f values, taken from all formed devices, as the Cumulative Distribution Function (CDF) in Figure 4.5a, regardless the CC. Likewise, I plot the CDF of the leakage current in Figure 4.5b, considering all the devices shown in Figure 4.4.

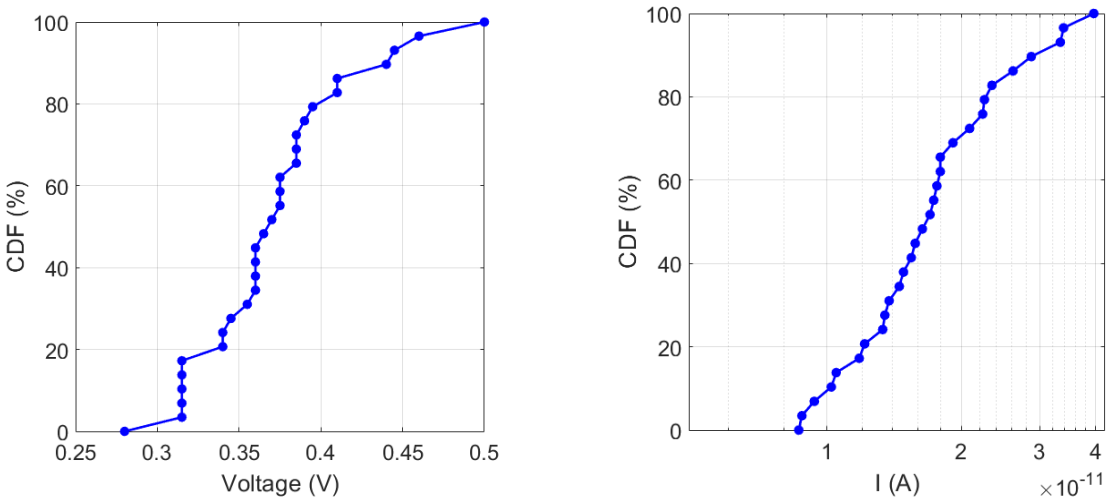


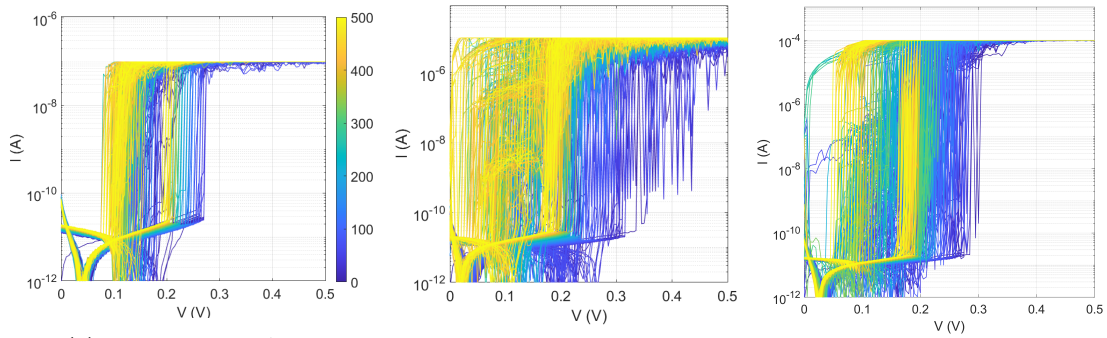
Figure 4.5: Sample $Pt/SiO_2/Ag$. (a) CDF of V_f for each formed device (represented by a dot) regardless the CC. (b) CDF of the leakage current, evaluated during the forming of all devices (at 0.15V) under three CC conditions, varies in the same order of magnitude.

4.2.2 Threshold Switching

In this subsection, I carry out the study of TS on sample *Si10* at various CCs ($100\,nA$, $10\,\mu A$, $100\,\mu A$, $1\,mA$).

I-V characteristics

For this analysis, I perform 500 consecutive threshold switching cycles on one representative device for each of the three tested CCs. Their I-V characteristics are shown in figures 4.6.



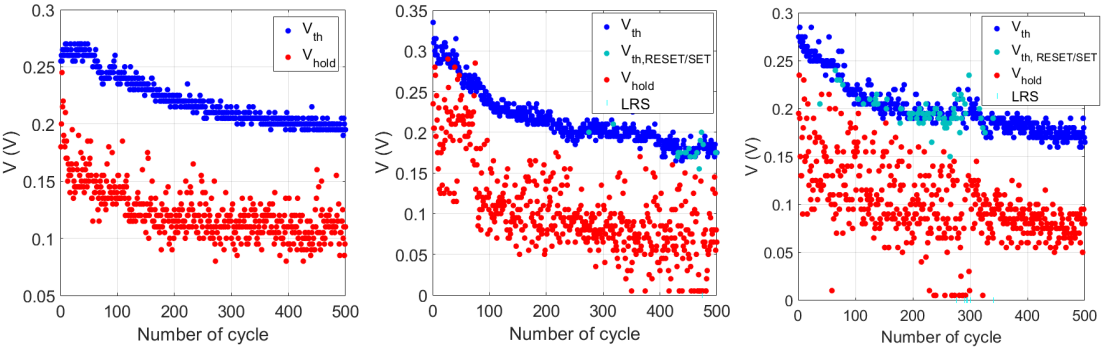
(a) TS I-Vs @100 $nA_{(CC)}$ **(b)** TS I-Vs @10 $\mu A_{(CC)}$ **(c)** TS I-Vs @100 $\mu A_{(CC)}$

Figure 4.6: Sample $Pt/SiO_2/Ag$. Each picture represents one tested CC, 100 nA, 10 μA, 100 μA, respectively. Current response of 500 cycles TS endurance is plotted (y-axis in logarithmic scale). The color of each cycle fades from blue to yellow to indicate the progression along successive TS events.

At a first analysis, I notice that for every tested CC, the threshold voltage V_{th} decreases as the number of TS cycles increases (gradually fading from blue to yellow following the sequence in the color bar of Figure 4.6a). From now on, I will refer to this decrement as *drift*.

V_{th} and V_{hold} variability

To analyse the drift of TS curves, I acquire V_{th} and V_{hold} from each I-V (from the same devices shown in Figure 4.6) and illustrate them as function of number of cycles in Figure 4.7, in blue and red respectively.



(a) TS endurance @100 $nA_{(CC)}$ **(b)** TS endurance @10 $\mu A_{(CC)}$ **(c)** TS endurance @100 $\mu A_{(CC)}$

Figure 4.7: Sample $Pt/SiO_2/Ag$. Evaluation of V_{th} (blue) and V_{hold} (red) as a function of number of cycles on the same devices shown in Figure 4.6, tested at various CCs, 100 nA, 10 μA, 100 μA, respectively. The $V_{th,RESET/SET}$ and LRS points in legends indicate switching failure, concept that will be clear later.

The cycle-to-cycle variation of V_{th} and V_{hold} confirms that both values decrease

increasing the number of TS cycles. Therefore, a drift is present.

So, to study the drift and its relationship with CC, I consider three device for each CC and analyse the first 150 TS cycles, because not all of them are tested for more than 150 cycles. On this range, I compute the difference ΔV_{th} and ΔV_{hold} between the arithmetic mean of V_{th} and V_{hold}, respectively, taken on the first 25 TS cycles, and the mean on the last 25 cycles (125^{th} to 150^{th}). The results are reported in Figure 4.8 for three devices (Dev1 Dev2, Dev3) tested for each CC $100\,nA$, $10\,\mu A$ and $100\,\mu A$.

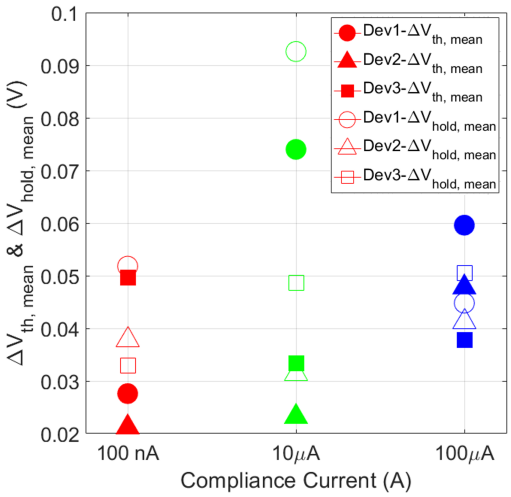
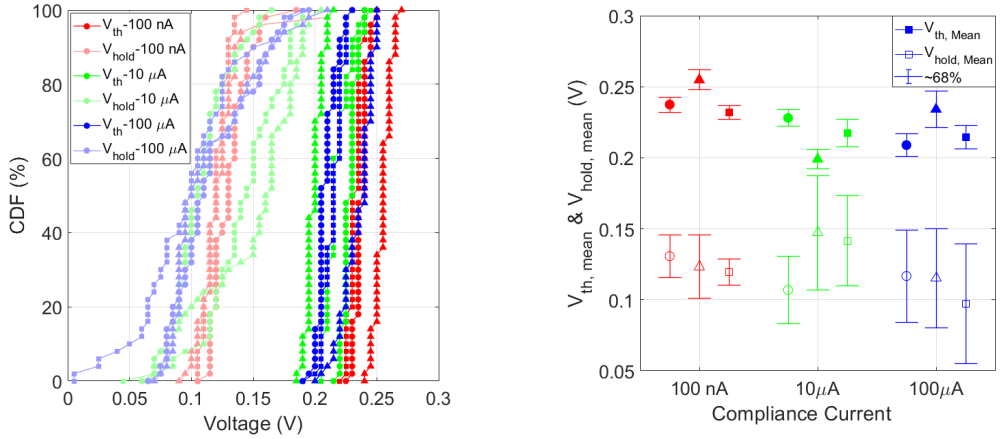


Figure 4.8: Sample $Pt/SiO_2/Ag$. Estimation of the initial drift of V_{th} and V_{hold} on the first 150 TS cycles on three devices for each CC. Each data point corresponds to the evaluation of the difference ΔV_{th} and ΔV_{hold} between initial values of V_{th} and V_{hold} (mean on the first 25 cycles) and last values (mean on the last 25 cycles) of V_{th} (full marker) and V_{hold} (empty marker).

From Figure 4.8 I conclude that there is no meaningful difference between the drift of threshold and hold voltages, and there is no correlation between ΔV_{th}, ΔV_{hold} and the compliance used for the DC endurance.

To evaluate the device-to-device variability of V_{th} and V_{hold} as function of CC, I plot in Figure 4.9a the CDF of V_{th} and V_{hold} detected on cycles 100^{th} to 150^{150}, since in this range the drift is less. Different colors, red, green and blue, represent the different CCs. I consider the same three devices for each CC shown in Figure 4.8. Since I tested minimum 150 TS cycles on each device, I exclude the first 100 rapidly drifting points and perform the calculation of both mean values and variability of V_{th} and V_{hold} on the last 50 cycles. Figure 4.9b shows the arithmetic mean of CDFs in Figure 4.9a and the variability, indicated as an error bar around each average point.



(a) **(b)**

Figure 4.9: Sample $Pt/SiO_2/Ag$. (a) CDF of V_{th} and V_{hold}. Three devices are tested at each CC: $100\,nA$,$10\,\mu A$ and $100\,\mu A$ are coloured in red, green and blue, respectively. Values considered in distribution curves belong to TS cycles going from the 100^{th} to the 150^{th}. (b) Mean value of threshold and hold voltage as function of the CC, for three devices tested at each compliance value ($100\,nA$,$10\,\mu A$ and $100\,\mu A$). The cycles considered for the computation of the mean value go from the 100^{th} to the 150^{th}. Error bars are computed as the standard deviation on the same cycles to give an indication of V_{th} and V_{hold} variability.

There is no dependence of threshold and hold voltage on the CC at which TS is performed. The error bars suggest that the variability of V_{hold} during the endurance test is higher than the variability of V_{th}. In fact, the CDFs of hold voltages are more spread than threshold ones, as already noticeable in Figure 4.7, where hold points, plotted as red dots, are characterized by a larger cycle-to-cycle variability with respect to threshold ones (blue dots).

Volatile switching failures

At higher CC, like $10\,\mu A$ and $100\,\mu A$ in figures 4.7(b-c), some cycles are plotted with a lighter colour, because they show current-voltage curves that do not follow the response path indicated in Figure 3.9b. In this work, these identified cases are called RESET/SET cycles and LRS cycles, and are distinguished in figures 4.7(b-c) with different colours and symbols. The first ones typically follow the characteristic shown in Figure 4.10a: are called like this because the RESET occurs before the SET. In fact, at the beginning of the voltage sweep, the current suddenly reaches a level that is comparable with the CC and then shortly falls back to I_{off}: after this, the actual SET of the device occurs, reaching again the compliance current. These are plotted as light blue dots in figures 4.7(b-c). The second cases, typical response in Figure 4.10b, are characterized by a high current level which remains at least comparable to the CC for the entire duration of the positive sweep (0V to V_{stop}). LRS events are plotted as cyan vertical sticks on the x-axis of figures 4.7(b-c).

While in RESET/SET events a SET can be distinguished, in the latter this is not possible, that is no V_{th} cannot be extracted. Threshold voltages associated to RESET/SET events are included in all V_{th} analysis presented in previous figures.

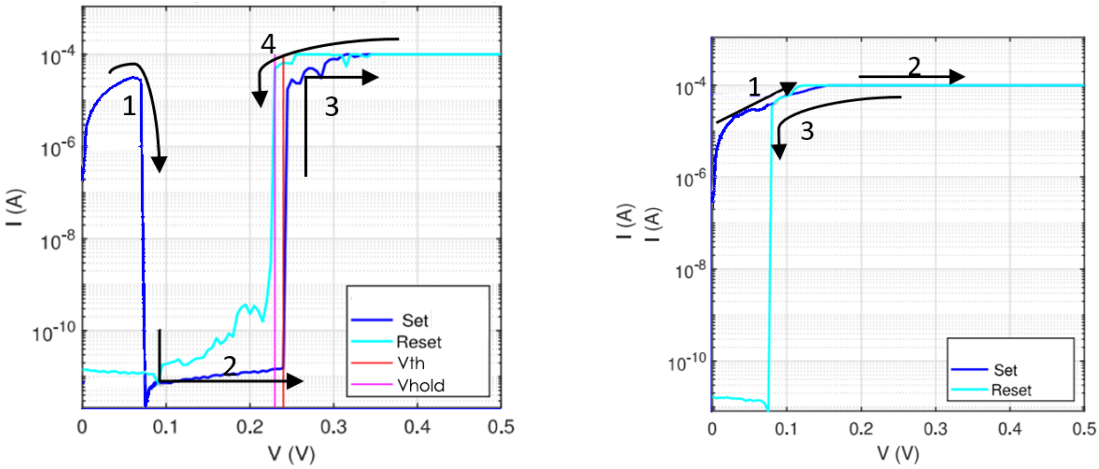


Figure 4.10: Example of RESET/SET (a) and LRS (b) response: different colours represent how they are interpreted by the MATLAB analysis algorithm (explained in Appendix B). Threshold voltages detected in the first case are still considered in cumulative distributions, whereas LRS failures are excluded.

The LRS and RESET/SET electrical behaviours indicate that the retention time of the device at the end of each TS cycle is affecting the state of the device itself at the beginning of the next cycle. The longer the retention, the more likely switching failure events occur. All failures contributions for each set of devices, grouped according to the used current compliance, are reported (Table 4.2), together with the respective failure probability in percentage (with respect to the total number of tested TS cycles on all devices). Performing TS endurance at higher CC leads to a higher probability of total failure events: the more current is allowed to flow through the device, the thicker the filament grows leading to longer retention.

CC	TOT Reset/Set	TOT LRS	% Reset/Set	% LRS
100nA	0	0	0%	0%
$10\mu A$	40	17	2.7%	1.1%
$100\mu A$	148	26	9.9%	1.7%

Table 4.2: Sample $Pt/SiO_2/Ag$. TS failures counted on the total of endurance cycles performed on all devices for each compliance. In the case of $10\mu A_{(CC)}$ and $100\mu A_{(CC)}$ the sum of failures was considered out of a total of 1500 TS cycles, while for I_{CC}=100nA the total number of tested cycles is 1600.

Leakage current variability

From the characterization of DC endurance I also analyse the behaviour of the leakage current, evaluated in the off-state in correspondence of 0.15 V, before the device switches to the ON state. The evolution of $I_{leakage}$ as function of number of cycles is depicted in Figure 4.11 for one representative device for every CC (same devices conseidered in Figure 4.7).

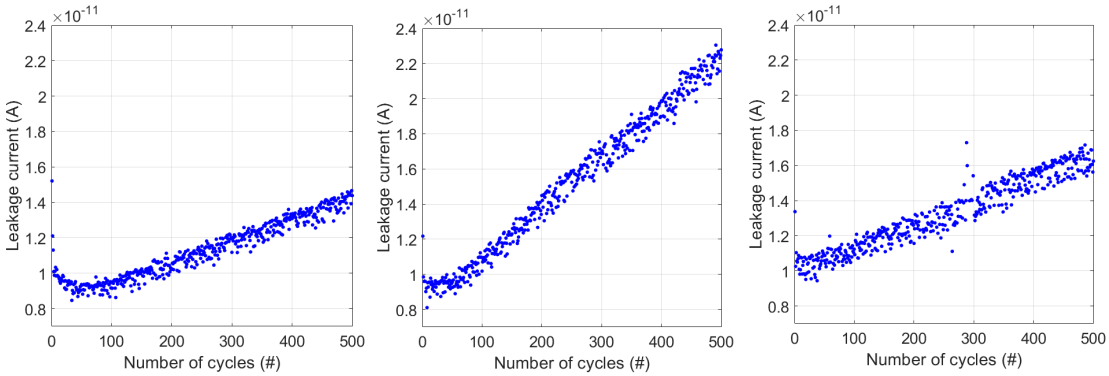


Figure 4.11: Sample $Pt/SiO_2/Ag$. Each plot represents one tested CC, $100\,nA$, $10\,\mu A$, $100\,\mu A$, respectively. Cycle-to-cycle variation of $I_{leakage}$ for each representative device at every CC.

Initially, at every CC, the leakage current $I_{leakage}$ decreases, up to about the 50^{th} cycle, and then gradually increases as the number of TS cycles increases.

Then, I carry out he study of the $I_{leakage}$ drift from the 50^{th} cycle to the 150^{th}. The evaluation is done by computing the difference $\Delta I_{leakage}$ between the arithmetic mean of $I_{leakage}$, taken on the first 25 TS cycles (50^{th} to 75^{th}), and the mean on the last 25 cycles (125^{th} to 150^{th}). The values of $\Delta I_{leakage}$ are reported in Figure 4.12 for three representative devices as function of CC.

It can be observed that during the endurance test, the drift $\Delta I_{leakage}$ is bigger at the CCs $10\,\mu A$ and $100\,\mu A$ than at $100\,nA$.

So, I analyse the cycle-to-cycle and device-to-device variability of $I_{leakage}$ detected

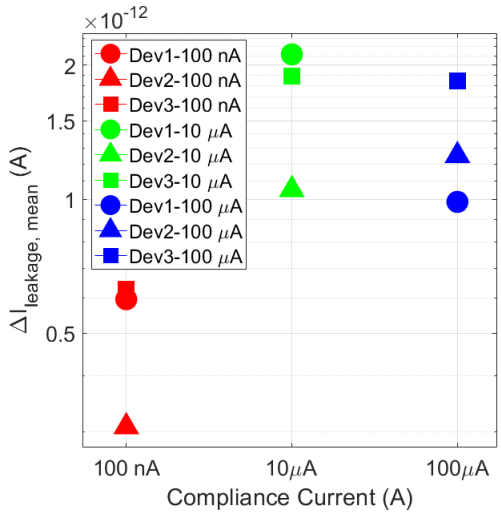


Figure 4.12: Sample $Pt/SiO_2/Ag$. Numerical estimation of the increasing trend of $I_{leakage}$ on 100 TS cycles, on three devices for each CC. Each data point corresponds to the evaluation of the difference $\Delta I_{leakage}$ between the arithmetic mean of $I_{leakage}$, taken on cycles 50^{th} to 75^{th}, and the mean on cycles 125^{th} to 150^{th}.

from cycle 100 to cycle 150, to see if there is any correlation between the average value of the leakage current at saturation (where drift is reduced) and the used value of the CC. Figure 4.13a shows the CDF of $I_{leakage}$ on the same devices analysed in Figure 4.12 for the three CCs, represented in red, green and blue, respectively. Figure 4.13b plots the $I_{leakage}$ arithmetic mean over the same cycles and for the same devices. The variability, computed as the standard deviation of the same cycles, is indicated as an error bar around each average point.

From figures 4.13, I notice that the leakage current, on average, increases with the CC. However, the CC does not affect neither the cycle-to-cycle variability nor the device-to-device variability.

In order to analyse the correlation between V_{th} and $I_{leakage}$, I relate their values, acquired during the 500 cycles endurance test, considering one representative device for each CC. Figure 4.14 depicts V_{th} on y-axis and $I_{leakage}$ on x-axis.

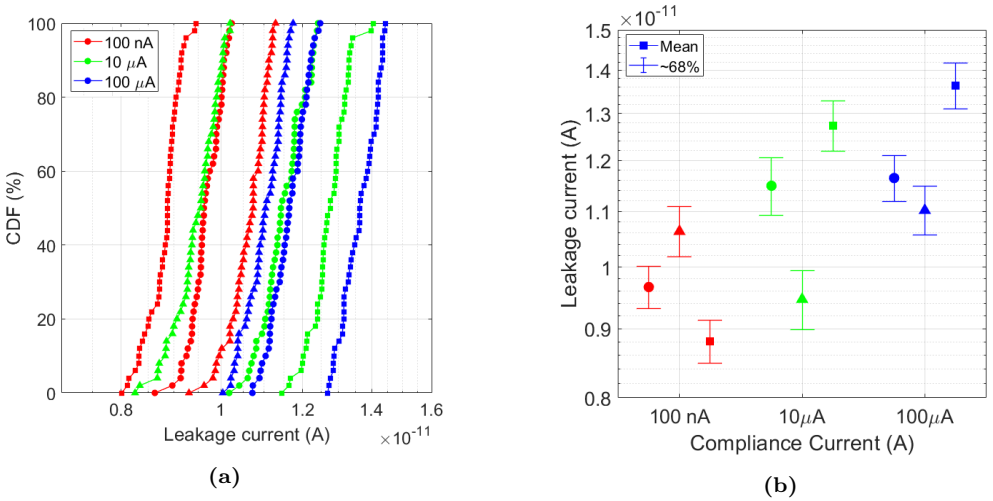


Figure 4.13: Sample $Pt/SiO_2/Ag$. (a) CDF of $I_{leakage}$. Three devices are tested at each CC, $100\,nA$,$10\,\mu A$ and $100\,\mu A$, coloured in red, green and blue, respectively. Values considered in distribution curves belong to TS cycles going from the 100^{th} to the 150^{th}. (b) Mean value of the leakage current as function of the CC, for three devices tested at each compliance value ($100\,nA$,$10\,\mu A$ and $100\,\mu A$). The cycles considered for the computation of the mean value go from the 100^{th} to the 150^{th}. Error bars are computed as the standard deviation on the same cycles to give an indication of $I_{leakage}$ variability.

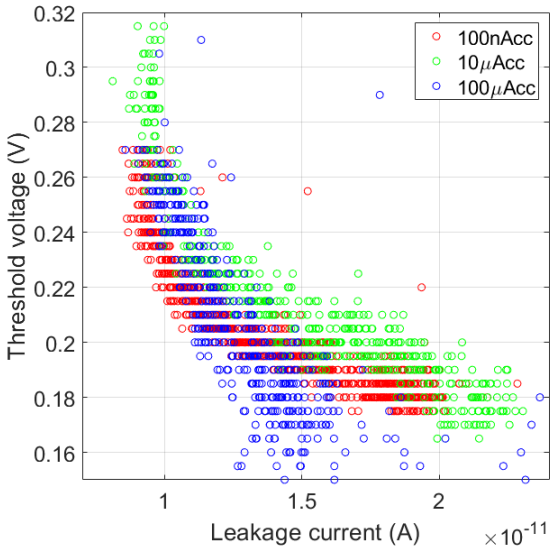


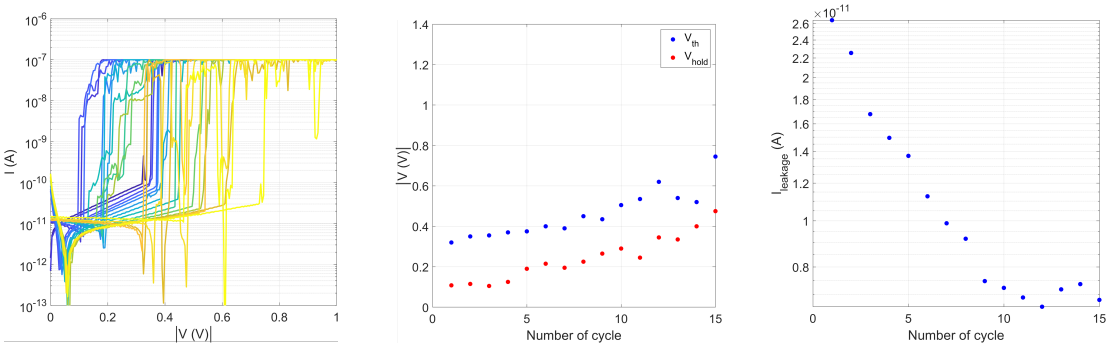
Figure 4.14: The threshold voltage (y-axis) put in relationship with leakage current @0.15 V (x-axis, linear scale) in the OFF state. One representative device is plotted for each CC. V_{th} has a decreasing trend with the increment of $I_{leakage}$.

The three sets of points follow the same trend: the threshold voltage decreases

as the leakage current increases (following the general trend with number of TS cycles).

4.2.3 Negative Threshold Switching

After endurance of TS at 100nA$_{(CC)}$, under positive applied voltage, I test 15 negative TS cycles at the same I_{CC} on one device. Figure 4.15a depicts the current response to negative voltage sweep (0V to -V_{stop}, and then back to 0V) of every cycle. The colour of the I-Vs fade from blue (first cycle) to yellow (last cycle). Figure 4.15b reports the values of V_{th} and V_{hold} for each negative TS cycle. I further consider the leakage current @0.15 V and its cycle-to cycle variation in Figure 4.15c.



(a) **(b)** **(c)**

Figure 4.15: Sample Pt/SiO_2/Ag. (a) Current response to voltage sweep, with $I_{CC} = 100nA$, is plotted for each cycle (x-axis reports the absolute value of voltage, y-axis is in logarithmic scale). Traces colour fade from blue (first cycle) to yellow (last cycle).(b) Cycle-to-cycle variation of V_{th} (blue) and V_{hold} (red). (c) Cycle-to-cycle variation of $I_{leakage}$.

From Figure 4.15a and Figure 4.15b I notice that the absolute values of both V_{th} and V_{hold} increase with the number of negative cycles. On the other hand, $I_{leakage}$ decreases as negative cycling goes on. Finally, I consider the relationship between V_{th} (on y-axis) and $I_{leakage}$ (on x-axis) in Figure 4.15c.

An additional graph (Figure 4.16) puts in relationship V_{th}, on y-axis, to $I_{leakage}$, on x-axis, similarly to what done for positive TS. The relationship is clear: the higher the $I_{leakage}$, the lower the V_{th}.

4.2.4 Summary

In the following list, I report the features of the analysed sample:

- It is possible to perform several TS cycles at different CC ranging from 100 nA to 1 mA.

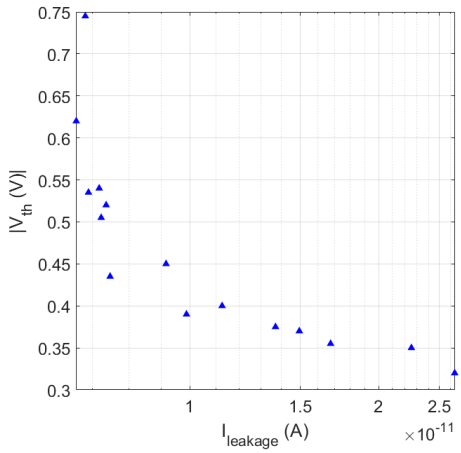


Figure 4.16: The threshold voltage (y-axis) put in relationship with leakage current (x-axis, log scale). V_{th} has an increasing trend with the decreasing of $I_{leakage}$ (following the cycle-to-cycle trend).

- Devices can sustain high endurance and have a good reproducibility.
- V_{th} decreases as function of the number of TS cycles at positive applied voltage.
- $I_{leakage}$ increases with number of TS cycles after the first $\sim$ 100 cycles at positive applied voltage.
- V_{th} relationship with $I_{leakage}$ is clear and is inversely proportional during positive TS.
- Number of switching failures increases with CC.
- Negative TS is possible for at least 15 cycles
- V_{th} relationship with $I_{leakage}$ is inversely proportional during negative TS.

4.3 Effect of stack composition on volatile switching at 100nA

This section is focused on the comparison of the results from DC measurements on samples *Si10*, Pt/10 nm SiO_2/Ag, *Alu1T*, Pt/10 nm SiO_2/1 nm Al_2O_3/Ag, *Alu2T*, Pt/10 nm SiO_2/2.5 nm Al_2O_3/Ag, *Alu2B*, Pt/2.5 nm Al_2O_3/10 nm SiO_2/Ag, to study the effect of different bi-layer insulating stacks. In the first subsection I present data acquired from DC analysis on samples Pt/10 nm SiO_2/1 nm Al_2O_3/Ag and Pt/10 nm SiO_2/2.5 nm Al_2O_3/Ag to explain the effect of introducing an alumina layer, on top of the insulating stack, on the device switching capabilities. The second subsection shows the DC analysis on sample Pt/2.5 nm Al_2O_3/10 nm SiO_2/Ag to study the effect of introducing an alumina layer, at the bottom of the insulating stack, that is at the Pt/SiO_2 interface. Since this thesis targets volatile ECM cells, I proceed analysing the forming and TS endurance of each sample all samples at $100\,nA_{(CC)}$, that is the only CC at which all samples show a volatile behaviour. A study on the negative threshold switching is also addressed for every sample. At the end of this section I report the discussion of the obtained results and give final considerations on the tested devices.

4.3.1 Effect of top alumina

The aim of this subsection is to introduce the most important figures of merit of samples Alu1T and Alu2T and to compare the analysed data to the sample Si10, so to provide a study of the effect of inserting 1 nm and 2.5 nm alumina layer on top of 10 nm SiO_2.

Forming

Figure 4.17 shows depicted the I-V curves of the forming process of different devices acquired at $100\,nA_{(CC)}$ on samples with 1 nm alumina and 2.5 nm alumina on top of the stack (in purple and blue, respectively).

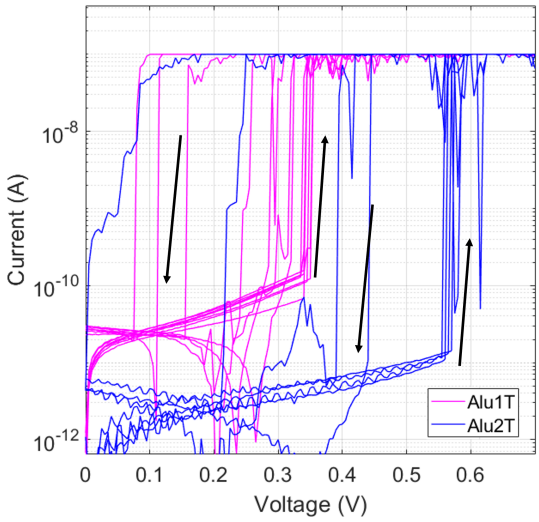


Figure 4.17: Samples Alu1T (Pt/10nm SiO_2/1nm Al_2O_3/Ag) and Alu2T (Pt/10nm SiO_2/2.5nm Al_2O_3/Ag. I-V characteristic of the forming process of a variable number of devices for sample Alu1T (purple) and Alu2T (blue) at the CC of 100 nA.

An indication on the device-to-device variability and differences from sample to sample of V_f and $I_{leakage}$, taken at 0.15V, is given by the CDFs in figures 4.18(a-b). Samples Alu1T (magenta) and Alu2T (blue) are compared to sample Si10 (red).

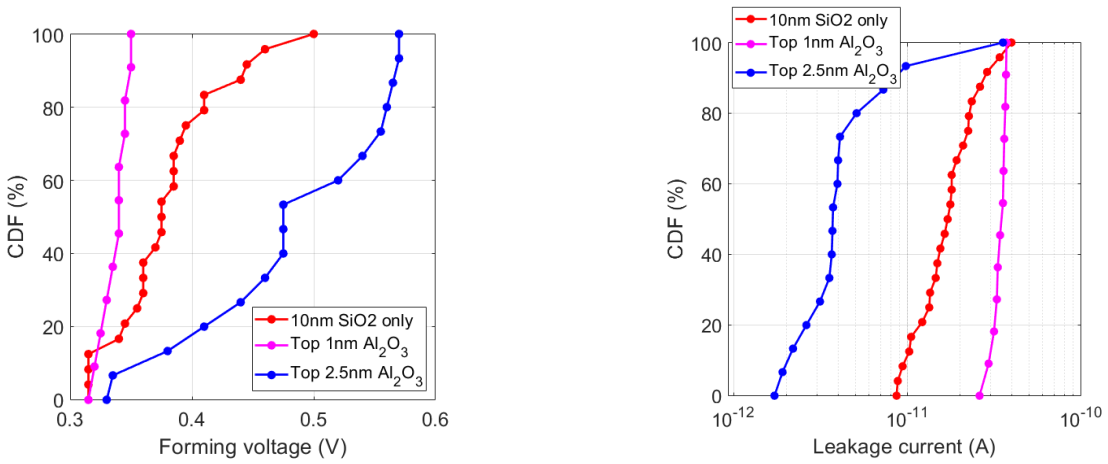


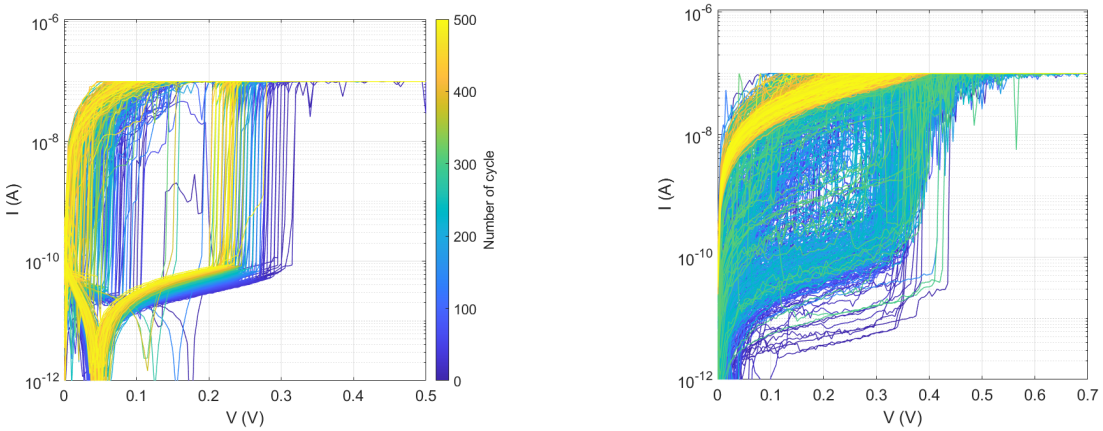
Figure 4.18: Samples Si10, Alu1T, Alu2T. CDF of forming voltage (a) and leakage current at 0.15V (b). Values taken from Alu1T are within the variability of Si10, so the slight difference can be attributed to sample-to-sample variability.

During forming, 2.5 nm top alumina increases the mean V_f and decreases $I_{leakage}$.

However, differences between Si10 and Alu1T can be attributed to sample-to-sample variability, since V_f and $I_{leakage}$ values fall within the variability of V_f and $I_{leakage}$ of sample Si10 (Figure 4.18).

Threshold Switching

In this subsection, I report the study of TS on samples Alu1T and Alu2T at $100\,nA_{(CC)}$.
I-V characteristics of 500 consecutive TS cycles on are shown in Figure 4.19: left picture depicts the characteristics of one representative device of sample Alu1T, while on the right I plot one representative device of sample Alu2T. On sample Alu2T, the TS endurance measurements is performed with hold time t_{hold}=2 s, that is the waiting time between the end of one voltage sweep and the next measurement, to let the self relaxation of the memory take place. I tested t_{hold} of 0 s, 1 s and 2 s. A t_{hold} of 2 s, is found to be the minimum sufficient time, for devices on sample Alu2T, to achieve more than 100 TS successive switching events at $100\,nA_{(CC)}$ without showing switching failures.



(a) **(b)**

Figure 4.19: Sample Alu1T (Pt/10nm SiO_2/1nm Al_2O_3/Ag) on the left, sample Alu2T (Pt/10nm SiO_2/2.5nm Al_2O_3/Ag) on the right. Current response to voltage sweep, with $I_{CC} = 100nA$, is plotted for 500 TS cycles (y-axis in logarithmic scale). The colour of I-V traces fades from blue to yellow to indicate the progression on both V_{th} and V_{hold} along the TS events.

On sample Alu1T, like in sample Si10, I-Vs colours in Figure 4.19a, fading from blue to yellow following the sequence in the color bar, indicate the clear presence of a decrement (drift) of the threshold voltage as the number of TS cycles increases. On sample Alu2T, instead, no clear decreasing trend of V_{th} is visible.

To better visualize the the cycle-to-cycle variation of V_{th} and V_{hold} for the same representative devices in Figure 4.19, I illustrate their values in Figure 4.20 over

500 TS cycles, in blue and red, respectively.

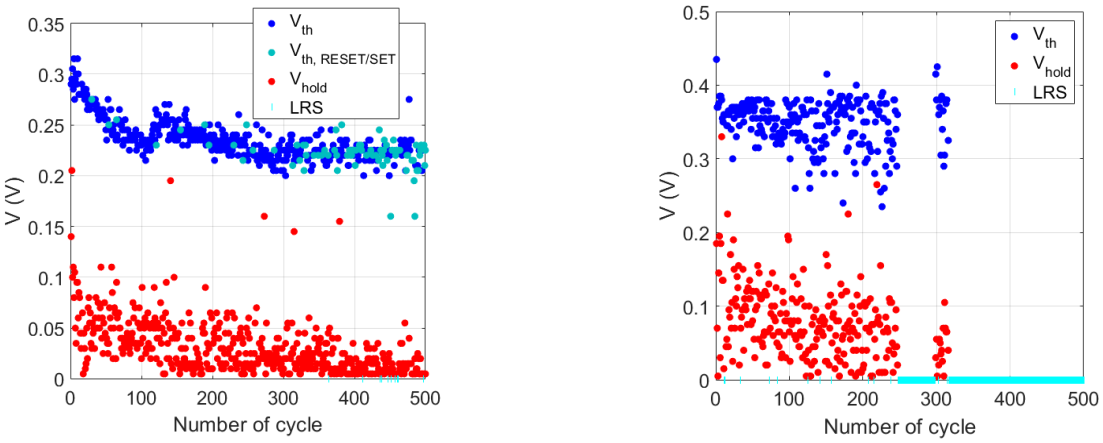


Figure 4.20: Cycle-to-cycle variation of V_{th} (blue) and V_{hold} (red) at $100\,nA_{(CC)}$ for 500 TS cycles on sample Alu1T (Pt/10nm SiO_2/1nm Al_2O_3/Ag) on the left, and sample Alu2T (Pt/10nm SiO_2/2.5nm Al_2O_3/Ag) on the right.

The drift of V_{th} on Alu1T is observable, especially up to 100 TS cycles, while on Alu2T the behaviour of threshold voltage as function of number of cycles consists of an increasing cycle-to cycle variability as the number of switching events increases. Both devices tend to show more LRS switching failures as I apply more TS cycles. Particularly, on the representative device for Alu2T, even though I set a higher t_{hold} (2 s) in the measurement settings, it is difficult to perform TS endurance for more than 250 cycles, as visible in Figure 4.20b: after cycle 250, all cycles go to LRS, and it is necessary to stop the measurement (at the 300^{th} cycle) to restore the volatile switching.

Figure 4.21 depicts the threshold voltage (y-axis) of five devices for each sample put in relationship with the number of TS cycles. Values are plotted superimposed up to 150 TS cycles; not all devices are tested up to 150 endurance cycles.

On average, samples show a V_{th} decreasing trend with the increment of endurance cycles. However, data from sample Alu2T have a very large cycle-to-cycle variability.

The results from the statistical analysis on V_{th} and V_{hold} are reported in Figure 4.22a. It shows three typical TS I-V characteristics taken after the forming of the samples under study. To see the difference between the values of V_{th} and V_{hold} from sample to sample and from device to device, I plot in Figure 4.22b their mean value, for five devices for each sample. The cycles considered for the computation of the mean value go from the 50^{th} to the 100^{th}. Error bars are computed as

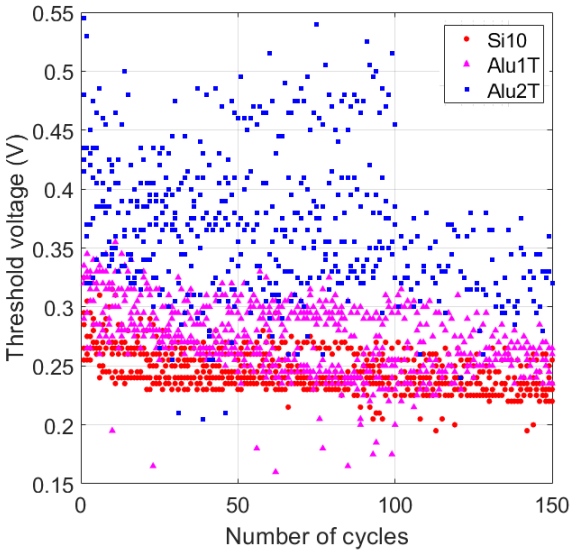
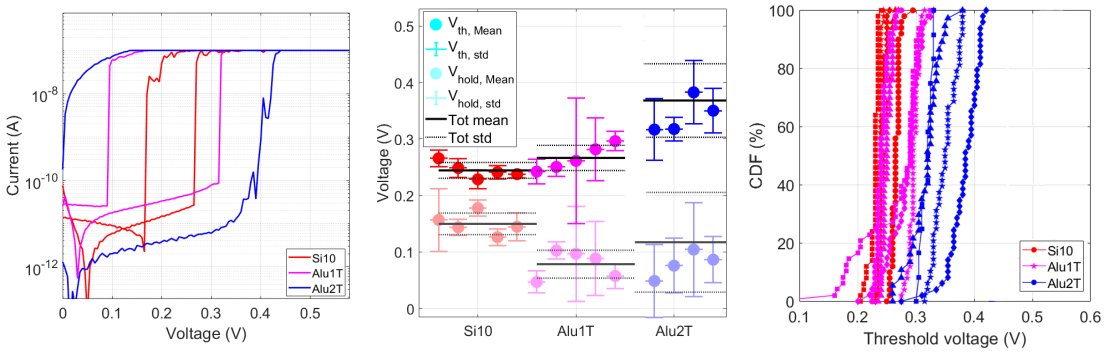


Figure 4.21: Samples Si10 (Pt/10nm SiO_2/Ag), Alu1T (Pt/10nm SiO_2/1nm Al_2O_3/Ag) and (Pt/10nm SiO_2/2.5nm Al_2O_3/Ag). Threshold voltage (y-axis) put in relationship with number of TS cycles. Five devices are plotted superimposed for each sample up to 150 TS cycles: not all devices are tested up to 150 endurance cycles. On average, samples show a V_{th} decreasing trend with the increment of endurance cycles. However, data from sample Alu2T have a very large cycle-to-cycle variability.

the standard deviation on the same cycles to give an indication of V_{th} and V_{hold} variability. Figure 4.22c plots the CDFs of V_{th} of five devices tested at $100\,nA_{(CC)}$ for samples Si10, Alu1T, Alu2T, coloured in red, magenta and blue, respectively. Values considered in distribution curves belong to TS cycles going from the 50^{th} to the 100^{th}.

As the thickness of the alumina layer on top of SiO_2 increases, the threshold voltage increases. Adding an alumina layer ha also an influence on the hold voltage (depicted in lighter colours) which is lower with respect to values obtained on only SiO_2 switching layer. The larger cycle-to-cycle variability of threshold voltage of Alu2T is confirmed by the CDFs in blue depicted in Figure 4.22c that are wider than red (Si10) and magenta ones (Alu1T).

In Figure 4.23 I plot the leakage current cycle-to-cycle variability of one representative device, tested with DC endurance up to 500 TS cycles, for sample Si10, Alu1T and Alu2T to show the differences in their behaviour. $I_{leakage}$ is acquired in correspondence of 0.15 V.



(a) **(b)** **(c)**

Figure 4.22: Samples Si10, Alu1T, Alu2T. (a) Three typical TS I-V characteristics taken few cycles after the forming of samples Si10, Alu1T, Alu2T coloured in red, magenta and blue, respectively. (b) Mean value of threshold and hold voltage for some devices tested on each sample at $100\,nA_{(CC)}$. The cycles considered for the computation of the mean value go from the 50^{th} to the 100^{th}. Error bars are computed as the standard deviation on the same cycles to give an indication of V_{th} and V_{hold} variability. (c) CDF of V_{th}. Five devices are tested at $100\,nA_{(CC)}$ for samples Si10, Alu1T, Alu2T, coloured in red, magenta and blue, respectively. Values considered in distribution curves belong to TS cycles going from the 50^{th} to the 100^{th}.

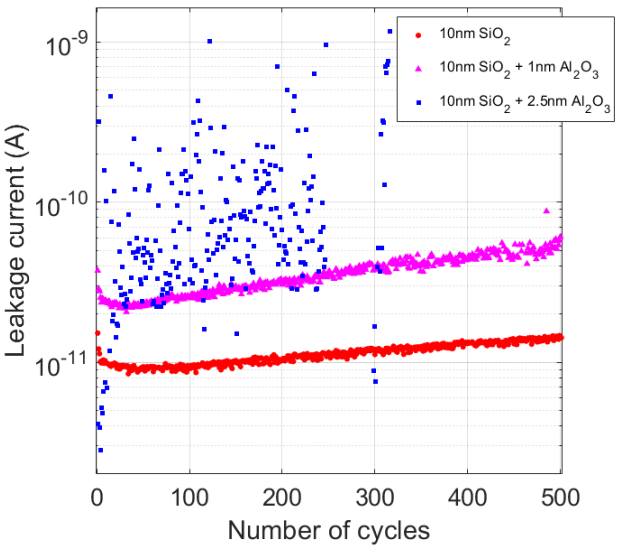


Figure 4.23: Samples Si10, Alu1T, Alu2T. Leakage current @0.15 V of one representative device for samples Si10, Alu1T, Alu2T. Initially, $I_{leakage}$ decreases until it reaches a minimum. After that, it keeps increasing as more switching events take place.

Sample Alu1T shows a $I_{leakage}$ which increases with the number of applied cycles. Like in SiO_2 stack, in the first cycles (1-50) the leakage decreases until it reaches a minimum. After that, it keeps increasing as more switching events

take place. Moreover, the slope of $I_{leakage}$ in Alu1T is slightly higher than in Si10. Concerning sample Alu2T, leakage values of each cycle are spread on a wide current range ($\sim 10^{-12} - 10^{-9}$) and on average they are bigger than $I_{leakage}$ in Si10 and Alu1T. Interestingly, the leakage in sample Alu2T increases within the first 50 TS cycles, then reaches an average level that not only is higher than the one extracted during the forming process (see Figure 4.18b), but is also higher than values taken on samples Si10 and Alu1T. Even though before the forming process the $I_{leakage}$ is higher in Si10 than in Alu2T (Figure 4.18b), during TS Si10 has lower $I_{leakage}$ than Alu2T. It is noticeable also in the first TS cycle (Figure 4.22a).

Then, I relate the endurance cycle-to-cycle variation of V_{th} to the cycle-to-cycle variation of $I_{leakage}$, considering one representative device for each sample. Figure 4.24 depicts V_{th} on y-axis and $I_{leakage}$ on x-axis. The sets of points belonging to samples Si10 and Alu1T follow the same trend: the threshold voltage decreases as the leakage current increases (following the general trend with number of TS cycles). Even though data from Alu2T are characterized by a larger variability, it is clear that with the increasing of the alumina thickness on top of SiO_2 the points on the graph move from bottom left (low V_{th}, low $I_{leakage}$) to top right (high V_{th}, high $I_{leakage}$).

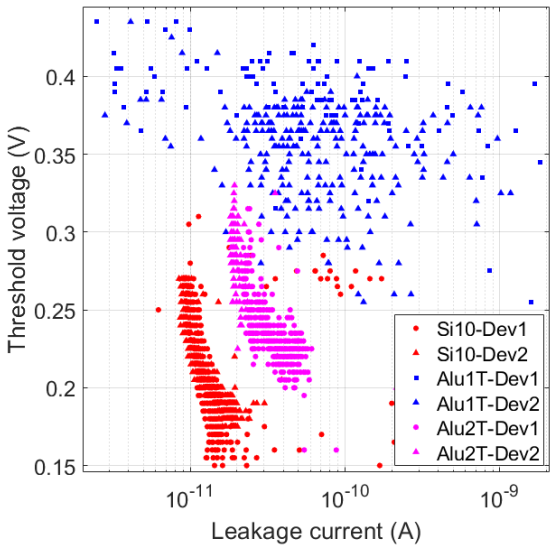


Figure 4.24: Samples Si10, Alu1T, Alu2T. The threshold voltage (y-axis) put in relationship with leakage current @0.15 V (x-axis, linear scale). Two representative devices are plotted for each sample. V_{th} has a decreasing trend with the increment of $I_{leakage}$, but.

Negative Threshold Switching

Alu1T and Alu2T samples are analysed with negative voltage sweeps to achieve

negative TS. The ability to show negative threshold switching just after positive TS endurance, is addressed. I-V characteristics of a variable number of negative cycles, are plotted in Figure 4.25 with voltage axis shown as its absolute value. First cycles are depicted in blue, whereas last ones are depicted in yellow.

I analyse one representative device for each of the samples: few cycles are tested and the value of $I_{leakage}$ is extracted in correspondence of $-0.15V$. Figure 4.25 shows the I-V traces for the three tested devices.

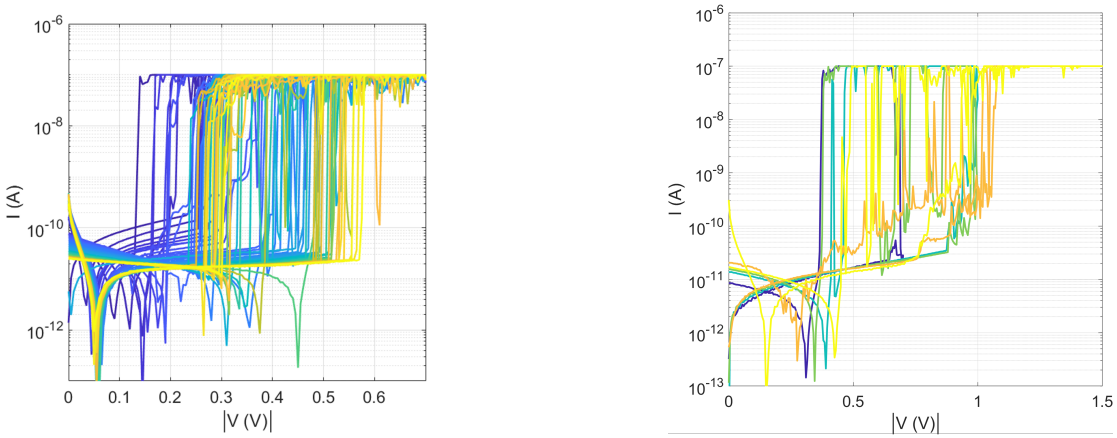
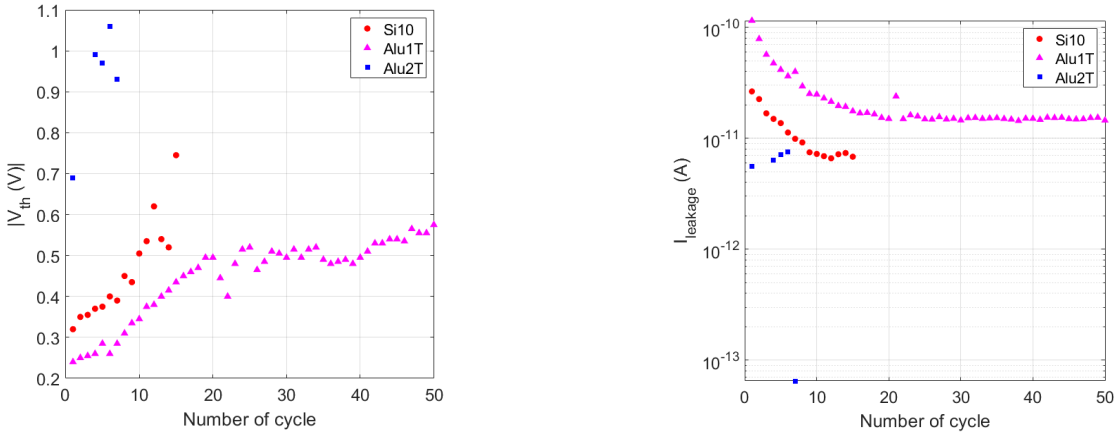


Figure 4.25: (a) Negative Threshold Switching current response of one representative device belonging to sample *Alu1T* (a) and *Alu2T* (b), respectively. A variable number of negative cycles is applied. Traces are coloured from blue, first cycle, to yellow, last cycle.

From Figure 4.25a and Figure 4.25ait is clear that while V_{th} increases as more negative cycles are applied, the leakage current decreases. The same devices are used for the comparison of the cycle-to-cycle variation of threshold voltage (Figure 4.26a) and leakage current (Figure 4.26b) during negative threshold switching, with sample $Pt/SiO_2/Ag$.



(a) **(b)**

Figure 4.26: (a) Negative TS cycle-to-cycle variation of V_{th}, considering one device for each of the three samples that can switch with negative TS cycles. Considered devices are all formed with a CC of 100 nA, and stressed for at least 150 positive consecutive TS cycles at the same compliance.(b) Cycle-to-cycle variation of the leakage current, evaluated during the negative threshold switching of the same devices shown in (a). $I_{leakage}$ was evaluated in correspondence of $-0.15V$.

The trend of V_{th} and $I_{leakage}$ noticed above is confirmed. Moreover, the addition of 1 nm alumina layer in the stack induces the negative switching voltage to be lower and the leakage current to be higher than values obtained from the sample $Pt/SiO_2/Ag$. Sample with 2.5 nm alumina layer on top of the stack, shows higher V_{th} than the other to samples, and its $I_{leakage}$ has same values of sample Si10 without drifting. Another figure that shows the difference between samples in both V_{th} and $I_{leakage}$ is the following (Figure 4.27), which reports threshold voltage in relation to leakage current. From the plot I can say that, in general, the lower leakage current, the higher threshold voltage.

Summary

In the following list, I report the features of sample Alu1T:

- It is possible to perform at least TS cycles at different CCs ranging from 100 nA to 10 μA (see Appendix A.1).
- V_{th} decreases as function of the number of TS cycles at positive applied voltage.
- $I_{leakage}$ increases as function of TS cycles after the first $\sim$ 50 cycles at positive applied voltage.
- V_{th} relationship with $I_{leakage}$ is clear and is inversely proportional during positive TS.

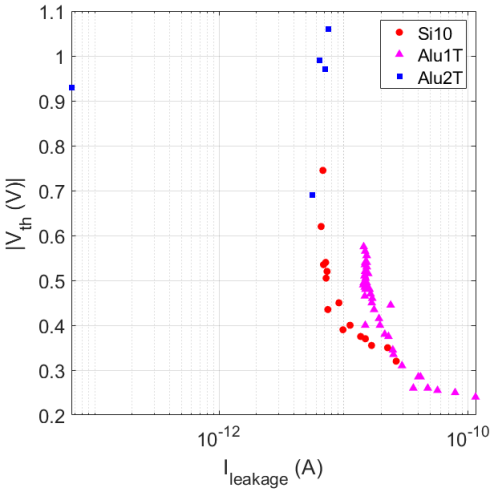


Figure 4.27: Threshold voltage in relation to the leakage current, evaluated at $-0.15V$ of the I-V response. One device for each sample is tested with negative TS, and values are indicated with a different colour.

- Negative TS is possible for at least 50 cycles
- V_{th} relationship with $I_{leakage}$ is inversely during negative TS.

The following list, reports the features of sample Alu2T:

- To perform at least 100 TS cycles at CC of 100 nA, I must set a t_{hold} of 2 s to support the long retention time of the device and to guarantee the volatile operation. TS at $10\,\mu A_{(CC)}$ and $1\,mA_{(CC)}$ is only possible for very few cycles.
- V_{th} decreases as function of the number of TS cycles, at positive applied voltage, even though there is a large cycle-to-cycle variability.
- $I_{leakage}$ during TS has a very large variability at positive applied voltage. No clear trend is detectable .
- V_{th} relationship with $I_{leakage}$ is not clear, since both values have a large variability.
- Negative TS is possible for at least 5 cycles

4.3.2 Effect of bottom alumina

This subsection shows the results on I-V measurements of sample Alu2B (Pt/2.5 nm Al_2O_3/10 nm SiO_2/Ag) and compares the analysed figures of merit to the data

obtained from sample Si10. The aim is to provide information for the study of the effect of putting 2.5 nm alumina layer at the bottom of 10 nm SiO_2.

Forming

Figure 4.28 depicts the I-V curves of the forming process of different devices acquired at $100\,nA_{(CC)}$. Each current response is plotted in different colour is used to distinguish between set (blue,from 0V to V_{stop}) and reset process (light blue, V sweep back to 0V).

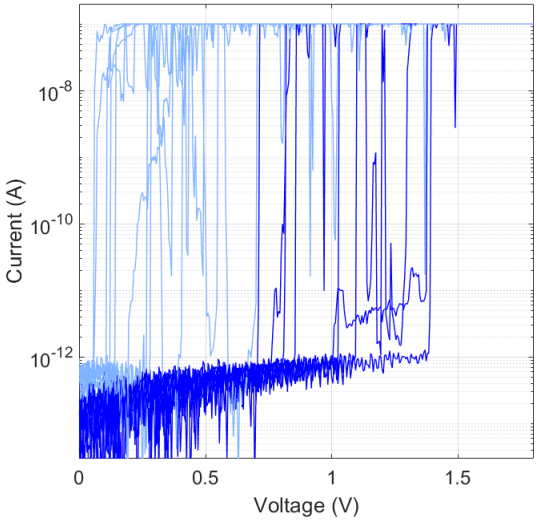


Figure 4.28: Sample Pt/2.5 nm Al_2O_3/10 nm SiO_2/Ag. Superposition of the forming process of an arbitrary number of devices at the CC of 100 nA. To visually distinguish between set and reset processes, current responses to voltage sweeping from 0V to V_{stop} is coloured in darker blue, while they are lighter during V sweep back to 0V.

The device-to-device variability of V_f and $I_{leakage}$, taken at 0.15V, on samples Si10 and Alu2B, are illustrated in the CDFs of Figure 4.29a and Figure 4.29b. Sample Alu2B (cyan) is compared to sample Si10 (red).

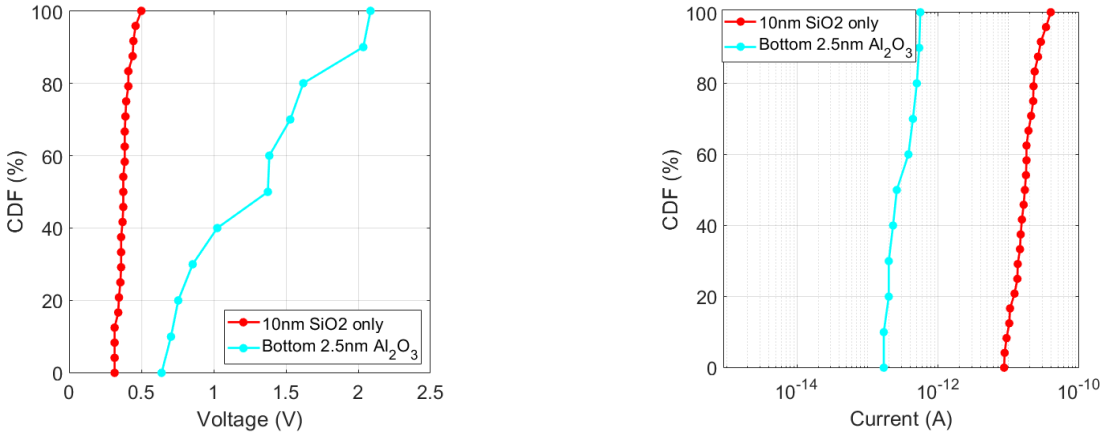


Figure 4.29: Samples Si10 and Alu2B. CDF of forming voltage (a) and leakage current at 0.15V (b).

During forming, 2.5 nm bottom alumina induces a reduction of about two orders of magnitude of $I_{leakage}$ and increases V_f. However, the device-to-device variability of the forming voltage is very high, from a minimum of 0.6 V to a maximum of 2.1 V.

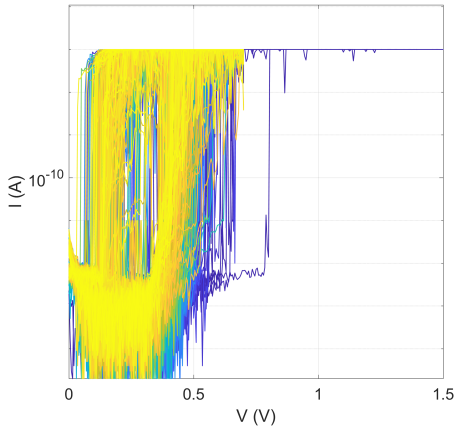
Threshold Switching

Current-voltage characteristics in Figure 4.30 represent 500 consecutive threshold switching cycles (fading from blue, first cycle, to yellow, last cycle) on one representative device.

After the very first TS cycles (depicted in dark blue), where the threshold voltage is high, V_{th} varies around a mean value for the rest of the endurance test. To understand the evolution of V_{th} and V_{hold}, I illustrate in Figure 4.31 the cycle-to-cycle variation of V_{th} (blue) and V_{hold} (red) over 500 TS cycles.

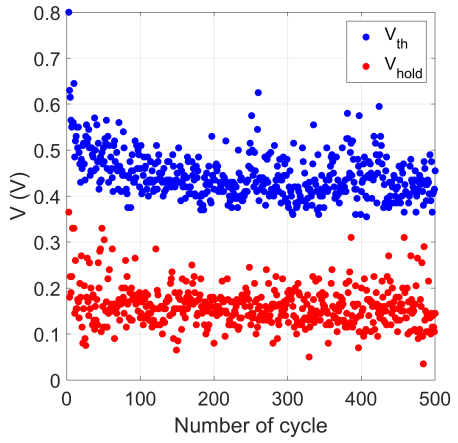
Figure 4.32 depicts the threshold voltage (y-axis) of five devices for each sample put in relationship with the number of TS cycles. Values are plotted superimposed up to 150 TS cycles: not all devices are tested up to 150 endurance cycles.

Threshold voltage is always higher in sample with 2.5 nm alumina at the bottom of SiO_2, with respect to only SiO_2 switching layer. In fact, as depicted in Figure 4.33a, two typical I-V characteristics, taken after the forming of the samples under study (at $100\,nA$ CC), show the difference in the V_{th}, as well as in the $I_{leakage}$. Sample to sample difference and device-to-device variability of V_{th} and V_{hold} are plotted in Figure 4.33b. In this picture, dots indicate their mean value for five devices and for each sample (Si10 in red, Alu2B in cyan). Error bars are computed as the standard deviation on the same cycles to give an indication of V_{th} and V_{hold} variability. The cycles considered for the computation of the mean value go from the 50^{th} to the 100^{th}. Figure 4.33c plots the CDFs of V_{th} of five devices tested



(a)

Figure 4.30: Sample Alu2B (Pt/2.5 nm Al_2O_3/10 nm SiO_2/Ag). Current response to voltage sweep, with $I_{CC} = 100nA$, is plotted for 500 TS cycles (y-axis in logarithmic scale). The colour of I-V traces fades from blue to yellow to indicate the progression on both V_{th} and V_{hold} along the TS events.



(a)

Figure 4.31: Sample Alu2B (Pt/2.5 nm Al_2O_3/10 nm SiO_2/Ag). Cycle-to-cycle variation of V_{th} (blue) and V_{hold} (red) at $100\,nA_{(CC)}$ for 500 TS cycles.

at $100\,nA_{(CC)}$ for samples Si10 and Alu2B, coloured in red and cyan, respectively. Values considered in distribution curves belong to TS cycles going from the 50^{th} to the 100^{th}.

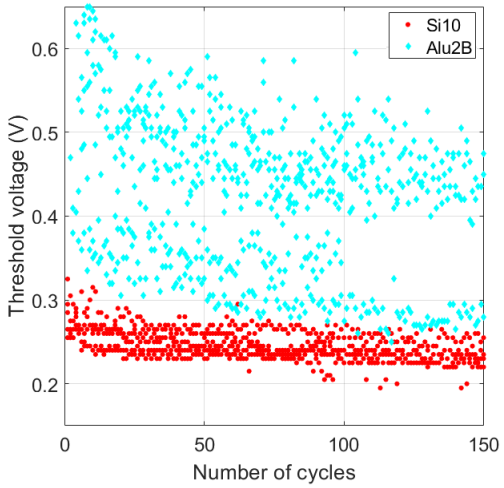
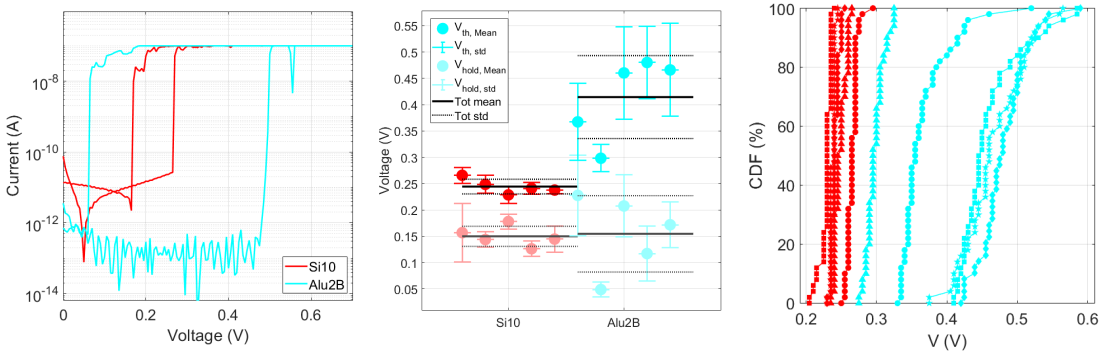


Figure 4.32: Sample Alu2B (Pt/2.5 nm Al_2O_3/10 nm SiO_2/Ag). Threshold voltage (y-axis) put in relationship with number of TS cycles. Five devices are plotted superimposed for each sample up to 150 TS cycles: not all devices are tested up to 150 endurance cycles.



(a) **(b)** **(c)**

Figure 4.33: Sample Alu2B. (b) Mean value of threshold and hold voltage for five devices tested on each sample at $100\,nA_{(CC)}$. The cycles considered for the computation of the mean value go from the 50^{th} to the 100^{th}. Error bars are computed as the standard deviation on the same cycles to give an indication of V_{th} and V_{hold} variability. (c) CDF of V_{th}. Five devices are tested at $100\,nA_{(CC)}$ for samples Si10, Alu2B, coloured in red and cyan, respectively. Values considered in distribution curves belong to TS cycles going from the 50^{th} to the 100^{th}.

Adding a 2.5 nm thick alumina layer at the bottom of SiO_2 increases the threshold voltage, but leaves average hold voltage at the same value of sample Si10. There is a large difference in the cycle-to cycle variability of both V_{th} and V_{hold} between the two samples.

Then, I analyse the leakage current difference, that as already shown above, is orders of magnitude lower in sample Alu2B with respect to Si10. This difference is

clearer in Figure 4.34, where I plot the leakage current cycle-to-cycle variability of one representative device, tested with DC endurance up to 500 TS cycles, for samples Si10 and Alu2B: $I_{leakage}$ is acquired in correspondence of 0.15 V.

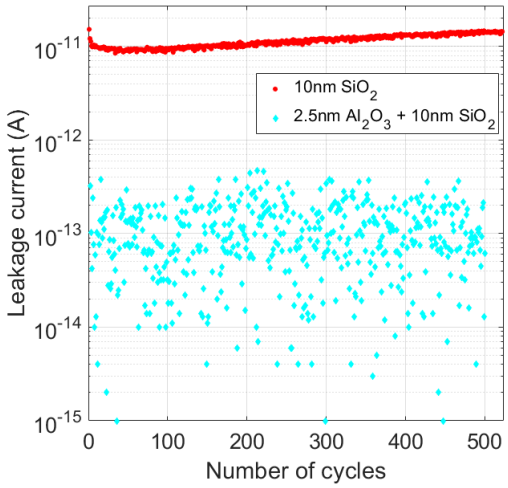


Figure 4.34: Samples Si10 and Alu2B. Leakage current @0.15 V of one representative device for samples Si10 and Alu2B. In sample Si10, $I_{leakage}$ decreases until it reaches a minima (within the first 50 cycles) and then keeps increasing as more switching events take place. $I_{leakage}$ in sample Alu2B does not show any global trend.

Sample Pt/10nm SiO_2/Ag shows a $I_{leakage}$ which increases with the number of applied cycles and is about two orders of magnitude higher than leakage in sample Alu2B. In the very first cycles the leakage decreases until it reaches a minima (within the first 50 cycles) and then keeps increasing as more switching events take place. $I_{leakage}$ in sample Alu2B, instead, does not show any global trend and values are spread on a wide current range ($\sim 10^{-15} - 5 \cdot 10^{-13}$).

As a further analysis I put V_{th} and $I_{leakage}$ in relationship, both with respect to the number of endurance cycles. In Figure 4.35 I consider the representative devices shown above for each sample, with V_{th} on y-axis and $I_{leakage}$ on x-axis. The set of points belonging to sample Alu2B has a cloud shape due to high cycle-to-cycle variability of both V_{th} and $I_{leakage}$. Adding a 2.5 nm thick alumina layer at the bottom of SiO_2, the points of Si10 towards the top left of the graph (high V_{th}, low $I_{leakage}$).

Negative Threshold Switching

Among all the tested samples, *Alu2B* does not switch until breaking down at very high V_{stop} (-9 V), as depicted in Figure 4.36. Eight negative sweeps are performed by progressively increasing V_{stop}: traces are coloured from blue, first cycle, to yellow, last cycle in which current switches from 1 nA to 100 nA leading the device to permanent low resistive state.

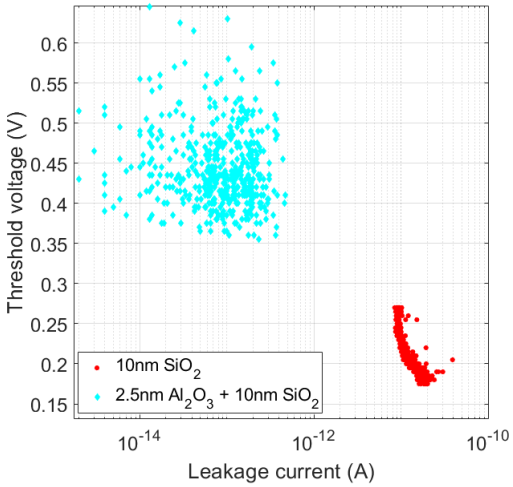


Figure 4.35: Sample Alu2B. The threshold voltage (y-axis) put in relationship with leakage current @0.15 V (x-axis, linear scale). Two representative devices are plotted for each sample. Differently from sample Si10, which shows a V_{th} with a decreasing trend with the increment of $I_{leakage}$, values on sample Alu2B have a large variability both in terms of V_{th} and $I_{leakage}$, so there is no clear relationship.

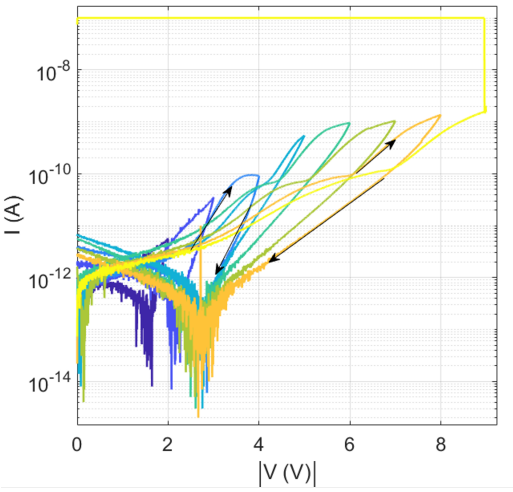


Figure 4.36: Current response to voltage sweep, with $I_{CC} = 100nA$, is plotted for each cycle (y-axis in logarithmic scale). On x-axis the absolute value of voltage is plotted. Traces are coloured from blue, first cycle, to yellow, last cycle in which current switches from 1 nA to 100 nA causing the break down of the device.

Summary

In the following list, I report the features of the analysed sample:

- It is possible to apply at least 500 TS cycles at 100 $nA_{(CC)}$. Volatile operation

is only possible at CC of 100 nA, when a low V_{stop} is used for forming.

- V_{th} decreases as function of number of TS cycles at positive applied voltage.
- Leakage current has no clear trend as function of number of TS cycles at positive applied voltage.
- V_{th} relationship with $I_{leakage}$ is not clear, since both values have a large variability.
- Negative TS is not possible.

4.4 Discussion

4.4.1 Effect of CC

The DC characterization of all samples at various CC, allows to know at which CC samples have a volatile behaviour. Table 4.3 shows the current range in which the tested samples can operate in volatile regime.

Sample	**Stack**	$100\,nA_{(CC)}$	$10\,\mu A_{(CC)}$	$1\,mA_{(CC)}$
Si10	10nm SiO_2	✓	✓	✓
Alu1T	10nm SiO_2 / 1nm Al_2O_3	✓	✓	X
Alu2T	10nm SiO_2 / 2.5nm Al_2O_3	✓	X	X
Alu2B	2.5nm Al_2O_3 / 10nm SiO_2	✓	X	X
Alu10	10nm Al_2O_3	X	X	X

Table 4.3: Table listing for each sample the compliances supported for volatile operation (✓) at positive applied voltage.

The role of CC, considering each device row by row, is critical: the higher CC, the more likely samples tend to need a reset process (at negative voltage) to achieve switching during successive cycles. Moreover, the CC supported for volatile operation reduces as the thickness of the Al_2O_3 increases [23]. The only CC at which all devices (except for Alu10 that is non-volatile at each CC) can support switching over 100 TS cycles is 100 nA.

The following paragraph aims to discuss the behaviour of each stack, illustrating the switching mechanism during the forming process, TS endurance test and negative TS.

4.4.2 Volatile switching at 100 nA

$Pt/SiO_2/Ag$

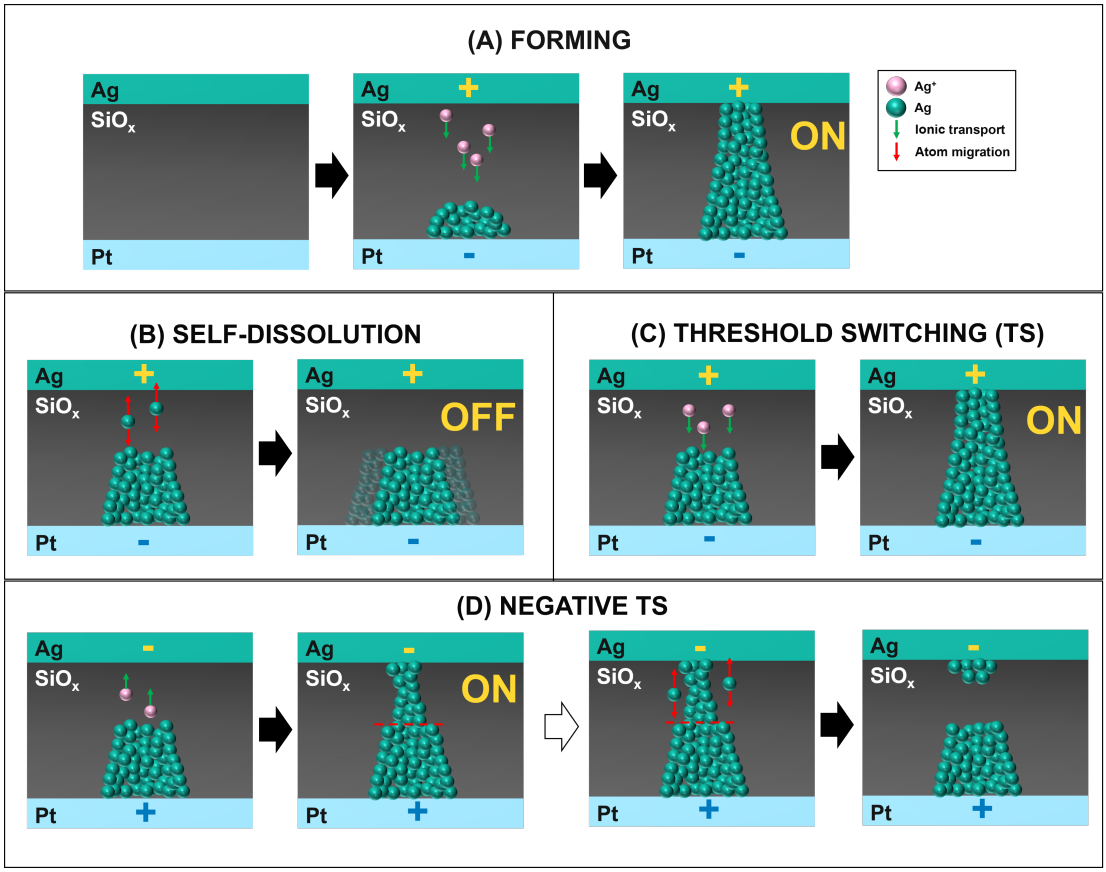


Figure 4.37: Schematic representation of the switching behaviour of sample $Pt/SiO_2/Ag$ under different processes: forming (Panel A), self-dissolution (Panel B), TS (Panel C), negative TS (Panel D).

I hypothesize that the switching in SiO_2 can be described according to the sketches in the Figure 4.37. Starting from the pristine state (panel A, left), when a positive voltage is applied Ag gets oxidized at the Ag/SiO_2 interface and Ag^+ ions migrate towards the bottom interface under the influence of the applied electric field (panel A, center). I suppose that the switching mechanism is limited by the nucleation (or electron transfer or reduction of Ag^+) at the bottom interface, as common in ECMs [24]. The switching operation results in the formation of a conductive filament shaped like an upward cone (or upward truncated cone) as shown in panel A right (ON state).

Once the voltage is removed or it is reduced below a certain level, V_{hold}, the self-dissolution of the filament starts. This process is mainly due to minimization of the Ag/SiO_2 interface energy and is driven by surface diffusion [25]. As the electric field is not playing a major role in this case, I can expect that there is no defined preferential migration direction of the Ag atoms (panel B, left): Ag atoms may move either upwards or downwards, in general. The process results in the modification of the filament shape and the restoring of an oxide gap between Ag electrode and Ag filament (panel B, right, OFF state).

When the device is in the OFF state, a positive voltage applied to the top electrode (panel C, left) produces again the Ag oxidation and Ag^+ migration and the re-formation of the filament (panel C, right, ON state).

Formation and self-dissolution are not symmetrical in the sense the at the end of each TS cycle, there may be a net migration out of the Ag electrode. There could be accumulation of Ag^+ in the oxide, or growth of bottom residual part of the filament (translucent particles in panel B, right). Therefore, according to this picture, this net outflow of Ag from the Ag electrode can be the source of the drift of the switching parameters encountered in the TS cycles (V_{hold} and V_{th}, Figure 4.7 ,$I_{leakage}$, Figure 4.11). It must be noticed that a conic conductive filament with downward orientation would hardly justify the drift of the quantities V_{hold}, V_{th} and $I_{leakage}$, as it will become clear in the following.

Furthermore, Figure 4.14 shows a clear correlation between $I_{leakage}$ and V_{th}. This may be coherent with a nucleation-limited, or more precisely an electron transfer limited process. Ag^+ reduction into Ag (nucleation) require one electron to be transferred to the Ag^+ cation. I can imagine that the higher the current, the higher the possibility that electrons are transferred to the Ag^+ ions. Therefore, Figure 4.14 may support a nucleation-limited mechanisms and a filament cone pointing upward [13][25].

An additional indication of a nucleation limited switching and upward conical conductive filament is the possibility of negative TS after positive forming. Indeed, the OFF state (panel D, left) is constituted of a symmetric structure formed by a silver top electrode, an oxide, and a bottom virtual electrode, which can switch under both voltage polarities. When negative voltage is applied, Ag oxidation happens from the bottom, followed by the Ag^+ migration and nucleation on the Ag top electrode. As opposite to the positive TS, there is an outflow of Ag from the bottom virtual electrode which produces a drift of V_{th}, V_{hold} and $I_{leakage}$ in the opposite direction with respect to what happens in positive TS (Figure 4.15) [26].

$Pt/SiO_2+Al_2O_3/Ag$

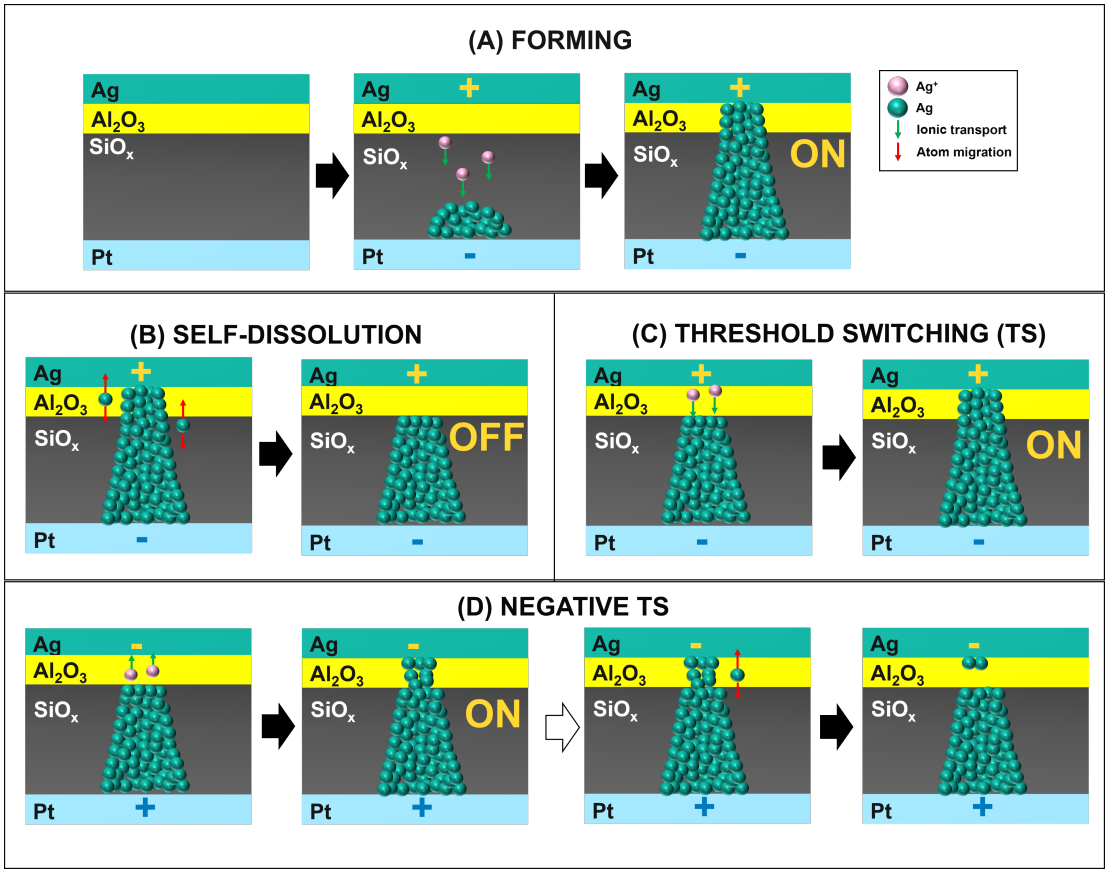


Figure 4.38: Schematic representation of the switching behaviour of samples $Pt/SiO_2+Al_2O_3/Ag$ under different processes: forming (Panel A), self-dissolution (Panel B), TS (Panel C), negative TS (Panel D).

For the Al_2O_3 (top) structure, I hypothesize again that the switching is limited by the nucleation at the bottom interface. The main reason lies in the fact that negative TS is observed after forming also for the Al_2O_3 (top) samples. A second reason is that forming and switching at the same voltage polarities and with similar voltages (especially for the 1nm case) and the volatile nature of the switching, at least for low compliance values, are not compatible with anion switching [13]. They are coherent with cation-based switching. Therefore, cations must pass through the Al_2O_3 layer and once passed, they easily drift through SiO_2 and eventually nucleate at the Pt interface. The nucleation limited mechanism described for single SiO_2 sample implies that the drift is not the limiting process, and it is "easy".

The experimental data show that the Al_2O_3 inter-layer affects all the V_{th}, V_{hold}

and $I_{leakage}$ parameters (Figure 4.22, Figure 4.23). This evidence makes us consider that the switching (filament formation/dissolution) occurs in the Al_2O_3 layer itself (the sketch is brutal, the remaining oxide may be shorter or longer than the Al_2O_3 layer itself).

In particular, I consider a switching as described in Figure 4.38. Let us consider the case of 2.5 nm Al_2O_3, first. The 1 nm case is somewhat an intermediate case with some peculiarities.
The following paragraphs report the process in each panel of Figure 4.39.

Panel A Forming occurs according to the following steps: Ag oxidation from top electrode, Ag^+ migration and nucleation at the bottom interface, filament growth. The higher value of V_f with respect to the SiO_2 sample may be due to higher thickness or higher barrier for Ag oxidation [20][27]. The filament may completely short the two electrode and leave a small gap to it.

Panel B The thinner filament part is within the Al_2O_3 layer, where Ag mobility is lower [28] (I consider it more dense and stoichiometric than SiO_2, given the deposition process). This results in lower V_{hold} with respect to the single SiO_2 sample (Figure 4.22b).

Panel C During TS switching, the filament must be re-instated in the Al_2O_3 which requires a higher voltage than the single SiO_2 for the same reasons as for the forming process [23]. A net continuous outflow of Ag from the top electrode may present also for the Al_2O_3 top case. This is coherent with the drift of V_{th}, V_{hold} and $I_{leakage}$ for the 1nm Al_2O_3 . In case of 2.5 nm Al_2O_3 top, the net outflow of Ag may reinforce the filament in the Al_2O_3 layer, which becomes more and more stable increasing the switching cycles, by virtue of the low Ag mobility in such oxide.

Panel D Explanation of switching during negative TS in agreement with the $Pt/SiO_2/Ag$ sample. It is an indication of the upward orientation of the filament cone.

In Figure 4.24, exactly the same correlation between $I_{leakage}$ and V_{th} is found for single SiO_2 and 1nm Al_2O_3 samples, while the correlation is less evident for 2.5nm. In this case, after forming Ag^+ diffusion may turn to be the most limiting process in device switching.

$Pt/Al_2O_3+SiO_2/Ag$

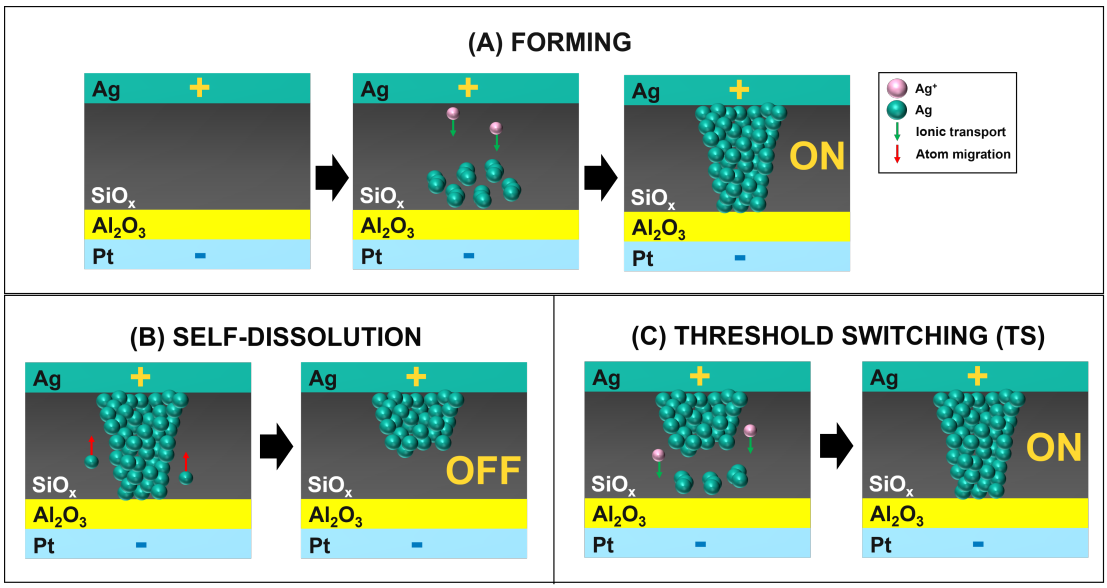


Figure 4.39: Schematic representation of the switching behaviour of samples $Pt/Al_2O_3+SiO_2/Ag$ under different processes: forming (Panel A), self-dissolution (Panel B), TS (Panel C).

For the Al_2O_3 (bottom) structure I hypothesize that the conductive filament is shaped like a downward pointing cone, because the oxidation and drift of Ag occur analogously to sample $Pt/SiO_2/Ag$, but the Al_2O_3 layer hinders Ag^+ the drift toward the Pt bottom electrode. This claim would explain also why negative TS cannot be performed on this sample (Figure 4.36). I consider that Ag^+ cations accumulate close to the SiO_2/Al_2O_3 interface without nucleation onto the inert electrode, until the local concentration of Ag^+ becomes so large that the Ag cluster coalesce as described in [29]. According to this hypothesis, switching occurs as illustrated in the figure above (Figure 4.39).
In the following paragraphs I describe the process in each panel of Figure 4.39.

Panel A Forming: Ag oxidation and drift of Ag^+ up to the SiO_2/Al_2O_3 interface, coalescence of disconnected Ag metallic clusters, cluster densification into a filament-like region. The switching process is hence different and the insertion of an additional layer can only induce an increment of the forming voltage.

Panel B filament retraction.

Panel C filament re-instatement according to forming process and then self-dissolution.

In this Al_2O_3(bottom) case, during the self-dissolution process Ag cannot diffuse both upward and downward, as in the previous samples, but the presence of an Al_2O_3 barrier forces the Ag to only diffuse in the upward direction. This fact justifies the observation that no drift of V_{th}, V_{hold} and $I_{leakage}$ is observed (Figure 4.32 and 4.34) for Al_2O_3(bottom). Furthermore, the fact that there is no clear correlation between $I_{leakage}$ and V_{th} (Figure 4.35) may be a further indication that the nucleation is no longer the limiting process. It is interesting to notice that the high CC results in nonvolatile operation and stable conductive filament, which maybe forms within Al_2O_3 bottom layer.

Chapter 5

Conclusion and future work

Memristive devices are nowadays promising candidates for the implementation of brain-inspired in-memory computing architectures. Thanks to their straightforward structure and involved materials, they can provide high scalability, as well as high stacking capabilities and compatibility with CMOS technology. Moreover, memristive devices can provide advanced functionalities as dynamical and non-linear elements, and can reproduce for instance the synaptic and neural dynamics. Memristive device are often based on a two-terminal structure, where a switching medium (oxide, electrolyte,...) is sandwiched between two electrodes, and their resistance can be reversibly modified in response to an external electrical stimulus.

Among the various class of memristive devices, this thesis is based on the electrochemical metallization memories (ECMs). The working mechanism is based on the formation and dissolution of a conducting filament shorting the two electrodes as a consequence of the movement of metals ions, such as Ag, from one of the two electrodes inside the switching electrolyte. Therefore, under repeated stimuli, it is possible to cycle the device resistance between a low resistance (ON state) and high resistance (OFF state). While ECMs has been exploited and studied as non-volatile memories, i.e. a device able to retain the stored information for long time (years) , there is an increasing interest to study ECM devices that exhibit a self-relaxation of the ON state (also called volatile memristors or threshold switching devices), which are the topic of this thesis. The interest for volatile ECM is due to their properties such as threshold switching and relaxation behaviours, which in perspective can be controlled over various time scales. The possible applications of volatile ECM span from selector to dynamics element as neuron, synaptic devices or true random number generators (TRGN).

The volatile behaviour can be achieved by engineering the material stacks both as electrode and switching medium. This thesis reports a deep study of $Ag/SiO_x/Pt$

based ECM volatile memristors and on the insulator engineering by using an oxide/electrode Al_2O_3 interfacial layer. The Ag/SiO_x/Pt devices have been studied by quasi-static I-V measurements, and by using different current compliance during the operation. After a forming operation, which establishes for the first time an Ag filament shorting the two electrodes, it is possible to reversible cycling the device among an ON and OFF state. Once the bias is removed, the filament self-dissolves in a certain time (< seconds). For the Ag/SiO_x/Pt device, the volatile switching is achieved for all current compliance between 100 nA and 1 mA.

The introduction of an alumina barrier in the switching layer deeply affects the switching mechanism inside the ECM cell, and as a consequence the electrical operation. The ECM structures proposed in this thesis, consisting of stacks made of SiO_x and Al_2O_3 with different thicknesses and arrangements (positioned at the top or bottom electrode interface), show the coexistence of both volatile and non-volatile features. Both features can be attained by adjusting the current limitation during the forming process and switching cycling, thus controlling the strength of the conductive filament. Data statistical analysis show that diverse combinations of SiO_x and Al_2O_3 lead to differences in electrical figures of merit like forming/threshold voltages and leakage current. Moreover, I found that in general, the thicker alumina layer, the lower the maximum supported CC for volatile operation.

Thanks to a statistical investigation of relevant switching parameters, I can also to provide a qualitative explanation of the switching processes and their differences among different oxide combinations.

In sample Pt/SiO_x/Ag, during TS, the Ag filament grows with a cone shape pointing toward the top electrode, and it self-dissolves restoring the gap between the Ag electrode and the conductive filament to minimize the Ag/SiO_x interface energy. After every TS cycle, there is an accumulation of Ag^+ in the oxide which causes the drift of the V^{th} and V^{hold}.

The introduction of a dense insulating layer in the stack, Al_2O_3, provides a barrier that hinders the Ag motion through the stack itself, thus increases the voltage required to switch. The switching and self-dissolution occur in the Al_2O_3 layer, where the thinnest part of the Ag cone resides.

For the Al_2O_3 (bottom) structure the conductive filament is shaped like a downward pointing cone, because the oxidation and drift of Ag occur analogously to sample Pt/SiO_x/Ag, but the Al_2O_3 layer hinders Ag^+ the drift toward the Pt bottom electrode. So, Ag^+ cations accumulate close to the SiO_x/Al_2O_3 interface without nucleation onto the inert electrode, until the local concentration of Ag^x becomes so large that the Ag cluster coalesce, densifying into a filament-like region. During the self-diffusion process the alumina barrier forces Ag to diffuse in the

upward direction.

The introduction of an alumina barrier in the switching layer has a strong influence on the Ag filament growth process, that is on the limiting physical processes, and on its morphology.

In summary, I demonstrated that, combining oxide layers that give different mobility to Ag^+ cation, it is possible to move the transition from volatile to non-volatile behavior to different values of programming current compliance.
Future work will include the study of the device response under applied pulses of variable amplitude and time to determine the switching kinetics and the relaxation time of the programmed ON state.

Appendix A

Detailed analysis on bi-layered stacks

The sections of this appendix show the detailed TS electrical characterization of samples SiO_2 + 1nm Al_2O_3 (top), SiO_2 + 2.5nm Al_2O_3 (top) and 2.5nm Al_2O_3 (bottom) + SiO_2.

A.1 TS on Pt/10nm SiO2/1nm Al_2O_3/Ag

This section reports the results from the electrical characterization on the sample with an insulating stack made of SiO_2 (10 nm) with Al_2O_3 (1nm) on top. Three levels of Current Compliance (CC) have been considered: 100nA, 10uA and 1mA.

$100\,nA_{(CC)}$ At least 100 TS endurance cycles are performed on five devices at 100 nA CC: the I-V curves are depicted in A.1(a-e). A.1(a) shows current response traces with colours fading from blue to yellow as the number of tested cycle increases (see colour legend in the colour bar).

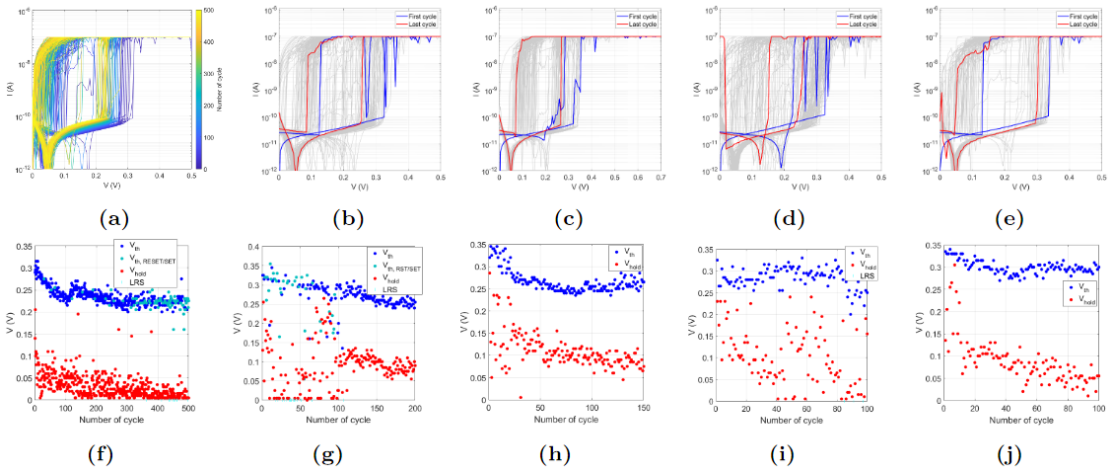


Figure A.1: Sample Pt/10nm SiO2/1nm Al_2O_3/Ag. On top (a-e), the current response to voltage sweep, with $I_{CC} = 100nA$, is plotted for each cycle (y-axis in logarithmic scale). In (a) the color fades from blue to yellow to indicate the progression on both V_{th} and V_{hold} along the TS events. Other I-Vs highlight the first (blue) and last cycle (red). On bottom (f-j), the evolution of V_{th} (blue) and V_{hold} (red) as function of number of cycles.

$10\,\mu A_{(CC)}$ TS endurance is also tested at $10\mu A_{(CC)}$. Current response of three devices previously formed at $10\mu A_{(CC)}$ is shown in Figure A.2(a-c). In Figure A.2(d-f) the values of threshold and hold voltages are plotted.

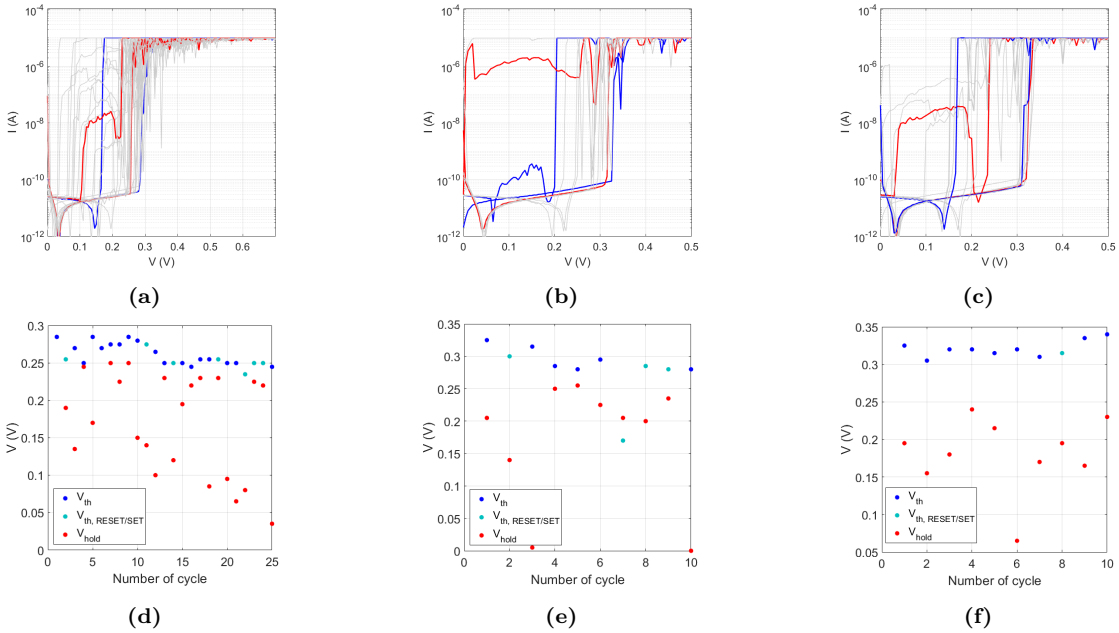


Figure A.2: Sample Pt/10nm SiO2/1nm Al_2O_3/Ag. On top (a-c), the current response to voltage sweep, with $I_{CC} = 10\mu A$, is plotted for each cycle (y-axis in logarithmic scale). I-Vs in blue and red highlight two typical kinds of response. On bottom (d-f), the evolution of V_{th} (blue) and V_{hold} (red) as function of number of cycles.

$1\,mA_{(CC)}$ Threshold Switching is also tested at $1mA_{(CC)}$. Current response of one device previously formed at $1mA_{(CC)}$ is shown in Figure A.3a. In Figure A.3b the values of threshold and hold voltages are plotted.

Figure A.3: Sample Pt/10nm SiO2/1nm Al_2O_3/Ag. (a) Current response to voltage sweep, with $I_{CC} = 1mA$, is plotted for each cycle (y-axis in logarithmic scale). I-Vs in blue and red highlight two kinds of response. (b) Evolution of V_{th} (blue) and V_{hold} (red) as function of number of cycles.

Switching failures

Concerning the threshold switching failures, a table containing all failures contributions for each set of devices, grouped according to the used current compliance, is reported (A.1), together with the respective failure probability in percentage. Performing TS endurance at higher CC leads to a higher probability of total failure events.

CC	**TOT Reset/Set**	**TOT LRS**	**% Reset/Set**	**% LRS**
100nA	110	34	10.5%	3.2%
$10\mu A$	12	0	26.7%	0%
$1mA$	1	15	5.8%	88.2%

Table A.1: Sample Pt/10nm SiO2/1nm Al_2O_3/Ag. TS failures counted on the total of endurance cycles performed on all devices for each compliance.

A.2 TS on Pt/10nm SiO2/2.5nm Al_2O_3/Ag

This section shows the results on the electrical characterization performed on the sample with an insulating stack made of SiO_2 (10 nm) with Al_2O_3 (2.5nm) on top. Three levels of Current Compliance (CC) have been considered: 100nA, 10uA and 1mA.

$100\,nA_{(CC)}$ At least 100 TS endurance cycles are performed on five devices at 100 nA CC. The I-V curves are depicted in A.4(a-e) and are shown with colours fading from blue to yellow as the number of tested cycle increases.

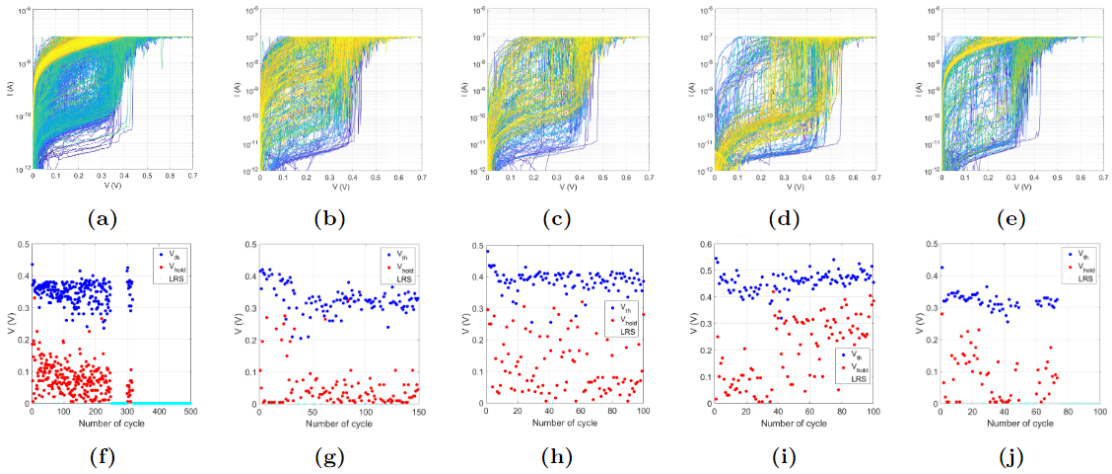


Figure A.4: Sample Pt/10nm SiO2/2.5nm Al_2O_3/Ag. On top (a-e), the current response to voltage sweep, with $I_{CC} = 100nA$, is plotted for each cycle (y-axis in logarithmic scale). In (a) the color fades from blue to yellow to indicate the progression on both V_{th} and V_{hold} along the TS events. Other I-Vs highlight the first (blue) and last cycle (red). On bottom (f-j), the evolution of V_{th} (blue) and V_{hold} (red) as function of number of cycles.

On the first device, endurance test was launched up to 300 cycles. From the 270^{th} to the 300^{th} there is no more switching. 200 more TS cycles are launched showing switching only for the first 13 cycles, and then going to LRS until the end of the test.

$10\,\mu A_{(CC)}$ Threshold Switching is also tested at $10\mu A_{(CC)}$. Current response of one of the two devices previously formed at $10\mu A_{(CC)}$ is shown in Figure A.5a. In Figure A.5(d-f) the values of threshold and hold voltages are plotted.

Figure A.5: Sample Pt/10nm SiO2/2.5nm Al_2O_3/Ag. On the left (a), the current response to voltage sweep, with $I_{CC} = 10\mu A$, is plotted for each cycle (y-axis in logarithmic scale). I-Vs in blue and red highlight two typical kinds of response. On the rigth (b), the evolution of V_{th} (blue) and V_{hold} (red) as function of number of cycles.

$1\,mA_{(CC)}$ Threshold Switching was also tested at $1mA_{(CC)}$. Current response of one device previously formed at $1mA_{(CC)}$ is shown in Figure A.6a. In Figure A.6b the values of threshold and hold voltages are plotted.

(a) **(b)**

Figure A.6: Sample Pt/10nm SiO2/2.5nm Al_2O_3/Ag. (a) Current response to voltage sweep, with $I_{CC} = 1mA$, is plotted for each cycle (y-axis in logarithmic scale). (b) Evolution of V_{th} (blue) and V_{hold} (red) as function of number of cycles.

Only the fist cycle shows threshold switching, whereas all the successive ones go to Low Resistive State (LRS).

Switching failures

Concerning the threshold switching failures, a table containing all failures contributions for each set of devices, grouped according to the used current compliance, is reported (A.2), together with the respective failure probability in percentage.

CC	TOT Reset/Set	TOT LRS	% Reset/Set	% LRS
100nA	0	339	0%	35.7%
$10\mu A$	3	0	12%	0%
$1mA$	0	12	0%	92.3%

Table A.2: Sample Pt/10nm SiO2/2.5nm Al_2O_3/Ag. TS failures counted on the total of endurance cycles performed on all devices for each compliance.

A.3 TS on Pt/2.5nm Al_2O_3/10nm SiO2/Ag

This section reports the results from the electrical characterization on the sample with an insulating stack made of Al_2O_3 (2.5nm) with SiO_2 (10 nm) on top. One level of Current Compliance (CC) has been considered: 100nA.

$100\,nA_{(CC)}$ At least 100 TS endurance cycles are performed on five devices at 100 nA CC. The I-V curves are depicted in A.7(a-e) and for the first device they

are shown with colours fading from blue to yellow as the number of tested cycle increases. From the cycle-to-cycle variability of V_{th} and V_{hold} the first cycle has often a set voltage which is much greater than the successive ones (>0.2V).

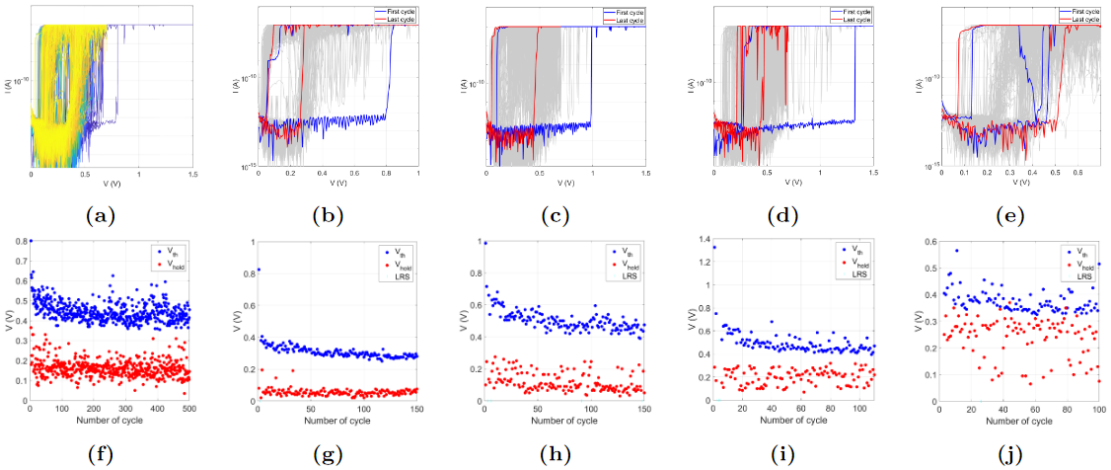


Figure A.7: Sample Pt/2.5nm Al_2O_3/10nm SiO2/Ag. On top (a-e), the current response to voltage sweep, with $I_{CC} = 100nA$, is plotted for each cycle (y-axis in logarithmic scale). In (a) the color fades from blue to yellow to indicate the progression on both V_{th} and V_{hold} along the TS events. Other I-Vs highlight the first (blue) and last cycle (red). On bottom (f-j), the evolution of V_{th} (blue) and V_{hold} (red) as function of number of cycles.

Switching failures

Concerning the threshold switching failures, a table containing the failures contributions is reported (A.3), together with the respective failure probability in percentage.

CC	TOT Reset/Set	TOT LRS	% Reset/Set	% LRS
100nA	0	11	0%	1.1%

Table A.3: Sample Pt/2.5nm Al_2O_3/10nm SiO2/Ag. TS failures counted on the total of endurance cycles performed on all devices.

Appendix B

MATLAB algorithm for automatic data analysis

This appendix addresses the explanation of the main routines implemented in MATLAB for the automatic analysis of data acquired and exported from EasyExpert©, via *.txt files, such as the detection of V_{th} and V_{hold} detection and switching failures detection.

B.0.1 Algorithm for threshold and hold voltage detection

The MATLAB© algorithm captures the V_{th} and V_{hold}, from data acquired measuring a switching memristor, by analysing the current variation. This is performed by computing the ratio between each sample (i) and its previous (i-1).

- V_{th}: detected when current ratio is bigger than a certain threshold: the first occurrence is considered. The threshold has been tuned device-by-device, by inspecting the visual representation of the algorithm in Figure (right). It still has to be adjusted for some cycles which may show a less steep current increase. Higher the sampling rate, smaller the threshold to be set for the similar switching behaviour.

- V_{hold} : detected when current ratio is smaller than a certain threshold: the last occurrence is considered, since it is then that the conductance will fall to the low reset value. The threshold has been tuned device-by-device, by inspecting the visual representation of the algorithm in Figure B.1(right).

The algorithm is robust enough to make successful detection even with set and reset irregularities (Figures B.2 and B.3a). During positive voltage sweeps, it filters out high current positive variations, due to retention effects, that may happen before V_{th} is reached. A threshold is fixed at 0.1V, below which all current values

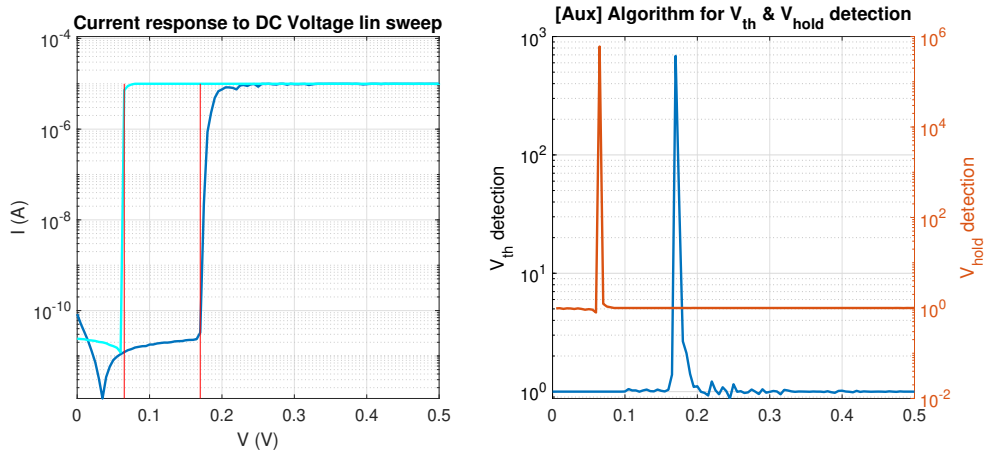


Figure B.1: On the left, the current response to DC linear voltage sweep: blue trace is the response to positive sweep (0V to 500mV), cyan trace is the response to negative sweep (500mV back to 0V). On the right, the visual feedback of the custom algorithm: blue trace for V_{th}.

are flattened to the one corresponding to 0.1V: flattening to an arbitrary current value may lead to an abrupt variation in correspondence of the fixed threshold, leading to a wrong detection in case it overcomes the ratio for the V_{hold} detection. Moreover, a conditioning on the input measurement, exported as a *.txt file by EasyExpert© (by Keysight), is performed, since it was realised that some current values saved by the software were zero. To avoid misinterpretation and plotting discontinuous curves ($log_{10}(0) = -\infty$), all zeroes were fixed to a current value of 10pA.

B.0.2 Algorithm for threshold switching "failure" detection

The algorithm detects also how many endurance cycles don't show a successful set. There can be two cases:

- During positive voltage sweep the device resets first, then sets (Figure B.3a).
- During positive voltage sweep the device is already set (high current state), so no switching occurs (Figure B.3b).

The former (later shortened to "RST/SET") is recognised if current reaches 1μA before 0.1V and if a threshold voltage is detected. The latter (later shortened to "LRS", Low Resistive State) is verified if current reaches 1μA before 0.1V, and no threshold was detected. During code execution, as the script reads the measurement data, it displays the number of cycle analysed and whether it has a regular set, or

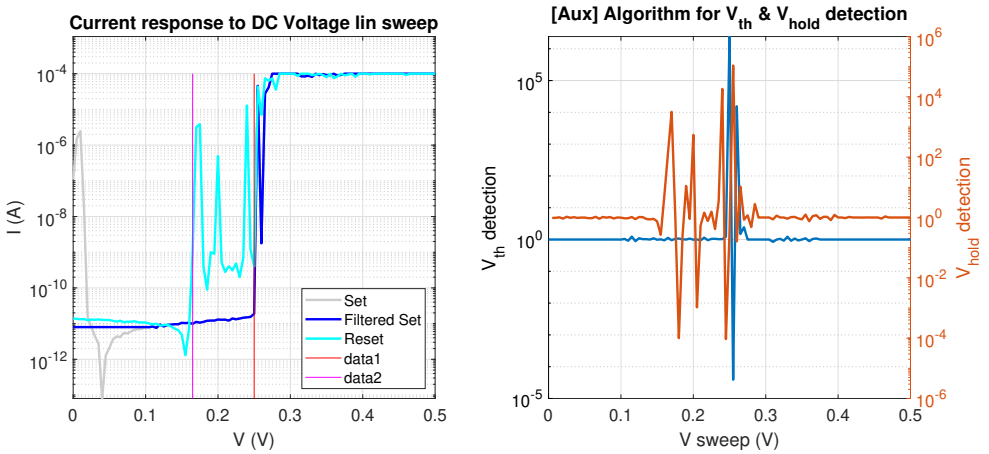
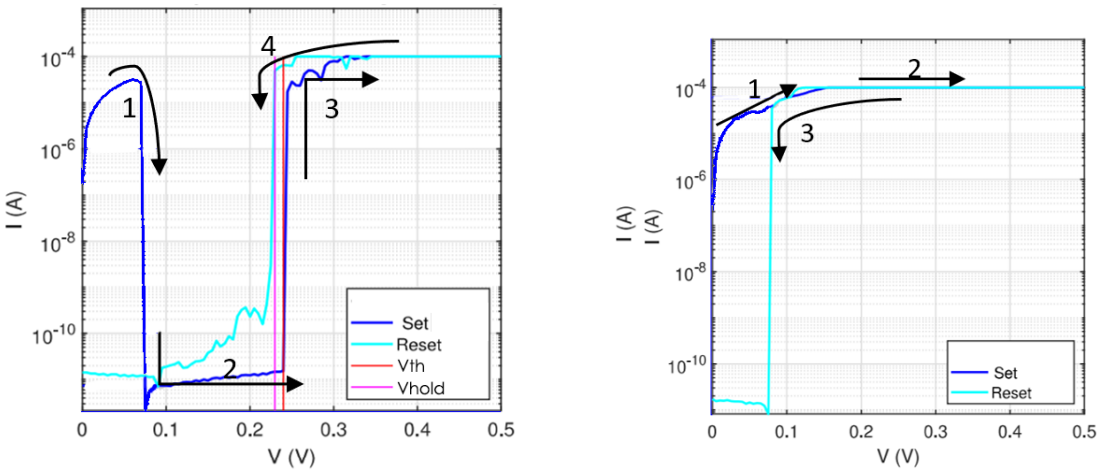


Figure B.2: Even though the I-V curve does not show clear rise and fall edges, the algorithm is still able to detect the values of interest. The grey trace represents the actual current variation, that is flattened (blue trace) by the algorithm to prevent initial positive variations to be detected as V_{th}. On the left, the algorithm detects multiple candidates both for threshold voltage and hold voltage, but only the first one and the last value satisfying the threshold condition are considered, respectively.

shows one of the two situations above. At the end, the program generates a report with the number of "failures" and which cycles showed which behaviour.



(a) **(b)**

Figure B.3: Example of RESET/SET (a) and LRS (b) response and how they are interpreted by the MATLAB analysis algorithm. The current follows the path indicated by arrows in the numerical order. With the aim of detecting and counting these kinds of failure, the algorithm flattens real current values when voltage sweeps from 0V to 0.1V to avoid current fluctuations to cause a wrong V_{th} detection. Two cases are possible: within 0.1V the current reaches a value comparable with I_{CC} and afterwards a switching from I_{off} to I_{ON} is detected, within 0.1V the current reaches a value comparable with I_{CC} and afterwards no switching occurs. Threshold voltages detected in the first case are still considered in cumulative distributions, whereas LRS failures are excluded. The probability of both failures is shown.

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"How could there have been stories about space travel before --"
"The writers," Pris said, "made it up."
Philip K. Dick, Do Androids Dream of Electric Sheep?