POLITECNICO DI TORINO

Master's degree course in

Mechatronic Engineering

(HW & Embedded System for Industry 4.0)

Master degree Thesis

GaN based DC-DC Converter for Automotive TEG

Politecnico di Torino

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Abstract

Energy saving is becoming so important since it reduces pollution and it saves economic costs as well.
Since combustion engines have low efficiency(less than 30% of the energy is used) the energy from the heat of the exhaust pipe using can be reused for thermoelectric generator (TEG).
It's an actuator based on the Seebeck effect : it takes thermal energy as input, it converts it to electrical energy.
To use this electrical energy, the output voltage of the TEG has to be controlled with a DC-DC converter. In this application the output voltage will be used to charge the battery of the car.
The thesis aims to design a DC-DC power electronic converter (power part and control part) that allows a thermoelectric generator to charge a 12V battery , using the latest GaN Tecnhology. This technology allows to use switch MOSFET with lower on-resistance, faster switching frequency and lower size in comparison to Silicon Mosfets, increasing the power density over the area in the process.

Contents

Chapter 1

Introduction

Energy saving is becoming so important since it reduces pollution and it saves economic costs as well.
Since combustion engines have low efficiency(less than 30% of the energy is effectively used) the heat of the exhaust pipe using can be used for the TEG.
The physical principle of this actuator resides on the Seebeck effect : it takes thermal energy as input and it converts it to electrical energy. The output voltage of the TEG is not regulated because it ranges from 0 to 60 V. To use the electrical energy efficiently a DC-DC converter has to be designed. The DC-DC converter is a power electronic device that takes as an input an unregulated voltage and it outputs a controlled voltage. By using the output voltage to recharge the battery the alternator's work is reduced as a result.

Aim of the Thesis

The thesis aims to design a DC-DC converter (both power and logic) allowing the Teg to charge the 12V battery, using the GaN Transistor Tecnhology. This technology allows to use a power transistor switch with lower on-resistance, faster switching frequency and lower size in comparison to Silicon Mosfets and Bipolar Transistors. Reduction in size and higher frequency has also impact on the temperature as well as the parasitic effect of the GaN which may cause irreversible damage, hence, a peculiar attention in the simulation and design of the layout was made.

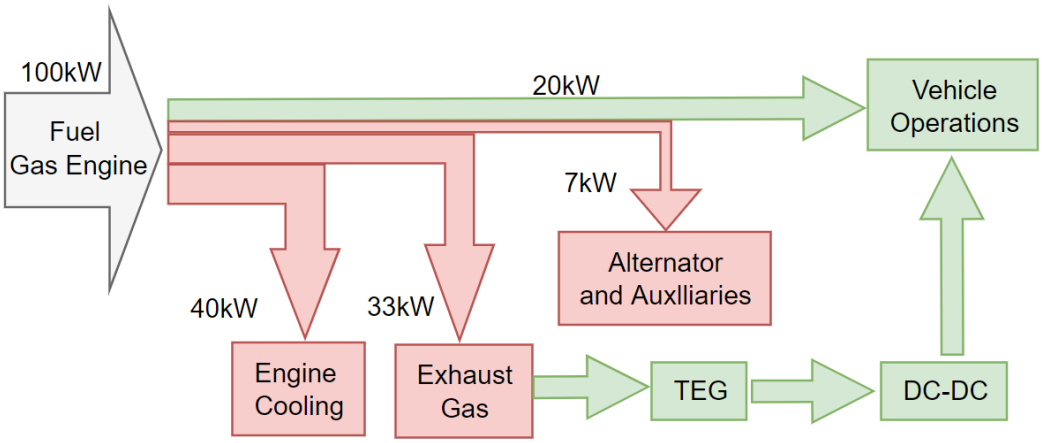


Figure 1.1: Fuel combustion energy diagram

Thesis Structure

The thesis is structured as follows:

Starting from an introduction in which TEG, suitable topologies and GaN technology state of art are explained. Then, once selected a suitable DC-DC topology for the project, the designed of the power stage, measure stage as well as the choice of the component and their impact on the efficiency , is showed in chapter 2. The logic board design and the PCB Layout in KiCad is showed in chapter 3, while the test results as well as the main waveform of the converter are showed in the last chapter of the thesis.

1.1 Thermoelectric Generator

The physical principle of this actuator resides on the Seebeck effect : it takes thermal energy as input and it converts it to electrical energy Thermoelectric generators are designed with a great amount of thermopiles,(since just one thermocouple doesn't give a significant energy) each of them consisting with p-n material. [15] Hence, to fully operate, they need a significant temperature gradient. The TEG are mostly used in Aerospace Applications, Waste Heat Recovery in both Automotive and Energy Applications and so on. The practical limitations of this actuator consist in his High Output resistance and Low thermal conductivity [1]. The aspect of study of the converter is the characteristics of the generator's output ,hence the characteristic of converter's input.
From figure 1.2 the Maximum Power vs Temperature Rise is shown In figure 1.3 is found the Resistance of the TEG vs Temperature Rise, while in Fig 1.4[2]

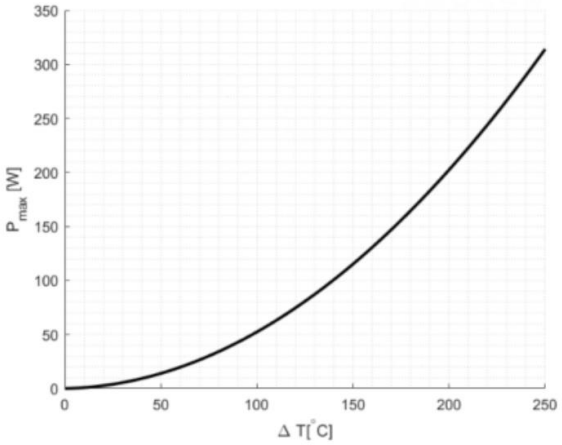


Figure 1.2 : Maximum output TEG Power

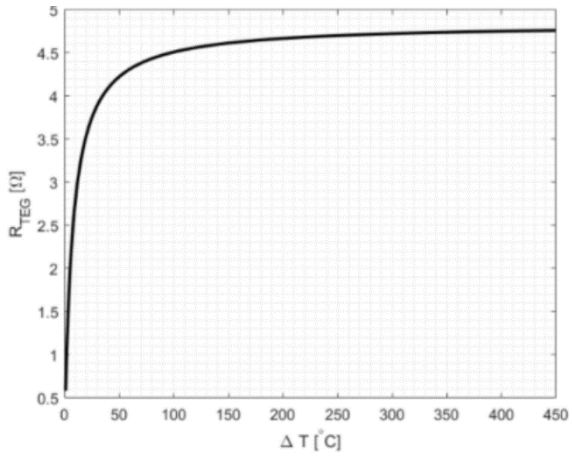


Figure 1.3 : Output Resistance of TEG

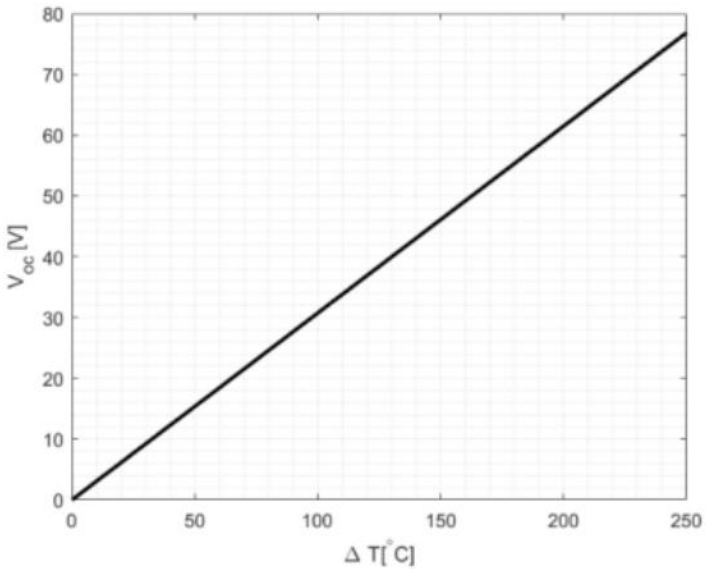


Figure 1.4 : Output Open Circuit Voltage of TEG

Where:

- Voc = Open Circuit Voltage
- RTEG = Output Resistance of the TEG
- PMAX= Max available output of the TEG

From the Maximum power transfer theorem ,to obtain the maximum power from the TEG, the converter's input resistance must match the TEG's output resistance.

In an electric circuit made with the internal resistance of the generator and the load resistance, the power transferred at the load is

$$P_{\mathrm{L}} = \frac{1}{2}\frac{|V_{\mathrm{S}}|^2 R_{\mathrm{L}}}{(R_{\mathrm{S}} + R_{\mathrm{L}})^2}$$

Where

- Vs is the source voltage
- Rs is the internal resistance of the source, namely the internal resistance of the generator
- Rl is the load resistance

In the figure below the Efficiency transferred at the load vs the Load Resistance is showed. Assuming that the TEG has an internal Resistance of 1Ω and, for this simulation only, a Fixed Output Voltage of 20V, the maximum power transferred is when the load resistance matches the internal resistance of the TEG.
This entails that the voltage at the load is half the voltage generated by the TEG, hence:

$$V_{mp} = V_{oc}/2$$

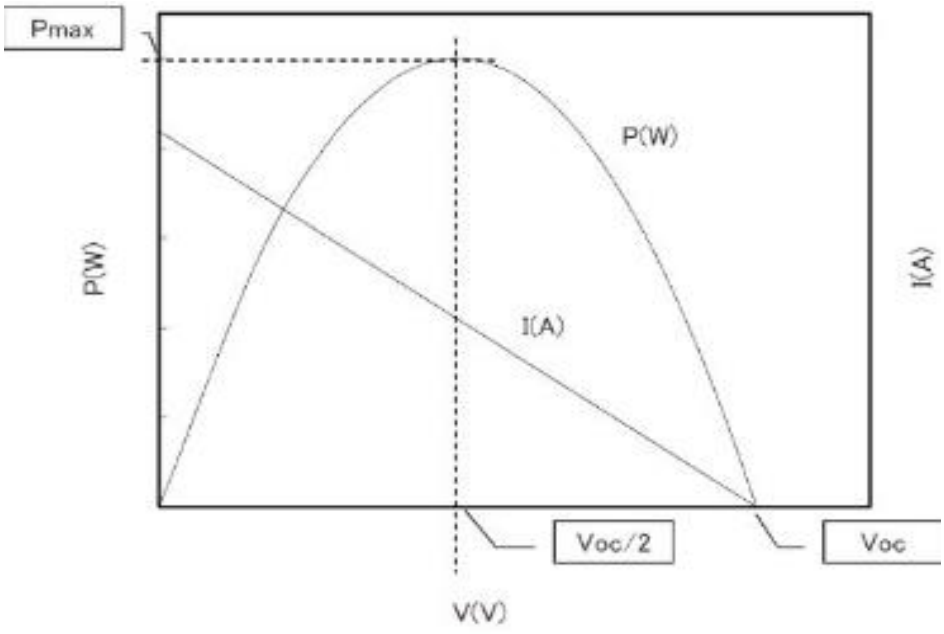


Fig 1.5 Power Transferred vs Input Voltage

Given all the above information the curve that correlates Pmax and Vmp is computed , adjusting the coefficients accordingly.
The graphical representation of equation (1) can be seen in fig.(1.2)

$$P_{max} = 0.4 * Vmp^2 + 0.35 * V_{mp} \quad (1)$$

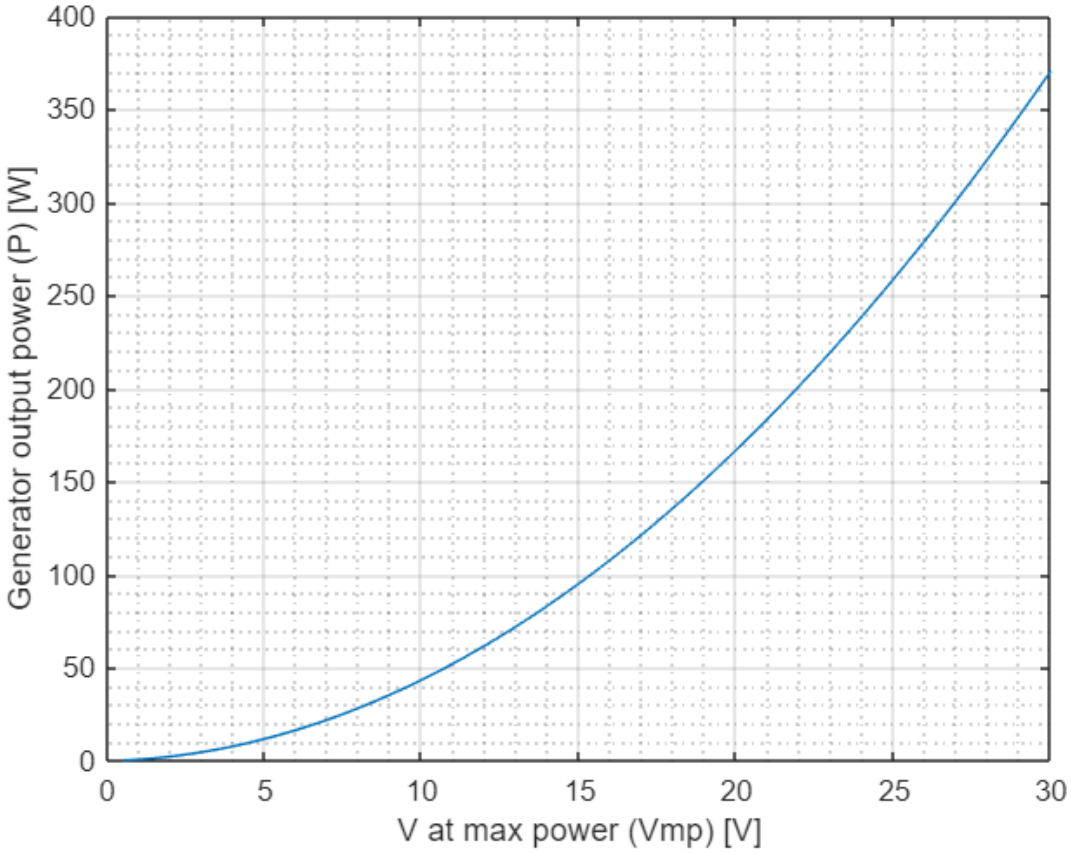


Figure 1.6 : Max Power vs Output Voltage

1.2 Suitable DC-DC Topologies

The input voltage of the converter will be approximately between 0 and 60 volts. On the other side of the converter there will be a 12V Battery, this means that the DC-DC converter has to work both as a step-up and a step-down converter. There are 4 converter topologies that are normally used in these situations:
1)Inverting buck-boost (fig 1.6)
2)Non-inverting buck-boost (fig 1.7)
3)the single-end primary inductor converter (SEPIC) (fig 1.8)
4)Cascade Boost Buck (fig 1.9)

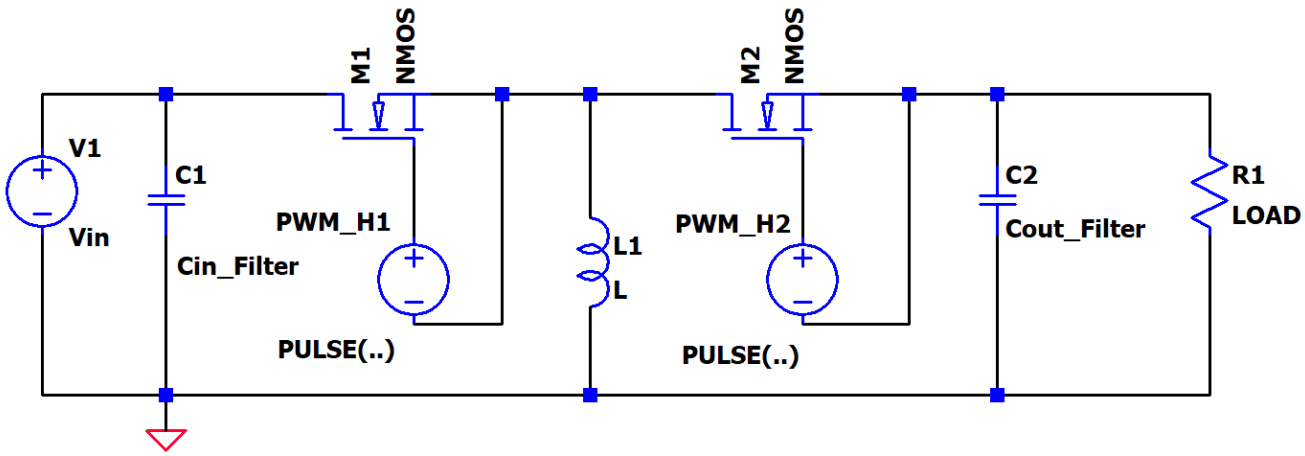


Figure 1.6 : Inverting Buck Boost

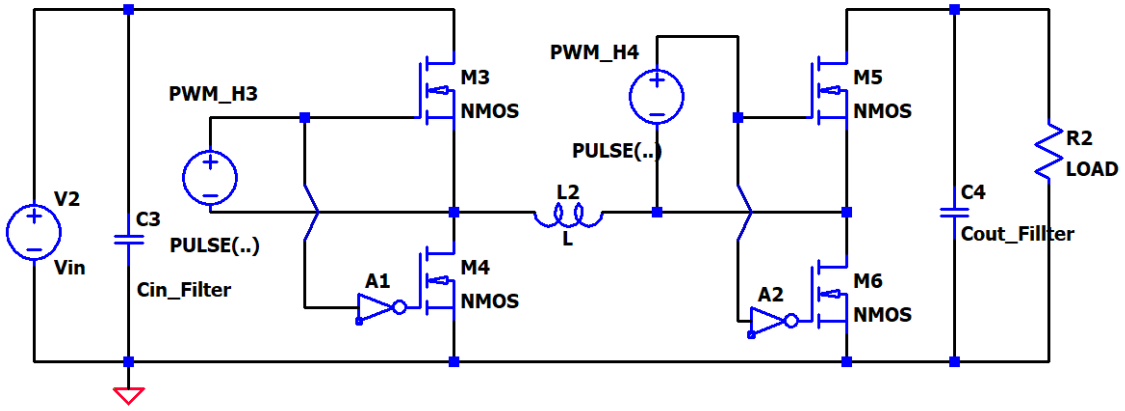


Figure 1.7 : Non inverting Buck Boost

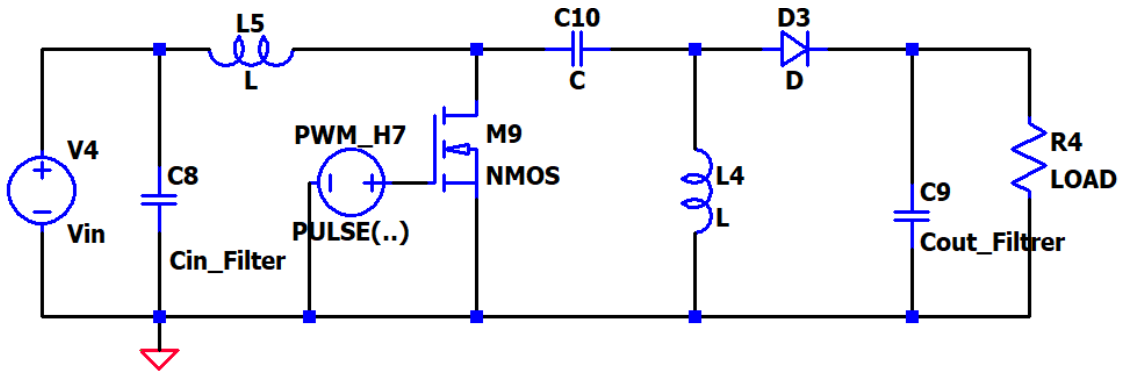


Figure 1.8 : SEPIC

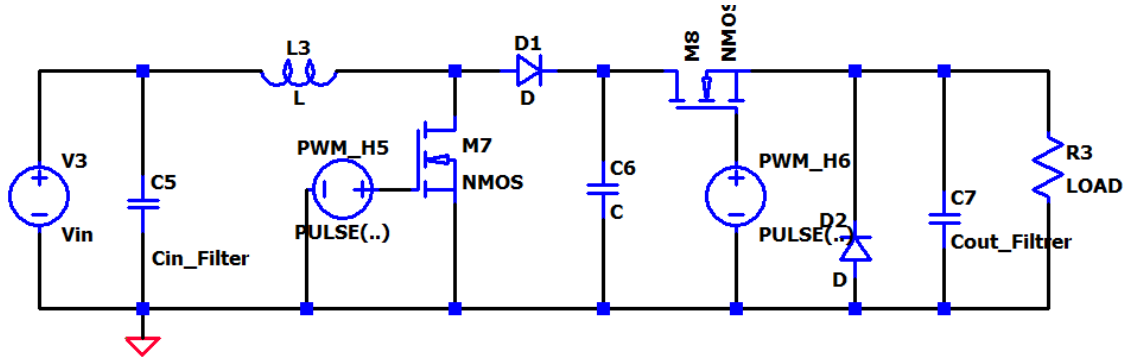


Figure 1.9 : Cascade Boost Buck

The inverting buck-boost is discarded because it inverts the polarity of the input voltage. SEPIC and Cascade Boost Buck are discarded due to the fact that they have two inductors, which are bulky, expensive in both costs and space requirements
On the other hand, NIBB has two additional switches which require less space in comparison but they dissipate more power and heats up the circuit more . Particular attention is then needed in the layout design in order to avoid too much overheating of the two switches.
In the table below there is a summary of the components needed for each topology

Topology	Passive Components	Active Switches	Inductors	Output Polarity
Nibb	3	4	1	Non-Inverted
Sepic	5	2	2	Non-Inverted
Buck-Boost	3	2	1	Invert
Cascade Buck-Boost	4	4	2	Non-Inverted

1.2 Transistor GaN Technology

Power Mosfet first appeared in 1976 outshining the old bipolar npn transistor. These devices were faster and proved more reliable than transistor since it could provide gate isolation, faster switching times ,less on-resistance and reliable gate control.
Nevertheless, one of the major problem of the Silicon Mosfet is that efficiency of Power Converters tends to drop significantly with switching frequency from 500 kHz onwards.

The Gallium Nitride Technology wants to keep high efficiency with faster switching frequency, with the goal of having a smaller MOSFET(given the same Breakdown voltage)and with less on-resistance . This allows the miniaturization of the circuits with more power-area ratio : with the GaN technology it is possible to design designed a 100W or even more Buck Converter with the size of a coin with 95% of efficiency even at 1MHz.
To understand why a comparison between the GaN and Silicon on-resistance can be seen in Figure (3.1) : with the same Breakdown voltage the GaN shows significant reduction (3 orders of magnitude or even more)

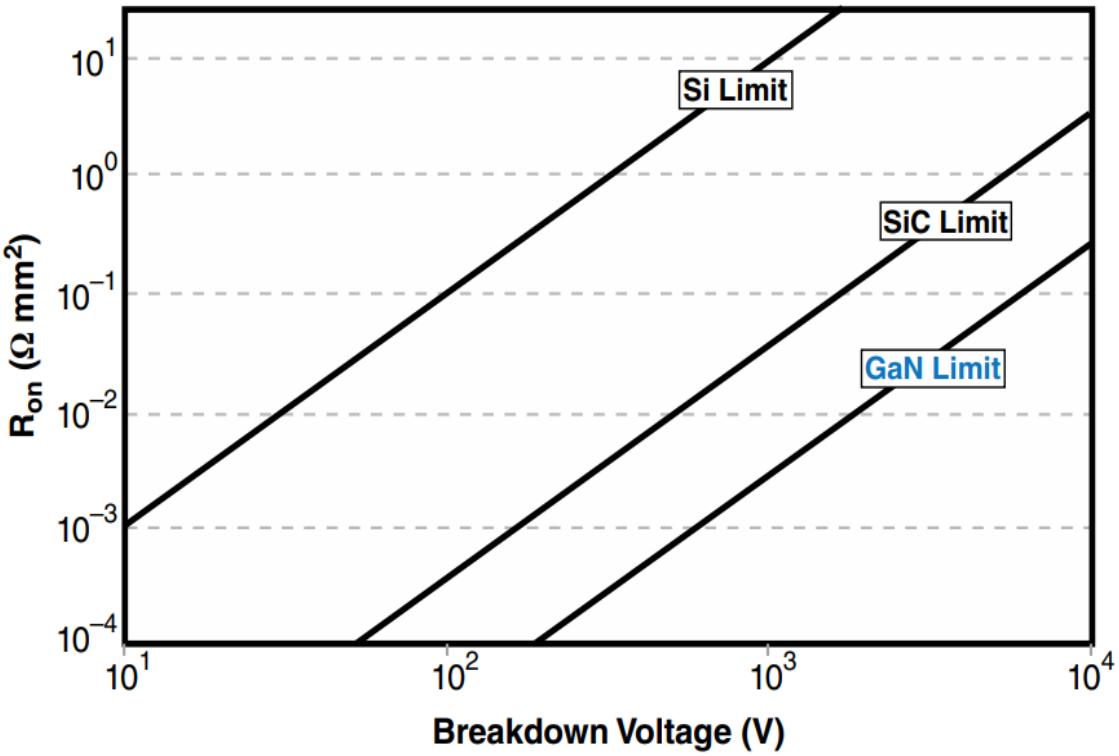


Fig 1.10 Rds on comparison vs Breakdown voltage[3]

Rds-on Temperature dependence

The Power Switch selection for any Power Converter is made by taking into account some key parameters.
The first is the dependence on the Ron Resistance vs Junction temperature . From the figure 3.2 it is clear that GaN Techonology allows to have less dependence with temperature's rise. For example, at T= 150 C a Silicon Mosfet has a more than double the normalized resistance , while the GaN less than double. Supposing, for instance, an on-resistance of 10m**Ω** for both transistor, at T=150 Silicon Mosfet will have more than 25m**Ω**, while the GaN Mosfet only 18m**Ω**.

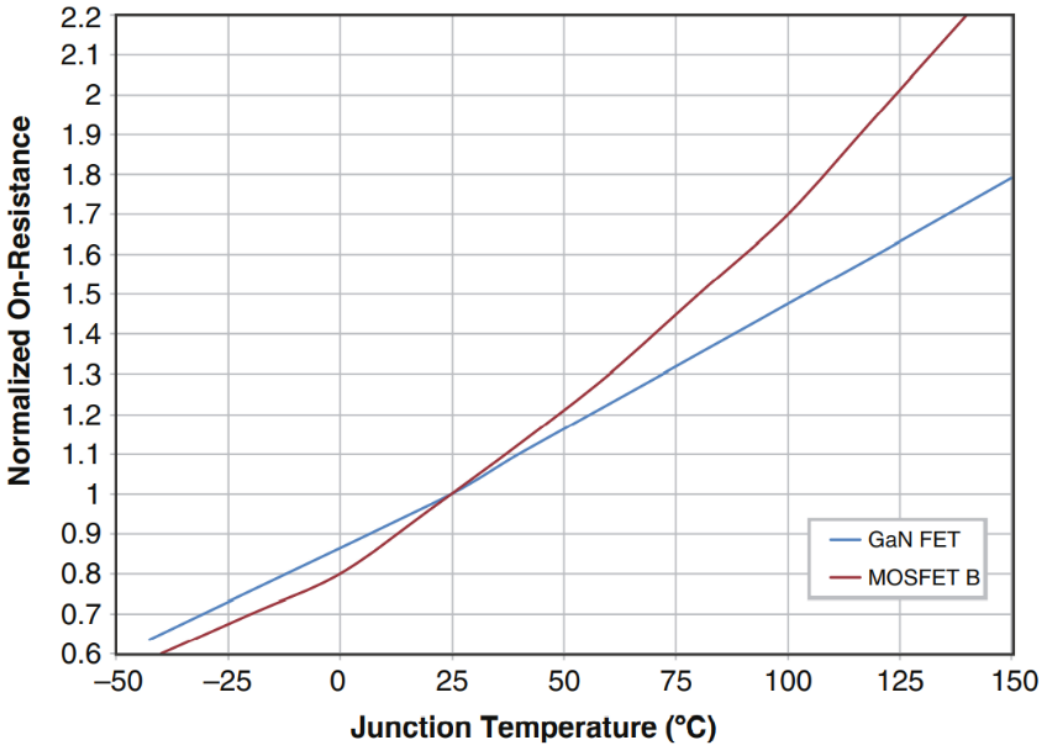
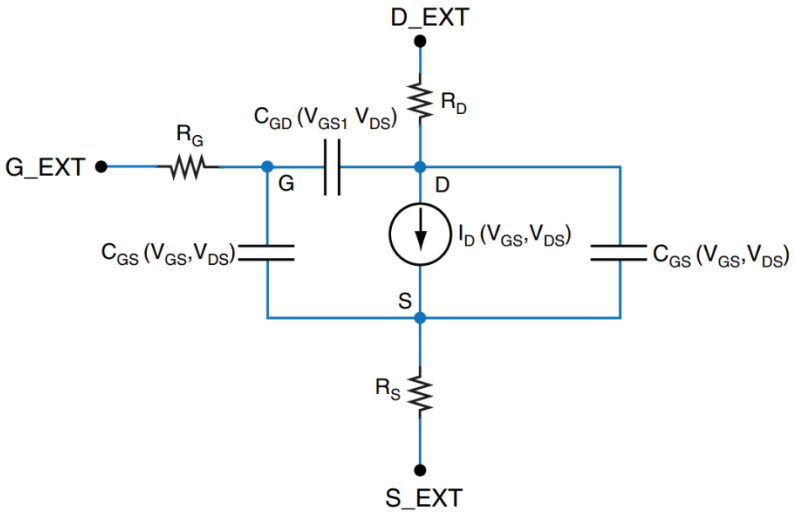


Fig 1.11 GaN vs Silicon Ron dependence of temperature[3]

Parasitic Capacitances

In every power mosfet there are some parasitic capacitances that must be taken into account. It's a significant factor in determing how much energy will be lost during the on-off transition. Hence the capacitance determines the amount of charge that need to be supplied to change the voltage across the terminals. The faster it is supplied, the faster the device[2]. An electrical Model of the parasitic Capacitance is shown in the figure 1.12



[3] Figure 1.12 Electrical Modeling of Mosfet

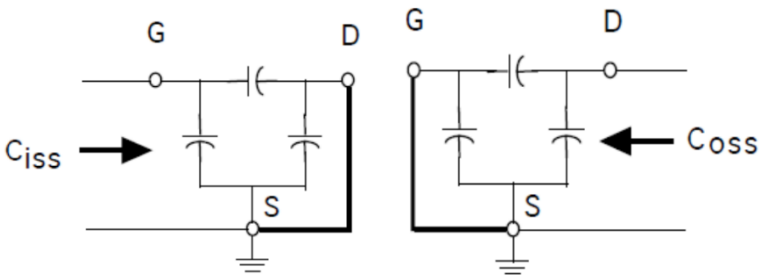
Where:

- Cds is the depletion layer of the drain-source junction
- Cgs is large, prattically constant w.r.t the voltage applied
- Cgd is strongly non linear, varies with the applied voltage
- Rs, Rd and Rg are constant parasitic resistance and they depend on package termination resistance and other fabrication processes.
- Drain Current Id is a non linear function of the Gate-Source Voltage and Drain Source Voltage

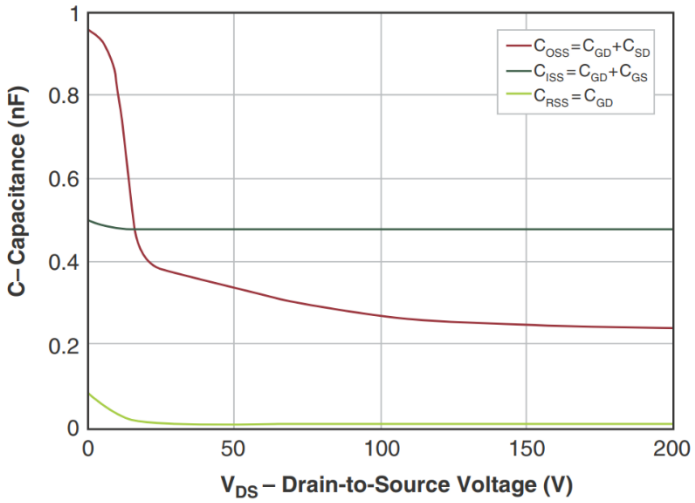
Switching Times are influenced by how much fast the gate driver can charge/discharge the Cgs and Cgd [4].
Usually datasheet gives the input and output parasitic capacitances of the MOSFET, defined as follows in eq(2) and eq(3). A graphical representation of the parasitic capacitances and their dependence of the Drain-Source Voltage is shown if figure 3.4

$$C_{iss} = C_{gs} + C_{gd} \tag{2}$$

$$C_{oss} = C_{gd} + C_{ds} \tag{3}$$



[4] Figure 1.13 Input/Output Parasitic Capacitances



[3] Figure 1.14 Parasitic Capacitances and their voltage dependence

Turn on-off

The two following circuits designed in LTSPICE, shows the effect of the parasitic capacitances previously seen, (fig1.15) used to compare the turn on-off of the two mosfet. The first is a Silicon Mosfet IRFP240 and the second is an EPC2001, coming from Efficient Power Converter GaN Techonology

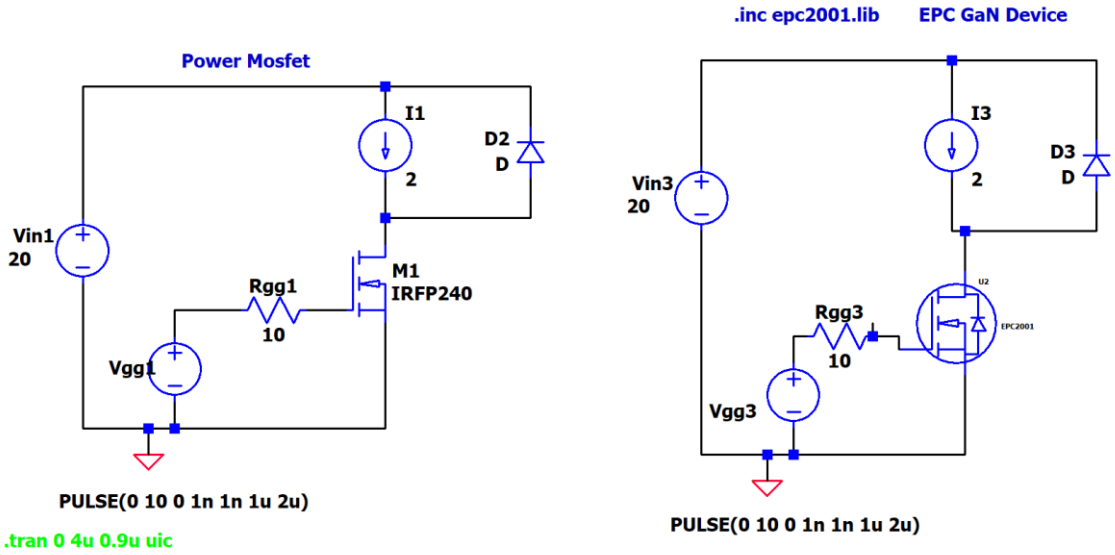


Figure 1.15 Test Circuit LTSPICE XVII To simulate turn on/off

The simulation results can be seen in the figure 1.16
The first plot pane shows the Drain Current, while the seconds shows the Drain Voltage. The results shows crealy that the GaN Transistor(respectively grey for current and blue for voltage curve) has faster rising time than Silicon Mosfet(respectively red for current and green for voltage curves). Specifically,EPC2001 has 10ns as rise time, while IRFP240 48ns.

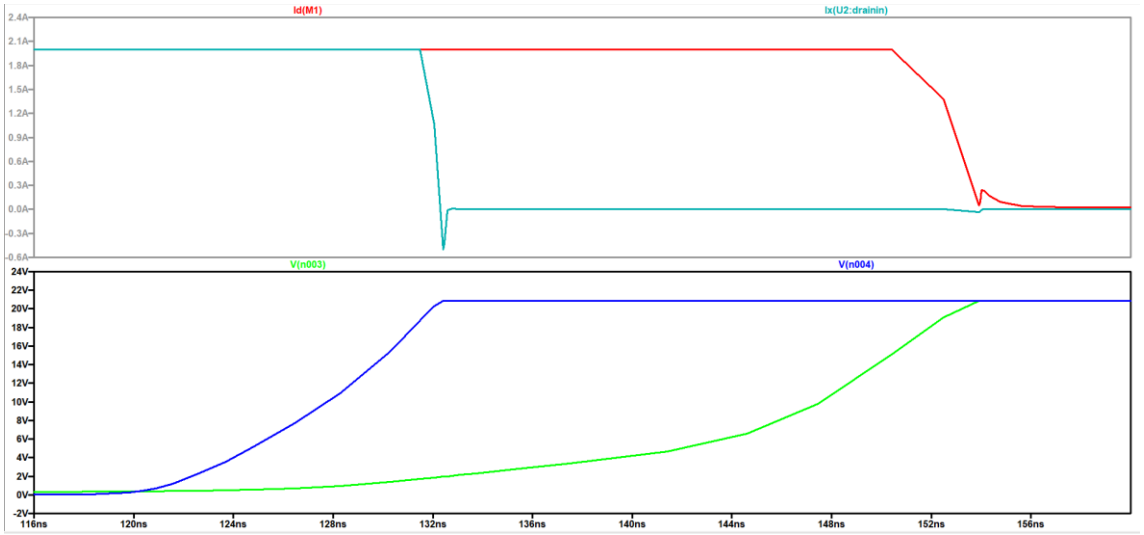


Figure 1.16 Simulation results of circuit in figure 1.15. Top Plot Pane shows the currents. Bottom Plot Pane shows voltage

As a consequence, the power dissipated by the GaN will be higher but lumped in 5ns, while the Silicon in 30ns, as shown in fig 1.17

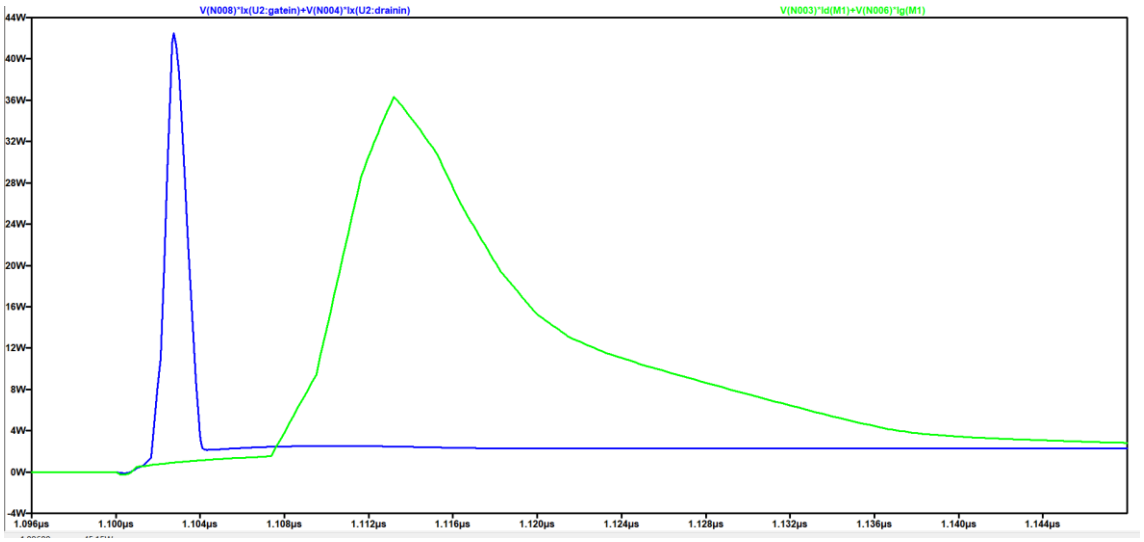


Fig 1.17 Dynamic Power dissipated during on-off transition of GaN(blue) and Silicon Mosfet(Green)

Transistor Driving Tecniques

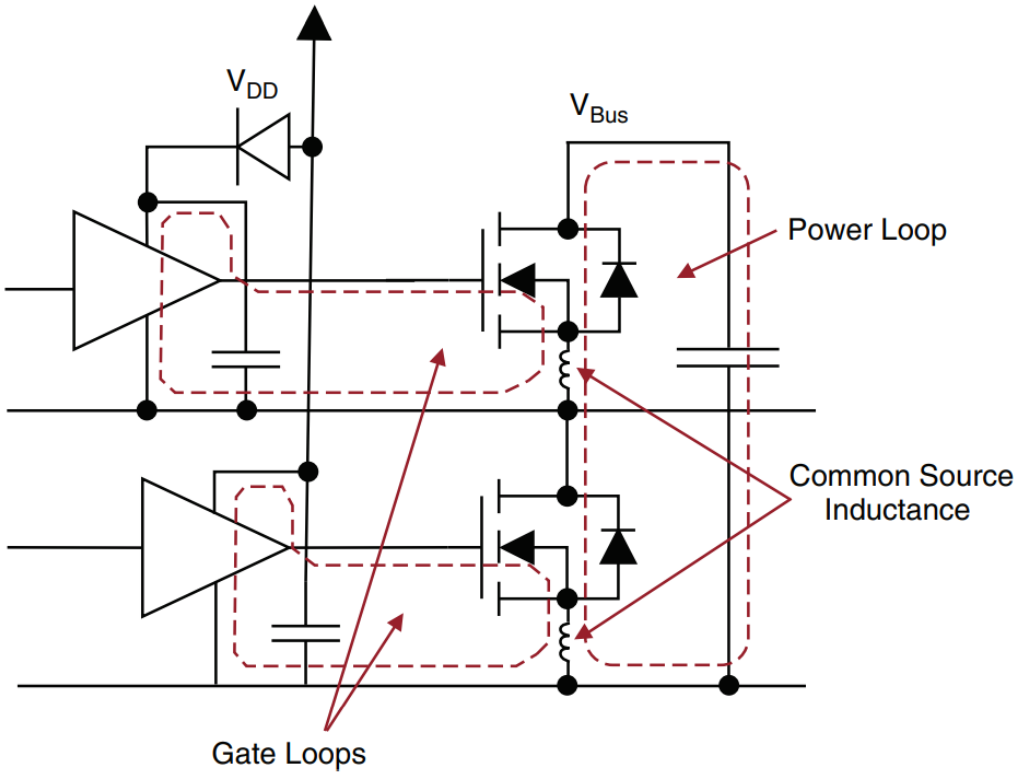
Power Mosfets need a driver to shift the control signal coming from the digital domain(Low Voltage and Low Current) to the power electronic domain, which requires higher current and voltages.
The faster switching speed also increases the the impact of parasitic inductances on the performance.

For a half-bridge configuration, there are two main power loops to consider:

1) The high-frequency power loop formed by the two GaN

2) The gate drive loop formed by the gate driver, power device, and high-frequency gate drive capacitor[3]

These two loops are showed in figure 1.18



[3] Figure 1.18 Half Bridge Power Stage with Parasitic Elements ,Gate loops and Power Loops

An LTSPICE simulation of an Ideal Synchronous Buck in Half Bridge Configuration with and without the parasitic element is shown to highlight the effect of the two inductive loops. The circuit is shown in fig. 1.19 while the simulation results in Fig 1.20. A switching frequency of 400 kHz has been used and a 6.8uH as a test inductor. The output results shows the Switching Node Voltage , which in the ideal case switches between 0V and Input Voltage Vin=30V

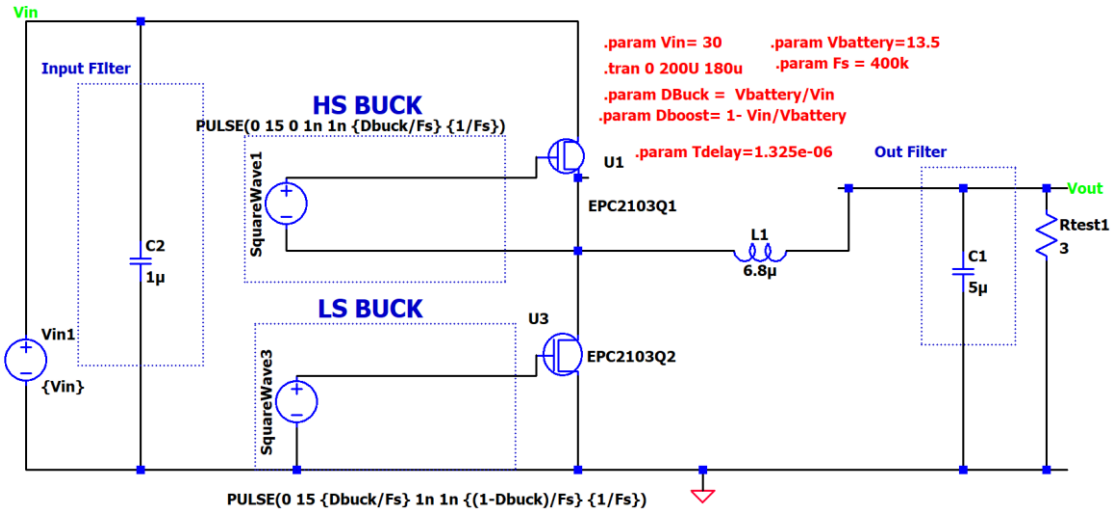


Fig 1.19 Ideal Synchronous Buck Converter LTSPICE

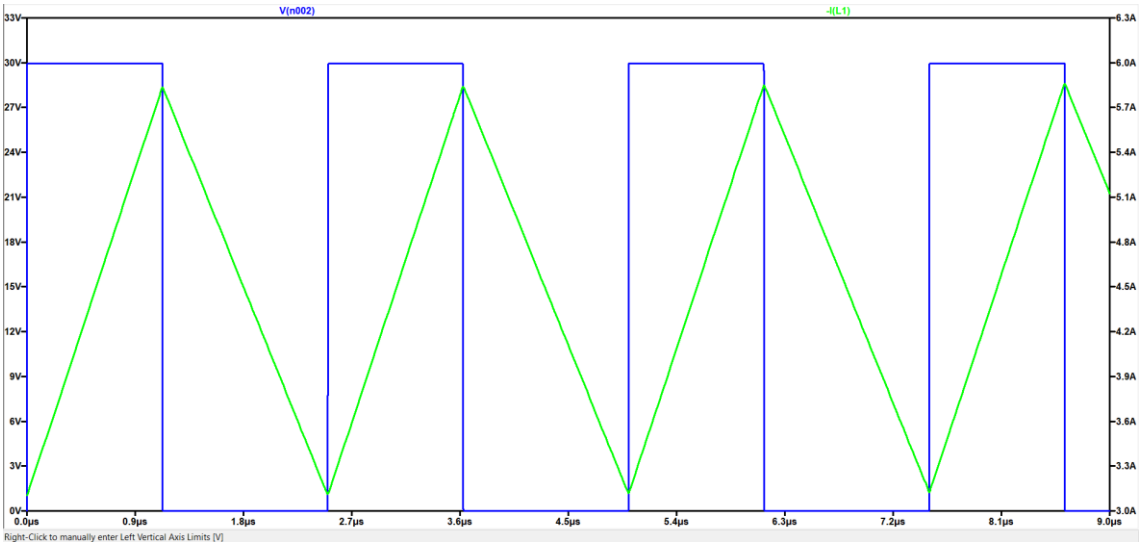


Fig 1.20 LTSPICE Simulation result of an ideal Synchronous Buck Converter

Now ,by adding the following elements

- Gate loop inductance

- Common Source Inductance
- Drain Parasitic Inductance
- Trace parasitic Inductance between Gate and GaN
- Internal Resistance of Gate Driver and Gate Resistance GaN

The circuit becomes as follows in Fig 1.21
In the Fig 1.22 the difference with the previous simulation are shown. Here there are dangerous spikes, which, if not attenuated properly they can damage permanently the GaN Mosfet by exceeding the maximum Drain-To-Source Voltage Rating . These parasitic effects are even more present with the increasing of the switching frequency. Hence, a particular attention to the Layout Design must be made in order to fully exploit the advantages of the GaN System Technology

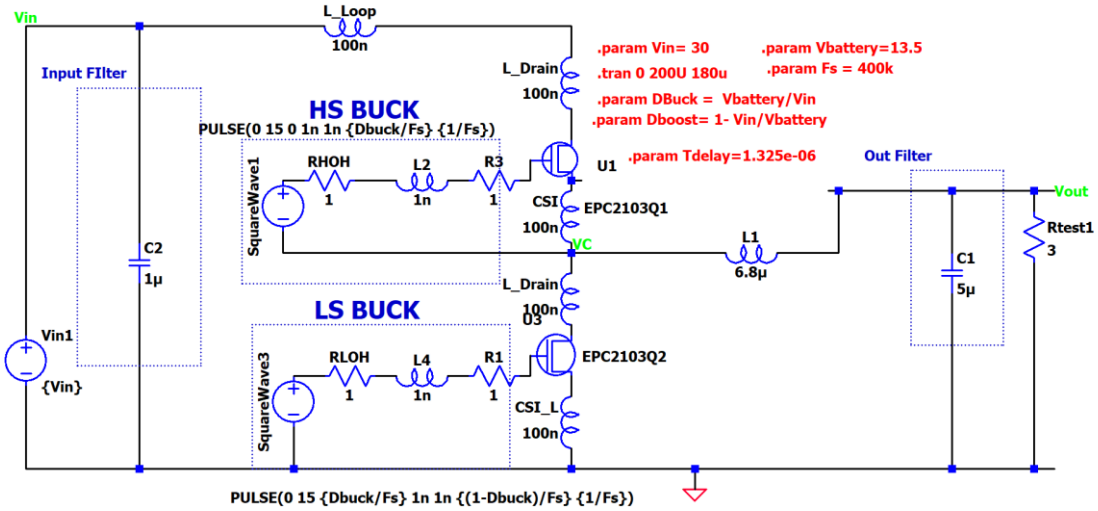


Fig. 1.21 LTSPICE Simulation of Synchronous Buck Converter with parasitic inductances

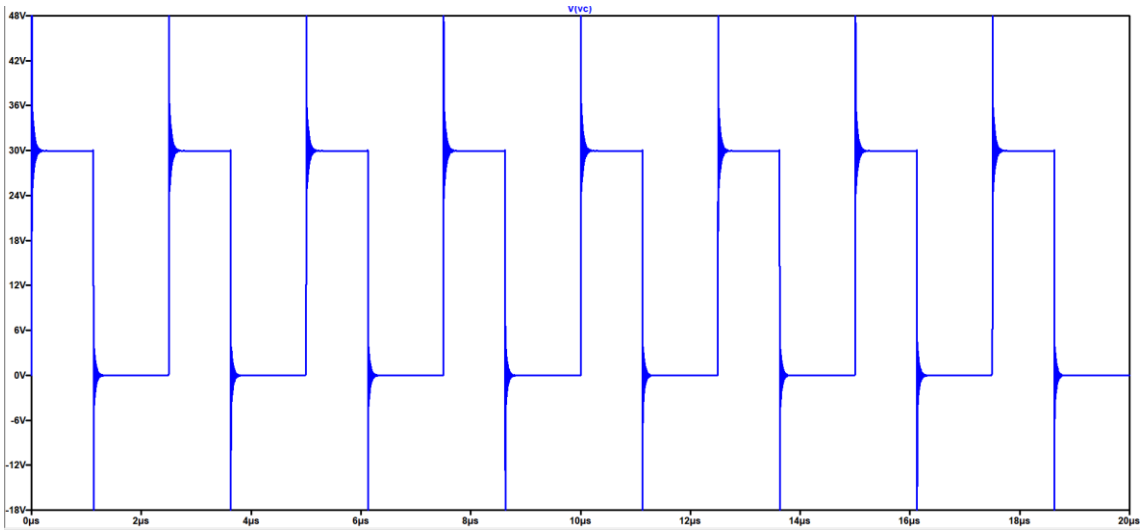


Fig. 1.22 LTSPICE Simulation Results of Synchronous Buck Converter showing the effect of the parasitic inductance on Sw Node

If those spikes are present during the testing, an RC series Snubber can be implemented between the GND and Switching Node to dump the ringing oscillation as shown in Fig 1.23. The problem in this solution is that the rising and fall time are significantly reduced, and even if the GaN is shielded by the ringing noise, not all the potential of GaN Technology is fully exploited.

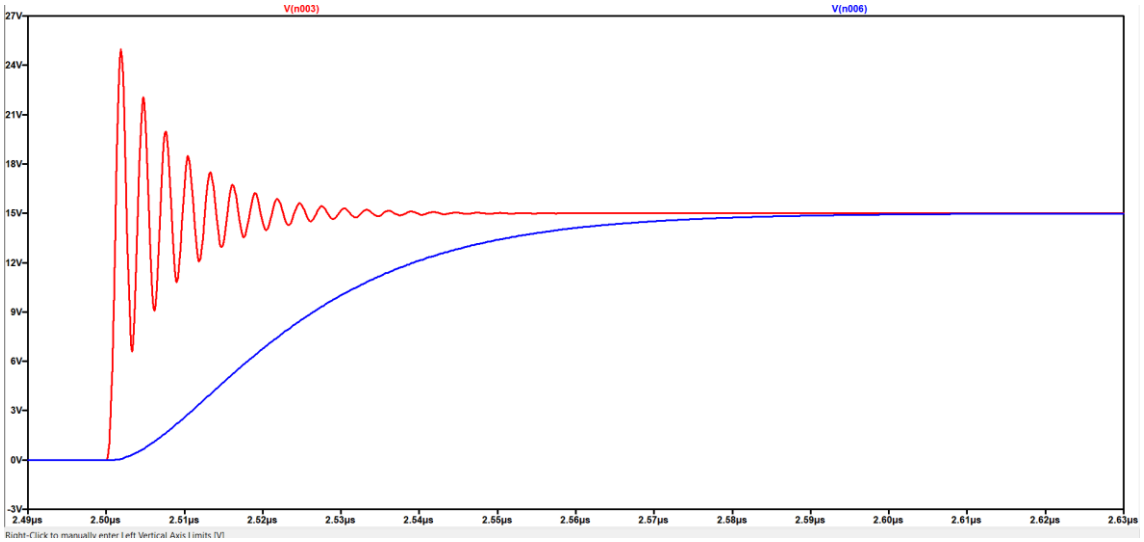
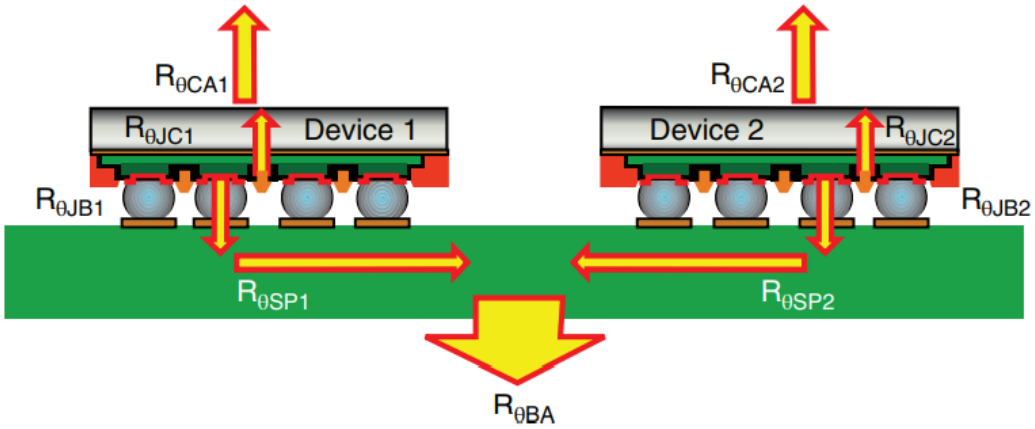


Fig. 1.23 LTSPICE Simulation of a noisy square wave with and without snubber circuit

Transistor Thermal Modelling

The thermal modelling of the Half Bridge Configuration GaN can be done as any other mosfets. The following thermal resistances are considered shown in Fig 1.24

- Rca = Thermal Resistance Case- Ambient
- Rjc = Thermal Resistance Case- Junction
- Rjb = Thermal Resistance Junction- Board
- Rsp = Thermal Resistance between the two GaNs
- Rba = Thermal Resistance Board- Ambient



[3] Fig. 1.24 Half Bridge GaN Configuration Thermal resistances

Even in this case, LTSPICE can be sed to perform a Thermal Analysis. The data found in the datasheet of EPC2206 is used as an example, like shown in the fig 3.15 below

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.4	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	1.1	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	42	

[3] Fig. 1.25 Thermal resistances of EPC2206

To use Electrical Elements in order to perform the Thermal Analysis, the conversion between electrical and thermal domain is exploited:

Electrical Domain	Thermal Domain
Voltage Source [V]	Temperature [C]
Current Source [A]	Heat Flow [W]
Electrical Resistance [Ω]	Thermal Resistance [C/W]
Electrical Capacitance [F]	Thermal Capacitance [Ws/K]

Hence, if the current source (Power Loss) is used as an input of the thermal model and the Thermal resistances as a device which opposes the Heat flow, the Voltages across the resistors hence is the equivalent the temperature. If thermal capacitances are take into account , the thermal transient can be modelled.
Therefore, designing a suitable heat sink will prevent the junction temperature to reach the Maximum Operating Temperature of the EPC2206 which is about 150 C.
In the figure 1.26 is shown the LTSPICE Half Bridge model, while in the figure 1.27 the Simulation result with a switching power source.

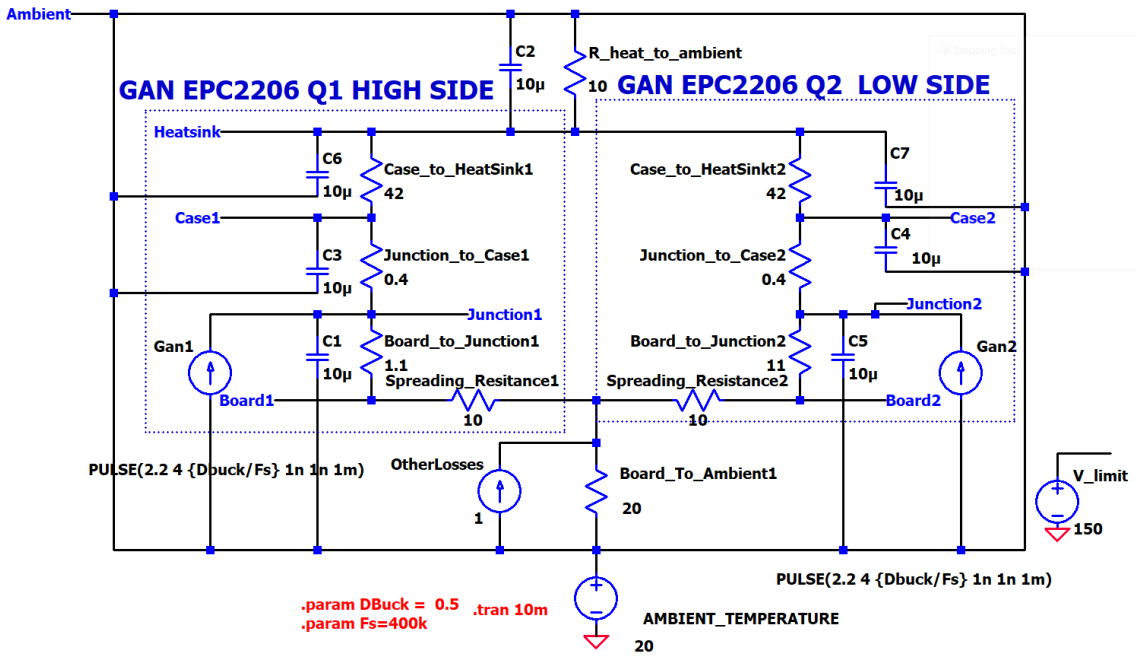


Fig. 1.26 Equivalent Thermal Model of Half Bridge Configuration

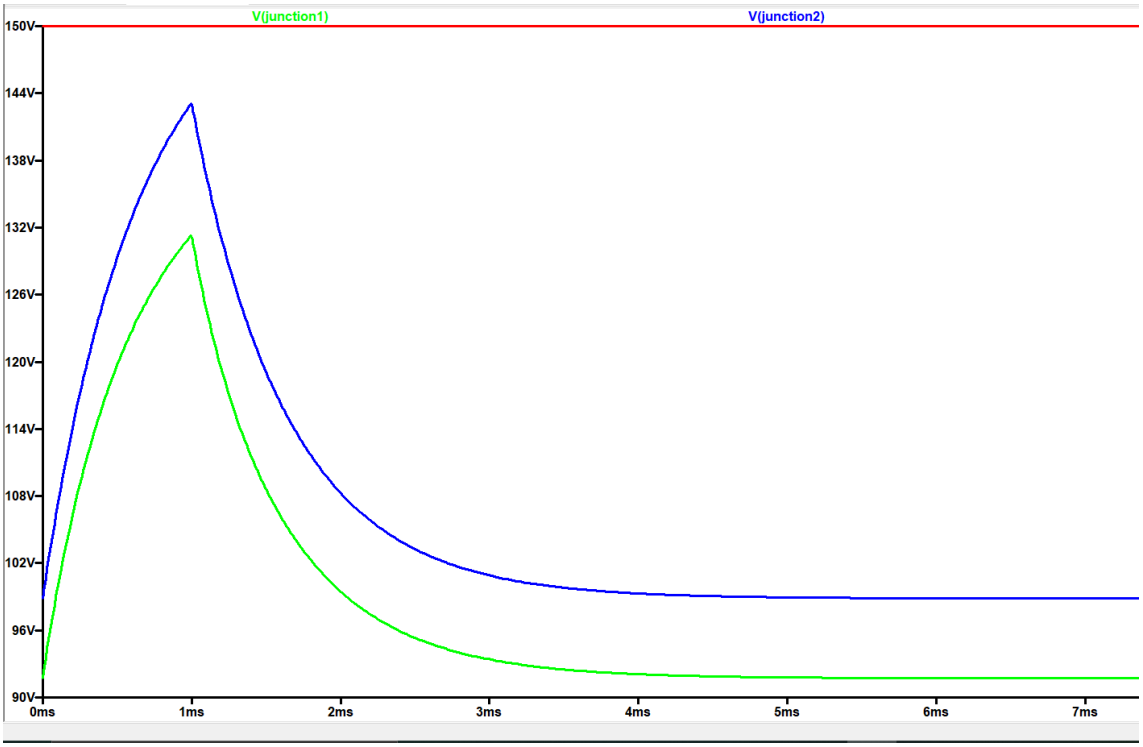


Fig. 1.27 Thermal Simulation Result of Thermal Model
In Red, Maximum Operating Temperature (150 C)
In Blue and Green, the Junction Temperature Curves of each GaN

Chapter 2
Power Converter Design

From the previous study it was determined that the Non inverting Buck Boost was the best suitable choice for this projec

In this chapter all the design phases are covered.
Starting by modelling the duty Cycle for each working voltage condition, all the power components design and choice are then explained (Power Inductor , GaN ,input/output filters and drivers)
In the next subchapter all the measure stage design is shown: starting from an high level design of the stage, then going in deep showing the design and choice of opamps, sensor current and shunt.
The last subchapter shows how all the component choice and design impact on the losses of the converter, hence the estimated efficiency.

This section presents how power components are design and which criteria were used to select the most suitable for the project

2.1 Non Inverting Buck Boost

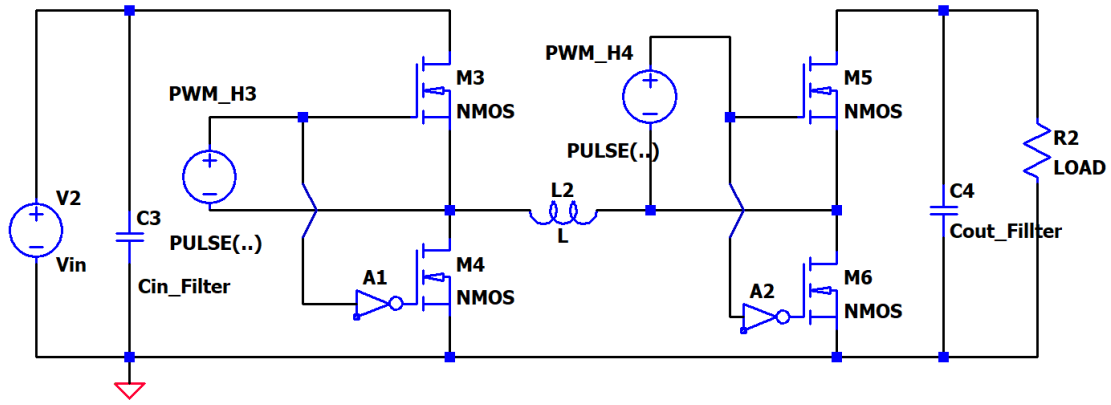


Figure 2.1 : NIBB

Buck Mode and Buck Boost Mode

The general equation(4) that describes the duty cycle of the NIBB is

$$D_{NIBB} = Vin * \frac{Da}{(1 - Db)} \tag{4}$$

Where Da and Db are the duty cycles given by the controller to drive the Buck Leg and Boost Leg using the Dual Carrier modulation tecnique, which exploits one unique signal to drive an half bridge leg

By diving the converter in the buck leg (two Mosfet on the left) and the boost leg (two Mosfet on the right), the working principle of the NIBB is easier to understand. As a reference it will be refered Dbuck as the duty cycle of the buck leg and Dboost as the duty cycle of the boost leg, having that:

- Dbuck=100%, Q1= ALWAYS ON, Q2=OFF
- Dboost=100% Q4= ALWAYS ON, Q3=OFF

Setting Null duty cycle of the boost leg results in having the high side boost switch always on, hence with direct connection between inductor and the load , making the circuit behave like a step-down converter. Operating when the output voltage is lower than the input voltage. It can be seen in the figure below.

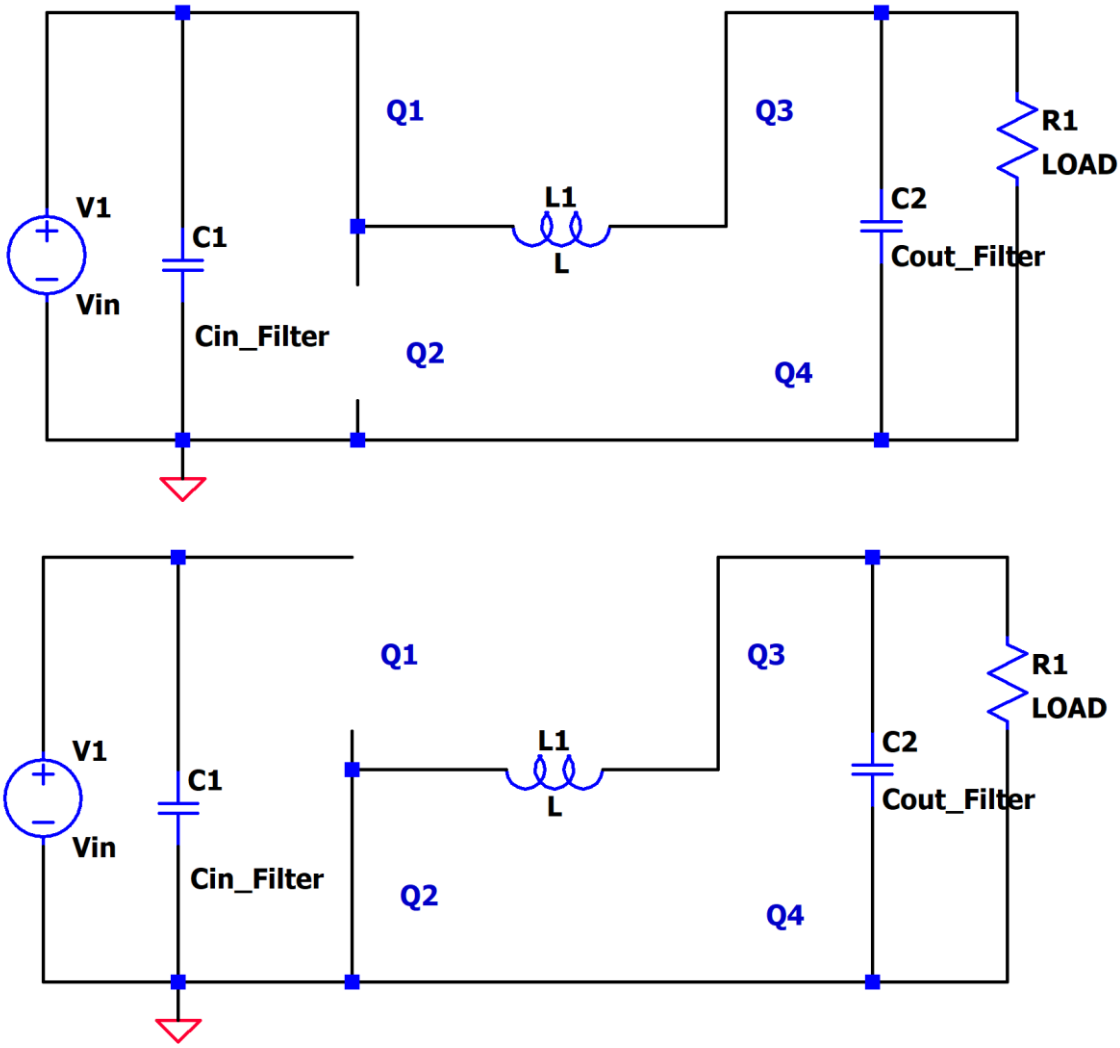


Figure 2.2 : Buck Converter Mode

By setting instead Dbuck =100% then Q1 is always ON and Q3 Q4 are switching according to the PWM signal given by the controller: the circuit behaves like a boost. Operating when $V_{out} > V_{in}$.
This can be seen in the figure 2.3

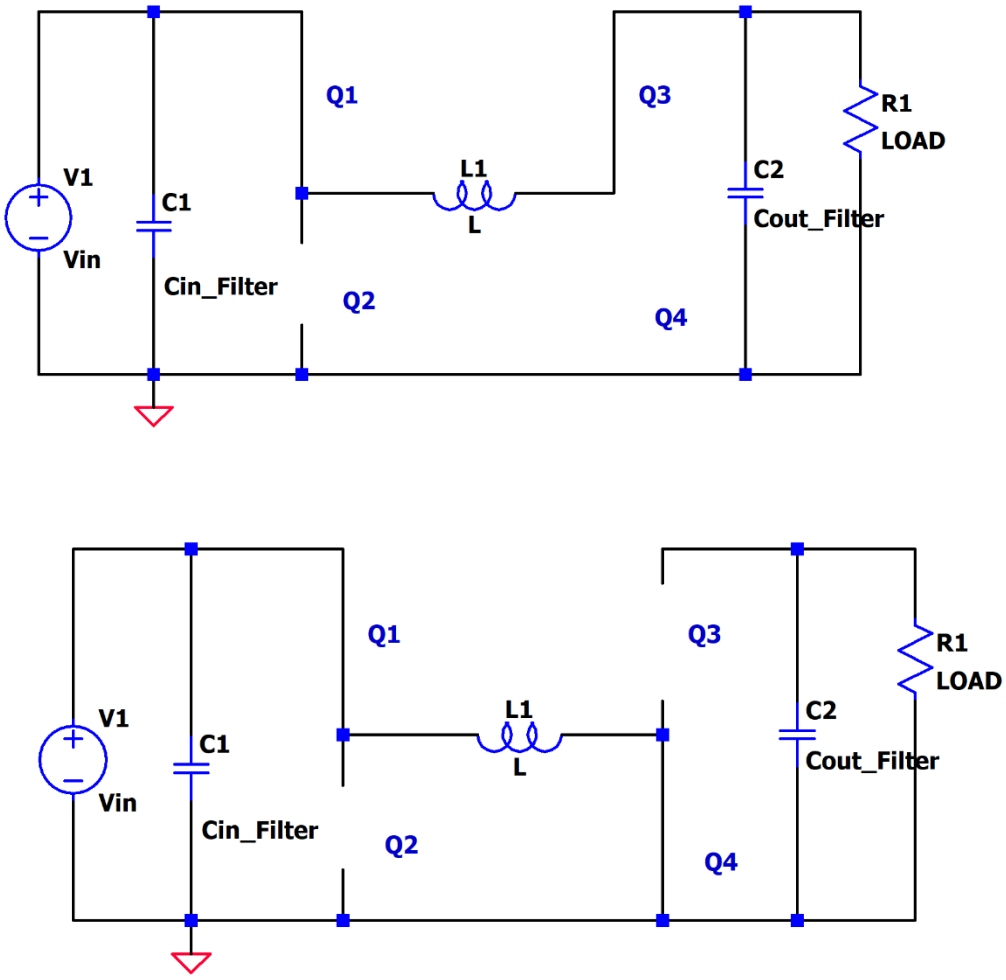


Figure 2.3 : Buck Converter Mode

Using the second volt-balance law, the corresponding Duty Cycles are found, assuming CCM conditions(Continuos Conduction Mode). This assumption is correct since the design of the inductance is to make the NIBB Work in CCM. The duty Cycles in Buck region and Boost region are written in eq. (5) and (6)

$$D_{buck} = \frac{V_{out}}{V_{in}} \tag{5}$$

$$D_{boost} = 1 - \frac{V_{in}}{V_{out}} \tag{6}$$

Buck Boost Mode

Owing to the limitations given by the previous founded duty cycles, it can't cover the case in which $V_{in} \approx V_{out}$
Since both the four legs are switching, the NIBB can be modelled as a cascade boost buck, by multiplying the previous founded duty cycles with the gain of the boost and buck respectively.
Hence, in this case, the duty cycles becomes as follow in the eq.(7) (8) defined below:

$$D_{buck(B-B)} = \frac{V_{out}}{V_{in}} \quad (1 - D_{boostmin}) \tag{7}$$

$$D_{boost} = 1 - \frac{V_{in}}{V_{out}} \quad D_{buckmax} \tag{8}$$

Where $D_{buckmax}$ and $D_{boostmin}$ are the maximum and minimum achievable duty cycles, which depends on transistor type, switching frequency and so on. Setting $D_{buckmax}$ =0.95 and $D_{boostmin}$=0.05, the range of the buck boost region is defined with a parameter p=2V. The duty cycles of the buck boost region are defined in eq. (9)and (10) and the plot of their Duty Cycles in the figure 2.4

$$V_{out} - p < V_{in} \leq V_{out}$$
$$D_{buck} = D_{buckmax} = 0.95 \qquad D_{boost} = D_{boostB-B} \tag{9}$$

$$V_{out} < V_{in} \leq V_{out} + p$$
$$D_{boost} = D_{boostmin} = 0.05 \qquad D_{buck} = D_{buckB-B} \tag{10}$$

Here a table to resume all the working points of the circuit

Mode	Input Voltage	Mainly Active Mosfets
Boost	$V_{in} \leq 11.5V$	Q3-Q4
Buck	$V_{in} \geq 15.5V$	Q1-Q2,
Buck-Boost	$11.5V < V_{in} < 15.5V$	Q1-Q2-Q3-Q4

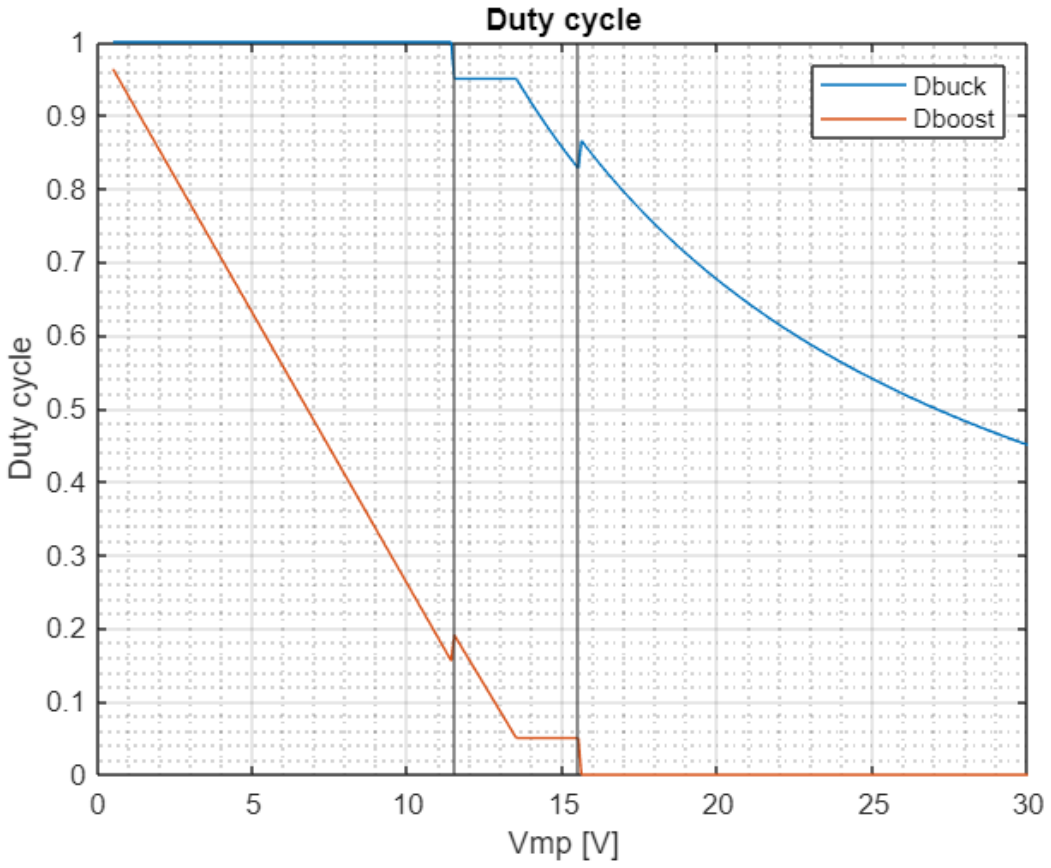


Figure 2.4 : Duty Cycles of Boost,Buck Boost and Buck Region

Inductor Design

To design any DC-DC converter it is necessary to start from the lowest possible inductance to make the circuit work in the CCM condition,since, w.r.t. to the DCM, the circuit present significant less stress onto the components as well as an increase in efficiency.

Since the Non Inverting Buck Boost has three operating region, it is necessary to both the condition for Buck and Boost minimum allowable inductance in order to stay in CCM for any given voltage,like shown in the equation below (11) (12).

[4] Hence, for the buck CCM condition it is needed :

$$L > \frac{R_0(1 - D_{buck})}{2f_{sw}} \tag{11}$$

[4] While for the boost CCM condition :

$$L > \frac{R_0(1 - D_{boost})^2}{2f_{sw}} D_{boost} \tag{12}$$

Where $R_0 = \frac{V_{out}}{I_{out}}$ is the output load resistance. Since the previous equation depends strongly on the switching frequency, a simulation analysis for a suitable range of possible switching frequencies is mandatory.
Running the matlab script the plot 2.5 is then created.

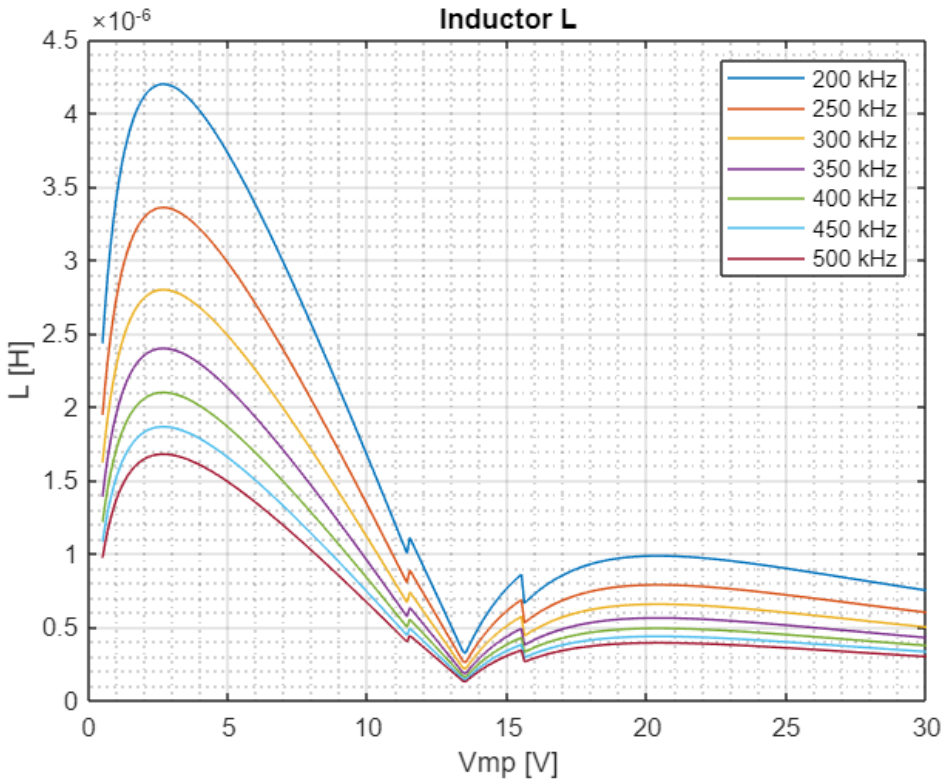


Fig 2.5 Inductance vs (Input Voltage) for each switching frequency

As it can be seen from the plot, as the switching frequency rises, so the minimum inductance decreases

By a practical point of view, having an higher inductance implies a heavier, bulkier and more space demanding inductance in the PCB, which is something that must be avoided since this thesis aims to design a small power board.
Moreover, it is not easy to find an high inductor with a suitable saturation current.

GaN Mosfet can even keep efficiency for higher frequencies than Silicon Mosfet, so the switching frequency is set to 400 kHz

The minimum allowable inductor then becomes L= 2.2 uH in the Boost Region like shown in fig. 2.6 at the previous selected frequency.

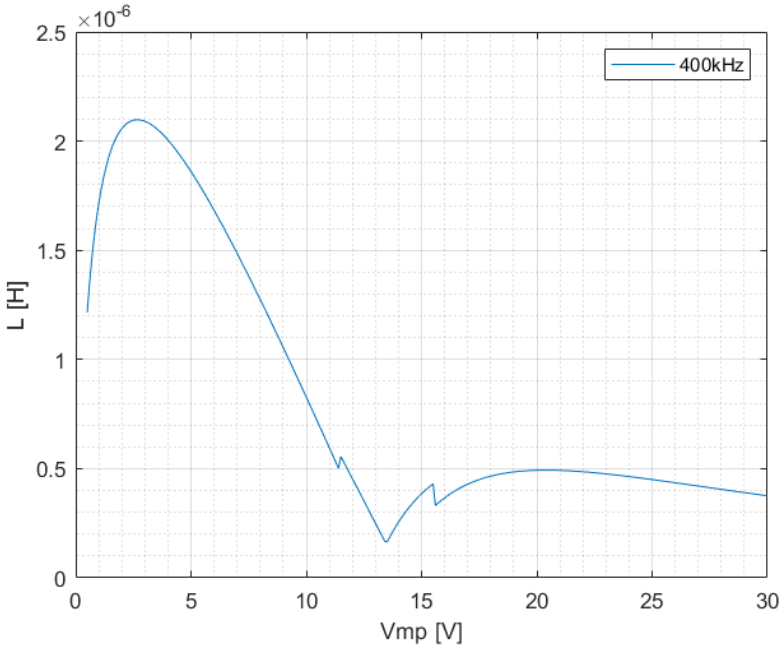


Fig 2.6 Inductance vs Input Voltage at 400kHz

Another two parameters to take into account are the Rms and average current which will be both useful to calculate losses and select the proper inductor.
Since the working condition is the CCM mode, the average current will be approximately equal to the RMS current, like shown in equation 13 and 14 . Their value in function of the duty cycle are shown in equation 15 and 16 .
NB: All these equation used to design inductance and capacitance, are all taken from the Power Electronics Course [4]

$$I_{Buckrms} \approx I_{out} \approx I_{Buckavg} \tag{13}$$

$$I_{Boostrms} \approx I_{out} \approx I_{Boostavg} \tag{14}$$

$$I_{\text{Lbuck }(B-B)RMS} \approx I_{\text{Lbuck }(B-B)\text{ ave}} = \frac{I_{\text{out}}}{1 - D_{\text{boostmin}}} \tag{15}$$

$$I_{\text{Lboost }(B-B)RMS} \approx I_{\text{Lboost }(B-B)\text{ ave}} = \frac{I_{\text{in}}}{D_{\text{buckmax}}} \tag{16}$$

To select the proper inductor the maximum rated current must be calculated which flows in the power inductor, obtained by summing the average current and half of the estimated ripple, showed in equation 17,18,19,20 and their relative plot showed in fig 2.7 2.8 2.9.

$$I_{Lbuckmax} = I_{Lbuckave} + \frac{\Delta I_{buck}}{2} \tag{17}$$

$$I_{Lbuckmax} = I_{Lbuckave} + \frac{\Delta I_{buck}}{2} \tag{18}$$

$$I_{Lbuck\,(B-B)\,\text{m}} = I_{Lbuck\,(B-B)\,ave} + \frac{\Delta I_{buck\,(B-B)}}{2} \tag{19}$$

$$I_{Lboost\,(B-B)\,\text{m}} = I_{Lboost\,(B-B)ave} + \frac{\Delta I_{boost\,(B-B)}}{2} \tag{20}$$

Where the ripple of the buck,boost and buck boost region are defined as follow in the equation 21,22,23,24:

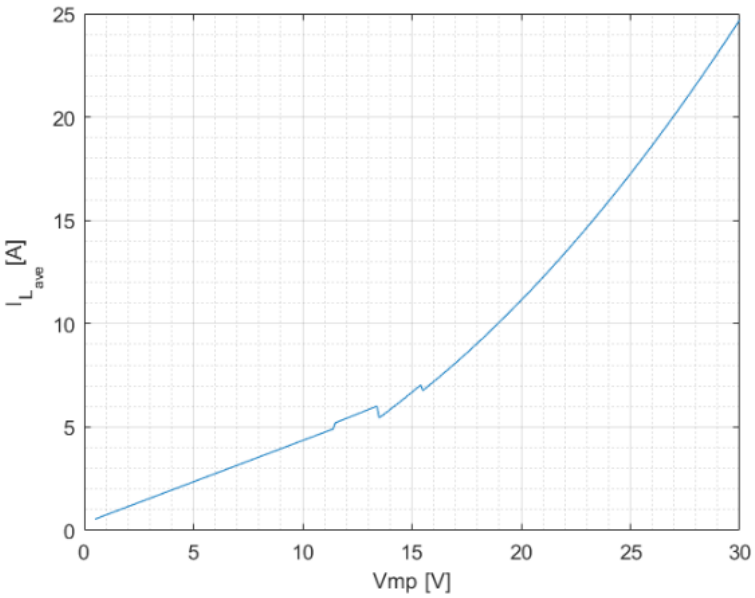
$$\Delta I_{buck} = \frac{(V_{mp} - V_{out})D_{buck}}{f_{sw}L} \tag{21}$$

$$\Delta I_{\text{boost}} = \frac{V_{mp}D_{\text{boost}}}{f_{\text{sw}}\,L} \tag{22}$$

$$\Delta I_{\text{buck }(B-B)} = \frac{V_{\text{out}}\left(V_{mp} - V_{\text{out}}\,(1 - D_{\text{boostmin}})\right)}{f_{\text{sw}}\,LV_{mp}} \tag{23}$$

$$\Delta I_{\text{boost }(B-B)} = \frac{V_{\text{in}}\left(V_{\text{out}} - V_{mp}D_{\text{buckmax}}\right)}{f_{\text{sw}}\,LV_{\text{out}}} \tag{24}$$

Fig 2.7 Average Inductor Current vs Input Voltage



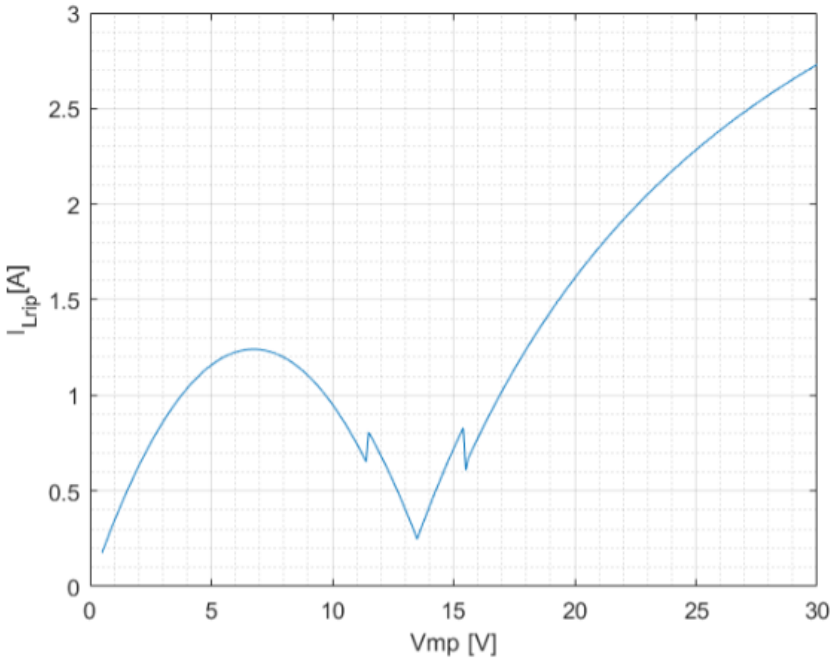


Fig 2.8 Maximum Inductor Current vs Input Voltage

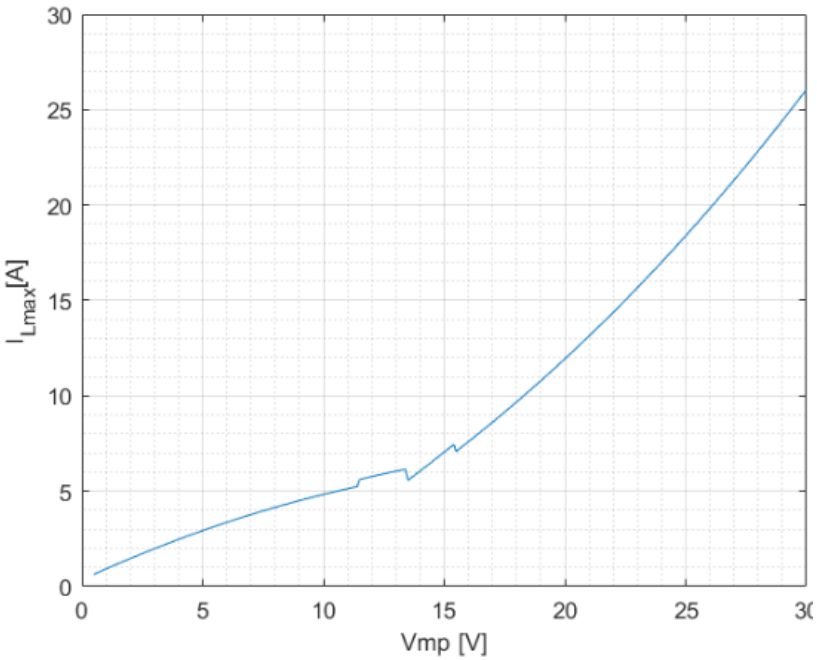


Fig 2.9 Peak to Peak Inductor Ripple vs Input Voltage

Inductor Selection

In order to choose a suitable power inductor, the following features should be taken into account:

1. Inductance Value : Henry [H]

2. Rated Current : max rms current which can flow in the power inductor without overheating[4]

3. Saturation Current : current at which the phenomenon of core saturation occurs and the value of the inductance drops significantly

4. Series Resistance : parasitic ESR resistance, should be as low as possible to minimize losses

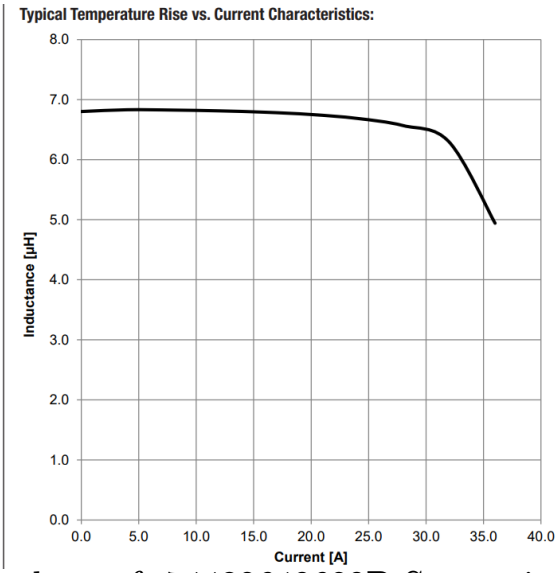
5. Maximum frequency : greatly influenced by the material [7]

6. Maximum Voltage : depends on the insultation material used between the coil windings [7]

From the previous calculation, a suitable inductor of value L=6.8uH is the Wurth Elektronik 7443640680B, since it has low DC resistance, suitable Ra

Properties		Test conditions	Value	Unit	Tol.
Inductance	L	100 kHz/ 10 mA	6.8	µH	±20%
Rated Current	$I_{R,50K}$	ΔT = 50 K	47.5	A	max.
Performance Rated Current [1)]	$I_{RP,40K}$	ΔT = 40 K	59.2	A	max.
Saturation Current @ 10%	$I_{SAT,10\%}$	|ΔL/L| < 10 %	31.9	A	typ.
Saturation Current @ 30%	$I_{SAT,30\%}$	|ΔL/L| < 30 %	36.3	A	typ.
DC Resistance	R_{DC}	@ 20 °C	0.88	mΩ	typ.
DC Resistance	R_{DC}	@ 20 °C	0.97	mΩ	max.
Self Resonant Frequency	f_{res}		18.8	MHz	typ.

[8] Fig 2.10 Datasheet of 74432640680B Electrical Proprieties



[8] Fig 2.11 Datasheet of 74432640680B Saturation Current and Inductance Losses

By using the previous Nibb circuit on LTSPICE simulating it with a .step param, the previous theoretical results are confirmed. As shown in figure 2.11 when the inductance is exactly L=6.8uH the current is less than 1.5A as ripple. By using the mimum value (2.2uH) instead, the ripple becomes too high since inductor current swings from 1.5A to 8A, resulting in too much stress for the components.

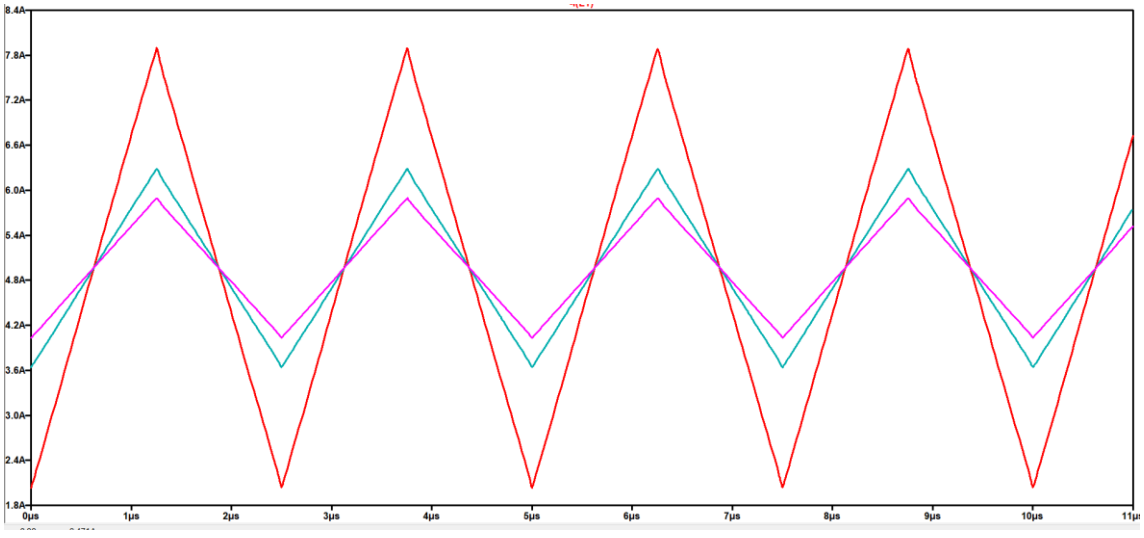


Fig 2.11 LTSPICE Simulation of NIBB Inductor current with different value of inductance (Red=2.2 uH, Blue=4.8uH, Violet=6.8uH)

Input Capacitor

The input capacitor is chosen by considering the following features:

1. Working Voltage
2. RMS Current
3. Maximum Rated Current
4. Parasitic Resistance(ESR) and Inductance(ESL)
5. Topology(Ceramic,Electrolitic,Film,Polypropilene,etc..)

The working voltage is the open circuit output voltage of the generator (60V).

The RMS calculation are mandatory since produces a temperature rise owing to the ESR. From equation 25 and its relative plot in fig 2.12, the maximum value is expected in the buck region.

The ESL instead is a series parasitic element which limits the maximum operating frequency of the capacitor.

$$I_{\mathrm{CinRMS}} = \begin{cases} I_{\mathrm{out}} \sqrt{\dfrac{V_{\mathrm{out}}}{V_{mp}}\left(1 - \dfrac{V_{\mathrm{out}}}{V_{mp}}\right)} & \textit{buck mode} \\ \dfrac{\Delta I_{\mathrm{boost}}}{\sqrt{12}} = \dfrac{V_{mp} D_{\mathrm{boost}}}{f_{\mathrm{sw}}\, L\sqrt{12}} & \textit{boost mode} \end{cases} \tag{25}$$

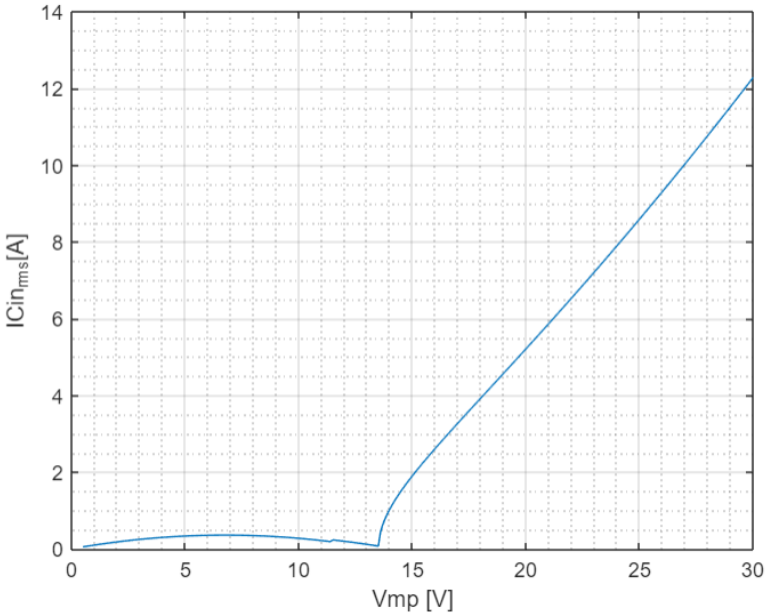


Fig 2.12 : RMS Input Current

For what regards the buck-boost, the same formula like the boost mode is used when $V_{out} - p < V_{in} \leq V_{out}$ because the duty cycle of the buck is very low. The same applies to the buck region.
From the previous plot in fig 4.9 it is clear that the maximum rms current is 12A. Since it is strongly suggested to use 0603 SMD Ceramic Capacitors to have less parasitic contributes as possible , a proper combination of series and parallel capacitance is designed to meet the requirements.(fig 4.10).
This combination entails :

1. Increase the total capacitance with the parallel,since 0603 smd ceramic capacitors don't have high value and an higher value of total capacitance decreases the voltage ripple
2. Decrease the total ESR resistance with the proprety of the parallel configuration: this result in an increase of the efficiency
3. Reduce the voltage across one single capacitor with the series of the same capacitance
4. Ensure safety avoiding a short circuit of the input if one of the capacitors brakes
5. Providing discharging resistor at the end of the input filter if the input is disconnected (hundreds of kohms) and also to ensure an equal voltage drop on the single capacitors

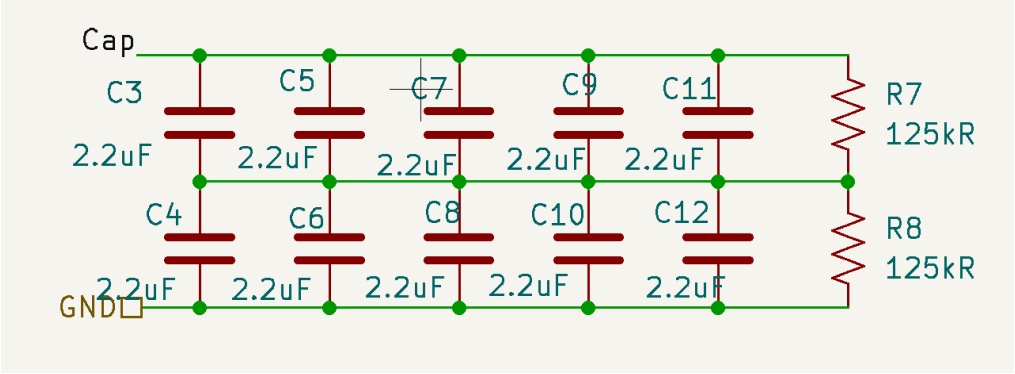


Fig 2.13:Input capacitance Filter

The chosen capacitance is the **UMK107BBJ225KA-T Ceramic SMD 0603 50V 2.2uF, 10%** since it was the best available on the market in terms of value and nominal voltage. With the series and parallel configuration the total capacitance becomes 5.5uF. In order to discharge the input capacitor when the DC input is disconnected a load resistance is added. Fig. 2.14 shows the effect of different values of the load resistance. From the simulation results it is selected a value of 125 kΩ as a trade off between the power dissipation and the discharging time.

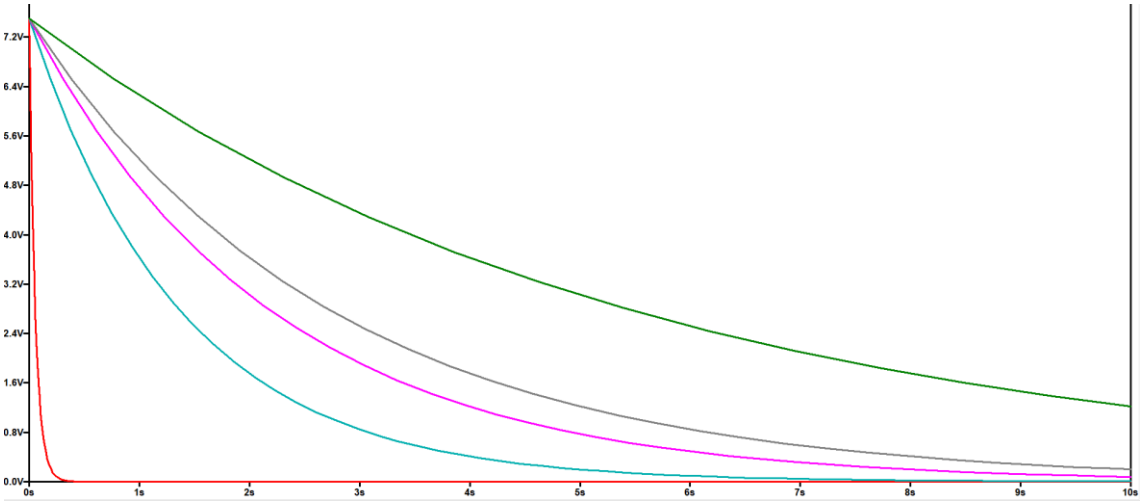


Fig 2.14 LTSPICE Simulation of input filter varying the value of the voltage divider. [Red 5kOhm] [Blue 125kOhm] [Violet 200k] [Grey 250kOhm] [Green 500kOhm]

Output Capacitor

All the previous features said for designing the input filter are valid for the output filter as well, only with few differences:

1. The nominal voltage can be lower, since the output voltage won't be higher than 15V
2. The formulae of the rms current changes
3. The output capacitance must be greater than a certain value to ensure that the ripple will be as low as possible

The output current rms (eq.26) must be calculated also for the output filter. the maximum value is expected to be reached in the boost mode, as shown in the plot (fig. 2.15)

$$I_{\text{CoutRMS}} = \begin{cases} I_{\text{out}} \sqrt{\dfrac{V_{\text{out}}}{V_{mp}} - 1} & \text{boost mode} \\ \dfrac{\Delta I_{\text{buck}}}{\sqrt{12}} = \dfrac{(V_{\text{mp}} - V_{\text{out}})D_{\text{buck}}}{f_{sw} L \sqrt{12}} & \text{buck mode} \end{cases} \tag{26}$$

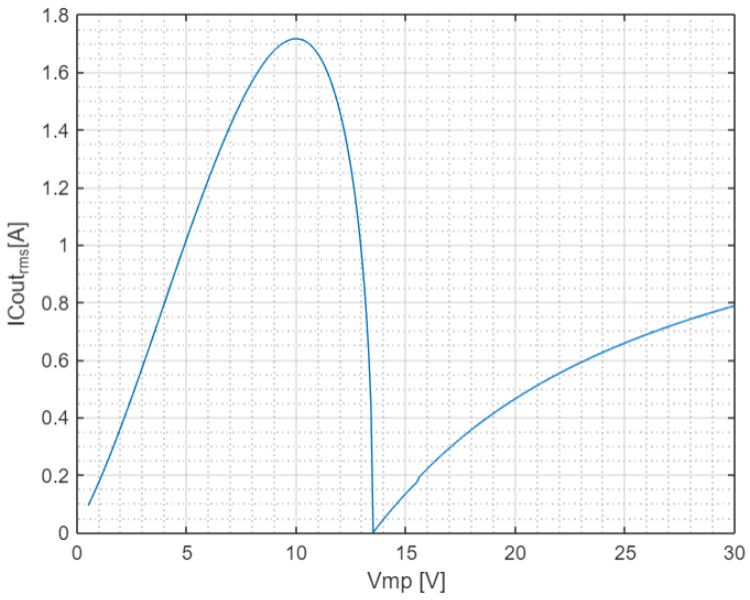


Fig 2.15 Output Capacitor RMS Current

Furthermore, to ensure a reduction in the output ripple given a certain output voltage and frequency, the following condition must be respected eq(27) [4]

$$C_O > \frac{\Delta i_L}{8\Delta v_o f_S} \tag{27}$$

Substituting the previous data in the eq.27 it is clear the total capacitance must be greater than 281nF. To ensure better results and reduction in the ripple as well, the same filter as the input is employed , which had a total capacitance of 5.5uF and enough nominal voltage for the output as well.

GaN Selection

In order to choose the transistor there are some features to take into account:

1. To be available on the market
2. To be a GaN Mosfet Device SMD
3. To be rated for Vds > 60V and Id >40A
4. To have the lowest Ron as possible to reduce dissipation
5. To have the lowest Output/Input parasitic Capacitances

A list of possible candidates is

1. EPC2003 (Half Bridge GaN)
2. EPC2065 (Single GaN)
3. EPC2206 (Single GaN)
4. GS61008T (Single GaN , GaN System)

MOSFET	Ron [mΩ]	Coss [pF]	Ciss [pF]	Qg [nC]
EPC2003	5.5	1500	3500	6.5
EPC2065	3.6	1700	4000	128
EPC2206	4	1800	2980	122
GS61008T	7	3000	6000	170

To select the best GaN SWITCH it is mandatory to consider how much these parameters impacts on the efficiency of the system.
For Each GaN it is mandatory to calculate the following losses:

- **Conduction losses(eq.28)** - Has importance in ON state are caused by the R_{on} resistance of the MOSFET. The Ron Resistance is considered when the Mosfet is switching, hence the true resistance is at least double the nominal one, due to the temperature dependence of the Ron resistance

$$P_{\text{cond}} = I_d^2 R_{on} \tag{28}$$

Where I_d is the drain current.

- **Switching losses (eq.29)** - each time the GaNs changes their state from ON to OFF or OFF/ON transition .

$$P_{sw} = \frac{V_{ds} I_d}{2} (t_r + t_f) f_{sw} \tag{29}$$

Where V_{ds} is the Drain-Sources voltage, t_r and t_f are the rise time and fall time of the GaN and were calculated using the techniques described in Vishay Power Mosfet Article , which exploits parasitic capacitances[9]

- **Gate drive losses (eq.30)** - Owing to the process of charge and discharge the gate capacitance.

$$P_{\text{gatedrive}} = Q_g V_{\text{driver}} f_{sw} \tag{30}$$

Where Q_g is the total gate charge, V_{drive} is the voltage that drives the MOSFET's gate.

- **Output capacitance losses (eq.31)** - are the losses due to the output capacitance C_{oss} ,charge and discharge processes.

$$P_{Coss} = \frac{1}{2} C_{oss} V_{ds}^2 f_{sw} \tag{31}$$

- **Dead time losses**(eq.32)- occur during the dead time. The dead time is the time during which both transistors in one leg are OFF to prevent short circuits ,but the body diode of the low side transistor will conduct and dissipate power.

$$P_{dt} = V_d I\left(t_{swon} + t_{swoff}\right) \tag{32}$$

Where V_d is the body diode forward voltage, $t_{swon} + t_{swoff}$ is the total minimum dead time, which is the time to switch OFF plus the time to switch ON the MOSFET.

- **Reverse recovery losses(eq.33)** - losses due to the MOSFETs' body diode reverse recovery.

$$P_{rr} = Q_{rr} f_{sw} V_{ds} \tag{33}$$

Where Q_{rr} is the reverse recovery charge of the body diode.

Actually, not all of these losses are present in GaN since there is not the body diode like in Silicon Mosfet, hence the Reverse Recovery charge is null, so are its losses.
Running the Matlab script it turns out that the best choice is the EPC2206 from Efficient Power Converters, taking into account also his commercial availability (more than 200.000 pieces) .
In figure 2.16 the difference between an EPC GaN and a GaN System GaN Device is shown. Basically, the losses are higher in the Gan System GS601 because the Ron is much higher .
In figure 2.17 it is shown how each losses impacts in a Silicon Mosfet suitable for this project (FDB035N10A, 80V,50A) and the EPC2206.

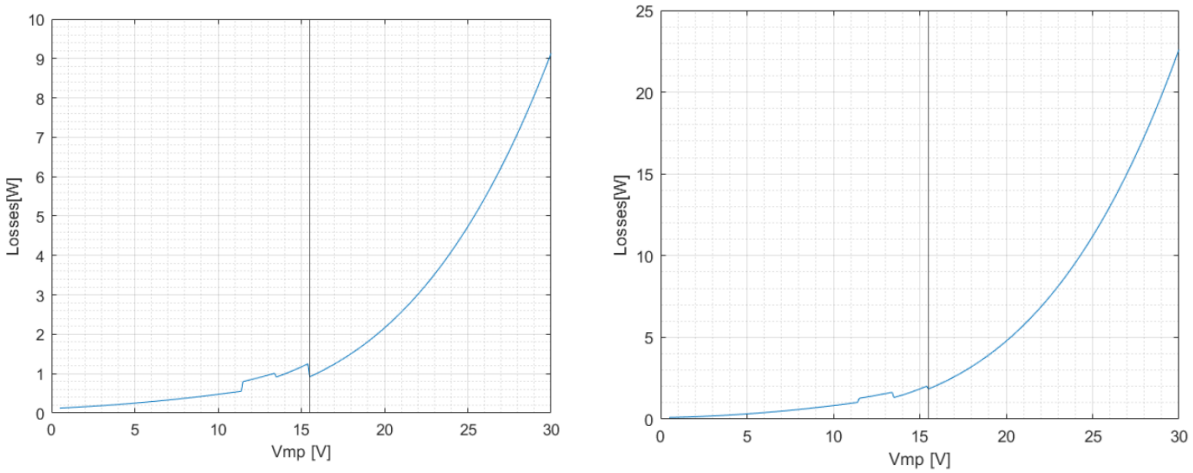


Fig 2.16 EPC GaN Mosfet (Left) vs GS61 Family Mosfet (Right)

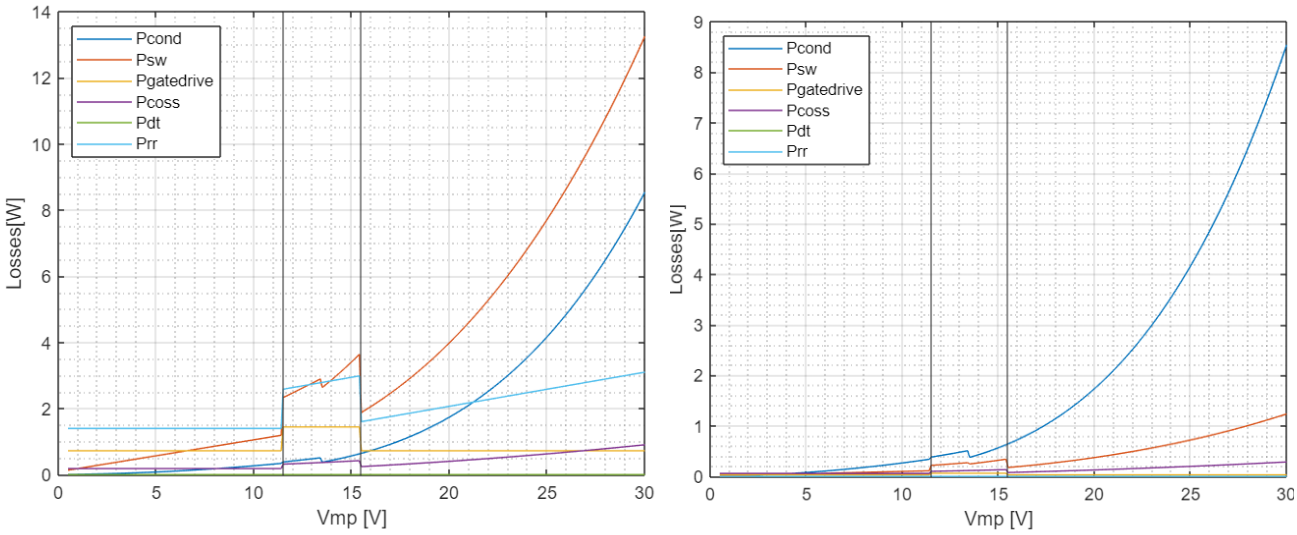


Fig 2.17 Silicon Mosfet FDB035N10A Losses vs EPC2206 Losses

From the previous chapter it was highlighted that GaN switches are way faster than Silicon Mosfet, having less falling and rising time. By taking a Silicon Power Mosfet suitable for this project, like the FDB035N10A, which has 40ns of rising/fall time with 4 Ron, the comparison with the previous chosen GaN , the EPC2206, which has 10ns of rising/fall time with almost the same Ron, can be made. The plot in fig 4.14 can indeed validate the theory:

- The conduction losses are very similar (similar Ron)
- The Reverse Recovery Losses are null in the EPC2206 since it doesn't have the body diode
- The switching Losses are lower in the EPC2206 since the rising and fall time are lower than the Silicon Mosfet
- The output capacitance losses are lower in the EPC2206 since the value of the Coss is lower as well.

Other Components

In figure 2.18 the high level design of the power stage is shown.

There are some elements that were not discussed in previous chapter .
The main power stage is split into PhaseA and PhaseB since they are symmetrical, connected by the 6.8uH inductor with a shunt resistor used in the measure stage, which will be discussed later
Several test point were placed to make the testing phase easier for the user.

In fig 2.19 it can be seen all the other components of Phase A(the same applies for Phase B, fig 2.20):

- **Red components (Measure stage)**
  - **1mohm Shunt :** Used to measure the input current trough a differential stage and low pass filter. Same applies for the 10mohm shunt used to measure the inductor current.
  - **Voltage divider** : Used to measure the input voltage trough the filter and measure stage
- **Blue components (Protection)**
  - **RC Snubber :** the space of two snubber circuits were predisposed so that if dangerous ringing are present in the switching voltage, an RC snubber must be designed in order to damp the oscillations
  - **Diodes:** the space of two fast recovery diodes is allocated to dampen the possible undervoltages due to dead time

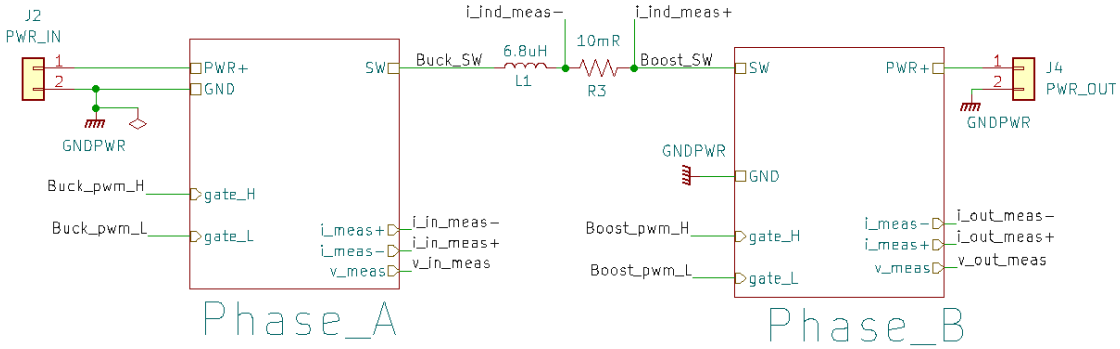


Fig 2.18 Full Power stage

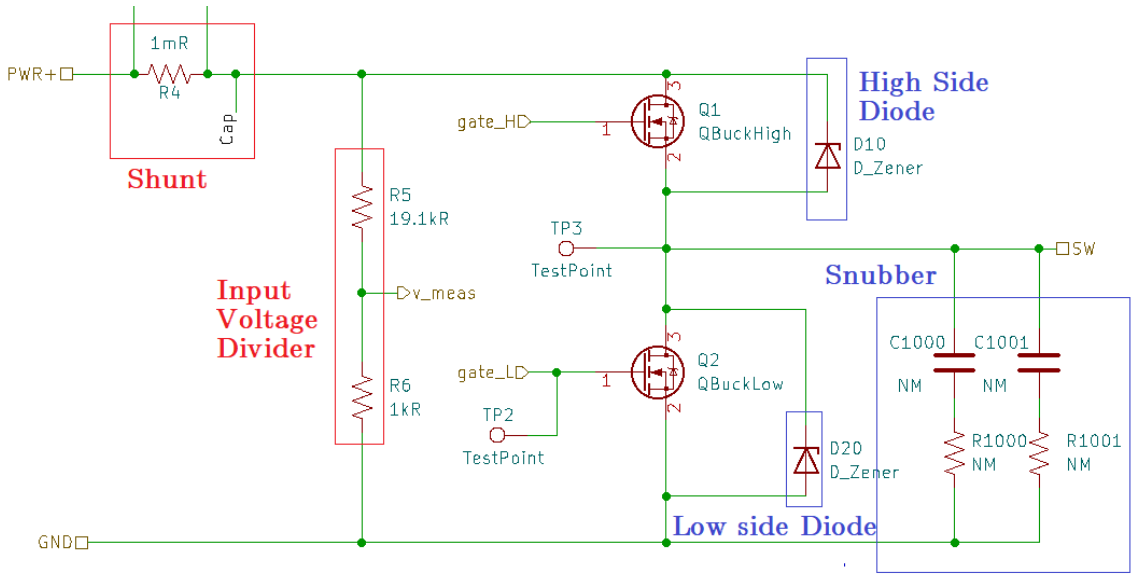


Fig 2.19 Phase A circuit, the Buck Leg of the Nibb

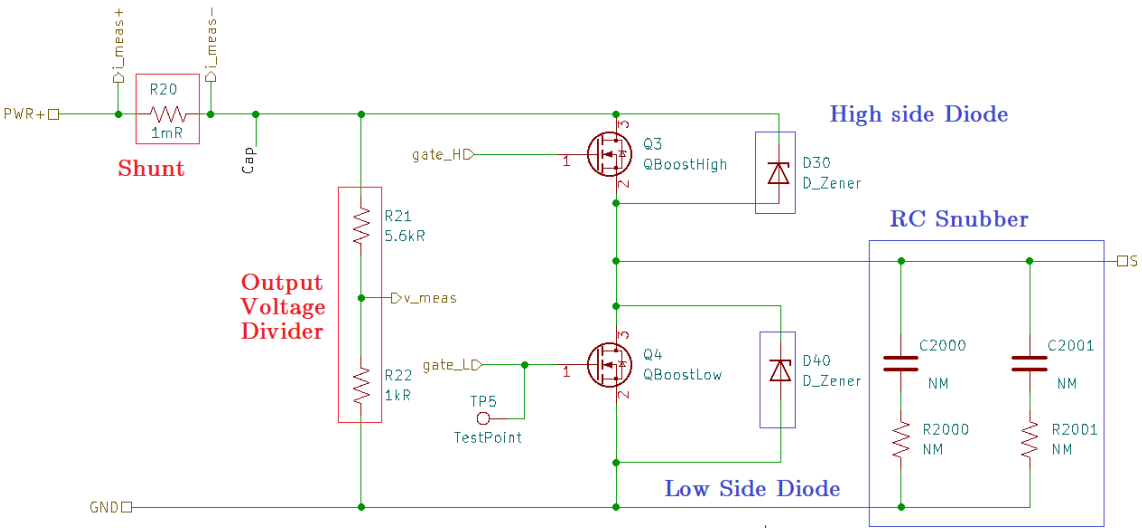


Fig 2.20 Phase B Circuit, The Boost Leg of the NIBB

Driver

The primary function of a driver is to switch a power device from the off state to the on state and vice versa. They present the following features:

1. Minimization of turn-on and turn-off times [5]
2. They provide suitable drive power to keep power switch in on-state where the conduction losses are low[5]
3. They are the interface between the control circuits and the power switch
4. Provide amplification of control signals to levels required to drive power switch using an integrated level shifter. [5]

GaN devices of the latest generation are able to increase the switching frequency of power circuits, hence the power density over unit. Nevertheless, higher switching frequencies need drivers to support higher dv/dt in order to keep the gate oscillations and ringing to minimum. Hence, not all the drivers which are suitable for Silicon devices can be adapted for GaN devices.
In order to choose a driver suitable for this project, it is needed:

1. Short propagation Delay(less than 50ns)
2. Stable and high dv/dt
3. Short rise and fall Time optimized for GaN Devices (less than 10ns)
4. To be in Half Bridge Configuration Driver (this will simplify the layout)
5. To be available on the market

A suitable driver which satisfy all the previous characteristics is the NCP51820AMNTVWG of the OnSemi.
In fig 2.21 the Half Bridge driver for the Buck Leg is shown

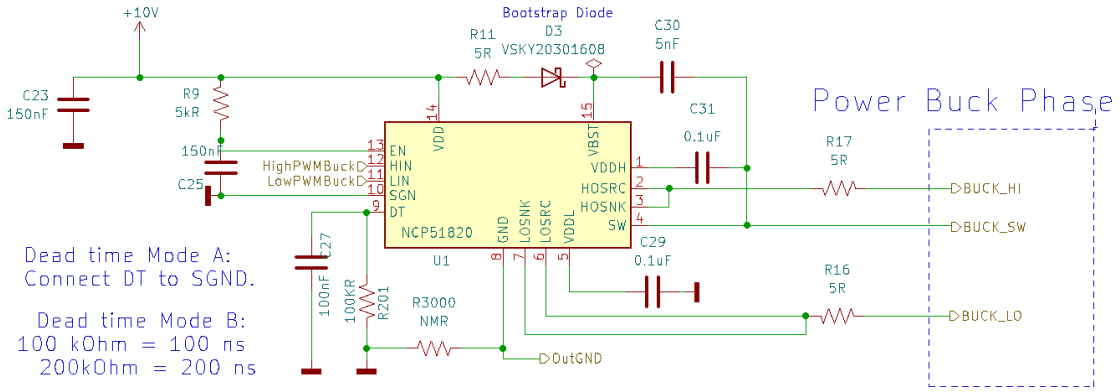


Fig 2.21 Half Bridge Driver GaN used for Buck Leg

The components were designed according to the driver's datasheet [9] In particular, the bootstrap diode needs to have

- Voltage rating greater than Vin
- High speed(Low reverse recovery)
- Low current
- Low junction Capacitance (for dv/dt issues)

The bootstrap series resistor is then used to limit the current[9] For what regards the dead time, there are mostly two operative modes:

- Mode A: Leave the Pin9 (DT) to GND. The dead time can be programmed by the user via software or if the two signals are overlapping with X time, then X will automatically become the dead time
- Mode B: Put a resistor of 100-200kOhm and a bypass capacitor to GND. As suggested in fig. 4.18, a programmable dead time can be generated with the corresponding value of the resistor.

In addition several bypass capacitors were placed and two gate resistor of 5Ω were placed in order to damp the gate ringing oscillation.

2.2 Current Measurement Stage

In this section will present how the current measure stage was designed.
It is a very crucial step in the NIBB design due to the high precision required : even few millivolts can have a non-negligible impact on the measurement.
An high level design scheme is shown for current measure stage, shown in fig 2.22

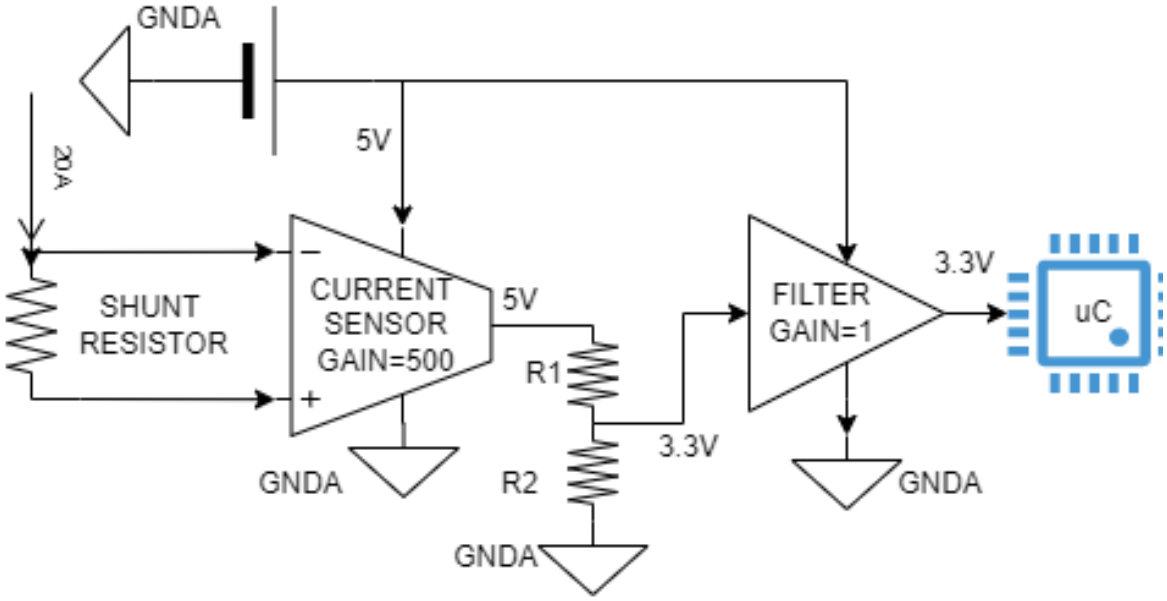


Fig 2.22 High level design of Current measure stage

Let's analyze each element of the current stage to understand how it works in detail

- The current flows through the shunt resistor: its aim is to convert an high current into a voltage readeable by current sensors. Hence is a particular resistor designed specifically to substain higher currents with very low resistance value(1-100 mohms). Such value allows a small drop voltage (in the order of millivolts) and it requires a current sensor with high gain to be read. A suitable shunt must be able to substain also the required Power, which in our case is less than 10W for every stage.

- The small drop voltage is amplified by the current sensor, which in our case is a differential amplifier.
- The Output of the INA goes trough a divider and then it is filtered with a low pass filter in order to cancel the effect of the ripple, which is around the switching frequency.

The current measure stages are used to measure the Inductor current and both the input and output currents.

Input and Output Current Stage Design

In order to choose the differential opamp current sensor there are some features to take into account:

1. The sensor must have an excellent CCMR (more than 100db at DC)
2. High Bandwith (especially for the inductor current since it is measured at the switching frequency)
3. Suitable GAIN for the project(20,50,100,200,500)
4. Lowest Slew rate possible
5. To be a SOT-23 packaging and available on the market

Two sensors which satisfies all the above condition is the INA293A5/INA293A3 with gain respecitvlely 500 and 100

To design the shunt resistor and choose the suitable Gain it is necessary to use the equation 34

$$I_{max} * R_{shunt} * GAIN < V_{sp} \quad (34)$$

Where

- I-max is the maximum current that can flow in the shunt resistance
- R-shunt is the numerical value of the shunt resistor
- Gain is a coefficient found in the datasheet of the INA opamp
- Vs is the voltage used to supply the ina(20V maximum)

For instance, with INA293A3 Gain=100 and Rshunt=1mohm and Vsp=5V a maximum current of 10A

will be readeable. With LTSPICEXVII the INA293A4 has been imported.

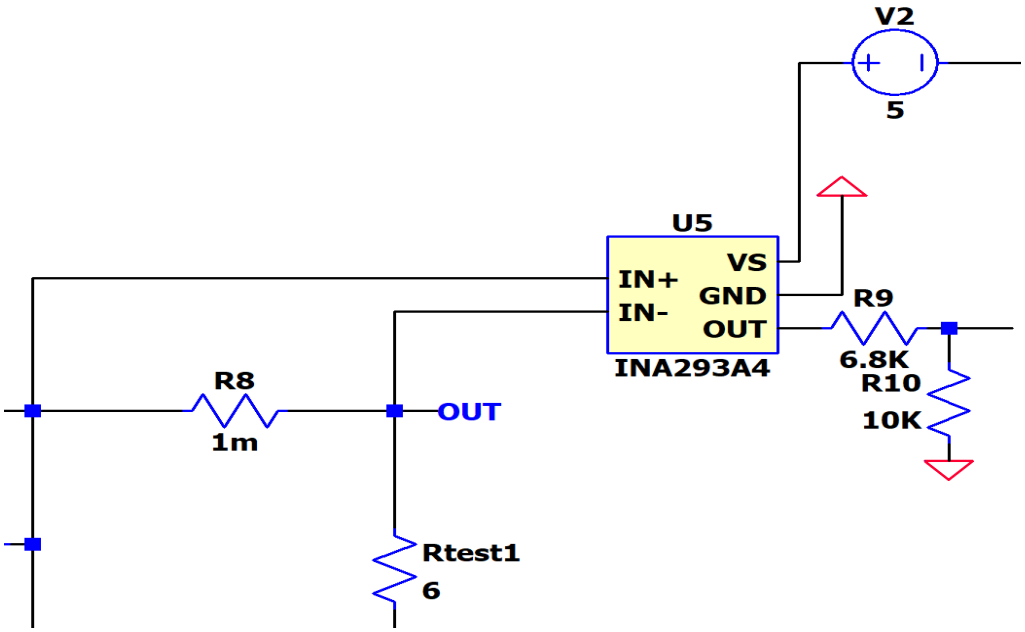


Fig 2.23 LTSpice Test of INA293A4 Out Current of Nibb

From the simulation results in Fig 4.24 it can be seen that the RMS current is about 2.5A with a ripple of 200mA.
From the FFT Simulation in Fig 2.25 it can be seen all the spectrum components: at 0Hz there is the DC component, while at the switching frequency the ripple component .
The ripple noise need to be filtered out in order to have a more reliable measurement to be given at the controller

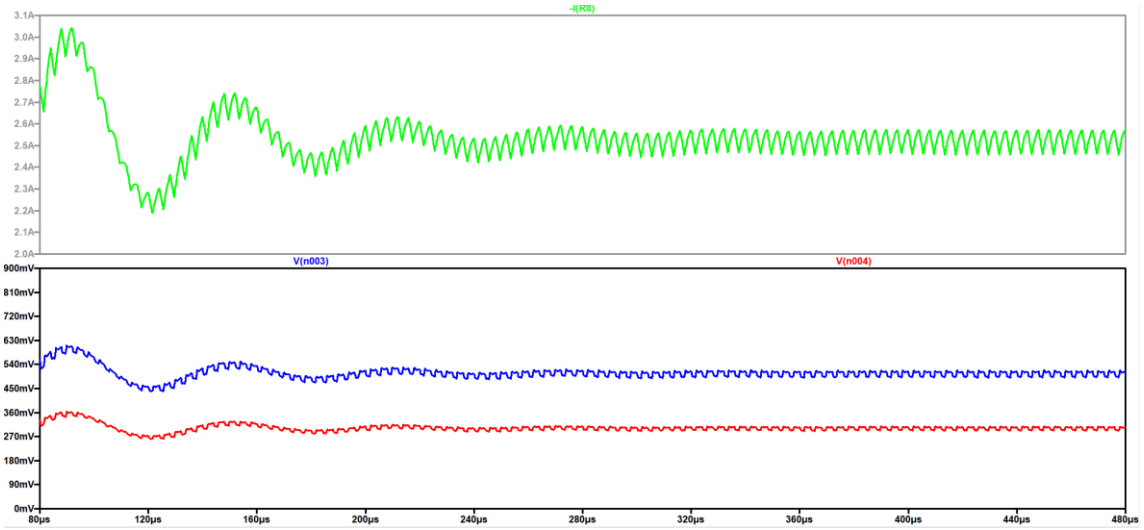


Fig 2.24 Simulation Results. In green the load current, in blu the output of the INA sensor, while in red the output of the divider

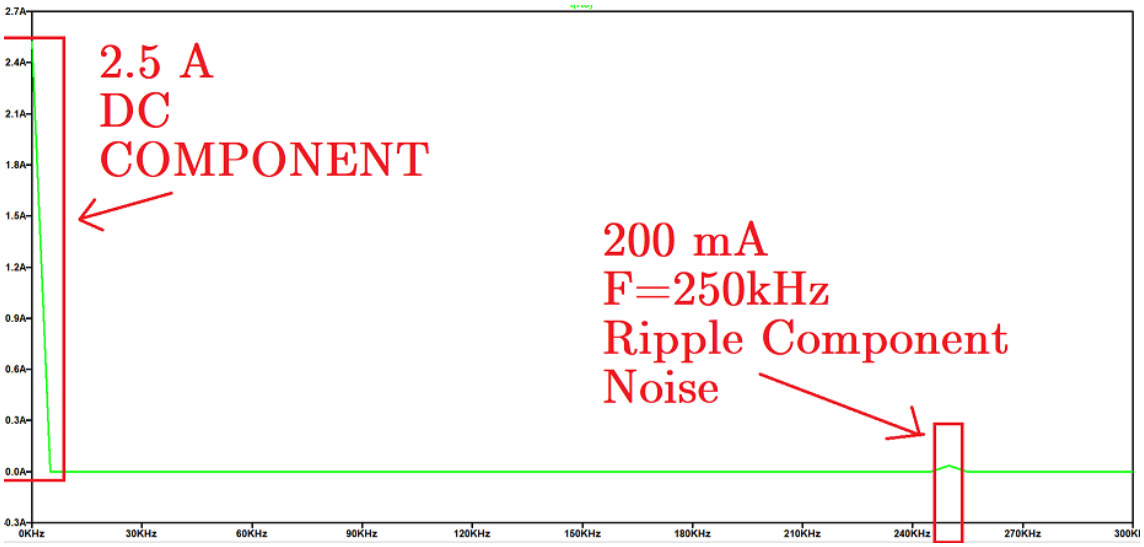


Fig 2.25 FTT of 2.5A load current and the ripple component at the switching frequency

From the previous simulation and in the fig 4.22 it is certain the Ripple component must be filtered which is found at the switching frequency.
A fourth order Bessel Filter with Sallen Key cells is the best suitable topology for the project since it gives smaller phase lag which is crucial to avoid delays and instability in control systems.
The cutting frequency is set at 5kHz , to guarantee an attenuation of at least 100 dB in the possible switching frequencies.

Filter cells are made with opamps and the selection of the suitable topology for this project should be done with care. It must have:

1. High CCMR
2. High Bandwith (More than 10 MHz)
3. Rail-To-Rail topology
4. Low input Voltage Offset and Currents(100uV)
5. SOT23 Packaging and to be available on the market

A suitable opamp which satisfies the previous point is the LM7715-MF-NOBP Texas Instrument.
Now that all the components are designed the complete filter in KiCad can be assembled and test its functionality on LTSPICE using the noisy output current in fig 2.24 of the circuit in fig 2.23

All the passive components used are SMD 0603(1603 Metric).
The LMP7115MF-NOBP Symbol was created manually since it was not present on the standard library component.
The ground used for these connection is the Analog Ground GNDA, which is the ground used for all the measurements signals.
Bypass Capacitors SMD 0603 of 0.1uF were placed in the power supplies to filter the noise of the power supply

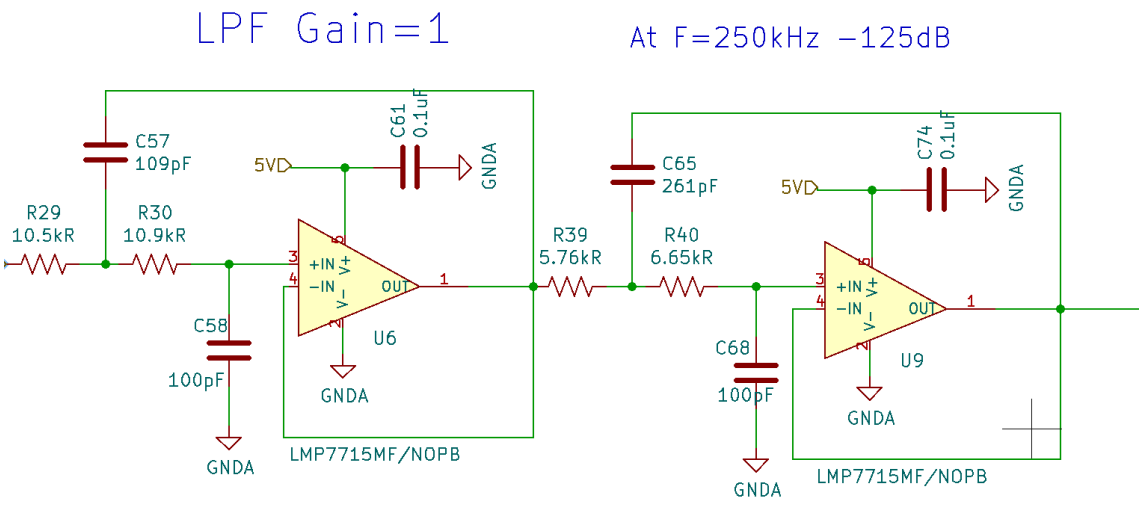


Fig 2.26 KiCad Low Pass Filter

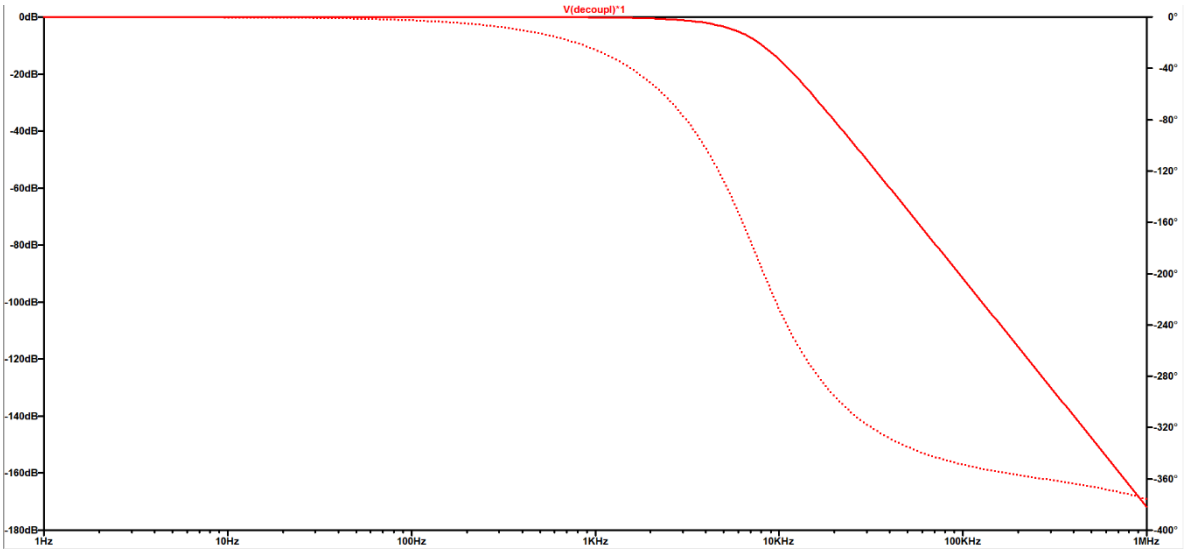


Fig 2.27 Phase and Magnitude of the Bessel Filter

Let's test the filter in LTSPICE

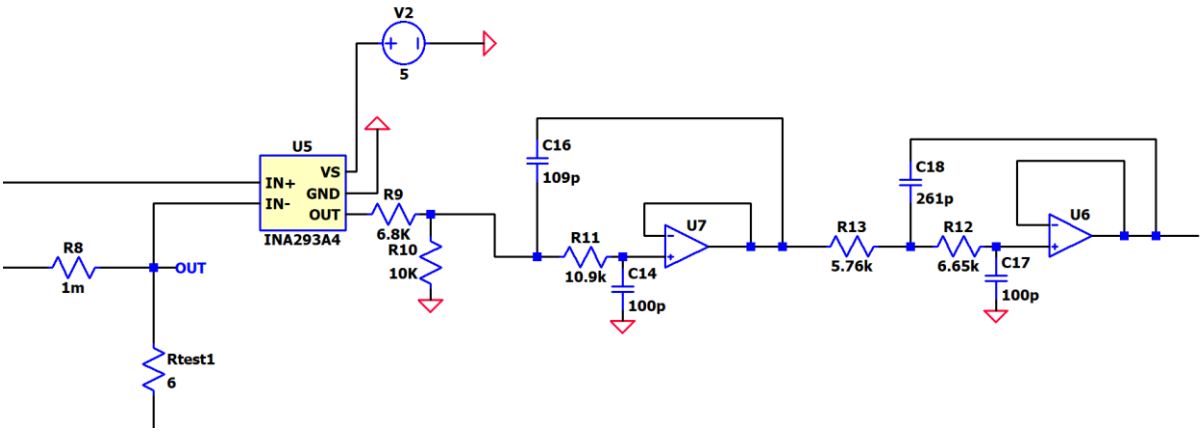


Fig 2.28 LTSpice Ina measure stage followed by the filter

As it can be seen from the simulation results in Fig 4.26, the filtered red signal is almost clear from the noise caused by the switching frequency's converter. In fig 4.27 it can be seen better the phase lag introduced by the filter stage.

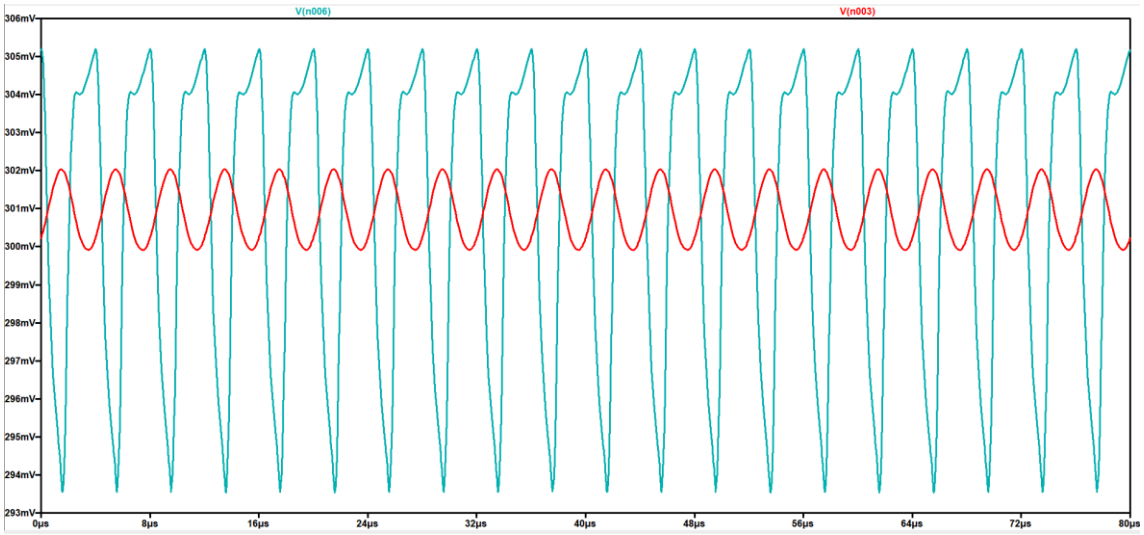


Fig 2.29 LTSpice Simulation results of circuit in Fig 2.28 with the same noisy current of Circuit Fig 2.23 Plotted in Fig 2.24. The Phase shift and attenuation of the filter can be seen from Fig 2.27 which eliminates the switching component plotted in the FFT in Fig 2.25

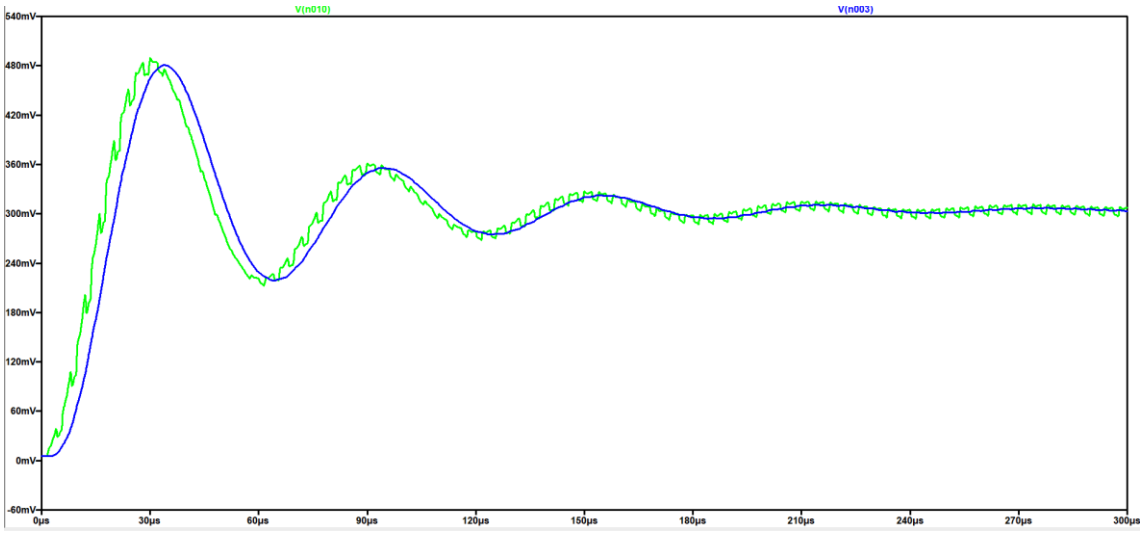


Fig 2.30 LTSpice Simulation results of circuit in Fig 2.28 This plot enhances the phase lag introduced by the filter stage

Inductor Current Stage Design

The shunt and current sensor were designed with the same equation used before (eq .38) . The only feature that is required from the shunt in addition is to be a non-inductive shunt, which will improve the relaiability of the measurement.

To verify this, let's simulate it on LTSpice using the a Non Inverting Buck Boost Converter with L=6.8uH and Vin=10V,Vout=15V. In fig 2.31 it is reported only the section of the circuit in our interest, with a 1mohm shunt and a parasitic inductance of 8nH, while in Fig 2.32 are showed the simulation results.

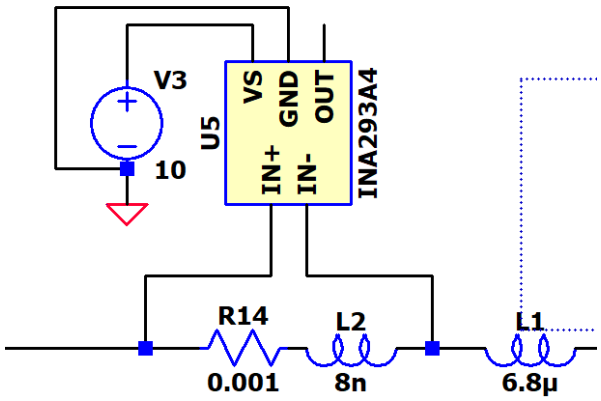


Fig 2.31 Test of 1mohm with 8nH parasitic Inductance

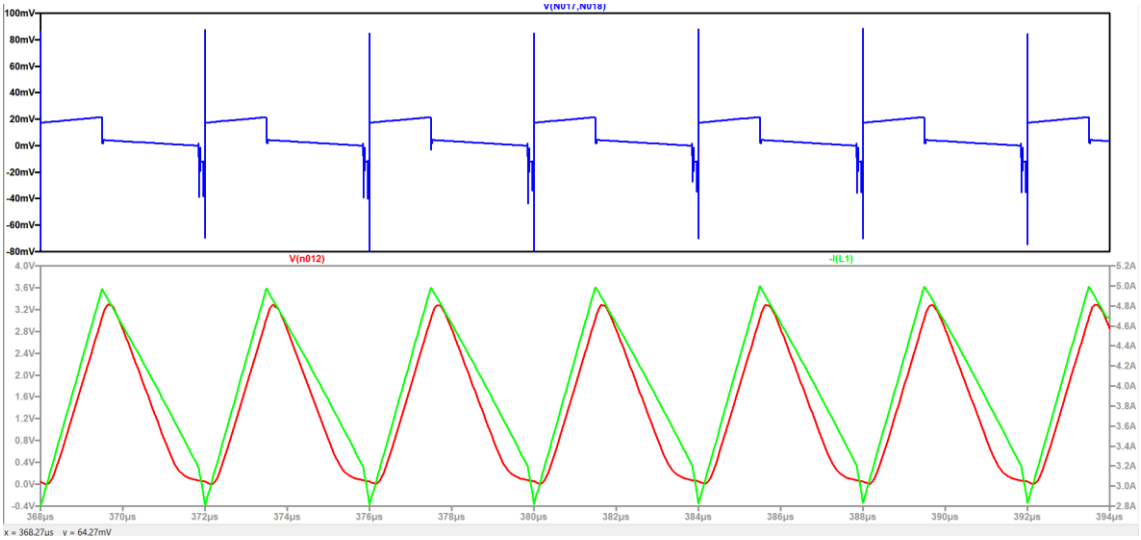


Fig 2.33 Simulation Results of 4.28. In blue, the differential voltage across the shunt and inductor, in green the inductor current and in red the output of the INA293A3

As it can be seen from the plot results in Fig 2.33, owing to the parasitic inductance the differential voltage across the shunt+inductor presents dangerous overvoltage (spikes) and a distorted waveform, and the output of the INA presents some distortions as well. In order to solve this problem it is necessary to:

1. Select a non-inductive shunt,as stated before
2. Increase the value of the shunt to minimize the inductive effect (this will result in a rise of the temperature as well so not to much high, at least 7W shunt is needed)
3. Design an RC Filter at the input of the INA stage to compensate the zero introduced by the parasitic inductor

To prove this, let's test it on LTSpice (fig 2.34). The results are shown in Fig. 2.35 and Fig 2.36

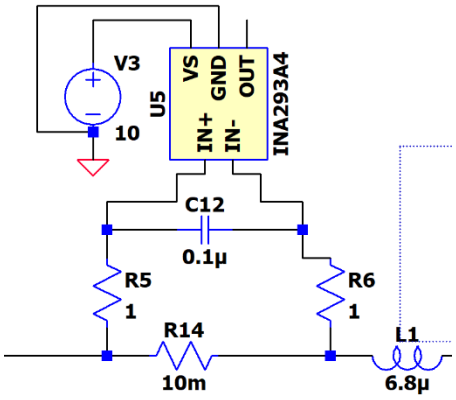


Fig 2.34 LTSPice 10 mohm and RC Filter Test

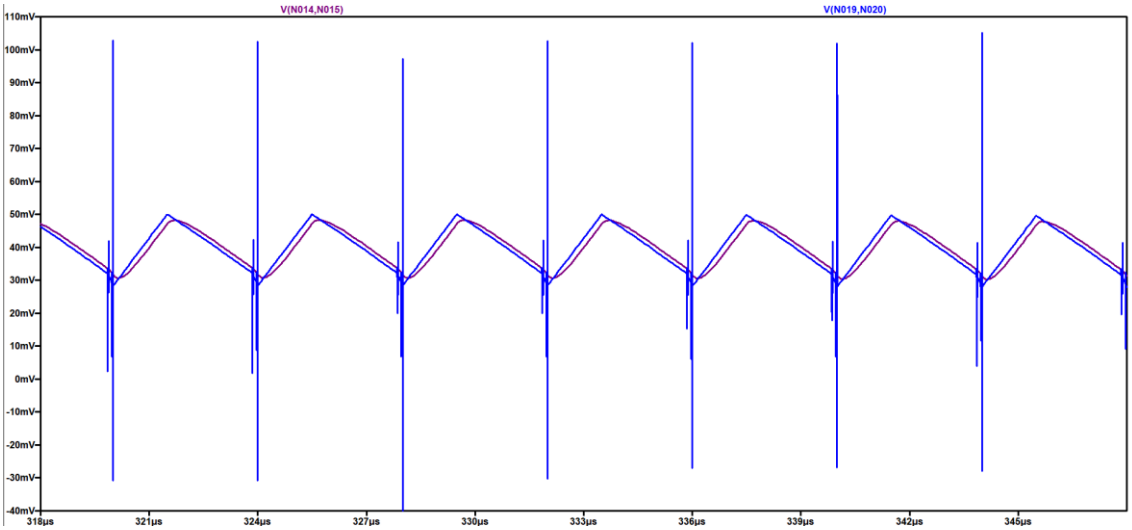


Fig 2.35 Simulation Results of Circuit in fig 4.30. In blue the differential voltage across the 10mohm shunt, in violet the input of the INA293, filtered by the RC stage

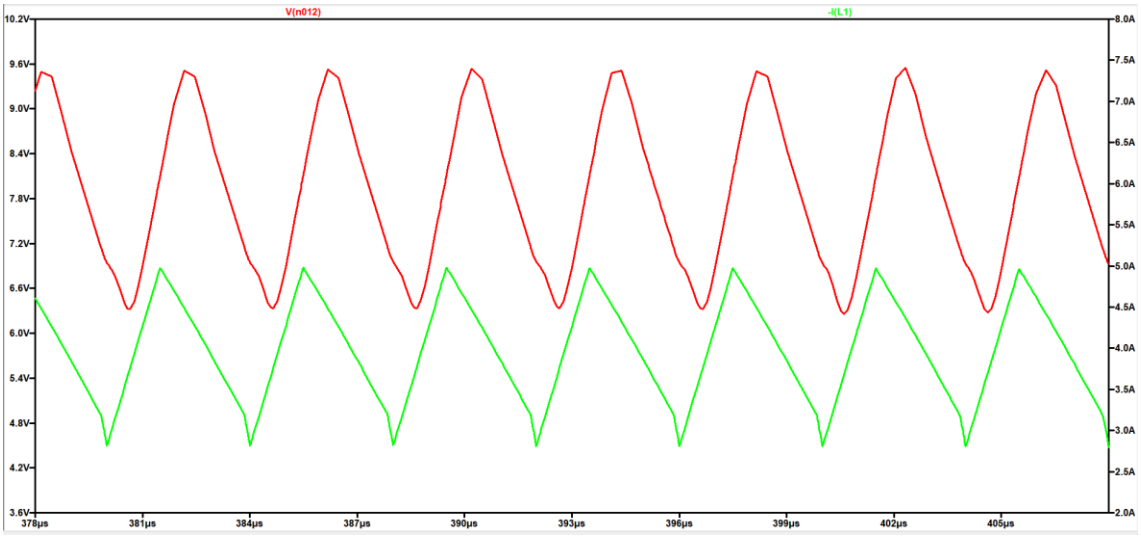


Fig 2.36 Simulation Results of Circuit in fig 2.34. In Red the output of the INA293A3, in green the inductor current

From the simulation results in Fig 4.31 it can be seen that the RC filter was well designed and the spikes as well as other unwanted distortion are cancelled. This entails a more reliable waveform to be fed into the INA. The output of the INA is shown in fig 2.36
Let's run an FFT simulation of the previous inductor current waveform (fig.2.37)

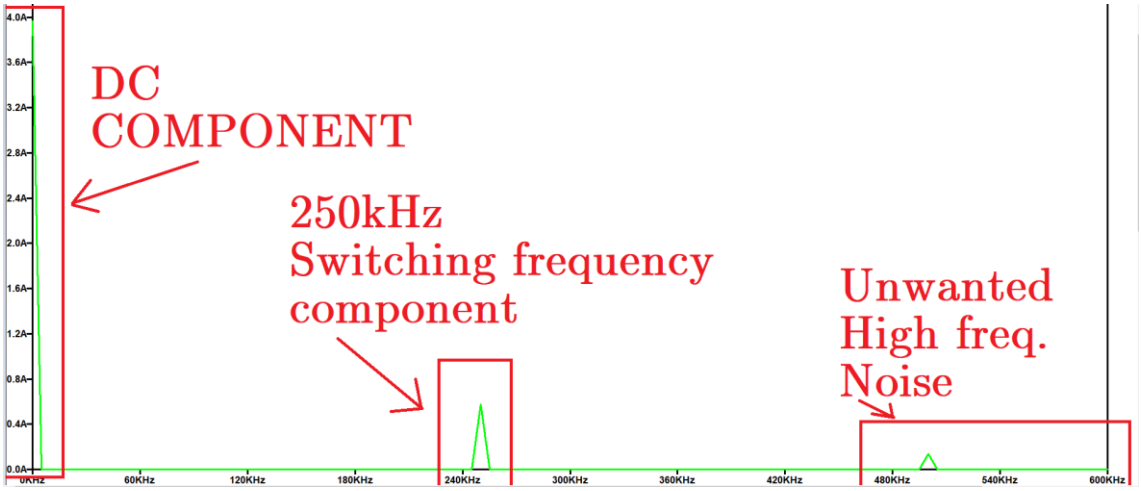


Fig 2.37 LTSpice FFT of inductor current

As it can be seen from Fig 2.37 it is necessary to design a filter that is able to keep null phase lag and no attenuation until the switching frequency, but at the same time to cancel the high frequency noise, namely to have at least -50 , -100 db of attenuation at high frequencies. For this reason, a sixt order Bessel Filter with cutoff frequency of 1.5 MHz was set.

A voltage divider was designed as well to scale the maximum output of the INA to 3.3V to be fed at the uC. Hence, the full stage is designed and simulated as well, shown in fig 2.38

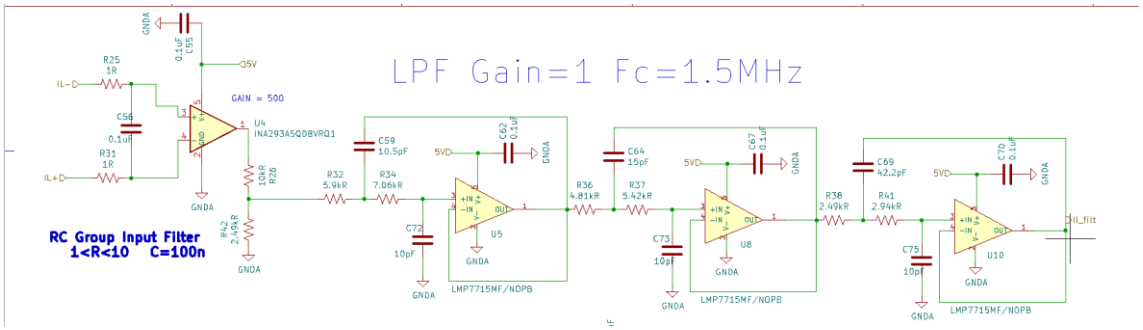


Fig 2.38 Full Inductor Measure stage with RC-Filter,INA,Divider and third order Bessel filter

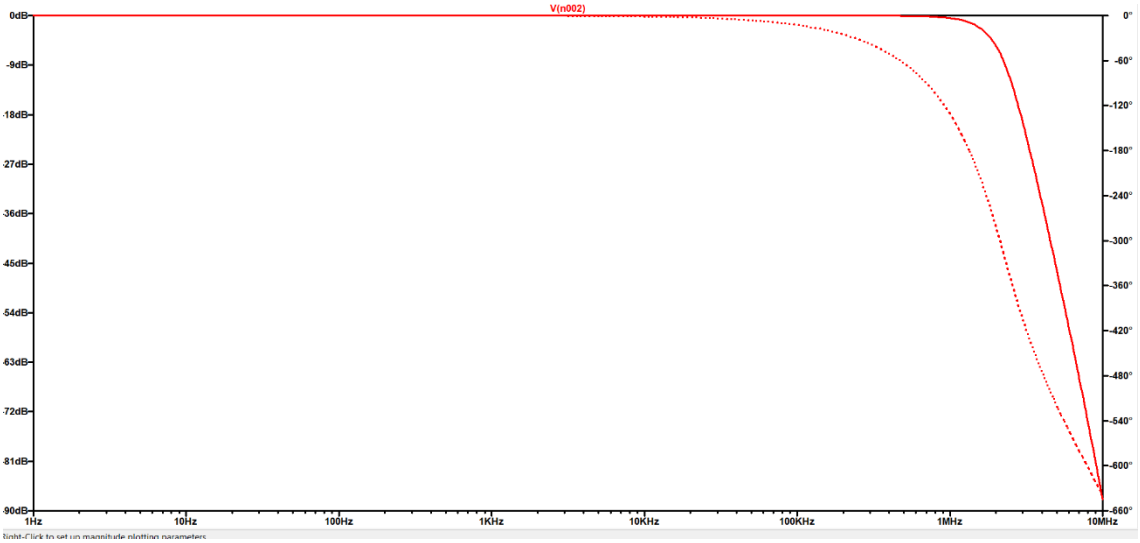


Fig 2.39 Third Order Bessel Filter Bode Diagram

Now let's test the full measure inductor stage on LTSpice, using the 10mohm shunt, RC Filter, INA293A3, Voltage divider and third order filter. This simulation is useful to confirm that there's negligible attenuation in the switching frequency as well as small phase lag. The circuit used is shown in Fig 2.40, while the simulation results in Fig 2.41

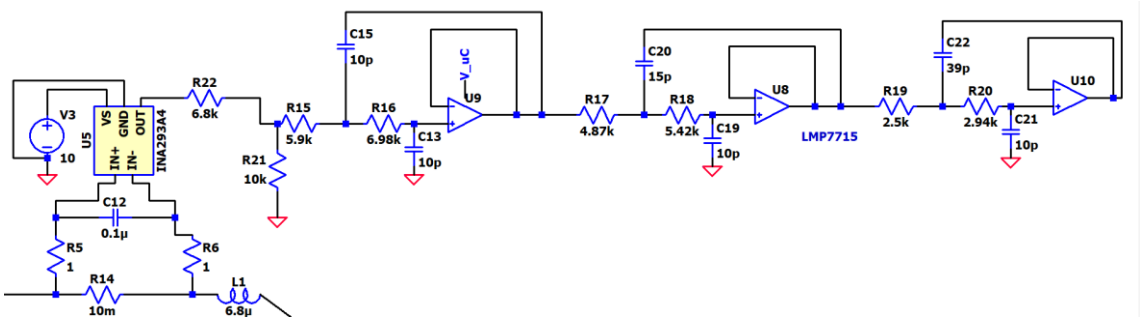


Fig 2.40 LTSpice Circuit of Full Inductor Stage

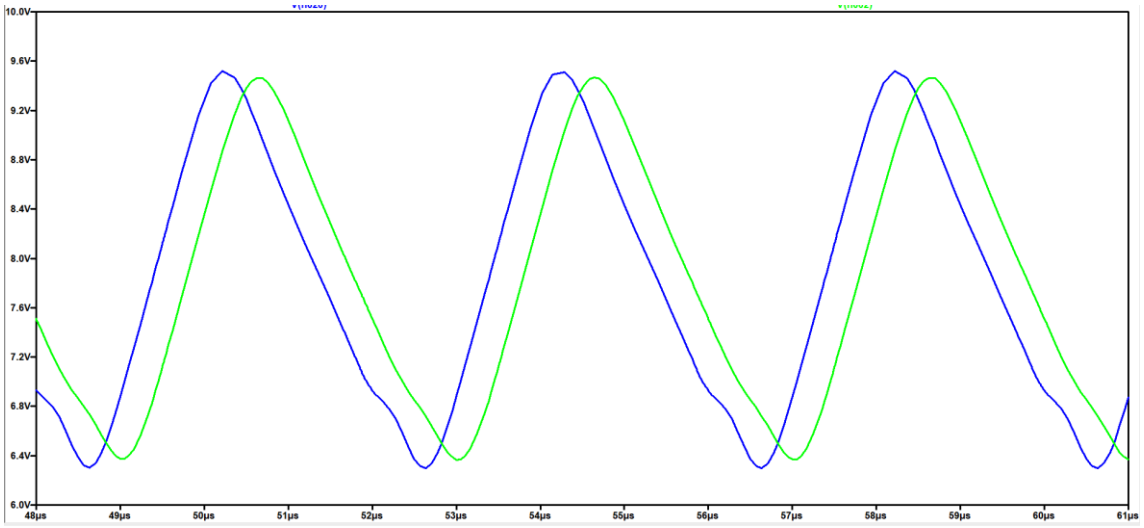


Fig 2.41 LTSpice Simulation Results of circuit in fig 4.36. In blue, the waveform before the filter and in green the waveform after the filter.

As it can be seen from the simulation results in Fig 2.41 , the waveform distortion are minimized, there is a negligible attenuation in the ripple of in the inductor waveform and the phase lag is small. Naturally in real measurement the high frequency noises are way higher than simulated, so the third order filter is still necessary. The filter as well as the measure inductor stage was well designed.

2.3 Voltage Measurement Stage

In order to acquire correctly the Input and the output voltages it is necessary to design a filter and a divider. The stage then is very similar to the current, with only two differences:

1) There's no need of the current sensor. The input divider will scale the input or output voltage from the maximum voltage readeable into 3.3V (30V for the input and 15V for the output)
2) The divider has GNDPWR as ground reference. The divider is placed near the analog section in order to minimize the loop between Analog Ground and GroundPower

The choice of the OPAMP (LM7715MF-NOBP) is explained in Chapter 2.2 and it is suitable even for the voltage measure stage

An high level design scheme is shown for voltage measure stage, shown in fig 2.42

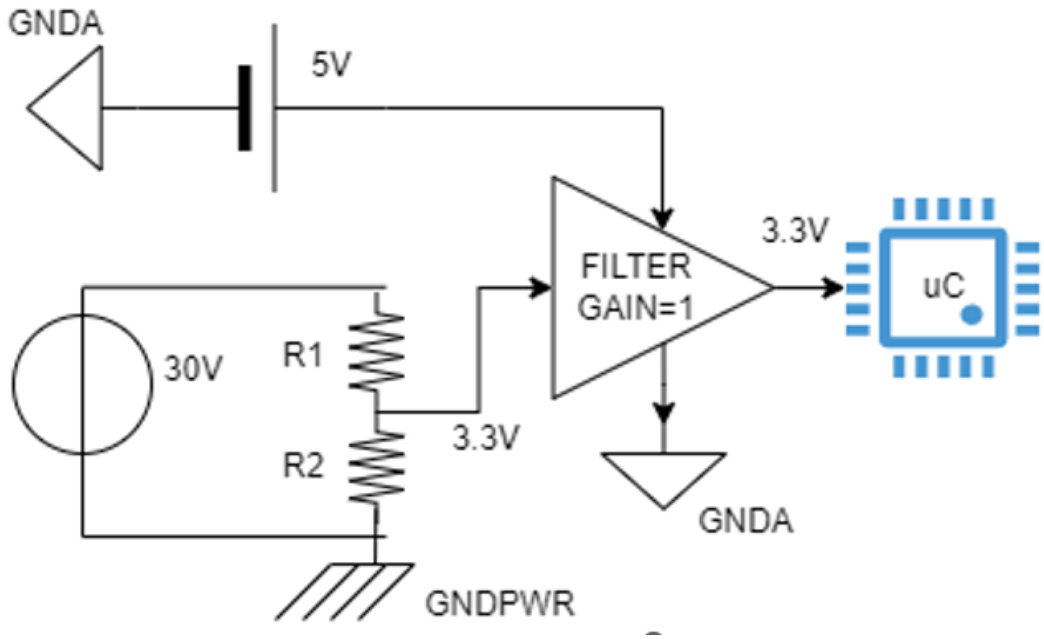


Fig 2.42 High Level Design of Voltage Measure Stage

Thanks to the FFT simulation in Fig 2.24 it was confirmed that DC currents and voltages have noise at the switching frequency, hence the choice of the filter is the same as before(Bessel, Fourth Order with Sallen Key Cells).
This time the voltage divider has to be designed differently for the input and the output stage.

For the Input Stage there is $Vmp_{max} = 60V$ when the TEG is OC condition. When there is the maximum voltage 3V it has to be fed to the uC, hence a suitable divider is given by R2=1kΩ and R1=19.1kΩ

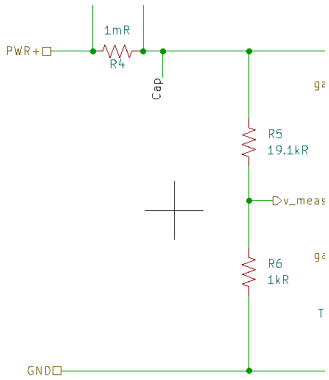


Fig 2.43 Input Divider

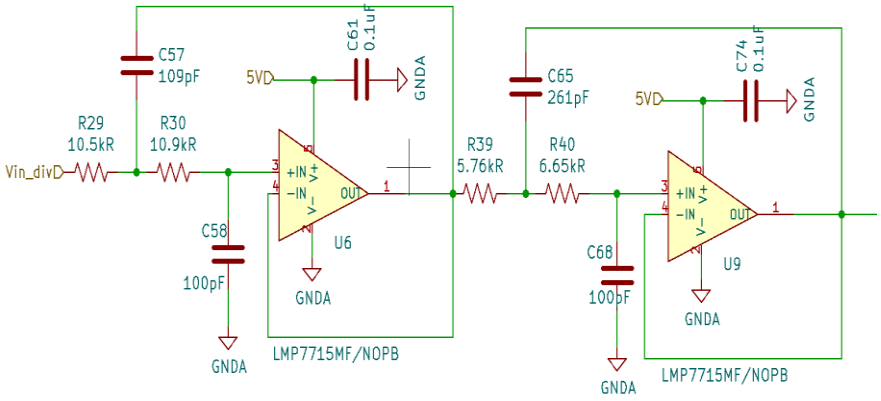


Fig 2.44 Input Filter Stage

For the Output Stage there is $Vout_{rms} = 15V$ in addition to some ripple that changes with the input voltage. The maximum voltage threshold is set to 20V to be sure. Hence a suitable divider is given by R2=1kΩ and R1=5.6kΩ. The divider is shown in fig 2.45 and filter stage in fig 2.46

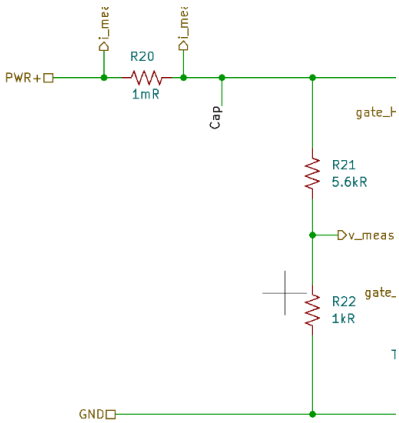


Fig 2.45 Output Divider

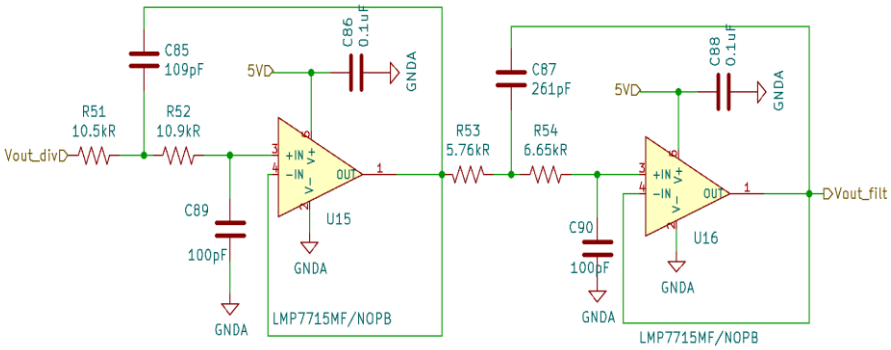


Fig2.46 Output Filter Stage

2.4 Efficiency Estimation

Finally the efficiency can be estimated taking all the other component's losses into account starting from equation (30), by adding the following losses:

- **Inductor losses** - the main inductor losses are the conduction losses due to the parasitic series resistance ESR (Eq 35)

$$P_L = I_{LRMS}^2 ESR_L \tag{35}$$

- **Capacitor losses** - the main capacitor losses are the conduction losses due to the parasitic series resistance ESR, very low in ceramic capacitor, almost neglettable (0.4 mohm at 150kHz) eq.36

$$P_C = I_{CRMS}^2 ESR_C \tag{36}$$

- **Shunt resistor losses** - Used in the measure stage, regards the conduction losses of the shunt resistors eq.37

$$P_{\text{shunt}} = I^2 R_{\text{shunt}} \tag{37}$$

A graph with all the main losses is shown in figure 4.16 . Once the losses have been calculated the standard formula can be used for the efficiency, with his plot in figure 2.47

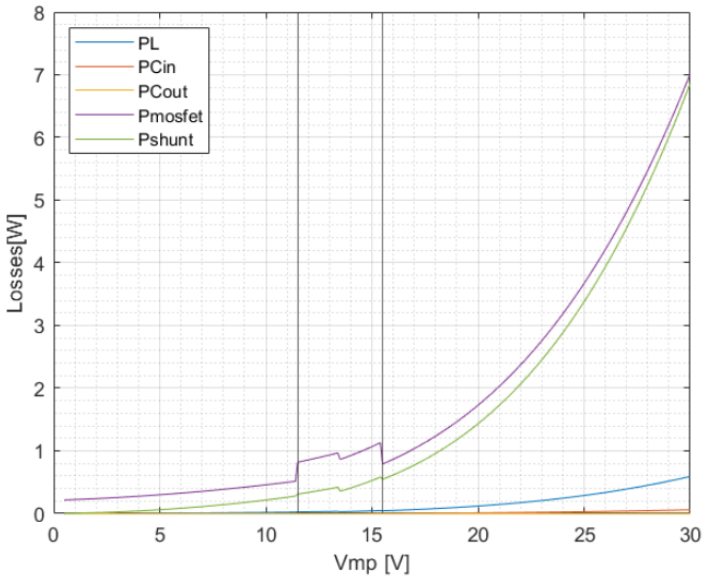


Fig 2.47 Main Losses in the Nibb

Hence the total efficiency is estimated using the equation 38.

$$\eta = \frac{P_{\text{in}} - P_{\text{loss}}}{P_{\text{in}}} \quad (38)$$

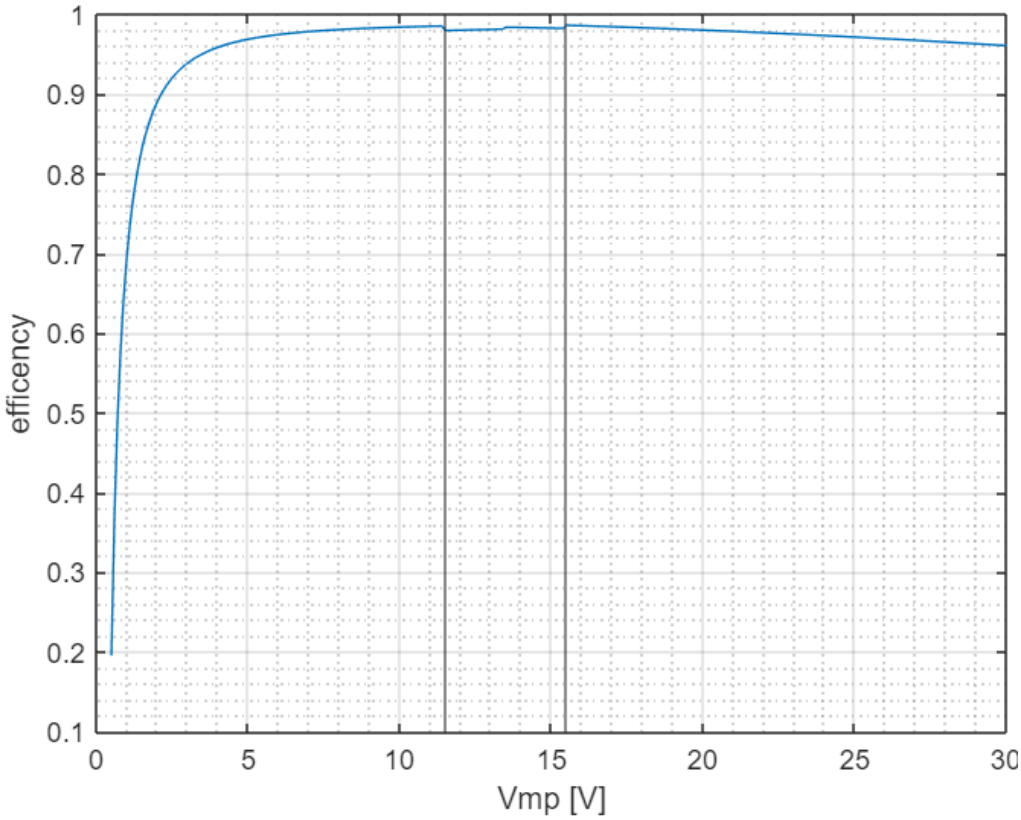


Fig 2.48 : Efficiency of the Nibb vs Input Voltage at 400kHz

Chapter 3
Logic Board Design

This section comprehends the microcontroller circuits itself, the fault detection circuitry, the power supplies, the JTAG and the Analog Circuitry as well as the Cristal Oscillator required by the microcontroller.
The microcontroller used is TMS320F28379DPTP from Texas Instrument. Since it has 180 pins, it has been divided into subunits in KiCad

3.1 Analog Section

The microcontroller needs two supplies: 1.2V and 3.3V. They must be very precise with very low ripple(less than 10mV). Each pin has a bypass capacitor suggested by the datasheet, all shown in fig 4.42

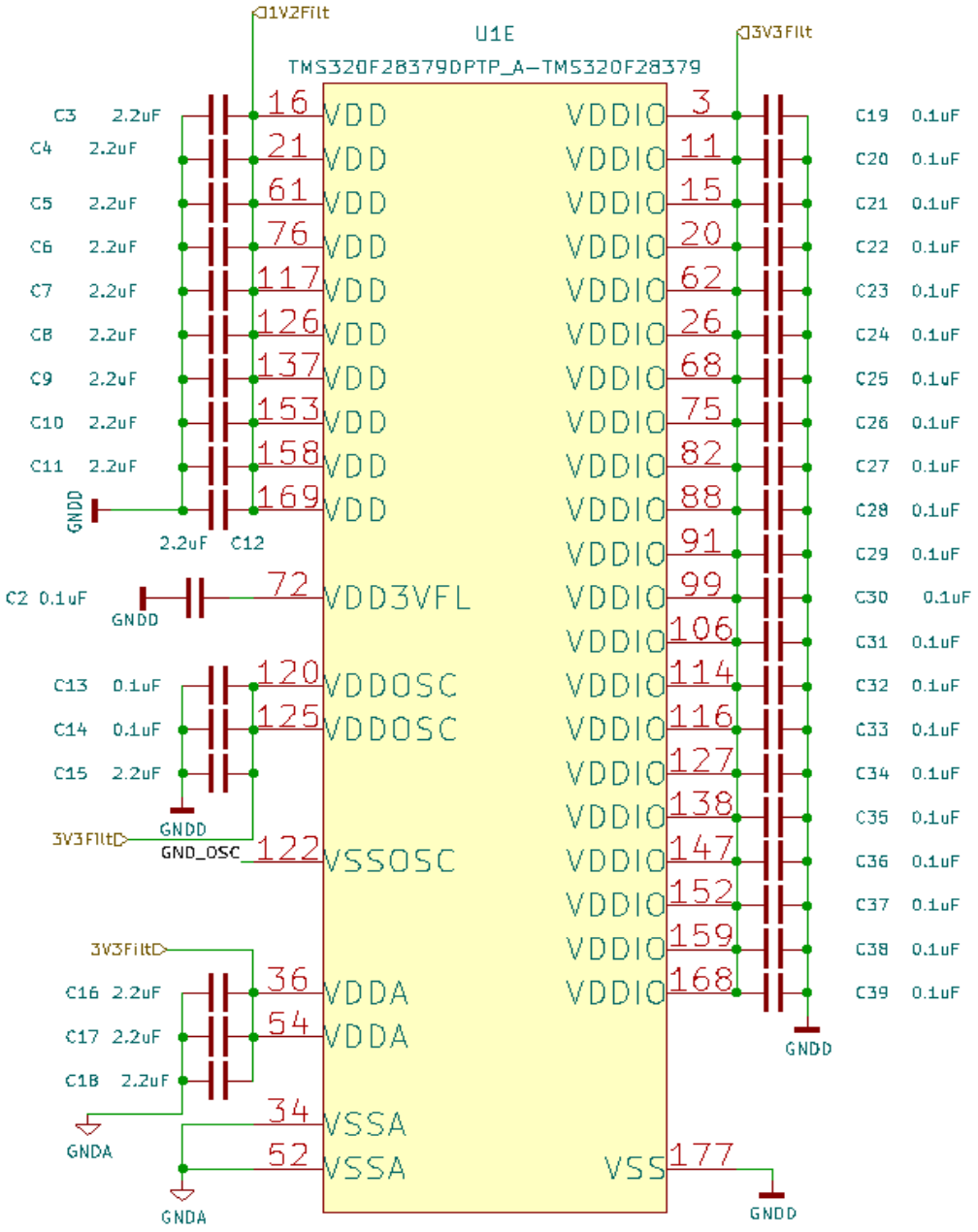
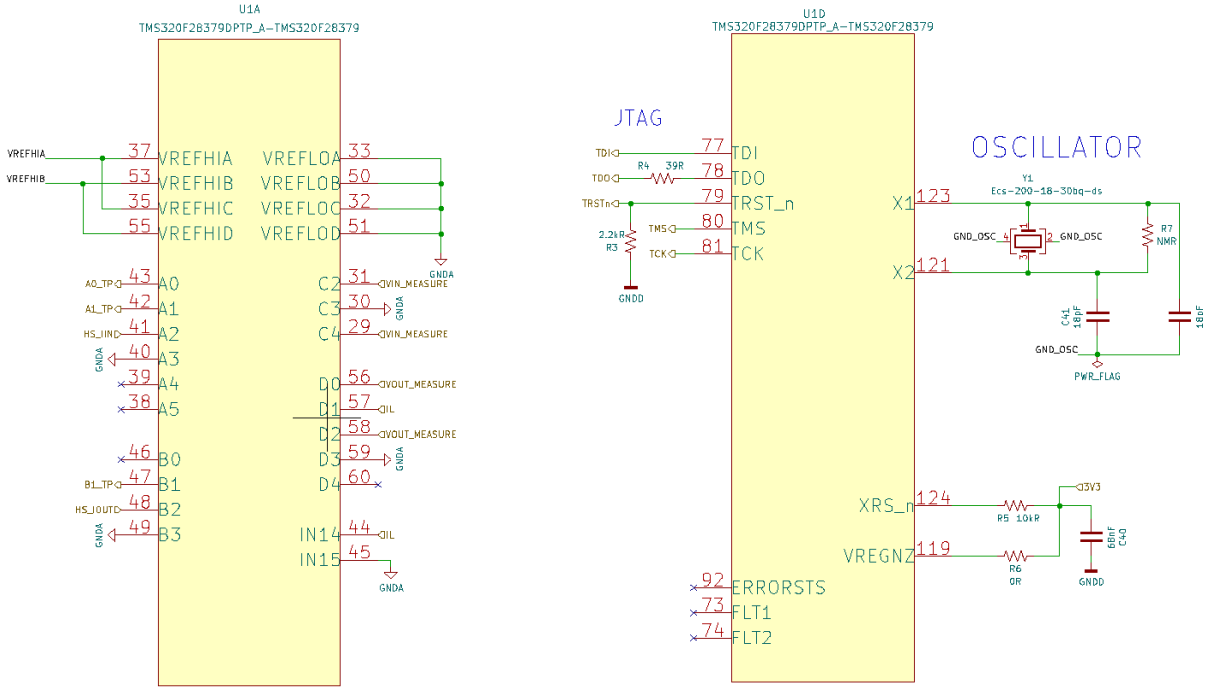


Fig 3.1 Supplies connections of Micocontroller

More than one ground is used: analog ground referred as GNDA, digital ground GNDD and Crystal Oscillator ground GNDOSC. This ensures protection against the digital ground which has noise coming from the microcontroller. This is possible by having different ground planes on the PCB that are then connected between them in a single point(with NMR) . This ensures that the noisy digital return currents travels only on the GNDD witouth affecting other grounds.

How the power supplies were chosen,designed and filtered , is discussed in the next chapter.



(a) uC Analog Input Circuit (b)uC JTAG and Crystal Ocillator

Fig 3.2 Microcontroller Analog Circuits

In fig 4.43 (a) all the measures of current and voltage and the end of the measure stage are connected to the ADCs. The pins are selected based on the sampling order of the ADCs. There are four ADCs (A, B, C, D), each of them have several input channels (A0, A1, A2, ...). The channels with the same number are sampled in the same time instant, for example channels A2, B2, C2 and D2 are sampled in the same instant. To have all the main measures (Input and Output Voltage and currents) taken at the same time they are put in the same order (A2,B2,C2,D2)

For the analogic part of the microcontroller to work properly 3V as reference signal have to be provided. This is design by the circuit in figure 4.44 , in which there is a precise regulator that transforms the 5V into 3V, followed by two voltage followers, shown in fig 4.45. Voltage dividers are not used in these cases since they have low efficiency and low precision due to resistance tolerances. The reference voltage is connected to the microcontroller through the pins 37, 53, 35 and 55.

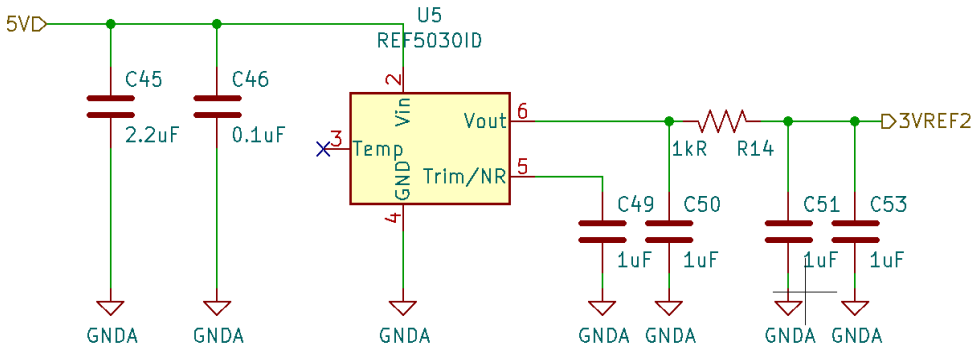


Fig 3.3 Reference Voltage Circuit

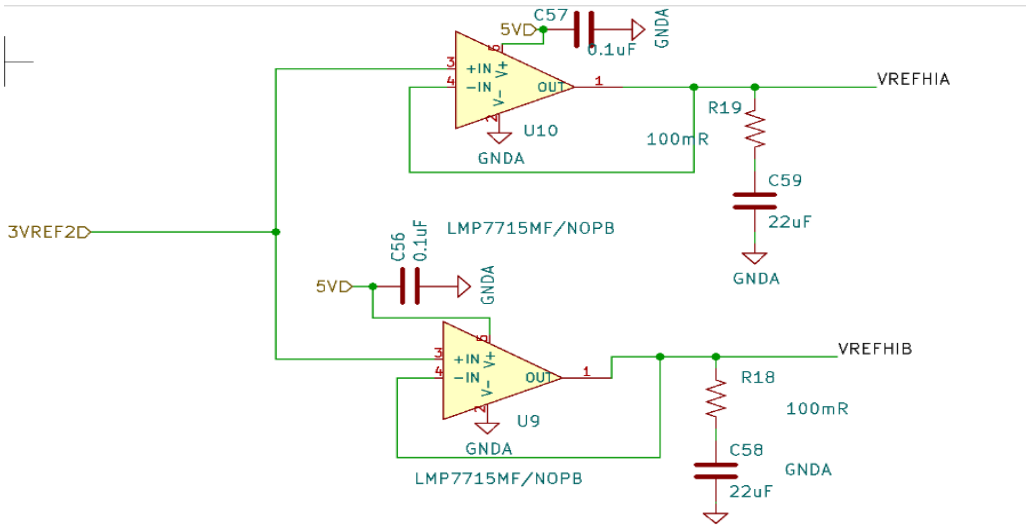


Fig 3.4 Voltage Followers Circuits

3.2 Fault Circuit

The high level design of the fault circuit is shown in fig 3.5

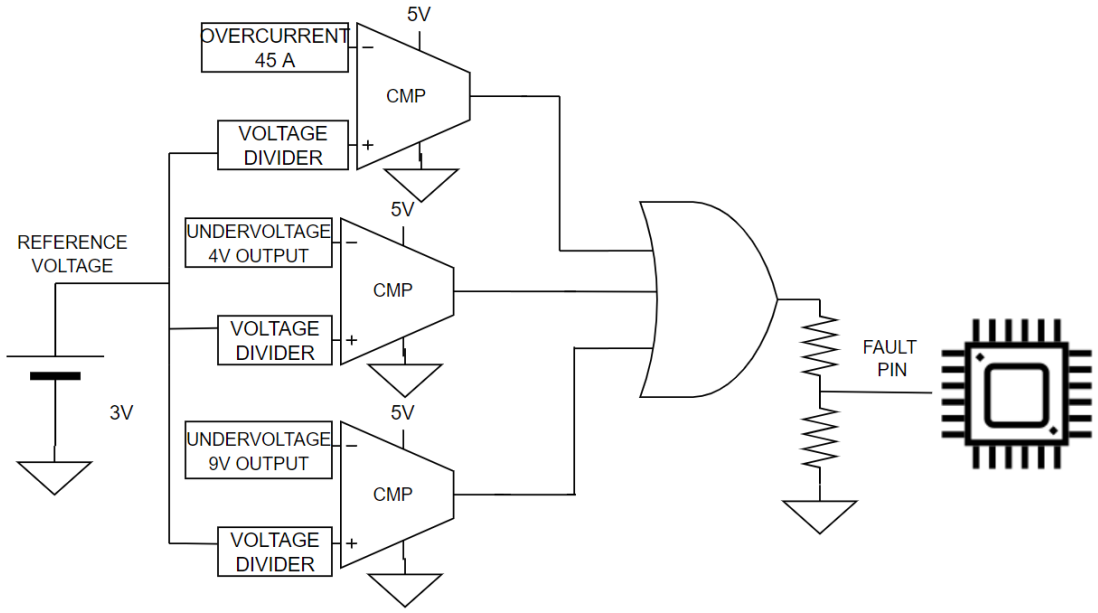


Fig 3.5 High Level Design of Fault Circuitry

The aim of the Fault Circuit is to prevent damage to the NIBB in case of Overcurrent (45A) and Undervoltage in both input and output In detail, there is:

1) Precise voltage reference of 3V.
2) 3 Opamps LM7115MF-NOBP which act as comparators. On the negative pin there is the faulty measurement and in the positive pin the equivalent voltage threshold. Since each threshold is different, it is necessary to design each divider for each faulty measurement
3) Even if one of the comparators saturates at 5V, the measure is considered faulty : the logic gate suitable for this condition is an OR
4) The OR circuit is supplied with 5V, it is necessary to design again another voltage divider in order to fed this 5V in the uC fault Pin

Given The divider equation as :

$$Vout = Vin\ \frac{R2}{R1 + R2} \tag{39}$$

Where Vin=3V, R1 and R2 are designed as follows:

1) For the input voltage, when there is the undervoltage of 4V (with an already present divider at the input) the threshold is set to be 200mV. Hence, a suitable combination of the divider is given by R1=140kΩ and R2=10kΩ
2) For the output voltage, when there is an undervoltage of 9V (with the already present divider at the output) the threshold is set to be 1.42V. Hence, a suitable combination of the divider is given by R1=11kΩ and R2=10kΩ
3) For the inductor current, when there is an overvoltage greater than 45A (after the measure stage) the threshold is set to be 2.67V. A suitable combination of the divider is given by R1=1.2kΩ and R2=10kΩ
4) At the output of the OR GATE there will be 5V even if just one of the previous condition is met. It is hence necessary to transform again this 5V into 3V readable by the uC. A suitable combination is given by R1=6.8kΩ and R2=10kΩ

Since the stage is quite complex , it is necessary to run an LTSPice simulation in order to verify the rightness of the circuit.
The circuit is shown in fig 3.6, while the plot results in fig 3.7

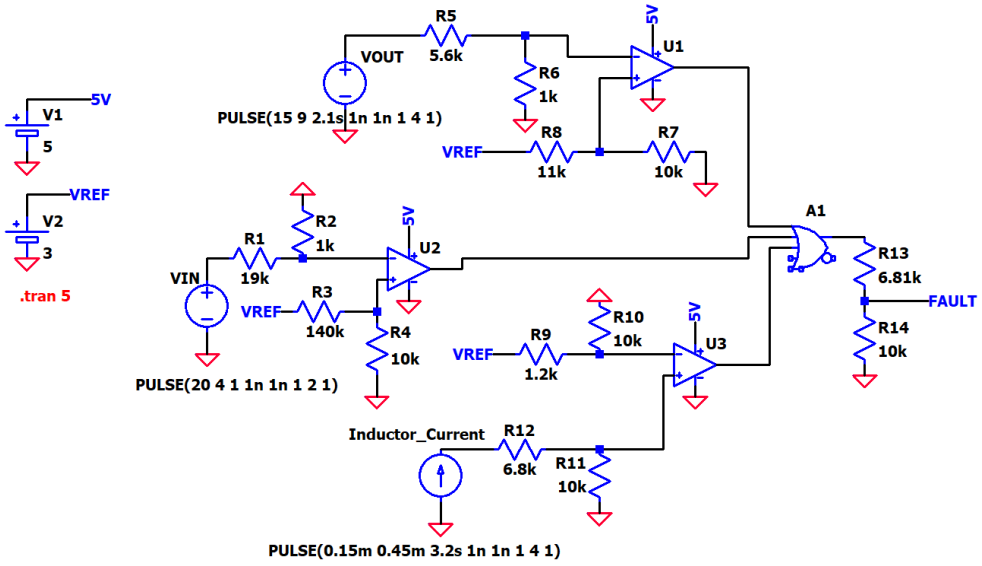


Fig 3.6 LTSPice simulation of the Fault Circuitry

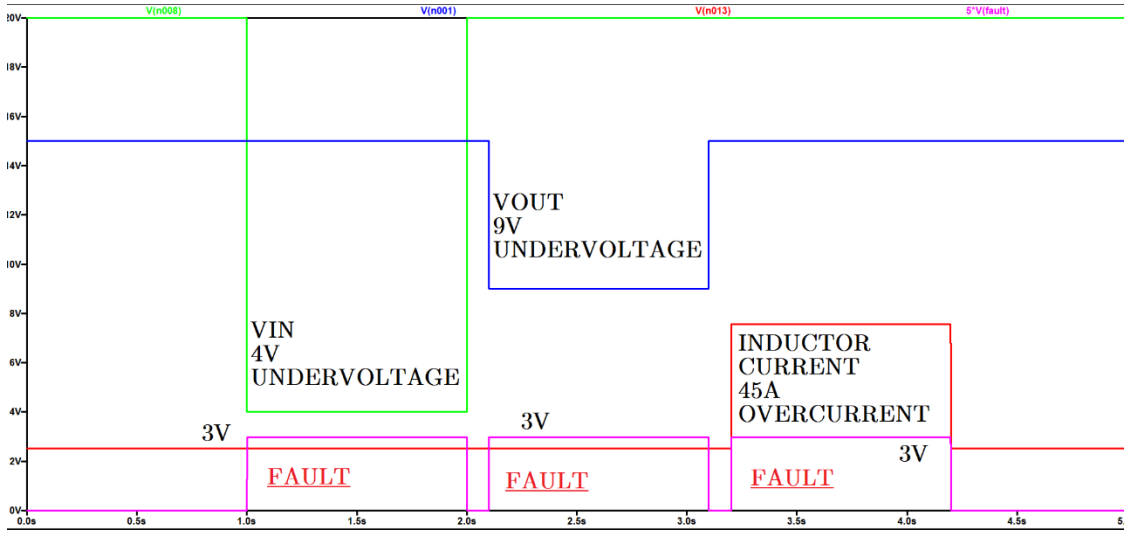


Fig 3.7 LTSPice Simulation Results of the Fault Circuitry
In green, the input Voltage, In blue, the Output Voltage, In red, the Inductor Current and in Violet the Output of the divider After the OR Logic Gate

The LTSPice function PULSE is used in order to verify that even if one faulty output occurs while the other are not, the fault output will be still triggered.
From the simulation results in Fig 4.49, it can be verified that, for instance, if there is an Output Voltage of 15V the fault is not triggered, while if there is an undervoltage of 9V which is not enough to charge the battery, the fault circuit will be triggered.
The output "fault" is about 3V, hence all the dividers as well as the comparator thresholds were well designed.

3.3 Digital Section

In figure 4.50 the Digital Section of the microcontroller.
The GPIO pins are internally connected in groups of 32

- Group A: GPIO0-GPIO31
- Group B: GPIO32-GPIO63
- Group C: GPIO64-GPIO95
- Group D: GPIO96-GPIO127
- Group E: GPIO128-GPIO159
- Group F: GPIO160-GPIO168

Each group is assigned to one of the two CPUs. The best choice is to assign group A and B to the CPU1 and group C to the CPU2.

In particular:

• GPIO0-GPIO3: are able to generate PWM signals for the drivers that will drive the two Half Bridge GaN Mosfet

• GPIO30-GPIO31: are used for the CANH and CANL

• GPIO43-GPIO44: are used to select if the dead time will be hardware or software. Put to GNDD since our dead time is software-generated.

• GPIO72, GPIO84: are used for the startup procedure.

• GPIO154, GPIO139: are used for boot procedure. They both must be connected to the 3.3V and GND(used NMR if necessary)

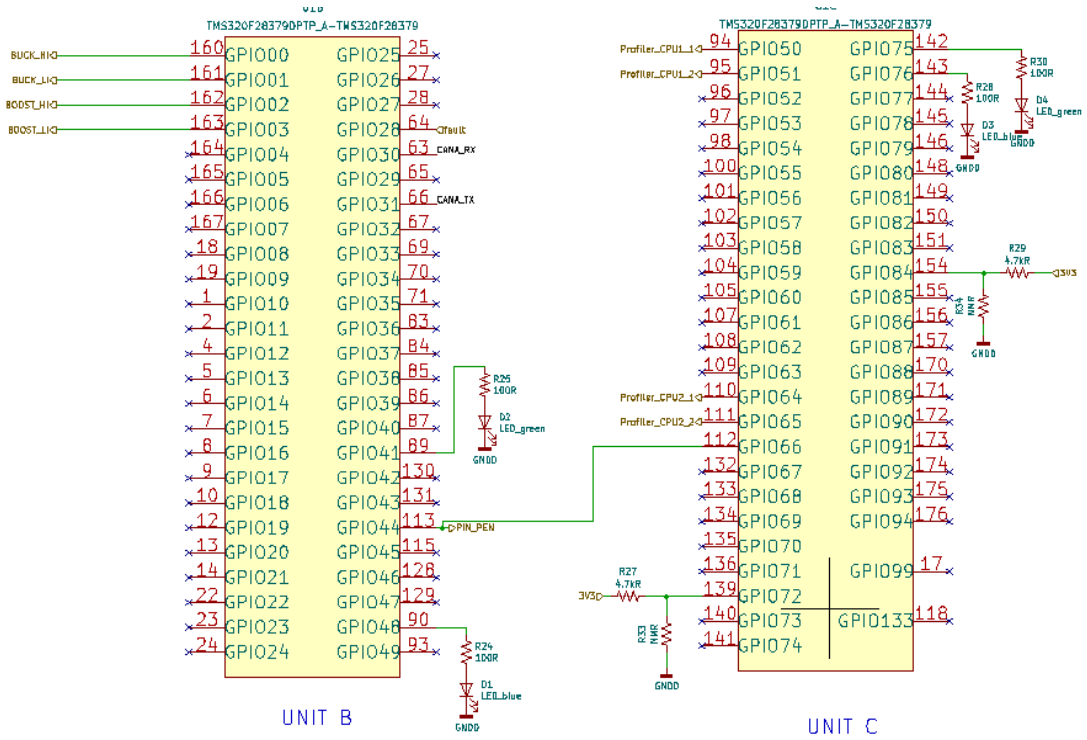


Fig 3.8 Digital Section of the Microcontroller

3.4 External Connection

In this section the analysis of the connectors used to communicate with the microcontroller, as well as JTAG and CAN are presented.

JTAG (Joint test action group)

The JTAG is a standard protocol which allows the programming of the microcontroller. It's most important signals are:

1) TCK : JTAG test Clock
2) TDI : JTAG Test Data Input
3) TDO: JTAG Test Data Output
4) TMS: JTAG Test Mode Select
5) TRST: JTAG Test Reset. Must be maintained low for normal operation conditions

The other signals are connected as suggested in the datasheet of the microcontroller.

Connections in KiCad are shown in fig 3.9

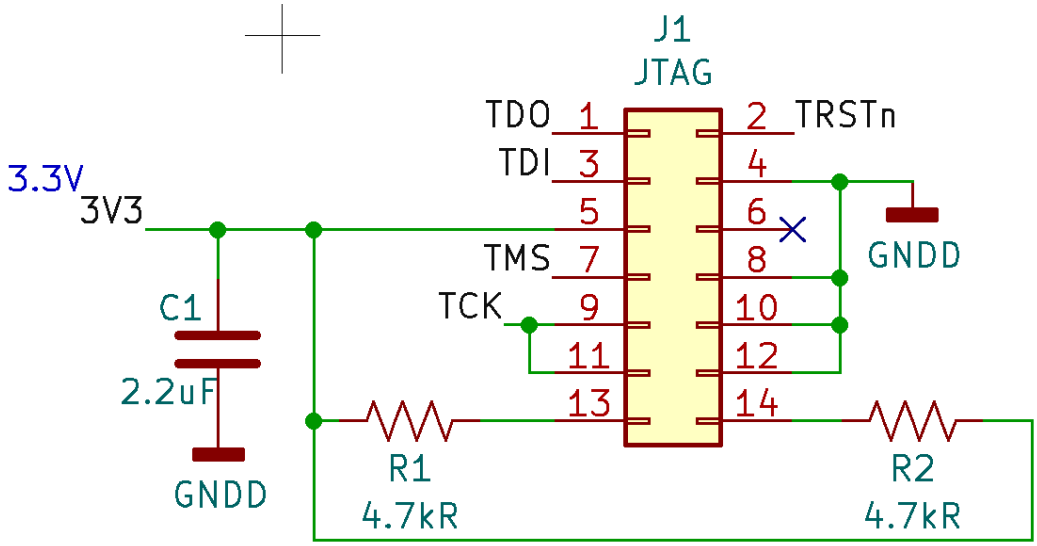


Fig 3.9 JTAG Connector with suggested datasheet connections

CAN

The CAN is a communication serial protocol very robust and strong against noise, specifically designed to work in noisy environments and for this reason is mostly exploited for automotive and mechatronic applications.
To fully understand how to use the CAN protocol, it is necessary to understand the meaning of each signal and port used in most common interface circuits, which are

1) TXCAN/RXCAN: Input signals in CAN Module, logic signal transmitted /received
2) CANL/CANH: Output Complementary Differential Signals

The CAN module employed is the HVDA5415QDRQ1 and its connection are showed in fig 3.10

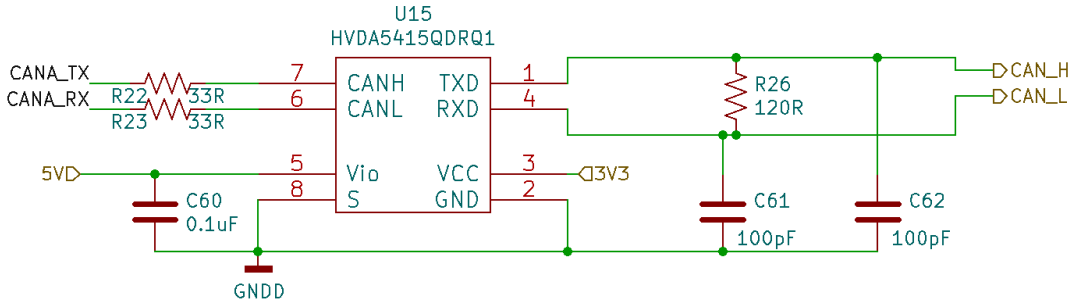


Fig 3.10 CAN Module Connection in KiCAD

In the electrical parameter of the datasheet of the HVDA5415QDRQ1 can module, the differential input resistance is 110Ω. Hence, a 120Ω resistor is necessary to satisfy the impedeance matching

3.5 Supplies

It is necessary to design many different power supplies in order to supply all the active components in the NIBB, like op. amplifiers, current sensors, microcontroller, logic gates and so on. In particular, it is necessary:

1) 5V for the operational amplifiers and all analog circuitry
2) 1.2V for the microcontroller (low ripple required)
3) 3.3V for the microcontroller
4) [9-12] V for the Gate Drivers

In order to design any power supply, it is necessary to take into account the following features:

1) Topology Choice (Buck, Boost, Buck-Boost, Isolated, Non-Isolated)
2) Input Voltage Requirements: both the minimum and maximum voltage must not be exceeded
3) High efficiency: at least 90% in the working condition
4) Output current requirements: the maximum output current should be enough to supply all the components in full load
5) Low ripple
6) Input and Output Capacitor Design

Since the nominal voltage of the battery (12V) is used and all the other voltages are less than 12V, buck converters are employed.
In order to have a more reliable input voltage for each buck converter, an CLC filter (fig 3.11) was designed to reduce furtherly the output ripple.
The frequency of the CLC low pass filter is given by equation(40)

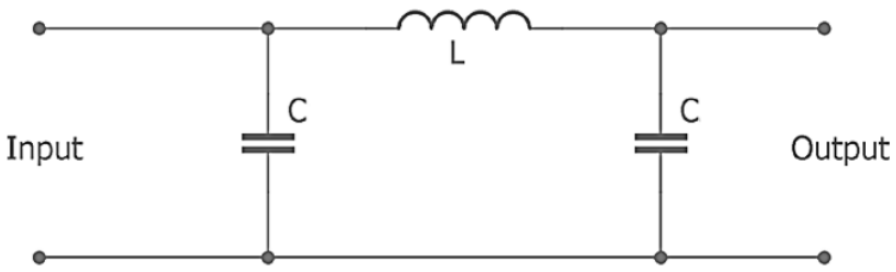


Fig 3.11 CLC Pi Filter

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{40}$$

From the previous chapter, it was confirmed that in DC-DC converters the noise in the output voltage and currents is mainly given by the switching frequency. Hence it is necessary impose an attenuation of at least -40/50dB at the switching frequencies.

A suitable combination is given by C=10uF and L=4.7uH. The bode diagram is showed in fig 3.11

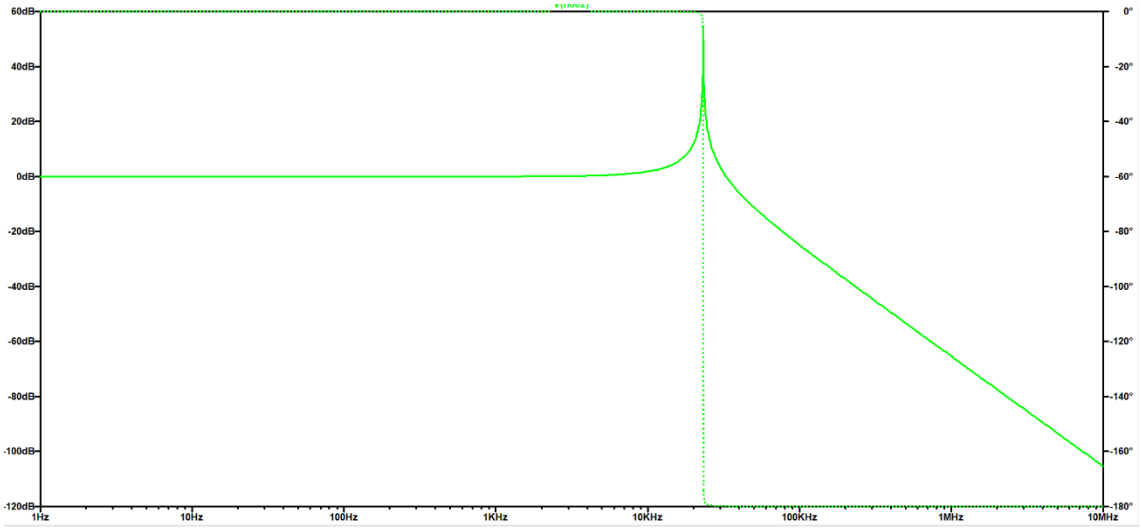


Fig 3.11 Bode Diagram of PI Filter

Let's test the filter by imposing to the nominal 12V battery a 1V ripple in LTSPICE. Simulation results are shown in Fig 3.12

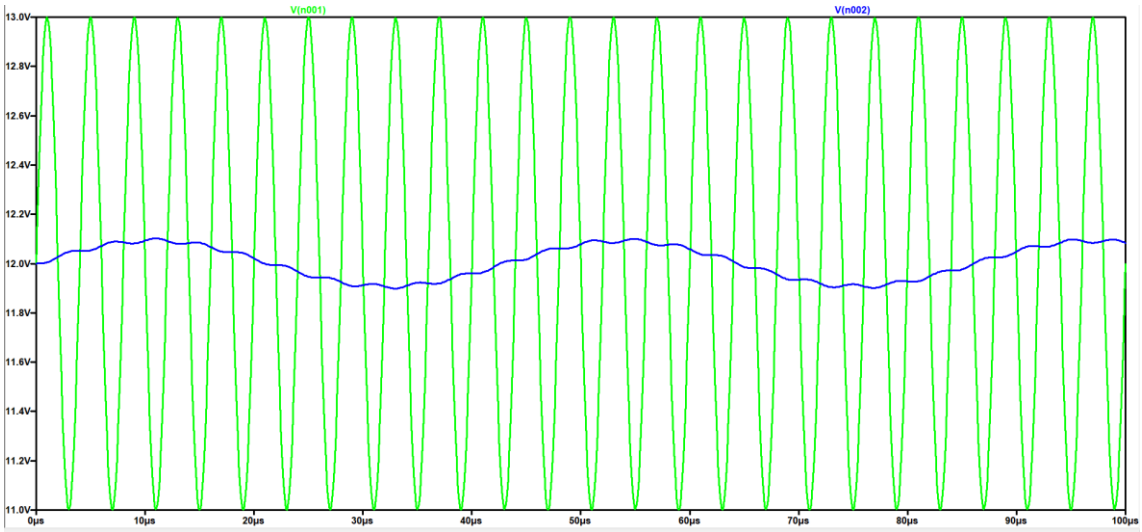


Fig 3.13 Simulation Results of a 12V Voltage with 1V ripple(green) compared with the filtered waveform after CLC filter (blue)

From the previous simulation results it is shown that 1V of ripple is greatly filtered, only less than 200mV remain.
L is a power inductor. Selection criterion of power inductor and capacitors are explained in chapter 2.
A suitable inductor is the SRU1048-R80Y, able to sustain up to 8A.
The full CLC filter in shown in fig 3.14
Since the 12V has reference to the GNDPWR and the 12V filtered to the GNDA instead, this filter decouples the two previous ground mentioned.

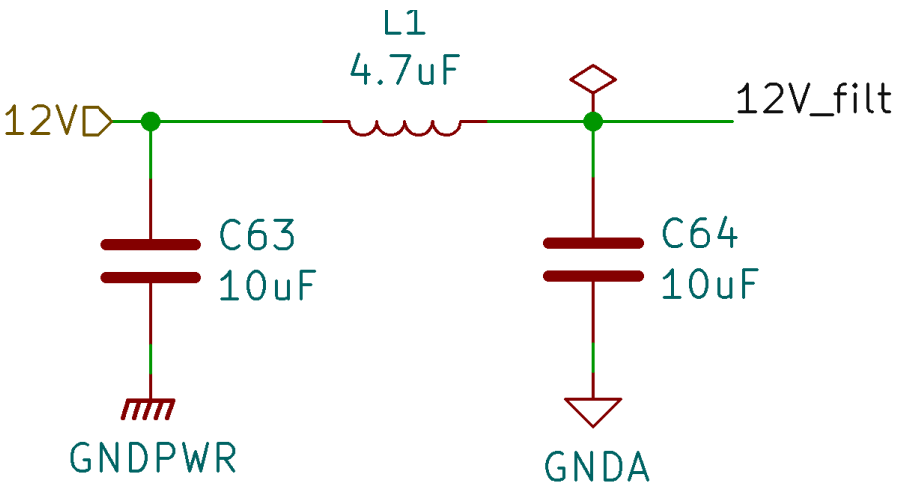


Fig 3.14 KiCad CLC Filter used to smooth the output voltage

From this point onwards the 12V filtered as input to each buck converter is used instead of the nominal 12V.

5V

The 5V Power supply was designed taking into account that the LMP7715MF-NOBP consumes only 1.15 mA of supply currents.
To be sure to supply all the opamps it is necessary at least 50mA. In addition to the opamps there are the logic gate and the three INA currents sensors.
The P7805-2000-S , suitable for 5V offers:

- 8-36V as Input Range
- 5VOutput Voltage with 75mV Output Ripple
- 2A maximum output current
- 90% efficiency
- Very easy connections since only two capacitors are required

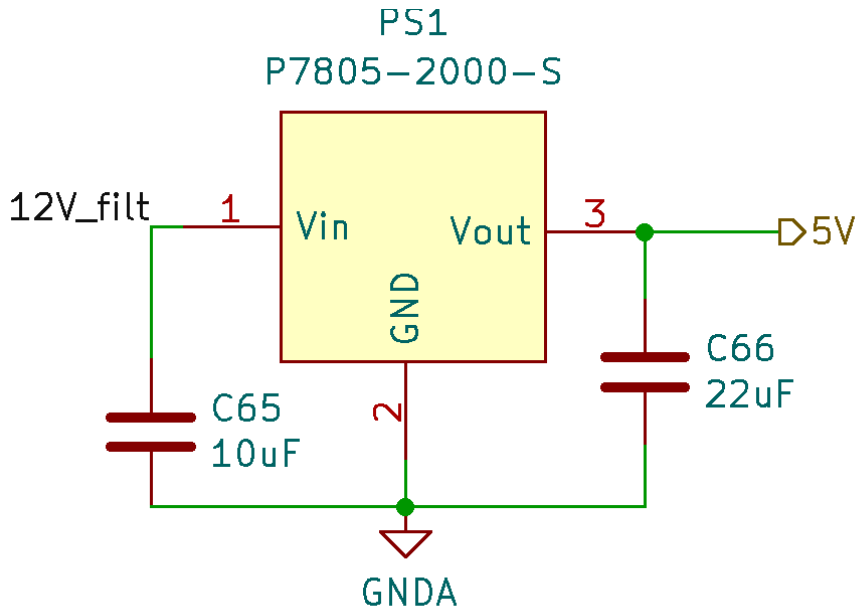


Fig 3.15

KiCad 5V Power Supply

From Fig 5.5 a typical application circuit suggested by the datasheet is shown. The input capacitance has to be 22uF/50V while the output capacitance must be 22uF/10V

3V and 1.2V

These two voltages must be very precise since they have to be fed to the microcontroller. Another π filter is then required.
Ferrite Beads are employed since the current requirements are not so high as in the previous case (power inductor not needed). Compared to standard inductors ferrite beads have:

1) High DC resistance (100-200 **Ω**)
2) Less Q
3) Capability to block high frequency noise with less demanding space (SMD 0603 package quite common on the market)

Let's test a CLC filter with a ferrite bead on LTSPICE and compare it to the previous filter in fig 3.12
The circuit is shown in fig 3.16, while the simulation results in fig 3.17

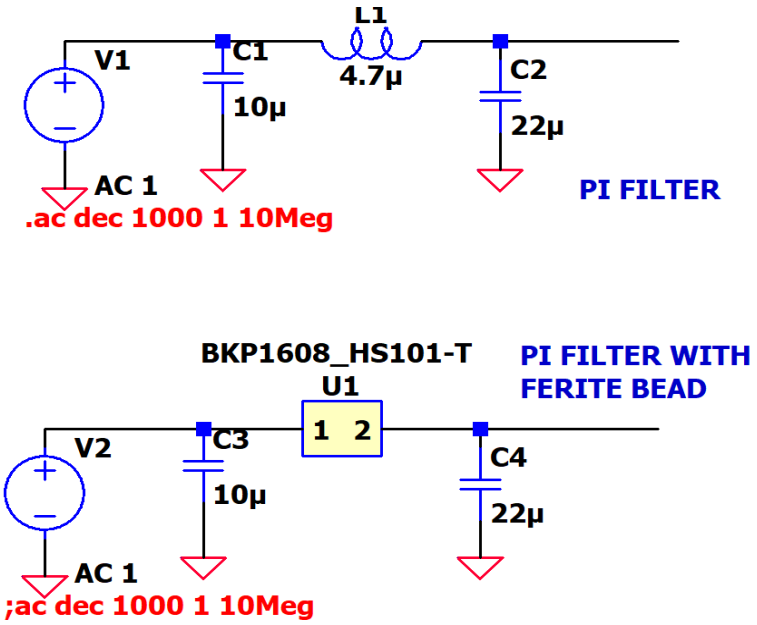


Fig 3.16 LTSPice circuit representing two PI filers. Above, Pi filter designed with standard inductor, while the other designed with ferrite bead.

The BKP1608˙HS101-T with 180Ω DC resistance is employed.

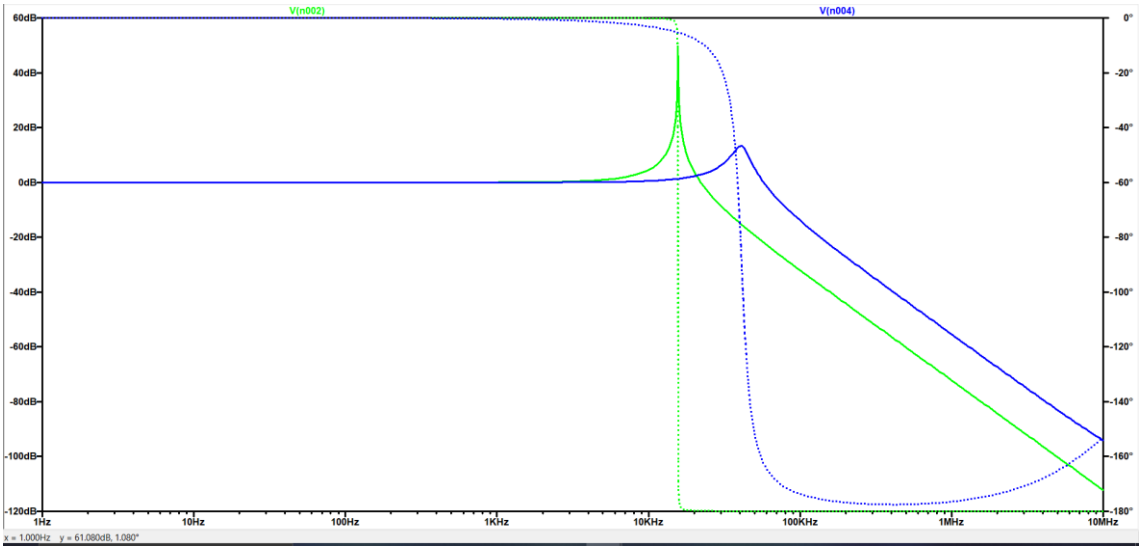


Fig 3.17 LTSPice results of circuit in fig 3.16 In blue, the PI filter with the ferrite bead, while in green the PI filter with the standard inductor

From the simulation results in fig 3.17 it can be verified that the behaviour of the PI filter with the ferrite bead is similar to the one designed with the standard inductor. As expected from the proprieties of the ferrite bead, the quality factor Q is way less than the standard inductor.

Then, for the same reason explained before, the P78003-2000 is employed for the 3V output voltage .The full circuit is showed in fig 3.18

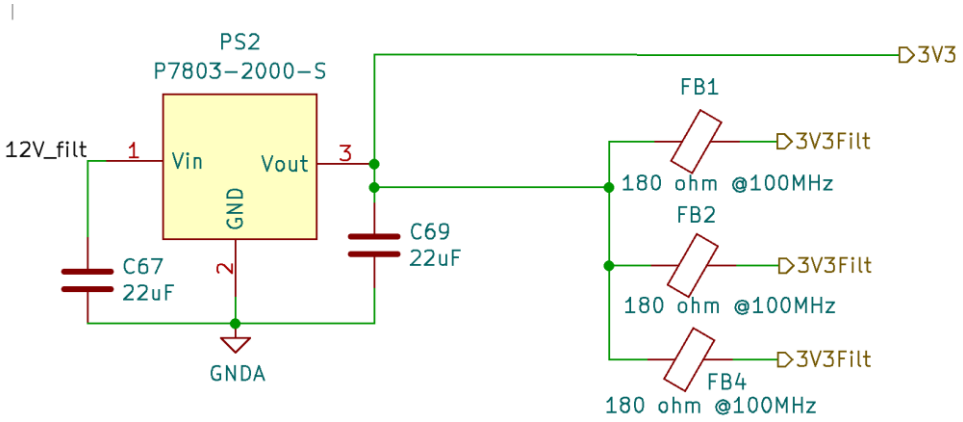


Fig 3.18 3.3V Buck Converter in KiCad with ferrite beads

The ferrite beads with the bypass capacitors of 0.1uF in the microcontroller (fig 4.42) create an CLC filter , filtering the 75mV output of the step-down.

The same applies for the 1.2V. The TSR˙1-2412 is chosen and the output voltage is followed by the ferrite bead.(fig 3.19).

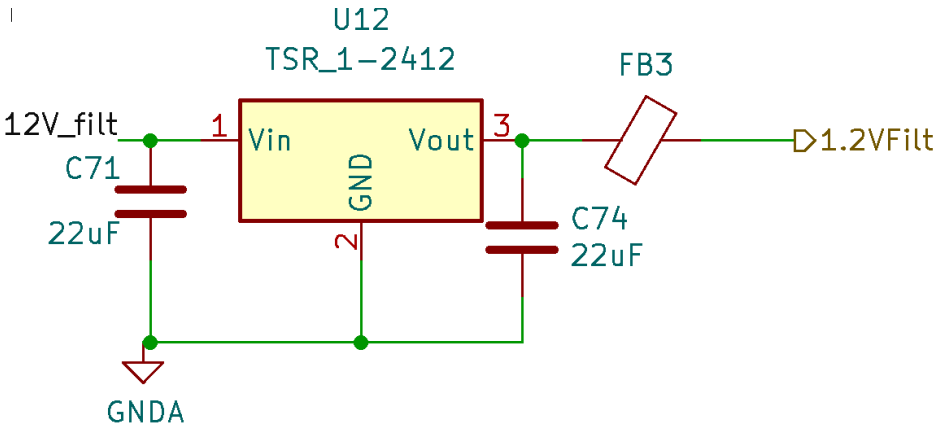


Fig 3.19 1.2V Output Step Down in KiCad

9V Driver

From the datasheet of the NCP51820 the sink current required is 1A while the minimum power supply is 9V.
Hence the P709-2000 is chosen, since it's able to provide up to 2A and designed like the previous case.

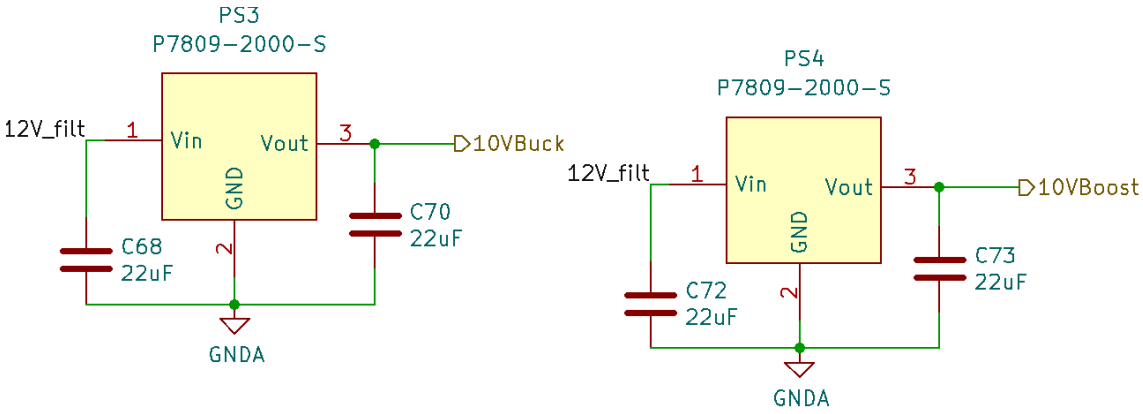


Fig 3.20 9V Power Supplies Driver

The optimal Voltage would be 10V to be sure that the driver is ON , but due to the lack of devices in the market, 9V are used instead.

Chapter 4 PCB Layout

Starting by describing the Pcb by a technological point of view, it follows the power plane layout with detailed description about the use of power planes as well as grounding planes, with in addition the layout realization of the logic board.

The PCB design is crucial in any electronic system and it can even make a big difference during the testing phase.
In this thesis two PCB were designed

1) The Power Plane, made of power components (GaN Mosfet and Power inductor) and large copper areas to sustain thermal increase during full load
2) The Logic Plane, made with the microcontroller connections and the power supplies

Before starting explaining the PCB design, it is necessary to build up some state of art regarding the pcb traces,vias and as well as some golden rules

The trace is the physical connection between two devices and it's visible at naked eye. It's size and it's proprieties are explained afterwards .The via is substantially the electrical connection between layers , hence a small size hole that goes throughout the layers and ensures conductivity and thermal dissipation.
In fig 4.1[11] the via and the trace are showed for better understanding.

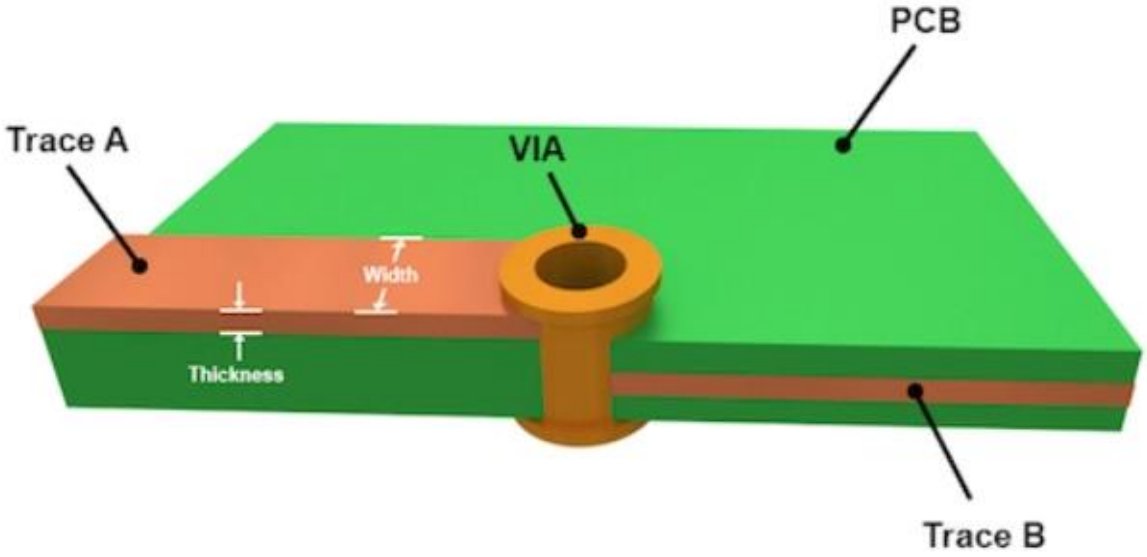


Fig 4.1 Trace and via in a PCB

4.1 Trace and via Parasitic Effects

In general PCB design is crucial in any electronic system and in order to understeand how to make a good design, a deep study of the parasitic effect is required

In equation 41[5] , 42[5], 43[13] the parasitic inductance , the parasitic resistance as well as the parasitic capacitance effect are showed, while in Fig 5.2 there is a clear reference to all parameters equation

$$L(nH) \approx 2x\ln\left(\frac{5.98h}{0.8w+t}\right) \tag{41}$$

$$C(pF) \approx \frac{0.264x(\varepsilon_r+1.41)}{\ln\left(\frac{5.98h}{0.8w+t}\right)} \tag{42}$$

$$R = \rho\frac{x}{tW}[1+\alpha(T-25°\mathrm{C})] \tag{43}$$

Where

- h is the height of the trace
- x is the length of the trace
- ε_r PCB permeability (4 for FR4)
- w is the width of the trace
- t is the thickness of the trace
- ρ is the resistivity of the metal trace

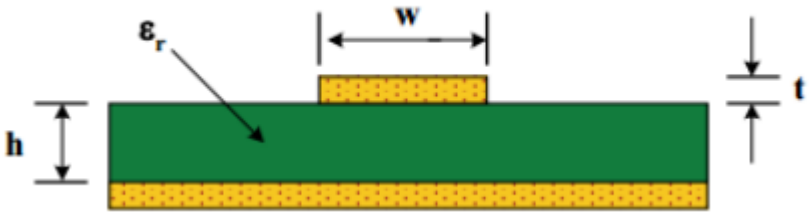


Fig 4.2 Section of the trace with the mentionend equation parameters

To give a practical example, let's use real pcb- data. Having:

- t=35um
- h=1.6mm
- W=8mil
- ε_r=4

The parasitic inductance will be 7.8nH/cm and the parasitic capacitance 0.37pF/cm.

From this analysis it can be immediately understand that

1)The PCB traces should be as short as possible

2)Increasing the width of the trace will result in a reduction of the parasitic resistance

From the inductance and the capacitance it can be studied also the nominal resistance as well as propagation times of the trace, showed in equation (44)[5] and (45)[5] valid for both traces and vias

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}} \tag{44}$$

$$T_p(ps/cm) = 31.6\sqrt{L(nH)C(pF)} \tag{45}$$

For what regards the vias's parasitics, eq(47)[5] and eq.48[5] shows the parasitic inductance and the parasitic capacitance, while in fig 5.3 the parameters are clearly shown in the image

$$L(nH) \approx \frac{h}{5}\left[1 + \ln\left(\frac{4h}{d}\right)\right] \tag{46}$$

$$C(pF) \approx \frac{0.0555\varepsilon_r h d_1}{d_2 - d_1} \tag{47}$$

Where

- h is the height of the via
- d is the real diameter of the via
- d1 and d2 are two other diameters specified in fig 5.3

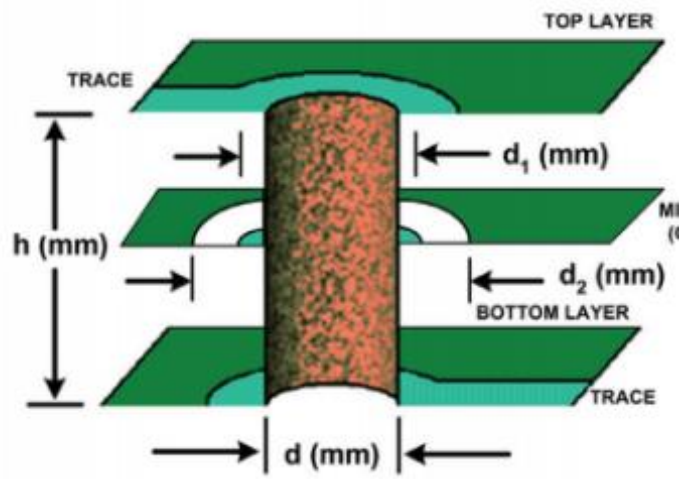


Fig 4.3 Representation of pcb via with all the parameters used in the equations above

To give a practical example, let's use real pcb numbers

- h=1.6mm
- d=0.6mm
- d1=0.8mm
- d2=1mm

The parasitic inductance and capacitance will be respectively 1.07nH and 1.4pF

Parallel Traces

Two metals in which in between there is an insulator form a capacitance. Hence, parallel traces forms a parasitic capacitance which should be avoided. [12]

Both the cases of the two tracks in the same layer (fig 5.4) [12] and in the adjacent layer are analyzed (fig 5.5)[12]

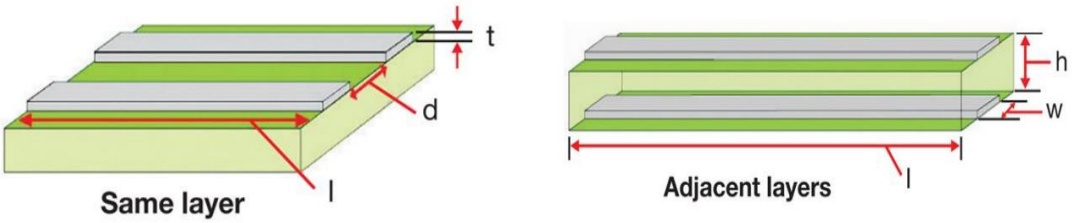


Fig 4.4 Two parallel tracks in same layer and Adjacent Layer

The equation that quantifiy this phenomena is described in eq 48 for the same layer case and eq(49) for the latter

$$C = \frac{k \times t \times l}{d} \tag{48}$$

$$C = \frac{k \times \varepsilon_r \times w \times l}{h} \tag{49}$$

Where

- k is the permittivity of free space
- t is the thickness of the trace
- l is the length of the trace
- ε_r dielectric of PCB (most commonly used FR4)
- w is the width of the trace
- d is the distance between two traces

Moreover, parallel traces can even be exposed to a parasitic inductance effect. A varying current in a metal conductor produces a magnetic field, which as a consequence generate current limitrophe conductive loops. This can be explained with the Faraday's Law and the coupling effect is enhanced with the lowering of the distance. [12] This problem is more evident in high speed signals.

Trace thermal considerations

In power electronics circuits traces must be able to sustain high currents, hence the width must be designed taking into account the maximum current that has to flow without incrementing too much the temperature

The formula used in most common PCB tools calculator like KiCad is from IPC 2221 standards eq(50)

$$I = K \cdot \Delta T^{0.44} \cdot (W \cdot H)^{0.725} \tag{50}$$

Where:

- I is the maximum current [A]
- ΔT is temperature rise [C]
- W is the width [mills]
- H is the thickness(height) [mills]
- K is 0.024 for internal traces and 0.048 for external traces

If the trace has to sustain a 25A of current with a temperature rise of 70C, the minimum trace width is 4mm with 2 oz/ft (0.068 mm) for the external trace while a 10mm of trace is required for internal traces.
To better improve the thermal performance of power traces, power planes are used instead.

General Rules for PCB Design

Now that we have covered the basis of the PCB, we can understand better some of the general common golden rules in the PCB design

1. Trace should be as short as possible to minimize parasitic effect

2. Traces should match the desired width to reduce parasitic inductance and to to sustain the desired current

3. Avoid vias as much as possible to furtherly reduce the parasitic effects and to avoid breaking power planes

4. Use at least one power plane with GND, grants noise reduction, strengthen mechanical board, resistance minimization.

5. Use bypass capacitors near the IC to filter the noise of the power supply

6. Take care of ground loops to reduce the EMI

7. Power Mosfet ,Drivers, Shunt resistor and other components may have precise consideration to take into account in their respective datasheet.

8. Avoid angles of 90 degrees traces or power planes. A 1mm radius fillet is used in the Layout Design for power ground and planes.

9. Separate Analog Ground, Digital ground and Power Ground

10. Leave space for No-mounting protective components for power devices like snubbers and body diodes, as well as space for various testing point to simplify the testing procedure

11. Use indicator devices like LEDs for the internal power supply, to simplify troubleshooting

12. Use thermal vias to improve thermal efficiency of power devices.

4.2 Power Board Design

The most important step in a PCB Design is the optimal placement of the components. Finding a good combination of component placement means optimizing areas,routing and traces as well. In fig 4.5 is shown the high level design -optimal placement of the power plane

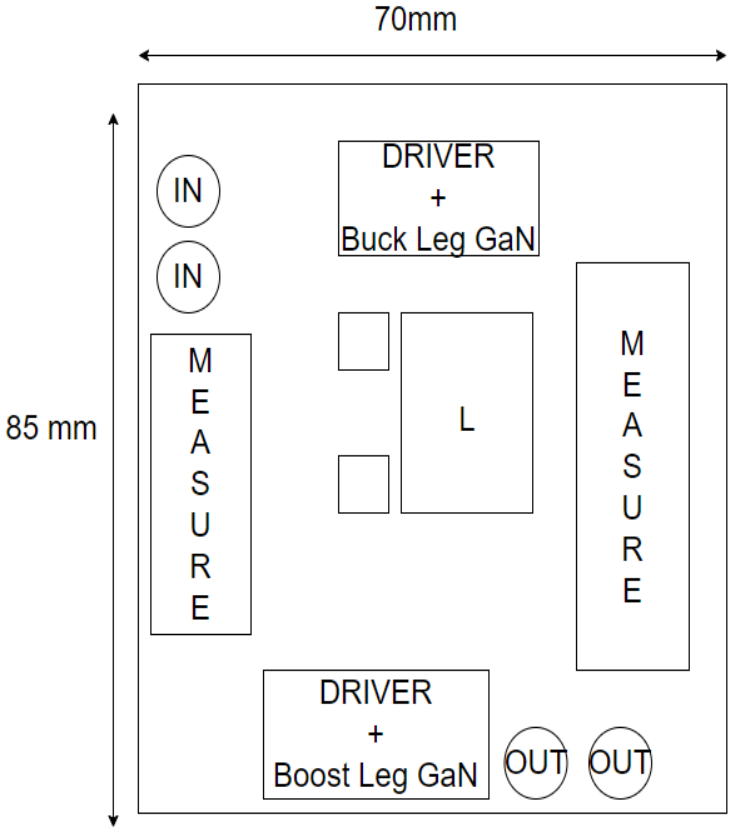


Fig 4.5 High Level Placement of components in the Power Plane

Since there are two legs the smartest choice was to put the inductor at the centre of the board and the two legs in the same line, to obtain almost a symmetrical structure and the power area as straight as possible

4 Layers have been used:

1) Top Layer (RED) : All the components are placed here as well as their main routing
2) Bottom Layer(BLUE): used for GNDA. No components are placed since the space can be used for heatsink
3) Internal Layer 1 (GREEN): Used for GNDPWR
4) Internal Layer 2 (ORANGE) : Used for 5V and 10V

For what regards the settings requirement in the power plane, these dimension have been used:

1) 0.2 mm track for Drivers and GaN
2) 0.508 mm for Measure Stage (Input,Output and Inductor)
3) Board Minimum Clearance : 0.1 mm (used to meet the requirements for the Driver and GaN)
4) Via size : 0.475mm Via Hole: 0.35mm

In fig 4.6. the use of the 4 layers is shown to better clarify the previous statements

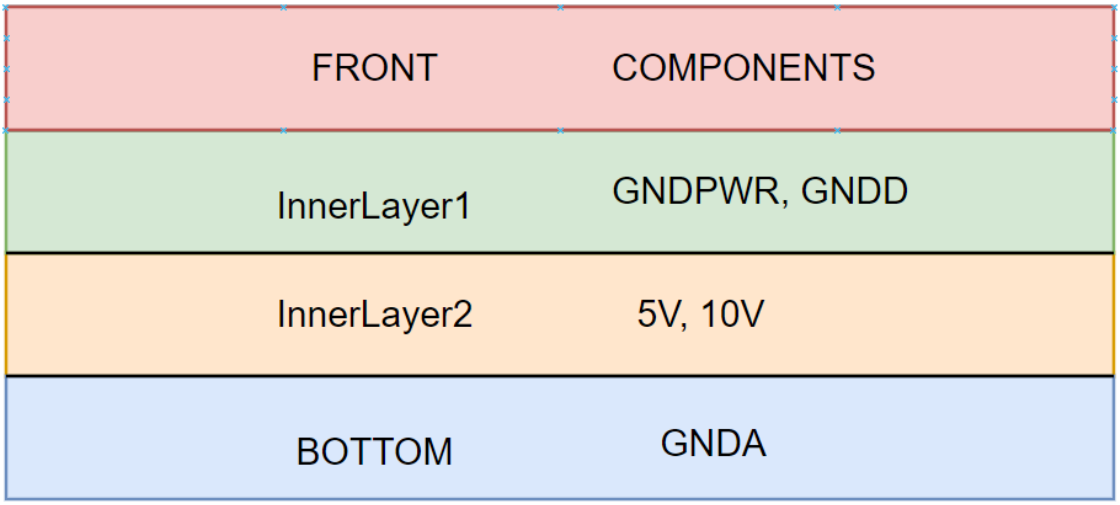


Fig 4.6 Use of the four layers in the

Top Layer

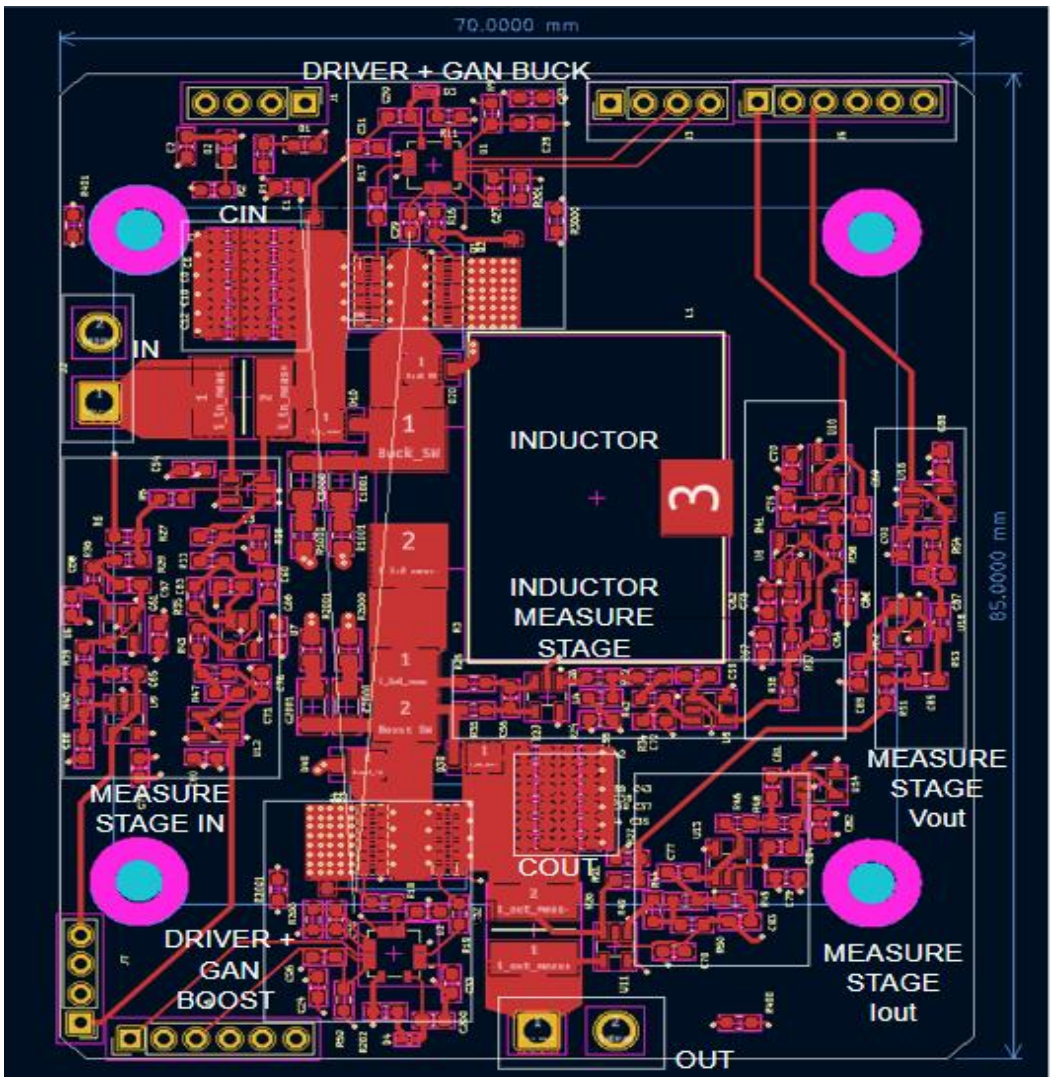


Fig 4.7 First Layer of Power Plane

In Fig 4.7 the first layer of the Power Plane (RED) is shown with all the major components highlighted.

Starting from the Power In connector, we have the 1mΩ shunt resistor (fig 4.8)

Copper areas have been used to match the maximum current requirements as well as heating performances.

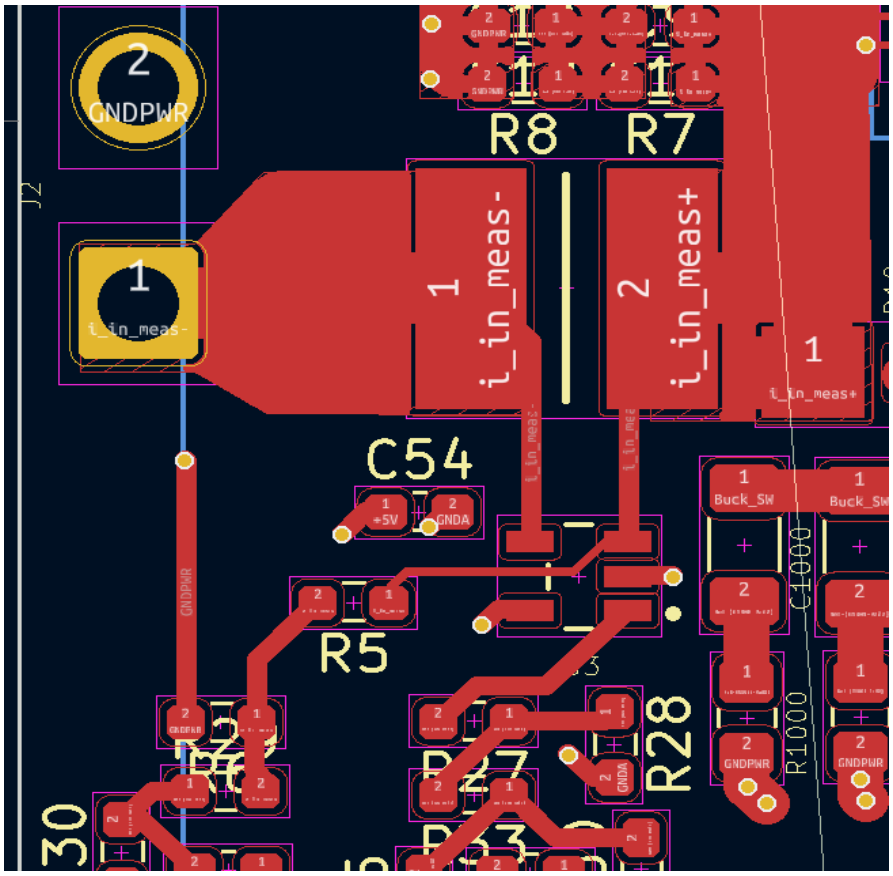


Fig 4.8 Shunt resistor and beginning of measure stage

The shunt connection are optimized following most datasheet suggestion routing, taken from [13]

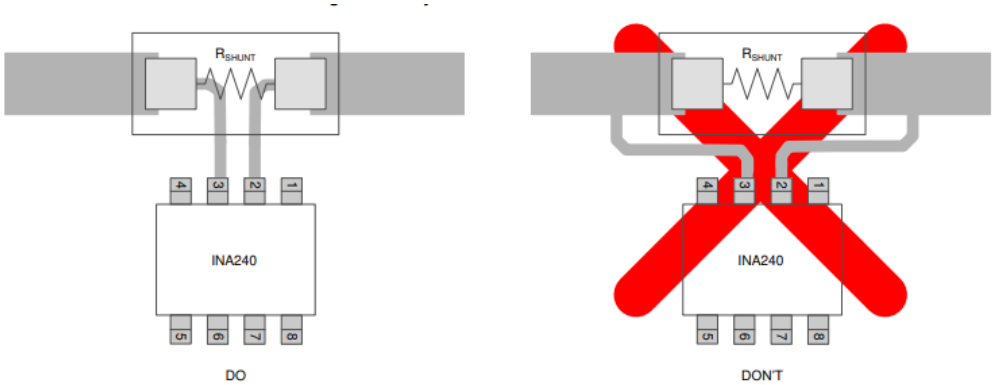


Fig 4.9 Suggested Routing for optimal measurment

In the figure below the two GaN (Buck Leg) as well as the input capacitances are shown in the figure below.
In the first instance , power areas have been used in the Switching Node as well as the Low Side Gan Ground and after the shunt to sustain enough current and provide thermal efficiency.
Then, as it can be seen, by placing the vias to GNDPWR on the left of the input capacitances and forty vias to GNDPWR on the right side of the Low Side GaN, the ground loop is minimized since the GNDPWR is in the second layer (which is an inner layer) hence ensuring a tradeoff between the shortest path and copper areas.

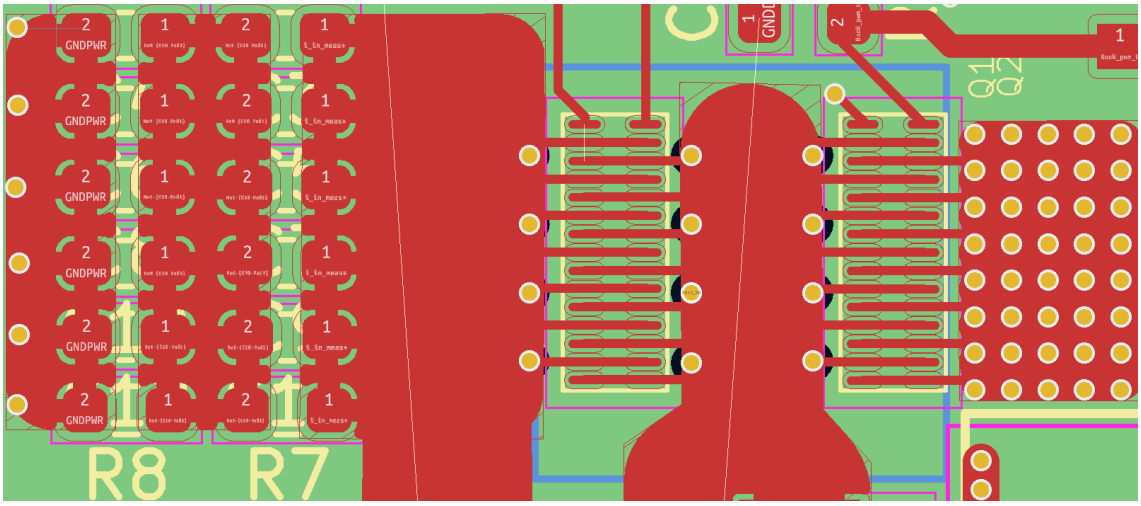


Fig 4.10 Input Capacitance and Two GaN. In Blue, the space used for the Top Heatsinker

For what regards the driver , the connection have been made following the datasheet's suggestion.
Three connectors are showed in the figure below. Starting from the left, the first connector is used for the 5V and 10V power supply with the blue and green led to simplify the testing procedure .

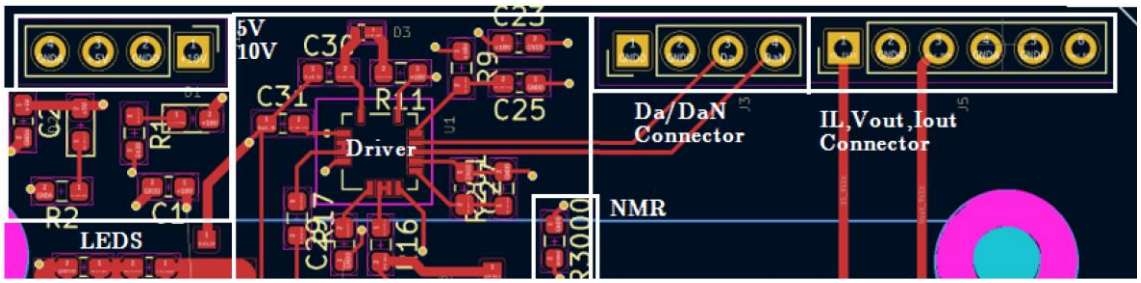


Fig 4.11 Power Plane Top Connectors and Driver Connection

Following the second connector, used for the Da and DaN PWM signals to be fed into the driver coming from the controller.
The last connector is used for the Inductor , Output Voltage and Current measure stage using the GNDA as a reference ground.

The bottom part of the front plane is showed in fig 4.12. The Boost leg as well as the driver have a symmetrical connection with respect to the Buck leg, hence all the consideration regarding the ground loops is valid as well. The two connectors in the bottom are used for the input Voltage and Current's output measure stage, and to provide the two PWM signal Db and DbN for the Boost Leg as well as the 10V for the driver

The importance of the NMR R3001 and R400 will be discussed afterwards.

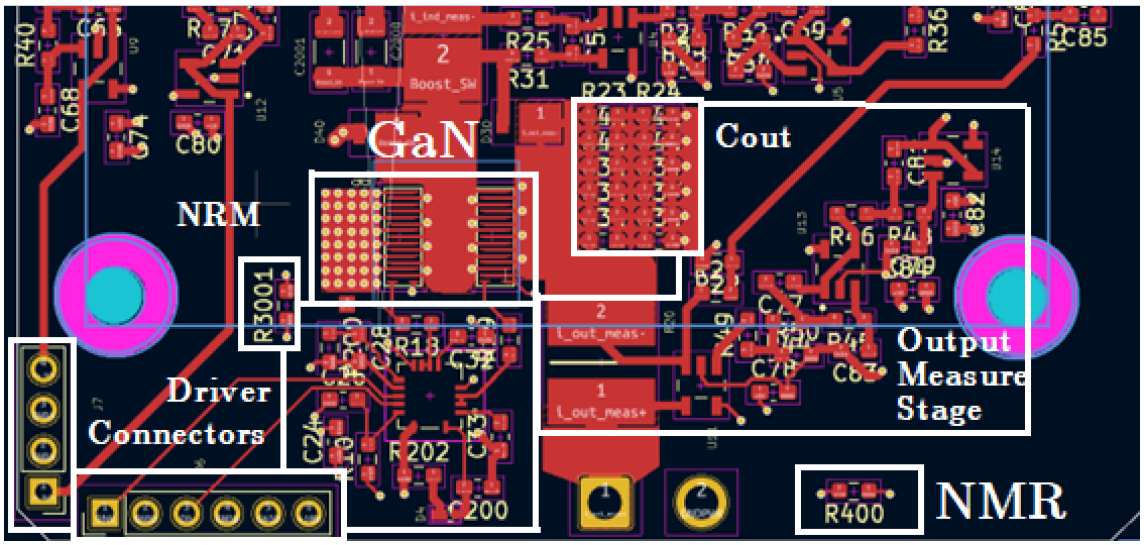


Fig 4.12 Boost Leg and Driver Connection of Power Plane

As explained in the previous chapters, some solder pads were left for the no mounting protective components as well as the no mount resistor. In fig 4.13 the snubber and the protective diode for both legs are shown
A thermal relief gap of 0.127mm and a thermal spoke width of 2mm has been selected as trade-off between the effective copper used and the thermal gaps useful for soldering the smd components.

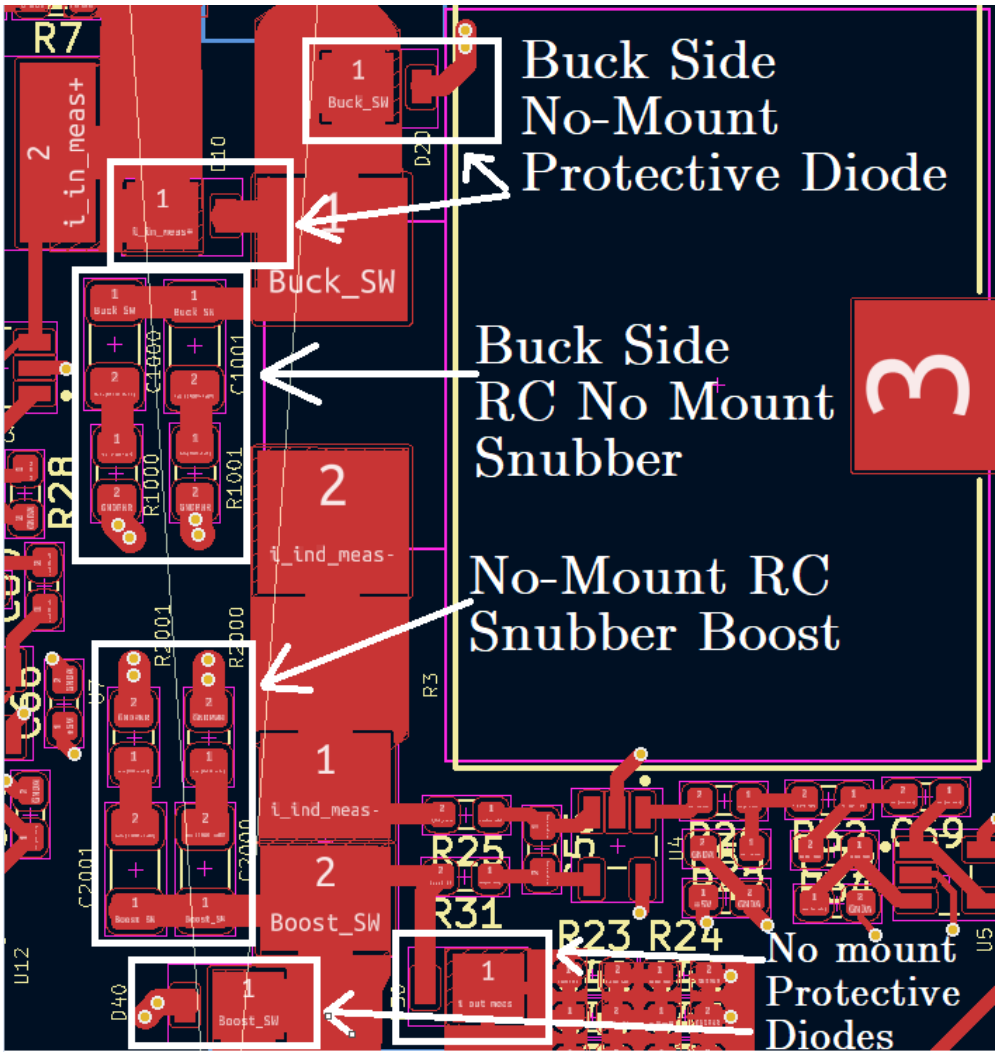


Fig 4.13 No mounting protective components.

Inner Layer 1

In the fig 4.14 below the first inner layer is shown. The Digital Ground (GNDD) has been used under the driver for both legs.

The power ground (GNDPWR) covers most of the areas since it has to sustain noisy currents as well as thermal efficiency. By avoiding to cover also the two measure stage(which uses GNDA) , noisy immunity is granted.
The NMR R3000 and R3001 are used to connect the digital ground with the powerground.

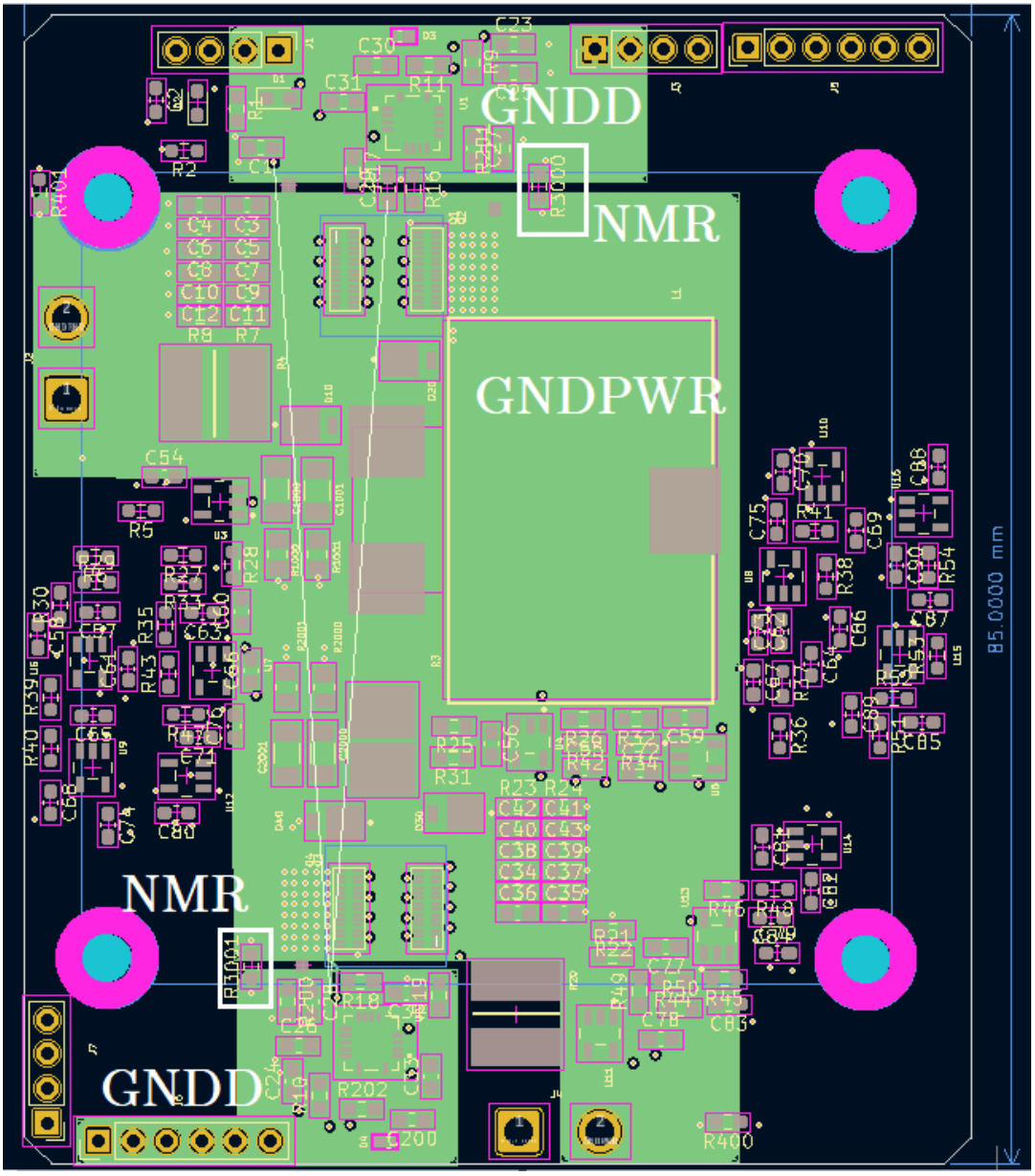


Fig 4.14 First Inner Layer of Power Plane

Inner Layer 2

In the fig 4.15 below it can be seen the inner layer used for power supplies (10V for drivers and 5V for opamps and current sensor) The output of the measure stage track comes from a via in the top Layer

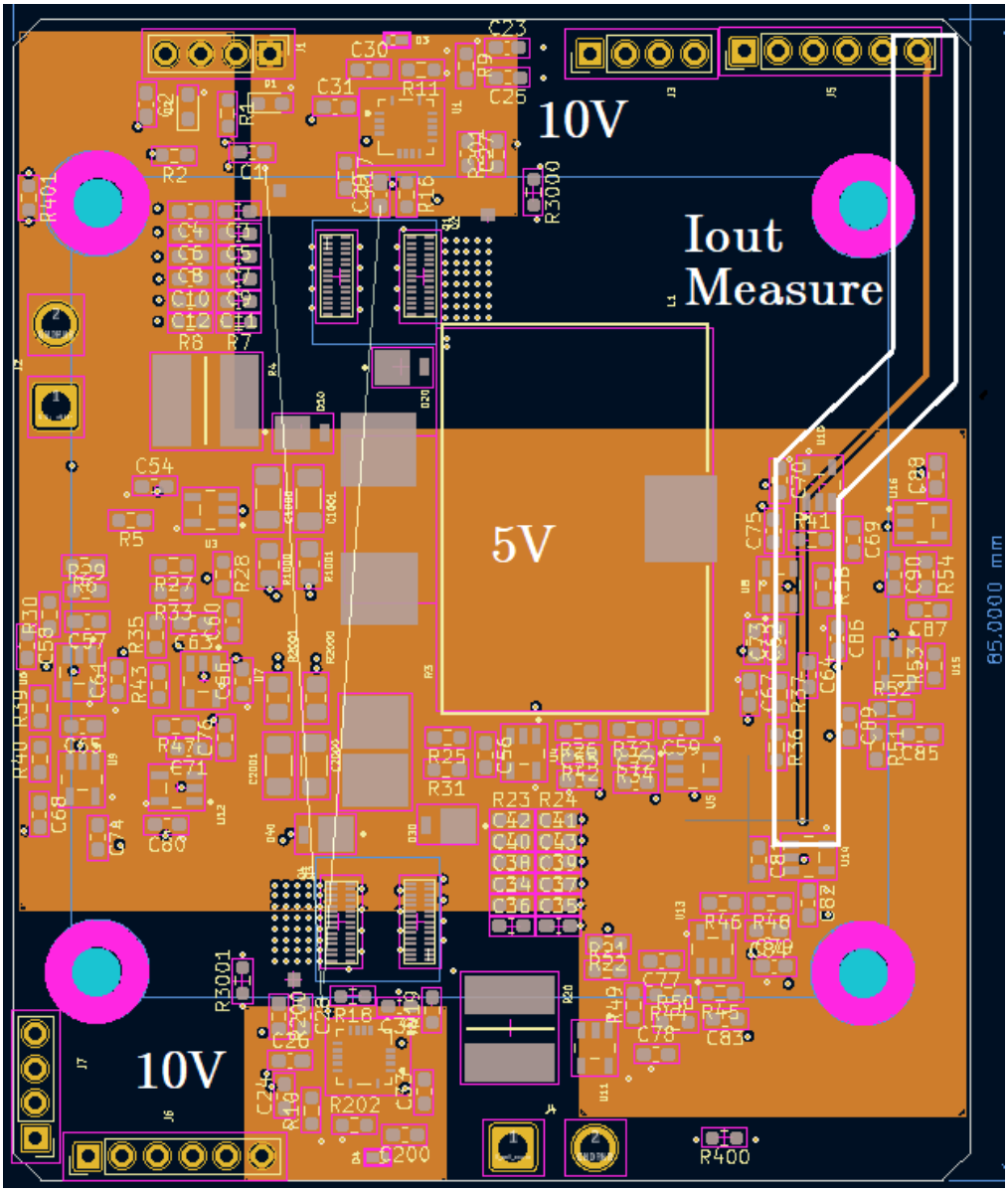


Fig 4.15 Second Inner Layer of Power Plane

Bottom Layer

Most of the bottom layer as it can be seen in fig 4.16 is occupied by the Analog Ground GNDA. Three copper planes have been placed under the front copper areas of GNDPWR, Switching Node Voltage and the area in series with the shunt resistor in order to provide better heat dissipation.

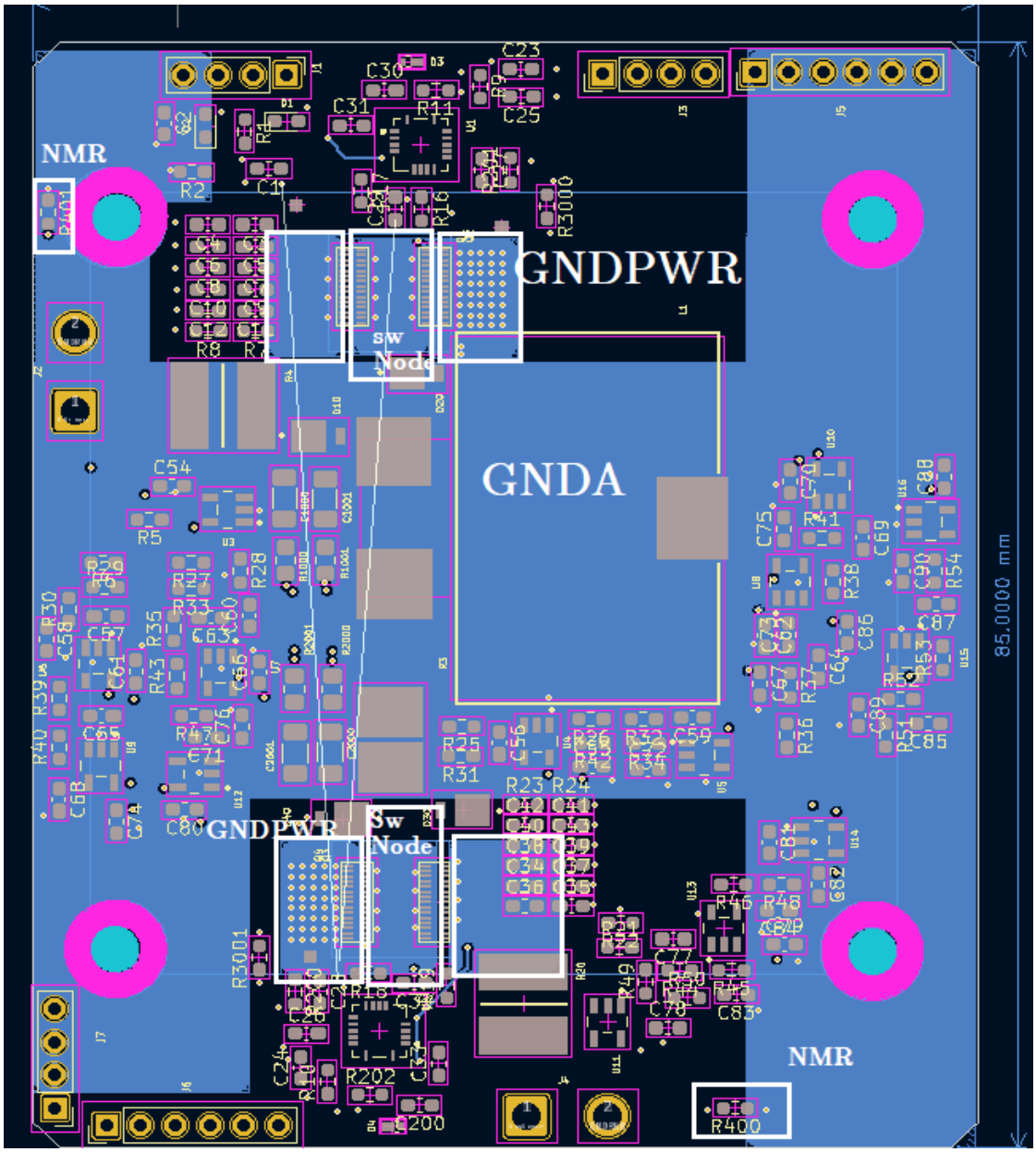


Fig 4.16 Bottom Plane of Power Plane

3D Rendering

The Top view of the Top Layer of the KiCad 3D rendering is shown in the figure below, while the Top view of the Bottom Layer in Fig 4.17

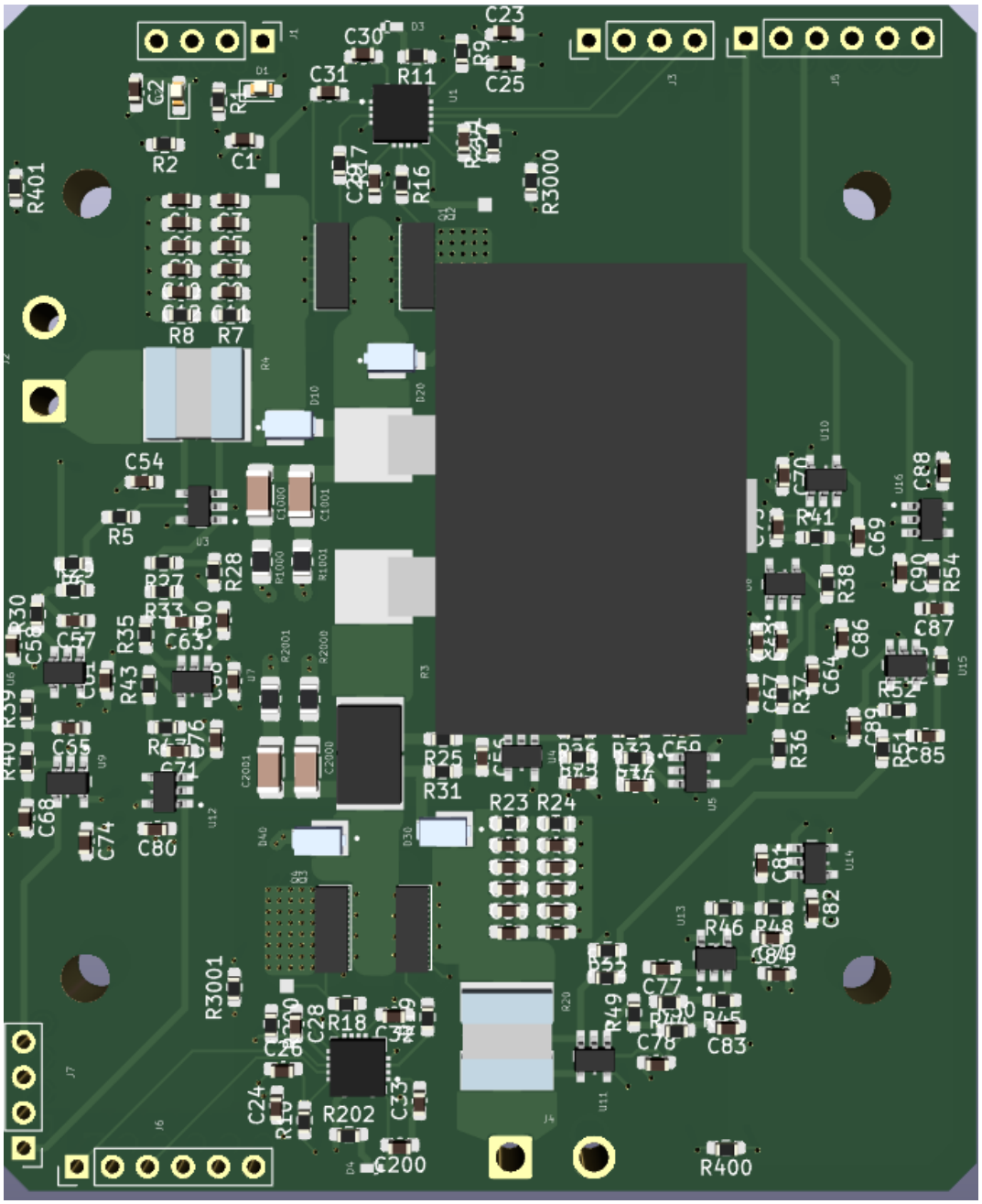


Fig 4.17 Top View of Top Layer Power Plane

Fig 4.18 Top View of the Bottom Plane

Furthermore, the two side 3D view are shown in the figures below for completeness.

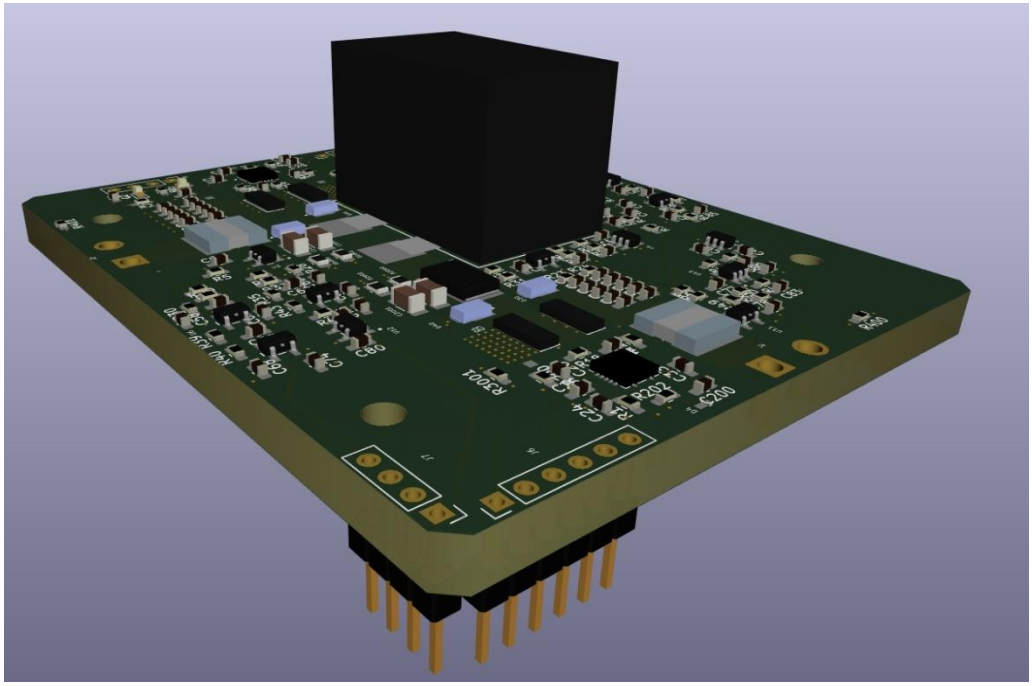


Fig 4.19 Right Side 3D View of Power Plane

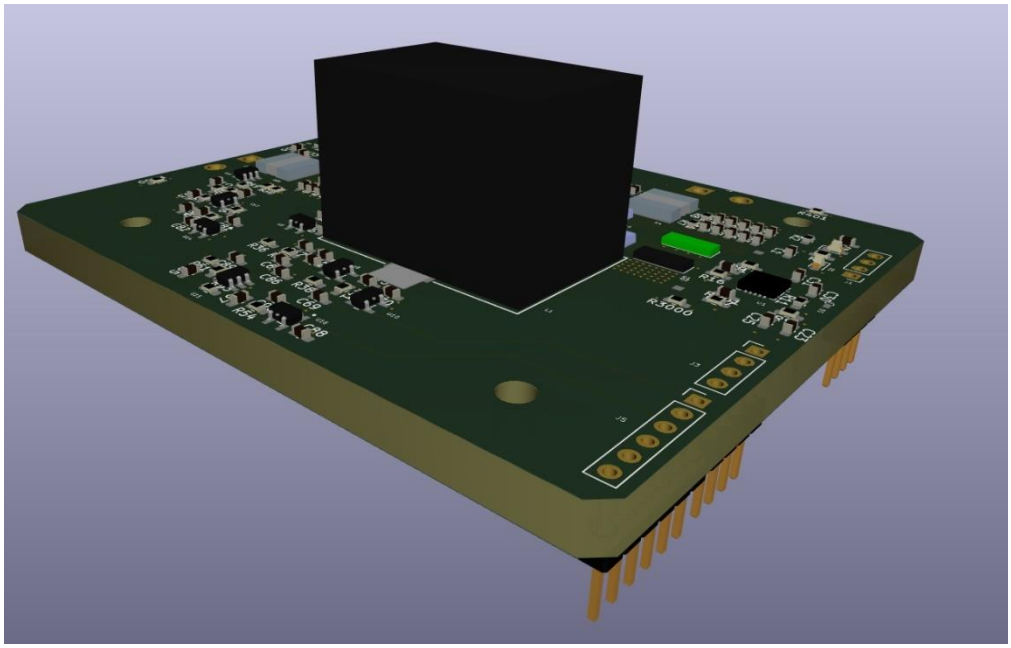


Fig 4.20 Left Side 3D view of Power Plane

Then, the circuit was printed according to the Eurocircuits PCB standards. In the following figures below different perspectives of the circuit are shown.

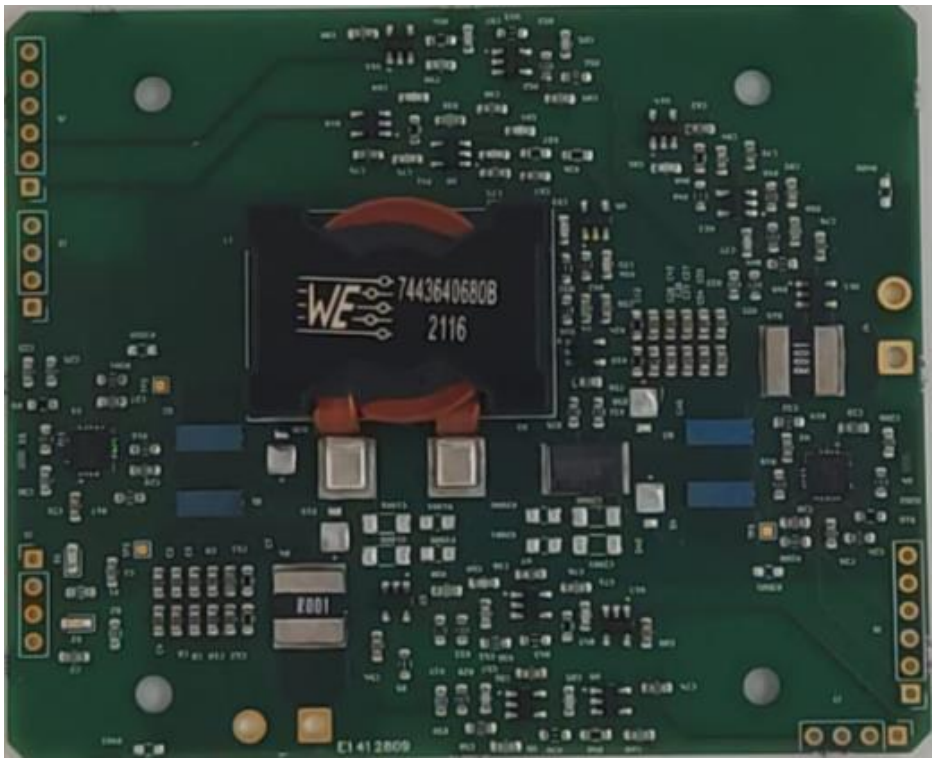


Fig 4.21 Top View of Power Plane

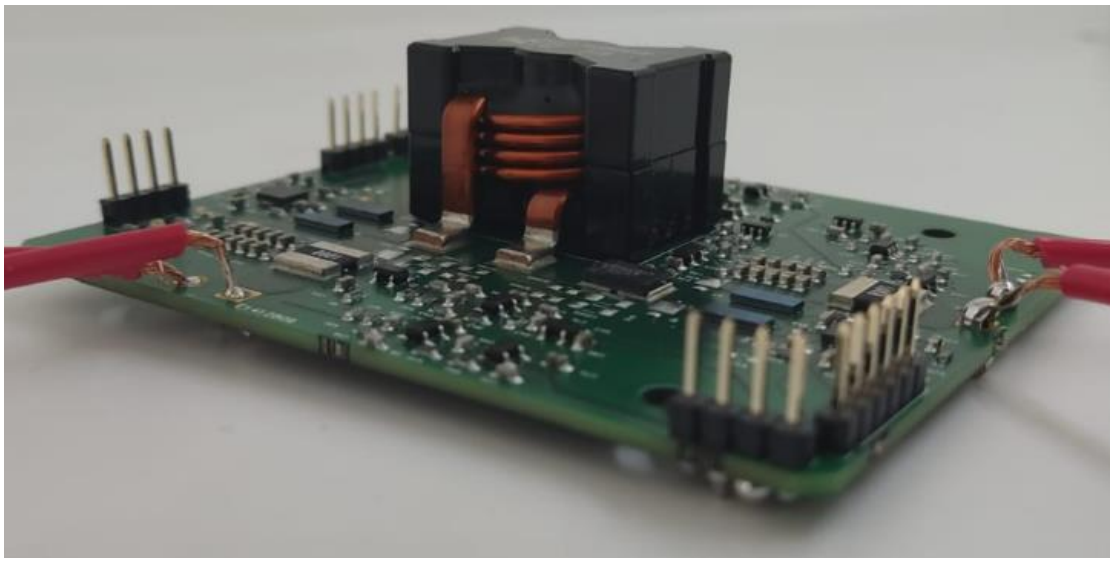


Fig 4.22 Another view of Power Plane

4.3 Logic Board Design

In fig 4.23 is shown the high level design and optimal placement of the logic board.

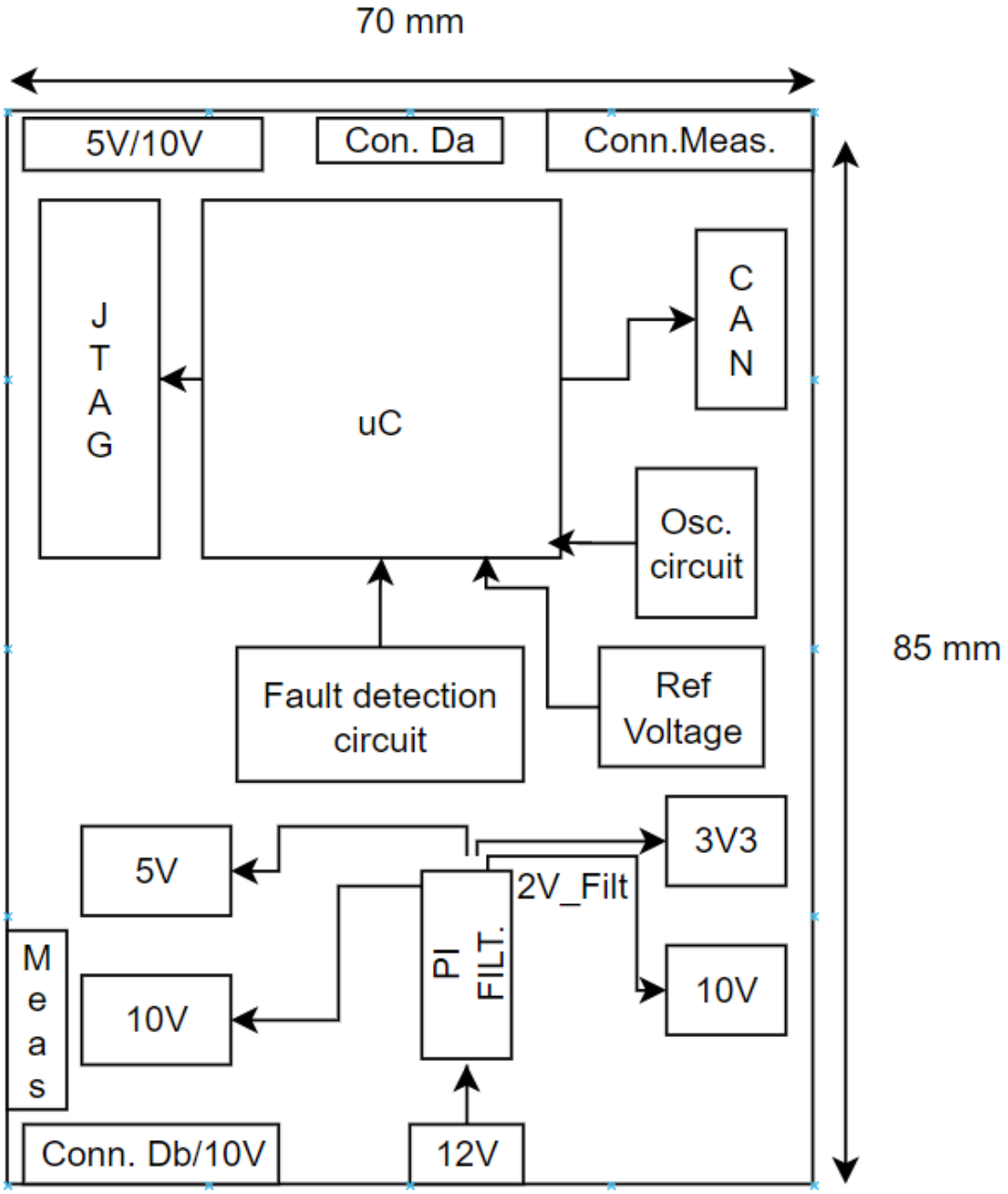


Fig 4.23 High Level Design Playout of Logic Board

4 Layers have been used:

5) Top Layer (RED) : Used for GNDD. Only few components are placed here
6) Bottom Layer(BLUE): All the major components are placed here, like uC, power supplies and fault circuitry.
7) Internal Layer 1 (GREEN): Used for GNDA and some tracks.
8) Internal Layer 2 (ORANGE) : Used for 1.2V,5V and 3.3V

For what regards the settings requirement in the power plane, these dimension have been used:

5) 0.2 mm track for Drivers and uC signals
6) 0.8 mm for power supplies tracks to meet current and thermal requirements
7) Board Minimum Clearance : 0.1 mm (used to meet the requirements for the Driver and uC)
8) Via size : 0.475mm Via Hole: 0.35mm

In fig 4.24 the whole disposition of the layer is shown

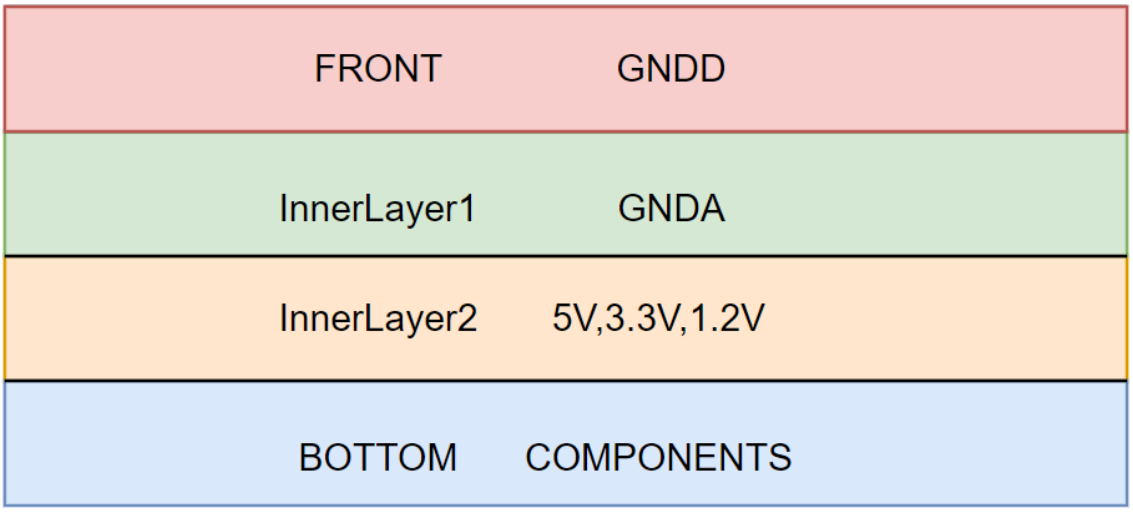


Fig 4.24 Use of the 4 layers in the Logic Board

Bottom Layer

In the figure below the Bottom Layer of the logic board is shown.

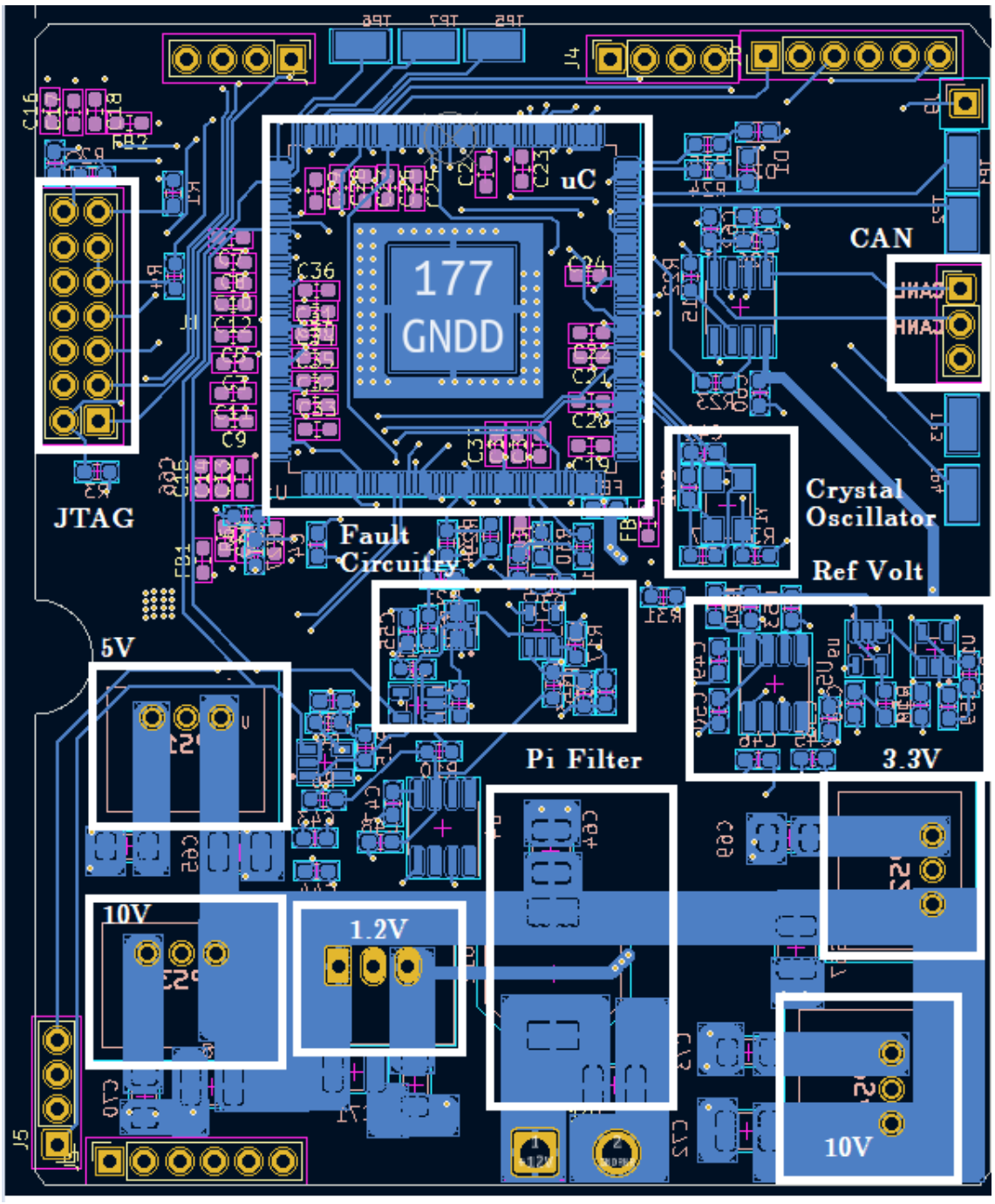


Fig 4.25 Bottom Layer of Logic Board

Starting from the lowest section of the layout(Fig 4.26) , as expected, there are all the power supplies used to supply the microcontroller(1.2V and 3.3V) as well as the opamps (5V) and the drivers (10V).
To ensure a further reduction in the ripple a PI filter has been previously designed

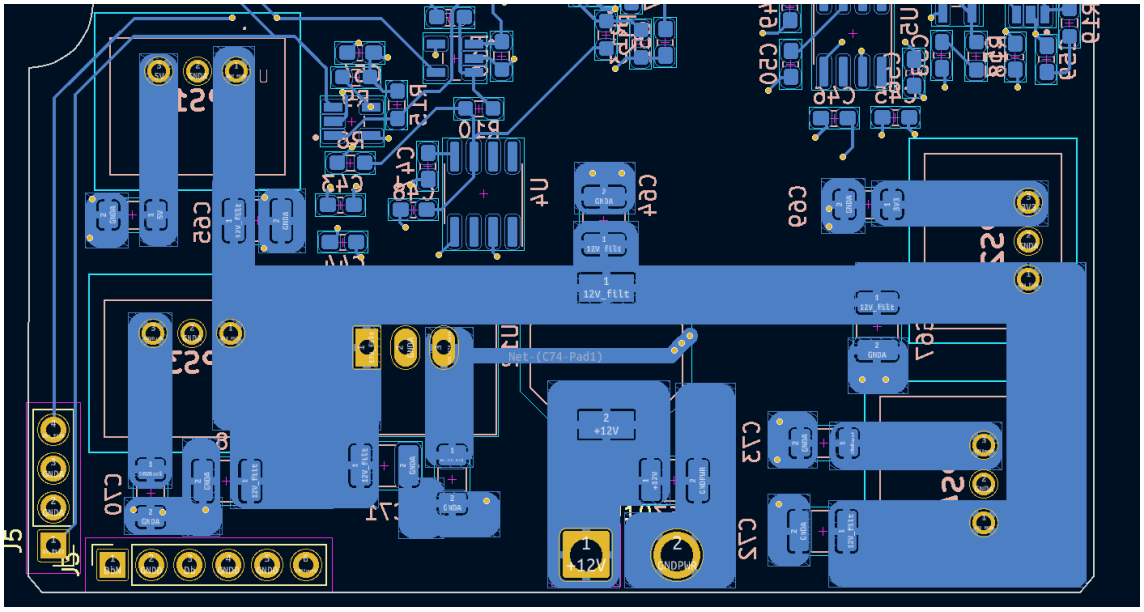


Fig 4.26 Lowest section of the Bottom plane of Logic Board

Moving to right-upwards (fig 4.27) it is clear that the Crystal Oscillator Circuits as well as the CaN interface circuit are placed as near as possible to the uC to optimize performance

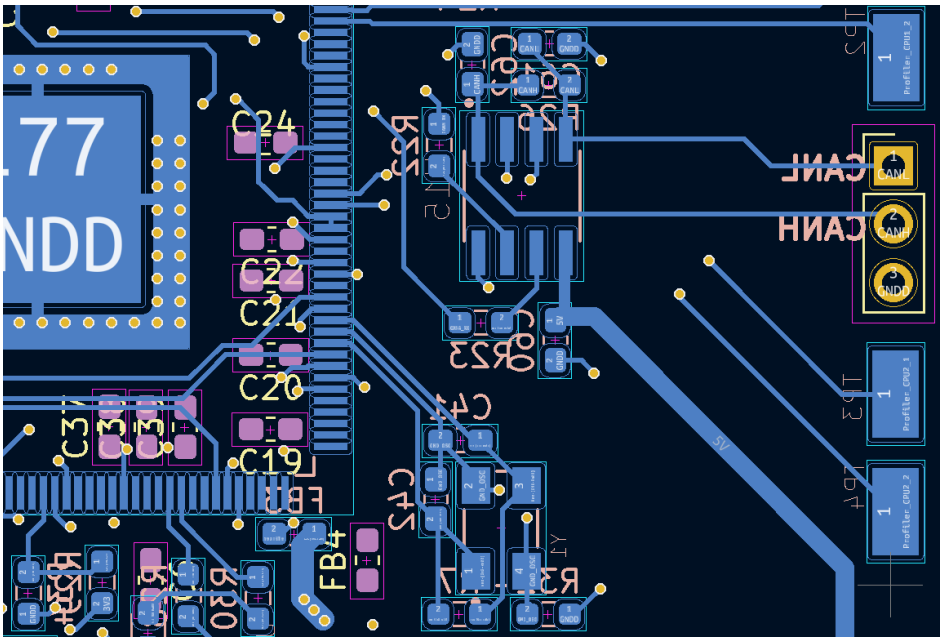


Fig 4.27 Top-Right Section of the Bottom Plane of Logic Board

Inner Layer 2

In the figure below the layer used for the power supplies areas is shown. The are two filtered supplies, which are the 1.2VFilt and the 3.3VFilt, so called because they have been filtered by another PI filter formed with the ferrite beards and some bypass capacitors. This ensures a further reduction in the ripple and greater stability in the supply of the microcontroller itself.

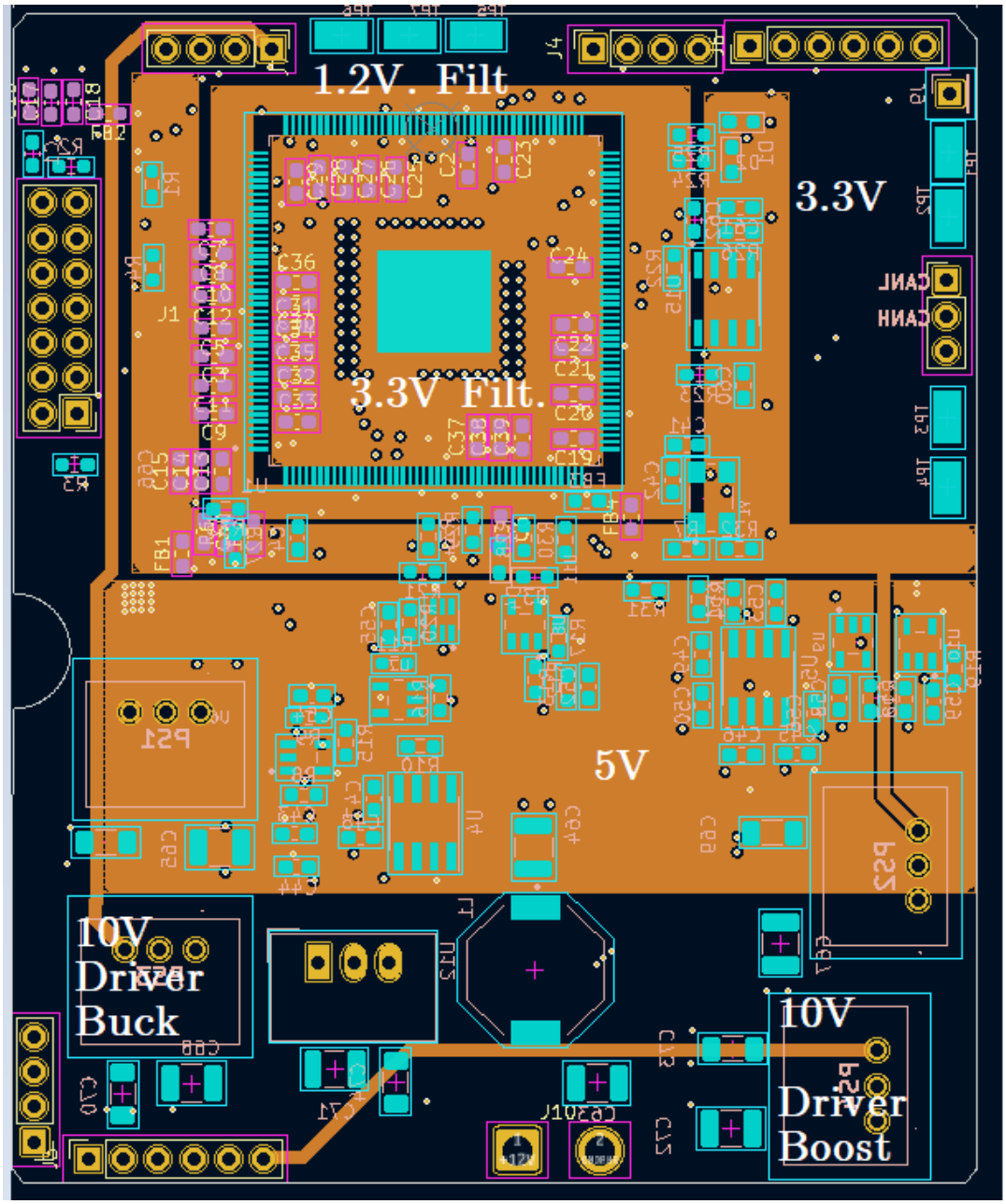


Fig 4.28 Inner Layer 2 of Logic Board

Inner Layer 1

In the figure below the layer used for the GNDA is shown. Particular attention has been made for the driver tracks. Since the driver signals can even arrive at half MHz, it is necessary to have the same length of the track in order to prevent unwanted delays. The GNDA in between the tracks is useful to reduce the parasitic capacitance between two parallel tracks. This technique has been exploited also for the two voltage reference tracks, since they must be as stable as possible.

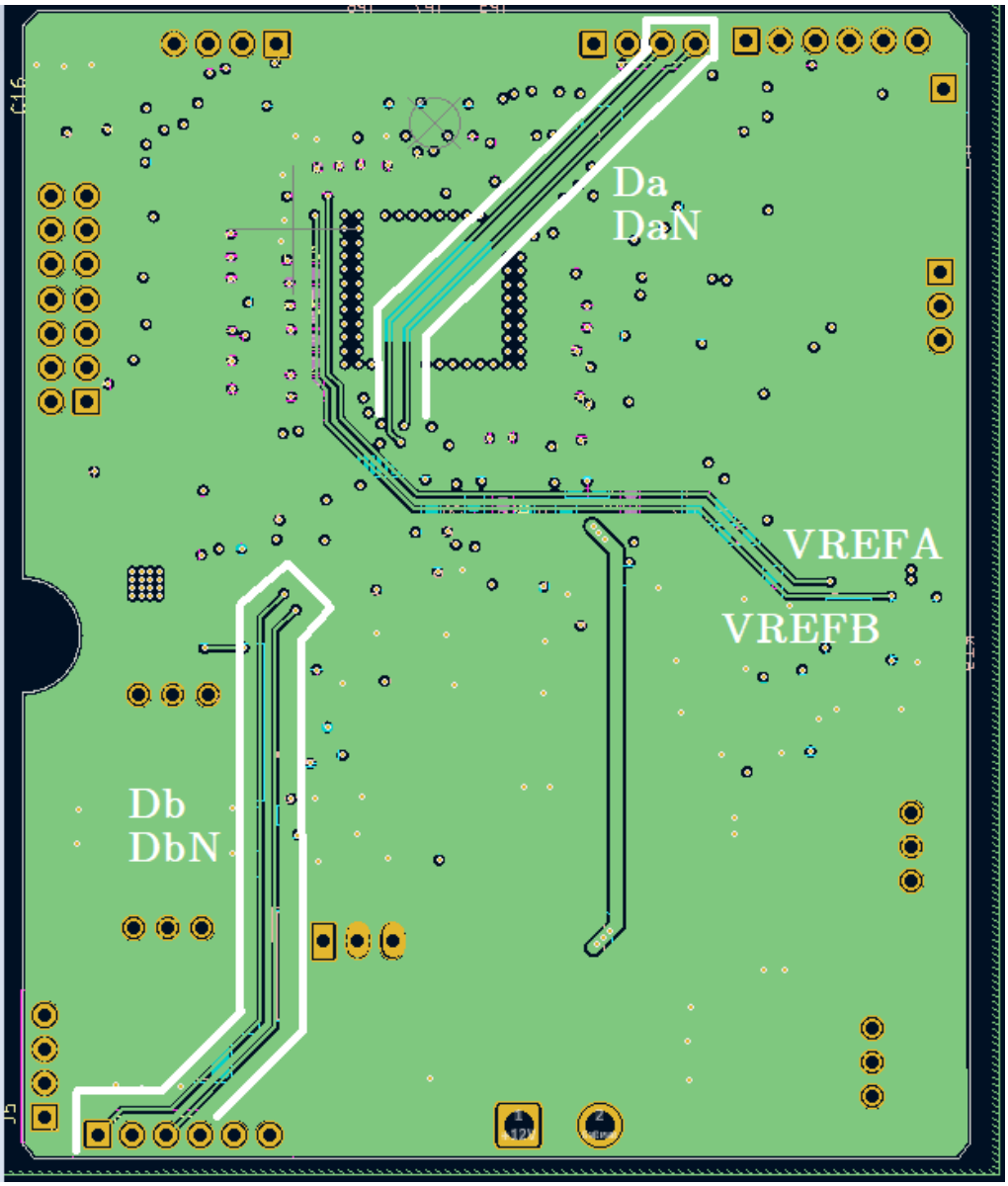


Fig 4.29 Inner Layer 1 of Logic Board

Top Layer

In the figure below the plane used mostly for the GNDD is shown. Another separate ground plane for the crystal oscillator has been used to guarantee better noise immunity. All the bypass capacitors are mostly placed here since no other components were placed.

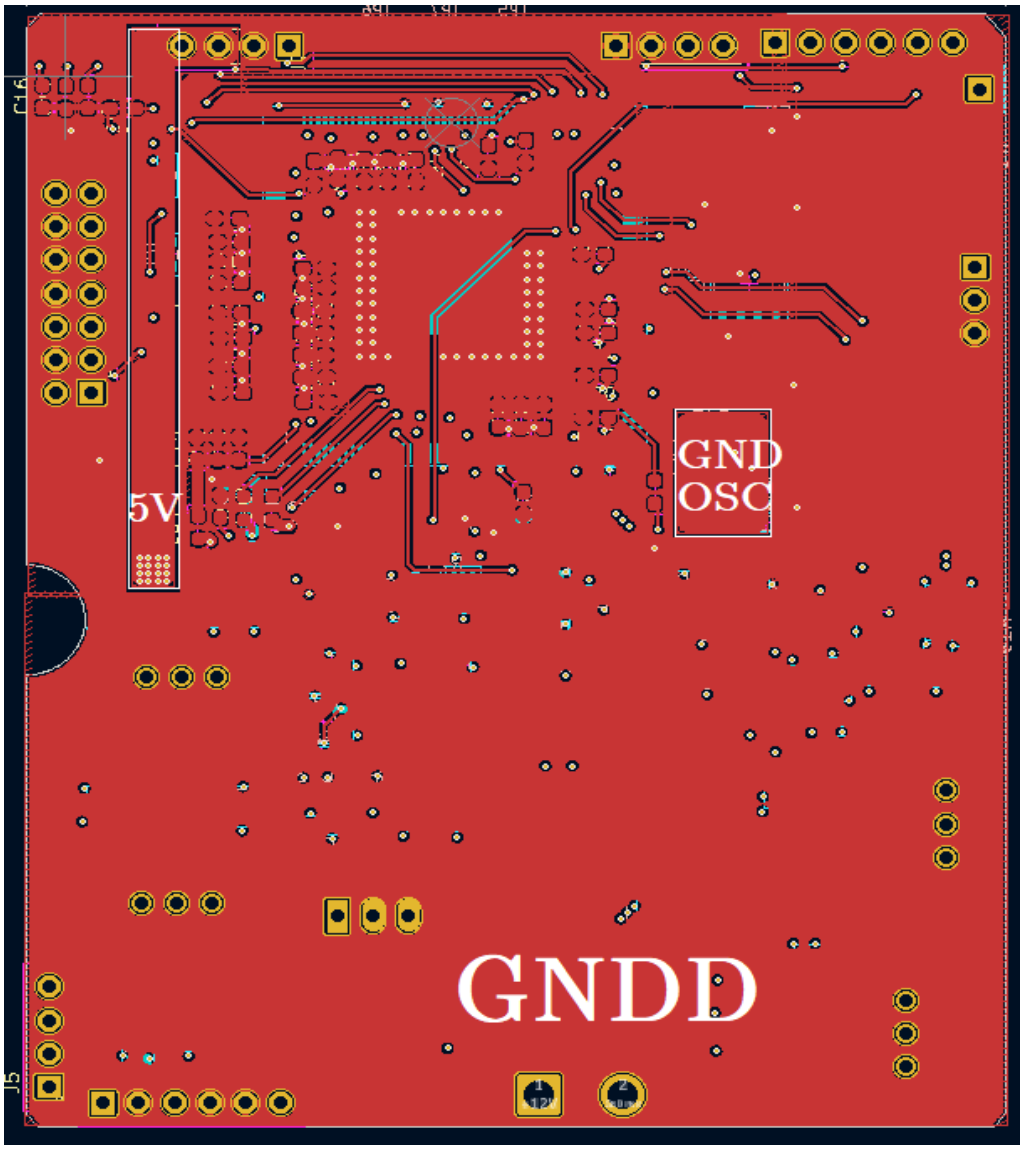


Fig 4.30 Top Layer of Logic Board

3D Rendering

In the figure below it is shown the Top view of the Top Layer, while in fig 4.31 it is shown the top view of the bottom layer.

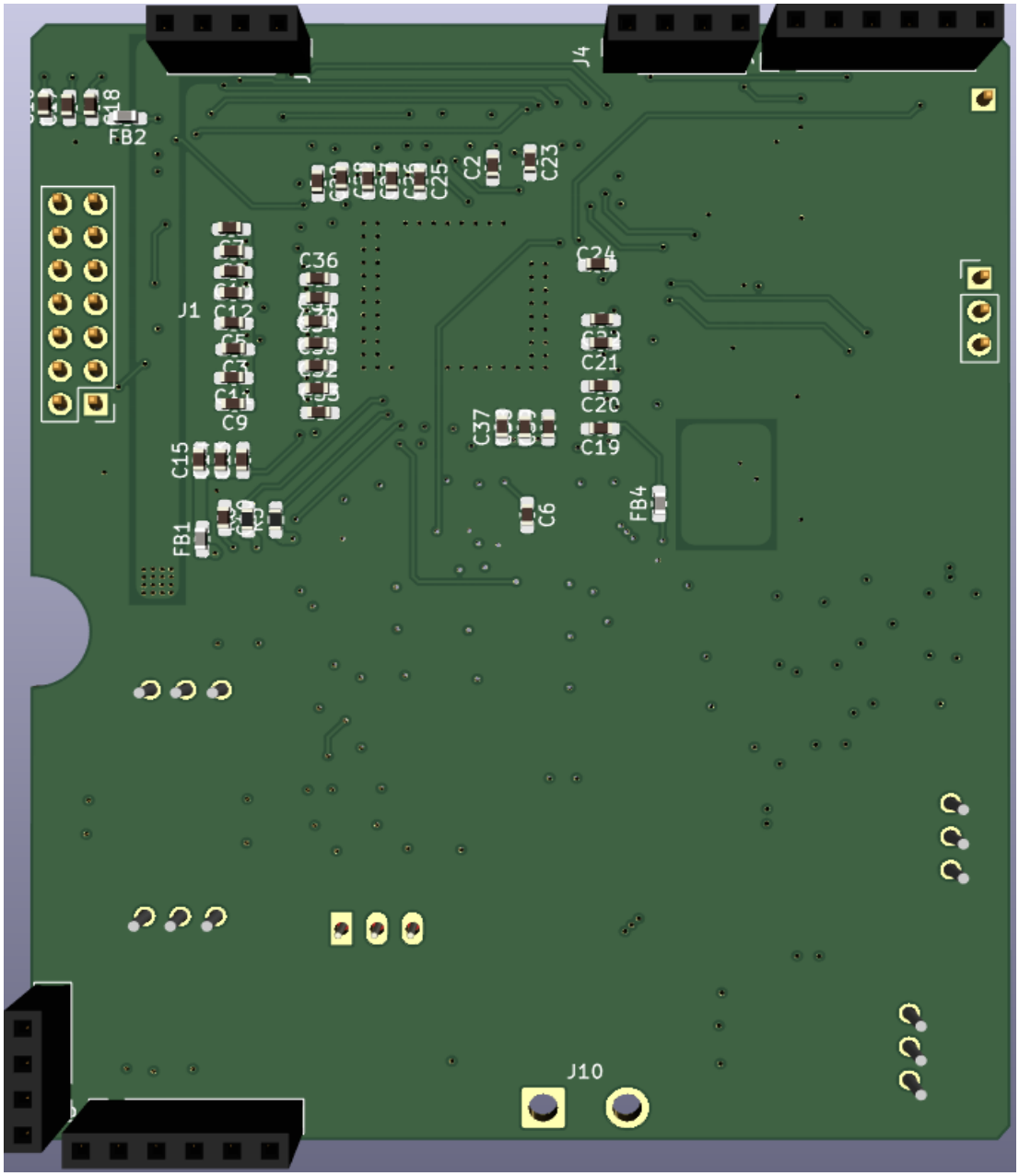


Fig 4.31 Top view of Top Layer, Logic Board

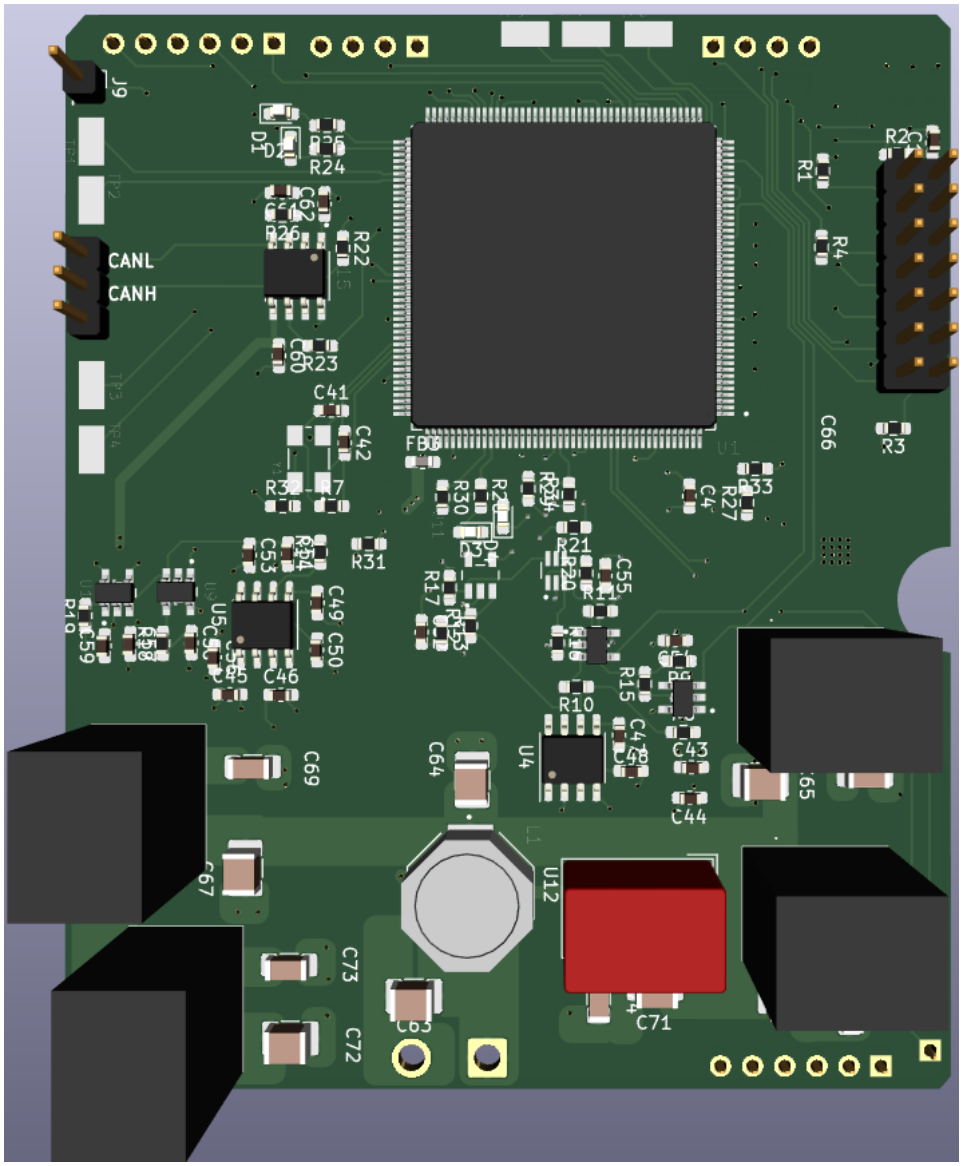


Fig 4.32 Top 3D view of Bottom Layer, Logic Board

Furthermore, there are shown two figures in isometric axonometry in fig 4.33 and 4.34 . The first enhances the microcontroller, the latter the power supplies.

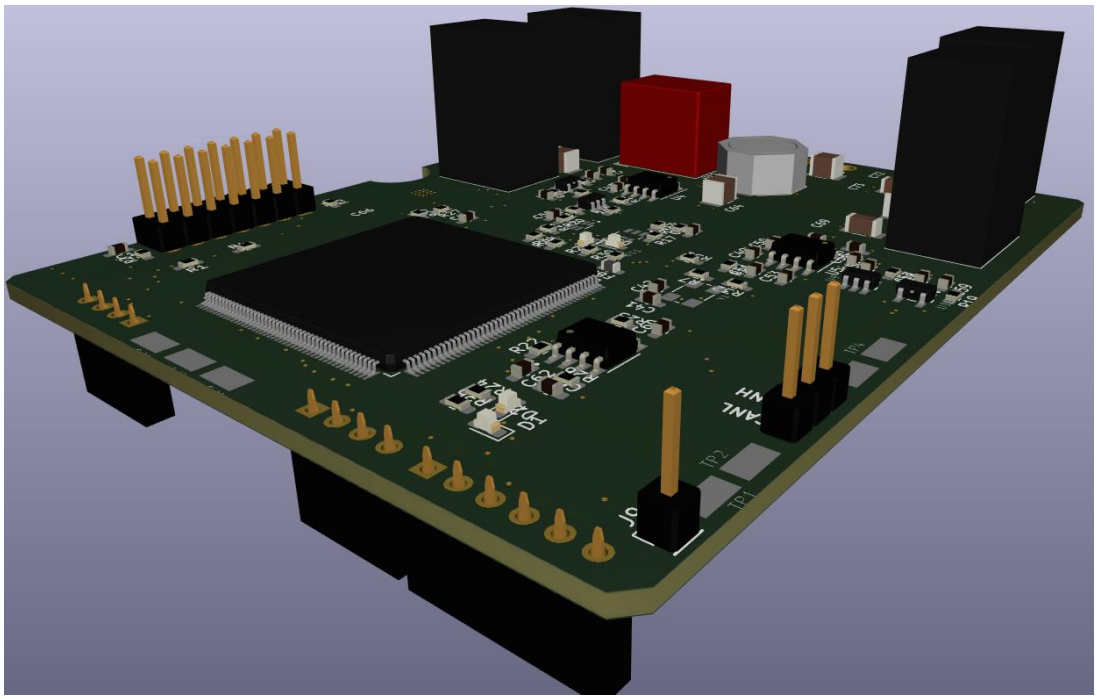


Fig 4.33 First axonometry of Bottom Plane, Logic Board

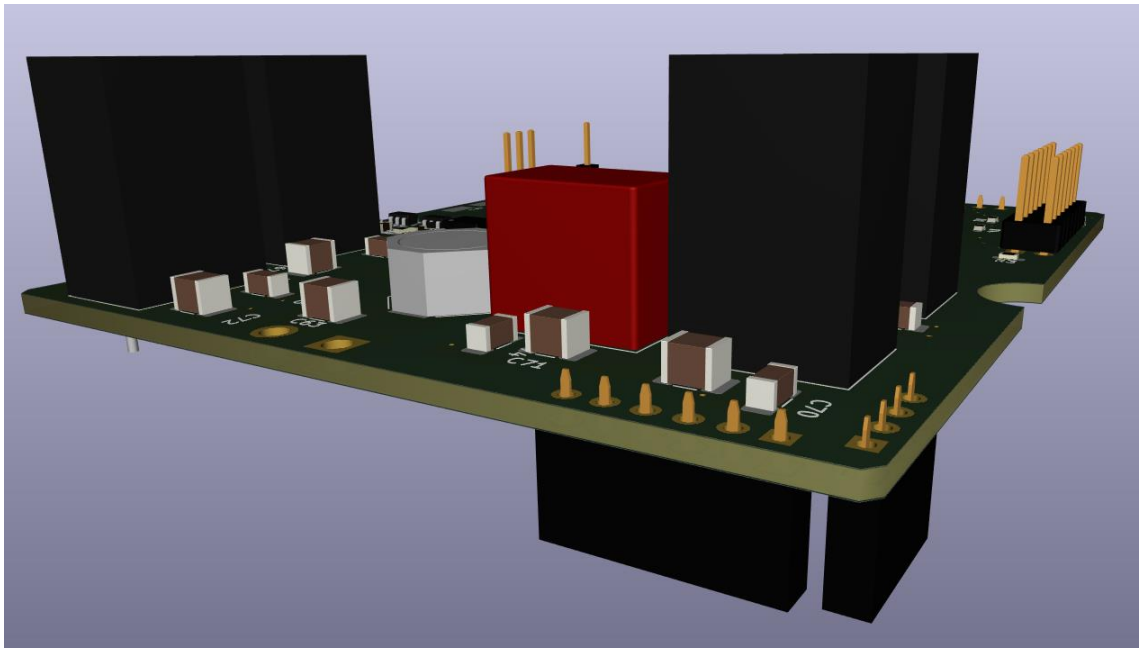


Fig 4.34 Second axonometry of Bottom Plane, Logic Board

Finally, using Autodesk Fusion 360, by exporting the .step files from KiCad, it is possible to join the two circuits (fig 4.35) to have a complete view of the project.

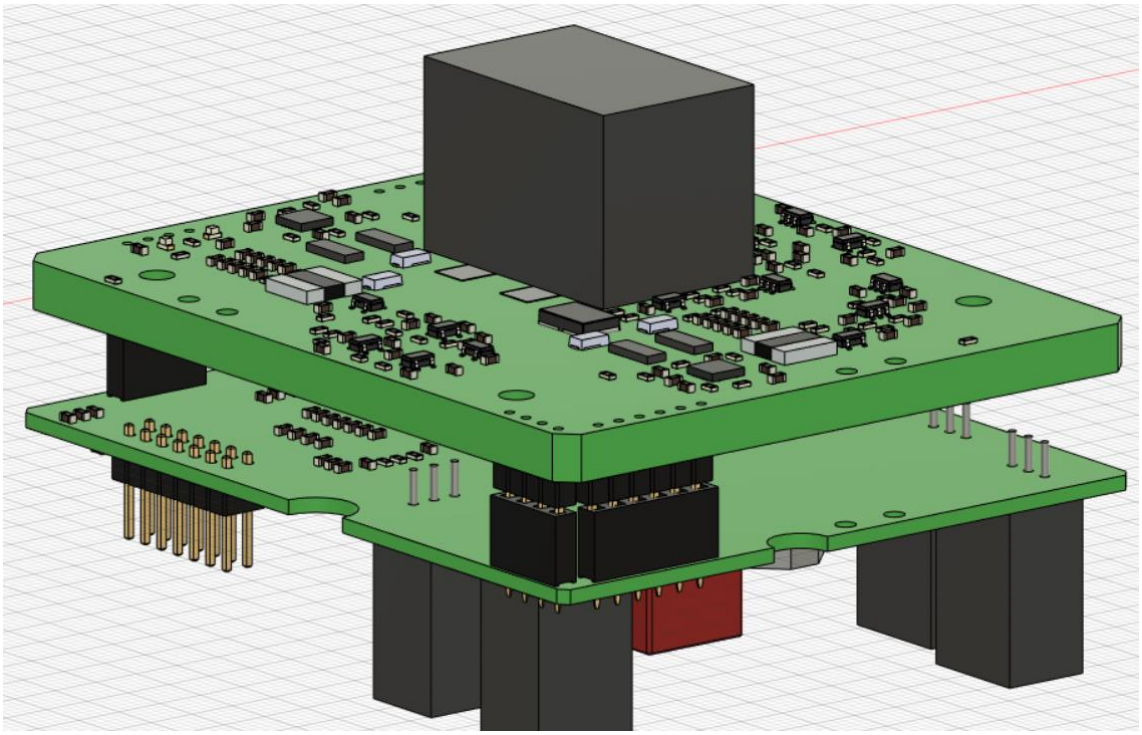


Fig 4.35 Complete Nibb (Power and Logic)

Chapter 5
Experimental Validation

All the testing was done in open loop, having as Vin a voltage coming from a generator and different loads for each test. The 5V supply and the supply for the drivers were coming from an external power supply.

The testing bench is shown in figure 5.1. The CPX400D from AIM-TTI Instruments, and the oscilloscope, Wavesurfer 434 from LeCroy were the two most used instruments. To generate the PWM signals to drive the circuit the F28C200X Delfino Board is employed.
The Fluke Thermal Camera has been used in order to monitor the temperature of the heat sinkers, preventing damage.

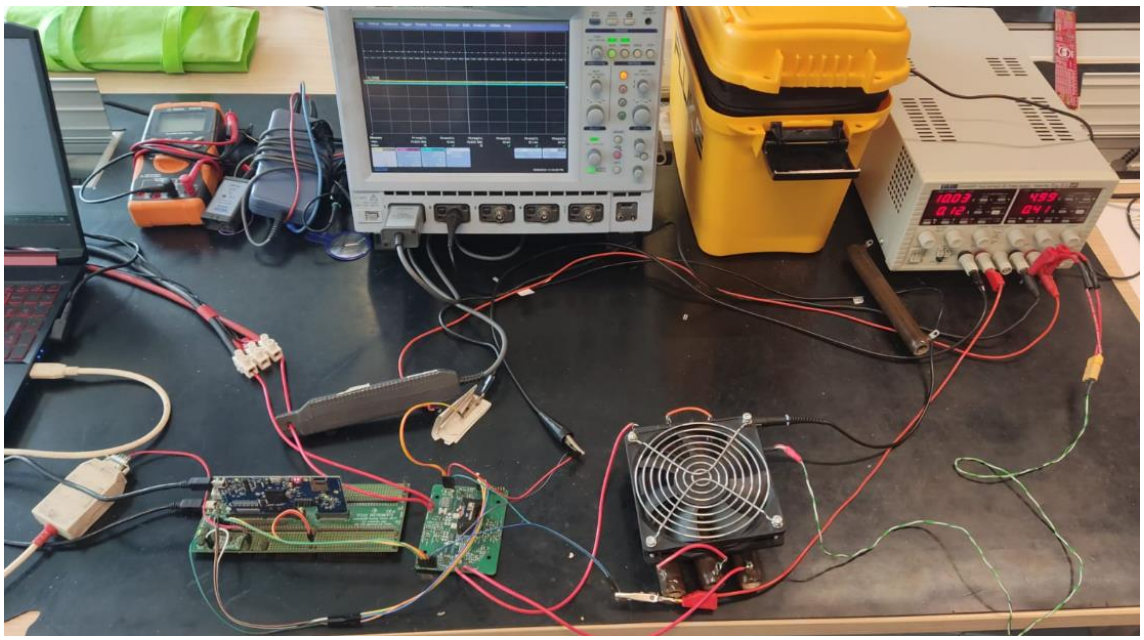


Fig 5.1 Testing Bench

5.1 Converter Waveforms

In order to drive the switches two square waves with 50ns of dead time were generated by the dual carrier control algorithm technique. In fig 5.2 there are shown the two square waves used to drive the GaNs

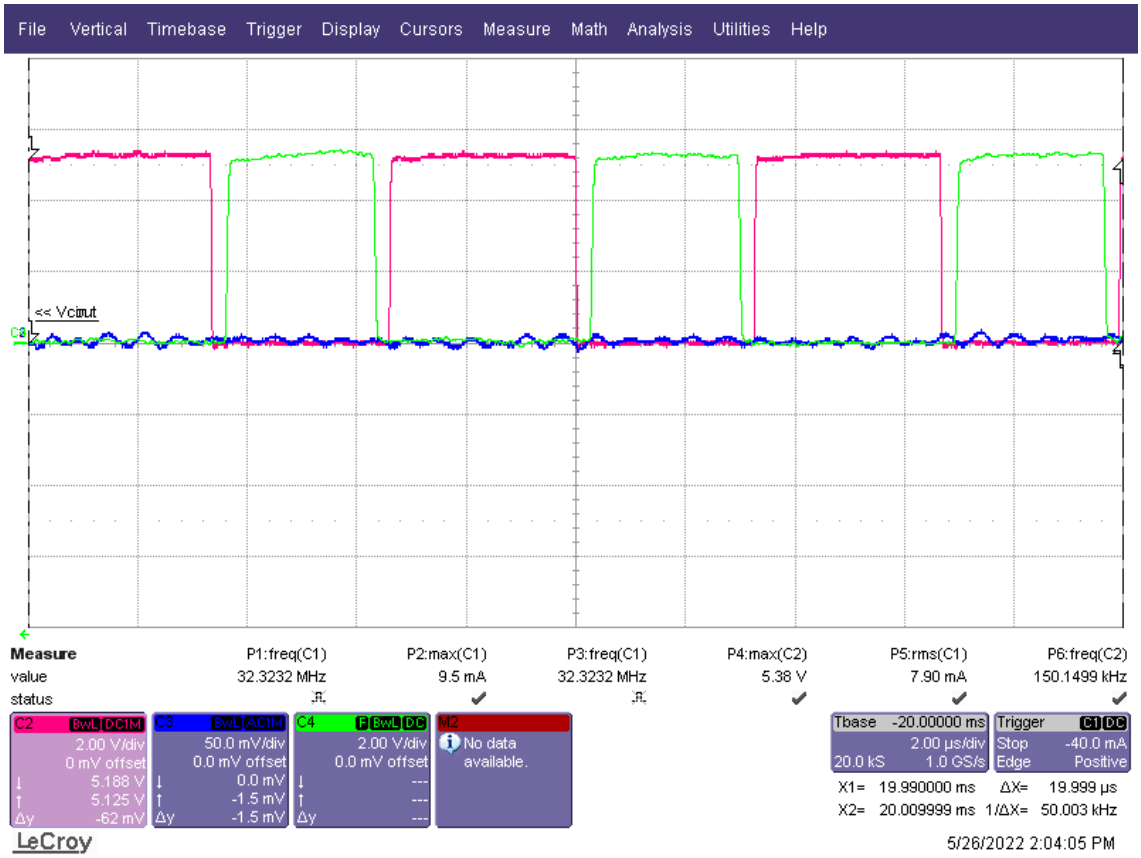


Fig 5.2 Complementary Square Waves for High and Low Side Switches

Understanding the impact of the dead time is crucial in the validation process of any dc-dc converter.
In fig 5.3 it is shown the voltage node switching waveform with excessive dead time. Compared to the LTSpice simulation, it is expected to have for the imposed dead time a bit of constant overvoltage. Hence, an excessive dead time could result in excessive dissipation and energy waste.

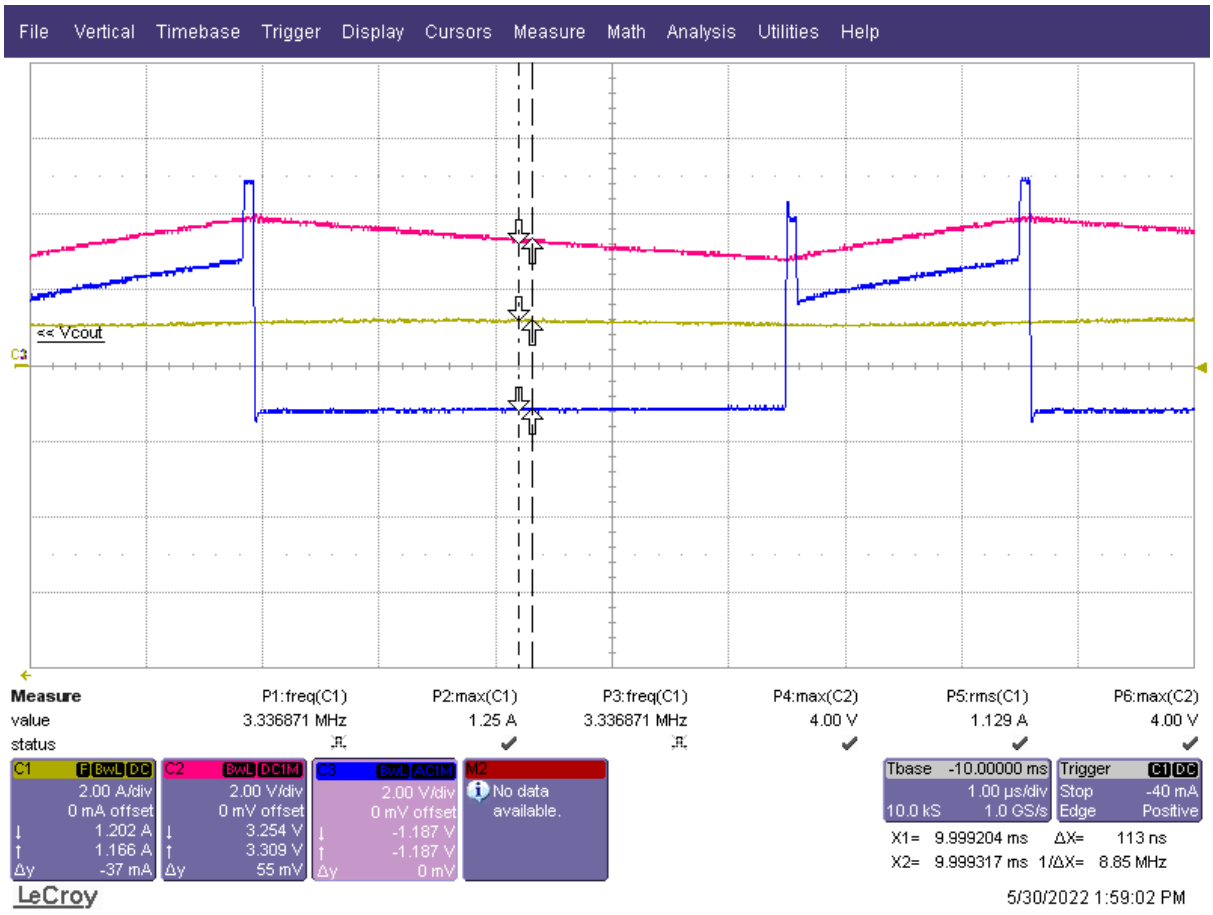


Fig 5.3 Switching Node Voltage(Blue) with Output Voltage (Red) and Output Current (Yellow)

In fig 5.4 it is showed that by putting a correct dead time, the period of time in which there is an unwanted overvoltage is greatly reduced.Hence a 50 ns of dead time was set since it didn't cause any short circuit or overcurrent problem

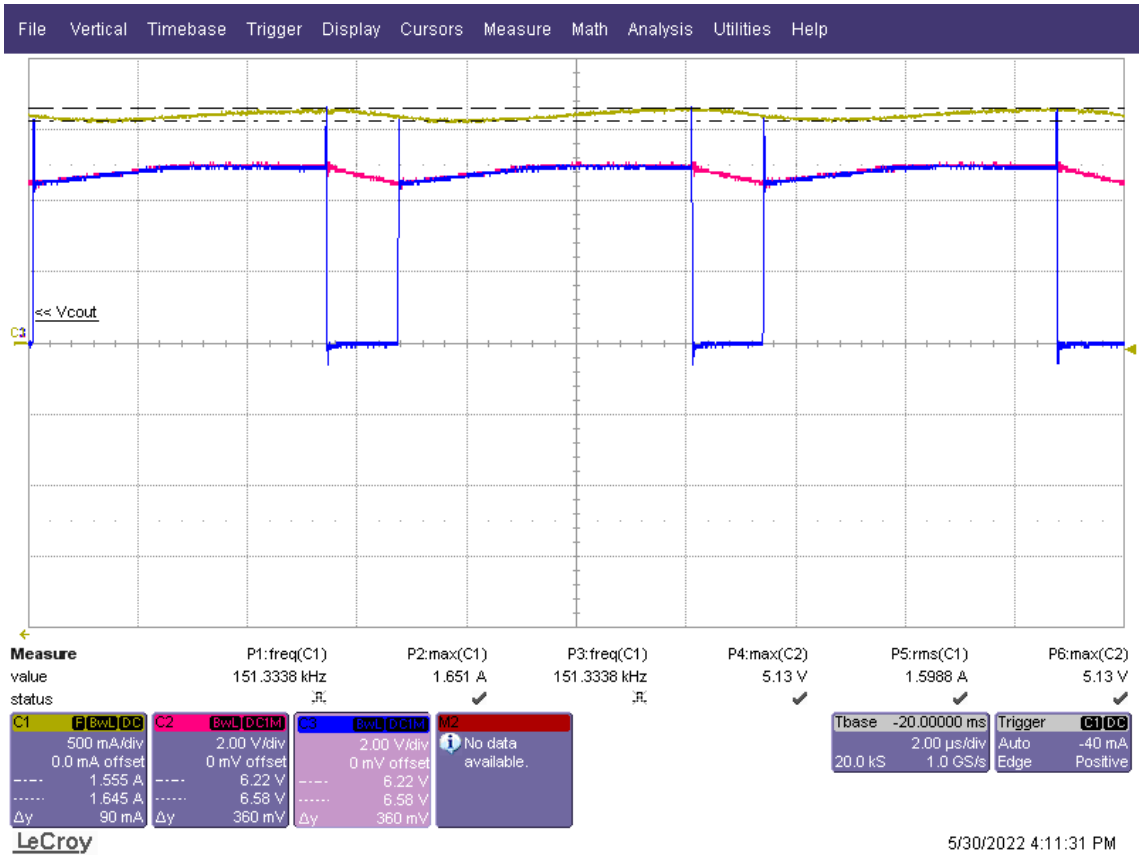


Fig 5.4 Switching Node Voltage(Blue) with Output Voltage (Red) and Output Current (Yellow) with 50ns of dead time

The Measure stage waveform were tested as well.
In fig 5.5 it is shown the input voltage measure(red), input current measure stage (yellow) and in blue the inductor current from the measure stage.
It is clear that for low voltages the fourth and sixth order Bessel filter have successfully filtered out the ripple component which causes unwanted noise.
A bit noise in the inductor waveform is seen towards the minimum value because of high dv/dt induced from the switching node voltage

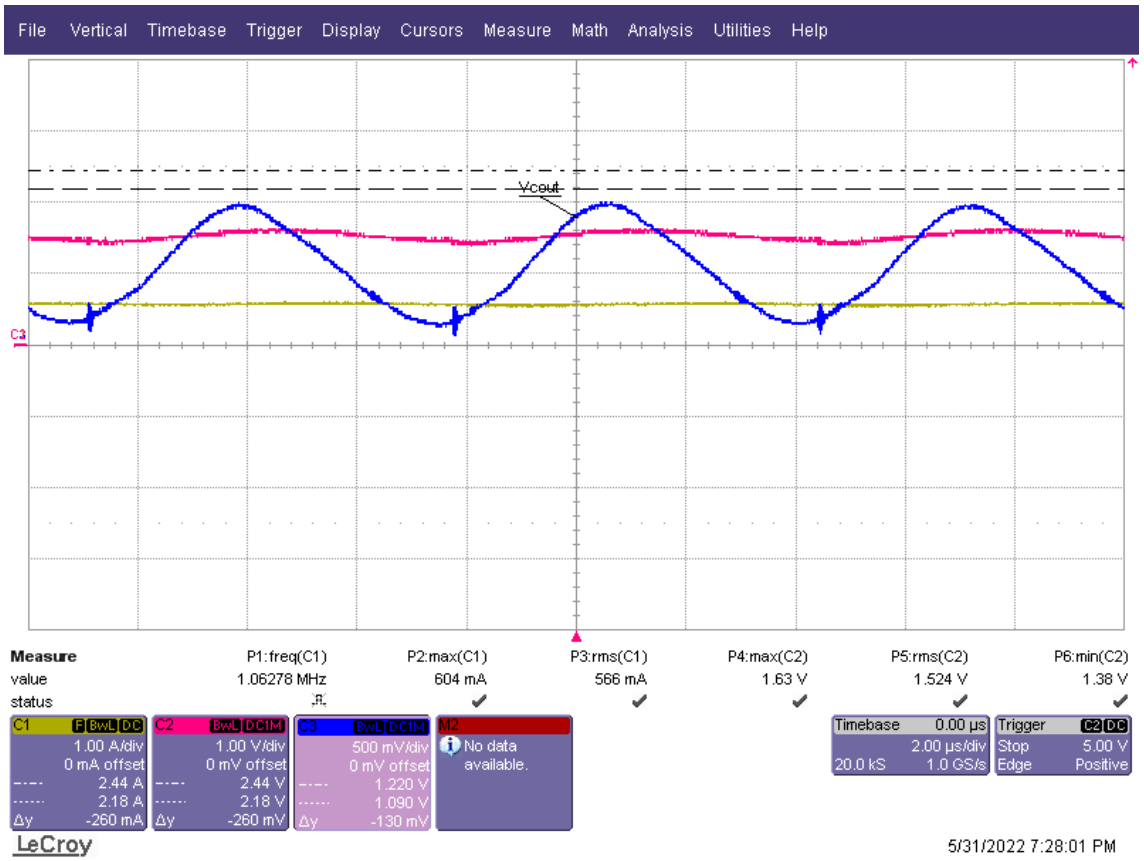


Fig 5.5 Output of the Input Voltage measure stage (red), Input current measure stage(Yellow) and Inductor Measure stage (Blue)

Finally, in fig 5.6 it is shown the output voltage and output current with 180W as input power. By setting the according options requirement in the LeCroy , it is possible to plot even the power(showed in the second plot pane).
In fig 5.7 it is shown another measure output stage, highlighting the noise components

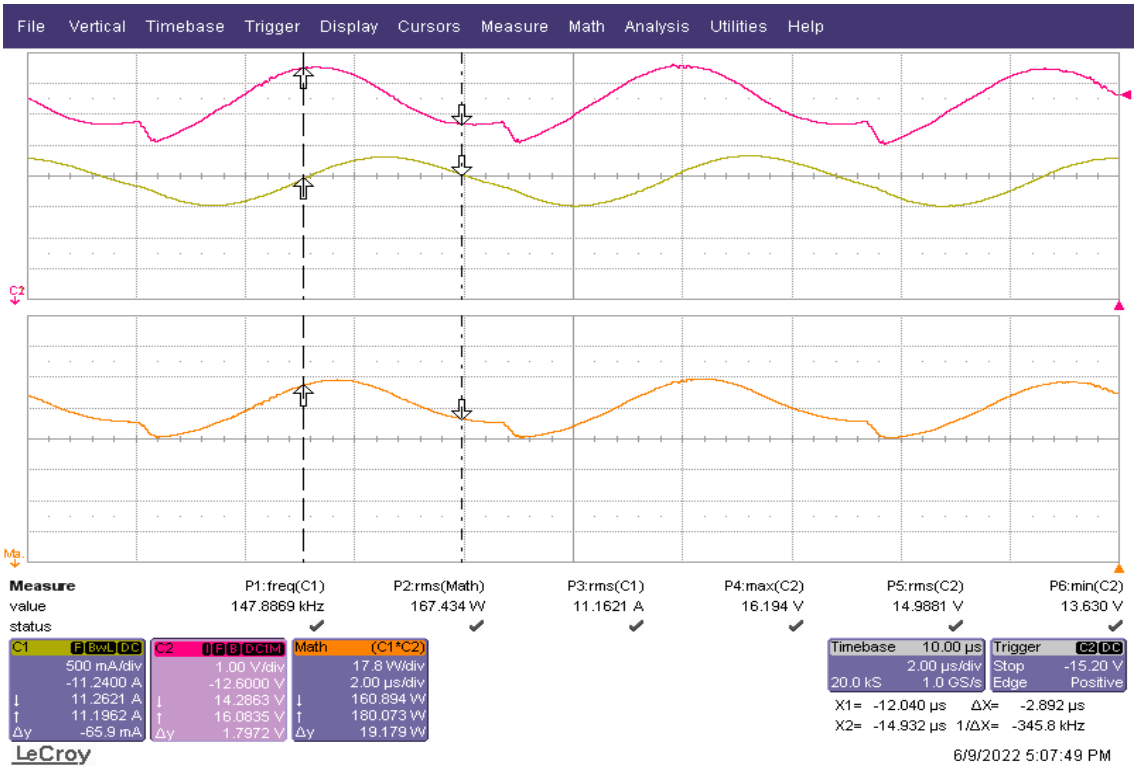


Fig 5.6 Output Current and Voltage (First plot pane, red and yellow respectively) and Power output in orange

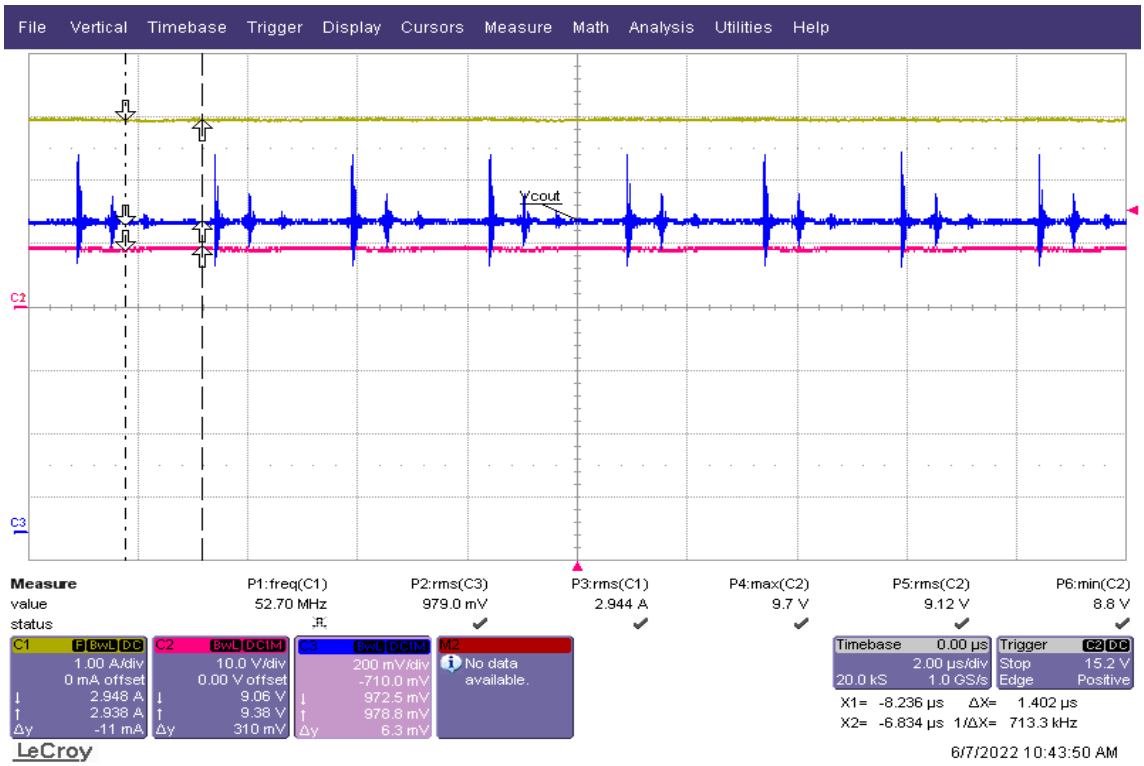


Fig 5.7 Output Voltage measure stage (In blue) enhancing noise components

5.2 Efficiency

Efficiency with constant Duty Cycle

The first test results which are shown regards the efficiency of the circuit with constant duty cycle, hence the varying the power for each working point, with a fixed load of 3Ω, all showed in fig 4.x. The experimental data can be found at Appendix A , Table A1-A2-A3 While it's difficult to understand the trend of the efficiency , since it is dependent on the input power and the duty cycle, it is clear from the plot results of the output voltage and current ripple that by increasing the switching frequency the ripple decreases.

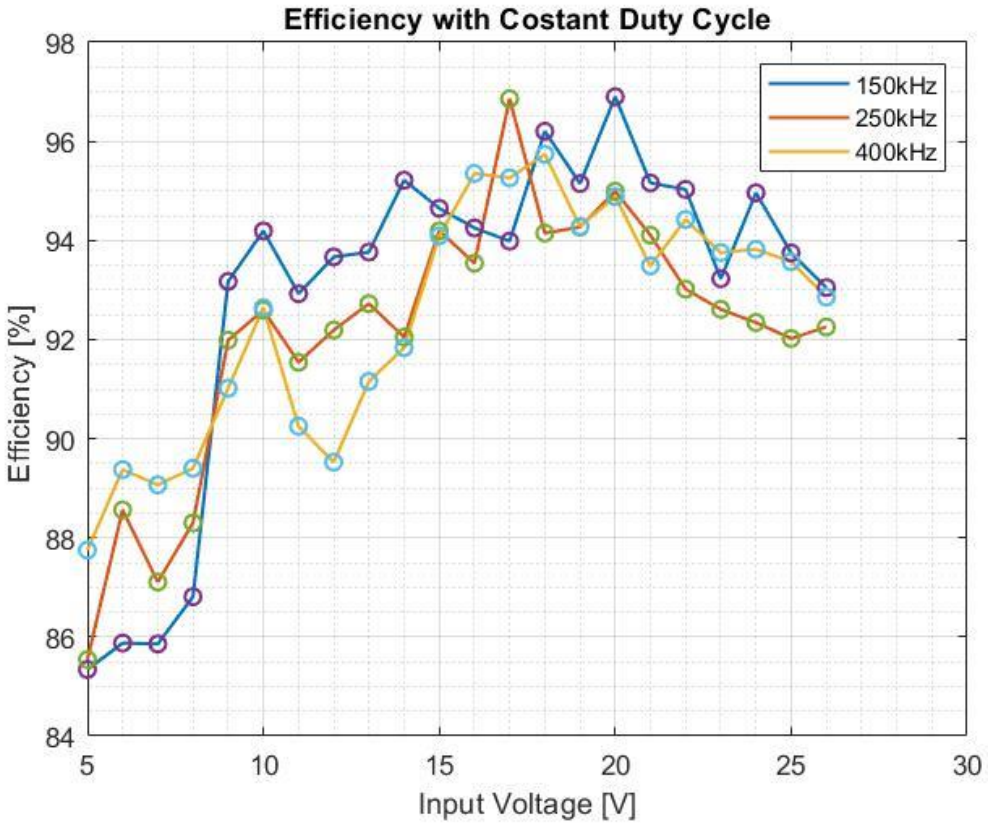


Fig 5.8 Plot Result of Efficiency at Constant Duty Cycle

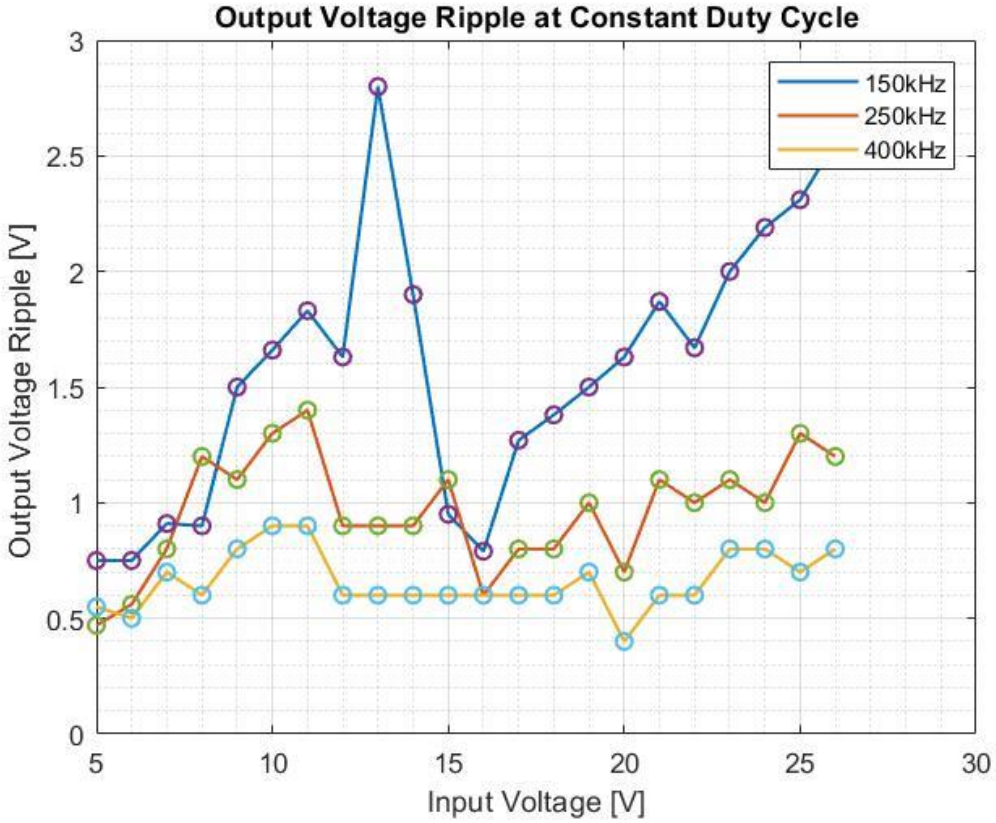


Fig 5.9 Output Voltage Ripple at Constant Duty Cycle, Varying Power

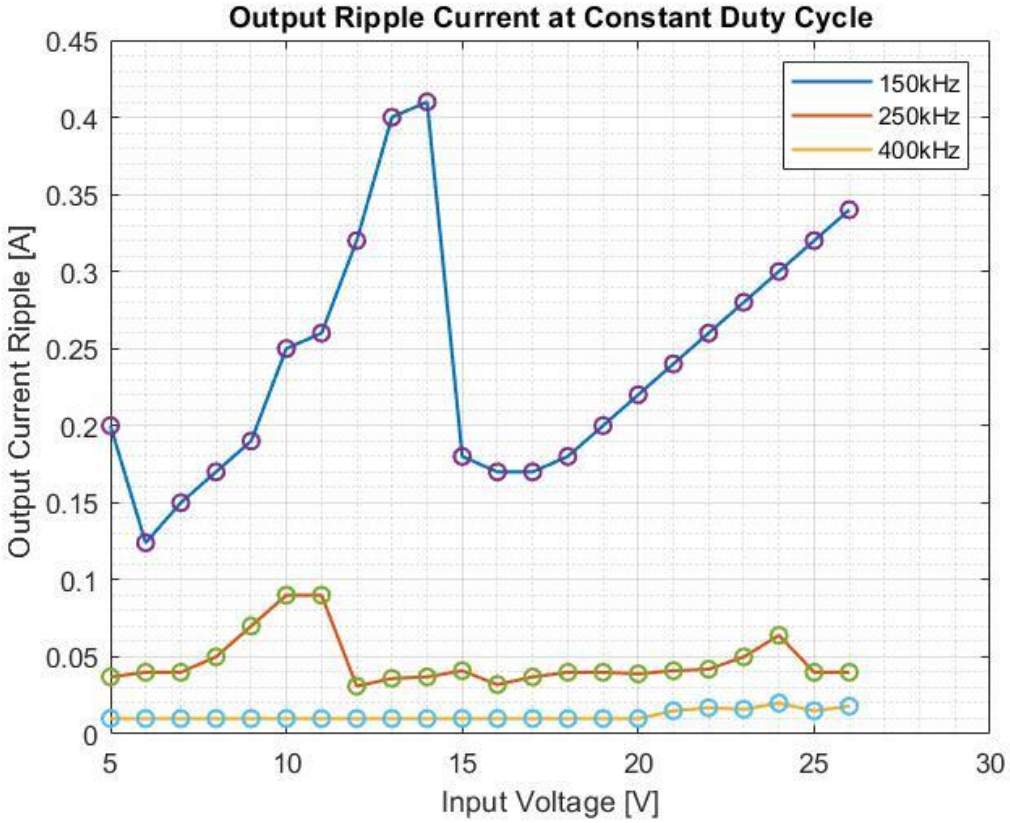


Fig 5.10 Output Current Ripple at Constant Duty Cycle, Varying Power

Since a dead time of 50ns is set for each duty cycle, we can expect a slightly different output voltage with respect the calculated one. Like shown in plot fig 5.11 this effect is far more evident as the frequency increases.
This implies that the same dead time has different impact on the output voltage based also on the switching frequency used.

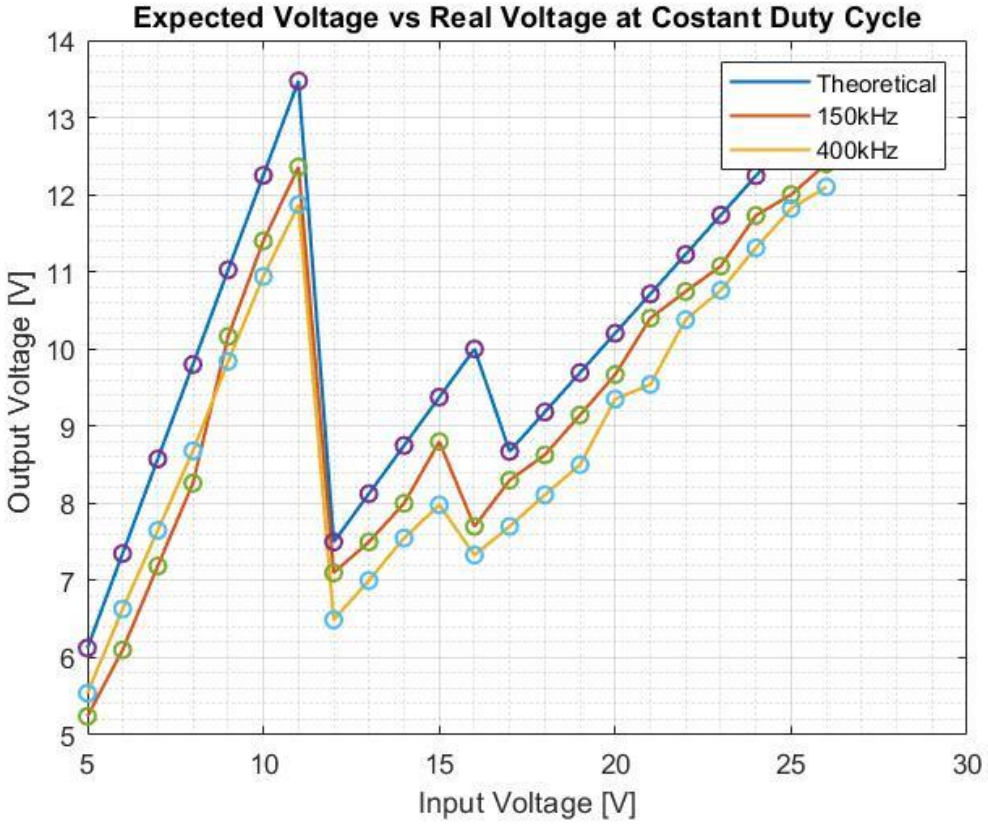


Fig 5.11 Expected Output Voltage vs Real Output Voltage

Hence the meaning of the plot in fig 4.x is that not every output voltage can be reached with only the buck mode or the boost mode at the given frequency owing to the dead time. This is more evident in the 180W Constant Power, Fixed 15V Output Voltage test, where from 16V at 400kHz is impossible to step down to 15V.

37 W TESTING

To give meaning at the efficiency plot, it is necessary to keep the power constant by varying the duty cycle.
It is expected that the efficiency has higher value in the boost region when the input voltage is higher since the boost is less stressed and higher efficiency in the buck region when the voltage is near 15V for the same reason.
The experimental data can be found at Appendix A , Table A4-A5-A6
The power is fixed around 37W, with 15V as fixed output voltage, 6Ω load and 2.5A as output current flowing in the load.
The efficiency plot with constant power is hence showed in fig 5.12 while the output current ripple and the output voltage ripple in fig 5.13 and 5.14

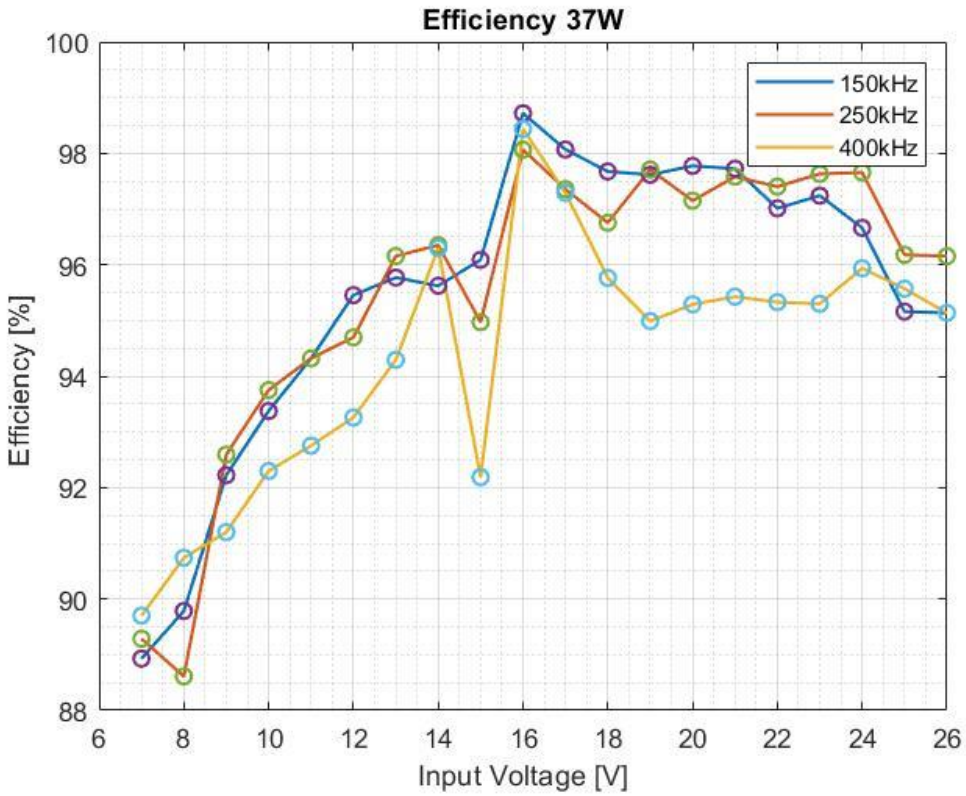


Fig 5.12 Efficiency Trend at 37W for different switching frequencies

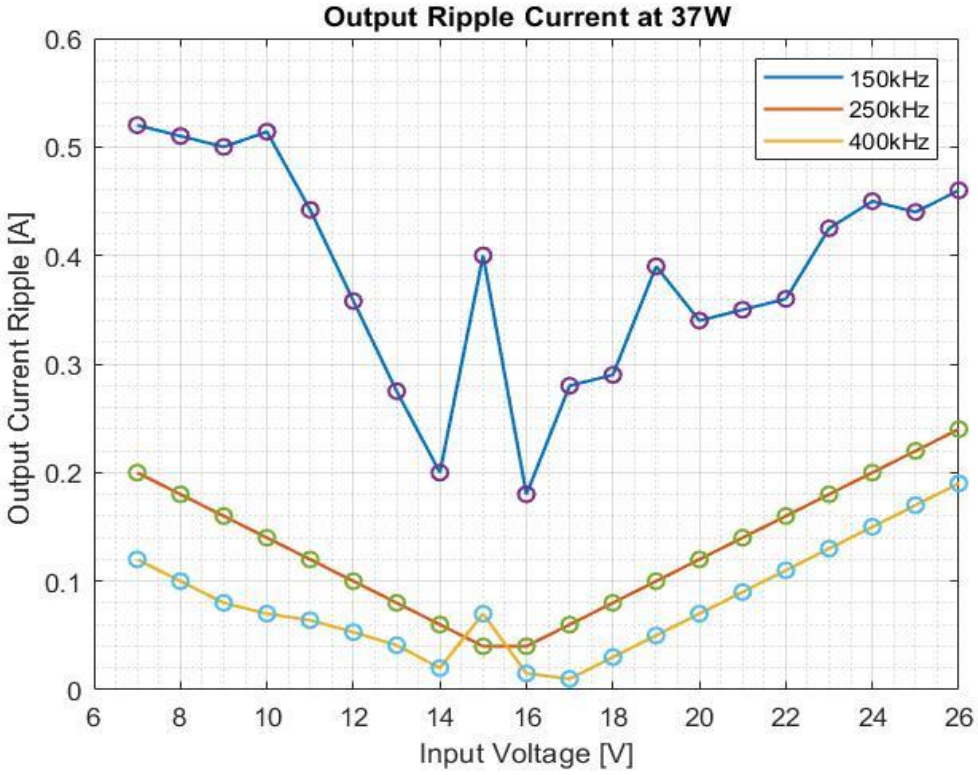


Fig 5.13 Output Current Ripple at 37W with different switching frequencies

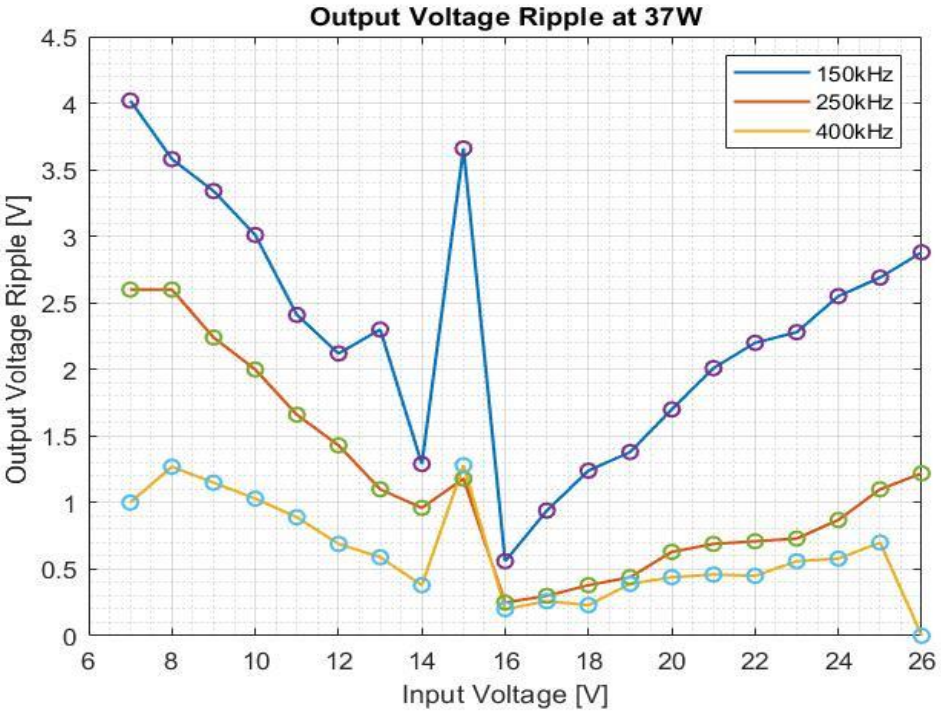


Fig 5.14 Output Voltage Ripple at 37W with different switching frequencies

As expected, both the output and voltage ripple decreases with the increase of the frequency.
Moreover, the ripple increases in the buck region as the input voltage increase because the duty cycle is higher to keep the output voltage constant. The same happens in the boost region.
For what regards the efficiency there is an expected trend as well as an expected decrease in the 15V (buck-boost mode) since all 4 switcher are active.
Moreover, as the switching frequency increases, especially at 400kHz, there is a significant drop in efficiency due to the fact that the switching losses as well as the dead time losses are strongly dependant from the switching frequency. This will be more evident as the power increases.

75 W TESTING

In fig 5.15 is showed the efficiency of the converter at 15V and 75W, hence using a 3Ω load. The ripple plot are omitted because they were very similar to the previous. The experimental data can be found at Appendix A , Table A7-A8-A9

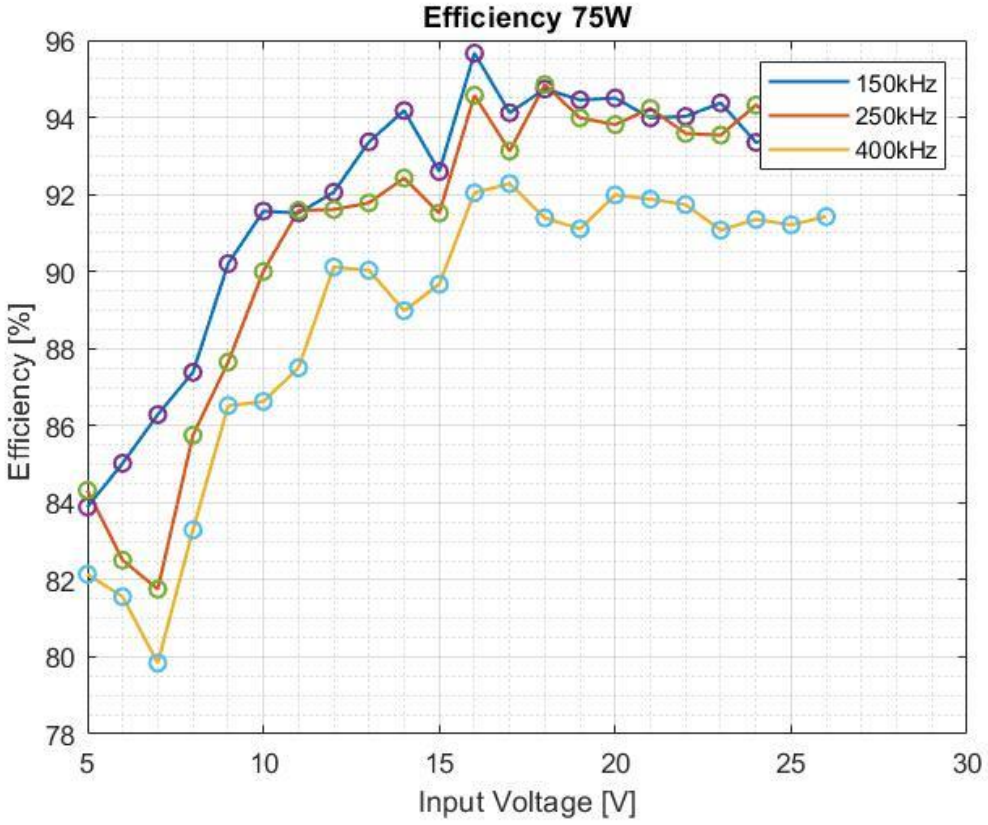


Fig 5.15 Efficiency at 75W of the converter varying switching frequencies.

In this test it is clear that the overall efficiency has decreased with respect to the previous test at 37W. More interesting results are showed in the next test performed at 180W.

180 W TESTING

The minimum input voltage for this test is 10V, because for less than 9V the expected input current was above 30A. Furthermore, the boost region is used with low voltages and low currents, hence with a total power less than 50W. The efficiency is showed in fig 5.16, while the output current and voltage ripple in 5.17 and 5.18 respectively.
The experimental data can be found at Appendix A , Table A10-A11-A12

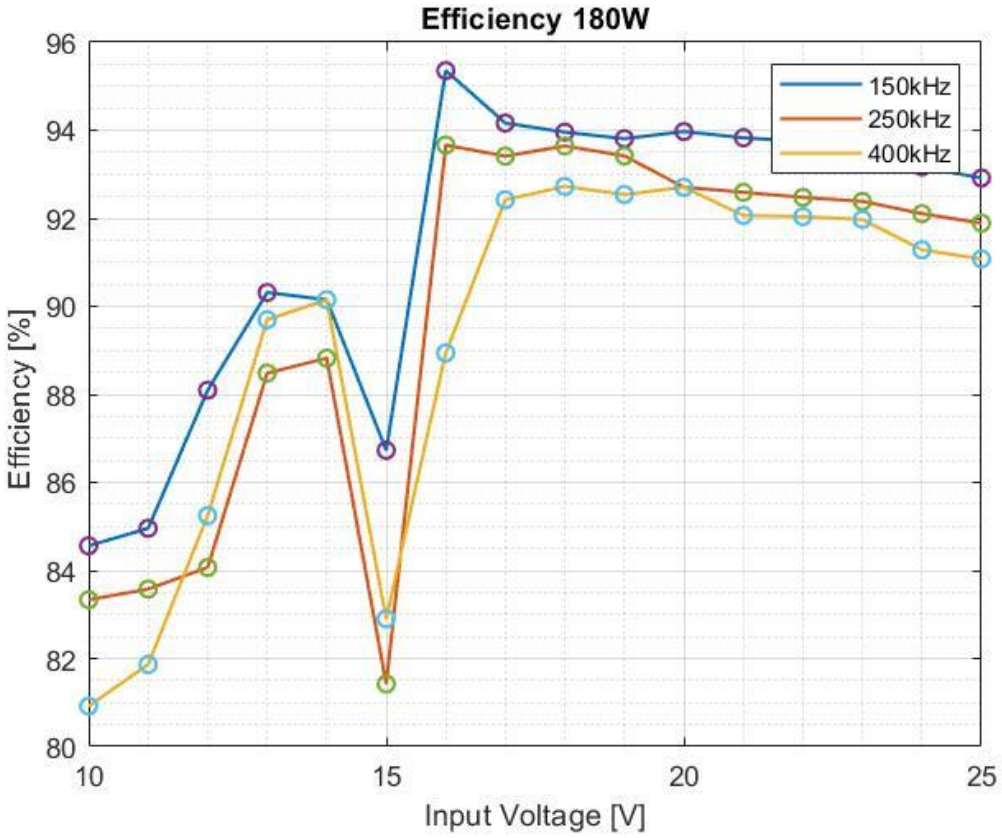


Fig 5.16 Efficiency at 180W, 15V Fixed Output Voltage

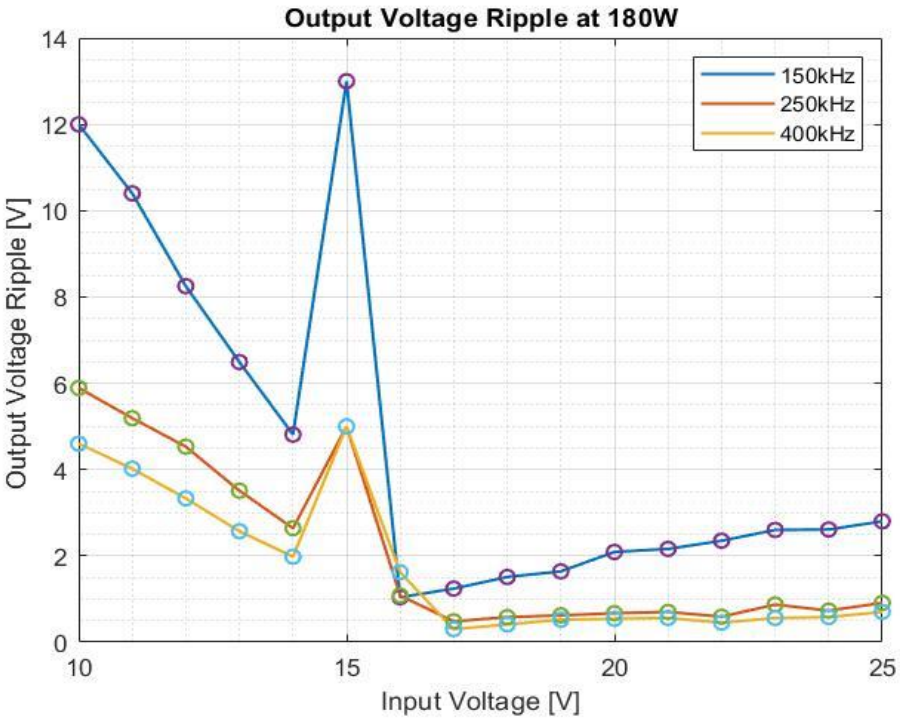


Fig 5.17 Output Current Ripple at 180W, 15V Fixed Output Voltage

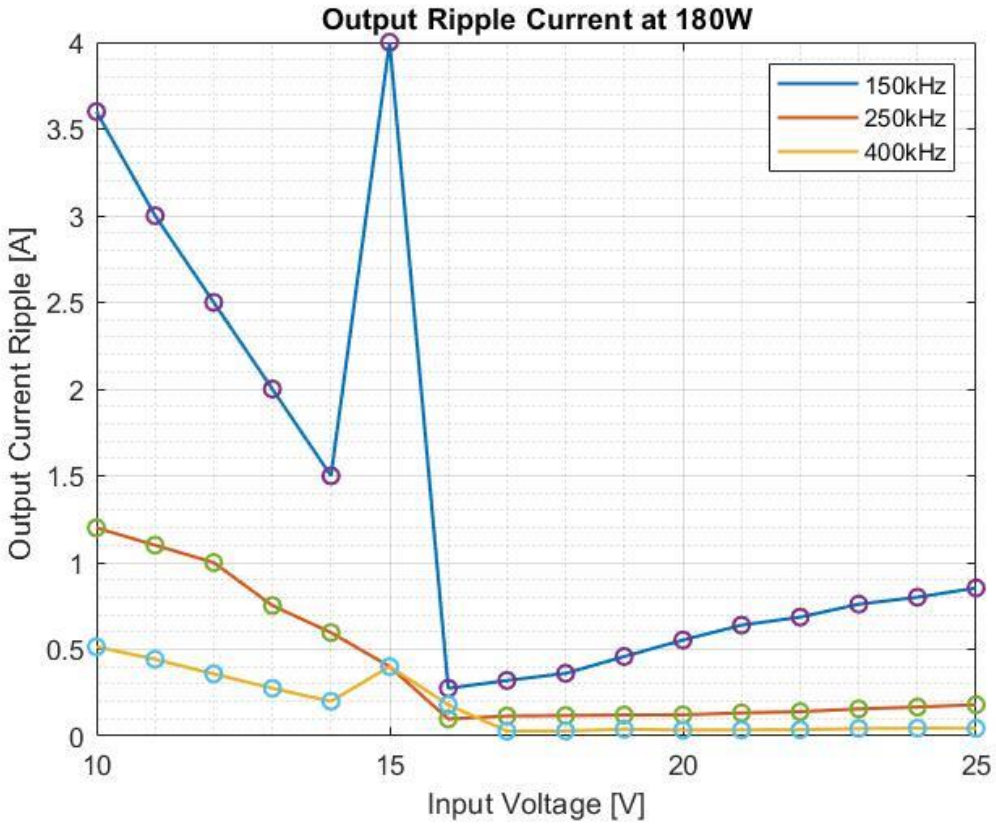


Fig 5.18 Voltage Current Ripple at 180W, 15V Fixed Output Voltage

As it can be seen from the previous results, the effiency starts to drop a little with the increase of the frequency as well as the ripple start decreasing.
Moreover, the effect of the dead time at 400kHz is far more relevant, and like shown in table A12, from 16V it is impossible to step down to 15V with only the buck mode active. Hence it was mandatory to use the buck-boost mode resulting in a 90% efficiency wrt the 94-96% of efficiency at 150-250kHz
It is clear that a good trade-off between reduction in ripple and efficiency is given by 250kHz as switching frequency, since at 400kHz the reduction in ripple is not so relevant.
Hence the last testing with the input varying power according to the Output TEG characteristics is performed at 250kHz.

Testing with TEG Output Power as Input Power

According to the Maximum power transfer Theorem, for a generator, in order to transfer the maximum power at the load both the impedances must be matched, hence, the impedance of the load must be equal to the one of the generator.

The TEG is modelled as a generator and 1Ω series resistor. By a practical point of view, the user should change the duty cycle and each time to have 1Ω as input resistance of the NIBB.

In high power test the input resistance was changed because the laboratory resistor can sustain only 100W, hence it was necessary to put 2 resistor in series with a parallel of other 2 series resistor with 1 ohm, so that for each branch only half of the current was received. This combination of parallel and series was then employed to sustain even 250W as input power, preventing damage to the resistors.

The ideal efficiency vs the experimental efficiency are showed in fig 5.19. In fig 5.20 it is showed that the input power follows correctly the TEG's output characteristics and in fig 5.21 it is clear that there was a correct impedance matching.
The experimental data can be found at Appendix A , Table A13

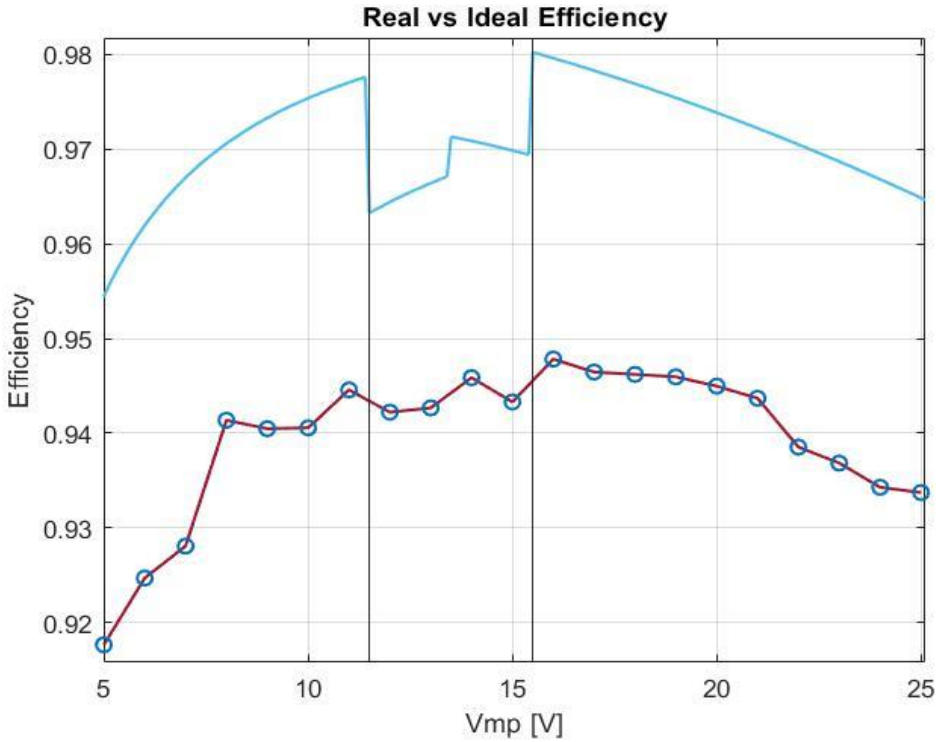


Fig 5.19 Ideal Efficiency (Red) vs Real Efficiency (Blue)

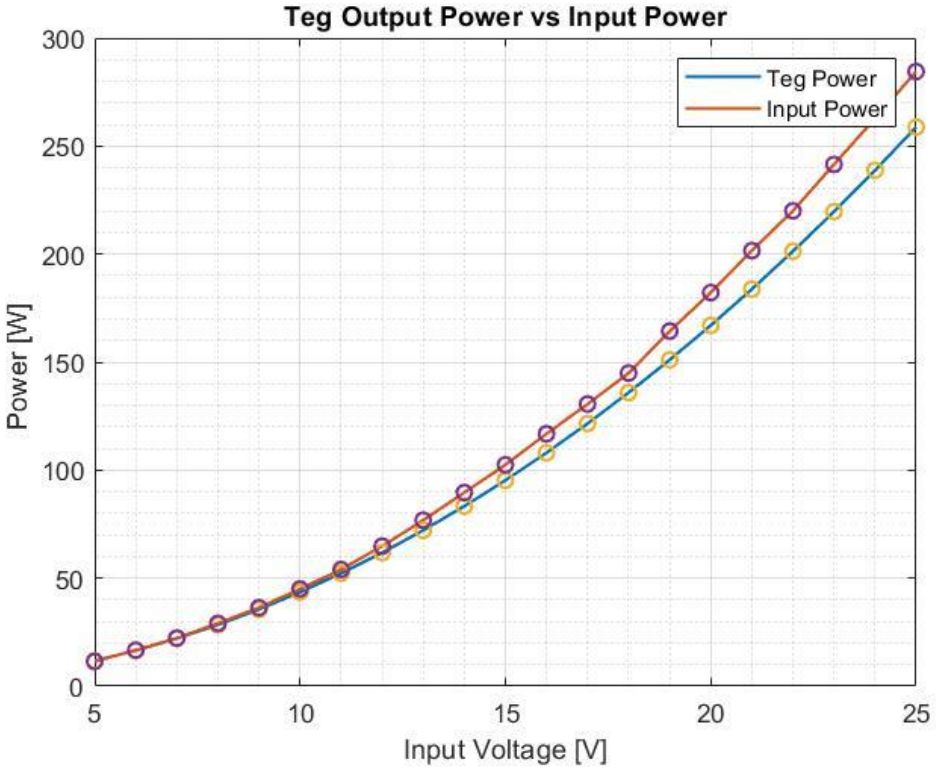


Fig 5.20 Teg power (Blue) vs Input Power(Orange) given

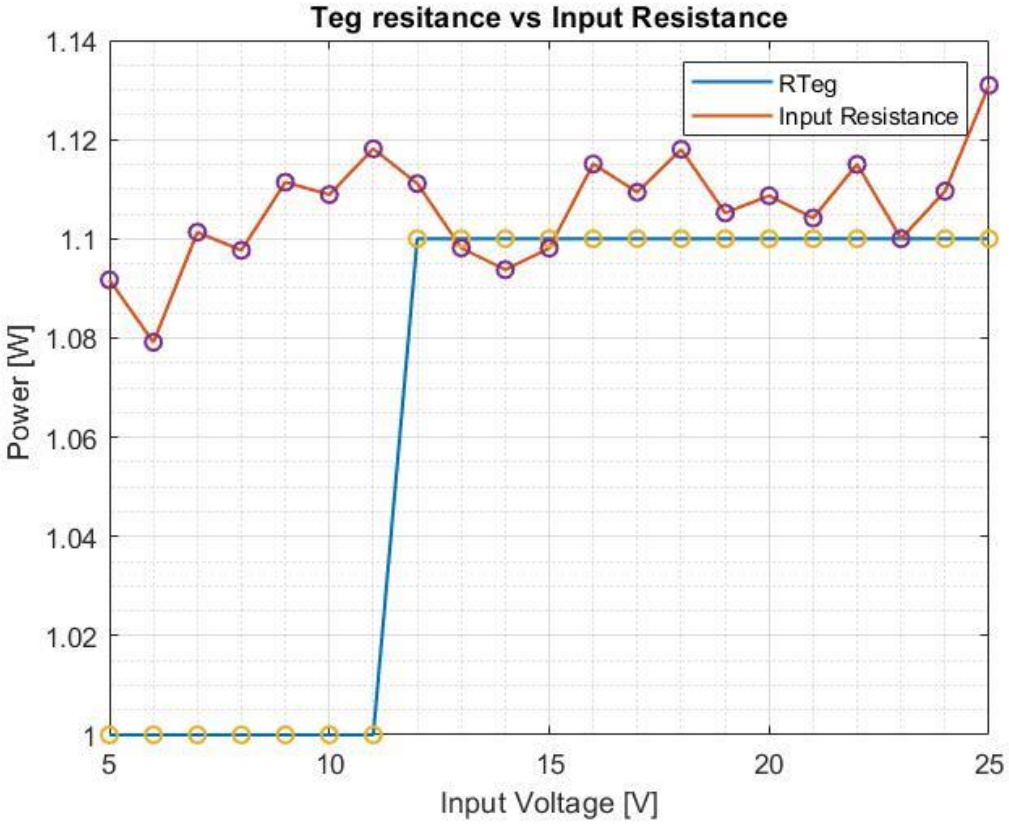


Fig 5.21 Equivalent resistance at input of Nibb (Orange) vs Teg

From the plot 5.19 the real efficiency is lower than the ideal one. This was expected since the simulation is done always in an ideal environment. Overall the efficiency is good with 95% of efficiency.
During the test it was also monitored the temperature using the Fluke Thermal Camera.
For each input power it was registered the temperature of the heatsink. Since the heatsink used had 74 C/W as thermal resistance, practically it had no impact by a thermal point of view.
The Temperature vs Input Power plot result is showed in figure 522E,along with all the thermocamera screenshots.
The maximum temperature reached is 65C at 180W, with 25V as Input Voltage.

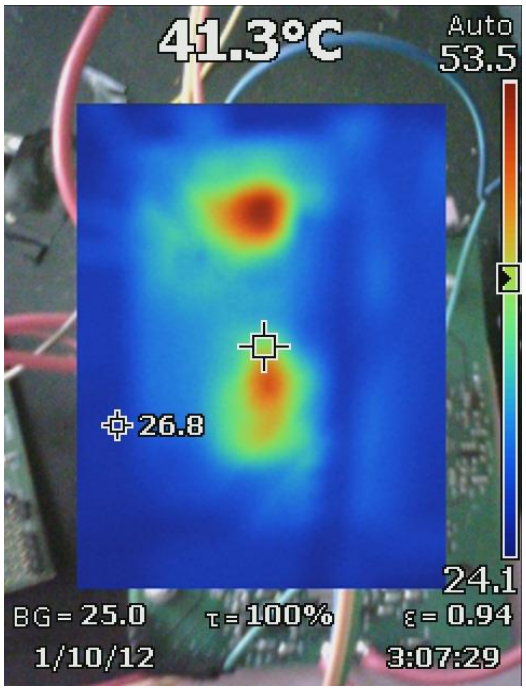


Fig 5.22 A Buck Mode

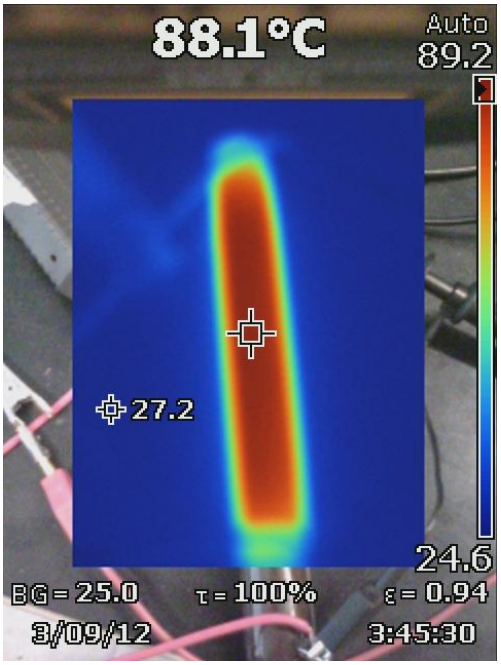


Fig 5.22B Load Temperature

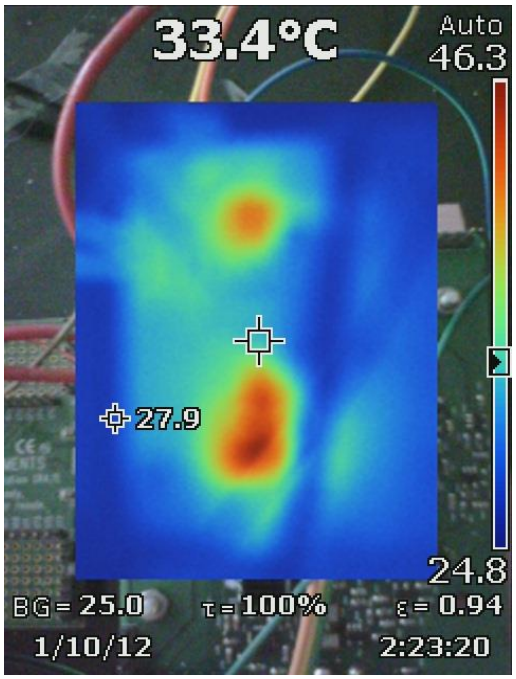


Fig 5.22C Boost Mode

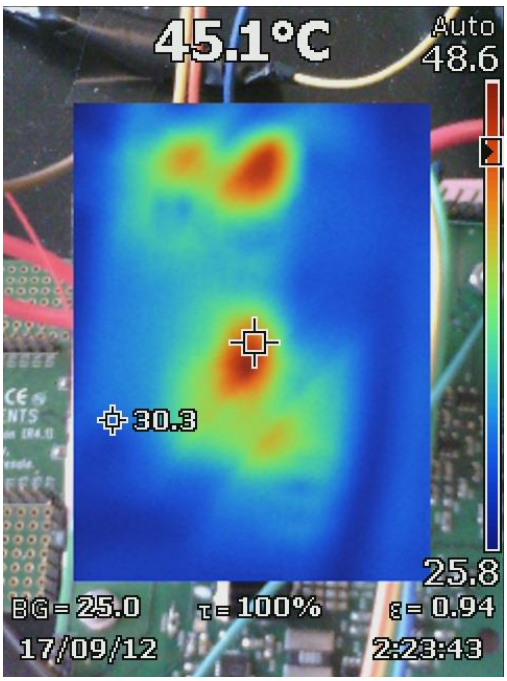


Fig 5.22D Buck Boost Mode

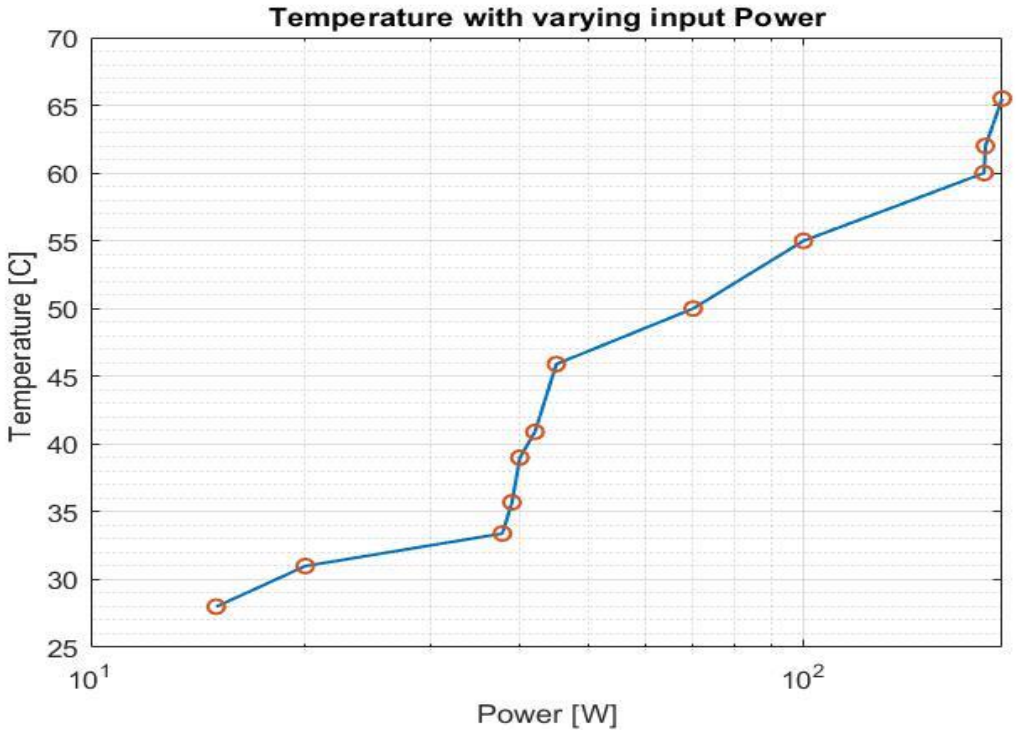


Fig 5.22 E Temperature vs Input Power Plot results

From the plot in Fix 5.22E it is clear that for 250W is necessary an heatsink with a lower thermal resistance.

5.3 Measure Stage Test

All the filters as well as voltage and current stage were tested, and their experimental data can be found in table A14 onwards.
The design of the measure stage has already been explained in chapter 3.1. As a brief recap, the voltage measure stage consists in a voltage divider followed by a fourth order Bessel filter with cutoff frequency set at 5kHz to eliminate the ripple component.
The input stage has a divider coefficient of 0.05, while the output stage has 0.15. Hence it is expected to have 1V if the input voltage is 20V, while 3V if the output voltage is 20V.
In fig 5.23 it is possible to see the characteristic of the voltage input stage and n fig 5.24 the output's one.

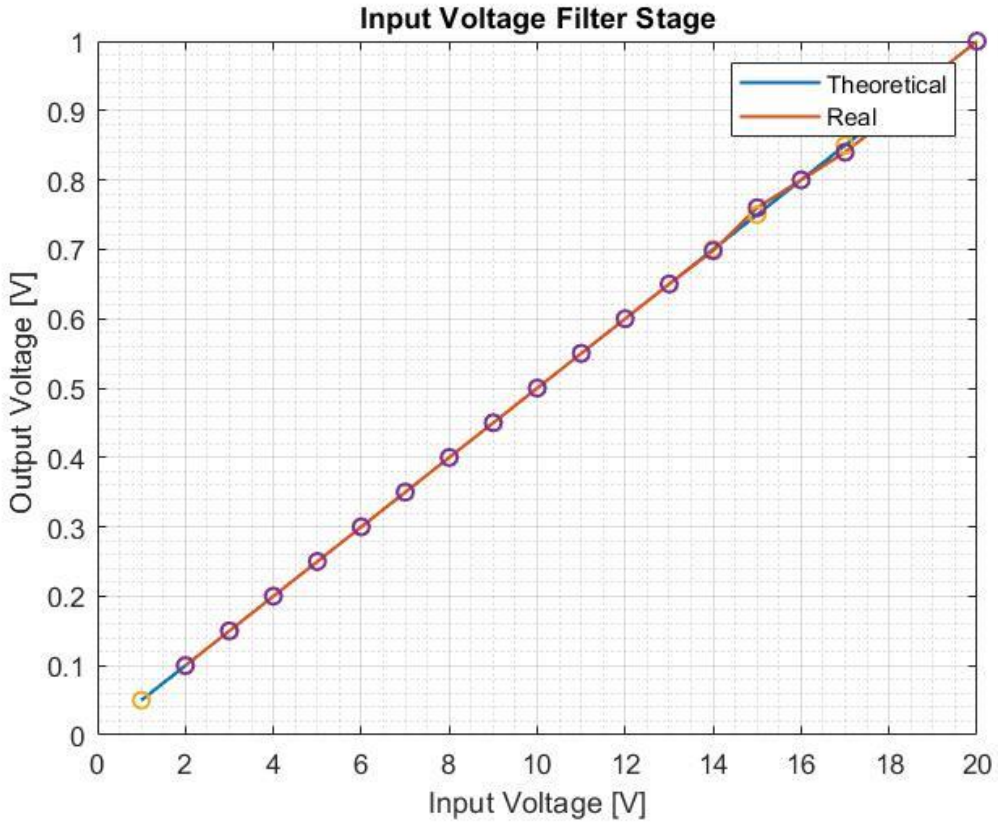


Fig 5.23 Input Voltage Filter Stage Theoretical(Blue) and Real(blue)

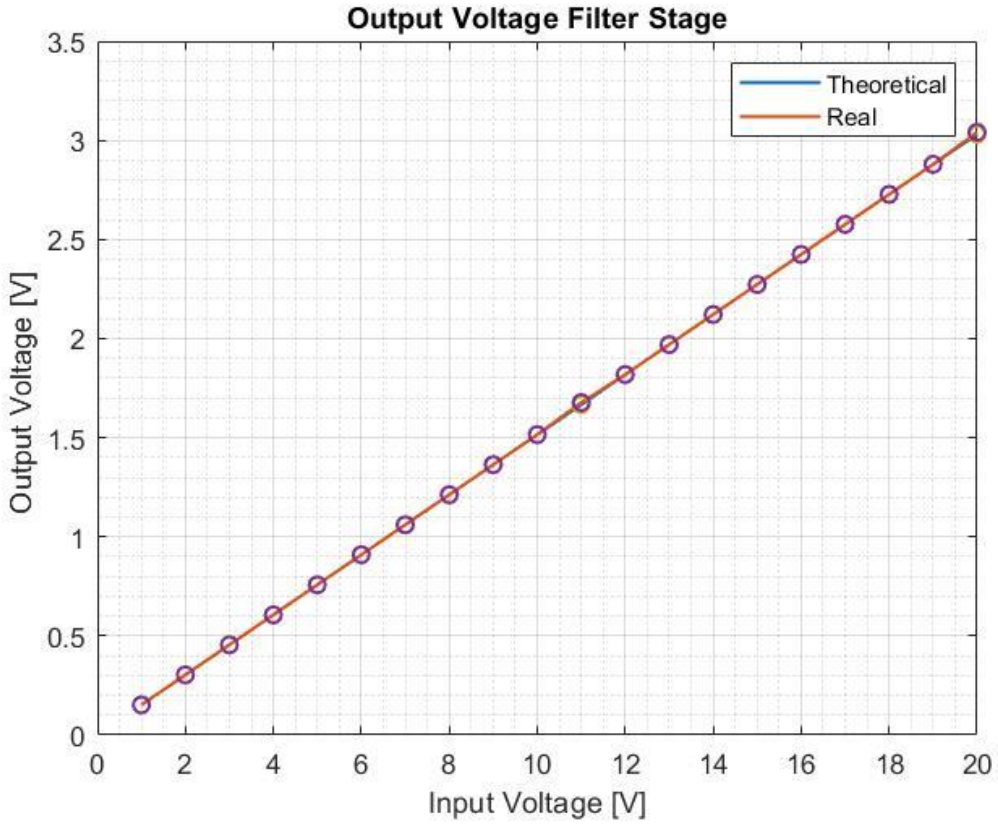


Fig 5.24 Output Voltage Filter theorical(blue) vs real(orange)

As expected, by using low tolerance resistances, the input and output measure stage were well designed.

For what regards the input and output current measure stage is designed with a shunt resistor, followed by a current sensor (INA293) plus a divider at its output and the low pass filter.
The following value were used:

- Gain Ina293 : 500
- Gain Divider : 0.19936
- Shunt Resistor : 0.001 Ω
- Gain ADC : 0.0024
- Bit ADC: 12
- INA Supply: 5V

Hence, for 5A we expect to read 0.5V. The plot is shown in fig 4.x

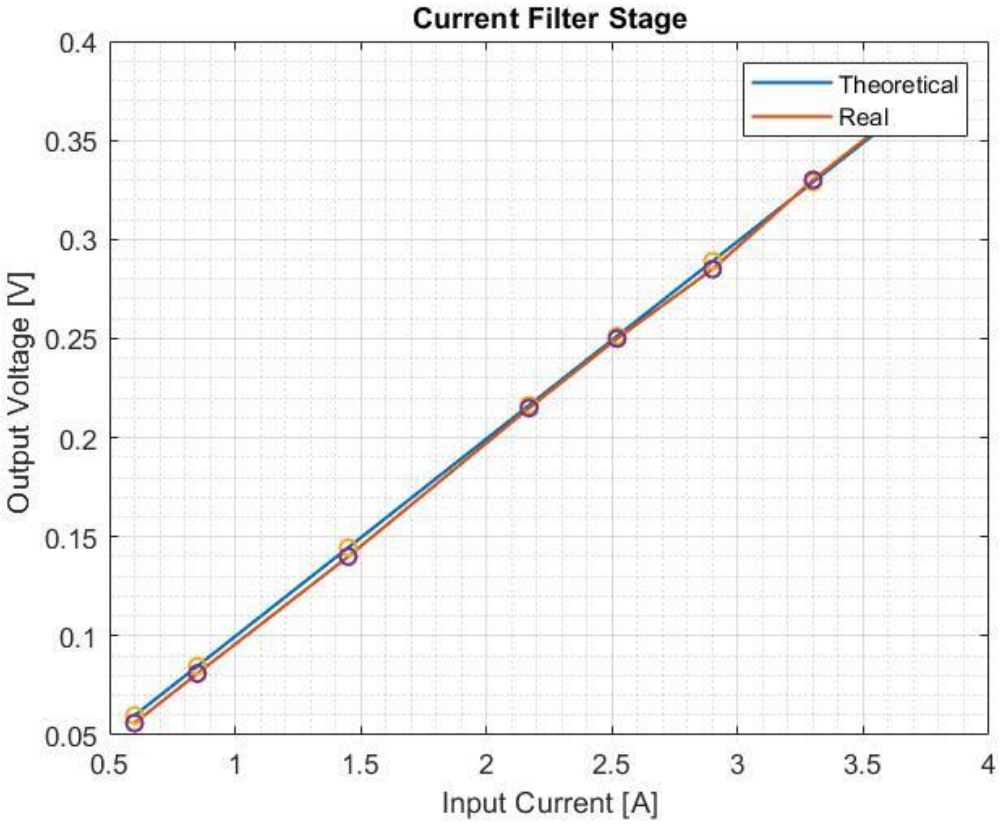


Fig 5.25 Output of Current Measure Stage

Fourth Order Bessel Filter Test

The fourth Order Bessel Filter has been tested separately. Magnitude and Phase are showed in fig 5.25 and with reference to the experimental data in table A16. As expected from the LTSPice simulation, it has low phase lag and more than 30db of attenuation at the switching frequency

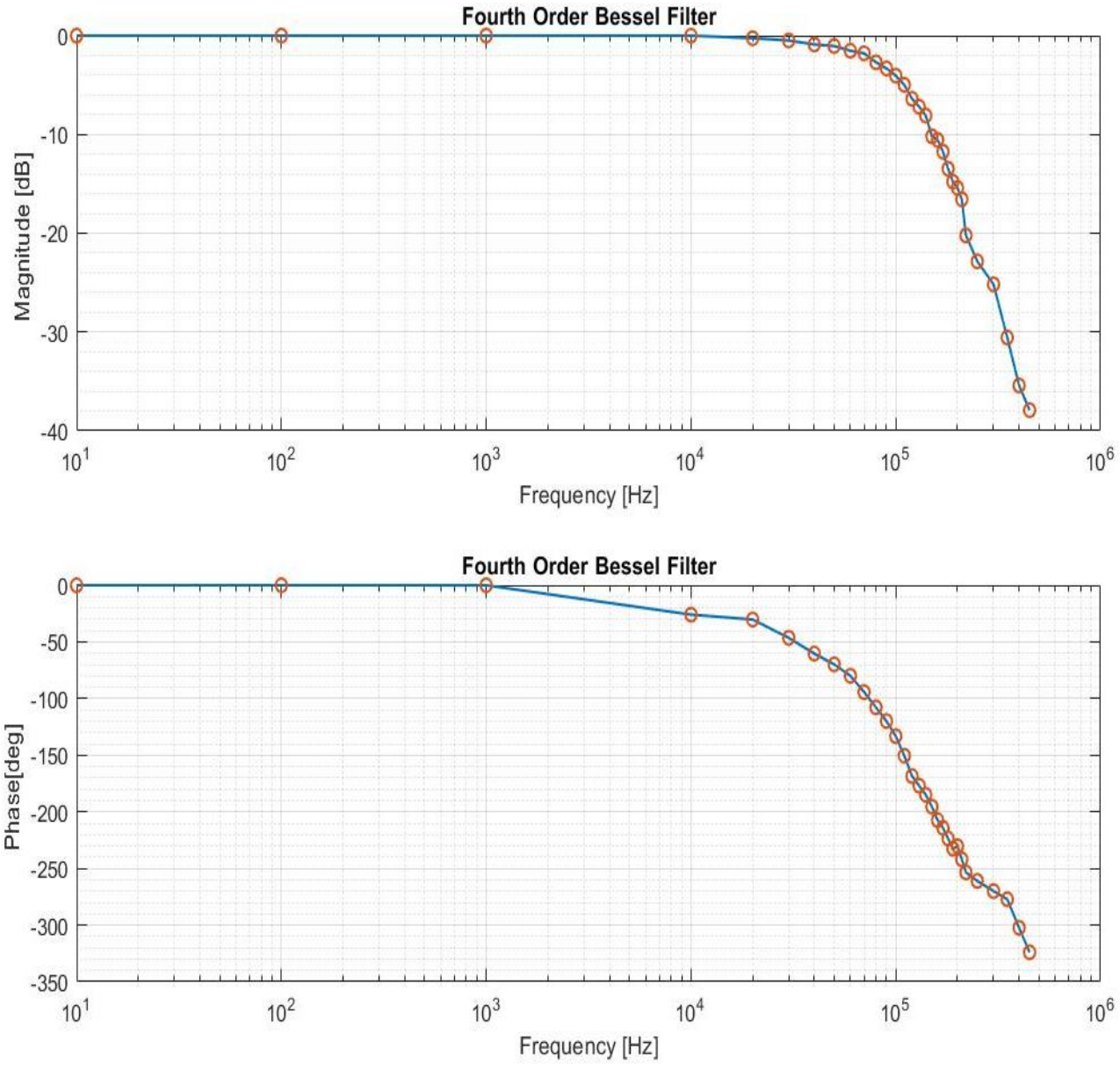


Fig 5.26 Experimental Data of Fourth Order Bessel Filter

Conclusion

From the experimental validation it is clear that there is a match between the experimental results and the simulation performed in Matlab, LtSpice and Simscape.
The efficiency of the converter is above 90% with it's peak at 95% with a temperature below 70 C.
This shows that the DC-DC converter as well as the measurement stage has been designed with care, with the correct selection of the components and the right design techniques.
Further improvement can be made by putting a power supply protection to protect the devices from polarity inversion and choosing a better driver.
Moreover, to further reduce the ripple, it can be added a big electrolytic capacitance even tough it will result in more space occupied.

Acronyms

ADC Analog to digital converter.

CAN Controller area network.

CCM Continuous conduction mode.

DAC Digital to analog converter.

DCM Discontinuous conduction mode.

EMI Electromagnetic interference.

ESR Equivalent series resistance

GPIO General purpose input/output.

JTAG Joint test action group.

MOSFET Metal–oxide–semiconductor field-effect transistor.

NIBB Non-inverting buck boost.

PCB Printed circuit board.

RMS Root mean square.

TEG Thermoelectric generator

GaN MOSFET Gallium Nitride Mosfet

Appendix A - Experimental Data Tables

Table A.1 : 150kHz Constant Duty Cycle

Vin	In	Vout	Iout	Pout	Pin	Eff	Vmax	Vmin	Iripp	Vripp	Da	Dbneg
5	2.1	5.24	1.67	8.7508	10.5	83.34095	5.56	4.81	0.2	0.75	98	80
6	2.4	6.1	1.98	12.078	14.4	83.875	6.37	5.62	0.124	0.75	98	80
7	2.9	7.188	2.34	16.81992	20.3	82.85675	7.54	6.63	0.15	0.91	98	80
8	3.3	8.262	2.71	22.39002	26.4	84.81068	8.9	8	0.17	0.9	98	80
9	4.1	10.164	3.31	33.64284	36.9	91.17301	10.66	9.16	0.19	1.5	98	80
10	4.6	11.4	3.72	42.408	46	92.1913	11.98	10.32	0.25	1.66	98	80
11	5	12.36	4.046	50.00856	55	90.92465	13.04	11.21	0.26	1.83	98	80
12	1.45	7.04	2.2	15.488	17.4	89.01149	9.83	8.2	0.32	1.63	98	80
13	1.5	7.3	2.37	17.301	19.5	88.72308	9.6	6.8	0.4	2.8	50	80
14	1.63	7.9	2.61	20.619	22.82	90.35495	10.1	8.2	0.41	1.9	50	80
15	1.83	8.8	2.89	25.432	27.45	92.64845	8.8	7.85	0.18	0.95	50	80
16	1.3	7.7	2.492	19.1884	20.8	92.25192	8.31	7.52	0.17	0.79	50	98
17	1.4	8.032	2.585	20.76272	23.8	87.23832	8.58	7.31	0.17	1.27	50	98
18	1.5	8.627	2.794	24.10384	27	89.27347	9.24	7.86	0.18	1.38	50	98
19	1.6	9.144	2.977	27.22169	30.4	89.54503	9.81	8.31	0.2	1.5	50	98
20	1.67	9.668	3.144	30.39619	33.4	91.00656	10.38	8.75	0.22	1.63	50	98
21	1.78	10.411	3.386	35.25165	37.38	94.30617	11.25	9.38	0.24	1.87	50	98
22	1.83	10.744	3.486	37.45358	40.26	93.02927	11.63	9.96	0.26	1.67	50	98
23	1.9	11.074	3.589	39.74459	43.7	90.94871	11.94	9.94	0.28	2	50	98
24	2	11.73	3.804	44.62092	48	92.96025	12.7	10.51	0.3	2.19	50	98
25	2.08	12.346	4.014	49.55684	52	95.30162	13.36	11.05	0.32	2.31	50	98
26	2.18	12.89	4.21	54.2669	56.68	95.74259	14.05	11.49	0.34	2.56	50	98

Table A.2: 250kHz Constant Duty Cycle Table Data

Vin	In	Vout	Iout	Pout	Pin	Eff	Vmax	Vmin	Iripp	Vripp	Da	Dbneg
5	2.1	5.2221	1.72	8.982012	10.5	85.54297	5.45	4.98	0.037	0.47	98	80
6	2.63	6.5	2.15	13.975	15.78	88.56147	6.79	6.23	0.04	0.56	98	80
7	2.8	7.19	2.32	16.6808	19.6	85.10612	8.2	7.4	0.04	0.8	98	80
8	3.2	8.28	2.73	22.6044	25.6	88.29844	9	7.8	0.05	1.2	98	80
9	4.1	10.23	3.318	33.94314	36.9	91.98683	10.7	9.6	0.07	1.1	98	80
10	4.58	11.4	3.72	42.408	45.8	92.59389	11.9	10.6	0.09	1.3	98	80
11	4.9	12.28	4.018	49.34104	53.9	91.54182	12.9	11.5	0.09	1.4	98	80
12	1.4	7.04	2.2	15.488	16.8	92.19048	7.4	6.5	0.031	0.9	98	80
13	1.5	7.3	2.37	17.301	19.5	88.72308	7.7	6.8	0.036	0.9		
14	1.6	7.9	2.61	20.619	22.4	92.04911	8.2	7.3	0.037	0.9		
15	1.8	8.8	2.89	25.432	27	94.19259	9.2	8.1	0.041	1.1		
16	1.3	7.63	2.55	19.4565	20.8	93.54087	7.8	7.2	0.032	0.6	50	98
17	1.4	8.34	2.65	22.101	23.8	92.86134	8.5	7.7	0.037	0.8	50	98
18	1.47	8.74	2.82	24.6468	26.46	93.14739	9.2	8.4	0.04	0.8	50	98
19	1.5	8.95	2.97	26.5815	28.5	93.26842	9.4	8.4	0.04	1	50	98
20	1.6	9.65	3.15	30.3975	32	94.99219	9.9	9.2	0.039	0.7	50	98
21	1.64	10.03	3.3	33.099	34.44	96.10627	10.5	9.4	0.041	1.1	50	98
22	1.69	10.36	3.41	35.3276	37.18	95.01775	10.9	9.9	0.042	1	50	98
23	1.79	10.88	3.58	38.9504	41.17	94.6087	11.5	10.4	0.05	1.1	50	98
24	1.89	11.26	3.72	41.8872	45.36	92.34392	11.7	10.7	0.064	1	50	98
25	1.94	12	3.8	45.6	48.5	94.02062	12.3	11	0.04	1.3	50	98
26	2.028	12.25	4.1	50.225	52.728	95.253	12.7	11.5	0.04	1.2	50	98

Table A3: 400kHz Constant Duty Cycles Experimental Data

Vin	In	Vout	Iout	Pout	Pin	Eff	Vmax	Vmin	Iripp	Vripp	Da	Dbneg
5	2.1	5.54	1.72	9.5288	10.5	90.75048	5.85	5.3	0.01	0.55	98	80
6	2.6	6.63	2.15	14.2545	15.6	91.375	6.9	6.4	0.01	0.5	98	80
7	2.9	7.65	2.39	18.2835	20.3	90.0665	8	7.3	0.01	0.7	98	80
8	3.3	8.68	2.78	24.1304	26.4	91.40303	8.9	8.3	0.01	0.6	98	80
9	3.9	9.84	3.318	32.64912	35.1	93.01744	10.2	9.4	0.01	0.8	98	80
10	4.3	10.94	3.72	40.6968	43	94.64372	11.4	10.5	0.01	0.9	98	80
11	4.7	11.87	4.018	47.69366	51.7	92.25079	12.3	11.4	0.01	0.9	98	80
12	1.3	6.49	2.2	14.278	15.6	91.52564	6.7	6.1	0.01	0.6	98	80
13	1.4	7	2.37	16.59	18.2	91.15385	7.3	6.7	0.01	0.6		
14	1.5	7.55	2.61	19.7055	21	93.83571	7.8	7.2	0.01	0.6		
15	1.6	7.98	2.89	23.0622	24	96.0925	8.3	7.7	0.01	0.6		
16	1.2	7.33	2.55	18.6915	19.2	97.35156	7.7	7.1	0.01	0.6	50	98
17	1.26	7.7	2.65	20.405	21.42	95.26144	8	7.4	0.01	0.6	50	98
18	1.3	8.11	2.82	22.8702	23.4	97.7359	8.3	7.7	0.01	0.6	50	98
19	1.38	8.5	2.97	25.245	26.22	96.28146	8.8	8.1	0.01	0.7	50	98
20	1.52	9.35	3.15	29.4525	30.4	96.88322	9.5	9.1	0.01	0.4	50	98
21	1.57	9.54	3.3	31.482	32.97	95.48681	9.7	9.1	0.015	0.6	50	98
22	1.66	10.38	3.41	35.3958	36.52	96.92169	10.6	10	0.017	0.6	50	98
23	1.74	10.76	3.58	38.5208	40.02	96.25387	11.1	10.3	0.016	0.8	50	98
24	1.82	11.31	3.72	42.0732	43.68	96.32143	11.6	10.8	0.02	0.8	50	98
25	1.88	11.82	3.82	45.1524	47	96.06894	12	11.3	0.015	0.7	50	98
26	1.97	12.1	4.1	49.61	51.22	96.8567	12.5	11.7	0.018	0.8	50	98

Table A4: 150kHz Constant Power 37 W, Fixed Output Voltage 15V

Vin	In	Vout	Iout	Pout	Pin	Eff	Vmax	Vmin	Iripp	Vripp	Da	Dbneg
7	6	15	2.49	37.35	42	88.92857	16.89	12.87	0.52	4.02	98	35
8	5.2	15	2.49	37.35	41.6	89.78365	16.63	13.05	0.51	3.58	98	45
9	4.5	15	2.49	37.35	40.5	92.22222	16.4	13.06	0.5	3.34	98	52
10	4	15	2.49	37.35	40	93.375	16.26	13.25	0.514	3.01	98	59
11	3.6	15	2.49	37.35	39.6	94.31818	15.85	13.44	0.442	2.41	98	63
12	3.3	15	2.52	37.8	39.6	95.45455	15.71	13.59	0.358	2.12	98	73
13	3	15	2.49	37.35	39	95.76923	15.61	13.31	0.275	2.3	98	80
14	2.79	15	2.49	37.35	39.06	95.62212	15.42	14.13	0.2	1.29	94	98
15	2.6	15.05	2.49	37.4745	39	96.08846	16.54	12.88	0.4	3.66	50	55
16	2.39	15.1	2.5	37.75	38.24	98.71862	15.37	14.81	0.18	0.56	96	96
17	2.28	15.12	2.514	38.01168	38.76	98.06935	15.61	14.67	0.28	0.94	89	96
18	2.15	15	2.52	37.8	38.7	97.67442	15.74	14.5	0.29	1.24	85	96
19	2.03	15	2.51	37.65	38.57	97.61473	15.78	14.4	0.39	1.38	81	96
20	1.91	15	2.49	37.35	38.2	97.77487	16	14.3	0.34	1.7	79	96
21	1.82	15	2.49	37.35	38.22	97.7237	16.01	14	0.35	2.01	70	96
22	1.75	15	2.49	37.35	38.5	97.01299	16.2	14	0.36	2.2	68	96
23	2	15	2.49	37.35	38.41	97.2403	16.28	14	0.425	2.28	66	96
24	1.61	15	2.49	37.35	38.64	96.66149	16.251	13.7	0.45	2.551	64	96
25	1.57	15	2.49	37.35	39.25	95.15924	16.39	13.7	0.44	2.69	62	96
26	1.51	15	2.49	37.35	39.26	95.135	16.4	13.52	0.46	2.88	60	96

Table A5: 250kHz Costant Power 37W Fixed Output Voltage 15V

Vin	In	Vout	Iout	Pout	Pin	Eff	Vmax	Vmin	Iripp	Vripp	Da	Dbneg
7	6	15	2.5	37.5	42	89.28571	16.4	13.8	0.2	2.6	98	35
8	5.29	15	2.5	37.5	42.32	88.61059	16.3	13.7	0.18	2.6	98	45
9	4.5	15	2.5	37.5	40.5	92.59259	16.13	13.89	0.16	2.24	98	52
10	4	15	2.5	37.5	40	93.75	16	14	0.14	2	98	59
11	3.6	15	2.49	37.35	39.6	94.31818	15.81	14.15	0.12	1.66	98	63
12	3.3	15	2.5	37.5	39.6	94.69697	15.68	14.25	0.1	1.43	98	73
13	3	15	2.5	37.5	39	96.15385	15.53	14.43	0.08	1.1	98	80
14	2.78	15	2.5	37.5	38.92	96.35149	15.47	14.51	0.06	0.96	94	98
15	2.65	15.1	2.5	37.75	39.75	94.96855	15.81	14.63	0.04	1.18	50	55
16	2.39	15	2.5	37.5	38.24	98.06485	15.15	14.9	0.04	0.25	96	96
17	2.29	15.1	2.51	37.901	38.93	97.35679	15.2	14.9	0.06	0.3	89	96
18	2.18	15.15	2.506	37.9659	39.24	96.75306	15.24	14.86	0.08	0.38	85	96
19	2.02	15	2.5	37.5	38.38	97.70714	15.27	14.83	0.1	0.44	81	96
20	1.93	15	2.5	37.5	38.6	97.15026	15.34	14.71	0.12	0.63	79	96
21	1.83	15	2.5	37.5	38.43	97.58002	15.4	14.71	0.14	0.69	70	96
22	1.75	15	2.5	37.5	38.5	97.4026	15.5	14.79	0.16	0.71	68	96
23	2	15	2.5	37.5	38.41	97.63083	15.43	14.7	0.18	0.73	66	96
24	1.6	15	2.5	37.5	38.4	97.65625	15.58	14.71	0.2	0.87	64	96
25	1.57	15.1	2.5	37.75	39.25	96.17834	15.4	14.3	0.22	1.1	62	96
26	1.5	15	2.5	37.5	39	96.15385	15.4	14.18	0.24	1.22	60	96

Table A6 : 400kHz Constant Power 37W Fixed Output Voltage 15V

Vin	In	Vout	Iout	Pout	Pin	Eff	Vmax	Vmin	Iripp	Vripp	Da	Dbneg
7	6	15.07	2.5	37.675	42	89.70238	15.7	14.7	0.12	1	98	35
8	5.19	15.07	2.5	37.675	41.52	90.7394	15.63	14.36	0.1	1.27	98	45
9	4.59	15.07	2.5	37.675	41.31	91.20068	15.65	14.5	0.08	1.15	98	52
10	4.09	15.1	2.5	37.75	40.9	92.29829	15.67	14.64	0.07	1.03	98	59
11	3.7	15.1	2.5	37.75	40.7	92.75184	15.46	14.57	0.064	0.89	98	63
12	3.38	15.1	2.505	37.8255	40.56	93.25814	15.49	14.8	0.053	0.69	98	73
13	3.1	15.2	2.5	38	40.3	94.2928	15.43	14.84	0.041	0.59	98	80
14	2.8	15.1	2.5	37.75	39.2	96.30102	15.11	14.73	0.02	0.38	94	98
15	2.73	15.1	2.5	37.75	40.95	92.18559	15.86	14.58	0.07	1.28	50	55
16	2.4	15.12	2.5	37.8	38.4	98.4375	15.2	15	0.015	0.2	96	95
17	2.29	15.15	2.5	37.875	38.93	97.29001	15.3	15.04	0.01	0.26	95	96
18	2.19	15.1	2.5	37.75	39.42	95.76357	15.2	14.97	0.03	0.23	90	96
19	2.1	15.16	2.5	37.9	39.9	94.98747	15.25	14.86	0.05	0.39	84	96
20	1.99	15.17	2.5	37.925	39.8	95.28894	15.28	14.84	0.07	0.44	79.5	96
21	1.89	15.15	2.5	37.875	39.69	95.42706	15.26	14.8	0.09	0.46	75	96
22	1.8	15.1	2.5	37.75	39.6	95.32828	15.25	14.8	0.11	0.45	73	96
23	2	15.08	2.5	37.7	39.56	95.29828	15.26	14.7	0.13	0.56	69.5	96
24	1.62	14.98	2.49	37.3002	38.88	95.93673	15.28	14.7	0.15	0.58	67	96
25	1.58	15.1	2.5	37.75	39.5	95.56962	15.26	14.56	0.17	0.7	63.8	96
26	1.51	15	2.49	37.35	39.26	95.135			0.19	0	60	96

Table A7: 150kHz Constant Power 75W Fixed Output Voltage 15V

Vin	In	Vout	Iout	Pout	Pin	Eff	Da	Dbneg	Dbneg	Db	Da
5	18	15.1	5	75.5	90	83.88889	98	30	0.3	0.7	0.98
6	14.8	15.1	5	75.5	88.8	85.02252	98	38	0.38	0.62	0.98
7	12.5	15.1	5	75.5	87.5	86.28571	98	42	0.42	0.58	0.98
8	10.8	15.1	5	75.5	86.4	87.38426	98	48	0.48	0.52	0.98
9	9.3	15.1	5	75.5	83.7	90.20311	98	53	0.53	0.47	0.98
10	8.3	15.2	5	76	83	91.56627	98	58	0.58	0.42	0.98
11	7.5	15.1	5	75.5	82.5	91.51515	98	63	0.63	0.37	0.98
12	6.88	15.2	5	76	82.56	92.05426	98	68	0.68	0.32	0.98
13	6.2	15.05	5	75.25	80.6	93.36228	98	77	0.77	0.23	0.98
14	5.7	15.03	5	75.15	79.8	94.17293	94	98	0.98	0.02	0.94
15	5.4	15	5	75	81	92.59259	50	55	0.55	0.45	0.5
16	4.9	15	5	75	78.4	95.66327	96	98	0.98	0.02	0.96
17	4.75	15.2	5	76	80.75	94.11765	92	98	0.98	0.02	0.92
18	4.41	15.04	5	75.2	79.38	94.73419	88	98	0.98	0.02	0.88
19	4.21	15.11	5	75.55	79.99	94.44931	82	98	0.98	0.02	0.82
20	4	15.12	5	75.6	80	94.5	78.5	98	0.98	0.02	0.785
21	3.8	15	5	75	79.8	93.98496	74	98	0.98	0.02	0.74
22	3.65	15.1	5	75.5	80.3	94.02242	70	98	0.98	0.02	0.7
23	3.46	15.02	5	75.1	79.58	94.37044	68	98	0.98	0.02	0.68
24	3.37	15.1	5	75.5	80.88	93.34817	65	98	0.98	0.02	0.65
25	3.25	15.21	5	76.05	81.25	93.6	63	98	0.98	0.02	0.63
26	3.05	15.1	5	75.5	79.3	95.20807	59	98	0.98	0.02	0.59

Table A8: 250kHz Costant Power 75W Fixed Output Voltage 15V

Vin	In	Vout	Iout	Pout	Pin	Eff	Da	Dbneg	Dbneg	Db	Da
5	17.8	15.1	4.97	75.047	89	84.32247	98	31	0.31	0.69	0.98
6	15.2	15.05	5	75.25	91.2	82.51096	98	32	0.32	0.68	0.98
7	13	15.03	4.95	74.3985	91	81.75659	98	36.5	0.365	0.635	0.98
8	11.3	15.2	5.1	77.52	90.4	85.75221	98	45	0.45	0.55	0.98
9	9.5	15.03	4.986	74.93958	85.5	87.64863	98	52	0.52	0.48	0.98
10	8.3	15	4.98	74.7	83	90	98	59	0.59	0.41	0.98
11	7.4	15	4.97	74.55	81.4	91.58477	98	66	0.66	0.34	0.98
12	6.8	14.98	4.99	74.7502	81.6	91.60564	98	73	0.73	0.27	0.98
13	6.24	14.95	4.98	74.451	81.12	91.77885	98	80	0.8	0.2	0.98
14	5.8	14.95	5.02	75.049	81.2	92.42488	94	98	0.98	0.02	0.94
15	5.5	15.1	5	75.5	82.5	91.51515	50	55	0.55	0.45	0.5
16	4.95	15.04	4.98	74.8992	79.2	94.5697	96	98	0.98	0.02	0.96
17	4.75	15.1	4.98	75.198	80.75	93.12446	91	98	0.98	0.02	0.91
18	4.39	15.05	4.98	74.949	79.02	94.84814	85	98	0.98	0.02	0.85
19	4.2	15.06	4.98	74.9988	79.8	93.98346	83	98	0.98	0.02	0.83
20	4	15.07	4.98	75.0486	80	93.81075	79	98	0.98	0.02	0.79
21	3.78	15.02	4.98	74.7996	79.38	94.22978	75	98	0.98	0.02	0.75
22	3.58	14.8	4.98	73.704	78.76	93.5805	69	98	0.98	0.02	0.69
23	3.5	15.12	4.98	75.2976	80.5	93.53739	65	98	0.98	0.02	0.65
24	3.3	15	4.98	74.7	79.2	94.31818	61	98	0.98	0.02	0.61
25	3.2	15.04	4.98	74.8992	80	93.624	58	98	0.98	0.02	0.58
26	3.1	15.08	4.98	75.0984	80.6	93.17419	54	98	0.98	0.02	0.54

Table A9 : 400 kHz Costant Power 75W Fixed Output Voltage 15V

Vin	In	Vout	Iout	Pout	Pin	Eff	Da	Dbneg	Dbneg	Db	Da
5	16.8	15	4.6	69	84	82.14286	98	31	0.31	0.69	0.98
6	14.1	15	4.6	69	84.6	81.56028	98	32	0.32	0.68	0.98
7	12.4	15	4.62	69.3	86.8	79.83871	98	35	0.35	0.65	0.98
8	10.4	15	4.62	69.3	83.2	83.29327	98	45	0.45	0.55	0.98
9	8.9	15	4.62	69.3	80.1	86.51685	98	52	0.52	0.48	0.98
10	8	15	4.62	69.3	80	86.625	98	59	0.59	0.41	0.98
11	7.2	15	4.62	69.3	79.2	87.5	98	63	0.63	0.37	0.98
12	6.4	14.98	4.62	69.2076	76.8	90.11406	98	73	0.73	0.27	0.98
13	6	15.2	4.62	70.224	78	90.03077	98	80	0.8	0.2	0.98
14	5.6	15.1	4.62	69.762	78.4	88.98214	94	98	0.98	0.02	0.94
15	5.4	15.1	4.81	72.631	81	89.6679	50	55	0.55	0.45	0.5
16	4.8	15.04	4.7	70.688	76.8	92.04167	96	96	0.96	0.04	0.96
17	4.5	15.02	4.7	70.594	76.5	92.27974	89	96	0.96	0.04	0.89
18	4.3	15.05	4.7	70.735	77.4	91.38889	85	96	0.96	0.04	0.85
19	4.1	15.1	4.7	70.97	77.9	91.10398	81	96	0.96	0.04	0.81
20	3.85	15.07	4.7	70.829	77	91.98571	79	96	0.96	0.04	0.79
21	3.62	15.02	4.65	69.843	76.02	91.87451	70	96	0.96	0.04	0.7
22	3.41	14.8	4.65	68.82	75.02	91.73554	68	96	0.96	0.04	0.68
23	3	15	4.72	70.8	77.74	91.07281	66	96	0.96	0.04	0.66
24	3.18	15.156	4.6	69.7176	76.32	91.34906	64	96	0.96	0.04	0.64
25	3.1	15.04	4.7	70.688	77.5	91.21032	62	96	0.96	0.04	0.62
26	2.95	15.08	4.65	70.122	76.7	91.42373	60	96	0.96	0.04	0.6

Table A10 150kHz Constant Power 180W Fixed Output Voltage 15V

Vin	In	Vout	Iout	Pout	Pin	Eff	Vmax	Vmin	Iripp	Vripp	Da	Dbneg	Db	Da
10	20	15.1	11.2	169.12	200	84.56	21	9	3.6	12	98	0.59	0.41	0.98
11	18	15.1	11.14	168.214	198	84.95657	20	9.6	3	10.4	98	0.63	0.37	0.98
12	15.8	14.98	11.15	167.027	189.6	88.09441	18.6	10.35	2.5	8.25	98	0.73	0.27	0.98
13	14.5	15.2	11.2	170.24	188.5	90.313	17.58	11.09	2	6.49	98	0.8	0.2	0.98
14	13.4	15.1	11.2	169.12	187.6	90.14925	16.8	11.99	1.5	4.81	94	0.98	0.02	0.94
15	13	15.1	11.2	169.12	195	86.72821	21	8	4	13	50	0.55	0.45	0.5
16	11.05	15.12	11.15	168.588	176.8	95.3552	15.42	14.38	0.275	1.04	96	0.96	0.04	0.96
17	10.6	15.15	11.2	169.68	180.2	94.16204	15.51	14.27	0.32	1.24	89	0.96	0.04	0.89
18	10	15.1	11.2	169.12	180	93.95556	15.72	14.21	0.361	1.51	85	0.96	0.04	0.85
19	9.56	15.2	11.21	170.392	181.64	93.80753	15.72	14.08	0.458	1.64	81	0.96	0.04	0.81
20	9	15.17	11.15	169.1455	180	93.96972	15.9	13.81	0.553	2.09	79	0.96	0.04	0.79
21	8.6	15.15	11.185	169.4528	180.6	93.82766	16	13.84	0.639	2.16	70	0.96	0.04	0.7
22	8.2	15.1	11.2	169.12	180.4	93.74723	16.05	13.7	0.685	2.35	68	0.96	0.04	0.68
23	8	15	11.18	167.7	179.4	93.47826	16.2	13.6	0.76	2.6	66	0.96	0.04	0.66
24	7.5	15	11.18	167.7	180	93.16667	16.21	13.6	0.8	2.61	64	0.96	0.04	0.64
25	7.2	15.04	11.12	167.2448	180	92.91378	16.3	13.5	0.853	2.8	62	0.96	0.04	0.62

Table A11: 250 kHz Costant Power 180W Fixed Output Voltage 15V

Vin	In	Vout	Iout	Pout	Pin	Eff	Vmax	Vmin	Iripp	Vripp	Da	Dbneg	Db	Da
10	19.8	15	11	165	198	83.33333	18.59	12.7	1.2	5.89	98	59	0.41	0.98
11	18.1	15.1	11.02	166.402	199.1	83.5771	18.17	12.98	1.1	5.19	98	63	0.37	0.98
12	16.8	15.2	11.15	169.48	201.6	84.06746	17.83	13.3	1	4.53	98	73	0.27	0.98
13	14.8	15.2	11.2	170.24	192.4	88.48233	17.11	13.6	0.752	3.51	98	80	0.2	0.98
14	13.6	15.1	11.2	169.12	190.4	88.82353	16.54	13.9	0.596	2.64	94	98	0.02	0.94
15	13.6	15.1	11	166.1	204	81.42157	17	12	0.4	5	50	55	0.45	0.5
16	11.3	15.12	11.2	169.344	180.8	93.66372	15.3	14.22	0.098	1.08	96	96	0.04	0.96
17	10.65	15.1	11.2	169.12	181.05	93.41066	15.41	14.93	0.115	0.48	89	96	0.04	0.89
18	10.1	15.2	11.2	170.24	181.8	93.64136	15.38	14.8	0.118	0.58	85	96	0.04	0.85
19	9.6	15.2	11.21	170.392	182.4	93.41667	15.42	14.8	0.121	0.62	81	96	0.04	0.81
20	9	15.17	11	166.87	180	92.70556	15.41	14.74	0.122	0.67	79	96	0.04	0.79
21	8.75	15.15	11.23	170.1345	183.75	92.5902	15.4	14.7	0.133	0.7	70	96	0.04	0.7
22	8.35	15.1	11.25	169.875	183.7	92.47414	15.39	14.8	0.14	0.59	68	96	0.04	0.68
23	8	15	11.12	166.8	180.55	92.38438	15.57	14.7	0.156	0.87	66	96	0.04	0.66
24	7.6	15	11.2	168	182.4	92.10526	15.43	14.7	0.167	0.73	64	96	0.04	0.64
25	7.3	15.04	11.15	167.696	182.5	91.88822	15.47	14.56	0.18	0.91	62	96	0.04	0.62

Table A12 : 400kHz Costant Power 180W Fixed Output 15V

Vin	In	Vout	Iout	Pout	Pin	Eff	Vmax	Vmin	Iripp	Vripp	Da	Dbneg	Da
10	20.9	15.1	11.2	169.12	209	80.91866	17.3	12.7	0.514	4.6	98	59	0.98
11	18.68	15.1	11.14	168.214	205.48	81.86393	17	12.98	0.442	4.02	98	63	0.98
12	16.35	15	11.15	167.25	196.2	85.24465	16.63	13.3	0.358	3.33	98	73	0.98
13	14.6	15.2	11.2	170.24	189.8	89.69442	16.17	13.6	0.275	2.57	98	80	0.98
14	13.4	15.1	11.2	169.12	187.6	90.14925	15.88	13.9	0.2	1.98	94	98	0.94
15	13.6	15.1	11.2	169.12	204	82.90196	17	12	0.4	5	50	55	0.5
16	11.9	15.12	11.2	169.344	190.4	88.94118	15.84	14.22	0.18	1.62	96	95	0.96
17	10.8	15.15	11.2	169.68	183.6	92.4183	15.23	14.93	0.028	0.3	95	96	0.95
18	10.2	15.2	11.2	170.24	183.6	92.72331	15.21	14.8	0.029	0.41	90	96	0.9
19	9.7	15.16	11.25	170.55	184.3	92.53934	15.32	14.8	0.039	0.52	84	96	0.84
20	9	15.17	11	166.87	180	92.70556	15.28	14.74	0.034	0.54	79.5	96	0.795
21	8.8	15.15	11.23	170.1345	184.8	92.06412	15.26	14.7	0.035	0.56	75	96	0.75
22	8.3	15.1	11.13	168.063	182.6	92.03888	15.25	14.8	0.036	0.45	73	96	0.73
23	8	15	11	165	179.4	91.97324	15.26	14.7	0.0425	0.56	69.5	96	0.695
24	7.6	15	11.1	166.5	182.4	91.28289	15.28	14.7	0.045	0.58	67	96	0.67
25	7.2	15.04	10.9	163.936	180	91.07556	15.26	14.56	0.044	0.7	63.8	96	0.638

Table A13: Varying Power according to TEG's output power curve, with 250kHz and input impedance matching

P_Teg	Vin	In	Vout	V_nib	Req_Real	Iout	Pin	Pout	Eff	Db	P_nib_ing	eff ing/usc
11.75	5	2.29	3.95	2.5	1.091703	1.33	11.45	5.2535	45.8821	56.5	5.725	0.917642
16.5	6	2.78	4.82	3	1.079137	1.6	16.68	7.712	46.23501	56.5	8.34	0.9247
22.05	7	3.178	5.58	3.5	1.101322	1.85	22.246	10.323	46.40385	56.5	11.123	0.928077
28.4	8	3.635	6.41	3.99	1.097662	2.13	29.08	13.6533	46.95083	56.5	14.50365	0.94137
35.55	9	4.04	7.15	4.49	1.111386	2.386	36.36	17.0599	46.91942	57	18.1396	0.940478
43.5	10	4.5	7.97	4.99	1.108889	2.65	45	21.1205	46.93444	57.02	22.455	0.94057
52.25	11	4.91	8.78	5.49	1.118126	2.9	54.01	25.462	47.14312		26.9559	0.94458
61.8	12	5.4	9.54	6	1.111111	3.2	64.8	30.528	47.11111	57	32.4	0.942222
72.15	13	5.91	10.45	6.49	1.098139	3.46	76.83	36.157	47.06104	56.5	38.3559	0.942671
83.3	14	6.4	11.3	7	1.09375	3.75	89.6	42.375	47.29353	56	44.8	0.945871
95.25	15	6.83	12.05	7.5	1.098097	4.01	102.45	48.3205	47.16496		51.225	0.943299
108	16	7.3	7.56	8.14	1.115068	7.45	116.8	56.322	48.22089	98	59.422	0.947831
121.55	17	7.68	7.95	8.52	1.109375	7.79	130.56	61.9305	47.43451		65.4336	0.946463
135.9	18	8.05	8.35	9	1.118012	8.21	144.9	68.5535	47.3109	97.5	72.45	0.946218
151.05	19	8.65	8.94	9.56	1.105202	8.75	164.35	78.225	47.59659		82.694	0.945957
167	20	9.11	9.41	10.1	1.108672	9.24	182.2	86.9484	47.72141		92.011	0.944978
183.75	21	9.6	9.9	10.6	1.104167	9.7	201.6	96.03	47.63393	95	101.76	0.943691
201.3	22	10	10.31	11.15	1.115	10.15	220	104.6465	47.56659		111.5	0.938534
219.65	23	10.5	10.8	11.55	1.1	10.52	241.5	113.616	47.04596		121.275	0.936846
238.8	24	10.95	11.3	12.15	1.109589	11	262.8	124.3	47.29833		133.0425	0.934288
258.75	25	11.38	11.83	12.87	1.130931	11.56	284.5	136.7548	48.06847		146.4606	0.933731

Table A14 Input and Output Voltage Measure Stage Data

Vin	Vin_filt	Theoretic.	Diff
1		0.05	0.05
2	0.1	0.1	0
3	0.15	0.15	0
4	0.2	0.2	0
5	0.25	0.25	0
6	0.3	0.3	0
7	0.35	0.35	0
8	0.4	0.4	0
9	0.45	0.45	0
10	0.5	0.5	0
11	0.55	0.55	0
12	0.6	0.6	0
13	0.65	0.65	0
14	0.698	0.7	0.002
15	0.76	0.75	-0.01
16	0.8	0.8	0
17	0.84	0.85	0.01
18	0.89	0.9	0.01
19	0.95	0.95	0
20	1	1	0

Table A15: Input and Output Current Measure Stage Data

In	In_filt	I_Theoretic	Retta Gain	Diff in %
0.6	0.056	0.059808	0.093333	6.366801
0.85	0.081	0.084728	0.095294	4.399717
1.45	0.14	0.144536	0.096552	3.13807
2.17	0.215	0.216305	0.099078	0.603335
2.52	0.25	0.251193	0.099206	0.474916
2.9	0.285	0.289071	0.098276	1.408392
3.3	0.33	0.328943	0.1	-0.32129
3.65	0.365	0.363831	0.1	-0.32129
			0.097691	

Table A16: Fourth Order Bessel Filter Magnitude and Phase Datas

freq	Vin	Vout	db	T	delta T	uT	Sfasf
10	4.63	4.63	0	0.1	0.1	1E-07	-0.00036
100	4.63	4.63	0	0.01	0.1	1E-07	-0.0036
1000	4.63	4.63	0	0.001	0.1	1E-07	-0.036
10000	4.63	4.63	0	0.0001	7.2	7.2E-06	-25.92
20000	4.63	4.56	-0.26153	0.00005	4.2	4.2E-06	-30.24
30000	4.63	4.5	-0.49214	3.33333E-05	4.3	4.3E-06	-46.44
40000	4.63	4.4	-0.89065	0.000025	4.19	4.19E-06	-60.336
50000	4.63	4.36	-1.05531	0.00002	3.88	3.88E-06	-69.84
60000	4.63	4.25	-1.52494	1.66667E-05	3.7	3.7E-06	-79.92
70000	4.63	4.19	-1.79222	1.42857E-05	3.744	3.74E-06	-94.3488
80000	4.63	4	-2.69732	0.0000125	3.744	3.74E-06	-107.827
90000	4.63	3.88	-3.32172	1.11111E-05	3.7	3.7E-06	-119.88
100000	4.63	3.75	-4.05301	0.00001	3.7	3.7E-06	-133.2
110000	4.63	3.6	-4.98121	9.09091E-06	3.8	3.8E-06	-150.48
120000	4.63	3.4	-6.39667	8.33333E-06	3.9	3.9E-06	-168.48
130000	4.63	3.3	-7.2015	7.69231E-06	3.78	3.78E-06	-176.904
140000	4.63	3.2	-8.08858	7.14286E-06	3.67	3.67E-06	-184.968
150000	4.63	3	-10.1918	6.66667E-06	3.62	3.62E-06	-195.48
160000	4.63	2.97	-10.5563	0.00000625	3.6	3.6E-06	-207.36
170000	4.63	2.88	-11.7516	5.88235E-06	3.5	3.5E-06	-214.2
180000	4.63	2.77	-13.4788	5.55556E-06	3.45	3.45E-06	-223.56
190000	4.63	2.7	-14.7889	5.26316E-06	3.4	3.4E-06	-232.56
200000	4.63	2.67	-15.417	0.000005	3.2	3.2E-06	-230.4
210000	4.63	2.62	-16.5769	4.7619E-06	3.2	3.2E-06	-241.92
220000	4.63	2.5	-20.2237	4.54545E-06	3.2	3.2E-06	-253.44
250000	4.63	2.44	-22.8493	0.000004	2.9	2.9E-06	-261
300000	4.63	2.4	-25.1794	3.33333E-06	2.5	2.5E-06	-270
350000	4.63	2.34	-30.5563	2.85714E-06	2.2	2.2E-06	-277.2
400000	4.63	2.31	-35.417	0.0000025	2.1	2.1E-06	-302.4
450000	4.63	2.3	-37.9158	2.22222E-06	2	0.000002	-324

Appendix B - Matlab Scripts

The following Matlab code is used to design the dividers as well as the gains for the current measure stage

```
clc
```

```
clear variables
close all
format shortEng
%Con Voc=30V, Imax=25A
%Con Voc=60V, Imax=50A
% Risultati con Filtro Gain= 1;
% Se G_ina=100, R1=6.81k, R2=10k, Gp=0.5949, Imin=12mA,  Imax=50A
% Se G_ina=500, R1=8.6k,R2=1.2k , Gp=0.122,  Imin=11.96mA,Imax=49A
% Se G_ina=500 R1=10k,R2=2.49k, Gp=0.199, Imin=7.3mA,Imax=30.1A;
```

```
%Divider
R1=7e+3;
R2= 10e+3;
Gp= R2/(R2+R1) %Gain Divider
G_f=1;%Gain filter stage
G_ina=500; %Gain Ina
Rs=1e-3; %Shunt Resistor
V_Max_Ina=5;
```

```
V_R2=Gp*V_Max_Ina
```

```
Imin=3/(2^12 -1)* 1/(Gp*G_ina*Rs*G_f) %Minumum current
Imax=3/(Gp*G_ina*Rs*G_f) %Max current readeable
```

```
%Value read my uC
I_read_min=Imin*(Gp*G_ina*Rs*G_f)
I_read_max=Imax*(Gp*G_ina*Rs*G_f)
```

The following code is used to compare the 4 switches

```
%EPC2103 Half Bridge Device Q1 e Q2

if transistor==1
     %Charges data
    Qg=6.5*10^-9; %total gate charge
    Qgd=1.1*10^-9 ; % gate to drain charge
    Qrr=0; % reverse recovery charge

    %Capacitances
    Ciss= 880*10^-12; %Input MOSFET capacitance at Vds (from the curves)
    Coss=790*10^-12; % Output MOSFET capacitance

    %Voltages
    Vdiode=0; %Since Qrr=0
    Vbreak=80; %Minimum breakdown voltage
    Vth= 1.3 ; % Gate threshold voltage  (Vgs(th))
    Vpl=2.3 ; % Miller plateau voltage from Gate Charge function
    Vgs= 5.8; % actual gate-source voltage, coming from the driver

    %Resistances
    Rg= 0.5 + 5; % gate resistance of the transistor + driver output resistance
    Ron=7*10^-3; %transistor on resistance HOT, 125 Degrees
    RJC=0.3; %Thermal resistance Junction to case
    RJB=2.2; %Thermal resistance Junction to Board
    RJA=42; %Thermal resistance Junction to Ambient
end
%EPC2065 Single GaN
if transistor==2
    %Charges data
    Qg=9.4*10^-9; %total gate charge
    Qgd=1.7*10^-9 ; % gate to drain charge
    Qrr=0; % reverse recovery charge

    %Capacitances
    Ciss= 1449*10^-12; %Input MOSFET capacitance at Vds (from the curves)
    Coss=801*10^-12; % Output MOSFET capacitance

    %Voltages
    Vdiode=0; %Since Qrr=0
    Vbreak=80; %Minimum breakdown voltage
    Vth= 1.2 ; % Gate threshold voltage  (Vgs(th))
    Vpl=2.3 ; % Miller plateau voltage from Gate Charge function
    Vgs= 5.8; % actual gate-source voltage, coming from the driver

    %Resistances
    Rg= 0.5 + 5; % gate resistance of the transistor + driver output resistance
    Ron=5*10^-3; %transistor on resistance Degrees
    RJC=0.5; %Thermal resistance Junction to case
    RJB=1.4; %Thermal resistance Junction to Board
    RJA=53; %Thermal resistance Junction to Ambient
```

```
%EPC 2206 Single GaN
if transistor==3
    Qg=15*10^-9; %total gate charge
    Qgd=3*10^-9 ; % gate to drain charge
    Qrr=0; % reverse recovery charge

    %Capacitances
    Ciss= 1600*10^-12; %Input MOSFET capacitance at Vds (from the curves)
    Coss=1150*10^-12; % Output MOSFET capacitance

    %Voltages
    Vdiode=0; %Since Qrr=0
    Vbreak=80; %Minimum breakdown voltage
    Vth= 2.5 ; % Gate threshold voltage  (Vgs(th))
    Vpl=2 ; % Miller plateau voltage from Gate Charge function
    Vgs= 10; % actual gate-source voltage, coming from the driver

    %Resistances
    Rg= 0.3 + 5; % gate resistance of the transistor + driver output resistance
    Ron=2*2.2*10^-3; %transistor on resistance
    RJC=0.4; %Thermal resistance Junction to case
    RJB=1.1; %Thermal resistance Junction to Board
    RJA=42; %Thermal resistance Junction to Ambient
end
```

```
%FDB035N10A Best SiC MoS
if transistor==4
    %Charges data
    Qg=90*10^-9; %total gate charge
    Qgd=25*10^-9 ; % gate to drain charge
    Qrr=129*10^-9; % reverse recovery charge

    %Capacitances
    Ciss= 5500*10^-12; %Input MOSFET capacitance at Vds (from the curves)
    Coss=2500*10^-12; % Output MOSFET capacitance

    %Voltages
    Vdiode=1; %body diode forward voltage
    Vbreak=100; %Minimum breakdown voltage
    Vth= 3 ; % Gate threshold voltage  (Vgs(th))
    Vpl=5 ; % Miller plateau voltage from Gate Charge function
    Vgs= 10; % actual gate-source voltage, coming from the driver

    %Resistances
    Rg= 1.1 + 5; % gate resistance of the transistor + driver output resistance
    Ron=0.0035*2; %transistor on resistance
    RJC=0.45; %Thermal resistance Junction to case
    RJA=62; %Thermal resistance Junction to Ambient

end
```

Conduction Losses for each of the transistors

```
for i =1:length(Vmp)

    if(Vmp(i) < (Vout-p) )
       P_cond(i)=(Imp(i))^2*(Ron+Dboost(i)*Ron+(1-Dboost(i))*Ron);
    end
    if(Vmp(i) >= (Vout-p) &&  Vmp(i) < (Vout))
       P_cond(i)=(Iave(i))^2*(Dbuckmax*Ron+(1-Dbuckmax)*Ron+Dboost(i)*Ron+(1-
Dboost(i))*Ron);
    end
    if(Vmp(i) < (Vout+p) &&  Vmp(i) >= (Vout))
        P_cond(i)=Io(i)^2*((1-Dboostmin)*Ron+Dboostmin*Ron+Dbuck(i)*Ron+(1-
Dbuck(i))*Ron);
    end
    if(Vmp(i) >= (Vout+p) )
       P_cond(i)=Io(i)^2*(Ron+Dbuck(i)*Ron+(1-Dbuck(i))*Ron);
    end
end
figure
plot(Vmp,P_cond)
grid on
grid minor
xlabel('Vmp [V]'); ylabel('P_{cond}[W]');
```

Vishay Method Script to calculate the rise and fall time

```
%VISHAY METHOD
for i=1:length(Vpl)
        tir(i)=Rg*Ciss*log((Vgs-Vth)/(Vgs-Vpl(i)));
        tif(i)=Rg*Ciss*log(Vpl(i)/Vth);
        tvr(i)=(Rg*Qgd)/Vpl(i);
        tvf(i)=(Rg*Qgd)/(Vgs-Vpl(i));
    end
tr=0;
tf=0;
for i=1:length(tvf)
    tr=tr+tvf(i)+tir(i);
    tf=tf+tvr(i)+tif(i);
end
tr=tr/length(tvf)
```

Switchig Losses Matlab Script

```
for i =1:length(Vmp)

    %For Boost Region
    if(Vmp(i) < (Vout-p) )
       P_sw(i)=Vout*Imp(i)*fsw*(tf+tr)/2;
    end
    %For Buck Region
    if(Vmp(i) >= (Vout+p) )
       P_sw(i)=Vmp(i)*Io(i)*fsw*(tf+tr)/2;
    end
    %For buck-boost region
    if(Vmp(i) >= (Vout-p) && Vmp(i) < (Vout+p) )
       P_sw(i)=Vout*Iave(i)*fsw*(tf+tr)/2 +
Vmp(i)*Iave(i)*fsw*(tf+tr)/2;
    end
end
figure
plot(Vmp,P_sw)
grid on
grid minor
xlabel('Vmp [V]'); ylabel('P_{sw}[W]');
```

Dead Time Calculation Script

```
%Dead Time from Vichay Notes

for i=1:length(Vpl)
        tdon=Rg*Ciss*log(1/(1-(Vth/Vgs)));
        tdoff_v(i)=Rg*Ciss*log(Vgs/Vpl(i));
end
%average value of tdoff
tdoff=0;
for i=1:length(Vpl)
    tdoff=tdoff+tdoff_v(i);
end
tdoff=tdoff/length(Vpl);
tswon=tr+tdon
tswoff=tf+tdoff
```

Gate Drive Losses Script

```
for i =1:length(Vmp)
    if(Vmp(i) < (Vout-p) )
       P_gatedrive(i)=Qg*Vgs*fsw*2;
    end
    if(Vmp(i) >= (Vout+p) )
       P_gatedrive(i)=Qg*Vgs*fsw*2;
    end
    if(Vmp(i) >= (Vout-p) && Vmp(i) < (Vout+p) )
       P_gatedrive(i)=Qg*Vgs*fsw*4;
    end
end
P_gatedrive(i)=Qg*Vgs*fsw*2;
```

Output Capacitance Losses Script

```
for i =1:length(Vmp)
    if(Vmp(i) < (Vout-p) )
       P_coss(i)=Coss*fsw*(Vout^2);
    end
    if(Vmp(i) >= (Vout+p) )
       P_coss(i)=Coss*fsw*(Vmp(i)^2);
    end
    if(Vmp(i) >= (Vout-p) && Vmp(i) < (Vout+p) )
       P_coss(i)=Coss*fsw*(Vout^2+Vmp(i)^2);
    end
end
```

Dead Time Losses Script

```
for i =1:length(Vmp)

    if(Vmp(i) < (Vout-p) )
       P_dt(i)=Vdiode*Imp(i)*(tswon+tswoff);
    end
    if(Vmp(i) >= (Vout+p) )
       P_dt(i)=Vdiode*Io(i)*(tswon+tswoff);
    end
    if(Vmp(i) >= (Vout-p) && Vmp(i) < (Vout+p) )
       P_dt(i)=2*Vdiode*Iave(i)*(tswon+tswoff);
    end
end
```

Reverse Recovery Losses

```
for i =1:length(Vmp)

    if(Vmp(i) < (Vout-p) )
       P_rr(i)=2*Qrr*fsw*Vout;
    end
    if(Vmp(i) >= (Vout+p) )
       P_rr(i)=2*Qrr*fsw*Vmp(i);
    end
    if(Vmp(i) >= (Vout-p) && Vmp(i) < (Vout+p) )
       P_rr(i)=2*Qrr*fsw*(Vout+Vmp(i));
    end
end
```

This script is used to calculate the Duty Cycle

```
p=2; %half the amount of voltage that separates buck and boost regions

for i =1:length(Vmp)
    Dboost(i)=0;
    Dbuck(i)=1;
    if(Vmp(i) < (Vout-p) )
        Dboost(i) = 1 - Vmp(i)/Vout; % Boost CCM
        Dbuck(i)=0.96;
    end
    if(Vmp(i) > (Vout+p) )
        Dbuck(i) = Vout/Vmp(i); % Buck CCM
        Dboost(i)=0.04;
    end
end
Dbuckmax=0.95;

Dboostmin=0.05;
for i=1:length(Vmp)
    if Vmp(i)>=Vout-p && Vmp(i)<Vout
        Dboost(i)=1-Vmp(i)/Vout*Dbuckmax;
        Dbuck(i)=Dbuckmax;
    end
    if Vmp(i)<=Vout+p && Vmp(i)>=Vout
        Dbuck(i)=Vout/Vmp(i)*(1-Dboostmin);
        Dboost(i)=Dboostmin;
    end
end
figure

plot(Vmp,Dbuck)
hold on
plot(Vmp,Dboost)
grid on
grid minor
hold on
xline(Vout-p);
hold on
xline(Vout+p);
title('Duty cycle');
xlabel('Vmp [V]'); ylabel('Duty cycle');
legend('Dbuck','Dboost');
```

This script is used to calculate the minimum inductance for CCM

```
%LIMITED RIPPLE Formula Version

for n = 1:length(fsw_v)
    for i =1:length(Vmp)
        if(Vmp(i) < (Vout) )
            %boost
            L_v_k(i,n) = Vmp(i)^2 * (Vout-Vmp(i)) / (Io(i) * Vout^2 * Kind * fsw_v(n));
        end
        if(Vmp(i) >= (Vout) )
            %buck
            L_v_k(i,n) = Vout * (Vmp(i) - Vout) / ( Io(i) * Vmp(i) * Kind * fsw_v(n) );
        end
    end
end


%LIMIT CONDITION
for n = 1:length(fsw_v)
    for i =1:length(Vmp)
        if(Vmp(i) < (Vout) )
            %boost
            L_v(i,n) = (Ro(i)*(1-Dboost(i))^2*Dboost(i))/(2*fsw_v(n));
        end
        if(Vmp(i) >= (Vout) )
            %buck
            L_v(i,n) = (Ro(i)*(1-Dbuck(i)))/(2*fsw_v(n));
        end
    end
end
figure
plot(Vmp, L_v); grid on;
grid minor
title('Inductor L');
xlabel('Vmp [V]'); ylabel('L [H]');
legend('200 kHz','250 kHz', '300 kHz','350 kHz','400 kHz','450 kHz','500 kHz');
```

This script is used to calculate the Inductor Maximum Current

```
for i =1:length(Vmp)

    if(Vmp(i) < (Vout-p) )
       Imax(i)=Imp(i)+(Vmp(i)*Dboost(i))/(fsw*L*2);
    end
    if(Vmp(i) >= (Vout-p) &&  Vmp(i) < (Vout))
       Imax(i)=Iave(i)+(Vmp(i)*(Vout-Vmp(i)*Dbuckmax))/(2*fsw*L*Vout);
    end
    if(Vmp(i) < (Vout+p) &&  Vmp(i) >= (Vout))
       Imax(i)=Iave(i)+(Vout*(Vmp(i)-Vout*(1-
Dboostmin)))/(2*fsw*L*Vmp(i));
    end
    if(Vmp(i) >= (Vout+p) )
       Imax(i)=Io(i)+((Vmp(i)-Vout)*Dbuck(i))/(fsw*L*2);
    end
end
figure
plot(Vmp,Imax)
grid on
grid minor
xlabel('Vmp [V]'); ylabel('I_{Lmax}[A]');
```

This script is used to estimate the Inductor Current Ripple

```
for i =1:length(Vmp)

    if(Vmp(i) < (Vout-p) )
       Irip(i)=(Vmp(i)*Dboost(i))/(fsw*L);
    end
    if(Vmp(i) >= (Vout-p) &&  Vmp(i) < (Vout))
       Irip(i)=(Vmp(i)*(Vout-Vmp(i)*Dbuckmax))/(fsw*L*Vout);
    end
    if(Vmp(i) < (Vout+p) &&  Vmp(i) >= (Vout))
       Irip(i)=(Vout*(Vmp(i)-Vout*(1-Dboostmin)))/(fsw*L*Vmp(i));
    end
    if(Vmp(i) >= (Vout+p) )
       Irip(i)=((Vmp(i)-Vout)*Dbuck(i))/(fsw*L);
    end
end
figure
plot(Vmp,Irip)
grid on
grid minor
xlabel('Vmp [V]'); ylabel('I_{Lrip}[A]');
```

This two scripts are used to calculate the RMS current of the input and outpu capacitors

```
for i=1:length(Vmp)

    if(Vmp(i) > (Vout) )
        ICin_rms(i) = Io(i)*sqrt((Vout /Vmp(i))*(1- Vout / Vmp(i)));
    end
    if(Vmp(i) <= (Vout) )
       ICin_rms(i)=(Vmp(i)*Dboost(i))/(fsw*L*sqrt(12));
    end
end
figure
plot(Vmp,ICin_rms)
grid on
grid minor
xlabel('Vmp [V]'); ylabel('ICin_{rms}[A]');
```

```
for i=1:length(Vmp)

    if(Vmp(i) < (Vout) )
        ICout_rms(i) = Io(i)*sqrt((Vout /Vmp(i))-1);
    else
        ICout_rms(i) =0;
    end
    if(Vmp(i) >= (Vout) )
       ICout_rms(i)=((Vmp(i)-Vout)*Dbuck(i))/(fsw*L*sqrt(12));
    end
end
figure
plot(Vmp,ICout_rms)
grid on
grid minor
xlabel('Vmp [V]'); ylabel('ICout_{rms}[A]');
```

This three scripts are used to estimate the Inductor Losses, Shunt Losses and Capacitor Losses

```
ESR_L=0.97*10^-3; %inductors equivalent series resistance [ohm]

for i =1:length(Vmp)
    P_L(i)=Iave(i)^2*ESR_L;
end
```

```
ESR_Cin=0.004/5; %input capacitor equivalent series resistance [ohm]

ESR_Cout=0.004/5; %output capacitor equivalent series resistance
[ohm]
for i =1:length(Vmp)
    P_Cin(i)=ICin_rms(i)^2*ESR_Cin;
    P_Cout(i)=ICout_rms(i)^2*ESR_Cout;
end
```

```
Rshunt=0.001;

RshuntL=0.01;
for i =1:length(Vmp)
    P_shuntInductor(i)= Iave(i)^2*RshuntL;
    P_shuntOut(i)=Io(i)^2*Rshunt;
    P_shuntIn(i)=Imp(i)^2*Rshunt;
end
figure
plot(Vmp,P_shuntInductor,'DisplayName','ShuntInductor')
hold on
plot(Vmp,P_shuntOut,'DisplayName','ShuntOut')
hold on
plot(Vmp,P_shuntIn,'DisplayName','ShuntIn')
```

Appendix -C Simscape Model

The Simscape Model of the Nibb is showed in fig C.1 and C.2.
It gives the same result of the LTSpice Simulation.
To understand better the model, here there are some consideration

Voltage sensor (Red) : Used to measure the voltage of the device
Current Sensor(Green) : Used to measure the current
Plot view (Yellow): Used to have a graphical representation of the measure

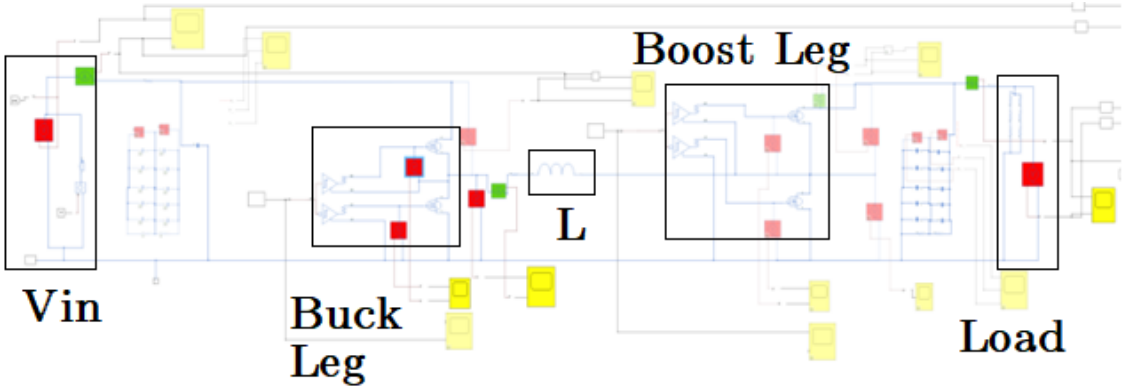


Fig C.1 Power Section of the NIBB Simscape Model

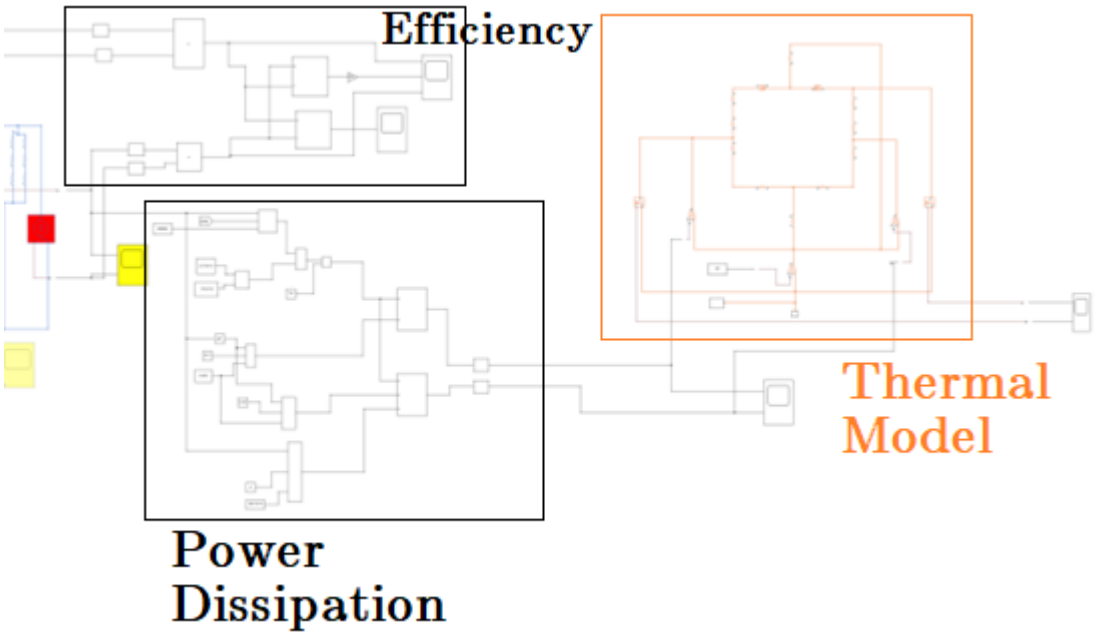


Fig C.2 Effiiency,Power Dissipation and Thermal model of NIBB Simscape Model

Pulse Generator Configuration

Before using the Half Bridge Gate Driver it is necessary to configure a pulse generator by setting

1. Amplitude: 5V
2. Period : 1/250kHz
3. Pulse Width: It is equivalent to the duty Cycle

Gate and Mosfet Configuration

It is necessary to understand all the parameters configuration of the Gate Drive and the Mosfet in order to avoid incorrect simulation results.

In the Half Bridge Gate Drive it is necessary to set

1. On-state gate-source voltage: Must at least 10V (15V)
2. Off-state gate-source voltage: 0V
3. Low/High Side Propagation Delay 0-1 1-0 : Must match propagation delay of the driver (50ns)
4. Dynamic parametrization: can be given by output gate resistance or rise/fall time found in the datasheet(1-5ns)
5. Dead time: Dead time between the high side and low side PWM waveform (50ns). It is mandatory because it avoids shorts and overcurrent in devices.

In the Mosfet it is necessary to set properly, from the datasheet of EPC2206:

1. Drain-source on resistance, R˙DS(on):0.003
2. Drain current, Ids, for R˙DS(on):6A
3. Gate-source voltage, Vgs, for R˙DS(on): 10V
4. Gate-source threshold voltage, Vth: 1V
5. Measurement temperature: 25
6. Input capacitance, Ciss: 1600 pF
7. Reverse transfer capacitance, Crss : 0
8. Output capacitance, Coss : 1150 pF

Inductor Configuration

For the inductor it is necessary to specify the value (6.8uH) and it's ESR, found in the datasheet (0.88mΩ)

If everything was done correctly, the waveform generated by the Half bridge Gate driver should be like shown in fig C.3
The duty Cycle is set to 77% (High side blue waveform) with a dead time of 50ns

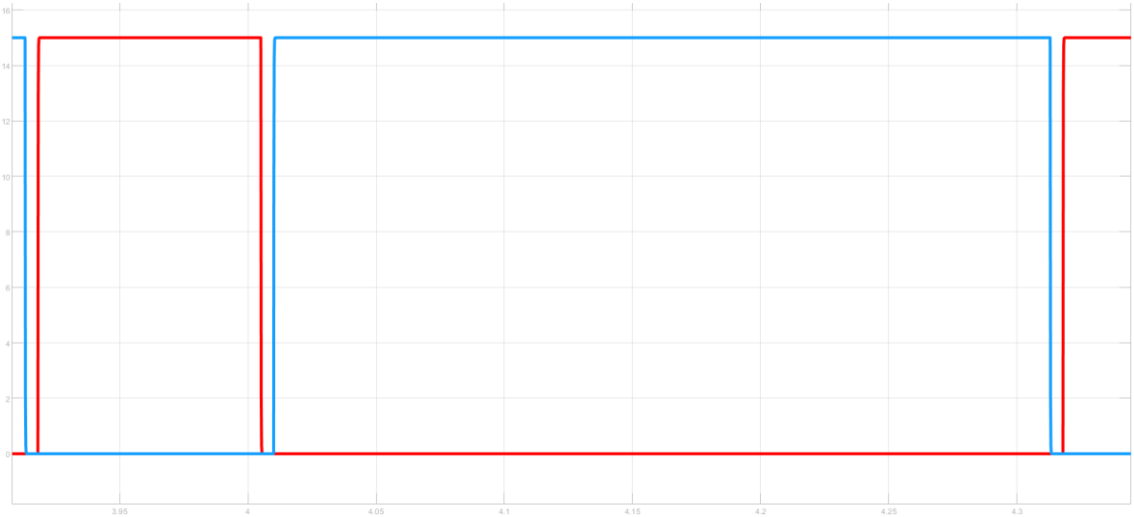


Fig C.3 In blue the high side waveform, in red the low side one.

By putting Vin=20V and Duty Cycle = 77% with a load of 1.5Ω is it possible to reproduce the 180W Testing with constant output voltage and input power.
In fig C.4 it is shown the switching voltage as well as the current inductor, while in fig C.5 both the output voltage and current are shown.

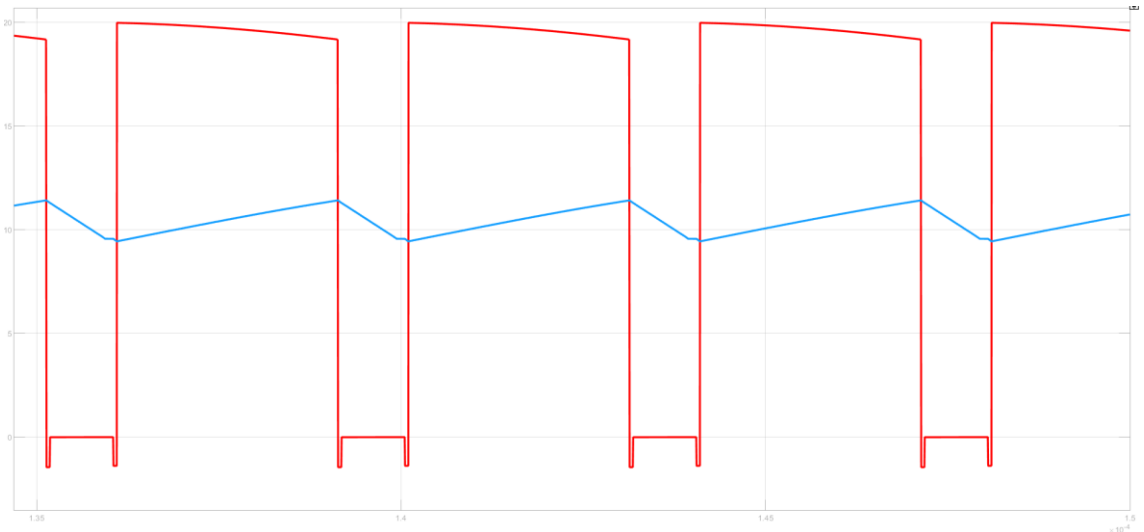


Fig C.4 Switching Voltage (red) with dead time effect and Inductor Current (blue) Plot

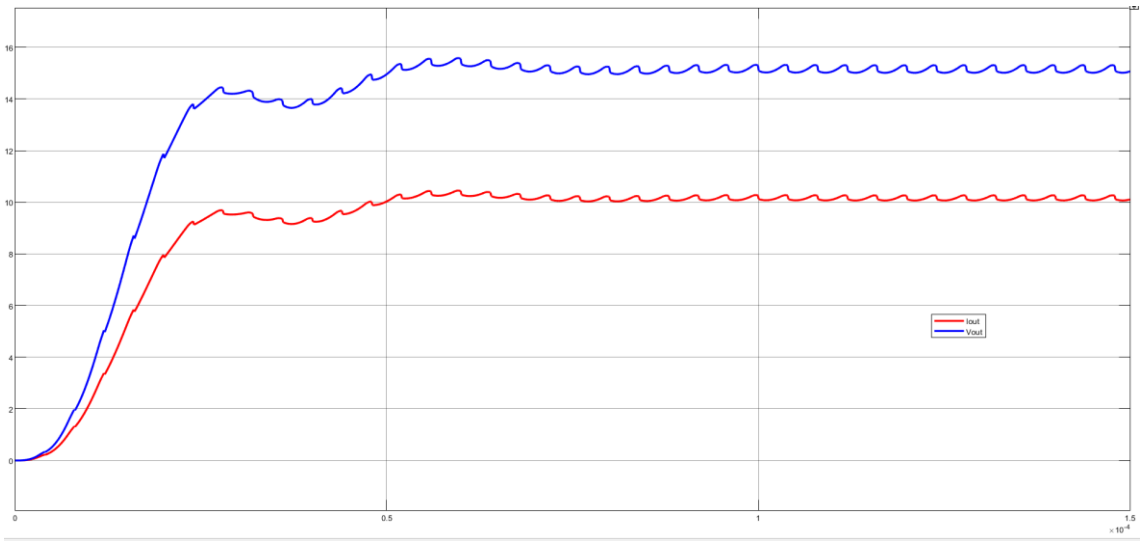


Fig C.5 Output Current (red) and Output Voltage(blue) Plot.
Their rms value are respectively 10.5A and 15V

Efficiency Estimation

In fig C.6 it is shown how the efficiency is calculated using the Simulink blocks. It is important to highlight that it is mandatory to use the RMS block set to the fundamental frequency harmonics at 250kHz to have a more reliable result.
Plot are sown in fig C.7, where it can be seen that the efficiency is around 92%, which is not far from the experimental result.

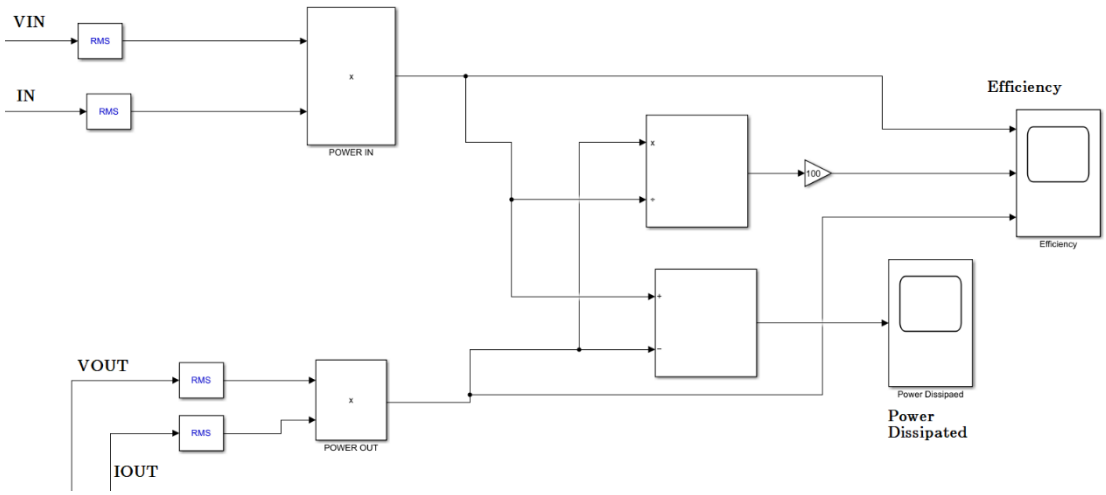


Fig C.6 Efficiency Calculation using Simulink Blocks

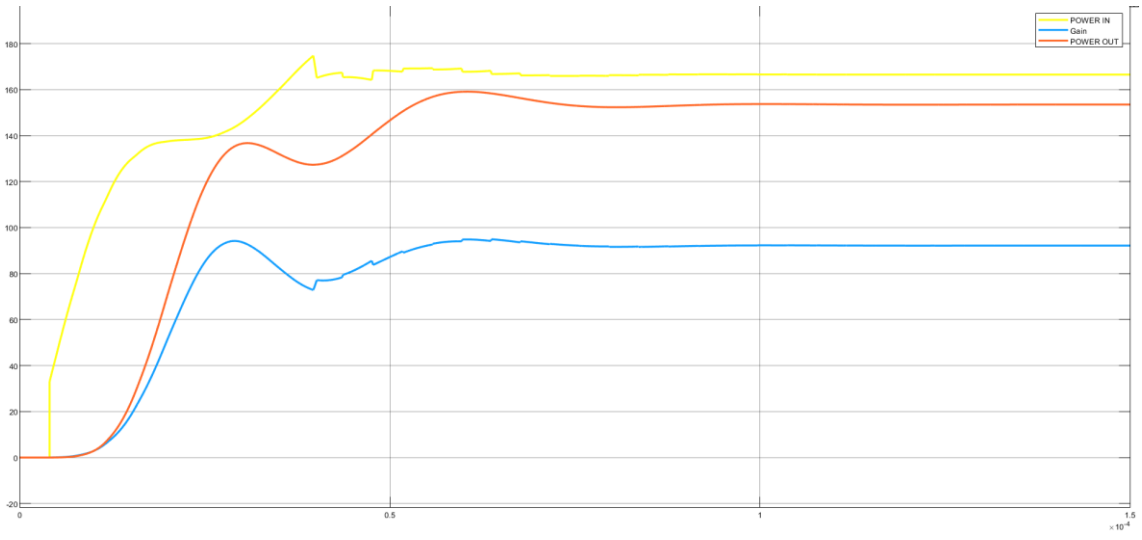


Fig C.7 Plot result of the scheme in fig C.6. In blue is represented the efficiency, while in yellow and red the input and output power respectively.

Temperature Estimation

From the Power Losses model in fig C.8 it is possible to study only the power dissipated by the two GaNs.
Only the Switching Losses, Conduction Losses and Dead Time losses were taken into account because they have the most impact on the efficiency.
By feeding those two power into the thermal model in Fig C.9 it is possible to estimate the junction temperature of the two GaNs.

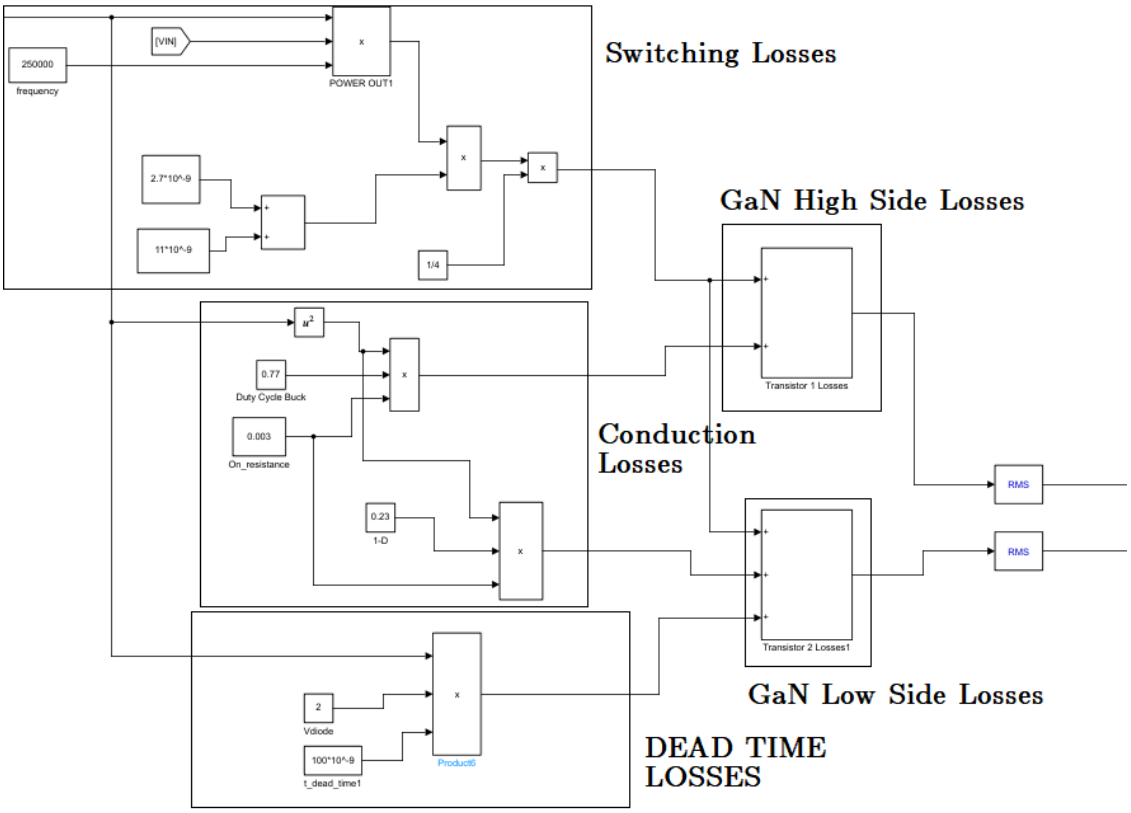


Fig C.8 High side and Low Side Losses to be fed in the Thermal model in fig C.9 using the Power Model in C.5

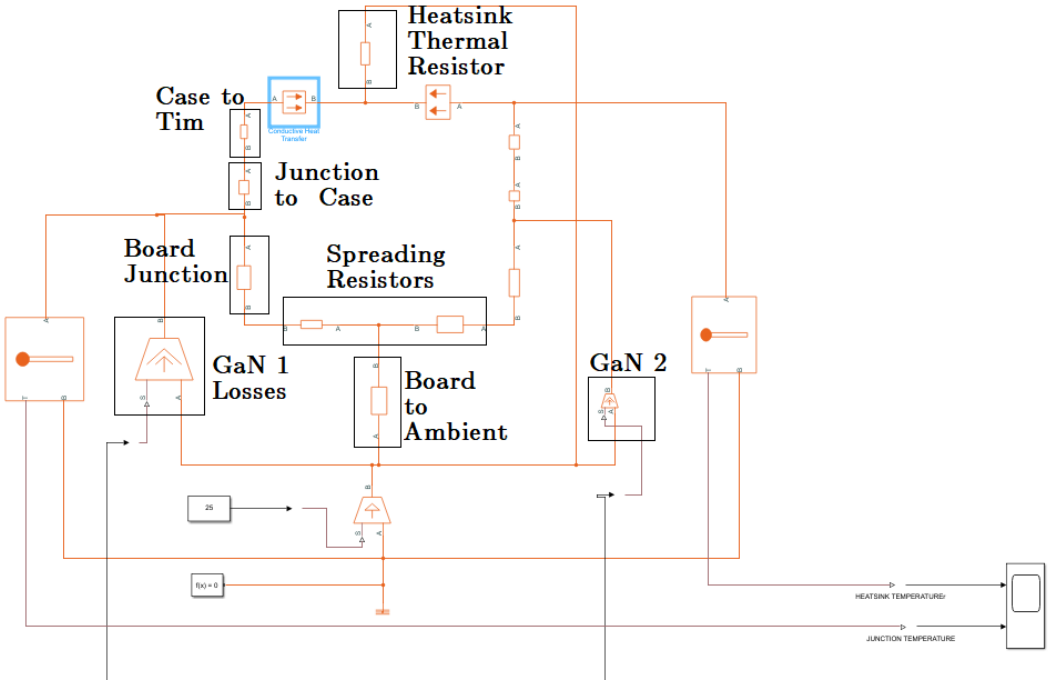


Fig C.9 Thermal Model , equivalent in values of LTSpice. Temperature sensors have the same role of the voltage sensors in the thermal domain.

The plot results can be seen in fig C.10. The effect of the thermal capacitance is neglected, hence the transient effect could not be modelled accordingly. After the transient the temperature of the junction reaches 48 C and the heatsink temperature is very near to the junction because the simulation supposes a small heatsink with a thermal resistance with 74 C/W. It is necessary a more efficient heatsinke for higher powers.

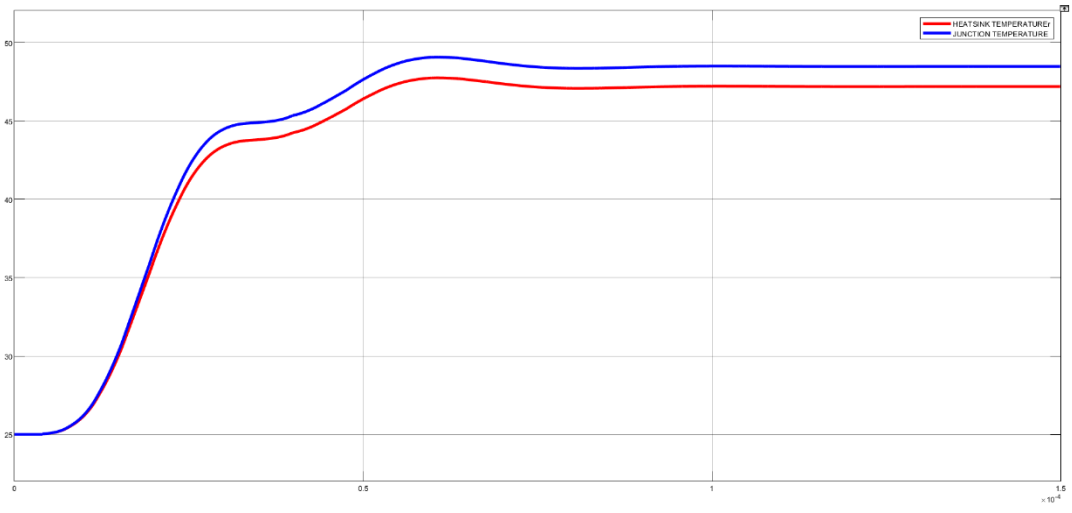


Fig C.10 Plot view of thermal Model. In blue the junction temperature , in red the heatsink temperature.

Appendix -D LTSpice Model

Along the SimScape model in the Appendix C, here it presented also the LTSpice model of the NIBB. (fig D.1)
Before commenting the simulation results it is necessary to understand how the pulses were set.

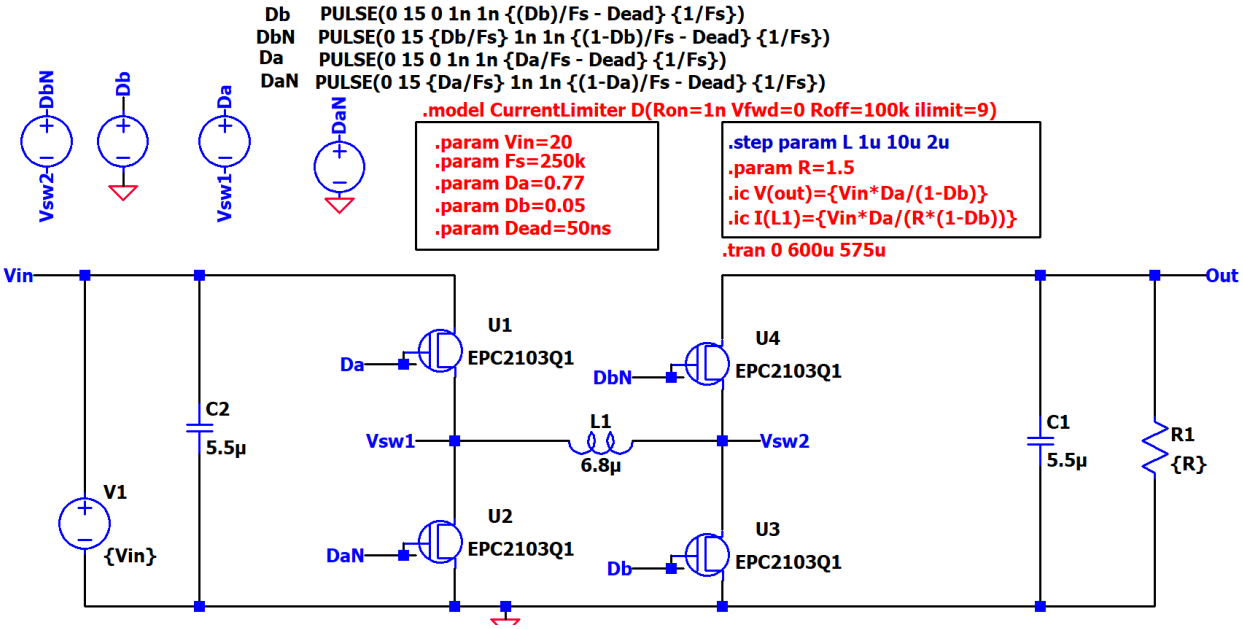


Fig D.1 LTSpice Model of NiBB

In particular:

Pulse(V1 V2 Tdelay Trise Tfall Ton Tperiod Ncycles)

- V1 and V2 are equivalent to Voff and Von: set to 0 and 15
- Tdelay must be set to Da/Fs and Db/Fs only in DaN and DbN
- Trise, Tfall. Set to 1n since it is a square waveform
- Ton: for the high side, set to Da/Fs - Dead. Dead time is mandatory to avoid overcurrent and short circuits
- Nycles: Number of cycles desired by the user. Leave blank if the waveform is periodic.

In fig D.2 it is possible to see the two gate driver, very similar to the SimScape models.

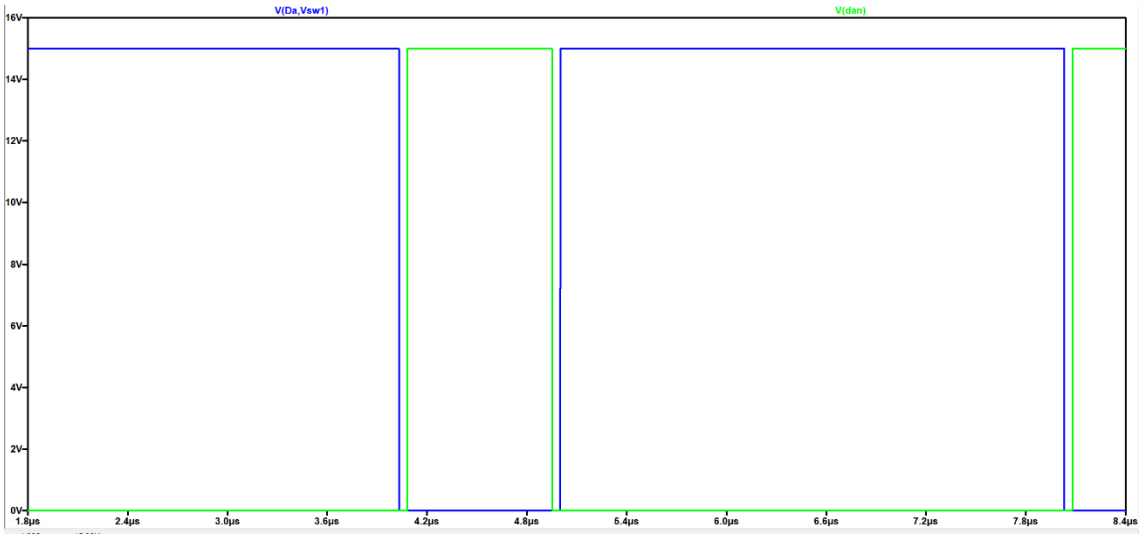


Fig D.2 High side (Blue) and Low Side(Green) Gate Waveform

The .IC statement is used to set the initial condition of the circuit. By charging the output capacitor at the expected voltage(15V) and by imposing the output current as the initial state of the inductor current, the transient is greatly reduced and the simulation in faster. In fig D.3 it is shown the switching node voltage as well as the inductor current, while in fig D.4 it is shown the output voltage and current.

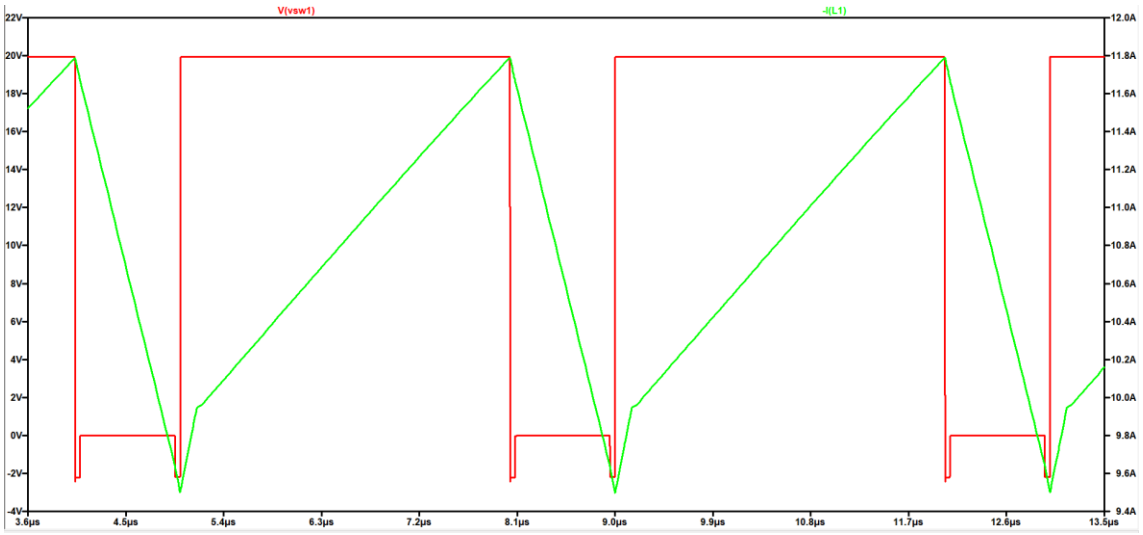


Fig D.3 Simulation results of Nibb Spice Model. In red the voltage node switching, in green the inductor current

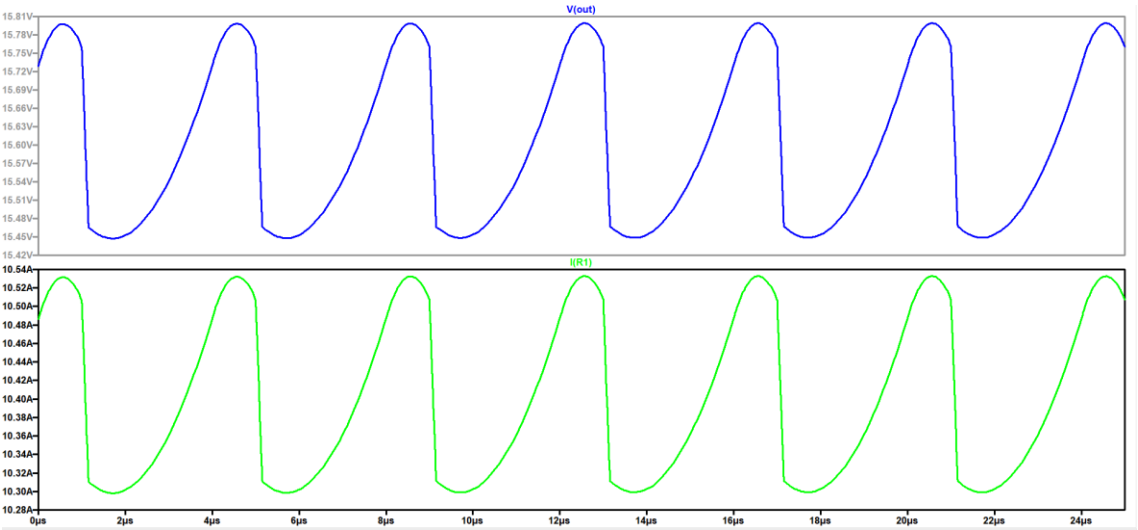


Fig D.4 Simulation results of Nibb Spice Model. In blue, the output voltage (15Vrms) and in green the output current (10.5A rms)

It is even possible to simulate a better behaviour of the gate drive voltage by adding the propagation delay as well as rise/fall time effect, like shown in the circuit in fig D.5 and its result in fig D.6.

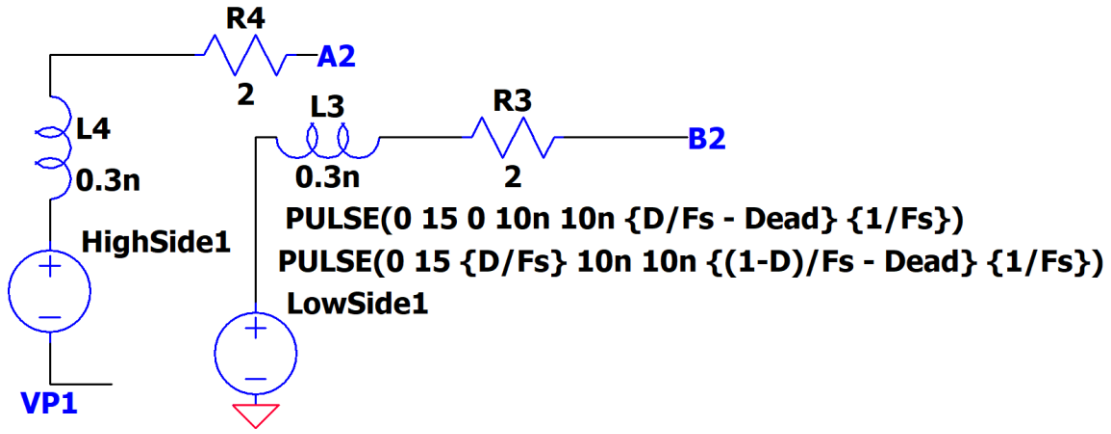


Fig D.5 Propagation Delay Simulation by adding inductance and series resistance to both pulses.

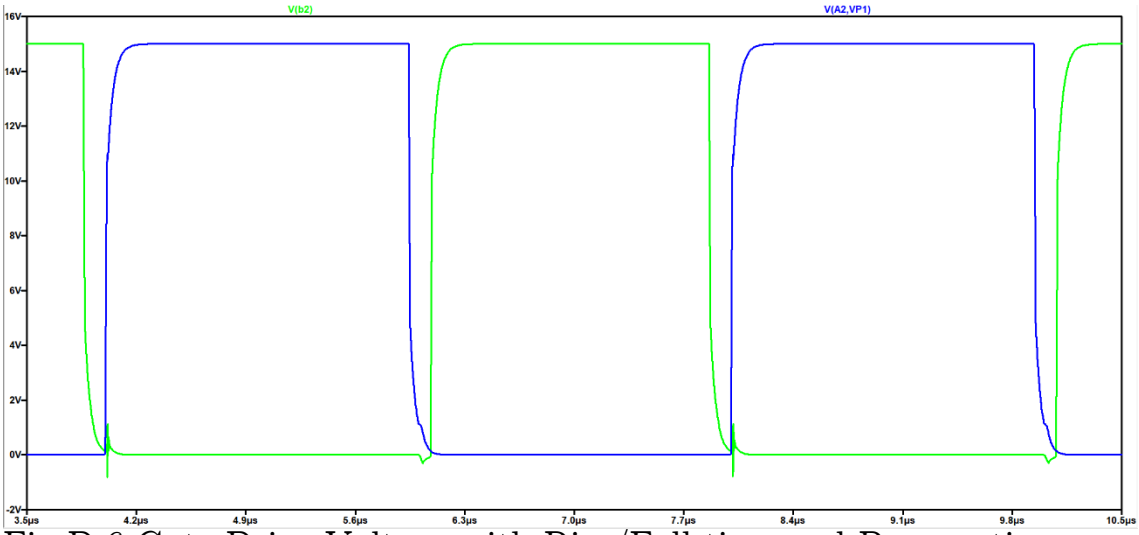


Fig D.6 Gate Drive Voltage with Rise/Fall time and Propagation Delay effect

From the plot in fig D.6 it is clear that this gate drive voltage is more reliable than the ideal, since it is . This however will slow the simulation since it adds more voltage node to be computed by LTSpice.

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