Comparison of AC/DC converters for MVDC applications

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A mis padres Héctor y Mariela
por darme la confianza para seguir mis sueños

Y a mi hermano Héctor y mi hermana Juliana
por estar a mi lado en todas nuestras aventuras

Abstract

In order to achieve the net zero CO_2 emissions goal and keep the world temperature from increasing beyond the 1.5°C threshold, several nations and institutions have established a pathway with measures that should be followed until 2050. One of the most significant ones is the need of integrating large shares of Renewable Energy Sources and shift from conventional internal engine vehicles to Electric Vehicles. Both of these actions will have a significant impact on the current AC electrical network.

The current power system will have to shift from a top-down AC grid architecture to a hybrid AC/DC grid in the transmission and distribution levels. Medium Voltage DC network (MVDC) will play a key role in the future to support the existing distribution system. To allow this hybridization, the use of power converters is essential, thus, studying this technology and determining which of the topologies is more suited to a certain application is of importance.

In this master thesis, a study of two interesting topologies of AC-DC converters is done, namely the Modular Multilevel Converter (MMC) and the Neutral Point Clamped Converter (NPC). The objective is to compare these two topologies in terms of sizing and losses for MVDC applications. For this, a general methodology for the design and evaluation of AC-DC converters is proposed. This methodology includes important steps such as the consideration of the grid requirements, the possibility to do the design considering different operating points, the validation of the design and the compliance with the grid requirements using a transient simulation and the evaluation of the obtained design using Key Performance Indicators (KPIs).

For the case study, a wide range of voltage and power levels is analysed, looking towards finding the point where one converter topology is preferred over the other one. A tool developed in MATLAB was used to do the rapid design and calculation of KPIs for both topologies. The results are shown as the evolution of the different design parameters and KPI along the MV range.

Abstract

Ai fini del raggiungimento dell'obiettivo di zero emissioni nette di CO2 per la limitazione dell'aumento della temperatura mondiale non oltre la soglia di 1,5°C, diverse nazioni e istituzioni hanno stabilito un percorso con misure da conseguire fino entro il 2050. Una delle misure più significative è la necessità di integrare grandi quote di fonti energetiche rinnovabili e passare dai veicoli convenzionali con motore a combustione interna ai veicoli elettrici. Entrambe queste azioni avranno un impatto significativo sull'attuale rete elettrica AC.

L'attuale sistema di alimentazione dovrà passare da un'architettura di rete AC top-down a una rete ibrida AC/DC nei diversi livelli di trasmissione e distribuzione. La rete a media tensione DC (MVDC) svolgerà nel futuro un ruolo chiave di supporto a tutto il sistema di distribuzione. Per consentire questa ibridazione, l'uso di convertitori elettronici di potenza diventa essenziale; quindi è importante studiare queste tecnologie ed individuare la topologia più adatta per una specifica applicazione.

In questa tesi di laurea viene svolto uno studio di due topologie di convertitori AC-DC; il convertitore MMC (Modular Multilevel Converter) e il convertitore NPC (Neutral Point Clamped converter). L'obiettivo è confrontare queste due topologie in termini di dimensionamento e perdite per le applicazioni MVDC. Viene dunque proposta una metodologia generale per la progettazione e la valutazione dei convertitori AC-DC. La suddetta metodologia comprende passaggi importanti come la considerazione dei requisiti di rete, la possibilità di eseguire il progetto considerando diversi punti di lavoro, la convalida del progetto e la conformità ai requisiti di rete mediante una simulazione dinamica e la valutazione mediante particolari indicatori chiave KPI (Key Performance Indicator).

Per il caso di studio, viene analizzata un'ampia gamma di livelli di tensione e potenza, cercando di trovare in quali situazioni una topologia di convertitore è più conveniente rispetto all'altra. Uno strumento sviluppato in ambiente MATLAB è stato utilizzato per eseguire la progettazione rapida e il calcolo dei KPI per entrambe le topologie. I risultati finali sono presentati illustrando l'evoluzione dei diversi parametri di progettazione e KPI in funzione del valore di tensione nominale della rete MVDC.

List of abbreviations

2L VSC	Two Level Voltage Source Converter
3L NPC	Three Level Neutral Point Clamped converter
3L VSC	Three Level Voltage Source Converter
5L ANPC	Five Level Active Neutral Point Clamped Converter
AC	Alternating Current
AI	Artificial Intelligence
BCA	Balancing Capacitor Algorithm
BESS	Battery Energy Storage Systems
BJT	Bipolar junction transistor
C3L-NPC	Cascaded 3 level NPC
CAPEX	Capital expenditure
CHB	Cascaded-H Bridge
DAB	Dual Active Bridge
DC	Direct Current
DG	Distributed Generator
DSO	Distribution System Operators
FBSM	Full bridge submodule
GTO	Gate turn-off thyristor
HBSM	Half bridge submodule
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
IoT	Internet of Things
KPI	Key Performance Indicator
LVDC	Low Voltage Direct Current
LVRT	Low Voltage Ride Through
MMC	Modular Multilevel Converter
MOSFET	Metal-oxide-semiconductor field-effect transistor
MVDC	Medium Voltage Direct Current
NPC	Neutral Point Clamped converter
OOP	Object Oriented Programming
OPEX	Operating expense
PCC	Point of Common Coupling
PSPWM	Phase Shifted Pulse Width Modulation
PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable Energy Sources
ROI	Return on Investment
SM	Submodule
SW	Switch
THD	Total Harmonic Distortion
TSO	Transmission System Operators
UML	Unified Modelling Language
VSC	Voltage Source Converter

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1 Introduction

1.1 Context

The United Nations Convention on Climate Change that took place in Paris in 2015, resulted in the goal of trying to limit the rise in global temperature to 1.5°C by 2050 [1] resulting in a number of countries making efforts to achieve net zero CO_2 emissions over the coming decades. Countries and institutions around the world have done comprehensive research and reports on the pathways that should be followed in order to achieve this goal [1]–[3]. The energy sector as the major source of global emissions [4], is the core of these efforts and actions that include changing the energy mix to integrate larger shares of Renewable Energy Sources (RES) and reduce dramatically the use of coal, oil and gas, decarbonizing the industry and the mobility sectors, reinforcing and modernizing the existing grids, increasing decentralized generation and exploring new energy vectors such as hydrogen. These actions, alongside with economics, policies and social behaviour changes represent the so-called energy transition [5].

In order to achieve the net zero CO_2 emissions goal by 2050, the massive deployment of Renewable Energy Sources is required. The International Energy Agency estimates that 90% of the global electricity generation should come from renewables, mainly solar and wind in 2050 and the International Renewable Energy Agency (IRENA) estimates that the RES share should be around 65% by 2030. This is key along with a decrease in the main sources of carbon, such as coal and oil power plants and combustion engines personal vehicles [2]. Actions have already been taken in this matter, as the European Union has already announced the sales ban of internal combustion engine vehicles from 2035 [6]. As a result of this action and of the expected electrification of other sectors, such as the steel production and heating and cooling, the electricity demand is expected to increase, which combined with an increase in RES, give as a result a very different electrical grid in the future, with a large presence of DC sources and loads. The energy efficiency has also been identified as one of the key solutions to achieve the 2050 goal [1], [2].

The large shares of RES, mainly solar and wind as well as the increase in EVs, make flexibility a key aspect for the future grids. There are many different ways of increasing the flexibility of the grid, among the possible solutions are storage systems, electric-vehicle smart charging, sector coupling (power-to-heat, power-to-gas), Internet of Things (IoT), Artificial Intelligence (AI), mini-grids, supergrids, different business models, market design and among system operation advanced forecasting of variable renewable power generation, cooperation between transmission and distribution system operators (TSOs and DSOs) and the future role of the DSOs [1].

This last aspect is particularly relevant, considering that the future (distribution) system planning, and operation will have to be coupled with the mobility sector in order to prepare the system for the extra load, and also to coordinate the charging infrastructure and smart charging that could support the integration of RES [7]. This would be done using the batteries of the EVs, as a flexible storage system, when they are not in use, by storing the excess production of renewables, and as a possible source of energy when there is no generation. By implementing smart charging strategies, it would also be possible to shift some of the peak load, ultimately reducing the peak and reducing the grid congestions, versus only expanding the distribution network for the extra load [1].

Furthermore, the current utility grid will change from a top-down architecture to a decentralized system with several small-scale distributed power generators, a multi-terminal grid that will allow to interconnect prosumers. The cost of electricity production using PVs is already lower than the cost of transmission and distribution [8], but the cost of storage is high if large amounts of energy have to be stored. Given that density of electrical storage systems is less than that of chemical ones, there is an economical competition between the price of storage and the price of transmission and distribution. Other obstacles for the spreading of distributed generators (DGs) include the lack of space in roofs for installation of PV panels that cover the local needs, the lower efficiency of smaller units, increasing the Levelized Cost of Electricity (LCOE) and the maintenance cost of so many small units. At the end the market price of electricity will always end up balanced among the cost of power generation, energy storage and transmission and distribution costs. A “one-third” rule applies, meaning

that around one third of the installed electrical energy production and power base is installed at the transmission level, one third at the medium voltage level and one third at the low voltage level [8].

The distribution network structure must change in order to cope with the different changes that decentralized generation brings. First of all, the bidirectional power means that the protection system may not be able to cope with the increase in the short-circuit current, not to mention that an increased number of prosumers would make the coordination of protection systems of classical radial AC grid quite difficult. Then, power quality regulations limit gravely the maximum peak power that can be installed from renewables in urban AC distribution cable networks. Cable currents are also limited to about 30% of their maximum continuous thermal current rating in order to limit the voltage drop caused by the reactance in AC cables [8]. The problem is that the electrification of different sectors will represent power quality challenges, as well as an increase in the required energy and peak power, but the AC grid requirements limit gravely the amount of RES to be installed. For the moment DSOs can only install larger transformers when the space allows, or they can provide intelligent energy demand-side services, but with all the previously mentioned constraints, one can only expect that their investment costs will have to increase in the following decades [3], [8].

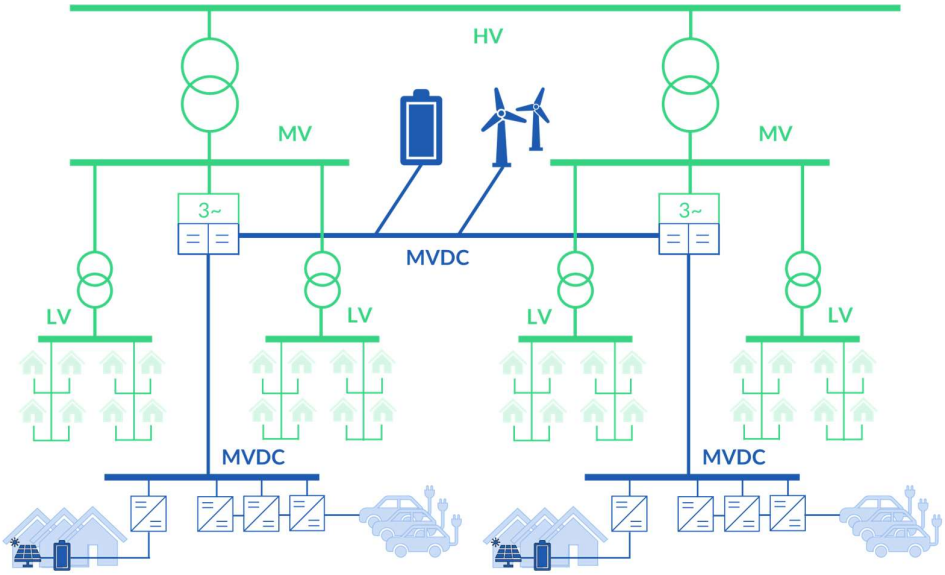

Figure 1 Hybrid approach to maximize capacity of distribution networks [9]

A possible pathway for the future distribution networks, is to have a hybrid AC-DC grid, where the DC grid comes to support the AC grid and helps maximizing its capacity as it can be seen in Figure 1. DC technology based on power electronics can provide technical solutions that can be less expensive than the classical grid expansion path. AC-DC converters can control the power flow dynamically, and when substations are linked together via a DC link, a flexible control of the power flow is possible. Hybrid AC-DC grids provide a high level of reliability and improved power quality and in the scenario of a fault, the power reserve of one substation can be easily shifted via the DC link to the consumers fed by the affected substation. According to [8], the price of the power electronic inverters is currently lower than a 50 Hz transformer, making power converters interesting also from an economic point of view.

As it can be seen, there are several advantages of DC networks with a large number of decentralized power generation. First of all, according to [8], the energy conversion will be more efficient, since power converters have less losses than 50Hz transformers. Then, DC cables have higher power capabilities than AC cables. The infrastructure cost as well as the amount of material used in the grid is less than in the full AC grid [10]. All of this adds up to cost reductions, that can be potentially improved with the development of new materials. Finally, due to the fact that DC converters can be easily connected in series or in parallel, they offer redundancy and reliability [8].

As a conclusion, MVDC networks in the range of ±1 kV to ±100 kV may play an important role in the future grids and represent a feasible solution that could allow to integrate large shares of RES and EVs, while ensuring that the load is supplied. Other relevant applications such as rail, ship and offshore wind have also been considered as feasible prospects of MVDC [11], [12]. A key technology of the development of this MVDC network are the power converters, that will be the interface between the AC and DC systems. Given that the MVDC network is still a relatively young concept [13], there are many questions regarding the most efficient or convenient technologies to use in these voltage levels. One of them, that is the core of this project, is which topology of AC-DC converter seems to be the most convenient.

1.2 SuperGrid Institute

The SuperGrid Institute is a research and innovation institute for the energy transition (IET) founded in 2014. ITEs in France are dedicated to researching new energy technologies, and their expertise comes from private companies as well as from academic organisations and laboratories. The SuperGrid Institute focuses on the development of technologies and services for the so called supergrid, the electricity transmission network of the future. This supergrid is designed to interconnect existing alternating current systems, enabling a wide-scale integration of renewable energy sources as well as to allow the integration of energy storage systems, which increase the flexibility of grids with large shares of renewable energy sources and to ensure the stability and security within the network [14].

The SuperGrid Institute is organized in five different research programs, each of them with different subprograms: [15].

- **Supergrid Architecture & Systems:** Focused on the technical challenges of DC grids. In this program control and protection strategies for High Voltage Direct Current (HVDC) systems are developed and requirements for key components of the system are defined.
- **High Voltage Substation Equipment:** Focused on the High Voltage Direct Current (HVDC) substation equipment, addressing the many challenges involved in these technologies. This program develops technologies associated with protection strategies that enable reduced infrastructure costs while maintaining the stability and availability of the networks. As a key part of the future DC networks, they also focus on gas-insulated substations (GIS).
- **Power Electronics & Converters:** This program focuses on developing power electronics technologies to meet the requirements of the future DC grid. The research covers innovative topologies and control systems which enable to build highly efficient MVDC and HVDC power converters.
- **HVDC Cable Systems & Junctions:** This program develops specific technological components for HVDC cable systems and study high-performance materials which will be used in DC network cables. They explore and develop accurate HVDC cable modelling.
- **Power Storage & Balancing:** This program develops solutions to support the grid flexibility including adaptative storage, as a key solution when integrating and managing renewable energy resources on a wide scale. They focus for now in Pumped Hydro Storage (PHS), as the most mature concept in terms of production capacity and storage volume.

This project took place within the program Power Electronics & Converters, specifically within the team New Concepts for MVDC Applications.

1.3 Thesis objectives and scope

The objective of the thesis is to do a comparison between two different converter topologies that could be interesting for MVDC applications. This project is the continuation of other works that have been done previously in the SuperGrid Institute. From these works, two topologies have been identified to be particularly interesting, namely the Modular Multilevel Converter (MMC) and the Neutral Point Clamped converter (NPC).

The comparison between these topologies should be made based on two different factors: sizing and power losses.

The MMC topology has been successfully used in HVDC and has become quite popular in the past 20 years, while the NPC topology is the preferred topology for MV drive applications [16]. Given that the MVDC utility networks are relatively new, the choice between both topologies is not evident and an assessment is needed to determine which topology would be better suited for MVDC network applications. This is the main goal of this project.

To assess these topologies, a methodology is needed. Thus, another goal of this master thesis is to propose a general methodology for the assessment of AC-DC converters that could be easily applied to any converter topology and keeping it as simple as possible, avoiding the extensive use of time-consuming simulations as much as possible. If a transient simulation is needed as part of the methodology, the models for both topologies of converters previously developed in the SuperGrid Institute will be used, adapting the models to the specific case study analysed in this thesis.

This document is organised as follows. Chapter 2 shows the state of the art of both topologies of converters, chapter 3 presents the steps and calculations needed for the design of both converter topologies, chapter 4 explains the proposed methodology for the comparison of AC-DC converters, chapter 5 shows the implementation of a tool for the automated calculation of the design parameters and KPIs of the NPC topology. The implementation for the MMC converter had already been done in the SuperGrid Institute. Chapter 6 shows the case study and the obtained results and discussion and finally chapter 7 contains the conclusions of the work and perspectives for future work.

2 State of the art

2.1 Electric networks

The power system is composed of transmission and distribution networks. In order to get connected to these networks, the compliance of a series of requirements is needed. In this section, a brief overview of some of these grid requirements is presented.

2.1.1 Grid requirements

The grid requirements are stated in documents with the technical specifications to get connected to a Transmission System Operator (TSO), RTE in France, or a Distribution System Operator (DSO), Enedis in France. For the study in this thesis, a decree of the French ministry for ecologic and solidarity transition [35] as well as technical documents from the RTE and Enedis were consulted to list the applicable requirements and the most relevant ones for MVDC applications. The existing standards are not made for MVDC installations, they are specified for the first connection of production and consumption installations to the AC public electricity network. There is however a section specifying the connection of HVDC systems to the public electricity network. Since the standards exist for both transmission and distribution levels, they are considered to be a good starting point for the assessment of MVDC systems.

2.1.1.1 Power limits to get connected to the transmission or distribution network

It was found that the requirements are different for producer and consumer installations, particularly as regards the maximum allowed power to be transmitted (in one direction or the other) for the connection. The reviewed documents have also some rules for prosumers (installations where consumers can also be producers). Different limits apply if the client is connected to a transmission or distribution level. Different voltage levels are defined in France, BT (Basse Tension), HTA (Haute tension A) and HTB (haute tension B), low voltage, medium voltage, and high voltage, respectively. BT is in the range of 50 to 1000 V in AC and between 120 and 1500 V in DC.

HTA is in the range of 1000 and 50000 V for AC and between 1500 and 75000 V for DC and HTB , from 75000 V in DC and from 50000 V in AC [36].

Table 1 shows the maximum installed power allowed to be connected for low and medium voltage levels. For the case of MV, the HTA level is of interest. From the table it can be seen that the maximum power that a production unit can generate to get connected to the distribution network is 12 MW. Beyond this level the production client would have to get connected to the transmission grid.

Table 1 Voltage level connection according to installed power for production units. From Art 24 du 9 juin 2020 [35]

Voltage level	Maximum installed power
BT single-phased	18 kVA
BT three-phase	250 kVA
HTA	12 MW

Table 2 shows the limit power of a consumption unit to get connected to different voltage levels. It can be seen that for the MV level (HTA), the maximum power that can be consumed is 40 MW, assuming that the consumption unit is very close to the transformation point (2-3km).

Table 2 Reference connection voltage level of a consumption unit (transmission level). Art 105 Ârreté du 9 juin 2020 [35]

Voltage reference level for the connection	Connection power of the consumption unit must be smaller than the smallest between the two values (in MW)	
HTA	40	100/d
HTB1	100	1 000/d
HTB2	400	10 000/d
Where d is the distance in km between the connection point and the transformation point to the higher voltage that is closer to the transmission grid		

In the decree it is also stated that the installations that act as consumers and producers at the same time must comply with the requirements for both producers and consumers. This is important to consider because the maximum power at which a production unit can get connected to the distribution network is 12 MW while for the consumption units is 40 MW, they are not the same limits.

2.1.1.2 Harmonic content

The harmonic current components are limited to the following value:

$$I_{n\ component\ harmonic} = \frac{k_n S}{\sqrt{3} U_n} \quad \textbf{(2.1)}$$

Where S is the installed power, U_n is the nominal voltage and k_n is a factor given by the following tables, for the transmission and distribution networks, respectively.

Table 3 k_n coefficients for harmonics, transmission grid. Art 111 Ârreté du 9 juin 2020 [35]

Odd components	k_n	Even components	k_n		kn
3	6,50%	2	3,00%	Tg	8,00%
5 and 7	8,00%	4	1,50%	$Tg = \sqrt{\sum_{n=2}^{40} k_n^2}$	
9	3,00%	>4	1,00%		
11 and 13	5,00%				
>13	3,00%				

Table 4 k_n coefficient for harmonics, distribution network. From Art 31 Âreté du 9 juin 2020 [35]

Odd components	k_n	Even components	k_n
3	4,00%	2	2,00%
5 and 7	5,00%	4	1,00%
9	2,00%	>4	0,50%
11 and 13	3,00%		
>13	2,00%		

As it can be seen from Table 3, the global harmonic content is also limited to 8%.

2.1.1.3 [P,Q] and [U,Q] diagrams

Connection to the distribution network

Figure 2 and Figure 3 show the [U,Q] and [P,Q] diagrams for production units type A and B (under 18 MW, see Table 5) connected to the distribution network. They represent the reactive power that a production unit has to be able to absorb or provide when the voltage in the connection point is above or below some limits. The data can be seen in Table 6 and Table 7.

Table 5 Categories for production units. From Art 35 Âreté du 9 juin 2020 [35]

Unit category	Maximum range of power	Voltage at PCC
Type A	0,8 kW ≤ P_{max} ≤ 1 MW	$U_{connection} < 110kV$
Type B	1 MW ≤ P_{max} ≤ 18 MW	$U_{connection} < 110kV$
Type C	18 MW ≤ P_{max} ≤ 75 MW	$U_{connection} < 110kV$
Type D	75 MW ≤ P_{max}	$U_{connection} < 110kV$

Table 6 Limits of [U,Q] diagram for distribution network

Voltage	Q_{min}	Q_{max}
0.9 – 0.95 U_c	>-0.35P_{max}	<0.4P_{max}
BT three-phase	-0.35P_{max}	0.4P_{max}
HTA	>-0.35P_{max}	<0.4P_{max}

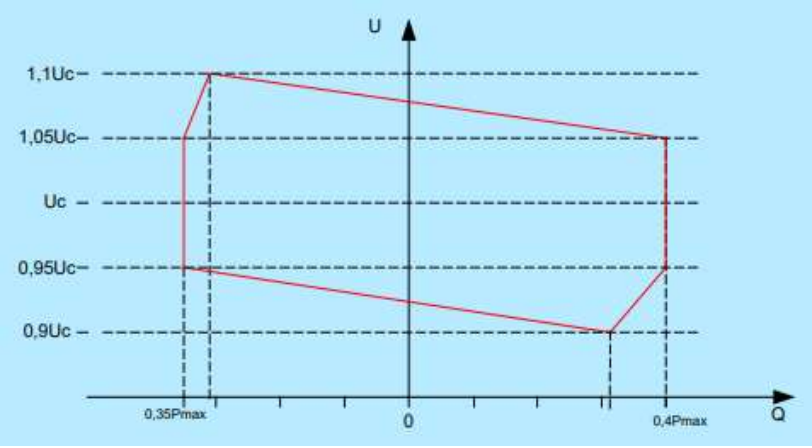

Figure 2 [U, Q] diagram required at the connection point for Type A and Type B units [37], Arts 43, 54 Âreté du 9 juin 2020

Table 7 Limits of [P,Q] diagram for distribution network

P/P_{max}	Q_{min}	Q_{max}
0.0	0	0
0.0 – 0.2	$>-0.35P_{max}$	$<0.4P_{max}$
0.2 – 1.0	$-0.35P_{max}$	$0.4P_{max}$

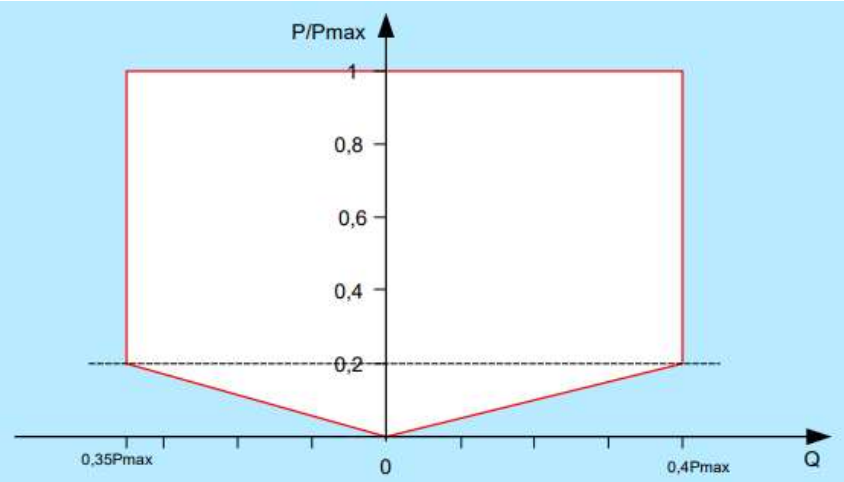

Figure 3 [P, Q] diagram required at the connection point for Type A and Type B units [37], Arts 43, 54 Âreté du 9 juin 2020

2.1.1.4 Low Voltage Ride Through

Distribution network

Figure 4 shows the low voltage ride through (LVRT) requirements for different types of production units. For instance, for a synchronous generator rated less than 5MW (red dotted line), the unit should remain connected for 0.15 seconds in the case that the voltage is at 30% of its nominal value. Likewise, it should remain connected for 0.55 seconds (from 0.15 to 0.7 seconds) if the voltage is at 70% of its nominal value and so on.

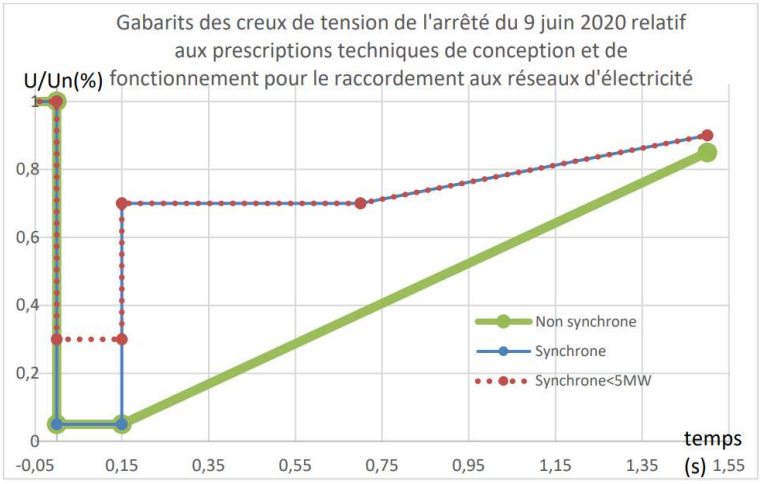

Figure 4 Low voltage ride through for different types of production units [37]

For AC-DC converters the low-voltage ride through is not defined, but such a behaviour in case of a voltage drop could be achieved with appropriate control.

2.2 Semiconductor devices

Power semiconductor devices development started with the invention of the thyristor in 1950. In the late 1960s the thyristors started being used for high-voltage valves for HVDC transmission and in 1972 the first thyristor-based HVDC link was put into service by General Electric [16] opening the door to the thyristor era in high voltage utility applications. Besides HVDC transmission, these semiconductor devices were also used for speed control of DC motors. The development on semiconductors went from gate turn-off (GTO) thyristors to bipolar junction transistor (BJT) and metal-oxide-semiconductor field-effect transistors (MOSFETs).

In the 1980s the technology nowadays called Insulated Gate Bipolar Transistor (IGBT) was developed. This device has a key feature that would put it ahead the previous technologies. They are voltage-controlled. The advantage of this is that the power consumption of the gate driver is substantially lower than for a current-controlled device such as the BJT. Besides the low gate power requirement, the IGBT could also switch faster than the GTO and BJT making it possible to increase the commutation frequency or to reduce the switching losses [16]. Finally, it provides controlled turn-off capability differently to the thyristors, enabling more flexibility and controllability.

In 1999 the first commercial IGBT-based HVDC transmission link was commissioned. This marked a new standard for HVDC transmission systems. The main difference compared to the previously dominant thyristor-based technology was the high controllability due to the fact that IGBTs can turn on and turn off a current in a desired moment. This is why they are usually seen as switches. Thyristors did not have this turn-off capability, giving the IGBT a big advantage, and allowing to control both active and reactive power independently. Another advantage of converter based in IGBTs is that they can operate without the presence of generators on the AC side, i.e., they provide black-start capability and can operate on weak AC systems. Nowadays, VSCs based on IGBTs are an interesting technology, not only for HVDC applications but also for the integration of RES and for electrical drives [16].

To allow the introduction of IGBTs in the VSC-based HVDC applications, an important phase of development was needed. Firstly, a packaging technology allowing the series-connection of stacks of IGBTs had to be developed. This was necessary due to the lack of power semiconductors able to withstand high voltages. The highest available voltage rating of a switch in the market today is 6.5 kV [17]. Then, a gate driver with passive elements had to be developed to allow the simultaneous switching of all IGBTs. Finally, a new converter type, the two-level converter had to be designed as well as new control systems and protection schemes [16].

Typical commercial power modules used for VSC-based applications have an IGBT with a diode connected in antiparallel, as shown in Figure 5. This diode provides a path for the current to flow in the reverse direction of the IGBT. These diodes should have similar ratings to the IGBT, and they must be compatible with the operating frequency and operating speed of the switches in the converter. They also must have a fast turn-off behaviour. The rating of these antiparallel diodes can be limiting factors in HVDC, because they must be able to withstand DC faults currents and overvoltages [18].

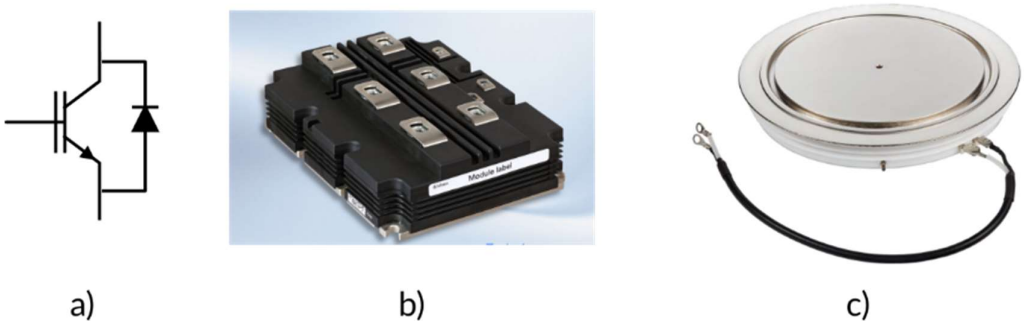

Figure 5 Typical power module with an IGBT and an antiparallel diode. a) circuit representation b) IGBT-diode module [17] c) press pack [19]

For high voltage applications, hundreds of IGBT switches are connected in series to form a valve. In each valve, the individual switch voltage during conduction and switching must be balanced. An unbalance in the switching events can be due to different device characteristics or to different signal delays between the control circuit and the devices [20]. It is possible to balance the switch voltage in steady state using large resistors in parallel to each switch in the chain. The dynamic balancing during switching is a more difficult issue due to the short time frames. It is however vital that that the voltage is balanced because each valve has to withstand a high voltage, and if one switch turns off first or last than the other ones, that switch would have to withstand all the voltage by itself, which could lead to the semiconductor breakdown. Usually, snubbers like the one shown in Figure 6 are used to slow down the switching process balancing the device voltage during the switching, although this represents a reduction in the efficiency. These snubbers limit the voltage and current values as well as the rising rates [18], [20].

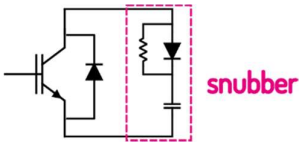

Figure 6 Snubber circuit in an IGBT module

To select a switch for a specific application it is necessary to consider the nominal current and voltages of the power module. But in VSC-based converters, the switches are not used at the nominal voltage, a de-rating factor or a security factor has to be introduced to consider the maximum preferred blocking voltage rating of the switch [21], [22]. The security factor is typically around 2, meaning that the maximum operating voltage of the switch should be around 0.5 its nominal value [23].

2.2.1 Power losses of semiconductor devices

The power losses in a converter are related to the efficiency of the system and they also play an important role in the design of the cooling system. In a power converter, the main source of losses are the semiconductor devices. Two types of power losses can be considered for the semiconductors, conduction and switching losses, explained in detail below.

2.2.1.1 Conduction losses

Conduction losses are caused by the voltage drop across the semiconductors during conduction. The conduction losses can be estimated using the I-V characteristics of a power module as presented in Figure 7 [18].

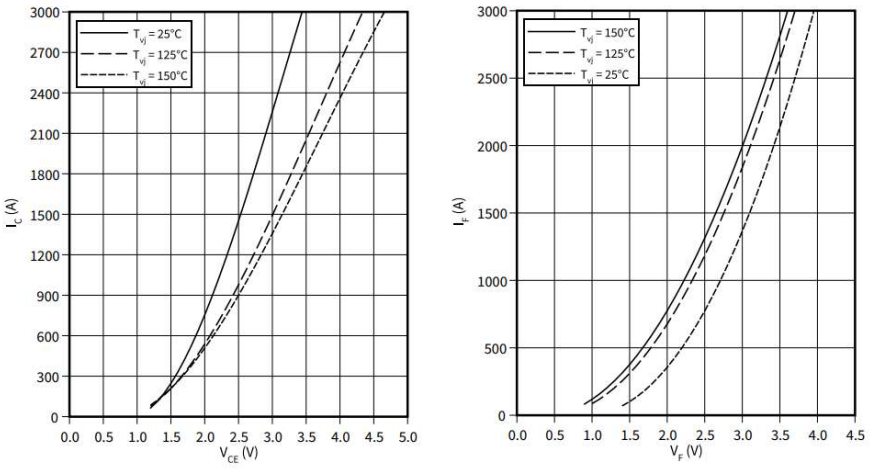

Figure 7 I-V characteristics of the IGBT and anti-parallel diode of a 3.3kV power module (Infineon FZ1500R33HE3) [24]

The instantaneous conduction losses can be found as the product between the characteristic voltage and currents, as shown in equations **(2.2)** and **(2.3)** for the IGBT and the diode, respectively. To find the conduction losses over one period, it would be necessary to find the average value by integrating the instantaneous losses along the period and dividing by the period, as shown in equation **(2.4)**.

$$P_{cond,IGBT} = V_{CE} I_C \tag{2.2}$$

$$P_{cond,Diode} = V_F I_F \tag{2.3}$$

$$P_{cond} = \frac{1}{T} \int_0^T P_{cond,instantaneous}(t)\, dt \tag{2.4}$$

Typically a linear approximation of these curves can be used taking data from the datasheet such as the saturation voltage for the IGBT, the threshold voltage for the diode and the equivalent resistance in the ON state [25], [26], [27].

2.2.1.2 Switching losses

The switching losses can be divided into two categories, the turn-on switching losses E_{on} and the turn-off switching losses E_{off}. They represent the energy lost during turn-on and turn-off of the semiconductor device. The total switching loss is the sum of E_{on} and E_{off} in one cycle. For the diodes, the turn-on loss is typically neglected.

The switching losses of a 3.3kV power module can be calculated using its characteristic curves shown in Figure 8, that show the turn-on and turn-off energies of the IGBT and the reverse recovery energy of the diode in function of the device current at the moment of the switching.

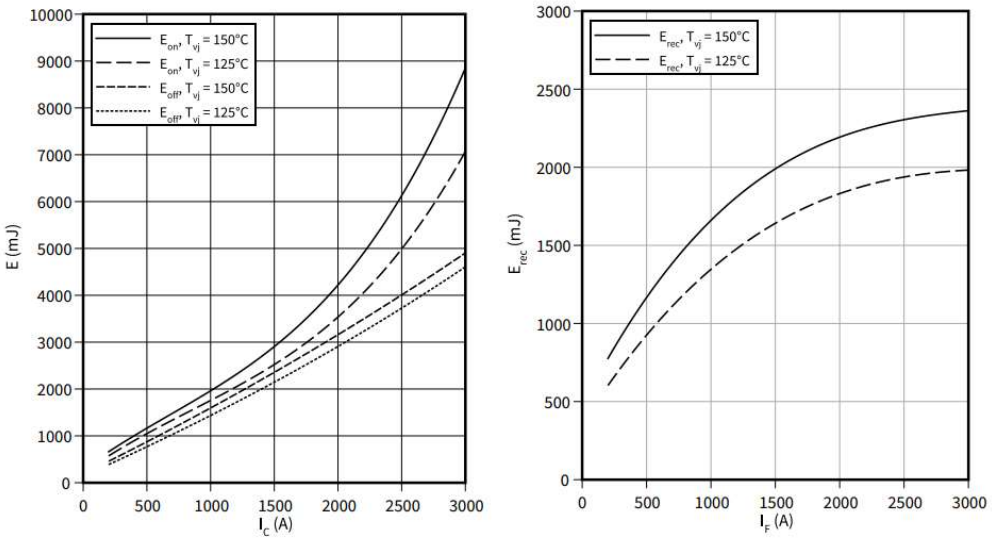

Figure 8 Switching losses characteristics for the IGBT and antiparallel diode of a 3.3kVr module (Infineon FZ1500R33HE3) [24]

An approximation is also usually used in this case, typically a first or second order polynomial whose coefficients will be determined with the characteristic curves [18], [25], [27].

The switching losses over one second are the product between the energy that is lost during turn-on or turn-off and the switching frequency:

$$P_{Sw} = f_{sw}(E_{on} + E_{off}) \tag{2.5}$$

2.3 VSC-based converter topologies

2.3.1 Two-Level converter

The first topology used for the VSC-based applications is the two-level converter shown in Figure 9. Nowadays it is still the preferred solution for low-voltage applications. However, for higher ranges or voltage, its implementation is difficult due to the lack of power semiconductors able to withstand high voltages and the need of series connection as explained in section 2.2.

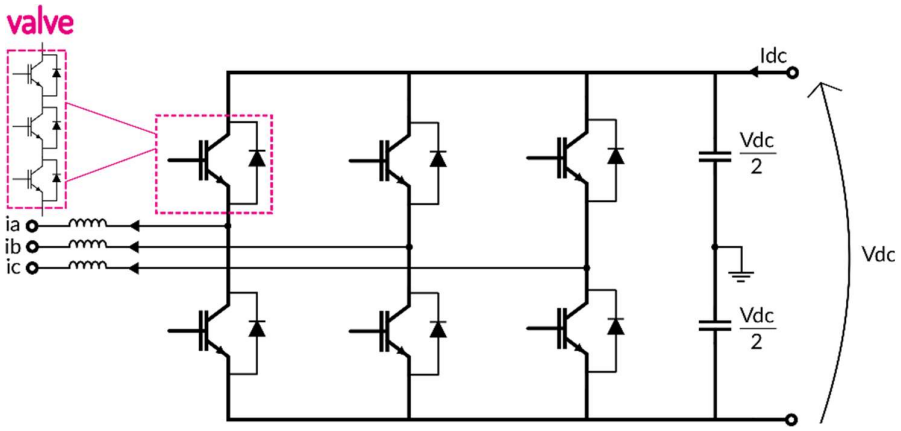

Figure 9 Two-level converter for high voltage applications

As it can be seen, each phase leg has two bidirectional valves composed of IGBTs and antiparallel diodes. The basic operation of the leg is to control the valves to obtain either $+V_{dc}/2$ or $-V_{dc}/2$ at the AC terminals as shown in Figure 10, assuming that the current is flowing out of the phase leg.

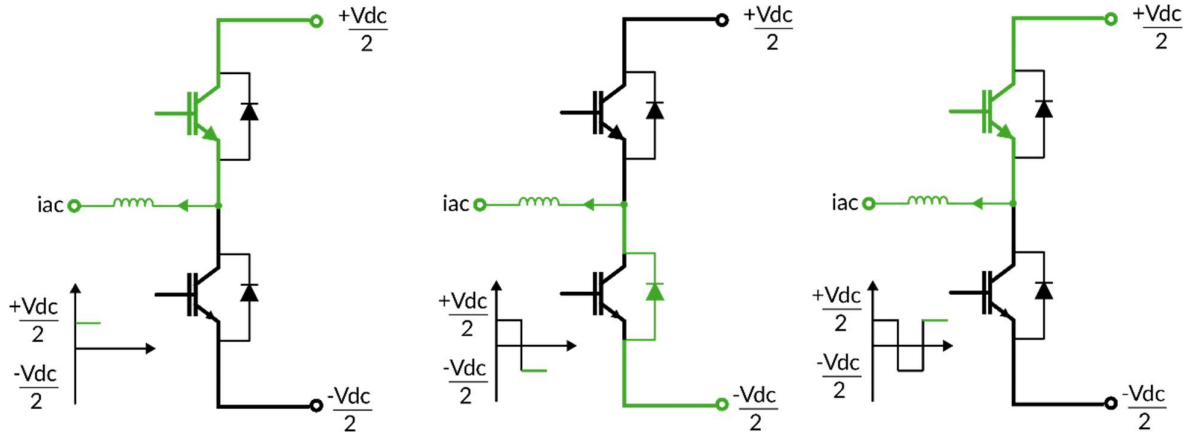

Figure 10 Switching stages in the operation of a 2-Level converter leg

2.3.2 Neutral Point Clamped Converter

After the two-level converter, a series of multilevel converter topologies was developed. These topologies present the advantage that compared to the 2-Level converter, they decrease the voltage that each valve needs to withstand. Thus, for the same valve technology, higher DC voltages can be achieved. They also presented an improvement in the AC output waveform quality in terms of harmonics with respect to the two-level converter [16], [28].

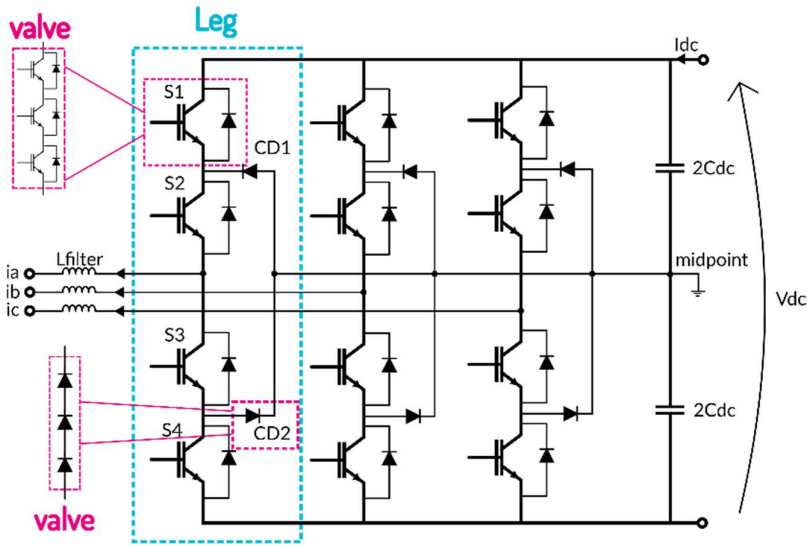

Figure 11 3-Level NPC Converter Topology

The Neutral Point Clamped Converter was the first multilevel topology to be used on a large scale. It was proposed in 1981 for wide range variable-speed drives [28]. They have clamping diodes that can link the midpoint created on the DC side to the AC terminals, creating a third level of voltage. Although, these converters can have more voltage levels than three, as they increase so do the number of clamping diodes and interconnections, making them unfeasible from a technical and economical point of view [16], [18]. Thus, the most common NPC is the three-level converter shown in Figure 11.

As it can be seen, the NPC has three legs (phases), each one has six valves, four pairs of IGBTs and antiparallel diodes and two clamping diodes. The middle point is created thanks to two DC capacitors. An AC low pass filter (an inductor for example) is added on the AC terminals. The operation principle is to control the valves to generate three different voltage levels on the AC terminals (+V_{dc}/2, 0 and -V_{dc}/2) as shown in Figure 12.

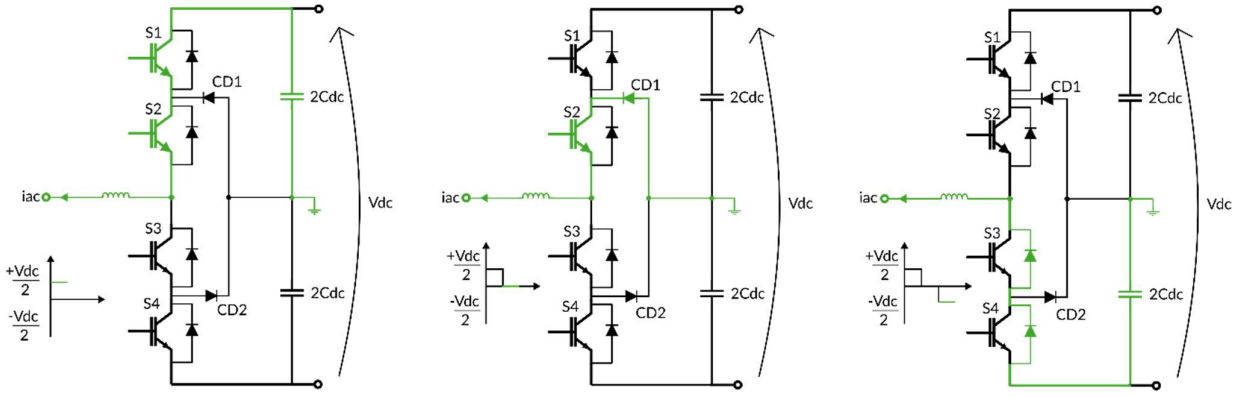

Figure 12 Switching states of the 3L-NPC assuming the current flowing out of the phase

One disadvantage of the topology is that at higher voltage levels, the valves would also need a series connection of semiconductors, bringing the difficulties mentioned previously. Another problem is the uneven distribution of losses between the external valves S_1 and S_4 and the internal valves S_2 and S_3. This creates the need of using overrated valves, which is not economically convenient [16].

2.3.3 Cascaded converters

Another type of multilevel converters are cascaded converters which use switching submodules (SM), each of which has pairs of IGBTs plus diodes and a capacitor. There are two main types of SMs used: the Half-Bridge

Sub-module (HBSM) and the Full-Bridge Sub-module (FBSM) shown in Figure 13. The HBSM can only generate a unipolar voltage while the FBSM can generate bipolar voltages. A converter with FBSMs also has fault blocking capability, although using FBSMs implies doubling the number of semiconductors installed, which produces higher losses and costs [30].

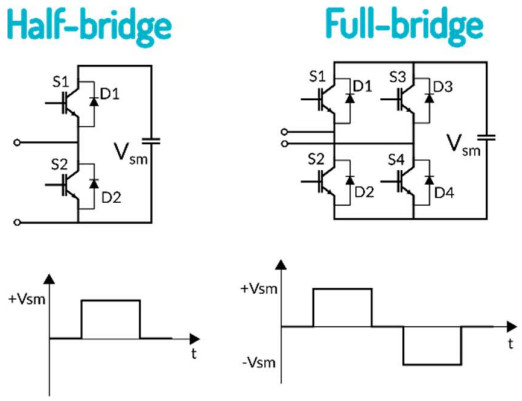

Figure 13 Type of converter submodules. HBSM and FBSM.

2.3.3.1 Cascaded-H-Bridge converter

The Cascaded-H-Bridge Converter is composed of FBSMs connected in series, which form a staircase output waveform, where each step corresponds to a SM voltage [31], [32], as it can be seen in Figure 14. Typically used for MV drives applications, each SM needs a separated DC source, generally a diode rectified is connected to each SM and to a secondary of a multiwinding transformer. A single bridge is capable of generating three voltage levels $+V_{sm}$, *0* and $-V_{sm}$. The number of levels depends on the number of FBSMs connected in series. Each phase of the CHB with *n* levels has (n-1)/2 FBSMs [33]. This topology has the advantage of requiring a smaller number of components than other topologies in order to obtain the same voltage level and it does not need any extra diodes or capacitors. The disadvantage is that the requirement of separate DC sources makes it difficult to reach high voltage levels [31]. A three-phase cascaded converter can be connected either in delta or star configuration, depending on the application.

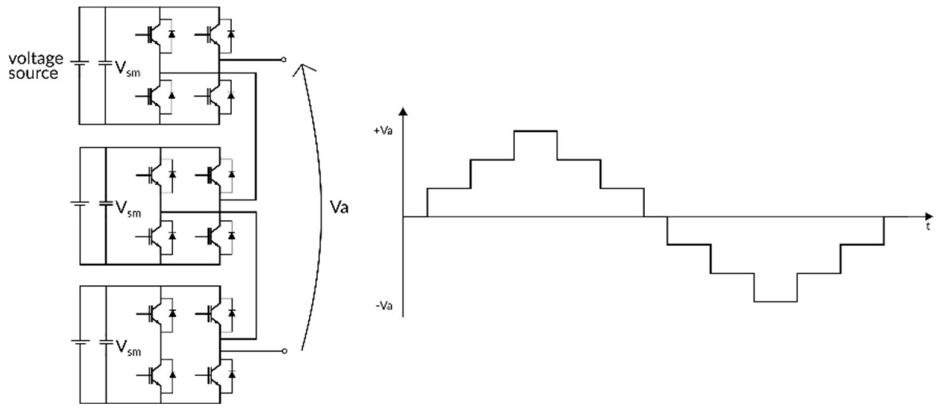

Figure 14 Cascaded-H-Bridge phase and staircase generated by the leg

2.3.3.2 Cascaded 3L-NPC

A variation of the NPC converter is the cascaded 3L-NPC (C3L-NPC). This topology is another approach to obtain high voltages based on the NPC. It consists in connecting an n number of 3L-NPCs cascaded [29] as shown in Figure 15. If this is the case, the power and voltage will be shared between all the converters, which allows to have smaller voltage and power ratings for each converter.

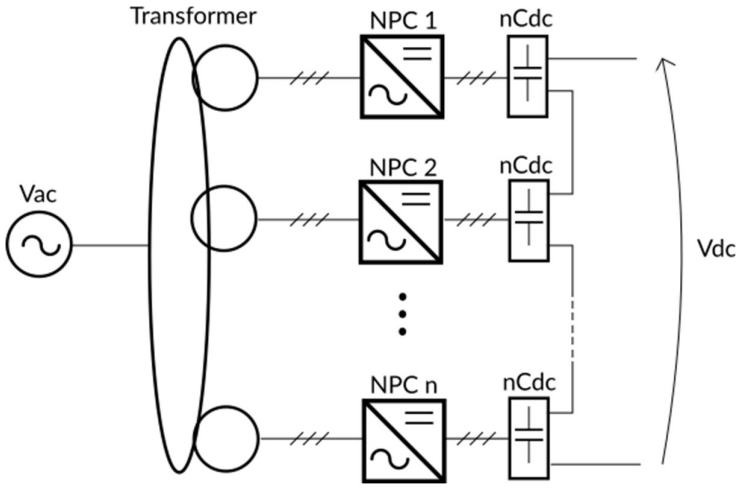

Figure 15 Cascaded 3L-NPCs

2.3.4 Modular Multilevel Converter

The Modular Multilevel Converter proposed in 2003 [34] is also based on SMs and it can have either HBSMs or FBSMs. This type of converter has gained a lot of popularity in HVDC because no series connection of semiconductors is needed, only a connection of SMs and because it does not need individual DC sources per SM. This is a big advantage, and it allows to have a truly modular design, where increasing the converter DC voltage rating or adding more levels for the AC output only requires the connection of more SMs [16]. It also has high efficiency and a superior harmonic performance, which allows to reduce the size of passive filters [30] reducing as well the footprint. This topology is however challenging in terms of control [18].

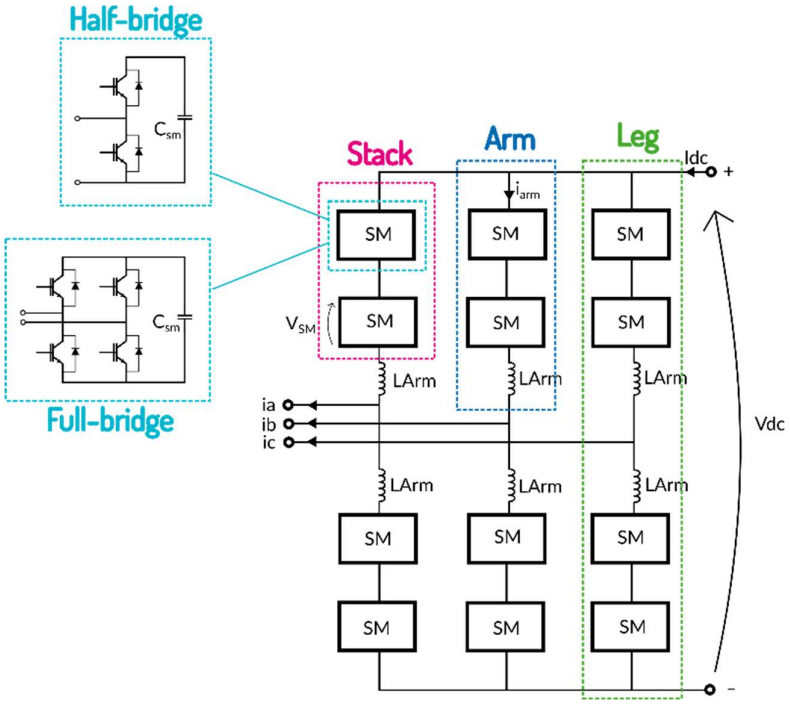

Figure 16 Modular Multilevel Converter topology

As it can be seen in Figure 16, the MMC converter has 3 legs (phases) each one with two arms, upper and lower. Each arm has an inductor and a SM stack (several SMs connected in series). Each stack can generate V_{dc} (and -V_{dc} if FBSMs are used). The operation principle is to control the six SM stacks to obtain the desired voltage. The

sum of the upper and lower stack is maintained to around the desired pole-to-pole DC voltage and the difference of these voltages gives the voltage value at the AC terminals. The converter can then behave like a controllable voltage source from the AC side and both the AC and DC voltage can be controlled with a lot of precision [16]. The output form will also be a staircase, the more SMs the better the quality of the signal.

2.4 Selection of converters for MVDC applications

Given the expected expansion of the MVDC network, and the key role that power converters will play in this scenario, some authors have already researched which topology would be more suited for MVDC applications, and comparison between the topologies of interest for this work such as the NPC and MMC, but also of other topologies like the Cascaded-H-Bridge (CHB). The findings of their researched is shortly described in this section.

In [22] a comparison is made between the 3L-NPC and the MMC for MV applications, specifically for Battery Energy Storage Systems (BESS). The comparison is made in terms of components, operational characteristics and investment costs. The converters are rated 5 MVA to be connected to the 10 kV AC grid. For the comparison in terms of components, the number and ratings of the semiconductor devices and the filter elements are considered. In the operational characteristics, the components losses, the system efficiency and the harmonic content are considered. The losses distribution is shown, classified in conduction and switching losses for the semiconductors, and losses of passive elements such as inductors and capacitors. Four variants of MMC and an NPC with an LCL filter are compared. For the MMC, a nearest-level modulation (NLM) is used with a high number of SMs and a phase-disposition PWM (PDPWM) modulation is used for the other cases with a carrier frequency of 2 kHz. The NPC is modulated with a switching-loss-optimized space-vector modulation with a switching frequency of 1.5 kHz.

From the results it was observed that for BESS applications, the MMC does not seem to present any significant improvement in cost or performance over the 3L-NPC. The NPC presented lower total losses than all the variations of the MMC. The MMC presented all the harmonic components although small. The NPC had only some components, some of them quite big due to resonance with the LCL filter. In both cases the design was made for a THD (Total Harmonic Distortion) smaller than 5%. It was also observed that although the MMC has a higher value of total capacitance installed (there is one capacitor in each SM vs. two DC link capacitors for the NPC), this doesn't seem to affect the cost significantly. The conclusion is that the 3L-NPC topology would be preferred unless modularity and very high reliability are critical or desired features for the system. It is also noted, however, that as the voltage level increases the MMC topology seems to present more advantages than other topologies.

Another comparison is done in [38] between the MMC and the CHB for MV and high power industrial motor drive applications. In this paper, 3 different voltage levels (4.16 kV, 6.9 kV and 13.8 kV) and 3 different power levels (1 MVA, 3 MVA, 5 MVA) are considered. The comparison was made in terms of the capacitance requirements point of view, semiconductor losses, the semiconductor rating and the junction temperature. The designs are made to have a THD smaller than 2%, based on standards.

From the results it can be concluded that the CHB presents better performance from the efficiency, semiconductor utilization and capacitor bank size points of view. Interestingly, a trend was observed for the MMC, as the voltage increases so does its efficiency. This is due to the fact that at low voltage levels the MMC has small arm inductances, which makes it necessary to increase the switching frequency to comply with the THD requirement. So, as the voltage level increases, the MMC presents better efficiency and semiconductor utilization, mainly due to the decrease in the switching frequency and in the RMS currents of the arms, which also reduces the conduction losses.

In [23] a similar comparison is presented between the CHB, the MMC and the 5L ANPC (Active Neutral Point Clamped) also for motor drive applications. The analysis is done with 1.7 kV IGBTs for the CHB and MMC converters and with 3.3 kV and 4.5 kV for the 5-L ANPC. The comparison is made for three different voltage levels (4.16 kV, 6.9 kV and 13.8 kV) and two different power levels (3 MVA and 5 MVA). The comparison is

made in terms of efficiency (considering only conduction and switching losses), capacitive energy storage, semiconductor utilization, parts count and power density.

From the results it was found that the CHB has a better efficiency for all the cases followed by the MMC. Due to the high switching frequency needed to operate the 5L ANPC, it presents high switching losses. As regards the capacitive energy storage, the MMC has a significant requirement compared to the other two topologies, while the 5L ANPC has the smallest amount of energy stored, meaning that its footprint is largely reduced. As an indicator of the semiconductor utilization, the semiconductor die size is considered. The CHB seems to need the smallest area of IGBT die to install and the 5-L ANPC the greatest area. This means that the CHB requires less initial investment compared to the other two topologies.

Reliability is considered with part counts. The 5-L ANPC has the lowest number of semiconductors and the MMC the highest, suggesting a reduced reliability. Analysing the number of secondary windings needed for the transformer, the CHB needs more and more as the voltage increases, and always more than the other two topologies, making it more complex and potentially increasing its cost. The MMC and CHB are modular and therefore they can keep operating in case of a single cell failure, in case of the 5-L ANPC, a cell failure would stop its operation. Finally, after making estimations of the total converter volume, it was found that the MMC occupies the most space for all the cases, and it is followed by the CHB with switch rating of 4.16 kV or the 5-L ANPC with a switch rating of 6.9 kV. In conclusion the CHB seems to be the best topology for drive applications between 4.16 and 13.8 kV for its efficiency and smallest footprint. Its biggest disadvantage is the transformer, at higher voltages there is a breakeven point where the MMC becomes better due to this.

In [21] an analysis is made in order to determine which topology is more suited for multi-MW applications at MVDC levels. Three topologies are considered, the 3L-NPC the cascaded 3L-NPC (C3L-NPC) and the MMC. The analysis is done based on the reliability and optimum redundancy levels of the VSC, taking also into account factors such as the operational efficiency and the Return on Investment (ROI) in the range of ±10 kV to ± 50kV.

From the results it can be seen that as the voltage level increases, the MMC shows better performance, whereas for the lower spectrum of the MVDC level, the 3L-NPC seems to be better. The MMC presents lower total losses (only conduction and switching losses considered) as the other two-topologies. Different charts showing the ROI of the different topologies vs. the voltage level are presented where it is possible to see exactly at which voltage level, the ROI is better of one topology or the other. It is shown that between ±10 kV and ±24.2 kV the 3L-NPC is more economical. Beyond ±24.2 kV the MMC shows the highest ROI due to the higher efficiency. Beyond ±34 kV the C3L-NPC also shows better performance than the 3L-NPC but still smaller than the MMC. It should be considered that these ranges are valid with the hypotheses considered by the authors.

In [21] crossover points between the 3L-NPC and the MMC depending on the DC rated currents are shown. Currents between 100 A and 1000 A are considered. It can be observed that for the smallest current, the crossover point is around ±28.3 kV, so below this level the 3L-NPC is preferred and beyond this level the MMC would be more convenient. It can also be seen that as the current increases, this voltage decreases, until at 1000 A, the MMC would always be more convenient regardless of the voltage level.

As it can be seen from the literature, the MMC seems to present favourable performance indicators as the voltage level increases, while for the lower voltage levels the 3L-NPC remains the best option. These are the conclusions from [22] and [38] where the comparison criteria were related to the number of components, the power losses, the operational performance and the economic investment. Both cases had different applications and some of the design parameters (ex. THD) were adapted to this application. In [21] even a crossover point was presented when the analysis is made based on reliability and ROI (Return on Investment). The application considered will affect the design and the relevant KPIs used to do the comparison, and therefore, the crossover point from 3L-NPC to MMC could also change.

For the work on this thesis, the goal is to make a comparison of both topologies for a connection between an AC and a DC grid, no specific application is considered, and it is thus necessary to select a list of KPIs that will allow a general quantitative comparison of both topologies. It is important to do the analysis in a wide range of voltage and power levels, which will allow to see the evolution of the KPIs with the voltage and power and to

find a crossover point, if there is any. Finally, it can be seen that none of the articles previously discussed deals with a comparison of topologies under fault conditions, which is an important topic for DC grids.

2.5 Evaluation and assessment of topologies

In the previous section, different research works done to compare AC-DC converter topologies were shortly described. Some of the KPIs used were related to the sizing of the converter, such as the number of components, the rating of the semiconductor devices used, the capacitor bank size and the filter elements. Some of them were related to the operational performance of the converter like the harmonic content, the efficiency, the junction temperature and the losses. Similar KPIs are presented in [39]. Special attention was given to the losses distribution, as they were classified in conduction, switching, magnetic and capacitor losses. The economical aspect was also considered for the comparisons, using the investment cost and the ROI as indicators. In this section, a further review of KPIs for the comparison of converter topologies is presented. This allows to have a more extensive list of KPIs that could be used in this master thesis.

In [25] a comparison of DC-DC converters for the interconnection of HVDC grids is presented. Three KPIs are considered, the utilization factor, the energy factor and the power losses factor. The utilization factor represents the ratio between the transmitted power and the total rating of the semiconductors of the converter, the energy factor represents the investment on the components that store energy, such as the capacitors in the converter. For MMCs this factor is also related to the footprint of the converter, since one SM's size depends largely on the capacitor. Finally, the power losses factor, which represents the percentage of conduction and switching losses in the converter.

In [40] a list of KPIs is proposed to evaluate modular topologies, with the goal of allowing a rapid evaluation of the topology. The goal is to have KPIs that are easy to calculate, so new emerging topologies can be evaluated without passing through transient simulations or control system design. These KPIs would be a first step to determine how much potential a topology has or how suited it is for a specific application. The proposed KPIs should be able to give hints on the converter cost, size and efficiency, which are the three main aspects of interest to evaluate a topology.

The proposed KPIs are meant to be for modular topologies, that make use of stacks and SMs, so two types of KPIs are proposed, dependant on the SM rated voltage and independent of it. This is an interesting classification, since the SM rated voltage is a degree of freedom of the design. Among KPIs with no dependency on the SM they propose the transformer number and their sizing power, the switch total sizing power, the stored energy and the DC voltage ripple. As for the KPIs showing a dependency on the semiconductor rated voltage, the switch and SMs number and the SM cell capacitance can be found. The power losses will also be affected by this choice. All these KPIs can be calculated without the need of a transient simulation, which makes their evaluation much simpler.

A methodology is also proposed for the sizing procedure of the converter. It is interesting because it presents a general methodology to size and obtain the KPIs of any topology, and it is not focused on any specific application. The methodology starts by the definition of the operating domain or the PQ diagram for which the converter should be designed, which will of course be determined by the application. Then the degrees of freedom of the system, like for example the semiconductor rating, or the voltage ripple of the SM capacitor are defined. These degrees of freedom will directly affect the design and when wanting to make a comparison of topologies, it is imperative to define which degrees of freedom will have to be common for all topologies in order to make a fair comparison, and which ones can be used to optimize the design. The constraints of the system should also be defined.

Once these entries are defined, one can proceed to do the steady state analysis of the system and model the converter behaviour with mathematical equations. With these equations, a sweeping of the PQ diagram can be done in order to identify the extreme conditions, the best or worst operating cases. Parallelly a sweeping of the degrees of freedom can be done to obtain the most convenient design. And once the design is ready, one can proceed to the calculations of the KPIs.

As it can be seen, [25] presents general KPIs that somehow relate to the cost, size and performance of a converter, and [40] presents a more extensive list of KPIs along with a methodology to obtain them for multilevel converters. The need of a general methodology for the design and evaluation of AC-DC converters that considers the grid requirements, the application, the design and the KPIs is identified.

3 Design of MMC and NPC converters

In this chapter, the equations for the calculation of the different design parameters of the MMC and NPC converters are presented in detail. The outputs of this stage are essential for the evaluation of KPIs and enable the comparison of both topologies.

3.1 Design of MMC converter

3.1.1 Number of submodules

In the MMC topology, there will be moments in which an arm will have to withstand the whole DC voltage, so the sum of the SM voltages will have to be greater or equal than the DC voltage. Equation **(3.1)** shows the number of required SMs in an arm assuming that the maximum voltage of the arm is V_{dc}. The SM voltage V_{SM} will be the average operating voltage of the switch, considering the de-rating factor. For instance, for a 3.3 kV switch, the maximum blocking voltage would be around 1.8 kV, and if the voltage ripple is assumed to be 10%, the operating voltage would be around 1.6 kV.

$$N_{SM,arm} = round\left\{\frac{V_{dc}}{V_{SM}}\right\} \quad \textbf{(3.1)}$$

Considering that there are six arms in the MMC, the number total of SMs can be found. The total number of switches will depend on the type of SMs, for HBSMs there are two IGBTs and two diodes per SM and for FBSMs there are four IGBTs and four diodes.

3.1.2 Arm inductance

The arm inductance has to be designed so that it suppresses the second harmonic of the circulation current between phases [41] and also to limit the fault current [42]. An approximated relation often used in HVDC is to take the arm inductance value as 15% of the base impedance of the system [18] dependant on the line to line RMS AC voltage and the nominal power as shown below. This assumption is taken for the rest of the thesis.

$$X_{L,arm} = 0.15 Z_{base} = 0.15 \frac{V_{ac}^2}{S_{nom}} \quad \textbf{(3.2)}$$

3.1.3 Submodule and equivalent arm capacitance

The capacitors of each SM can be seen as independent voltage sources. The SM capacitance depends on the SM voltage V_{SM}, the number of SMs in the arm, the energy swing ΔW experienced by the capacitor during one period and the voltage ripple ε, as shown in the following equation [25].

$$C_{SM} = \frac{\Delta W}{2\varepsilon N_{SM} V_{SM}^2} \quad \textbf{(3.3)}$$

The energy swing ΔW can be found with the following expression, where $cos\varphi$ is the power factor of the converter at the AC interconnection point, f is the frequency of the AC network (50 Hz) and k is the arm modulation index, i.e., $k=V_{arm,\,ac}/V_{dc}$, the peak value of the arm AC voltage divided by the DC voltage

$$\Delta W = \frac{V_{dc} I_{dc}}{2\pi f}\left(1 - \frac{1}{\left(\frac{2}{k\cos\varphi}\right)^2}\right)^{\frac{3}{2}} \frac{4}{\cos\varphi} \quad \textbf{(3.4)}$$

3.1.4 Modulation index MMC

If it is assumed that the voltage ripple on the SM capacitor is small, the modulation index of the MMC can be estimated with the AC voltage of the arm and the sum of the voltages of the SMs [25], which from equation **(3.1)** is around the same as the DC voltage as shown below.

$$m_{arm}(t) = \frac{v_{ac,arm}(t)}{v_{dc}} \quad \textbf{(3.5)}$$

3.1.5 RMS current in a submodule

The RMS current in a switch can be found using the following equation [25]:

$$I_{sw\,RMS} = \sqrt{\frac{1}{T}\int_{t_a}^{t_b} \left(I_{sw}(t)\right)^2 \alpha(t)\, dt} \quad \textbf{(3.6)}$$

Where T is the period of the arm current, t_a and t_b are two adjacent zeros of the current and $\alpha(t)$ is the duty cycle. For the MMC the duty cycle is defined per SM, taking as a reference the HBSM shown in Figure 13, the duty cycle is defined based on the modulation index as follows:

$$\alpha(t) = \begin{cases} m(t) \;\; for\; S1 \\ 1 - m(t)\; for\; S2 \end{cases} \quad \textbf{(3.7)}$$

It is also important to consider the direction of the current to know through which of the devices of the switch (diode or transistor) is the current flowing. Then, the maximum RMS current between both devices will be the one used to calculate the semiconductor's VA rating. A similar analysis can be done for the FBSM, as explained in [25].

3.2 Design of NPC converter

3.2.1 Number of switches

For the NPC topology, each valve withstands half of the DC voltage. If the DC voltage is high, there might not be available semiconductors with the needed rating, so it is necessary to connect some switches in series. The number of switches connected in series for each valve is given by:

$$N_{SW,series} = round\left\{\frac{V_{dc}}{2V_{SW}}\right\} \quad \textbf{(3.8)}$$

Just like for the MMC, the switches used are derated to keep a safety margin. V_{sw} is the derated value of the selected switch. To find the total number of semiconductors, it has to be considered that there are 12 valves of switches in the 3L-NPC and 6 valves of clamping diodes.

3.2.2 DC link capacitor

DC bus capacitors can be calculated using the following equation, where S_{VSC} is the power of the VSC, V_{dc} is the DC pole to pole voltage of the VSC and E_S is the energy to power ratio, usually between 10 and 50 kJ/MVA [18].

$$C_{DC} = \frac{2 S_{VSC} E_S}{V_{dc}^2} \quad \textbf{(3.9)}$$

Thus, each one of the DC bus capacitors of the NPC would be equal to two times C_{DC}.

3.2.3 AC filter

The AC filter design for an NPC converter is usually done to comply with a specific value of THD. In the literature different types of filters have been used, like for instance an LCL filter or a series of LC filters connected to the AC terminals of the converter [43]. However, designing such filters requires detailed simulations or complex analysis and it is a time-consuming process. As a first step in this work a simple approach for the design of the filter is explored. Firstly, a simple filter (only an inductor) is considered, and its maximum value is determined by the maximal voltage drop on the inductor that would allow to obtain the desired AC voltage. Thus, the value of this inductor is given by the PQ requirements, the grid AC voltage, and the maximum AC voltage that the NPC can generate. With these constraints, an admissible value of the filter X_{AC} can be found. Nevertheless, it is important to note that with this approach it is unknown whether the filtering requirements will be met or not, and in later steps of the design this point should be checked. In case the inductor is not enough to comply with the THD requirements, a more sophisticated filter such as an LCL can be designed.

For the sizing of this simple AC filter, the equivalent circuit of Figure 17 was used. In the figure the 3L-NPC can be seen connected on one side to the DC grid and on the other side to the inductive filter X_{AC} and the AC grid. The point of common coupling (PCC) is where the exchanges between the AC and DC grids of active and reactive power P and Q occur. Considering that the voltage values of the AC and the DC grid are known and fixed, it is now of interest to know the value needed for the AC filter.

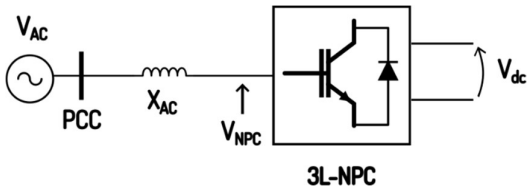

Figure 17 System diagram with AC filter

Doing the circuit analysis of the system, the AC current is:

$$I_{AC} = \frac{V_{NPC} - V_{AC}}{X_{AC}} \tag{3.10}$$

The apparent power per phase can then be expressed as follows:

$$V_{AC} I_{AC} = \frac{V_{AC} V_{NPC} - V_{AC}^2}{X_{AC}} \tag{3.11}$$

Then, considering the three phases of the system, the active and reactive power can be expressed as shown in the following equations, where δ is the angle between the AC voltage and the NPC voltage.

$$P = \frac{3 V_{AC} V_{NPC}}{X_{AC}} sin\delta \tag{3.12}$$

$$Q = 3\left(\frac{V_{AC} V_{NPC}}{X_{AC}} cos\delta - \frac{V_{AC}^2}{X_{AC}}\right) \tag{3.13}$$

Using the trigonometric identity $\sin^2 \delta + \cos^2 \delta = 1$, the reactive power can also be expressed as follows:

$$Q = \sqrt{\left(\frac{3 V_{AC} V_{NPC}}{X_{AC}}\right)^2 - P^2} - \frac{3 V_{AC}^2}{X_{AC}} \tag{3.14}$$

From equation **(3.14)** it can be found that the value for X_{AC} is:

$$X_{AC} = -6V_{AC}^2 Q + \sqrt{\frac{36V_{AC}^4 Q^2 - 4(P^2+Q^2)(9V_{AC}^4 - V_{AC}^4 V_{NPC}^2)}{2(P^2+Q^2)}} \quad \textbf{(3.15)}$$

As it can be seen the value of X_{AC} will be determined by the voltage levels of the AC and DC grids and by the active and reactive power exchanged between them.

3.2.4 Modulation index NPC

For the NPC, the modulation index can be computed with the AC voltage in each phase (leg) and the voltage generated by each valve, from equation **(3.8)**, around half of the DC voltage.

$$m_{leg}(t) = \frac{v_{ac,leg}(t)}{v_{dc}/2} \quad \textbf{(3.16)}$$

3.2.5 RMS current in a valve

For the NPC, the RMS current is also calculated using equation **(3.6)**, where *T* is the period of the leg (phase) current. The duty cycle is defined for each of the valves, as shown in equations **(3.17)** to **(3.20)**, and for the clamping diodes, a relation depending on the duty cycle and the direction of the current can also be found, as shown in equations **(3.21)** and **(3.22)**. These relations were verified and validated using the simulation model.

Recalling Figure 11, for the uppermost valve S_1, current is flowing through the valve if the modulation index is positive.

$$\alpha_{S1}(t) = \begin{cases} m(t) \text{ if } \mathrm{m(t)} > 0 \\ 0 \text{ otherwise} \end{cases} \quad \textbf{(3.17)}$$

For S_2 and S_3, since they are active for all three of the voltage levels, they also depend on when the clamping diodes are conducting, so they not only depend on the sign of the modulation index but also on the direction of the current.

$$\alpha_{S2}(t) = \begin{cases} 1 \text{ if } \mathrm{m(t)} > 0 \text{ and } \mathrm{I(t)} > 0 \\ m(t) \text{ if } \mathrm{m(t)} > 0 \text{ and } \mathrm{I(t)} < 0 \\ 1 - |m(t)| \text{ if } \mathrm{m(t)} < 0 \text{ and } \mathrm{I(t)} > 0 \\ 0 \text{ if } \mathrm{m(t)} < 0 \text{ and } \mathrm{I(t)} < 0 \end{cases} \quad \textbf{(3.18)}$$

$$\alpha_{S3}(t) = \begin{cases} 0 \text{ if } \mathrm{m(t)} > 0 \text{ and } \mathrm{I(t)} > 0 \\ 1 - m(t) \text{ if } \mathrm{m(t)} > 0 \text{ and } \mathrm{I(t)} < 0 \\ |m(t)| \text{ if } \mathrm{m(t)} < 0 \text{ and } \mathrm{I(t)} > 0 \\ 1 \text{ if } \mathrm{m(t)} < 0 \text{ and } \mathrm{I(t)} < 0 \end{cases} \quad \textbf{(3.19)}$$

S_4 has a similar operation mode as S_1, it only conduces when the modulation index is negative.

$$\alpha_{S4}(t) = \begin{cases} |m(t)| \text{ if } \mathrm{m(t)} < 0 \\ 0 \text{ otherwise} \end{cases} \quad \textbf{(3.20)}$$

The clamping diodes are only conducing if the AC phase current *I(t)* has a particular direction, for the upper diode, the current should be positive and for the lower diode the current should be negative. For the other cases, their operation mode is like that of valves S_2 and S_3 respectively.

$$\alpha_{CD1}(t) = \begin{cases} 1 \text{ if } \mathrm{I(t)} > 0 \text{ and } \mathrm{m(t)} > 0 \\ 1 - |m(t)| \text{ if } \mathrm{I(t)} > 0 \text{ and } \mathrm{m(t)} < 0 \\ 0 \text{ if } \mathrm{I(t)} < 0 \end{cases} \quad \textbf{(3.21)}$$

$$\alpha_{CD2}(t) = \begin{cases} 1 - m(t) \text{ if } \mathrm{I(t)} < 0 \text{ and } \mathrm{m(t)} > 0 \\ 1 \text{ if } \mathrm{I(t)} < 0 \text{ and } \mathrm{m(t)} < 0 \\ 0 \text{ if } \mathrm{I(t)} > 0 \end{cases} \quad \textbf{(3.22)}$$

4 Methodology for the comparison of AC-DC converters

In this section, a general methodology for the design and evaluation of AC-DC converters is proposed and every aspect is explained in detail. At the end, the KPIs selected for the assessment of the two chosen topologies are presented. This methodology was proposed with the aim to be easily applicable to any converter topology, using analytical expressions as much as possible to allow for a rapid evaluation of the converters.

4.1 Flow chart

Figure 18 shows the flow chart with the general proposed methodology for the design and evaluation of AC-DC converters. As it can be seen, the methodology includes the consideration of grid requirements, topology selection, operating points and degrees of freedom, steady state analysis and design of the converter, transient simulation and finally calculation of the KPIs. These represent the different steps needed to assess a topology. Some iterative loops are shown along the process to verify the compliance with the grid requirements and a satisfactory value for the KPIs. The proposed methodology was used to assess the MMC and the NPC.

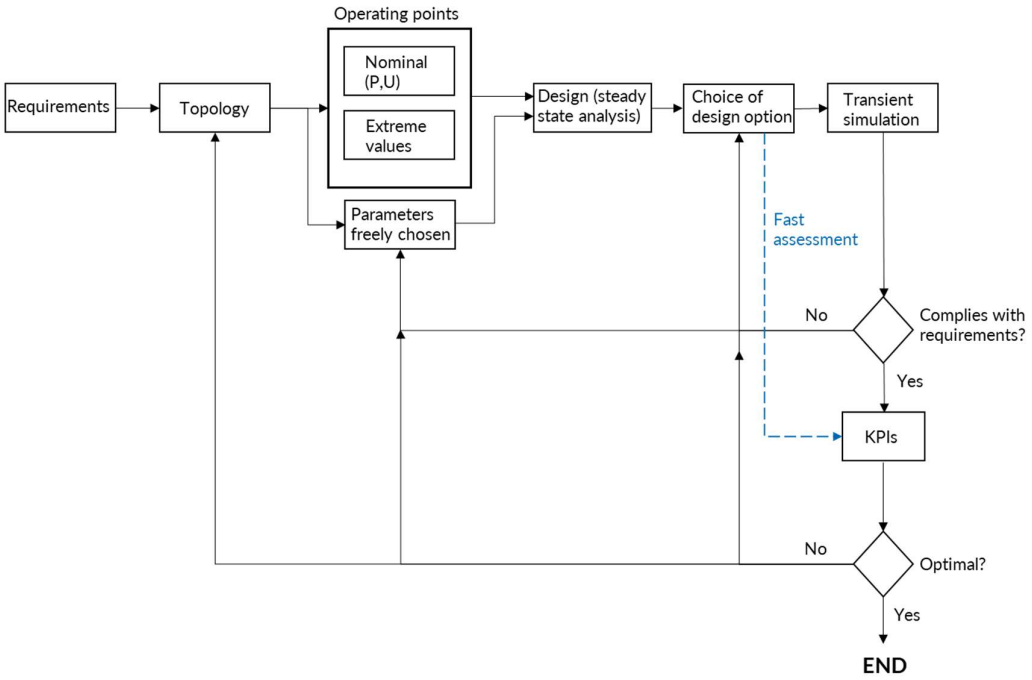

Figure 18 Methodology to follow for the design and evaluation of AC-DC converters

4.2 Requirements

As it can be seen, in Figure 18, the first step is to identify the grid requirements, which are stated by the TSO or the DSO, in France, RTE and Enedis, respectively. As it was explained in section 2.1.1, the requirements change depending on the type of unit, production or generation. They are also different for the transmission and distribution levels. The list of requirements is extensive, and it is key to be familiar with it because a real converter design will have to comply with all the requirements in a real project. The engineer can choose to do a design considering already these requirements or to do a design using other criteria and verify at the end that the chosen design complies with the grid requirements.

4.3 Topology selection

The next step in the methodology is to select a converter topology to evaluate, as it has been mentioned before, for this work the NPC and MMC topologies are studied. In a general case, the selection of topologies can be done based on the state of the art or literature review. The selection will of course depend on the specific application. Depending on the needs, even innovative designs could be proposed and assessed with this methodology. For the purpose of comparison between topologies, the different candidates should be assessed with the methodology independently and at the end, depending on the obtained KPIs, a good indicator of the suitability of a topology for a specific application will be obtained.

4.4 Operating points

It is necessary to define the operating points of the converter. This part depends on the specific application for which the topology is intended to be used. The analysis can be done either with the nominal operating point, or it can cover a range of values, which would be possible operating points or conditions. In other words, depending on the application, an analysis can be done only on the operating point or considering the extreme values or worst-case scenario at which the converter would operate.

4.5 Parameters freely chosen

The parameters freely chosen or degrees of freedom have an impact on the design of the converter so they should be chosen to optimize the design. An example of these degrees of freedom would be for instance, the rating of the IGBT modules to be used in the design, the voltage ripple of the submodule capacitor in the MMC, the choice of using HBSMs or FBSMs or a mix between both for the MMC or the switching frequency for the NPC.

4.6 Design

Once the operating points and the degrees of freedom have been established, the next step is to do a steady state analysis of the topology. In this step, the values of currents and voltages in the equivalent circuit will be found based on the previously chosen operating points. With these values, the design parameters for each topology can be found. For the MMC this could be for instance, the number of switches, the arm inductor or the submodule capacitor. For the NPC, the number of switches, the phase filter or the DC link capacitors. The result of the design will be the sizing of the converter, as it was presented in chapter 3.

4.7 Choice of design option

Depending on the considerations done for the operating points, it is possible to obtain one or several designs, or if only the nominal operating point was considered, a change in the degrees of freedom will also result in different designs. In this step, the different designs obtained should be analysed and the best or most convenient design for the desired application should be selected. This choice can be made depending on different factors that could be important for the project. It could be related to investment cost, reliability, or any other aspect as size or footprint. In some cases, choosing a suitable design option requires to evaluate some KPIs to have a selection criterion thus when the methodology is run for the first time some assumptions can be done to pre-choose an appropriate design option that could be modified once the KPI evaluation is done.

4.8 Transient simulation

After the design stage, one can go a step further and do a transient simulation. The purpose of this simulation is to verify the behaviour and the performance of the design but also to check some parameters which are hard to calculate analytically, like for example the switching losses for some topologies. But most importantly, this step is required to verify that the design complies with the grid requirements, like for example a specific value of THD or the Low Voltage Ride Through (LVRT) characteristic. This step requires having simulation models for

the topologies in study. In case no simulation models are available, the converter modelling should be done and a control design for the topology should be designed, thus this is a time-consuming step.

Therefore, this stage should be avoided when a fast assessment is required. This would be the case in early stages of a converter evaluation or if a comparison between topologies is done. However, to do a complete assessment of the converter (requiring more precise KPIs and the grid requirements validation) this stage will be a must.

If doing the transient simulation, it is noted that the design does not comply with the grid requirements, an iterative process has to be done until the requirements are met. Maybe a different design of the ones obtained can be chosen or the degrees of freedom can be changed. Once it is verified that the design complies with the requirements, the KPIs can be calculated.

4.9 Key Performance Indicators

The last step in the methodology is to calculate the KPIs. If they are not satisfactory or not as good as expected, another iterative process can be carried out, possibly by tuning the freely chosen parameters until a satisfactory result is obtained. If the goal is to make a comparison between topologies, the methodology should be applied to both and the topology with the best KPIs should be chosen. It is possible that some KPIs are better for one topology and some others are better for the other one. In this case, it should be evaluated which KPIs are more important.

Considering the criteria that has been used for making comparisons between converter topologies found in the state of the art and presented in section 2.5, the following KPIs have been selected to assess the two topologies of interest. It should be noted that there could be different KPIs not considered here that could be relevant for other topologies or applications. It is up to the designer to define which ones are important.

- Number of switches
- VA rating of the semiconductors
- Semiconductor utilization factor
- Electric energy factor
- Magnetic factors
- Power losses factor

In the following sections, each of these factors is described in detail for the MMC and NPC.

4.9.1 Number of switches

Table 8 shows the number of switches (IGBT modules with antiparallel diode) and clamping diodes needed for each topology depending on the number of levels. For a 3L-NPC, one would need 4 switch valves and 2 clamping diodes per phase. For the MMC it depends on the number of levels and on the type of SM used.

Table 8 Number of switches and clamping diodes for the NPC and MMC [19]

For (n+1) level	NPC	MMC - HB	MMC - FB
Switches per phase	2n	4n	8n
Clamping diodes per phase	2(n-1)	0	0

Recalling equations **(3.1)** and **(3.8)**, it can be seen that each valve of the NPC needs to withstand half of the DC voltage while a single arm of the MMC has to be able to withstand the entire DC voltage. Considering switches with an ideal rating, one can see that the NPC, having four valves per phase would need the number of switches shown below per phase:

$$N_{sw,phase,NPC} = round\left(\frac{4V_{dc}}{2V_{sw}}\right) = round\left(\frac{2V_{dc}}{V_{sw}}\right) \quad \textbf{(4.1)}$$

The MMC, on the other hand, has two arms per phase, and if only HBSMs are considered, two switches per SM, so the number of switches per phase can be computed with the expressions shown below.

$$N_{SM,phase,MMC} = round\left(\frac{2V_{dc}}{V_{sw}}\right) \quad (4.2)$$

$$N_{sw,phase,MMC} = round\left(\frac{4V_{dc}}{V_{sw}}\right) \quad (4.3)$$

As it can be seen, the MMC would have twice as many switches as the NPC per phase, while the number of clamping diodes per phase would be two for the 3L-NPC, as shown in Table 8.

4.9.2 VA rating of the semiconductors

Two different approaches can be taken for this KPI. The first one is to consider the VA rating of the semiconductors with the operating values of voltage (derated voltage) and current taken from the datasheet. This would be the total installed semiconductor power of a real switch. The other option is to consider the VA rating of the semiconductors if an adapted switch could be used for the specific amount of power that is needed. For this option the real RMS currents of the switch would be considered instead of the one provided in the datasheet. The first approach would be the one used for economic analysis, since the switches should be commercially available, and the price of an adapted switch would be considerably higher. The second approach allows to make a real comparison between the topologies, and it is more interesting to do sensitivity analysis and see how the real *RMS power* changes with other parameters.

Total installed semiconductor power

This is the VA rating of the real component. It is computed with the operating voltage and the DC current of the semiconductor as shown in the equation below.

$$S = V_{operating} I_{nom.switch} \quad (4.4)$$

Switch VA rating based on RMS current

NPC

For the NPC, the VA rating based on the RMS current flowing through a valve is considered. All the switches connected in series would have the same RMS current flowing through them, so they are all behave like one. The RMS current of the switch is the maximum RMS current between the transistor and the diode, as shown in the equations below.

$$VA_{valve} = N_{sw,valve} V_{operating} I_{RMS} \quad (4.5)$$

$$I_{RMS} = max\{I_{IGBT,RMS}, I_{Diode,RMS}\} \quad (4.6)$$

MMC

For the MMC, the average voltage of the SM V_{SM} is considered. Given that there is a capacitor, this voltage unlike for the NPC is not the operating voltage as there is a voltage ripple ε. For the MMC, similarly as for the NPC, the RMS current is the maximum RMS current flowing through any of the transistors or the diodes of a HBSM as shown in Figure 13. These equations can also be extended to the case with full-bridge SMs.

$$VA_{HB} = 2\overline{V_{SM}}(1+\varepsilon) I_{HB,RMS} \quad (4.7)$$

$$VA_{arm} = N_{SM,HB} VA_{HB} \quad (4.8)$$

$$I_{HB\ RMS} = max\{I_{S1\ RMS}, I_{D1\ RMS}, I_{S2\ RMS}, I_{D2\ RMS}\} \quad (4.9)$$

4.9.3 Semiconductor utilization factor

This factor is an indicator of how much the semiconductors are being used, comparing the total semiconductor rating of the topology with the transmitted DC power. The inverse of this factor would be an oversizing factor. They are both related with the investment cost of the semiconductors.

$$U_{SW} = \frac{P_{DC}}{\sum_{i=1}^{N_{switches}} VA_{switch,i}} \tag{4.10}$$

Similar to the VA rating of the semiconductors, the utilization factor can also be considered from two different approaches. One considering the total installed power of the semiconductors and the other one considering the semiconductor rating based on the RMS currents. The first one will show the utilization factor of the real components while for the second one the utilization factor of a fictitious component with the exact VA rating obtained with the RMS currents. The first one will be more interesting for economic analysis while the second one allows a comparison purely of the topology.

4.9.4 Electric energy factor

This factor represents the investment in the capacitors on the topology. For the case of the MMC, the capacitors in the SMs are the ones that determine their size, so for the MMC, this factor is related to both the investment cost of capacitors and the footprint. A small value of E would be preferred from the point of view of investment in capacitors.

$$E = \frac{\sum_{i=1}^{N_{capacitors}} W_{capacitor,i}}{P_{DC}} \tag{4.11}$$

4.9.5 Magnetic factors

The magnetic factors, similarly to the energy factor, represent the investment made in the inductances of the topology. There are two types of inductances considered, inductances with an air core and with a ferromagnetic core that lead to two different factors, as shown in equations **(4.12)** and **(4.13)**. The inductance price depends directly on its apparent power. For the case of a winding around a magnetic core, the size of the inductor will also depend on the frequency, the higher the frequency the smaller the equipment, but this is not at all relevant for inductances with an air core, which is why a distinction is made with the factors.

$$k_{inductance,air} = \frac{\sum S_{inductances,air}}{P_{DC}} \tag{4.12}$$

$$k_{inductance,core} = \frac{\sum S_{inductances,core}}{f.P_{DC}} \tag{4.13}$$

4.9.6 Power losses factor

Unlike the previous two factors that represent in a way the investment costs of the converter, the power losses represent the operation costs of it. For this work only conduction and switching losses on semiconductors will be considered, but the losses of the passive elements (capacitors and inductors) could also be considered for a more complete analysis. To calculate these factors, the total losses of the converter are calculated and presented as a percentage of the transmitted DC power.

$$P_{Sw} = \frac{\sum P_{SW\ switching}}{P_{DC}} \tag{4.14}$$

$$P_{C} = \frac{\sum P_{SW\ conduction}}{P_{DC}} \tag{4.15}$$

5 Implementation

As it can be seen from the previous chapters, there are a lot of analytical calculations to be performed to do the sizing of the converters and to calculate the different KPIs. In this section, the design and implementation of a tool that allows to automate the calculation of all these parameters and KPIs for both topologies is explained in detail. This tool was developed because it is useful to make fast analytical calculations and to allow to compare the KPIs of different topologies for a specific application or to compare different operating conditions or designs of the same topology.

5.1 Programming environment

The tool was implemented in MATLAB. This is because it is the standard software used in the SuperGrid Institute and most of the people in the company are familiar with it. Another important reason is that the simulation models of both topologies are done in MATLAB/Simulink. Even though the goal of the tool is to simplify the design and calculation of the KPIs, there are still some steps in the methodology that require a transient simulation, like for instance the verification of the THD. Therefore, having a tool that allows easy coupling with the Simulink models is important. It is also important to avoid the need of advanced toolboxes, to make the tool as accessible as possible for everyone in the company. Recalling the methodology presented in Figure 18, this tool would perform the steps of Design and calculation of KPIs only.

The tool was implemented with the Object-Oriented Programming (OPP) paradigm. This paradigm was chosen for this tool because it allows to have a modular structure, where it is easy to add and modify functionalities, and simplifies the reutilization of different parts of the code. By splitting the different components of the converters into as many objects as possible, it is possible to use the same objects for different topologies. An example of this would be a class Switch, because all the topologies will be composed of switches in different configurations. MATLAB allows to create classes, which are the building blocks of the tool.

5.2 Tool design

The design of a tool developed with OOP must be planned carefully, since OPP is not sequential, which means it is not executed in a top-to-bottom direction. The tool is composed of classes that represent different parts of the converter. A typical way for representing the classes and its relationships is means a Unified Modelling Language (UML) diagram, as the ones shown in Figure 19. The UML diagram includes key information of the classes. In the top part is the name of the class, then the properties are listed and on the bottom part the methods of the class. The properties are the attributes of the class, which will be used to identify the object, attributes can be different types of variables, and even other classes. The methods are the functions of the class, they describe what the object can do.

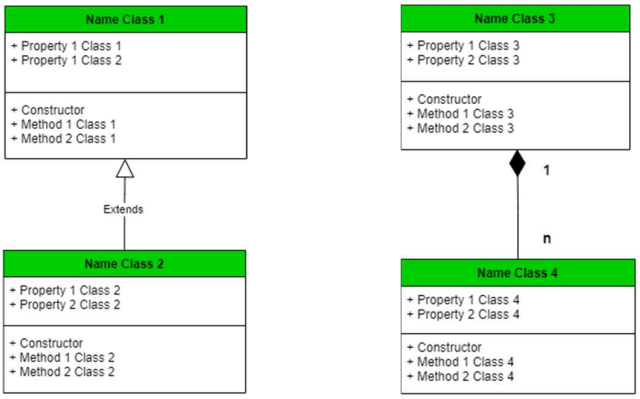

Figure 19 UML diagram representation. Inheritance and composition relationships

From a class, an object can be built, for example from a class *Converter*, a converter object can be built. This object will have all the attributes and methods of the class *Converter* and one can create as many converter objects as desired. Once again, this shows why OPP is so convenient for this tool, one can create as many converters as needed, changing only the input parameters to see how the design evolves, and all this without the need of repetitive scripts. All the classes have a constructor method, which is the method that creates the object.

Another important thing to consider for the design of a code written with OOP is the relationships between classes. There are two main interactions between objects, inheritance, and composition, shown in Figure 19. The inheritance relationships indicates that the Class 2 inherits all the properties and methods of Class 1 plus, it has its own properties and methods. Class 1 is called the parent class and Class 2 the child class. An example of this would be a parent class Converter, which could have many children classes, namely all the different types of converters. The other relationship is the composition. It represents that a class is composed of other classes. For instance, the SM of an MMC converter is composed of switches and a capacitor. The number n in the figure indicates the multiplicity of the composition, i.e., how many objects of one class compose another class. For example, two would be the multiplicity of the switches that compose a HBSM.

The UML diagram of the NPC converter is shown in Figure 21. As it can be seen, the NPC is composed of three legs (3 phases), three inductors which are the AC filters of the three phases and the two DC link capacitors. The inductors and capacitors are the children class of the *Passive* class. Each Leg or phase is composed of six valves, four IGBT modules and two clamping diodes valves. Each valve is composed of several semiconductor devices, which can be IGBT modules (bidirectional switch, IGBT + antiparallel diode) or diodes connected in series. The different power modules are created using features of real devices, whose data is stored in a database, making it possible to make a design with real components.

A detailed UML diagram of the NPC class is shown in Figure 20 as an example of the design done for each class. An implementation example can be found in the Appendix.

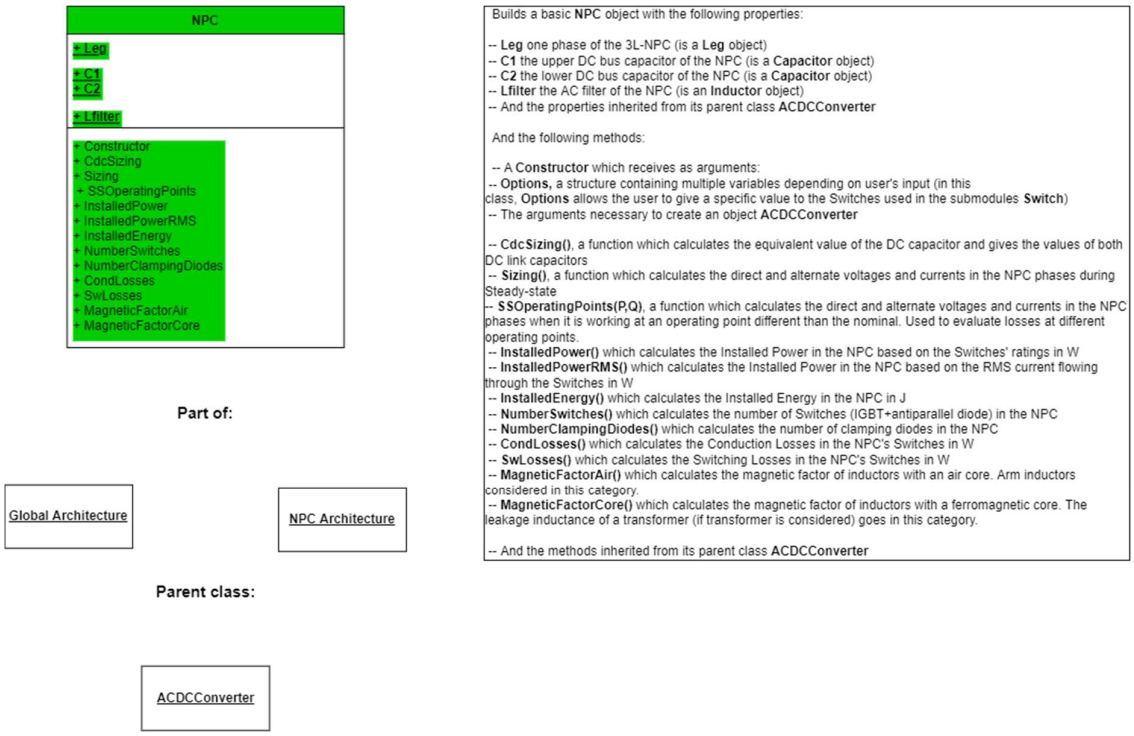

Figure 20 NPC class detailed page

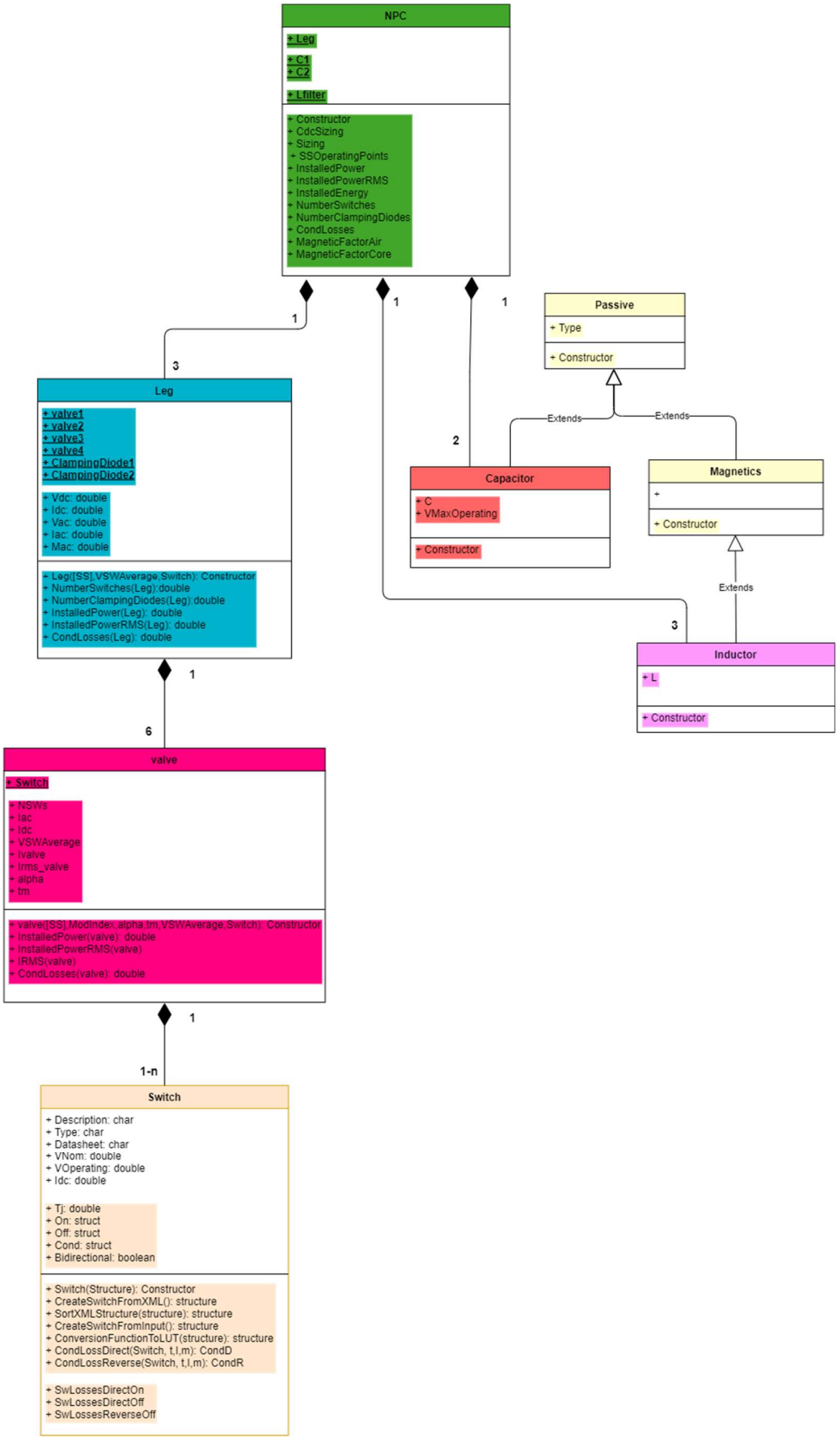

Figure 21 UML diagram of the NPC converter

5.2.1 NPC construction

The construction of an NPC object begins with the input variables that the class needs to create the design. Once the object NPC is created, it will call all the constructor functions of the objects contained in the NPC, sequentially, as it can be seen in Figure 22. As it can be seen, inside the class *NPC*, there is an instantiation for the classes *Leg*, *Inductor* and *Capacitor*. Inside the class *Leg* there is an instantiation for the six valves of each phase, all of them corresponding to the class *valve*. Each valve is itself composed of one or several objects of the class *Switch*. Each class that instantiates other classes needs to send some information, to create the object. In the class NPC, the results of the steady state currents and voltages, and the value of the DC link capacitors and the AC filter are calculated, and so, their values can be sent to the corresponding classes. Likewise, inside the class *Leg*, the modulation index is computed, which is then sent to the corresponding valves.

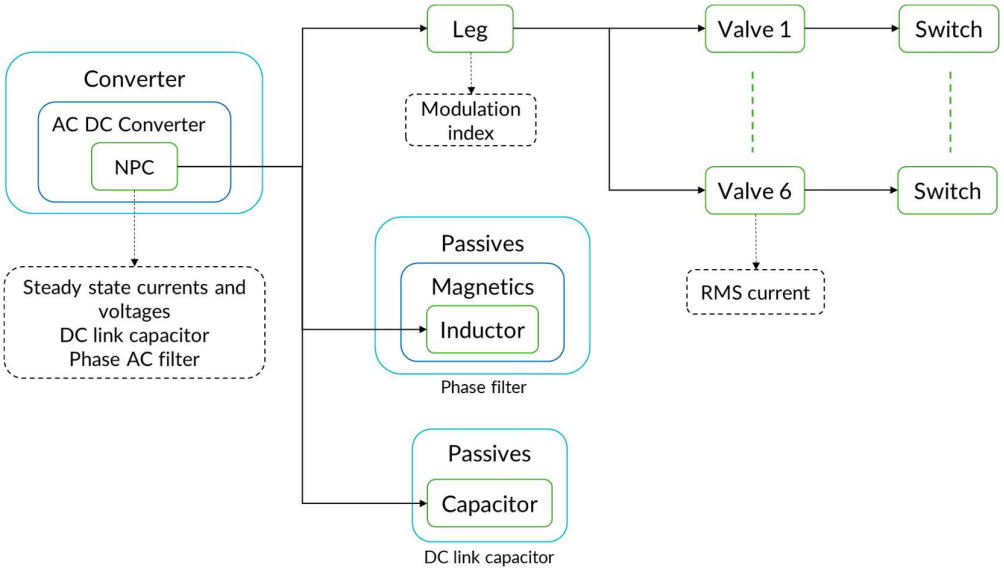

Figure 22 NPC instantiation with all the stages

The class *Switch* is the exception, as it is not instantiated inside the class valve. Instead, the Switch object is created apart from the NPC converter, its information is taken from a database containing the datasheet information, and the design is made based on the characteristics of the selected module. In fact, the selection of the module to be used for the design is part of the inputs, as the data is taken from an external source.

The inputs needed to create an NPC object are the following:

- *VdcNom*, the nominal voltage of the DC grid
- *VacNom*, the nominal voltage on the AC side
- *PNom*, the nominal active power at the PCC, the point of connection to the grid
- *QNom*, the nominal reactive power at the PCC
- *FreqOp*, the operating frequency of the AC side
- *Nphases*, the number of phases of the converter
- Options, a variable containing the degrees of freedom for the design. If no value is given, a default value will be used
    - Switch, the model of the power module to be used for the converter design. A single model can be chosen for all the valves, or two models can be chosen, one for the IGBT modules and one for the clamping diodes.

The detailed process of calculation needed for the NPC is shown in Figure 23. This methodology of calculation starts with the inputs mentioned above and the desired outputs, shown in the right-hand side of the diagram are the KPIs, defined in section 4.9.

As it can be seen, the design of the converter is done using the nominal operating point of the system. But if a different operating point was chosen, some of the KPIs shown in the diagram would change. To be clear, the design would remain unchanged, and with the fixed design, different values of current would be obtained. The variables that would change with the operating point are the RMS current, the total semiconductor VA rating based on the RMS currents and the switching and conduction losses.

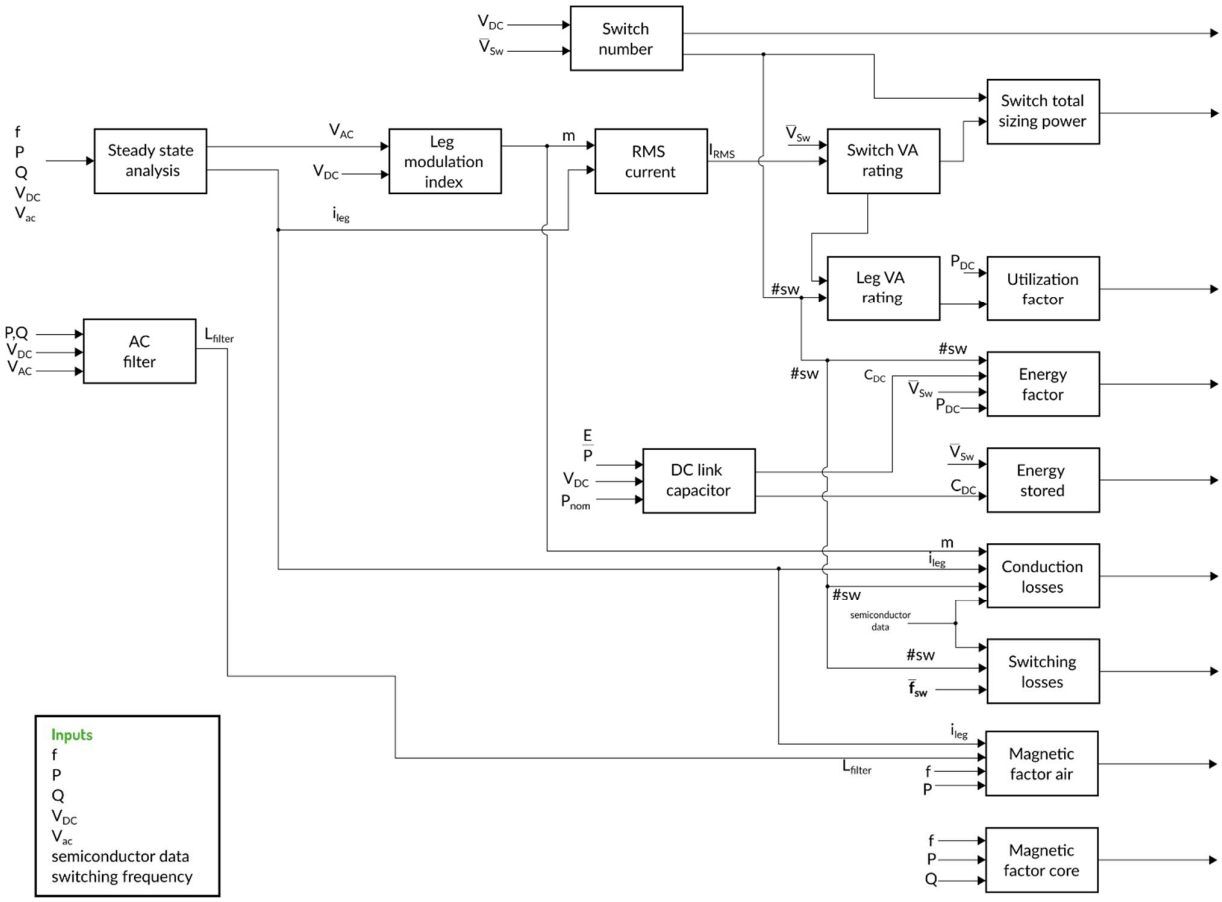

Figure 23 Methodology for the obtention of the proposed KPIs for the NPC

5.2.2 Tool workflow to calculate the KPIs

The tool calculates the KPIs by retrieving the values from the lower level to the higher one. There are functions implemented in each class that are recovered and summed by the higher class until the highest level is reached. In Figure 24 it can be seen for instance how the conduction losses are first calculated in the switch, then the sum of the conduction losses of all the switches in a valve is retrieved in the class valve. Similarly, the sum of the conduction losses of all the valves in a phase are retrieved in the class Leg and so it continues until the highest class. This is done not only for the KPIs but also for other design parameters such as the number of switches.

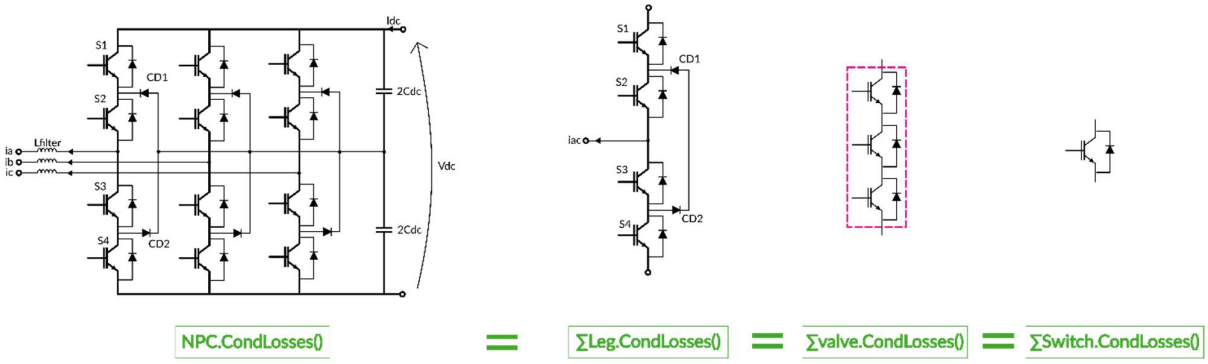

Figure 24 Tool workflow for calculation of conduction losses

The modularity of the tool allows to know not only the values of the KPIs and design parameters for the full NPC converter, but also in the different levels of the converter. One can easily get the conduction losses in a single switch, or the number of switches in a single valve if needed.

5.3 Detailed workflow

The process that follows the utilization of the tool is shown in Figure 25. As it was mentioned previously, some input data are needed for the tool to create the converter objects with the design and KPIs calculation automatically. These data include the semiconductor data, the operating conditions, and the degrees of freedom, such as the type of switch to be used, the voltage ripple for the SM capacitor or the switching frequency. With these inputs the tool creates an object with all the stages shown in Figure 22. Inside the tool, a steady state analysis of the system is done, and the result is a design based on the nominal operating points. This step is automated. The next stage is the post processing with the obtained design. Here, a script retrieving the results of the internal functions of the converter is needed to do data treatment and analysis. Finally, given that this tool is not meant to be user friendly and has no graphic interface, the designer can decide how the results will be displayed, depending on the needs. Tables or figures summarizing the results of the post-processing stages could be done in this part.

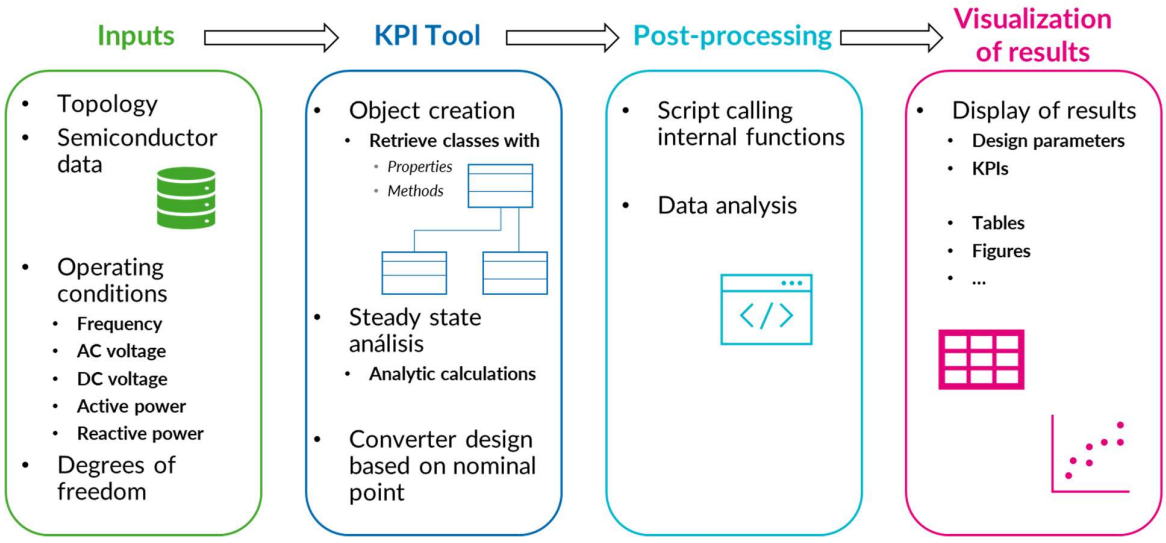

Figure 25 Workflow to use the tool

In this section, the design of the tool for the NPC converter has been explained in detail. The same philosophy applies for the MMC converter, whose implementation had already been done previously in the SuperGrid Institute and it is thus not presented here.

6 Case study and results

The general system considered consists of the AC grid, an AC/DC converter and the DC grid, as it can be seen in Figure 26. The NPC would also include an AC filter. The goal is to analyse how the KPIs and other design parameters of the converters evolve with all these inputs to finally determine which topology is more appropriate for a specific voltage and power level.

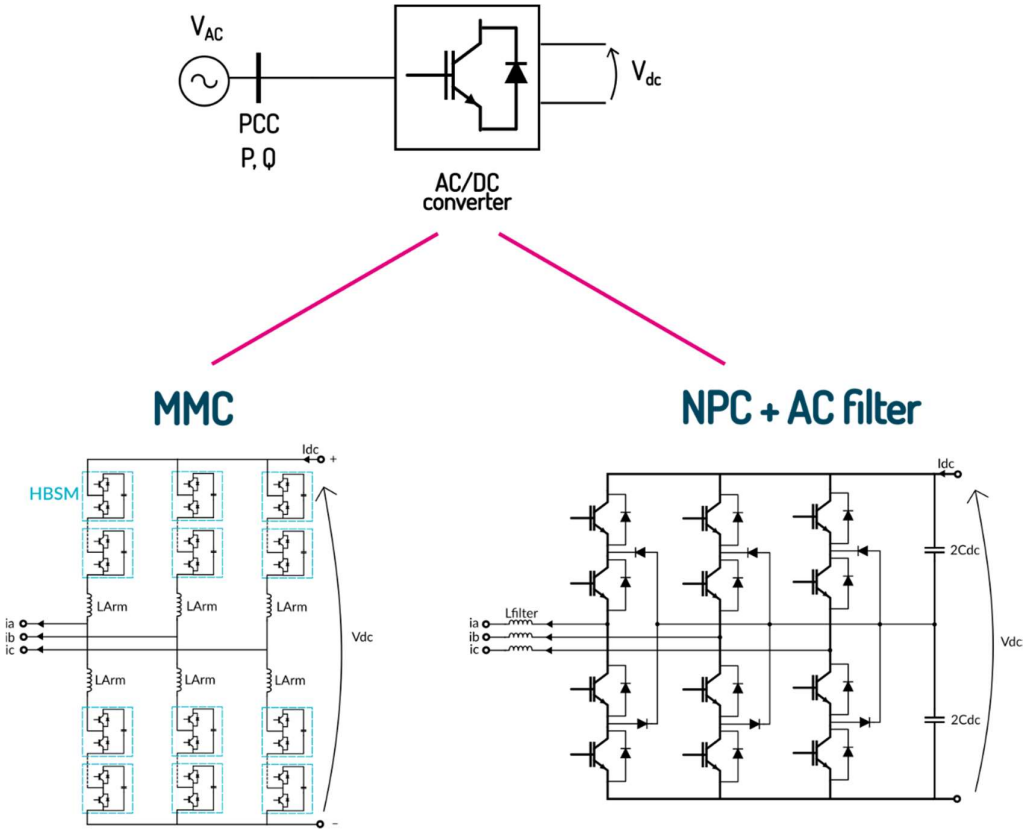

Figure 26 General scheme of the system under study

6.1 Selection of voltage level and power levels

As starting point, the voltage levels at which it the comparison is done are determined. The CIGRE [13] proposes some recommended DC voltage levels for distribution networks, based on different criteria such as the insulation requirements of the lines and cables, matching the voltage levels of the DC loads and connecting the AC and DC grids without a transformer. The following equation shows the maximum AC voltage that a VSC converter can produce at its AC terminals depending on the DC voltage. In this equation no third harmonic injection is considered.

$$U_{AC} \leq \frac{U_{DC}}{2}\sqrt{\frac{3}{2}} \tag{6.1}$$

In Table 9 the DC distribution voltage levels recommended by the CIGRE are presented. In the left-hand side, the nominal levels of the AC grid are presented, on the middle column, the recommended DC voltage levels and on the right-hand side, the maximum calculated voltage that the converter could generate in its AC terminals depending on the DC voltage.

Table 9 Recommended DC distribution voltage levels [13]

AC Voltage levels [kV]	Recommended DC distribution voltage levels [kV]	Max U_{AC} calculated with equation (6.1) [kV]
6	±6	7.3
10	±10	12.2
20	±20	24.5
35	±35	42.9
110	±100	122.5

As it can be seen in the third column of the table, for all the recommended levels, equation **(6.1)** shows that it is possible to generate the required AC voltage (shown in the first column) without the need of a transformer, which is why no transformer is considered for the general system. Besides the shown voltage levels for the DC distribution network, the value of ±50 kV is of interest, so it will also be considered in this study case for a total of six voltage levels.

As regards the DC current, two different values are considered 630 A and 1500 A. The first value is chosen because the equipment for distribution level networks has as nominal current 630 A. The second value is chosen because it is the nominal current used in HVDC applications. These two values plus the different voltage levels should allow to have a wide range of cases for the analysis.

In Table 10 all the possible combinations for voltage and current are presented on the first three columns. On the right hand side the grid requirements for the connection to the distribution or transmission grid are considered, and taking into account Table 1 and Table 2 it is shown to which system operator can a producer or a consumer get connected to according to the power level. As it can be seen, the producers are required to get connected to RTE in most of the cases. This information is important because as it was shown in section 2.1.1 the requirements are different for transmission and distribution levels.

Table 10 Transmission or distribution system operator to get connected to according to the power level for each case

DC voltage [±kV]	DC current [A]	DC power [MW]	Producer Can connect to	Load Can connect to
6	630	7,6	Enedis	Enedis
10	630	12,6	RTE	Enedis
20	630	25,2	RTE	Enedis
35	630	44,1	RTE	RTE
50	630	63	RTE	RTE
100	630	126	RTE	RTE
6	1500	18	RTE	Enedis
10	1500	30	RTE	Enedis
20	1500	60	RTE	RTE
35	1500	105	RTE	RTE
50	1500	150	RTE	RTE
100	1500	300	RTE	RTE

Degrees of freedom in the system

The main degree of freedom that can be considered for the general system is the semiconductor rating. This will affect the entire design of the converter, namely by altering the number of power modules needed and the losses of the overall system. Other degrees of freedom for the MMC include the selection of HBSMs or FBSMs, the voltage ripple of the SM capacitor or the criteria used for the design of the arm inductor. For both converters, the switching frequency could be varied, which would not affect the design, but would have an impact on the switching losses. Table 11 shows the design hypotheses and degrees of freedom selected for both topologies.

Table 11 Design hypothesis and degrees of freedom for both topologies

Degree of freedom	MMC	NPC
Switch rating	3.3 kV	3.3 kV
Switching frequency	175 Hz	1250 Hz or 650 Hz
Voltage ripple C_{SM}	10%	-
Arm inductance	15% of Z_{nom}	-
Type of SM	HBSM	-
Energy to power ratio	-	10 kJ/MVA

6.2 Results and discussion

For the results the proposed methodology was used for the evaluation of both topologies of converters. Firstly, the design was obtained for each case, using the developed tool and taking as operating points the cases presented in Table 10. Then, a transient simulation was performed to check the switching losses and the compliance with the THD requirement. An iterative process was done when needed and finally, after checking the compliance of the THD requirement with the simulation, a comparison of the KPIs was done. In a first analysis, the analysis was done only on the nominal operating point, and it as assumed that only active power is transmitted.

6.2.1 Harmonic analysis

A harmonic analysis was done using the transient simulation. A discrete Fourier transform was done in MATLAB for the AC current extracted from the Simulink model. Considering that for most of the cases, a production unit would have to get connected to the transmission grid of RTE, as shown in Table 10, the requirements for the transmission level shown in Table 3 have been considered here. The first thing that was checked was the THD, which must be under 8%.

6.2.1.1 THD for the MMC

Figure 27 shows the THD of the MMC for the different voltage levels. The switching frequency used for the MMC was 175 Hz. This frequency was chosen for being high enough (at least three times higher than the fundamental frequency) and not a multiple of the fundamental frequency. On the left-hand side figure, it can be seen, the THD of the MMC remains below 2% for almost all the voltage levels, except for the lowest value. For this value (±6 kV) the quality of the AC current is not very good, and there is a voltage ripple higher than 10% in the DC bus. One of the reasons for this could be the selected switches of 3.3 kV. The average voltage of the SMs is 1.8 kV, so every time a SM is inserted or bypassed the transition is of more than 10% of the DC voltage value.

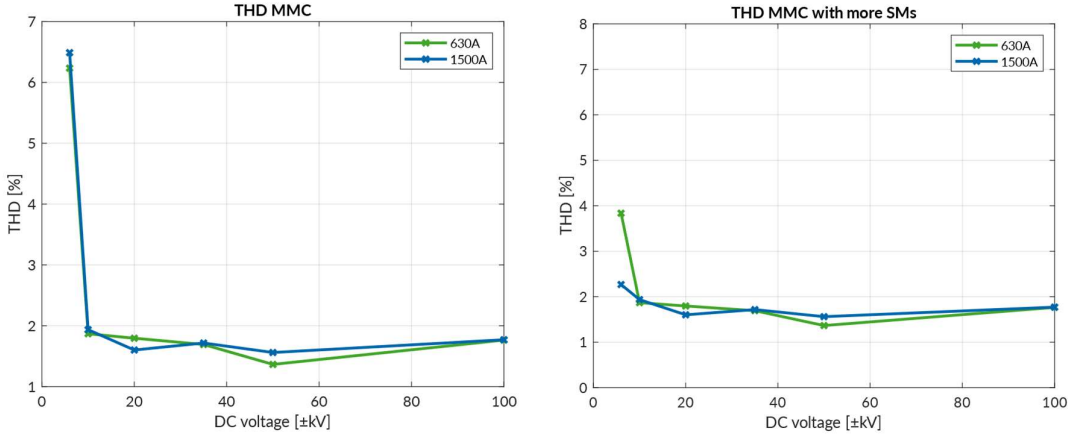

Figure 27 THD for the different voltage levels for the MMC

A possible solution is to increase the number of SMs in the arm in order to decrease the voltage step size, and thus to improve the quality of the output voltage. With this approach, an improvement in the AC current (as well as a decrease in the DC voltage ripple) was observed but increasing the number of SMs also means an increase on losses. An important improvement on the THD was obtained, as it can be seen on the right-hand side figure.

Considering the grid requirement to have a THD smaller than 8%, it is achieved for the MMC for all voltage levels with any of both design choices. In view of this, the initial design is maintained, without adding more SMs, as this would affect the KPIs.

6.2.1.2 THD for the NPC

Figure 28 shows the THD obtained for the NPC at two different switching frequencies f_{sw}, 1250 Hz and 650 Hz. The first switching frequency was chosen for being used in real projects with topologies based on the NPC [18]. Considering that this is, however, quite a high frequency and that therefore it is expected that there will be high switching losses as a result, a smaller frequency or around half of the value was chosen to see the impact on the THD. This analysis was done to check one of the degrees of freedom for this topology, and to choose the most convenient option.

As it can be seen, the THD seems to increase as the voltage increases, already a big difference compared to the MMC, whose THD remains almost constant over the entire voltage range. It can also be seen that the THD for the NPC operated with a switching frequency of 650 Hz is much higher than the THD for the NPC with a switching frequency of 1250 Hz. In fact, the NPC with a switching frequency of 650 Hz has a THD much higher than the required 8%. This option must be then discarded as it does not comply with the grid code. The design of an NPC with a switching frequency of 1250 Hz is kept and the rest of the analysis are made for this design. As alternative a more complex AC filter could be proposed to make the 650 Hz design comply with the grid requirements.

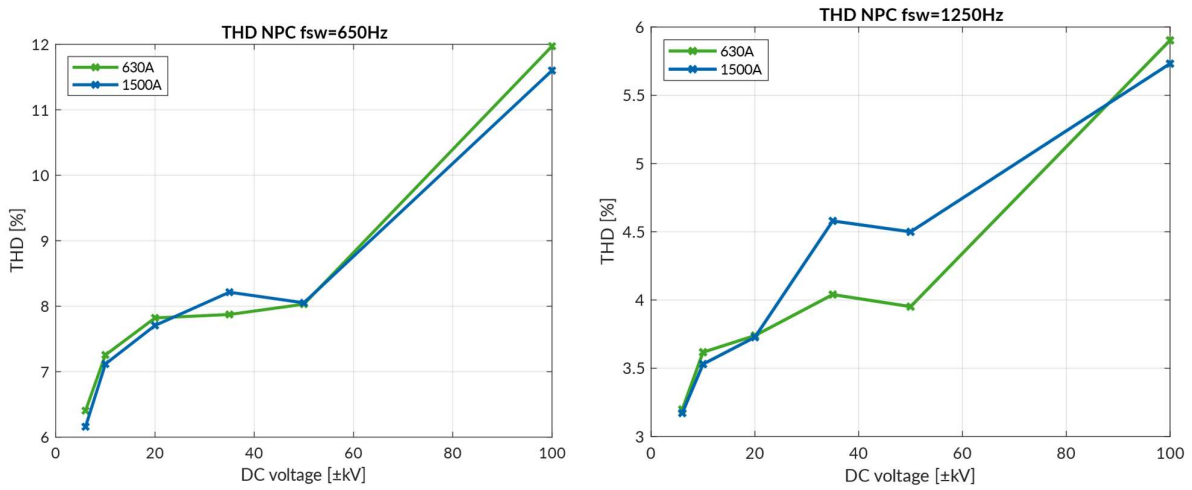

Figure 28 THD for the different voltage levels for the NPC at two different switching frequencies; 650 Hz and 1250 Hz

6.2.1.3 Harmonic spectrum

Figure 29 shows the harmonic spectrum for the MMC and the NPC with both switching frequencies for one of the cases, ±35 kV (70 kV pole to pole) and 630 A. In the figure, the limits of each harmonic component are shown with an "X", according to the grid requirements of Table 3. As it can be seen, the NPC has high harmonic components for their respective switching frequencies, being much worse for 650 Hz. This trend was observed for all the different cases, becoming worse at higher voltages. It should be noted that the AC filter was not resized for each switching frequency, thus it is expected that at lower switching frequencies the AC inductor presents a lower impedance to attenuate sufficiently the harmonics.

This high harmonic at the switching frequency causes the THD to worsen with the voltage, which explains the trends of Figure 28. It can be seen that these harmonics values are actually beyond the levels stated in the requirements, meaning that the filter designed as explained in section 3.2.3 is not enough for the filtering needs.

Recalling, the AC filter for the NPC converter was done to guarantee a specific AC voltage in the terminals of the converter, and the THD requirements were not taken into account for the design stage. The results here presented show that a more sophisticated filter is needed for both switching frequencies, according to the state of the art a series of LC or an LCL filter. However, the design of such a filter requires an iterative process with time consuming simulations, which goes beyond the scope of this project. Thus, the inducive filter is kept for the rest of the analysis.

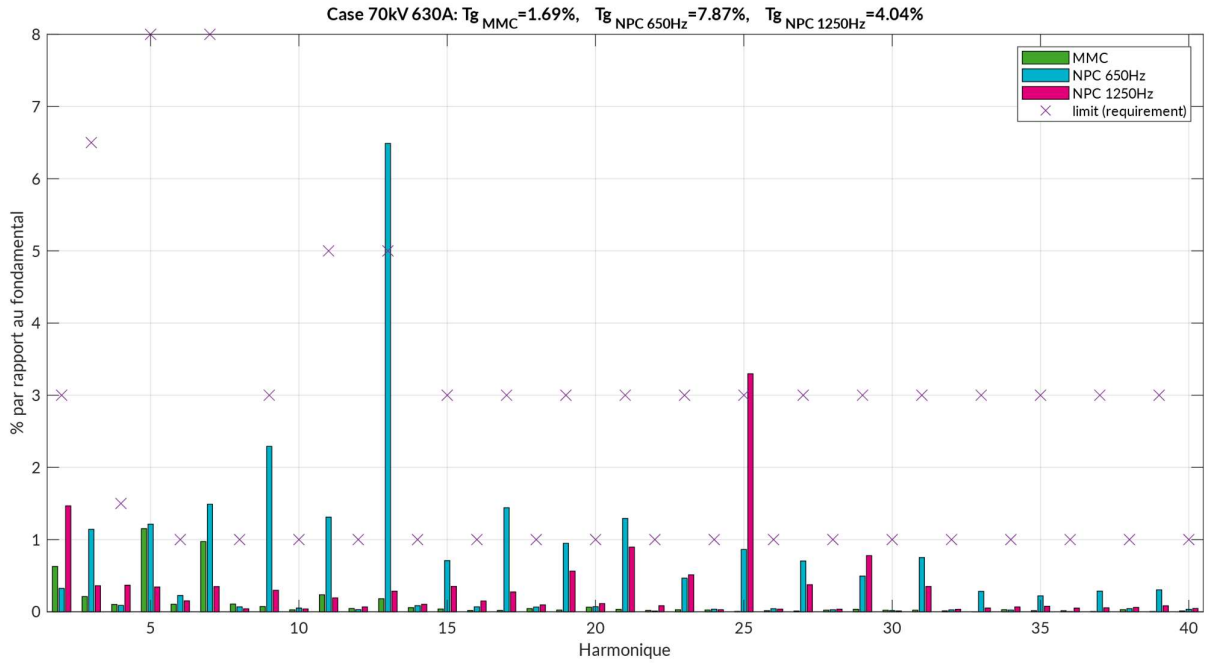

Figure 29 Comparison of harmonics distribution for 70 kV and 630 A

From Figure 29 it can also be seen that the harmonic components of the MMC are quite small, much below the maximum stated limit. The results here discussed show that the MMC has a much better performance in terms of THD, and the design stage is much easier, considering that no filter is needed.

6.2.2 Semiconductor number and installed power

The first set of KPIs refer to the semiconductors installed in the converter, which accounts for the initial investment. The number of switches, the total installed power on semiconductors and the utilization factor are indicators of this. As it is expected, the number of semiconductor devices increases as the voltage increases, and as it is expected, the MMC has a higher number of switches than the NPC. In total, the number of semiconductor devices considering the clamping diodes for the NPC is still higher for the MMC, meaning that a greater investment is needed for this topology.

This can be confirmed by Figure 30, which shows the RMS power for both topologies and the utilization factor. For purposes of comparison, the RMS power, meaning the real power that is used in the topology is considered here. As it is expected, the RMS power is higher when working with a DC current of 1500 A. This is because the RMS current flowing through the switches or diodes will be higher. In addition, the MMC has a higher RMS power due to the higher number of switches.

From the utilization factor graph it can be seen that the utilization factor does not change with the DC current. This is because even though the nominal power increases with the DC current, the RMS current also increases

proportionally to the nominal power, so the ratio shown in equation **(4.10)** is the same regardless of the DC current. On the other hand, the NPC has a higher utilization factor, meaning that it is better than the MMC for this type of KPIs.

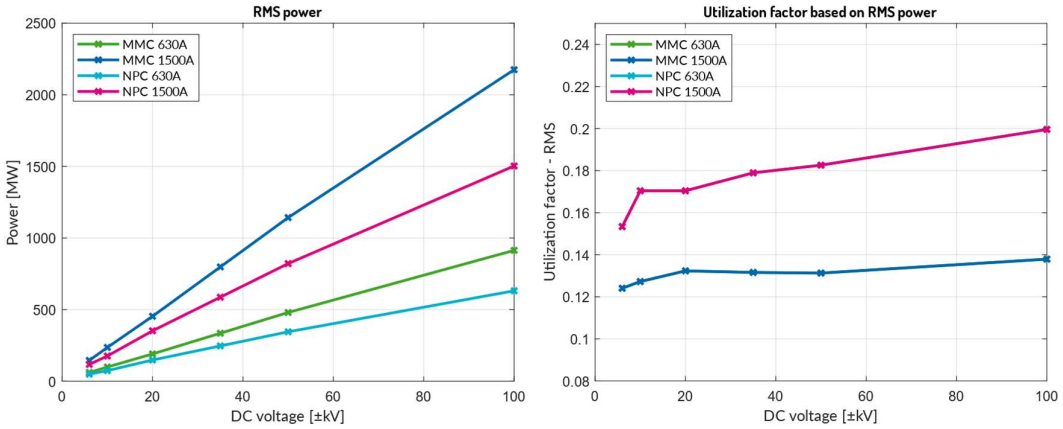

Figure 30 Semiconductor power based on the RMS currents and corresponding utilization factor for both topologies

It is important to mention that although the NPC needs less semiconductors as a topology, the series connection of these devices in the valves require the use of snubbers, which were not taken into account for this analysis.

6.2.3 Weight/size of the converter

The passive elements of a converter are a good indicator of its weight and size. The size of an MMC SM for example, is basically determined by the SM capacitors [38]. KPIs such as the energy and magnetic factors can give a good hint on the weight and size. In this section, the topologies are compared based on the passive elements.

6.2.3.1 Inductances and magnetic factor

Figure 31 shows the phase inductances of each topology and the magnetic factor for inductors in air. For the MMC it shows twice the arm inductance and for the NPC, the AC filter. As it can be seen, with the selected methodology to calculate the AC filter, the NPC would need a higher inductance per phase compared to the MMC. This is not a surprise, as one of the advantages of the MMC is precisely that it doesn't require an AC filter, due to its numerous voltage levels. It can also be seen that as the voltage increase so do the inductances, which is expected, and that the inductors are higher for the higher DC current. This all has to do with the fact that the nominal power is increasing, and the calculations of the inductors depend on this power.

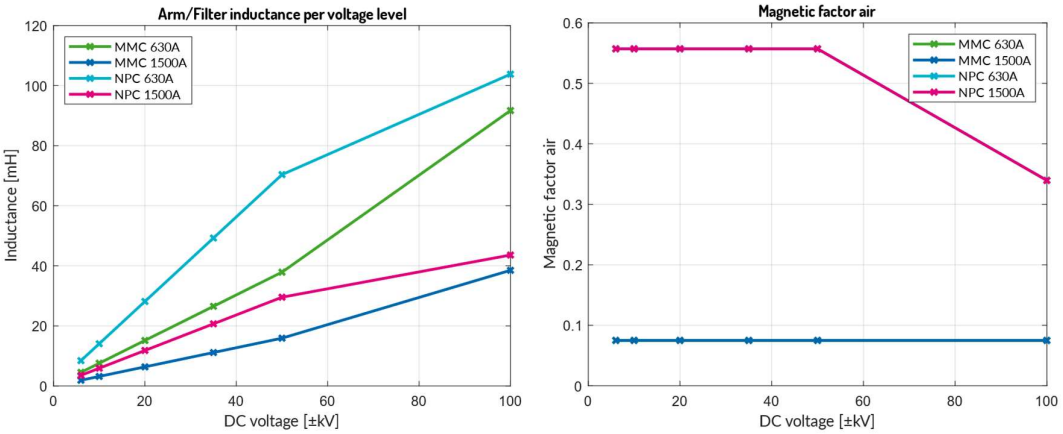

Figure 31 Phase inductance and magnetic factor for both topologies

For the magnetic factors, it should be noted that a hypothesis of all the phase inductances having an air core was made and the conclusions derived from it are only valid under that assumption. It can be seen on one side, that the NPC has a much higher magnetic factor. It is interesting to see how for the MMC the magnetic factor does not change with the DC current nor with the voltage. This is because of the assumptions made for the design of the MMC arm inductors: the arm inductance is a fixed percentage of the system base impedance, which increases in the same proportion as the nominal power, so the relation between the apparent power and the transmitted power is a constant value. For the NPC this is not the case, it can be seen that the last point is different from the rest. This is because the reactor value depends not only on the transmitted power but also on the AC and DC voltages, as shown in equation **(3.15)**. The AC and DC voltages increase in the same factor for all the points except the last one, resulting in the last point being different from the rest.

6.2.3.2 Installed energy and energy factor

Figure 32 shows the installed energy and the energy factor for both topologies. As it can be seen, the MMC has a higher installed capacitor energy regardless of the voltage level or DC current. This is logical, since it has capacitors installed in every submodule, while the NPC only has two DC link capacitors. For the NPC, the two DC bus capacitors only filter high frequencies, the low frequencies are cancelled out on the capacitor terminals because of the three-phase equilibrated system. On the other hand, for the MMC, each capacitor has to filter the grid frequency (50 Hz), which is very low. It can be seen that for both topologies, the installed energy is higher with the higher DC current. For the MMC this is because when the DC current increases, so does the nominal power and thus the energy swing, as shown in equation **(3.4)**. For the NPC it is simply because the higher the DC current the higher the power and hence the capacitor needed is bigger, as shown in equation **(3.9)**.

It is interesting to see the energy factor. As mentioned before, the value obtained for the NPC depends entirely on the hypothesis made for the energy to power ratio, which is typically between 10 kJ/MVA and 50kJ/MVA. From the graph, it would seem like the energy factor of the MMC is higher than that of the NPC, but if the hypothesis of the energy to power ratio changed from 10 kJ/MVA to 30 kJ/MVA, both topologies would have around the same value. If then the hypothesis was that the energy to power ratio is 50 kJ/MVA, the NPC would have a higher energy factor than the MMC. On that account it is not possible to conclude from this, which topology has a higher energy factor. More details should be considered to estimate the energy to power ratio and to be able to make an evaluation and comparison between both topologies. Moreover, the distribution of energy is very different in both topologies. For the MMC the energy is distributed in several low voltage capacitors while for the NPC all the energy is concentrated in only two high voltage devices in the DC bus.

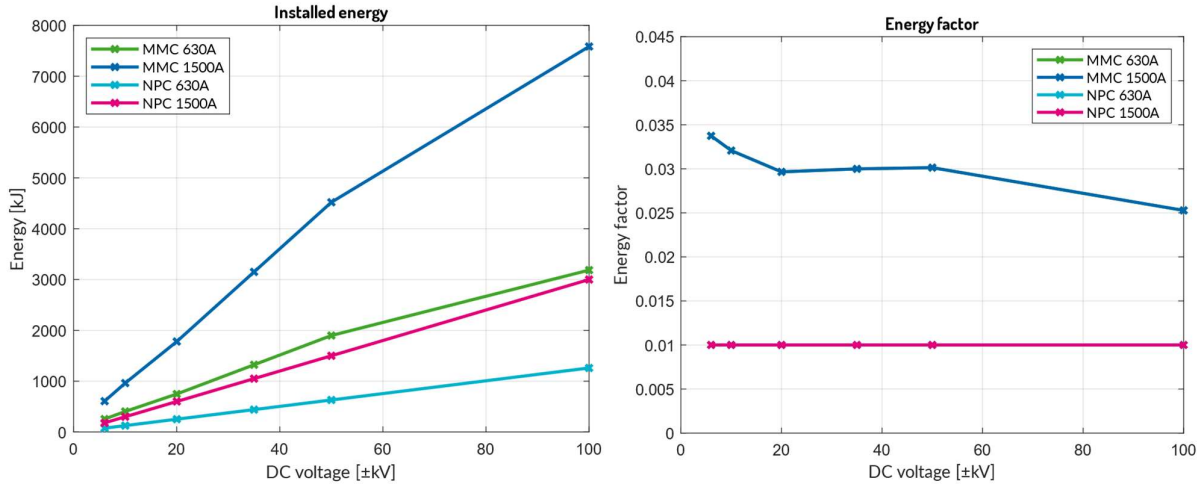

Figure 32 Installed Energy and Energy Factor for both topologies

6.2.4 Efficiency of the converter

The efficiency of the converter and the operating costs are related to the converter losses. Here, only semiconductor losses have been considered.

The losses were estimated using equations **(2.2)** and **(2.3)** and the curves presented in Figure 7. No linear approximation was done, instead a look-up table was built from the curves and the points that are not to be found in the table were estimated using linear interpolation.

The switching losses for both topologies were estimated using the simulation models. For the MMC, the data of a single switch was taken, and its losses were multiplied by the number of switches, making the assumption that this single switch would behave as the average switch. A test was done taking the data of several switches and an error of around 3-4% was found. For the NPC, the data from all the valves in one Leg were taken.

Figure 33 shows the losses distribution for the 12 different cases. On each case, the bar on the left represents the MMC losses and the bar on the right the NPC losses. On each bar, the bottom part represents the conduction losses and the top part the switching losses. At a first glance it is easy to see that the losses of the NPC are considerably higher than those of the MMC, and taking a closer look, it is easy to see that this is particularly due to the switching losses. The conduction losses do not seem to be too different between both topologies, but the switching losses are much higher for the NPC. Of course, this result was expected, due to the high commutation frequency of the NPC and since one of the very well-known advantages of the MMC is the reduction in switching losses. Additionally, the difference between the switching losses for both topologies is important, the losses are almost doubled on the NPC, at least with the hypothesis made for this case study. This difference could be reduced if a better filter was designed allowing for a smaller switching frequency for the NPC and thus reducing its switching losses.

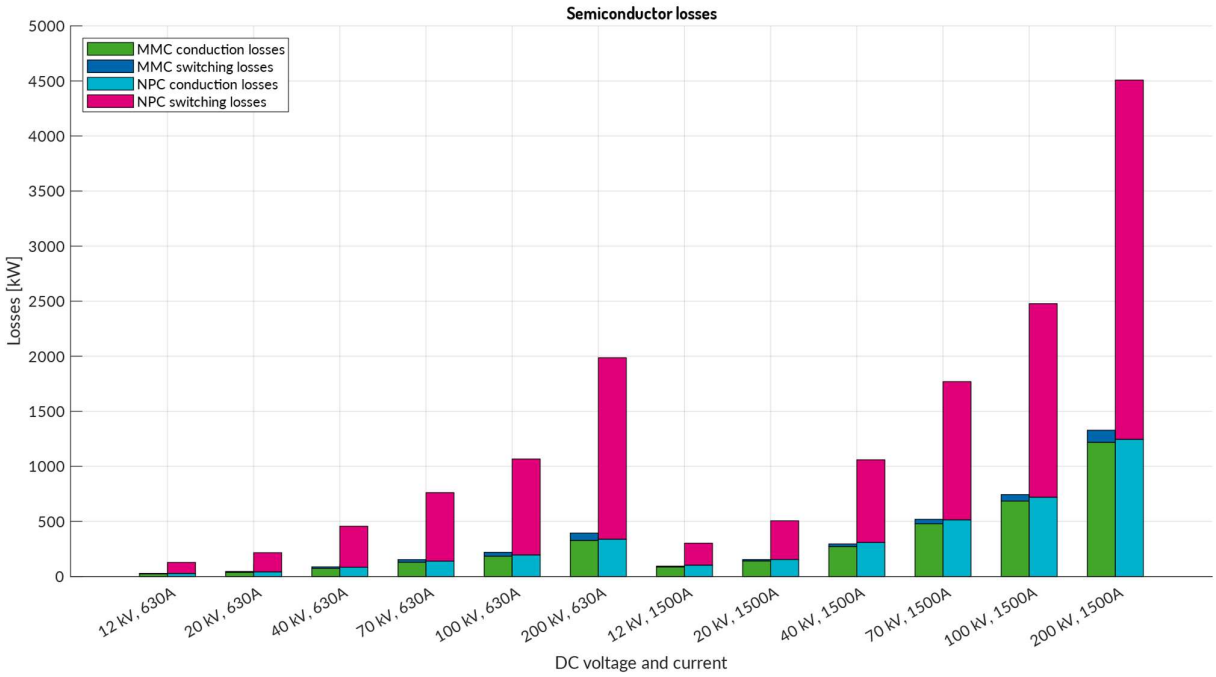

Figure 33 Semiconductor losses for each case

It can also be seen that at higher DC current, the losses will also be higher, which is expected since the power is higher and therefore the current flowing through the Leg and Arm of the NPC and MMC respectively will be higher. Something interesting that was observed is that the losses seem to be inherent to the topology.

When comparing the losses to the nominal power in each case, it was found that the losses factor is pretty much constant, around 0.5% for the MMC and 1.7% for the NPC, as it can be seen in Figure 34. This suggests that the losses are inherent to the topology and do not depend on the voltage level.

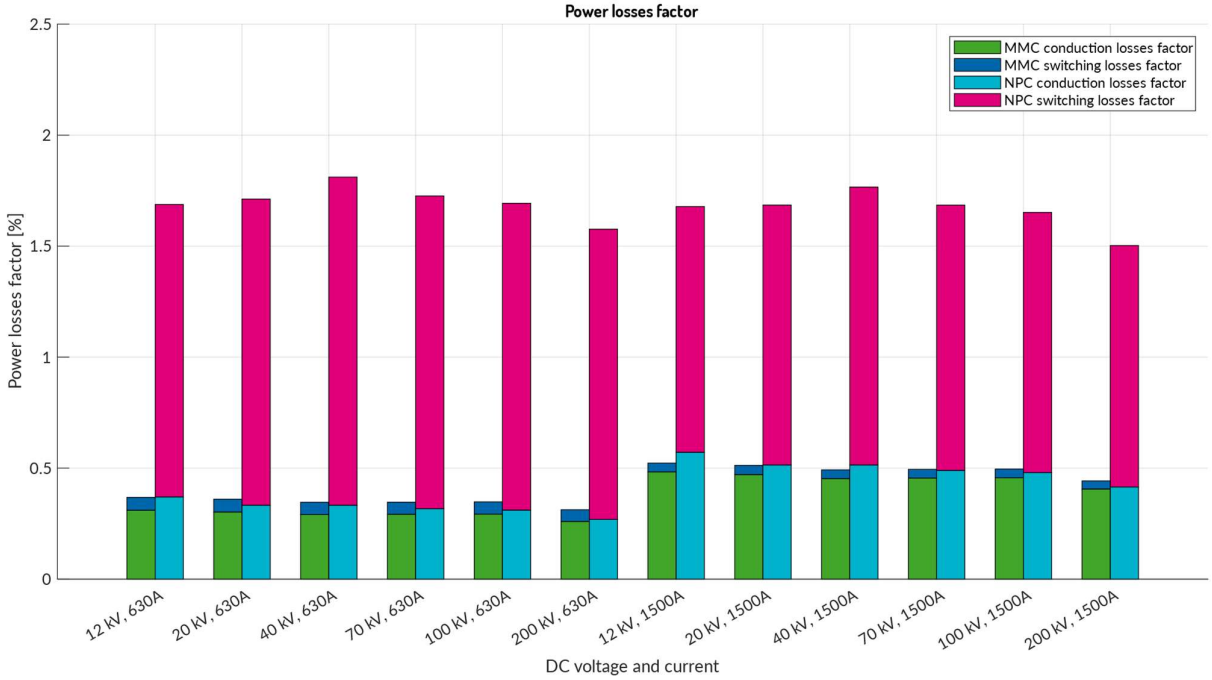

Figure 34 Semiconductor losses factor for each case

An iterative process was done with two different switching frequencies for the NPC, 1250 Hz and 650 Hz as previously and it was found that the converter has much smaller switching losses at the lower frequency, but they were still however much greater than the switching losses of the MMC. This case is however not here shown as that particular design does not comply with the THD requirements.

6.2.5 Synthesis of results

Figure 35 shows the KPIs for both topologies in a condensed way. Four cases have been chosen to evaluate the changes with voltage and power, the lowest and the highest DC voltage ±6 kV and ±100 kV and the two values for the DC current, 630 A and 1500 A. The spider charts show the values of each KPIs in a grid, where the highest value is in the outer part. In this case, the inner part shows the better performance, so the closer to the centre, the better the KPI. In order to keep this as a rule for all the KPIs, the utilization factor is not represented here, instead the oversizing factor is shown to maintain the better value towards the centre.

Starting with the KPIs related to sizing or semiconductors, namely the number of switches, clamping diodes and the oversizing factor (inverse of the utilization factor), it can be seen that the NPC is more advantageous. Even when considering the clamping diodes for the total semiconductor devices, the investment in terms of semiconductors for the NPC is much lower than for the MMC.

On the weight or size related factors, i.e., the energy and magnetic factors, it is hard to reach a conclusion, on the one hand due to the hypothesis made for the inductances, assuming they are all in air. If this was the case, the MMC would be much better. For the energy factor, it is hard to reach a conclusion, since it could change depending on the assumption done for the energy-to-power ratio for the NPC, as explained earlier.

Moving on to the power losses, it is clear that the MMC presents a better performance than the NPC in terms of losses, particularly due to the switching losses, since the conduction losses do not seem to be too different between the two topologies. For the losses, it would be more convenient to work at the lowest DC current.

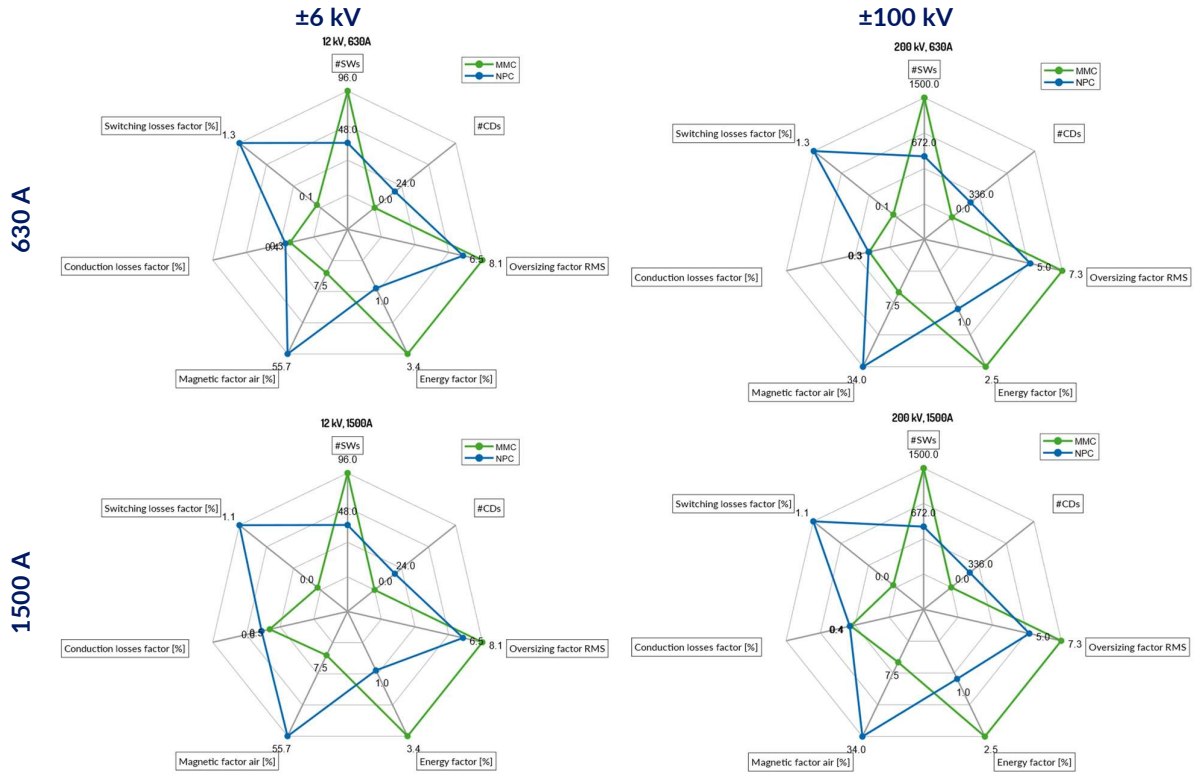

Figure 35 Spider charts comparing NPC and MMC KPIs for four different cases

It is interesting to see that these trends do not change with the voltage or DC current. The sizing is always better for the NPC and the losses are always better for the MMC. With the KPIs considered here, no crossing point (where one topology becomes more advantageous than the other) was found over the voltage range. Another possibility would be to do a further analysis considering the economic aspect, as it was done in [21]. Given that the NPC has a lower investment cost (related to the semiconductors) but a higher operating cost (related to the losses), the crossing point where one topology is more advantageous than the other will depend on the application load profile and the time horizon of each project, for which more economical aspects must be considered. Finally other aspects such as the technical difficulty of series connection, modularity, reliability, maintenance ease and fault behaviour could also be evaluated and different KPIs could be proposed to consider these aspects.

7 Conclusions and perspectives

MVDC networks will be key for the development of the future electrical grid. Power converters are the key enabling technology that will allow to connect the existing AC grid with the MVDC network to support the integration of large shares of renewable energy sources and electric vehicles. Among the available technologies of AC-DC converters in the industry, two interesting topologies were studied and evaluated in this work, namely the Modular Multilevel Converter and the Neutral Point Clamped Converter. The goal was to compare these technologies to find which one of them is more suited for MVDC applications.

As a first step for the comparison, a methodology for the design and evaluation of AC-DC converters was proposed. This methodology included a review of the applicable requirements, stated by the grid code, the TSOs and DSOs. Among the requirements of interest one can find the harmonic content, the low voltage ride-through and the maximum power that is allowed to be transmitted. It was found that different requirements apply for producers and for consumers, and for different voltage levels (MV, HV).

The design of the topologies was done following principles and methods proposed in the literature, and in some cases, system analysis was used to determine some parameters, like for instance the AC filter for the NPC. The

Key Performance Indicators used to do the comparison were selected from the ones found in the literature. Analytical expressions were used for all the design parameters and most of the KPIs calculation, except for the switching losses, that were found using the simulation models.

A more detailed methodology of calculation for each topology was established, in which the steps for the obtention of every design parameter and KPI is clearly shown. The operating points were selected following a recommendation for DC distribution levels given by the CIGRE, and an extra point was added for being of interest, namely the ±50 kV level. For this work, it has been assumed that no transformer is needed for voltage transformation, and hence no transformer is considered as part of the overall system. Two relevant DC current levels were chosen for a total of twelve cases. For the degrees of freedom, a voltage ripple of 10% and a switch of 3.3 kV were used. The switches were considered to be the same for both topologies and in all different cases. A sensitivity analysis was done with another degree of freedom, the switching frequency for the NPC, and it was found that one of the designs did not comply with the requirements, leaving the switching frequency of 1250 Hz as the chosen one. It could be interesting to do a sensitivity analysis also on the switch rating used, particularly for the lower voltage levels.

In order to accomplish the goals mentioned in section 1.3, another objective was identified, the need to add the NPC topology to the existing tool developed for the MMC. The tool is based on OOP and implemented in MATLAB to allow for easy coupling with the simulation models and it is designed to be modular. This tool allowed to do assessment of several operating conditions to compare both topologies, which is the main goal of the thesis. The results are displayed as a function of the voltage level, which would allow to identify any crossing point if there is any.

A transient simulation was done to check the compliance of the designs with the THD requirements. It was found that the MMC has a much better performance than the NPC in terms of harmonic content and losses, being below 2% for all the cases but the lowest voltage one. On the other hand, the NPC which was evaluated for two different switching frequencies was found to meet the THD requirement only with the switching frequency of 1250 Hz, given the retained inductive filter. Furthermore, it was found that the components corresponding to the switching frequency are very high for the NPC, getting worse as the voltage increases. This means that the designed filter is not enough for the filtering needs of the system, and a more sophisticated one is needed.

From the results it was found the NPC is a better topology in terms of semiconductor devices, as it requires overall less semiconductor devices to be installed, reducing the investment cost compared to the MMC. Additionally, to have a better semiconductor utilization factor, it would be better to work at the higher DC current. As regards the passive elements of the converters, that relate to the weight and size, it is not clear which topology is better. The MMC has better magnetic factor indicators than the NPC. As regards the capacitive energy factor, it is not possible to reach a conclusion about which topology is better, since the results would change depending on the assumption made for the energy-to-power ratio design parameter for the NPC. Furthermore, if a different filter was to be designed for the NPC, all of these results could change, and also if taking into account the passive elements on the snubbers required for the series connection of semiconductors in the NPC.

Concerning the semiconductor losses, it is clear that the MMC has a superior performance than the NPC in this aspect. The difference lies namely in the switching losses which are much greater for the NPC, given the high switching frequency. A smaller frequency could be used to reduce the losses, but the THD requirements should be considered to make a new filter design. The MMC would still probably have a better performance since the bigger number of SMs allows for a slower commutation of each switch. The conduction losses were calculated analytically using the tool and the switching losses were estimated taking data form the simulation models.

As it can be seen, the main objectives of this master thesis were accomplished. The main contributions of this work are the proposal of a general methodology for the design and assessment of AC-DC converters, the comparison of the MMC and NPC in terms of sizing and losses over a wide range of voltage and power and the implementation of the NPC converter in an existing tool developed in the SuperGrid Institute to design and evaluate converters in a rapid way, which can be reused later in the company. The results of this master thesis

can be used by the scientific and technical community, and the writing of a scientific article is in progress based on the results here presented and some further works.

As part of the future work to be done in the topic, different perspectives can be identified. Firstly, a sensitivity analysis could be performed for some of the degrees of freedom. The switch rating used for the design, for example. Also, a different type of KPI could be considered, in order to consider the technical difficulties of the installation of switches connected in series for the NPC into the analysis. Another thing that could be changed in the converter design stage would be to consider the grid requirements actively in the design, namely, the AC filter of the NPC converter. Better criteria are also needed to determine an energy-to-power ratio on the NPC that would allow to make a comparison of the topologies in terms of installed energy. The consideration of the passive elements losses could also be included in the analysis. The behaviour of the converters in case of faults was identified as an important topic to add to the comparison, yet it hasn't been explored in the literature as a KPI. Finally, a further analysis could be done to consider the economic aspects in the assessment of the converters and given that the NPC has a lower initial investment but higher operating costs, it would be possible to find a crossover point in time.

8 Appendix

8.1 Implementation example: Leg class

In this section, the implementation of the *Leg* class is shown as an example of the implementation of the entire tool as explained in the previous sections. Figure 36 shows the name of the class and the properties. As it can be seen, the Leg is composed of the four IGBT modules and two clamping diodes for a total of six valves. Note that these properties are in fact other objects. On the bottom part, the values of AC and DC currents and the modulation index are shown. These are the steady state values of the voltages and currents, calculated in the class *NPC*.

```
classdef Leg
    properties
        valve1
        valve2
        valve3
        valve4
        ClampingDiode1
        ClampingDiode2
        Vdc
        Idc
        Vac
        Iac
        Mac
    end
```

Figure 36 Leg class properties

Figure 37 shows the constructor of the *Leg* class. As it can be seen, the object needs some inputs, received from the *NPC* class to be created. Some of these values are also the properties of the class, so they are assigned correspondingly.

```
    methods
        function obj = Leg(Vdc,Idc,Vac,Iac,VSWAverage,Switch)
            % VSWAverage: Average switch voltage [V]
            % FreqOp: Operating frequency [Hz]
            % Switch: IGBT used
            obj.Vdc = Vdc; % Vdc: DC voltage pole to pole [V]
            obj.Idc = Idc; % Idc: DC current [A]
            obj.Iac = Iac; % Iac: Leg AC current in RMS [A] in phasor form a+jb
            obj.Vac = Vac; % Vac: Leg AC voltage in RMS [V] in phasor form a+jb per phase
            obj.Mac = obj.Vac/(Vdc/2); % Converter modulation index
```

Figure 37 Leg constructor 1/2

Figure 38 shows the instantiation of the six valves inside the constructor of the *Leg* class. As it can be seen, the *Leg* class sends the inputs to the different valves, based on calculations done in the constructor. It is observed for example, how the clamping diodes have a different power module than the four switches in the leg. Or how each valve receives a different alpha, representing the duty cycle of each one.

```
            % Instanciation of the valves
            % Ileg and alpha# are vectors, will be used to calculate the
            % RMS currents
            obj.valve1 = valve(Vac,Vdc,Ileg,Idc,alpha1,tm,VSWAverage(1),Switch{1});
            obj.valve2 = valve(Vac,Vdc,Ileg,Idc,alpha2,tm,VSWAverage(1),Switch{1});
            obj.valve3 = valve(Vac,Vdc,Ileg,Idc,alpha3,tm,VSWAverage(1),Switch{1});
            obj.valve4 = valve(Vac,Vdc,Ileg,Idc,alpha4,tm,VSWAverage(1),Switch{1});
            obj.ClampingDiode1 = valve(Vac,Vdc,Ileg,Idc,alpha_cd1,tm,VSWAverage(2),Switch{2});
            obj.ClampingDiode2 = valve(Vac,Vdc,Ileg,Idc,alpha_cd2,tm,VSWAverage(2),Switch{2});
```

Figure 38 Leg constructor 2/2

Finally, Figure 39 shows the different methods implemented in the *Leg* class. The sequential calling of classes can be seen with the method *NumberSwitches*, which adds all the switches in the four valves of the Leg.

```
98      function Nsw = NumberSwitches(obj)
99          Nsw = obj.valve1.NSWs+obj.valve2.NSWs+obj.valve3.NSWs+obj.valve4.NSWs;
100     end
101     function Ncd = NumberClampingDiodes(obj) ...
104     function W = InstalledPower(obj) ...
109     function WRMS = InstalledPowerRMS(obj,SS) ...
122     function CondLosses = CondLosses(obj,NameOperatingPoint,SS) ...
126     function SwLosses = SwLosses(obj,f,NameOperatingPoint,SS) ...
```

Figure 39 Leg class methods

8.2 MMC design parameters and KPIs

8.2.1 Number of switches and submodules

Figure 40 shows the number of SMs and switches for the MMC as a function of the DC voltage. As it is expected, the number of SMs increases with the DC voltage as determined by equation **(3.1)**. For now, only half-bridge SMs have been considered. Therefore, the total number of switches (IGBT module + antiparallel diode) in the MMC is twice as much the number of SMs.

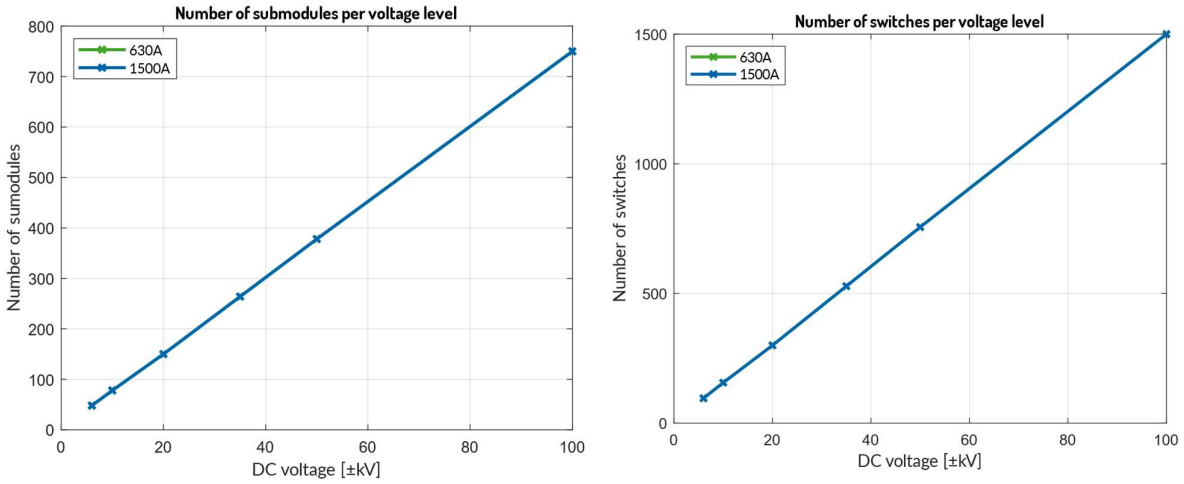

Figure 40 Number of submodules and number of switches according to the DC voltage level for the MMC

8.2.2 Arm inductance

The arm inductance for the MMC is set at 15% of the base impedance value. As it can be seen in Figure 41, the value of the arm inductance increases as the DC voltage increases. It can also be seen that there is a different slope for the last value, slightly higher than for the rest of the graph. In fact, this is because as the DC voltage increases, so does the AC voltage. Furthermore, they increase in the same proportion as shown in Table 9, except for the last point, in which the AC voltage is higher than the DC voltage.

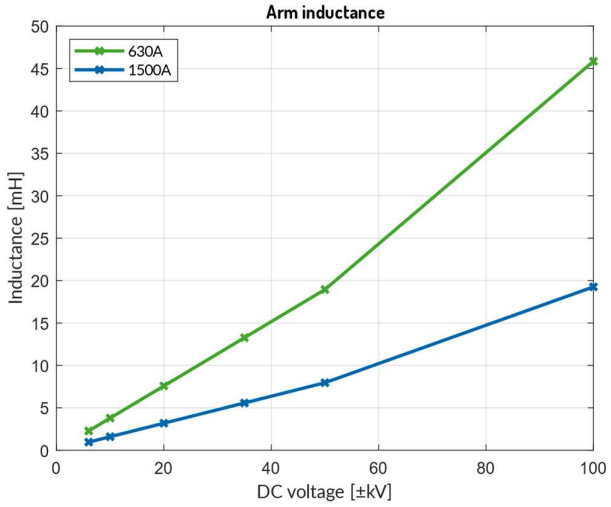

Figure 41 Arm inductance according to the DC voltage level for the MMC

Taking a closer look at equation **(8.1)** and considering that $P=V_{dc}I_{dc}$ it can be seen that the inductance value increases because the AC voltage increases and that the different slope is due precisely to the fact that for the last point the proportion for both voltages is different.

$$Z_C = \frac{V_{ac}}{\sqrt{3}\left|\frac{P - jQ}{\sqrt{3}\,V_{ac}}\right|} \qquad \textbf{(8.1)}$$

It can also be seen that the inductance value is smaller with a higher DC current. This is because increasing the DC current will make the base impedance to decrease, and thus the arm inductance also decreases.

8.2.3 Submodule capacitor and equivalent arm capacitor

As mentioned in section 3.1.3, the capacitors of the SMs are often considered as an equivalent capacitor for the entire arm. Figure 42 shows both the equivalent arm capacitor and the SM capacitor. As it can be seen, the equivalent arm capacitor tends to be smaller as the DC voltage increases, this is because the arm's capacitor is inversely proportional to the arm's voltage, which is around the same as the DC voltage. It can also be seen that for a higher DC current, the capacitance value increases. This is due to the fact that as the DC current increases, so does the power and thus the energy swing, as shown in equation **(3.4)**.

The SM capacitor on the other hand, is calculated from the arm's capacitor with the following relation:

$$C_{SM} = N_{SM} C_{eq,arm} \qquad \textbf{(8.2)}$$

Similarly to the arm inductance's case, the last point has a significant slope. This is because the relation between the AC and the DC voltages changes for this last point. Namely, the modulation index k in equation **(3.4)** is now bigger, causing the energy swing to be smaller and therefore the SM capacitance to be smaller.

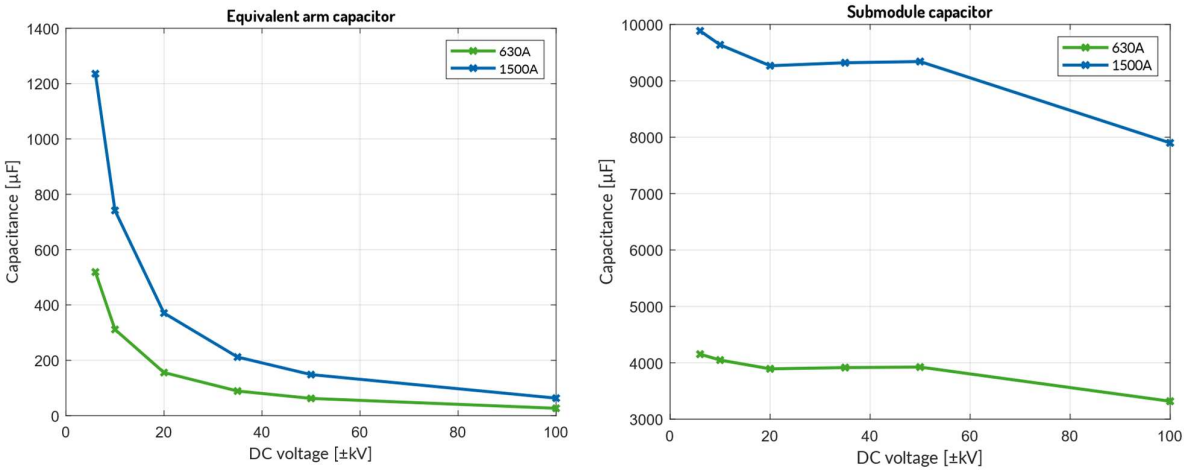

Figure 42 Equivalent arm capacitor and submodule capacitor for the MMC

8.2.4 VA semiconductor rating

Figure 43 shows the VA rating of the semiconductor devices, on the left side using the nominal values of the devices and on the right side, the semiconductor rating that an ideal adapted switch would need to withstand the RMS currents flowing through it, as explained in section 4.9.2.

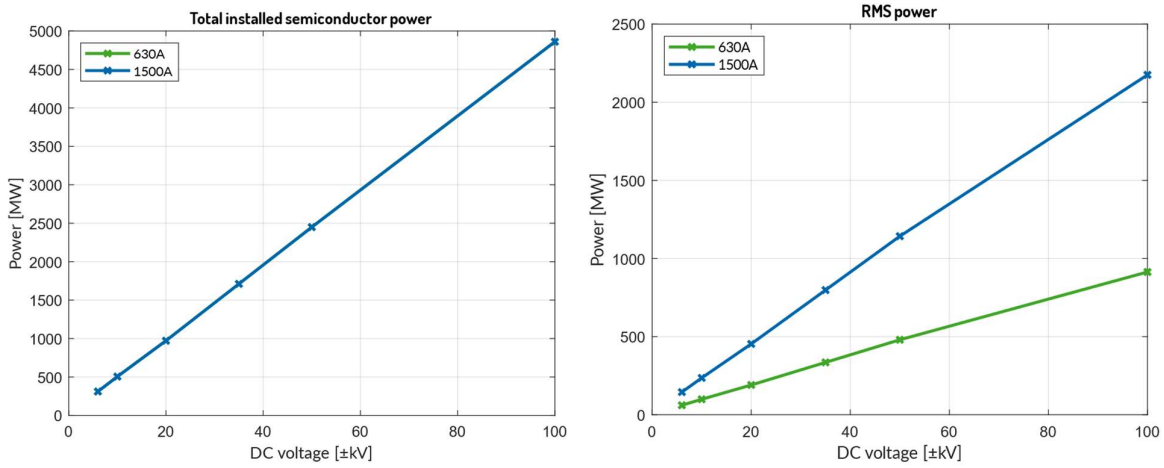

Figure 43 Total installed semiconductor power and power based on RMS currents for the MMC

As it can be seen, the total installed semiconductor power doesn't change if the DC current of the grid changes because it depends solely on the nominal values of the switch. It increases with the DC voltage because the number of SMs (therefore switches) increases as well. From the economic point of view, there would not be a difference between both current levels, because the investment for the semiconductor devices would be the same regardless.

$$P_{installed} = N_{sw} V_{operating} I_{dc.switch} \quad \textbf{(8.3)}$$

On the other hand, the RMS power changes depending on the value of the DC current. It is smaller for the smaller DC current value. This is because the power is smaller for this case, and therefore the AC current from which the RMS currents flowing through the switches depend, are also smaller.

$$P_{RMS} = N_{sw} V_{operating} I_{RMS} \quad \textbf{(8.4)}$$

8.2.5 Utilization factor based on total installed semiconductor power and on the RMS current-based power

Following the same analysis of the installed semiconductor power using a real switch and a switch adapted to the RMS current needs, Figure 44 shows the two different utilization factors that would be obtained for each of these cases. As it can be seen, for the first case, the utilization factor when working with the higher DC current is better. This makes sense because the switch has a nominal DC current, and the closer the DC grid current to this nominal value, the better utilized will be the switch, as the power will be closer to the transmitted power. Moreover, the utilization factor for this case would be almost constant for the entire voltage range.

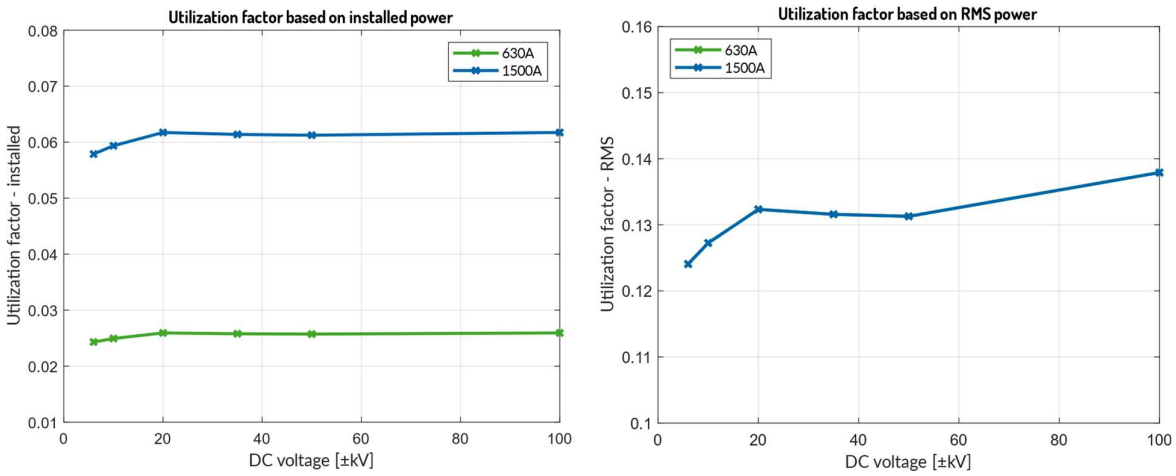

Figure 44 Utilization factor based on total installed semiconductor power and on RMS current-based power for the MMC

For the second case, the utilization factor doesn't depend on the DC current, as the switch would be considered to be adapted to the required power computed with the RMS currents. For this case, the utilization factor is the highest for the last point.

8.2.6 Installed energy and energy factor

Figure 45 shows the installed energy and the energy factor for the MMC. As mentioned previously, the installed energy is the energy that can be stored in the SM capacitors. It is also possible to see it as the energy stored in the equivalent arm capacitor, as shown in equation **(8.5)**. As it can be seen, the installed energy increases with the DC voltage and the last point has a different slope because the ratio between the AC and the DC voltage for this point is different. It can also be observed that the installed energy is smaller for a smaller DC current, this is because at a smaller DC current, the equivalent arm capacitor decreases.

$$W_{installed,arm} = N_{SM,arm}\frac{1}{2}C_{arm}V_{arm}^2 \qquad \textbf{(8.5)}$$

From Figure 45 the energy factor is around 0.03, which besides giving a hint on the size of the capacitors and the SMs, it can also be interpreted as the inertia of the system.

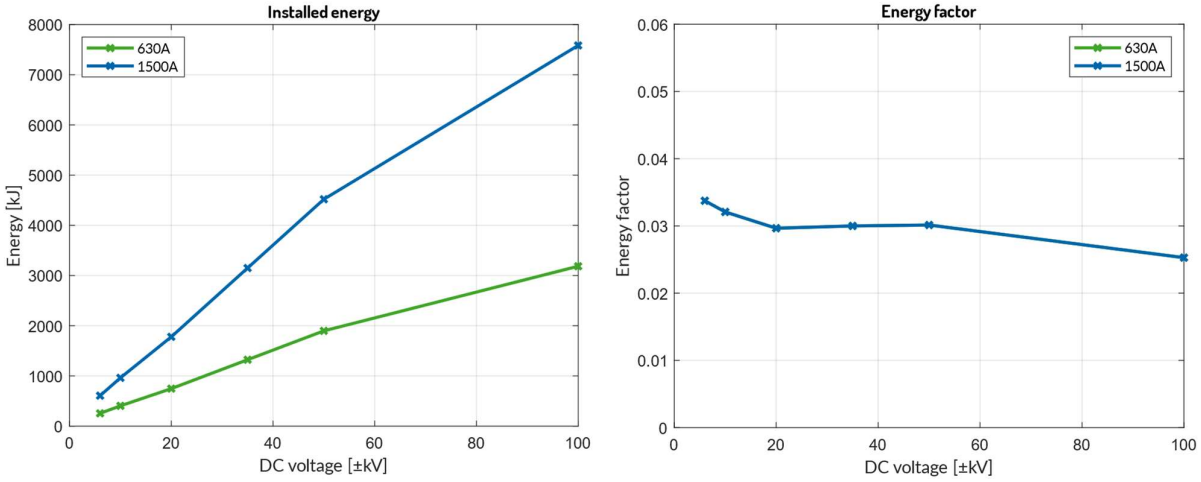

Figure 45 Installed energy and energy factor for the MMC

8.2.7 Magnetic factors

Figure 46 shows the magnetic factors for the inductors with an air core (in this case the arm inductance is assumed to have an air core) and with a ferromagnetic core (e.g., a transformer, if one is considered). As it can be seen, these factors are constant no matter what the level of voltage is. This is because they are both ratios of the total transmitted power. For the first case, the arm inductance, which is a percentage of the base impedance, depends on the AC current and voltage. The AC current itself depends on the transmitted power and the AC voltage. At the end, the apparent power of the arm inductance depends only on the transmitted power, so the relation between the apparent power and the transmitted power is a constant value.

$$S_{iductances.air} = |X_{arm} I_{ac}^2| \quad \textbf{(8.6)}$$

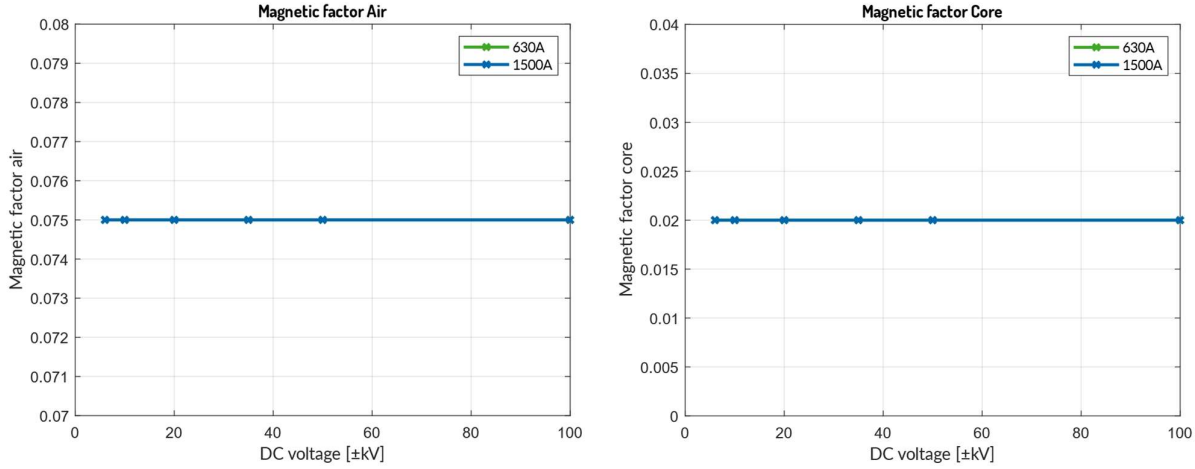

Figure 46 Magnetic factors for inductors with an air and a ferromagnetic core for the MMC

In the case of the inductances with a ferromagnetic core, like for instance a transformer if it was considered in the system, the apparent power would depend entirely on the transmitted power (active and reactive), so also in this case, the factor has a constant value along the voltage range.

$$S_{inductances,core} = |P + \boldsymbol{j}Q| \quad \textbf{(8.7)}$$

8.2.8 Conduction losses and losses factor

The conduction losses have been estimated using equations **(2.2)** and **(2.3)** and the curves presented in Figure 7. In this case no linear approximation was done. A look-up table was built from the curves and the points that are not to be found in the table were estimated using linear interpolation.

The conduction losses in a switch depend on the current flowing through the switch. If in a first case it is considered that no reactive power is being transmitted, the AC current would depend on the DC current and voltage and on the AC voltage, as shown in equation **(8.8)**. If only one switch was considered, the conduction losses for the single switch would be the same for every voltage level, except for the last point, where the relation V_{dc}/V_{ac} is different. This can be seen as usual by the different slope in the last point. It can also be observed that for a bigger DC current, the losses will also be bigger. Furthermore, as the number of switches increase so do the conduction losses.

$$I_{ac} = \frac{P}{\sqrt{3}V_{ac}} = \frac{I_{dc}V_{dc}}{\sqrt{3}V_{ac}} \tag{8.8}$$

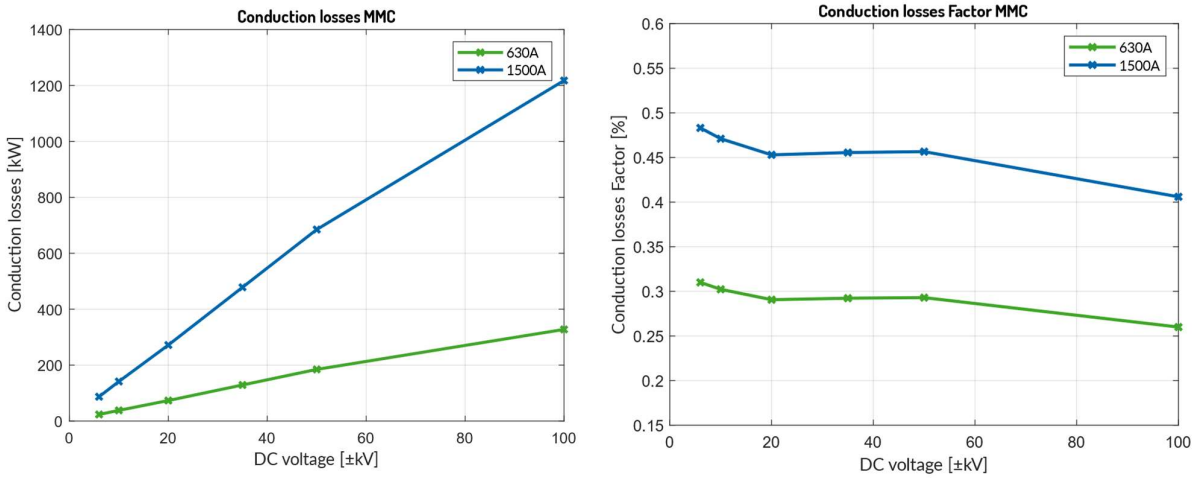

Figure 47 Conduction losses and conduction losses factor for the MMC

Following the same logic for the conduction losses factor, it should be noted that in fact, when considering one switch only, the power losses factor should be the same for all voltage levels except for the last point. However, due to probably numerical error the value differ slightly between voltage levels for a switch and the error gets magnified when multiplying by the number of SMs. It can also be noted that there will be less conduction losses for the lowest DC current level. This is because the power transmitted is smaller and the AC current will also be smaller, resulting in a reduction in the switch current and thus in the conduction losses of the switch.

8.2.9 Switching losses and losses factor

For the switching losses a switching frequency of 175 Hz has been used. This value was chosen for being more than three times the fundamental frequency, not a multiple of it and yet not too big to avoid high losses. In a first stage the switch current and the control signals were taken from the previously existent simulation model. The losses were estimated taking the data of one switch and multiplying its losses by the total number of switches. A test taking the data of four different switches was done and it was found that the difference between switches gives an acceptable error (around 3-4%). Thus, the data of a single switch was taken, and it is considered to behave as the average of all the switches.

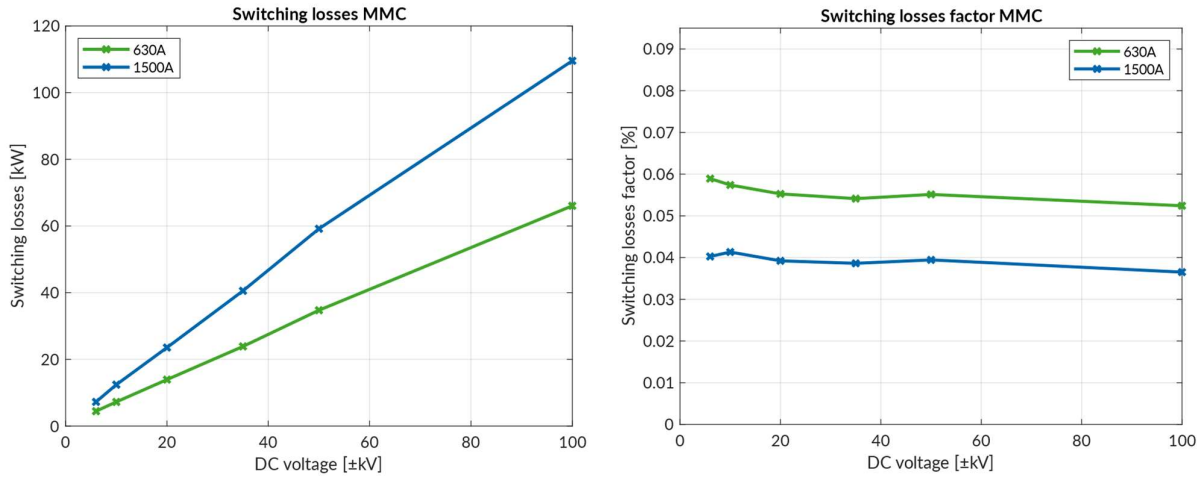

Figure 48 Switching losses and switching losses factor for the MMC

Like the conduction losses, the switching losses are calculated using the current flowing through the switches, so they depend ultimately on the AC current. Equation **(2.5)** is used along with the curves presented in Figure 8 and as in the previous case a look-up table was built to estimate the turn-on and turn-off energies.

It is worth noting that the switching losses presented in Figure 48 have a similar behaviour as the conduction losses, but they are considerably smaller. This result is expected, as small switching losses is one of the features and advantages of the MMC.

8.3 NPC design parameters and KPIs

8.3.1 Number of switches

As expected, the number of switches (IGBT modules + antiparallel diode) and clamping diodes increases with the DC voltage level, and it depends solely on the DC voltage, which is why the number of switches and clamping diodes is the same for both DC current values.

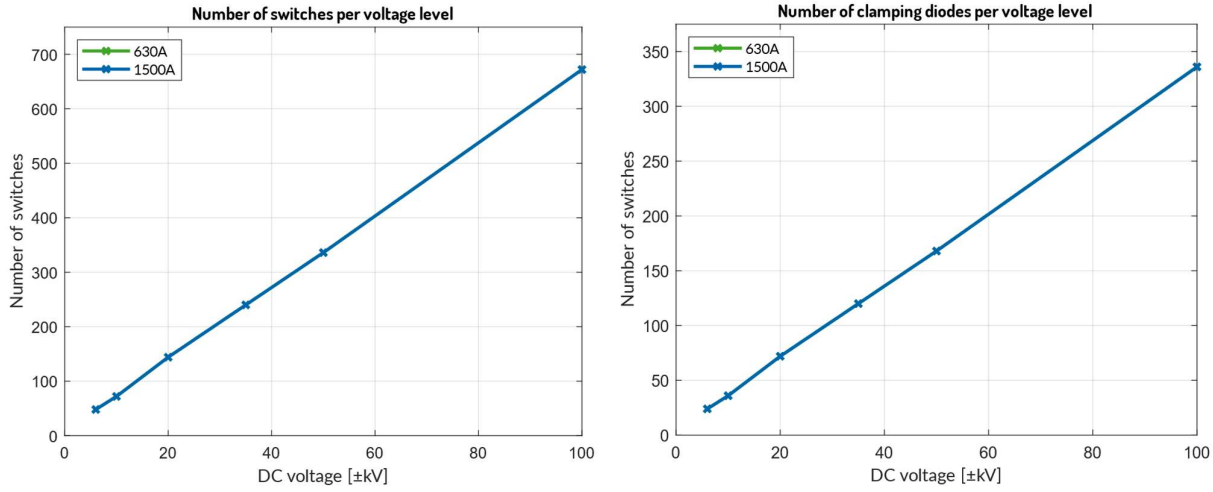

Figure 49 Number of switches vs. DC voltage level for the NPC

8.3.2 Filter inductance

It is rather difficult to understand how the filter inductance changes with a single parameter from equation **(3.15)**. However, if it is considered that the transmitted reactive power is a percentage of the active power according to the grid requirements presented for instance in Figure 2, it can be seen that as the DC voltage (and thus the AC) voltage increases, so does the value of Xp shown in equation **(3.15)**. If the reactive power was assumed to be zero, for instance, the inductance value is inversely proportional to the transmitted power and thus to the DC current. Therefore, the higher the DC current, the smaller the filter inductance, as shown in Figure 50.

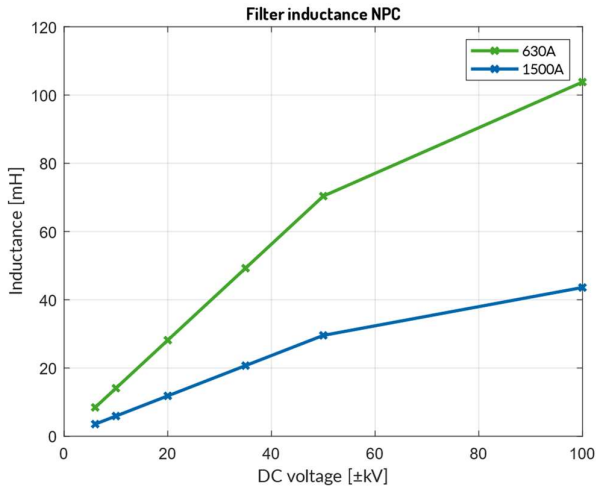

Figure 50 Filter inductance value according to the DC voltage level for the NPC

8.3.3 Equivalent DC link capacitor

Figure 51 presents the equivalent DC link capacitor for the NPC. Looking at equation **(3.9)**, it can be seen that the capacitance value is inversely proportional to the DC voltage, therefore the decreasing trend of the capacitor. It can also be seen that the higher the DC current, the higher the power and hence the capacitance value needed for 1500 A is higher than that needed for 630 A.

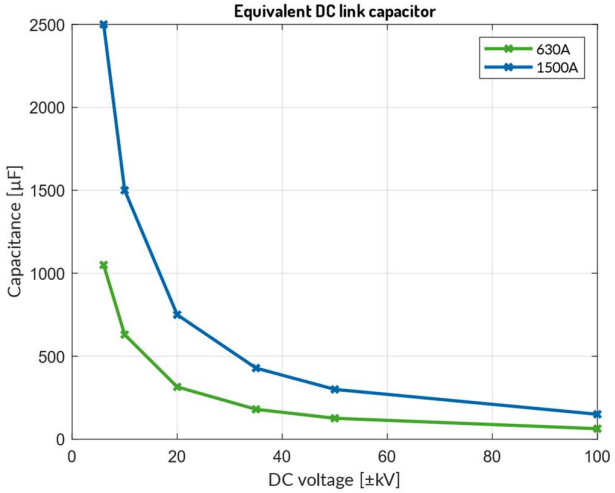

Figure 51 Equivalent DC link capacitor according to the DC voltage level for the NPC

For this parameter it is important to notice that the energy to power ratio was assumed to be 10 kJ/MVA.

8.3.4 Total installed semiconductor power and power based on RMS currents

Figure 52 shows the semiconductor power based on the installed switch and on the RMS currents. The same comments made for the MMC apply for the NPC. The total installed semiconductor power does not change with the DC current because it depends on the parameters of the switch, and the same switch is considered for both cases. It could be interesting to make an analysis with different switches for both current levels in the future.

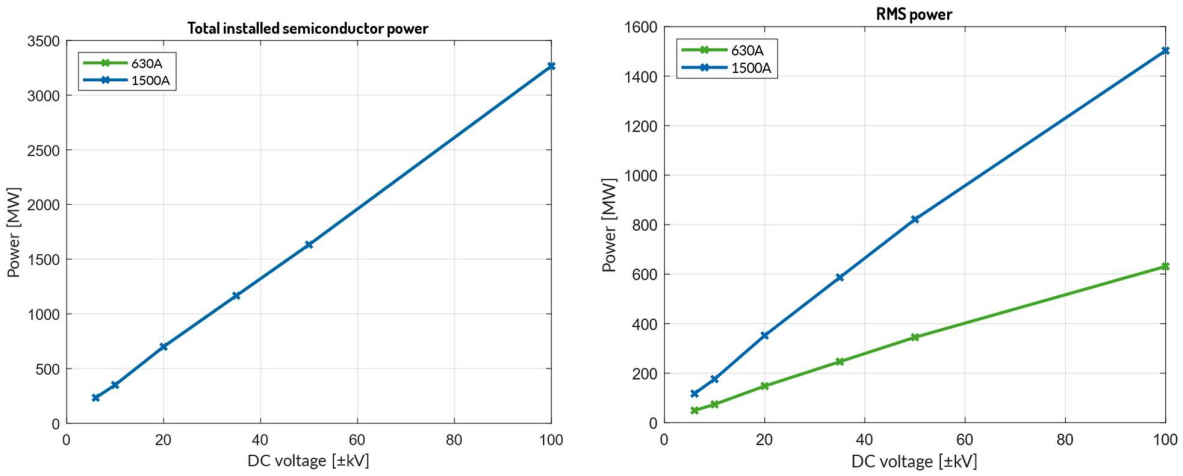

Figure 52 Total installed semiconductor power and power based on RMS currents for the NPC

The RMS power shows the real behaviour of the switches and allows to see that for higher DC currents, the RMS power of the switch is also higher.

8.3.5 Utilization factor based on total installed semiconductor power and on RMS current-based power

Figure 53 shows that the real installed utilization factor of a switch would be higher if the DC current is higher and closer to the switch rated current, as it is expected. This is a similar result to that obtained for the MMC. The utilization factor for the RMS currents-based power would be the same regardless of the DC current and has an increasing trend as the DC voltage increases.

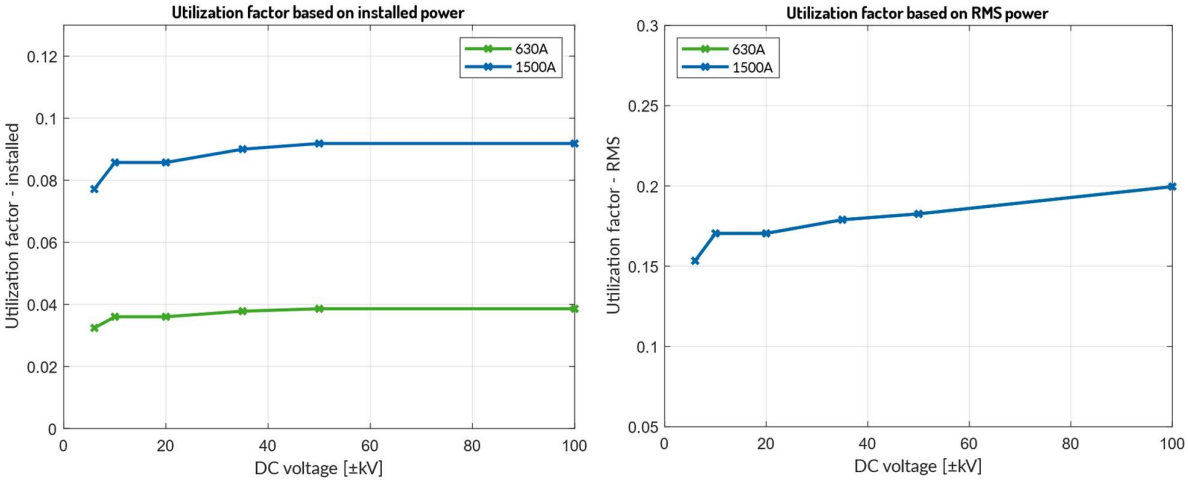

Figure 53 Utilization factor based on total installed semiconductor power and on RMS current-based power for the NPC

8.3.6 Installed energy and energy factor

In the case of the NPC, the installed energy is the one that would be stored in the DC link capacitors. As it can be observed, for the higher DC current, the installed energy is also higher since the capacitor value is higher. The energy factor on the other hand, is a constant value, and it is in fact the value taken for the hypothesis of the energy to power ratio in the calculation of the DC link capacitor. Had a different hypothesis been taken, the energy factor would change correspondingly. It can also be seen that the energy factor doesn't change with the DC current.

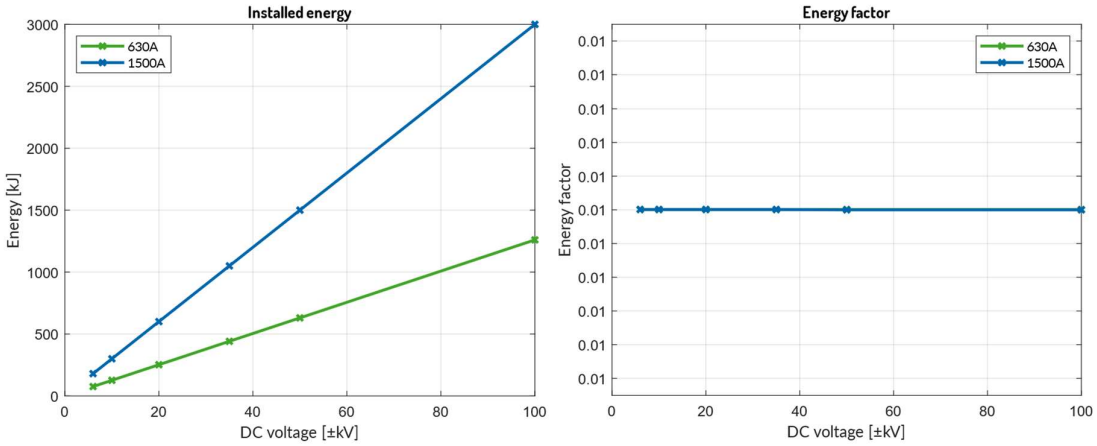

Figure 54 Installed energy and energy factor for the NPC

8.3.7 Magnetic factors

Figure 55 shows the magnetic factors for the NPC considering the AC filter as a reactor with an air core. The graph on the right represents the magnetic factor of an inductance with ferromagnetic core, in this case it shows the inductance of a transformer, although one is not originally considered in the system. For the case of the transformer, the magnetic factor would be exactly the same, it is the same situation as for the MMC. For the AC reactor however, it can be seen that the last point is different from the other ones. This is because, in this case, the reactor's value depends not only on the transmitted power but also on the AC and DC voltages, which as it has been many times explained, have a different ratio for the last point.

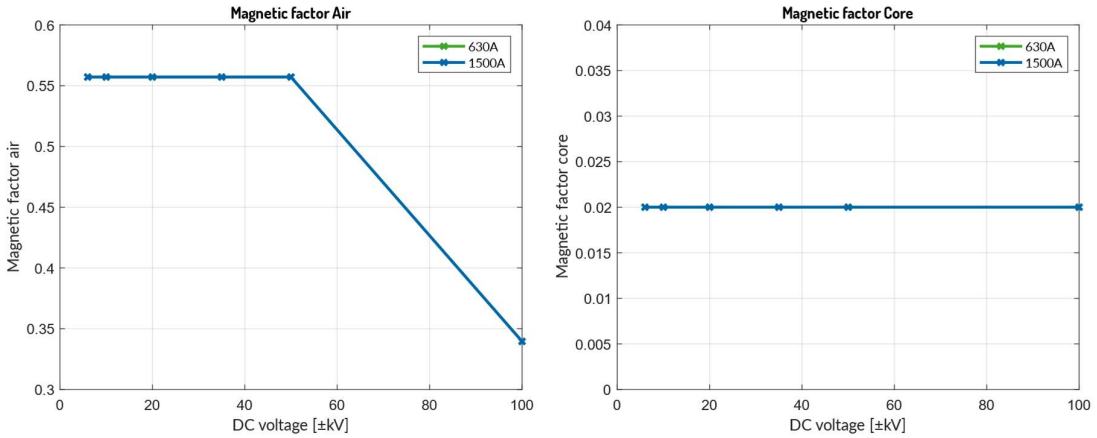

Figure 55 Magnetic factors for inductors with an air and a ferromagnetic core for the NPC

These analyses are only valid with the hypothesis that the AC reactor has an air core and not a ferromagnetic one. The conclusions could clearly change given a different hypothesis.

8.3.8 Conduction losses and losses factor

The methodology followed to find the conduction losses for the NPC is the same as the one used for the MMC, the switch currents were taken from the simulation model (already existent) and then the curves presented in Figure 7 were used with a look-up table to estimate the losses in the switches. Similarly, as for the MMC, if only one switch was considered, the conduction losses and power losses factor of the single switch should be the same, but due to numerical error and the magnification of the error once multiplied by the number of switches, it does not look constant for the total of the switches. Once again it can be seen that as the voltage increases so do the conduction losses due to the higher number of switches. The conduction losses factor has its lower value in the last point, due to the different ratio between V_{AC} and V_{dc}.

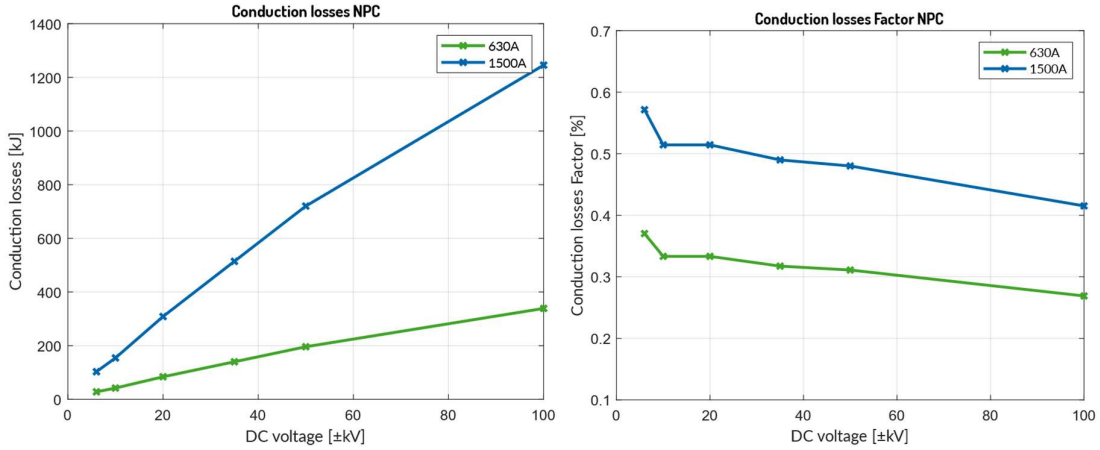

Figure 56 Conduction losses and conduction losses factor for the NPC

8.3.9 Switching losses and losses factor

In order to estimate the switching losses for the NPC, the simulation model was used and the currents of the four switches and two clamping diodes of a single phase were extracted. Then, using the same methodology as for the MMC, the turn-on and turn-off losses of Figure 8 were estimated using a look-up table. This process was done twice, with two different switching frequencies, 1250 Hz and 650 Hz as shown in Figure 57 and Figure 58. These two switching frequencies were chosen, the first one for have been used in several HVDC projects with the 3L-NPC or a variation of the NPC [18], and the second one for being the standard used by GE for industrial drives.

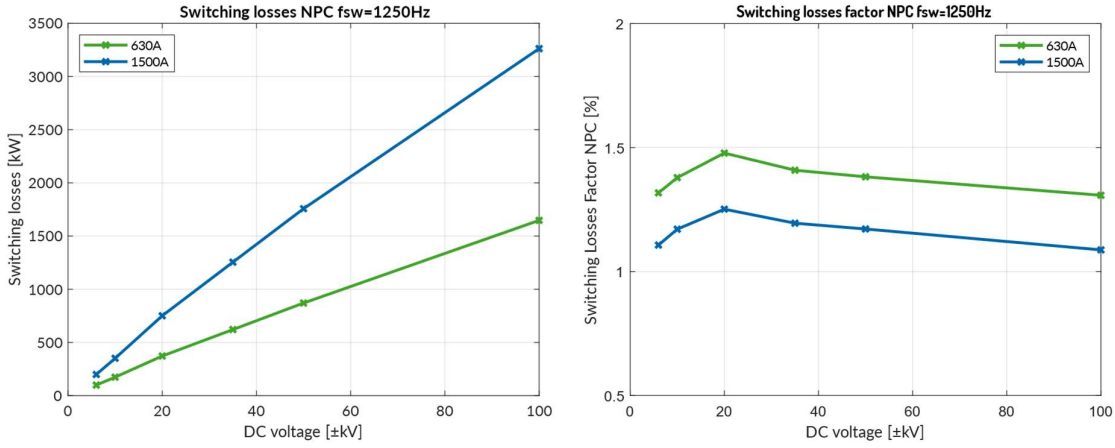

Figure 57 Switching losses and switching losses factor for the NPC at 1250 Hz

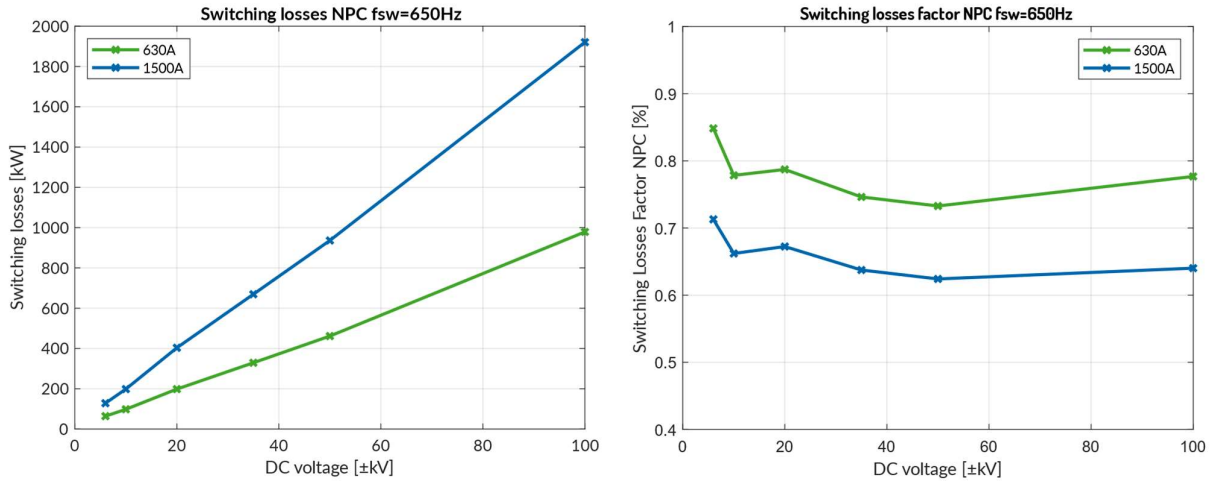

Figure 58 Switching losses and switching losses factor for the NPC at 650 Hz

As it was expected, the switching losses are much greater with the biggest switching frequency, this comes from the fact that the switching losses increase linearly with the switching frequency.

8.4 Comparison MMC vs. NPC

8.4.1 Number of switches

Figure 59 shows the number of switches needed in each voltage level for both topologies. As it was expected, the NPC requires a smaller number of switches than the MMC, around 50% if only HBSMs are considered for the MMC. The DC current has no effect in the number of switches. If the MMC had only FBSMs or some stacks of HBSMs and some other stacks of FBSMs, the number of switches needed for the MMC would be even higher. Therefore, in this first KPI, the NPC seems more advantageous.

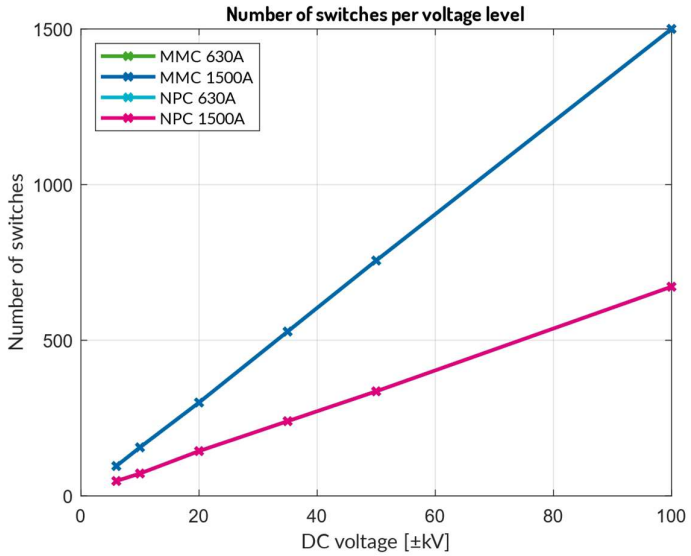

Figure 59 Number of switches for each topology according to the DC voltage level

It should be however considered that the NPC also requires clamping diodes, which will be added to the total number of semiconductor devices needed for the converter.

8.4.2 Total installed semiconductor power and utilization factor

Figure 60 shows the total installed semiconductor power considering a real switch and the corresponding utilization factor for both topologies. As it is expected, the MMC has a higher installed power because it has more switches. Focusing now on the utilization factor, it is interesting to see that the NPC has a higher utilization factor than the MMC for the same DC current. However, the utilization factor of the MMC with DC current 1500 A is still better than that of the NPC with DC current 630 A, suggesting that it is better to work at higher currents to take better advantage of the installed power. The NPC would show a better performance than the MMC for this KPI.

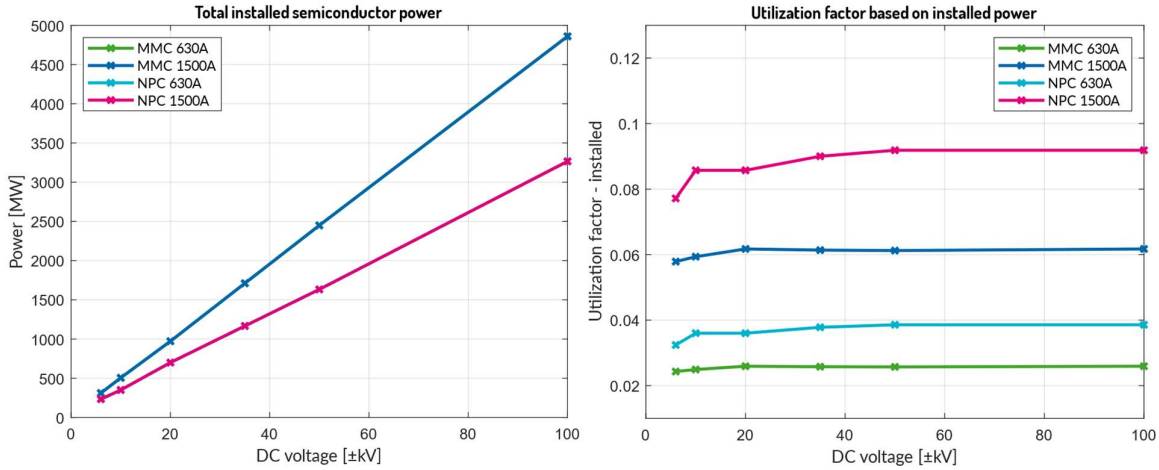

Figure 60 Total installed semiconductor power and utilization factor for each topology

8.4.3 Magnetic factors

In the case of the magnetic factors, it can be seen that if a transformer with a ferromagnetic core was considered to be part of the system, the magnetic factor for inductances with ferromagnetic core would be the same for all the voltage levels. This is because the power considered would be the power transmitted, which is the same for both topologies.

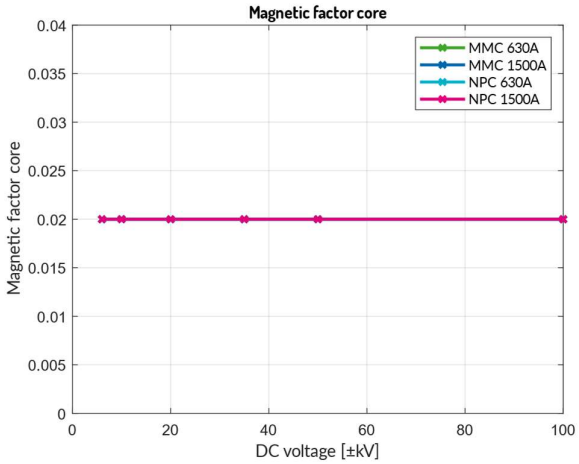

Figure 61 Magnetic factors for both topologies

For these factors it should be noted that the hypothesis made about the core of the inductances will have a direct effect on the behaviour of the factors, so the results here discussed are only valid when assuming that

the phase inductances (arm inductors for the MMC and AC filters for the NPC) have an air core. If these inductances were considered to have a ferromagnetic core, the results might change.

8.4.4 Conduction losses and losses factor

The conduction losses and conduction losses factor are shown in Figure 62. It can be seen that the conduction losses are slightly higher for the NPC converter than for the MMC for each DC current, so the power losses factor is also greater for the NPC. There are also higher power losses with the higher DC current so it would seem preferable to work at lower DC currents in order to have lower conduction losses, but this could mean a worse value for other KPIs, which is why it is important to weight which factors are more important, or which operation point is preferred.

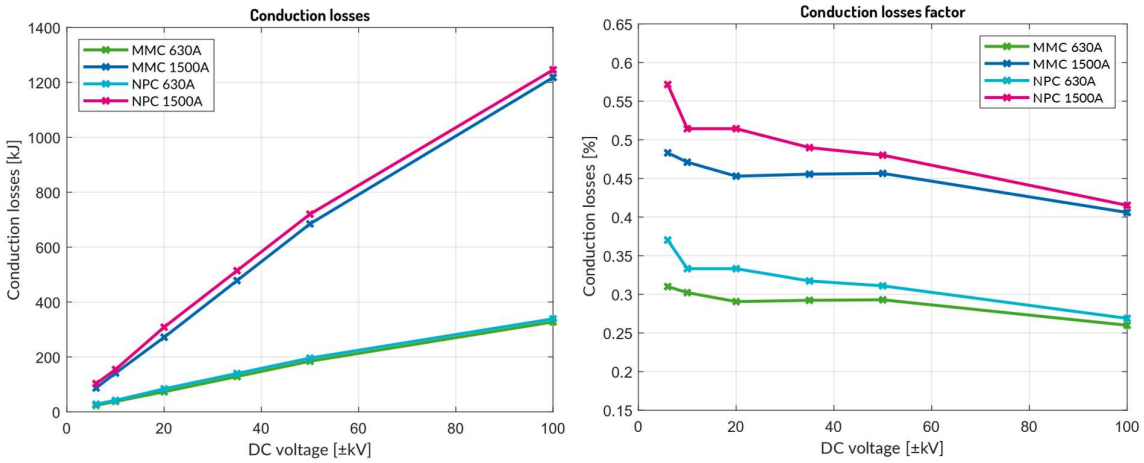

Figure 62 Conduction losses and conduction losses factor for both topologies

8.4.5 Switching losses and losses factor

As mentioned before, the switching frequency used for the MMC was 175 Hz while for the NPC two different switching frequencies (1250 Hz and 650 Hz) were used and the comparison is shown for both cases in Figure 63 and Figure 64. It is clear from the figures that in any case the NPC has switching losses significantly higher than the MMC. The reduction of the switching frequency naturally reduces the switching losses for the NPC, but they are still considerably higher than the MMC's switching losses. This is not a surprising result, since one of the advantages of the MMC over the NPC is precisely a better performance in terms of switching losses.

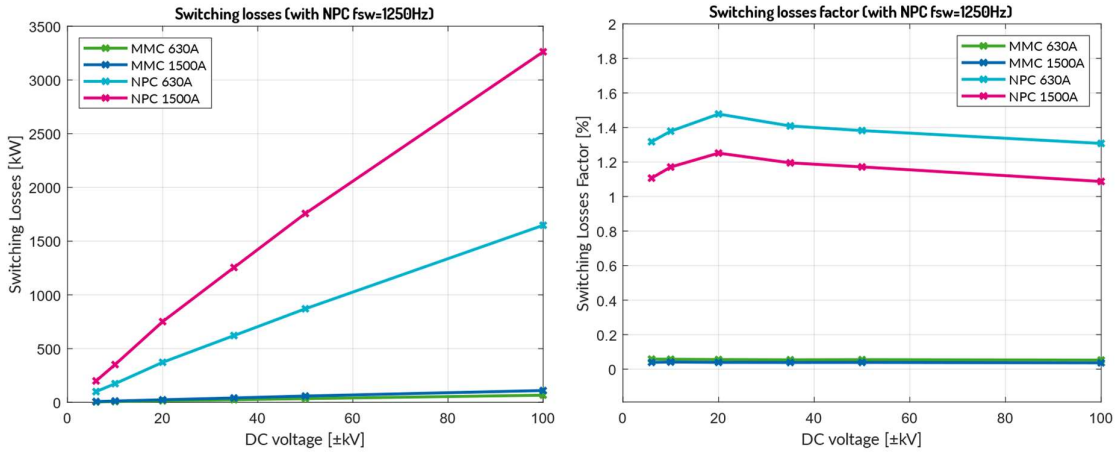

Figure 63 Switching losses and switching losses factor for both topologies with a fsw=1250 Hz for the NPC

It is evident from the graphs that the MMC is better for this KPI, and checking the semiconductor losses as a whole, i.e., conduction losses plus switching losses, the MMC has a much better performance than the NPC.

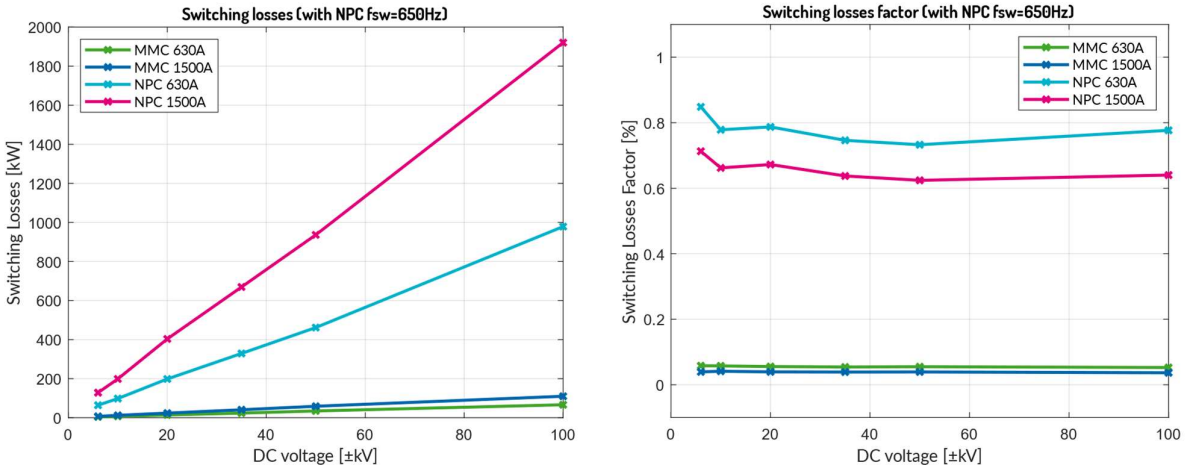

Figure 64 Switching losses and switching losses factor for both topologies with a fsw=650 Hz for the NPC

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