Sequential Phase-Shifted PWM for Cascaded-H-Bridge Multilevel Converters

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***Abstract*—The Cascaded-H-Bridge (CHB) converter has been demonstrating over the last years to be an adequate multilevel topology for high voltage and high power applications. In this regard, it is possible to exploit the Phase-Shifted Pulse Width Modulation (PS-PWM) strategy with the sub-modules' full-bridge structure in order to achieve a higher closed-loop control bandwidth at parity of switching frequency by sequentially commanding the cascaded cells. Therefore, the goal met in this master thesis was to design and test the proposed Sequential PS-PWM algorithm, which is capable of obtaining a precise output voltage average at the equivalent output frequency. Thus, improving the equivalent sampling and update frequency of a CHB multilevel converter. Moreover, simulation results in open- and closed-loop, confronted with standard unipolar modulation, are presented to verify the performance of the proposed algorithm.**

I. Introduction

Among existing multilevel converter topologies, the Cascaded-H-Bridge (CHB) converter was found useful in applications such as high-voltage dc conversion stations and renewable generation plant connection to the grid. Its modular characteristic provides some benefits as: reduced manufacturing costs and replacement; capability for higher voltage connection; low output voltage distortion due to several voltage levels. Hence, the improvement of features from this type of converter becomes encouraging. Considering the CHB control, its closed-loop bandwidth may be extended at parity of switching frequency by making use of the Phase-Shifted Pulse Width Modulation (PS-PWM) technique.

II. Objectives of Master Thesis

The main objective of this project is to design and test the proposed Sequential PS-PWM algorithm, compare it with standard unipolar modulation, and assemble a two-step current model predictive control (MPC) in order to achieve the highest possible bandwidth. The second objective involves rending the proposed algorithm more suitable for a practical application. Therefore, taking into account non-idealities and mitigating them. The activity is mainly evolved on concept layout, model implementation in PLECS environment, method and numerical validation, followed by a comparative analysis.

My key personal contribution is the Sequential PS-PWM algorithm for a 5-cell CHB converter for operation on Single-Update mode on carrier peaks and on Double-Update mode.

Secondary implementations include:

- PLECS model of a CHB in single and three-phase
- Two-step current MPC
- Load parameter estimator
- Current regulators
- Blanking time compensation
- Decoupled Second-Order Generalized Integrator (DSOGI) and Phase-Locked Loop (PLL)

III. Methods

The PS-PWM is the modulation strategy on which the Sequential Algorithm was build upon. Its working principle is shown in Fig. 1, where each series-connected SM has its own carrier signal of period T_c, shifted from one another in time by T_c/N.

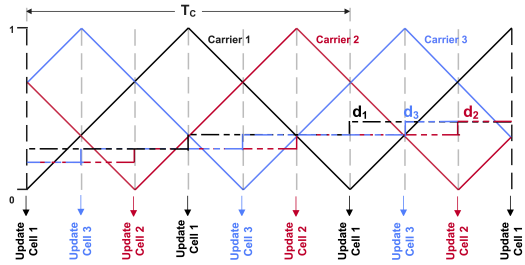

Figure 1: PS-PWM working principle operating on Double-Update mode, for three half-bridge converters connected in series. Where $T_{eq} = T_c/(2N)$.

The algorithm is based on achieving a CHB output voltage average, in the update period, equal to a given reference, as shown in Eq. 1.

$$\langle v_{CHB} \rangle_{T_{eq}} = v^*_{CHB} \tag{1}$$

The update period T_{eq} is the equivalent converter output voltage, and it is equal to T_c/N and $T_c/(2N)$ for Single- and Double-Update mode, respectively. Therefore, the starting method was to study the cell modulation on both carrier peaks and valleys for a 5-cell CHB converter, and consequently investigate how to exploit the duty-cycle common-mode d_{CM}, degree of freedom given by the full-bridge structure.

IV. Models

The Sequential Algorithm was first constructed for a single-phase open-loop CHB. For that, two voltage references are computed, one for each converter leg, each

ensuring the condition of voltage balancing in a specific segment of the carrier period. Thereupon, the circuit was closed with an RLE-load, where a two-step current MPC had to be assembled discretizing a generic circuit expression. A minimum receding horizon of two steps is needed to overcome the one-step delay introduced by the converter and to model the current in the following step, so that a specific total voltage reference v^*_{CHB} can be computed. At the end, an extension of the model in three-phase was done, as depicted in part by Fig. 2, along with the implementation of the DSOGI and PLL block functions for grid monitoring and synchronization, allowing robustness tests for a grid coupling application.

Furthermore, since the dynamics of input capacitor were out of the scope, input voltage of the SMs remained constant. Nonetheless, in order to create a more realistic model, other non-idealities were taken into account:

- Current regulators: set as proportional-resonant in stationary frame and proportional-integral in synchronous frame.
- Load estimation: achieved with a Least-Mean-Squares algorithm.
- Blanking time effect: compensated by adding to voltage references the voltage loss expression multiplied to a Sigmoid function, as a function of phase-current.

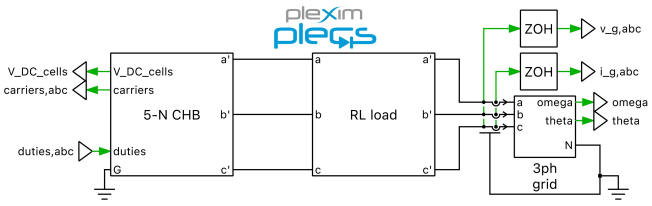

Figure 2: Three-phase CHB model with grid coupling, where five SMs are contained on each branch.

V. Results

The achievement of the main goal was verified on both open- and closed-loop conditions. The Sequential PS-PWM algorithm was able to successfully provide a voltage output in the equivalent period average equal to the voltage reference, as shown in Fig. 3. A test on equal conditions was done with the standard unipolar modulation method, with non-negligible errors found in the same averaging. When both modulation strategies were tested in a closed-loop control, the former modulation strategy was observed to hold a stable control, while the later was unable to withstand the control at such high bandwidth, presenting elevated current oscillations. An example of the duty-cycle scope, resulting from the Sequential Algorithm, from one of the SMs, is depicted in Fig. 4. It is possible to observe the bouncing effect of the common-mode in the Double-Update mode as it uses the modulation mechanism from both updates on carrier peaks and valleys, one after the other.

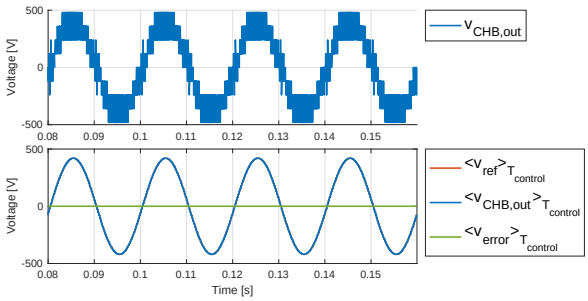

Figure 3: CHB voltage output for $M_{idx} = 0.7$ in an open-loop control at period of $T_c/5$ in Single-Update mode.

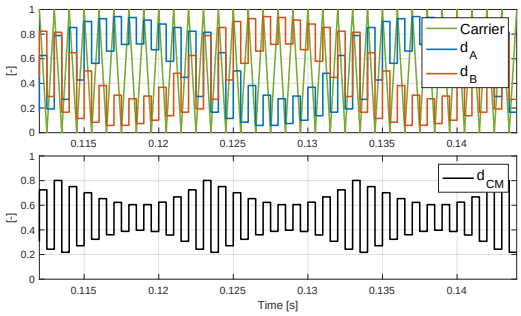

Figure 4: Modulation scope in Double-Update mode using the Sequential PS-PWM Algorithm.

VI. Discussion

The main drawback is related to the saturation of the immediate balancing voltage, leading to a limitation of modulation index of 72% and 87% for Single- and Double-Update mode, respectively. This happens when the balancing voltage requested to the following activation cell is larger than its input voltage. It occurs for quick changes of reference amplitude as well as after reference zero-crossings. However, this problem can be attenuated with a more clever choice of the estimated voltage given by other cells, object of further work.

VII. Conclusions

In this master thesis, the Sequential PS-PWM algorithm for CHB converters was designed and build in PLECS environment. Its functionalities were demonstrated and verified by open- and closed-loop tests and were compared to a standard unipolar modulation technique. Complementary features comprises the set-up of the two-step current predictor, the compensation of non-idealities, and a grid coupling simulation for a three-phase system. Drawbacks were identified and possible mitigation measures were suggested. Further work may include the implementation of the Sequential PS-PWM algorithm in a hardware-in-the-loop or in the modulation control of a Virtual Synchronous Generator.