POLITECNICO DI TORINO

Department of Energy
Master Thesis in Electrical Engineering

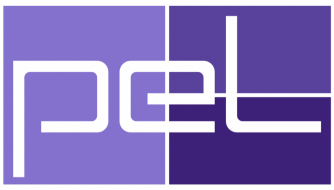
Sequential Phase-Shifted PWM for Cascaded-H-Bridge Multilevel Converters

Candidate: Luca Vincenzo Stroppiana

Advisor: Andrea Cervone
Supervisor: Prof. Radu Bojoi
Supervisor: Prof. Dražen Dujić

October 2022

Work carried out at:



Power Electronics Laboratory

École Polytechnique Fédérale de Lausanne

Acknowledgements

I only have words of gratitude and esteem towards my thesis advisor, Andrea Cervone. Besides all that I could learn with him, he helped me realize a greater meaning for guidance and availability.

I would like to express my deepest gratitude and respect with regard to my thesis supervisors: Prof. Radu Bojoi, whose insights and reviews were fundamental; Prof. Dražen Dujić for the clarifying dialogues.

Per la fine di questo ciclo di cinque anni, io vorrei ringraziare la mia famiglia, che pur stando lontano mi ha dato un sostegno insostituibile. In specifico ringrazio: mia madre Eliana, base di tutta la mia formazione; mio padre Giovanni che avrò sempre nel cuore; mia sorella Monaliza, la mia più grande fonte di ispirazione; mia zia Bruna, per la quale provo una grande tenerezza.

Altresì, vorrei ringraziare i miei amici di Torino per aver aggiunto tanta gioia a questo percorso e per i momenti indimenticabili.

L. S.

Abstract

The full-bridge topology and the modular multilevel structure of Cascaded-H-Bridge (CHB) converters give advantageous features as voltage distribution along the cells, making them an adequate choice when it comes to medium and high voltage applications. Such applications include high voltage direct-current conversion stations [1], Static Synchronous Compensators [2], rail interties [3], and direct renewable generation plant to distribution grid [4]. Bearing in mind the possible benefits in industry and in for the renewable energy integration, the improvement in control methods of this converter type becomes interesting.

For instance, it is possible to use the Phase-Shifted Pulse Width Modulation (PS-PWM) method along with the full-bridge structure in order to increase the update and control frequency of the CHB converter, at parity of switching frequency, by sequentially commanding the cascaded cells. Therefore, this thesis aims at providing a modulation algorithm for a CHB multilevel converter, modelled in PLECS environment, that is able to achieve null modulation error at the equivalent output frequency.

First, the fundamental converter structure and the PS-PWM working principle is explained following by the analysis of modulation functions and the exploitation of the common-mode, degree of freedom provided by the full-bridge structure. Then, the process of construction of the Sequential PS-PWM Algorithm is described, along with the explanation of the standard unipolar and Multisampled modulation functions, used in different moments for comparison. A model predictive control with two-step receding horizon is set so as to achieve the maximum theoretical bandwidth of the current controller. Then, open- and closed-loop simulation results using the proposed modulation algorithm are shown and confronted with the standard unipolar modulation function under the same update conditions. Thereupon, it is presented the mitigation of non-idealities as load estimation, current correction actions and blanking time compensation. Finally, CHB converter model is extended to a three-phase system and the Decoupled Second-Order Generalized Integrator and Phase-Locked Loop function blocks are implemented for grid monitoring and synchronization, in order to perform robustness tests of a grid-connected application.

Keywords: Cascaded-H-Bridge, Phase-Shifted Pulse Width Modulation, modular multilevel converter, model predictive control, grid-connected converter.

Contents

List of Figures

List of Tables

1 Introduction

1.1 Motivation

The continuous industrial development in the last years were key for the price decrease of renewable electricity generation technologies and, consequently, for its emerging implementation, as shown in Fig. 1.1. This action is crucial in order to meet medium and long global terms of carbon-emission shift.

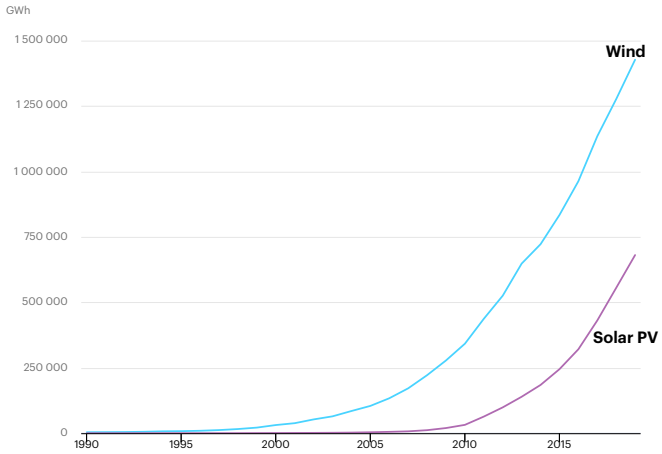


Figure 1.1: Renewable electricity generation by source, World 1990-2019. IEA, [5].

On the other hand, it is possible to note a trend in the investment on direct-current (dc) electricity transmission with high voltage dc (HVDC) lines, which can be convenient for extensive connections in terms of investments costs and losses, compared to the scale used in alternate-current (ac) transmission. Also, a positive feature is their suitability for renewable energy integration. The relevance of HVDC connections are, for instance, well present in northern Europe, as shown in Fig. 1.2.

The replacement of stable traditional fossil fuel plants to intermittent renewable generators also yields the grid less robust. When considered also industrial processes, ancillary services,

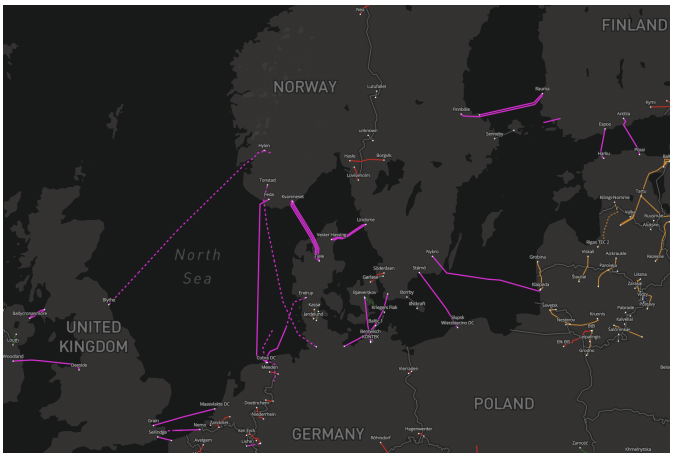


Figure 1.2: HVDC lines in northern Europe. Dotted lines indicate connections under construction. ENTSOE, [6].

as provided by Static Synchronous Compensators (STATCOMs), are of great use to ensure ac grid stability, specially when employed in weak networks.

Overall, there are many applications in the medium and high voltage range which may benefit from the employment of adequate converters. For instance, challenges may rise both in terms of product manufacturing and in the spread of decentralized electricity production. In order to easy this process, it is important to make use of converter topologies that may possibly allow the spare of bulky and expensive components like transformers, while guaranteeing power quality requirements.

In the last decade, modular multilevel converters (MMC), branch of voltage source converters, has became one of the most attractive options for use in high voltage applications as in HVDC conversion stations and in the grid connection of renewable power plants. A common MMC example is the Cascaded-H-Bridge (CHB) converter. The modular feature provides some attractive characteristics as reduced manufacturing costs and replacement, capability for higher voltage connection and low output voltage distortion due to several voltage levels, [7].

For instance, the use of CHB converters in large photovoltaic (PV) farms have been studied and is already present in literature [4]. The Fig. 1.3 depicts a possible configuration of coupling between PV arrays directly to the medium voltage (MV) network.

Regarding the control strategy, there are different modulation techniques that make use of these converter type with, however, different performance and advantages. The Phase-Shifted Pulse Width Modulation (PS-PWM) is a type of modulation technique capable of improving the equivalent sampling and update frequency of multilevel converters by increasing the output equivalent frequency. Additionally, the full-bridge cell structure provides a degree of freedom in the cell modulation, named duty-cycle common-mode, which may be exploited with the PS-PWM strategy in order to obtain a higher bandwidth of the closed-loop control, at

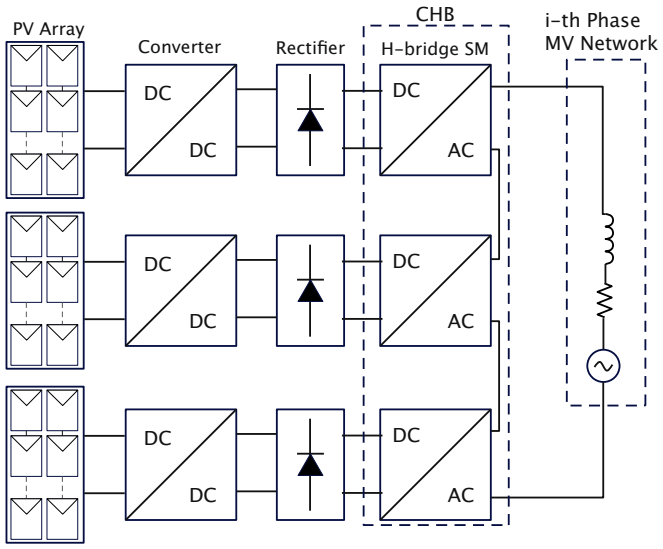


Figure 1.3: PV farm connected to grid with CHB.

the parity of switching frequency, by sequentially commanding the cells.

1.2 Thesis objectives and personal contributions

The main objective of this project is to design and test the proposed Sequential PS-PWM modulation algorithm, compare it with the standard unipolar and Multisampled modulation techniques, under appropriate conditions. In accordance with the main objective, a current model predictive control (MPC) had to be implemented in order to achieve the highest possible bandwidth in closed-loop. Complementary objectives involving the experimentation of the CHB control includes mitigating non-idealities.

The activity is mainly evolved on concept layout, model implementation in PLECS environment, method and numerical validation, followed by a comparative analysis.

My key personal contributions are:

- Sequential PS-PWM Algorithm for Single-Update mode on carrier Peaks
- Sequential PS-PWM Algorithm for Double-Update mode

Other implementations, which include the knowledge on mature literature material, are:

- PLECS model of a CHB in single and three phase
- Two-step current MPC
- Load estimator

- Blanking time compensation
- Proportional resonant and integral current regulators
- Grid coupling using a Decoupled Second-Order Generalized Integrator and a Phase-Locked Loop

1.3 Work structure

This master thesis is organized as to proportionate a clear building-up thought process to the reader.

In chapter 2, the fundamental concepts and working principles, from which the models used in the project are based on, are explained. In chapter 3, the algorithm and construction of the proposed Sequential PS-PWM control method is described, along with resulting end-effect. In chapter 4 the process of closing the loop adding a generic load to the CHB converter is delineated, including the construction of the current MPC used in both stationary and synchronous reference frames. Chapter 5 presents open- and closed-loop results and discusses drawbacks of the proposed algorithm. Then, on chapter 6, the mitigation process of certain non-idealities taken into account is presented, in order to rend the model more suitable for a possible real implementation. Moreover, in chapter 7 the three-phase model extension and the grid coupling process are explained, along with a robustness test under frequency change and unbalanced grid voltage conditions. Finally, the conclusions are then drawn and future aspects are outlined in chapter 8.

Theory is added when judged necessary for the sake of clear understanding for the reader. The material reported in the appendixes should complement, in a helpful but not essential way, points which are reported throughout the thesis. It does not depletes, however, all the theory which may be behind certain topics.

2 Fundamental concepts and model configuration

In this chapter, the basic structures are presented, along with key concepts, which altogether form the conceptual building blocks used in the understanding of the main proposal.

2.1 H-bridge cell

The converter topology chosen for the project development was the H-bridge, or full-bridge, cell. It consists of two converter legs, namely A and B, each of them with a pair of switching devices, such as Insulated Gate Bipolar Transistors, coupled with anti-parallel diodes. A scheme is represented by Fig. 2.1, although simplified since the structure of other functionalities such as gate driver and snubber circuit are not present.

When self-commutated transistors are used, the H-bridge cell can be seen as a voltage source converter. Furthermore, because of its structure, it is possible to obtain three voltage levels at the output: 0, $+V_{DC}$ and $-V_{DC}$, where V_{DC} is the voltage across the cell's input capacitor.

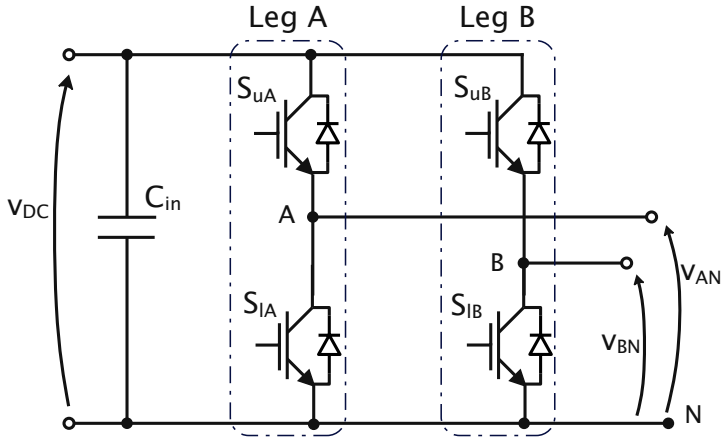


Figure 2.1: Full-bridge single cell.

When used in a multilevel converter, each H-bridge cell can be viewed as a sub-module (SM).

2.2 Cascaded-H-Bridge converter

Fig. 2.1 depicts the basic topology of a single-phase CHB converter, where each branch is composed of N SMs connected in series. Thanks for the full-bridge cell, the CHB converter has bidirectionally capability and an intrinsic degree of freedom in modulation.

Each phase can be understood as a controllable voltage source with N possible voltage steps, resulting in the partition of the total input voltage $V_{DC,tot}$, which in a balanced case is equally shared among the branch SMs, $V_{DC,tot}/N$. Thus, higher the number of sub modules, the closer the ac output will be to a sine waveform.

Advantages of the CHB include lower switching losses because of its low dv/dt over an individual switching device, compared to a higher voltage rated converter. Its modular structure allows easier replacement or repair of SMs, capability for MV connection because the sum of many voltage levels at the output, which also contributes to lower output distortion. In fact, a CHB is characterized by having $2N+1$ voltage levels at the output.

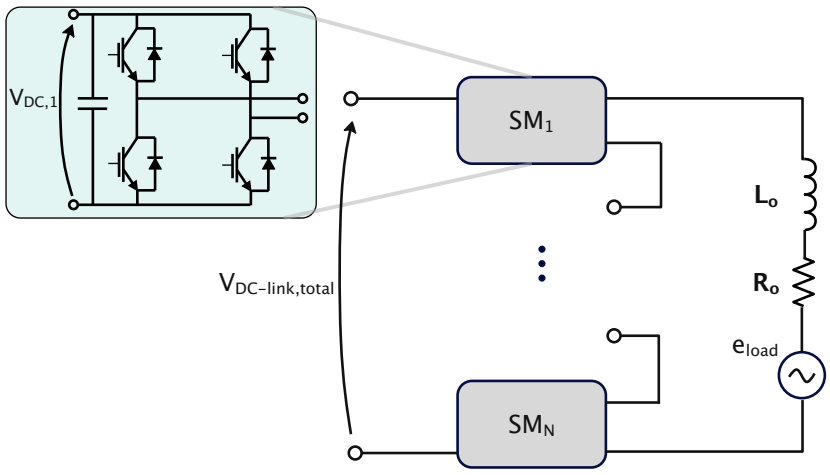


Figure 2.2: N-cell Cascaded-H-Bridge converter scheme.

2.3 CHB converter power supply

The CHB multilevel converter requires a number of isolated dc supplies, each of which feeds an H-bridge power cell. The dc supplies are normally obtained from multipulse diode rectifiers as depicted in Fig. 2.3. The three-phase diode rectifier, 6 diodes per pack, are fed by a galvanic-isolated transformer secondary windings. Each winding is phase-shifted from one another in order to cancel low-order harmonics.

Even so, by neglecting the still existent harmonics injected at the full-bridge input, it was assumed throughout the work that the input voltage between all the cells is balanced and constant.

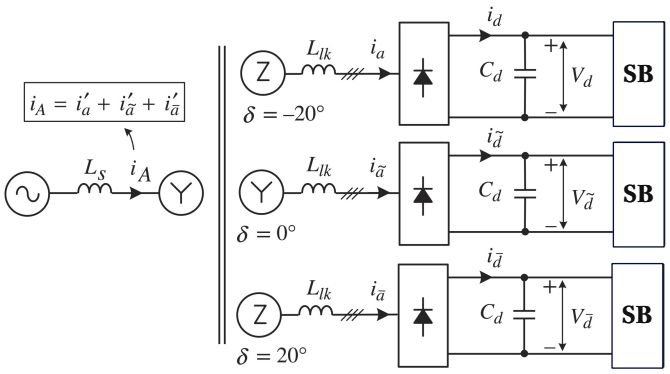


Figure 2.3: 18-pulse separate-type diode rectifier used for the voltage supply of a 7-levels CHB [8].

2.4 Three-level full-bridge PWM

As shown in Fig. 2.4, the full-bridge converter legs are controlled separately by comparing $v_{control}$ and $-v_{control}$ to the triangular waveform v_{tri}, also called the carrier signal.

$$v_{control} \geq v_{tri} \longrightarrow S_{uA} \text{ on and } V_{AN} = V_{DC}$$
$$v_{control} < v_{tri} \longrightarrow S_{uA} \text{ off and } V_{AN} = 0$$

Analogously for the other converter leg:

$$-v_{control} \geq v_{tri} \longrightarrow S_{uB} \text{ on and } V_{BN} = V_{DC}$$
$$-v_{control} < v_{tri} \longrightarrow S_{uB} \text{ off and } V_{BN} = 0$$

If the output voltage is averaged in the whole carrier period, then it is possible to express it with duty-cycles, as shown in Eq. 2.1.

$$v_{iN} = V_{DC}\frac{t_{on}}{T_c} \tag{2.1a}$$
$$= V_{DC} \cdot d_i \quad i = \{A, B\} \tag{2.1b}$$

A duty-cycle represents the portion of intermittent operation of a switching device, that is, the period of time that it stays on during the whole switching period. Thus, it varies in the interval [0, 1].

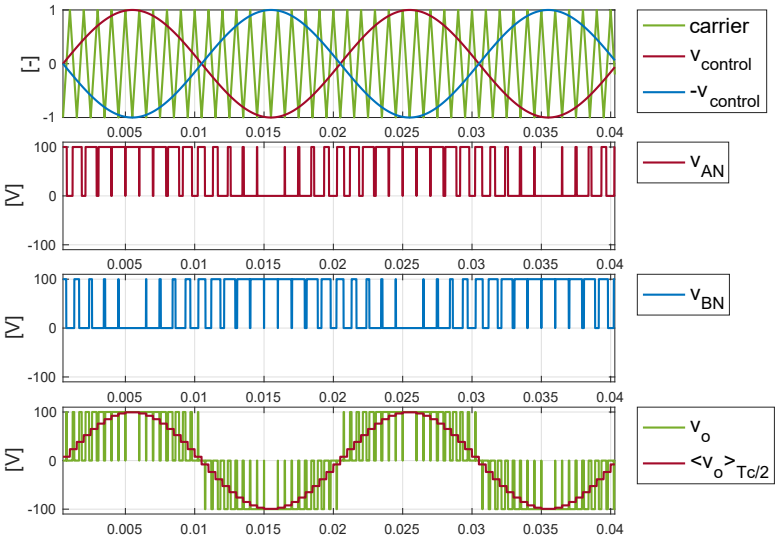


Figure 2.4: PWM with unipolar voltage switching on a full-bridge converter.

When using duty-cycles, the carrier must as well vary in the same range, so that the average voltage in that switching will have the same modulation index of the duty-cycle value. After the signal comparison, the switching signals s_{uA} and s_{uB} are generated to command the switching device. s_{lA} and s_{lB} are the negated signals with respect to the commanding signal of that converter leg.

The state permutation of four switching devices gives $2^2 = 4$ possible conduction configurations. This permutation of conduction states is listed in Table 2.1, where 1 stands for when a switching device is conducting (on-state) and conversely for 0 (off-state). The case of the simultaneous conduction of two devices from the same converter leg is excluded, since it represents a short-circuit of the dc-link.

	Switching device			
V_o	s_{uA}	s_{lA}	s_{uB}	s_{lB}
$+V_{DC}$	1	0	0	1
0	1	0	1	0
0	0	1	0	1
$-V_{DC}$	0	1	1	0

Table 2.1: Single cell output voltage according to switching device state.

Equation 2.2 shows the full-bridge instantaneous output voltage, giving the possible states $\{-V_C, 0, +V_C\}$.

$$v_{out} = V_{DC} \cdot (s_A - s_B) \tag{2.2}$$

In the average equivalent update period, the voltage expression is described by Eq. 2.3.

$$\langle v_{out} \rangle_{T_{eq}} = V_{DC} \cdot (d_A - d_B) \tag{2.3a}$$

$$d_{diff} = d_A - d_B \tag{2.3b}$$

Where d_{diff} is the differentiable duty-cycle. Therefore, the individual control of the duty-cycles d_A and d_B allows to control the desired averaged output voltage $\langle v_{out} \rangle^*_{T_{eq}}$ in the interval $[-V_{DC}, +V_{DC}]$.

From the control point of view, it becomes also appropriate to define the modulation index, different from d_{diff}, as shown in 2.4. Where $\langle \hat{v_{out}} \rangle_{T_{eq}}$ is the peak amplitude of the averaged voltage reference.

$$M_{idx} = \frac{\langle \hat{v_{out}} \rangle_{T_{eq}}}{V_{DC}} \tag{2.4}$$

It is important to note that there is a degree of freedom in the computation of the differentiable duty-cycle due to the presence of two converter legs. Therefore, in order to quantize this degree of freedom, it can be defined the duty-cycle common-mode, which expression is demonstrated in Eq. 2.5.

$$d_{CM} = \frac{d_A + d_B}{2} \tag{2.5}$$

Using the Equations 2.3 and 2.5, a relation can be obtained for duty-cycle computation, if d_{CM} is imposed.

$$d_A = d_{CM} + \frac{1}{2} \frac{\langle v_{out} \rangle^*_{T_{eq}}}{V_{DC}} \tag{2.6a}$$

$$d_B = d_{CM} - \frac{1}{2} \frac{\langle v_{out} \rangle^*_{T_{eq}}}{V_{DC}} \tag{2.6b}$$

However, the conditions of having concurrently $d_A, d_B \in [0,1]$ impose boundaries to the choice of duty-cycle common-mode. By comparing the cases of output voltage sign $v_o \lessgtr 0$, it is possible to find an expression for the boundaries.

$$d_{CM,max} = 1 - \frac{|d_{diff}|}{2} \tag{2.7a}$$

$$d_{CM,min} = \frac{|d_{diff}|}{2} \tag{2.7b}$$

Since d_{diff} is in the range [-1, 1], then $d_{CM} \in [0,1]$. An example of the boundaries of d_{CM} is shown in Fig. 2.5 for a $M_{idx} = 0.75$, where the duty-cycle common-mode is referenced at 0.3.

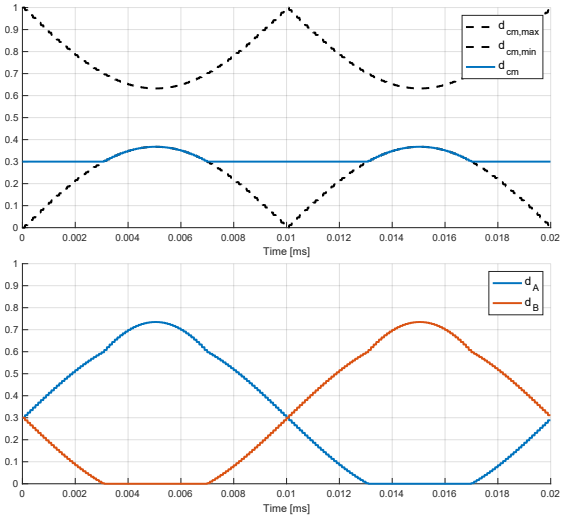


Figure 2.5: Duty-cycles and common-mode on fundamental period, for sinusoidal modulation and $d^*_{CM} = 0.3$.

Fig. 2.6 demonstrates an example of modulation with d_{CM} imposed to 0, which is then saturated with $d_{CM,min}$. Hence, it is observed that the common-mode can be arbitrarily chosen to be set anywhere within its boundaries.

The degree of freedom of d_{CM} may be explored for the subsequent considerations in case of a cascaded converter. It is important to note that for this analysis, d_{CM} with operation on Double-Update and a Single-Update modes behave in the same way. However, this is not the case in a sequential PS-PWM.

2.5 Sequential PS-PWM working principle

PS-PWM is one of the most popular modulation techniques for multilevel converters as the CHB, since it provides natural balancing of SMs' capacitor voltage, even distribution of power

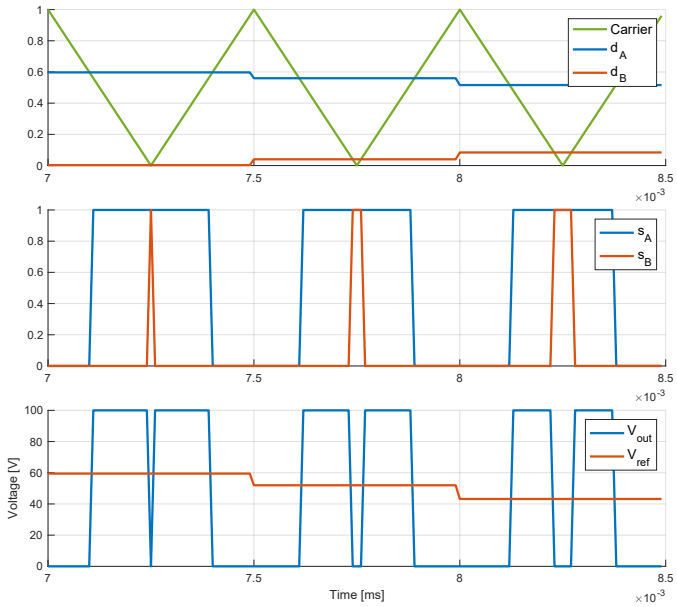


Figure 2.6: Single full-bridge cell scope, working on Single-Update.

losses among the SMs, and minimization of the dc-link current ripple. Additionally, it has been associated with predictive control strategies for multilevel converters [9],[10], [11].

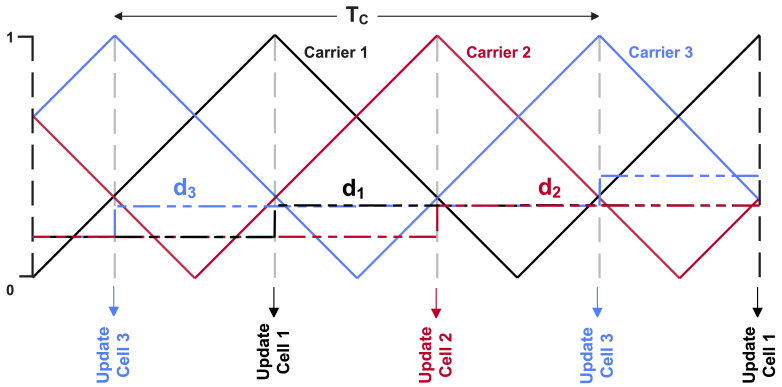
The PS-PWM has the advantage of providing an apparent switching frequency at the output voltage, of a single converter leg, equal to $N \cdot f_c$ for Single-Update and $2N \cdot f_c$ for Double-Update mode; being f_c the carrier frequency, which is limited by the switching frequency.

The Sequential PS-PWM Algorithm is based on the assumption that, if there are N full bridge cells and they locally generate carrier signals shifted from one another in time by T_c/N, it is still possible to keep a regular sampling in each cell, that is, its duty-cycle is only updated at the peaks and/or valleys of the corresponding carrier.

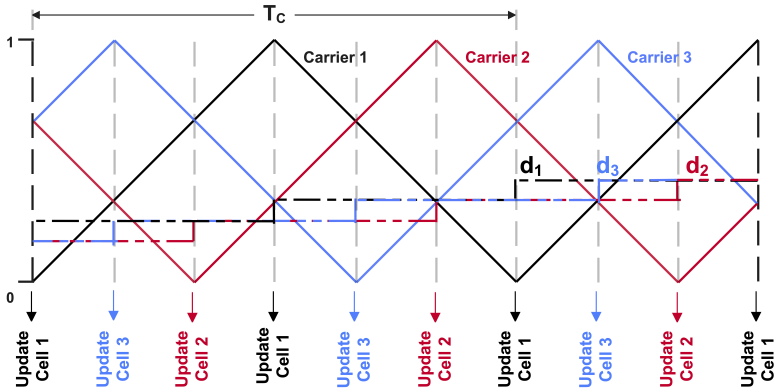
Fig. 2.7 depicts the working principle of the PS-PWM for a $N = 3$ half-bridge cells connected in series operating on Single- and Double-Update modes. In the latter case, the duty-cycles of a single cell are updated with a sampling period of $T_s = T_c/2$, obtaining an overall apparent switching frequency of the output voltage of $2N \cdot f_c$, equivalent to an equivalent period of $T_{s,eq} = T_s/3 = T_c/6$.

If the average overall voltage of the output series is controlled in each $T_{s,eq}$ period, then the overall update rate is increased and, as a consequence, not only the apparent switching frequency can be enhanced but also the net control bandwidth improved.

Furthermore, from the controller point of view, the maximum bandwidth can be obtained with a current MPC and is theoretically limited by the Nyquist frequency $f_{Nyq} = f_s/2$. Where f_s is the analog-to-digital sampling, synchronized with the update period of the PWM.



(a) Single-Update on carrier peaks. $T_{eq} = T_c/N$



(b) Double-Update. $T_{eq} = T_c/(2N)$

Figure 2.7: Timing diagram of standard PS-PWM according to update mode, for three half-bridge converters connected in series.

However, differently from the standard PWM, for the sequential PS-PWM, Single-Update on carrier peaks and valleys behave differently in terms of modulation function and the resulting degree of freedom d_{CM}.

2.6 PS-PWM analysis according to update configuration

In order to depict a PS-PWM control algorithm, it is necessary to investigate modulation properties that vary with the number of cells and update mode.

From now on, for the sake of consistency, the analysis will be done for a 5-cells CHB converter. Nevertheless, the final expression of modulation functions and voltage references used in an algorithm with an arbitrary number of cells would follow the same concepts. Each cell has its own carrier signal of period T_c, shifted from one another in time by $T_c/5$. The two duty-cycles of each cell, one for each converter leg of the full-bridge, are updated only on the characteristic point of that mode. The working principle represented is in one full carrier period.

2.6.1 Single-Update on carrier peaks

The update frequency of the overall CHB branch is $T_{s,eq} = T_c/5$, as depicted in Fig. 2.8.

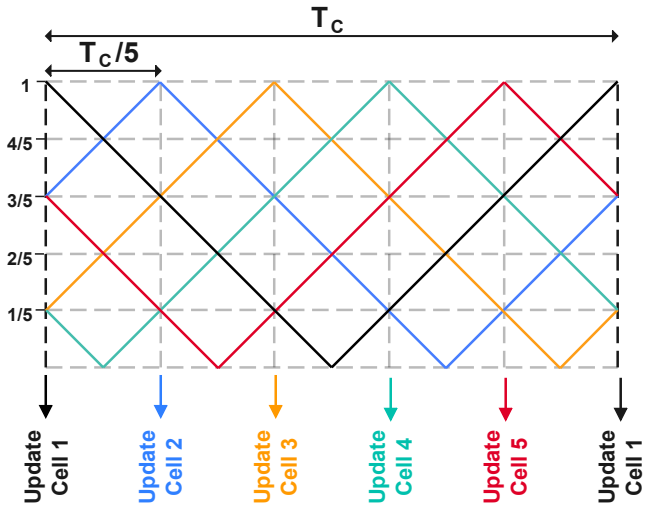


Figure 2.8: Timing diagram of standard PS-PWM working on Single-Update mode, with update on carrier peaks.

Suppose to consider the interval of time between the update of Cell 1 and Cell 2. In this interval, of length $T_{s,eq}$, the CHB is asked to generate, on average, the output voltage v^*_{CHB}. The output voltage of the CHB is given by the sum of the output voltages of the 5 series-connected full-bridges, meaning the expression in Eq. 2.8.

$$\begin{aligned} v^*_{CHB} &= \sum_{k=1}^{5} \langle v_{out,k} \rangle_{T_c/5} \\ &= \langle v_{out,1} \rangle_{T_c/5} + \langle v_{out,2} \rangle_{T_c/5} + \langle v_{out,3} \rangle_{T_c/5} + \langle v_{out,4} \rangle_{T_c/5} + \langle v_{out,5} \rangle_{T_c/5} \end{aligned} \tag{2.8}$$

Since at the beginning of this interval only the duty-cycles of Cell 1 are updated, the output voltages of Cell 2 to Cell 5 were already pre-determined, they will be function of the corresponding duty-cycles computed in the previous update instants. Consequently, only $\langle v_{out,1} \rangle_{T_c/5}$ can be guided, and the aim of the control may be to achieve the expression below.

$$\langle v_{out,1} \rangle_{T_c/5} = v^*_{CHB} - \left(\langle v_{out,2} \rangle_{T_c/5} + \langle v_{out,3} \rangle_{T_c/5} + \langle v_{out,4} \rangle_{T_c/5} + \langle v_{out,5} \rangle_{T_c/5} \right)$$

The difference between a standard PWM algorithm is that, in this case, the desired output voltage does not need to be applied on average in a T_c period, but in a $T_c/5$ period, refereed here also as sub-period. During the sub-period, the carrier signal does not have a full excursion

between 0 and 1, meaning that the average output voltage in $T_c/5$ is not directly proportional to the duty-cycles. Therefore, the corresponding average voltage in the sub-period will be a linear piece-wise function with respect to the duty-cycle, represented by Eq. 2.9.

$$\mathcal{F}_1(d) = \begin{cases} \dfrac{d-3/5}{2/5} & \text{if } d \geq \dfrac{3}{5} \\ 0 & \text{if } d < \dfrac{3}{5} \end{cases} \tag{2.9}$$

Since the reasoning is true for both full-bridge legs, the output voltage of the single cell can be expressed as:

$$\begin{aligned} \langle v_{out} \rangle_{T_c/5} &= \langle v_{out,A} \rangle_{T_c/5} - \langle v_{out,B} \rangle_{T_c/5} \\ &= V_{DC} \left(f_p(d_A) - f_p(d_B) \right) \end{aligned} \tag{2.10}$$

It is important to note that at this point, as described in the section 2.4, there is still a degree of freedom to be set. It may be imposed, for example, to achieve the following condition in the whole carrier period.

$$\langle v_{out} \rangle_{T_c} = V_{DC} (d_A - d_B) = v^*_{out}$$

Other choice could be made. Still, $\langle v_{out} \rangle_{T_c}$ is arbitrarily imposed as an additional low-priority requirement.

By examining the expression of $\langle v_{out} \rangle_{T_c/5}$ from Eq. 2.10, four different cases are delineated in Table 2.2.

	$d_B < 3/5$	$d_B \geq 3/5$
$d_A < 3/5$	0	$-V_{DC} \cdot \frac{d_B - 3/5}{2/5}$
$d_A \geq 3/5$	$V_{DC} \cdot \frac{d_A - 3/5}{2/5}$	$V_{DC} \cdot \frac{d_A - d_B}{2/5}$

Table 2.2: Expression of $\langle v_{out} \rangle_{T_c/5}$ function of SM's duty-cycles, for update on carrier peaks. Undesired cases are marked in red.

Case analysis:

- $d_A, d_B < 3/5$

Is undesired because $\langle v_{out} \rangle_{T_c/5} = 0$.

- $d_A, d_B \geq 3/5$

It would be disadvantageous in obtaining high modulation index values, since the lack of voltage produced on average by the k-th CHB cell would need to be compensated by the (k+1)-th cell in the subsequent equivalent period.

- $d_A \geq 3/5$ and $d_B < 3/5$

The duty-cycles can be computed by solving the linear system:

$$\begin{cases} V_{DC} \cdot \dfrac{d_A - 3/5}{2/5} = \langle v_{out} \rangle_{T_c/5} = v^*_{out} \\ V_{DC} \cdot (d_A - d_B) = \langle v_{out} \rangle_{T_c} = v^*_{out} \end{cases}$$

The solution of the previous linear system is shown in Eq. 2.11, from which is possible to obtain $v^*_{out} \in [0, V_{DC}]$.

$$d_A = \frac{3}{5} + \frac{2}{5}\frac{v^*_{out}}{V_{DC}} \tag{2.11a}$$

$$d_B = \frac{3}{5} - \frac{3}{5}\frac{v^*_{out}}{V_{DC}} \tag{2.11b}$$

- $d_A < 3/5$ and $d_B \geq 3/5$

The duty-cycles can be computed by solving the linear system:

$$\begin{cases} -V_{DC} \cdot \dfrac{d_B - 3/5}{2/5} = \langle v_{out} \rangle_{T_c/5} = v^*_{out} \\ V_{DC} \cdot (d_A - d_B) = \langle v_{out} \rangle_{T_c} = v^*_{out} \end{cases}$$

The solution of the previous linear system is shown in Eq. 2.12, from which is possible to obtain $v^*_{out} \in [-V_{DC}, 0]$.

$$d_A = \frac{3}{5} - \frac{3}{5}\frac{v^*_{out}}{V_{DC}} \tag{2.12a}$$

$$d_B = \frac{3}{5} + \frac{2}{5}\frac{v^*_{out}}{V_{DC}} \tag{2.12b}$$

Having both cases chosen, it is possible for the full-bridge duty-cycles to be updated according the law below.

$$d_A = \begin{cases} \frac{3}{5} + \frac{2}{5}\frac{v^*_{out}}{V_{DC}} & v^*_{out} \geq 0 \\ \frac{3}{5} + \frac{3}{5}\frac{v^*_{out}}{V_{DC}} & v^*_{out} < 0 \end{cases} \qquad d_B = \begin{cases} \frac{3}{5} - \frac{3}{5}\frac{v^*_{out}}{V_{DC}} & v^*_{out} \geq 0 \\ \frac{3}{5} - \frac{2}{5}\frac{v^*_{out}}{V_{DC}} & v^*_{out} < 0 \end{cases}$$

Which is equivalent to impose a common-mode component as:

$$d_{CM} = \frac{3}{5} - \frac{1}{10} \cdot \frac{|v^*_{out}|}{V_{DC}}$$

This modulation can be locally applied to each CHB cell module. The only calculation that should be centralized is the computation of v^*_{out} from the knowledge of the modulation index and of the sub-period average voltages from the other CHB cells.

2.6.2 Single-Update on carrier valleys

This is the dual case with respect to the previous one. The timing diagram of the Phase-Shifted carriers is illustrated in Fig. 2.9.

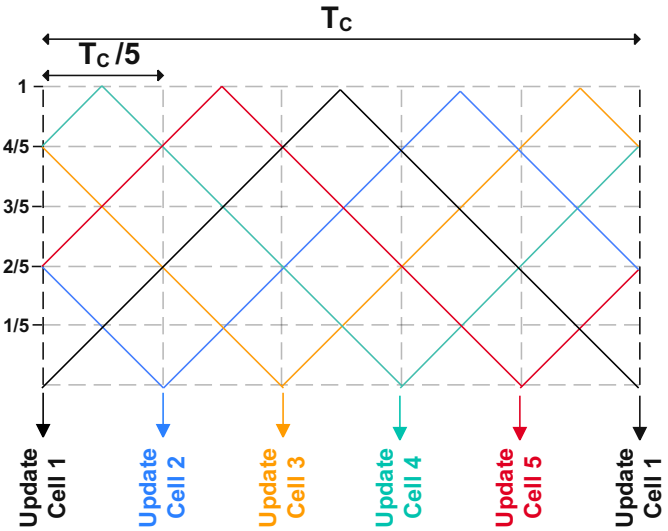


Figure 2.9: Timing diagram of standard PS-PWM working on Single-Update mode with update on carrier valleys.

If the same reasoning from the previous case is adopted, it is possible to focus on just one full-bridge cell, whose aim is to develop the voltage v^*_{out} on average, both in a $T_c/5$ and T_c

periods. By focusing in the sub-period, the output voltage of a single leg can be expressed as in 2.13.

$$\langle v_{out,leg} \rangle_{T_c/5} = \begin{cases} V_{DC} \cdot \dfrac{d}{2/5} & \text{if } d < \dfrac{2}{5} \\ V_{DC} & \text{if } d \geq \dfrac{2}{5} \end{cases} \tag{2.13}$$

From which is possible to identify four cases.

	$d_B < 2/5$	$d_B \geq 2/5$
$d_A < 2/5$	$V_{DC} \cdot \frac{d_A - d_B}{2/5}$	$-V_{DC} \cdot \frac{2/5 - d_A}{2/5}$
$d_A \geq 2/5$	$V_{DC} \cdot \frac{2/5 - d_B}{2/5}$	0

Table 2.3: Expression of $\langle v_{out} \rangle_{T_c/5}$ function of SM's duty-cycles, for update on carrier valleys. Undesired cases are marked in red.

In the larger period, the condition 2.14 is imposed.

$$\langle v_{out} \rangle_{T_c} = V_{DC}(d_A - d_B) = v^*_{out} \tag{2.14}$$

The cases where d_A and d_B are both less than $2/5$ or both greater than $2/5$ at the same time can be discarded, since they do not allow a simultaneous control of both $\langle v_{out} \rangle_{T_c/5}$ and $\langle v_{out} \rangle_{T_c}$.

- $d_A \geq 2/5$ and $d_B < 2/5$

The duty-cycles can be computed by solving the linear system:

$$\begin{cases} V_{DC} \cdot \dfrac{2/5 - d_B}{2/5} = \langle v_{out} \rangle_{T_c/5} = v^*_{out} \\ V_{DC} \cdot (d_A - d_B) = \langle v_{out} \rangle_{T_c} = v^*_{out} \end{cases}$$

The solution of the previous linear system is shown in Eq. 2.15, from which is possible to obtain $v^*_{out} \in [0, V_{DC}]$.

$$d_A = \frac{2}{5} + \frac{3}{5}\frac{v^*_{out}}{V_{DC}} \tag{2.15a}$$

$$d_B = \frac{2}{5} - \frac{2}{5}\frac{v^*_{out}}{V_{DC}} \tag{2.15b}$$

- $d_A < 2/5$ and $d_B \geq 2/5$

The duty-cycles can be computed by solving the linear system:

$$\begin{cases} -V_{DC} \cdot \dfrac{2/5 - d_A}{2/5} = \langle v_{out} \rangle_{T_c/5} = v^*_{out} \\ V_{DC} \cdot (d_A - d_B) = \langle v_{out} \rangle_{T_c} = v^*_{out} \end{cases}$$

The solution of the previous linear system is shown in Eq. 2.16, from which is possible to obtain $v^*_{out} \in [-V_{DC}, 0]$ in the SM output.

$$d_A = \frac{2}{5} + \frac{2}{5}\frac{v^*_{out}}{V_{DC}} \tag{2.16a}$$

$$d_B = \frac{2}{5} - \frac{3}{5}\frac{v^*_{out}}{V_{DC}} \tag{2.16b}$$

Once the modulation cases are chosen, it is possible to formulate the duty-cycle update law.

$$d_A = \begin{cases} \frac{2}{5} + \frac{3}{5}\frac{v^*_{out}}{V_{DC}} & v^*_{out} \geq 0 \\ \frac{2}{5} + \frac{2}{5}\frac{v^*_{out}}{V_{DC}} & v^*_{out} < 0 \end{cases} \qquad d_B = \begin{cases} \frac{2}{5} - \frac{2}{5}\frac{v^*_{out}}{V_{DC}} & v^*_{out} \geq 0 \\ \frac{2}{5} - \frac{3}{5}\frac{v^*_{out}}{V_{DC}} & v^*_{out} < 0 \end{cases}$$

Which is equivalent to impose a common-mode component as:

$$d_{CM} = \frac{2}{5} + \frac{1}{10} \cdot \frac{|v^*_{out}|}{V_{DC}}$$

Being the only differences in the duty-cycle common-mode between the update on carrier peaks and valleys is the term 2/5 instead of 3/5 and the sign of the term multiplying $|v^*_{out}|$.

Again, this modulation can be locally applied to each CHB cell module. The only calculation that should be centralized is the computation of v^*_{out} from the knowledge of the modulation index and of the average voltages (in the equivalent period) of the other CHB cells.

2.6.3 Double-Update

In the Double-Update case, the algorithm will vary. Considering once again the case of a 5-cell CHB, the resulting timing diagram can be refereed in Fig. 2.10. Now the equivalent update period will be $T_c/10$ due to the duty-cycle update at both carrier peaks and valleys, and the desired output voltage should be imposed in the halved sub-period with respect to the previous cases.

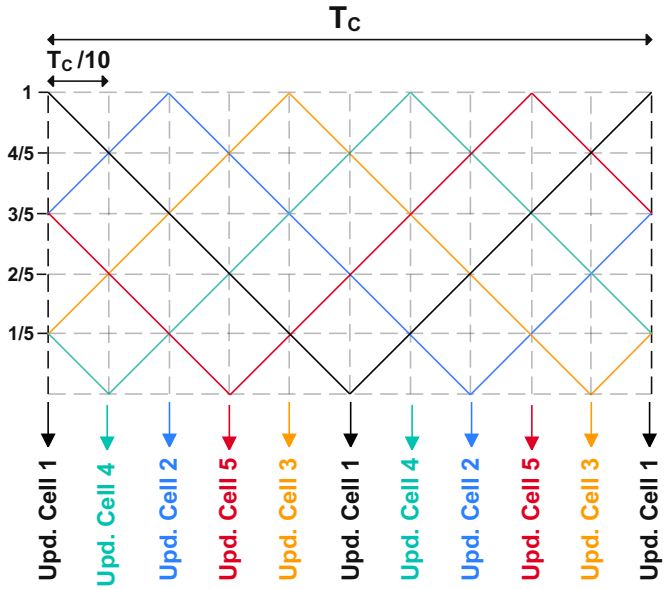


Figure 2.10: Timing diagram of standard PS-PWM working on Double-Update mode. Equivalent period equals $T_c/(2 \cdot N)$.

The same approaches of the previous subsections can be applied, by just modifying the interval of interest from $T_c/5$ to $T_c/10$ and by recomputing the modulation piece-wise linear function.

In case of update on peaks the results are:

$$d_A^p = \begin{cases} \frac{4}{5} + \frac{1}{5}\frac{v_{out}^*}{V_{DC}} & v_{out}^* \geq 0 \\ \frac{4}{5} + \frac{4}{5}\frac{v_{out}^*}{V_{DC}} & v_{out}^* < 0 \end{cases} \qquad d_B^p = \begin{cases} \frac{4}{5} - \frac{4}{5}\frac{v_{out}^*}{V_{DC}} & v_{out}^* \geq 0 \\ \frac{4}{5} - \frac{1}{5}\frac{v_{out}^*}{V_{DC}} & v_{out}^* < 0 \end{cases} \qquad d_{CM}^p = \frac{4}{5} - \frac{3}{10} \cdot \frac{|v_{out}^*|}{V_{DC}}$$

In case of update on valleys the results are:

$$d_A^v = \begin{cases} \frac{1}{5} + \frac{4}{5}\frac{v_{out}^*}{V_{DC}} & v_{out}^* \geq 0 \\ \frac{1}{5} + \frac{1}{5}\frac{v_{out}^*}{V_{DC}} & v_{out}^* < 0 \end{cases} \qquad d_B^v = \begin{cases} \frac{1}{5} - \frac{1}{5}\frac{v_{out}^*}{V_{DC}} & v_{out}^* \geq 0 \\ \frac{1}{5} - \frac{4}{5}\frac{v_{out}^*}{V_{DC}} & v_{out}^* < 0 \end{cases}$$

$$d_{CM}^{v} = \frac{1}{5} + \frac{3}{10} \cdot \frac{|v_{out}^{*}|}{V_{DC}}$$

The same full-bridge cell must apply both results on each carrier period, alternating from one mode to the other.

3 Modulation algorithms

This chapter focuses on the construction process of the proposed modulation algorithm and on the presentation of the other modulation functions used for comparison. At last, the Sequential PS-PWM Algorithm's end-effect for each corresponding update mode is shown.

3.1 Proposed cyclic voltage prediction algorithm

In order to exploit the PS-PWM characteristics along with the CHB converter structure, an algorithm for the computation of the SM's duty-cycle was constructed. Fig. 3.1 shows a qualitative scheme of how references are given to a N-cells CHB converter.

First, according to the chosen update mode, the equally shifted carriers are used to generate a pulse signal, which will trigger the c-script program when to be activated. The script also verifies the carrier index, which is enough information for the algorithm to identify which cell will be activated next. The activation cell order is known previously, and is different according to the update mode. Then, having the information of the cells input voltage, present duty-cycle and reference voltage, it is possible to estimate the average voltage to be given in the immediate interval.

Hereafter, the algorithm is going to be treated separately for each update mode, always for a 5-cell CHB converter. Still, the notation is common in all the cases.

V_s : Balancing voltage in the active sub-period.

V_q : Balancing voltage in the larger period.

V^*_{CHB} : CHB converter reference voltage.

$V_{i,live}$: Voltage of inactive cells in the subsequent sub-period.

$V_{i,average}$: Total average voltage of single inactive cell in the larger period.

$V_{a,b,c,d}$: Average voltage of the inactive cells in order of activation.

$\langle V_{pred} \rangle_{T_c/5}$: Voltage parameter, presumed to be outputted in the future by inactive cell's .

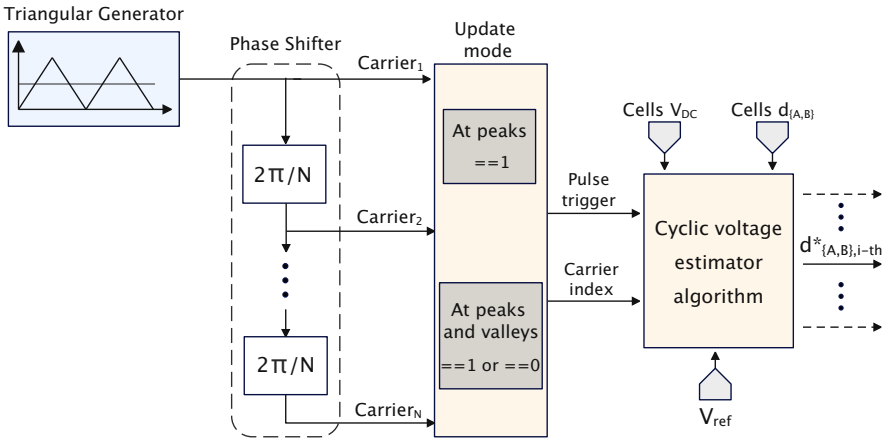


Figure 3.1: Sequential PS-PWM scheme.

3.2 Single-Update mode

For the Single-Update configuration, the duty-cycle is updated exclusively on carrier peaks or valleys.

The degree of freedom arisen from the two converter legs on each SM is exploited by assigning two different voltage references, one for each leg.

$$V_s = \langle V^*_{CHB} \rangle_{T_c/5} - \sum_{i \in \mathcal{J}} V_{i,live} \qquad \mathcal{J} = a,b,c,d \tag{3.1a}$$

$$V_q = \langle V^*_{CHB} \rangle_{T_c} - \sum_{i \in \mathcal{J}} V_{i,average} \qquad \mathcal{J} = a,b,c,d \tag{3.1b}$$

The calculation of $V_{i,live}$ and $V_{i,average}$ is based on using each cell's duty-cycle with the respective modulation function for which its carrier finds itself. As seen previously, these modulation functions changes with respect to the carrier point of update.

3.2.1 Update on carrier peaks

The main result is shown beforehand in Fig. 3.2, and construction of it is explained throughout the subsection. The boundary between the first/immediate sub-period and the next larger period pins down the division of symmetry. The same principle is true for the other update modes.

It is possible to observe the translation of both voltage references V_s and V_q at the output of a single cell by noting the division of symmetry.

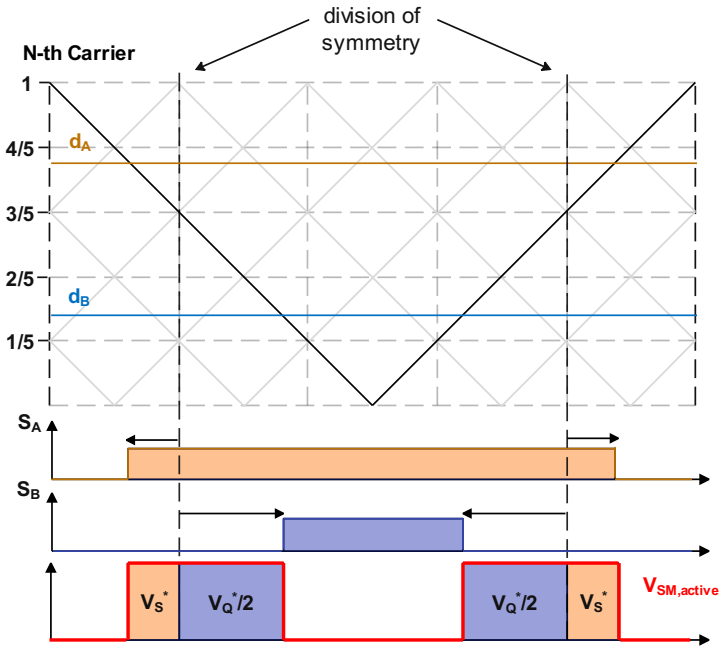


Figure 3.2: Working principle of modulation algorithm for Single-Update on carrier peaks, for a 5-cells CHB and a positive output voltage.

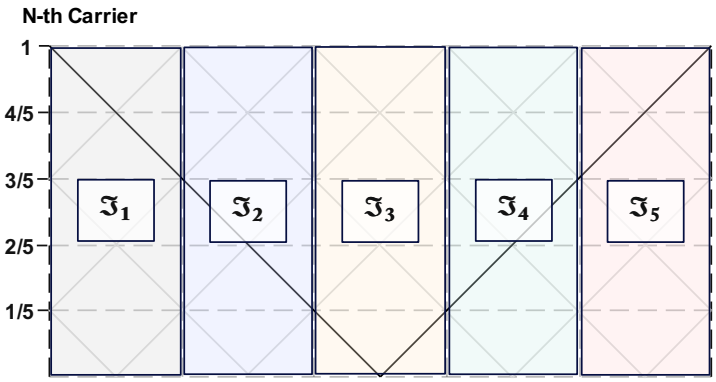


Figure 3.3: Arrangement of modulation functions for Single-Update on carrier peaks, for a 5-cell CHB.

Fig. 3.3 describes the argument presented in 2.6.1, that since the duty-cycle no longer has a full excursion between one a zero, the modulation function over the whole carrier can be divided into N piece-wise linear functions. Therefore, a function for each sub-period is retrieved in order to reconstruct the exact average voltage in the respective sub-period. These functions are listed below:

$$\mathcal{F}_1(d) = \begin{cases} \dfrac{d-3/5}{2/5} & \text{if } d \geq \dfrac{3}{5}, \\ 0 & \text{if } d < \dfrac{3}{5}. \end{cases} \tag{3.2a}$$

$$\mathcal{F}_2(d) = \begin{cases} 1 & \text{if } d \geq \dfrac{3}{5}, \\ \dfrac{d-1/5}{2/5} & \text{if } \dfrac{1}{5} \leq d < \dfrac{3}{5}, \\ 0 & \text{if } d < \dfrac{1}{5}. \end{cases} \tag{3.2b}$$

$$\mathcal{F}_3(d) = \begin{cases} 1 & \text{if } d \geq \dfrac{1}{5}, \\ \dfrac{d}{1/5} & \text{if } d < \dfrac{1}{5}. \end{cases} \tag{3.2c}$$

By symmetry:

$$\mathcal{F}_4(d) = \mathcal{F}_2(d) \tag{3.2d}$$

$$\mathcal{F}_5(d) = \mathcal{F}_1(d) \tag{3.2e}$$

Note that $\mathcal{F}_1$ corresponds to the modulation function in the first equivalent period, and is the one used for every cell when it is being activated.

Regarding the algorithm internal process, the first step is to use the duty-cycle given to the current inactive cell, and use one of the functions in 3.2 to estimate the voltage which the respective cell is giving in the immediate sub-period, as shown in Eq. 3.3.

The modulation function associated with inactive cell has to match the region representative of its carrier at that instant. Since every active cell updates at the same point relative to its own carrier in the first sub-period, it ends up that the order of the $\mathcal{F}_i$ function remains unaltered with respect to the alphabetical order regardless of the cell that is being activated. Hence, the fixed expression of Eq. 3.3.

On the other hand, what changes with the activation index is the assignment of a given SM to the respective voltage label. For example:

$$\text{If active cell is SM}_3 \begin{cases} V_a = V_4 \\ V_b = V_5 \\ V_c = V_1 \\ V_d = V_2 \end{cases}$$

The voltage of the inactive cells in the immediate sub-interval are given in Eq. 3.3.

$$V_a = V_{DC,a} \cdot (\mathcal{F}_2(d_{A,a,old}) - \mathcal{F}_2(d_{B,a,old})) \tag{3.3a}$$
$$V_b = V_{DC,b} \cdot (\mathcal{F}_3(d_{A,b,old}) - \mathcal{F}_3(d_{B,b,old})) \tag{3.3b}$$
$$V_c = V_{DC,c} \cdot (\mathcal{F}_4(d_{A,c,old}) - \mathcal{F}_4(d_{B,c,old})) \tag{3.3c}$$
$$V_d = V_{DC,d} \cdot (\mathcal{F}_5(d_{A,d,old}) - \mathcal{F}_5(d_{B,d,old})) \tag{3.3d}$$

At this point, the balancing reference voltage for the sub-period can be calculated.

$$V_s = V^*_{CHB} - (V_a + V_b + V_c + V_d)$$

It is important to remark that, in Single-Update mode, due to the intrinsic control structure, V_s is not only outputted by the active cell in the first sub-period but also in the last one. In other words, a duty-cycle reference pair encounters the carrier signal ramp twice in the whole carrier period. By symmetry, V_s is reflected in the last sub-period. For a more clear understanding with this regard, the Fig. 3.4 may be noted.

The remaining intermediate intervals within the carrier period is left to be assigned by the complementary voltage reference V_q. This reference contains both voltages that are yet to be assigned and of voltages that were given in the last time that these cells were updated.

The parameter here is the choice of the total reference voltage which is presumed that the inactive cells will output at their next update, namely V_{pred}. As a simple and safe assumption, it was defined to be the equally shared total reference.

$$V_{pred} = V^*_{CHB}/5$$

Once V_{pred} is defined, the next step is to retrieve the correspondent duty-cycle, $d_x, pred$, as shown in Table 3.1. Here the duty-cycle function is based on the case study done in the

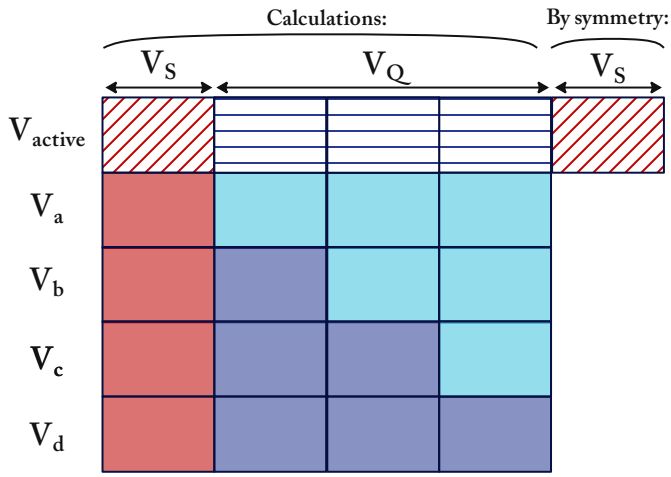


Figure 3.4: Calculation blueprint of voltage references. Plain red spaces represent direct voltage computation based on last given duty-cycle; dark blue represents already defined voltage value; light blue represents the voltage values which are yet to be defined.

modulation analysis section 2.6.1.

	Expression	
Duty-cycle	$V^*_{CHB} \geq 0$	$V^*_{CHB} < 0$
$d_{A,pred}$	$\frac{3}{5} + \frac{2}{5}\frac{V_{pred}}{V_{DC}}$	$\frac{3}{5} + \frac{3}{5}\frac{V_{pred}}{V_{DC}}$
$d_{B,pred}$	$\frac{3}{5} - \frac{3}{5}\frac{V_{pred}}{V_{DC}}$	$\frac{3}{5} - \frac{2}{5}\frac{V_{pred}}{V_{DC}}$

Table 3.1: Function for duty-cycle prediction, whereas $V_{pred} = V^*_{CHB}/5$.

Finally, expressions of the estimated voltages given by the inactive cells are shown in Eq. 3.4, and the complementary voltage reference shown in 3.5.

$$\begin{aligned} V_{a,average} &= \big[V_{DC,a}\cdot\big(\mathcal{F}_1(d_{A,a,pred})-\mathcal{F}_1(d_{B,a,pred})\big) \\ &\quad + V_{DC,a}\cdot\big(\mathcal{F}_2(d_{A,a,pred})-\mathcal{F}_2(d_{B,a,pred})\big) \\ &\quad + V_{DC,a}\cdot\big(\mathcal{F}_3(d_{A,a,pred})-\mathcal{F}_3(d_{B,a,pred})\big)\big]/3 \end{aligned} \tag{3.4a}$$

$$\begin{aligned} V_{b,average} &= \big[V_{DC,b}\cdot\big(\mathcal{F}_5(d_{A,b,old})-\mathcal{F}_5(d_{B,b,old})\big) \\ &\quad + V_{DC,b}\cdot\big(\mathcal{F}_1(d_{A,b,pred})-\mathcal{F}_1(d_{B,b,pred})\big) \\ &\quad + V_{DC,b}\cdot\big(\mathcal{F}_2(d_{A,b,pred})-\mathcal{F}_2(d_{B,b,pred})\big)\big]/3 \end{aligned} \tag{3.4b}$$

$$\begin{aligned} V_{c,average} &= \big[V_{DC,c}\cdot\big(\mathcal{F}_4(d_{A,c,old})-\mathcal{F}_4(d_{B,c,old})\big) \\ &\quad + V_{DC,c}\cdot\big(\mathcal{F}_5(d_{A,c,old})-\mathcal{F}_5(d_{B,c,old})\big) \\ &\quad + V_{DC,c}\cdot\big(\mathcal{F}_1(d_{A,c,pred})-\mathcal{F}_1(d_{B,c,pred})\big)\big]/3 \end{aligned} \tag{3.4c}$$

$$\begin{aligned} V_{d,average} &= \big[V_{DC,d}\cdot\big(\mathcal{F}_3(d_{A,d,old})-\mathcal{F}_3(d_{B,d,old})\big) \\ &\quad + V_{DC,d}\cdot\big(\mathcal{F}_4(d_{A,d,old})-\mathcal{F}_4(d_{B,d,old})\big) \\ &\quad + V_{DC,d}\cdot\big(\mathcal{F}_5(d_{A,d,old})-\mathcal{F}_5(d_{B,d,old})\big)\big]/3 \end{aligned} \tag{3.4d}$$

$$V_q = V^*_{CHB} - \big(V_{a,average} + V_{b,average} + V_{c,average} + V_{d,average}\big) \tag{3.5}$$

Table 3.2 depicts the final computation of the duty-cycle for the active cell. The references V_s and V_q are given, and depending on their condition, d^*_A and d^*_B are calculated and then sent to the active cell, which will output the references exactly in their respective periods, if no saturation occurs.

	Expression			
	$V_s \geq 0$		$V_s < 0$	
Duty-cycle	$V_q \geq 0$	$V_q < 0$	$V_q \leq 0$	$V_q > 0$
d^*_A	$\frac{3}{5}+\frac{2}{5}\frac{V_s}{V_{DC}}$	$\frac{3}{5}+\frac{2}{5}\frac{V_s}{V_{DC}}$	$\frac{3}{5}+\frac{3}{5}\frac{V_q}{V_{DC}}$	$\frac{3}{5}$
d^*_B	$\frac{3}{5}-\frac{3}{5}\frac{V_q}{V_{DC}}$	$\frac{3}{5}$	$\frac{3}{5}-\frac{2}{5}\frac{V_s}{V_{DC}}$	$\frac{3}{5}-\frac{2}{5}\frac{V_s}{V_{DC}}$

Table 3.2: Final active cell modulation function given both voltage references, for Single-Update mode on carrier peaks.

It is also important to note the assignment of priority when conditions are in contrast. When

V_s and V_q have opposite signs, the later will be dropped and set to zero, so that at least the average in the immediate equivalent interval is guaranteed.

After having defined the modulation function, it is possible to observe the resulting configuration of the degree of freedom. That is, the common-mode duty-cycle d_{CM}, becomes restricted under a possible range of values, as shown in Fig. 3.5.

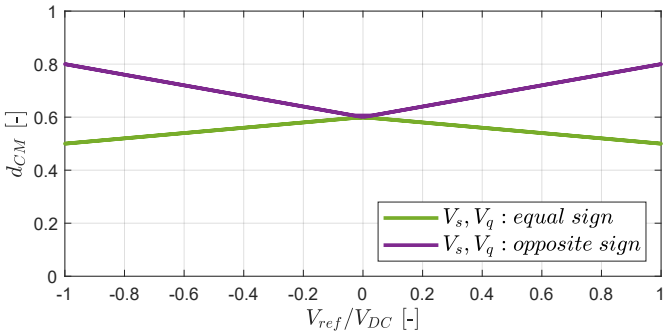


Figure 3.5: Resulting possible excursion of degree of freedom, for both positive and negative voltage references.

Finally, Fig. 3.6 displays the scope of the duty-cycle and common-mode for a sinusoidal reference using the Sequential Algorithm, from where is possible to observe how the common-mode is not fixed during modulation. In fact, the d_{CM} trend is not identical between the sub-modules but changes slightly, but always within the boundaries shown in Fig. 3.5.

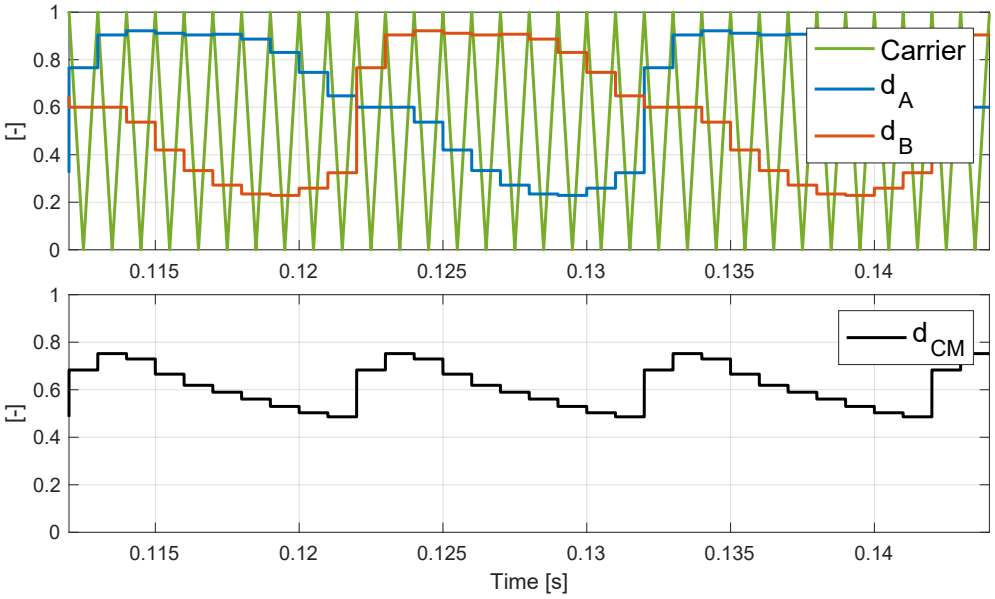


Figure 3.6: Duty-cycles and common-mode from a single cell using the Sequential Algorithm on Single-Update on carrier peaks, with $M_{idx} = 0.65$.

3.2.2 Update on carrier valleys

The algorithm was not constructed separately for the case of Single-Update mode on carrier valleys because it was considered redundant when one case in Single-Update was already assembled and the Double-Update mode uses modulation functions for Single-Update on both carrier peaks and valleys.

The same concept from the Single-Update modulation on carrier peaks is implemented for the modulation on carrier valleys, with a reciprocal arrangement in most of the time. This can be seen, for instance, in Fig. 3.7, which presents the regions of each piece-wise linear function partition within the carrier signal.

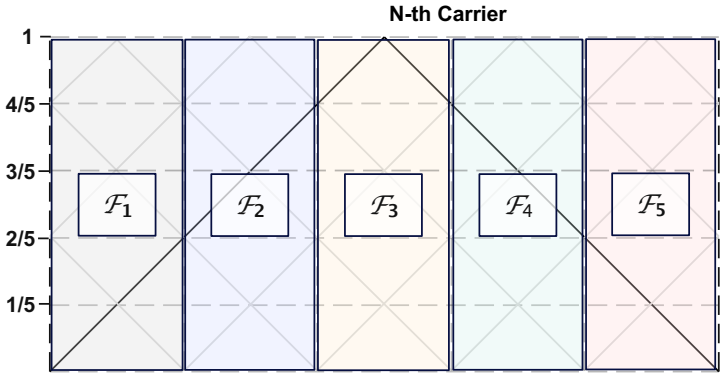


Figure 3.7: Arrangement of modulation functions for Single-Update on carrier valleys, for a 5-cell CHB.

The modulation functions are then shown in Eq. 3.6.

$$\mathcal{F}_1(d) = \begin{cases} 1 & \text{if } d \geq \frac{2}{5}, \\ \frac{d}{2/5} & \text{if } d < \frac{2}{5}. \end{cases} \tag{3.6a}$$

$$\mathcal{F}_2(d) = \begin{cases} 1 & \text{if } d \geq \frac{4}{5}, \\ \frac{d-2/5}{2/5} & \text{if } \frac{2}{5} \leq d < \frac{4}{5}, \\ 0 & \text{if } d < \frac{2}{5}. \end{cases} \tag{3.6b}$$

$$\mathcal{F}_3(d) = \begin{cases} \frac{d-4/5}{1/5} & \text{if } d > \frac{4}{5}, \\ 0 & \text{if } d \leq \frac{4}{5}. \end{cases} \tag{3.6c}$$

By symmetry:

$$\mathcal{F}_4(d) = \mathcal{F}_2(d) \tag{3.6d}$$

$$\mathcal{F}_5(d) = \mathcal{F}_1(d) \tag{3.6e}$$

For instance, the point of reference is equivalent for a carrier value of $1/5$. As shown in Table 3.4, it is important to note the switch in the leading active sub-module leg: for a positive voltage reference, d_B is modulated by V_s, d_A is modulated by V_q. It works the other way around given a negative voltage reference.

Table 3.3 shows the expressions for computation of the presumed duty-cycles of the inactive cells.

	Expression	
Duty-cycle	$V^*_{CHB} \geq 0$	$V^*_{CHB} < 0$
$d_{A,pred}$	$\frac{2}{5} + \frac{3}{5}\frac{V_{pred}}{V_{DC}}$	$\frac{2}{5} + \frac{2}{5}\frac{V_{pred}}{V_{DC}}$
$d_{B,pred}$	$\frac{2}{5} - \frac{2}{5}\frac{V_{pred}}{V_{DC}}$	$\frac{2}{5} - \frac{3}{5}\frac{V_{pred}}{V_{DC}}$

Table 3.3: Function for duty-cycle prediction, whereas $V_{pred} = V^*_{CHB}/5$.

Moreover, the computation of the voltage references V_s and V_q have the same exact expression shown in the case of update on carrier peaks. Then, the active duty-cycles are calculated according to the conditions expressed in Table 3.4.

	Expression			
	$V_s \geq 0$		$V_s < 0$	
Duty-cycle	$V_q \geq 0$	$V_q < 0$	$V_q \leq 0$	$V_q > 0$
d_A^*	$\frac{2}{5} + \frac{3}{5}\frac{V_q}{V_{DC}}$	$\frac{2}{5}$	$\frac{2}{5} + \frac{2}{5}\frac{V_s}{V_{DC}}$	$\frac{2}{5} + \frac{2}{5}\frac{V_s}{V_{DC}}$
d_B^*	$\frac{2}{5} - \frac{2}{5}\frac{V_s}{V_{DC}}$	$\frac{2}{5} - \frac{2}{5}\frac{V_s}{V_{DC}}$	$\frac{2}{5} - \frac{3}{5}\frac{V_q}{V_{DC}}$	$\frac{2}{5}$

Table 3.4: Final active cell modulation function given both voltage references, Single-Update on carrier valleys.

In a reciprocal way to the Single-Update on carrier peaks, the excursion of the degree of freedom d_{CM} for the update on carrier valleys was found to vary in the range of [0.2, 0.5], as shown in Fig. 3.8.

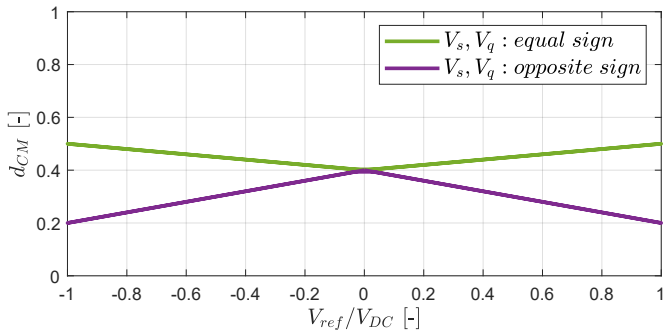


Figure 3.8: Resulting possible excursion of degree of freedom, for both positive and negative voltage references.

Finally, Fig. 3.9 depicts the modulation end-effect of the Single-Update on carrier valleys. It is important to note that the sub-module leg that controls V_s and V_q voltages change.

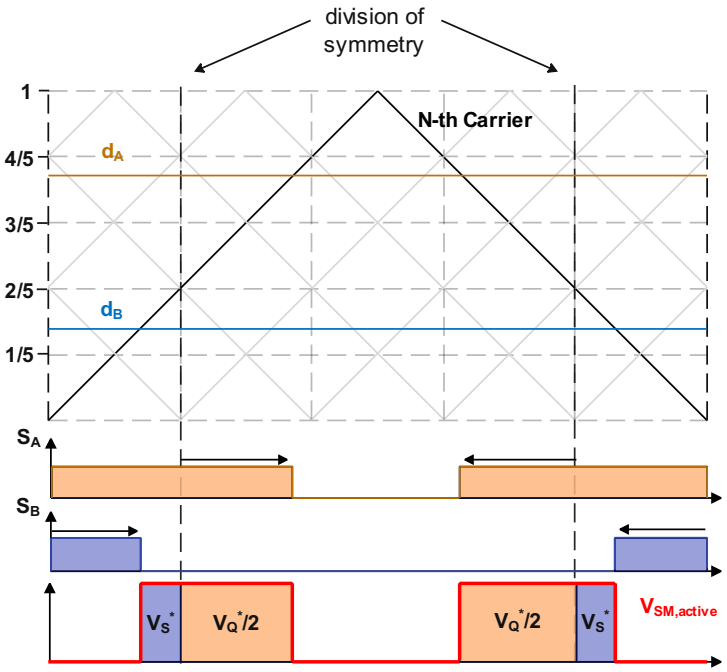


Figure 3.9: Working principle of modulation algorithm for Single-Update on carrier valleys, for a 5-cells CHB and positive output voltage.

3.3 Double-Update mode

In the case of Double-Update mode, the duty-cycle update occurs both on carrier peaks and valleys. Fig. 2.10 shows this concept precisely. For this reason, the equivalent period also halves in comparison of the Single-Update mode, being $T_{eq} = T_c/10$.

Furthermore, both modulation functions of Single-Update on carrier peaks and valleys are used. Now a single carrier period contains double the amount of sub-functions for voltage estimation, as it is depicted on Fig. 3.10 and reported for completeness in appendix C. In this case, the use of each set of sub-functions is alternated.

In order to have a more visual understanding of the prediction scheme of voltage estimation, the Fig. 3.11 may be used.

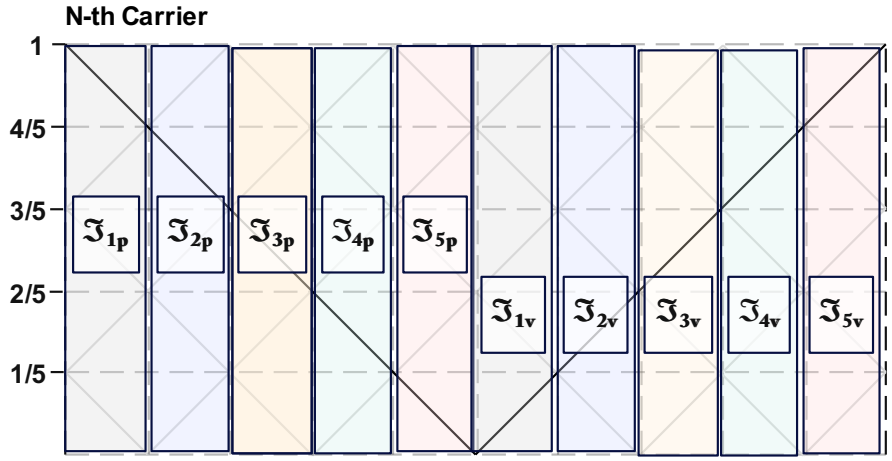


Figure 3.10: Arrangement of modulation functions for Double-Update, for a 5-cell CHB.

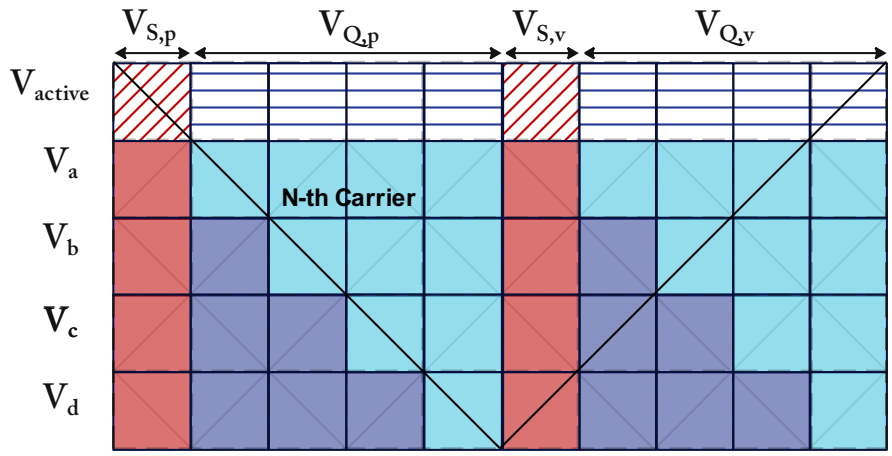


Figure 3.11: Conceptual scheme for computation of voltage references V_s and V_q for Double-Update mode. Plain red spaces represent direct voltage computation based on last given duty-cycle; dark blue represents already defined voltage values; light blue represents the voltage values which are yet to be defined.

The interesting point is that, differently from the Single-Update mode, V_s is not reflected in the last sub-period, allowing V_q to be directly computed. Hence, Eq. 3.7 is obtained, where V_q was chosen to be simply the total voltage reference equally shared between the cells.

However, this is only a safe choice, since the value of V_q in this case is only an estimation of what the other cells may give when they are not on their active sub-period. As it is going to be demonstrated in the results section 5, this value highly impacts the voltage sum which will have to be compensated by the active cell.

$$V_s = V^*_{CHB} - \sum_{i \in \mathcal{J}} V_{cells,live} \quad \mathcal{J} = a,b,c,d \tag{3.7a}$$

$$V_q = V^*_{CHB}/5 \tag{3.7b}$$

A consequence of the modulation process is the new value of duty-cycle that separates the active and complementary legs, which are $4/5$ and $1/5$ for update on carrier peaks and valleys, respectively. This is shown in Fig. 3.12.

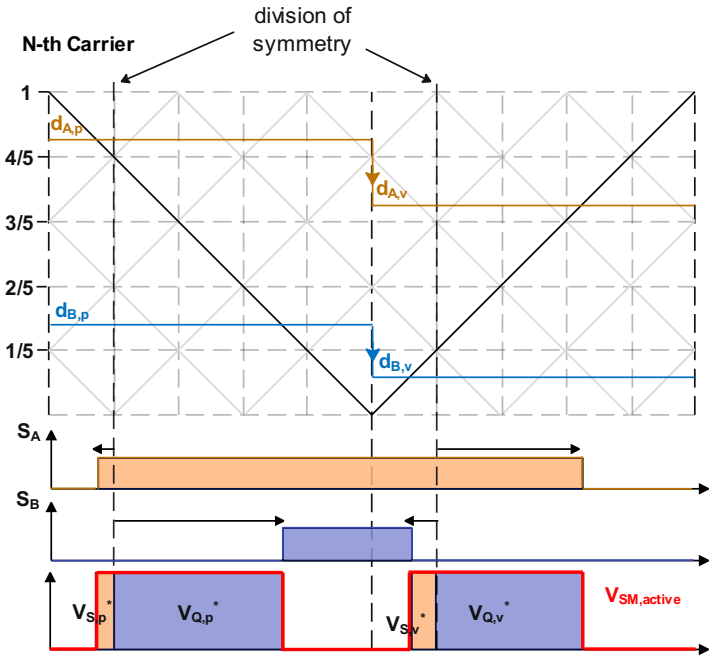


Figure 3.12: Working principle of modulation algorithm for Double-Update, for a 5-cells CHB and positive output voltage.

In summary, Fig. 3.13 shows a qualitative trend of the duty-cycles for when Sequential Algorithm is used with Double-Update modes. A sinusoidal waveform reference was given in that case.

It is worth noting that there is a bouncing behavior of the duty-cycle due to the alternating use of modulation functions between the update on carrier peaks and valleys, and consequently the same effect is seen in d_{CM}. The common-mode in this case will vary within the union of the ranges in the individual update cases, that is, between 0.2 and 0.8.

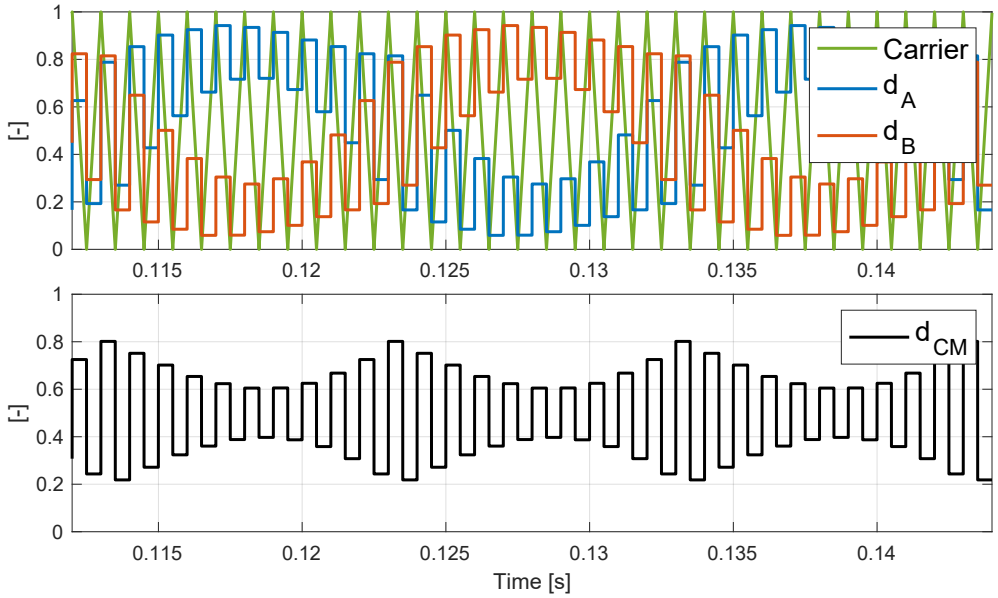


Figure 3.13: Duty-cycles and common-mode from a single cell using the Sequential Algorithm on Double-Update, for a $M_{idx} = 0.65$.

Note that these jumps do not add additional switching transitions. Indeed, similar to any other standard technique applied to a full-bridge, each leg will only have one turn-on and one turn-off transition for each carrier period. On the other hand, the output voltage, $v_{cell} = v_{AN} - v_{BN}$, will have 2 turn-on and 2 turn-off transitions for each carrier period.

3.4 Secondary modulation functions

Secondary modulations functions are necessary in order to evaluate the performance of the proposed algorithm. One of them, the standard unipolar PS-PWM will be used in the same update condition as the Sequential PS-PWM Algorithm. While the Multisampled modulation function is useful not for a direct comparison but just to highlight the effect of the condition of being able to update multiple cells multiple times within the carrier period, giving a simultaneous reference to all the cells rather than in a sequential manner.

3.4.1 Standard unipolar PS-PWM

The PS-PWM technique with unipolar modulation is the main function used in comparison with the cyclic voltage algorithm. It consists of the same model and is used under the same limiting factor of updating the duty-cycle of each SM sequentially, because each SM will only update at the characteristic point of its carrier.

The scheme of this method is shown in Fig. 3.14, where a balancing algorithm does not compute two voltage references but only one reference is given to the SMs, which is the

equally shared total voltage reference, $V^*_{CHB}/5$.

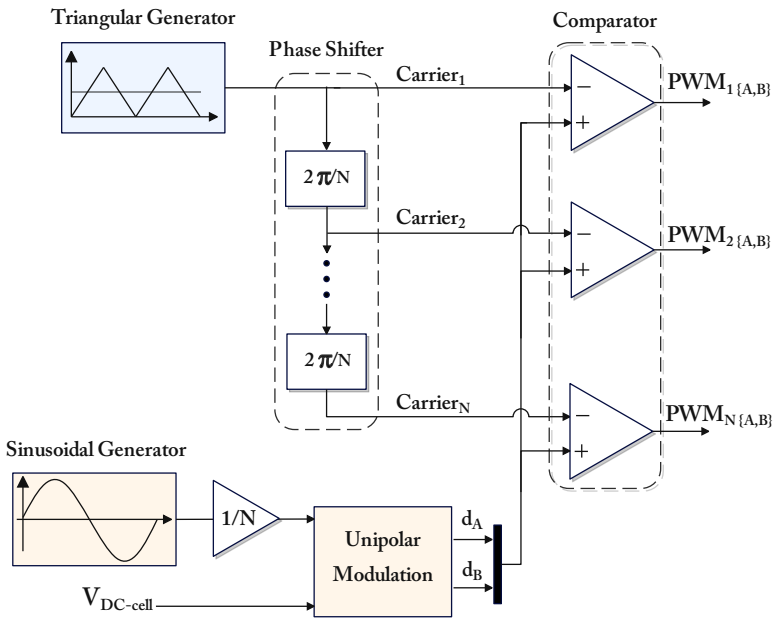


Figure 3.14: Standard unipolar PS-PWM modulation scheme. Again, only one pair of duty-cycles is updated on every equivalent period.

The standard unipolar PS-PWM is characterized by having a constant common-mode component of 0.5, and a symmetrical PWM. Hence, the output double-pulse voltage of the single cell will be centered in the carrier period.

The modulation function boils down to Eq. 3.8.

$$d^*_A = \frac{1}{2} + \frac{1}{2}\frac{V_{ref,cell}}{V_{DC,cell}} \tag{3.8a}$$

$$d^*_B = \frac{1}{2} - \frac{1}{2}\frac{V_{ref,cell}}{V_{DC,cell}} \tag{3.8b}$$

3.4.2 Multisampled PS-PWM

The Multisampled PS-PWM is a competitive operating mode if the crucial limiting factor is neglected. That is, when it is possible to update the duty-cycle into the SMs multiple times within a carrier period.

This modulation technique lies between the natural and regular sampling. Its working principle can be visualized on Fig. 3.15. It has an update period on each carrier of $T_{up} = T_c/(2 \cdot \text{rsr})$,

where rsr is defined as the re-sampling ratio. It is important to note that this is the number of samples per switch edge, rather than per pulse; hence the factor of two.

Other works have demonstrated that this approach results in the decrease of sampling delay [12], [13]. Thus, it becomes a relevant case of comparison for highlighting the limiting factor.

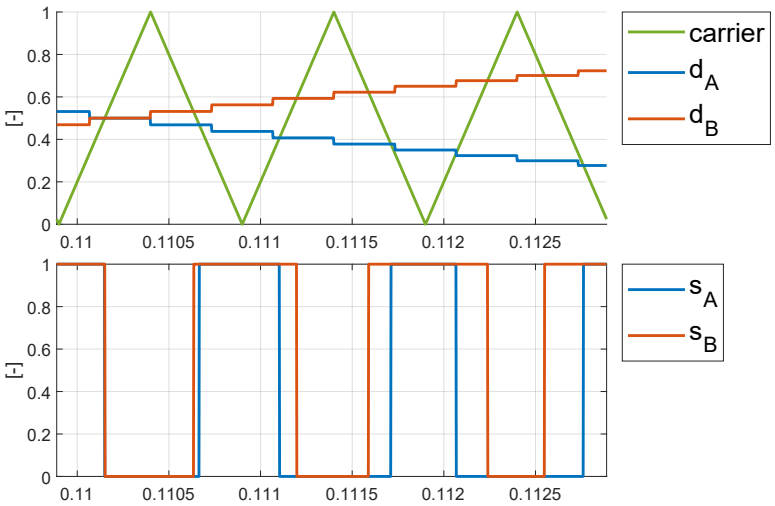
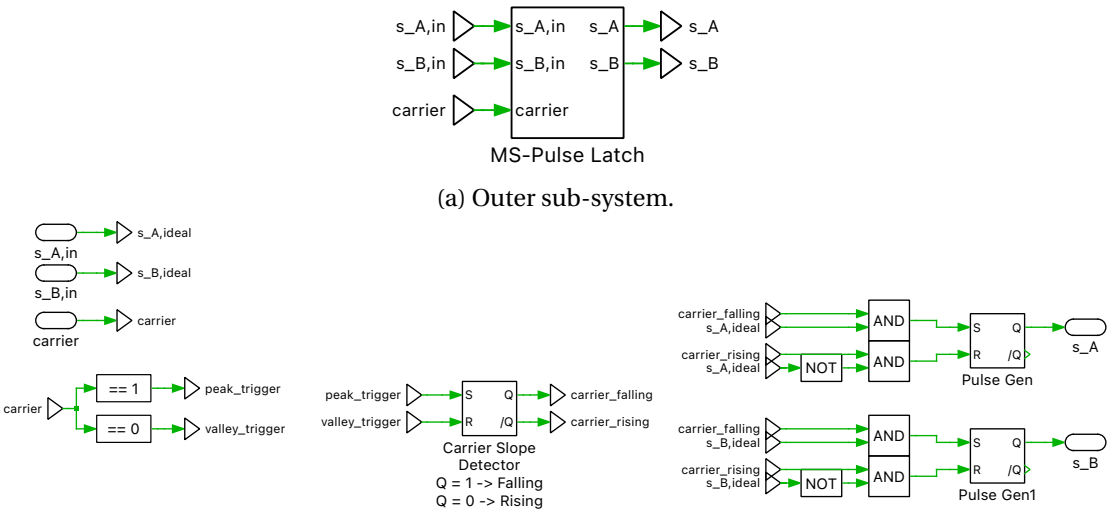


Figure 3.15: Multisampled working principle, operating on Single-Update mode with rsr= 3

However, without further modification, the modulation signal will often vertically intersect the carrier signal, creating a circumstance known as vertical crossing. When not taken into account, this generates additional pulse signals, inducing high frequency harmonics. One mitigation found for this was to allow only one rising edge per period fired by the first intersection with the carrier, so as to guarantee the latch avoidance. Fig. 3.16 shows the PLECS block scheme used to perform this task.



(a) Outer sub-system.

(b) Inner-block schematic.

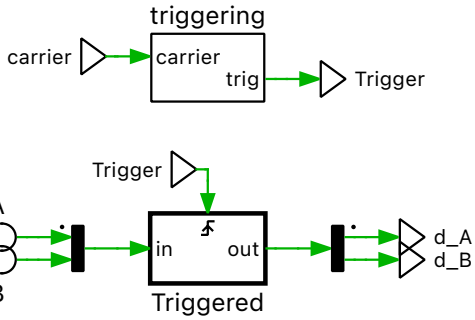
Figure 3.16: PLECS implementation of latch avoidance function.

It is important to highlight the circumstances on which the proposed Sequential PS-PWM Algorithm works and is competitive. In this sense, the affirmation is accurate when the controller updates only one single cell at a step; different when there is the possibility to update many SMs in a Multisampled fashion. Hence, it is only fair to compare control strategies that are bounded by this limiting factor. For this reason, the standard unipolar modulation method was chosen to be directly confronted with the proposed Sequential Algorithm. Following the result comparison of the modulation strategies, the Multisampled technique will be demonstrated for the sake of completeness, showing that a better result may be reached only at the cost of lifting certain constraints.

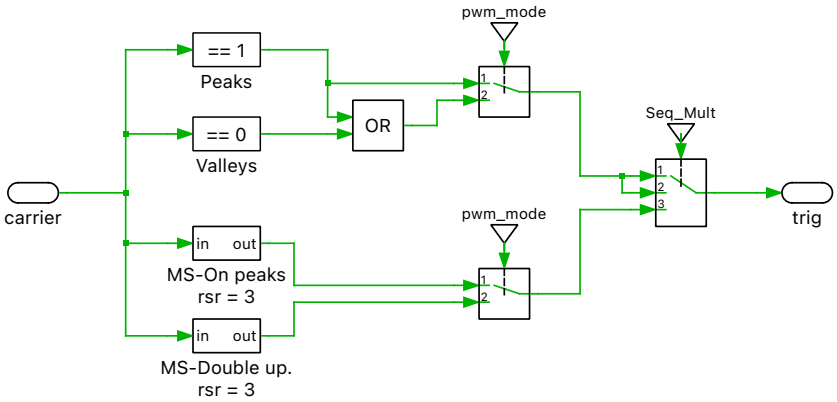
3.4.3 Cell mechanism for duty-cycle update

Regarding with the internal mechanism of duty-cycle update on a single cell, Fig. 3.17 shows the PLECS schematic of the function blocks engaged on this task. Every SM has these function blocks, where its carrier generates a trigger impulse signal which is then used to sample the value of duty-cycle that comes from the algorithm and that is then used for the commutation of the switching signals.

Note in Fig. 3.17 that the both Sequential and unipolar modulation techniques use the same upper triggering configuration, while the Multisampled technique is supported by the lower triggering route.



(a) Outer sub-system.



(b) Triggering inner-block schematic.

Figure 3.17: Triggering mechanism within cell.

4 Closed-loop model

In order to effectively make use of a converter, it has to be closed in a loop with some sort of connection that, according to Thévenin's theory, may always be represented by an equivalent circuit. With that, it becomes essential to have a current control, which is the state variable resulting from the interaction between a voltage source converter and an equivalent inductive load.

4.1 Model discretization

In practice, there are many practical steps in the control of a converter; output signals have to be sampled and control actions are synchronized by an internal oscillator, or clock, which counts time steps. In order to model a converter and the discrete nature of theses processes in a computer, the responses from the converter coupling with a circuit are obtained by solving a discretized equivalent circuit. The circuit is formed essentially by the CHB converter output, and an RLE-load. An example is depicted in Fig. 4.1.

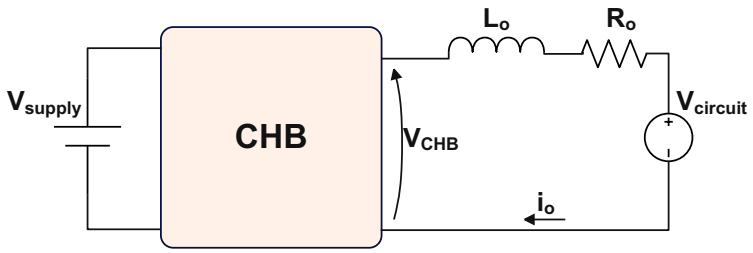


Figure 4.1: Generic one-phase equivalent circuit.

First, the continuous-time response is derived. Applying Kirchhoff's voltage law:

$$V(t) = R\,i(t) + L\frac{di(t)}{dt} + e(t) \tag{4.1a}$$

$$i(t) = (V(t) - e(t))\frac{1}{R}(1 - e^{-t/\tau}) + i_o e^{-t/\tau} \tag{4.1b}$$

With $\tau = L/R$ being the circuit time constant.

The current response from the circuit can more easily discretized with a linear approximation. It consists in linearizing an exponential function within a fixed time step, which is set to be equal to one equivalent output period T_{eq}, that varies according to the update mode. Thus, 4.2 is obtained.

$$i_{k+1} = (V_k - e_k)\frac{1}{R}(1 - e^{-T_{eq}/\tau}) + i_k e^{-T_{eq}/\tau} \tag{4.2a}$$

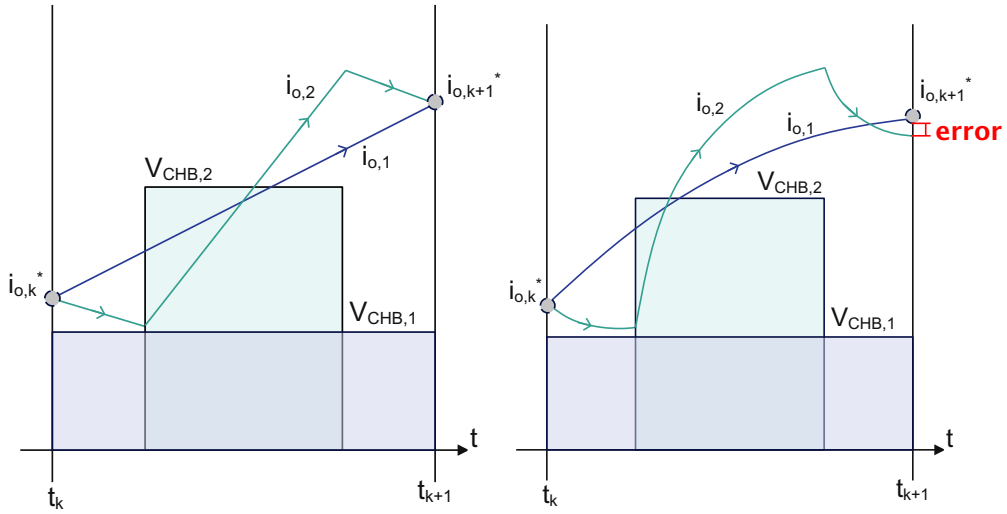
$$i_{k+1} = (V_k - e_k)b + i_k a \tag{4.2b}$$

Where the current coefficients a and b are time-invariant and depend purely on the load parameters, once the update mode is fixed.

$$a = 1 - e^{-T_{eq}/\tau} \tag{4.3a}$$

$$b = \frac{1}{R}(1 - e^{-T_{eq}/\tau}) \tag{4.3b}$$

However, such approximation relies on the assumption that the circuit time constant is much smaller than the discretization step. Hence, the current expression becomes approximately linear and the average applied voltage yields the same current change as the instantaneous applied voltage, as shown in Fig. 4.2.



(a) $\tau = \frac{L}{R} \gg T_{eq}$ (b) $\tau = \frac{L}{R} \approx T_{eq}$

Figure 4.2: Current response in case assumption is met or not.

For this reason, the load parameters were properly chosen, as shown in Table 4.1. Even with

largest equivalent period, for Single-Update mode, the linear approximation is still found to hold true, while $\frac{\tau}{T_c/5} = 2500 \gg 1$.

Parameter	Value	Unit
R_{load}	20	mΩ
L_{load}	10	mH
T_c	1	ms

Table 4.1: Simulation load parameters.

4.2 Two-step current MPC

In order to promptly know which voltage should the CHB converter output at every time step, it is necessary to implement a two-step current MPC. This is now possible with the use of Eq. 4.2. This minimum step horizon is needed to overcome the one-step delay introduced by the converter and to model the current in the following step.

Firstly, at moment $t = k$ a current reference i^*_{k+2} is given, while i_k is the current from the previous time step delayed by $T_{sampling}$, delineating the latest current measurement. Until a new reference voltage v_{k+1}, in average, is given, there will be another time delay of one sampling time. Therefore, in order for the circuit current to follow the reference in one step, a two-step prediction algorithm is necessary, that is, a current MPC with receding horizon with length of two steps. The idea can be visualized with Fig. 4.3.

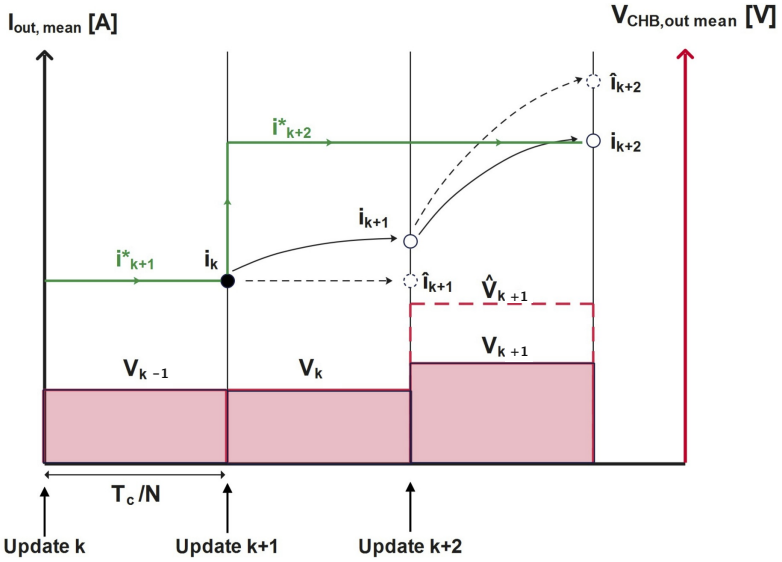


Figure 4.3: Two-step prediction algorithm scheme.

Equation 4.2 is used to compute the voltage reference, that is then sent to the CHB modulation

algorithm. Coefficients a, b are constant, i_{k+1} is computed from 4.2 and e_{k+1} can be predicted depending on the type of load.

$$v_{k+1} = \frac{i^*_{k+2} - a \cdot i_{k+1}}{b} + e_{k+1} \tag{4.4}$$

Finally, Fig. 4.4 displays the schematic of the current MPC implementation. Circuit equations were set in a c-script, and the CHB voltage reference equals the predicted voltage v_{k+1} delayed by one time step.

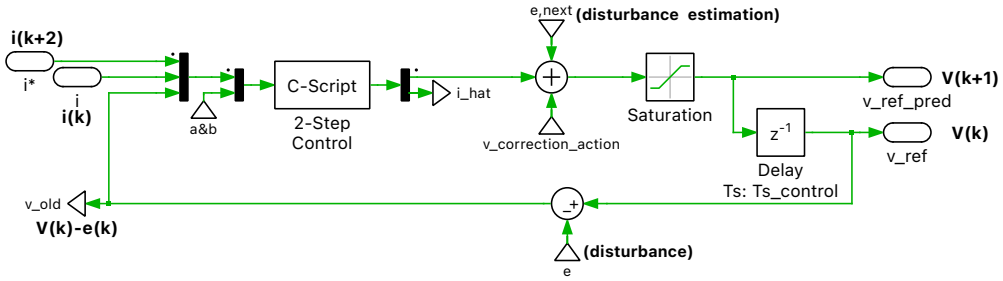


Figure 4.4: PLECS schematic of current two-step predictor.

4.3 Current control in dq-frame

It was also thought to implement the current MPC in the dq-frame in order to have an alternative control than that in the regular abc-frame.

For this purpose, Park transform was used to obtain synchronous two-phase circuit equations equivalent to the one defined in stationary three-phase reference, B.3.

$$\frac{di_d}{dt} = \frac{1}{L}\left(V_d - V_{g,d} - Ri_d + jwLi_q\right) \tag{4.5a}$$

$$\frac{di_q}{dt} = \frac{1}{L}\left(V_q - V_{g,q} - Ri_q - jwLi_d\right) \tag{4.5b}$$

The cross-coupling terms between the axis are a result from the reference transformation. Then, a state model can be identified in the continuous time-domain.

$$\dot{x} = Ax + B(V - V_g) \tag{4.6}$$

$$x = \begin{bmatrix} i_d \\ i_q \end{bmatrix} \qquad V = \begin{bmatrix} V_{CHB,d} \\ V_{CHB,q} \end{bmatrix} \qquad V_g = \begin{bmatrix} V_{g,d} \\ V_{g,q} \end{bmatrix}$$

$$A = \begin{bmatrix} -R/L & w \\ -w & -R/L \end{bmatrix} \qquad B = \begin{bmatrix} 1/L & 0 \\ 0 & 1/L \end{bmatrix}$$

Equation 4.6 can be discretized and approximated. Matrices A and B remain unvaried.

$$\frac{x_{k+1} - x_k}{T_{eq}} = A\left(\frac{x_{k+1} + x_k}{2}\right) + B\left(V_k - V_{g,k}\right) \tag{4.7}$$

$$x_{k+1} = \left[\left(I - \frac{T_{eq}}{2}A\right)^{-1}\left(I + \frac{T_{eq}}{2}A\right)\right] x_k + \left[\left(I - \frac{T_{eq}}{2}A\right)^{-1} T_{eq}B\right]\left(V_k - V_{g,k}\right) \tag{4.8a}$$

$$x_{k+1} = M_i x_k + M_v\left(V_k - V_{g,k}\right) \tag{4.8b}$$

Where I is a 2x2 identity matrix. The matrices M_i and M_v also have 2x2 size, and its coefficients were obtained using symbolic expression simplification in Matlab. The anti-diagonal entries $M_v^{1,2}$ and $M_v^{2,1}$ can be discarded since cross-coupling does not occur with the voltage terms. Yet, there are in total 6 coefficients that are essential for the realization of the current control in the dq-frame.

Following the same MPC concept presented previously, Eq. 4.9 shows how both components of the voltage reference are calculated. The control is then implemented in a c-script.

$$V_{k+1} = M_v^{-1}\left(x_{k+2} - M_i x_{k+1}\right) + V_{g,k+1} \tag{4.9}$$

5 Results

This chapter presents discusses simulation results found using the modulation strategies in different update configurations.

5.1 Open-loop results

In this section, results from the functioning of the CHB with the respective modulation functions are presented. Having a user-defined carrier frequency and voltage reference, the CHB output is measured both instantaneously and in the equivalent period average.

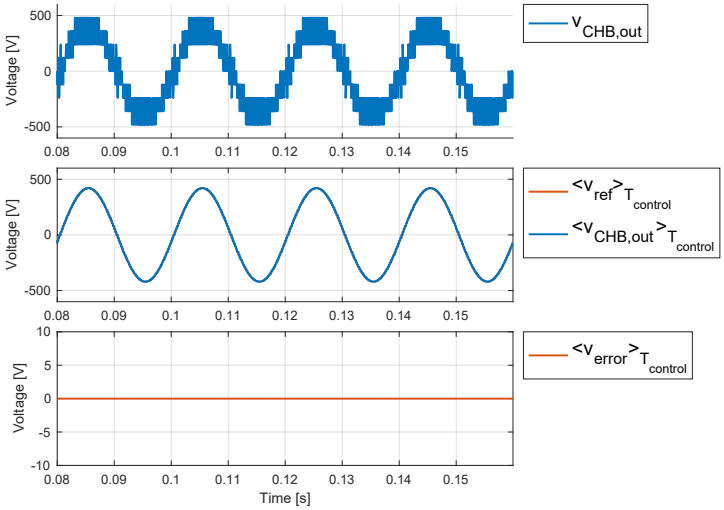
For that, the parameters presented in Table 5.1 were chosen. The switching frequency in CHB converters is generally not elevated since the equivalent frequency at the output is multiplied by the number of cells in a single branch.

Parameter	Value	Unit
f_c	1	kHz
$V_{DC,eq}$	600	V

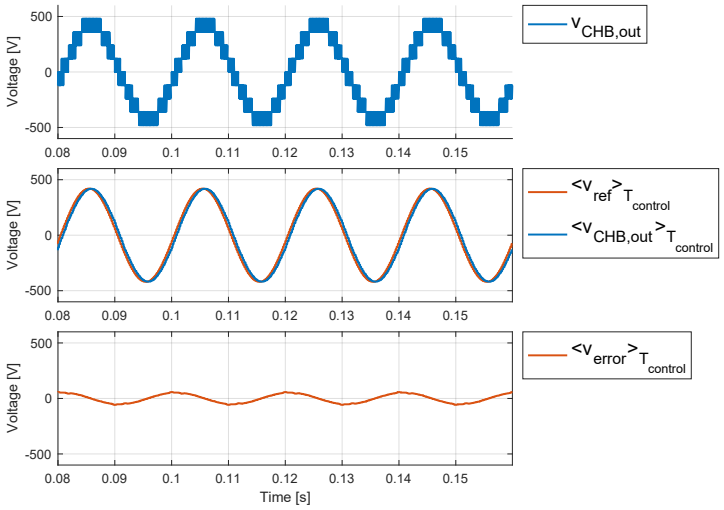
Table 5.1: User-defined CHB converter parameters.

It becomes important to bare in mind that having defined an equivalent dc voltage at the input, the saturation voltage level for every SM can be computed as $V_{DC,eq}/N$. The transient dynamics of the input capacitors was not considered, thus leading directly to an equally spread input voltage. In this case, a single SM may provide an output voltage in the range [-120, +120] V. This consideration is relevant since it defines a limit of who much a cell can compensate for the others, given a reference to follow.

5.1.1 Single-Update on carrier peaks



(a) Sequential Algorithm.



(b) Unipolar modulation.

Figure 5.1: CHB voltage output for $M_{idx} = 0.7$ and $T_{control} = T_c/5$.

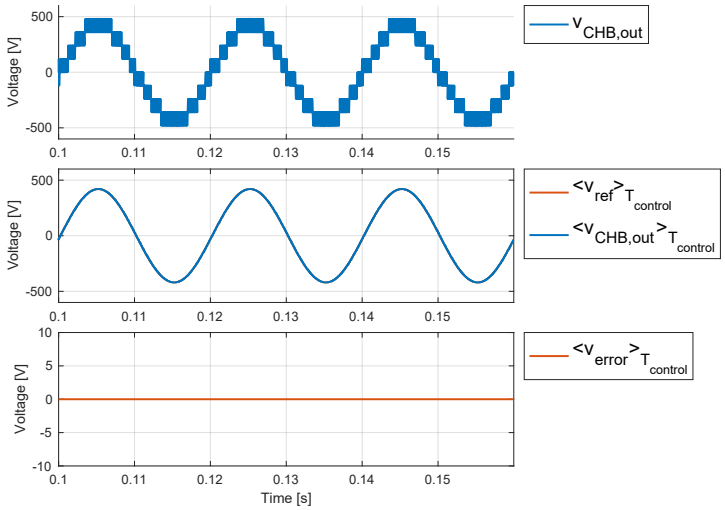
The result on Fig. 5.1 demonstrates the effectiveness of the Sequential PS-PWM Algorithm compared to when a standard unipolar modulation function is used instead. The later is capable of tracking the voltage reference only with a delay of two samples of equivalent period, yet, with non-negligible errors. On the other hand, the Sequential Algorithm mechanism works in a way that the voltage reference is efficiently provided at the analysed average period.

Naturally, it is also desired that every signal at the output approximates a sinusoidal waveform as close as possible so that most of a wave's energy content is at the grid's nominal frequency. When the instantaneous voltage is observed at the uppermost plot, it is possible to foresee that

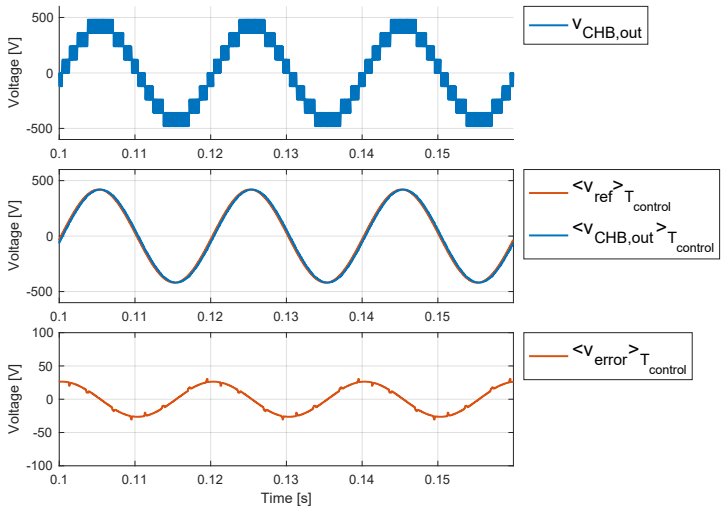
the Sequential Algorithm, despite having null average error, recedes from having a sinusoidal waveform when compared to the standard unipolar modulation function result. This effect will be better treated in the drawback subsection.

5.1.2 Double-Update

Similar results are found on Double-Update operation mode, as shown in the Fig. 5.2. Compared to the previous update mode and regarding the standard unipolar modulation, the voltage error in the average equivalent period decreases with the equivalent period. The maximum voltage error decreased from 58 V to 30 V. Still, this error is considerable non-negligible.



(a) Sequential Algorithm.



(b) Unipolar modulation.

Figure 5.2: CHB voltage output with $M_{idx} = 0.7$ and $T_{control} = T_c/10$.

5.2 Closed-loop results

This section reports the simulation results when the CHB is coupled with an RLE load, with parameters described in Table 5.2, on a closed circuit using the current controller. Here, the possibility of properly modulating the voltage reference at the equivalent period highly impacts the stability of closed-loop control.

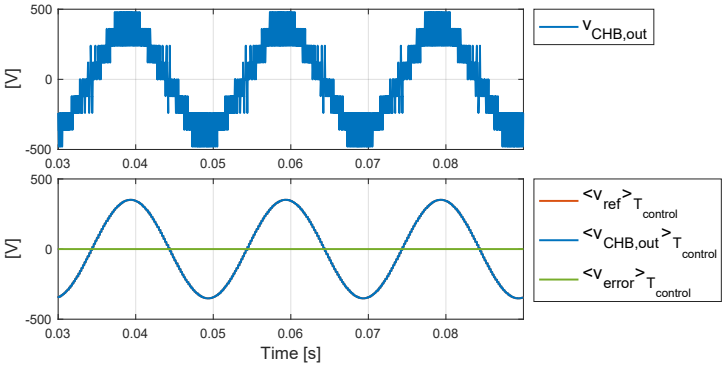
The voltage disturbance V_e is compensated in this case. It is important to note that current correction action is disabled, so that there is no interference of this factor during simulation.

Parameter	Value	Unit
R_{load}	20	mΩ
L_{load}	10	mH
V_e	230	V (rms)

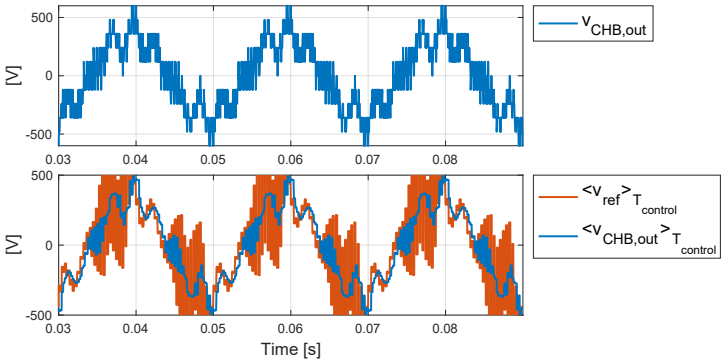
Table 5.2: Closed-loop simulation load parameters.

5.2.1 Single-Update on carrier peaks

Fig. 5.3 and 5.4 compares the voltage and current scopes, respectively, between the model operating under the Sequential Algorithm and the standard unipolar modulation. Current reference was set to 28 A.

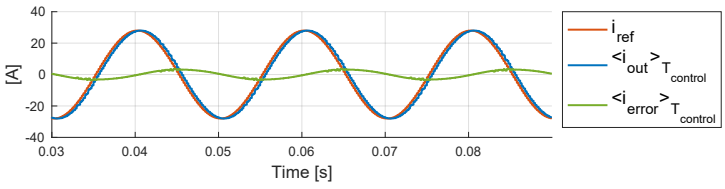


(a) Sequential Algorithm.

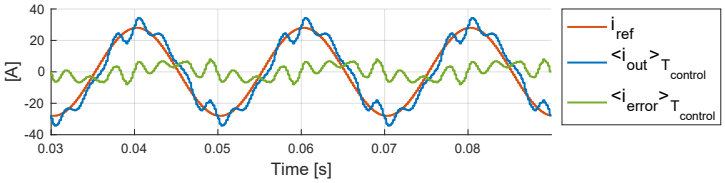


(b) Unipolar modulation.

Figure 5.3: CHB voltage output, $T_{control} = T_c/5$.



(a) Sequential Algorithm.

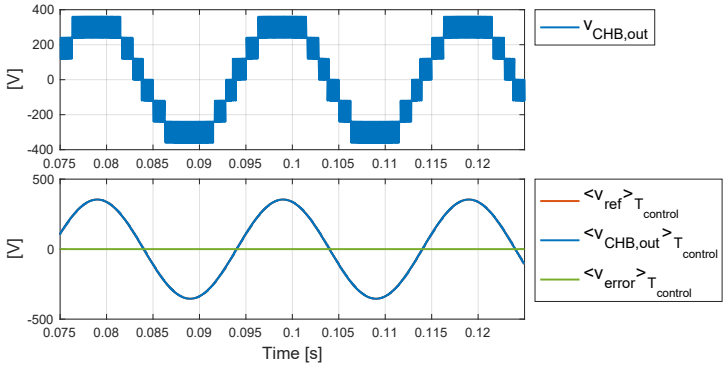


(b) Unipolar modulation.

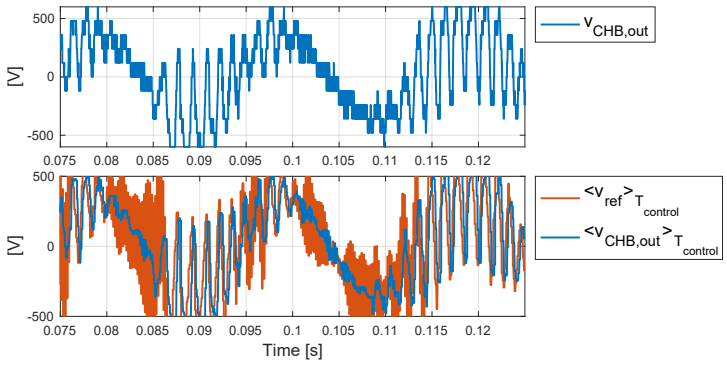
Figure 5.4: CHB current output, $T_{control} = T_c/5$.

5.2.2 Double-Update

Now the same comparison is done, but with model operating on Double-Update mode. Current reference was increased to 36 A.

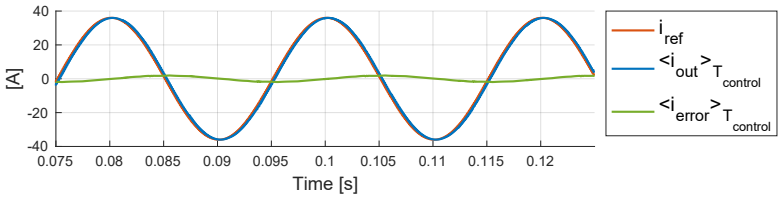


(a) Sequential Algorithm.

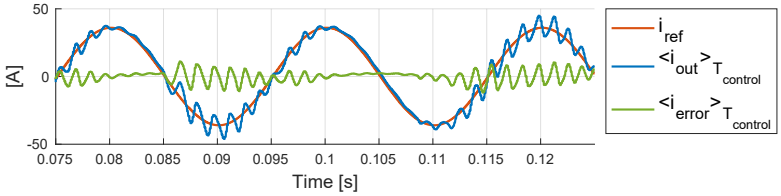


(b) Unipolar modulation.

Figure 5.5: CHB voltage output, $T_{control} = T_c/10$.



(a) Sequential Algorithm.



(b) Unipolar modulation.

Figure 5.6: CHB current output, $T_{control} = T_c/10$.

As expected from open-loop results, on both Single- and Double-Update cases, the Sequential PS-PWM Algorithm yields a stable current control. Whereas the modulation errors provoked with the standard unipolar modulation, added to its limited update frequency, compromises the current model.

5.2.3 Standard unipolar technique with slower control frequency

This case demonstrates that the model is controllable with the standard unipolar modulation strategy, under the aforementioned conditions, if the control frequency is smaller or equal to the carrier frequency, limited in its turn by the switching frequency. This effect is observable in Fig. 5.7, which shows the waveform of the controlled states of the CHB converter operating in Single-Update mode and with $T_{control} = T_c$.

Even if the output current does not follows properly the current reference, i_{out} is not dominated by large oscillations; different from the previous cases when the control was done at the equivalent output period, when the control was inappropriate.

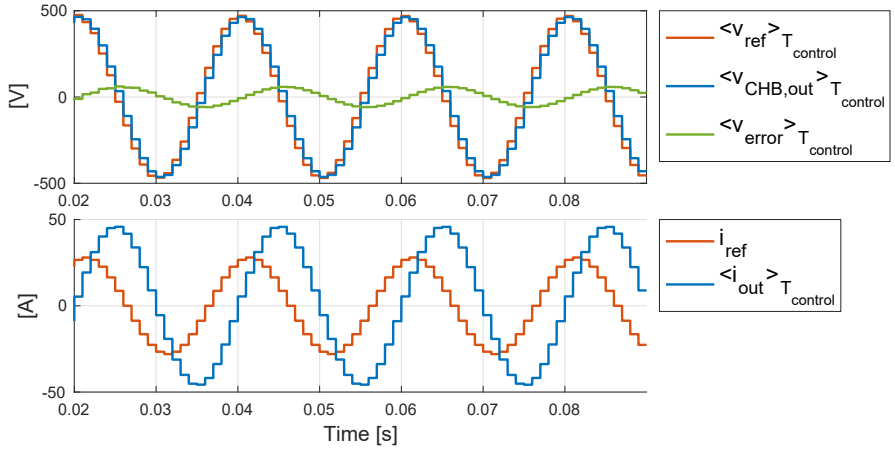


Figure 5.7: Standard unipolar modulation operating in Single-Update mode, with $T_{control} = T_c$

5.2.4 Multisampled technique

It is also possible to indirectly compare the Sequential Algorithm with the Multisampled technique by showing how the voltage error in the average update period decreases when the resampling rate increases. Fig. 5.8 depicts this effect, when the reference signal is re-sampled twice withing one switching edge, that is with rsr = 3.

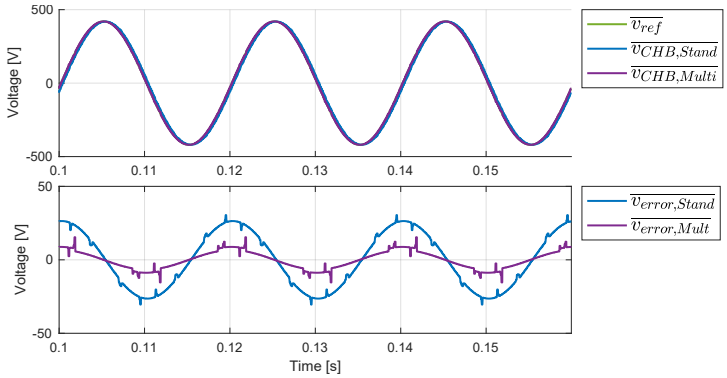


Figure 5.8: Comparison between standard unipolar and Multisampled modulation techniques on Double-Update mode.

Despite the small decrease in modulation error, the Multisampled modulation strategy can be expected to work in closed-loop when operating at the equivalent period because it further increases the update frequency. Thus, the Nyquist frequency in this case is higher than that of the standard unipolar modulation technique.

It is possible to highlight the limiting factor when the Multisampled modulation technique is used in closed-loop control, using only a two-step current MPC. Specially at the same conditions for which the standard unipolar technique did not work.

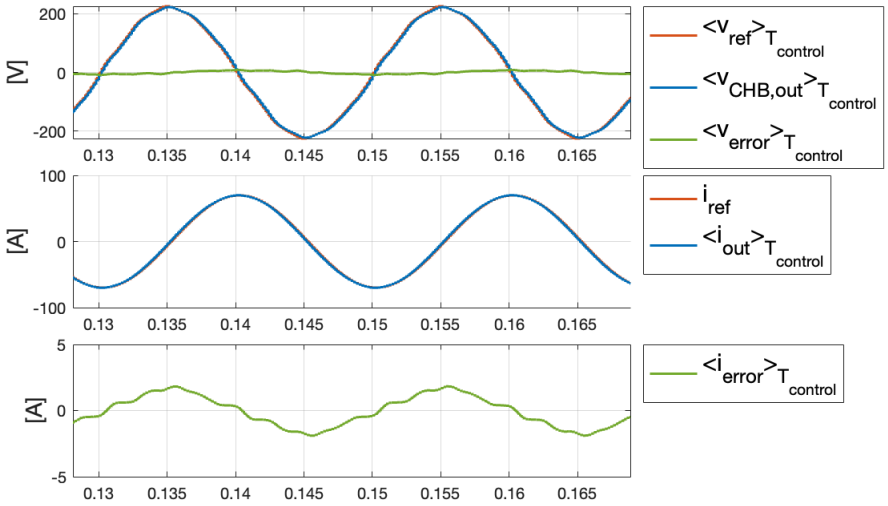


Figure 5.9: Multisampled modulation technique used in closed-loop operation on Single-Update mode, with $T_{control} = T_c/5$.

Fig. 5.9 shows that it is possible to have a stable control at the equivalent update period when the individual SMs can have their duty-cycle pair updated multiple times within one carrier period.

Other than using the Sequential PS-PWM Algorithm, Multisampled modulation is the only way to rend the system controllable at its equivalent period. In this case, however, the update frequency within every SM is augmented.

5.3 Drawbacks and limitations

The proposed Sequential Algorithm has the advantage of extending the update frequency up to the equivalent output frequency. However, this benefit is limited to some extent and comes at the detriment of other factors associated with harmonics and maximum modulation index.

5.3.1 Harmonics

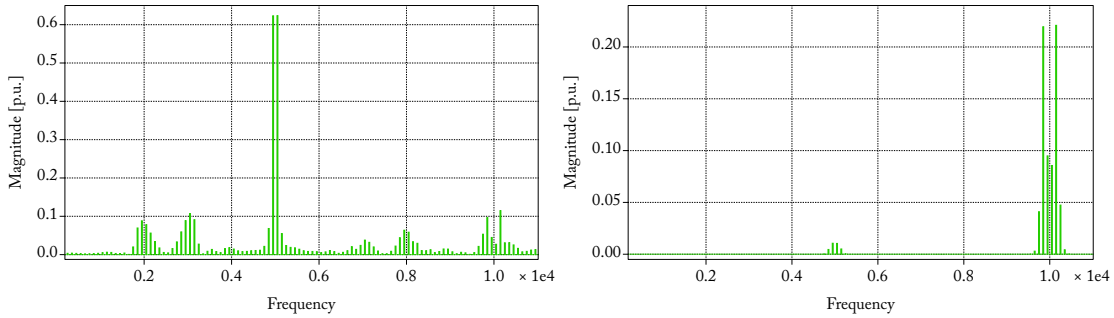
It is known that useful electric power can be only transferred with its fundamental component. Since the European grid operates ideally at 50 Hz, every other frequency component in analysis is considered to be a distortion. In practice, the transfer of power never occurs perfectly. For instance, power injected at the grid network will always have some level of distortion. Therefore, every country has its own grid code which sets the quality of power that is to be provided at the point of common coupling. In other words, it catalogs the maximum level of distortion accepted for current injection [14], being it at the frequency and magnitude levels and also duration of action. This helps Power System Engineers to design power components in accordance with requirements.

From the power quality point of view, it is desired to have a lower normalized magnitude distortion at higher frequencies, so to avoid possible interactions with other components connected to the grid.

This concept is important in order to evaluate the distortion levels characteristic of a given modulation strategy. From Fig. 5.10, it is possible to observe that the voltage output using Sequential Algorithm has distortions with higher magnitude around 5 kHz, while the unipolar modulation function yields main distortion components around 10 kHz. This difference in location of prevalent harmonics is due to the PWM symmetry. The unipolar modulation function has a common-mode of 0.5, resulting in the centering of the cell pulse in its carrier period. On the other hand, the Sequential Algorithm is characterized by having a non-constant and non-centered common-mode.

Nonetheless, the important factor is that a power device has to be compliant with the grid harmonic standard, which more commonly expresses these limits as a function of the Total Harmonic Distortion. If the limits are not respected, then external actions have to be taken into account, as the addition of filters.

In this case, the output presented in Fig. 5.10 give more of a qualitative than a quantitative result, but it is still useful for highlighting the differences of the two modulation methods in terms of distortions.



(a) Sequential Algorithm.
Dominant harmonics around 5 kHz

(b) Standard unipolar modulation.
Dominant harmonics around 10 kHz

Figure 5.10: CHB output voltage frequency spectrum, in open-loop operation, for both modulation functions with update period $T_{sampling} = T_c/N$.

5.3.2 Instantaneous balancing voltage

The second, and main, drawback is the transitory behaviour of the voltage reference at the immediate sub-interval V_s. Figures 5.11 and 5.12 show the waveform of the reference signals on both update modes, as well as the saturation point, which is the input voltage of an individual cell.

This occurrence is due to the accumulation of error once that the total voltage reference changes sign and where all the other inactive cells still have an output of opposite sign.

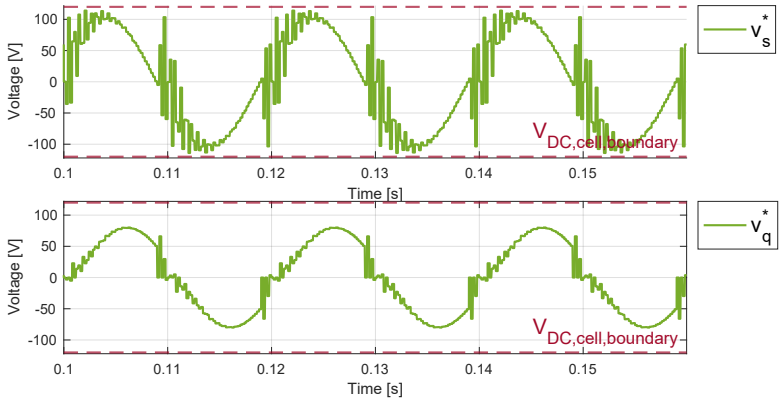


Figure 5.11: Voltage references for Sequential PS-PWM modulation, for $T_{sampling} = T_c/5$ and $M_{idx} = 0.7$, on Single-Update mode.

In Single-Update mode, the reflection of V_s in the last equivalent period worsens this event. On the other hand, this problem is naturally attenuated in the case of Double-Update; there is no large oscillatory behaviour but only spikes after the zero-crossing. This is due because V_q is not estimated but imposed, as the total voltage reference divided by the amount of cells. Being V_q a smoother signal, the cell's output in the inactive period is more stable, leading consequently to a more uniform balancing voltage, that is, V_s.

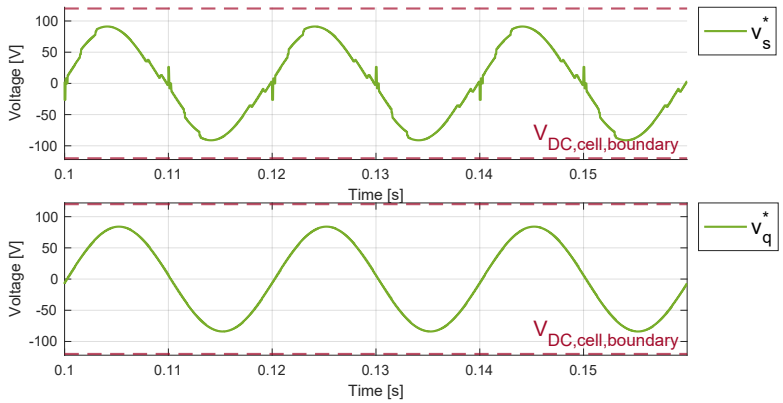


Figure 5.12: Voltage references for Sequential PS-PWM modulation, for $T_{sampling} = T_c/(10)$ and $M_{idx} = 0.7$, on Double-Update mode.

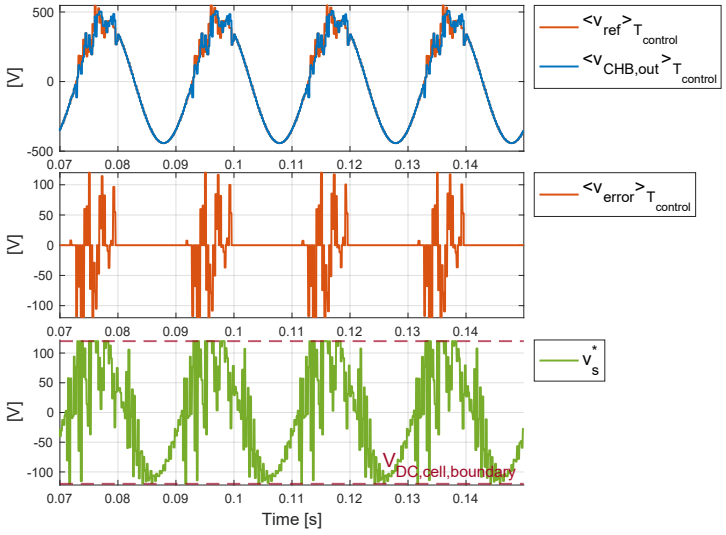
Nevertheless, the oscillating issue may be mitigated by a more clever choice of V_{pred}, in the Single-Update case, or a different value of V_q, in the Double-Update mode. It is important to bare in mind that V_q is the SM voltage reference, which should be outputted after the immediate sub-period. Thus, it is an estimation.

The transient behaviour effect is reflected on the limitation of the modulation index. The CHB converter is incapable of achieving balance if the required balancing voltage is larger than the sum available at the input. For instance, Fig. 5.13 shows what happens when this limit is exceeded. Large errors appear at the CHB modulation level due to the saturation of V_s, resulting in additional distortions at the output.

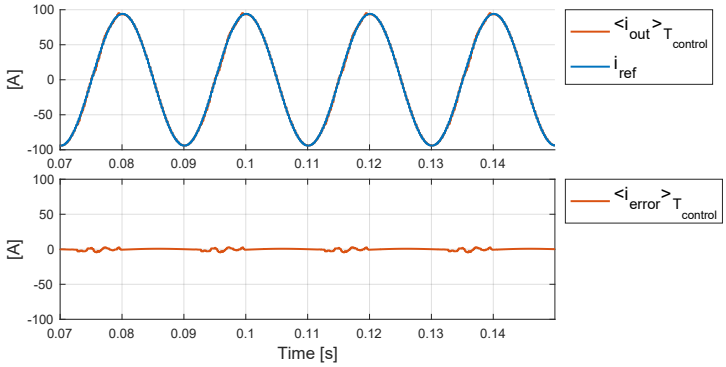
The maximum modulation index found for each update mode are reported below.

Update mode	M_{idx}^{max}
Single	0.72
Double	0.87

Table 5.3: Modulation index boundaries.



(a) Voltage scope.



(b) Current scope.

Figure 5.13: Operation on Single-Update, with $T_{control} = T_c/5$, $M_{idx} = 0.8$.

6 Non-idealities

This chapter presents the construction of secondary subsystems that take into account non-idealities, valuing a more realistic application.

6.1 Current coefficient estimation

In practice, often the load inductance and resistance might not be well known. However, as seen previously, it is crucial for the current MPC to have an accurate knowledge of the load parameters, so that the coefficients a and b are precisely known. Hence, a current coefficient estimator should be constructed. In this sense, a Least-Mean-Squares based algorithm was developed in a c-script. It stores values of both current and voltage converter references and compares it with the actual sampled output current.

Therefore, a difference minimization function is described.

$$\begin{aligned} f &= min\{||Y-\hat{Y}||\} \\ &= min\{||Y-Ap||\} \\ &= min\{(Y^T-p^TA^T)(Y-pA)\} \\ &= min\{Y^TY-p^TA^TAp-2A^TYp\} \end{aligned}$$

It essentially minimizes the difference between the predicted current value and the actual current output, sampled in the subsequent time step. In the algorithm, $n+1$ points are sampled. Thus, vectors of are sorted in the following manner.

$$Y = \begin{bmatrix} i_{o,2} \\ \vdots \\ i_{o,n+1} \end{bmatrix}_{(n,1)} \qquad A = \begin{bmatrix} i_{o,1} & v_{o,1} \\ \vdots & \vdots \\ i_{o,n} & v_{o,n} \end{bmatrix}_{(n,2)} \qquad p = \begin{bmatrix} a \\ b \end{bmatrix}_{(2,1)}$$

Setting the derivative of the objective function to zero, a formula for the optimal parameters is obtained.

$$\frac{\partial f}{\partial p} = 0 \quad \longrightarrow \quad p^* = (A^T A)^{-1} A^T Y$$

The problem of finding the actual current coefficients can be thought as finding the plane that best fits the sampled points, as illustrated by Fig. 6.1.

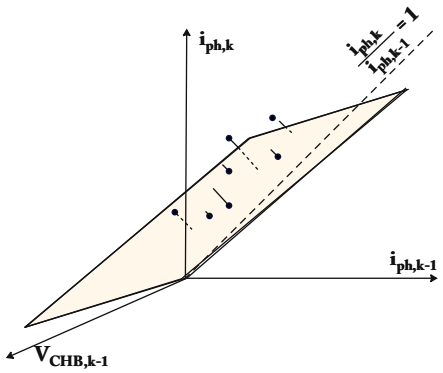


Figure 6.1: Visualization of objective function, samples against real coefficients.

Equation 6.1 expresses the load parameters as a function of the current coefficients. Thereby, with current coefficient estimator, also the load parameters are obtained.

$$R = \frac{(1-a)}{b} \tag{6.1a}$$

$$L = -\frac{R \cdot T_{eq}}{\ln(a)} \tag{6.1b}$$

Figure 6.2 shows a estimation test of load parameters, where the algorithm is initiated with inaccurate load parameters, and consequently inaccurate current coefficients. Given a sinusoidal reference, the coefficients are updated providing also an estimation of the load parameters. Information is summarized on Table 6.1.

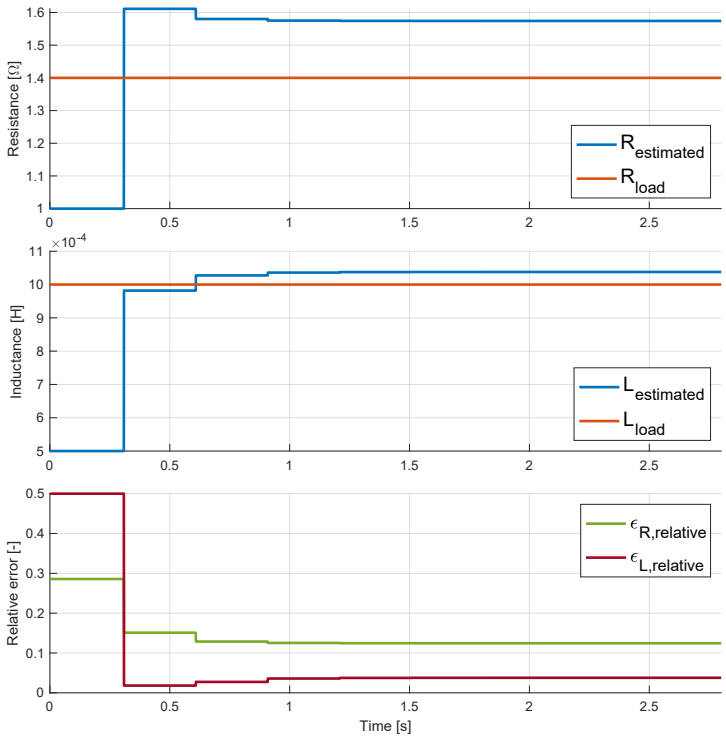


Figure 6.2: Performance of load parameter estimation algorithm.

Parameter	Value	Unit
R_{actual}	1.30	Ω
R_{est}	1.46	Ω
ϵ_R	12.3	%
L_{actual}	0.90	mH
L_{est}	0.94	mH
ϵ_L	4.5	%

Table 6.1: Load parameter estimator performance.

Additionally, it is possible to update the current coefficients online. Once an estimation is considered to be good enough, the estimator can be deactivated and a correction action would, for that step on, adjust the current controller.

It is important to highlight that this load parameter estimation was only able to be performed under very limiting conditions. For instance, for a single full-bridge cell working on standard unipolar modulation. Nevertheless, it was considered relevant its presence in this thesis, since it could build the ground for another attempt.

6.2 Correction factors

Any real model is ideal. Error compensation is a necessary element when a model control is closed in a loop.

A generic structure of a closed-loop system in the frequency domain is represented by Fig. 6.3, with main functions divided into transfer function blocks. The regulator block $C(s)$ is where correction occurs, treating the difference between the desired signal and its effective trend. The subsequent transfer function $A(s)$ represents the actuator, followed by the plant $P(s)$, which represents the load.

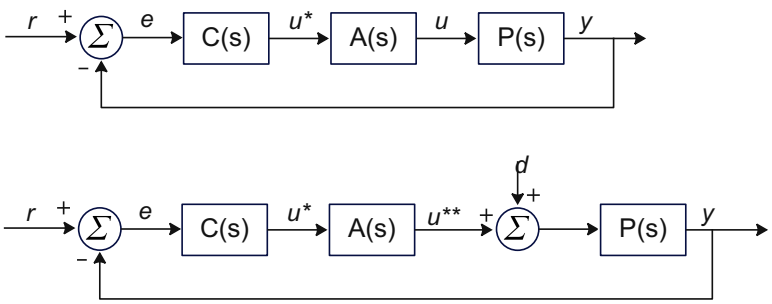


Figure 6.3: Generic control scheme of a closed-loop system, without and with disturbance.

Often, correction factor uses the difference between the reference signal and a sensed output to compensate for this error. There are, however, different methods with distinct advantages, from which two are presented.

The translation of an input to an output signal can be modelled using transfer functions, modelling the system's response as a function of frequency. Transfer functions appear as the ratio of two polynomials in s, the Laplace operator.

$$\frac{y}{r} = H(s)$$
$$H(s) = \frac{M(s)}{N(s)} = \frac{m_o + sm_1 + ... + s^m m_m}{n_o + sn_1 + ... + s^n n_n}$$

The zeros of $M(s)$ defines the zeros of the transfer function, and the zeros of $N(s)$, the poles. In order to have a stable system, the order of the denominator has to be equal or larger than the numerator's order, $n \geq m$. Also, for the system to be asymptotically stable, all poles must have all real part smaller than zero, $\Re(s) < 0$.

It is possible for the system to be open-loop or closed-loop. The open-loop transfer function for the generic block-scheme is determined as:

$$H_{OL}(s) = \frac{M(s)}{N(s)} = C(s) \cdot A(s) \cdot P(s)$$

The closed-loop transfer function, with negative feedback, is determined as:

$$H_{CL}(s) = \frac{H_{OL}(s)}{1 + H_{OL}(s)} = \frac{C(s) \cdot A(s) \cdot P(s)}{1 + C(s) \cdot A(s) \cdot P(s)}$$

Since $C(s)$ is the only block designed for regulation, it has render the system proper. For that purpose, the other system blocks have to be studied.

Considering the current as the state variable of interest, and the system under study to be the circuit shown in Fig. 4.1, the plant's transfer function can be identified.

$$\frac{i_o}{\Delta V} = P(s) \tag{6.2a}$$

$$P(s) = \frac{1}{R + s \cdot L} = \frac{K_1}{1 + sT_1} \tag{6.2b}$$

If the disturbance is taken into account, then $\Delta V = V_{CHB} - V_d$.

The actuator in the study case is the converter, represented by $A(s)$, defining the transfer function between the command and the actual CHB converter output. Assuming that the converter will effectively output the command reference by PWM means having as an effect a delay T_σ introduced by the modulation process and computational delay, or internal processes in general. T_σ is generally considered to be a function of the sampling period, normally equivalent to $1.5T_{sampling}$. Thus, Eq. 6.3 is presented.

$$\frac{V^*_{CHB}}{V_{CHB}} = A(s) \tag{6.3a}$$

$$A(s) = \frac{K_\sigma}{1 + sT_\sigma} = e^{-sT_\sigma} \tag{6.3b}$$

Where K_σ is the voltage scaling factor, equal in this case to unity. All the information is summarized in Table 6.2.

Term	Expression	Unit
K_1	$1/R$	Ω^{-1}
T_1	L/R	$\mathrm{H}\cdot\Omega^{-1}$
K_σ	1	-
T_σ	$1.5\,T_{control}$	s

Table 6.2: System transfer function terms.

6.2.1 Proportional-integral action

The proportional-integral (PI) regulator has the contribution of two terms. The former term is proportional to the error, heavily influencing the system transitory response. The integral term is proportional to the average error, which serves for eliminating constant disturbances. Its generic scheme is represented in Fig. 6.4. Its transfer function may be represented by expression 6.4, in terms of gains and time-constant.

$$C(s) = K_p + \frac{K_i}{s} = K_p + \frac{1}{sT_i} \tag{6.4}$$

Where $K_i = 1/T_i$.

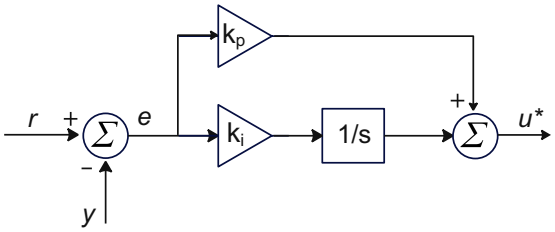


Figure 6.4: Simple PI regulator in the frequency domain.

Magnitude Optimum tuning approach was used for tuning. Its target is to maintain the amplitude of the frequency response loop as close to unity in the largest possible frequency range. The calculation steps are described below.

$$H_{OL}(s) = \frac{1+sT_iK_p}{sT_i}\frac{K_\sigma}{1+sT_\sigma}\frac{K_1}{1+sT_1} = \frac{K_\sigma K_1}{sT_i(1+sT_\sigma)} \tag{6.5}$$

$$H_{CL}(s) = \frac{1}{1 + s\frac{T_i}{K_\sigma K_1} + s^2\frac{T_i T_\sigma}{K_\sigma K_1}} \tag{6.6}$$

With Eq. 6.5, the whole expression of the closed-loop transfer function can be obtained, as shown in Eq. 6.6. Then, if the denominator amplitude is set to unity and the fourth-order velocity term (high frequency component) is neglected, it is possible to obtain an expression for T_i.

$$\left(\frac{T_i}{K_\sigma K_1}\right)^2 - 2\frac{T_i T_\sigma}{K_\sigma K_1} = 0 \quad \longrightarrow \quad T_i = \frac{1}{K_i} = 2K_\sigma K_1 T_\sigma$$

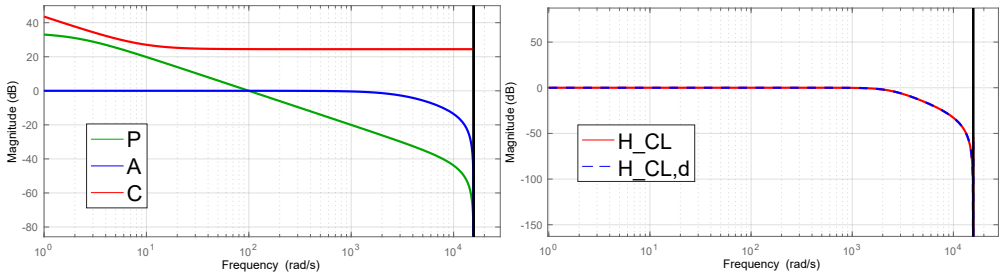
The information gathered so far is summarized in Table 6.3, where $T_{control} = T_{sampling}$.

Gain	Expression	Unit
K_i	$(2K_\sigma K_1 T_\sigma)^{-1}$	$\Omega \cdot s^{-1}$
$K_{i,d}$	$K_i T_{control}$	Ω
K_p	$T_1 K_i$	$H \cdot s^{-1}$
$K_{p,d}$	$K_p + K_{i,d}/2$	$H \cdot s^{-1}$

Table 6.3: PI regulator terms.

It is important to remark that, when the control design is done digitally, that is, in discrete-time domain, the gain expression is modified into a discrete form. This is due to the direct feed-through paths introduced by the discretized model.

From Fig. 6.5, it is possible to observe the magnitude response of the system's individual blocks and the closed-loop transfer function with the controller block.



(a) Individual blocks from the system.

(b) Closed-loop system.

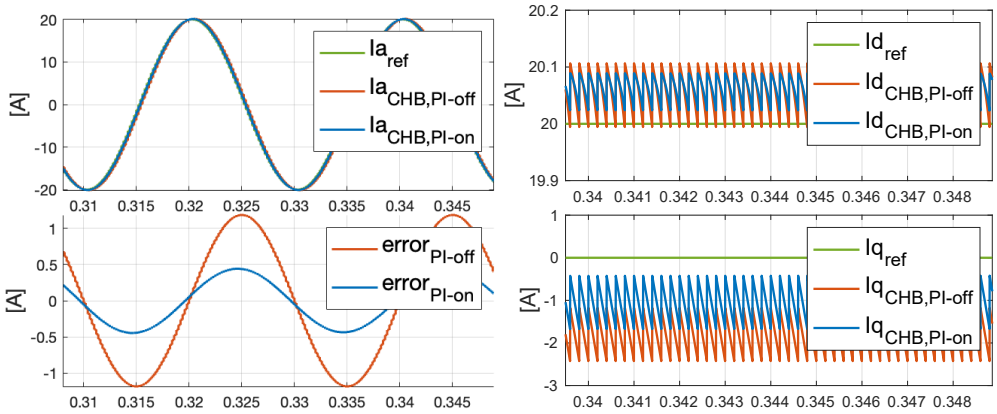
Figure 6.5: Bode plot of relevant transfer functions.

Furthermore, regarding the bode plot of the closed-loop transfer function, once the magnitude drops from 0dB, it means that the system is incapable of tracking the reference at unity. This is the drawback of the PI regulator, it is inherently incapable of tracking ac signals. The expression bellow demonstrates why.

$$w = 0: \ |H_{CL}(0)| \ = 1, \quad \angle H_{CL}(0) \ = 0$$
$$w > 0: \ |H_{CL}(jw)| \neq 1, \quad \angle H_{CL}(jw) \neq 0$$

Thus, this controller is only used with the current controller in dq-frame.

A test to evaluate the performance of the PI regulator was done under the Sequential PS-PWM Algorithm. For instance, Fig. 6.6 shows the current waveform, on both stationary and synchronous frames, for the cases when the PI controller is enable and disabled. The model in that case was being controlled with current in the dq-frame, with a PI controller for each current component, that is both i_d and i_q.



(a) abc-frame, scope from phase a. (b) dq-frame.

Figure 6.6: PI steady-state performance for 3-phase model, coupled with grid.

It is possible to note that the PI correction effectively pushes the i_q closer to its reference, and the i_d decreases its ripple amplitude. As a result, the output current in the stationary reference frame decreases its amplitude error.

6.2.2 Proportional-resonant action

The proportional-resonant (PR) regulator takes into account the sinusoidal nature of the signal by setting, from its transfer function, a high gain around the frequency of interest. Thus, making the steady state error negligible for an AC variables. The generic schematic is displayed by Fig. 6.7.

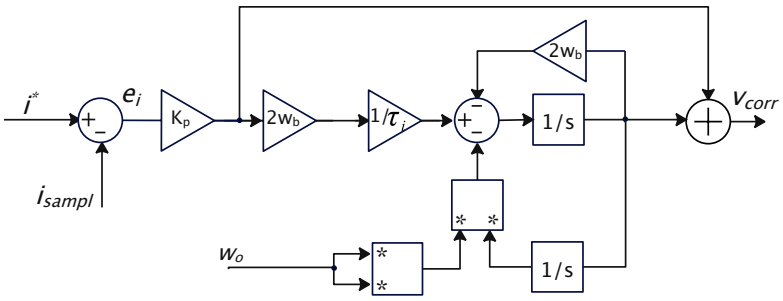


Figure 6.7: Non-ideal PR block scheme in frequency domain.

A non-ideal PR model was chosen so that the model would approximate better a real application, when it becomes important to take into account stability issues. The PR controller block is represented by expressions in 6.7, in ideal and non-ideal form, respectively.

$$C_{PR}(s) = K_p\left(1+\frac{1}{\tau_i}\frac{s}{s^2+w_o^2}\right) \tag{6.7a}$$

$$C_{PR,non-id}(s) = K_p\left(1+\frac{1}{\tau_i}\frac{2w_b s}{s^2+2w_b s+w_o^2}\right) \tag{6.7b}$$

Where w_o is the grid frequency in rad/s, which in practice is not constant and is provided by the Phase-Locked-Loop.

The tuning of its parameters is done by verifying the maximum possible gain of the system open-loop transfer function at the cut-off frequency, w_c. For instance, the Phase-Margin (PM) is an indicator of robustness of the retroactive system, and a distance in phase from the instability. A least 30^o is considered to be a safe margin.

Parameter	Value	Unit
PM	$\pi/4$	rad
w_B	10	rad/s
w_c	$\frac{\pi/2-PM}{T_\sigma}$	rad/s
τ_i	$10/w_c$	s
K_p	$\frac{w_C \cdot L}{K_\sigma}\cdot\frac{1}{5}$	H·rad/s

Table 6.4: PR tuning expressions.

Table 6.4 reports the used parameters, where w_b is the bandwidth around the frequency of interest. The gain adaptation for the discretized model is analogous to the one done in the PI regulator. In this case, the Trapezoidal integration method was used, A.2.3.

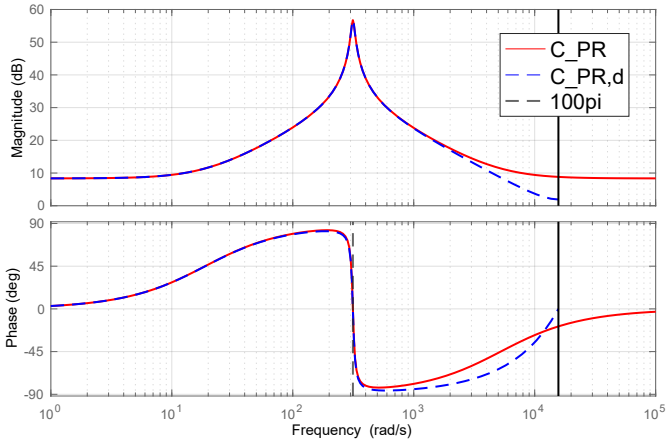


Figure 6.8: Bode plot of used non-ideal discretized PR regulator transfer function.

From the bode plot reported in Fig. 6.8 is possible to verify a gain of about 60dB in the neighborhood of the grid frequency, equal to $2\pi 50$ rad/s.

Actual performance is displayed in Fig. 6.9, when the PR regulator was tested for a simulation with the CHB modulated with the Sequential Algorithm. It is possible to see that without the controller, the signal is incapable of tracking the reference; whereas with the PR regulator, an approximately null error is obtained.

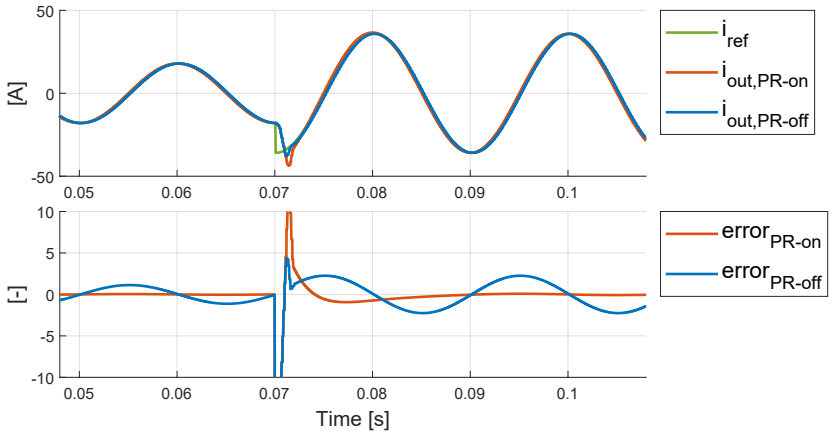


Figure 6.9: Output current response with and without PR correction action, for single-phase model in Double-Update mode.

6.3 Blanking time compensation

In full-bridge converters, is common practice to introduce a time interval between the switch of conduction state of two switching devices from the same converter leg so to avoid the risk of short-circuiting the dc-link. This additional time, t_b, is called dead or blanking time and

is the time a switching device takes to turn on after its complementary switching device has turned off.

This safety measure has the drawback of introducing voltage loss at the converter output, which on its turn is not dependent on the current value but on its polarity, due to both leg transistors that are off. As scheme of this event is depicted in Fig. 6.10

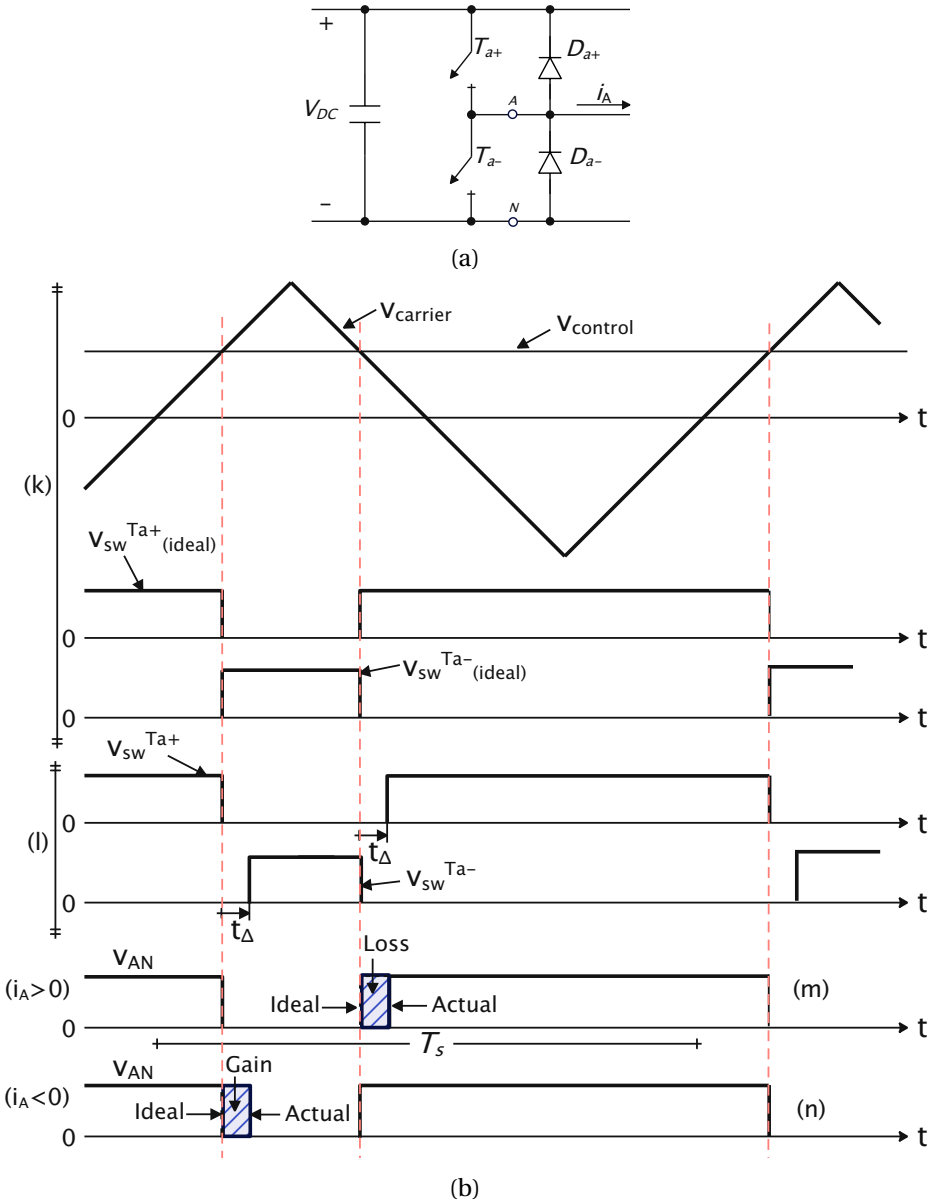


Figure 6.10: Dead-time effect. Being indications, (k) ideal case, (l) actual case, (m/n) when current polarity is positive/negative.

The voltage loss can, however, be at least compensated at the moment of modulation. In order

to evaluate the voltage loss, let the voltage difference between the ideal and actual case [15].

$$\Delta V = (V_{AN})_{(ideal)} - (V_{AN})_{(actual)} \tag{6.8}$$

By averaging the output voltage in the whole carrier period, it is possible to obtain a formula with respect to the blanking time and the switching period.

$$\Delta V_{AN} = \begin{cases} +\frac{t_b}{T_{sw}} V_{DC} & i_A > 0 \\ -\frac{t_b}{T_{sw}} V_{DC} & i_A < 0 \end{cases} \tag{6.9}$$

Regarding the full bridge topology, already demonstrated in the introduction 1, the expression for voltage loss in the second converter leg will have a dual expression, as shown in Eq. 6.10.

$$\Delta V_{BN} = \begin{cases} -\frac{t_b}{T_{sw}} V_{DC} & i_B > 0 \\ +\frac{t_b}{T_{sw}} V_{DC} & i_B < 0 \end{cases} \tag{6.10}$$

Therefore, the total voltage loss, ΔV_o, due to blanking time for a full-bridge SM will be doubled than the one for a single converter leg.

$$\Delta V_o = \begin{cases} +2\frac{t_b}{T_{sw}} V_{DC} & i_o > 0 \\ -2\frac{t_b}{T_{sw}} V_{DC} & i_o < 0 \end{cases} \tag{6.11}$$

Although the effect is well known, in practice blanking time is not straightforward to perfectly compensate because of factors such as strain capacitance and fall-time, but it may still be modelled and partially compensated within the modulation process.

First of all, in order to model the compensation of the blanking time, it can be thought to sum a term to the voltage references.

$$V_s\prime = \langle V^*_{CHB}\rangle_{T_{eq}} - \sum_{i\in\mathcal{J}} V_{i,live} + V_{s,comp} \tag{6.12a}$$

$$V_q\prime = \langle V^*_{CHB}\rangle_{T_c} - \sum_{i\in\mathcal{J}} V_{i,average} + V_{q,comp} \tag{6.12b}$$

As for the summing terms, they were chosen to be a function of the output current value coupled with the voltage loss expression retrieved in Eq. 6.11. Since the output current will have an intrinsic ripple, it was thought to under-compensate the references rather than risk to over-compensate. For that, some Sigmoid functions, being function of the output current, were analysed, as displayed in Fig. 6.11. This way, as the current approaches zero, the compensation factor is attenuated.

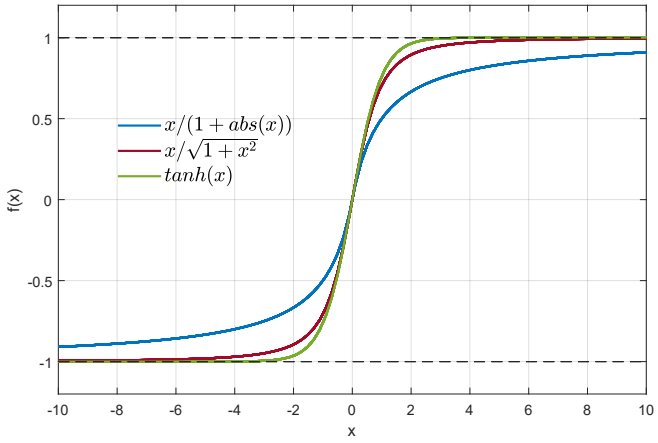


Figure 6.11: Sigmoid function examples.

A way to quantitatively assess the performance of a given Sigmoid function, the current Total Harmonic Distortion (THD) was measured. THD is a metric of signal components different than the component of the n-th order, typically set with respect to the fundamental component (n=1), as defined in Eq. 6.13.

$$THD_n = \frac{\sqrt{\sum_{h\neq n}^{+\infty} I_h^2}}{I_n} \tag{6.13}$$

One of the examples that resulted in a low THD is $\tanh(x)$, but being a trigonometric function, it slows down the simulation.

Equation 6.14 shows a Sigmoid type function found to have an effective compensation, which altogether is not computationally demanding.

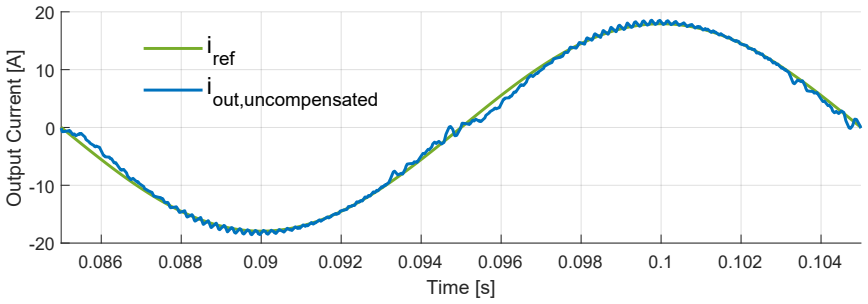
$$\mathcal{S}(x) = \frac{x}{\sqrt{1+x^2}} \tag{6.14}$$

After some empirical testing, an approximate optimal compensation expression was found for Single-Update mode, shown in Eq. 6.15.

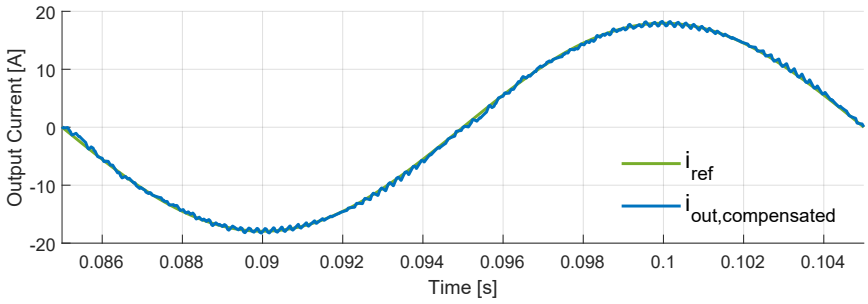
$$V_{q,comp} = V_{DC,cell} \cdot \frac{t_b}{T_c \cdot 4/5} \cdot \mathcal{S}(i_{ref}) \cdot 2 \tag{6.15a}$$

$$V_{s,comp} = V_{DC,cell} \cdot \frac{t_b}{T_c/5} \cdot \mathcal{S}(i_{ref}) \cdot 2 \tag{6.15b}$$

Finally, Fig. 6.12 shows the blanking time compensation effect on the output current, with the CHB converter operating with the Sequential Algorithm in Single-Update mode. The simulation parameters chosen are reported in Table 6.5.



(a) No compensation.



(b) Voltage references compensated.

Figure 6.12: Instantaneous output current response with presence of blanking time.

Parameter	Value	Unit
T_c	1	ms
t_b	20	μs
i_{ref}	20	A

Table 6.5: Simulation parameters.

Although the output current still manifests distortions, the compensation was able to reduce the current THD. This way, the Sigmoid functions were tested and the resulting THD are reported on Table 6.6, establishing the choice of the most adequate option.

Function	THD (%)
0	4.8779
$\frac{x}{\sqrt{1+x^2}}$	1.9872
$\tanh(x)$	1.9784
$\frac{x}{1+\lvert x\rvert}$	2.1601

Table 6.6: Output current THD with respect to Sigmoid function used in compensation algorithm.

7 Three-phase extension

In order to represent a practical application and to further verify the proposed content, the CHB converter model is extended to three-phase. Therewith, the control has to be slightly adapted, as it is going to be shown. In this chapter, the three-phase model extension is presented, along with the demonstration of a grid coupling example in order to perform a robustness test of the CHB controller with the Sequential Algorithm under unbalanced grid conditions.

7.1 Grid coupling

A converter may work with different types of equivalent loads, but the most common cases would be a connection to motor or grid. The case of connection with the grid can be thought of a HVDC conversion station, at the dc-ac end. The inverter handles high voltage from a stable dc-bus and converts the electricity in ac mode. However, in order to correctly exchange energy, some conditions must be satisfied:

- knowledge about grid phase voltages, frequency and angle
- heavy disturbances should be detected
- grid monitoring and synchronization must be fast and robust against disturbances

7.1.1 Phase-Locked Loop

The Phase-Locked Loop (PLL) is a mature method that allows an effective grid monitoring and synchronization. The energy can only be transferred by the voltage fundamental component, any other component is considered distortion and will turn into losses. This is why the PLL is essential for the grid coupling of the inverter, so that energy can be exchanged effectively.

Various and adaptations for specific issues can be found in literature [16], but here the PLL

type chosen is the synchronous reference frame. Fig. 7.1 shows the PLL structure with its basic functions highlighted. It consists of a Phase-Detector (PD), a Loop-Filter (LF) and a Voltage-Controlled-Oscillator (VCO).

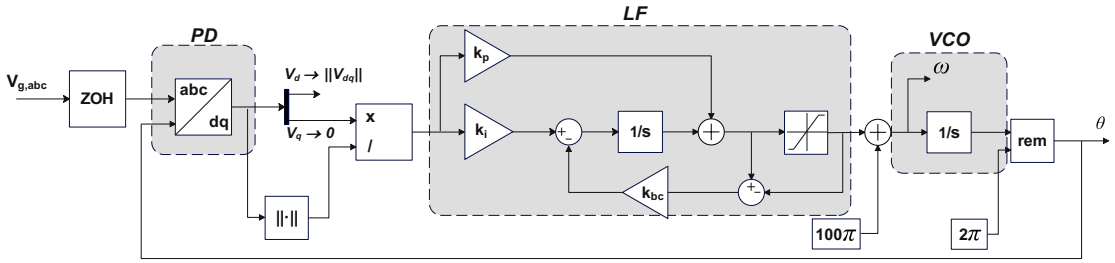


Figure 7.1: PLL scheme with main components highlighted.

As input, the sampled grid voltage is transformed from three-phase abc reference frame into dq-frame using Park transform B.3. This process represents the phase detection, as the loop is latched at that point. Being so, the normalized reactive voltage component $v_{q,n}$ will be driven to zero and the d-axis of the dq-frame will be aligned with a phase-voltage space vector.

The LF consists of a simple PI regulator with back-calculation. A saturation block was used in order to prevent the velocity to deviate more than a certain limit, in this case of ± 1 Hz from the fundamental frequency. Whereas the back-calculation term acts on the integral value, which is reduced or increased by feeding back the difference of the saturated and unsaturated control signal. It prevents the local controller to provoke excessive overshoots and larger settling times.

In addition, there's a feed-forward term equal to the fundamental grid velocity used to speed up the initialization of the tracking process. Finally, the VCO integrates the velocity, in rad/s, into angle unit, in radians.

The PLL controller can be tuned by analysing the local system closed-loop transfer function in the canonical form.

$$H_{OL} = \frac{K_p s + K_i K_p}{s^2} \tag{7.1a}$$

$$H_{CL} = \frac{K_p s + K_i K_p}{s^2 + sK_p + K_i K_p} \longrightarrow \frac{2\zeta s + w_n^2}{s^2 + s2\zeta w_n + w_n^2} \tag{7.1b}$$

Where $w_n = \sqrt{K_i \cdot K_p}$ is the nominal frequency and $\zeta = \frac{1}{2}\sqrt{K_p / K_i}$ is the damping factor. The overall desired response characteristic set is shown in Table 7.1.

Parameter	Value	Unit
t_s	80	ms
ζ	$\sqrt{2}/2$	-
w_n	$9.2/(t_s \cdot \zeta)$	rad/s
w_{sat}	$2\pi(50 \pm 1)$	rad/s
$K_{i,d}$	$T_{control} \cdot w_n/(2 \cdot \zeta)$	rad/s^2
$K_{p,d}$	$2\zeta w_n + K_{i,d}/2$	rad/s
K_{bc}	$K_{i,d}/K_{p,d}$	1/s

Table 7.1: PLL tunning.

7.1.2 Decoupled Second-Order Generalized Integrator

The Decoupled Second-Order Generalized Integrator (DSOGI) is an Adaptive Filter, used to decouple two sequences from a signal and which bandwidth does not depend on the estimated grid velocity [16]. It is useful in practice for grid monitoring under unbalanced conditions, enhancing the PLL.

The decoupling between positive and negative symmetrical sequences from a disturbed signal can be done with the expressions shown in Eq. 7.2. Further explanation on sequence decomposition is presented in appendix B.1.

$$\mathbf{v}^{+}_{\alpha\beta} = \left[T_{\alpha\beta}\right]\left[T_{+}\right]\left[T_{\alpha\beta}\right]^{-1}\mathbf{v}_{\alpha\beta} = \left[T_{\alpha\beta+}\right]\mathbf{v}_{\alpha\beta} = \frac{1}{2}\begin{bmatrix}1 & -q\\ q & 1\end{bmatrix}\mathbf{v}_{\alpha\beta} \tag{7.2a}$$

$$\mathbf{v}^{-}_{\alpha\beta} = \left[T_{\alpha\beta}\right]\left[T_{-}\right]\left[T_{\alpha\beta}\right]^{-1}\mathbf{v}_{\alpha\beta} = \left[T_{\alpha\beta-}\right]\mathbf{v}_{\alpha\beta} = \frac{1}{2}\begin{bmatrix}1 & q\\ -q & 1\end{bmatrix}\mathbf{v}_{\alpha\beta} \tag{7.2b}$$

Where $q = e^{-j\pi/2}$, which corresponds to the orthogonal signal. After the signal is decoupled, each voltage component undergoes the SOGI transfer function 7.3.

$$SOGI(s) = \frac{\omega' s}{s^2 + \omega'^2} \tag{7.3}$$

Being ω' the tracking variable. The DSOGI also includes in its structure a quadrature signal generation (QSG) structure, that is used to obtain the orthogonal equivalent signal from the original signal component. Its equivalent expression is shown in 7.4.

$$\frac{q v'_x}{v'_x} = \frac{w}{s} \tag{7.4}$$

Fig. 7.2 shows the PLECS implementation of the DSOGI structure.

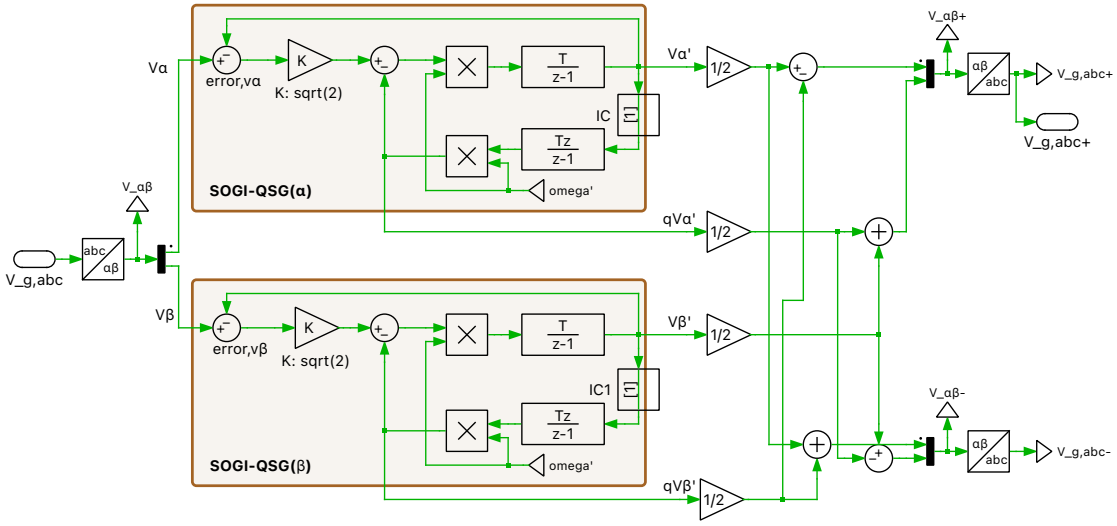


Figure 7.2: DSOGI schematic on PLECS.

One relevant factor to be taken into account are algebraic loops, which happen when the output of a block is dependent on the input of the same block. Algebraic loops naturally cause simulation errors and must be avoided. For this reason, Forward and Backward Euler integration methods were used in the forward path and backward path, respectively. Additionally, an initial condition is used in the backward path to launch the simulation.

7.2 Model adaptation

The grid measurements, of voltage and current, are performed at the point of common coupling. The voltage at the output of the CHB converter is also retrieved but only for analysis purposes, not taking any role in the controlling process.

Based on the tests to be carried, the reference current was chosen to be set in the dq-domain. Generally, in direct power conversion from a generation plant, only active power is of interest. Therefore, the reactive component reference is always set to zero. Figure 7.3 shows a didactic scheme of how the model was assembled.

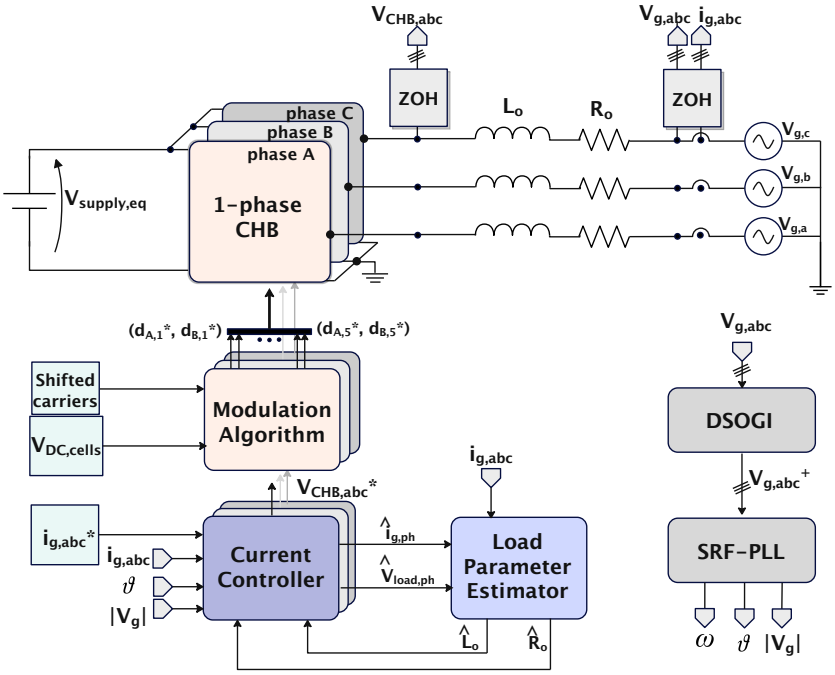


Figure 7.3: 3-phase model schematic.

Figure 7.4 displays the CHB converter schematic in PLECS, where each phase has an identical branch of SMs, forming a star connection.

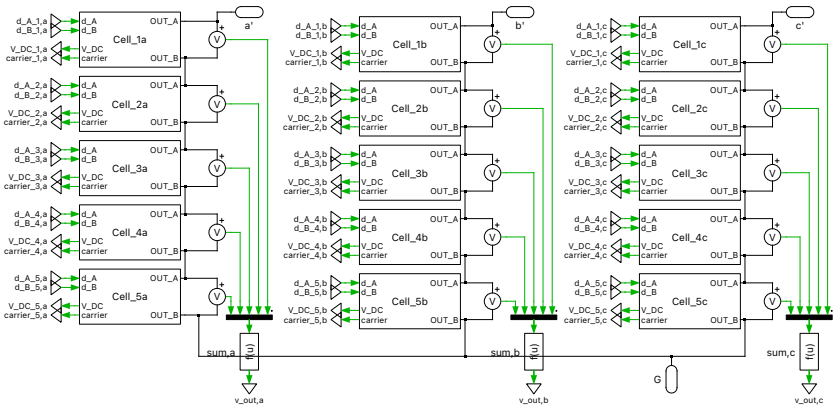


Figure 7.4: PLECS schematic of three-phase CHB converter.

The current control may be performed in abc-frame with resonant action, and in dq-frame with integral action. In both cases the control has a parallel structure, where each phase or component has its own current controller and regulator. However, since current error was smaller for current control in the three-phase domain, this method was given the preference in the grid-coupling tests.

Now that the CHB converter is connected to the grid, the grid voltage can be seem as a disturbance. Thanks for the implementation of the DSOGI and the PLL, the amplitude of the grid voltage positive sequence can be identified and compensated at the current controller.

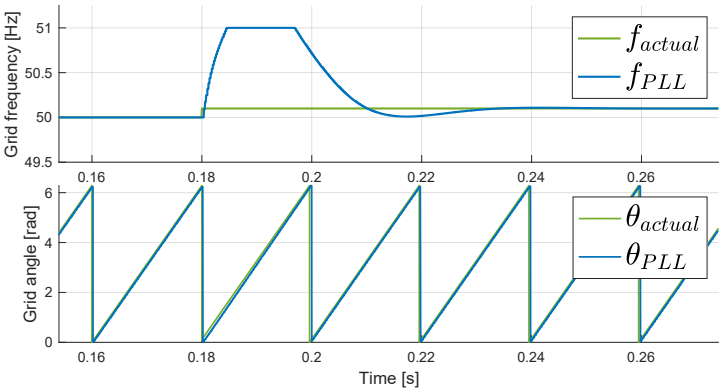
7.3 Three-phase model validation

The synchronization with the grid voltage becomes crucial for grid converters to exchange power. Therefore, it is key for the detection instrument to be capable of obtaining certain information from the grid even when it is heavily affected by disturbances.

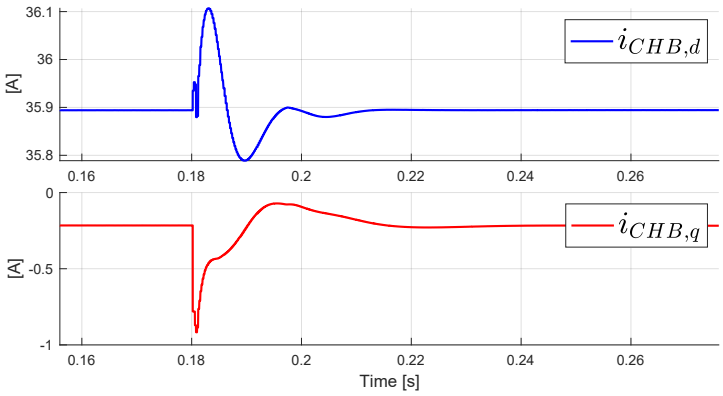
7.3.1 Change in frequency

It is known from power systems theory that changes in grid frequency are due to differences between generated power and the demand. For instance, when the grid is more loaded than what it is currently providing, the synchronous machines that are injecting power into the near region grid endure a heavier torque and they slow down their rotor speed. Therefore, the example under study could be the case of a heavy industry which disconnects from the grid, causing a quick increase in the grid frequency.

Figure 7.5 shows the performance of the PLL for an aggressive step change in frequency of 100 mHz, in terms of change of active and reactive current components, for the three-phase model working with the Sequential PS-PWM Algorithm, on Single-Update mode.



(a) Estimated grid frequency and phase.



(b) Output current.

Figure 7.5: PLL response for frequency step change of 100mHz.

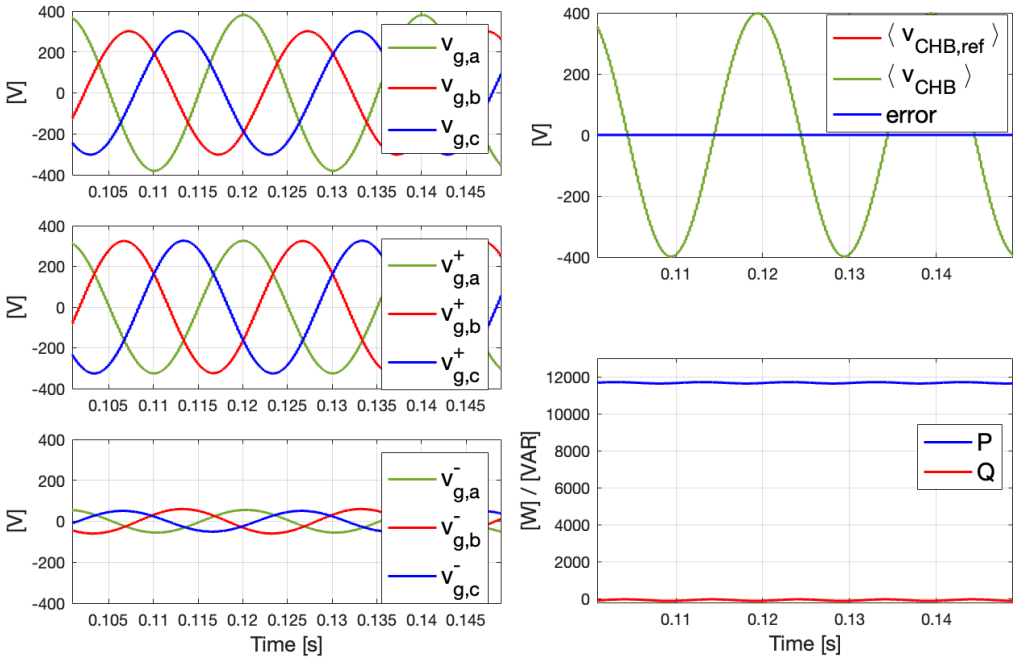
It is possible to see that, despite the settling time being larger than expected, each current component undergoes a relatively small overshoot value and quickly returns to the previous steady-state value. This experiment may be an initial verification of the functioning of the Sequential Algorithm for the three-phase CHB converter synchronized with a balanced grid.

7.3.2 Unbalanced grid

A final experiment was done for a unbalanced grid in steady-state, as observed in Fig. 7.6. In the case, the ideal grid voltage has a negative sequence symmetrical component of amplitude $0.17V_{g,pk}$, of the first order. This disturbance causes the grid phase voltage amplitudes to differ, and can be caused by load imbalances across the grid.

The DSOGI is capable of decoupling the symmetrical sequences, providing only the positive sequence to the PLL. Even so, the conversion is not perfect. The transmitted power has an oscillation of 10 ms, that is, half of a fundamental period. Yet, the ripple amplitude constitutes only 0.3 % of the apparent power.

Finally, the CHB converter control is still able of supplying at the output a perfect balanced voltage at the equivalent period average.



(a) Unbalanced grid voltage.

(b) CHB output.

Figure 7.6: Unbalanced grid test, CHB converter working with Sequential PS-PWM Algorithm on Single-Update mode.

8 Conclusion

CHB converters are a promising type of MMC, in much relevance in medium and high voltage applications. Their use can be seen in applications as HVDC conversion stations, STATCOMs, MV drives and direct connection of renewable energy plants to MV grid. Therefore, the improvement of features that could easy the spreading of this mean becomes encouraging. With that, this master thesis focused on the realization of a Sequential PS-PWM Algorithm that can extend the update frequency and closed-loop bandwidth of a CHB converter at parity of switching frequency by sequentially commanding the cascaded cells.

In this chapter, the work done on the master thesis is briefly over-viewed, as well as the recap of the main results. At the end, possible further works are cited.

8.1 Modulation algorithms

Primarily, within this thesis, motivational content was introduced. Fundamental concepts of the CHB converter were studied and its modulation was explained. Then, a detailed description of the PS-PWM working principle was delineated, followed by the explanation of the Sequential PS-PWM Algorithm for possible update modes.

It was found in the results that it is possible to obtain null error of the modulated voltage reference, in the equivalent period average, with the Sequential PS-PWM Algorithm. The comparison with the standard unipolar modulation function is summarized in Table 8.1.

Limitations were also pointed out, along with suggestions for possible mitigation.

In order to demonstrate how the possibility of being able to update only a single cell at a time imposes a performance limitation in the model, the CHB converter model was also tested with the resampled unipolar modulation method, also known as Multisampled technique. With a resampling ratio of at least 3, the closed-loop model was verified stable operating at the equivalent frequency. Nevertheless, even with the Multisampled technique inducing non-negligible modulation errors, it still requires extra update conditions that are not needed

Configuration		Modulation	
		Seq. Algorithm	Stand. unipolar
Open-loop	Single-Upd.	negligible error	substantial error
	Double-Upd.	negligible error	substantial error
Closed-loop	Single-Upd.	stable	unstable
	Double-Upd.	stable	unstable

Table 8.1: Summary of both PS-PWM modulation techniques under study, operated at the equivalent period of each respective update mode.

when using the Sequential PS-PWM Algorithm.

8.2 Complementary features

Two-step current MPC: The solution of a generic RLE circuit was discretized in order to set a two-step current model predictive control in a c-script, which was done both in single phase and in dq-frame for a three-phase model. Closed-loop modulation tests were done with an RLE load, while the most complete load model was done in three-phase, where the access to a voltage disturbance estimation is possible thanks to the grid monitoring system.

Load parameter estimation: For the sake of completeness, it was thought to construct a load parameter estimator in order to guarantee the awareness of the current coefficient, necessary for the proper functioning of the current predictor. An algorithm based on Least-Mean-Squares method was assembled. However, as it was shown, the load parameter estimator algorithm did not succeed in functioning in a complete CHB converter model, but only for one full-bridge cell working with standard unipolar modulation. Nonetheless, the integrity of the attempt is not harmed by the failure of completion of this method, since the conditions of experiment were declared.

Current controller correction actions: Proportional Integral and Resonant correction actions were properly set by the modelling of the plant and of the converter in transfer functions. Supporting theory was demonstrated, tuning procedure was shown, as well as bode plots of the current regulators in order to demonstrate it effectiveness.

Blanking time compensation: An attempt to compensate the blanking time was done by studying the voltage loss effect and by choosing an adequate Sigmoid function. Despite the challenge to perfectly compensate it, the method demonstrated a significant decrease in current THD factor.

Grid-connected application: The initial single-phase CHB converter model was extended to a

three-phase grid-connected inverter so that the robustness of the whole system functioning with the proposed algorithm could be tested. This extension includes the implementation of grid monitoring and synchronization blocks as a DSOGI and PLL. The test involved a step change of grid frequency, and functioning with grid voltage heavily disturbed by a negative sequence component, showing reasonable results.

8.3 Further work

– Scale the implementation of the algorithm with an arbitrarily large number of cells

In every practical case of application there will be some sort of peculiarity that may play a role with the number of necessary SMs, also taking into account the redundancy. In addition, other features could be included in the analysis, such as the optimal number of operating cells for input capacitor charging.

– Study of choice of low priority voltage reference

A punctual study on the choice of the second voltage reference V_q may be done, in order to extend the modulation index limit.

– Hardware-in-the-loop test

Hardware-in-the-loop implementations are useful when experimenting control methods in testing phase, it allows a real-time simulation without making use of actual hardware, which could be prompt to damage in case of failure or bugs in the control software.

– Implementation in Virtual Synchronous Generator

Considering the promising use of Virtual Synchronous Generators in incorporating important features of grid-connected synchronous machines, it could be propitious to study it under the proposed Sequential PS-PWM Algorithm.

A Appendix - Discretized systems

Digital computers work by definition with discretized values. For example, when an physical, therefore continuous, signal is sampled and reconstructed by the analog-to-digital converter, the sampled signal will be then discretized. It is not different when it comes to simulating a real system. Hence, it can be valuable to note some aspects of discrete signal treatment.

A.1 Z-transform

The definition of the Z-transform is an elementary factor of signal discretization. With this motivation, a definition from the book "Fondamenti di Controlli Automatici" is provided. "Given a complex function f by the integer variable k, and the complex variable $z = \rho e^{j\theta} \in \mathcal{C}$, being ρ and θ the modulus and angle, respectively. If function A.1 exists for at least some value of z, then the former is called the *Z-transform* of $f(k)$", [17].

$$F(z) = \sum_{k=0}^{+\infty} f(kT_s) \cdot z^{-k} \tag{A.1}$$

The Z-transform becomes useful when treating discrete signals, as it can be used as the Laplace-transform of a continuous signal. In other words, both transformations are related by the expression A.2.

$$z = e^{sT_s} \tag{A.2}$$

Where T_s is the sampling period. Thus, this is the domain used for the definition of discrete transfer-functions and is used for integral operations in simulation softwares.

A.2 Discretization methods

Here some examples of popular integration methods in discrete-time systems are presented. Each of them have the integral determined by a specific value of the sample within both edges after the ZOH operation.

A.2.1 Forward Euler

Integral at time kT_s defined by sample $x(t)$ at time $kT_s - T_s$:

$$\int_{kT_s-T_s}^{kT_s} x(t) \approx x(kT_s - T_s) \cdot T_s$$

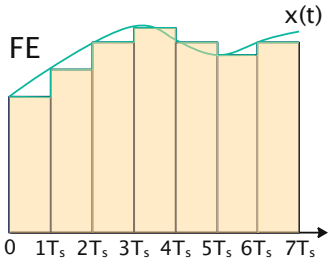


Figure A.1: Forward Euler.

A.2.2 Backward Euler

Integral at time kT_s defined by sample $x(t)$ at time kT_s:

$$\int_{kT_s-T_s}^{kT_s} x(t) \approx x(kT_s) \cdot T_s$$

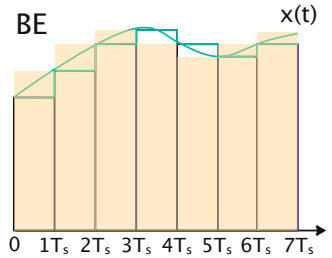


Figure A.2: Backward Euler.

A.2.3 Trapezoidal (Tustin)

Integral at time kT_s defined by sample $x(t)$ both at times $kT_s - T_s$ and T_s:

$$\int_{kT_s-T_s}^{kT_s} x(t) \approx \frac{x(kT_s - T_s) + x(T_s)}{2} \cdot T_s$$

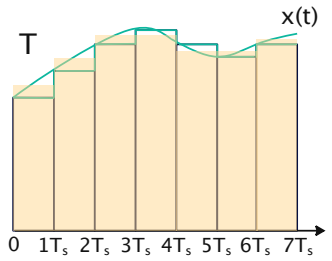


Figure A.3: Trapezoidal.

The result is that if the Backward Euler or Forward Euler integration method are used in a discrete transfer function, the input signal has direct feed-through on the output signal. Therefore, a suitable choice of integration method, or the non straightforward substitution of the variable s, becomes important to avoid algebraic loops on the simulation environment.

The frequency-domain Laplace operator s can be replaced by the equivalent expressions

presented on Table A.1, according to each integration method.

FE	BE	T
$\frac{1-z^{-1}}{z^{-1}T_s}$	$\frac{1-z^{-1}}{T_s}$	$\frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}$

Table A.1: Replacement expressions of the Laplace operator to the discrete counterpart z-operator according to integration method.

B Appendix - Space vector transformations of three-phase systems

B.1 Symmetrical components

An three-phase set of sinusoidal waves with different amplitude and not equally phase-shifted in the Cartesian plane may be representative of grid voltage system under unbalanced conditions. This unbalanced three-phase grid voltage may be decomposed in positive, negative and zero sequences.

The decomposition into symmetrical components of phasors, that is, in steady-state and in the frequency domain, proposed by Fortescue [18], can be applied.

$$\begin{bmatrix} v_a^+ \\ v_a^- \\ v_a^o \end{bmatrix} = \left[T_{+-o}\right] \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{B.1a}$$

$$\left[T_{+-o}\right] = \frac{1}{3} \begin{bmatrix} 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \\ 1 & 1 & 1 \end{bmatrix} \tag{B.1b}$$

Where $\alpha = e^{j2\pi/3}$ also known as the Fortescue operator.

Another form of extraction is demonstrated below, obtaining the three-phase components of both positive and negative sequences.

$$\mathbf{v}^{+}_{abc} = \left[T_{+}\right]\mathbf{v}_{abc} = \frac{1}{3}\begin{bmatrix} 1 & \alpha & \alpha^2 \\ \alpha^2 & 1 & \alpha \\ \alpha & \alpha^2 & 1 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{B.2a}$$

$$\mathbf{v}^{-}_{abc} = \left[T_{-}\right]\mathbf{v}_{abc} = \frac{1}{3}\begin{bmatrix} 1 & \alpha^2 & \alpha \\ \alpha & 1 & \alpha^2 \\ \alpha^2 & \alpha & 1 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{B.2b}$$

B.2 Two-phase components in stationary reference frame

It is possible to represent three-phase stationary system in a two-phase stationary system by using the Clarke transform, as shown in Eq. B.3.

$$\begin{bmatrix} y_\alpha \\ y_\beta \end{bmatrix} = \left[T_{\alpha\beta}\right]\begin{bmatrix} y_a \\ y_b \\ y_c \end{bmatrix} \tag{B.3a}$$

$$\left[T_{\alpha\beta}\right] = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \tag{B.3b}$$

Here the zero component is neglected since it is considered that the system contains only three-wire connections.

Figure B.1 shows how the stationary reference frames are set in Cartesian coordinates. The two-phase disposition of the $\alpha\beta$-frame allows to treat signals with real and imaginary components.

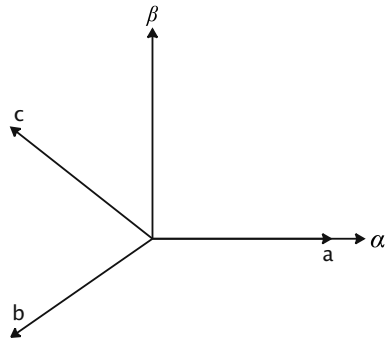


Figure B.1: Three-phase abc and two-phase $\alpha\beta$ stationary reference frames.

It is important to note that there are two ways of defining the transformation; one conserving the amplitude (abc-frame uses RMS values), and the other conserving the power (when the norm from both frames are equal).

Since the way the transformation previously defined is in power non-invariant form, in order to obtain the real power amplitudes it is necessary to use a scaling factor, as shown in Eq. B.7.

$$p_{\alpha\beta} = \frac{3}{2}(v_\alpha i_\alpha + v_\beta i_\beta) \tag{B.4a}$$

$$q_{\alpha\beta} = \frac{3}{2}(v_\alpha i_\beta - v_\beta i_\alpha) \tag{B.4b}$$

B.3 Two-phase components in synchronous reference frame

In case of grid synchronisation, it can be useful to operate with synchronous variables because it allows to tread dc signals instead of ac. It can be applied a rotational transformation directly from the two-phase stationary reference frame:

$$\begin{bmatrix} y_d \\ y_q \end{bmatrix} = \begin{bmatrix} T_{dq} \end{bmatrix} \begin{bmatrix} y_\alpha \\ y_\beta \end{bmatrix} \tag{B.5a}$$

$$\begin{bmatrix} T_{dq} \end{bmatrix} = \begin{bmatrix} cos(\theta_k) & sin(\theta_k) \\ -sin(\theta_k) & cos(\theta_k) \end{bmatrix} \tag{B.5b}$$

Figure B.2 depicts this transformation.

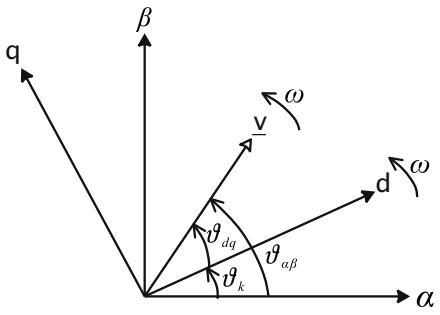


Figure B.2: Two-phase stationary reference frame to two-phase synchronous reference frame.

The combination of both rotational and Clarke transform yield the Park Transform, direct transformation between three-phase stationary reference frame into two-phase synchronous

reference frame.

$$\begin{bmatrix} y_d \\ y_q \end{bmatrix} = \begin{bmatrix} T_\theta \end{bmatrix} \begin{bmatrix} y_a \\ y_b \\ y_c \end{bmatrix} \tag{B.6a}$$

$$\begin{bmatrix} T_\theta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos(\theta_k) & cos(\theta_k - \frac{2\pi}{3}) & cos(\theta_k + \frac{2\pi}{3}) \\ -sin(\theta_k) & -sin(\theta_k - \frac{2\pi}{3}) & -sin(\theta_k + \frac{2\pi}{3}) \end{bmatrix} \tag{B.6b}$$

Similarly to the previous case, the transformation in B.6 is expressed conserving the peak amplitude of the three-phase components. Therefore, the real instantaneous active and reactive power contains a 3/2 scaling factor.

$$p_{dq} = \frac{3}{2}(v_d i_d + v_q i_q) \tag{B.7a}$$

$$q_{dq} = \frac{3}{2}(v_d i_q - v_q i_d) \tag{B.7b}$$

C Appendix - Modulation functions

Here are reported the modulation functions used in Double-Update mode.

$$\mathcal{F}_1(d)^p = \begin{cases} \dfrac{d-4/5}{1/5} & \text{if } d \geq \dfrac{4}{5}, \\ 0 & \text{if } d < \dfrac{4}{5}. \end{cases} \tag{C.1a}$$

$$\mathcal{F}_2(d)^p = \begin{cases} 1 & \text{if } d \geq \dfrac{4}{5}, \\ \dfrac{d-3/5}{1/5} & \text{if } \dfrac{3}{5} \leq d < \dfrac{4}{5}, \\ 0 & \text{if } d < \dfrac{3}{5}. \end{cases} \tag{C.1b}$$

$$\mathcal{F}_3(d)^p = \begin{cases} 1 & \text{if } d \geq \dfrac{3}{5}, \\ \dfrac{d-2/5}{1/5} & \text{if } \dfrac{2}{5} \leq d < \dfrac{3}{5}, \\ 0 & \text{if } d < \dfrac{2}{5}. \end{cases} \tag{C.1c}$$

$$\mathcal{F}_4(d)^p = \begin{cases} 1 & \text{if } d \geq \dfrac{2}{5}, \\ \dfrac{d-1/5}{1/5} & \text{if } \dfrac{1}{5} \leq d < \dfrac{2}{5}, \\ 0 & \text{if } d < \dfrac{1}{5}. \end{cases} \tag{C.1d}$$

$$\mathcal{F}_5(d)^p = \begin{cases} 1 & \text{if } d > \dfrac{1}{5}, \\ \dfrac{d}{1/5} & \text{if } d \leq \dfrac{1}{5}. \end{cases} \tag{C.1e}$$

By symmetry, the modulation functions for update on carrier valleys match the ones for update

on carrier peaks.

$$\mathcal{F}_1(d)^v = \mathcal{F}_5(d)^p \tag{C.2a}$$
$$\mathcal{F}_2(d)^v = \mathcal{F}_4(d)^p \tag{C.2b}$$
$$\mathcal{F}_3(d)^v = \mathcal{F}_3(d)^p \tag{C.2c}$$
$$\mathcal{F}_4(d)^v = \mathcal{F}_2(d)^p \tag{C.2d}$$
$$\mathcal{F}_5(d)^v = \mathcal{F}_1(d)^p \tag{C.2e}$$

Bibliography

[1] K. Friedrich, "Modern hvdc plus application of vsc in modular multilevel converter topology," in *2010 IEEE International Symposium on Industrial Electronics*, 2010, pp. 3807–3810. DOI: 10.1109/ISIE.2010.5637505.

[2] Y. Neyshabouri, K. K. Monfared, H. Iman-Eini, Q. Xiao, and M. Farhadi-Kangarlu, "Cascaded h-bridge based statcom with improved ride through capability of submodule failures," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 4, pp. 4034–4045, 2022. DOI: 10.1109/TIE.2021.3071703.

[3] M. Winkelnkemper, A. Korn, and P. Steimer, "A modular direct converter for transformerless rail interties," in *2010 IEEE International Symposium on Industrial Electronics*, 2010, pp. 562–567. DOI: 10.1109/ISIE.2010.5637826.

[4] A. El-Sanabary, G. Konstantinou, S. Mekhilef, C. Townsend, M. Seyedmahmoudian, and A. Stojcevski, "Medium voltage large-scale grid-connected photovoltaic systems using cascaded h-bridge and modular multilevel converters: a review," *IEEE Access*, vol. 8, pp. 223 686–223 699, Dec. 2020. DOI: 10.1109/ACCESS.2020.3044882.

[5] I. E. A. IEA, *Electricity - fuels & technologies - iea*, https://www.iea.org/fuels-and-technologies/electricity., Accessed: 2022-9-7, 2022.

[6] E. association for the cooperation of transmission system operators (TSOs) for electricity, *Grid map*, en, https://www.entsoe.eu/data/map/., Accessed: 2022-9-7.

[7] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings,*, vol. 3, 2003, 6 pp. Vol.3-. DOI: 10.1109/PTC.2003.1304403.

[8] B. Wu and M. Narimani, "Voltage source inverter fed drives," in *High-Power Converters and AC Drives*. 2017, pp. 287–308. DOI: 10.1002/9781119156079.ch12.

[9] R. H. Cuzmar, J. Pereda, and R. P. Aguilera, "Phase-shifted model predictive control to achieve power balance of chb converters for large-scale photovoltaic integration," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 10, pp. 9619–9629, 2021. DOI: 10.1109/TIE.2020.3026299.

[10] P. Poblete, S. Neira, R. P. Aguilera, J. Pereda, and J. Pou, "Sequential phase-shifted model predictive control for modular multilevel converters," *IEEE Transactions on Energy Conversion*, vol. 36, no. 4, pp. 2691–2702, 2021. DOI: 10.1109/TEC.2021.3074863.

[11] R. P. Aguilera, P. Acuna, X. Su, P. Lezana, and B. McGrath, "Sequential phase-shifted model predictive control for multicell power converters," in *2017 IEEE Southern Power Electronics Conference (SPEC)*, 2017, pp. 1–6. DOI: 10.1109/SPEC.2017.8333644.

[12] G. Walker, "Digitally-implemented naturally sampled pwm suitable for multilevel converter control," *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1322–1329, 2003. DOI: 10.1109/TPEL.2003.818831.

[13] X. Zhang and J. W. Spencer, "Study of multisampled multilevel inverters to improve control performance," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4409–4416, 2012. DOI: 10.1109/TPEL.2012.2187313.

[14] "Ieee recommended practice and requirements for harmonic control in electric power systems," *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)*, pp. 1–29, 2014. DOI: 10.1109/IEEESTD.2014.6826459.

[15] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics. Converters, Applications and Design*, third. John Wiley and Sons, Inc, 2003.

[16] R. Teodorescu, M. Liserre, and P. Rodriguez, "Grid synchronization in threephase power converters," in *Grid Converters for Photovoltaic and Wind Power Systems*. 2007, pp. 169–204. DOI: 10.1002/9780470667057.ch8.

[17] P. G. E. Bolzern, R. Scattolini, and N. L. Schiavoni, *Fondamenti di controlli automatici*. McGraw-Hill, 2008.

[18] C. L. Fortescue, "Method of symmetrical co-ordinates applied to the solution of polyphase networks," *Transactions of the American Institute of Electrical Engineers*, vol. XXXVII, no. 2, pp. 1027–1140, 1918. DOI: 10.1109/T-AIEE.1918.4765570.