POLITECNICO DI TORINO

Master of Science in Electrical Engineering

Master Thesis Dissertation

Design of an Industrial Power Converter for Adjustable Speed Drives

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Summary

Electrolytic capacitors are nowadays widely used as DC link for industrial Adjustable Speed Drives (ADS), however they present a lower lifetime with respect to other capacitor technologies. For this reason, there is the trend to replace electrolytic capacitors with film ones to increase the system reliability. In addition, film capacitors are characterized by a much smaller capacitance per volume with respect to electrolytic ones. Thus, the DC link capacitance can be drastically reduced, leading to the concept of slim DC link power converters. However, by decreasing of orders of magnitude the dc-link capacitance, resonances between the dc-link capacitors and the grid inductance can occur. These resonances cause very high dc-link voltage ripple and the increase of grid current Total Harmonic Distortion (THD). This problem has to be properly solved at control level to avoid the use of other hardware components.

The goal of my master thesis is the design of a slim dc-link drive system for ADSs featuring low THD of input grid current, being suitable for data centers' cooling system. This is done through the following steps: electrical stress calculation, components choice, losses computation and cooling system design. In addition, the thesis proposes a method to actively damp the DC link resonances, using motor control.

Acknowledgements

Innanzi tutto, voglio ringraziare il prof.Radu Bojoi, per l'opportunità e la fiducia che mi ha dato e le cui lezioni sono da sempre state per me la principale fonte di conoscenza, ammirazione e ispirazione; e Fabio Mandrile, che con la sua grandissima disponibilità e pazienza mi ha seguito ed insegnato tantissimo, diventando per me un punto di riferimento ed un esempio da seguire.

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Simone

To my parents and to all those who supported me in these years.

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Chapter 1

Introduction

Power electronic converters are widely used and consolidated in traditional industrial applications guaranteeing high efficiency and versatility in the production systems. This thesis focus on the design of an industrial converter for Heating, Ventilation and Air Conditioning (HVAC) systems, which require cost effective solutions with low grid current Total Harmonic Distortion (THD) and high reliability.

1.1 Problem Statement

Electrolytic capacitors are commonly used in industrial application as dc-link for its high capacitance per volume and cost. However, they are not a lot reliable being statistically one the most probable cause of failure in a power converter, therefore, there is the trend to replace it with a more reliable capacitor technology.

Film capacitors are the best solution in terms of reliability due to their self-healing capability in case of failure. However, they presents a capacitance per volume order of magnitude lower than the electrolytic one and an higher price per volume. As a consequence, maintaining the same dc-link capacitance, the price and particularly the size of the converter increases a lot, up to not acceptable values.

To solve this problem the idea is to reduce the dc-link capacitance with respect to the traditional values, driving it to the concept of slim dc-link converter. However, this drastic reduction of the dc-link capacitance can lead to dangerous resonances due to interaction with the grid inductance. This problem has to be solved at control level to avoid the use of extra components that would decrease the power density.

1.2 Thesis Objective

The objective of this thesis is to completely design a 7.5kW industrial converter, starting from the active switch sizing up to the heatsink sizing for the thermal management. Moreover, the control to damp the resonances is developed and all the system is

simulated to evaluate the correctness of the control algorithm. Finally, the converter is experimentally tested to confirm the simulation results.

1.3 System Description

The required converter specifications are resumed in Tab.1.1. It can to be connected both to the European and American grid with an output power of 7.5kW and a desired dc-link capacitance of approximately $20\mu F$. The converter can be connected only to grid which have a maximum Short Circuit Ratio (SCR) of 100. Moreover, one requirement is that the converter has the ability to work in extremely hot environments with ambient temperature of 65°C.

Table 1.1: Main converter specifications.

Grid	3-phase	RMS Grid Voltage	380V (EU)/460V (USA)
DC-link Capacitance	$\simeq 20\mu F$	AC/DC Conversion	Diode bridge rectifier
DC/AC Conversion	Two-level VSI	Power	7.5kW
Grid SCR	≤ 100	Communication	CAN

1.3.1 Hardware Block Scheme

The converter structure consists of: a three-phase diode rectifier connected to the grid, the film dc-link capacitor and an IGBT-based two-level Voltage Source Inverter (VSI) to control the electric machine, as shown in Fig.1.1. The control routine requires the measurements of v_{dc}, i_{abc} for the motor control, the measure of the junction temperature T_j of the module for safety reasons and a CAN bus to communicate with the external world.

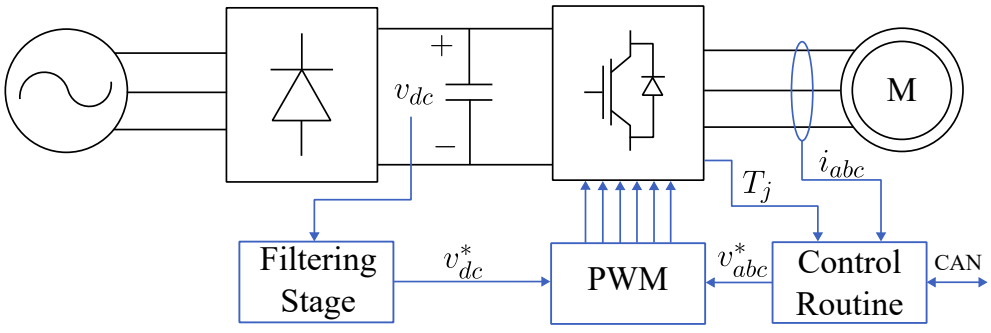


Figure 1.1: Considered variable speed drive hardware structure..

Chapter 2

Voltage Modulation using Virtual Positive Impedance Concept

Fig.2.1 shows the circuit diagram representative of the schematic in Fig.1.1. The figure highlight the simplified circuit, as in Fig.2.2, useful to develop a mathematical model to evaluate the converter behavior, in which $R_{gd} = 2R_g$ and $L_{gd} = 2L_g$. The inverter and the electric machine are modeled as a current generator which absorb i_{inv}. Instead, the diode rectifier is represented with a voltage source as in (2.1). The voltage drop in v_{in} during the commutation period T_{cc} is taken into account in (2.2), calculated as in (2.3), where $i_g(t_0)$ is the grid current at the initial time when the commutation start [1].

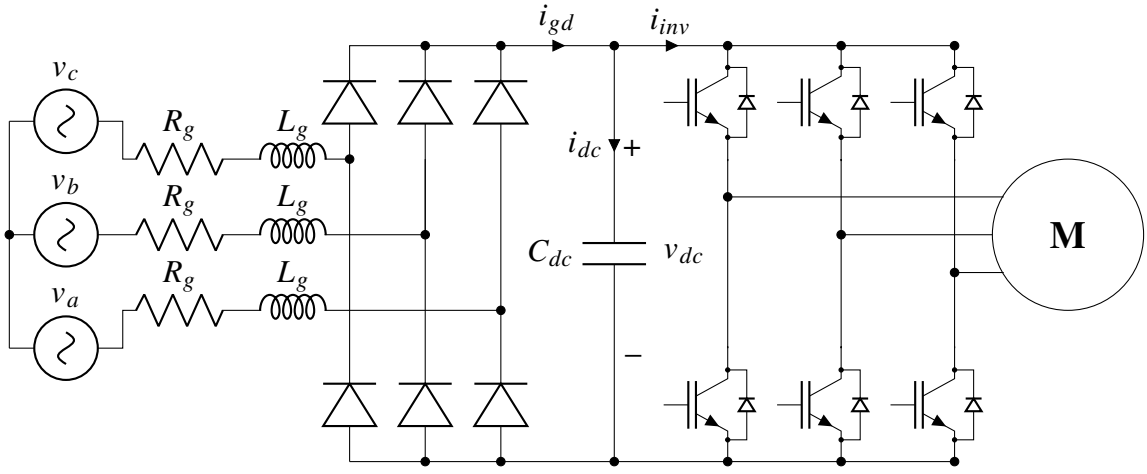


Figure 2.1: Circuit diagram.

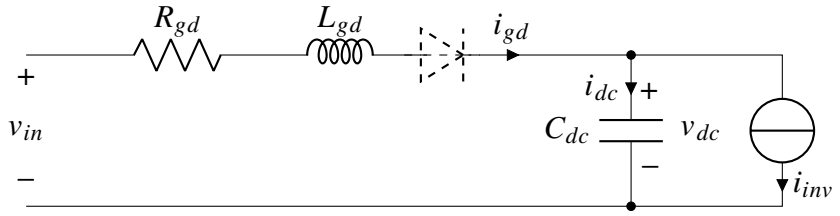


Figure 2.2: Simplified circuit diagram.

$$v_{in} = \frac{3\sqrt{3}V_{ph}}{\pi}\left(1 - \sum_{n=1}^{\infty} \frac{2}{(6n)^2 - 1} cos(6n\omega_g t)\right) \tag{2.1}$$

$$\Delta v_{in} = \sqrt{3}V_{ph}(sin(\pi/3) - sin(\pi/3 + \omega_g t)), \quad 0 \leq t \leq Tcc \tag{2.2}$$

$$T_{cc} = \frac{1}{\omega_g} cos^{-1}\left(1 - \frac{2\omega_g L_g}{\sqrt{3}V_{ph}} i_g(t_{c0})\right) \tag{2.3}$$

The inverter current consists of two main components: one constant and one related to the oscillations (2.4). In (2.5) it is possible to define the small signal impedance of the inverter, which is a negative value.

$$i_{inv} = I_{inv} + \tilde{i}_{inv} = \frac{P_L}{V_{dc} + \tilde{v}_d c} \simeq \frac{P_L}{V_{dc}} - \frac{P_L}{V_{dc}^2}\tilde{v}_{dc} \tag{2.4}$$

$$Z_{inv} = \frac{\tilde{v}_{dc}}{\tilde{i}_{inv}} = -\frac{V_{dc}^2}{P_L} \tag{2.5}$$

In (2.6) are reported the state equation of the simplified system (Fig.2.2). Using (2.4) and (2.6), the v_{dc} differential equation is obtained (2.7).

$$\begin{cases} L_{gd}\frac{di_g}{dt} = v_{in} + \Delta v_{in} - R_{gd} i_g - v_{dc} \\ C_{dc}\frac{dv_{dc}}{dt} = i_g - i_{inv} \end{cases} \tag{2.6}$$

$$\frac{d^2 v_{dc}}{dt^2} + \left(\frac{R_{gd}}{L_{gd}} - \frac{P_L}{C_{dc}V_{dc}^2}\right)\frac{dv_{dc}}{dt} + \frac{1}{C_{dc}L_{gd}}\left(1 - \frac{R_{g,eq}P_L}{V_{dc}^2}\right)v_{dc} = \frac{v_{in} + \Delta v_{in}}{C_{dc}L_{gd}} - \frac{2R_{gdP_L}}{L_{gd}C_{dc}V_{dc}} \tag{2.7}$$

It can be notice that Δv_{in} only appears at in the right hand of the equation, thus it only influence the initial value of the particular solution. The characteristic equation of the second-order system in the Laplace domain can be obtained as:

$$s^2 + \underbrace{\left(\frac{R_{gd}}{L_{gd}} - \frac{P_L}{C_{dc}V_{dc}^2}\right)}_{a_{10}} s + \underbrace{\frac{1}{C_{dc}L_{gd}}\left(1 - \frac{R_{gd}P_L}{V_{dc}^2}\right)}_{a_{20}} = 0. \tag{2.8}$$

The system is stable when the coefficients a_{10} and a_{20} are greater than zero, according to the Routh-Hurwitz criterion. In this case, $a_{20} > 0$ because, in general, V_{dc}^2/P_L is much higher than R_{gd}. Therefore, the system stability depends on the sign of coefficient a_{10}. In standard applications, where the dc-link capacitance is large, the system is stable. However, in case of the reduced capacitance of the slim dc-link drive, the stability condition $a_{10} > 0$ is not satisfied leading to oscillations and instability in the dc-link voltage and grid current. The system have to be damped at control level to avoid this behavior.

The chosen method to actively damp the oscillations is based on a proper voltage modulation in which the sign of Z_{inv} is changed. The idea is to change the dc-link voltage reference v_{dc}^* by reversing the sign of $\tilde{v}_{dc}$. In this way the power absorbed by the load contains not only the constant term but even the extra oscillating components proportional to $\tilde{v}_{dc}$. The load power P_L is calculated in (2.9) using the vector scalar product, in which $\bar{v}_{abc}$ is the machine voltage vector and $\bar{i}_{abc}$ is the machine current vector. The dc-voltage reference is reconstructed as $v_{dc}^* = V_{dc} - \tilde{v}_{dc}$ instead of $V_{dc} + \tilde{v}_{dc}$, therefore, the output voltage vector of the inverter becomes $\bar{v}_{abc,rec}$ (2.10) instead of $\bar{v}_{abc}$ [1].

$$P_L = \bar{v}_{abc} \cdot \bar{i}_{abc} \tag{2.9}$$

$$\bar{v}_{abc,rec} = \frac{\bar{v}_{abc}}{v_{dc}^*} v_{dc} = \bar{v}_{abc} \frac{V_{dc} + \tilde{v}_{dc}}{V_{dc} - \tilde{v}_{dc}} \tag{2.10}$$

Consequently, the load power becomes $P_{L,rec}$ instead of P_L (2.11), therefore, the inverter current can be calculated as in (2.12). It is possible to notice that the inverter impedance is now positive.

$$P_{L,rec} = \bar{v}_{abc,rec} \cdot \bar{i}_{abc} = \frac{V_{dc} + \tilde{v}_{dc}}{V_{dc} - \tilde{v}_{dc}} \bar{v}_{abc} \cdot \bar{i}_{abc} = P_L \frac{V_{dc} + \tilde{v}_{dc}}{V_{dc} - \tilde{v}_{dc}} \bar{v}_{abc} \tag{2.11}$$

$$i_{inv} = I_{inv} + \tilde{i}_{inv} = \frac{P_{L,rec}}{v_{dc}} = \frac{P_L}{V_{dc} - \tilde{v}_{dc}} \simeq \frac{P_L}{V_{dc}} + \frac{P_L}{V_{dc}^2} \tilde{v}_{dc} \tag{2.12}$$

Following the same step as before, in (2.12) is shown the system characteristic equation. Now, the two new coefficients a_{11} and a_{21} are always greater than zero, guaranteeing the system stability in every condition.

$$s^2 + \underbrace{\left(\frac{R_{gd}}{L_{gd}} + \frac{P_L}{C_{dc} \cdot V_{dc}^2} \right)}_{a_{11}} s + \underbrace{\frac{1}{C_{dc} \cdot L_{gd}} \left(1 + \frac{R_{gd} \cdot P_L}{V_{dc}^2} \right)}_{a_{21}} = 0 \tag{2.13}$$

It is possible to further generalize the virtual positive impedance concept by introducing the coefficients k_v and k_{v0} in the reconstructed voltage, as in (2.14). According to what previously done, in (2.15) and (2.16) are reported the main results of the generalized system.

$$v_{dc}^{*} = k_{v0}V_{dc} - k_{v}\tilde{v}_{dc} \tag{2.14}$$

$$i_{inv} = I_{inv} + \tilde{i}_{inv} \simeq \frac{P_L}{k_{v0}V_{dc}} + \frac{k_v P_L}{k_{v0}^2 V_{dc}^2}\tilde{v}_{dc} \tag{2.15}$$

$$s^2 + \underbrace{\left(\frac{R_{gd}}{L_{gd}} + \frac{k_v P_L}{C_{dc}k_{v0}^2 V_{dc}^2}\right)}_{a_{12}} s + \underbrace{\frac{1}{C_{dc}\cdot L_{gd}}\left(1 + \frac{k_v R_{gd}\cdot P_L}{k_{v0}^2 V_{dc}^2}\right)}_{a_{22}} = 0 \tag{2.16}$$

It is important to notice that if $k_v \geq 0$ the system is always stable, because the coefficients a_{12} and a_{22} are greater than zero. In this condition, when k_{v0} is reduced a_{12} increases and consequently even the damping effect on $\tilde{v}_{dc}$ increases. However, the large signals of the commanded reference voltages are lower than that of the real machine voltages, causing difficulties when applying state observers to estimate machine flux linkage, speed, and position. As a consequence, it is better to keep k_{v0} to one and manipulating only k_v for the active damping control.

Chapter 3

Hardware Design

After explaining the control strategy, this chapter aims to size and design the power electronic converter. The schematics have been developed using the software Altium Designer. In Fig.3.1 are represented the main functional block, divided in high voltage-high power blocks (red) and low voltage-low power one (green), that have to be design to develop the converter. In particular:

- Power Module: represents the heath of the converter in which take place the power conversion;
- Power Supply: containing all the auxiliary supply circuits to satisfy the different supply voltage requirements of all the devices;
- Gate Drivers:includes the gate driving circuits;
- Analog Conditioning: to condition the signals coming from the various sensors and adapting it to the microcontroller input;
- Sensors: includes all the devices that are used to measure the quantities required by the control, such as the phase currents or the dc-link voltage;
- Microcontroller: representing the intelligent part of the converter, where the control algorithm run and the commands are actuated;
- Communication: including the bidirectional communication system of the converter with the external world;
- EMI Filters: containing the grid filters to comply the EMI standars.

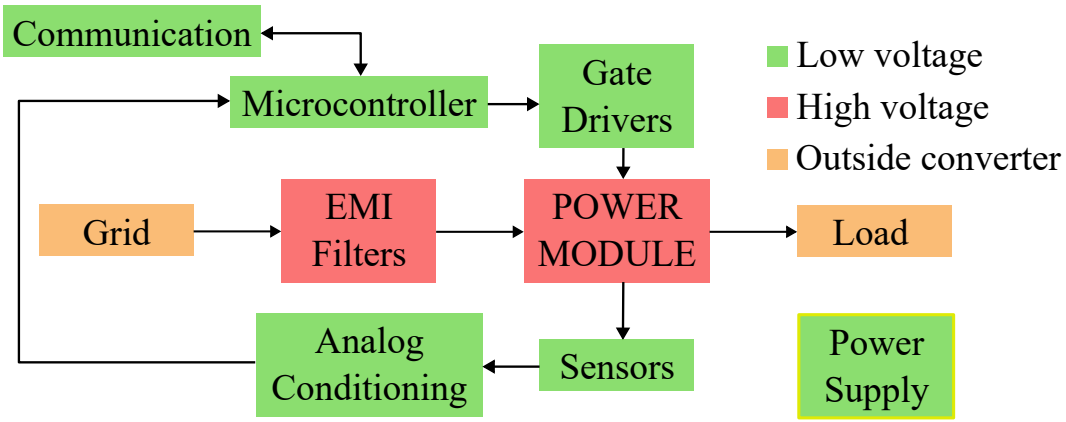


Figure 3.1: Hardware main functional blocks.

The hardware design procedure consists of consecutive steps, summarized in Fig.3.2, starting from the module choice and finishing with the thermal design validation and the low voltage components choice. In particular the main steps are:

- Module choice: based on figures of merit;
- Losses evaluation: computation of the switches losses in worst case condition;
- Heatsink choice: based on the total power loss information is computed the minimum thermal resistance required and consequently the heatsink is chosen;
- Thermal validation: thermo-fluid dynamic simulation to validate the sizing, if it is necessary have a forced cooling system a fan can be added;
- Iterations: if the thermal limits are not satisfied, another heatsink is choice or, in some cases, the starting module is discarded and another one is chosen;
- Low voltage component choice: define the main low voltage devices, such as sensors, gate drivers and power supply.

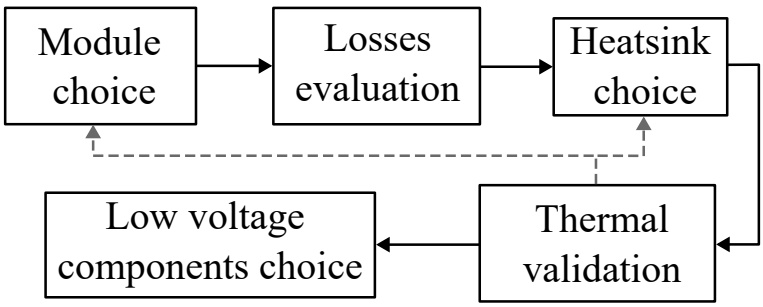


Figure 3.2: Hardware design procedure block scheme.

3.1 Figure of Merit

The traditional IGBT figure of merit is calculated as the product between the collector-emitter threshold voltage and turn-off energy loss, as in (3.1). These two parameters are in opposition to each other, decreasing one the other increases and vice versa. Therefore, lower values of FOM means better electrical performances.

$$FOM = E_{off} \cdot v_{CE,on} \tag{3.1}$$

However, this FOM does not provide much information about the module package. For this reason, it is necessary to take into account also the thermal properties of the module casing. In (3.2) it is proposed a new figure of merit called Package FOM (PFOM) that consider the thermal characteristics of the module. Lower thermal resistance R_{th} and exchange surface S_{pack} means better thermal properties and higher power density, instead, higher maximum junction temperature $T_{j,max}$ allow to better exploit the module, giving an higher temperature range that permit less efforts in the cooling system design or higher overload capability.

$$PFOM = E_{off} \cdot v_{CE,on} \frac{R_{th} \cdot S_{pack}}{T_{j,max}} \tag{3.2}$$

By substituting $T_{j,max} = P_{d,max}/R_{th}$ in (3.2) the PFOM is rewritable as in (3.3), in which, at numerator there are the electrical characteristics and at denominator the thermal one.

$$PFOM = \frac{E_{off} \cdot v_{CE,on}}{P_{d,max}/S_{pack}} \tag{3.3}$$

3.1.1 Module Comparison

As previously said, the required module topology have to include: a three phase diode bridge rectifier, a two level voltage source IGBT inverter, a brake leg, to dissipate eventual power coming from the electric machine, and a temperature sensor to monitor the mean internal temperature of the module.

To choose the module a comparison between similar devices from different manufacturer, such as Infineon, Vincotech, Semikron and Starpower, is performed. For semplicity, in Tab.3.1 are reported only the modules with the best performances.

As it could have been expected, in general the IGBT7-based modules feature the best electrical characteristics, however, in some cases due to its higher thermal resistance and different package the overall performance is worst than the IGBT4-based.

Table 3.1: FOM and PFOM comparison.

	Part N°	IGBT Type	FOM	PFOM
INFINEON	FP15R12W1T7	IGBT7	1.47	24.6
	FP15R12W1T7P	IGBT7	1.47	25.4
	FP15R12W1T4	IGBT4	1.53	34.5
	FP15R12W2T4	IGBT4	1.48	38.4
VINCOTECH	V23990-P840-A58Y-PM	IGBT4	1.65	**10.3**
	V23990-P588-A41-PM	IGBT4	1.61	18.6
	80-M112PMA015M7	IGBT7	1.68	11.3
	10-EY12PMA015SC	IGBT4	1.63	19.3

The module V23990-P840-A58Y-PM has the best PFOM, however, after a thermo-fluid dynamic analysis, to maintain its temperature in a safe range it would require a very performant heatsink, due to its low exchange surface. This would increase a lot the cost of the converter, therefore, this module was discarded. At this point, looking at the price of the IGBT7-based module, it is possible to notice that they present an higher price with respect to the IGBT4 one. Therefore, it is decided to maintain the price of the converter low by not choosing the IGBT7-based modules. For all this reason, it is chosen the module V23990-P588-A41-PM due to its best compromise in terms of electrical and thermal characteristic and price.

3.1.2 PFOM Validation

To validate the results of the PFOM the module V23990-P840-A58Y-PM (IGBT4) and the 80-M112PMA015M7 (IGBT7) are compared, the first module is characterized by a lower PFOM (best performance) with respect to the second one. In Tab.3.2 are reported the parameters for the PFOM calculation at 25°C. It is possible to notice that in this case the IGBT4-based module has a bit better electrical performances and almost half the package interface surface with respect to other one, howerver, the IGBT7-based module has lower thermal resistance so better thermal properties. In Fig.3.3 are shown the power losses and the junction temperature of the to modules. At steady state the differences among the two junction temperature are practically negligible, the power loss difference its around 15W and the surface of the IGBT7-based module is almost double of the other. This lead to have for the IGBT4 inverter higher efficiency and higher power density, exploiting the same junction temperature, with respect to IGBT7 one. These results are coherent with the PFOM one, validating the correctness of this new figure of merit.

Table 3.2: Modules electrical and thermal specifications for PFOM comparison.

	E_{off}	$v_{CE,on}$	R_{th}	S_{pack}
V23990-P840-A58Y-PM	0.883mJ	1.87V	1,45K/W	$753.7mm^2$
80-M112PMA015M7	0.987mJ	1.7V	1,21K/W	$1391.3mm^2$

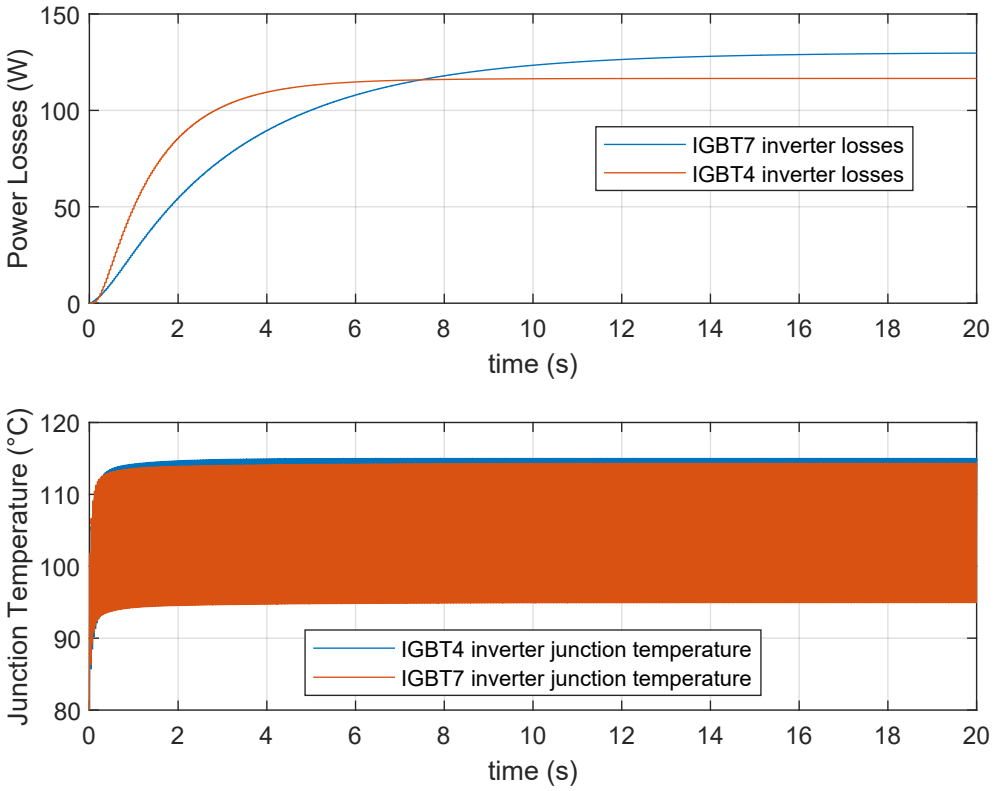


Figure 3.3: Power losses and junction temperature comparison.

3.2 Power Module

In Fig.3.4 and Fig.3.5 are respectively represented the chosen module 3D model and its main dimensions. In Fig.3.6 is shown from datasheet the internal topology of the module, it possible to notice that a temperature sensor and a brake leg are included.

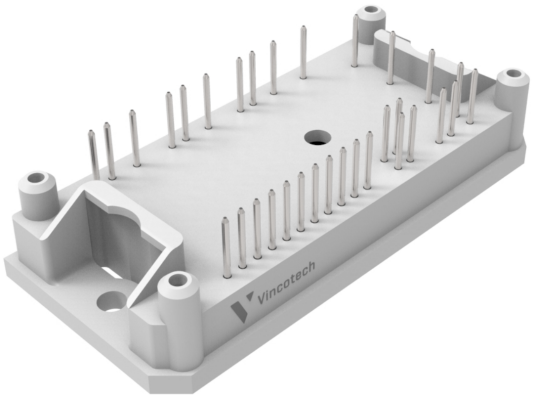


Figure 3.4: Module 3D model [2].

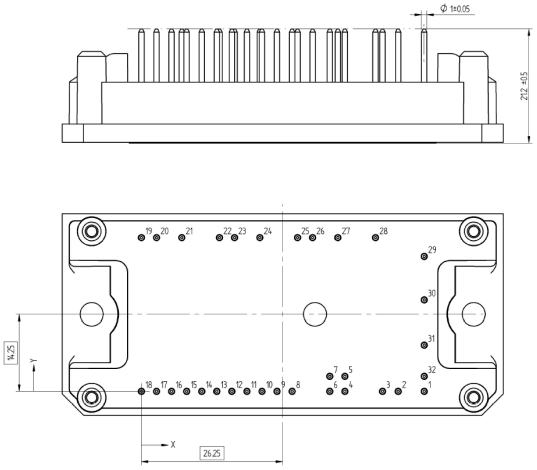


Figure 3.5: Module dimensions [2].

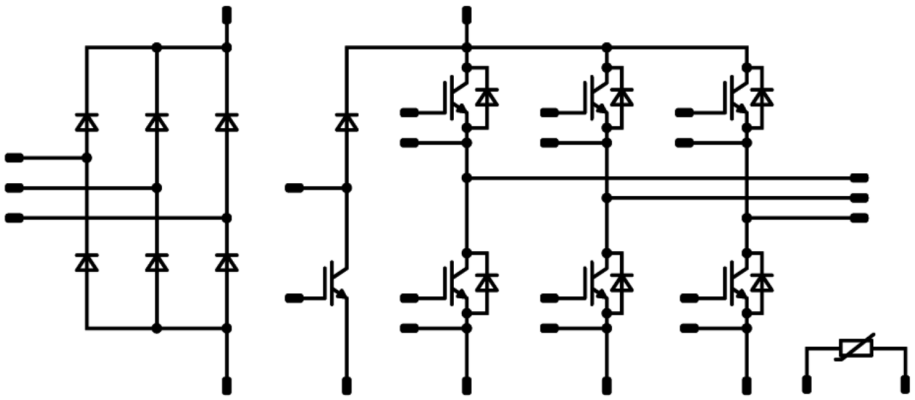


Figure 3.6: V23990-P588-A41-PM module internal connections [2].

In the following tables (Tab.3.3 and Tab.3.4) are reported the main module and internal switches specifications. In particular, for the IGBT, inverter anti-paralle diode (FWD) and three phase bridge diode (RECTD) the specifications are referred to a junction temperature T_j=150°C, gate resistance R_G=32Ω, gate-emitter voltage V_{GE}=+15V, dc bus voltage V_{dc}=600V.

Table 3.3: Main module specifications.

$V_{dc,nom}$	$I_{rms,nom}$	T_j max
1200V	15A	175°C

Table 3.4: Main switches specifications.

IGBT	V_{CES}	I_C	$T_{j,max}$	$R_{th,j-s}$
	1200V	23A	175°C	1.35K/W
FWD	V_{RRM}	I_F	$T_{j,max}$	$R_{th,j-s}$
	1200V	23A	175°C	1.83K/W
RECTD	V_{RRM}	I_F	$T_{j,max}$	$R_{th,j-s}$
	1200V	46A	150°C	1.25K/W

3.3 Stress Calculation and Plecs Simulation

At this point it is necessary to evaluate, in the worst case, the power losses in the power module to perform all the thermal simulations required to check the correctness of the design. Considering the worst case, the calculations are referred to the EU standard because it is characterized by a lower voltage with respect to the USA one and consequently higher current to satisfy the same load, this means higher losses so higher junction temperature of the switches. This analysis is performed once using analytical calculations and once using the software Plecs, then the two results are compared to have a confirm of the correctness of the results.

3.3.1 Analytical Calculations

To analytically calculate the power losses it is necessary to calculate the main dc-voltage component V_{dc} (3.4), the fundamental inverter current peak $\hat{I}_1$ (3.5) and the modulation index m, defined as peak of the fundamental inverter voltage and half of V_{dc}. Considering a regular sampled voltage modulation with middle voltage third harmonic injection, the value of the modulation index is $2/\sqrt{3}$.

$$V_{dc} = \frac{3\sqrt{3}V_{ph}}{\pi} = 513V \tag{3.4}$$

$$\hat{I}_1 = \frac{4S}{3mV_{dc}} = 22.51A \tag{3.5}$$

$$m = \frac{\hat{V}_{out_1}}{V_{dc}/2} = \frac{2}{\sqrt{3}} = 1.1547 \tag{3.6}$$

In Tab.3.5 are reported the all the parameters to compute the losses in the transistor (T) and the diode (D) of the inverter, as in (3.7), (3.8), (3.9) and (3.10). This parameters are obtained approximating the switches characteristics with the linear one, as a consequence, it is expected to see some differences in the analytical calculations and Plecs

results.

Where:

- S: nominal apparent power of the load;
- P: nominal power of the load;
- I_{out}: nominal rms output current;
- $cos\phi$ is the power factor of the electic machine;
- T_j: junction temperature at which the losses are calculated;
- V_{ref}: reference dc-link voltage at which the parameters are reported in the datsheet;
- T_{ref}: reference junction temperature at which the parameters are reported in the datsheet;
- E_{sw}^{TOT}: sum of the turn-on and turn off energy losses (reported at the reference value previously declared);
- $TC_{E_{sw}}$: coefficient which adjust the IGBT switching losses in case of $T_j \neq T_{ref}$;
- $TC_{E_{rr}}$: coefficient which adjust the IGBT switching losses in case of $T_j \neq T_{ref}$;
- k_{vT}: exponential parameters which adjust the IGBT switching losses in case of $V_{dc} \neq V_{ref}$;
- k_i: exponential parameters which adjust the forward diode switching losses in case of $I_{out} \neq I_{ref}$;
- k_v: exponential parameters which adjust the forward diode switching losses in case of $V_{dc} \neq V_{ref}$;
- $V_{CE0}(T_j)$: IGBT collector-emitter threshold voltage at T_j;
- $R_{CE}(T_j)$: IGBT collector-emitter resistance at T_j;
- $V_{F0}(T_j)$: forward diode threshold voltage at T_j;
- $R_F(T_j)$: forward diode resistance at T_j;
- V_{th}: rectifier diode threshold voltage at T_j;
- $R_{D,on}$: rectifier diode resistance at T_j.

Table 3.5: Parameters for power loss computation.

S	P	$cos\phi$	T_j	V_{ref}	T_{ref}	E_{sw}^{TOT}	$TC_{E_{sw}}$	$TC_{E_{rr}}$
10kVA	7.5kW	0.85	150°C	600V	150°C	1.61mJ	0.003 1/K	0.006 1/K
k_{vT}	k_i	k_v	$V_{CE0}(T_j)$	$R_{CE}(T_j)$	$V_{F0}(T_j)$	$R_F(T_j)$	V_{th}	$R_{D,on}$
1.4	0.6	0.6	0.8V	0.105Ω	0.6V	0.05 Ω	0.6V	0.035 Ω

$$P_{cond}^{T} = \left(\frac{1}{2\pi} + \frac{m \cdot cos\phi}{8}\right) V_{CE0}(T_j)\hat{I}_1 + \left(\frac{1}{8} + \frac{m \cdot cos\phi}{3\pi}\right) R_{CE}(T_j)\hat{I}_1^2 = 17.26W \tag{3.7}$$

$$P_{sw}^{T} = f_{sw} E_{sw}^{TOT} \frac{\sqrt{2}}{\pi} \frac{I_{out}}{I_{ref}} \left(\frac{V_{dc}}{V_{ref}}\right)^{k_{vT}} (1 + TC_{E_{sw}}(T_j - T_{ref})) = 10.17W \tag{3.8}$$

$$P_{cond}^{D} = \left(\frac{1}{2\pi} - \frac{m \cdot cos\phi}{8}\right) V_{F0}(T_j)\hat{I}_1 + \left(\frac{1}{8} - \frac{m \cdot cos\phi}{3\pi}\right) R_F(T_j)\hat{I}_1^2 = 1.02W \tag{3.9}$$

$$P_{sw}^{D} = f_{sw} E_{rr}^{TOT} \frac{\sqrt{2}}{\pi} \left(\frac{I_{out}}{I_{ref}}\right)^{k_i} \left(\frac{V_{dc}}{V_{ref}}\right)^{k_v} (1 + TC_{E_{rr}}(T_j - T_{ref})) = 5.31W \tag{3.10}$$

To calculate the three phase diode bridge rectifier losses it necessary to compute the mean and RMS diode current ($I_{AK,mean}$ and $I_{AK,rms}$ respectively), starting from main dc current I_d (3.11). Even in this case the diode conduction characteristic is linearized, therefore, as previously said, little differences in the results among the two calculation approach are expected.

$$\begin{aligned} I_d &= P/Vdc = 14.6A \\ I_{AK,mean} &= I_d/3 = 4.87A \\ I_{AK,rms} &= I_d/\sqrt{3} = 8.44A \end{aligned} \tag{3.11}$$

$$P_{cond}^{D,RECT} = V_{th} I_{AK,mean} + R_{D,on} I_{AK,rms}^2 = 5.41W \tag{3.12}$$

Knowing all the power losses contribution of the single switches it possible to obtain the total losses of the module summing it all and multiply it by the number of corresponding switches, as in (3.13).

$$P_{TOT} = 6 \cdot (P_{cond}^{T} + P_{sw}^{T} + P_{cond}^{D} + P_{sw}^{D} + P_{cond}^{D,RECT}) = 244.60W \tag{3.13}$$

3.3.2 Plecs Simulation

The software Plecs allows to simulate both the electrical and thermal behaviour, however, this let the simulation more complex and slower. For this reason, to reduce the computation time the system is divided in two sub-systems:

- Inverter side (Fig.3.7), where: the voltage source is constant and equal to the constant value of the dc-link voltage, the control is simplified without considering the voltage modulation using the vitual positive impedance concept and the electric machine is modeled as a sinusoidal current source which absorb the nominal power;
- Grid side (Fig.3.8), where: the grid is modeled with a three phase voltage generator (380Vrms, 50Hz) and a resistors and inductances which are calculated dependently of the Short Circuit Ratio (SCR), the dc-link capacitor is modeled with a capacitance and a resistance (ESR) and the inverter is modeled as a current source which absorb its mean dc current (neglecting ripple).

To evaluate the losses in worst case, in the thermal models of the switches the thermal impedance it is not implemented (imposed zero) and the temperature source is considered at 150°C. This correspond to impose the junction temperature to 150°C, therefore, the losses are calculated at that temperature and in this way it is possible to compare them with the analytical calculated one.

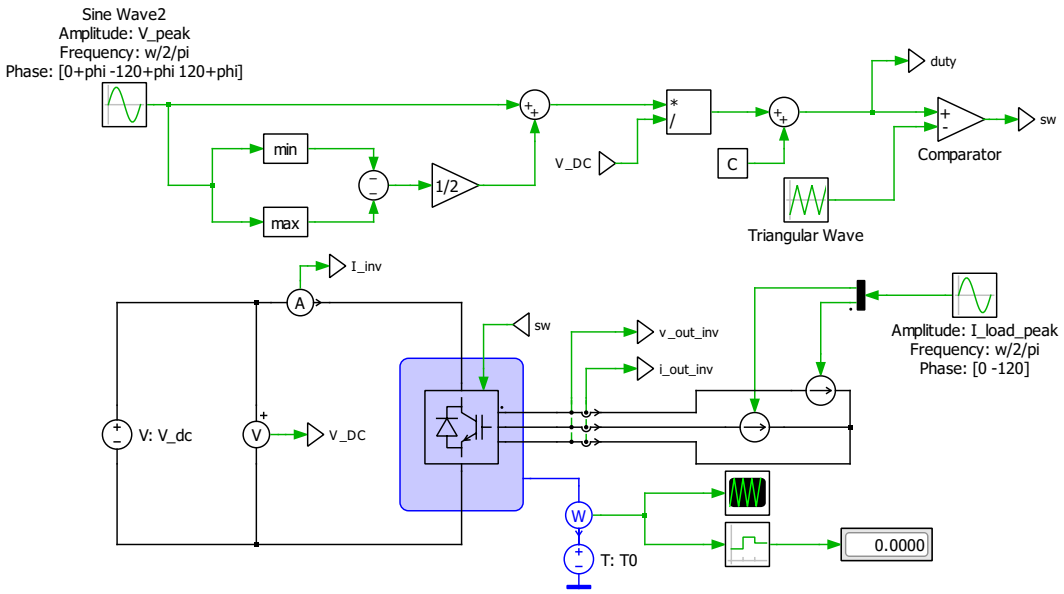


Figure 3.7: Simplified Plecs inverter schematic for power loss evaluation.

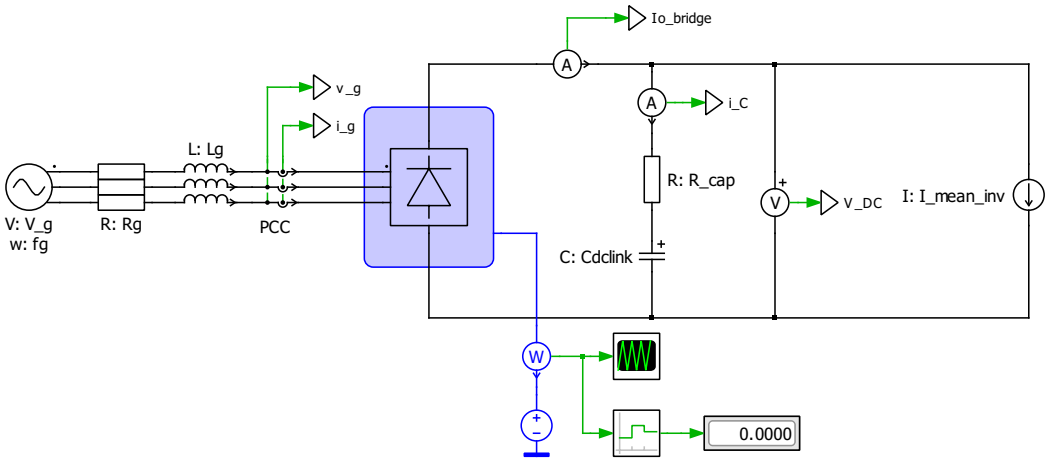


Figure 3.8: Simplified Plecs diode bridge schematic for power loss evaluation.

In Tab.3.6 are compared the output results coming from the analytical calculations and the Plecs simulation. It is possible to notice that the results are very close to each other, as previously said, the small differences are related to the linear approximation in the conduction switches in the analytical calculation characteristics and the exponential coeffiecient approximation (k_{vT},k_v,k_i).

Table 3.6: Analytical calculations and Plecs simulation results comparison.

	P^T_{cond}	P^T_{sw}	P^D_{cond}	P^D_{sw}	$P^{D,RECT}_{cond}$	P_{TOT}
Analyt. Calc.	17.26W	10.17W	1.02W	5.31W	5.41W	**235.1W**
Plecs Sim.	17.29W	10.78W	0.51W	4.83W	5.42W	**233.2W**

Including the thermal impedance characteristics in the switches thermal model it is possible to evaluate the temperature transient and the steady state behaviour, in particulat in Fig.3.9 are reported the mean switches junction temperature and in Tab.3.7 the maximum steady state values. In this case, as declared in the datasheet of the module, the thermal impedance characteristic includes the case to sink thermal resistance ($R_{th,c-s}$), with a thermal paste with a thermal conductivity parameter of 3.4W/mK, as interface between the module and the heatsink. Moreover, the heatsink temperature T_0 is fixed at 80°C, this value is considered as a reasonable maximum value that have to be considered as a specification in the heatsink design part. Finally, it is possible to notice that at steady state the maximum junction temperature of the switches are extensively inside the corresponding maximum values, guaranteeing a wide termperature margine useful in case of transient overload.

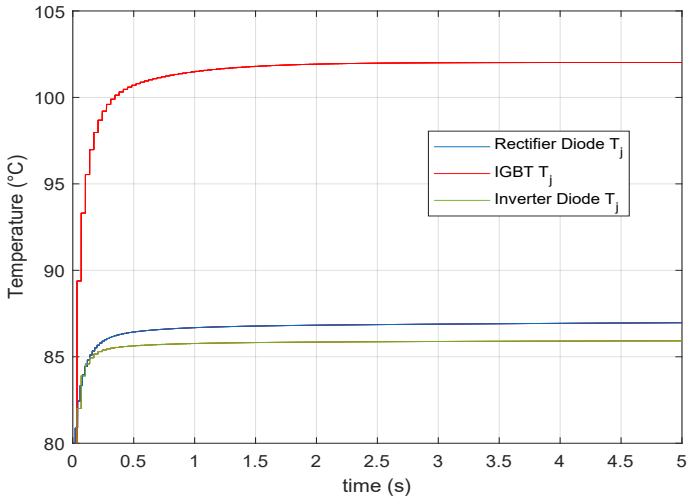


Figure 3.9: Mean switches junction temperatures.

Table 3.7: Maximum steady state switches junction temperature.

	IGBT	FWD	RECTD
$T_{j,MAX}$	122°C	89.5°C	88.5°C

3.4 Gate Drivers

The output command switch signals of the microcontroller GPIO has a maximum voltage of 3.3V and can provide only limited current to avoid damaging the device. For these reasons it is necessary a proper gate driver which allow to pilot the IGBT at higher voltage and consequently increase the transistor performances, moreover, it can provide an higher current to charge the IGBT gate capacitance to turn on the device. For the high switches, to separate the low power side (primary) to the high power (secondary) one it is mandatory tho choose an isolated gate driver. The chosen gate driver is the UCC21220, from Texas Instruments, which is an isolated dual channel gate driver with capacity barrier that guarantee high noise immunity and can provide up to 4A output current. Moreover, the gate driver has an disable pin (DIS) which allow to shut down the output commands, this pin is connected to a microcontroller GPIO, when the logic input is low the system is enabled and when high is disabled. All supplies have undervoltage lockout (UVLO) and active pull down protection clamping the output below 2.1V when they are not powered or floated.

The UCC21220 maximum ratings are summarized in Tab.3.8 and its internal functional block diagram is represented in Fig.3.10, where:

- DIS: disable/enable both driver outputs;

- GND: primary side ground reference;
- INA,INB: Input signal for channels A and B respectively;
- NC: no internal connection;
- OUTA,OUTB: output of driver A and B respectively;
- VCCI: primary side supply;
- VDDA,VDDB: secondary side supply for driver A and B respectively;
- VSSA,VSSB: secondary side ground for driver A and B respectively.

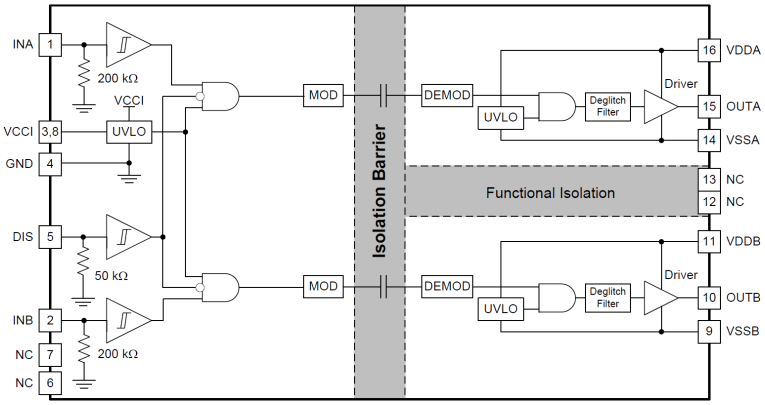


Figure 3.10: Gate driver functional block scheme [3].

Table 3.8: UCC21220 gate driver maximum ratings.

VCCI to GND	-0.5V to 6V
INA,INB,DIS to GND	-0.5V to 6.5V
VDDA-VSSA,VDDB-VSSB	-0.5V to 20V
OUTA to VSSA, OUTB to VSSB	-2V to 20.5V

In Fig.3.11 is shown the connections of the gate driver in Altium, it is only reported for one inverter leg but the same schemes are used for the other phases. At the input signals coming from the microcontroller are added 1μF capacitors to ground to reject disturbances, moreover, to stabilize the supply voltages one capacitor of 100nF is inserted at the primary side (+3.3V) and two capacitors of 22μF at the secondary side (+15V isolated). To achieve a better noise immunity of pin DIS a resistor (10kΩ) and a capacitor (1nF) are connected to ground.

The gate resistance, which connect the output of the gate driver to the IGBT gate and a resistance, of 32Ω and 1kΩ from gate to source to discharge the internal IGBT capacitance. Moreover, it is added, but not mount, a fast diode and a resistor to have the possibility of having two different gate resistor for turn on and turn off.

To reach the +15V isolated supply voltage is used an isolated DC/DC converter with 15V input voltage, as reported in Fig.3.12.

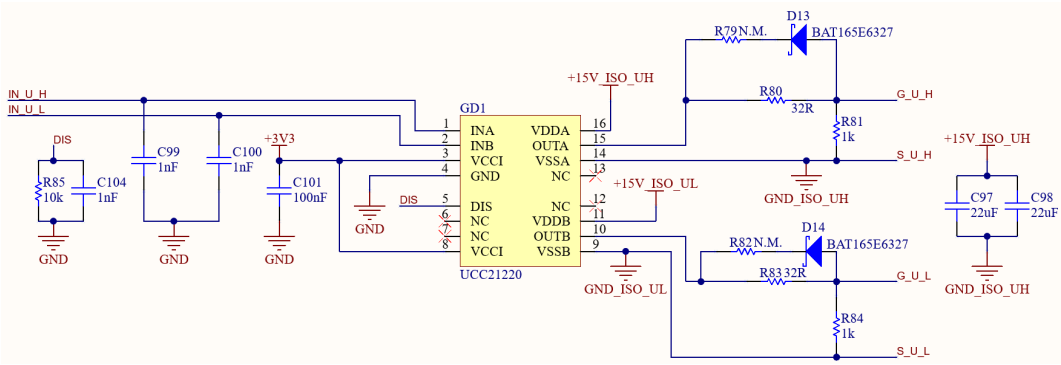


Figure 3.11: Gate driver Altium schematic.

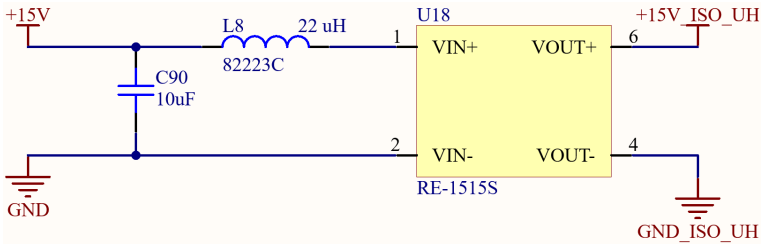


Figure 3.12: Gate driver secondary side supply Altium schematic.

3.5 Measurements

This part aims to choose the sensors and design the analog conditioning circuits to properly measure the quantities required by the control, shown in Tab.3.9.

Table 3.9: Required measurements.

3	Phase current measurements
1	Dc-link voltage measurement
1	Module internal temperature measurement
1	External temperature measurement

The outputs of the sensors have to be sent to the microcontroller as input, which accepts only unipolar signals from 0V to 3.3V. To comply this requirement a proper analog conditioning circuit is needed. In Fig.3.13 is shown a general configuration to condition the signals coming from the sensors, it consists of a non-inverting amplifier which output is limited from 0V to 3.3V. This circuit can only work with unipolar input signal and the gain of the amplifier reported in (3.14). To better reject disturbances capacitors can be added in parallel to the R_2 resistors. The voltages $in+$, $in-$, v_o are referred to ground.

$$G = \frac{R_2}{R_1} \tag{3.14}$$

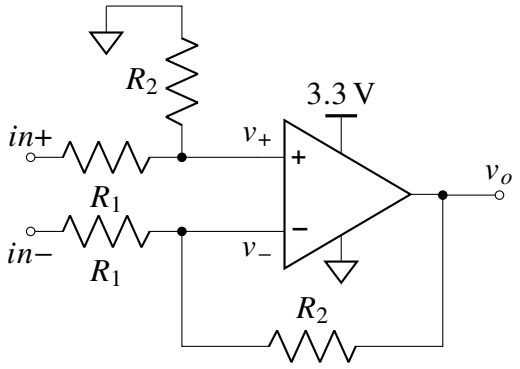


Figure 3.13: General schematic of analog conditioning.

3.5.1 Current Measurements

As calculated in (3.5), the maximum nominal current is 22.51A, therefore, considering an overload factor of 1.5 times, the current sensor measurable range have to be at least ±34A. Moreover, is required a fixed mode operation and a SOIC8 package. The chosen current sensor is the open loop hall effect MLX91221KDC-ABF-050-RE from Melexis, which specifications are resumed in Tab.3.10 and functional block diagram in Fig.3.14. It is important to notice that the output of the sensor is unipolar, therefore, no level shifter circuit is required to condition the output signals.

Table 3.10: MLX91221KDC-ABF-050-RE main specifications.

Measurement Range	-50A to +50A
Sensitivity (S)	25mV/A
Reference Voltage (V_{ref})	1.65V
Measured Current	$(V_{out} - V_{ref})$/S
Package	SOIC8

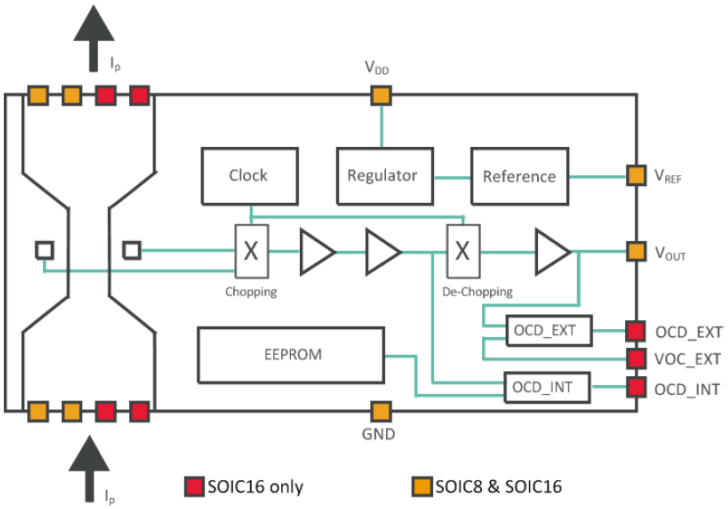


Figure 3.14: Current sensor functional diagram [4].

The fixed mode operation consists of two signal OUT and REF as output of the current sensor and sent as input to the microcontroller, as shown in Fig.3.15. The two supply voltages can be different but the reference ground is the same. To better reject disturbances it is preferred to use a non-inverting amplifier structure, similar to Fig.3.13, with unitary gain.

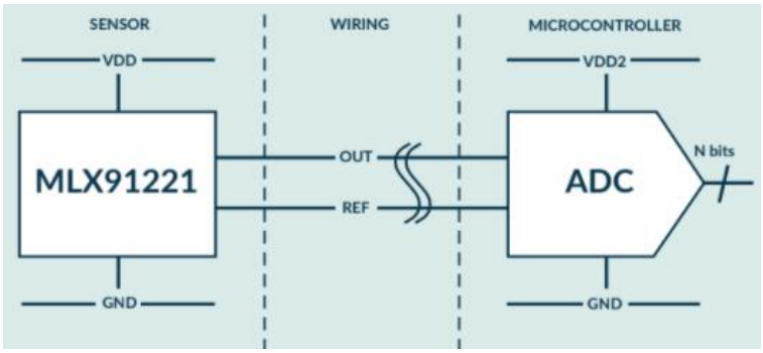


Figure 3.15: Current sensor fixed mode operation [4].

In Fig.3.16 and Fig.3.17 are reported the Altium schematics for the current sensor connections and the analog conditioning respectively. Three capacitors of 47nF are connected to VDD, to stabilize the supply voltage, and to VOUT and VREF to create a path for disturbances which does not arrive at the analog conditioning circuit. The resistors used for the analog conditioning are all 10kΩ to obtain a unitary gain, moreover, some 1nF capacitors are added to better reject disturbances.

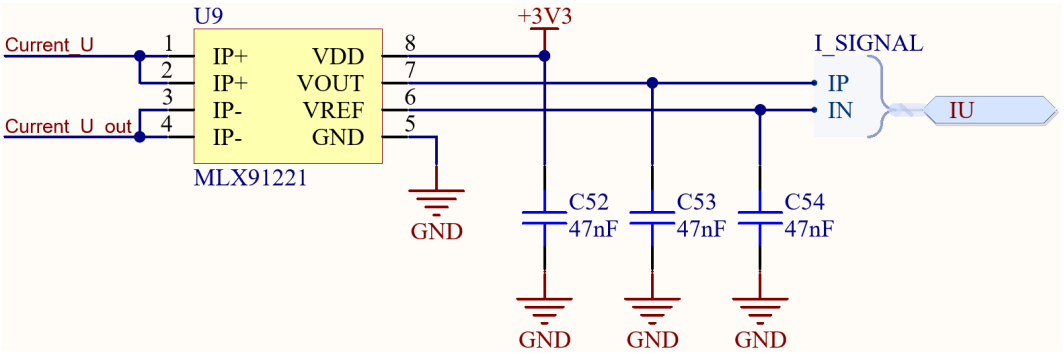


Figure 3.16: Current sensor connection Altium schematic.

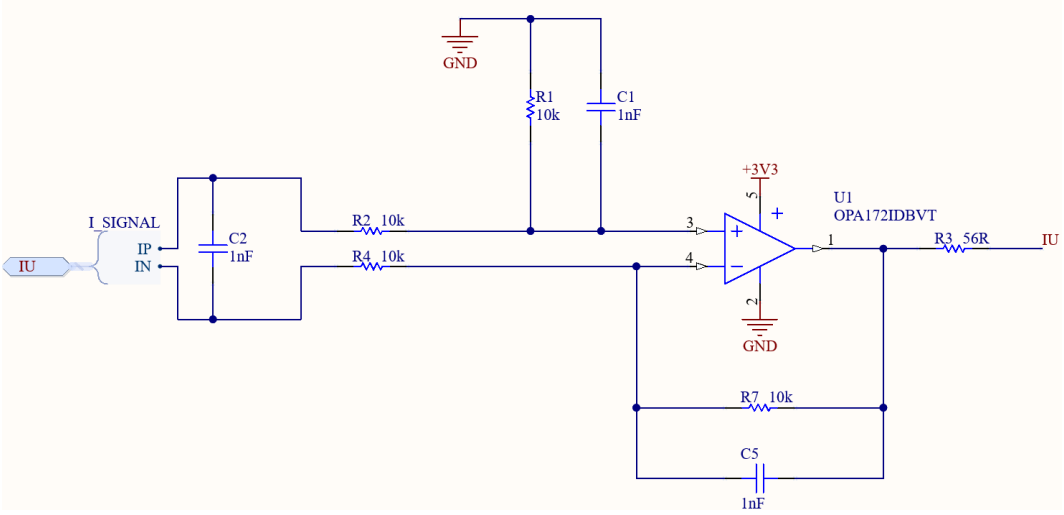


Figure 3.17: Current measurement analog conditioning Altium schematic.

3.5.2 DC-link Voltage Measurement

To measure the dc-link voltage is required an isolated amplifier, to separate the high power side with the low power one, and a voltage divider, to scale the dc-link voltage to the differential input voltage of the amplifier v_S. The resistor divider scheme is represented in Fig.3.18, where R_2 is the series of various resistors to reach the desired total resistance value ($R_{TOT} = R_1 + R_2$). The total resistance has to be sufficient high to limit the current and consequently the losses ($P_{loss} = V_{DC}^2/R_{TOT}$), the resistors package has to be properly chosen dependently on the required dissipated power capability by the resistors. The maximum measurable dc-link voltage is fixed to 900V, including an abundant margin in case of resonances, and the R_{TOT} is in the order of 1.5MΩ, with this values the maximum losses are 0.54W.

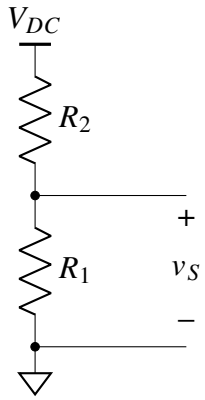


Figure 3.18: Resistor divider for dc-link voltage measurement.

The chosen isolated amplifier is the TLP7920 from Toshiba with optical isolation, which internal functional diagram is represented in Fig.3.19 and main features are resumed in Tab.3.11, where:

- VDD1 and VDD2 are the input and output supply voltages;
- VIN+ and VIN- are the positive and negative input voltages;
- VOUT+ and VOUT- are the positive and negative output voltages;
- GND1 and GND2 are the input and output side grounds.

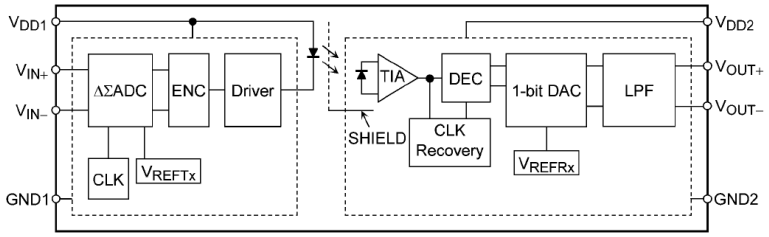


Figure 3.19: Isolated amplifier TLP7920 functional diagram [5].

Table 3.11: TLP7920 main specifications.

VDD1, VDD2, VIN+, VIN-, VOUT+, VOUT-	-0.5V to +6V
Typical Differential Input Voltage	±200mV
Operating Temperature	-40°C to 150°C
Power Dissipation	60mW

In (3.15) is reported the calculation to size the resistor R_1. The result is approximated to the closest standard resistor value, with ±5% tolerance, and the chosen package is the 0603 which can dissipate 1/16W. This same reasoning is used to define the resistors composing R_2, in this case the higher resistances have higher voltage drop and consequently higher losses, is chosen the 1206 package with 1/8W of power dissipation. In (3.16) is resumed the composition of the resistor divider, in which the resistor values are approximated at standard values. It is possible to notice that the total resistance is very close to 1.5Ω.

$$\frac{v_s}{V_{DC}} = \frac{R_1}{R_{TOT}} \rightarrow R_1 = R_{TOT}\frac{v_s}{V_{DC}} = 333.3\Omega \rightarrow 300\Omega \tag{3.15}$$

$$R_{TOT} = \underbrace{6 \cdot 240k\Omega}_{R_2} + \underbrace{300\Omega}_{R_1} = 1.44M\Omega \tag{3.16}$$

The resistor divider is sized to give as input at the isolated amplifier 173mV at 900V, reaching approximately 1.65V at the output due to it gain of 8.2. Therefore, an analog conditioning circuit is required to amplify of a factor two this signal to reach 3.3V, in this way all the ADC scale is exploit and the error is minimized. In Fig.3.20 are represented the main blocks of the dc-link voltage measurements and the voltages in each step at 900V.

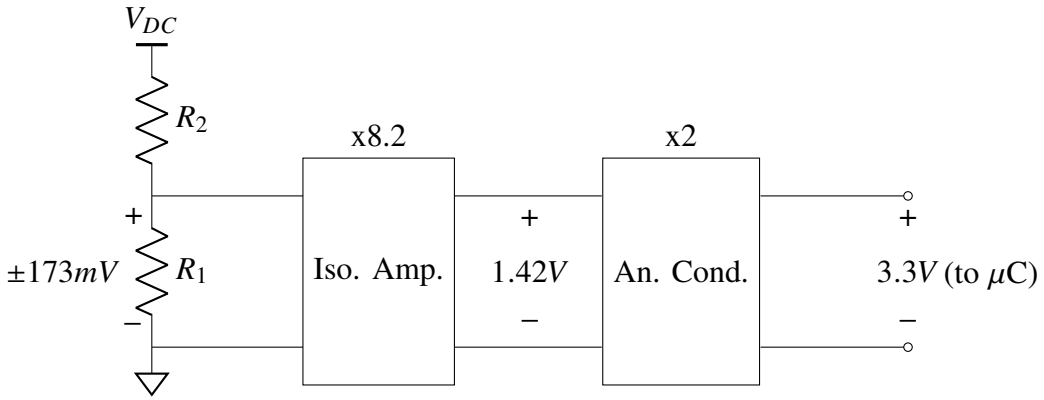


Figure 3.20: Dc-link voltage measurement signal conditioning.

In Fig.3.21 is shown the Altium schematic of the resistor divider and isolated amplifier. The input side of the amplifiers is supplied at +5V with a proper isolated power supply, instead, the output side is supplied at 3.3V. Even in this case, to stabilize the supply voltage two capacitors of 1μF and 100nF are added. The filter the input voltage a 47μF capacitor is used and two 10kΩ are added to limit the current entering in the amplifier. In Fig.3.22 is reported the Altium schematic of the analog conditioning circuit and as required the gain is 2.325 (G=51kΩ/22kΩ ≃ 2.32), the other components are the same of the analog conditioning circuits previously explained.

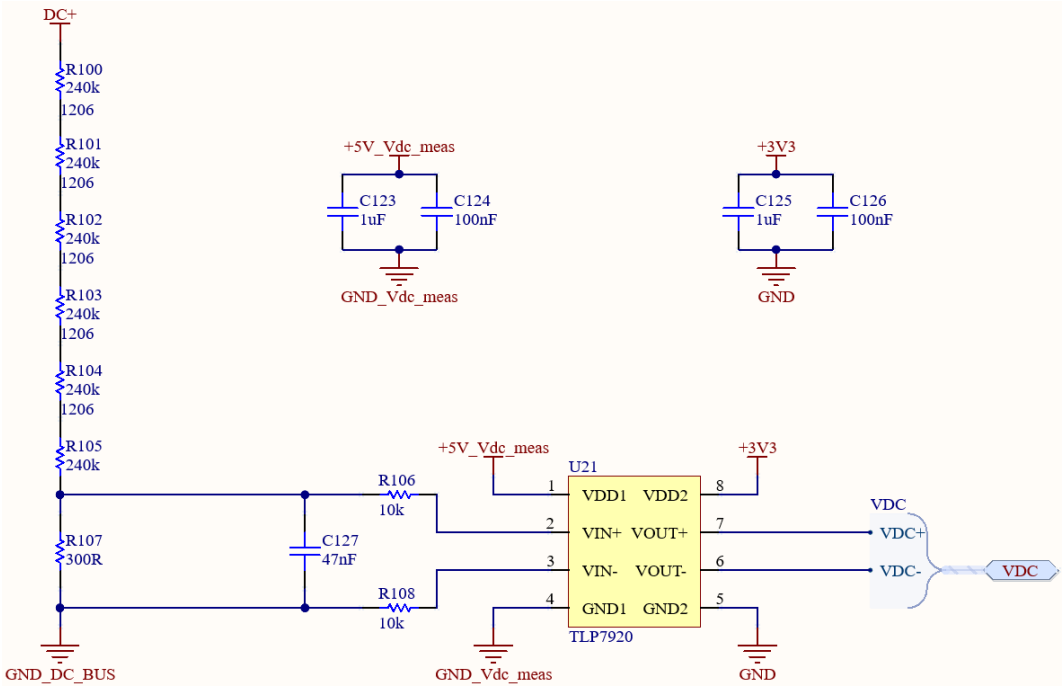


Figure 3.21: DC-link voltage measurement Altium schematic.

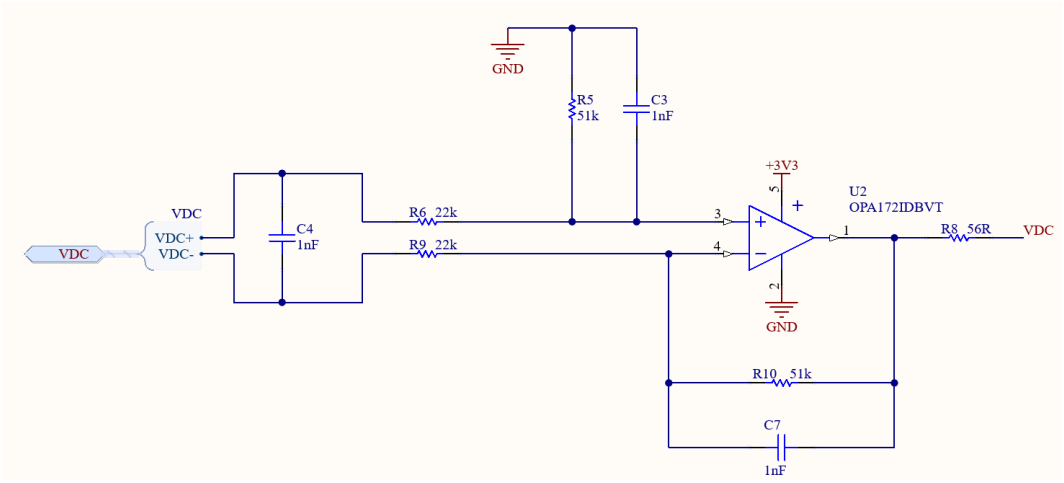


Figure 3.22: DC-link voltage measurement analog conditioning Altium schematic.

3.5.3 Temperature Measurements

The converter is designed to have two temperature measurements: one is inside the module, to avoid damages in the power modules, and one external to connect a sensor to monitor the temperature of an external device, for example the electric machine. The

sensors used are thermistor, wich can have negative temperature coefficient (NTC) or positive temperature coefficient (PTC).

3.5.4 Module Internal NTC Sensor

In Fig.3.23 is shown the characteristic of the module internal NTC. According to what previously said, the characteristic is a decreasing exponential in which the resistor tend to zero at the increase of the temperature and vice versa. In Tab.3.12 are reported the main specifications of the module internal NTC sensor, where:

- T_0 is the reference temperature;
- $R_0(T_0)$ is the rated resistance at 25°C;
- $B_{25/50}$ is the B-value valid in the range 25°C-50°C with a certain tollerance;
- $B_{25/100}$ is the B-value valid in the range 25°C-100°C with a certain tollerance;
- P_d is the power dissipation.

Table 3.12: Module internal NTC main specification.

T_0	$R_0(T_0)$	$B_{25/50}$	$B_{25/100}$	P_d
25°C	22kΩ	3950K±3%	3998K±3%	200mW

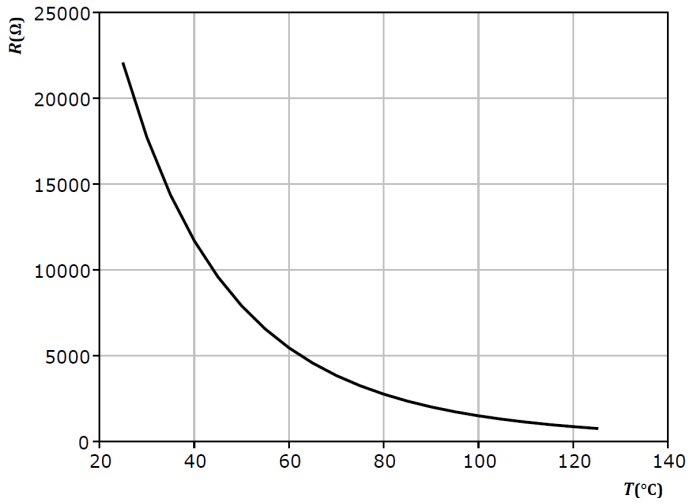


Figure 3.23: Module Internal NTC sensor characteristic [2].

To obtain the temperature measurement is required a resistor divider, to reach the NTC resistor (R) information starting from the measure in the voltage drop in the NTC,

and a characteristic equation to convert the resistor information in a temperature one. In (3.17) is reported the second order approximated Steinhart-Hart equation, manipulating it is possible to obtain the characteristic equation, in (3.18), putting in relationship the NTC resistance variation with the temperature one dependently on its parameters.

$$\frac{1}{T} = \frac{1}{T_0} + \frac{1}{B} ln\left(\frac{R}{R_0}\right) \tag{3.17}$$

$$T = \frac{B}{ln\left(\frac{R}{R_0 e^{-B/T_0}}\right)} \tag{3.18}$$

In Fig.3.24 is shown the Altium schematic of the module internal temperature measurement. The voltage divider is supplied at 3.3V and the resistor (R_c), with constant resistance, is 3kΩ. The voltage drop in the NTC (v_T) can be calculated as (3.19), moreover, v_T can vary at the limit from 0V to 3.3V, due to the supply voltage of 3.3V. This satisfy the input voltage standard of the microcontroller, for this reason it is only added the analog condition previously shown with unitary gain to better reject disturbances and stabilize the measure. Moreover, a filter capacitor of 1nF is added in parallel the NTC to filter v_F and a 56Ω resistor is added before the microcontroller to limit the current.

$$v_T = 3.3V \frac{R}{R + R_c} \tag{3.19}$$

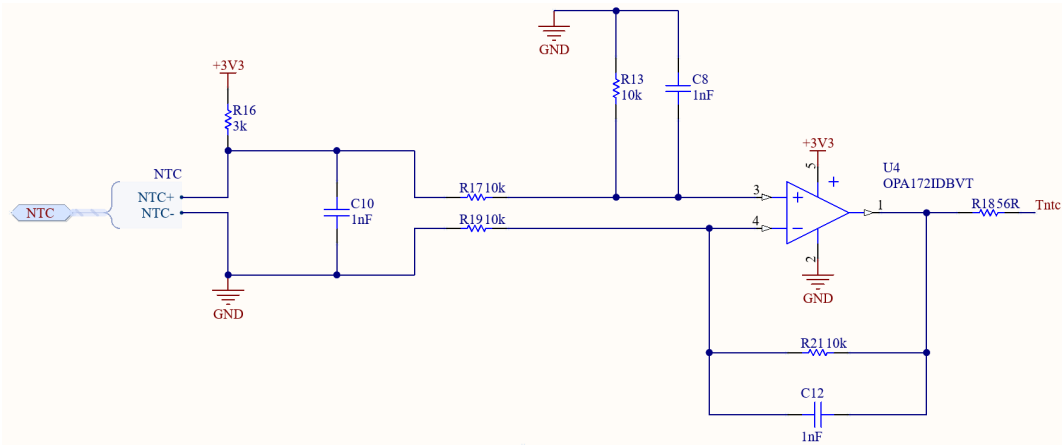


Figure 3.24: Module internal temperature sensor analog conditioning.

3.5.5 External PTC Sensor

The external temperature measurement is performed with a PTC that is not defined from beginning and the possibility to use it is left to the customer, which can use whichever PTC has available in that moment. Therefore, the measuring structure has to be general

and adaptable. The structure requires a 2-pin header to connect the external sensor, moreover, the voltage divider is supplied at 15V and the constant resistor is not mount (N.M.) to be defined once the sensor is defined. The gain of the amplifier is 1.25.

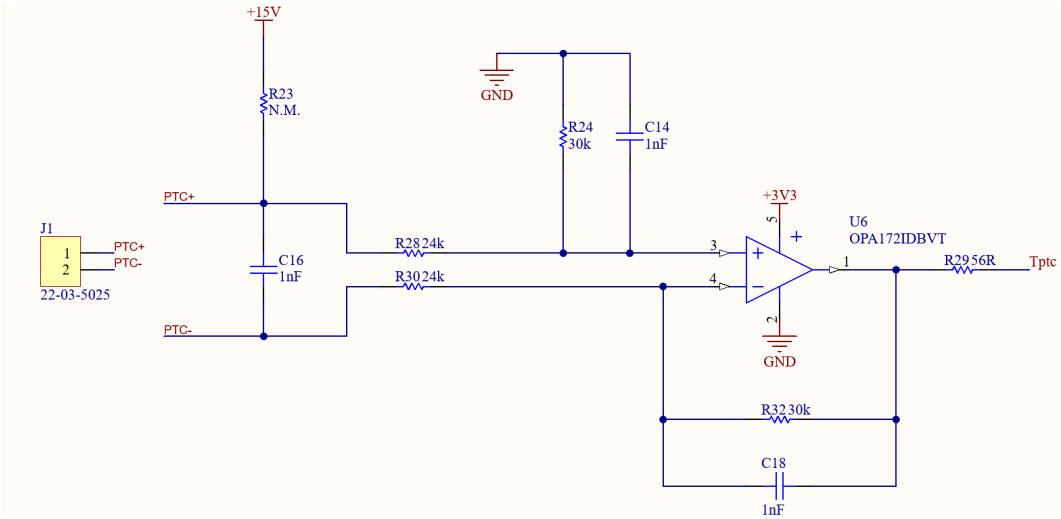


Figure 3.25: External temperature sensor analog conditioning.

3.6 DC-link Capacitor

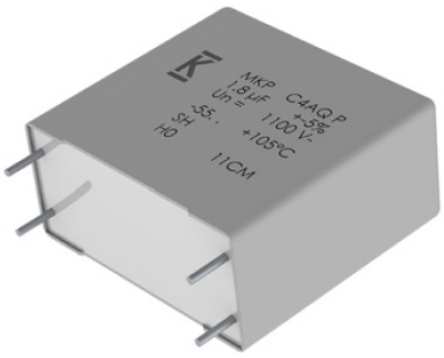
This section aims to choose the dc-link capacitor. To increase the system reliability it is mandatory to use film technology, and, as reported in Tab.1.1, the desired capacitance for the slim dc-link is approximately 20μF. Using the simulation which include the control algorithm to damp the oscillations in Sec.4.4, it is possible to obtain the RMS current stress in the capacitor, in worst condition of SCR and no damping control the RMS current in the capacitor is 14A, instead, when the damping control is activeted it is 11.8A independently the SCR value. The chosen capacitor is the C4AQOBW5120P3FJ (4 pins) from Kemet manufacturer, represented in Fig.3.26, which main features are resumed in Tab.3.13, where:

- C: nominal capacitance;
- V_{dc}: voltage class at 85°C;
- T: thickness;
- H: height;
- L: length;
- S: space between opposite wires;

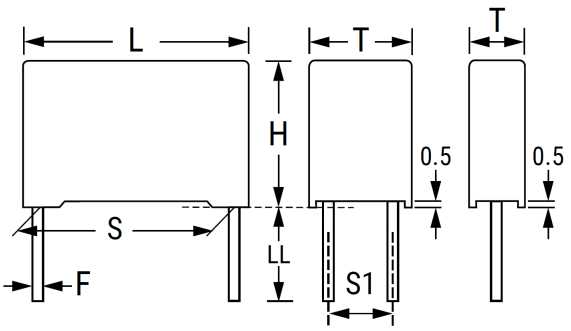
- S1: space between wires of the same side (4 pin);
- I_{pk}: maximum acceptable current;
- ESL: parasitic inductance;
- ESR: equivalent internal resistance;
- I_{rms}: nominal rms current;
- R_{th}: thermal resistance form loss source to ambient.

Table 3.13: Module internal NTC main specification.

C	V_{dc}	T	H	L	S
12μF	900V	20mm	40mm	42mm	37.5mm
S1	I_{pk}	ESL	ESR	I_{rms}	R_{th}
10.2mm	420A	12nH	6.9mΩ	14.4A	20°C/W



(a) Capacitor representation [6].



(b) Capacitor sizes [6].

Figure 3.26: C4AQOBW5120P3FJ dc-link capacitor.

To reach a desired capacitance value close to 20μF, two capacitors in parallel are required, obtaining a dc-link with 24μF. The rms current stress is divided between the two capacitance that in worst case it is 7A for each, this value is abundantly inside the nominal one of the capacitor (14,4A). It is important to verify that no resonances occur between the capacitance and the ESL, the rule of thumb is that the resonance frequency have to be at least ten times higher than the switching one. In (3.20) is reported the calculation of the resonance frequency, it is possible to notice that it is more than ten times higher the switching one, avoiding dangerous resonance in the dc-link.

$$f_{res} = \frac{1}{2\pi\sqrt{C \cdot ESL}} = 420kHz \tag{3.20}$$

Knowing the capacitor current stress ($I_{C,rms}$), the ESR and R_{th}, it possible to evaluate the power losses and consequently the overtemperature, as in (3.21) and (3.22). It possible to notice that the losses are practically negligible and the overtemperature (ΔT) is not relevant.

$$P_{loss} = ESR \cdot I_{C,rms}^2 = 0.34W \tag{3.21}$$

$$\Delta T = P_{loss} \cdot R_{th} = 6.8°C \tag{3.22}$$

3.7 MCU

The intelligent part of the converter is the microcontroller, which required features for the control are:

- At least 5 Analog to Digital Converter (ADC), one for each measurement apart the temperature one (1 ADC for 2 signals);
- At least 1 Advanced-control Timers to generate the 6 gate commands;
- 1 CAN communication interface;
- At least 100MHz of clock.

The chosen one is the STM32G474VE from STM manufactures, which main features are summarized in Tab.3.14. The microcontroller has to be properly programmed and the General Purpose Input Output (GPIO) functions have to be defined, to do this it is used the STMCubeMX program to design the pinout. More detail about the microcontroller configuration are reported in the next chapter.

Table 3.14: STM32G474VE main features.

Core	Arm®32-bit Cortex®-M4
Benchmark	213DIMPS
Frequency	170MHz
Flash memory	512kbytes
SRAM	96kbytes
Timers (PWM)	12×16-bit
ADC	5×12-bit resolution

In Fig.3.27 is reported the defined microcontroller pinout where the most important section are highlighted with different colors, in particular:

- ADC-Phase Currents, pins for the phase current measurements with one ADC per each (ADC1, ADC2, ADC3);
- ADC-Dc Voltage, pin for the dc-link voltage measurement connected to a dedicated ADC (ADC4);
- ADC-Temperatures, pins for the temperature measurements both connected to the same ADC (ADC5);
- PWM Commands, pins for the inverter switching commands generation using one Advanced-control Timer (TIM1);
- CAN, pins for the CAN communication interface;
- JTAG, pins for the microcontroller programming;
- External Oscillator, pins to connect external crystal oscillator of 25MHz;
- Emergency, pins for the emergency stop commands in case of failure.

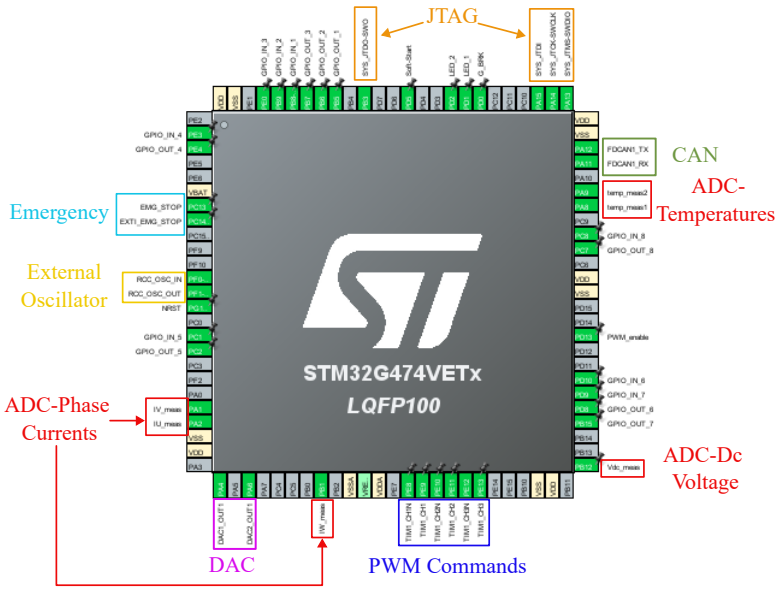


Figure 3.27: Mcu pinout.

As can be deduced by the previous paragraph, the most important measurements (phase currents and dc-link voltage) have its own ADC. This guarantee that the measurements occur at the same time corresponding to the triangular upper front, and to avoid sampling errors related to the measurement delay in case of multiple measurements with the same ADC. To protect the microcontroller from negative voltages and dangerous overvoltages, the ADC signals are clamped between GND and 3.3V, as shown in Fig.3.28.

Moreover, a capacitor is added at each pin as close as possible to the microcontroller to reject disturbances and stabilize the ADCs conversions.

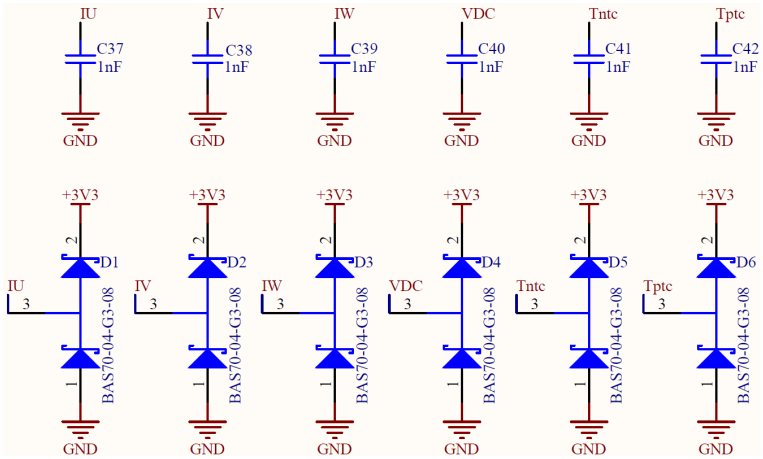
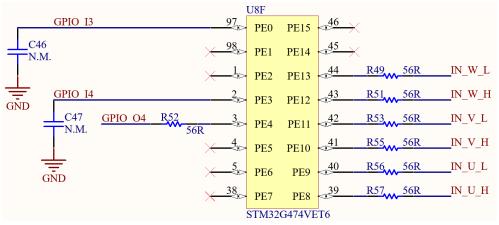
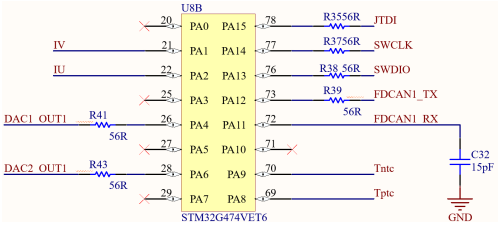


Figure 3.28: ADC microcontroller signal filtering and clamping.

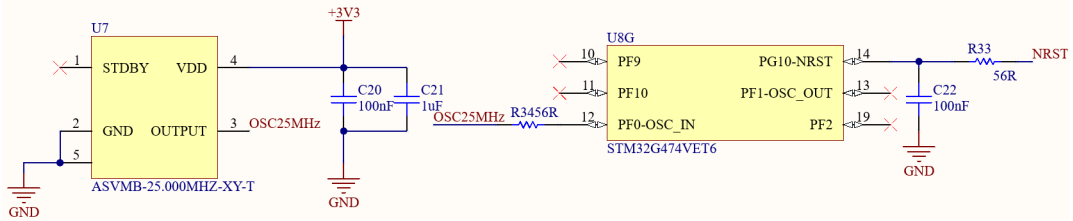
The main microcontroller Altium schematics are shown in Fig.3.29, in particular are reported: some measurements, the JTAG, the CAN interface, two Digital to Analog Converter (DAC), the six gate commands and the external oscillator connection.



(a) Gate commands.



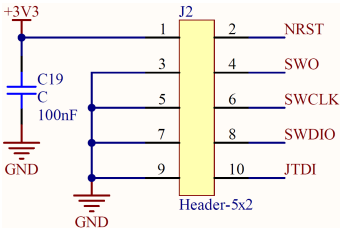
(b) CAN, JTAG, measurements.



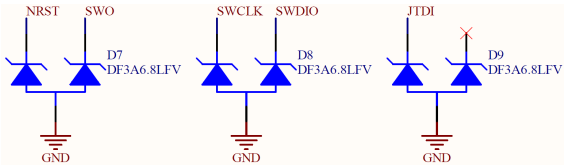
(c) External oscillator.

Figure 3.29: Microcontroller main Altium schematics.

In Fig.3.30 are reported the JTAG header for microcontroller programming and debugging. Moreover, according to what previously said, these signals are clamped to ground to avoid negative voltages inside the microcontroller.



(a) JTAG header.



(b) JTAG signal clamping.

Figure 3.30: JTAG signals.

To let the converter more adaptable some GPIOs are connected to an header (Fig.3.31), but them function are not define from the beginning. This allow to easily use this pins for extra functions out of the control. Moreover, a reset button is connected to the microcontroller reset pin and two LEDs are added that can be employed by the user.

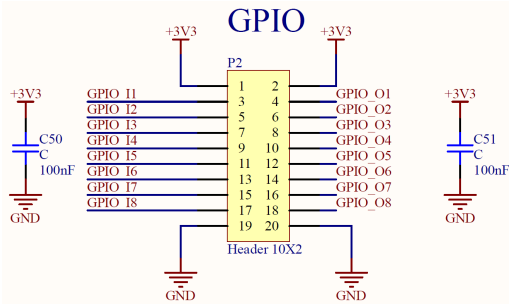


Figure 3.31: GPIO header.

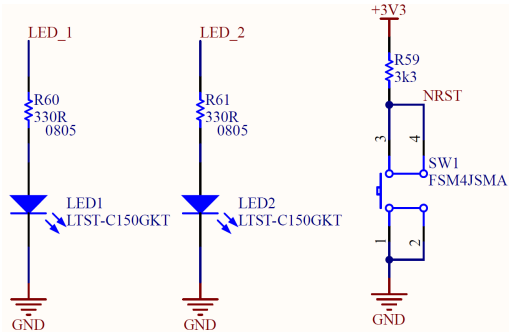


Figure 3.32: Reset button and general purpose LEDs.

3.8 CAN Communication

The converter requires a communication system to exchange information with the external world, the required one is the Controller Area Network (CAN) system to properly work even in high disturbed environment. In Fig.3.33 are shown the main block of the communication system, in which: the transmitter pin from the microcontroller is connected to the receiver of the isolated transceiver to provide communication and vice versa, the other side create the CAN bus which is connected to the external world thank to a connector.

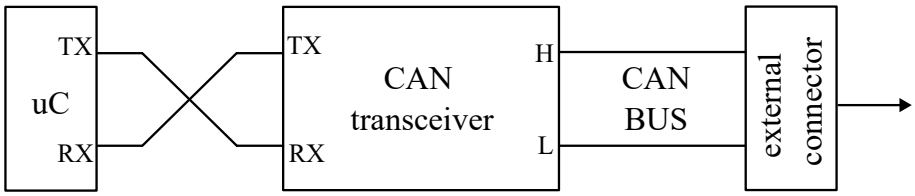


Figure 3.33: CAN main blocks.

The chosen isolated transceiver is the ISO1042 from Texas Instruments manufacturer that meets the specifications of the ISO11898-2 standards. In Fig.3.34 is reported the Altium schematic of the isolated transceiver and the external connector. The fist device is supplied at 3.3V at the primary side and 5V isolated at the secondary, capacitors are added to stabilize the supply voltage. The signals CAN_TX and CAN_RX come from the microcontroller and a 15pF capacitor is connecter to CAN_TX to reject disturbances. To reject common mode disturbances a common mode inductance is added at the output of the transceiver.

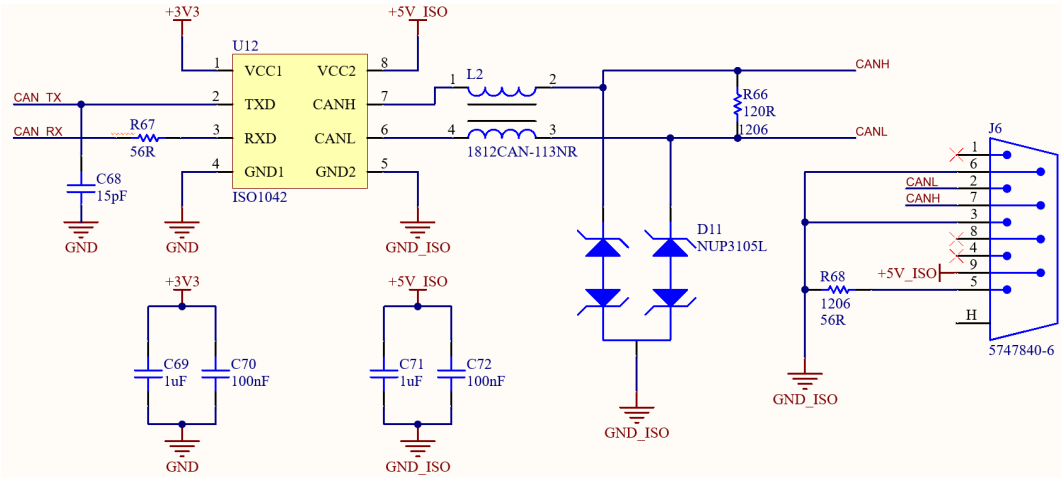


Figure 3.34: CAN Altium schematic.

3.9 EMI filter

In Fig.3.35 is shown the Altium schematic of the EMI filtering stage. It consists of: a three phase common mode choke, before and after the choke are inserted three capacitors, connected at each phase and all connected to the power earth (PE) through a reinforced capacitor, and four varistors connected as the capacitors to limit the converter input voltage in case of grid overvoltages. This configuration rejects the EMI noise, the chosen choke is the RT8532-16-3M0 (Fig.3.36), the reinforced capacitors chosen are the PME295 (Fig.3.37) and the varistors are the B72210S2421K101 (Fig.3.45). In Tab.3.15, Tab.3.16, Tab.3.17 are summarized the main features of these components.

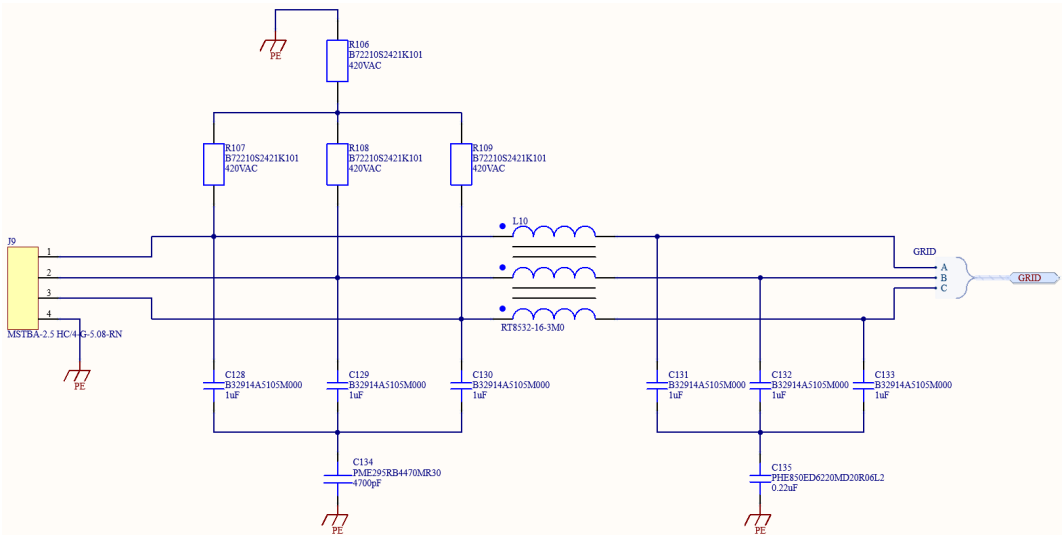


Figure 3.35: EMI filter Altium schematic.

Figure 3.36: RT8532-16-3M0 [7].

Table 3.15: Common mode choke main specifications.

Maximum voltage AC	600V
Operating frequency	DC to 400Hz
Rated current	20A
Temperature range	-40°C to 100°C

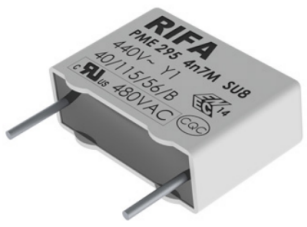


Figure 3.37: PME295 [8].

Table 3.16: Common mode capacitor main specifications.

Rated voltage AC	480V
Capacitance	4700pF
Capacitance tolerance	±20%
Temperature range	-40°C to 115°C

Figure 3.38: B72210S2421K101 [9].

Table 3.17: Common mode capacitor main specifications.

RMS voltage AC	420V
Maximum voltage	560V
Nominal current	1500A
Power dissipation max	0.4W
Temperature range	-40°C to 125°C

3.10 Power Supply

For this prototype it is requested to use an external power supply which give as output 15V. In Fig.3.39 are resumed the main bocks to satisfy the various supply requirements of the chosen devices, starting from the 15V. In particular, it is exploited a not isolated DC/DC converter and a linear regulator to obtain the 5V and 3.3V supply respectively, used to supply the majority of the devices (microcontroller, operational amplifiers, etc.). To obtain the isolated 5V required by the CAN transceiver it is used an isolated DC/DC converter which has the 15V as input. Instead, the isolated 5V for the optically isolated amplifier supply are obtained always with an isolated DC/DC converter but with 5V input. The three gate drivers isolated sides are supplied at 15V with an isolated DC/DC converter, to guarantee the separation of the low and high power.

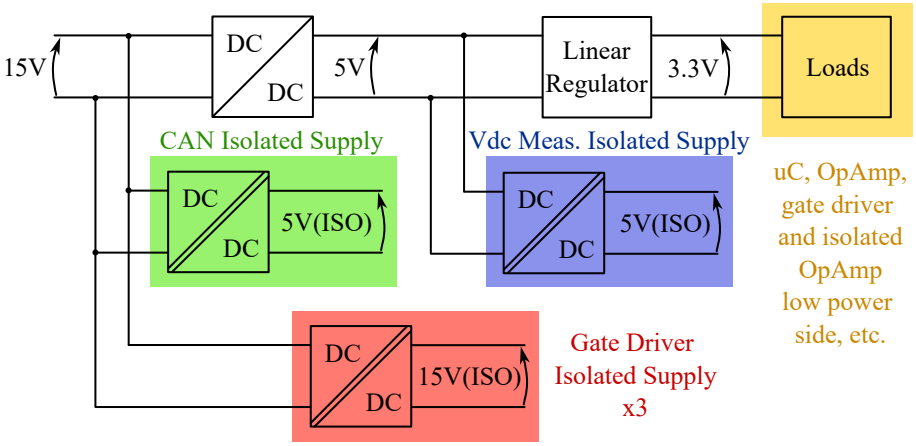


Figure 3.39: Power supply representative blocks.

3.11 Thermal Design

At this point, the only component that to be designed is the heatsink. In Fig.3.40 is shown the steady state thermal model of the heatsink, it consists of a thermal resistance sink to ambient ($R_{th,s-a}$) and the power losses (P_d) are that coming from the power module. To choose the heatsink is necessary to calculate the maximum thermal resistance, as in (3.23), require to dissipate the maximum losses ($P_{d,max}$), in this case, the heatsink temperature (T_s) is imposed equal to 80°C, as reasonable value for this application, and the ambient temperature (T_{amb}) considered in worst case equal to 45°C.

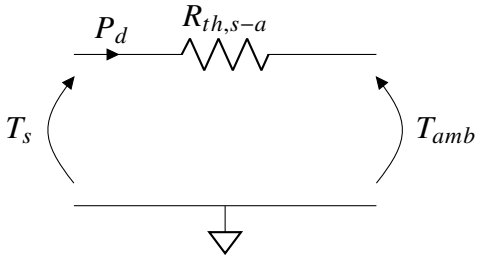
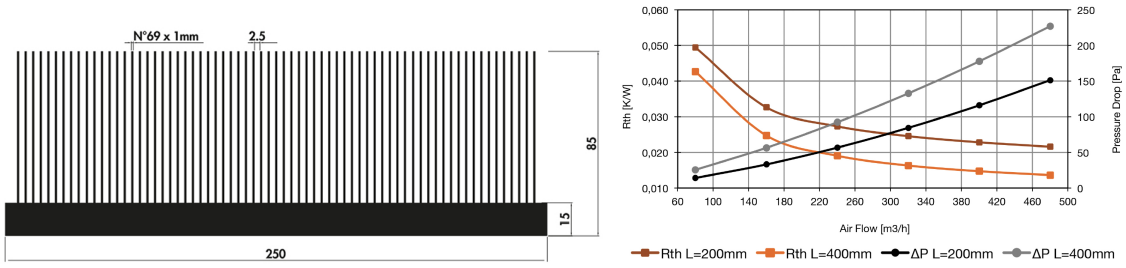


Figure 3.40: Steady state heatsink thermal model.

$$R_{th,max} = \frac{T_s - T_{amb}}{P_{d,max}} = 0.15K/W \tag{3.23}$$

The chosen heatsink is the PM250 85 from Meccal manufacturer. As reported in Fig.3.41b to satisfy the thermal resistance requirement it is necessary to guarantee a proper forced ventilation. It is important to notice that the heatsink provide the mechanical support of the power converter, therefore, the maximum size of the PCB have to be smaller than the heatsink surface.

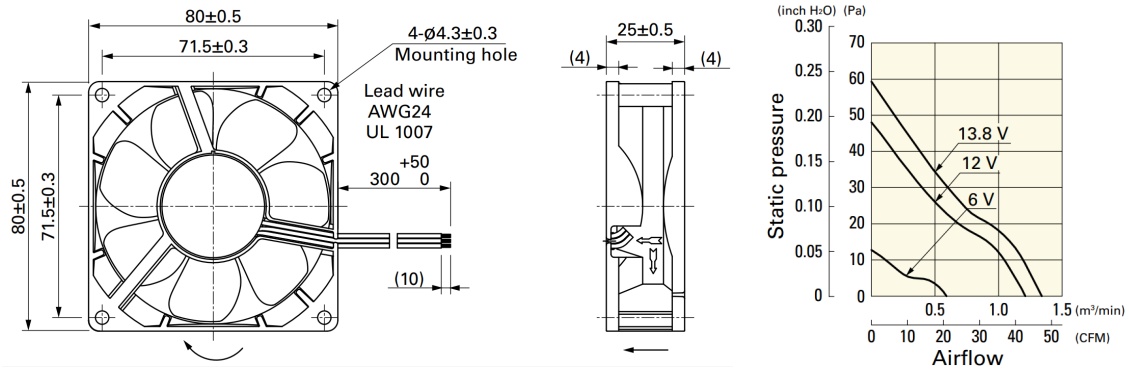
The chosen fan is the 9A0812S402 from Sanyo Denky manufacturer which air-flow static pressure characteristic is reported in Fig.3.42. In Tab.3.18 are summarized the main heatsink and fan specifications.



(a) Heatsink size [10].

(b) Heatsink properties [10].

Figure 3.41: PM250 85 main features.



(a) Fan size [11].

(b) Fan static curve [11].

Figure 3.42: Fan main features.

Table 3.18: Main fan and heatsink specifications.

FAN	Rated voltage	12V
	Rated current	0.18A
	Rated power	2.16W
	Rated speed	3400rpm
	Max air flow	1.2 m^3/min
	Max static pressure	48Pa
	Sizes	80x80x25mm
SINK	Thermal resistance	0.05K/W at 1.25m^3/min
	Pressure drop	20Pa at 1.25m^3/min
	Sizes	250×250×85mm

To verify the correctness of the design a thermo-fluid dynamic analysis is performed using the FlowSim tool of the software Solidworks. In Fig.3.43 is reported the temperature distribution of the in the heatsink, the module is represented with its only thin copper interface to the heatsink and corresponding to it two fan are inserted. The module is not located in the center but only exploit a portion of the heatsink, the other part play a secondary role in the cooling, however, it is important for the mechanical support of the converter. The simulation results shows that the maximum temperature is 75.7°C, according to the requirement of 80°C, moreover, in Fig.3.44 are reported the air flow lines created by the forced ventilation of the fans.

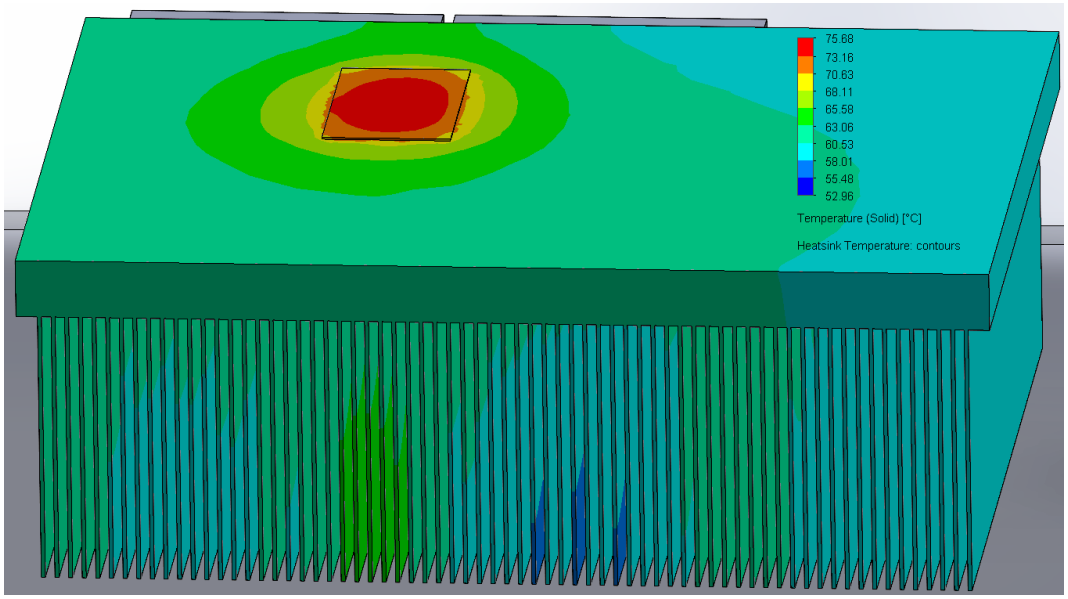


Figure 3.43: Heatsink temperature distribution.

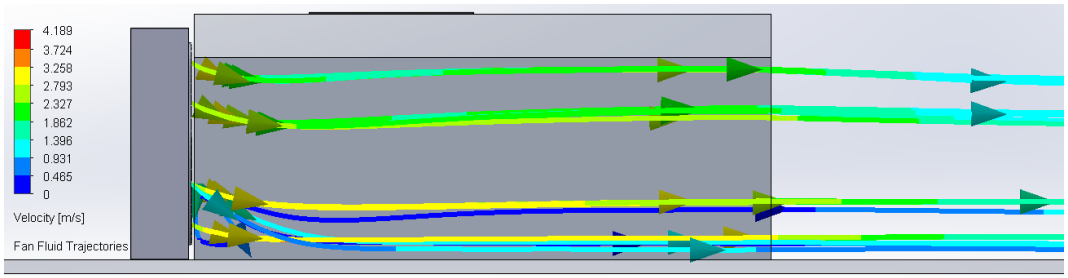


Figure 3.44: Heatsink fan air flow lines.

3.11.1 Extremely hot environments

As declared in Sec.1.3, one of the requirement of the converter is the capability to work in extremely hot environments with ambient temperature of 65°C. This is a very strict specification that would require an high performing heatsink increasing complexity and costs. The proposed solution is to change the fan, with a more powerful one, in case of hot environments condition, but maintaining the same heatsink. This maintain the main structure unchanged, however, a more powerful fan means higher consumption leading to a drop in the efficiency. This side effect is accepted as a compromise between cost, complexity and efficiency. The chosen fan is the PMD1208PMB1-A (2).GN from Sunon manufacturer, in Tab.3.19 are resumed the main specifications. How it could be expected the maximum air flow increases (more or less 1.5 times higher) leading to a better forced ventilation, consequently, the power consumption increases (approximately

four times higher, because the power depends on the cubic of the air speed) reducing the efficiency. The bigger fans replace the previous smaller ones. In Fig.3.46 and Fig.3.47 are shown the simulation results, in this case, the maximum heatsink temperature is 88.4°C that is considered an acceptable value for this condition.

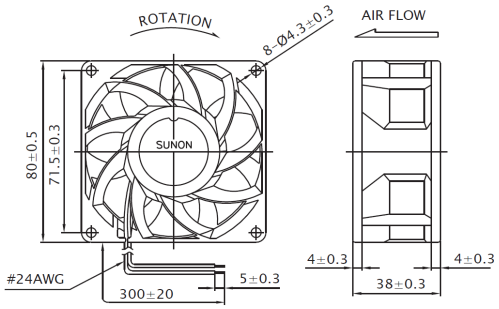


Figure 3.45: PMD1208PMB1-A (2).GN fan size [12].

Table 3.19: PMD1208PMB1-A (2).GN fan main specifications.

Rated voltage	12V
Rated current	0.76A
Power consumption	9.1W
Rated speed	5700rpm
Max air flow	$2.4m^3$/min
Size	80×80×38mm

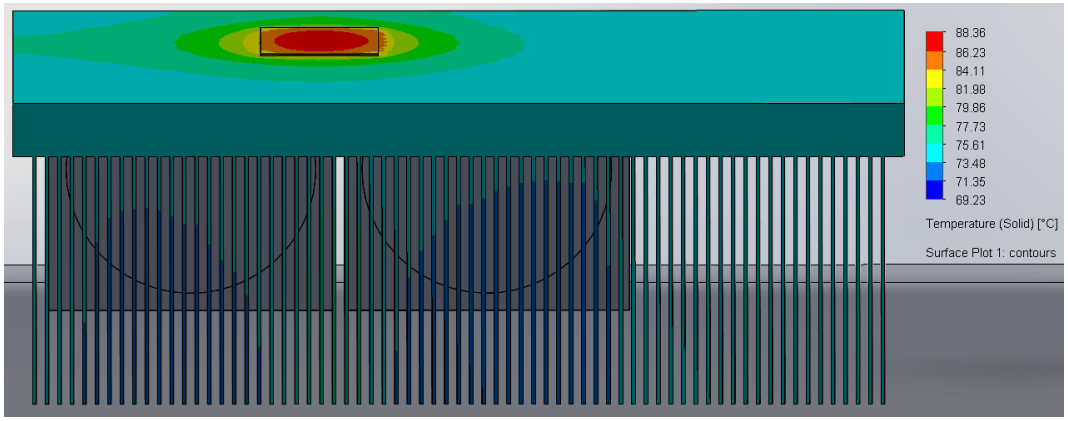


Figure 3.46: Heatsink temperature distribution with ambient temperature 65°C.

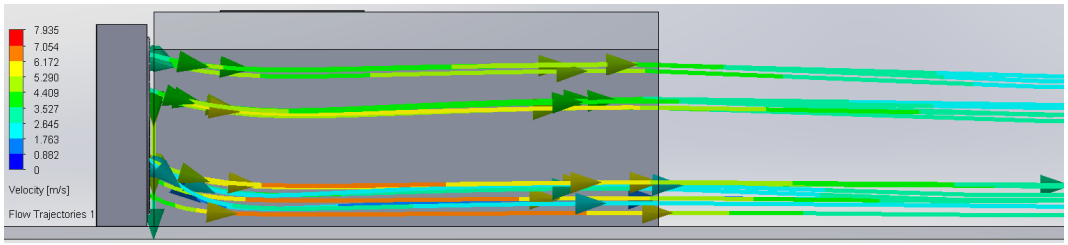


Figure 3.47: Heatsink fan air flow lines with ambient temperature 65°C.

Chapter 4

Control Design

4.1 Resonance Problems

How declared in the previous chapters, when drastically reducing the dc-link capacitance resonances occur. This resonances have to be damped at control level to avoid extra hardware components. As reported in Fig. 4.1, the dc-link voltage consists of three main components: one constant, one at six time the grid frequency (300Hz) and other related to resonances. Therefore, the voltage ripple can be written as $\tilde{v}_{dc} = \tilde{v}_{rip} + \tilde{v}_{osci}$.

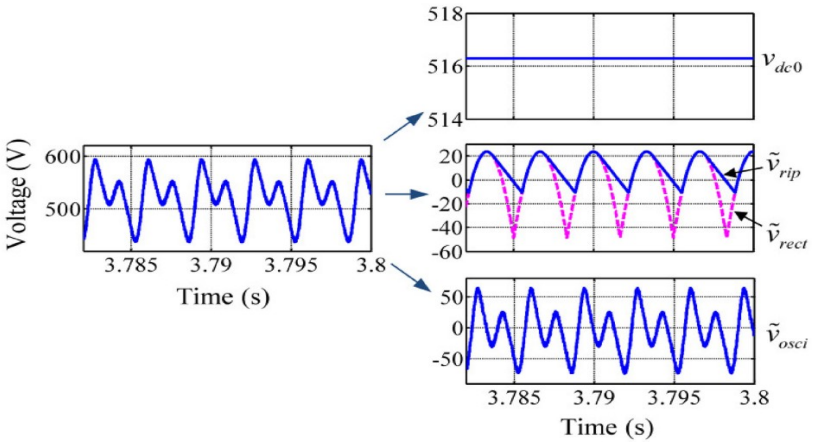


Figure 4.1: DC-link voltage components [1].

According to the formulation before, all the components of $\tilde{v}_{dc}$ are damped. However, the 300Hz component $\tilde{v}_{rip}$ would cause a low frequency torque ripple not easily damped by the rotor mechanical inertia that would cause relevant speed oscillations. For this reason it is preferred to only damp the resonant component $\tilde{v}_{osci}$, at an higher frequency with respect to 300Hz one causing lower speed ripple. Even in this case, all the previous considerations about the system stability are still valid.

4.2 Control Scheme

Fig.4.2 represents the general control scheme of the system. In general, the first block is related to the analog conditioning stage in which the motor currents and the dc-link voltage quantities are measured and filtered to avoid disturbances. The i_{abc}^{meas} enters in the motor control block in which, using the position information, are computed the output voltage references. The v_{dc}^{meas} signal enters in the filtering stage block in which the three voltage components are separated and elaborated to obtain the dc-link voltage reference v_{dc}^{*}. The v_{c}^{*} and the v_{dc}^{*} signals are used to compute the duty cycles and consequently the leg commands, using the regular sampled modulation with mid-voltage third harmonic injection.

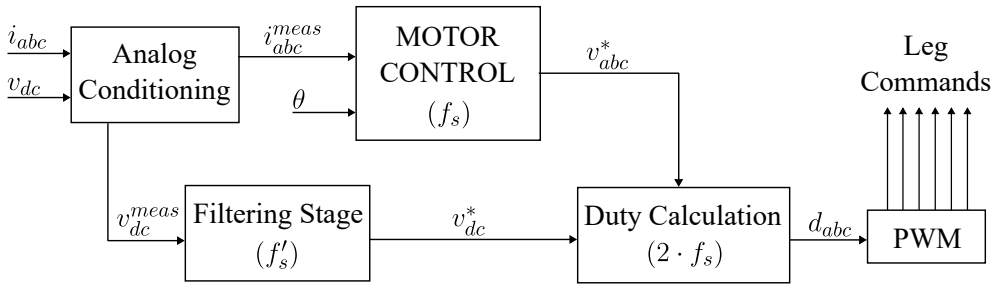


Figure 4.2: Control general structure.

4.3 Filters

In Fig.4.3 is shown the block scheme to obtain the dc-link voltage reference v_{dc}^{*}. To compute the constant voltage V_{dc} is used a Low Pass Filter (LPF) tuned at 10Hz, instead, for the 300Hz component is used a Resonant Filter (RF) based on sinusoidal signal integrator.

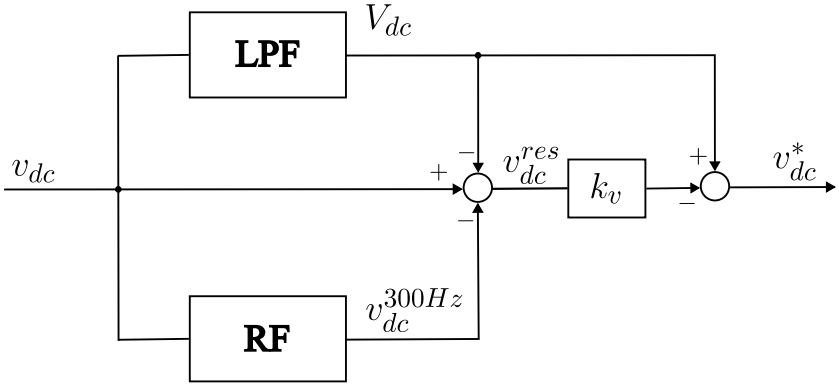


Figure 4.3: Reference dc-link voltage computation.

The switching frequency f_s is 10kHz and the motor control Interrupt Service Routine (ISR) is synchronized with the upper front of the triangular carrier. To properly let the v^*_{dc} discretized the filtering stage ISR frequency f'_s is imposed 10 time higher the switching one. As reported in Fig.4.4, the 100kHz ISR has an higher priority with respect to 10kHz one. This require a microcontroller performant enough to do all the calculation inside before the main ISR (at f_s) finishes.

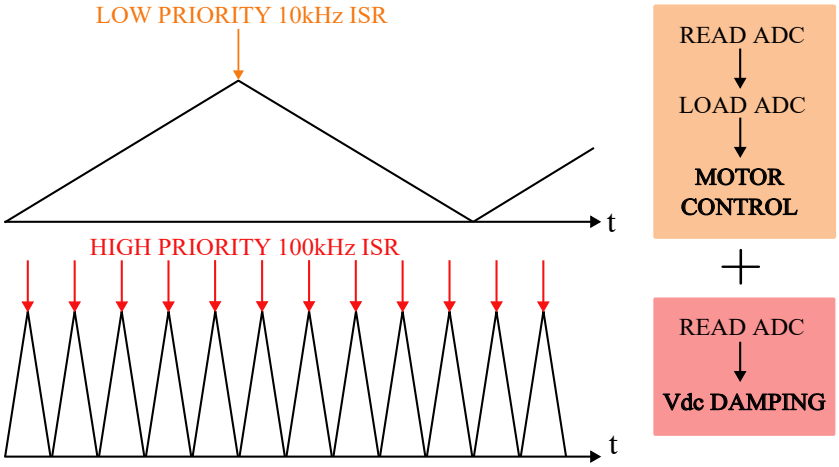


Figure 4.4: Interrupt Service Routine comparison.

4.4 Plecs Validation

At this point the system is implemented in Plecs to verify the control strategy. In Fig.4.5 is reported the Plecs simulation structure. The type and the size of the electrical machine is not defined, therefore, to let the simulation faster and in the absence of information about the motor, it is modeled with the series of a Resistance, an Inductance and an Electromotive force (RLE load). The parameters are estimated based on machines with similar size (7.5kW): the resistance is imposed equal to 0.1Ω, the inductance equal to 100$\mu\Omega$ and the peak of the electromotive force equal to 100V.

The control requires the rotor electrical position information to compute the Park and Clarke coordinate transformations to convert the quantities in d-q axis. The operating frequency (f_o) of the electric machine is imposed to 28.7Hz, approximately 1700rpm, and the electrical position is obtained integrating the speed and compute the inverse tangent to have a signal limited from 0 to 2π. The other main blocks are:

- Analog conditioning, simulate the filtering stage, low pass filter at control level to reject disturbances, and the quantization inside the microcontroller;
- Control, models the ISR main control (10kHz) which compute the reference voltage commands;

- Filtering Stage compute the different dc-link voltage components with the high priority ISR at 100kHz;
- Duty Calculation, calculate the reference duty cycles;
- PWM, transform, using the regular sampled modulation, the reference duty cycles in switching commands.

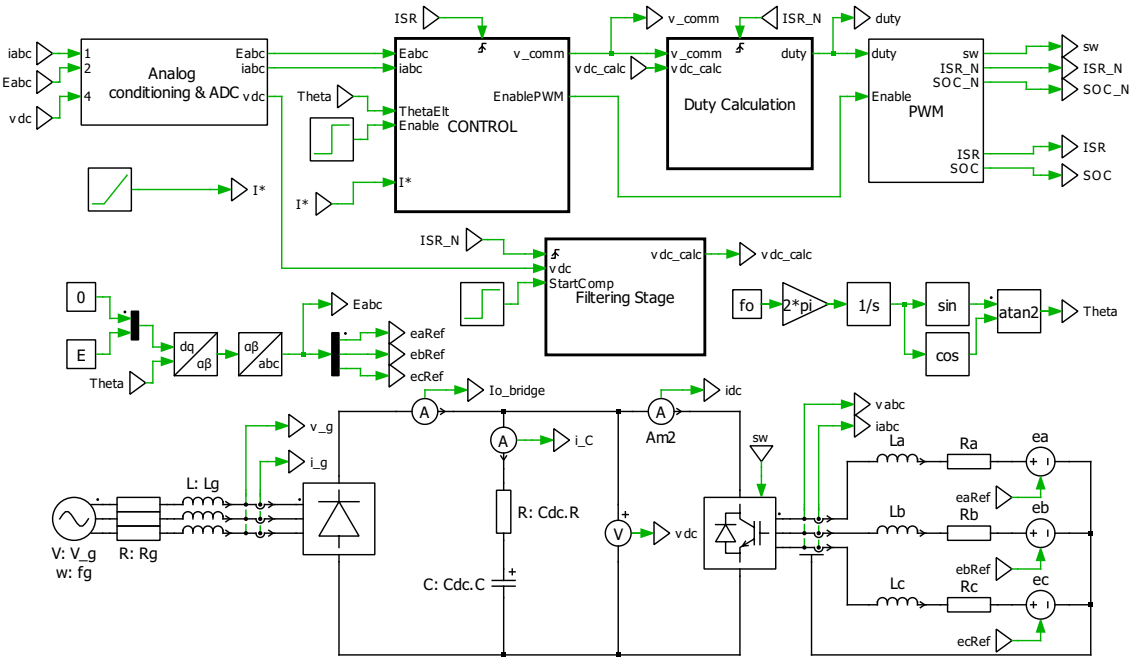
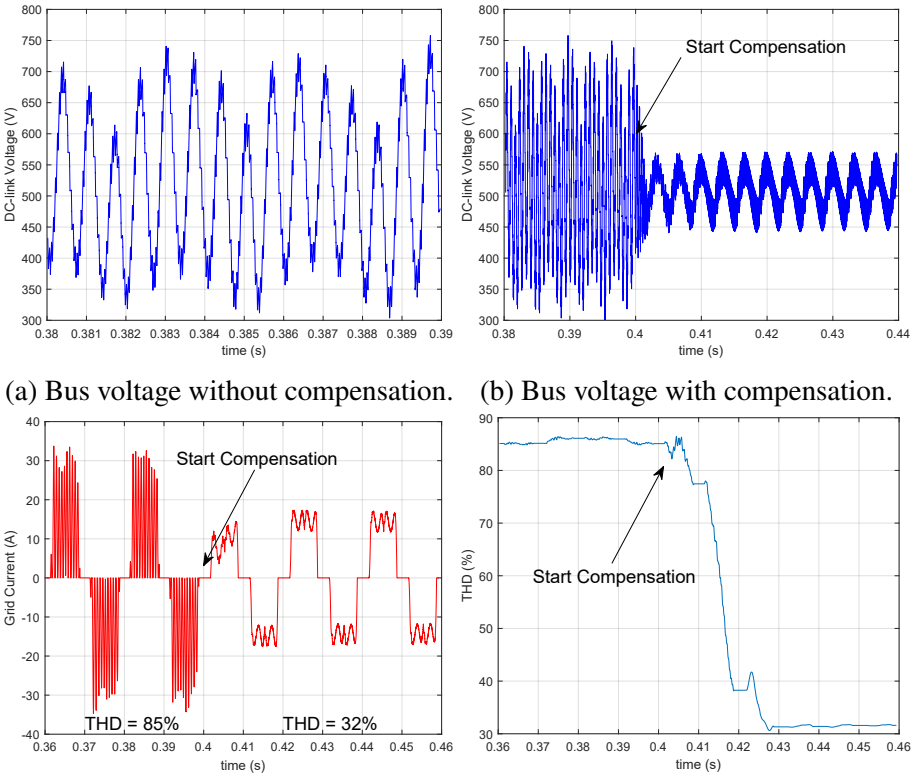


Figure 4.5: Plecs simulation structure.

In Fig.4.6 are reported the main Plecs simulation results, as shown in Fig.4.6a the dc-link voltage without compensation consists of three main component: the dc one, the 300Hz component and that related to the resonances. The switching ripple is practically negligible compared to the other components. When the resonances compensation starts, as shown in Fig.4.6b, Fig.4.6c and Fig.4.6d, the dc-link voltage low frequency resonant components are damped, the voltage ripple is mainly related to the 300Hz component due to the three phase rectifier bridge behavior. Consequently, the Total Harmonic Distortion (THD) of the grid current drops down from 85% to 32%, very close to the theoretical limit of 31% corresponding to the square wave waveform. In Fig.4.7 are shown the dc-link voltage components computed by the filtering stage block (ISR at 100kHz), it possible to notice that the dc component is not perfectly flat but it has a small overlapped ripple at 300Hz. The resonance components have a so higher frequency that are completely rejected by the low pass filter. Moreover, it possible to notice that the resonance components are drastically reduced after the active damping.



(a) Bus voltage without compensation.

(b) Bus voltage with compensation.

(c) Grid current with compensation.

(d) THD with compensation.

Figure 4.6: Main Plecs simulation results.

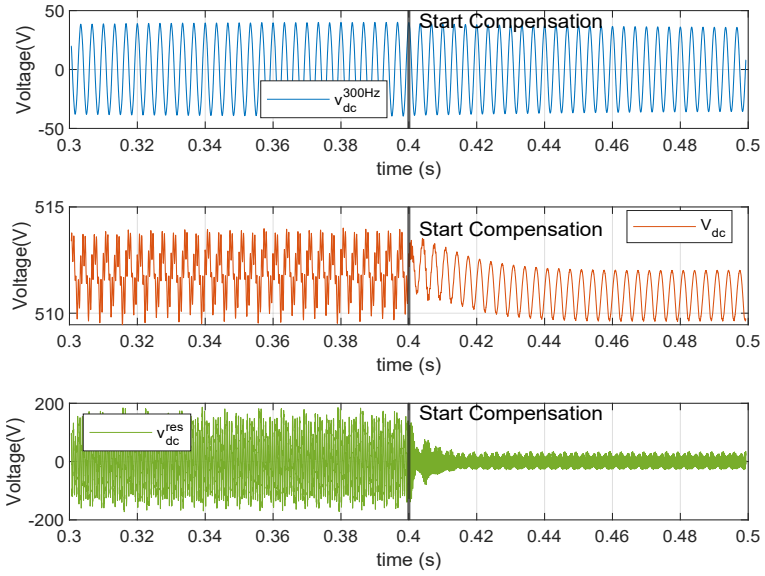


Figure 4.7: Computed dc-link voltage components.

For completeness, in Fig.4.8 are reported the motor phase currents and the duty cycles, it is possible to notice that the waveforms are more distorted. The active damping control use the motor to dissipate the oscillations, therefore, there is an distortion effect in the motor phase currents which cause an increase of noise and losses.

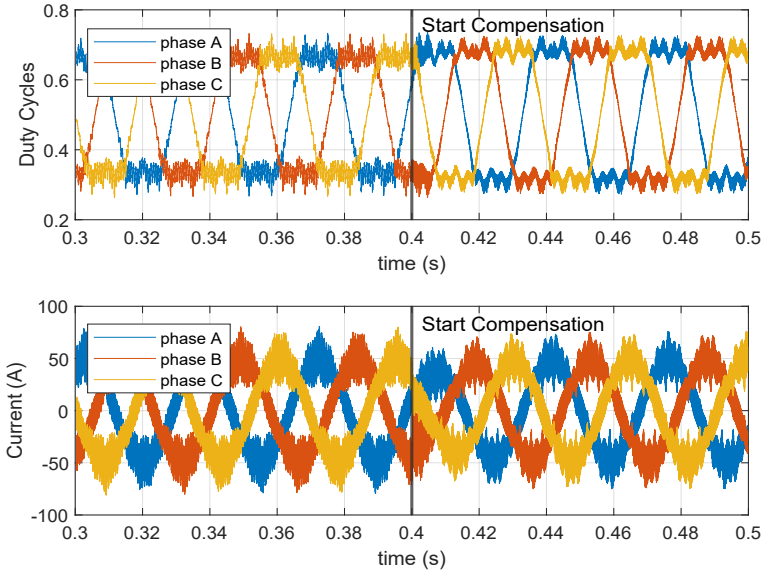


Figure 4.8: Motor phase currents and duty cycles.

4.5 MCU Configuration

Once the control strategy is validated and the converter schematics have been made, it is necessary to configure the script in C-code. In particular are reported: the external clock configuration, the timer structure and dead time computation and the ADC functional blocks with the type of conversion choice. The code is implemented using the software development tool STM32CubeIDE, which include the STM32CubeMX tool to configure the microcontroller functions at its pinout.

4.5.1 External Clock

As previously said, the microcontroller has an external crystal oscillator with 25MHz frequency, more precise than the internal 16MHz one. In Fig.4.9 is reported the system clock (SYSCLK) configuration at 170MHz starting from the 25MHz of the oscillator. This is done by selecting the external source and manipulating the frequency through the Phase Locked Loop (PLL) block, which allow to obtain the desired frequency. The choice of a system clock at 170MHz is related to the microcontroller specifications, reported in Tab.3.14, and the its manual recommendations to achieve the best performance guaranteed by the producer.

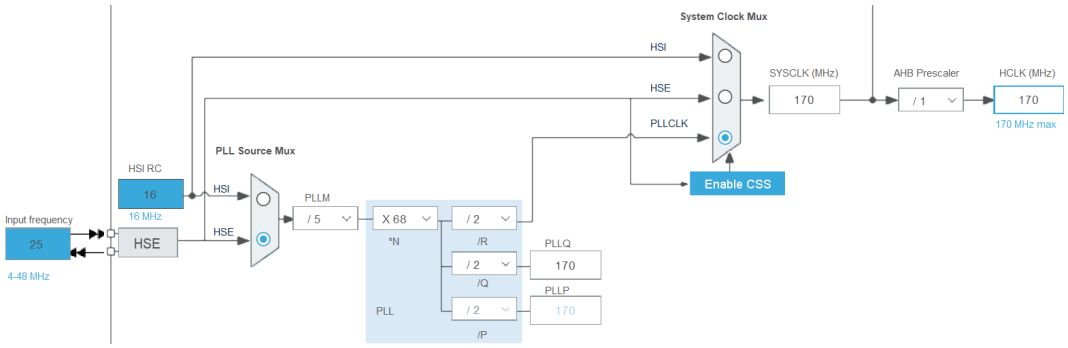


Figure 4.9: External clock configuration.

The Internal Watchdog timer (IWDG) is a down counter which guarantee the real-time execution of the control and it is mandatory in the power conversions. When the ISR occur the IWDG start the down count, from a predefined value written in an Auto Reload Register (ARR), and if it arrives to zero stops the power conversion. The ARR is set to arrive at zero after the interrupt duration, in this case it is sure that the real time execution is not guaranteed. The IWDG has to be manually set to the ARR value every time a new ISR starts.

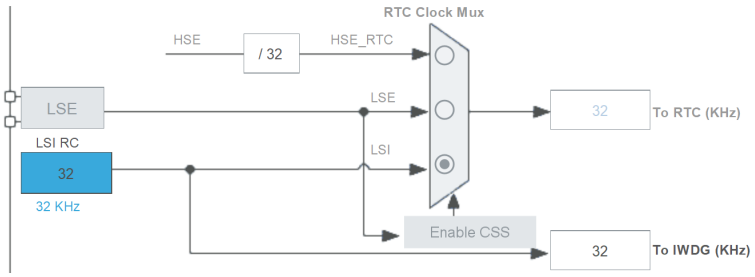


Figure 4.10: IWDG clock configuration.

4.5.2 Timer

Inside the microcontroller there are three types of timers: basic timers, general purpose timers, advanced-control timers. In this application is only used an advanced-control timer which is the core of the PWM operation and the interrupt generation. In Fig.4.11 is shown how an advanced-control timer to generate the triangular carrier and then the switching commands. In particular:

- CLK is the internal clock of the timer;
- CNT is the counter register, it counts the upper fronts of the timer clock signal up to a predefined value (ARR) and then down count to zero, this way to count is called Center Aligned Mode 3 and it allows to generate a symmetrical discretized triangular carrier;

- ARR is the auto reload register, its a register in which is written upper limit of the counter, this value define the triangular period and therefore the switching frequency;
- CCR is the capture/compare register, in this register are written the duty cycles, multiplied by the ARR and computed in the control routine code, to be compared with the carrier;
- UEV is the update event, when the CNT reaches the ARR value a trigger event is generated, this is the ISR signal which guarantee the real time execution;
- OCx and OCxN are the dual switching commands obtained by the PWM operation, they include the dead time (turn-on delay) defined by the user.

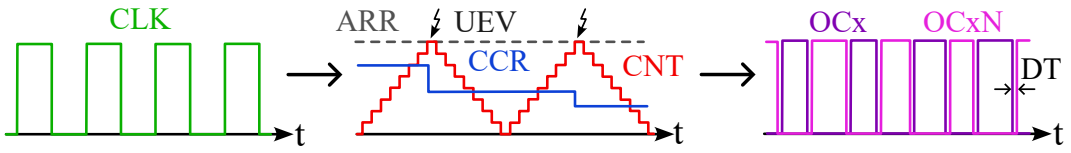


Figure 4.11: Timer general operation.

The timer clock (CLK) is generated starting from the system clock (SYSCLK) and then arrives to a prescaler block (PSC), which gives the possibility to obtain a clock signal with a lower frequency. In (4.1) is reported the formula to set the PSC value, in this application the PSC is imposed to 0, therefore, the timer clock is the same of the system one at 170MHz.

$$f_{CK\_CNT} = \frac{f_{CK\_PSC}}{PSC + 1} \tag{4.1}$$

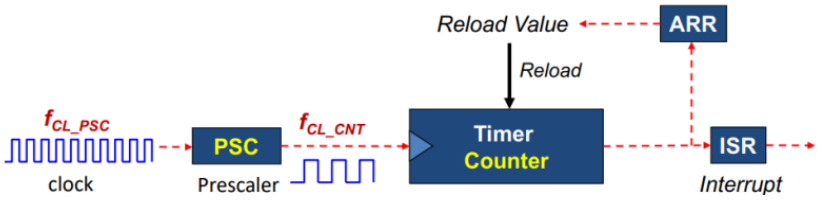


Figure 4.12: Timer prescaler block [14].

How previously said, the switching frequency (10kHz) is set by the ARR value, as the ratio between the clock and the switching frequency (4.2). It is important to notice the factor two at denominator, it is related to the symmetrical triangular carrier which requires half switching period to arrive from 0 to ARR and an other half back to front.

$$ARR = \frac{f_{CK\_CNT}}{f_{sw} \cdot 2} = 8500 \tag{4.2}$$

At this point it is necessary to set the Repetition Counter Register (RCR), which define when the interrupts have to be generated. In this case the RCR is imposed to 1, which means that the trigger events are generated only in the upper front of the triangular carrier, as shown in Fig.4.13.

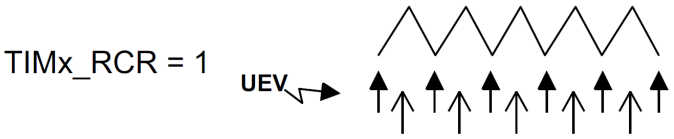


Figure 4.13: Timer RCR configuration [13].

When the switching command change its state from on to off, the switches commutation it is not instantaneous and have a certain transient which depends on the switch technology. In an inverter leg, if a switch is turned on when the other is still commuting, it can lead to not desired turn on of the switch imposed off creating a dangerous short circuit between the high voltage dc bus and the ground. The dead time (DT) is the turn-on delay time that is mandatory to avoid this situation, for this IGBT inverter it is chosen a dead time of 1μs. In Fig.4.14 are shown the dead time formulas to set the turn-on delay dependently on the desided dead time, where:

- DTG[7:0] is the 8 bit register of the dead time;
- t_{dtg} is the dead time period;
- t_{DTS} is the clock period.

DTG[7:5]=0xx => DT=DTG[7:0]x t_{dtg} with $t_{dtg}=t_{DTS}$.
DTG[7:5]=10x => DT=(64+DTG[5:0])xt_{dtg} with $T_{dtg}=2xt_{DTS}$.
DTG[7:5]=110 => DT=(32+DTG[4:0])xt_{dtg} with $T_{dtg}=8xt_{DTS}$.
DTG[7:5]=111 => DT=(32+DTG[4:0])xt_{dtg} with $T_{dtg}=16xt_{DTS}$.

Figure 4.14: Dead time configuration [13].

The first three most significant bit of the dead time register defines a specific turn on delay interval that can be exploited, in particular:

- 0xx: from 0ns to 749ns;
- 10x: from 750ns to 1.49μs;
- 110: from 1.5μs to 2.9μs;

- 111: from 3μs to 5.9μs.

To set 1μs dead time the useful formula is the second obtaining in the DTG register the value 149, as in (4.3).

$$DTG[5:0] = DT/t_{dtg} - 64 = 21(10101) \rightarrow DTG[7:0] = 149(10010101) \quad (4.3)$$

Once the main function blocks have been presented, in Fig.4.15 is shown the advanced-control timer block diagram where it is possible to notice how the previous functions interact to each other. Moreover, it is highlighted the break function block that allows to connect an emergency signal which instantaneously stops the PWM signal output.

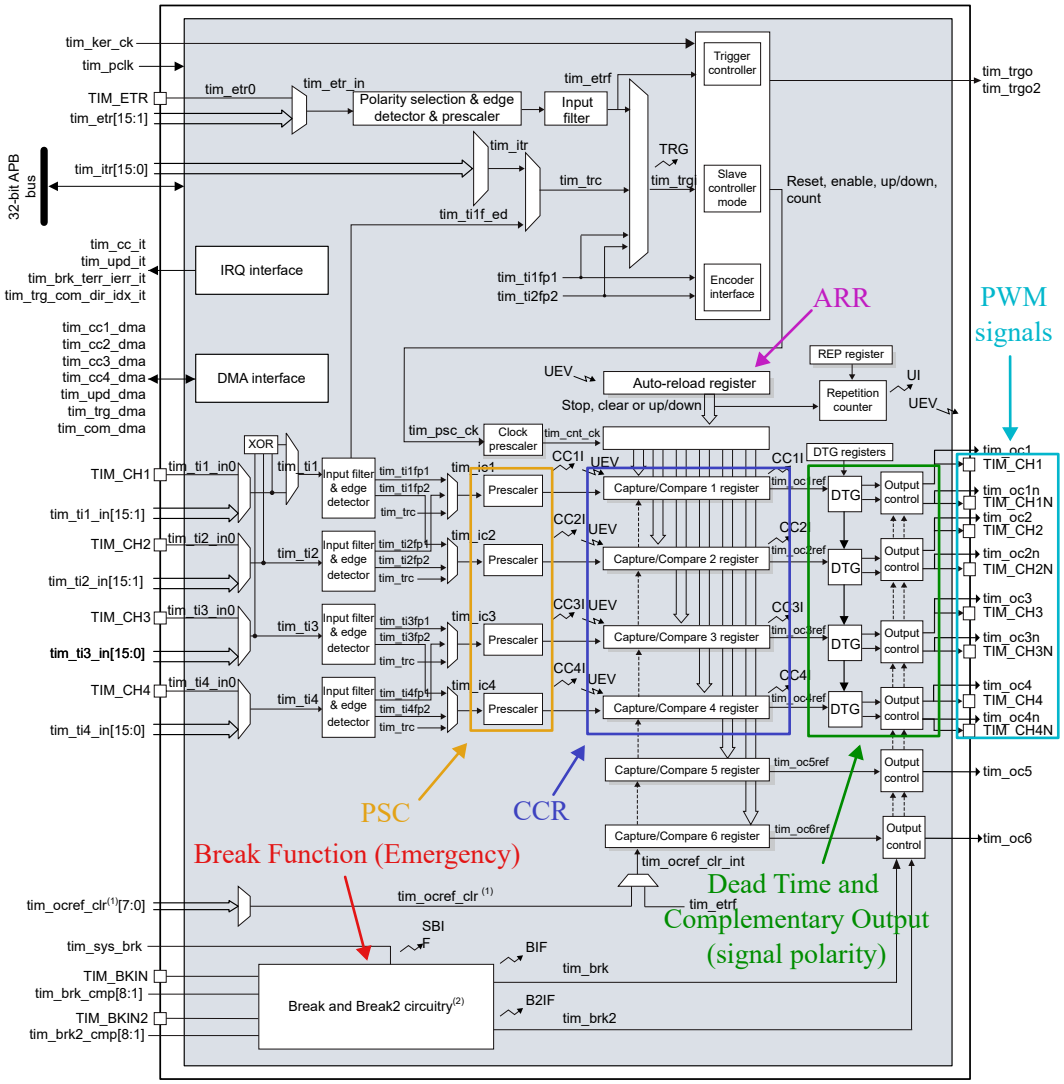


Figure 4.15: Advanced-control timer block diagram [13].

4.5.3 ADC

The Analog to Digital Converter is the one of the key element of the microcontroller, it allows to acquire the measurements coming from the sensors and translate them at the control as feedback. The ADC only accept signals from 0V to 3.3V and convert it in discrete form. In Fig.4.16 is shown the ADC equivalent model: there is a switch that is closed at each T_s, which represent the start conversion interrupt, and a Zero-Order Holder (ZOH) which reconstruct the continuous signal in a sample sequence. As shown in Fig.4.17, the analog to digital conversion is based on the Successive Approximation Register logic, in which, the digital data are written in the data register inside the SAR logic block and DAC converter [C!] and are compared with the analog input. The conversion start from the most significant bit (MSB) until the less significant one (LSB) and at each cycle is defined one bit, therefore, increasing the precision of the ADC, which meas higher number of bits, the conversion time increases. The compromise is to have a precise feedback wasting less time possible, this microcontroller have a 12-bit precision, which are written in a 16-bit data register. The ADC conversion delay is computed in (4.4), considering 2.5 ADC clock cycles.

$$T_{ADC} = (2.5 + 12.5) \cdot T_{CLK} \simeq 8.8ns \tag{4.4}$$

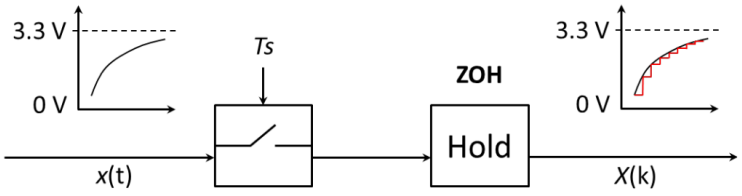


Figure 4.16: ADC equivalent model [14].

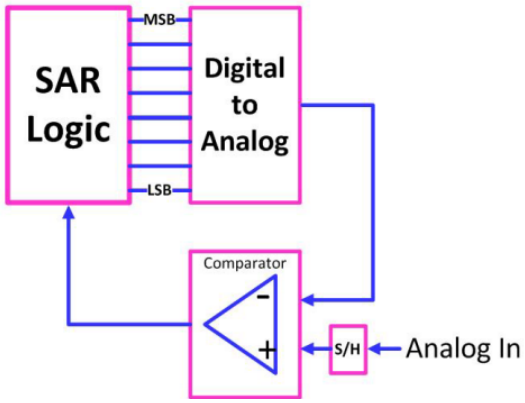


Figure 4.17: ADC SAR [14].

In Fig.4.18 is represented with more detail what the circuital ADC model. The sample and hold ADC converter have inside a capacitor that is charged at the input voltage value to be converted in discrete form. Moreover, it is possible to notice two diodes which have the role to clamp the input signal from 0V to 3.3V protecting the device.

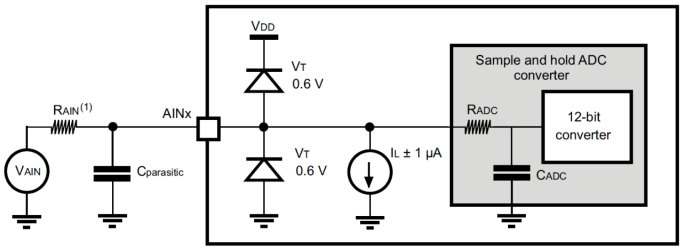


Figure 4.18: ADC structure [14].

The ADC has two types of conversions: single (Fig.4.19) and injected (Fig.4.20). In particular:

- Single conversion is a discontinuous operation mode which execute one conversion per each trigger event, it is used to acquire the the phase current and dc-link voltage measurements in which is reserved one ADC for each signal;
- Injected conversion execute conversions in sequence (up to four) per each trigger event and write it in a proper register which contain all of it, it is used to acquire the two temperature signals with the same ADC.

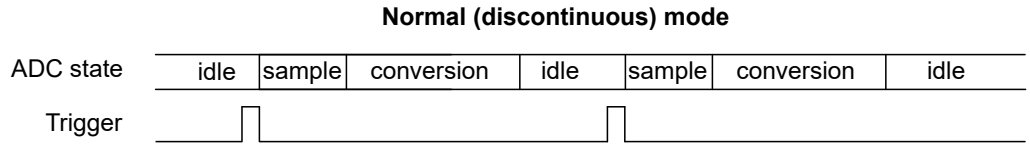


Figure 4.19: ADC single conversion mode [14].

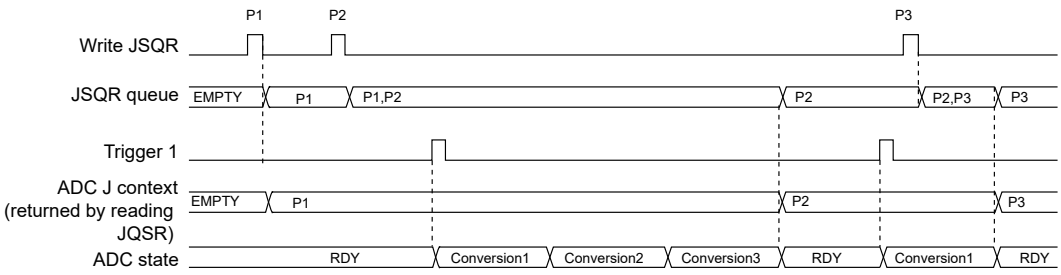


Figure 4.20: ADC JSQR [13].

Besides, in Fig.4.22 is reported the ADC block diagram where it possible to notice the SAR ADC connected to a Start& Stop control, linked to the timer trigger event, and the different types of A/D conversion configurations. Moreover, each ADC has up to 19 multiplexed channels.

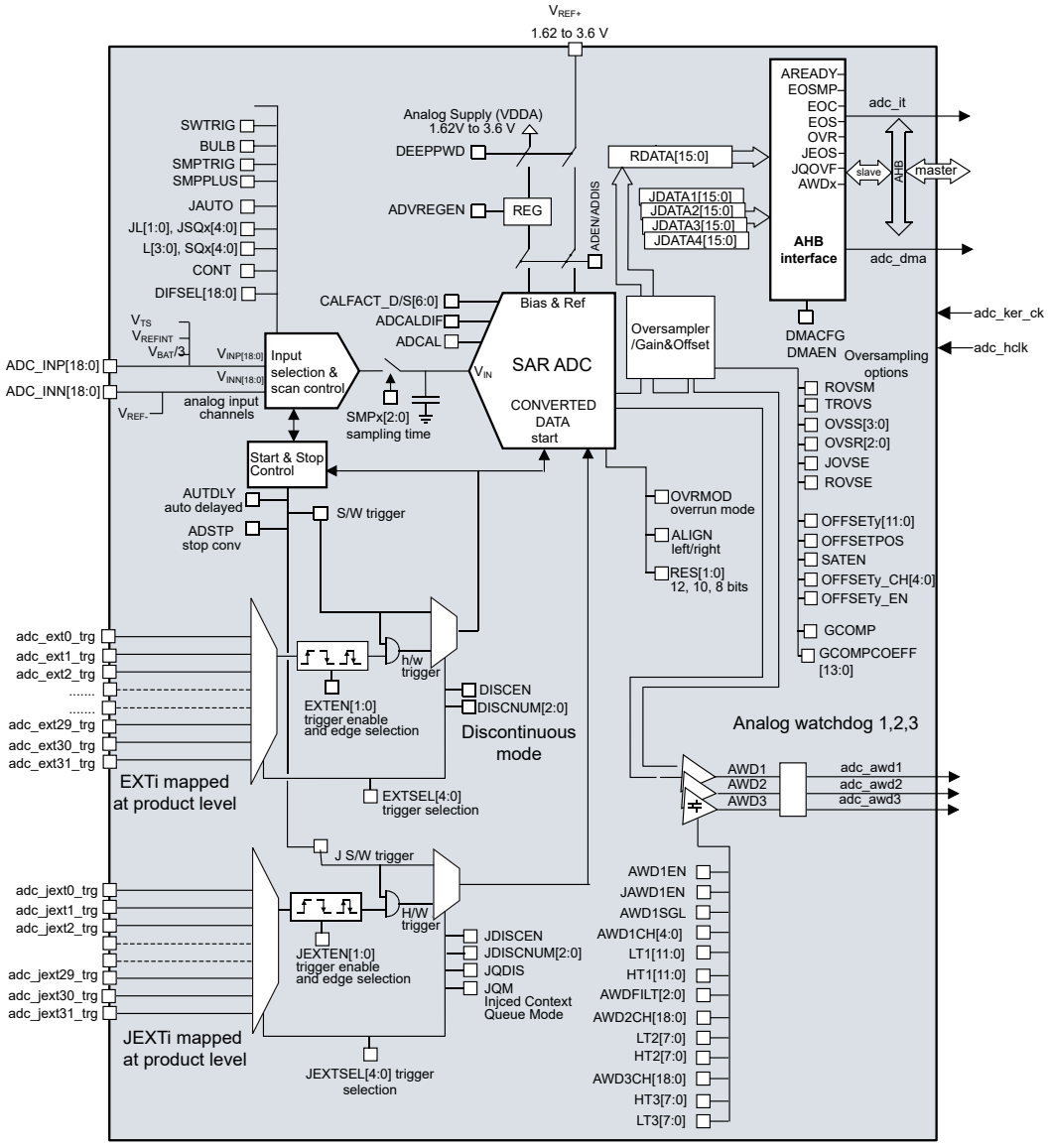


Figure 4.21: ADC block diagram [13].

4.5.4 C-Code

The C-code represents the control routine of the converter. The main motor control code is not reported, howeveer, it consists of: the coordinates transformations, the PI

regulators in d-q axis and the inverse transformations to compute the reference signals. To let the code running faster, all the variables and the mathematical operations are in float. Instead, in Fig.4.1 is shown the dc-link voltage filtering stage at 100kHz, the code is quite simple ad allow to obtain all the voltage components. Besides, to let the code more clear the PI regulators and the filters are written as functions, the variables in the electrical planes (abc, $\alpha\beta$, dq) are organized in term of structure and the coordinate transformations are defined as macro. The other parts of the code are not presented because they would require too much space and it is not the goal of this thesis focused on the hardware design.

```
1  //Resonant Filter at 300Hz
2  SSI.input = vdc;
3  ResFilter(&SSI);
4  vdc_6fg = SSI.output;
5  //vfilt_old = vdc_6fg;
6
7  //Low Pass Filter
8  LowPassF.input = vdc;
9  LPFilter(&LowPassF);
10 Vdc = LowPassF.output;
11
12 //Output Recostruction
13 vdc_res = vdc-Vdc-vdc_6fg;
14 vdc_id = Vdc+vdc_6fg;
15 vdc_rec = EnableComp*(kv0*vdc_id-kv*vdc_res);
```

Listing 4.1: Filtering stage C-code at 100kHz.

4.5.5 CCM SRAM Configuration

To improve the control routines computational time, the micrcontreller allows to use a Core-Coupled Memory (CCM) SRAM, the evaluation of the improvement will be discussed in the experimental results chapter. The CCM SRAM is tightly coupled with the Arm®Cortex®core, to execute the code at the maximum system clock frequency without any wait-state penalty. This also brings a significant decrease of the critical task execution time, compared to code execution from Flash memory [15].

When the code is located in CCM SRAM and data stored in the regular SRAM, the Cortex®-M4 core is in the optimum Harvard configuration. A dedicated zero-wait-state memory is connected to each of its I-bus and D-bus (Fig.**??**) and can thus perform at 1.25 DMIPS/MHz, with a deterministic performance of 213 DMIPS in STM32G4 devices. This also guarantees a minimal latency if the interrupt service routines are placed in the CCM SRAM [15].

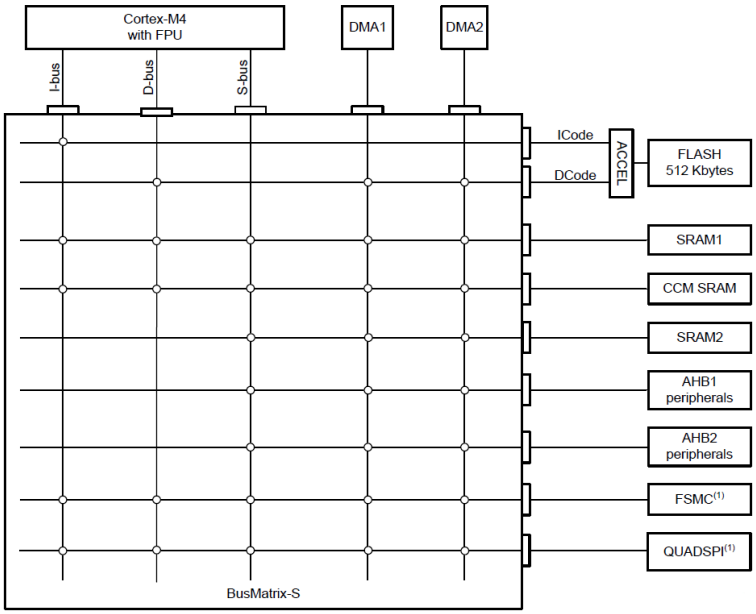


Figure 4.22: STM32G4 device system architecture [13].

The CCM SRAM has to be properly configured modifying the predefined microcontroller code. The first step is to define a new region (ccmram) in the linker file (.ld) by defining the start address and the size of the CCM SRAM region [15], as in Fig.4.2.

```
1
2 /* Memories definition */
3 MEMORY
4 {
5 RAM (xrw) : ORIGIN = 0x20000000, LENGTH = 112K
6 FLASH (rx) : ORIGIN = 0x8000000, LENGTH = 512K
7 CCMRAM (xrw) : ORIGIN = 0x10000000, LENGTH = 32K
8 }
```

Listing 4.2: CCM SRAM memory definition.

Then, it is necessary to instruct the linker that code sections with the ccmram attribute must be placed in CCM SRAM [15], the code is shown in Fig.4.3 .

```
1
2 /*--- New CCMRAM linker section definition ---*/
3 _siccmram = LOADADDR(.ccmram);
4 /* CCMRAM section */
5 .ccmram :
6 {
7 . = ALIGN(4);
8 _sccmram = .; /* define a global symbols at ccmram start */
9 *(.ccmram)
10 *(.ccmram*)
11 . = ALIGN(4);
```

```
12 _eccmram = .; /* define a global symbols at ccmram end */
13 } >CCMRAM AT> FLASH
14 /*--- End of CCMRAM linker section definition ---*/
```

Listing 4.3: CCM SRAM linker section definition.

At this point, as reported in Fig.4.4, the startup file is modified to initialize data and code to place in CCM SRAM at startup time [15].

```
1
2 /* Copy data from FLASH to CCMRAM */
3   movs r1,#0
4   b  LoopCopyCcmInit
5
6 CopyCcmInit:
7   ldr r3, =_siccmram
8   ldr r3, [r3, r1]
9   str r3, [r0, r1]
10  adds r1, r1, #4
11
12 LoopCopyCcmInit:
13  ldr r0, =_sccmram
14  ldr r3, =_eccmram
15  adds r2, r0, r1
16  cmp r2, r3
17  bcc CopyCcmInit
18 /* Enf of copy to CCMRAM */
```

Listing 4.4: CCM SRAM strat up modification.

Finally, it is possible to place the part of code to be executed from CCM SRAM in the .ccmram section by adding the attribute key word in the function prototype [C!] (Fig.4.5). In particular, it is necessary to place in the CCM SRAM the two ISR (10kHz and 100kHz) and the timer and ADC HAL interrupts.

```
1
2 __attribute__((section (".ccmram")));
```

Listing 4.5: CCM SRAM function prototype.

Chapter 5

Experimental Results

Once the control strategy is explained and simulated, this chapter aims to validate experimentally the active damping control based on the dc-link voltage compensation. The test bench used for the validation is not the one designed during this thesis, but it is an existing three-phase drive, modified with a slim DC-Link. For this reason, it is expected that the results obtained from this test and that coming from the PLECS simulation are not the same. Therefore, the objective is not to see in detail the real component behavior and how they influence the results with respect to the simulation one, but to qualitative highlight the damping control effects on the main electrical quantities and validate its effectiveness.

In Fig.5.1 is shown the scheme of the adopted test bench, it is possible to notice that, before the rectifier there is an LC circuit that there is not in the designed converter. Moreover, There are no information about the grid parameters, especially the grid inductance, which influences a lot the system behavior.

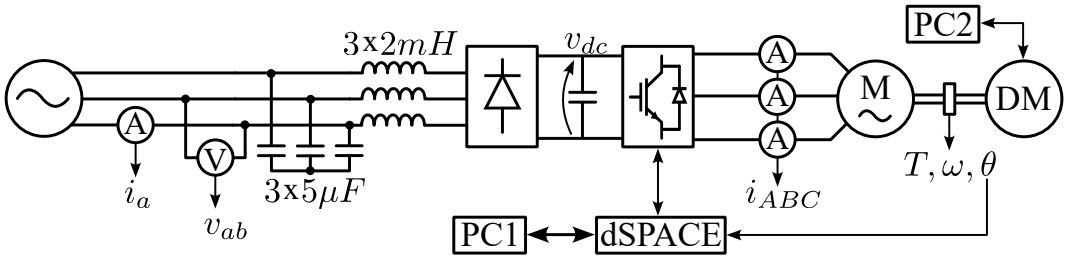


Figure 5.1: Test bench schematic.

The developed test bench is reported in Fig.5.2 where are highlighted the main components, more precisely:

- The MOTOR (Fig.5.3a) is the electric machine under test, where in Tab.5.2 are resumed its main characteristics, it is important to notice that its nominal power (2.2kW) is lower than the 7.5kW considered in the sizing, this is another important difference between the two system;

- The CONVERTER (Fig.5.3b and Fig.5.3c) consists of a 2-levels, three-phase drive inverter (which main characteristics are summarized in Tab.5.1), the relays and the LC filter;
- The DRIVING MACHINE (Fig.5.3a) simulate the load and it controlled at constant speed;
- In the CONTROLLER is located the control algorithm, for the motor it is adopted a current control where the references are imposed through a proper Graphical User Interface (GUI);
- The ACQUISITION SYSTEM consists of a series of tools which condition and sample the quantities to be measured.

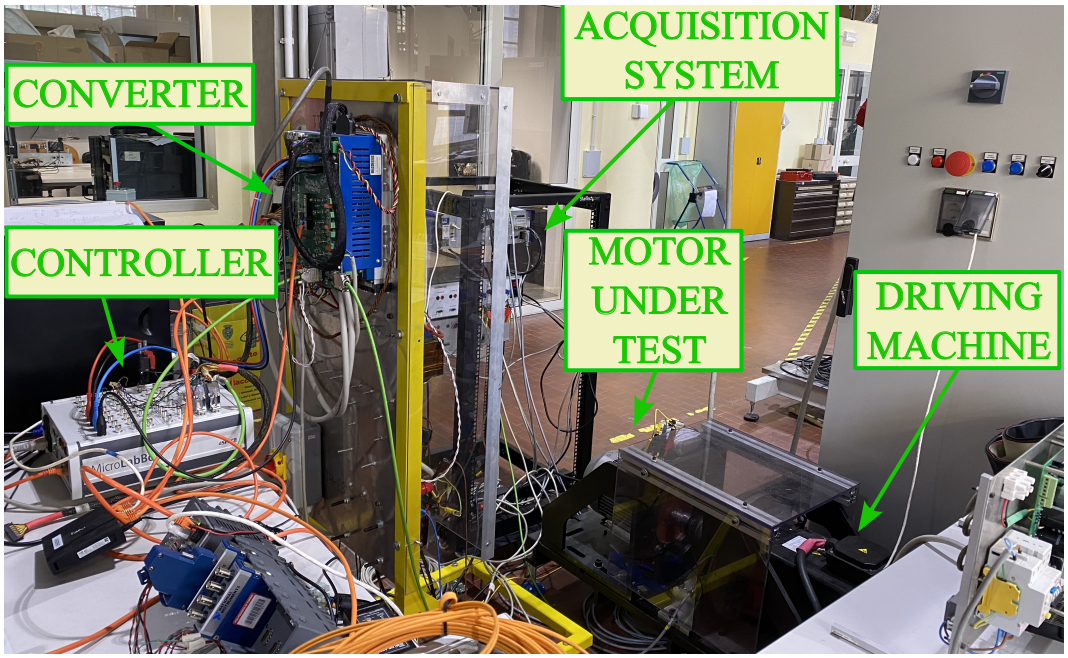
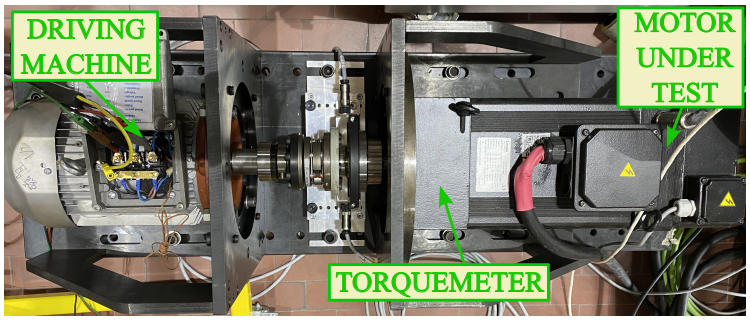


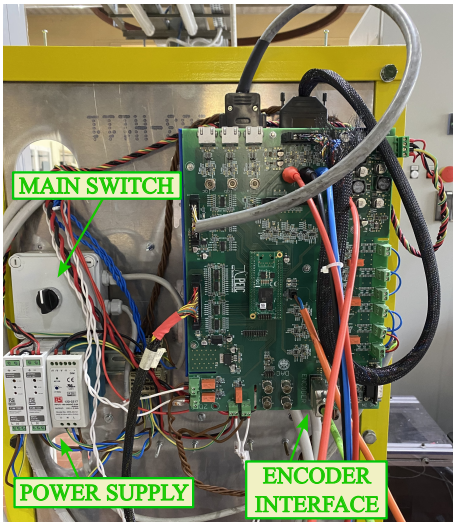
Figure 5.2: Test bench implementation.

Table 5.1: Converter under test specifications.

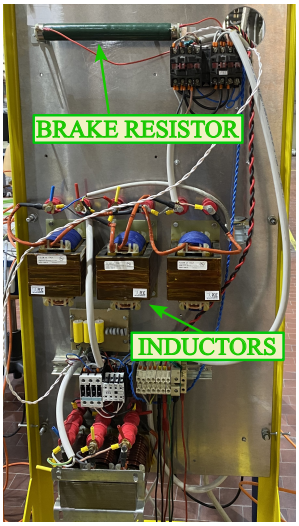
Topology	3-phase diode bridge+2-level IGBT inverter+brake leg
Dc-link Capacitance	10μF
Switching Frequency	10kHz
Maximum Dc-link Voltage	750V
Nominal Output Current	$25A_{RMS}$



(a) Motor bench.



(b) Converter front view.



(c) Converter back view.

Figure 5.3: Test bench main component.

Table 5.2: Motor under test specifications.

Motor type	PM-Assistant SyncRel
Rated Power	2.2kW
Poles	4
Rated Speed	1800rpm
Rated Torque	11.7Nm
Rated Voltage	460V
Current at Full Load	3.4A

The GUI for the data acquisition, shown in Fig.5.4, has to be properly configured by selecting the sensors dependently on the quantities that have to be measured. Moreover, this software allows to perform calculations and it is useful in this case to compute in real time the THD of the grid current. Instead, in Fig.5.5 is reported the dSPACE

interface, it allows to control the converter with the active damping control algorithm and it can be configured using the software Simulink. Besides, it is possible to notice the control buttons to impose the current reference and enable or disable the dc-link voltage compensation.

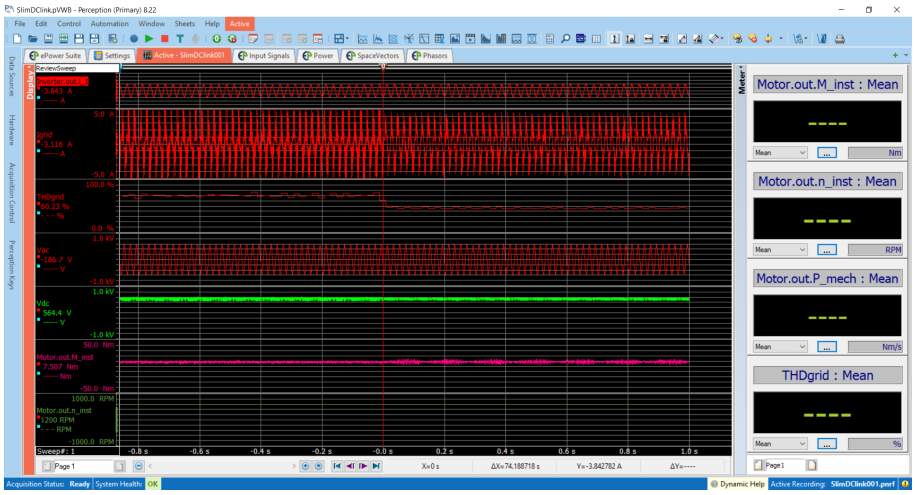


Figure 5.4: Software for data acquisition (Perception).

Figure 5.5: Software for motor control (dSPACE).

As previously declared, the driving machine imposes the speed and motor is controlled in torque by manipulating the two current reference i_d, i_q. The algorithm is tested in three different conditions:

- Constant speed at 1200rpm, with a mechanical torque of 8Nm(i_d=2A, i_q=3A) and an output power of 1kW;

- Constant speed at 600rpm, with a mechanical torque of 8Nm(i_d=2A, i_q=3A) and an output power of 0.5kW;
- Zero speed and zero torque (i_d=0A, i_q=0A).

The experimental results of the first condition are reported in Fig.5.6. According to the simulation outcome, when the compensation starts the dc-link voltage and the grid current resonances are reduced, the motor damps this oscillations in Joule losses and for this reason the harmonic content of the phase currents increases. Moreover, the damping effect increases by increasing the output power.

In Fig.5.7 is shown the second condition and, how could be expected, it possible to notice that halving the mechanical power the compensation effect is reduced.

The third case, in Fig.5.8, shows how the compensation is only needed when active power is transferred by the inverter. When the inverter works at no load, then the DC-link is not subject to oscillations.

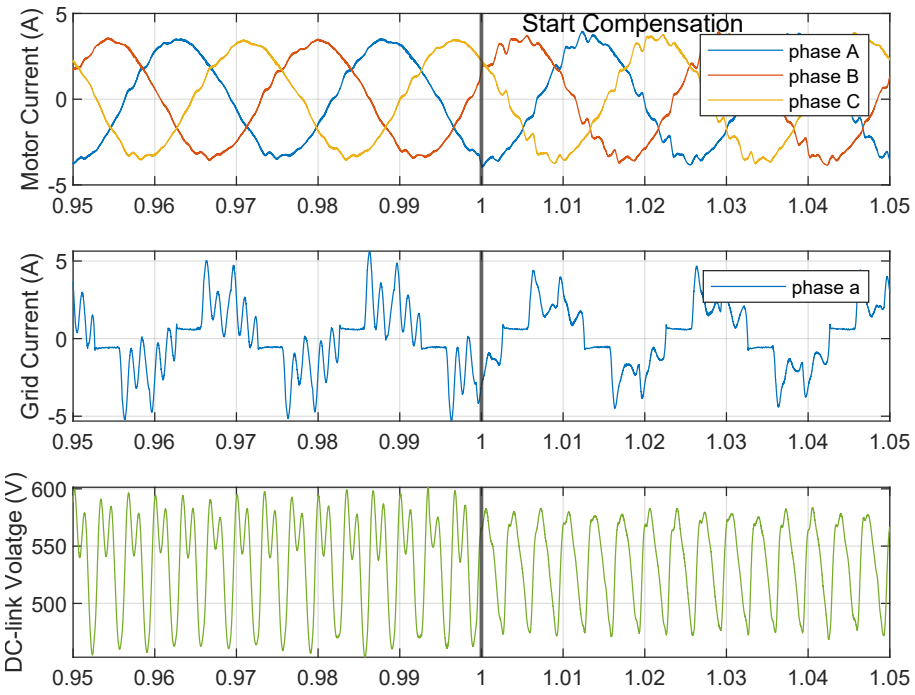


Figure 5.6: Experimental test at 1200rpm.

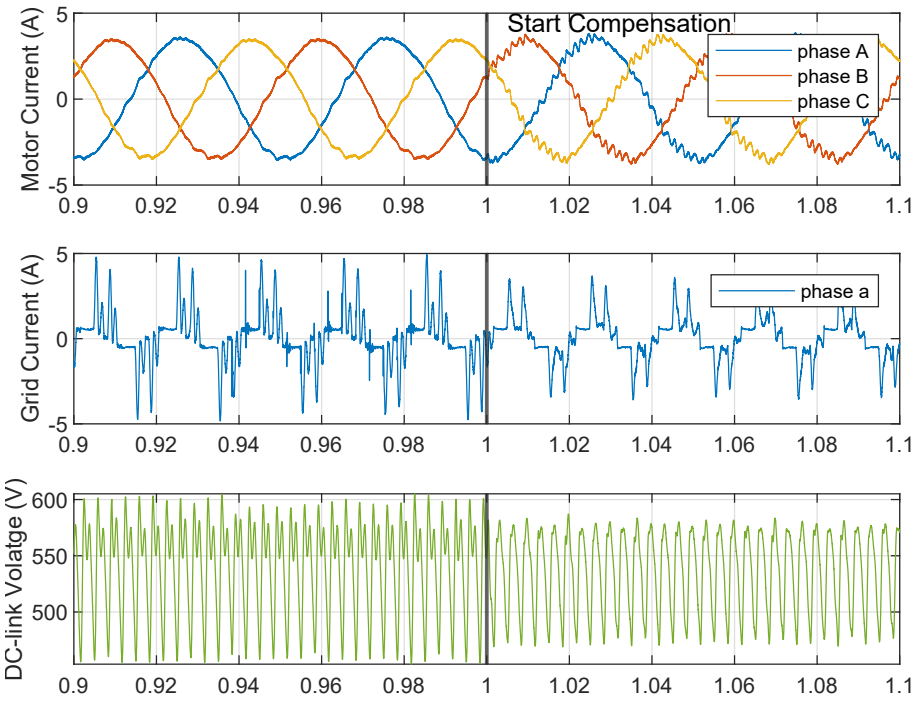


Figure 5.7: Experimental test at 600rpm.

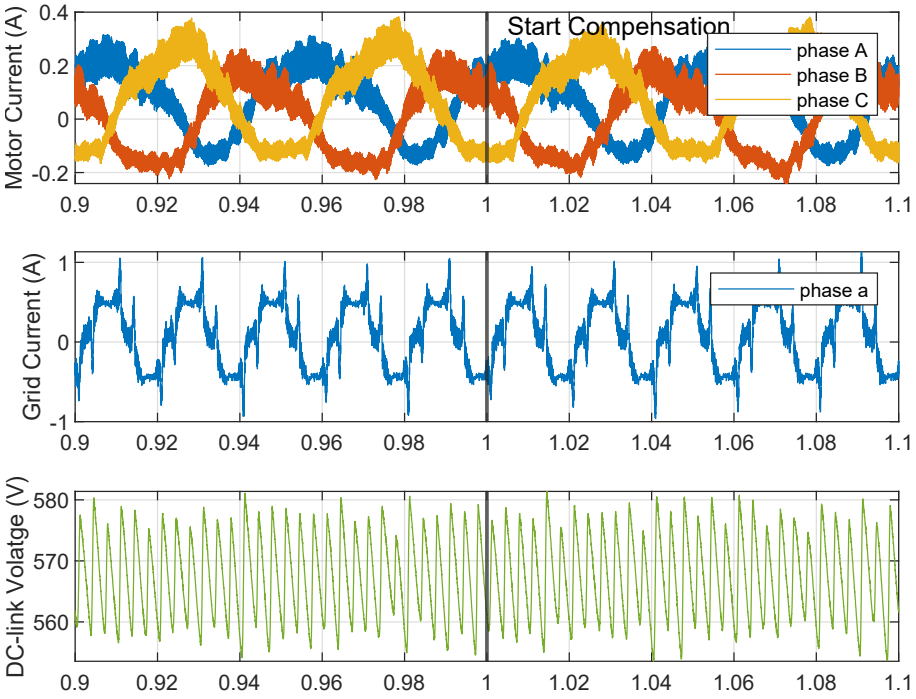


Figure 5.8: Experimental test at zero speed.

In Fig.5.9 are reported the grid current THD results in the three conditions and, in general, when the dc-link voltage compensation starts the harmonic content decreases. Even in this case, it is confirmed that the damping effect increases by increasing the power, in facts, the THD is lower when the power output is 1kW. The condition at zero speed is not so relevant but it underline that in this condition the compensation is null and consequently there is not effect in the grid current THD.

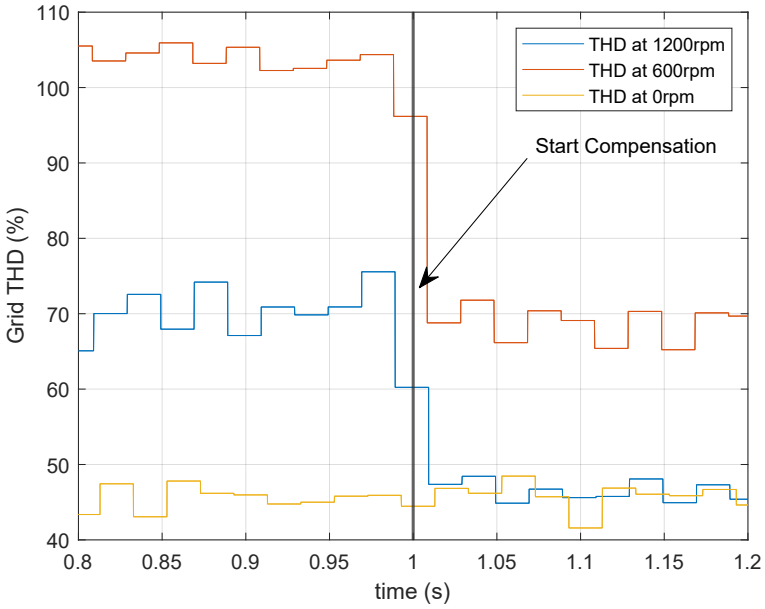


Figure 5.9: Grid current THD experimental results.

As previously declared, once the compensation starts the harmonic content increases to damp the oscillations, with an increase in the current RMS value and consequently a rising in the power losses and a decrease in the efficiency. Besides, it is possible to hear a small noise increase in the motor, which cause higher mechanical stress in the bearing with a consequent lower lifetime. In Fig5.10 and Fig.5.11 are reported the motor power losses and efficiency acquired in the test bench, these curves are computed in real-time starting from the measurements and, due to the huge number of samples per seconds, the calculations are not very precise and cause an overlapped ripple in the graph. However, it is possible to distinguish, after the compensation, a modest increase in the power losses and small reduction in the motor efficiency. For example, considering the first case with 1kW output power, the RMS current change from 2.46A to 2.57A with an increase of the 4.65% which correspond (assuming the resistance constant) approximately to a rise of the 9.5% in the power losses. Considering in this condition 90W of losses it follows that after the compensation they approximately reach 99W, this small increase is the reason why in the large y-axis scale the variations are not so clear.

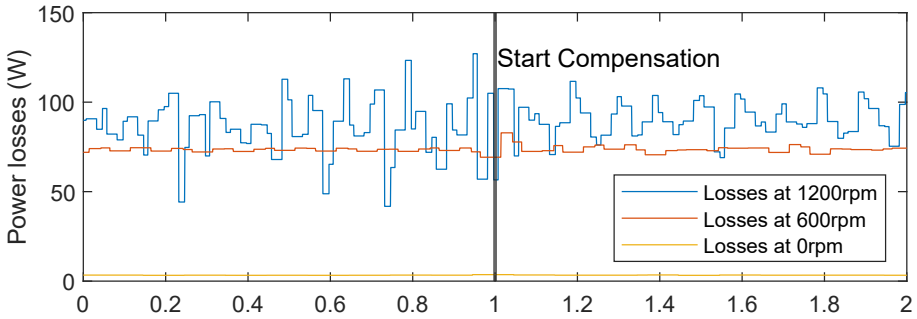


Figure 5.10: Motor power losses.

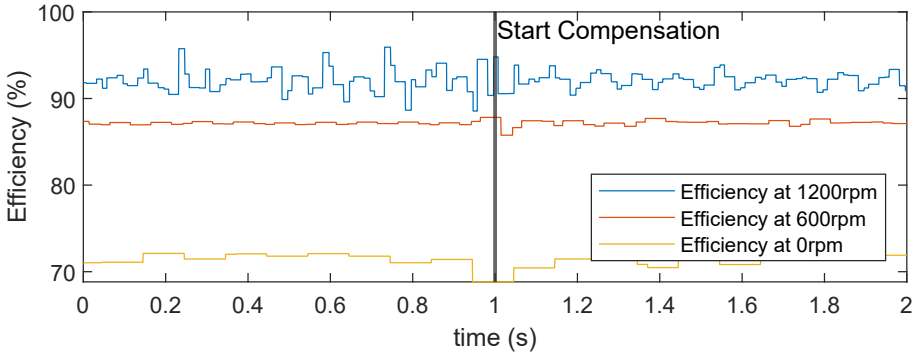


Figure 5.11: Motor efficiency.

For completeness, in Fig.5.12 are shown the brake leg commands which is piloted ON when the dc-link voltage exceed 600V. It is interesting to notice that after the compensation the brake leg is always OFF because the resonance oscillations are abundantly reduced.

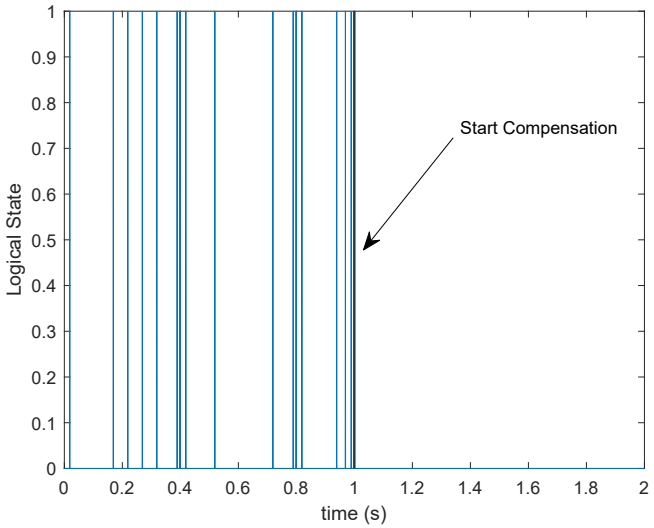


Figure 5.12: Brake leg logical switching commands.

Chapter 6

Conclusions

In this thesis is presented, simulated and experimentally tested the design of a slim dc-link converter for industrial adjustable speed drives composed of a three phase diode rectifier and a 2-level IGBT-base three phase inverter, featuring low grid current total harmonic distortion (THD) and increasing the converter reliability by exploiting the film capacitors for the dc-link. The focus is mainly centered in the converter hardware design, with the components choice to met the specifications and the development of the schematics, and in the control strategy to stabilize the dangerous resonance caused by the reduced dc-link capacitance. In particular, the implementation steps are the following:

- Build a mathematical model of the system to analyze the resonances to choose the best control strategy;
- Simulate the system to evaluate the performance of the control code;
- Find the power module which met all the requirements;
- Based on the measurement required by the control, choosing all the sensors and the devices to let the system work, such as gate drivers, power supply, etc.;
- Develop the schematics of the converter;
- Size the heatsink and validate it with a thermo-fluid dynamic analysis;
- Perform experimental tests to validate the control algorithm.

The presented control strategy is based on the voltage modulation using virtual positive impedance concept (VPIC), which damp the resonances in the grid currents and in the dc-link voltage exploiting the electric machine and generating additional losses. The pros and cons of a slim dc-link drive with this control strategy, with respect to standard applications with electrolytic capacitors, are summarized in the following table:

Table 6.1: Slim dc-link drive with voltage modulation using VPIC pros and cons.

PROS	CONS
higher power density	higher losses and consequently lower efficiency
higher reliability	higher noise and mechanical stress
lower grid current THD	requires higher computational performances

How it could be expected, the experimental results (using an existing converter with a slightly different topology) shows an important decrease in the grid current THD and the almost complete disappearance of resonances in the dc-link voltage, confirming qualitatively the simulation results.

6.1 Personal Contribution

My personal contributions to this project are:

- Literature review about the active damping control algorithm;
- Choice of the most suitable control strategy;
- Simulation of the system and control validation;
- Choice of the power module based on a personalized figure of merit;
- Sensors and devices overview and choice of the bests in terms of performances, complexity and cost;
- Developments of the schematics;
- Choice of the heatsink and fans with thermo-fluid dynamic analysis to validate the sizing;
- Configuration of the microcontroller peripherals and code and memory optimization to reduce the computational time.

6.2 Future Work

At the end of this thesis work, the converter is totally design and control strategy is validated, however, to realize the final products the PCB has to be routed, soldered and tested. Then, control algorithm has to be implemented in the microcontroller and the results has to be compared with the simulations one to obtain the same behavior. Moreover, the converter has not an encoder interface, therefore, it is necessary to develop a sensorless control of the electric machine which is suitable with the voltage modulation using virtual positive impedance concept.

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