

POLITECNICO DI TORINO

Master's Degree in Biomedical Engineering



Master's Degree Thesis

**Design and Development of an
External Processing Unit for Wireless
Power and Data Transmission
to Miniaturized Neural Implants for
Reverting Blindness**

Supervisors:

Prof. Danilo DEMARCHI

Prof. Sandro CARRARA

Eng. Gian Luca BARBRUNI

Candidate

Francesca RODINO

Co-Supervisors:

Dott. Paolo MOTTO ROS

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*“Alla mia mamma:
a te che mi hai dato la vita,
a te che sei sempre stata al mio fianco,
a te che mi hai insegnato a non smettere di sognare”.*

*“Al mio papà:
la mia forza,
la mia determinazione,
il mio coraggio”.*

Abstract

For decades, the investigation of brain functionalities has been a point of care for neuroscientists. The accelerated progress of knowledge of the neural motor system and the significant advances in nano- and micro-technology have led to solid growth in implantable devices technology. Despite the promising prospects of these devices, most of these implants still face limitations due to the bulky implant, the wiring, the limited number of channels, and the invasiveness of the surgical procedure, which cause significant risks for the patient and may cause the failure of the implant.

The next generation of implantable neural devices aims to build battery-free, miniaturized, and wirelessly powered implants to achieve a new approach for neural interfaces, thus developing innovative implantable neural prostheses to restore impaired or lost neurological functions. Ultra-miniaturized and wirelessly powered devices, freely distributed in the human brain, are the cornerstone of *Neural Dust*. Starting from this concept, the ongoing research project in which my master's thesis is inserted aims to develop an innovative CMOS-based cortical neuroprosthesis to restore vision by stimulating the visual cortex through penetrating and intracortical microelectrodes.

This work, carried out in Bio/CMOS Interfaces group at Integrated Circuits Laboratory (EPFL, Neuchâtel), has focused on the design and optimization of the External Processing Unit (EPU) for such cutting-edge cortical prostheses. The EPU includes the: i) video-capturing unit; ii) image processing system; and iii) radiofrequency (RF) base station for simultaneous power and data transfer through an innovative 3-coils inductive link.

The transmitter coil was designed and fabricated, focusing on the power transmission and bandwidth trade-off. The adopted solution is based on an L-type impedance matching circuit, and the optimization has been achieved with coils of different shapes and sizes.

The printed circuit board (PCB) of the RF base station has been designed and manufactured starting from the work of Barbruni et al. [1] and Barbara Gentile [2]. The system generates an amplitude-modulated RF signal at 433,92 MHz by deploying the amplitude-shift keying (ASK) modulation technique and can deliver

32 dBm combined with a data rate up to 10Mbps and a modulation index of 15.7%. The acquisition and processing of the images and the information delivery to the PCB have been programmed to be synchronous to ensure the real-time operation of the entire process flow. Each frame is captured from a webcam and processed in real-time with a segmentation algorithm implemented in MATLAB software and sent via UART to the RF base station, ensuring data modulation.

Finally, validation experiments were conducted on the completed system setup. Based on the satisfactory results, the project concluded with the design and manufacturing of a plastic package for the entire EPU.

The latter can wirelessly transmit information regarding the activation and the intensity of the stimulation of each active pixel of each frame toward the implanted free-floating CMOS-based units in real-time.

Keywords: Implantable Medical Device, Neural Implants, Miniaturisation, Cortical Visual Prostheses, Wireless Power Transfer, Inductive Power Transfer, RF Transmitter, ASK Modulation, Matching Network, Image Processing.

Sommario

Per decenni, l'indagine sulle funzionalità cerebrali è stata un punto di attenzione per i neuroscienziati. Il progresso accelerato della conoscenza del sistema neurale-motorio e i significativi progressi nella nano- e microtecnologia hanno portato a una solida crescita nella tecnologia dei dispositivi impiantabili. Nonostante le promettenti prospettive di questi dispositivi, la maggior parte di questi impianti deve ancora affrontare le limitazioni dovute alle dimensioni ingombranti, al cablaggio, al numero limitato di canali e all'invasività della procedura chirurgica, che causano rischi significativi per il paziente nonché il possibile fallimento dell'impianto stesso.

La prossima generazione di dispositivi neurali impiantabili mira a costruire impianti senza batteria, miniaturizzati e alimentati in modalità wireless per raggiungere una nuova concezione di interfacce neurali, quindi sviluppando protesi neurali impiantabili innovative per ripristinare le funzioni neurologiche compromesse. I dispositivi ultra-miniaturizzati e alimentati in modalità wireless, distribuiti liberamente nel cervello umano, sono i punti chiave del *Neural Dust*, letteralmente polvere neurale. Partendo da questo concetto, il progetto di ricerca in corso, in cui è inserita la mia tesi di laurea magistrale, mira a sviluppare un'innovativa neuroprotesi corticale basata sulla tecnologia CMOS per ripristinare la visione stimolando la corteccia visiva attraverso microelettrodi intracorticali.

Questo lavoro, svolto in collaborazione con il gruppo Bio/CMOS Interfaces presso il Laboratorio di circuiti integrati (EPFL, Neuchâtel), si è concentrato sulla progettazione e l'ottimizzazione dell'unità di elaborazione esterna (EPU) per tali protesi corticali all'avanguardia. L'EPU comprende: i) unità di acquisizione video; ii) sistema di elaborazione delle immagini; e iii) trasmettitore a radiofrequenza (RF) per il trasferimento simultaneo di potenza e dati attraverso un innovativo collegamento induttivo a 3 bobine.

La bobina del trasmettitore è stata progettata e fabbricata concentrandosi sul miglior compromesso tra trasmissione di potenza e larghezza di banda. La soluzione adottata si basa su un circuito di matching di impedenza di tipo L, e l'ottimizzazione è stata ottenuta con bobine di diverse forme e dimensioni. Il circuito stampato (PCB) del trasmettitore a RF è stato progettato e realizzato a partire dal lavoro di Barbruni et al. [1] e Barbara Gentile [2]. Il sistema genera un segnale RF

modulato in ampiezza a 433,92 MHz implementando la tecnica di modulazione ASK (amplitude-shift keying) e può fornire 32 dBm con una velocità di dati fino a 10Mbps e un indice di modulazione del 15,7%.

L'acquisizione e l'elaborazione delle immagini, e l'invio delle informazioni alla PCB sono state programmate per essere sincrone per garantire il funzionamento in tempo reale dell'intero processo. Ogni fotogramma viene catturato da una webcam ed elaborato in tempo reale con un algoritmo di segmentazione implementato con il software MATLAB, e inviato tramite UART al trasmettitore a RF garantendo la modulazione dei dati.

Infine, sono stati condotti esperimenti di validazione sulla configurazione completa del sistema. Sulla base dei risultati soddisfacenti ottenuti, il progetto si è concluso con la progettazione e la produzione di una custodia di plastica per l'intera EPU. Quest'ultima può trasmettere in modalità wireless e in tempo reale le informazioni riguardanti l'attivazione e l'intensità della stimolazione di ciascun pixel attivo per ciascun fotogramma verso le unità CMOS impiantate.

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Acronyms

AI

artificial intelligence

AMD

Age-related Macular Degeneration

APT

Acoustic Power Transfer

ASK

Amplitude-Shift Keying

ASIC

Application-Specific Integrated Circuit

BW

BandWidth

CMOS

Complementary Metal-Oxide Semiconductor

CPT

Capacitive Power Transfer

DC

Direct Current

DR

Data Rate

DRC

Design Rules Check

DSO

Digital Storage Oscilloscope

EM

ElectroMagnetic

EMI

ElectroMagnetic Interference

EPU

External Processing Unit

FCC

Federal Communications Commission

FFT

Fast Fourier Transform

GPIO

General Purpose Input/Output

IC

Integrated Circuit

IEU

Implantable Electronic Unit

IMDs

Implantable Medical Devices

IMN

Impedance Matching Network

IPT

Inductive Power Transfer

ISM

Industrial, Scientific and Medical

I2C

Inter-to-integrated Circuit

LGA

Lateral Geniculate Nucleus

LSK

Load-Shift Keying

MEA

Micro Electrodes Array

MCU

MicroController Unit

MI

Modulation Index

OOK

On-Off Keying

PA

Power Amplifier

PC

Personal Computer

PCB

Printed Circuit Board

PDL

Power Delivered to the Load

PLL

Phase-Locked Loop

PT

Power Transfer

PTE

Power Transfer Efficiency

Q

Quality Factor

RP

Retinitis pigmentosa

RF

Radio Frequency

SAR

Specific Absorption Rate

SMA

SubMiniature version A

SPI

Serial Peripheral Interface

SW

Switch

UART

Universal Asynchronous Receiver/Transmitter

US

UltraSound

USB

Universal Serial Bus

USCI

Universal Serial Communication Interface

VNA

Vector Network Analyzer

VSWR

Voltage Standing Wave Ratio

WDT

Wireless Data Transfer

WHO

World Health Organization

WPT

Wireless Power Transfer

WG

Waveform Generator

Chapter 1

Introduction: The Impact of Neurotechnologies

Neural interfaces are an emerging technology that has undergone considerable progress over the last few decades, becoming the principal technique for brain monitoring, sensing, and stimulation.

Up to now, electrical modulation techniques used in neuroscience are divided into *invasive* and *non-invasive* brain stimulation methods. *Non-invasive* methods exploit an approach based on electromagnetic interaction for brain neuromodulation to affect neural electrical activity without needing implanted parts. The *invasive* approach, on the contrary, exploits the use of micro-electrodes arrays (MEAs) implanted in the cerebral cortex at specific points according to the therapy to be delivered. This method connects the MEAs to an implantable electronic unit (IEU) via cable.

Since the first pacemaker implantation in 1958, the technological development of implantable medical devices (IMDs) has undergone enormous growth in terms of batteries, power consumption, materials, and miniaturization [3]. In 1969, the first cochlear implant to restore the sense of sound demonstrated the feasibility of neural implants [4].

The first recorded use of electrical stimulation dates to AD 46 as a therapy to relieve headaches, and nowadays, neurostimulation is considered an established and effective approach to treat a vast number of diseases, from movement disorders and chronic pain to sensory prosthetic devices, such cochlear implants, spinal cord stimulators [5] and visual prosthesis.

1.1 Visual Prosthesis

According to the World Health Organization (WHO), visual impairment is one of the ten most prevalent causes of disability that afflicts more than 43 million people worldwide [6]. Although a non-negligible percentage has a treatable or predictable disease, most patients have a non-curable disease.

Blindness is caused by the interruption of the normal flow of signals along the visual pathway, whose main blocks are the *eye*, the *optic nerve*, the *lateral geniculate nucleus (LGN)*, and the *visual cortex* located in the occipital part of the brain [5], as shown in Fig. 1.1.

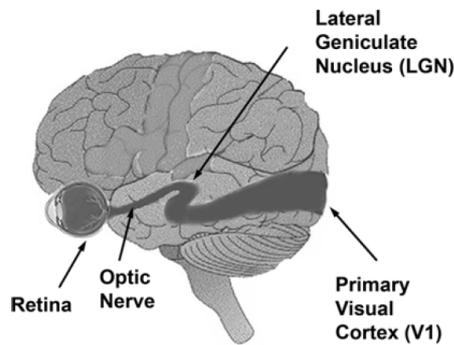


Figure 1.1: Visual pathway. Reprinted from [5].

Depending on the target location to be stimulated among the visual pathway, three different types of implants are developed: *retinal*, *optic nerve*, and *cortical* prostheses (Fig. 1.2).

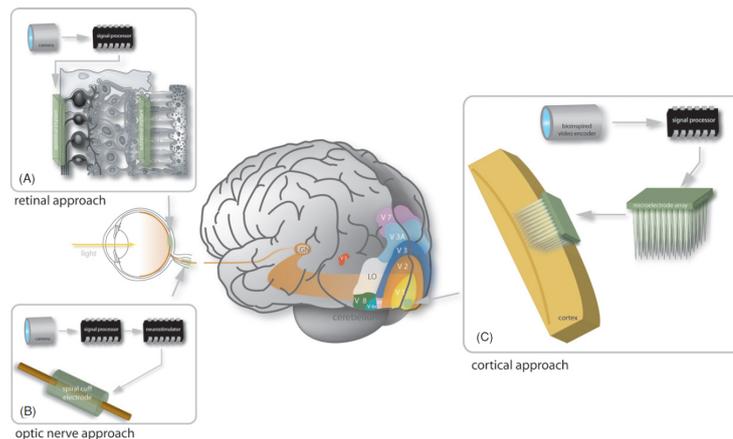


Figure 1.2: Different approaches for vision treatment along visual pathway. Reprinted from [6]. (A) Schematic diagram of a retina cross-section showing the

epiretinal and subretinal method of stimulating ganglion cells. (B) Stimulation of the optic nerve by implanting a spiral cuff electrode around the nerve. (C) Cortical approach: implanted microelectrode array for visual cortex stimulation.

The progressive degeneration of *retinal* photoreceptors is one of the significant causes of adult blindness in humans [7]. Retinitis pigmentosa (RP) and age-related macular degeneration (AMD) are the most common pathologies in retinal degenerative diseases that progressively lead to complete blindness. Epiretinal, subretinal, and suprachoroidal are different retinal stimulation approaches that stimulate remaining retinal neural cells, allowing the visual signal to reach the brain, thus partially restoring the vision. However, the retinal prosthesis can only treat diseases affecting the photoreceptors; if the interruption is beyond the retina, another approach must be chosen.

The *optic nerve* stimulation can be applied in blind patients with surviving retinal ganglion cells and an intact optic nerve. This approach is based on using an implant composed of a series of electrodes positioned all around the optic nerve to generate “points of light,” called phosphenes [8].

Over the years, *cortical prostheses* have aroused increasing interest due to their strong potential in treating visual impairment in patients with late blindness due to diseases or lesions of the retina or optic nerve [8]. Moreover, the large surface area of the visual cortex allows the implants of more electrodes, compared to the other approaches, offering a higher resolution.

1.2 Challenges of Neural Implants

The field of neural stimulation interfaces with the nervous system through implantable units that exploit electrical impulses to generate a neuronal response, modulating its functions.

Traditional neurostimulation with MEAs directly connected to IEU has no negligible limitations. Cables, connectors, and batteries lead to a considerable increase in the risks of implant failure, an increase in dissipated power that causes heat generation with the risk of tissue damage. Moreover, the use of implanted batteries, whether disposable or rechargeable, contributes significantly to the overall weight and dimensions of the implanted unit, as well as the increasing risks due to more complex and invasive surgical procedures [9].

Nowadays, new IMD technologies aim to make neural implants more portable and stable for long-term installations by minimizing their invasiveness and increasing patient comfort and safety.

For these reasons, battery-free implants have become the main target in developing

neural stimulation systems in the last few years. In this context, modern implantable neural prostheses can be used to provide neurostimulation to both the brain and peripheral nerves with high selectivity and low power requirements [10].

Therefore, miniaturization and wireless technology are the keys target for the next generation of neural implants to be able to cover larger areas of the cortex, minimizing the risk of infections and achieving safe surgical implantation and long-term tolerability [11].

1.2.1 Wireless Neural Implants

Wireless technologies result in the key strategy to overcome the limitations related to the dimensions and invasiveness of the implants and to avoid altogether the use of cables and transcutaneous connectors, which are a risk of infections.

For the next generation of neural implants, the main technical challenges are *miniaturization*, *chronic reliability*, hence device longevity and stability, and *scalability*. This means extending the number of recording and stimulation sites, targeting wirelessly powered freestanding electrodes array, no longer relying on IEOs and wired connections [12].

Wireless capability is essential to achieve these goals, but it brings challenges such as wireless power transfer efficiency and data throughput [13].

Wireless technology is essential to deliver enough power and establish robust data communication to implanted devices [14].

Typically, an implantable system comprises two fundamental parts:

- An external module is located outside the body to address power and data wirelessly.
- An internal module is implanted in the target region for stimulation or recording.

In the field of implanted neurostimulators, several methods have been proposed to power these sub-mm and mm-scale neural implants, including acoustic power transfer (APT), capacitive power transfer (CPT), and inductive power transfer (IPT) [15]. IPT is the most used technique in wireless technology for IMDs. This resonance-based method leverages near-field magnetic coupling to address power and data wirelessly [16]. In this context, RF near-field approach is preferred as the RF is less attenuated by the tissues [11], thus leading to greater efficiency.

However, WPT systems must be carefully designed considering the international guidelines provided by the Federal Communications Commission (FCC), and the operating frequency must be chosen according to the ISM radio bands. Thus, for designing a wireless system that uses RF, it is imperative to respect the limits

imposed by the FCC regarding the Specific Absorption Rate (SAR) to prevent permanent damage to the patient's tissue.

1.2.2 Miniaturized Neural Implants

Significant micro-nano technology advances have allowed ever-greater miniaturization of implantable devices to the sub-millimetric scale [17].

MEAs are still the most widely used method for wireless power transfer for neural applications; nevertheless, to reach even more miniaturized dimensions, CMOS is an emerging technology that allows further scalability of systems down to a size of the order of a micrometer. Furthermore, thanks to the small dimensions, it becomes possible to distribute free-floating micro-implants over larger areas of the cerebral cortex and, at the same time, increase the positioning precision on the region of interest, reaching high spatial specificity [17]. Another great advantage of miniaturized implants is the decrease in tissue stress which triggers an immune response that can lead to implant failure.

Therefore, free-floating neural implants applied for visual restoring, in addition to the advantages already mentioned, arouse a strong interest for their great potential to stimulate many more channels, or pixels, in the visual cortex to achieve higher spatial resolution. The new cutting-edge technology offers a unique and innovative approach to neural stimulation by exploiting *miniaturized, free-floating micro-electrodes* respecting the requirements in terms of bio-integration and biocompatibility, wireless technology, and long-term tolerability. These are the goals of the *Neural Dust*.

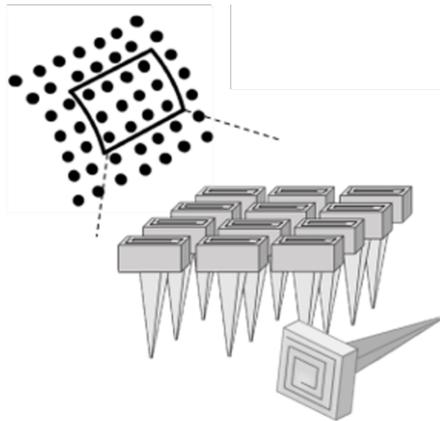


Figure 1.3: CMOS pixels for neural stimulation.

1.3 The Smart Dust concept

In 1999, researchers Joseph Kahn, Randy Katz, and Kristofer Pister from the University of Berkeley, California, introduced the term Smart dust in history for the first time. This new innovative idea aimed to build highly miniaturized structures, hence the term "dust," for sensing, mobile networking, and systems communication [18].

In the last 20 years, the concept of smart dust has developed more and more, finding great applications in biological systems and giving birth to two new challenging and innovative fields: *neural dust* and *body dust*. Body dust aims to develop innovative human body metabolism monitoring technology, introducing the new concept of shrinkable and drinkable electronics that can flow through the human blood.[19, 20]

Neural dust theory, published in 2013, aims to develop a new generation of ultra-miniaturized and wirelessly powered devices freely distributed in the human brain.[21] Although its application for brain monitoring is not yet proven [20], neural dust has great potential for developing the next generation of neural implants for neural stimulation.

1.4 State-of-the-Art: Wireless Miniaturized Neural Implants

Starting from the first work developed from the neural dust approach, this section presents the state-of-the-art the main IMDs wirelessly based for power and data communication toward and from miniaturized neural implanted microelectrodes. The chapter is concluded with a description of the architecture implemented for this project.[22]

1.4.1 Neural Dust

In 2013 researchers at Berkeley University presented the first brain-machine interface (BMI), named Neural Dust, to provide a new solution for chronic BMI systems [21].

The two main technology innovations introduced are using thousands of 10 – 100 μm scales, free-floating, independent sensor nodes (neural dust) to detect local electrophysiological data, and a sub-cranial transceiver to communicate with the "speck of dust" implanted deploying ultrasound (US) coupling link.

Fig.1.4 shows the neural dust system diagram. In addition to the two parts mentioned above, an external transceiver is used to power the sub-dural transceiver via RF power transfer (PT).

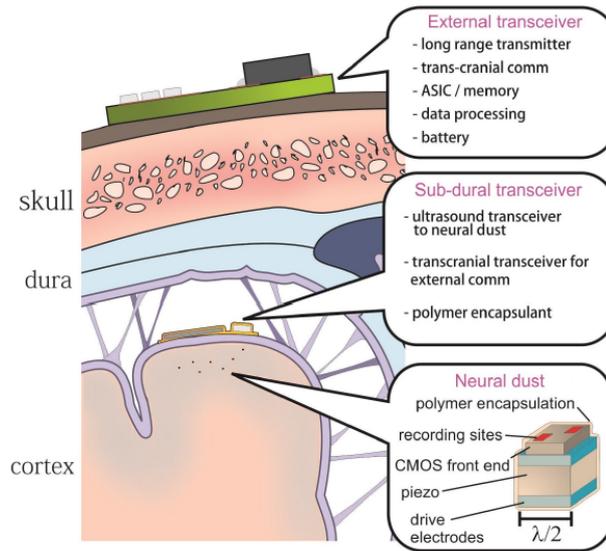


Figure 1.4: Neural dust system. Reprinted from [21].

Furthermore, in 2016 the same research team developed the first in vivo electrophysiological recordings system in the sciatic nerve with the ultrasonic neural dust motes in anesthetized rats [23].

1.4.2 StimDust

StimDust, developed in 2018 at Berkely University, is a wireless neural stimulator based on an ultrasound (US) system for power delivery and bidirectional communication between the external transceiver and the implanted mote. The system is based on an external $0.422mm^3$ electric transducer used for powering and downlinking wireless data communication and finally stimulating the peripheral nerve [24]. The total stimulator size is $6.5 mm^3$ and consists of a piezoceramic transducer, an energy storage capacitor, and a stimulator integrated circuit (IC) [25].

The IC collects the ultrasonic power, decodes the downlink data concerning the time-encoded stimulation parameters, and generates current-controlled stimulation pulses. The carrier frequency is 1.85 MHz and represents a trade-off between the charge storage and US attenuations through the tissue. In fact, higher frequencies lead to more attenuation.

Fig. 1.5 shows the StimDust wireless neural stimulator system diagram and the implanted mote for sciatic nerve stimulation in rats.

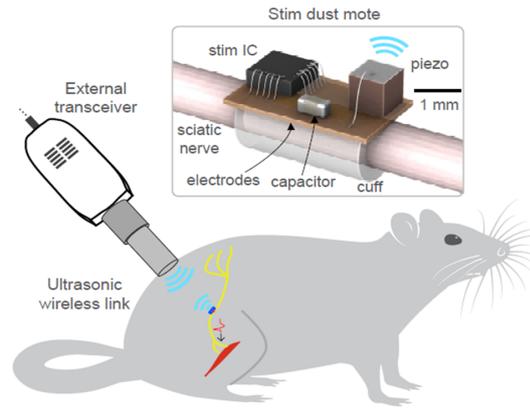


Figure 1.5: StimDust wireless neural stimulator system overview. Reprinted from [25].

1.4.3 ENGINI

The Empowering Next Generation Implantable Neural Interfaces (ENGINI) platform is a 3-coil-based architecture system composed of an external processor, a cranial transponder, and freely-floating mm-scale probes for recording extracellular action potential (EAP). Each probe contains an integrated wireless recording system for managing the power sent by the external module and transmitting previously amplified recorded data.

The carrier frequency used for the wireless power transmission (WPT) is 433 MHz ISM radio band, which represents the optimal trade-off between the maximum amount of power delivered to load (PDL) and the specific absorption rate (SAR) limits. The carrier signal is modulated through a load-shift keying (LSK) modulation technique, and the data communication data rate is 205 kbps.

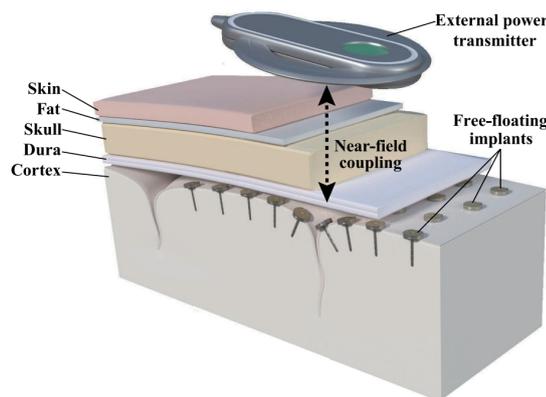


Figure 1.6: ENGINI platform system. Reprinted [15].

1.4.4 Microbead

Microbead is a miniaturized and injectable neural stimulator wirelessly powered using on-chip inductors fabricated in 130-nm CMOS technology [11]. The system's functioning is based on an IPT link and composed of a 2-coils architecture for recording and stimulating the brain.

Each CMOS chip consists of an on-chip printed spiral coil (PSC), an analog signal processing circuitry, and four electrodes for brain cortex stimulation. The operating frequency is 1.18 GHz, and the distance between the transmitter coil and the implanted receiver is 6 mm. The PSC is designed with an octagonal shape and area of $300 \times 300 \mu\text{m}^2$. The microbeads stimulators are implanted into the brain using a syringe with a 22G needle [26]. Fig. 1.7 shows the microbead technology, from an overview of the system to the insertion technique.

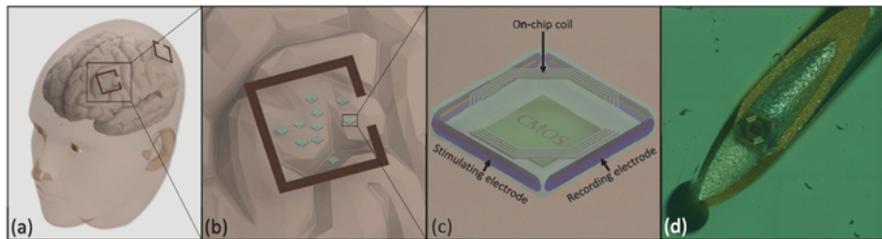


Figure 1.7: Microbead technology. (a) 3D model of the microbeads in the cerebral cortex, (b) view of the transmitting coil (Tx), (c) The packaged microbeads with two stimulating electrodes and two for recording. (d) Micrograph of the microbead, implantable with a 22G needle syringe. Reprinted [26].

1.4.5 Michigan/ETH

A team of researchers formed with members from the University of Michigan and ETH Zurich proposed a wireless neural recording system composed of three major components: an external interrogator, an epidural repeater, and micro-probes. The concept of the system goal is to insert many micro-probes into the sub-dural space for a more extensive neural recording activity, utilizing electromagnetic (EM) and near-infrared (NIR) waves for power and data transmission [17]. Each probe is designed with a $0.74\mu\text{W}$, $0.19 \times 0.17\text{mm}^2$ IC to record neural spikes using a carbon fiber electrode inserted several mm into brain tissue and powered by 850nm NIR light emitted by a repeater placed in the epidural space [27].

1.4.6 Neurograin

Neurograins are wireless microscale neural sensors based on CMOS technology to stimulate and record neural activity via inductive coupling link [28]. Each

neurograin is a $500\ \mu\text{m} \times 500\ \mu\text{m}$ Application Specific Integrated Circuit (ASIC) containing an RF micro-antenna and the associated analog front-end, networking, and backscatter circuits [29]. The system's configuration is based on a 3-coils architecture. In fact, a supplementary subcutaneous resonant co-planar relay coil is added to improve the WPT efficiency [30]. The additional relay PSC coils are positioned 8 mm distant from the transmitting coil, and the operating frequency of the RF power system is 915 MHz. Data telemetry is bi-directional, and the uplink-downlink network operates at 1 GHz. Furthermore, the uplink data transmission rate can achieve 10 Mbps.

Fig. 1.8 shows the transcutaneous RF transmission of power and data via IPT.

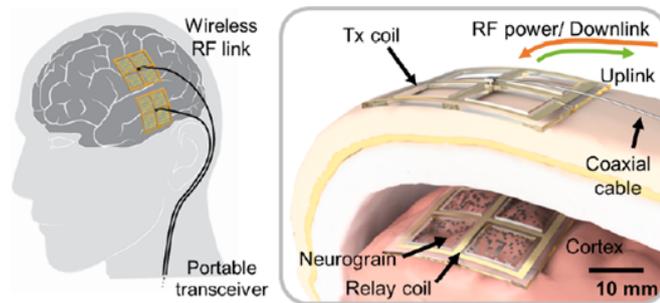


Figure 1.8: Concept of a transcutaneous RF power and data link for a neurograin array. Reprinted from [30].

1.4.7 Comparison

In this chapter, several sub-mm neural IMDs have been presented. Fig. 1.9 illustrates the main miniaturized devices described above.

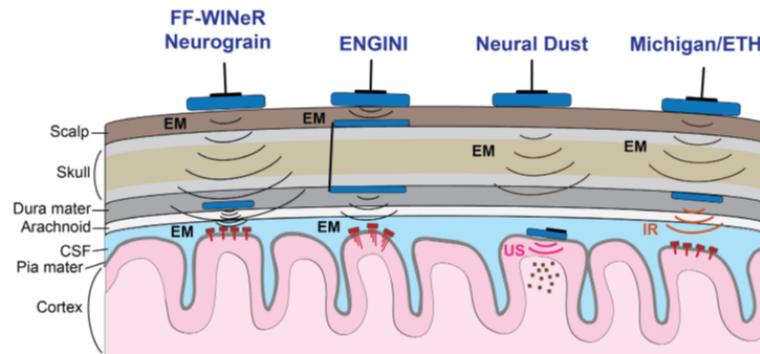


Figure 1.9: Overview of the main sub-mm neural IMDs. Reprinted from [17].

In particular, the figure compares four devices for recording applications based on

two-tier hybrid powering schemes [17].

Table 1.1 summarizes the main characteristics of state-of-the-art millimeter-scale free-floating implantable neural interfaces. The comparison also includes the project in which this thesis is involved, Smart Micro Neural Dust (SMND), for cortical stimulation to revert blindness.

Table 1.1: Comparison of state-of-the-art sub-mm free-floating neural IMDs.

	recording				Stimulation		Both
	Neural Dust	ENGINI	Michigan/ETH	Neurograins	StimDust	Microbead	
General	Neural Implant Volume (mm^3)	2.4	12.56	0.00323	0.00675	6.5	0.009
	IC Area (mm^2)	/	2.1	0.0323	0.25	6.5	0.12
	Size (μm^3)	/	650x650x250	190x170x100	3500x3500x0.55	750x750x750	340x330x80
	Extra components Implanted	Sub-dural Transceiver	Cranial Transponder	Repeater	Relay Coil	Piezocrystal	none
	Number of channels	1	8	1	1	1	1
	CMOS Technology (μm)	/	0.35 AMS AG	0.18 NA	TSMC MS/RF LP	TSMC LPCMOS	0,13 RF
	Power Supply (V)	NA	1.5	1.5	0.6	2.5	1
	Total Power Consumption (mW)	0.12	0.092	0.00074	0.04	0.035	NA
	Number of Chip	NA	10-100	NA	1000	1	10
	Testing	<i>in vivo</i>	/	<i>in vivo</i>	<i>in vivo, ex vivo</i>	<i>in vivo, in vitro</i>	<i>in vivo</i>
Powering	Scheme	EM/US	EM	EM/IR	EM	US	EM
	Frequency (Hz)	1.85M	433M	NA	915M	1.85	1,18G
	Number of Coils	/	3	/	3	/	2
	Rx Coil Size (mm^2)	0.56	12.25	0.01615	0.25	/	0.09
Communication	Distance (mm)	8.8	8	NA	12	21.5	4.6
	Modulation Down-/Up- link	NA	-/LSK	PWM/SIM	ASK-PWM /BPSK	NA	FDMA
Recording	Data Rate (bps)	-/0.5M	-/205k	NA	1M/10M	NA	NA
	Input Noise (μV)	180	1.8	4.8	2.2	/	NA
	ADC Resolution	8	12	NA	8	/	NA
Stimulation	Max Current (μA)	/	/	/	/	400	46

1.5 Smart Micro Neural Dust Project

Smart Micro Neural Dust (SMND) is an innovative wireless CMOS-based cortical neuroprosthesis to revert blindness by stimulating the visual cortex through penetrating and intracortical microelectrodes.

The wireless device consists of an array of thousands of freestanding, ultra-small, and individually addressable CMOS pixels of size $250 \times 250 \times 75 \mu m^3$. Each CMOS pixel is an active element composed of three units: a receiving, a conditioning, and a stimulating unit; in this way, each SMND can receive the signal sent wirelessly from an external transmitter and convert it into an electrical pulse to stimulate the visual cortex. The RF transmitter generates an ASK modulated signal at the frequency of 433,92 MHz for sending power and data simultaneously to the implanted CMOS microelectrodes via an inductive link. The inductive transmission is based on a 3-coil architecture to achieve higher PTE and PDL with respect to 2- and 4-coil link [31].

This project aims to develop ultra-miniaturized CMOS microelectrodes, exploiting the smart neural dust approach, to stimulate the primary visual cortex to restore vision wirelessly by inducing phosphene perception.

For this purpose, the entire process flow consists of four main parts, from image processing to the stimulation of the visual cortex through implanted microelectrodes. Referring to Fig. 1.10, the system is composed as follows:

1. **Webcam and Image processing:** consists of a edge detection segmentation algorithm that processes the images captured in real-time by an external webcam;
2. **RF SWIPT Base station:** transmitter device to generate an RF signal modulated accordingly to the digital data coming from the image processing for simultaneous power and data transfer;
3. **3-coils inductive link:** an inductive-based link consisting of a transmitter coil connected to the base station, an implanted resonator to increase PT efficiency, and a receiving coil placed on the CMOS neurostimulator to address power and data;
4. **CMOS implants:** miniaturized implanted CMOS microelectrodes to stimulate the visual cortex for inducing phosphene perception;

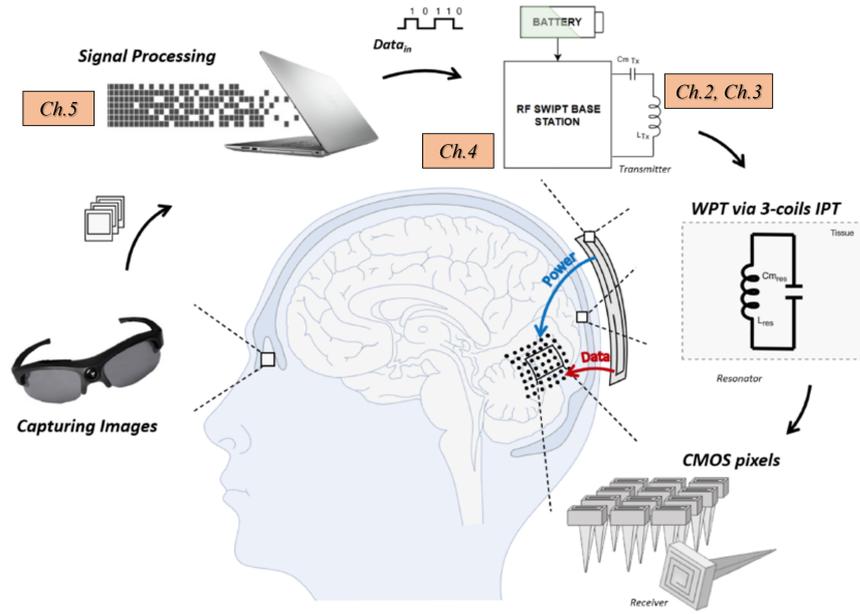


Figure 1.10: Overview of the system: Smart neural dust to revert blindness. The corresponding chapters of this thesis are indicated.

1.5.1 Outline of The Master Thesis

The aim of this masters' thesis is to design and develop the External Processing Unit (EPU) to simultaneously transfer power and data wirelessly using an inductive link.

For this purpose, the thesis focused on:

- i) optimizing the transmitter coil for both power and data inductive transfer;
- ii) designing and manufacturing the RF base station to generate the modulated RF signal through the ASK modulation technique;
- iii) designing the real-time processing system starting from a webcam-based video capturing unit;
- iv) packaging of the entire EPU to realise a dedicated and portable device;

More in detail, the remaining chapters of this thesis are organized as follows.

In *chapter 2*, the theoretical principles of wireless power transfer and data communication will be explained. Also, the different impedance matching network architectures will be described. *Chapter 3* will show the final transmitter coils designed and manufactured. The results will be presented. *Chapter 4* will present the new design and layout of the RF Base station PCB, concluding with the results

of the manufactured device. *Chapter 5* will describe how the image processing algorithm works for sending real-time digital data to the PCB. Aiming to realize a single portable device, in *chapter 6*, the case realized for the EPU will be presented. *Chapter 7*, concludes the thesis, and the proposals for future developments for this project will be presented.

Chapter 2

Inductive link and Matching Networks

The most challenging aspect of the inductive power transmission (IPT) is to be able to transfer sufficient power to the load (PDL) besides preserving high power transfer efficiency (PTE).

Thus, to optimize the maximum power transfer to the implanted receivers, the first step is to guarantee the maximum power delivery from the RF source to the transmitter coil minimizing the losses. Sensitivity to noise, electromagnetic interference (EMI), and reflections play the majority roles in designing a system based on radiofrequency. In fact, further precautions must be considered to achieve the desired performance in terms of power transfer.

Since the transmitting system of this project is designed to simultaneously transfer data and power, it is necessary to ensure sufficient bandwidth to correctly demodulate the information signal sent from the RF Base station.

For this purpose, an *impedance matching network* (IMN) has been designed by focusing on the *optimization* of both *power* and *data* transfer.

In this chapter, the procedure followed to design the IMN for optimizing power and data transfer will be explained starting from the theoretical basis of impedance matching and wireless data communication.

In the next chapter (Ch.3), the manufactured transmitter coils with the implemented matching circuit will be presented together with the results obtained in terms of S11 and S21.

2.1 Inductive Power Transfer

Inductive power transfer (IPT) is a resonance-based approach that leverages magnetic coupling for power delivery and data communication. IPT is the most widely used WPT method to power implantable microelectronic devices (IMDs)[31] since it exploits the RF in the near-field region, which is less attenuated by the human tissues.

The operating principle of an inductive system consists of at least two coils, transmitter and receiver, in close proximity so that they are magnetically coupled. This concept is illustrated in Fig. 2.1: the power is transferred from the transmitting coil (Tx) to the receiving coil (Rx) through an induced magnetic field [32].

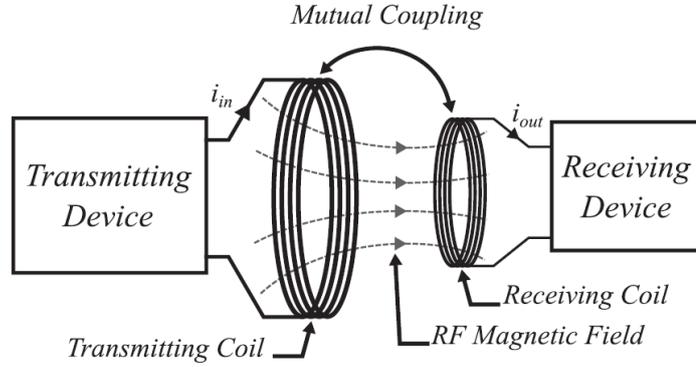


Figure 2.1: Conceptual overview of IPT system. Reprinted from [32].

This system can be considered as a pair of inductors L_1 and L_2 , coupled with a mutual inductance M which is related to the distance between the center of the coils according to an inverse cubic proportionality (d^{-3}) [31]. The relation that binds the mutual inductance (M_{ij}), the values of the inductances (L_i, L_j), and the coupling factor (k_{ij}) is explained in Eq.2.1

$$k_{ij} = \frac{M_{ij}}{\sqrt{L_i L_j}} \quad (2.1)$$

For the best power transfer efficiency, all the LC tanks must resonate at the same frequency $f_{res} = \frac{1}{2\pi\sqrt{LC}}$. This frequency can be modified by adding a proper impedance matching network to tune all the coils to the same resonant frequency and, thus, optimize the coupling (Fig. 2.2).

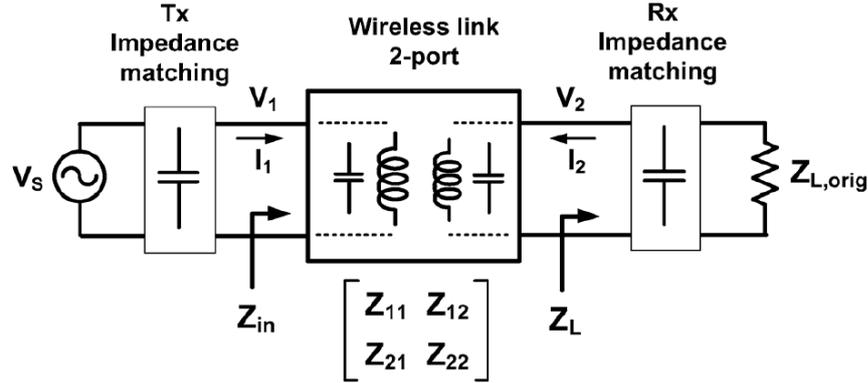


Figure 2.2: General model of two-port wireless power link. Reprinted from [33].

Referring to Fig. 2.2, the transmitting coil (Tx) is located outside the body, and the power supply comes from an external power source, such as a battery. Z-parameters represent the environmental effect of the parasitic capacitances, surrounding air, and tissue media between the transmitter and receiver coil (Rx) implanted inside the body [33]. Tx and Rx impedance matching circuits are placed to maximize PTE and PDL for the best performance of the inductive link.

The essential requirements in inductive power transfer systems are to deliver sufficient power to the load together with high power transfer efficiency avoiding heat dissipation in the tissues. PDL and PTE are affected by many parameters such as coil geometry, distance, alignment, and inductive link architecture. The latter can be based on a 2-, 3-, or 4-coils configuration. Fig. 2.3 show a comparison between the 3-coil and 4-coil inductive links. From the graph, it can be seen that with a *3-coil configuration* it is possible to achieve high PTE and high PDL at the same time.

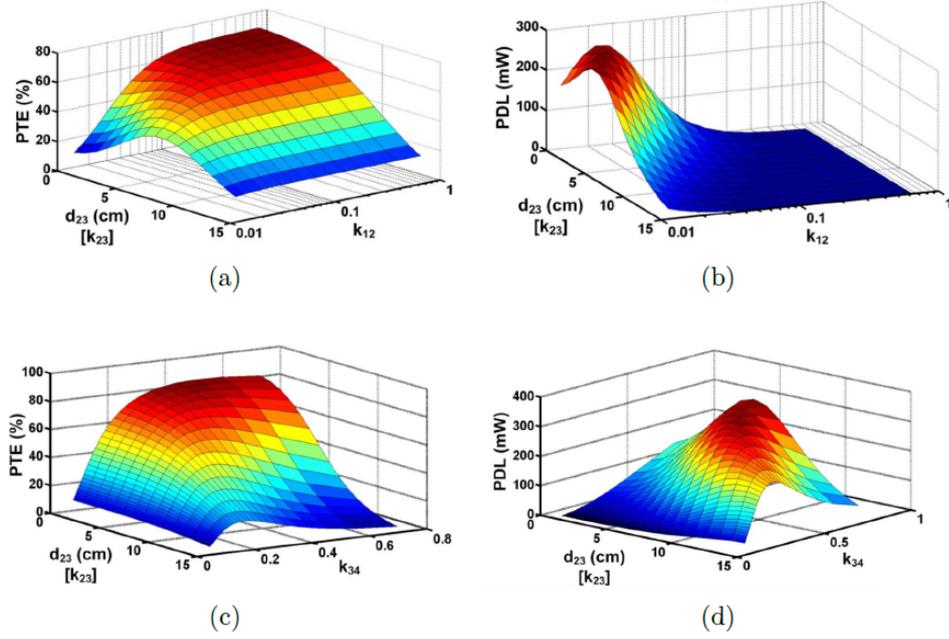


Figure 2.3: Comparison of PTE and PDL as a function of distance d_{ij} and coupling coefficient k_{ij} in 3-coil and 4-coil IPT. (a) PTE_{4-coil} and (b) PDL_{4-coil} IPT; (c) PTE_{3-coil} and (d) PDL_{3-coil} IPT. Reprinted from [31].

The 3-coil configuration uses an additional *resonator* at the Rx plane. With the miniaturization of the receiving systems, a high-quality factor resonator results in a better distribution of the magnetic field in the interior area of the resonator leading to a significant increase in PTE [34].

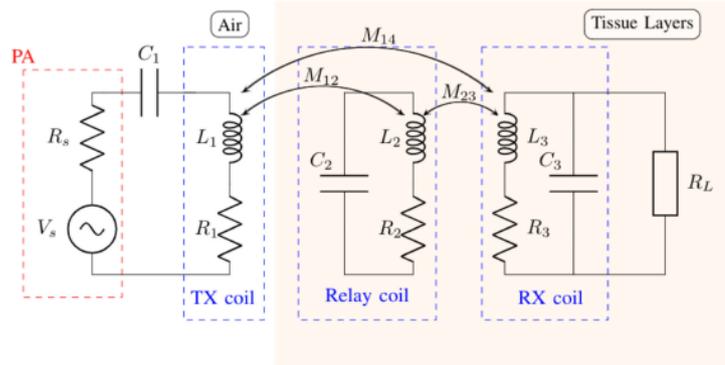


Figure 2.4: 3-coil inductive link. Reprinted from [11].

Fig. 2.4 shows the 3-coil configuration circuit schematic. When the coils resonate to

the same operating frequency, the nearby relay coil (L_2) increases the magnetic field generated by L_1 , thus increasing the coupling coefficient between the coils. This leads to a significant increase in PTE concerning the two coil architecture. In particular, the efficiency of the 3-coil configuration is illustrated in Eq. 2.2

$$\eta_{3-coil}(\omega) = \frac{\kappa_{12}^2 Q_1 Q_2}{1 + \kappa_{12}^2 Q_1 Q_2 + \kappa_{23}^2 Q_2 Q_{3L}} \cdot \frac{\kappa_{23}^2 Q_2 Q_{3L}}{1 + \kappa_{23}^2 Q_2 Q_{3L}} \cdot \frac{Q_{3L}}{Q_L} \quad (2.2)$$

Where Q_{iL} are the load quality factors, Q_i are the quality factors of the coils.

As the last point, the ultimate goal of the IPT for IMDs is to reach the highest possible power transfer efficiency (PTE) without violating the *Specific Adsorption Rate* (SAR), that for the human head is set to 1.6 W/Kg for 1g of tissue mass measured during 6 minutes of exposure [11].

For this project, the WPT via IPT with a 3-coils configuration is used since it shows the best performance in PTE, tolerance to misalignment, and SAR-constrained PDL [33].

2.2 Theory of Wireless Power Transfer Optimization

In electronic circuits, the maximum power transfer theorem, published by Moritz Von Jacobi in 1840, states that to obtain the maximum output power from a generator with its internal impedance, the load impedance must be equal to the equivalent output impedance of the source [35].

2.2.1 Importance of Impedance Matching in RF Design

Circuits for radiofrequency applications are composed of a generator (*RF source*), and a load (an *antenna*) that transmits the generated RF signal.

For any efficient RF circuit, it is necessary to maximize the power transfer between the source and the load by minimizing the losses and internal reflections [36].

When the output of the RF transmitter is connected through a cable to a load, in this case, a coil, it must be considered that the cable acts as a transmission line if the following condition is verified:

$$L_{cable} > \frac{\lambda}{8} \quad (2.3)$$

Where L_{cable} is the length of the cable, and λ is the wavelength of the operating frequency. This means that to achieve the maximum power transfer, the presence of the cable must be considered as a part of the circuit to be matched (Fig. 2.5).

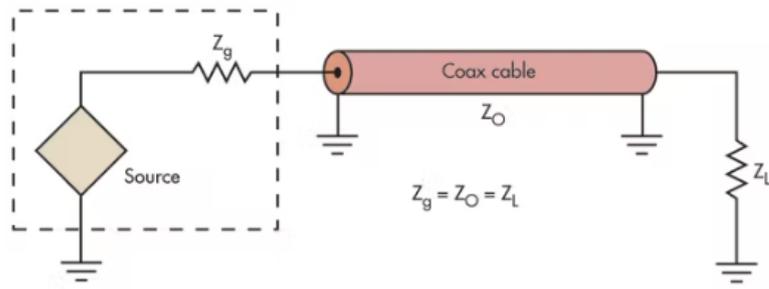


Figure 2.5: Transmission lines with a characteristic impedance (Z_0).

For power transfer based on time-varying signals, such as radio frequencies, it is important to consider that both RF source and load impedance values are complex numbers. The imaginary part of the impedance, the reactance, adds a delay in the current waveform with respect to the voltage one, making them out of phase (Fig. 2.6).

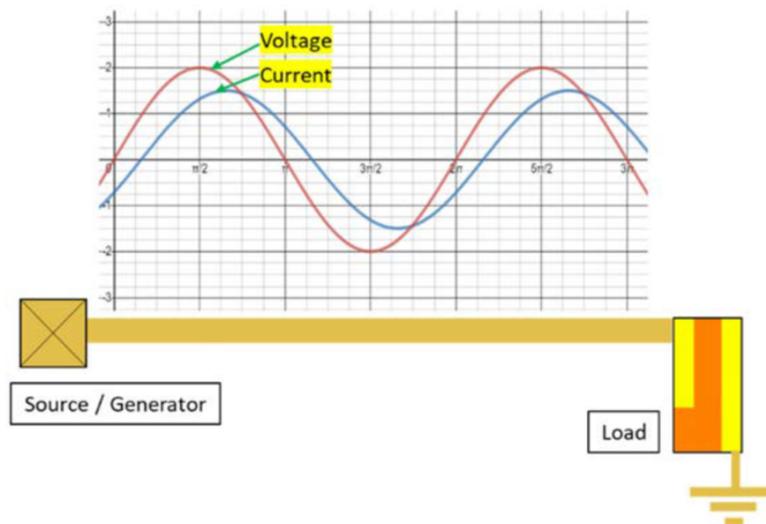


Figure 2.6: Voltage and current waveforms for complex impedance. Reprinted from [36]

This leads to the generations of reflections between the source and the load. The reflected signal is added to incident one resulting in a standing wave measured by the *voltage standing wave ratio* parameter (VSWR).

In a transmission line, the VSWR is defined as the ratio between the maximum and the minimum amplitude voltage of a standing wave along the line and represents the goodness of the impedance matching. VSWR parameter is defined by the

following formula.

$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|} \quad (2.4)$$

Where the parameter Γ is the *reflection coefficient*, which describes the power reflected from the load back to the source.

To have maximum power transfer, which means a perfect impedance match ($Z_L = Z_O$), a minimum reflection coefficient is desired, ideally zero as described in the following formula [36].

$$\Gamma = \frac{Z_L - Z_O}{Z_L + Z_O} \quad (2.5)$$

2.2.2 Scattering Parameters

The reflection coefficient is also known as return loss or S11. The latter is part of the *S-parameters*, or *scattering parameters*, that describe the input/output relation between two ports in a communication system [37].

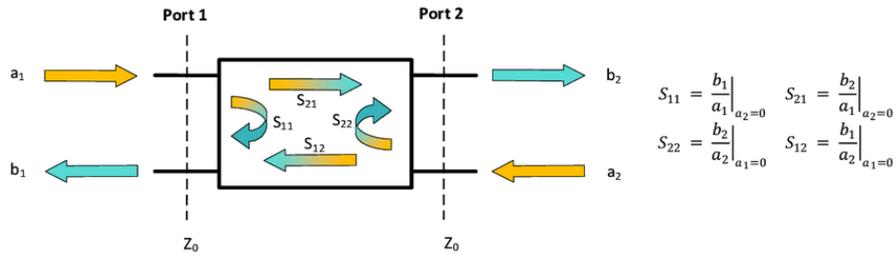


Figure 2.7: S-parameter representation of a two-port network. Reprinted from [38].

As shown in Fig 2.7, considering a two-ports system, we obtain four S-parameters:

- S11: represents the reflected power that is reflected back to port 1;
- S12: represents the power transferred from port 2 to port 1;
- S21: represents the power transferred from port 1 to port 2;
- S22: represents the reflected power that is reflected back to port 2;

Therefore, the final goal to guarantee the maximum power transfer between the RF transmitter and the transmitter coil Tx is to minimize the return loss at the working frequency of the system, which is 433.92 MHz. For this purpose, S11 was used as a reference parameter in the optimization strategy of the impedance matching network.

2.3 Theory of Wireless Data Transfer Optimization

Since the transmitting system of this project is designed to transfer data as well as power simultaneously, it is necessary to ensure sufficient bandwidth to correctly demodulate the information signal sent from the RF Base station.

2.3.1 Theory of Digital Data Communication

In a digital communication system, to ensure correct data transmission, it is essential that the digital information signal can be clearly reconstructed on the receiver side.

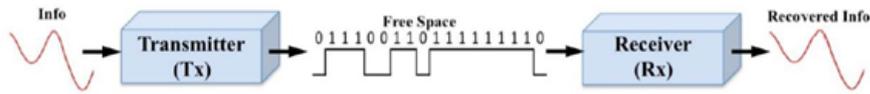


Figure 2.8: Concept of digital data communication.

Thus, when designing an inductive communication system, it is necessary to consider the *bandwidth (BW) requirements* to be able to recover the digital signal and therefore be able to demodulate the data correctly.

2.3.2 Bandwidth and Fourier Analysis

A digital signal, in the time domain, is a square wave with a certain frequency f_0 . To design a communication system ensuring the minimum bandwidth required concerning a given data rate, it is necessary to consider the frequency content of the digital signal, thus passing in the *Fourier domain*.

Fourier's theorem states that any continuous periodic function can be represented as a linear combination of sinusoidal functions with appropriate amplitudes and frequencies multiple of the frequency of the original one [39]. The sinusoid with the same frequency f_0 of the primary function is called *fundamental*, while the sinusoids with a frequency multiple to the fundamental f_n are called *harmonics* [40].

Therefore, a periodic signal $f(t)$ of period T can be expressed as a series defined by Eq. 2.6.

$$f(t) = A_0 + \sum_{n=1}^{\infty} [A_n \cdot \sin(n\omega t) \cos(\phi_n) + A_n \cdot \cos(n\omega t) \sin(\phi_n)] \quad (2.6)$$

This is the Fourier series of a periodic signal, and A_0 represents the amplitude of the fundamental and corresponds to the mean value of the original function $f(t)$;

A_n and ϕ_n represent the amplitude and the phase of the subsequent harmonics respectively.

Considering the case of a square wave with a duty cycle of 50%, the *Fourier transform of a square wave* is defined as follows.

$$f(t) = \frac{4}{\pi} \cdot \sum_{n_{odd}=1}^{\infty} \frac{1}{n} \cdot \sin\left(\frac{2\pi nt}{T}\right) \quad (2.7)$$

From equation 2.7, it can be noticed that the terms of the series are infinite, and the harmonic components have progressively decreased amplitudes by increasing the frequencies due to the $\frac{1}{n}$ factor, as also displayed in Fig 2.9.

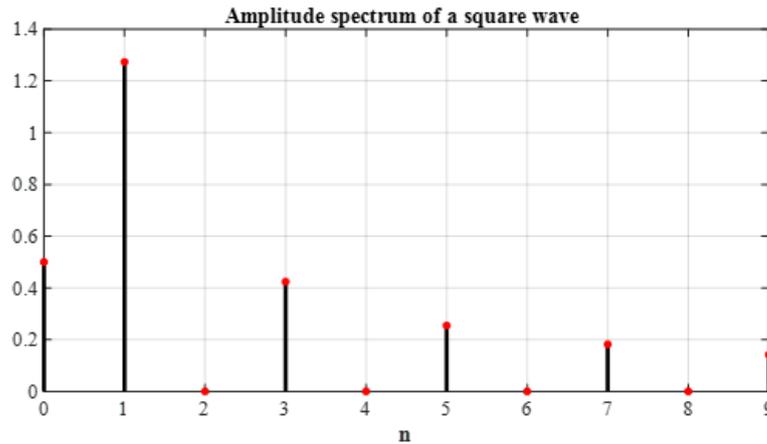


Figure 2.9: Amplitude spectrum of a square wave.

Therefore, the reconstructed signal will represent an approximation of the original signal. The greater the number of harmonics considered, the greater the precision with which the signal will be reconstructed. For example, the figure below (Fig. 2.10) shows the reconstructed square wave until the 9th harmonic.

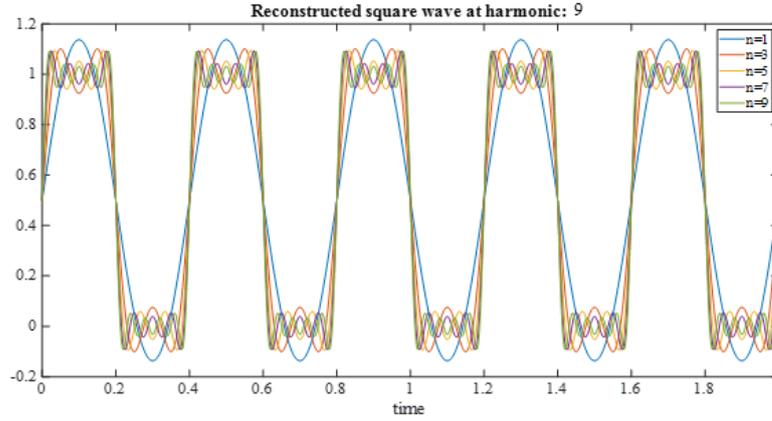


Figure 2.10: Reconstructed square wave until 9th harmonic.

The *bandwidth*, defined as the frequency range within which the transmitting signal is sent, depends on the *number of harmonics* included and the information signal's *data rate* (DR). The relation that links these three parameters is the following:

$$BW = 2 \cdot \left(n \cdot \frac{DR}{2} \right) \quad (2.8)$$

That is to say that the BW must be at least equal to twice the fundamental frequency (f_0) of the original signal, according to the Shannon sampling theorem [41], and multiplied by the last desired harmonic number. Remembering that $DR = 2 \cdot f_0$.

The choice of the number of harmonics to consider depends on the compromise between the goodness of the approximation to be obtained, and the maximum bandwidth allowed by the system requirements. From literature, as a rule of thumb, adding the first five odd harmonics is a close approximation of a square wave [42].

The *cumulative sum* as a function of the number of harmonics was plotted to examine the power contribution added by each harmonic. From Fig. 2.11 after the 5th or 7th harmonics, it can be considered indeed negligible.

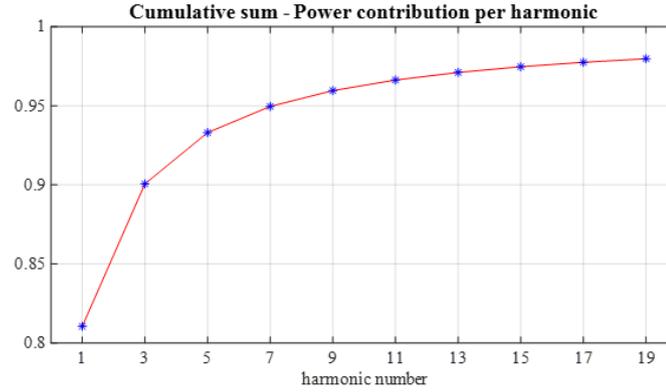


Figure 2.11: Cumulative sum: power contribution per harmonic.

2.4 Impedance Matching Network Architectures

As described in section 2.2, to obtain the maximum power transfer from a source to a load, avoiding internal reflections due to impedance mismatches, the load's impedance must be equal to the source's internal impedance [43].

In addition, in the design of an inductive link, all the LC tanks (external and internal) must resonate at the same frequency to optimize the magnetic coupling. This means that the matching circuit must be carefully designed to minimize the return loss (S11) at the specific working frequency of the system.

In the following paragraphs, the different architectures of the IMNs will be described, and the calculation procedures explained. Ch.3 will present the implementations and the experimental results.

Impedance matching is designing and implementing an additional circuit between the RF source and the load to make their impedances the *complex conjugate* of each other [44]. This means that the real part of the impedances must be equal, and the imaginary part must be the opposite of the other.

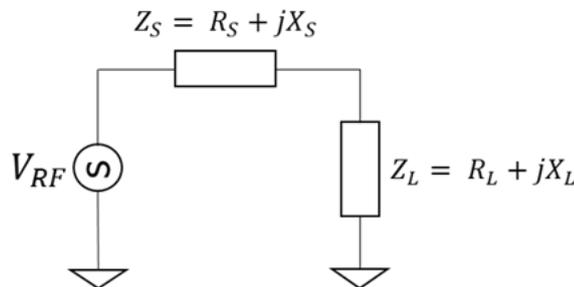


Figure 2.12: General circuit schematic of RF source and load.

Referring to the general circuit schematic shown in the Fig 2.12, the final goal of the IMN is to obtain:

$$Z_S = R_S + jX_S = R_L - jX_L = Z_L \quad (2.9)$$

From the relation written above, it can be seen to achieve a perfect match between the source and the load, the value of load reactance must be equal to and opposite to the value of source reactance. Since the reactance is *frequency-dependent*, the perfect match will occur at one particular frequency. This is very important to ensure that the maximum power transmission occurs at the working frequency of the system.

Furthermore, the matching network is designed to ensure impedance matching as well as sufficient bandwidth for the application [45].

The frequency band and the operating frequency are linked by the *quality factor* Q, according to the relation:

$$BW = \frac{f_0}{Q} \quad (2.10)$$

The quality factor of a network is a dimensionless parameter that indicates the “goodness” of the performance of an RF resonant circuit. A high value of Q means a narrower BW, often preferred in many applications [46]. The correct choice of the IMN architecture is therefore essential to obtain the quality factor desired and consequently determine the frequency band over which the impedance is matched. Different possible *architectures* can be implemented to achieve the considered system’s requirements: *two-element* and *three-element* networks [36].

2.4.1 Two-Element IMN

The *two-element* matching network is also known as *L-type* due to its orientation and shape, as shown in the general sketch 2.13. The advantages of this configuration are the simplicity of the design and the few losses.

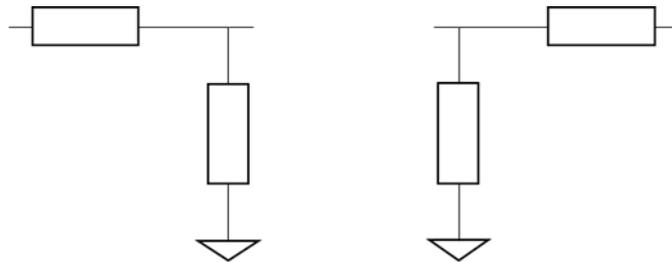


Figure 2.13: L-type IMN.

As shown in the figure above, the L-shaped matching circuits can be divided into two sub-groups: *Parallel-Series* or *Series-Parallel* networks whose components,

capacitors, and inductors, are selected to match the impedance of the load. The function of the parallel component is to transform a certain impedance value into a lower one, thus equalizing the impedance between source and load. Similarly, the role of the series component is to compensate the reactive part of the element that is to be matched by resonating with an equal and opposite reactance. Combining these two components will equalize the equivalent impedance of the load and the source, obtaining the maximum power transfer as a final result. Fig. 2.14 shows the eight possible combinations for designing an L-type matching network.

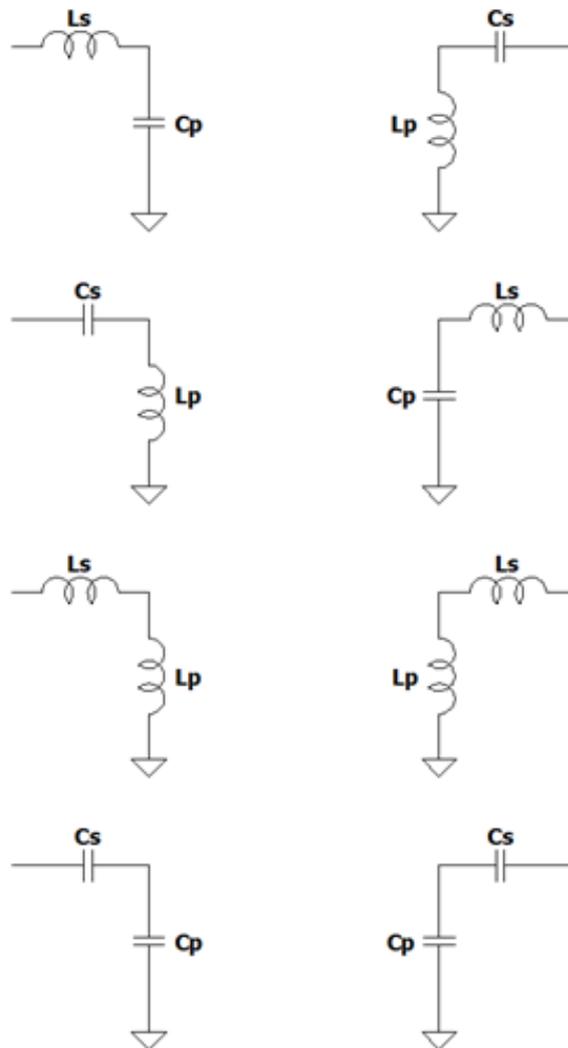


Figure 2.14: L-type IMN: circuit combinations.

To decide the positioning of the parallel component on the left or the right side of

the series component, it is necessary to know the biggest resistance between the source and the load. If the load impedance is higher than the source, then the parallel component must be positioned on the right side of the series component, assuming the load is on the right and the source is on the left in the circuit. The configurations where the two elements are of the same type, ($L - L$ or $C - C$), are used when the load has low resistance and low reactance at the same time. The limitation of the two-element network is that there is no control over the value of the quality factor, which is determined by the values of the series and parallel matching components.

Design procedure

Considering a network composed by the $C-C$ configuration and a source with a purely resistive behavior, Fig. 2.15 shows the resulting circuit. L_{coil} and R_{coil} are the *self-inductance* and the *parasitic resistance* of the coil; C_s and C_p are the added *series* and the *parallel* capacitors for the impedance matching, respectively.

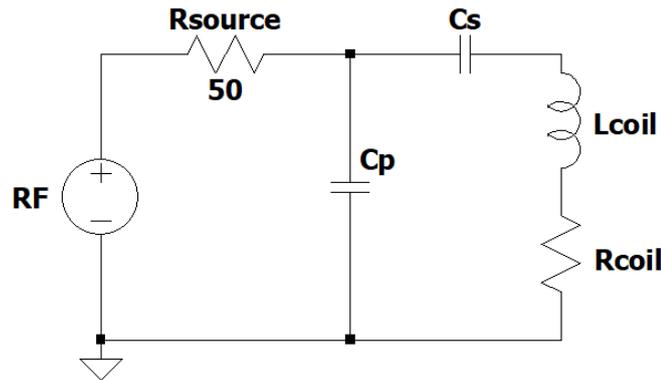


Figure 2.15: Model circuit of CC-L-type network.

The procedure for calculating the values of the series and parallel capacitor of the matching network is the following:

1. Q calculation: $Q = \sqrt{\frac{R_{source}}{R_{load}} - 1}$
2. Calculate the *series reactance*: $X_S = Q \cdot R_{load}$
3. Calculate the *equivalent reactance*: $X_{C_s} = X_S - |X_{load}|$
4. Calculate the *parallel reactance*: $X_{C_p} = \frac{R_{source}}{Q}$
5. C_s and C_p calculation: $C_s = \left| \frac{1}{2\pi f X_{C_s}} \right|$; $C_p = \left| \frac{1}{2\pi f X_{C_p}} \right|$

2.4.2 Three-Element IMN

The *three-element* matching networks are composed of three components, always chosen between inductors and capacitors, providing the great advantage of having the possibility to design the matching circuit by selecting the desired value of the quality factor of the network.

There are two possible architectures: *Pi-type* and *T-type* IMN. Fig. 2.16 shows the general schematic of these networks. Like the L-network, the Pi-type and T-type circuits also owe their names to the shape of the circuit.

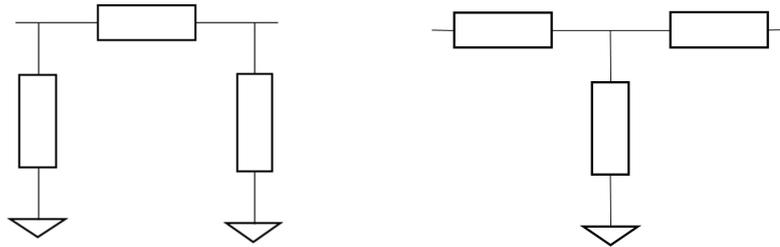


Figure 2.16: Pi-type and T-type IMN.

Both circuits are composed by connecting two L-shape networks: back-to-back for the Pi-shape and vertically mirrored for the T-shape.

Design procedure

Fig. 2.17 shows the model of the circuit used for the calculation of the parameters.

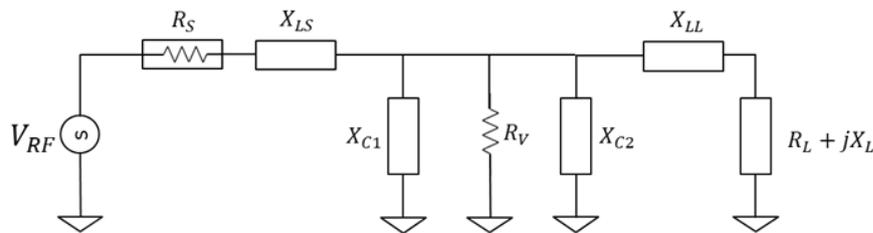


Figure 2.17: T-type model circuit.

To determine the values of the components of the circuit, one additional *virtual resistance* (R_v) is considered between the right (load side) and left part (source side) of the network. The function of the virtual resistor R_v , positioned in parallel in the network, is to raise or lower the equivalent impedance of the circuit to obtain the impedance matching.

The value of R_v is determined starting from the quality factor Q of the circuit,

chosen a priori based on the design requirements. The relation between the quality factor and the virtual resistance is:

$$Q = \sqrt{\frac{R_V}{R_L} - 1} \quad (2.11)$$

Once the value of R_v has been determined, all the other network components can be calculated, finally designing the IMN with the required specifications. Therefore, the value of Q is a crucial parameter that must be chosen carefully, considering the trade-off with the bandwidth over which the impedance remains matched.

Referring to Fig. 2.17, table 2.1 summarizes the circuit parameters to design the matching network.

Circuit parameters
Reactance X_{LS} and X_{LL}
Reactance X_C
R_L
R_S
Frequency
Q

Table 2.1: Circuit parameters for the design of the IMN.

Starting from the load side of the circuit 2.17, the procedure used is the following:

1. Q choice;
2. Calculate the *series reactance*: $X_S = Q \cdot R_L$
3. Calculate the *equivalent reactance*: $X_{LL} = X_S - |X_L|$
4. Calculate the *parallel virtual resistance*: $Q = \sqrt{\frac{R_V}{R_L} - 1} \rightarrow R_V = R_L \cdot (Q^2 + 1)$
5. Calculate the *parallel reactance*: $X_{C2} = \frac{R_V}{Q}$

Moving on to dimension of the source side of the circuit[47, 44]:

1. Find the loaded Q of the parallel circuit: $Q_{source} = \sqrt{\frac{R_V}{R_S} - 1}$
2. Calculate the *parallel reactance*: $X_{C1} = \frac{R_V}{Q_{source}}$
3. Calculate the *equivalent reactance*: $X_{LS} = Q_{source} \cdot R_S$
4. Calculation of the values of the inductors LS , LL and the parallel capacitor C

Chapter 3

Transmitter Coil Fabrication and Experimental Results

Considering the design procedures explained in the previous chapter, this chapter will present the results obtained. In particular, a first implementation was made using a T-type architecture and then verified through LTspice software. Finally, the results and the Ansys HFSS simulations related to the final implementation, L-type, chosen for the new transmitter coils will be shown.

3.1 IMN Design and Implementation

Figure 3.1 shows the general scheme of the system regarding this project. The source is the RF base station PCB, designed to have an output impedance equal to 50Ω , and the load is a single-turn transmitter coil for inductively transferring power and data.

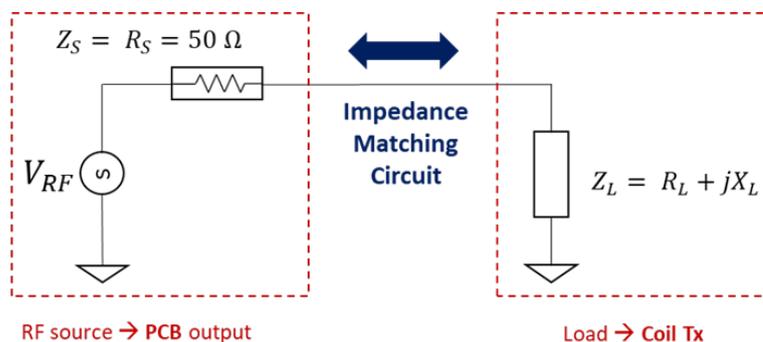


Figure 3.1: General scheme of the system of this project.

Hence, the IMN has been designed with the following objectives:

- Match the load resistance (R_L) with the source impedance of 50Ω ;
- Cancel the reactive components to obtain $jX_{match} = -jX_L$;

T-type Implementation

To verify the design procedure of the impedance matching circuit, a first test was made on the *Würth Elektronik* coils by designing a circuit that matches the impedance on 50Ω at the frequency of 13.56 MHz. This frequency was chosen according to the geometric characteristics of the coil. To obtain the best optimization in terms of power transmission, a T-type matching network was designed to select a high-quality factor.

According to the equations explained in section 2.4.2, and the reference circuit presented in Fig. 2.17 the values of the components of the network were calculated considering the the coil's inductance equal to $L_{coil} = 2.5 \mu H$ [48] with a Q previously selected equal to 25. Table 3.1 and Fig. 3.2 present the results obtained.

Results	Values
L_L	343.3 nH
L_S	6.54 μH
C	67.78 pF

Table 3.1: Calculated values of the components of the T-type IMN.

To verify the performance of the matching, the final circuit was simulated using *LTspice software*.

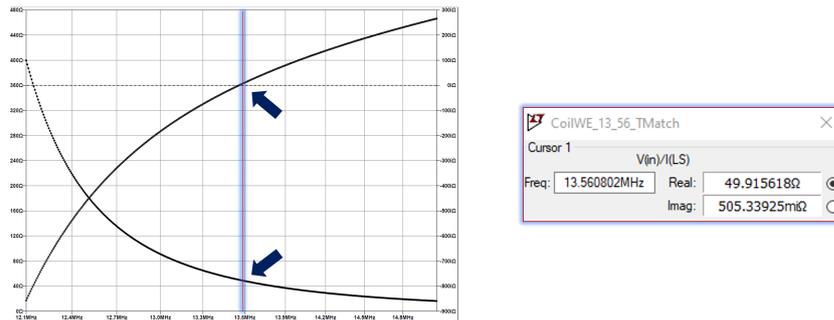


Figure 3.2: Results after the impedance matching. *left:* plot of the real and imaginary part of the matched coil impedance; *right:* resulting values ($Re_L = 49.92 \Omega$ and $Im_L = 0.5 \Omega$).

Fig. 3.3 shows the reflected power $S11$ and the transferred power $S21$ of the network. The peaks are correctly tuned at the working frequency selected, 13.56 MHz; hence, the correctness and effectiveness of the IMN are validated.

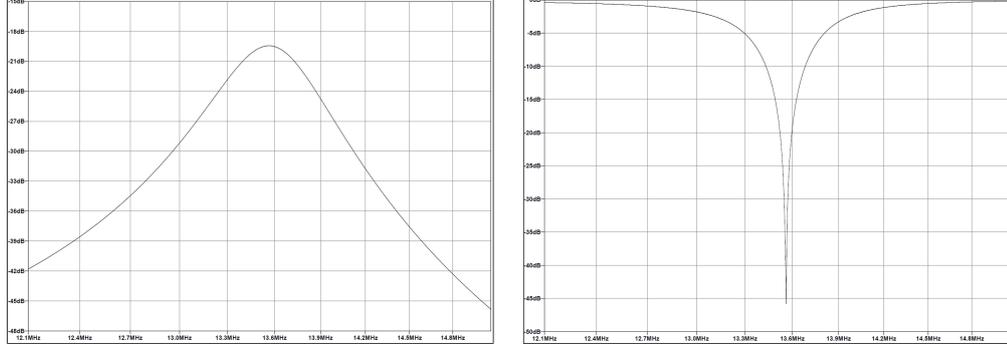


Figure 3.3: S_{21} and S_{11} parameters of the matched circuit.

The next step has been to apply the same concepts to design the matching circuit for the transmitter coil to be integrated into the RF transmitting system of this project.

L-type Implementation

Once the design procedure was validated, the final step was to design the IMN to optimize the RF transmitter coils to simultaneously send power and data to the implanted receivers through an inductive coupling link at the working frequency of 433.92 MHz .

Aiming to transmit both data and power, it is necessary to consider the minimum bandwidth needed for sending and receiving the information signal correctly for brain stimulation. This limits the maximum acceptable quality factor of the matching circuit, as already explained in section 2.3.2.

Considering a maximum data rate of 10 Mbps, to reconstruct at least the first 3 harmonics of the digital signal, a minimum BW of 30 MHz is needed. This means that Q cannot be greater than 14. Considering instead of keeping the first 7 harmonics, Q cannot exceed 6. Therefore, to accomplish the BW specification, selecting a high Q is not needed. For this reason, the final implementation selected is the *L-type matching network*.

Two considerations were taken into account to design the most suitable matching network for this application:

- the values of impedance and conductance of the coils remain low due to the size and geometry;
- a negative series reactance is required to compensate for the positive one of the coil, considering the inductive behavior of the coils;

Therefore, the configuration selected was the *CC-L-type* network and the reference circuit is shown in Fig. 2.15.

Before proceeding with the computation of the IMN as explained in section 2.4.1, the range of values of the *self-inductance* and the *parasitic series resistance* of the coils were calculated in function of the geometries selected to be fabricated. From [11], the self-inductance L is calculated according to equation 3.1.

$$L = \frac{c_1 \mu n^2 d_{avg}}{2} \cdot \left[\ln \left(\frac{c_2}{\varphi} \right) + c_3 \varphi + c_4 \varphi^2 \right] \quad (3.1)$$

Where the values of the coefficients c_1, c_2, c_3, c_4 (3.2) depend on the geometry shape of the coils, μ is the permeability, d_{avg} is the average diameter of the coil and φ the fill factor, which is equal to:

$$\varphi = \frac{(d_{out} - d_{in})}{(d_{out} + d_{in})} \quad (3.2)$$

Where d_{out} and d_{in} are the outer and internal diameters, respectively.

Layout	c_1	c_2	c_3	c_4
<i>Square</i>	1.27	2.07	0.18	0.13
<i>Hexagonal</i>	1.09	2.23	0.00	0.17
<i>Octagonal</i>	1.07	2.29	0.00	0.19
<i>Circle</i>	1.00	2.46	0.00	0.20

Table 3.2: Coefficients in function of the coils' shape.[49]

The calculated theoretical values of inductance and capacitance were verified using the *Ansys HFSS* simulation software.

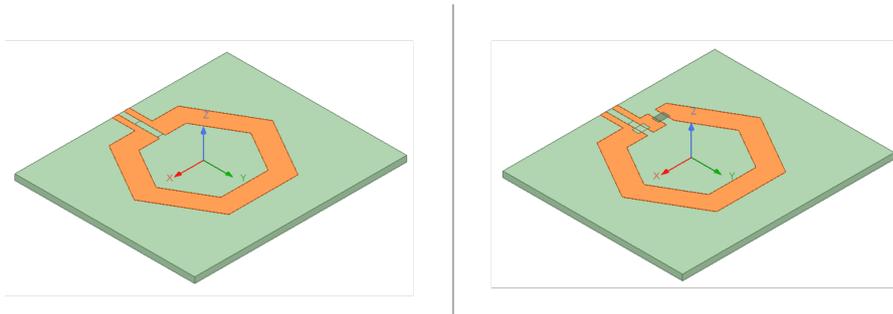


Figure 3.4: Ansys 3D model of a transmitter coil. *Left:* model w/o matching capacitors; *right:* model with matching capacitors.

In addition, the shift in frequency of the return loss (S11) was also controlled to be minimized at the proper operating frequency of 433 MHz. Fig. 3.5 shows the return loss of the coil after adding the corresponding matching capacitors.

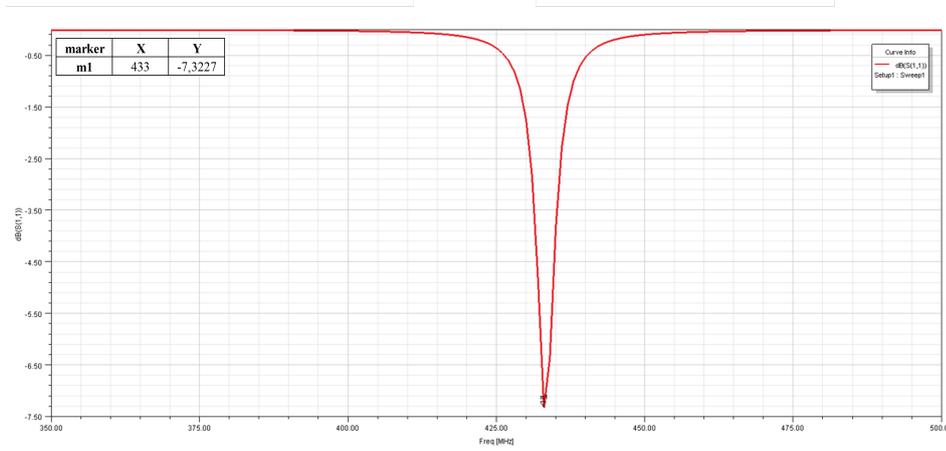


Figure 3.5: Return loss simulated with Ansys HFSS.

The peak is correctly positioned at the 433 MHz frequency, thus validating the design procedure.

In the final implementation and subsequent fabrication of the coils, the use of *capacitive trimmers* has been preferred with respect to fixed capacitors to perfectly match the impedance considering possible variations in inductance and resistance due to manufacturing or parasitic factors.

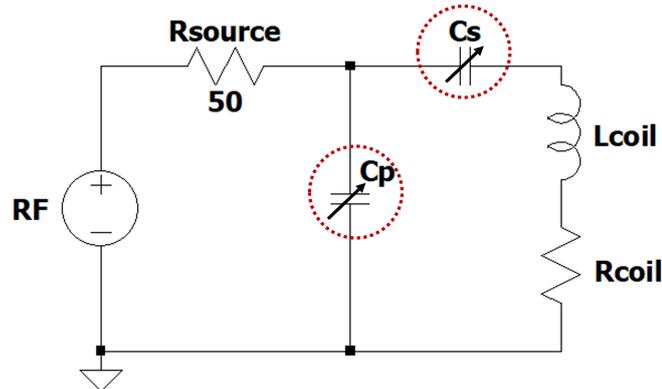


Figure 3.6: Equivalent circuit with L-matching IMN: trimmers implementation.

The trimmers selected were the *JR150* and *JR500* by *Voltronics* [50] for the series and parallel capacitor respectively. By tuning the *series trimmer*, it is possible

to control the *shift* of the self-resonance frequency of the coil, while by adjusting the *parallel trimmer*, it is possible to regulate the *bandwidth* and the *amplitude* of the S11 peak. In this way, the coil can be optimized for power delivery and data transmission simultaneously.

The manufactured coils and the testing results are presented in the following section.

3.2 Coil Fabrication

The transmitter coils with their respective trimmers were designed in *Altium Designer* and manufactured on a 1.55 mm thick FR4 substrate (Fig. 3.7). The coils are made with a 35 μm thick single-turn copper trace. Different shapes with different sizes and widths were tested. The copper trace was left uncovered to have a higher current density flux and, therefore, an increase in the induced magnetic field to increase inductive coupling.

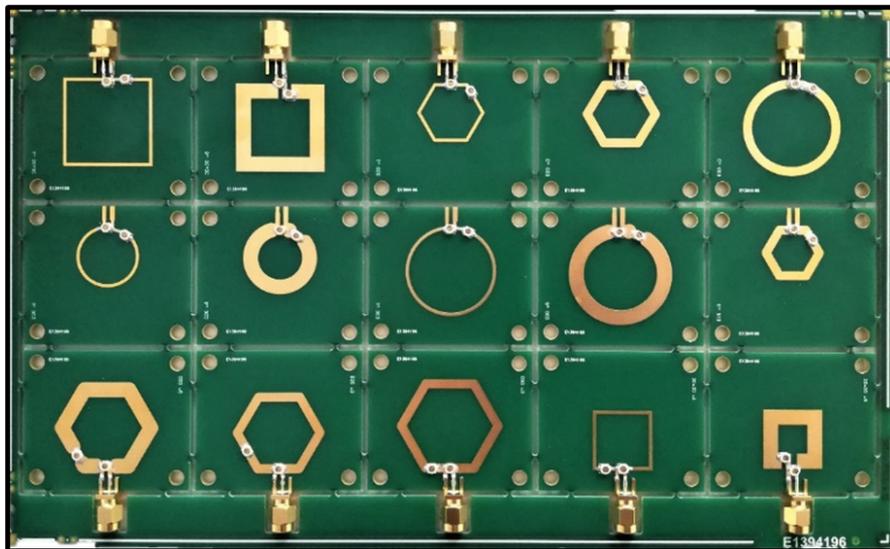


Figure 3.7: Manufactured transmitter coils.

3.3 Measurements and Results

With the coils manufactured, each coil's impedance value was measured with the *Vector Network Analyzer* (VNA). Once the experimental value was known, the values of the matching capacitors were then calculated. The equivalent circuit with the values obtained from the experimental measurements was simulated using LTspice. The simulated parameter S11 was compared with the experimental measures of the coils after tuning the matching capacitors.

Fig. 3.8 shows the comparison between the LTspice simulation and the experimental measurement of S11 for the square coil with a size of 20x20 mm and a width of 5 mm, used as a demonstrative example.

The same procedure was then performed for each coil manufactured, leading to an equivalent result.

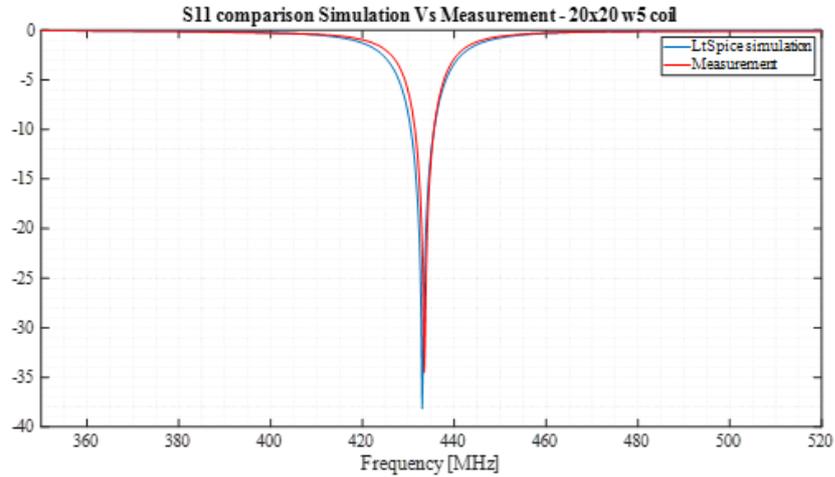


Figure 3.8: S11 comparison: LTspice simulation Vs measurement.

Fig. 3.9 displays the S11 parameter in function of the different shapes and geometries of the coils fabricated after the tuning of the trimmers.

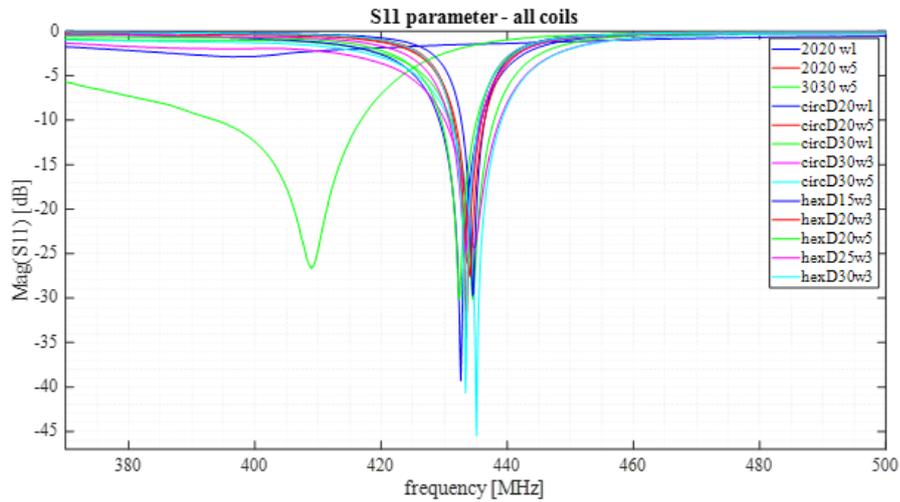


Figure 3.9: S11 of all the manufactured coils.

The results obtained confirm the expectations from the simulations. The IMN correctly tuned the transmitter coils to have the maximum performance in terms of power transfer at the frequency of 433,92 MHz.

For most of the coils, the peak is correctly positioned at the desired frequency with amplitudes ranging from -25 to -45 dB. Only the circle coil 30 mm in diameter (green) and the squared coil 20x20 (blue) show worse performance due to the width traces of 1 mm that take the capacitance values out of range for the matching.

Finally, the parameter S_{21} was measured with the VNA to evaluate the power transferred by a transmitter coil (Tx) and a receiver coil (Rx) to control the bandwidth for correct data transmission up to the data rate of 10 Mbps. For the tests, the hexagonal coils with an internal diameter of 25 mm and 20 mm were used as Tx and Rx, respectively.

Fig. 3.10 displays S_{21} as a function of frequency at different distances between Tx and Rx.

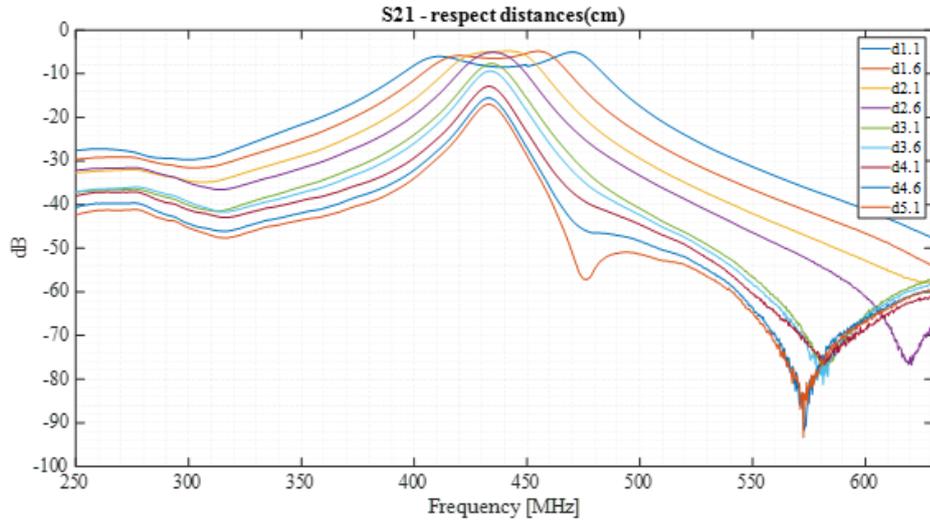


Figure 3.10: Measurement of parameter S_{21} of all the manufactured coils.

Considering these results, a qualitative evaluation of the *signal distortion* based on the designed BW was performed.

The measurement setup is shown in Fig. 3.11. It includes the RF base station PCB (presented in Ch.4), a power amplifier (PA), a directional coupler for measuring the power transferred from the PA to the coil, and Tx and Rx coils.

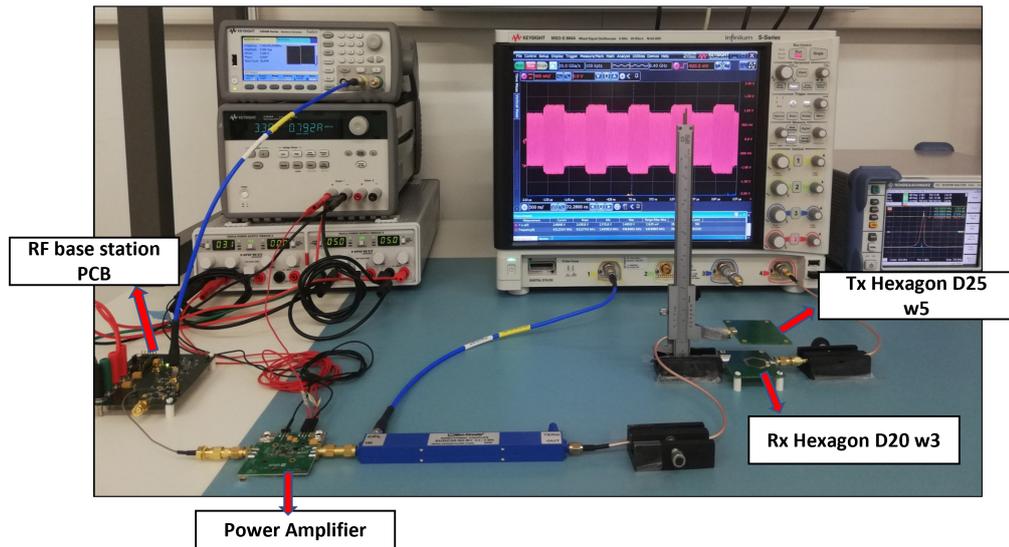


Figure 3.11: Setup for S₂₁ measures.

Fig. 3.12 shows the ASK modulated signal received at the Rx side at different data rates, from 2 Mbps to 20 Mbps, with a distance of 2.1 cm between Tx and Rx coils.



Figure 3.12: Received signal at different data rate: a) 2 Mbps, b) 4 Mbps, c) 6 Mbps, d) 8 Mbps, e) 10 Mbps, f) 20 Mbps.

From this figure, the modulated signal is correctly received up to 10 Mbps; on the contrary, rising the DR up to 20 Mbps, the signal loses its correct squared shape, meaning that the bandwidth available is insufficient to reconstruct the digital signal properly. In fact, considering the curve of Fig. 3.10 relative to the distance of 2.1 cm, the band at -3dB is 40 MHz and, assuming a data rate of 20 Mbps, only the first harmonic of the signal can be reconstructed, resulting in a very deformed signal.

Chapter 4

Radio-frequency Base Station Design

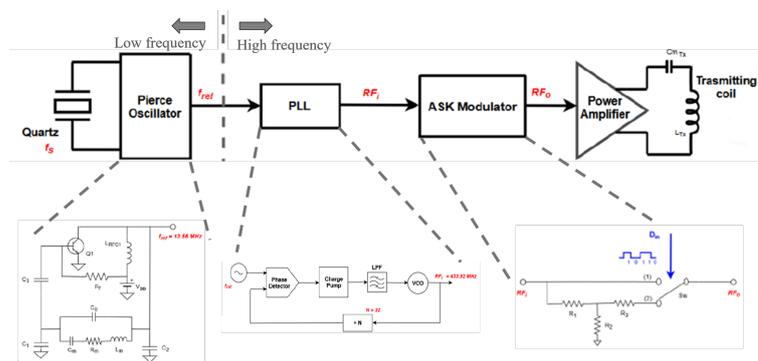
The PCB is the external RF base station transmitter designed to generate a radiofrequency carrier signal of 433.92 MHz and properly modulate it according to the digital data received from the image processing. Power and data are sent to the implanted CMOS microelectrodes using an amplitude-shift keying modulation technique (ASK).

My work aimed to design and fabricate a new PCB starting from the work of Gian Luca Barbruni [1] and Barbara Gentile [2].

This chapter will provide a brief overview of the system's architecture, and the proposed new design of the PCB will be explained. Afterward, the measures performed to test the correct functioning of the fabricated PCB circuit will be presented.

4.1 System Architecture

The main blocks of the RF transmitter are illustrated in the figure below:



In detail, the complete PCB circuit design includes:

- **Pierce Oscillator:** first block of the PCB, intended to generate the initial sinusoidal wave at the fixed frequency of 13.56 MHz. This oscillator uses a quartz crystal to guarantee the optimal stability of the oscillation. This is fundamental for the next step to precisely fit the narrow ISM band chosen in this project, which is $[433.05 \div 434.79]$ MHz. The crystal chosen is the *NX5032GA* manufactured by *NDK* [51].
- **Phase-Locked Loop (PLL):** this feedback control system generates the target RF band frequency of 433,92 MHz, multiplying the input frequency by an integer factor selected from the programming of the PLL registers. Starting from the oscillation frequency of 13,56 MHz, the PLL registers must be programmed to obtain a multiplication factor of 32. To set the registers of the PLL properly, without depending on an external programming board, the microcontroller (MCU) *MSP430G2553* from *Texas Instruments*[52] was added to the circuit. In this way, the instructions to fill the registers are directly sent from the MCU to the PLL, exploiting the Serial Peripheral Interface (SPI) protocol. The PLL used is the *LTC6948-1* manufactured by *Analog Devices*[53].
- **Amplitude-Shift Keying (ASK) Modulator:** realized employing a switch to divert the signal on an attenuated or non-attenuated line depending on the digital signal sent from the image processing that controls the position of the switch. The attenuation occurs through the implementation of a symmetrical T-pad attenuator composed of three resistors chosen to attenuate the signal's amplitude by the desired value (Fig. 4.2).

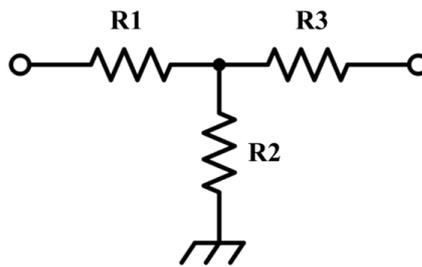


Figure 4.2: T-pad attenuator.

The values of the resistors are $R1=R3=10\Omega$ and $R2=120\Omega$ to have an attenuation of 3.5 dB. Thus, the result is to be able to distinguish the digital bits

related to the data without ever turning off the output power necessary to continuously power on the implanted circuit.

The switch used is the *M3SW-2-50DRA+* switch manufactured by *Minicircuits* [54].

- **Power Amplifier (PA):** to increase and enforce the modulated RF signal's robustness to reach better power and data transfer performance. Differently from the prototype proposed [2], the selected PA used in the new design is the class-AB PA: *RF6886* by *Qorvo* [55]. Section 4.2.2 details related to the integration of this component will be provided.

4.2 New PCB Design

Starting from the first PCB prototype [2], the design has been modified to overcome the issues related to the RF reflections and by removing the unnecessary components used for preliminary tests, thus realizing a more compact circuit to optimize the power delivery. Specifically, three main improvements have been made:

- The implementation of a *double switch configuration* in the ASK module to avoid the intersection of the RF traces, which leads to problems with the reflection of the RF signal, consequently worsening the performance of the circuit in terms of PDL.
- The replacement of the *power amplifier* with a new one, also manufactured by Qorvo, with better performance in terms of gain and maximum output power. Furthermore, the complete RF evaluation board, tuned to work in the frequency range of 433 MHz up to 470 MHz, was used to test the new PA's performance properly.
- A *power management system* based on rechargeable battery DC/DC converters to power the entire EPU.

The new implementations mentioned above will be described in detail in the following paragraphs, and the final schematics and layout will be presented.

Fig. 4.3 shows the work flow of the new PCB design:

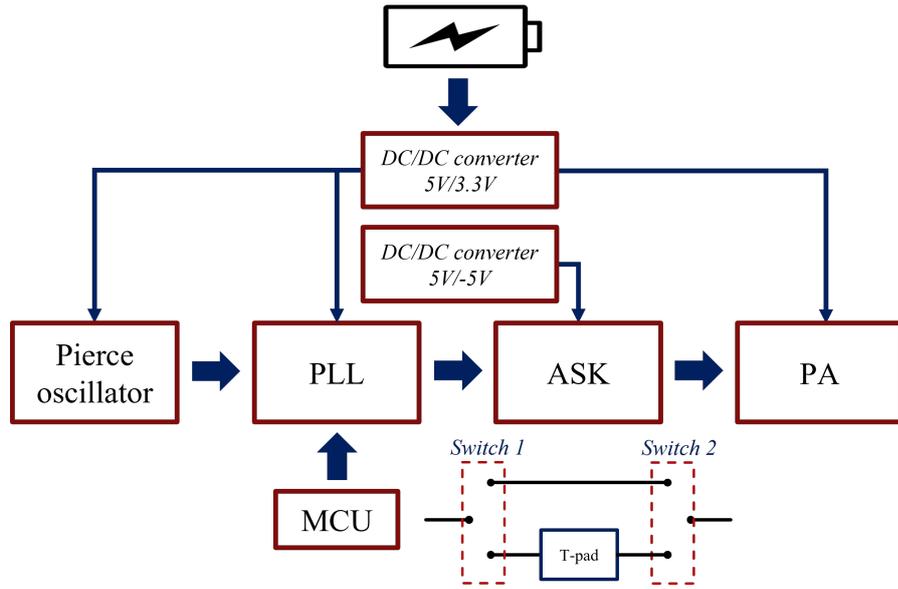


Figure 4.3: General scheme of the new PCB design.

4.2.1 Double Switch Configuration for ASK modulation

As anticipated in the previous paragraph, a second switch was added after the T-Pad attenuation to prevent the crossing of the traces that leads to reflections. Since the switch M3SW-2-50DRA+ is bidirectional, the same component was selected to guarantee the same transition times of both switches, allowing the passage of the RF signal only in one of the two traces. To simplify the final layout without making new intersections between signal traces, the two switches have been positioned in opposite orientations, one concerning the other.

The new configuration is shown in the figure below:

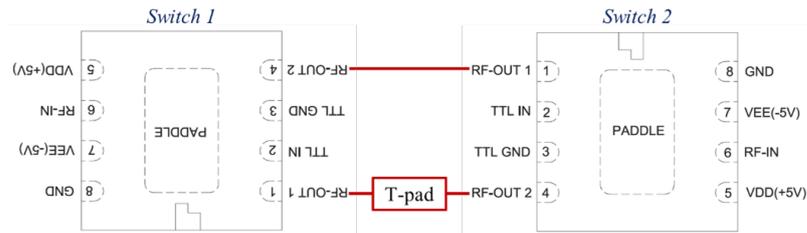


Figure 4.4: Double switch configuration.

In this configuration (Fig. 4.4), the RF outputs of the switches are inverted. RF-out1 is connected with RF-out2 and vice versa. This means that one of the two switches must reverse its working logic. For this purpose, the initial idea was to

add only one inverter before the TTL input of the second switch. However, this would have led to a delay in the propagation of the signal. This was unacceptable as it is essential that the two switches change simultaneously. So, the final solution was to add a buffer before the TTL input of the first switch, thus creating the same propagation delay, and ensuring the simultaneous triggering of the switches. Thus, to control both switches with the same digital signal and ensure the state's simultaneous change, a buffer and an inverter were placed before the TTL input of switch1 (SW1) and switch2 (SW2), respectively. This way, when a certain logical state arrives, the first SW will read the same state, and the other will read the inverted value. This allows the two switches to coordinate correctly, allowing the RF signal to pass only through the attenuated or non-attenuating trace, consequently avoiding any intersection between them.

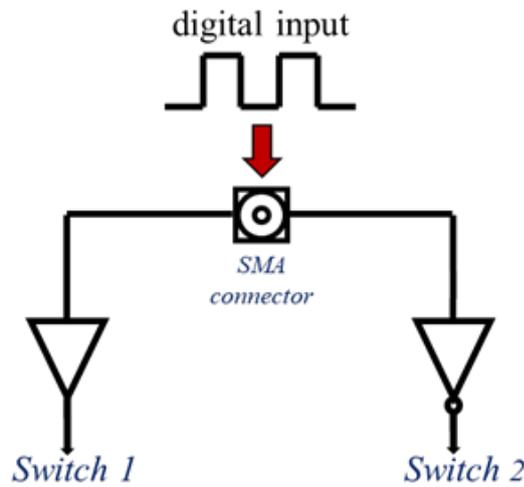


Figure 4.5: Buffer and Inverter integration for the ASK modulation.

To ensure that the propagation delay times were the same, two components of the same family were chosen: *SN74LVC1G34 Single Buffer Gate* [56] and *SN74LVC1G04 Single Inverter Gate* [57] by *Texas Instruments*. The TTL input signals of both switches were then measured to verify the correct operation of the buffer and the inverter, respectively, as shown in Fig. 4.6 and Fig. 4.7.

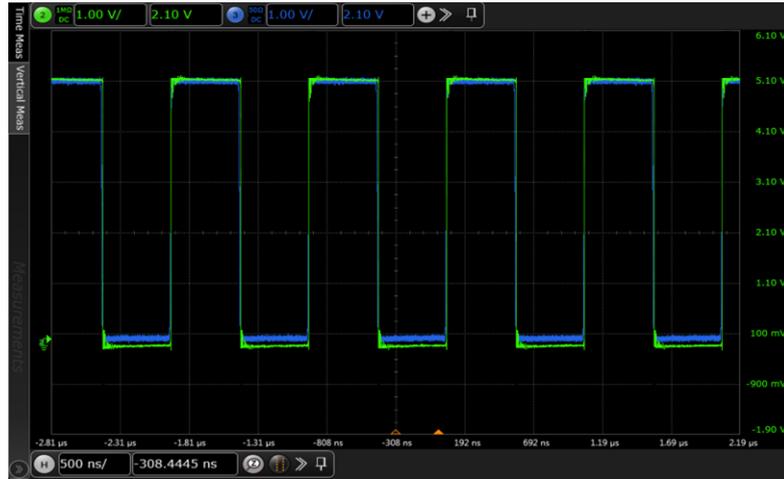


Figure 4.6: TTL input signal after the buffer. *Green trace:* the original signal sent from the waveform generator. *Blue trace:* the signal after passing the buffer.



Figure 4.7: TTL input signal after the inverter. *Green trace:* the original signal sent from the waveform generator. *Blue trace:* the signal after passing the inverter.

4.2.2 Power Amplifier: Qorvo RF6886

To increase the RF output power of the system, the power amplifier chosen was the class-AB PA: RF6886 manufactured by Qorvo [55]. The class AB was preferred since it represents the best trade-off between power, linearity, efficiency, and robustness in terms of susceptibility to the load network. The main electrical specifications of the RF6886 PA are summarized in table 4.1 and compared with those of the previous PA RF5110G [58].

Parameters	RF5110G	RF6886
Output Power	32 dBm	36.5 dBm
Gain	32.5 dB	33 dB
Efficiency	50%	>50%
Working frequency	450 MHz	433.92 - 470 MHz

Table 4.1: Comparison of the Power amplifiers from Qorvo: *RF5110G* and *RF6886*.

As demonstrated in the table above, the RF6886 PA performs better than the previous one. To validate the performance of the RF6886, the evaluation board *RF6886PCK-411* [59] was tested and then integrated into the transmitting system. Figure 4.8 shows the schematics of the RF6886 Evaluation board optimized to work in the frequency range of [433 ÷ 470 MHz].

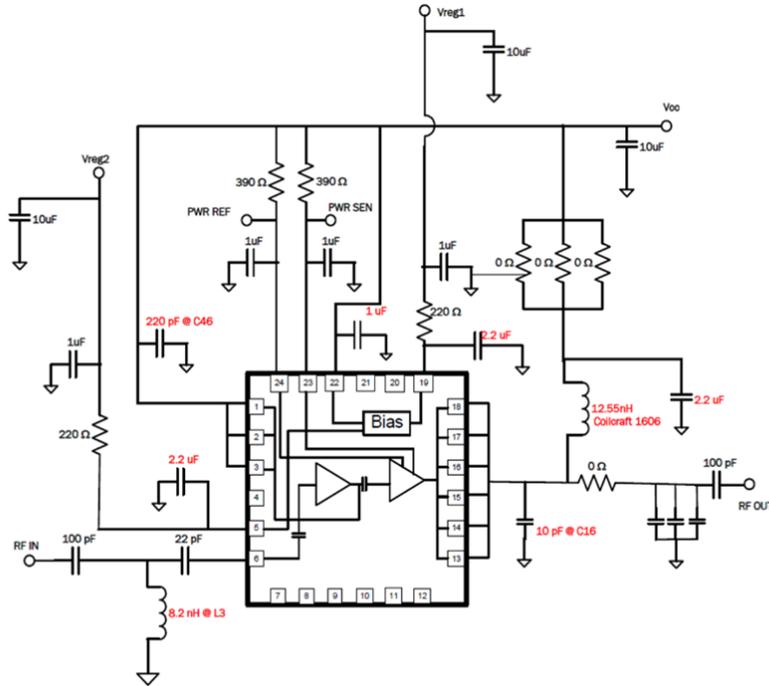


Figure 4.8: Schematics of the RF6886 Evaluation board. Reprinted from [55].

4.2.3 Power Management

To reach a final portable external processing unit device, all the reference voltages of the PCB need to be generated from one single power source. A dedicated *power management system* was designed using DC/DC converters to accomplish this target. In detail, for powering the PCB, the DC voltages needed are 3.3 V, 5V, and -5V.

In addition, it is essential to consider the amount of current consumed by the circuitry; in fact, the current consumption of the PA can reach a maximum of 3A. The last important factor to be considered before choosing the proper battery is to ensure sufficient autonomy for a minimum duration of active operation of the device.

Considering these specifications, a *portable power bank* was finally chosen. The standard commercial power banks provide a DC voltage of 5V and currents between 1.5A and 3A. For this project, a power bank with an output voltage of 5V, output current of 3A, and a minimum battery capacity of 20000 mAh was selected to guarantee an operating duration of at least 6 hours.

Therefore, the DC/DC converters selected to supply the PCB are:

- Isolated 5V to 5V DC/DC Converter *NMR100C* [60] from *Murata* to generate -5V;
- 5V to 3.3V DC/DC Converter *TSR3-0533* [61] from *Traco Power* capable of supporting until 3A;

4.3 PCB Design: Schematics and Layout

The software used for the PCB design was *Altium Designer*.

Starting from the schematic drawings of the circuits of the components selected, the final layout was created following the guidelines for the radiofrequency PCB design [62].

While designing a PCB's layout is essential to respect the production constraints dictated by the company chosen for the manufacturing. In this case, the company selected for the production and assembly of the PCB was *Eurocircuits*.

4.3.1 Schematics

Figure 4.9 shows the overall schematic of the transmitter PCB.

400 FR4 with a thickness of 0.36mm, dielectric constant $Dk=3.90$, and dissipation factor $Df=0.022$.

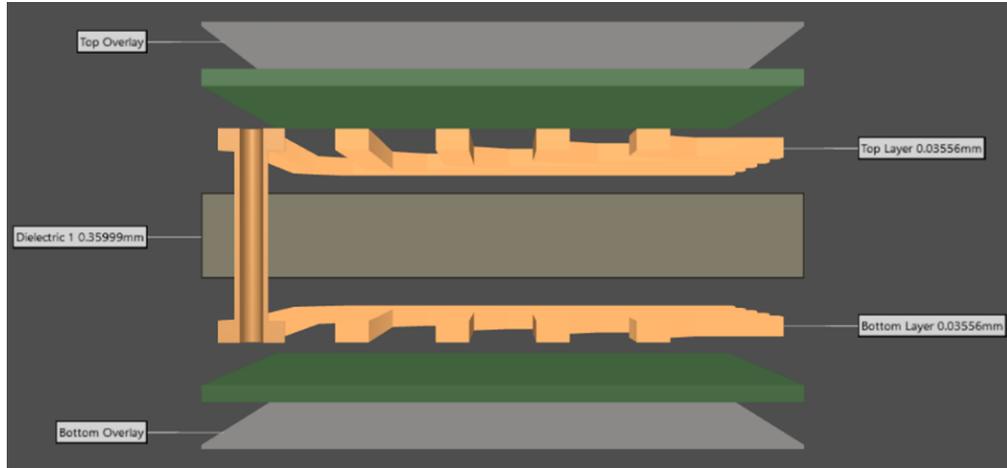


Figure 4.10: Board layer stack.

The last step for achieving the desired characteristic impedance of the traces is to derive the value of the trace width from the geometric parameters already defined. Thanks to the *Altium calculator tool*, a track width of 0.71 mm was derived, obtaining an impedance of 49.98Ω , as shown in Fig. 4.11.

#	Name	Material	Type	Weight	Thickness	Dk	Top Ref	Bottom Ref	Width (W1)	Impedance (Z0)	Devia...
	Top Overlay		Overlay								
	Top Solder	Solder Resist	Solder Mask		0.01016mm	3.5					
1	Top Layer		Signal	1oz	0.03556mm		✓	2 - Bottom L	0.70841mm	49.98	0.04%
	Dielectric 1	FR-4	Dielectric		0.35999mm	3.9					
2	Bottom Layer		Signal	1oz	0.03556mm		✓	1 - Top Layer	0.70841mm	49.98	0.04%
	Bottom Solder	Solder Resist	Solder Mask		0.01016mm	3.5					
	Bottom Overlay		Overlay								

Figure 4.11: Altium impedance calculator tool. Resulting impedance obtained: 49.98Ω .

In addition, *via stitching*, and *via shielding* techniques were used to avoid radiofrequency noise [63].

Via stitching is a technique used to create a solid vertical connection through the board layers, helping maintain a low impedance and short return loops. This is made by adding vias over the entire area of the PCB.

Via shielding is created by placing rows of vias alongside the RF signal traces to reduce crosstalk and electromagnetic interference (EMI) [64]. Also, the RF track has been designed by minimizing changes in direction to avoid the creation of reflections.

The final layout has been designed (Fig. 4.12) by paying attention to all the above-mentioned considerations.

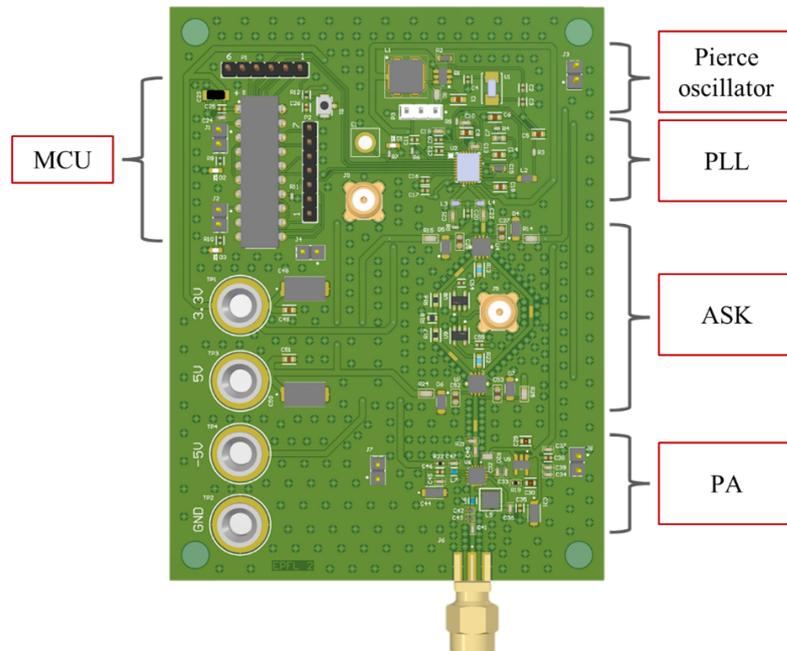


Figure 4.12: PCB layout of RF SWIPT base station (top view).

4.4 PCB Experimental Results

Fig. 4.13 shows the RF SWIPT base station PCB manufactured and assembled by *Eurocircuits*. As shown in the figure, small pads on the RF traces were exposed to be able to measure the passing signal and test the correct functionality of the circuit.

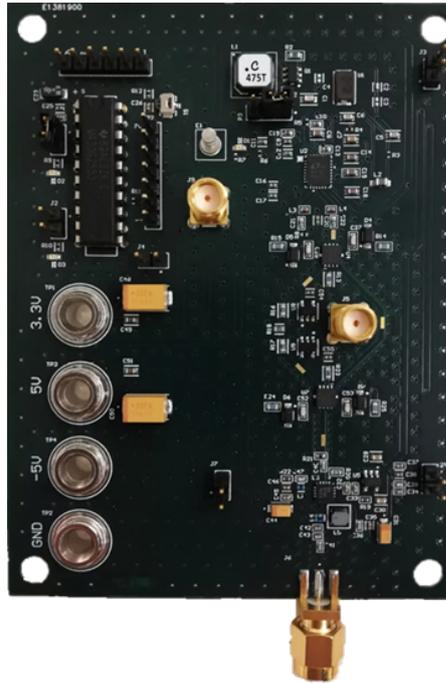


Figure 4.13: Manufactured RF SWIPT base station PCB (top view).

For the first usage time of the PCB, the microcontroller MSP430 must be programmed by using the dedicated *eZ-FET Onboard Debug Probe* of the *Launchpad MSP-EXP430G2ET* [65]. For this purpose, the launchpad must be connected to the GND, STBWIO, SBWTCK pins of the MCU on the PCB through the P1 header. After the execution of this process, the MCU will remain programmed.

Once the MSP430 on the board is programmed, it sends the signals needed to program the PLL registers every time the board is powered on. When the registers of the PLL are filled correctly, the D1 LED is turned on. A reset button S1 is present to eventually re-send the signals to the PLL.

When the PCB is turned on, the PLL receives the sinusoidal signal from the pierce oscillator. There is also the possibility of sending the signal from an external device using the SMA connector J9 by switching the pin of the header P3. SMA J5 is intended to receive the digital signal from the image processing to control the two switches generating the ASK modulation. Also, four more ground headers J3, J4,

J7, and J8 were added to always have a close reference pin during the testing stage, facilitating the measuring procedure. The final modulated output signal is taken from the SMA J6 to be connected to the transmitter coil.

4.4.1 Signal Testing

To measure the signal flow of each block, the Digital Storage Oscilloscope (DSO) was connected in parallel to the circuit with an internal impedance of $1\text{M}\Omega$. The measures were taken in the points indicated in the scheme below (Fig. 4.14).

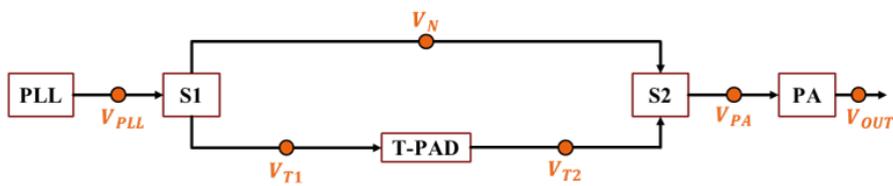


Figure 4.14: Test point scheme of the circuit.

The output signals of the tested blocks are presented below.

- **Pierce Oscillator**

Fig. 4.15 shows the output signal from the Pierce oscillator. Fig. 4.16 displays the FFT to check the frequency of the signal. The peak is centered at 13,56 MHz, as expected.

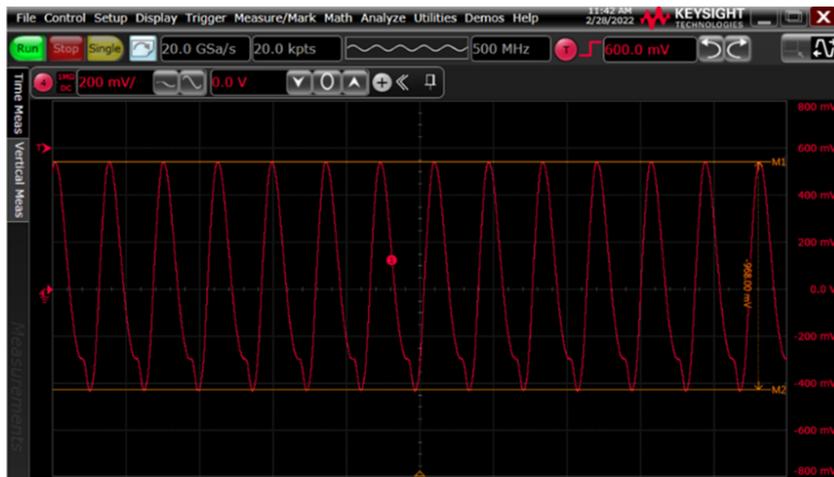


Figure 4.15: Pierce oscillator output; $V_{pp} = 986\text{ mV}$.

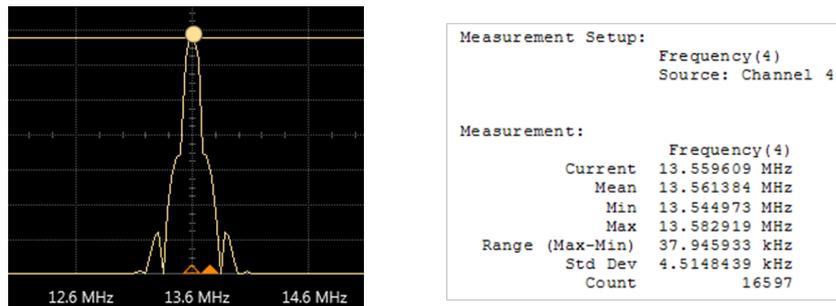


Figure 4.16: FFT of Pierce oscillator output signal; $f = 13.56$ MHz.

- PLL

Fig. 4.17 shows the output signal from the PLL (V_{PLL}), and, as shown in Fig. 4.18, the frequency is correctly locked at 433,96 MHz with minimum and maximum values included in the ISM band [433.05 ÷ 434.7] as desired.



Figure 4.17: PLL output; $V_{PLL}^{pp} = 533$ mV.

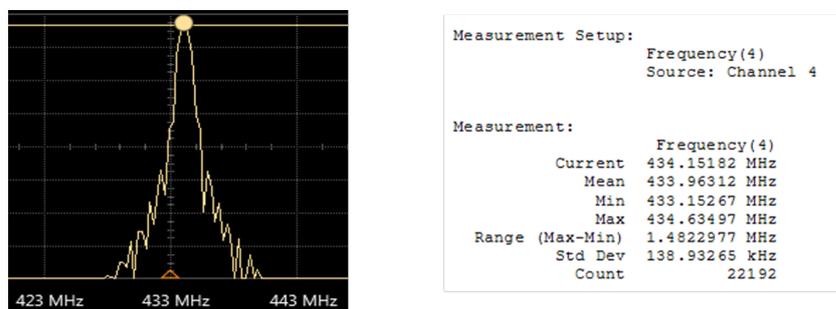


Figure 4.18: FFT of PLL output signal; $f = 433.96$ MHz.

This result confirms the correct functioning of the PLL and the correct sending of the instruction signals from the MCU to the PLL registers.

- **ASK**

To test the correct performance of the two switches, the digital signal was supplied by the waveform generator (WG) with a duty cycle of 50%, representing the worst operating condition. A fixed logic value of “0” or “1” has been set with the WG to measure the signal passing through only in one trace, either attenuated or not attenuated.

Starting with the *attenuated trace*, Fig. 4.19 show the signals before (V_{T1}) and after (V_{T2}) the T-pad attenuator, respectively.

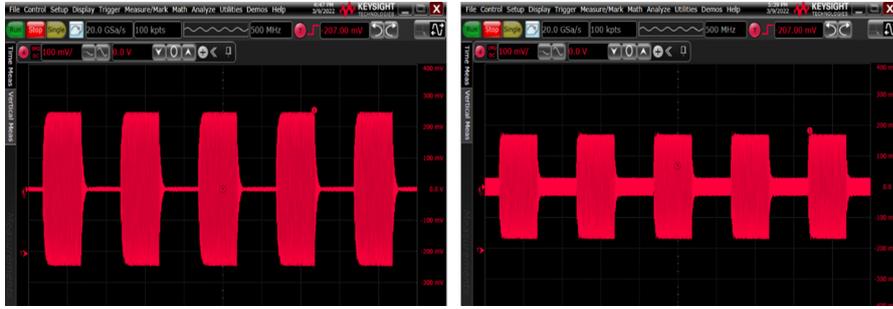


Figure 4.19: Signal before (on the left) and after (on the right) T-pad attenuator; $V_{T1}^{pp} = 470.90 \pm 19,74$ mV, $V_{T2}^{pp} = 343.30 \pm 19,67$ mV.

The attenuation calculated from the experimental analysis is 2.75 dB resulting in a modulation index (MI) of 15.7%, calculated following the equation below:

$$MI_{\%} = \frac{V_{max}^{pp} - V_{min}^{pp}}{V_{max}^{pp} + V_{min}^{pp}} \times 100 \quad (4.1)$$

The difference between the measured attenuation and the expected one of 3.5 dB can be due to the tolerances of the 5% from the nominal values of the resistances that compose the T-pad.

Fig. 4.20 displays the signal passing through the *not-attenuated trace*.

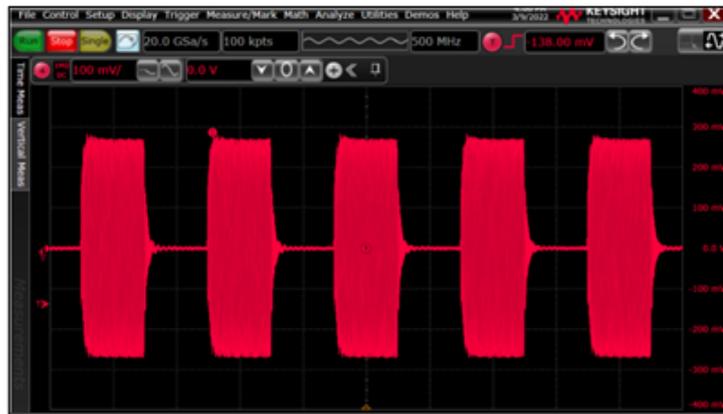


Figure 4.20: Signal passing through not-attenuated trace; $V_N^{pp}=593.58 \pm 23.55$ mV.

From the results shown, the RF signal correctly presents a duty cycle of 50% with an OOK (On-off keying) modulation in both traces.

- **PA input signal**

Fig. 4.21 shows the resulting signal after the modulation block. As displayed in the figure, the RF signal's amplitude is correctly modulated according to the digital signal sent from the WG.

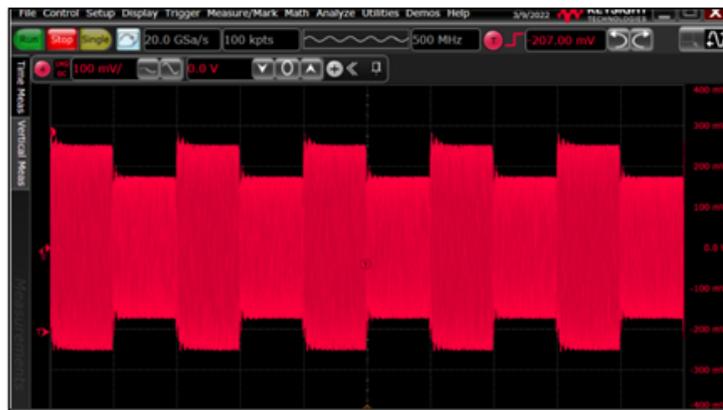


Figure 4.21: Power amplifier input signal; $V_{PA}^{pp}=542.08 \pm 4.98$ mV.

- **PCB output signal**

The final output signal is shown in Fig. 4.22. The blue track is the digital signal from the WG (square wave $V_{pp}=5V$, $DC=50\%$). The red signal is the final modulated output signal for transmitting power and data simultaneously to the implanted receivers.



Figure 4.22: Output signal after the amplification; $V_{OUT}^{pp}=7.93$ V.

From the image, it is possible to observe that when a digital “1” is given, the RF signal goes on the non-attenuated trace. On the contrary, when a digital “0” is received, the signal passes on the attenuated one, consequently reducing the amplitude.

A 10 dB attenuator between the PA output and the DSO was used to not damage the instrument. The maximum output power is equal to 32 dBm, which corresponds to 1.58 W.

The total maximum consumed power of the PCB is 7.9 W, and the absorbed power of the single input voltage provided by the voltage generators is summarized in table 4.2.

Voltage	Current	Power
5 V	60 mA	300 mW
-5 V	6 mA	30 mW
3.3 V	2.3 A	7.6 W

Table 4.2: Power consumed for each input voltage.

Once the functionality of the PCB was validated, *the entire RF transmitter setup* was assembled (Fig. 4.23). It includes the *RF base station PCB*, the *power amplifier RF6886 Evaluation board*, and the *transmitter coil* already optimized for power and information transfer, as explained in chapter 3.

In the setup shown, a directional coupler was added to monitor the signal passing through the line between the PA output and the Tx coil. Furthermore, the transmitter coil has been mounted with a caliper to accurately measure the distance between the transmitter and the receiver coil.

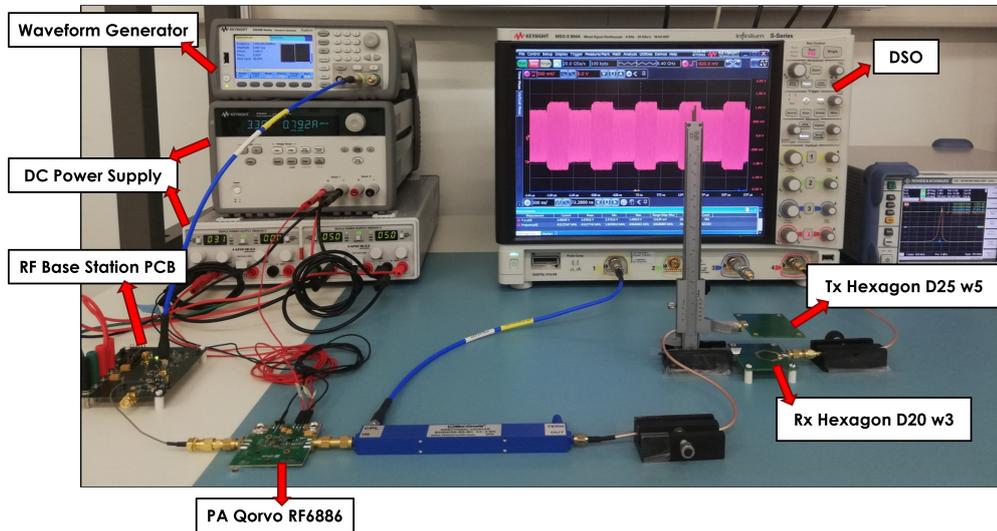


Figure 4.23: Final setup of the transmitting unit.

Chapter 5

Real-Time Image Processing

Until this moment, the digital signal responsible for the modulation of the RF carrier signal was given from a waveform generator.

However, in the final application, the signal containing the information about the stimulation of the implanted CMOS μ electrodes came from processed images captured by a camera mounted on sunglasses.

Recalling the structure of the entire project shown in Fig. 5.1, the complete external transmitting system, including the image processing block, will be presented in this section.

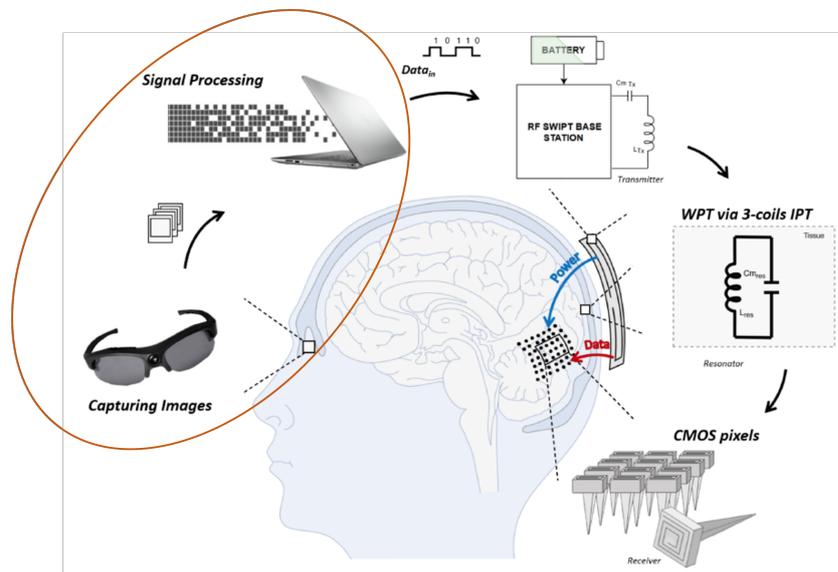


Figure 5.1: Smart neural dust to revert blindness: image processing block.

Starting from the work on the image processing of Simone Emiliani, supervised

by Prof. Sandro Carrara and Eng. Gian Luca Barbruni [66], the process flow has been adapted to make recording, processing, and information delivery *real-time*.

5.1 Image Processing for Artificial Vision

To recreate the sense of vision through the production of phosphenes (points of light), electrical stimulation to specific points of the visual cortex is necessary to form a black and white image in blind patients [67].

For this purpose, the previously developed Matlab algorithm has been used [66]. In particular, a video is processed frame by frame to collect information about the addressing and the intensity of the stimulation that will be sent to the RF base station for the ASK modulation.

The process flow of the Matlab algorithm is summarised below:

- **Conversion to greyscale:** to reduce the number of pixels to be processed;
- **Contrast adjustment:** to improve the performance of the subsequent edge detection and to differentiate the indoor from the outdoor environment;
- **Filtering:** to remove the noise from the input images;
- **Edge detection:** segmentation algorithm to find the discontinuities points in the images;
- **Dilation:** to uniform the edges detected in the previous step;
- **Resizing:** to match the number of pixels with the amount of the CMOS microelectrodes implanted;

The result of each step is depicted in Fig. 5.2.

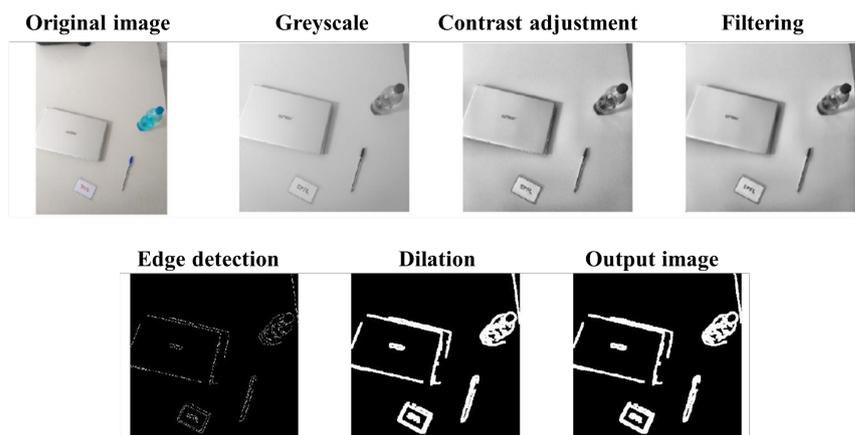


Figure 5.2: The image processing flow, reprinted from [66].

The output is a binary image in which the active pixels are represented with the digital 1 (white pixels) and the non active ones with a digital 0 (black pixels).

The information related to the active pixels is encoded on 14-bit binary strings. The first bit is the *string header*, represented with a 0, the next 10 bits contain the *XY address* of the pixel in the image, and the last 3 bits contain the information concerning the *intensity of the stimulation*.

At the end, only the strings referring to the active pixels (white spots) for each frame are sent to the RF base station.

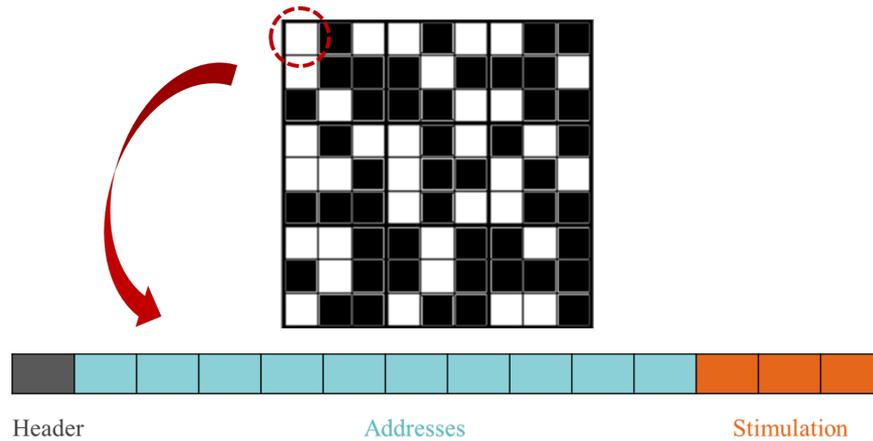


Figure 5.3: Encoding of information regarding the stimulation of active pixels.

The correct function of the processing algorithm was initially tested by processing a pre-recorded video and saving the data to be sent in matrices. Therefore, the next step was to make the whole system working real-time.

5.2 Real-Time Video and Processing

To make the entire process flow real time, two main improvements have been made:

1. The integration of an *external webcam* to capture real time video;
2. The setting of *serial communication* to send data from the MATLAB processing to the RF Base station PCB;

The webcam used is the “C270 HD WEBCAM” from Logitech, connected to the PC via USB port.

MATLAB Support Package for USB Webcams was used to import live images from the webcam into MATLAB [68]. Once the webcam was connected to MATLAB,

a loop was set to capture a frame, process it, and send it out to compose the information signal for the ASK modulation. The time required for capturing, processing, and sending data for one frame is between 80ms and 120ms, depending on the number of pixels activated for each frame.

To send the data regarding the captured images from MATLAB to the outside, it is necessary to open a serial communication from the PC to the external device.

As the first prototype, the microcontroller *MSP430G2553* by Texas Instrument, already used to set the PLL registers, was employed to send data from MATLAB to the PCB.

To be able to connect the microcontroller to the PC via USB cable, the *MSP-EXP430G2ET Launchpad* was employed.

The following section will briefly explain the different universal serial communication interface (USCI) protocols offered by the *MSP430x5xx Family* before describing the communication setting chosen.

5.2.1 Serial Communication Protocols

The USCI protocols available for the MSP430G2553 microcontroller are *SPI*, *I2C*, and *UART* [69].

Serial communication protocols

- SPI: Serial Peripheral Interface.

The SPI is a synchronous serial communication interface that provides full-duplex communication using a master-and-slave architecture.

To connect the master with one or multiple slaves, this protocol is based on four digital signals, which are:

SCLK: *serial clock*, is the synchronization signal sent from the master to the slave.

MISO: *master-Input / slave-Output*, is the data line sent from the slave.

MOSI: *master-Output / slave-Input*, is the data line sent from the master.

SS: *slave select*, to indicate that data is being sent or used to select a specific slave in case of multiple slaves' configuration.

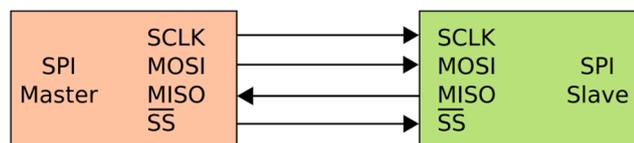


Figure 5.4: SPI protocol.

To start the communication the master configures the clock, and from that point, each clock cycle, the data transmission occurs via MOSI/MISO buses.

- I2C: Inter-Integrated Circuit.

I2C is a half-duplex synchronous serial communication protocol based on a master-and-slave configuration. This protocol, differently from the previous one, establishes the communication by using two lines:

SCL: *serial clock* for synchronizing the communication.

SDA: *serial data* for sending data.

The communication begins when the master sends a start sequence to the slave via SDA line. Then, data are transferred in packets. Each packet is composed of the binary address of the slave, in case of multiple slaves, and by the data to be transmitted. Start and stop conditions are used to discriminate each packet of data from another.

The start and stop sequence are exclusive strings where the SDA line can change while the SCL (clock line) is high level. Otherwise, when the data is transferred, the SDA must remain stable while the SCL is at a high level.

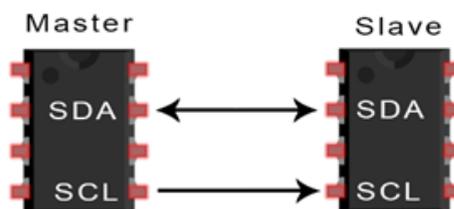


Figure 5.5: I2C protocol.

- UART: Universal Asynchronous Receiver/Transmitter.

UART is a hardware asynchronous serial communication protocol. This is a full-duplex based communication that directly connects one transmitter device to a receiver through two lines: Tx and Rx.

Since the transmission is asynchronous, the clock signal is not present; hence, start and stop bits are added to the UART communication data packet to be able to discriminate one packet to the new one transmitted. The base of this communication protocol is the *parallel-to-serial* conversion, as shown in the scheme below.

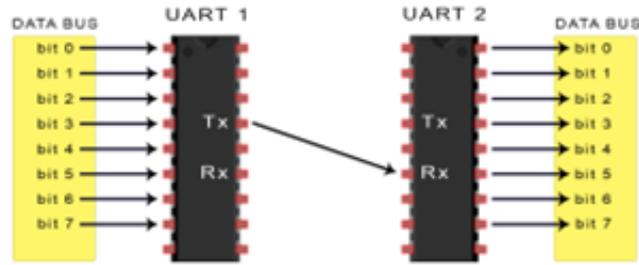


Figure 5.6: UART protocol, *parallel-to-serial* conversion.

The transmitting side converts parallel data into serial for the transmission to the receiving part, which then converts the serial data back into parallel data. Also, data format and baud rate, responsible for the transmission speed, are configurable.

Since the launchpad has an eZ-FET onboard debug probe containing an integrated *USB-to-serial* converter, the UART protocol was chosen to transfer data from MATLAB to the microcontroller. In fact, through a USB connection, the laptop can recognize the UART as a virtual COM port and establish communication.

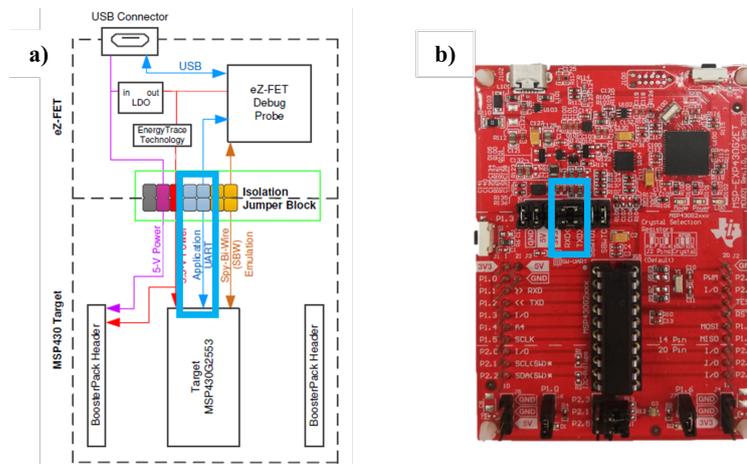


Figure 5.7: eZ-FET Isolation Jumper Block Diagram. Reprinted from [69].

Fig. 5.7a shows the block diagram of the MSP-EXP430G2ET Launchpad, while Fig. 5.7b shows the configuration to set the UART connection between the eZ-FET part of the board and the microcontroller mounted on the bottom part. Finally, the microcontroller was programmed to read the incoming data from the PC through the receiver pin (Rx) and send them out to an output General-Purpose

Input/Output (GPIO) pin.

The final configuration model is shown in the figure below.

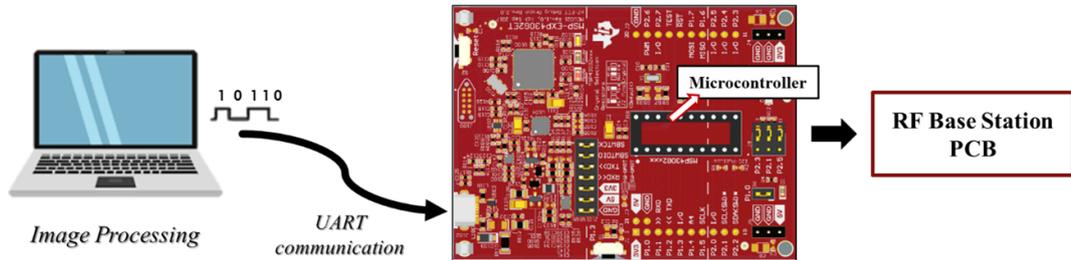


Figure 5.8: Configuration model for the UART communication between the laptop and the microcontroller.

5.3 Experimental Setup and Results

The first step had been to verify that the data from MATLAB were sent correctly in output through the microcontroller, as shown in the figure below. As displayed in the DSO in the figure, the digital strings data are rightly received after the image processing.

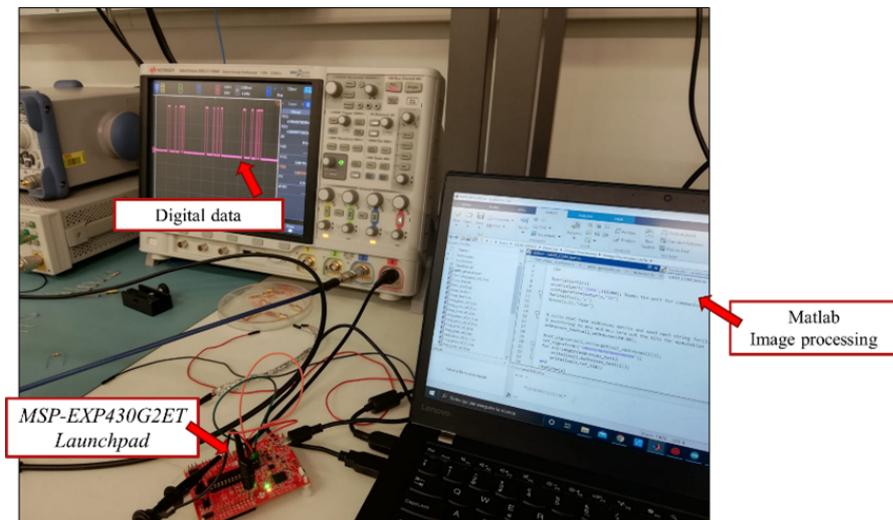


Figure 5.9: Validation of data transfer from MATLAB processing.

Once the correctness of the data had been verified, the waveform generator was replaced with the real data coming from the real-time processing of the captured images from the external webcam.

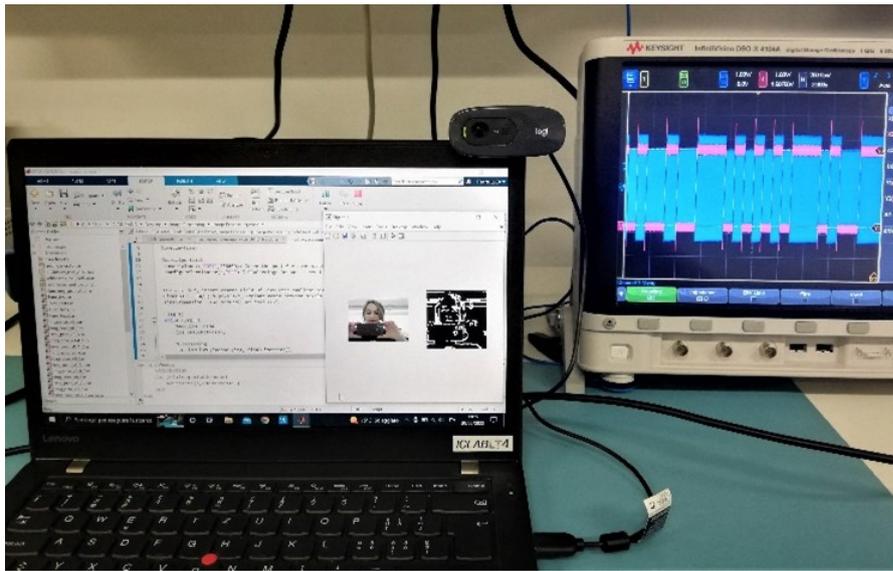


Figure 5.10: Real time recording and processing.

Finally, the entire image processing block was added to the transmission system. The final complete setup is shown in Fig. 5.11.

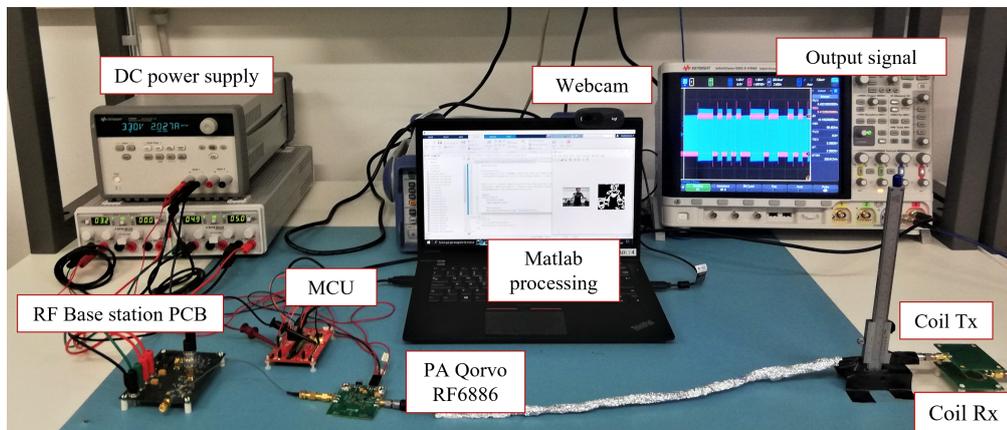


Figure 5.11: Final setup of the complete transmitting system.

Therefore, the full transmission system to send simultaneously power and data is complete. In detail, it is composed of the *DC power supply* to power the PCBs, the RF base station *PCB* with the *PA* evaluation board, the *PC* with the *webcam* plus the *microcontroller* to send the information signal, and the *transmitter coil*.

The final output at the receiver side (Rx coil) is presented in Fig. 5.12.

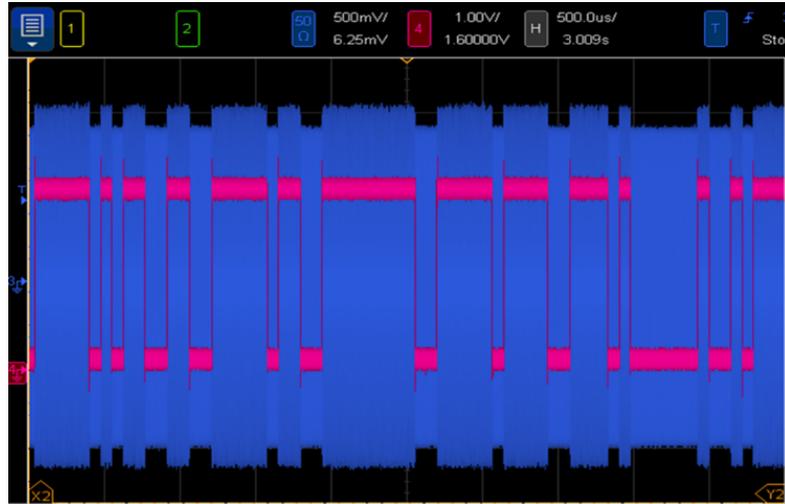


Figure 5.12: Amplitude modulated signal for the simultaneous transmission of power and data.

The pink signal is the data signal that comes from the image processing. It is a signal between 0 and 3.3V, which is the maximum output voltage of the GPIO output pins of the microcontroller. The blue signal is the modulated signal received at the receiver coil.

Fig. 6.2 shows the final EPU system no longer powered by the DC power supply but by the rechargeable power bank, thus making the device portable.

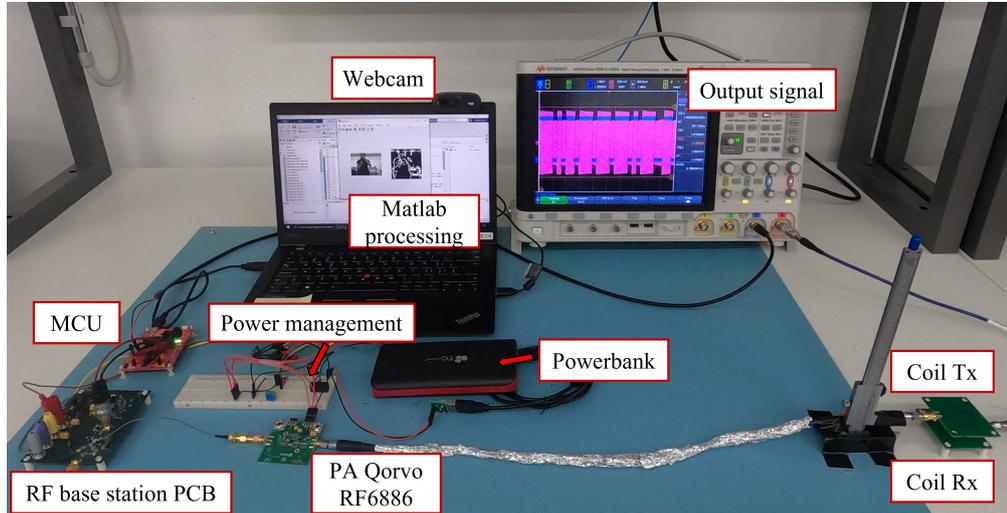
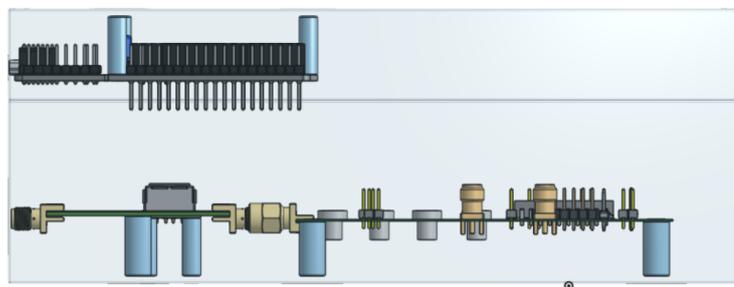


Figure 6.2: Complete EPU powered through the rechargeable powerbank.

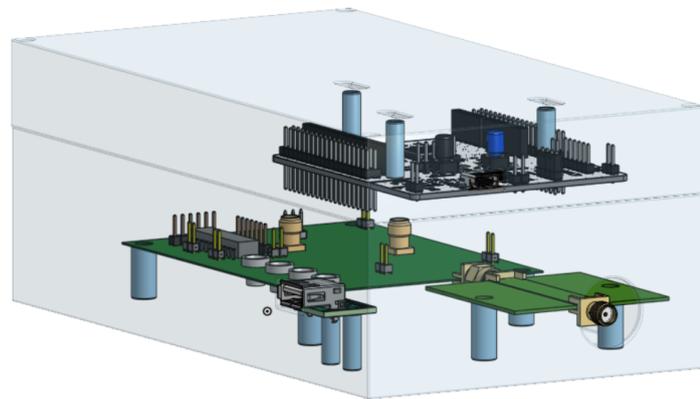
6.1 EPU Packaging

After the entire validation of all the blocks of the entire system, a transparent plastic *case* was designed. The latter was fabricated using *laser cutting* manufacturing process to have a single dedicated and portable device containing all the electronic parts of the entire EPU. Fig. 6.3 and Fig. 6.4 show the 3D model and the 3D printed case, respectively.

The case has been designed with *Onshape* software and comprises two parts: cover enclosure and bottom enclosure. Fig. 6.3 shows the 3D model created of the box.



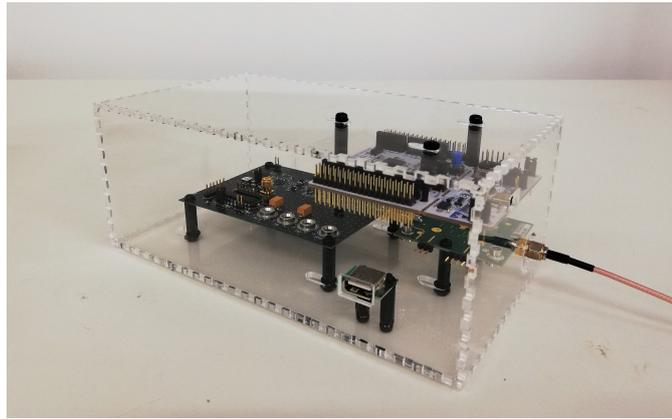
(a) front view



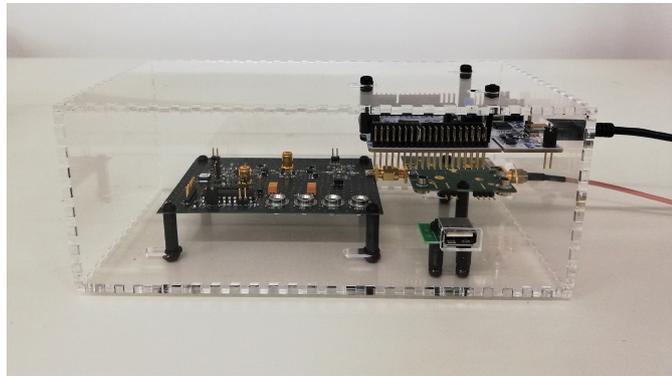
(b) isometric view

Figure 6.3: 3D model of the case for the EPU

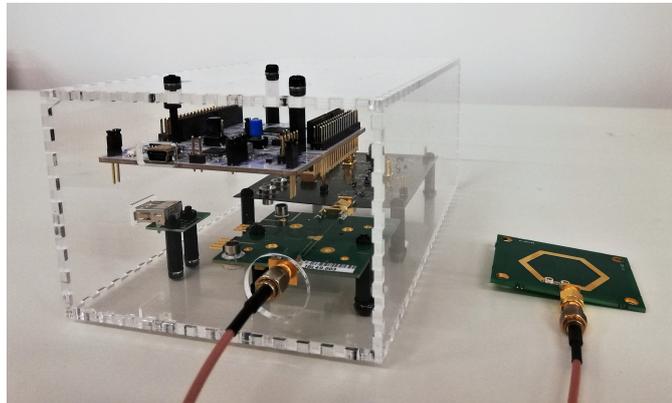
Referring to Fig. 6.4, the EPU is powered by using a power bank connected to the USB input; the laptop is connected via cable to the microcontroller mounted on the cover enclosure; the transmitter coil is connected to the SMA connector and then fixed to a helmet worn by the patient.



(a) *perspective view*



(b) *front view*



(c) *perspective view, with mounted Tx coil*

Figure 6.4: printed 3D model of the case for the EPU

Chapter 7

Conclusions and Future Developments

In recent years, the technology of implantable neural systems has undergone enormous advances.

Wireless power transfer is the key point for the next generation of miniaturized micro-implants for brain monitoring and stimulation. In this context, the neural dust concept is the pathway to the progressive development of cutting-edge neuro-prosthesis. In particular, visual prostheses have shown a great potential for visual impairment treatments by taking advantage of the neural dust approach.

In this project, an external processing unit for simultaneous wireless information and power transfer has been designed and fabricated for developing an innovative CMOS-based cortical neuroprosthesis to restore vision. Firstly, the acquisition, processing, and delivery of the image information concerning the brain stimulation have been programmed to be in real-time.

A new RF Base station PCB has been designed and manufactured to generate the ASK modulated signal for simultaneously sending the information signal from the image processing and the power achieving an output power of 32 dBm and a maximum data rate up to 10 Mbps. To finally send power and data wirelessly to the implanted micro-electrodes, new transmitter coils were designed and fabricated, including an L-type matching network to maximize the power transfer.

The validation experiments were conducted, and the correct operating of the device was verified. Hence, a polymer case for the entire device has been fabricated through the laser cutting process completing the device.

Therefore in this project, the single portable external processing unit, powered by a rechargeable battery, was realized.

7.1 Future Developments

A further step will be integrating the RF power amplifier evaluation board from Qorvo with the same RF base station PCB. Hence, a *new PCB* can be designed by merging the two parts mentioned, including the DC/DC converters for the power management. Also, to further optimize the power generated by the RF transmitter device, the design of a *class-E power amplifier* can be considered to increase the total amplifying efficiency of the system. In addition, others solution to optimize the performance of the system can be implemented.

FTDI FT232H

It is possible to use a serial adapter cable to transfer the data from the laptop, after the image processing, to the PCB without using a microcontroller. In particular, *FTDI* provides *USB-to-serial hi-speed adapter* cables with embedded electronics. For this project, the cable *C232HM-DDHSL-0* [70] can be a good solution to transfer the data with high data rate up to 30 Mbps. This is a USB 2.0 Hi-Speed to MPSSE (Multi-Protocol Synchronous Serial Engine) cable that contains a small internal electronic circuit board utilizing the FTDI FT232H chip; this is encapsulated into the USB connector end of the cable and handles all the USB signaling and protocols. The C232HM MPSSE cable can be configured into JTAG, SPI, I2C interface.

Image Processing into Embedded Systems

To obtain a more compact and portable device for increasing the comfort of the patients, it is preferable to minimize the number of different electronic parts to reduce the weight and dimensions of the device itself.

For this purpose, the next step can be replacing the laptop and the microcontroller with a single platform. One possible solution is to integrate the image processing into embedded systems, such as *Raspberry Pi* (Fig. 7.1).



Figure 7.1: Raspberry Pi 4B board. Processor: quad-core Cortex-A72 (ARM v8) 64-bit SoC @ 1.5GHz.

Raspberry Pi is a small single-board computer to which a webcam can be connected via USB or the dedicated module already mounted on the board. Also, the MATLAB processing algorithm can be deployed on the RAM of Raspberry pi. In this way, the captured images are directly processed, and the stimulation information data are sent directly to the PCB through the Raspberry GPIO pins to generate the ASK signal.

Furthermore, considering the final use of the designed system in this project, the real-time operation of the device is crucial.

One of the significant drawbacks of MATLAB is its slow code execution concerning other generic programming languages, such as C, C ++, and Python. The *Python* programming language is an interpreted, general-purpose language [71] and is one of the most mature, prevalent, and well-supported languages in the machine learning area. The excellent advantage is its simplicity in writing code and, indeed, is always a preferable choice for running computer vision code. On the other hand, Python is an interpreted language, so it can sacrifice the speed of a compiled language, leading to slow code execution.

Alternatively, for guaranteeing the best speed performance in code execution, C/C++ is the optimal choice.

Appendix A

Additional Content

A.1 Code Composer Studio for MSP 430

Code for setting UART communication with MSP430 MCU.

```
1 #include "msp430g2553.h"
2
3 #define TXLED BIT6
4 #define RXLED BIT0
5 #define TXD BIT2
6 #define RXD BIT1
7
8 int main(void)
9 {
10     WDCTL = WDIPW + WDIHOLD; // Stop WDT
11     P1DIR |= BIT3; // Set P1.3 to output direction
12     DCOCTL = 0; // Select lowest DCOx
13     BCSC1 = CALBC1_16MHZ; // Set DCO
14     DCOCTL = CALDCO_16MHZ;
15     P2DIR |= 0xFF; // All P2.x outputs | Disable Port2 that is not
16     // needed
17     P2OUT &= 0x00; // All P2.x reset
18     P1SEL |= RXD + TXD; // P1.1 = RXD, P1.2=TXD
19     P1SEL2 |= RXD + TXD; // P1.1 = RXD, P1.2=TXD
20     //P1DIR |= RXLED + TXLED; // set pin leds as output pins
21     P1DIR |= RXLED; // set pin led as output pin
22     //P1OUT &= 0x00; //setup on board led | starting from off value
23     UCA0CTL1 |= UCSSEL_2; // SMCLK
24     UCA0BR0 = 62; // 16MHz 256000. This is the low byte (page424 of
25     // User manual)
26     UCA0BR1 = 0x00; // 16MHz 256000 | it is 0x00 because 2 stays one
27     // byte. This is the high byte
```

```

25 UCA0MCTL = UCBS2; // Modulation UCBSx = 4
26 UCA0CTL1 &= ~UCSWRST; // **Initialize USCI state machine**
27 UCOIE |= UCA0RXIE; // Enable USCI_A0 RX interrupt
28 __bis_SR_register(CPUOFF + GIE); // Enter LPM0 w/ int until Byte
   RXed
29 while (1)
30 { }
31 }
32
33 #pragma vector=USCIAB0RX_VECTOR
34 __interrupt void USCI0RX_ISR(void)
35 {
36     P1OUT |= RXLED;
37     P1OUT = (UCA0RXBUF<<3); //shift 3 times the bit to have it at P1.3
   pin
38     P1OUT &= ~RXLED; //turn off the led
39 }

```

A.2 MATLAB code for real time processing

Main code for real-time image processing.

```

1 %% Test webcam video Streaming
2 clear
3 close all
4 clc
5
6 %webcamlist
7 cam=webcam(); %cameraname
8 %preview(cam)
9
10 %serialportlist
11 s=serialport('COM4',256000); % open the port for communication
12 configureTerminator(s,"CR") % CR=Carriage Retour
13
14 FOV = 5; % degree, insert camera Field Of View
15 Pixel_FOV = 64/5; % pixels/degree, Implant ratio between pixels and
   FOV
16 finalDimension = 32;
17
18 flag=1;
19 while flag==1
20     %Acquire frame
21     img=snapshot(cam);
22
23     %Processing - Edge detection

```

```
24 BW= im2uint8(indoor2(img, finalDimension));
25
26 % generation of addresses
27 [addresses, all_addresses] = addr_generator(BW);
28
29 %Display
30 subplot(1,2,1);imshow(img);
31 subplot(1,2,2);imshow(BW)
32 axis image;
33 axis off;
34
35 %ADDRESSING
36 for j=1:length(addresses)
37     writeline(s,addresses(j));
38 end
39 end
40 %clear cam
```

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