POLITECNICO DI TORINO

Master's Degree in ELECTRONICS ENGINEERING

Master's Degree Thesis

FIRMWARE DESIGN OF 3-PHASE GRID-TIED CONVERTER

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Summary

The grid-connected systems are being developed very fast and are now in operation worldwide. As an important source of distributed generation the systems need to comply with standard requirements in order to ensure the safety and the seamless transfer of the electrical energy to the grid. But the converters has highlighted the some problems specifically of harmonic interaction between converters and the grid. Because, electrical grids are complex and dynamic systems affected by multiple factors such as continuous connection of loads and an abruptly disconnection of loads, disturbances and resonances resulting from the harmonic currents flowing through the lines, lightning strikes. This thesis aims to implement the three phase Grid-tied converter and test at different loads. In the meanwhile, by monitoring continuously the grid parameters in order to make sure that grid is suitable for normal power converter operation. The test bench behaves like a Boost-Converter which is connected with grid at normal grid dedicated voltage and performs accordingly at variable loads. The designed system can also be use for lab activities by students of Electrical Engineering.

Acknowledgements

I would like to thanks first and foremost the God Almighty for His endless grace. A debt of gratitude is also owed to my advisor Fausto Stella and supervisor Gianmario Pellegrino for their continuous support and help whenever I stuck in a problem or had any question about my project. They always helped me in this endeavour. Without their active guidance, help, cooperation and encouragement, I would not have made headway in this project.

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Introduction

1.1 Future Scope of Grid Connected Converters

It has been seen that in past few decades, the use and dependency on renewable energies has been significantly increased and all future predictions are giving a strong sign of more dependency on renewable energies in near future.

There is an increase in the trend of power converters due to an increase in the reliability of renewable energy resources. These power converters help these resources to easily connect with the grid lines.

As the field of power electronics is expanding its horizon, there is a great development in the power converters on the side of EV's battery charges. In the coming future the electric mobility is continue to increases exponentially. In 2018, the selling of electric car increases 5.1 million and increases day by day. China is become the largest buyer of these electric car's. US and Europe are on the second and third tier.

Electric cars basically save more energy as compare to the oil driven electric cars. Increasing demand in the electric car's basically have a great impact on demand of the oil use products. In the recent stock exchange, the EV's stock is estimated to escape 127 million tonnes of oil equivalent according to the New Policies Scenario.

The electrification in car market result in a rapid growth of automotive battery manufacturing capacity. The reason behind is the maximum number of electrical car sold as compare to the other modes of car. This electrification result in reducing the cost of automotive battery pack. EV's play a pivotal role to facilitate the availability of energy storage at a low cost. EV's also play an instrumental role in the future for the cleaner energy system.

In the case of power systems, the EVs are now becoming the integral part as compare to the past due to its advancement. The incremental need for the peak power generation and transmission capacity can be achieved when we run EVs drive

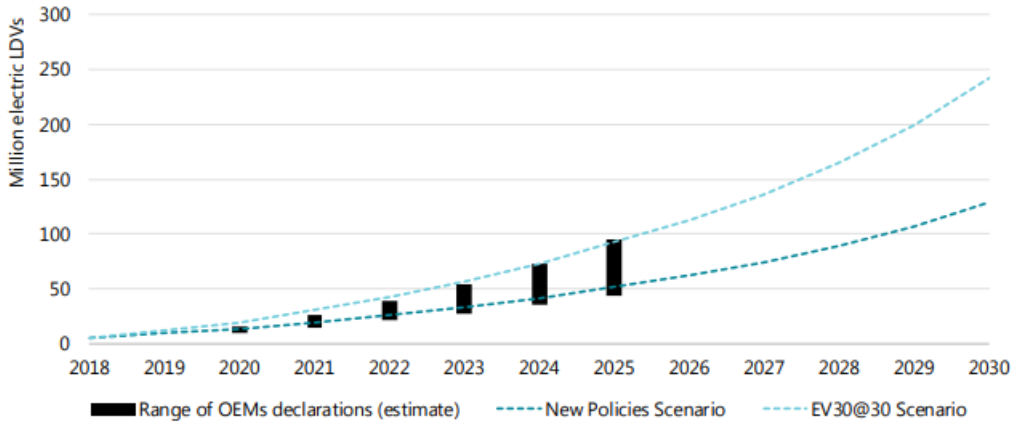

Figure 1.1: Global Electrical Car Stock

at uncontrolled charging mode. These EVs drives can greatly impact our power system total annual electricity demand, daily charging pattern on load profiles and location of power levels utilized under charging.

The recent development in Electric batteries greatly influence the road transport which are running on oil. The total global EVs stock is approximated nearly 127 million of oil equivalent in 2030. The product EV30@30 will move toward 215 MToe of oil product in 2030.

The electricity demand for the global EV fleet will surpass 640 TWH in 2030 in the figure below according the New Policies Scenario. In 2018, it was approximately 58 TWH but it is exponentially increase altogether. Its equal to final consumption of France and Spain in 2016. In the EV30@30 Scenario, the larger volume of the global EV fleet leads to 1 110 TWH of electricity demand in 2030, nearly double the amount of the New Policies Scenario. [1]

The light-duty vehicles (LDV's) are growing its user as compare to the other modes of wheeler's in 2020. The expert predicts that in 2030 LDV's will get 60% of total vehicles as compare to buses 26%, two wheeler's 12% and trucks 3%. So, LDV's in the coming future will be use by everyone throughout the world.

EV's can play its part in the flexibility of Power System when it is used in a controllable mode. When it is operated in this mode it has a very good results on the variable renewable energy, power generation mix and grid stability issues. Here are following features of EV's are as follow:

- In a power system, the load profile can be reduced by using the EV's which can control the charging patterns to occur with low demand periods.
- In a power system, when utilize EV's it can give us the feature of ultra-short

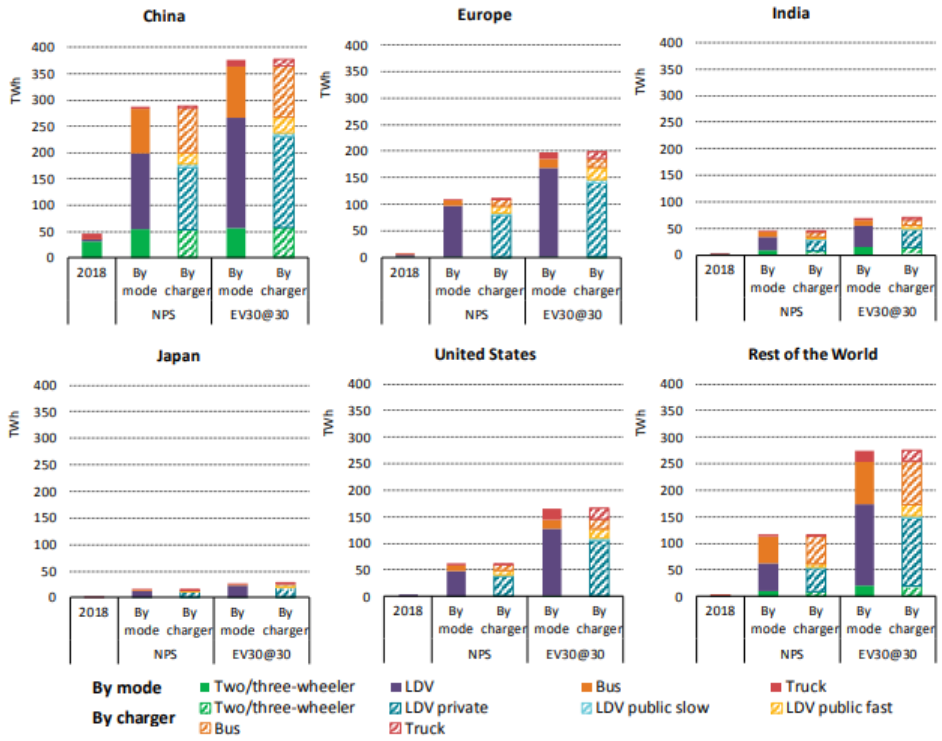

Figure 1.2: Demand of EV's Electricity by Region, Mode and charger

term demand response and provide use very fast and precise response to control signals.

- The energy store in EV's can use for multi-purpose other than providing energy to the locomotive.

1.2 Dynamic Problems in Grid monitoring and Grid Synchronization

As the renewable energy, distribution generation resources and EV charging stations are evolving with the time, the importance of power converters is also simultaneously increases. But there is a downside to use the converter due to harmonic interactions between multiple converters. The drawback of these harmonics is that they bring instability in the system and produces resonances which affect the quality of power in the grid. When these sort of oscillations and harmonics produced in such a grid which is connected of multiple converters so it will damage the grid due to the unbalance voltage and current in result of those oscillations. So we have to rectify

this problem on bus system level.

In a year 1995, due to these high frequency switching oscillations it damages the new generation trains lines started in Zurich. Similarly, its happen in Swiss Railway when they interchange the old locomotive design with the new high switching frequency design, the trains automatically stop due to increase strength of the oscillation produced on those locomotive. So on the side the old design was far better than this modern design because the old design produces less oscillation in the system.

Due to this evolving issue, the Italian Transmission Service Operator(TSO) Terna is deploying the dynamic model of machines which should be used in the plants. Every wind or solar plant owner must interact with Terna to show the simulation of working of their plant under following conditions:[2]

- Steady-state condition.
- Transient state condition.
- Both electrically and magnetically steady-state condition.
- Steady-state condition connected with grid under the influence of harmonics.

We must have to do the literature review of dynamic interaction of power converter with the transmission lines to have complete insight of the connection. The analysis can be performing through different methods so we have to select that one which is best suited for our model. Power electronic systems are non-linear due to these high frequency switching harmonics and oscillation produced in the practical grid systems. There are some technical points that we have to check when we are doing the literature review which are follow as:

- We have to study the linear state space model in the control system in which analysis is done through eigenvalue. In the eigenvalue analysis the system is divide into two blocks one is the hardware and other is a software block which are connected with each other through Component Connection Method (CCM). This method helps us to change the parameter of a single block without changing the parameter of the whole single block. We can also see the result of each block and change the setting of each block according to our desire result. The participation factors are used to identify zero and pole to address the dynamic interaction between the power converters. It provides us the analytical modelling but require much more information of both the block hardware and software which are not quite available in commercials systems.
- We utilize Nyquist criterion to study the frequency domain analysis on the admittance model of the converters. In this model we can represent each block

of converter with the Thevenin or a Norton equivalent model which is show in the figure below. There are following advantages of the method:

i The integration of power converter with grid will be simple because all the converter changes into generator-admittance circuits.

ii We can analyze the negative resistance behavior in our controllers by the help of bode diagram.

iii Equivalent admittance can be achieved using measurement so black box method is suited for commercial use of the converters.

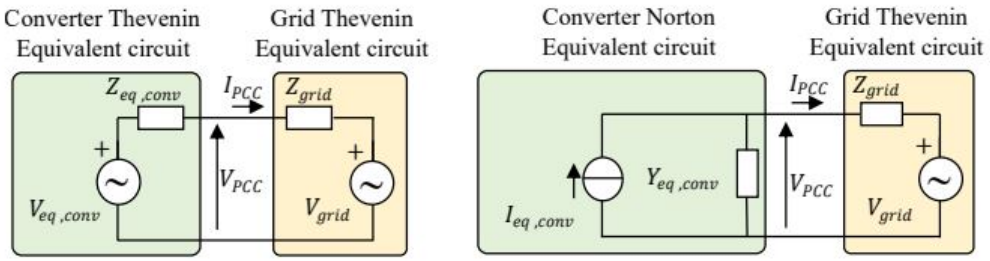

Figure 1.3: Norton and Thevenin Equivalent Circuit of Grid [3]

1.3 Standards Requirements for Grid-Tied Converters

Power generating system are rapidly growing with the time and we have to connect these sources to our grid. For instance, the energy generated by the solar PV cell must be processed and filter through an inverter before we connect the energy to our grid system. So, a converter is placed between the power generating system and the grid system which is responsible for the proper connection of energy. As there is an advancement in the field of power electronics, it become necessary for us to utilize the renewable resources energies to connect with our small and medium grid level system. Especially the solar and wind energy sources are very cheap and it's playing to be competitive sources of energy in comparison with fossil fuels so converter plays an important role for the connection of these sort of energy resources with transmission line.

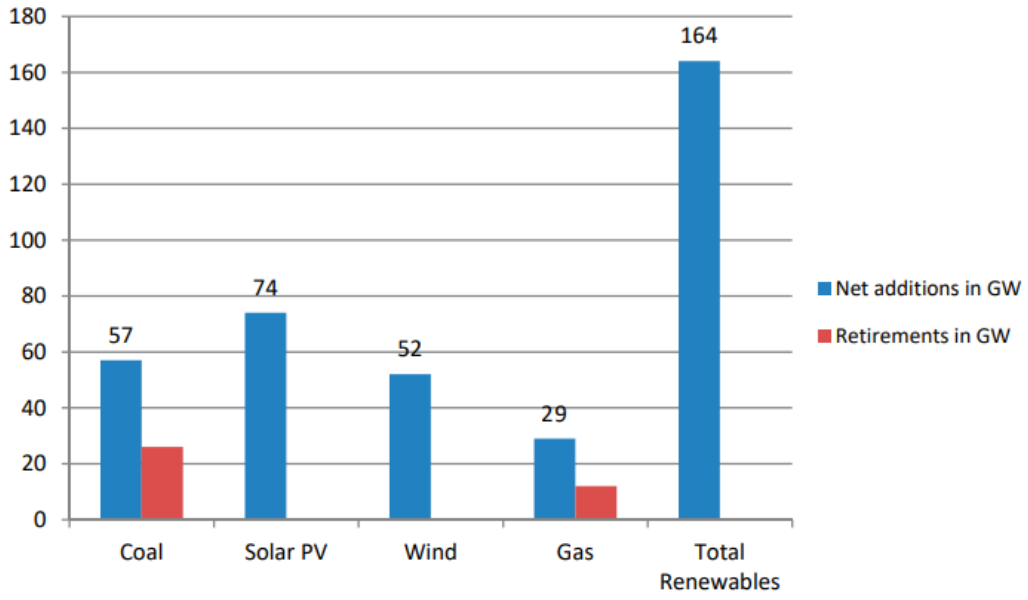

Figure 1.4: Total Energy capacity in 2016

From the above graph you can see that the Solar PV cell is producing more energy that the remaining renewable resources. We can analyze from the growing trend of producing energy from renewable resource, it become very vital for us to produces the converter circuit which would add this energy to our current grid system. There are following Standard requirement that we have to follow in order to connect it with the grid which are as follows:[2]

- Less cost at the power converter level.
- Converter should be reliable.
- Output harmonics should be minimum.
- Reduced switch to be deploy in integration with the grid.
- Continuity in the input supply should be required.
- Maximum Power Point Tracking (MPPT) must be used to find the maximum operating power point in case of solar system.

The power converters are very sensitive to harmonics and oscillation produced in the transmission line under abnormal condition which can trip the protection system and damage our power converter or utilities other services. At the coupling stage, power converter connects the renewable energy with the grid system and it generally reduced the voltage abnormality and other undesired effects. These voltage oscillations and harmonics should be detected by both the synchronization system and power converts so to have smooth connection between the two source of energies.

Three phase voltage converter grid synchronization also used advance detection schemes which basically reject the higher order harmonics in the voltage and current and identify the sequence of voltage vector in a very quick and accurate way. Flexible Alternating Current Transmission System (FACTS) basically used STATCOM (Static Synchronous Compensator) and SSSC (Static Series Synchronous Compensator) is also used to detect the harmonics and remove it from the transmission line and can help to inject or reject the active and reactive power in the transmission line according to our desire requirements.

1.4 Literature Review on Converter

1.4.1 Converter General Description and Schematic

This converter is designed by the department of Electrical Engineering of Politecnico Di Torino. This converter has the ability to work for motor drive applications or also as the Grid-Tied converter and or as an On-Board Battery charger. The main goal of design of this thesis was to be a operate this multi-purpose converter which can mold itself according to different applications as a Grid-connected converter. One of the main feature of this converter that it would sustain with least amount of THD (Total Harmonic Distortion) when we utilize in above mentioned applications. It increases the efficiency of performance when we integrate this circuit with those applications. There are a number of components which are being used on this converter and we can discuss those component below:.

The following Fig. 1.5 shows the complete PCB structure of the converter which is under test.

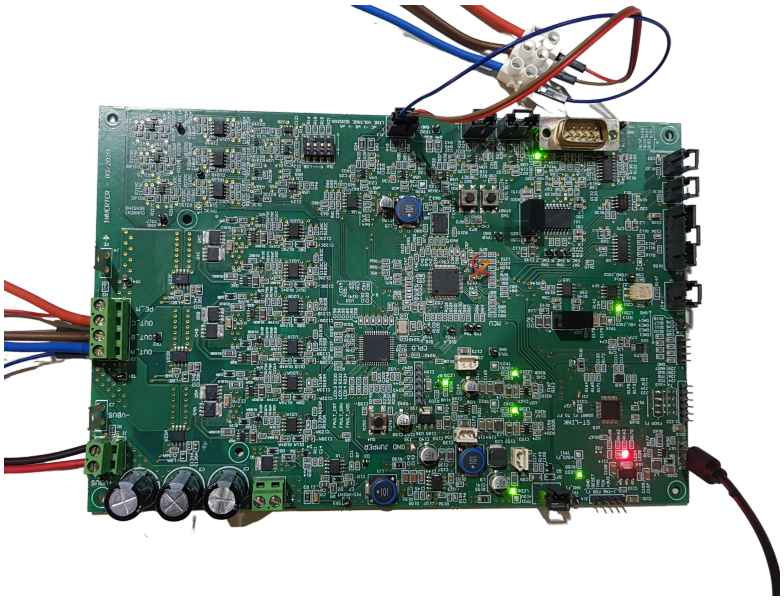

Figure 1.5: PCB Circuit

There are number of components which are being used on this converter and some of those components explained below and there are follow as:

1.4.2 Micro controller STM32

The central unit of any circuit is known as the "Micro-controller". This is an integrated circuit which is operated at 3.3 V, and can be programmed using various software. It is showing in the following Fig. 1.6 as where it is present on the printed Circuit Board (PCB).

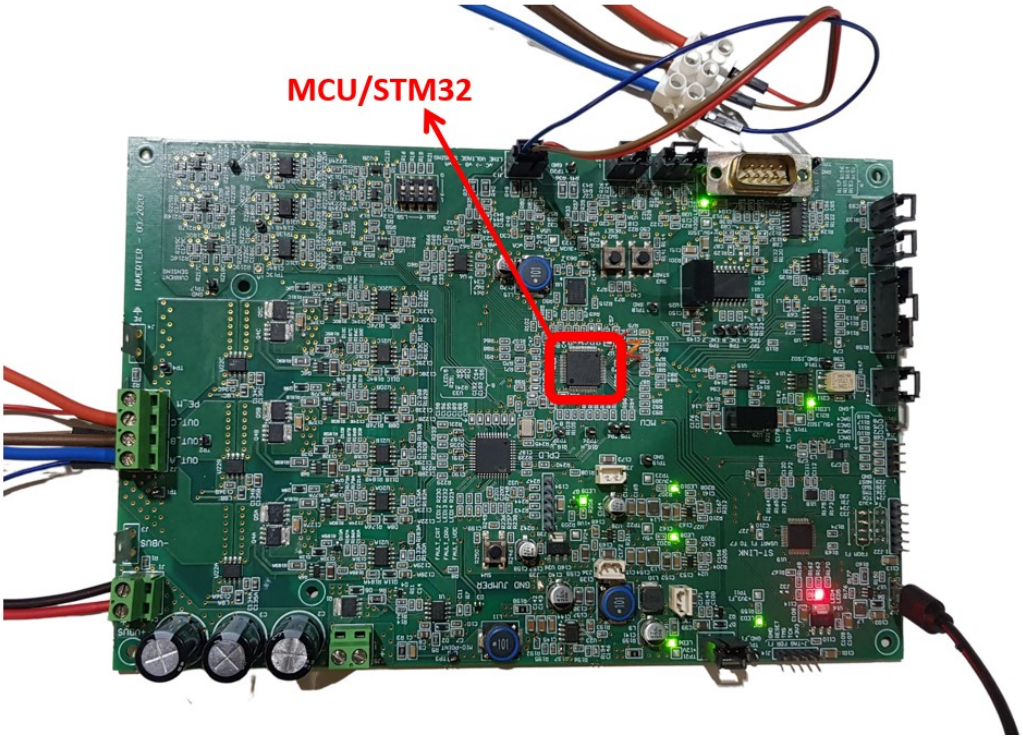

Figure 1.6: MCU STM32 on Converter

The chosen micro-controller is part of a family of 32-bit micro controllers, i.e. STM32. The STM32 micro-controllers are characterized by their excellent performance, as well as operation at minimal voltage, and availability of flexible management. The micro-controller used here is called STM32F703RE, which has been developed on the ARM Cortex M processors. Such micro-controllers have certain vital components. The essential parts of this type of micro-controller are following:

- First is the processor of the microcontroller, also called its CPU.
- A volatile memory, known as RAM is required for implementation of operations as well as calculations.

- Flash: non-volatile memory, contains program instructions.
  Several peripherals including:

- Timers: all digital operations are managed by one or more timers, which they synchronize the inputs (sampling and communication), the execution of the algorithm (calculations) and the execution of commands and monitoring signals (outputs). Furthermore, the timers they can also have the functionality of PWM modulators, generating the commands of the switch, starting from the desired duty cycles, according to the usual method of comparison with a triangular carrier. They can also be used as signals for encoders or as pulse counters

- 4. Analog to Digital Converters (ADC) are used, which have a general conversion time of 20 us. The resolution can be varied between 0 and 12 bit.

- CAN.

The micro-controller is programmed using a method called 'Host-Target programming', in which these are programmed using a PC. In such a case, the PC would correspond to the host, while the micro-controller would correspond to the board. Typically, C++ language can be used for programming purposes. Another code editor that could be used is the KEIL uVision. This consists of a compiler as well as a linker, which enables it to produce a code that could be generated on the micro-controller.

- Program memory (CODE), where the program instructions reside.

- Data memory (SRAM), volatile memory used for program execution.

- Device configuration registers and I/O port contents, described thereafter.

The micro-controller memory consists of 32-bit registers, which include the Program Memory (CODE). This is where the instructions of the program are stored. They also have the Data Memory (SRAM). This is the volatile memory which is utilized during execution of the program. Finally, the Device configuration registers are also present. The code of the machine's control and mapping routine is executed electric, is performed with a frequency of 10 kHz.

As mentioned above, the main peripherals of the micro-controller include the ADC converter, and timers. Now, there are 14 timers with the micro-controller. Out of these, two timers (TIM1 and TIM8) are known as advanced-control timers. TIM1 timers creates the PWM signals. These are sent over to the gate drivers. They then provide drive power for the mosfets. All timers have input as well as output channels, which are utilized in input appears, and hence judge the duration

of impulses of both input and output appears. This helps generate command output. The advantage of the advanced control timers is that they allow generation of complementary PWM commands with dead time insertion. Some of the main features of timers include:

- A 16-bit up down counter.
- A 16-bit pre-scalar. This programmable unit allows slowing the clock by up to 65536 times.
- Input and Output channels.
- PWM generation with saw-tooth (edge) or triangular (Center-aligned)
- Connection of multiple timers and synchronization of external signals.
- Generation of complementary three-phase PWM commands with dead-time, only for timers
- Presence of a repetition counter.
- Interrupt generation, if an underflow or overflow occurs during update event, or in case of a trigger event of a software. Interrupt can also be triggered in the event of input capture, or output appears.
- A compatibility with incremental encoders. Now, while each timer has registers, there are four major ones. These include the counter register, the auto-reload register, the repetition count register, and the pre-scalar register.

The execution of the program therefore consists in the sequential execution of instructions. However, the program execution sequence can be interrupted by a jump of address due to calling a subroutine. In real-time systems like this one case, this happens following an interrupt and the routine to be executed is indicated with Interrupt Service Routine (ISR).

1.4.3 CPLD

A Complex Programmable Logic Device, also known as CPLD, is a logic device which consists of macro-cells as well as totally programmable AND OR arrays. The CPLD is situated on PCB. Much like the micro-controller, the hardware of the CPLD can be configured using appropriate firmware. The CPLD comes into use for monitoring the system if any issue arises during the execution of the code by the microcontroller. The CPLD is used mostly in an educational context, and allows students the required protection in case a faulty programming code is used. In such

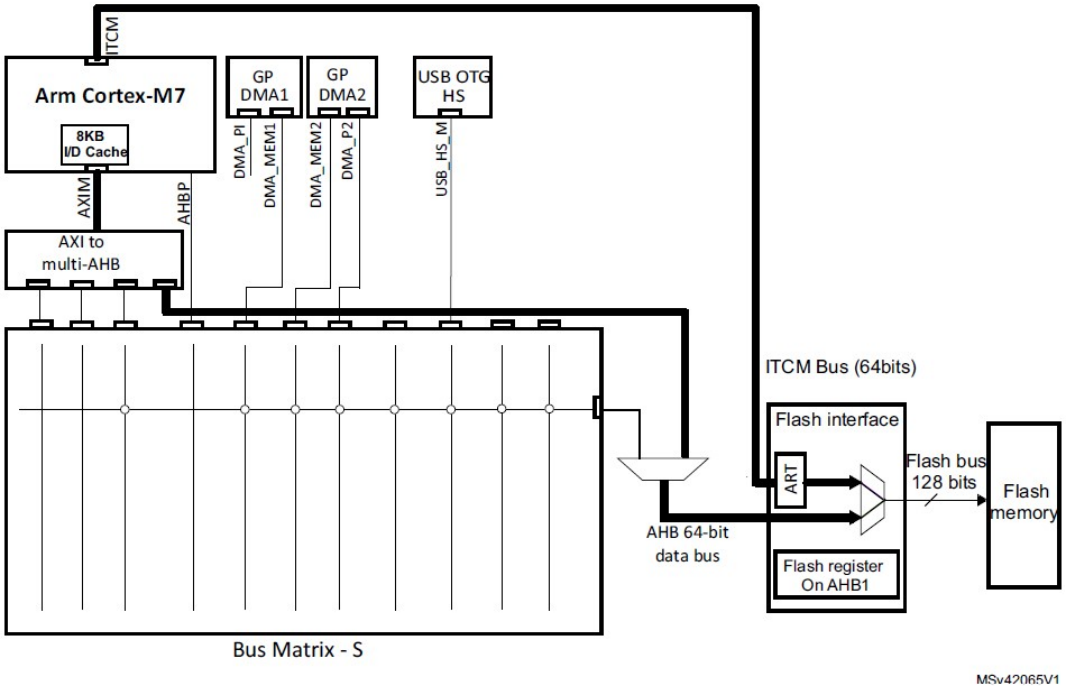

Figure 1.7: Flash Memory Interface Connection inside System Architecture

a case, the CPLD comes into play, and through activation of a special protection pin. This allows prevention of damage of the hardware due to implementation of incorrect programming.

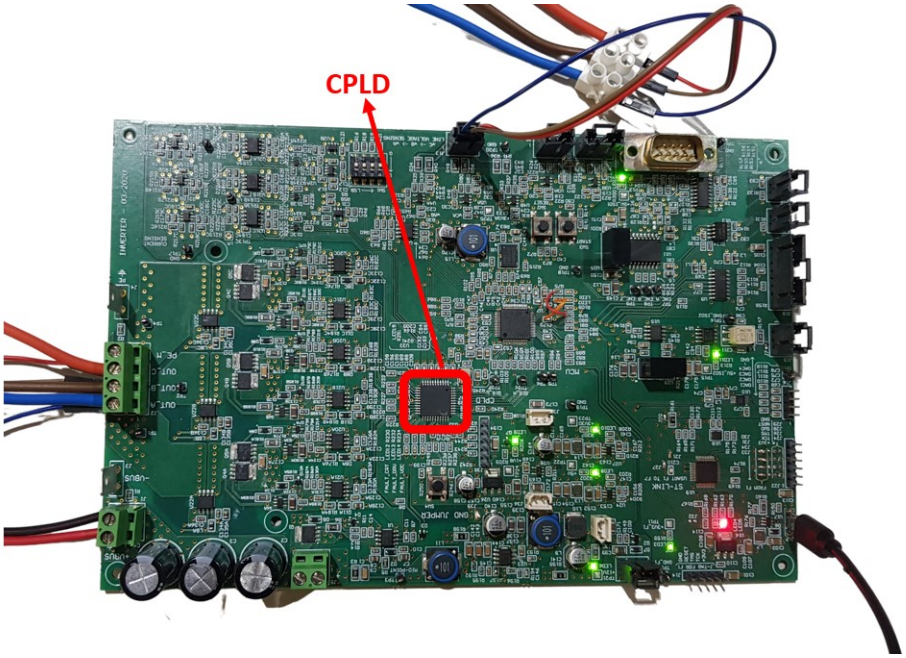

Figure 1.8: CPLD on PCB

1.4.4 Gate Drivers

Gate drivers are devices that amplify power, by receiving low power input from IC controller, and outputting the relevant high current gate drive which is required for a power drive. They are basically integrated circuits, which are used, in this scenario, to provide drive to the MOSFET's used with the PCB. The PCB contains a total of 7 drivers, which are provided by 12 V power. One of them would control the brake-leg MOSFET, while remaining 6 would control the 6 respective 3-phase inverter MOSFET's. The purpose of the brake leg in the system to prevent any occurring bus surges. In practical application, the power flow is reversed during slowing down of the motor. This results in an increased voltage difference at the DC link. This could cause damage to it if the voltage is too high. Therefore, if and when the voltage increases past the allowed limit, it is closed by the driver and the MOSFET's of the brake leg. Also, to prevent damaging components, some portion of the braking energy is used on external resistance. It may be noted that the command for closing may be initiated from either the micro-controller or the CPLD, both are valid.

The following Fig. 1.10 shows the placement of Gate Driver's on Converter.

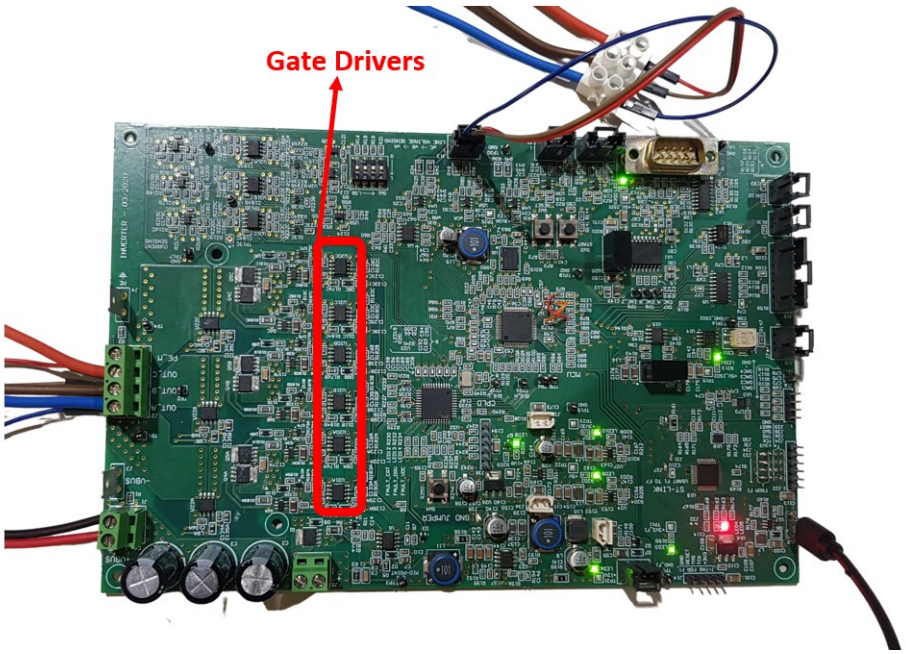

Figure 1.9: Gate Driver on Converter

The break leg closing command can come from both the micro-controller and by the CPLD. Each of these drivers has 8 pins, each of which is assigned to a specification function. Below is a schematic image of a driver, highlighting the functionality of each pin. The unsaturated pin is fundamental and has dual functionality. The first is that of making the MOSFET work on that area, on the voltage-current level, where it has a resistive behavior, far from the saturation zone, otherwise for currents high, too high voltages would occur and the component would burn, which would be lost too.

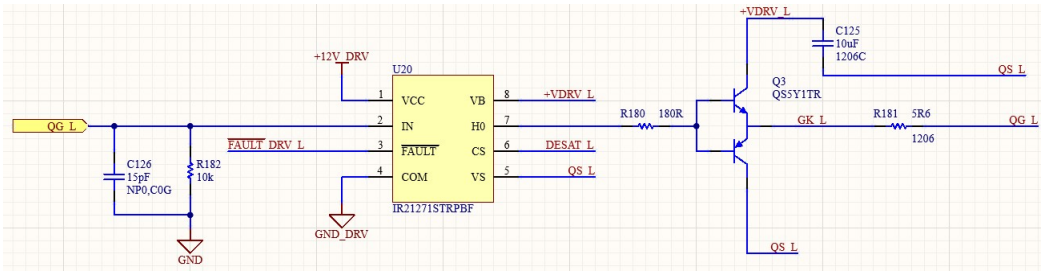

Figure 1.10: Gate Driver Control Architecture

In that area, you can end up there either because there is too much current and therefore the MOSFET is characterized by a characteristic on the volt-ampere plane in which at the point of work loses too much, or because the MOSFET is badly

driven, for example because the bootstrap capability has discharged and I would go to apply a drive voltage lower, which would mean that with the same current, the voltage across the device is shifts more towards the saturation zone, compared to that for correct piloting. Of Consequently, the protection of the unsaturated pin must be incurred.

On the data-sheet of the MOSFET there is an estimate of its resistance value in a determined temperature range, the unsaturated pins detect the voltage across the MOSFET, for which an estimate of the current flowing through the device can be traced back, if too high, the driver commands the OFF state and the passage of current is prevented in the device.

An important aspect of the unsaturated pin is that of the analog circuit that characterizes it: the voltage on the MOSFET depends on its state, ie. conduction. Taking the high side MOSFET as a reference, when it is open, the de-saturation pin would have all the bus voltage, V_bus, in our case 48V, whereby we condition the signal using a diode, in order to prevent the voltage of the bus arrives on the driver pin, which is a signal pin. The two top diodes, take care instead of preventing the voltages from going beyond the 0-12 V range. The analog circuit just explained is the following.

Another fundamental utility of the unsaturated pin is the protection guarantee, when the current sensors, due to band problems, do not intervene. The sensors of in fact, they have a limited bandwidth. In the event that faults occur, and the currents rise suddenly (short of leg or phase-to-phase short) the current sensors would not be able to detect them, for which the unsaturated protection would intervene again, which it generally protects from current peaks, not due to a thermal fault pin which comes from the micro-controller. When the 3.3 V comes from the micro-controller at that pin, the input rises to 12 V and is communicated at the output with the following circuit analog, between pin V_B and pin V_S.

If the driver goes into fault it is necessary to communicate it out to the CPLD and then to the micro controller, closing with an open drain.The fault is denied, when in fault they are 0 V present, when no 3.3 V is present.

1.4.5 MOSFET's

The switches that have been used for modulation and consequent regulation of the average value of the motor power supply voltage are the MOSFET's, two for each leg, and an additional one placed on the brake leg, to avoid damage of the DC link, in case of braking by the motor. They are controlled by the drivers, which through the DC capacitors apply a voltage of 12 V between gate and source, commanding its conduction, or a zero voltage, resulting in its interdiction. [**IEEEexample:article_typical**]

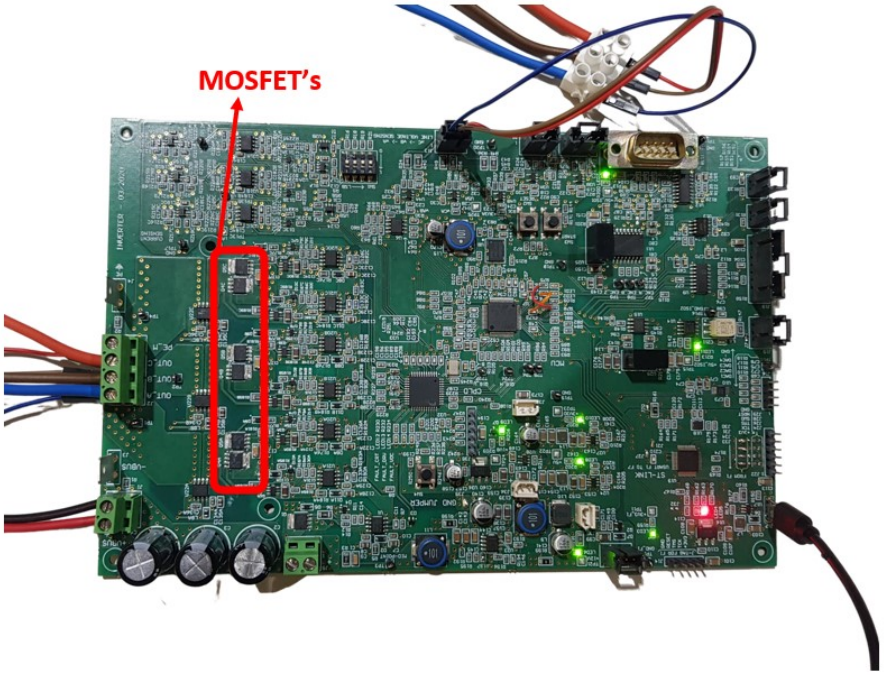

Figure 1.11: MOSFET's placement on Converter

Chapter 2

Preliminary Tests on Converter

2.1 PWM Control of Converter

Now in order to generate PWM, our converter is become the source and our transformer act as an inductive load. We give 5V to the micro-controller which is on the converter which provide us the 12V PWM at the output of the converter. In the normal case our converter behave as the rectifier, but we want to generate PWM from the converter board.

Our load is Y-connected 3 phase inductor transformer. The current loop make sure that the output voltage remain constant which is done by the micro-controller. We are using constant voltage topology, in which we have a value of the voltage but the value of current is zero. In our preliminary test on the converter the output current was zero but have a constant voltage there.

2.2 Execution of Finite State Machine on Micro-controller

We can design logical connection by utilizing the Finite State Machine (FSM) which basically execute the mathematical expressions. Electronic design mostly used this type of machines to implement their model. It consists of finite number of state and transition between each state is run in such a way when desire condition is met. FSM start with the start state and then went to other states depending upon the inputs and finally reach its ending state. The following model is followed by FSM shown in the Fig. 2.1 below.

The micro-controller STM32 is being used for the implementation of FSM

irrespective of using CPLD for the following reason:

- Micro-controller performance increases exponentially.
- Cost of such micro-controllers are very less.

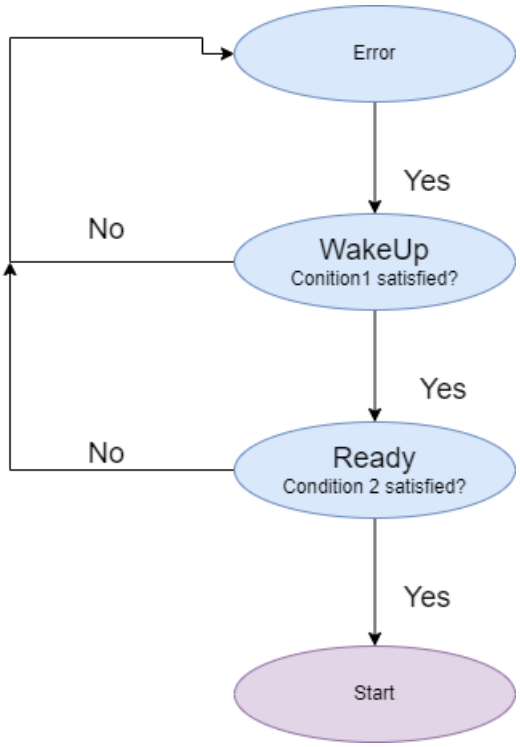

Figure 2.1: Finite State Machine Implementation Loop

These micro-controllers are very easy to use with FSM and are low power devices with many input peripheral's. There are many advantages of using software based Finite State machines which are follow as:

- Flexibility: When we implement Finite State on a micro-controller, it will give us the leverage of changing the design at any time during the project cycle. If we implement FSM on hardware side, the behavior of FSM can be change when the circuit is produced. If we have to change anything, we would have to redesign the circuit again. So this facility to executed the FSM on micro-controller help us to change the design according to our requirement at any time.
- Error Detection: Micro-controller software development environment helps us to debug the error in our FSM easily. For instance, you can use break point

in the software to check every step of code in the micro-controller which help you to debug your error very easily.

- Capability of software control FSM: One of the major advantage of using software FSM is that we can manage the complicate sequential problem very easily because it helps us to debug every error line by line using the breakpoints. We can also use the multiple peripherals for the micro-controller design so that our FSM design can handle multiple I/O operation as well.

In recent times, the use of finite machines with the micro-controller is usual industrial approach in coding, although there use is beyond the scope of coding. These are now used in-order to rectify bugs, to prevent indefinite loops and especially for the ease of debugging. The first state in which the control enters by default at startup is that of error. In this state the inverter outputs are disabled and all the control variables are initialized.

The error state is entered when the micro-controller is turned on or reset, or when something abnormal occurs during the check routine, which can produces the larges amount of current which damages the hardware circuits and devices.

In this Finite state machine I have used 4 major states which are Error, Wake-up, Ready and Start states. Using these four states I can get my desire outcome. Next, the state START, where the machine control code is executed.

2.3 LCL Filter Design Analysis

In the last decade, the demand of energy is escalating day by day and its result in more depletion of overall fossil fuels. As the world is supporting the cause of using renewable energy due to environmental concern as well. The use of power converter is increasing day by day due to growth in renewable energy resources especially wind and solar. We want extract maximum energy from these two sources and also interfacing these sources with our power grid lines. In the connection of a power converter with power grid lines the LCL plays a very vital role in it.[4]

Grid code play an important role in the making of small, medium, and large wind turbines designs. These grid codes vary from one country to another counter which make it difficult for the vendor to select an optimum grid codes for the wind turbine. Due to variations of these grid codes, when we try to integrate wind energy with power grids LCL plays an important role to control and mitigate the harmonics and oscillations in the voltage and current.

LCL filter plays an important role in the mitigation of oscillations, less costly and give us the high quality of power. Now a day, LCL filter is becoming the main requirement for grid-connected converter and rectifiers to use it mainly to control the current and voltage mitigation's which is injected in the grid lines. It is

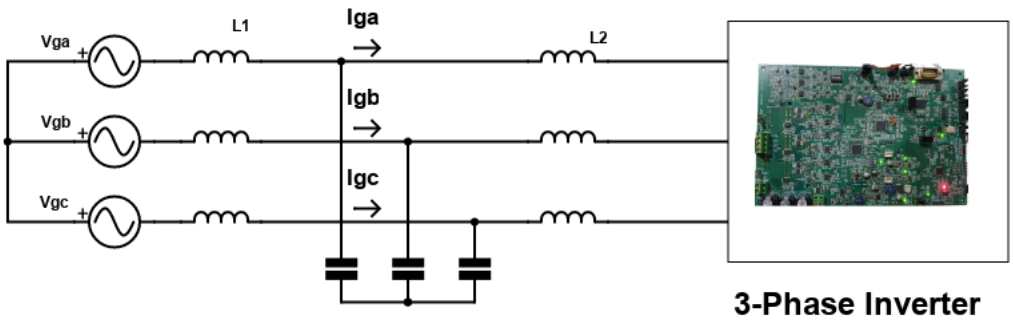

Figure 2.2: LCL Filter Configuration with Grid and Converter

very cost-effective and we can simply use small values of capacitor and inductor to control power of hundreds of kW. In order to calculate the efficient working LCL filter we have to design an appropriate mathematical model to calculate the values of capacitor and inductor.

The following Fig. 2.3 shows the per-phase model of LCL Filter

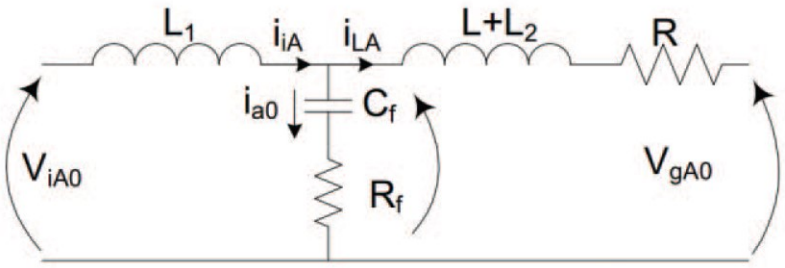

Figure 2.3: Per-Phase Configuration of LCL Filter [4]

The values of the capacitor and inductors can be calculated by the following formulas:

$$Z_b = \frac{{E_n}^2}{P_n} \tag{2.1}$$

$$C_b = \frac{1}{\omega_n Z_b} \tag{2.2}$$

$$L_{inv-side} = \frac{V_{DC}}{6 f_{sw} \triangle I_{Lmax}} \tag{2.3}$$

while the I_{Lmax} would be:

$$I_{max} = \frac{P_n\sqrt{2}}{3V_{ph}} \tag{2.4}$$

$$L_{grid_side} = \frac{\sqrt{\frac{1}{K_a^2}} + 1}{\omega_{sw}^2 C_f} \tag{2.5}$$

$$R_f = \frac{1}{3\omega_{res}C_f} \tag{2.6}$$

While according to the configuration of $\triangle - Y$ configuration,

$$R_{f_\Delta} = 3R_{f_Y} \tag{2.7}$$

$$C_{f_\Delta} = \frac{C_{f_Y}}{3} \tag{2.8}$$

After calculating all the parameters, make sure that the resonant frequency should fulfill the following rule.

$$10f_g < f_{res} < 0.5f_{sw} \tag{2.9}$$

if it is not satisfying then the components should be chose again.

2.3.1 Software Modelling

The LCL filter was being designed in MATLAB program using the formulas discussed above in equations at the base frequency of 10kHz and below are the real event values.

LCL Filter Parameters		
Converter's Nominal Data		
Converter Rated Power (W)	P_n	720 W
Switching Frequency (Hz)	f_{sw}	10 kHz
DC-Link Voltage	V_{dc}	48 V
Converter's Bandwidth Frequency	f_{bw}	1000 Hz
Switching Frequency (rad/sec)	f_{sw}	$2\pi f_{sw}$
Grid Frequency	f_g	50 Hz
Design Constraints		
Reactive Power w.r.t Grid Power (4%)	β	0.04
Inverter Side Ripple (pk-pk)	$\triangle I_{inv}$	0.1
Grid Side Ripple (pk-pk)	$\triangle I_g$	0.02
LCL Filter Parameters		
Capacitance Filter (5%)	C_f	106.1μF
Inverter Side Inductance	L_{inv}	979.6 μH
Grid Side Inductance	L_{grid}	14.3 μH
Resonant Frequency	f_{res}	4112 Hz
Damping Resistor	R_f	0.12 Ω
$\triangle - Y$ **Parameters**		
$\triangle$ Configuration Resistor	$R_{f\triangle}$	0.36Ω
$\triangle$ Configuration Capacitor	$C_{f\triangle}$	35.4μF

Table 2.1: MATLAB based LCL Filter Specifications

2.4 Converter Configuration with Grid

The connection of renewable energy source with the grid line is implemented through a power converter. Power converter make sure to provide the high quality of power to the grid lines. In the figure below you can see a three phase converter that is connected to the grid lines through C_f and L_f and inductor and capacitor of filter. In the figure we represent equivalent grid resistance and inductance with R_g and L_g. We assume that DC source is an ideal and have the ability to decouple AC and DC sides. But the smoothing capacitor is also included in it.

Mostly, the grid connected converter are three phase devices that are utilizing the semiconductor power switches which can turn on and off itself from the pulse width modulation (PWM) which can turn on one switch for small duration and others will be off and this is how it works. Power converter convert the source energy into the AC frequency voltage and current.

Ac grid fundamental changes when we used different topology converters like source-side, load-side and bus-side converter. For instance, in a grid where we're using power transformer, synchronous generator and capacitor bank we often utilized grid-side power converter. It response under steady state and transient state is different from other converter and it will suite our design procedure.

The transformer that we used in our topology have a primary side voltage of 220V and secondary side voltage of 24V and these both value are in RMS. We can find the peak values using the formula below,

$$V_{peak} = \frac{V_{rms}}{\sqrt{2}} \tag{2.10}$$

The configuration of transformers behaving as a Grid is shown in Fig. 2.4 below:

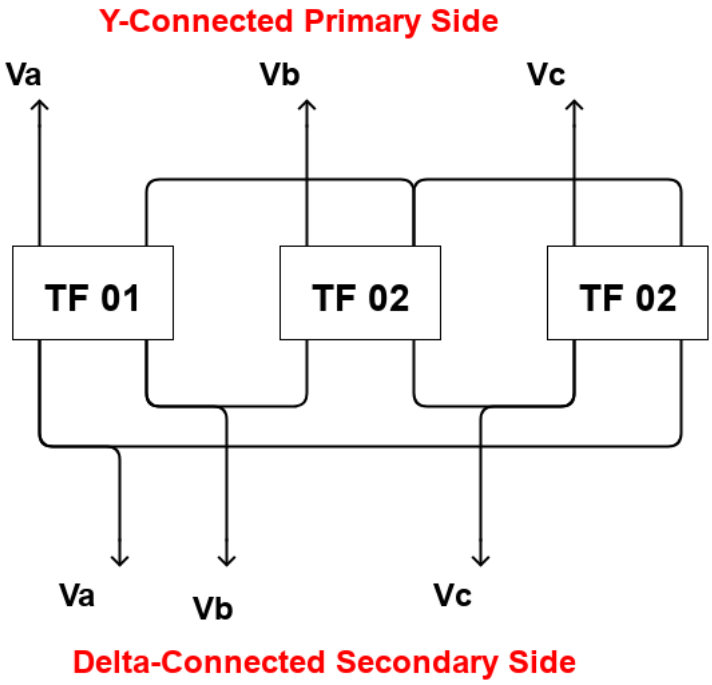

Figure 2.4: Transformer's Y-△ Configuration as a Grid

The peak values of these two side of transformer will become 269V on the primary side and 34V on the secondary side of the transformer. The primary side of the transformer is coming from the main grid lines and it is Y-configuration and secondary side is coming from our -energy source which is in Δ-configuration. The three lines voltage coming from our energy source are going directly to the

converter which will integrate our energy source voltage to the main grid. The grid frequency is running on 50Hz.

2.4.1 Calculation of Grid Impedance

In order to calculate the grid impedance we have two transformer one is a tap changer and other one is grid transformers and we perform two test one is the open circuit test and other one is short circuit test and there are discussed below:

Open Circuit Test

When we have to perform the open circuit test, the secondary side load is removed and it is open and we connect ammeter in series to low voltage side and similarly connect the voltmeter in parallel to the low voltage side which is shown in the figure below:

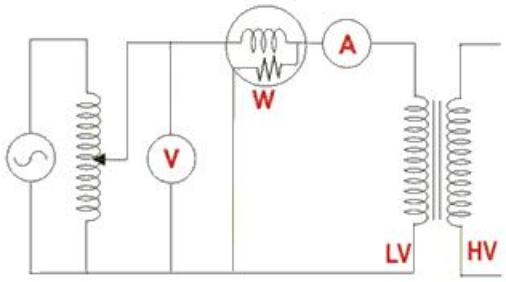

Figure 2.5: Open-Circuit Test Configuration

Now the high voltage secondary side is open and we will increase the primary side voltage slowly until it reaches the rate voltage which we can check from the voltmeter connected to the primary side. When it reaches it's maximum rated voltage we record all the values of the ammeter, voltmeter and watt-meter. We utilized following equations to find the respective parameters of transformer.

$$P_{out} = \frac{V_1}{R_m} \tag{2.11}$$

The impedance of the transformer will become

$$Z_m = \frac{V_1}{I_e} \tag{2.12}$$

We can then easily find the shunt reactance using

$$\frac{(1)}{(X_m)^2} = \frac{(1)}{(Z_m)^2} - \frac{(1)}{(R_m)^2} \tag{2.13}$$

After we calculate these values we can easily refer this to the HV side of the transformer using the transformer ratio. So open test is performed to find the core losses in the transformer and find out the values of the shunt reactance and impedance.

Short Circuit Test

Now we will perform the short circuit test on the transformer in which we connect ammeter in series and voltage in parallel to high side of the transformer. We short circuit the low voltage side of the transformer. We increase the voltage zero to rated slowly and when current reaches to maximum value we records all the values of the transformer.

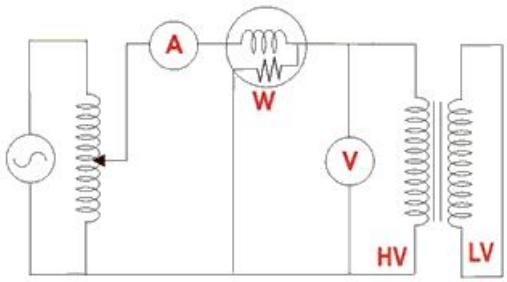

Figure 2.6: Short-Circuit Test Configuration

Let us now we consider the watt-meter reading where P_{sc} is

$$P_{sc} = R_e I_L \tag{2.14}$$

Similarly, the equivalent impedance of the transformer can be found using

$$P_e = \frac{V_{sc}}{I_L} \tag{2.15}$$

Therefore the equivalent resistance can be found by

$$X_e^2 = Z_e^2 - R_e^2 \tag{2.16}$$

2.4.2 Test-Case for Short-Circuit Test

We utilized the above formula's to determine the values of primary and secondary side voltages, currents and impedance's. Here in these test cases we use two transformer one was a tap change transformer and other one was grid transformer and we then perform the short circuit test to find the grid impedance. Here in the

Transformer's Parameters	
Parameter	**Value**
Primary Side Voltage	220 V
Secondary Side Voltage	24 V
Apparent Power	500 VA
Frequency	50 Hz
Primary Side Current (max)	2.272 Amps
Secondary Side Current (max)	20.83 Amps

Table 2.2: Under-Test Transformer's Parameters

test-cases we test four different transformer to check our results and we observe following result extracted.

The transformer with the above mentioned parameters is connected with the tap-changing transformer to perform the short-circuit test in the following configuration.

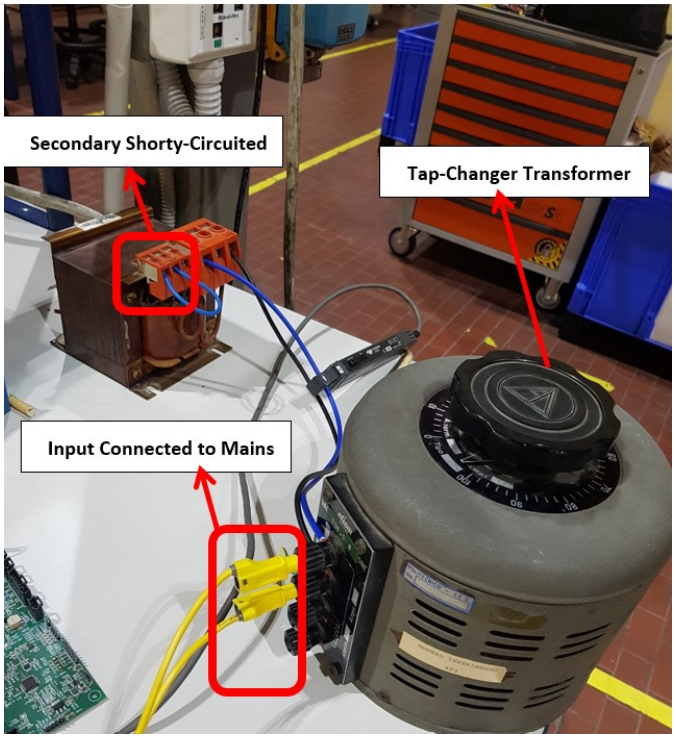

Figure 2.7: Short-Circuit Test Configuration with Tap-Changing Transformer

The following four tests are being deployed on transformer and obtained the following results on oscilloscope through current probes.

Test 01

Voltage is leading current by the phase angle of 7.03°
V = 540mV
A= 9.08A

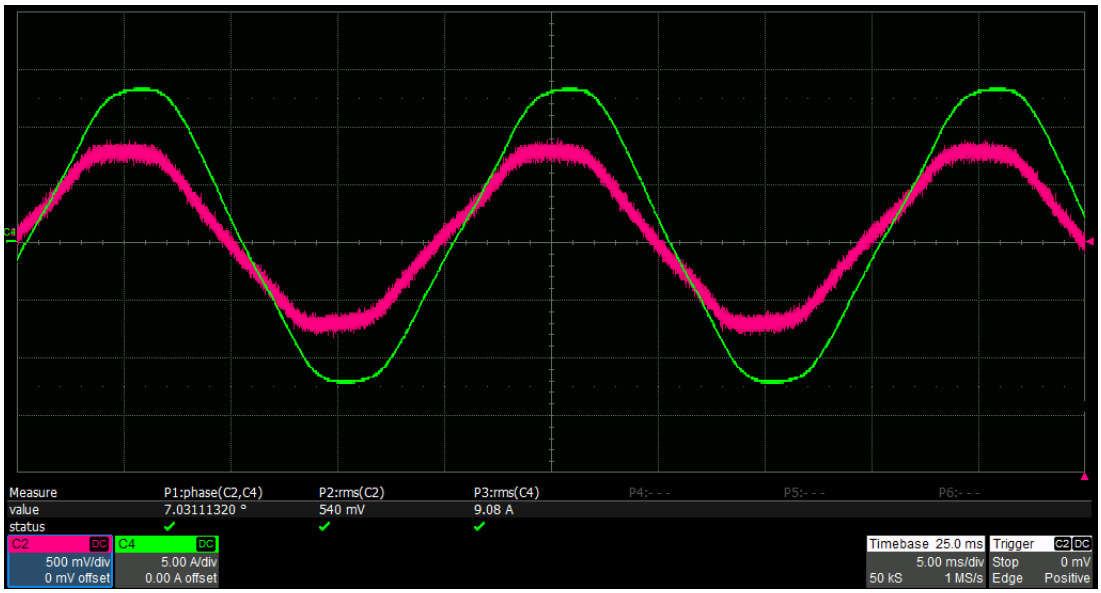

Figure 2.8: Test 01 Result on Oscilloscope

Test 2

In the test 2 the voltage is leading the current by a phase angle of 10.019°
V=532mV
A=8.97A

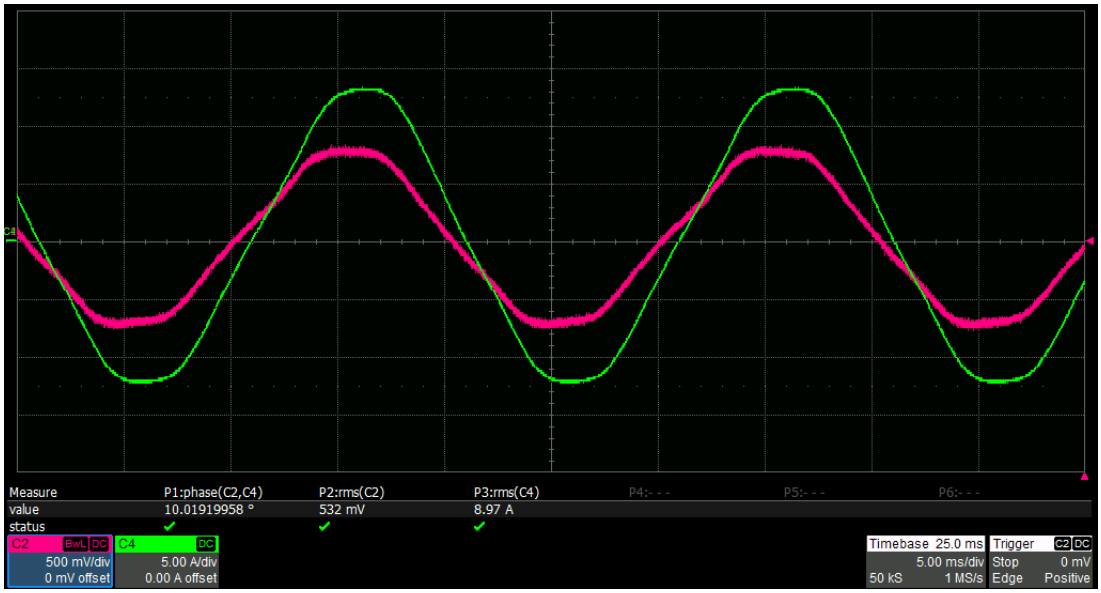

Figure 2.9: Test 02 Result on Oscilloscope

Test 3

In the test 3 the voltage is leading the current by a phase angle of 10.21°
V=536mV
A=9.03A

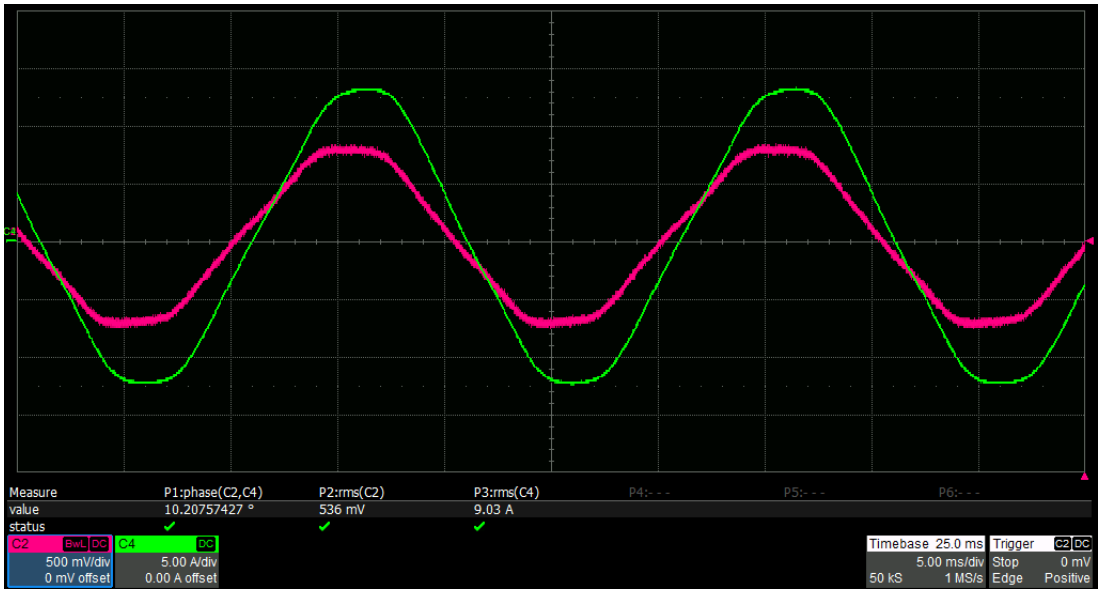

Figure 2.10: Test 03 Result on Oscilloscope

Test 4

In the test 4 the voltage is leading the current by a phase angle of 10.21°
V=752mV
A=12.58A

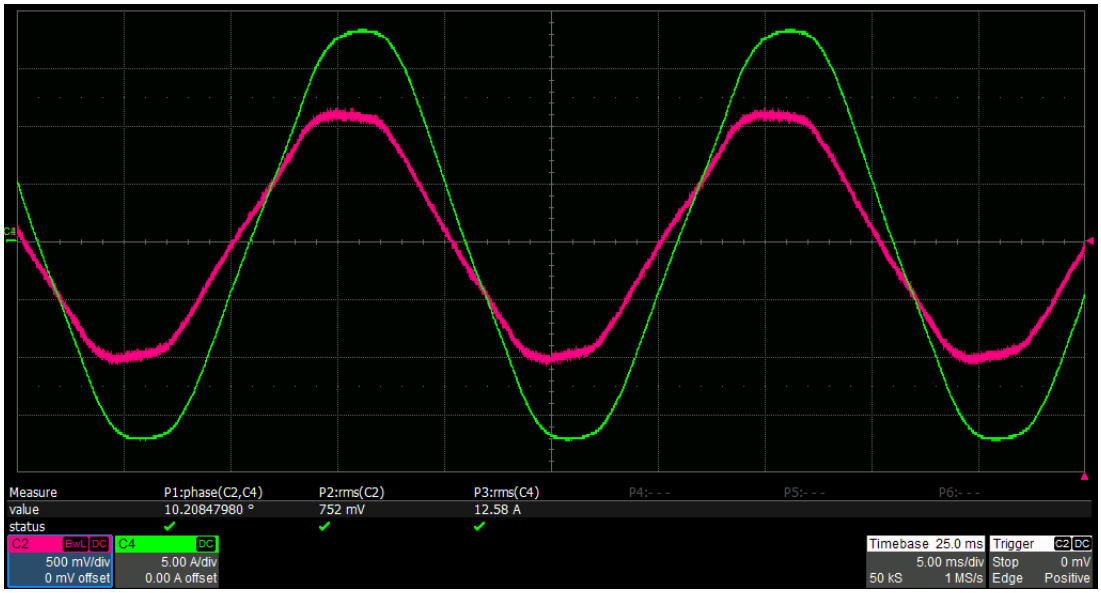

Figure 2.11: Test 04 Result on Oscilloscope

The following table shows the complete results of the test performed on transformer during experiment.

Test Cases Results			
$\mathbf{I}_{SC}$ (Amps)	$\mathbf{V}_{SC}$ (mVolts)	θ_{SC}**(degree)**	θ_{SC}**(rad)**
9.08 A	540 mV	7.03°	0.12269 rad
8.97 A	532mV	10.019°	0.17486 rad
9.03 A	536mV	10.21°	0.17819 rad
12.58 A	752mV	10.21°	0.17819 rad

Table 2.3: Short-Circuit Test Results

Average Values:
$I_{SC} = 9.915A$
$V_{sc} = 590mV$
$\Theta_{sc}(rad) = 0.1634825$ rad

Grid Impedance Calculations

$$S = VA = 590mV * 9.915 \tag{2.17}$$

$$S = 5.84985VA \tag{2.18}$$

$$P = S\cos\theta = 5.84985 * cos(0.1634825) \tag{2.19}$$

$$P = 5.7718W \tag{2.20}$$

$$Q = S\sin\theta = 5.84985 * sin(0.1634825) \tag{2.21}$$

$$Q = 0.9521VAR \tag{2.22}$$

$$R_g = \frac{P}{(I_{sc}^2)} \tag{2.23}$$

$$R_g = 58.71m\Omega \tag{2.24}$$

$$X_I = \frac{Q}{(I_{sc}^2)} \tag{2.25}$$

$$X_I = 9.684m\Omega \tag{2.26}$$

$$L_g = \frac{X_s}{(2\pi 50)} \tag{2.27}$$

$$L_g = 33\mu H \tag{2.28}$$

Hence, the Grid Impedance (R_g & L_g) is obtained through the short-circuit test.

Chapter 3

Converter Model and Control Scheme

3.1 General Converter Structure

In general a converter is made up of multiple stages connected in series with each other, which all regulates the conversion process smooth. It ensures high efficiency in order to reduce losses. Hence, the following figure 3.1 depicts the general working of a converter. It shows that, it starts by AC/DC conversion stage, (AFE) connected to a capacitive DC-link that allows the connection to the battery/load mediated by a DC/DC converter.

Figure 3.1: General Converter Structure

The DC/DC stage provides:

- Galvanic isolation between AC grid and battery through AFE stage and then DC-Link.
- Voltage level adaptation, according to application.
- Control of the charging power and battery current.
- On-Board Battery Charger.
  This term is based on the position of the charger with respect to the vehicle

and it depends on the power of the converter. If the mains are single-phase or three-phase, and having low power, the battery charger consider to be on-board, because of its small size and easy to install in vehicle.

3.1.1 Active Front End

The stage of the power converter which allows the conversion from alternating current to direct current (AC/DC), is called Active Front End (AFE).

This term (AFE) represents the basic structure of a converter which performs the AC/DC conversion, which is basically consisted of an active rectifier or Power Factor Corrector (PFC), which is composed of controlled transistors (MOSFET, IGBT) through MCU, Instead of using un-controlled diodes. Beside this, being an power converter application which interfaces with the mains, the basic power quality standards for the grid connected converters (e.g. CEI EN 61851 for EV's) should meet, specifically the Total Harmonic Distortion (THD) factor, which must not exceed the 5% and also the Low reactive power (PF>0.95) .Moreover, in this test case which is taken into account, which considers On-board Battery Charger (OBC) or Grid-Connected Converter, the adapted regulation technique for the switching of power MOSFET's, it is Pulse Width Modulation (PWM).

The following block diagram figure 3.2 gives an overview on the AFE structure.

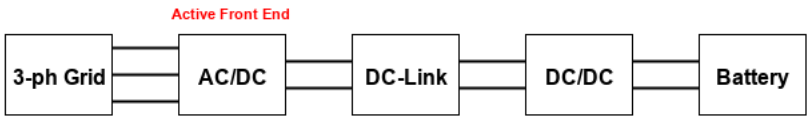

Figure 3.2: Converter Block Scheme with AFE

The most of the grid-connected converter or OBC's are composed by a grid side AC/DC rectifier. So, the main object of this converter, is an Active Front End (AFE), of this Two-Levels, three phase converter. And represents the AC/DC stage of the grid connected converter in the above figure 3.2.

The basic role of the AC/DC rectifier is to:

- Ensure sinusoidal grid current with unitary power factor, in the meantime by following the grid standards in terms of total harmonic distortion (THD) and and its respective reactive power.

- And also make sure to provide a stable DC voltage to fed the DC/DC stage through DC-Link.

Stand Alone OBC

The typical OBC can be designed for single or three phase main input. The AFE and the DC/DC can be unidirectional (G2V) or bidirectional (V2G).A power converter will be defined as uni-directional if it allows the flow of energy in one direction only. Which means that as for battery charger that the power direction goes from the grid to the battery (G2V). However, if we modify the design of the converter, by agreeing the increase in complexity and as well as in the cost, it is possible to design a bidirectional structure Fig.3.3, which allows the flow of energy in both directions, even from the Vehicle to the Grid (V2G). But in this scenario it is important to care about the battery degradation which is generated by frequent charge and discharge cycles.

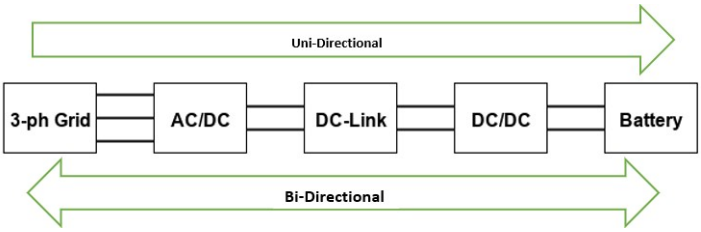

Figure 3.3: Complete Hardware Setup

3.2 Topology under Test

The adopted topology for grid-connected converter is consist of:

- Grid-side converter: a two level three phase inverter.
- Load-side converter: a bidirectional DC/DC converter.

The considered topology is bidirectional, hence it could show both an active rectifier,i.e, Grid to Vehicle (G2V), or a converter for generation purpose, i.e, Vehicle to Grid (V2G). In fact, the load side converter (DC/DC) is controlled as a current generator which imposes either as a load operation, i.e, for an instance a battery charge. In this the load/battery voltage is considered as variable load. While the other scenario is it behave as a generation operation, in which the load/battery voltage is considered as variable source. In both cases it is considered as variable voltage, which must be keep below than than DC-link voltage set point in order to permit the correct operation.

The load side converter is actually a step up (boost) converter behaving as current controlled boost rectifier, it ensures the current regulation on the load side. This produces a disturbance on the DC-link capacitor, whose voltage is kept

constant by the three-phase inverter. Thus on the load side the power regulation is achieved and the inverter follows the requested power indirectly by controlling the voltage on the DC-link capacitor.

In order to meet the power quality standards for electrical energy distributors, an LCL filter is added at the grid side. This filter decreases the current and voltage switching harmonics.

The following figure 3.4 shows the general block diagram of complete architecture.

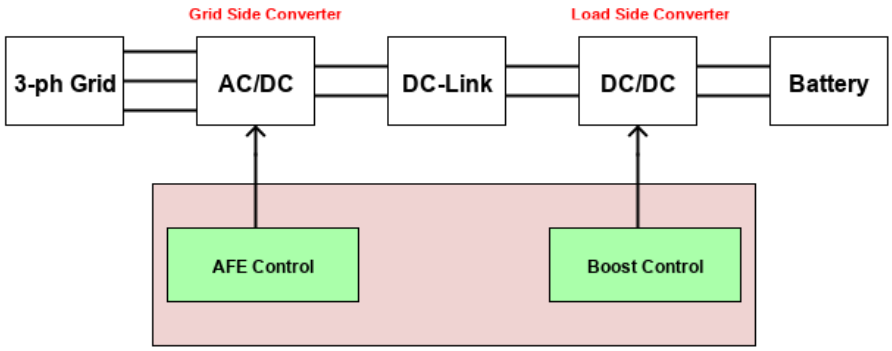

Figure 3.4: Block Diagram of Complete System

The three-phase bidirectional AFE architecture is consists of two instantaneous modulation levels and current independent phase voltage formation. It uses six controlled switches (MOSFET's). The semiconductors are then subjected to the full DC-link voltage. The following figure 3.5 represents the Two-Level, Three-Phase Converter topology which is under test.

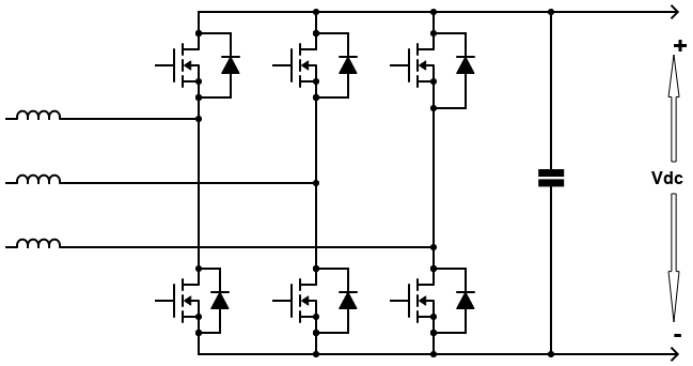

Figure 3.5: 2 Levels Three-Phase Converter Topology

3.2.1 Converter's Main Specifications

The following table 3.1 shows the main specifications of this converter.
The rated power of the converter, which has been tested in experiment can be

Converter's main Parameters		
Grid Data		
Grid Phase Voltage (RMS)	$V_{g,RMS}$	24 V_{RMS}
Grid Frequency	f_g	50 Hz
Impedance of Grid		
Grid Resistance	R_g	59 mΩ
Grid Inductance	L_g	34 μH
DC Link		
DC-Link Capacitor	C_{dc}	990 μF
DC-Link Set Point	$V_{dc,ref}$	48V
Boost		
Bost Inductor	L_{DC}	102 μH
Switching Data of Converter		
Switching Frequency	f_{SW}	10 kHz
Switching Timing	T_{SW}	100 μsec
MOSFET's Parameters		
MOSFET Type	N-Channel	Enhanced Mode
Drain-Source Voltage	V_{DS}	100 Vc
MOSFET On-Resistance	R_{DS-on}	11 mΩ
Drain Current	I_D	82 A
Diode Voltage Drop	V_{SD}	0.82 V
Converter's Rating		
Output Power	S_{AC}	0.320 kVA
Load's Data		
Load DC Voltage	V_{Load}	48 V

Table 3.1: Converter's Specifications

assumed to 0.320 kVA, which is suitable for On-board Battery Chargers (OBC) for electric vehicles. While on the connection side (grid), hence it is a 24 $V_{g,RMS}$ phase voltage system. This choice leads us to find the maximum input phase AC current which can be calculated as:

$$\hat{I}_{AC,in} = \frac{2}{3} \times \frac{S}{\hat{V}_{ph}} \tag{3.1}$$

Where:

- $\hat{I}_{AC,in}$: Input phase AC current (Peak).
- S: Apparent Power (VA).
- $\hat{V}_{ph}$: Phase Peak Voltage (V_{pk}).

3.2.2 Converter's Configuration with Grid

The existence of power electronic semiconductor in the grid-tied converter, featuring as the switching device plays an vital role in this field. So, their basic structure should be very compatible to our requirement and much efficient. With aim of the constant DC-link voltage and the unity power factor, the topology which is under test for the three-phase grid-tied converter, the basic configuration is shown in figure 3.2 below. Where the six MOSFETS's are switching according to the commands generated by AFE.

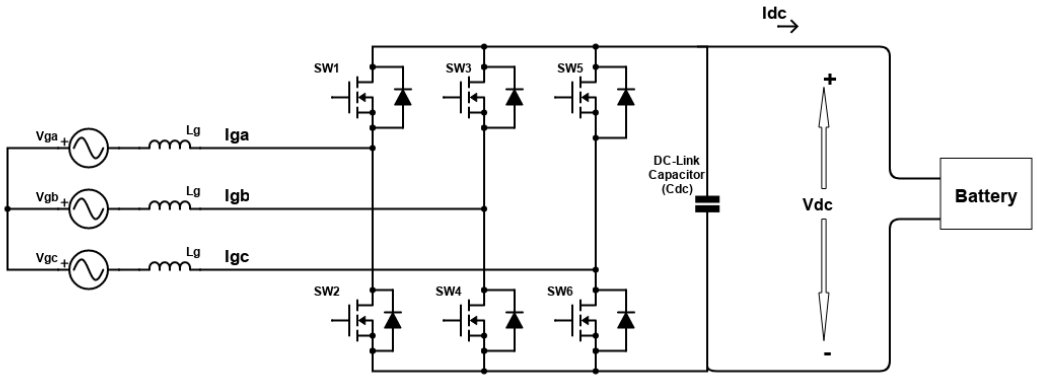

Figure 3.6: Structure of 3-phase Grid-Connected Converter

3.3 Converter Control Scheme

In technical literature the converters control strategies are mostly similar. The most adapted control scheme for converters is a cascaded control strategy with having two loops. (An Inner-grid current control with nested loops and an outer DC-link voltage control). While for the synchronization with grid, a PLL (phased-locked loop) technique is used which monitors the synchronization of converter with the grid voltage. Fig. 3.7 represents an idea on the of the adopted control scheme.

As it can be notice that the outer voltage control loop maintains the voltage on the DC-Link capacitor v_{dc} constant and equals to reference v_{dc}*. This outer loop

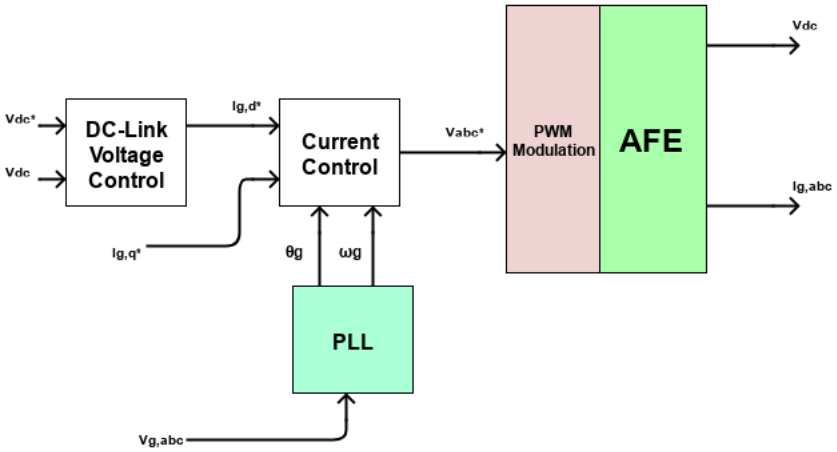

Figure 3.7: Converter Control Overview

measures the necessary output current and sends it as a reference for the current control on the d-axis.

The current control loop is basically applied in the rotating reference frame (d,q), where the d-axis is coincides with the voltage vector angle. In the three phase system when balanced sinusoidal wave forms are present, the rotational speed and the module of the grid voltage vector remains constant with equal frequency, amplitude, and relative phase shifting angle. On the basis of these ideal operating conditions, the voltage vector represents a circular locus on a Cartesian plane, generally known as the $\alpha\beta$ plane.

The Figure 3.8 shoes the three phase voltage vector under ideal operating conditions.[3]

The vector equations for this three phase system can be shown as:

$$V_{abc} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = V \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - 2\pi/3) \\ cos(\omega t + 2\pi/3) \end{bmatrix} \tag{3.2}$$

$$|V| = \sqrt{v_a^2 + v_b^2 + v_c^2} = \sqrt{\frac{3}{2}} V \tag{3.3}$$

So, it is quite possible to obtain the null steady state average error from the rotation of this reference frame. The current control strategy receives the reference inputs from two axis. First one, on the d-axis, and other on the q-axis. The prior one measures the injected active power towards the grid, while the last one to measure the reactive power.

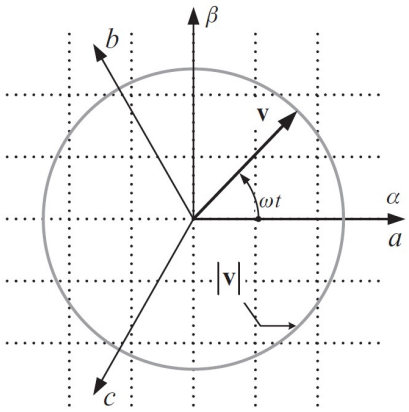

Figure 3.8: 3-Phase Voltage Vector under Ideal conditions

The Figure 3.9 shows the dq-axis on the 3-phase voltage vector reference plane.

Thus to reach reach the references level the complete control measures the required duty cycles.

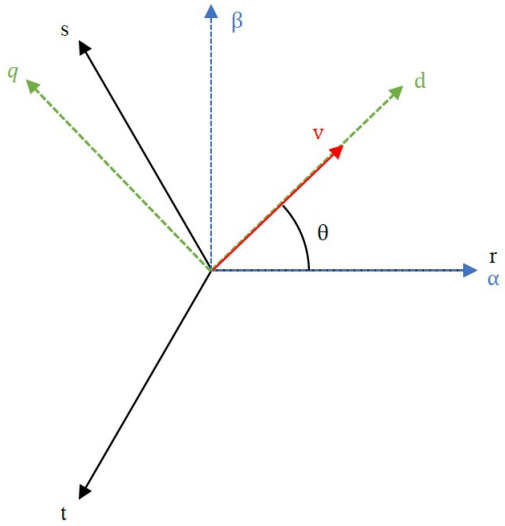

Figure 3.9: Positioning of the dq-axis on Rotating Reference Frames. [3]

3.4 Grid Synchronization in Three-Phase Power Converters

In the control of grid-tied power converter the most important key factor which can never be neglect is the proper synchronization of the power converter with the 3-phase grid voltages. This synchronization is not simple as just multiplying by three the synchronization of single-phase. Since, the three phases of the system works in coordination with each other, keeping particular relationships in terms of phase sequencing and phase shifting. Hence, we consider these three-phase of voltages as a vector components and assumed that these vector would be able to generate and and consume power in the system.

The grid-tied power converters are majorly sensitive to voltage perturbation. Because, there is a chance under such disturbed operative conditions that the power converter control system can lose it's control on the power signals, which then lead to operate any protective scheme of the converter or sometimes the chance of destroying the complete converter. Hence, to reduce these undesirable effects the power converter should couple at the common coupling point with the grid. That's why, the synchronization system should be much capable to detect these voltage vector disturbances, and in this meantime the power converter's control system should coincides such operating conditions and give some relief to the mains.[2]

In control of the grid connected converter, the Synchronization of the power converter with the grid voltage phase angle θ_g is a matter of great importance. Therefore it is really necessary the correct determination of the grid angle θ_g in very precise way so that it can make possible the regulation of power flow (active and reactive power) between the load side and the grid side of the power converter.

Once the proper synchronization of the power converter with grid is achieved the converter will operate correctly. In the estimation of synchronization, a minor mistake will also lead to an error in the output generated voltage, and its consequence will also be seen at the power flow or the output current w.r.t to the selected reference. That's why the grid synchronization should be well designed and also tested for different conditions of the grid to make sure the correct operation of the power converter. [3]

There are some events that can create disturbance in grid voltage. For example, harmonic current in power lines can cause resonance and non-constant loads on distributive lines and also environmental conditions like lightening and surges. According to the standards of IEEE 1159 [5], these faults could lead to several unwanted transients, unbalanced and distortions in system and also abrupt change in frequency. So that's in the control system the grid voltage amplitude and frequency cannot be taken as constant magnitudes. Therefore, they must be monitored constantly. Moreover, it should be take care that at the time of coupling

between converter and grid there must be a significant power involved from the converter w.r.t to the rated power of grid, because the frequency and the voltage of grid can be changed by the converter behaviour. The grid synchronization and control under distorted and unbalanced operating conditions was not implemented in this experiment. Since it was not the main goal of the experiment and this could be discussed later.

3.4.1 Modeling under abc Reference Frame

By knowing the function of constant DC-link voltage and assuming the power factor equals to unity, the topology of the three-phase grid-connected converter is shown in Figure 3.6 above. For large frequency applications, normally in industries, we use the same adaptation with LCL filter. But for the low frequency, normally we use the simple series L filter in each phase as shown in the Figure 3.2. [6]

Now by applying the KVL rule and KCL rule on the AC side and DC side of converter respectively. We can write the following equations:

$$V_{g,a} - L_g\frac{\mathrm{d}i_{g,a}}{\mathrm{d}t} - S_aV_{dc} = V_{g,b} - L_g\frac{\mathrm{d}i_{g,b}}{\mathrm{d}t} - S_bV_{dc} = V_{g,c} - L_g\frac{\mathrm{d}i_{g,c}}{\mathrm{d}t} - S_cV_{dc} \tag{3.4}$$

$$\frac{\mathrm{d}V_{dc}}{\mathrm{d}t} = S_ai_{g,a} + S_ai_{g,b} + S_ai_{g,c} - i_{load} \tag{3.5}$$

Here;
S_x: It shows the switches status (0 or 1) of the MOSFET's (Switches).
$V_{g,x}$: It shows the grid voltage of either phase.
$I_{g,x}$: It shows the grid current of either phase on AC side.
L_g: It shows the boost inductor.
C: It shows the DC-link capacitor.
I_{load}: Load Current.

In a balanced 3-ϕ three-wire system, the sum of all voltages and currents in each phase are equals to zero. i.e,

$$V_{g,a} + V_{g,b} + V_{g,c} = 0 \tag{3.6}$$

and similarly,

$$I_{g,a} + I_{g,b} + I_{g,c} = 0 \tag{3.7}$$

So, we can write Eq. 3.4 and Eq. 3.5 as:

$$\begin{bmatrix} V_{g,a} \\ V_{g,b} \\ V_{g,c} \end{bmatrix} = L_g\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{g,a} \\ i_{g,b} \\ i_{g,c} \end{bmatrix} + \begin{bmatrix} S_a - \frac{S_a+S_b+S_c}{3} \\ S_b - \frac{S_a+S_b+S_c}{3} \\ S_c - \frac{S_a+S_b+S_c}{3} \end{bmatrix} V_{dc} \tag{3.8}$$

$$C\frac{\mathrm{d}V_{dc}}{\mathrm{d}t} = \begin{bmatrix} S_a & S_b & S_c \end{bmatrix} \begin{bmatrix} i_{g,a} \\ i_{g,b} \\ i_{g,c} \end{bmatrix} - i_{load} \tag{3.9}$$

Where, $\frac{S_a+S_b+S_c}{3}$*V_{dc} is zero-sequence voltage. But it is important to note that, the eq. 3.8 and eq. 3.9 behaves discontinuously and also complicated to solve. So to achieve the continuous control circuit, a state-average technique is used for obtaining the integral of variable for one switching period (T_s), which gives us:

$$\langle x \rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} x(\tau) d\tau \tag{3.10}$$

Here, $\langle x \rangle_{T_s}$ represents the state-average value. By this approach, the switching function behaves same as the duty cycle (D) and hence by this approach the equations for inductive current and capacitive voltage becomes as follows:

$$\begin{bmatrix} \langle V_{g,a} \rangle_{T_s} \\ \langle V_{g,b} \rangle_{T_s} \\ \langle V_{g,c} \rangle_{T_s} \end{bmatrix} = L_g \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} \langle i_{g,a} \rangle_{T_s} \\ \langle i_{g,b} \rangle_{T_s} \\ \langle i_{g,c} \rangle_{T_s} \end{bmatrix} + \begin{bmatrix} D_a - \frac{D_a+D_b+D_c}{3} \\ D_b - \frac{D_a+D_b+D_c}{3} \\ D_c - \frac{D_a+D_b+D_c}{3} \end{bmatrix} V_{dc} \tag{3.11}$$

$$C\frac{\mathrm{d}}{\mathrm{d}t}\langle V_{dc} \rangle_{T_s} = \begin{bmatrix} D_a & D_b & D_c \end{bmatrix} \begin{bmatrix} \langle i_{g,a} \rangle_{T_s} \\ \langle i_{g,b} \rangle_{T_s} \\ \langle i_{g,c} \rangle_{T_s} \end{bmatrix} - \langle i_{load} \rangle_{T_s} \tag{3.12}$$

In above equations, the D denotes the duty cycle which is same as the switching status. In this way, the control circuit will operate continuously.

3.4.2 Coordinates Transformation from abc to $\alpha\beta$ Reference Frame

The 3-ϕ system is consider as static abc reference fram and then by applying the Clarke transformation on static abc frame, it can be transformed into the static 2-ϕ static $\alpha\beta$ reference frame. It can be notice that, in Figure 3.10, the following equations can be derived by the projection of static abc reference frame to the $\alpha\beta$ reference frame. While to maintain the amplitude a gain around 2/3 is being multiplied. [6]
By equations, it can be represent as;

$$C_{32} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{3.13}$$

$$C_{23} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{3.14}$$

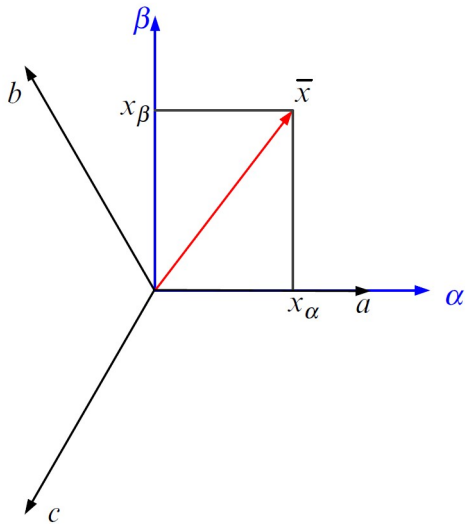

Figure 3.10: Coordinate Transformation from 3-ϕ static abc to 2-ϕ static $\alpha\beta$ reference frame.

So after reducing, we obtain the following transformation results for 2-ϕ $\alpha\beta$ stationary reference plane.

$$V_{\alpha\beta 0} = \begin{bmatrix} V_\alpha \\ V_\beta \\ 0 \end{bmatrix} = \begin{bmatrix} \widehat{V} cos\omega t \\ \widehat{V} sin\omega t \\ 0 \end{bmatrix} \tag{3.15}$$

As it is a 3-wire system, So, the only $\alpha\beta$ references are taken into account. As written in Eq. 3.16;

$$V_{\alpha\beta} = \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} \widehat{V} cos\theta \\ \widehat{V} sin\theta \end{bmatrix} \tag{3.16}$$

3.4.3 Modeling under dq Reference Frame

Furthermore, by applying the Park Transformation on the stationary $\alpha\beta$ reference plane it could be transformed in rotating reference plane (dq) through rotating angle θ. This rotating angle θ, is the angle between the d-axis and the α-axis. As it is shown in the Fig. 3.11. While the ω is the angular speed of the mains (gird).[6]

This transformation leads the results in form of following Eq. 3.17;

$$\widehat{V}_{dq} = R(\widehat{\theta}) * V_{\alpha\beta} = \begin{bmatrix} \widehat{V}.cos(\theta_g - \widehat{\theta}_{PLL}) \\ \widehat{V}.sin(\theta_g - \widehat{\theta}_{PLL}) \end{bmatrix} \tag{3.17}$$

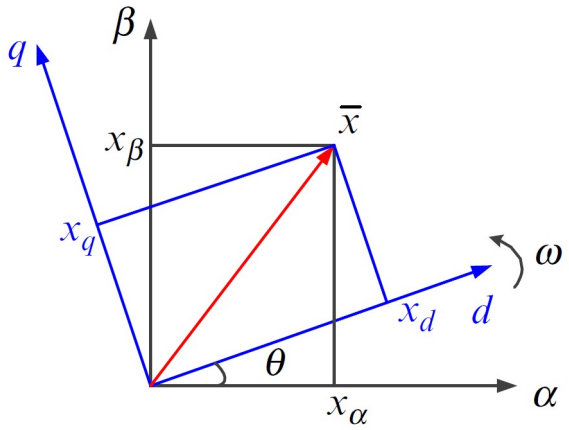

Figure 3.11: Coordinate Transformation from 3-ϕ stationary $\alpha\beta$ to rotating dq reference frame.

By considering the difference between θ and $\widehat{\theta}$ is so small and it's able to neglect it then the Eq. 3.17 can be written in more simplified form as:

$$\widehat{V}_{dq} = \begin{bmatrix} \widehat{V}_d \\ \widehat{V}_q \end{bmatrix} \approx \begin{bmatrix} \widehat{V}.1 \\ \widehat{V}.(\theta_g - \widehat{\theta}_{PLL}) \end{bmatrix} \tag{3.18}$$

It is worth while to notice that from the Eq. 3.18, can be noted from (2.6) that θ and $\widehat{\theta}$ are almost same, while the V_d is same as the amplitude of the voltage vector. And similarly, the V_q is derived as the error signal between angles θ and $\widehat{\theta}$.

3.5 Techniques for Grid Synchronization

Different approaches for grid synchronization techniques are already existing, and still they are under critical investigations for the sake of achieving fast and precise synchronization. And in all this, the grid angle θ_g plays an important role. Which is taken from the rotating reference frame (dq) transformation. For synchronization purpose, an already adapted and much popular technique Phase-Locked-Loop (PLL) has been taken into account.

3.5.1 Phase-Locked Loop

This section describes the basic structure about the Phase-locked loop techniques. PLL have basically two techniques, Synchronous Reference Frame PLL (SRF-PLL). This is the basic technique implemented in rotating/synchronous reference frame (dq). While the other technique named as, Dual Second-Order Generalized

Integrator-PLL (DSOGI-PLL). It is an advanced technique of PLL which is normally implemented on the stationary reference frame. [6]

SRF-PLL

There are three main components of SRF-PLL. Phase Detector (PD), Low-Pass Filter (LPF) and Voltage-Controlled Oscillator (VCO). This type of PLL is applicable for the the synchronous reference frame. It's general block schematic is explained in Fig. 3.12 below.

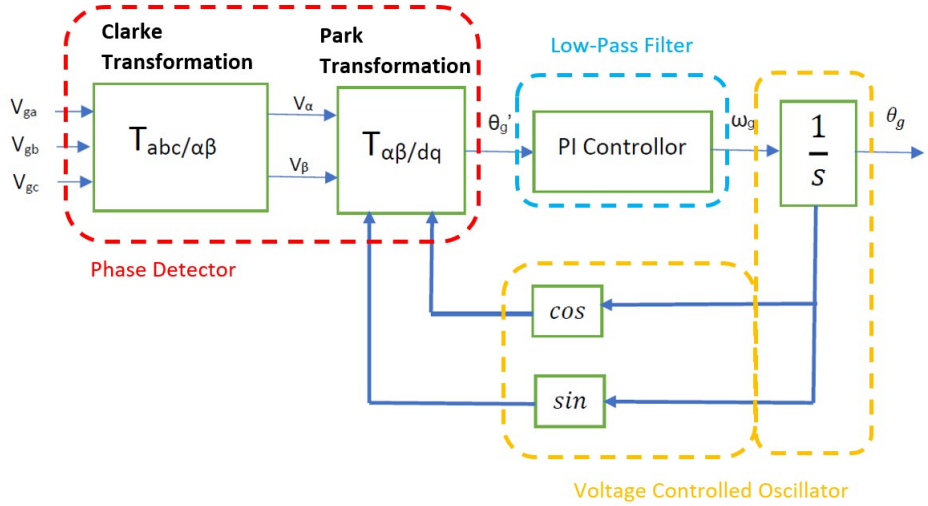

Figure 3.12: Block Diagram for Grid Synchronization of SRF-PLL

From Fig 3.12 it is shown the three main building blocks of SRF-PLL. Every building block behaves differently as explained below:

- Phase Detector: The 3-ϕ synchronous voltage ($V_{g,abc}$ is applied into the Clarke Transformation to transform it into the 2-ϕ stationary ($\alpha\beta$) reference frame. After that, through cosine and sine values of grid phase angle (θ_g) the Park transformation is applied to transform the stationary reference frame ($\alpha\beta$) to synchronous reference frame (dq).
- Low-Pass Filter: The PI Controller behaves as the Low-Pass filter. It's input is taken as the voltage amplitude along q-axis (V_q). While the output of this filter is the angular speed (ω_g) of the mains (grid) voltage. Thus, the voltage (V_q) is then normalized to zero. Hence, the grid voltage can be normalized against d-axis.
- Voltage Controlled Oscillator: Now the phase angle is needed to know, which is obtained through the grid voltage angular speed, which is applied to an

integrator, and then through cosine and sine sine and cosine the phase angle is retrieved. Which is then feed backed to the Park Transformation.

For better understanding the SRF-PLL, the simulation in PLECS is done for SRF-PLL under ideal 3-ϕ voltage system is shown in Fig 3.13. It can be seen that the grid-voltages are quietly following the ideal conditions. While the Grid-Power (P_g) and output DC-Power (P_{DC}) are also following each other. Which shows the correct synchronization of the converter with the mains. Similarly the currents in stationary reference frame (dq) are accroding to the theory explained above. The current through d-axis is around 7 Amps. Which is in the result of voltage loop. So that the active power properly saturated. And it's almost same as noticed during experiment. While the d-axis current is zero for imposing the unity power factor. (No Reactive Power)

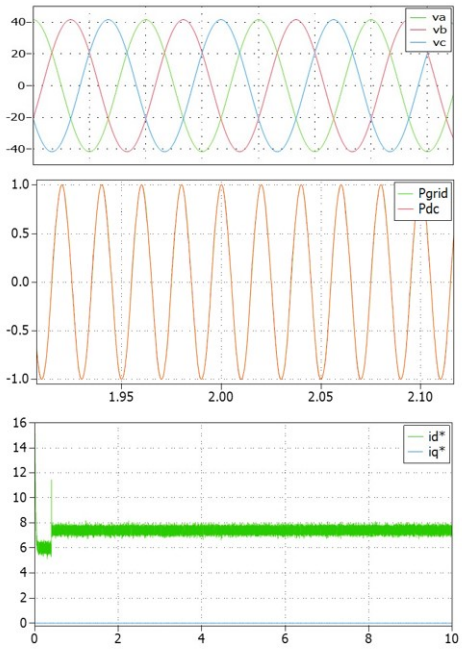

Figure 3.13

3.6 Control Design of 3-ϕ AFE (PI Controller)

As it is clear from Fig. 3.1 that the Grid-Tied converter are normally cascaded-control of the two loops and they are normally PWM controlled through AFE. The two loops includes, Outer Voltage loop to impose V_{dc} for the sake of independent control and other two inner current loops in grid dq coordinates to impose grid

power factor and current wave forms. The following Fig. 3.14 represents the complete block structure of the converter control.

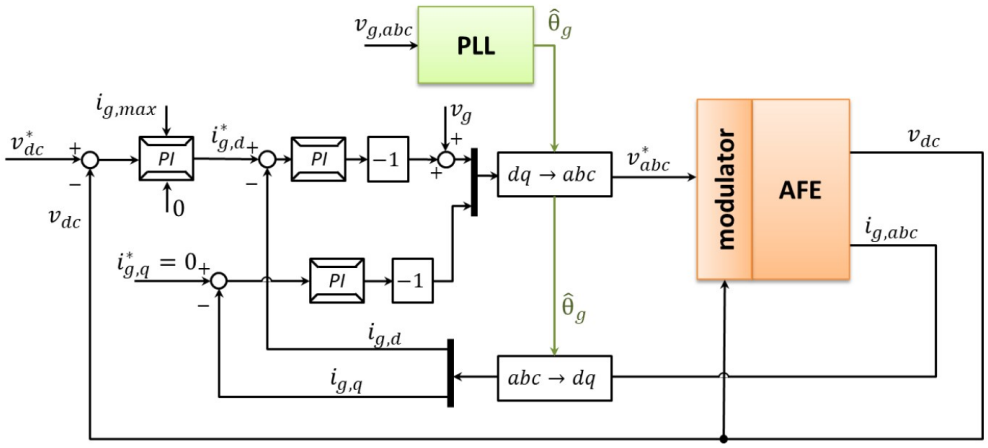

Figure 3.14: Complete Block Schematic for Converter Control

The position of d-axis is obtained through PLL using grid voltage. And current along d-axis extracted through voltage loop.

3.6.1 Design of Controller for AFE - Inner Current Loop

The converter current control loop is applied in the synchronous rotating (d,q) reference frame, which is synchronized with the voltage vector of grid. There are few advantages of this;

- Through proportional-integral it is possible to cancel-out the steady-state errors which could be present on reference.
- The total computational time is become less, as there are now only two regulators are present as compare to three which are needed.
- From Power theory, the active power (P) and the reactive power (Q) can be written as:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \frac{3}{2} * \begin{bmatrix} v_d & v_q \\ -v_q & v_d \end{bmatrix} * \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{3.19}$$

  As all the voltage amplitude is along d-axis and null along q-axis. So, the i$-d$ current gives us the information of active power while the i$_q$ is proportional to reactive power.[7]

So we the active and reactive power equations in the system can be written as:

$$P = \frac{3}{2}.v_d.i_d \tag{3.20}$$

$$Q = \frac{3}{2}.v_d.i_q \tag{3.21}$$

So from these power equations it is more easy and possible to control the power in converter.

The voltage loop gives the information of d-axis reference, but it not possible to control the active power directly from this loop. On the other hand, set the q-axis reference which allow to change the reactive power suitable according to grid codes.

The following block diagram shows the complete architecture of inner current loops.

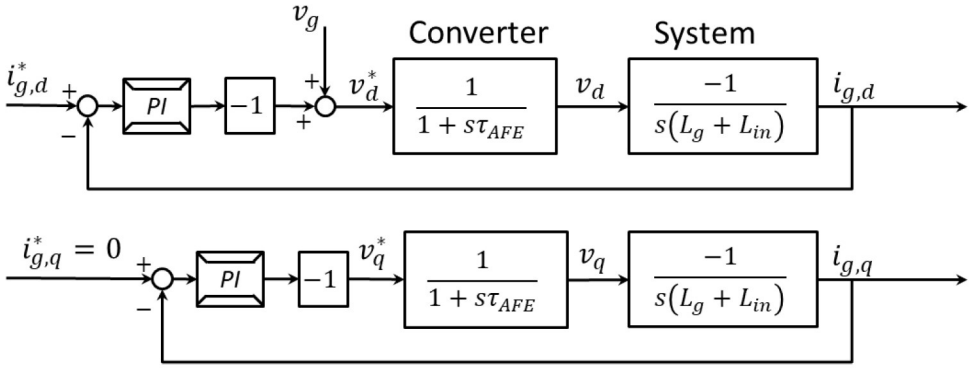

Figure 3.15: Complete Block Architecture of Inner Current Loops

- **Execution Delay of Converter:**

  It is the delay executed by the converter and known as the time constant delay of active front end (AFE) named as (τ_{AFE}). It is designed as the Low Pass filter (LPF) in converter. While in the Bode plot it gives us a pole at (τ_{AFE}) as it's shown below in following Fig. 3.16 below.

- **Open-Loop Transfer Function**

  By assuming the ideal PLL, ($\widehat{\theta}_g$=θ_g), the open loop transfer function can be written as;

$$\frac{i_{g,x}}{i^*_{g,x}}|_{OL} = \frac{k_{i,i} + sk_{p,i}}{s} . \frac{1}{s(L_g + L_{in})} . \frac{1}{1 + s\tau_{AFE}} \tag{3.22}$$

  Here, x=(d,q) reference coordinates.

  From the Eq. 3.22, it is clear that we have two poles. One due to the execution delay of the converter and second due to the system. While we have one zero due to the PI regulator. As it's shown in Fig 3.16 below.

- **Calibration of AFE-Inner Current Loops**

  For the calibration of current loops we can exploit the closed loop function in order to obtain the bandwidth closed loop transfer function and other parameters. i.e, the proportional gain would be as;

$$\omega_{b,i} \approx \frac{k_{p,i}}{L_g + L_{in}} \ll \frac{1}{\tau_{AFE}} \tag{3.23}$$

  So, the calibration can be achieved for the $k_{p,i}$ at certain bandwidth as;

$$k_{p,i} = \omega_{b,i} * (L_g + L_{in}) \tag{3.24}$$

  And for relatively high phase margin of the system the zero of the system which is introduced by the PI regulator should be set sufficiently lower than the bandwidth, i.e the integral gain should be as;

$$\frac{k_{i,i}}{k_{p,i}} \ll \omega_{b,i} \tag{3.25}$$

  or,

$$k_{i,i} = k_{p,i} \times \omega_{b,i} \tag{3.26}$$

  Keep note that, this calibrated bandwidth must be sufficient lower than the execution delay (τ_{AFE}).

The Bode plot is shown as:

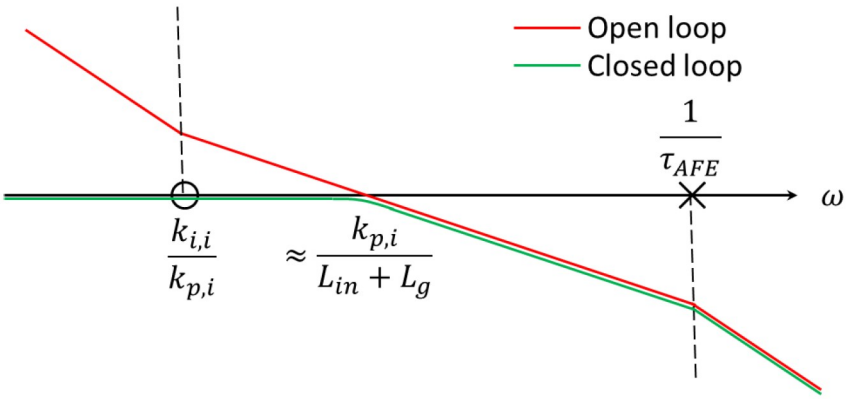

Figure 3.16: Bode Plot for Open-Loop and Closed-Loop Transfer Functions

The table 3.2 below shows the calibration of AFE control for current control.

Calibration for Current Control	
Parameter	**Value**
$f_{bw,i}$	1000 Hz
$\omega_{bw,i}$	6283.19 rad/sec
$f_{z,i}$	500 Hz
$\omega_{z,i}$	3141.595 rad/sec
$k_{p,i}$	0.854513 Ω
$k_{i,i}$	2684.53377 Ωrad/sec

Table 3.2: Calibration for Current Control

3.6.2 Control of AFE - Outer Voltage Loop (Vdc)

In this control V($_{dc}$) is imposed externally. Its is done so because if the initial DC link voltage is less than the required by load/battery then converter must be able to withdraw more power from grid to fulfill the needs of the loads and to charge the DC-Link capacitors.[7]

The calibration of voltage loop is done based on the current in DC link capacitors. i.e,

$$V_{dc} = \frac{i_c}{s.C_{dc}} = \frac{i_{dc} - i_{load}}{s.C_{dc}} \tag{3.27}$$

Consider that the input power (P_g) is same is the output power (P_{dc}). From Eq. 3.20, the expression for (P_g)=(P_{dc}) can be written as;

$$\frac{3}{2}.V_g.i_{g,d} = V_{dc}.i_{dc} \tag{3.28}$$

So the Dc-Voltage would be obtained through the following expression.

$$V_{dc} = \frac{1}{s.C_{dc}}.(G.i_{g,d} - i_{load}) \tag{3.29}$$

where, $G = \frac{\frac{3}{2}V_g}{V_{dc}}$ is a constant. It is computed by the grid voltage and DC voltage. And the Eq. 3.29 shows that the DC current is proportional to the grid current along d-axis with constant G.

So the equivalent transfer function in terms of block architecture would become as:

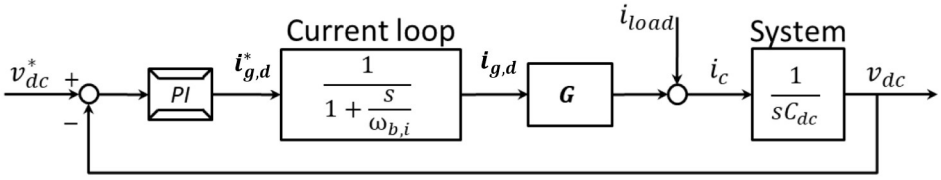

Figure 3.17: Voltage Control Loop

From the Fig. 3.17, the referenced DC voltage gives the information of current along d-axis. Because along the q-axis it is zero. i.e,
$|i_{g,dq}| = i_{g,d}$
Because, $|i_{g,q}| = 0$

And the bandwidth of my voltage loop must be much lower than the bandwidth of my current loop. i.e,

$$\omega_{b,v} \approx \frac{k_{p,v}.G}{C_{dc}} \ll \omega_{b,i} \tag{3.30}$$

So, the expression for the voltage proportional gain as follows;

$$k_{p,v} = \frac{\omega_{b,v}.C_{dc}}{C_{dc}} \tag{3.31}$$

Similarly the expression for the zero of PI regulator would be as,

$$\frac{k_{i,v}}{k_{p,v}} \ll \omega_{b,v} \tag{3.32}$$

$$k_{i,v} = \omega_{b,v} k_{p,v} \tag{3.33}$$

The table 3.3 below shows the calibration of AFE control for voltage control.

Calibration for Voltage Control	
Parameter	**Value**
$f_{bw,v}$	100 Hz
$\omega_{bw,i}$	628.319 rad/sec
$f_{z,i}$	10 Hz
$\omega_{z,i}$	62.831 rad/sec
$k_{p,v}$	0.586273 Ω
$k_{i,i}$	36.8366 Ωrad/sec

Table 3.3: Calibration for Voltage Control

3.7 Hardware Setup

The physical system on which the complete demo was conducted is constituted by a PCB, which is used for the purpose of multi-purpose three-phase grid-connected converter functionality and by the three step down transformers connected in Y-configuration. These step-down transformers (220/24)V are considered as the Grid which is connected with our converter. Their per-phase RMS voltage is 24 V_{rms}. While the peak voltage is around 33.94 V_{pk} per phase.

The DC supply is used to pre-charge DC-Link capacitor before the converter connected to grid/mains. And the oscilloscope is used for the visualization of final results through current probes. The electronic load is used as a battery. It has a variable setup values of battery rating with respect to the current.

The complete setup of test-bench is shown below in figure 3.1.

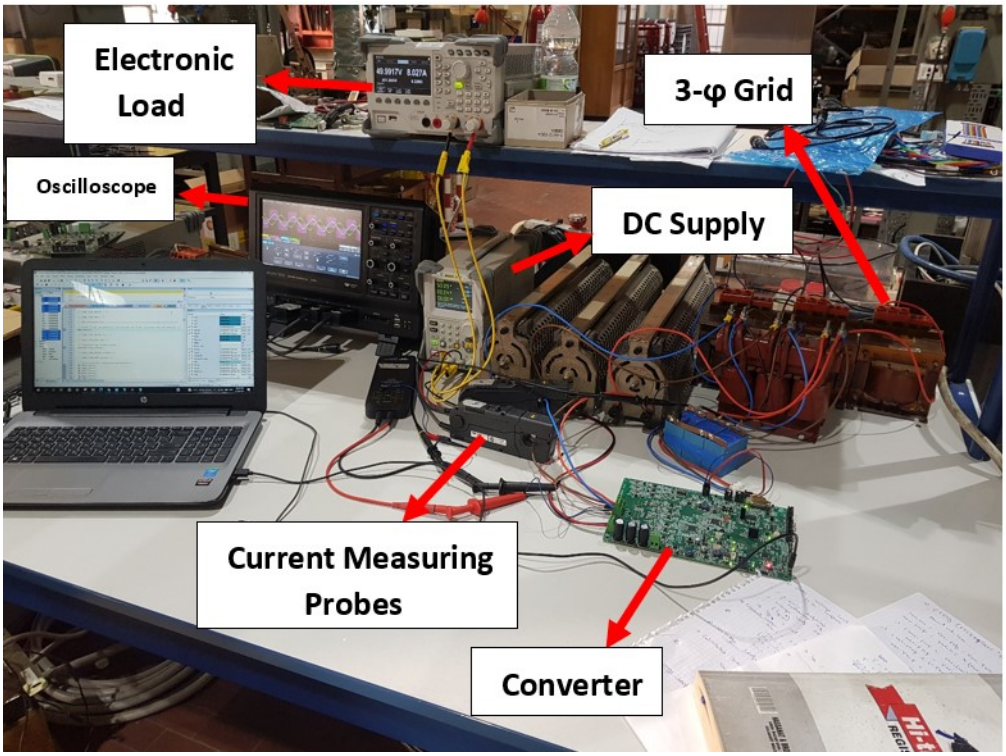

Figure 3.18: Complete Hardware Setup

Chapter 4

Conclusions

This chapter comprises the final steps of the experimental activity done in the PEIC lab under the supervision of Prof. Gianmario Pellegrino and advisor Dott. Fausto Stella. It concludes the simulation validation of the results on PLECS and compares them with the final results of the firmware design on the converter. The final activities can be summed up as following:

- Validation of results on PLECS program.
- Assembly of the components on test bench and validation of Active Front End (AFE) for Grid-Tied Converter.
- Verification of the designed firmware work on test-bench and testing on different switching frequency on same working conditions.

The following topics shows the results of experimental activity.

4.1 Simulation Validation using PLECS

The software simulation for the design of AFE of grid-connected converter was being carried out in PLECS tool. The following Figs. shows the results of the grid and their respective transient behaviour in order to observe the results through software simulation.

The converter is fed by the three-phase voltage generators and their respective currents. At 0.40 seconds the voltage step performed, in order to produce the current transient in the system. The amplitude of voltage is being calculated for the three-phase system which produces the correspondence current in the system. The following Fig. 4.1 shows the voltage and its correspondence transient behaviour of current.

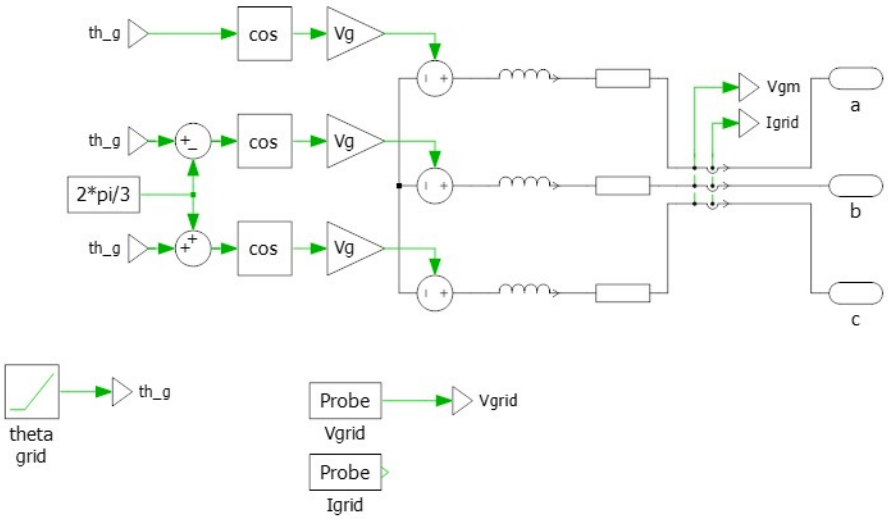

Figure 4.1: PLECS Schematic of Grid Design

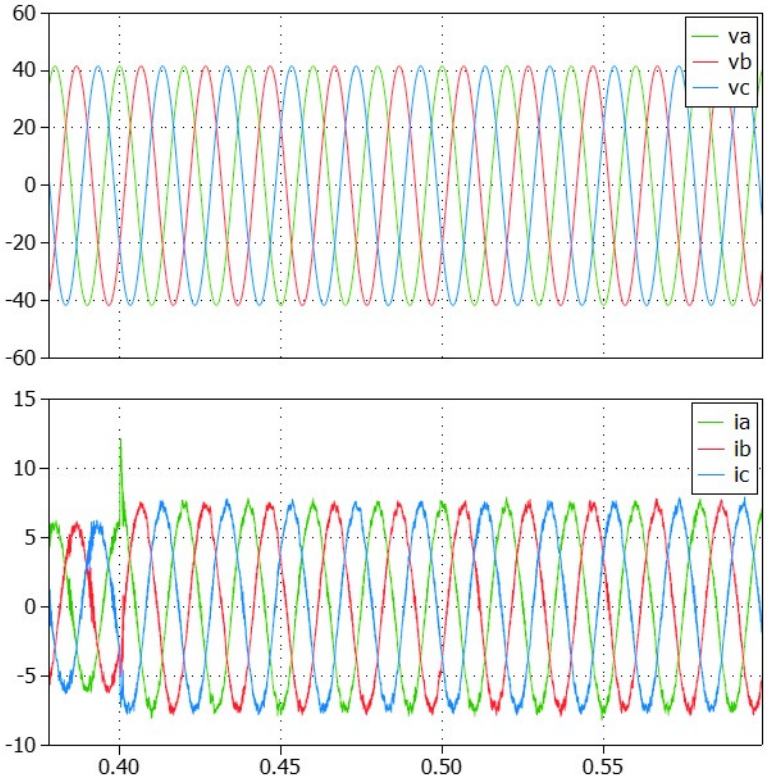

Figure 4.2: Transient behaviour of Current during Voltage Step in 3-Φ Frame

Similarly, the figure 4.3 shows the transition response of the voltage (Vdc) from 38V to 48V at 0.40 sec using PLECS. Distortaion

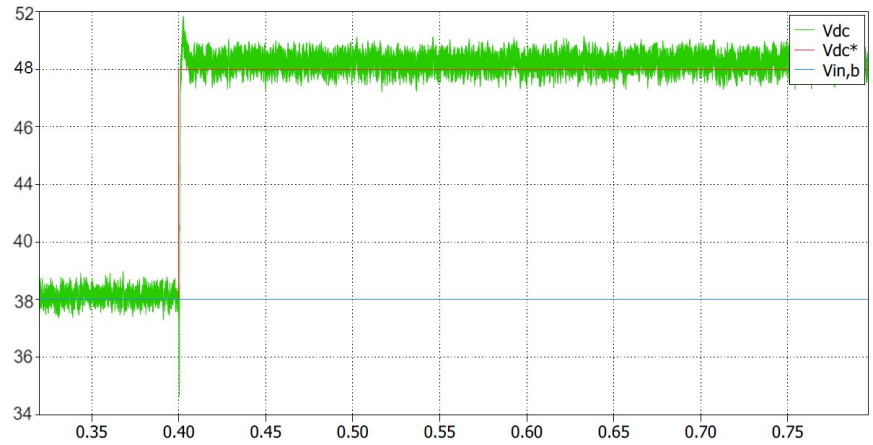

Figure 4.3: Validation of Transient behaviour of DC-Link Voltage using PLECS

The following Fig 4.4 shows the Total Harmonic Distortion (THD), at 10 kHZ switching frequency, it is around 4%, Which validates the results of experimental test in laboratory.

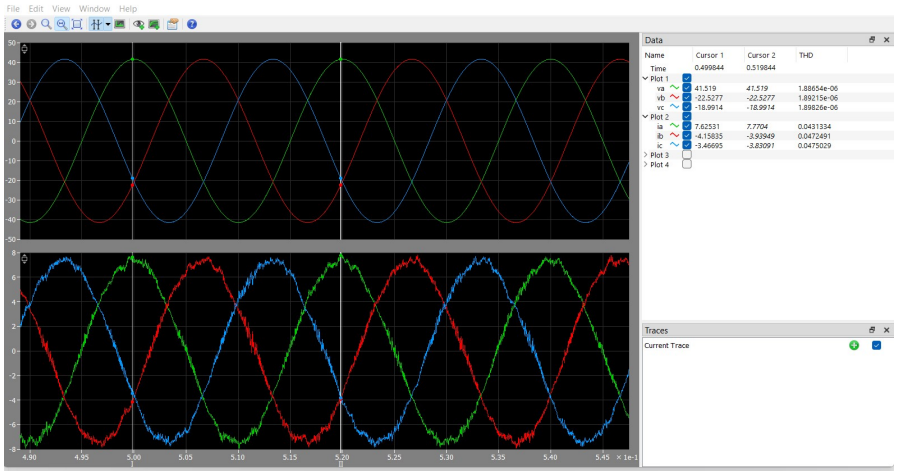

Figure 4.4: Validation of Total Harmonic Distortion (THD) at 10 kHz using PLECS

4.2 Experimental Results

The converter has been tested for multiple routines under different switching frequencies, while keeping the working load conditions same for all the tests. It has been observed that, according to the international standards and rules of grid tied converter the total Harmonic Distortion (THD) for the converter was being observed under 5%.

The converter is being tested under multiple frequencies while keeping the load conditions same to see the functional behaviour and efficiency of the converter. It was observed that converter can work under multiple frequencies by adjusting the controlling gains.

The following results are being observed at the end of experiment.

Total Harmonic Distortion (THD)

To analyse the behaviour of converter Total Harmonic Distortion (THD), experiment was being carried our at four different switching frequencies, 8kHz, 10kHz, 15kHz and 20 kHz.

At 8kHz

The following figure shows the converter behaviour under 8kHz switching frequency.

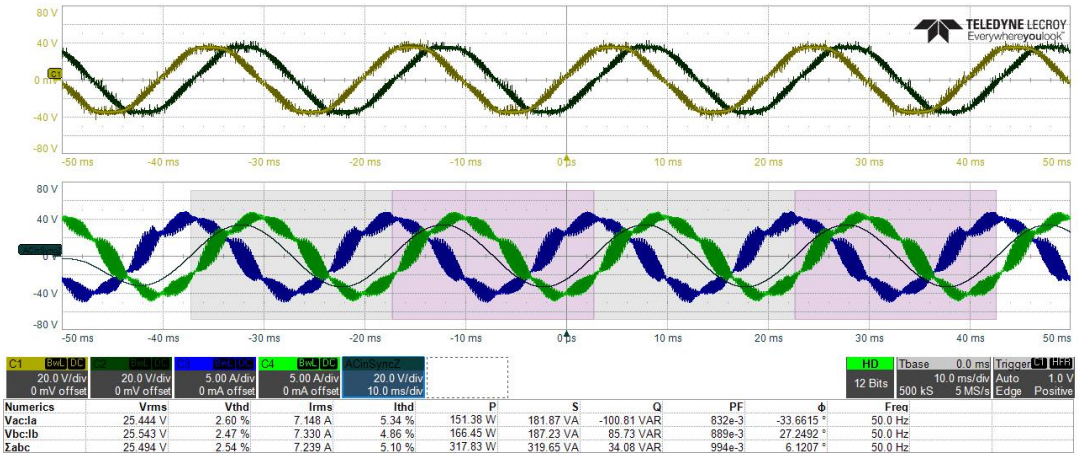

Figure 4.5: Converter results under 8kHz Switching Frequency

While it is being noticed that, by enabling the harmonics at converter, it starts behaving as the rectifier and the 5th harmonic was noticed failed. The following figures shows the behaviour before and after enabling the Harmonics.

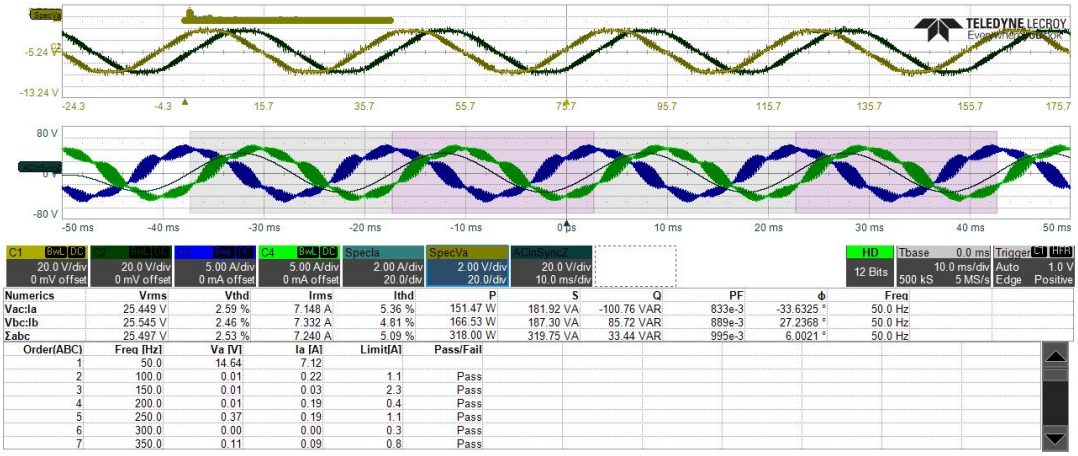

Figure 4.6: Converter results under 8kHz Switching Frequency before enabling the Harmonics

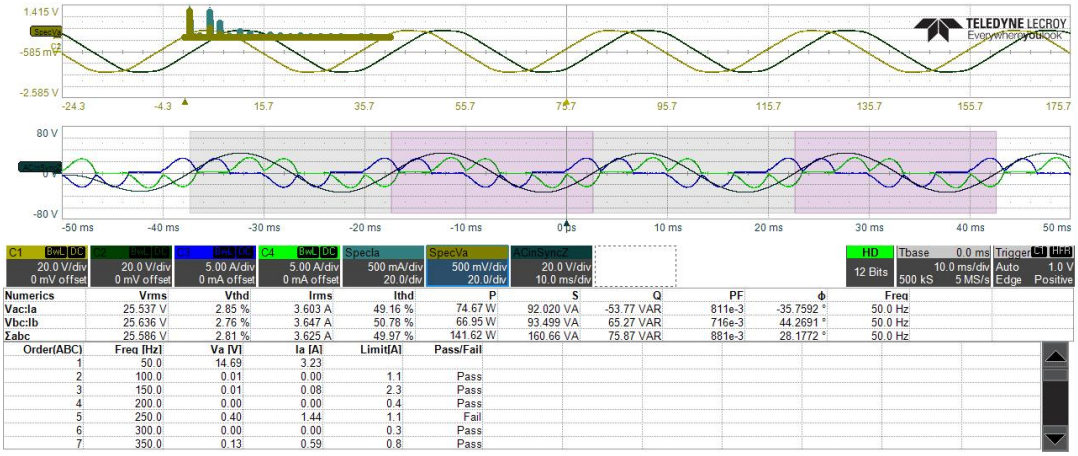

Figure 4.7: Converter results under 8kHz Switching Frequency after enabling the Harmonics

The following integral and proportional gains are adjusted for 8kHz switching for converter. While maintaining the DC-Link voltage at 48V.

Calibration for Current Control Gains $f_{sw,i}$ = 8 kHz	
Parameter	**Value**
TIM_1_Cycles	13500
$f_{sw,i}$	8 kHz
$k_{p,i}$	1.200 Ω
$k_{i,i}$	4000 Ωrad/sec

Table 4.1: Gains for Current Control Loop

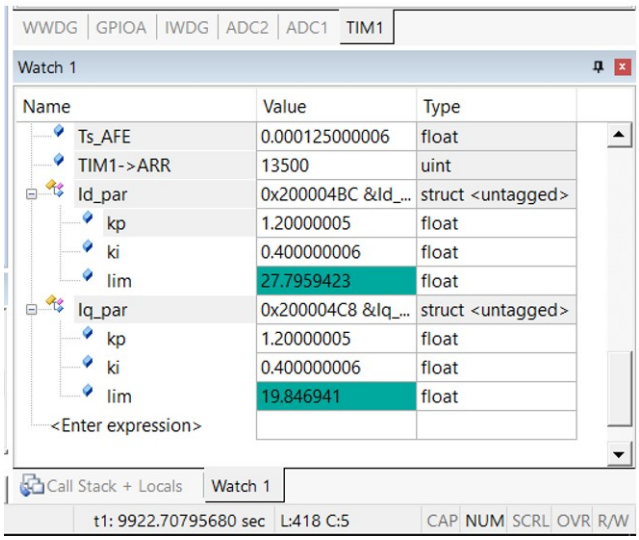

Figure 4.8: Current Control Gains for 8kHz Switching Frequency

It can be seen in results that, at 8kHz the THD is around 2.6%. While the converter active power is around 320W for measured two phases through oscilloscope. Similarly the other parameters can also be observed.

At 10 kHz

The following figure shows the converter behaviour under 10kHz switching frequency.

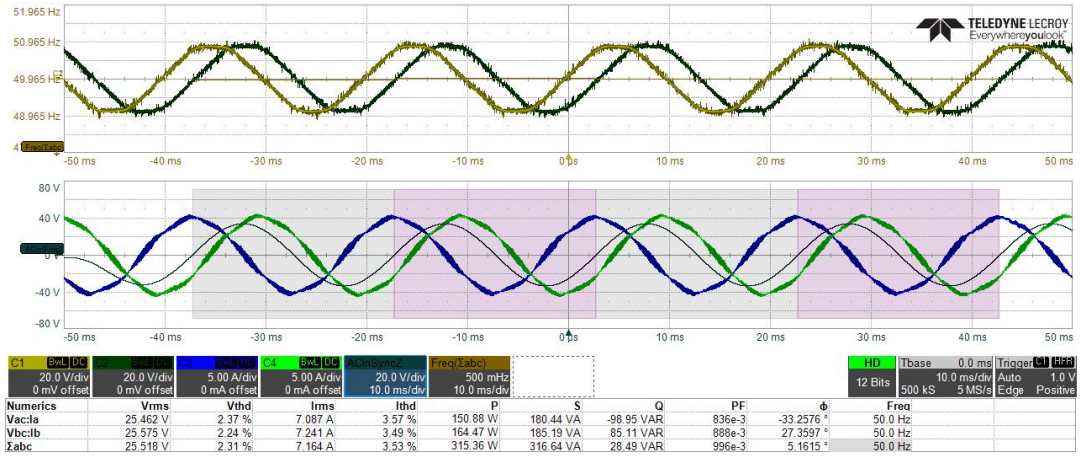

Figure 4.9: Converter results under 10kHz Switching Frequency

While it is being noticed that, even by enabling the harmonics at converter all the harmonics testes passed. It was tested upto 40 harmonics. The following figures shows the behaviour before and after enabling the Harmonics.

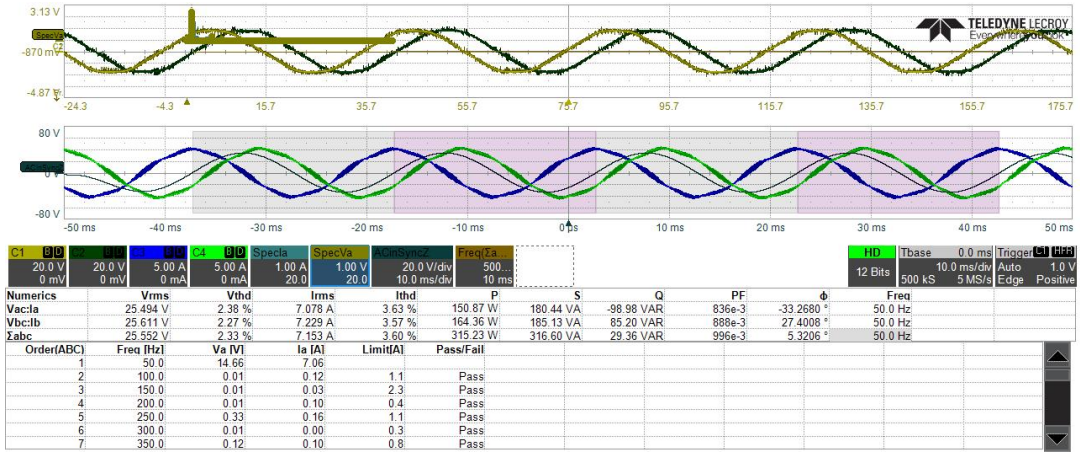

Figure 4.10: Converter results under 10kHz Switching Frequency after enabling the Harmonics

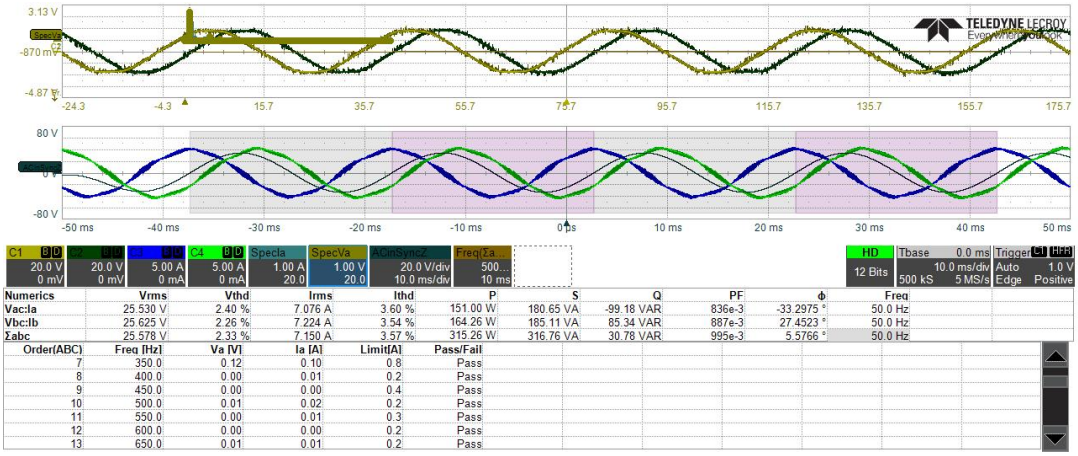

Figure 4.11: Converter results under 10kHz Switching Frequency after enabling the Harmonics

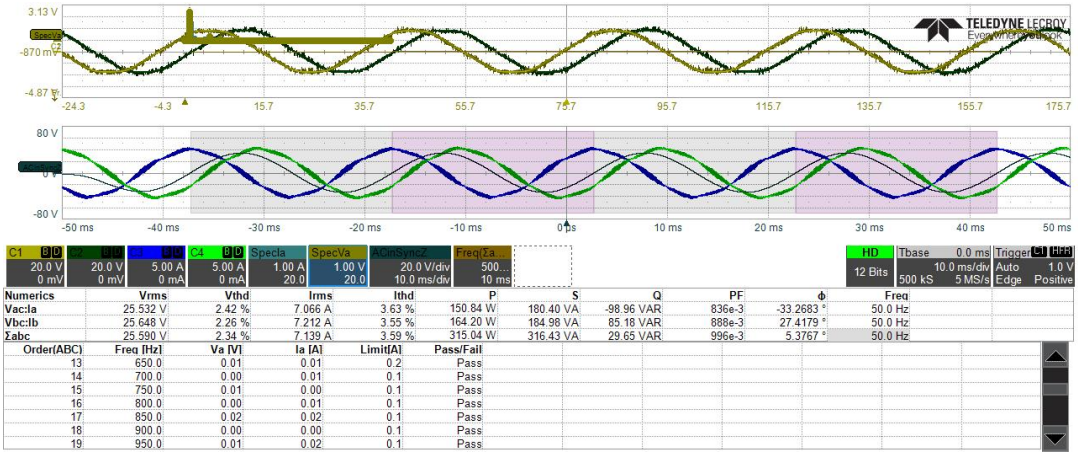

Figure 4.12: Converter results under 10kHz Switching Frequency after enabling the Harmonics

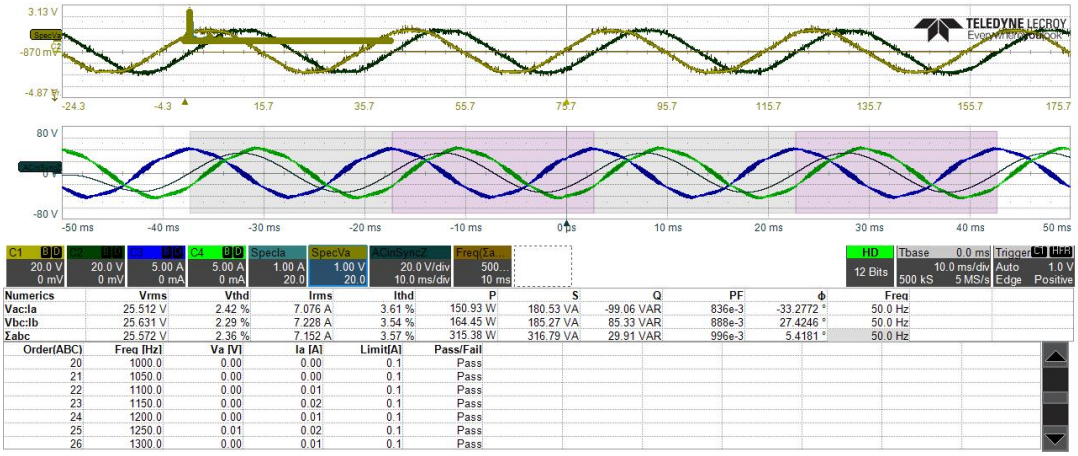

Figure 4.13: Converter results under 10kHz Switching Frequency after enabling the Harmonics

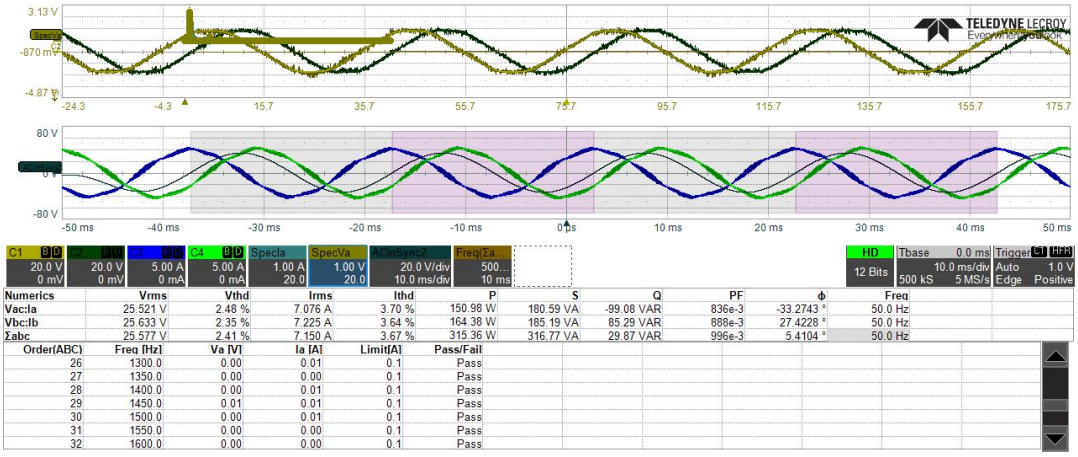

Figure 4.14: Converter results under 10kHz Switching Frequency after enabling the Harmonics

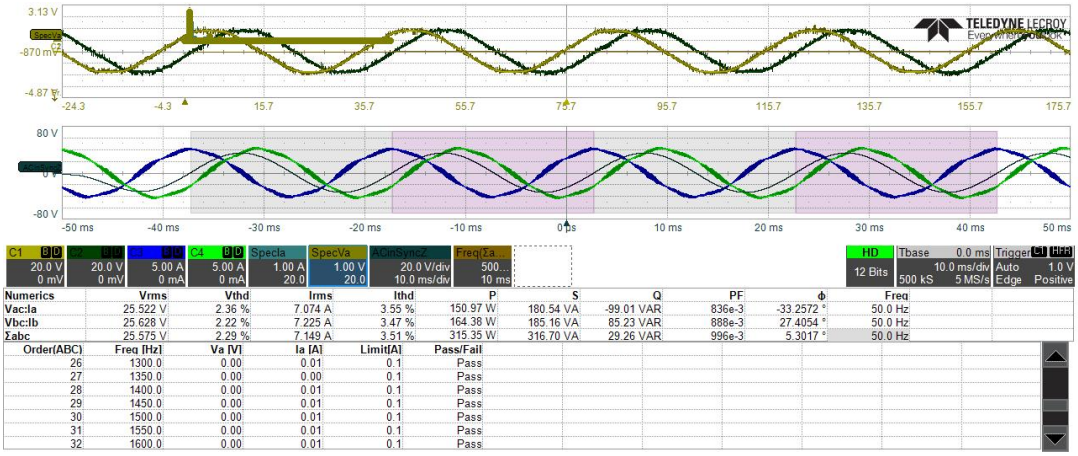

Figure 4.15: Converter results under 10kHz Switching Frequency after enabling the Harmonics

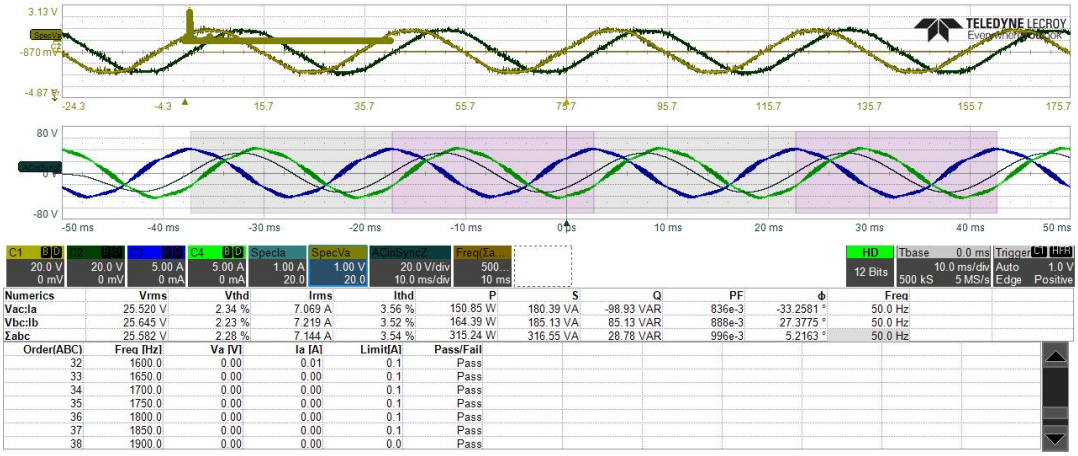

Figure 4.16: Converter results under 10kHz Switching Frequency after enabling the Harmonics

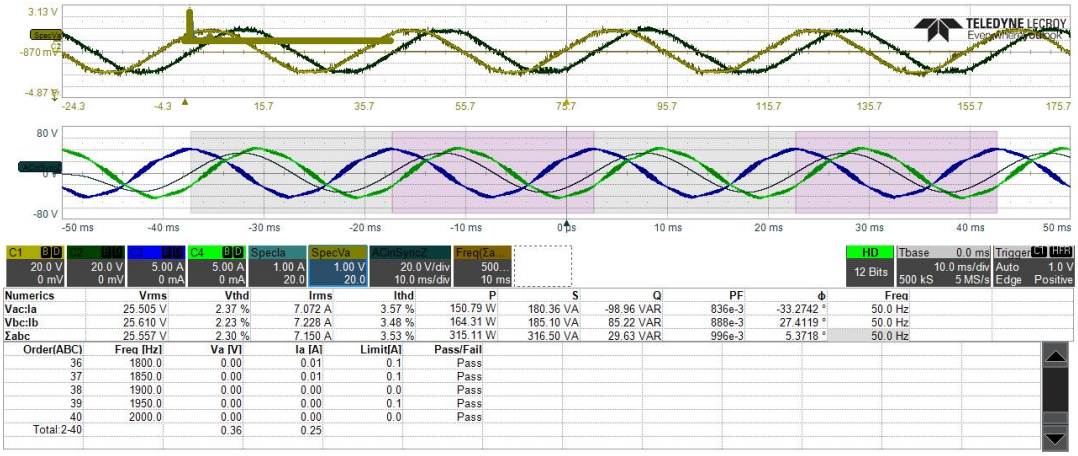

Figure 4.17: Converter results under 10kHz Switching Frequency after enabling the Harmonics

It can be clearly seen that throughout the harmonics enabled upto 40th. The first one at 50Hz there was noticed the output. While at the others it is not observed which means that the converter is being able to carry out this more efficiently at this 10 kHz switching frequency.

The following integral and proportional gains are adjusted for 10kHz switching for converter. While maintaining the DC-Link voltage at 48V.

Calibration for Current Control Gains	
Parameter	**Value**
TIM_1_Cycles	10800
$f_{sw,i}$	10 kHz
$k_{p,i}$	1.300 Ω
$k_{i,i}$	3000 Ωrad/sec

Table 4.2: Gains for Current Control Loop for $f_{sw,i}$ = 10 kHz

It can be seen in results that, at 10kHz the THD is around 2.3%. While the converter active power is around 320W for measured two phases. Similarly the other parameters can also be observed.

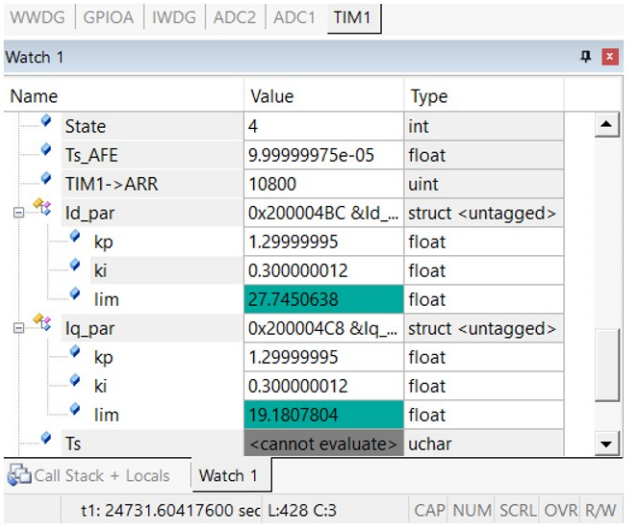

Figure 4.18: Current Control Gains for 10kHz Switching Frequency

At 15 kHz

The following figure shows the converter behaviour under 15kHz switching frequency.

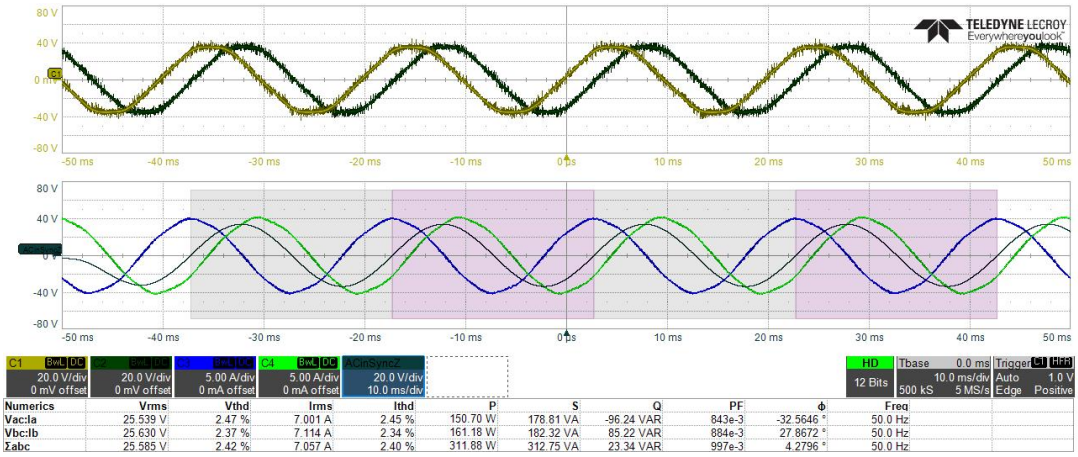

Figure 4.19: Converter results under 15kHz Switching Frequency

The following figures shows the behaviour after enabling the Harmonics in converter.

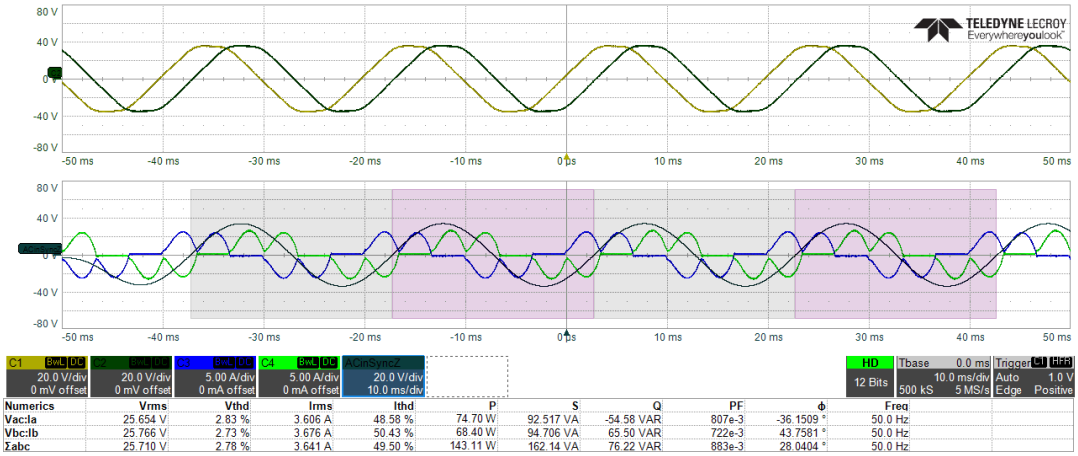

Figure 4.20: Converter results under 15kHz Switching Frequency after enabling the Harmonics

It has been observed in above figures, at 15 kHz, the converter is working with around 2.5% of THD. While during State 0 which is error state it works as a diode rectifier.

The following integral and proportional gains are adjusted for 15kHz switching for converter. While maintaining the DC-Link voltage at 48V.

Calibration for Current Control Gains	
Parameter	**Value**
TIM_1_Cycles	7200
$f_{sw,i}$	15 kHz
$k_{p,i}$	2.000 Ω
$k_{i,i}$	4500.000 Ωrad/sec

Table 4.3: Gains for Current Control Loop for $f_{sw,i}$ = 15 kHz

Watch 1

Name	Value	Type
Ts_AFE	6.66666674e-05	float
TIM1->ARR	7200	uint
Id_par	0x200004BC &Id_...	struct <untagged>
kp	2	float
ki	0.300000012	float
lim	27.7959423	float
Iq_par	0x200004C8 &Iq_...	struct <untagged>
kp	2	float
ki	0.300000012	float
lim	20.1632996	float
<Enter expression>		

Figure 4.21: Current Control Gains for 15kHz Switching Frequency

At 20 kHZ

The following figure shows the converter behaviour under 20 kHz switching frequency.

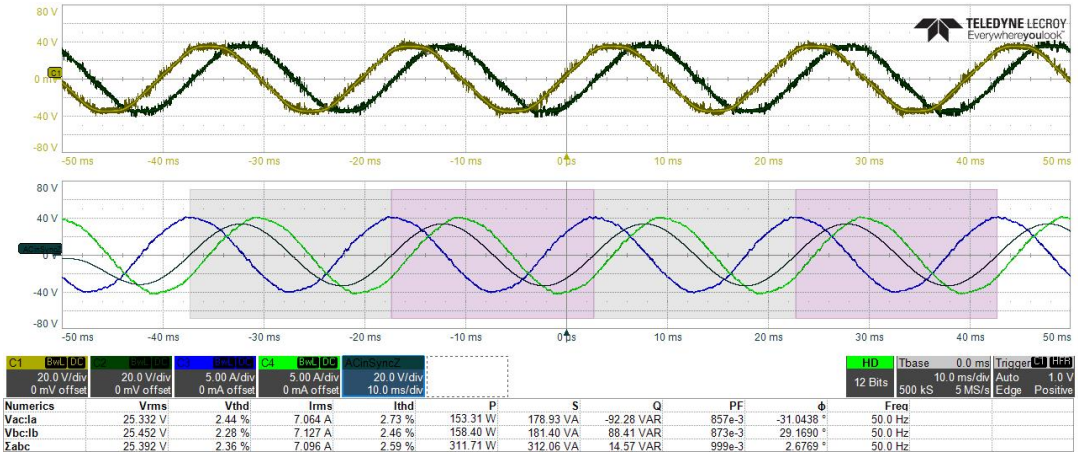

Figure 4.22: Converter results under 20kHz Switching Frequency

The following figures shows the behaviour before and after enabling the Harmonics in converter.

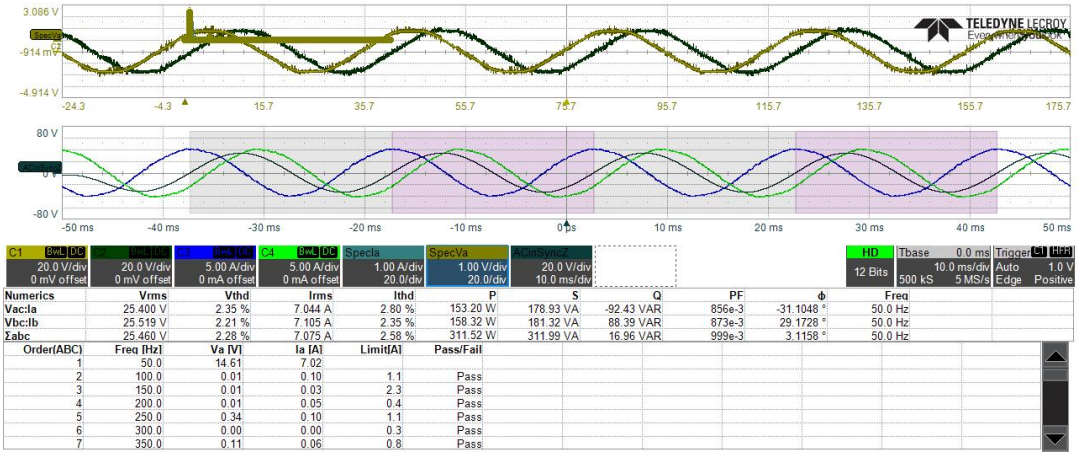

Figure 4.23: Converter results under 20kHz Switching Frequency before enabling the Harmonics

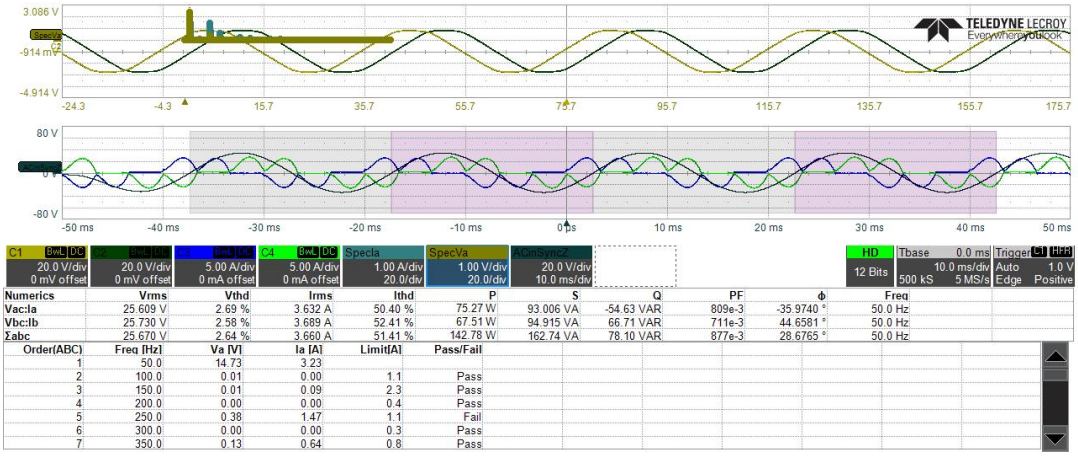

Figure 4.24: Converter results under 20kHz Switching Frequency after enabling the Harmonics

It is being noticed that, by enabling the harmonics at converter, it starts behaving as the diode rectifier and the 5^{th} harmonic was noticed failed.

The following integral and proportional gains are adjusted for 20kHz switching for converter. While maintaining the DC-Link voltage at 48V.

Calibration for Current Control Gains	
Parameter	**Value**
TIM_1_Cycles	5400
$f_{sw,i}$	20 kHz
$k_{p,i}$	1.50 Ω
$k_{i,i}$	3500.000 Ωrad/sec

Table 4.4: Gains for Current Control Loop for $f_{sw,i}$ = 20 kHz

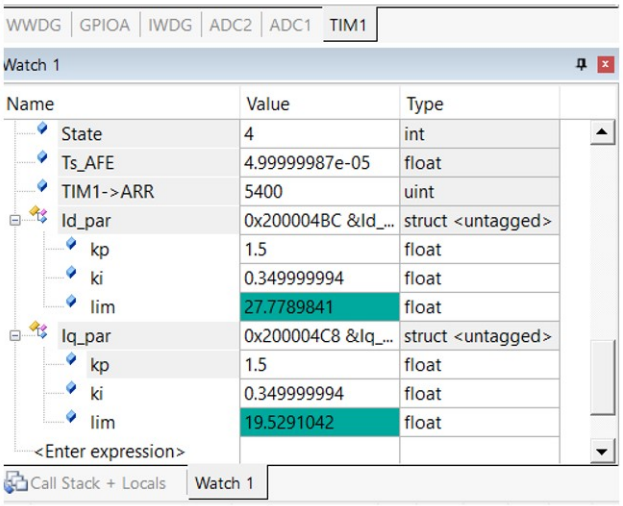

Figure 4.25: Current Control Gains for 20kHz Switching Frequency

PWM Output at 10 kHz with 48V

The converter's PWM output according to the electronic load connected behaving as a battery of load around 8Ω and absorbing the current around 13A through converter. The DC-Link voltage is considered as 48V connected with converter.

The following figures shows the final PWM wave-forms at output side of the converter.

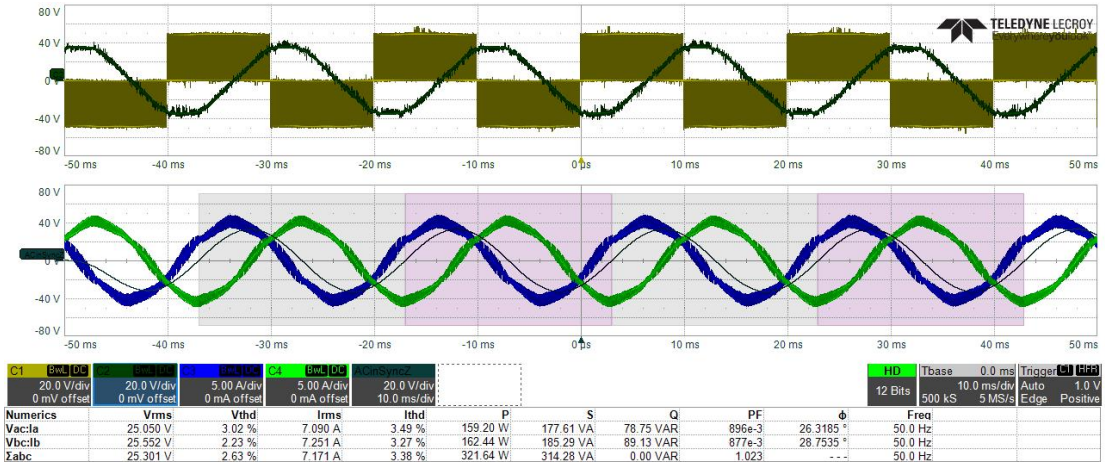

Figure 4.26: Converter Output Waveforms at 10 kHz Switching Frequency

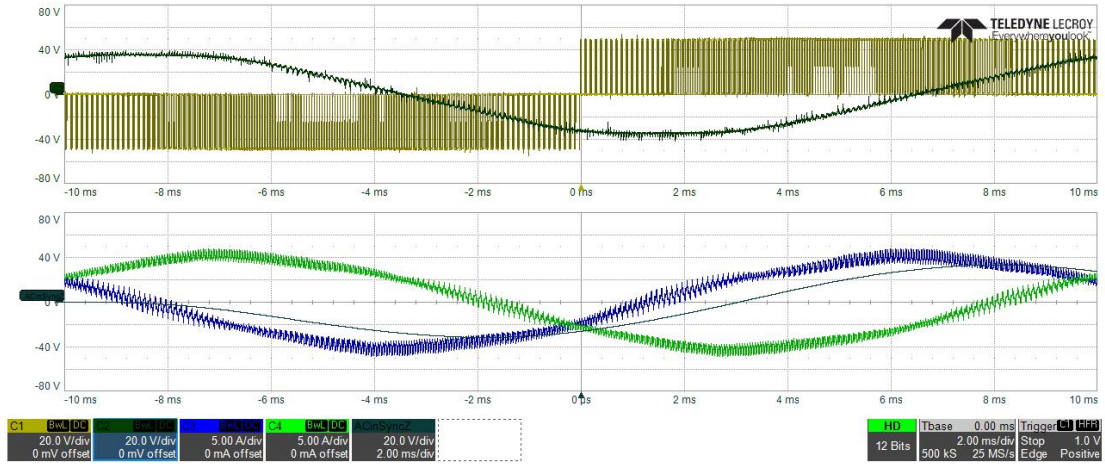

Figure 4.27: Converter PWM Output Waveform at 10 kHz Switching Frequency

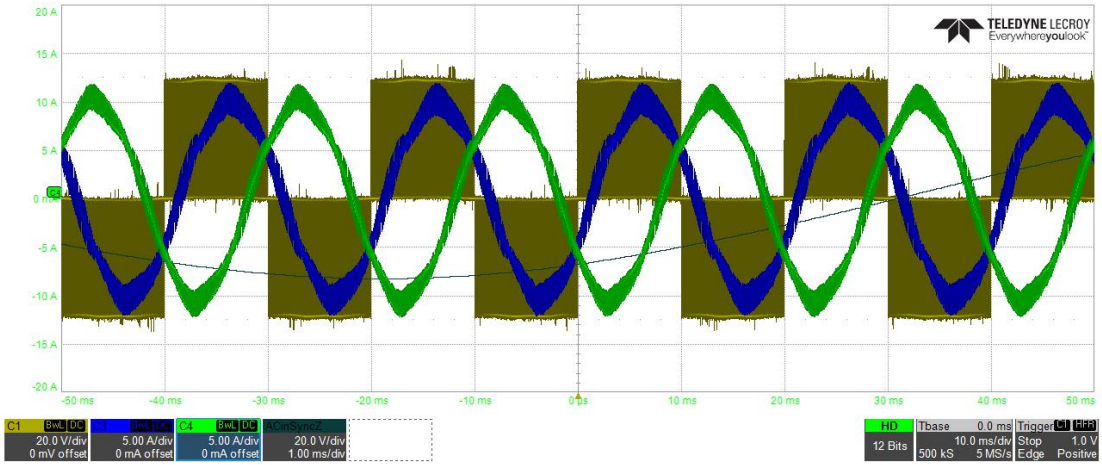

Figure 4.28: Converter Current Waveform w.r.t to PWM Output at 10 kHz Switching Frequency

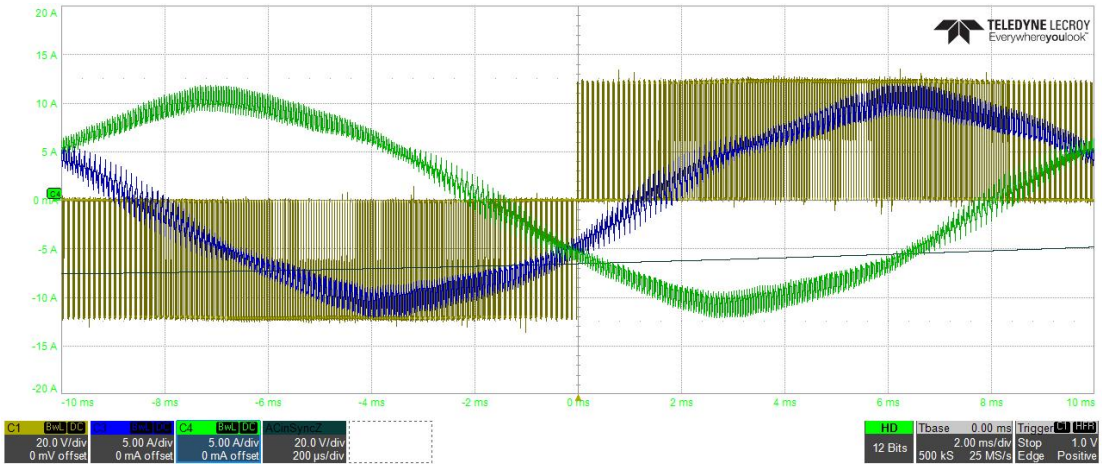

Figure 4.29: Converter Current Waveform w.r.t to PWM Output at 10 kHz Switching Frequency

DC-Link Voltage (Vdc)

The following figures shows the DC-Link voltage obtained during the experiment when the converter is connected to the grid. It is set to 48 Vdc as the set point for the DC-Link for this converter. While the switching frequency is set as 10 kHz.

Following figures shows as:

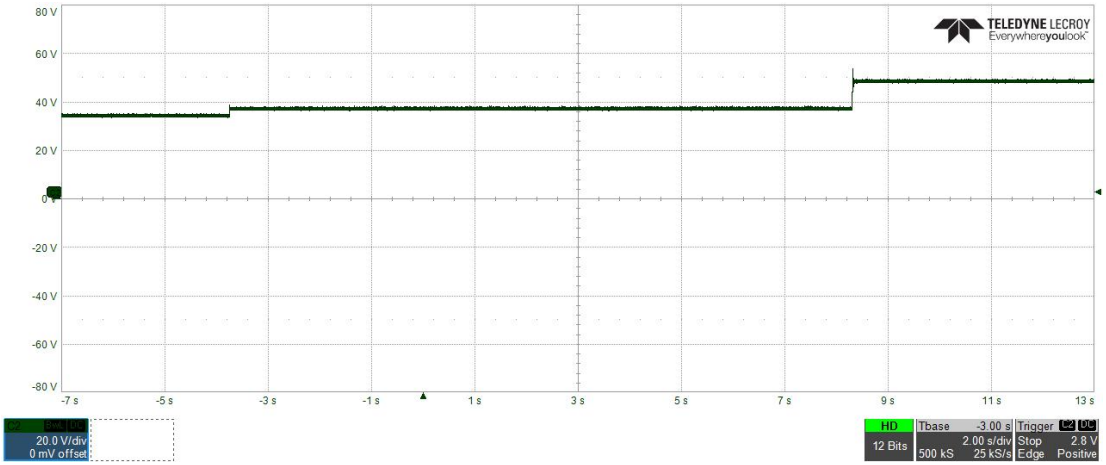

Figure 4.30: Transient Response of Vdc triggering at 48V

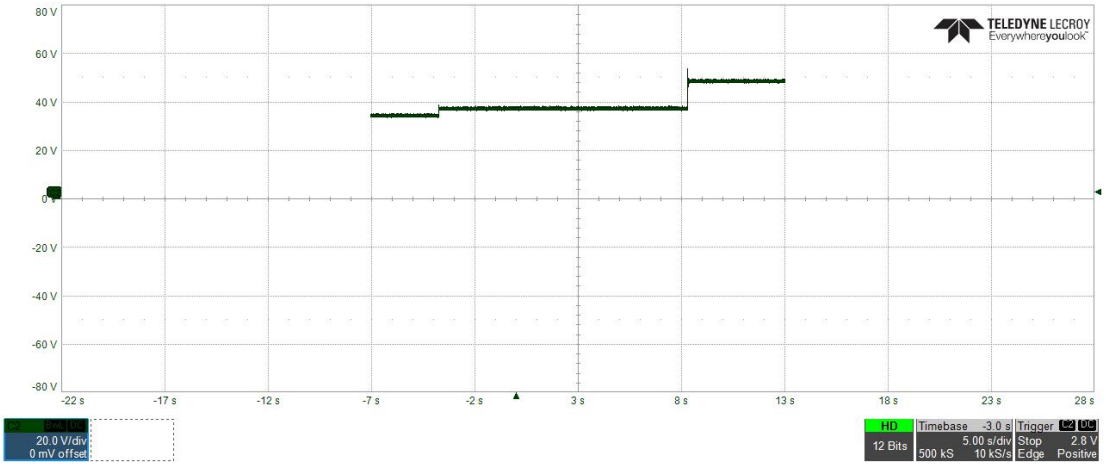

Figure 4.31: Transient Response of Vdc triggering at 48V

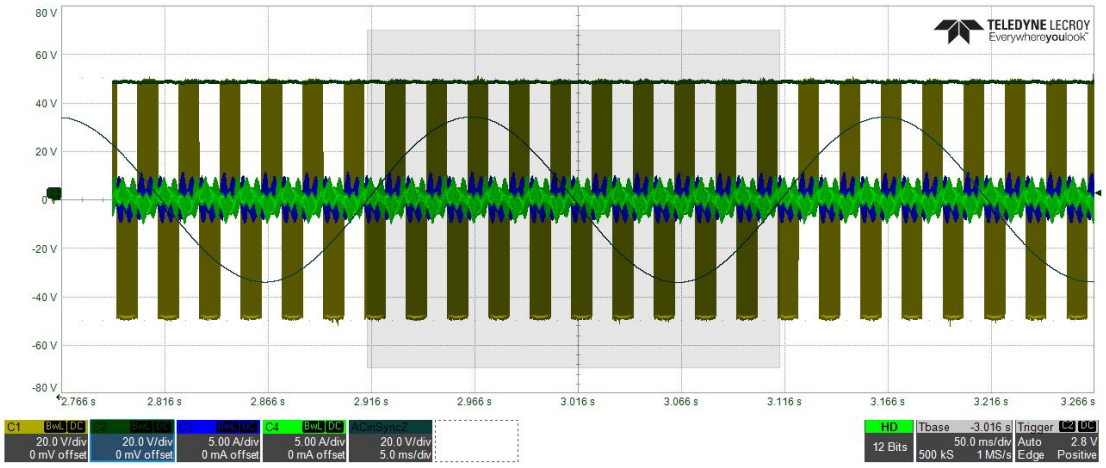

Figure 4.32: Transient Response of Vdc triggering at 48V w.r.t to PWM at Output

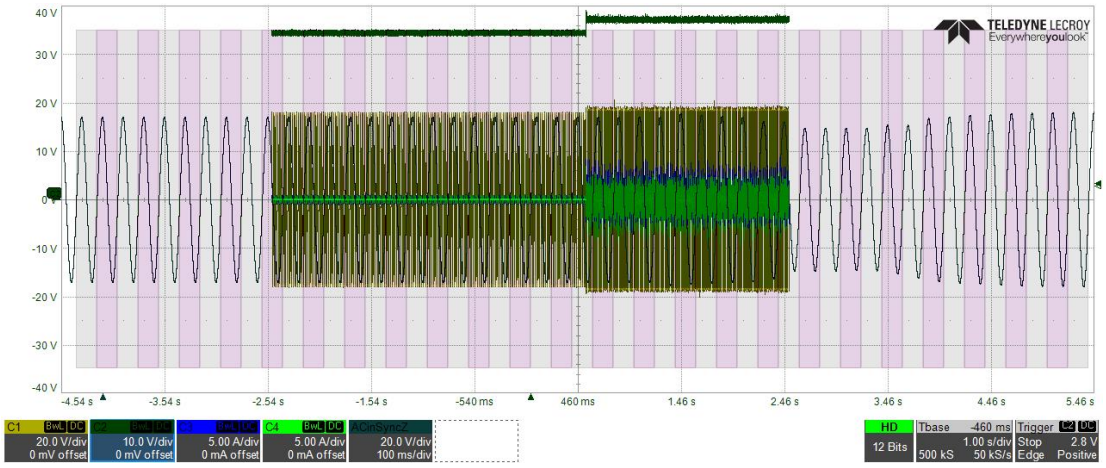

Figure 4.33: Transient Response of Vdc triggering at 48V w.r.t PWM at Output

4.3 Conclusion

As, it has been explained above, the results are complaint to standard and are verified using software as well as at the test-bench in laboratory. It has been observed that, the PLL works well which ensures the Grid Synchronization and it was achieved very well and smoothly. The THD has been reduced to below 5% and verified on test-bench which is the compliant to the Automotive standard. It has also been observed that, the converter is working very smoothly at 10 kHz switching frequency. Hence, the 3-phase Grid Connected Converter firmware is developed and tested on real time hardware.

4.4 Future Works

Furthermore, in future this converter can use to perform the Lab experiments in the class of Laboratory of Power Converters and Electrical Drives. Beside this, the Single-Phase Grid Connected Converted can also be developed using the same board.

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