DELFT UNIVERSITY OF TECHNOLOGY

&

POLITECNICO DI TORINO

Master Degree in Electronics Engineering

Master Degree Thesis

Design a programmable clock generator for unique pixelated Capacitive Biosensor chip

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To my Family and Friends

“Failure is simply an opportunity to begin again,
this time more intelligently”
Henry Ford

Abstract

Label-free biosensors for the study of cell biology have finally come of age. Recent developments have transformed biosensors from low throughput, high maintenance research tools to high throughput, low maintenance screening platforms. In parallel, biosensors have evolved from analytical tools designed exclusively for the analysis of molecular interactions to powerful platforms for the study of cell biology at the whole-cell level. Despite these successes, however, bioelectronics has not yet succeeded in developing a widely applicable all-electronics biosensor platform. This is partly because in the most promising CMOS-based capacitive biosensors, DC or low-frequency signals cannot be used to probe beyond the electrical double layer formed by shielding salt ions, which means that under physiological conditions the sensing of a target analyte is located even at a short distance from the sensor (∼1 nm) is severely hampered.

The PT2 biosensor platform, originally developed by NXP Semiconductors, offers massively parallel, label-free biosensing that can, in principle, be created by combining all-electrical detection with low-cost integrated circuits. It has been demonstrated that high-frequency impedance spectroscopy can be used to detect and image microparticles and living cells under physiological salt conditions. The test uses a large-scale, high-density array of nanoelectrodes integrated with CMOS electronics on a single chip. The response of the sensor depends on the electrical properties of the analyte, enabling impedance-based fingerprinting. The PT2 biosensor platform allows real-time imaging of the dynamic attachment and micromotion of BEAS, THP1, and MCF7 cancer cell lines with sub-micrometer resolution in growth medium. This demonstrates the potential of the platform for label/tracer-free high-throughput screening of e.g. novel drug candidates for cancer treatment.

However, this platform with its current control system, can only reliably operate the biosensor chip up to a switching frequency of 70 MHz. But the chip itself can run up to at least 350 MHz. At this frequency, biosensing measurements will suffer less from false signals caused by non-specific binding of molecules to the nanoelectrodes. Also, at higher frequencies, the clock pulses are distorted too much because of non-optimal impedance matching conditions and

cross-talk in the long clock wires. With a new clock generator chip, we want to unlock this extended frequency range and overcome the problems.

In this thesis, we report the design of a non-overlapping clock generator chip for frequencies up to 500 MHz. The chip also generates an ADC clock for the on-chip ADCs of the PT2 sensor chip, and a reference clock for frequency calibration. The main features of the clock signals are coarsely programmable, i.e. pulse width, non-overlap delay, and clock pulse amplitudes. The non-overlapping clock generator can be configured by writing configuration bits via a serial interface. Apart from the functional parts, the chip also has ESD protection, with special attention for the high-frequency pins, i.e. the ESD protection should not disturb the clock pulses.

Acknowledgment

The realization of this project would not have been possible without the advice and support of many people.

Firstly, I would like to thank my supervisor at the Delft University of Technology, prof.dr.ir. Frans Widdershoven for his assistance and guidance during this entire project, He has done his best to work in the best conditions especially during the pandemic situation, and shared with me many working and thinking methodologies related to analog and digital design. He expressed his support and patience many times when I needed it.

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1 Chapter 1

In this chapter, we briefly introduce the motivation and objectives of the thesis and explain its structure.

1.1 Motivation

The functional unit of life is the cell. The capability to understand cell biology is crucial. In the past decades, advanced molecular biology has made it a routine practice in their laboratory to manipulate a cellular target in living cells. Gene expression is used to increase the amount of specific protein in a cell. While interference RNA is used to suppress or eliminate a specific protein. And mutagenesis to change the structure and functional consequence of the targeted protein [1,2]. There are increasing demands in technologies that not only allow you to investigate cellular response at the whole cell and cell system level, but also enable mechanistic delineation. Label-free biosensors achieve these needs by measuring integrated and phenotypic responses of whole cells with the high temporal resolution, label-free biosensor uses in cell biology are depicted in Figure 1-1 [3,4]. Further, these biosensors empower non-invasive and exceptionally sensitive estimations of various cell reactions, going from cell grip to cell hindrance capacities, signaling, disease, relocation, multiplication and demise, and differentiation.

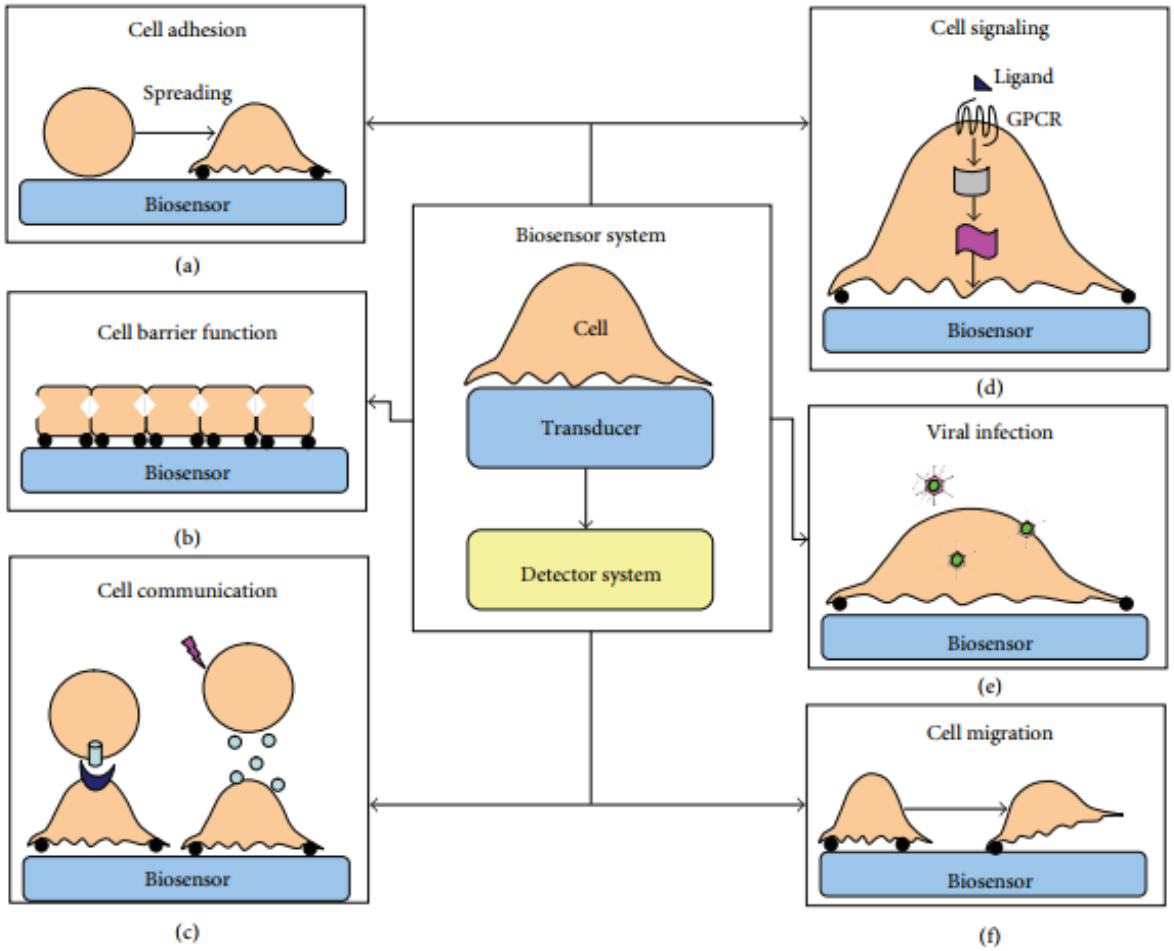

Figure 1-1 Label-free biosensor and its uses for cell biology.
(a) Cell adhesion to a surface; (b) cell barrier functions and regulation; (c) cell-to-cell communication via direct interactions or chemical communication; (d) cell signaling via the receptor activation by an agonist (e)viral infection; and (f) cell migration.

Label-free biosensors utilize a transducer to translate cell reaction into a quantifiable signal (i.e., biosensor signal) [4]. Upon the idea of transducers, label-free biosensors utilized for entire cell detection are generally divided into optical-and electric-based, Figure 1-2. Significantly, there are different types of biosensors, that work is in progress. These include nuclear power microscopy for estimating biomechanics of cells [5, 6], Raman imaging for estimating the creation and association of unsaturated greasy particles in cells [7, 8], furthermore, murmuring display mode biosensors [9] and full mirrors [10] for biosensing. Since these biosensors have restricted throughput for entire cell detecting right now, they are excluded from the discussion.

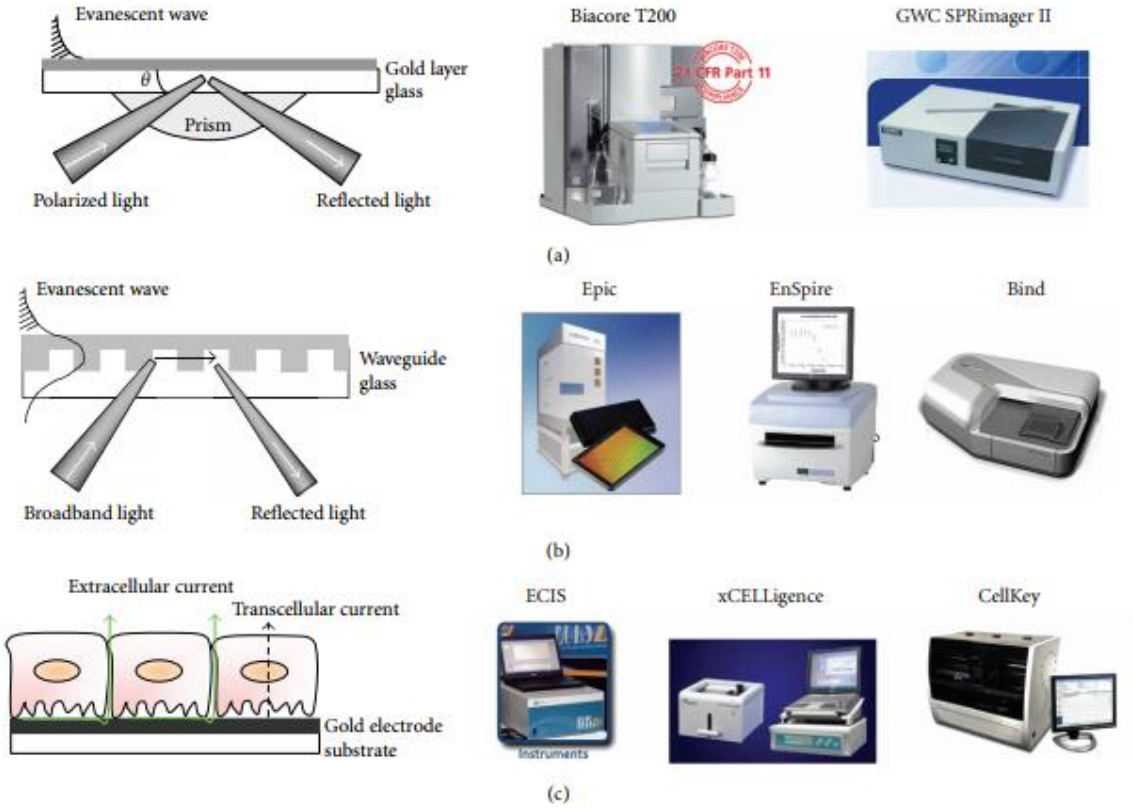

Figure 1-2 Standards and commercial instruments of three particular kinds of label-free biosensors
(a) Surface plasmon resonance, which utilizes light-induced surface plasmon polaritons to detect entire cells. Biacore SPR T200 and GWC SPRImagerII are two instances of commercial models. (b) Full waveguide grinding, which utilizes flawed mode nanograting waveguide construction to produce a transitory wave to sense entire cell reactions. Epic, EnSpire, and Tie are three commercially available instruments. (c) Electric biosensor, which utilizes a low electrolyte impedance interface to detect entire cell reactions. ECIS, xCELLigence, and CellKey are three commercial models.

We describe the realization of an electronic, label-free, temperature-controlled biosensor platform - PT2 Biosensor, Figure 1-3 , that aims to overcome the Debye screening limit over a wide range of electrolyte salt concentrations. It is based on an improved version of a 90-nm CMOS integrated circuit with a nanocapacitor array, readout and A/D conversion circuits, and a field-programmable gate array (FPGA)-based interface board with NIOS II soft processor.

We describe the chip processing, assembly, microfluidics, temperature control system, and as well as the calibration and compensation procedures to reduce systematic errors, which together form a complete quantitative biosensor platform. The capacitance spectra recorded up to 70 MHz are shown and successfully compared with predictions made by numerical

simulations using the finite element method (FEM) in the Poisson drift-diffusion formalism. They show that the chip can achieve a high upper operating frequency, overcoming the low-frequency Debye screening limit at physiological salt concentrations in the electrolyte and detecting events occurring beyond the electrical double layer. In addition, calibrated multi-frequency measurements allow quantitative recording of capacitance spectra, the features of which can reveal new properties of the analytes. With the scalability of the electrode dimensions, the electrode spacing, and the size of the array, this sensing approach is quite generally applicable, even in a non-biological context (e.g. gas sensing) [11].

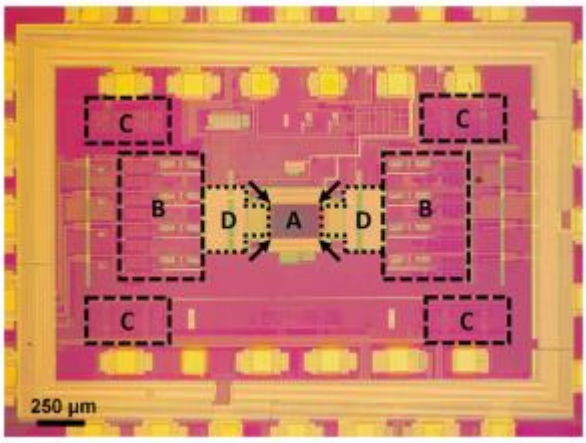

Figure 1-3 PT2 biosensor chip

These platforms, that enable massively parallel, label-free biosensing, can in principle be created by combining purely electrical detection with low-cost integrated circuits. Examples include field-effect transistor arrays used for mapping neuronal signals [12-14] and sequencing DNA [15,16]. Despite these successes, however, bioelectronics has not yet succeeded in developing a widely applicable biosensor platform. This is partly because DC or low-frequency signals cannot be used to probe beyond the electrical double layer formed by the screening salt ions [17-20], which means that under physiological conditions, detection of a target analyte located even at a short distance from the sensor (~1 nm) is severely hampered. Here we demonstrate that radiofrequency impedance spectroscopy can be used to detect and image microparticles and live cells under physiological salt conditions. The assay uses a large, high-density array of nanoelectrodes integrated with CMOS electronics on a single chip. The response of the sensor depends on the electrical properties of the analyte and enables impedance-based fingerprinting. The platform allows to image the dynamic attachment and micromotion of BEAS, THP1, and MCF7 cancer cell lines in real-time with submicron

resolution in the growth medium. This demonstrates the potential of the platform for label and tracer-free high-throughput screening of anti-tumor drug candidates [12].

The nanoelectrodes are row-wise selectable and read out individually column by column, Figure 1-4 (left).When immersed in the fluid they form metal/liquid nano-capacitors. A selected row of nanocapacitors is repeatedly charged/discharged at 50 MHz with a modulation voltage step V_{mod} = 245 mV via two single MOS transistors Figure 1-4 (right), using all unselected nanoelectrodes in parallel as the counter electrode. The charge/discharge current of a selected nanocapacitor is integrated over several cycles and read out via on-chip analog-to-digital converters. In this way, we achieve high-frequency operation with attofarad resolution (standard deviation of ~1 aF at a modulation frequency of 50 MHz and a frame rate of 4.8 Hz, as used here). We express the measured response signal as the equivalent switching capacitance C_{exp}, defined as the integrated charge per charge/discharge cycle divided by the modulation voltage step [12]. This approach simultaneously exploits three strengths of integrated circuits: high frequency, miniaturization, and large-scale integration. Although other promising concepts have been reported [21–25], this is currently the only existing biosensor platform capable of real-time, massively parallel, high-frequency impedance measurements and imaging with submicron attofarad resolution on the submicrometric scale.[12]

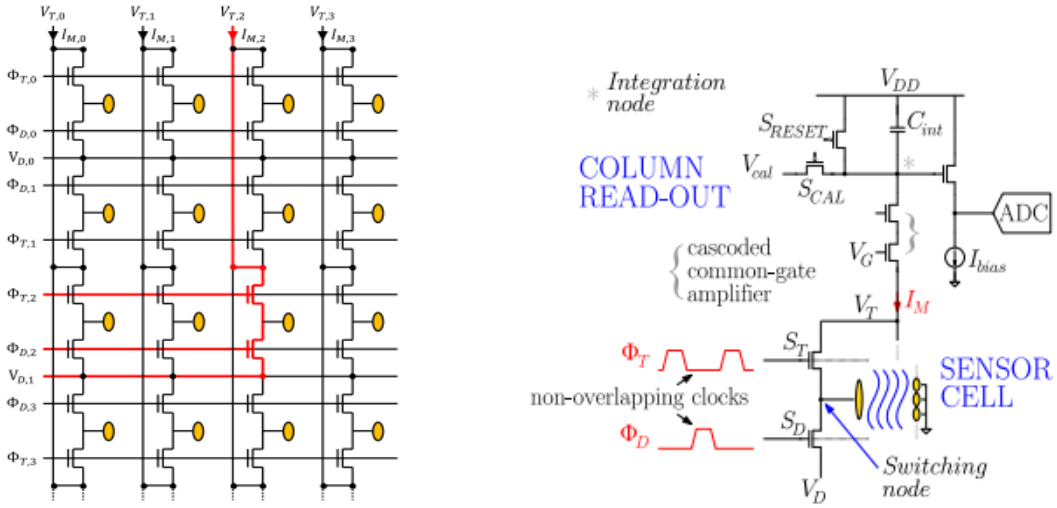

Figure 1-4 Left: Biosensor 256 × 256 nanoelectrode array with column-wise selectable and row-wise readable sensor cells. The golden ellipses are the sense electrodes. A sensor cell and its selection and read paths are highlighted in red. Right: Sensor cell and column read-out circuit.

As the first proof of concept, microspheres with a radius of 4.4 µm are deposited on the surface of the array, with each sphere spanning multiple contiguous electrodes. Figure 1-5 shows

experimental time traces recorded from three adjacent electrodes during sedimentation of the microspheres. A microsphere induces a position-dependent change ΔCexp(experimental) in electrode switching capacitances. To quantitatively elucidate the mechanism of signal transduction, extensive three-dimensional finite element simulations based on the Poisson-Nernst-Planck formalism are done. Figure 1-6-left shows a map of the AC potential amplitude generated by three electrodes in 150 mM salt at a DC bias of zero and a modulation frequency of 10 kHz, typical of conventional electrochemical impedance spectroscopy [26,28]. In this case, the electrical double layer (EDL) is capable of rearranging so quickly that it instantaneously screens the electrode potential. The AC electric field thus decays exponentially from the electrode surface with a decay length equal to the equilibrium Debye screening length λ_D (~0.8 nm at physiological salt concentrations) [29]. Analogous to field-effect detection, the electric field, in this case, is only affected by the presence of a dielectric microsphere when the distance between the electrode and the sphere is of the order of λ_D or less (central electrode in Figure 1-5 and Figure 1-6) measured experimentally. On the other hand, at modulation frequencies above a cutoff frequency $f_l = 1/(2\pi R_E(C_S + C_E))$ that depends on the salt concentration, where R_E and C_E are the spreading resistance and the spreading capacitance of the electrode, respectively, and C_S is the double-layer capacitance, the EDL no longer fully shields the applied potential (see Figure 1-6-right). The electric field then penetrates radially into the solution, as shown by the potential map for 50 MHz, a frequency well above the limit for probing beyond the EDL ($f_l \approx 3$ MHz at 150 mM salt concentration for these nanoelectrodes). This frequency-dependent sensitivity can be directly observed experimentally. Figure 1-7 shows two-dimensional maps of the measured response ΔC_{exp} of the nanoelectrode array to sedimented dielectric microspheres at three different modulation frequencies. At 1.6 MHz, i.e. below the cut-off frequency f_l, the microspheres are undetectable except when they land directly on an electrode (red circle). When the frequency is increased to 7.1 MHz and 50 MHz, the microspheres have an increasingly larger apparent diameter, showing that the EDL shielding has been overcome.

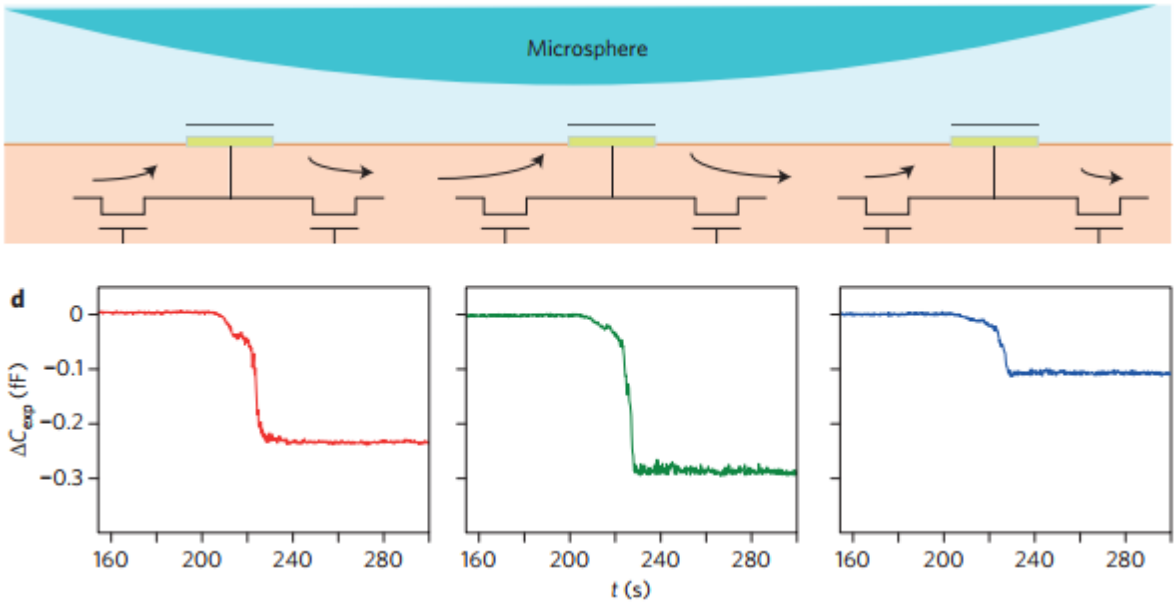

Figure 1-5 Time traces recorded from three contiguous nanoelectrodes during sedimentation

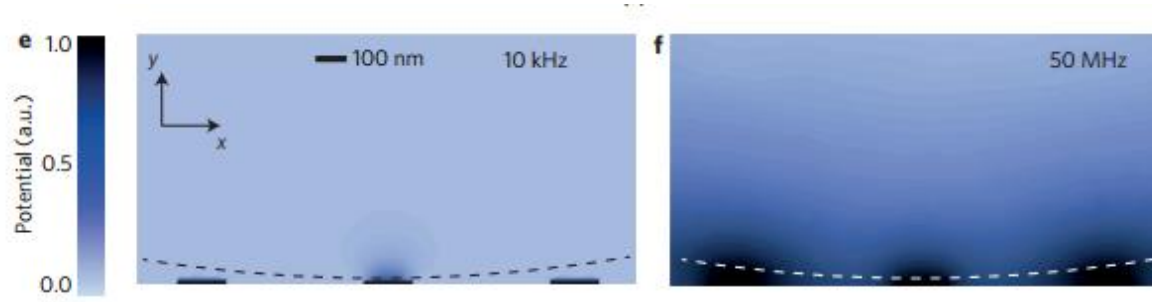

Figure 1-6 Maps of the AC potential amplitude generated by three electrodes at 150 mM salt concentration at zero DC bias and 10 kHz and 50MHz modulation frequencies

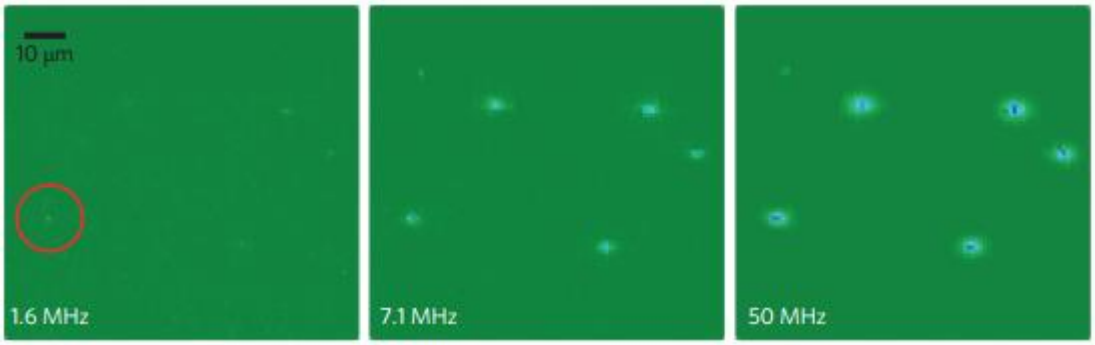

Figure 1-7 Two-dimensional maps of the measured response ΔCexp at different modulation frequencies

A dielectric sphere replaces the high permittivity electrolyte by a medium of lower permittivity, thereby repelling the electric field lines and decreasing the nanoelectrode capacitance.

Conducting sphere showed the opposite effect as they attract the electric field and increase the nanoelectrode capacitance. This property was used to discriminate the different particles. Figure 1-8 shows experimental ΔC_{exp} maps of a mixture of dielectric (latex) and conducting (gold-coated polystyrene) microspheres (both 2.5 µm radius). The apparent particle sizes are similar for both microspheres ($\sigma \approx 1.7$ µm), but the conductive microparticles show an increase in capacitance ($\Delta C_{exp} > 0$) instead of a decrease. Once again, the experimental responses, in particular the sign changes, are well reproduced by the simulations (Figure 1-8c), thus proving the ability of the physical model to capture the features of the experiment. This capability of discriminating between particle-based on their intrinsic electrical properties is unique to high-frequency spectroscopy [12].

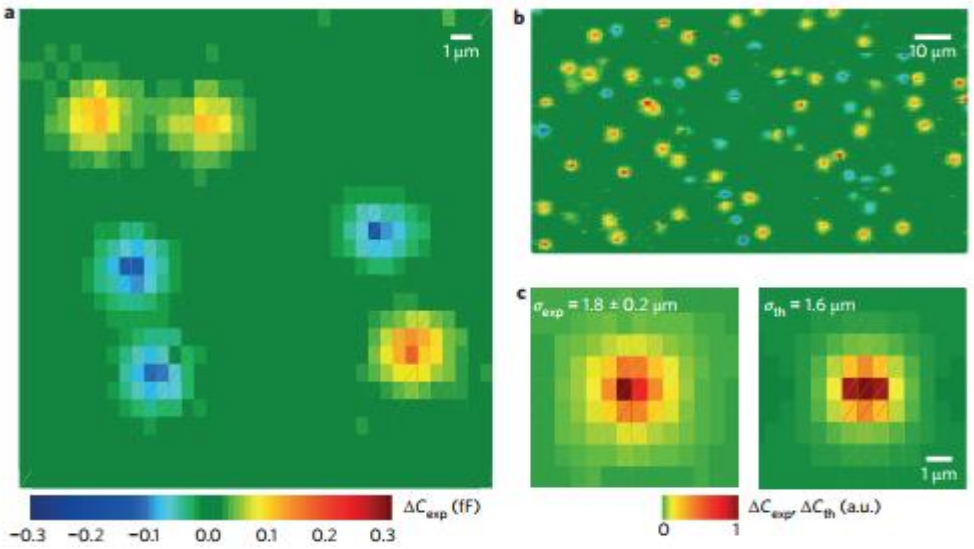

Figure 1-8 a and b: Response to conducting (yellow/orange) and dielectric spheres (cyan/blue). c: comparison of measured (left) and simulates (right) apparent particle sizes.

1.2 Objective

From the explanations, it is evident that modulation frequency plays a vital role in the identification of cells. Now the described biosensor is working up to a frequency of 70 MHz. But the chip itself can run up to 500 MHz where the biosensor will show its maximum potential. The theory predicts that at frequencies above 360 MHz capacitive biosensor measurements

suffer less from disturb signals caused by nonspecific binding of molecules to the nanoelectrode. The maximum frequency of the current biosensing system is limited to 70 MHz by the off-chip clock generator and its connecting wires to the sensor chip . Therefore, we need a clock generator that works up to 500 MHz, and that has a small foot print so that it can be mounted immediately next to the sensor chip. For frequencies up to 90 MHz, the sensor chip can derive an internal clock for the on-chip A/D converters from the non-overlapping clocks that operate the switching transistors of the sensor cells. But, at higher frequencies, an external ADC clock up to 45 MHz must be supplied. For calibrating the non-overlapping clock frequency, a lower-frequency reference clock must be derived from the non-overlapping clock signal that can be measured easily at a remote location without suffering from stringent impedance matching constraints at high frequencies.

The clock generator must generate non-overlapping clocks with coarsely programmable frequency, non-overlapping delay, rising and falling edges, and variable amplitude (because the biosensor requires clock signals of 0.7-1.2 V). (Fine-grain programmability of the frequency is not needed because capacitive biosensor signals don’t have sharp resonance features.)

I addition to this, the chip must have basic ESD protection, with special attention to the high-frequency pins (because it should not disturb the clock pulses). The chip must be packaged in a tiny package (e.g. QFN24) because it must be placed as close as possible to the biosensor chip on a new PCB.

1.3 Structure

In Chapter 2 the circuit topology to design a programmable clock generator chip for a unique Pixelated Capacitive Biosensor chip will be presented and analyzed. The analysis of this chip will begin using some simplifications, and the necessary working conditions to obtain high efficiency will be established. Then, the equations that rule the behavior of the circuit will be provided and the block diagram and functional specifications will be presented.

Once the block diagram and functional specifications are determined, each block will be designed and explained. Foremost the programmable Ring oscillator and Frequency Divider with Multiplexer will be detailed in Chapter 3.

In Chapter 4 the design of the non-overlapping delay line and the amplifier will be specified, and the final circuit will be tested on different load conditions and frequencies to verify the results.

Finally, the ESD and packaging of the chip will be described, the precautions taken to place the high-frequency pins, supply voltages, separate the analog and digital domain, will be presented in Chapter 5.

2 Chapter 2

In this chapter, a lumped model of the biosensor will be introduced. The working principle of the clock generator are explained. The importance of signals produced by the clock generator will be briefly discussed. The functional specification of each block will be analyzed along with the simplified block diagram for the clock generator.

2.1 Implementation

Our biosensor chip consists of 65,536 individually addressable gold-copper nanoelectrodes of 90 nm nominal radius. They are arranged in a 256×256 array with 550nm×720nm, 600nm×720nm, or 600nm×890nm column and row pitches. The chip works as charge-based capacitance measurement (CBCM) [30] at switching frequencies up to 300 MHz.

The CBCM is implemented using two switching transistors S_T and S_D per sensor cell, which repeatedly charge and discharge the capacitance of a nanoelectrode to potentials V_T and V_D, respectively, connected to the switching node. S_T and S_D are controlled by two non-overlapping clocks Φ_T and Φ_D, respectively. The frequency and pulse shapes are programmable. To avoid interference in ground return paths of the chip, Φ_T and Φ_D are imported on the chip as the 2 differential clock pairs, which are routed differentially to the row selection circuitry alongside the array, where the non-inverted clock signals are passed on to a selected row of sensor cells. The clock waveforms for measurements at 50 MHz switching frequency have 1 ns rise and fall times, 7 ns high times, and 10 ns delay between the Φ_T and Φ_D pulses. So, the clock generator must have these properties too. The Φ_{TB} and Φ_{DB} pulses are the exact inverse of Φ_T and Φ_D pulses, respectively. This way, the net high-frequency clock components entering the chip are exactly zero. This is important to avoid high-frequency return paths through other bond pads than the clock pads [11].

2.2 Lumped Model

The basic operation principle of a sensor cell of the biosensor chip PT2 can be seen in Figure 2-1. It works as a charge pump by repetitively charging and discharging the nanoelectrode capacitor C. The resulting charge pumped from the charge node at potential V_T to the discharge node at potential V_D is a measure for capacitance C. It can be determined by measuring the average charge pumping current flowing into the charge node.

$$I = f_p(C + C_P)(V_T - V_D), \tag{1}$$

where f_p is the switching or pump frequency, and C_P is the parasitic capacitance of the switching node.

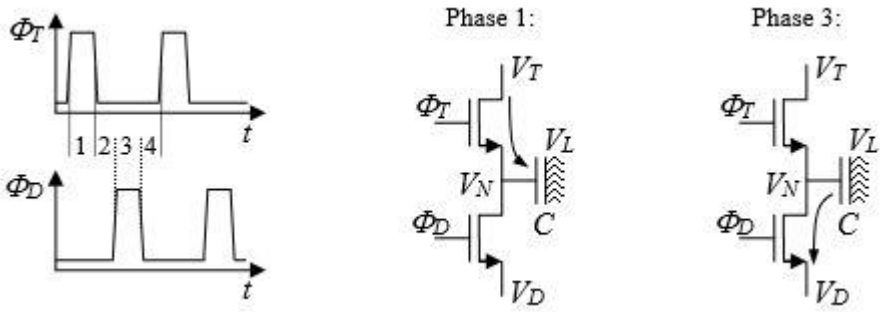

Figure 2-1 The 4 phases of the non-overlapping clock for charging (1) and discharging (3) of the nanoelectrode capacitor C

To avoid a short circuit path between the charge and discharge nodes the 2 switch transistors should never be on simultaneously. Therefore, the charge and discharge phases 1 and 3, respectively, are separated by 2 separation phases 2 and 4, respectively, in which both transistors are off.

The nanoelectrode capacitance is not pure. A more realistic model consists of a capacitor C_S, representing a self-assembled monolayer or/and a Debye screening layer at the nanoelectrode surface, in series with a parallel section of a capacitor C_E and a resistor R_E, representing the permittivity and resistivity of the electrolyte, respectively.

Figure 2-2, 2-3, 2-4, and 2-5 show the equivalent circuit of the sensor cell for the 4 different timing phases. Equations 2 – 15 describe the transients taking place during the switching phases 1 – 4. Equations 16 and 17 are periodic boundary conditions for stationary switching. The notation "$t_i - 0$" is used to represent a moment in time infinitesimally before t_i.

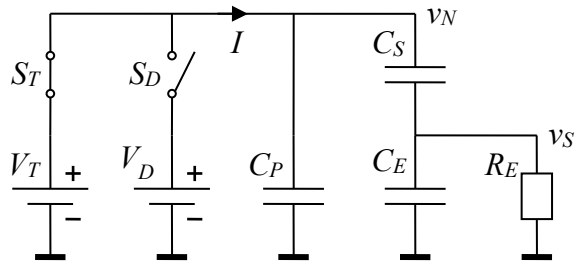

Figure 2-2 Bias conditions in phase 1 ($0 < t < t_1$)

$$v_S(t_1) = \left(v_S(-0) + \left(V_T - v_N(-0)\right) p_a\right) e_1 \tag{2}$$

$$p_a = \frac{C_S}{C_S + C_E} \tag{3}$$

$$e_1 = \exp\left(-\frac{t_1}{\tau_a}\right) \tag{4}$$

$$\tau_a = R_E\left(C_S + C_E\right) \tag{5}$$

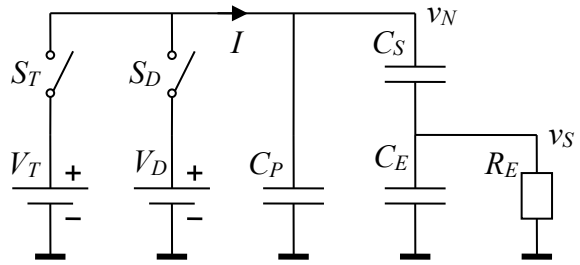

Figure 2-3 Bias conditions in phase 2 ($t_1 < t < t_2$)

$$v_S(t_2 - 0) = v_S(t_1) e_2 \tag{6}$$

$$e_2 = \exp\left(-\frac{t_2 - t_1}{\tau_b}\right) \tag{7}$$

$$\tau_b = R_E\left(\frac{C_S C_P}{C_S + C_P} + C_E\right) \tag{8}$$

$$v_N(t_2 - 0) = V_T + (v_S(t_2 - 0) - v_S(t_1))\, p_b \tag{9}$$

$$p_b = \frac{C_S}{C_S + C_P} \tag{10}$$

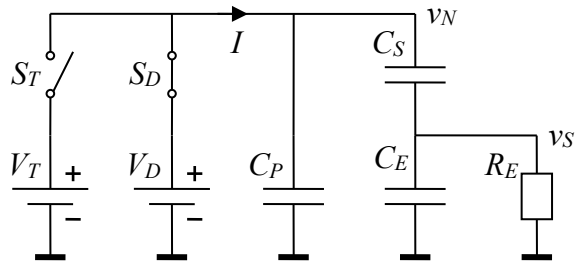

Figure 2-4 Bias conditions in phase 3 ($t_2 < t < t_3$)

$$v_S(t_3) = (v_S(t_2 - 0) + (V_D - v_N(t_2 - 0))\, p_a)\, e_3 \tag{11}$$

$$e_3 = \exp\left(-\frac{t_3 - t_2}{\tau_a}\right) \tag{12}$$

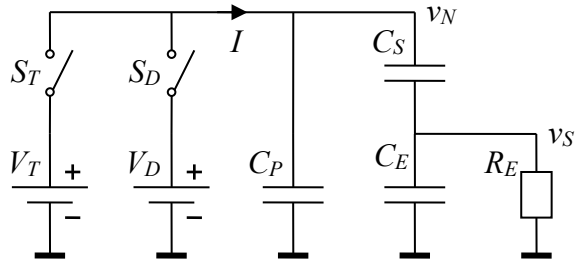

Figure 2-5 Bias conditions in phase 4 ($t_2 < t < t_4$)

$$v_S(t_4 - 0) = v_S(t_3)\, e_4 \tag{13}$$

$$e_4 = \exp\left(-\frac{t_4 - t_3}{\tau_b}\right) \tag{14}$$

$$v_N(t_4 - 0) = V_D + (v_S(t_4 - 0) - v_S(t_3))p_b \tag{15}$$

$$v_S(-0) = v_S(t_4 - 0) \tag{16}$$

$$v_N(-0) = v_N(t_4 - 0) \tag{17}$$

From these equations it follows:

$$v_S(t_1) = (V_T - V_D)\frac{p_a e_1(1 - e_3(e_4 + (1 - e_4)p_b p_a))}{1 - (e_2 + (1 - e_2)p_b p_a)e_3(e_4 + (1 - e_4)p_b p_a)e_1} \tag{18}$$

Finally, the charge

$$Q_{Charge} = C_P(V_T - v_N(-0)) + C_S(V_T - v_S(t_1)) - C_S(v_N(-0) - v_S(-0)),$$

transferred from the charge node to the discharge node during 1 switching period, can be calculated, leading to the following charge pump efficiency factor:

$$\begin{aligned}\gamma &= \frac{Q_{Charge}}{(C_S + C_P)(V_T - V_D)} \\ &= 1 - p_b p_a \frac{e_1(1 - e_3(e_4 + (1 - e_4)p_b p_a)) + e_3(1 - e_1(e_2 + (1 - e_2)p_b p_a))}{1 - e_1(e_2 + (1 - e_2)p_b p_a)e_3(e_4 + (1 - e_4)p_b p_a)}\end{aligned} \tag{19}$$

Similar to equation 1, the corresponding average charge pumping current is:

$$I = f_p(C_S + C_P)(V_T - V_D)\gamma \tag{20}$$

Some interesting limiting cases are the small duty cycle limit

$$\gamma \to \frac{1 - p_b p_a}{1 + p_b p_a},\ e_1 \to 1,\ e_2 \to 0,\ e_3 \to 1,\ e_4 \to 0, \tag{21}$$

the high pump frequency limit

$$\gamma \to 1 - p_b p_a,\ e_1 \to 1,\ e_2 \to 1,\ e_3 \to 1,\ e_4 \to 1, \tag{22}$$

and the 50% duty cycle limit

$$\gamma = 1 - p_b p_a \frac{2e_1}{1+e_1},\ e_1 = e_3 = \exp\left(-\frac{t_4}{2\tau_a}\right),\ e_2 = e_4 = 1 \tag{23}$$

From equation 19 it follows that the sensitivity of the charge pump current I to changes in the electrolyte properties (mediated via changes in C_E and R_E) proceeds entirely through γ. In particular, the relative change in the charge pump current is given by

$$\frac{\delta I}{I} = \frac{\delta \gamma}{\gamma} \tag{24}$$

From equation 1 the importance of the frequency in the potential of the biosensor is evident. As explained in the introduction, the clock generator signals must be coarsely programmable, i.e. pulse width, selectable non-overlapping delay, and low & high voltage levels (rising and falling edge times are kept fixed). And we must have a differential clock to avoid the cross talk and parasitic ground return paths. With all the requirements in mind, the preliminary block diagram is explained below.

2.3 Block Diagram

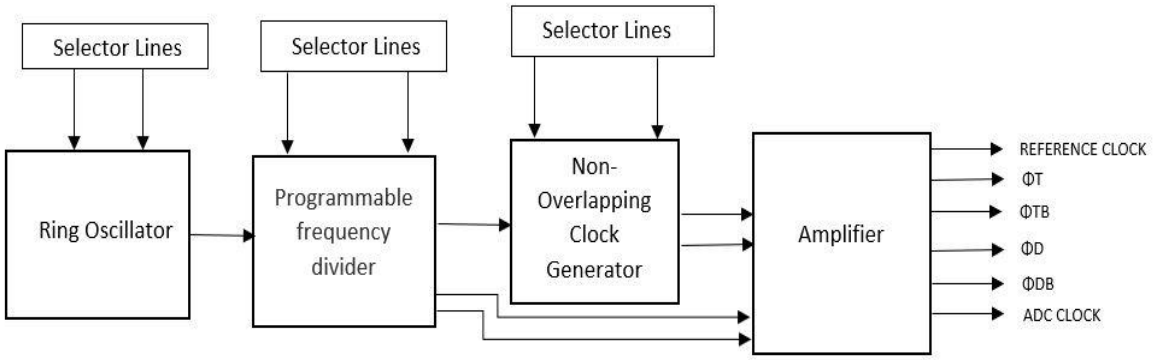

Figure 2-6 Block diagram of the clock generator

The system (Figure 2-6) consists of a ring oscillator that generates the master clock signal. It has 4 selectable loop delays to produce 4 different frequencies between 600 MHz to 1.8GHz.

These frequencies are divided by a selectable power of 2 by a programmable asynchronous frequency divider, consisting of chain of 9 D Flip Flops. From this, we also generate the clock signal for the ADC, ranging from 20 to 45 MHz, and the reference clock for the frequency calibration. The non-overlapping block receives the divided clock signal and generates two non-overlapping clock signals. It is also programable as we can select the delay we need to separate the two signals so that the cross talk is avoided. The Amplifier block is used to vary the amplitude of the clock signal ranging from 0.7 to 1.2 V.

This block diagram explains the complete blocks used in generating the 6 clock signals needed for the biosensor chip. The functional specification of each block is explained as follows.

Biosensor Chip

- Temperature range 0 – 85 degrees C
- Supply voltage (e.g. 3.3V or 5 V)
- Pins + drive strength + output impedance + CLK_T/D amplitude, and supply pins
- The internal supply voltage generation

Ring Oscillator

- Frequency Tuning Range 0.6-1.8 GHz. – extra tuning range to compensate for PVT corners; specify tunings steps; also include a method to calibrate frequency.
- It should be programmable (Selector Lines)
- Supply Voltage 1.8V
- Low Power Consumption
- Stability
- Sensitivity to supply voltage ripples and drops

3 Chapter 3

In this chapter, we will discuss the ring oscillator and the frequency divider circuits developed from the conventional circuits for specific use as programmable ring oscillators and frequency dividers. The design is performed using TSMC 180nm process design kit.

3.1 Programmable Ring Oscillator

Integrated circuits have entered the era of System on a Chip (SOC), meaning that millions of transistors can be connected in a single chip. One of the most developed integrated circuits is the ring oscillator, which consists of a closed loop of an odd number of inverting delay stages whose outputs toggle between two voltage levels, which represent high and low. Although foundries use ring oscillators on each semiconductor wafer to monitor gate delay and the speed vs power product of manufactured MOS inverters, they are mainly used in the construction of Phase-locked loop (PLL) signal generators.

A ring oscillator is an integral part of most electronic systems. The importance of ring oscillators in the electronics industry is undeniable. With the immense and rapid developments in the field of VLSI, their importance has also increased. Ring oscillators have held this role since the earliest days of MOS IC technology because they are simple to build, always oscillating, and easy to measure. Compared to their LC-VCO counterparts, ring oscillators have the advantage of small size, high integration, polyphase outputs, and wide oscillation range [31]. A ring oscillator is a closed-loop system consisting of an odd number of stages of identical inverters (or other inverting gates) forming a feedback loop. An even number of transistors in a closed loop cannot be used to design a ring oscillator because it will settle in one of two possible static states. The even-numbered design can be considered as a memory element and serves as the basic building block of SRAM. The ring oscillator becomes a better choice in low-cost CMOS digital processes and scales with technology, promising higher operating frequencies for deep submicron technologies. By reducing the size of transistors and

interconnects, more circuits can be fabricated on a silicon wafer, making each circuit cheaper. Since the CMOS inverter does not draw significant current from the power source in either operating state, the DC power dissipation of the circuit is almost negligible.

Ring oscillators, which are constructed with a chain of delay stages, have attracted considerable interest because of their many useful features. These attractive features are: (i) they can be designed using modern integrated circuit technology (CMOS, BiCMOS), (ii) they can oscillate at low supply voltage, (iii) they can generate high-frequency oscillations at low power consumption, (iv) they can be electrically tuned, (v) they can provide a wide tuning range, and (vi) they can provide polyphase outputs due to their basic structure. These outputs can be logically combined to realize multiphase clock signals, which are of great use for several applications in communication systems however they also has their limitations (i) supply sensitivity, (ii) process voltage temperature (PVT) sensitivity ,(iii) suffers from poor phase noise performance(low Figure of Merit(FOM)).

In the ring oscillator circuit, the feedback from the last output to the input causes the oscillations as shown in Figure 3-1[31].

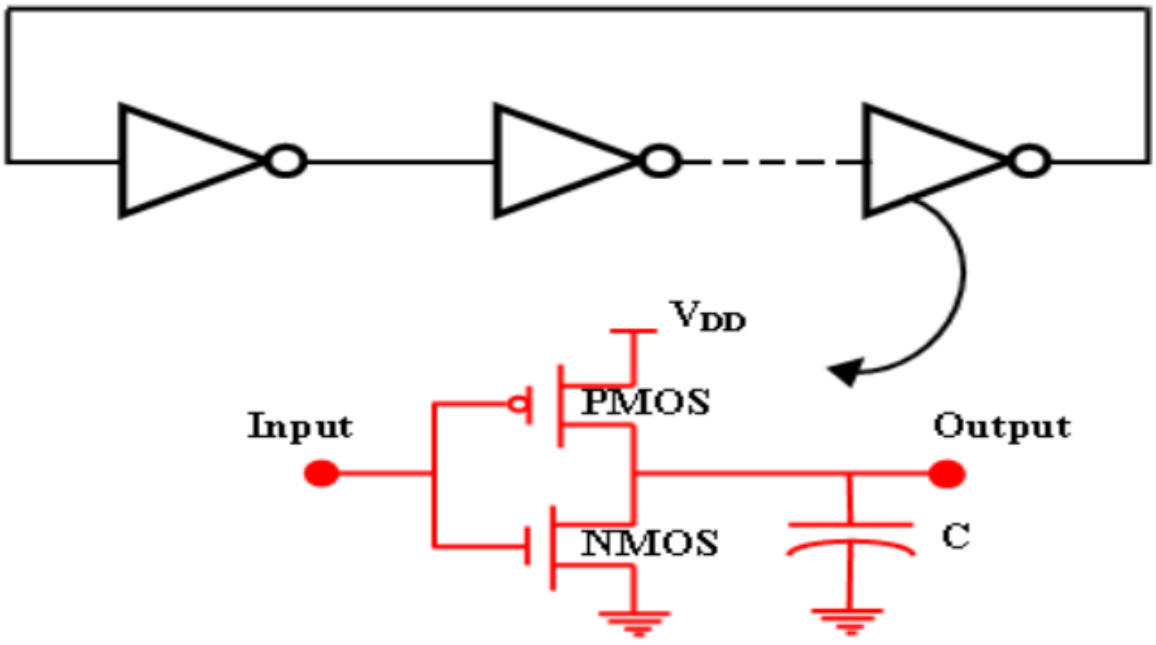

Figure 3-1 Hardware structure of single-ended inverter-based ring oscillator

An odd number of inverter stages are used to achieve the effect of a single inverter amplifier with a negative feedback gain greater than 1 so that the static output is opposite to the input. The ring oscillator needs only one power source to operate above the threshold voltage, and then the oscillations starts spontaneously by amplifying the initial noise.

3.1.1 Oscillation Frequency

To achieve self-sustaining small-signal oscillations, the ring must have a phase shift of 2π and a voltage gain of one at the oscillation frequency. In an N-stage ring oscillator, each stage provides a phase shift of π /N and the dc inversion provides the remaining phase shift of π. Therefore, the oscillating signal must pass through each of the m delay stages once to achieve the first π-phase shift in a time of N $*t_d$ and it must pass through each stage a second time to obtain the remaining phase shift in a time of 2N* t_d. Thus, the oscillation frequency is given by:

$f_0 = \frac{1}{2Nt_d}$,

where t_d the gate delay of each delay stage, and N is the number of stages. The oscillation frequency of a ring oscillator can be determined using the expression of t_d, which depends on the circuit parameters. However, the main difficulty in determining t_d arises from the nonlinearities and parasitics of the circuit. Increasing the oscillation frequency can be achieved in two ways: by reducing the propagation delay of the inverter stages or by reducing the number of stages used in the ring structure. The delay of each stage depends on the circuit structure and process parameters.

Reducing the number of stages in the ring structure is attractive not only because of the increase in operating speed but also saving of area when implemented in ICs. However, the number of available multiphase outputs decreases with the reduction of the number of stages.

The ring oscillator needed for the clock generator chip must be frequency selectable so an oscillator built with inverters can’t be used, and the implementation will include NAND gates.

A NOT gate is formed by connecting the inputs of a NAND gate together. Since a NAND gate corresponds to a AND gate followed by a NOT gate, only the NOT gate remains after connecting the inputs of a NAND gate. Also, it can be achieved by giving VDD to one pin all the time Figure 3-2.

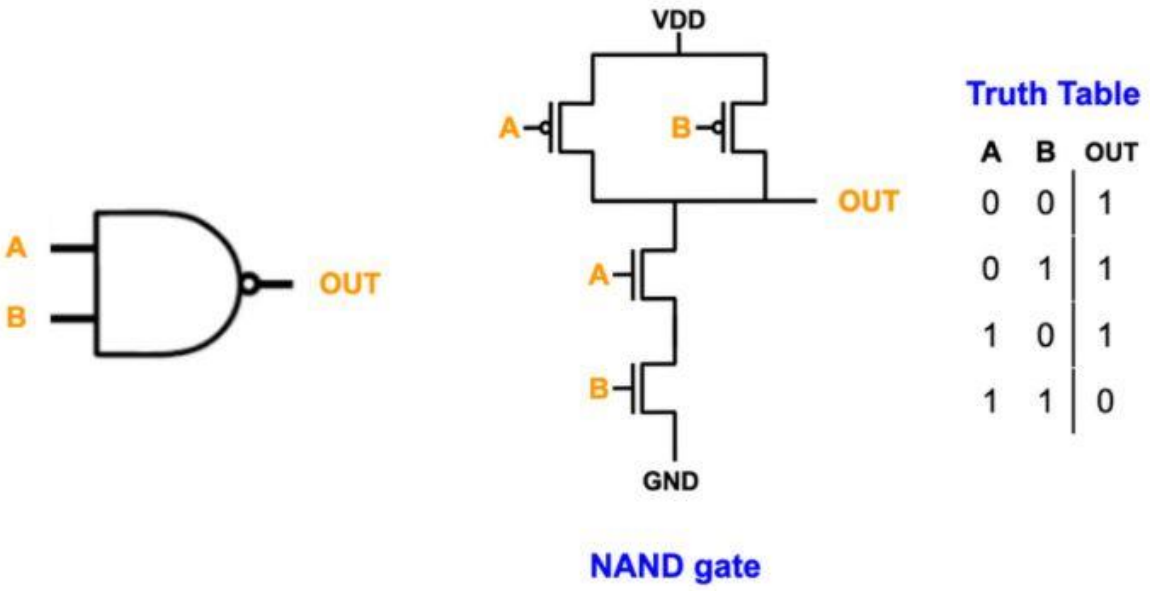

Figure 3-2 Gate-level and transistor-level representation of NAND2 and its truth table.

This way we can make a ring oscillator using NAND gates. But for selecting each of the delay path we need another method.

3.2 Digitally Controlled Delay Lines

Digitally Controlled Delay Lines (DCDLs) are used to create an intentional delay for each clock distribution network. They define the timing reference for the movement of data through the thermometric code obtained from a timing digital converter. This digital code makes the delay lines digitally controllable. The glitches are the momentary unwanted changes in the output and these are seen. Due to the shortcomings of inverter-based delay lines, NAND-based delay lines are preferred. The conventional NAND-based DCDLs suffered from glitches when the number of control codes increased beyond one due to propagation over multiple paths. The

glitches are momentary undesired changes in the output. This arise due to changing selection bits in a running oscillator.

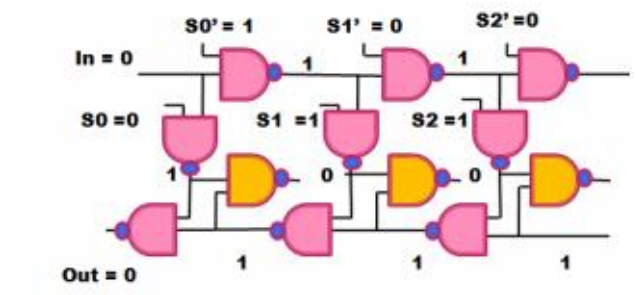

Figure 3-3 Glitching when Delay Path is one

When the delay path is one: Figure 3-3 shows the glitching activity. The orange NAND Gate is used to are use to balance the loads, i.e. to load each of the NAND gates by 2 other NAND inputs. When the delay path is one; S0 = 0, S1 = 1 under the condition that Si = 0 for i < c and Si= 1 for i ≥ c, where S represents the control bit, i is an integer between 1 and n, and c is the control code. In this case, no interference occurs because there is only one path from input to output, but the problem occurs when multiple paths are involved.

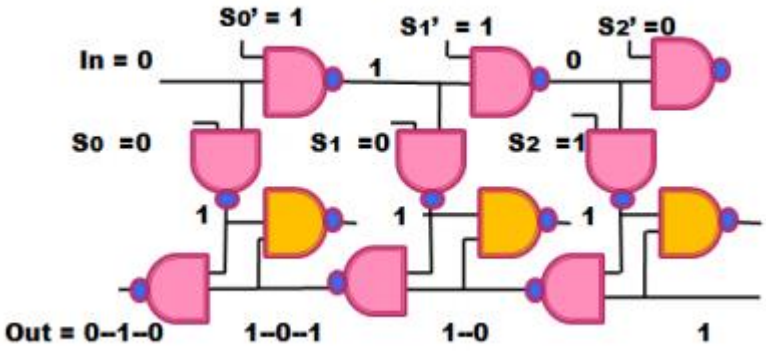

Figure 3-4 Glitching when Delay Path increases by one

When the delay path is increased by one: Figure 3-4 shows the glitching activity when the control code is increased by more than one. The control bit at this stage would be S0 = 0, S1 = 0, S2 = 1. Therefore, there is a momentary change in the output, which results in a glitch due to the intrusion of multiple paths between input and output. For example, if the input is '0', the output should remain at 0 in the non-inverting topology, but it goes to 1 and then returns to 0. Therefore, the intermediate signals contribute to the glitch [32].

Digitally Controlled Delay Lines can produce short delays. And all gates to the right of the selected delay path do not switch. As the S1' and S2' is 0. This limits the total power dissipation. And since there is no activity in the unselected delay paths, they cannot crosstalk to the selected path (e.g., by drawing switching current spikes from the supply line). If we use the cross-coupled NAND gates, we can ignore the orange load-balancing dummy NAND gates in figure 3.3, since we only need to select a single path for the clock signal. We also do not need to worry about glitches, since we will not change the delay code during operation. This has the additional advantage that the rising edge of the enable input immediately start the oscillation (instead of waiting until the oscillator starts oscillating by amplifying the initial noise). The possible implementation of a programmable ring oscillator is shown inFigure 3-5.

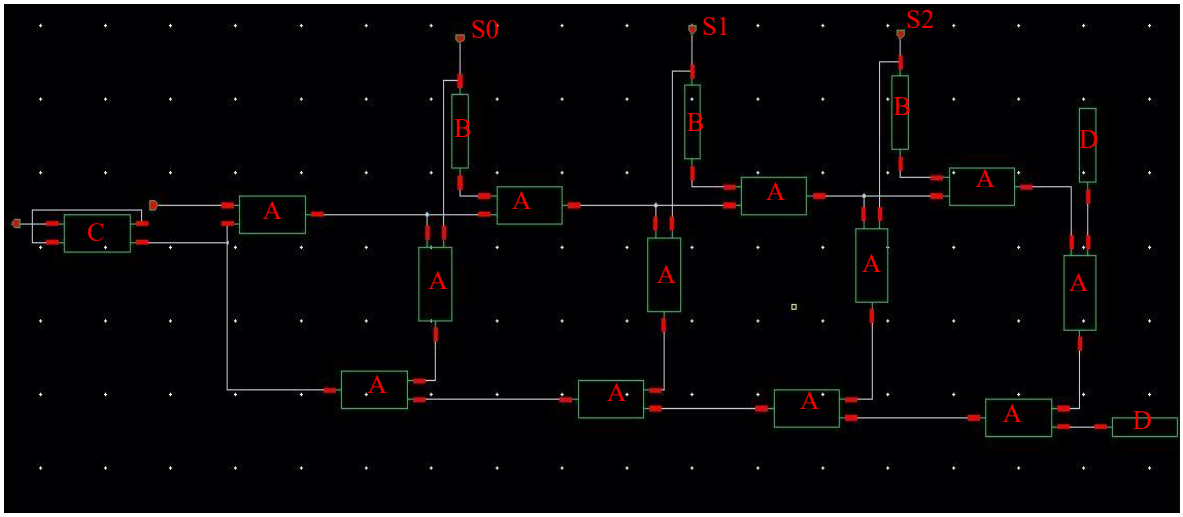

Figure 3-5 Ring Oscillator with selectable path. A: NAND gate, B: inverter, C: D Flip Flop and D: GTIE Cell

The ring oscillator working depends on the selection bits S0 S1 S2. When S0 is '1' and S1, S2 '0' the first three NAND gates in the loop from left are turned on and the remaining path is unselected with the help of an inverter which gives 0 to the NAND gate. This path gives the highest frequency as the delay is only due to the 3 NAND gates. Similarly, if S1 is '1' and S0, S2 is 0 then the second path is taken by the signal, and the frequency decrease as the delay increases. Here we have the delay of 5 NAND gates. To avoid direct connection of the NAND gate to VDD Tie cells are used to give a high signal in the last path. Thereby we can protect the transistor from getting damaged by sudden overshoots in the supply voltage. As we need to feed the frequency divider with frequencies ranging from 0.6 - 1.8 GHz. Divide-by-2 circuit is needed to make a master clock with a duty cycle of 50%. Without the divide-by-2 circuit,

the duty cycle can deviate from 50%. We use a divide-by-2 circuit consisting of the D Flip Flop represented as ‘C’ in the figure. To store the selection bits, we use shift registers.

3.3 Shift Registers in Digital Logic

D Flip Flops can be used to store a single bit of binary data (1 or 0). However, to store multiple bits of data, we need multiple flip-flops. N flip flops are connected in a chain to store n bits of data in a shift register.

The bits stored in a shift register can be moved within the register, and in and out of the register, using clock pulses. An n-bit shift register can be formed by connecting n flip-flops, where each flip-flop stores a single bit of data. Registers that shift the bits to the left are called "shift left registers”. Registers that shift the bits to the right are called "shift right registers".

There are 4 types of shift registers:

1. Serial In Serial Out
2. Serial In Parallel Out
3. Parallel In Serial Out
4. Parallel In Parallel Out

3.3.1 Serial-In Parallel-Out shift Register (SIPO)

The shift register that provides serial input (one bit at a time over a single data line) and produces parallel output is called a serial-in parallel-out shift register.

The logic circuit in Figure 3-6 illustrates a serial-in parallel-out shift register. The circuit consists of four connected D flip-flops. The clear signal (CLR) is connected to all 4 flip-flops in addition to the clock signal to RESET them. The output of the first flip-flop is connected to the input of the next flip-flop and so on. All these flip-flops are synchronous to each other as the same clock signal is applied to each flip-flop.

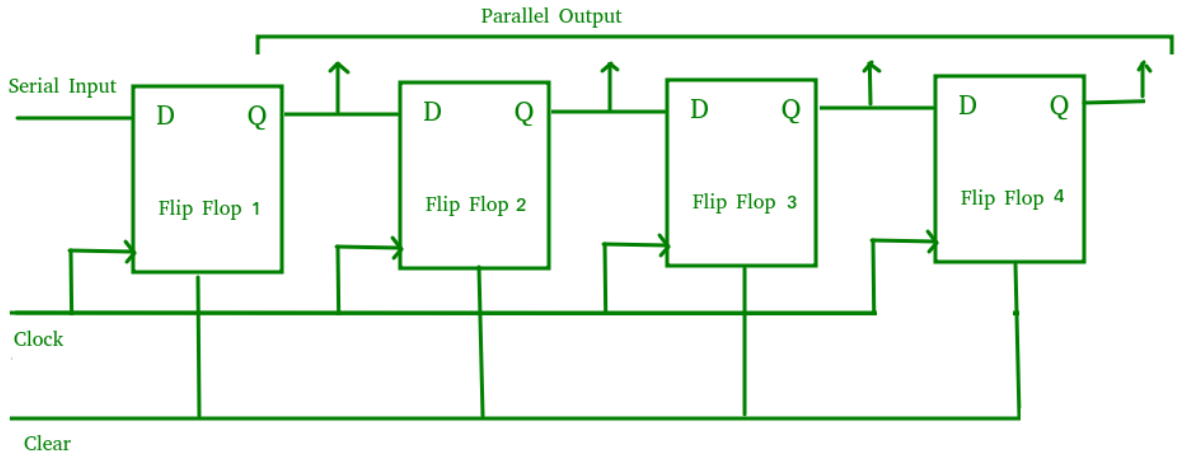

Figure 3-6 Serial In Parallel Out Shift Register

The above circuit is an example of a right shift register that takes serial data input from the left side of the flip-flop and produces a parallel output. They are used in communication lines where demultiplexing a data line into multiple parallel lines is required, since the main application of the SIPO register is to convert serial data into parallel data [33].

With this idea we made a 3 bit Serial in Parallel Out for the ring oscillator to save the serial data bits. The circuit is shown in Figure 3-7.

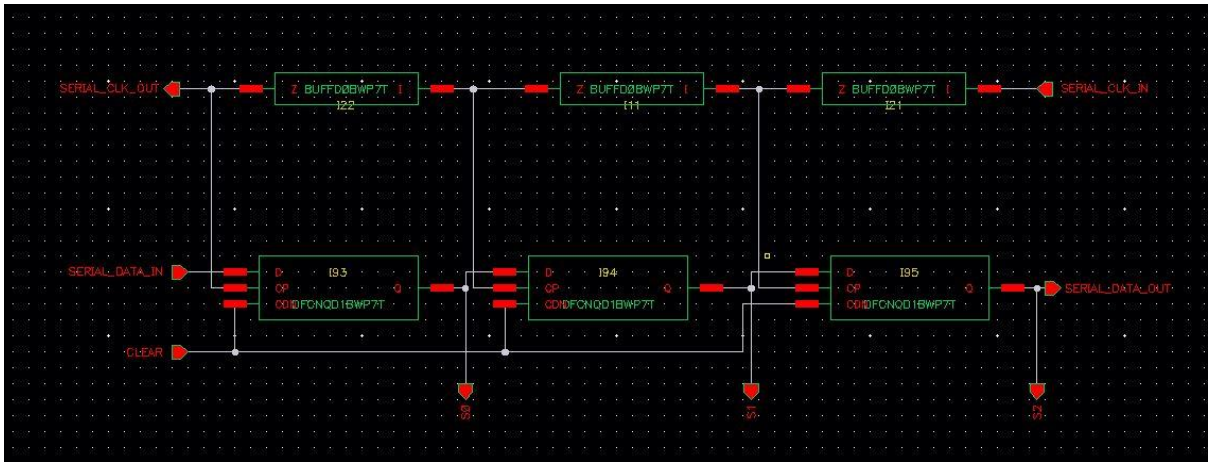

Figure 3-7 SIPO used for Ring Oscillator

Apart from the conventional SIPO, we have added buffers to have small delays in the clock signal to respect the hold and setup time constraint of the flip flops. The clock is given from right to left, and data from left to right, so that no errors arises because of statistical variations between the speeds of the flip flops when writing data.

Figure 3-8 shows the symbol of the SIPO register, and Table 3-1 describes the pins.

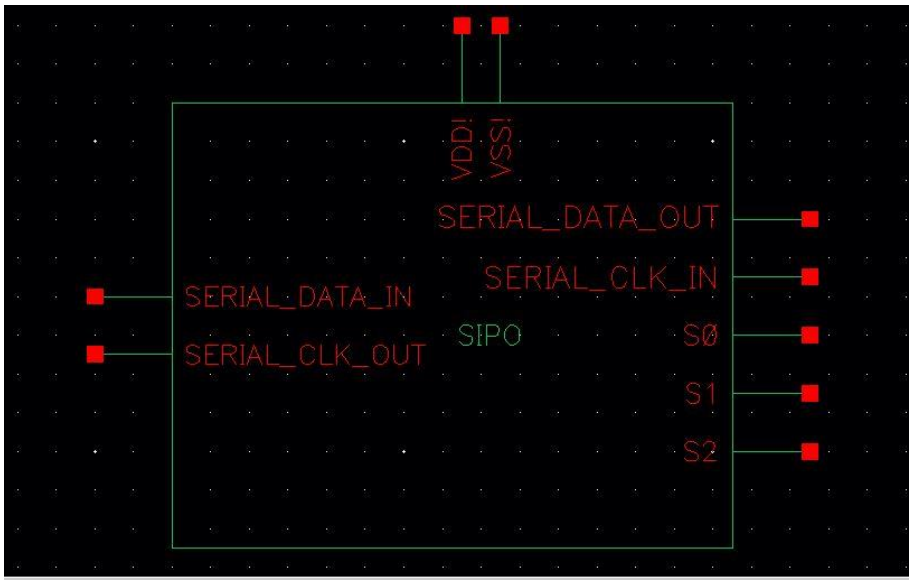

Figure 3-8 Symbol of SIPO

No.	Pin	Description
1	VDD	Supply Voltage (1.8 V)
2	VSS	Ground (0 V)
3	SERIAL_CLK_IN	Clock signal input for FIFO
7	SERIAL_CLK_OUT	Clock signal output from FIFO

4	SERIAL_DATA_IN	Data input for FIFO
5	SERIAL_DATA_OUT	Serial data output from FIFO to read
6	S[0:2]	Selection bit for Non-overlapping delay line to select delay

Table 3-1 Pin Description of SIPO

The SIPO combined with the ring oscillator gives a programmable ring oscillator with 4 different frequency. The complete circuit and layout of ring oscillator is shown in Figure 3-9 and Figure 3-10 respectively.

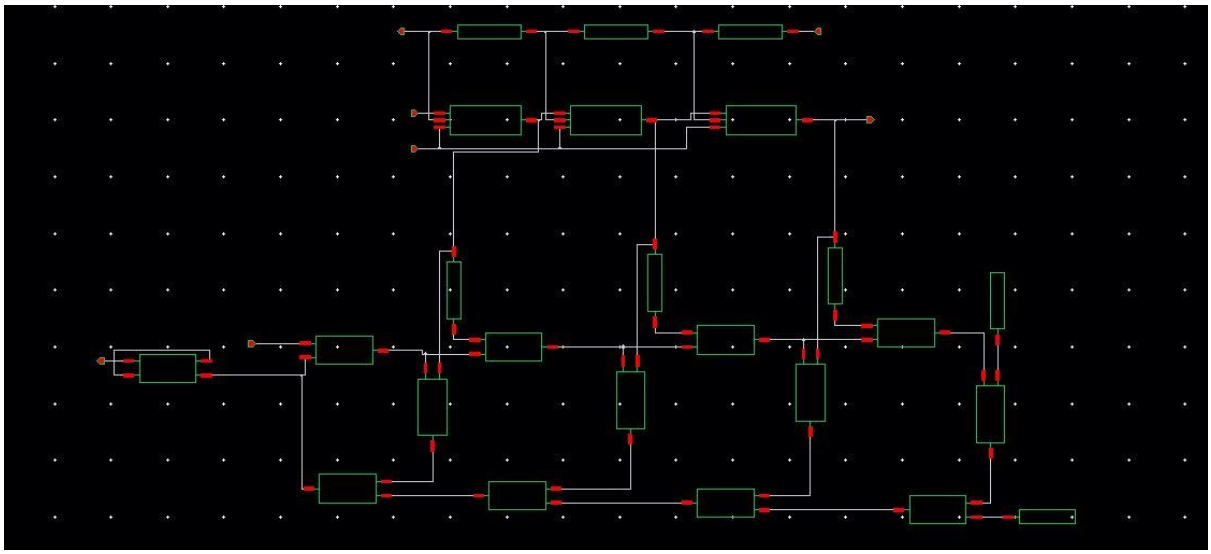

Figure 3-9 Schematic of Programmable Ring Oscillator

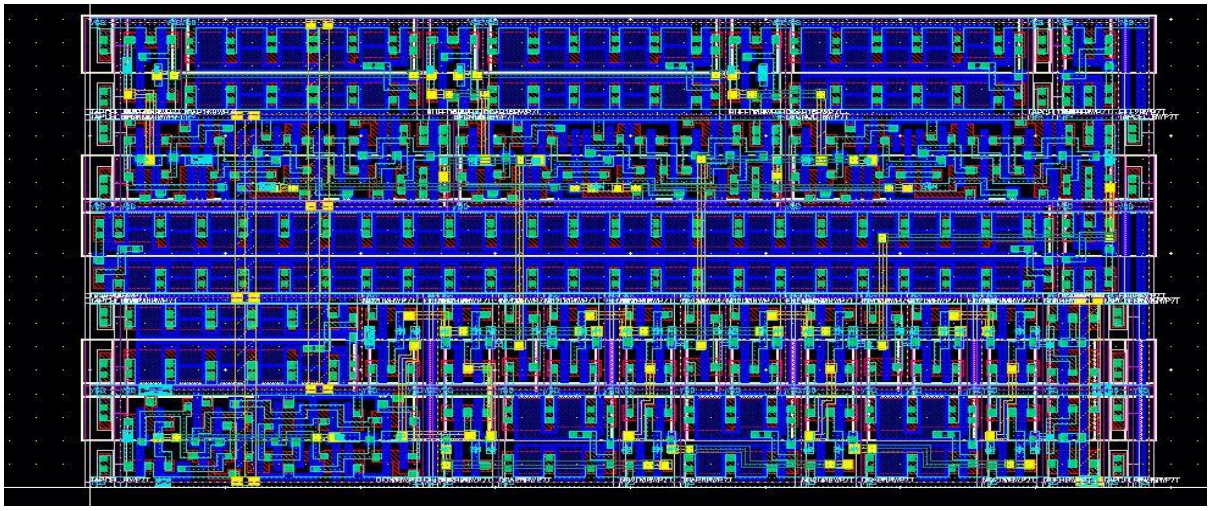

Figure 3-10 Layout of Programmable Ring Oscillator

Table 3.2 shows the frequencies generated from the schematic and post-layout netlist. It is evident that due to the parasitic the frequencies are lower.

Selection Bits S0S1S2	Frequency (Schematic) GHz	Frequency (Layout) GHz
100	1.758	1.353
010	1.050	0.763
001	0.764	0.551
000	0.618	0.4493

Table 3-2 Frequency distribution

The symbol (Figure 3-11) and pin description (Table 3-3) are given below.

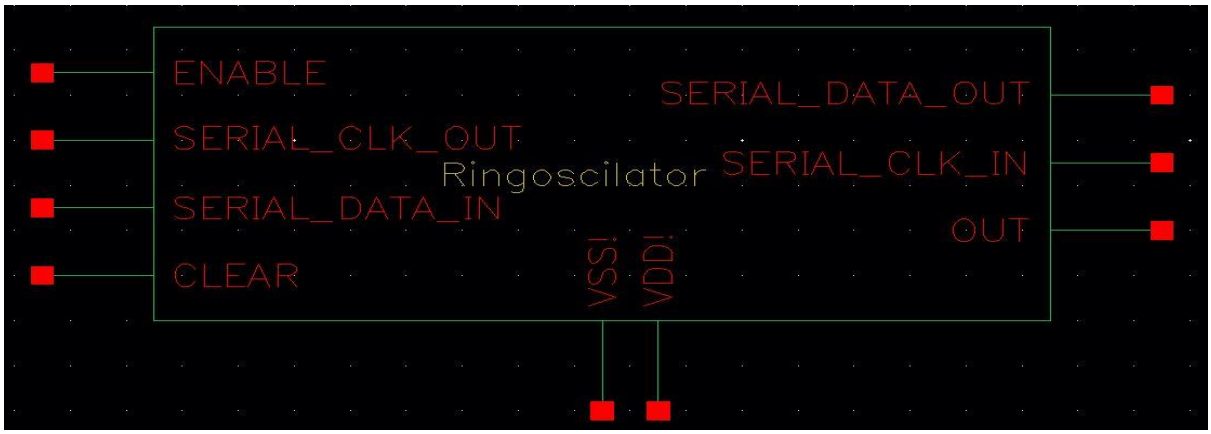

Figure 3-11 Symbol of Oscillator

No.	Pin	Description
1	VDD	Supply Voltage (1.8 V)
2	VSS	Ground (0 V)
3	ENABLE	The pin should be switched from low to high and held constant
4	SERIAL_CLK_IN	Clock signal input for FIFO
5	SERIAL_DATA_IN	Data input for FIFO
6	SERIAL_CLK_OUT	Clock signal output from FIFO
7	SERIAL_DATA_OUT	Data output for FIFO
8	OUT	Ring oscillator output clock signal
9	CLEAR	To rest the SIPO

Table 3-3 Pin description of Programmable Ring Oscillator

A Spectre transient simulation of the ring oscillator for selection ’010’ is shown in Figure 3-12.

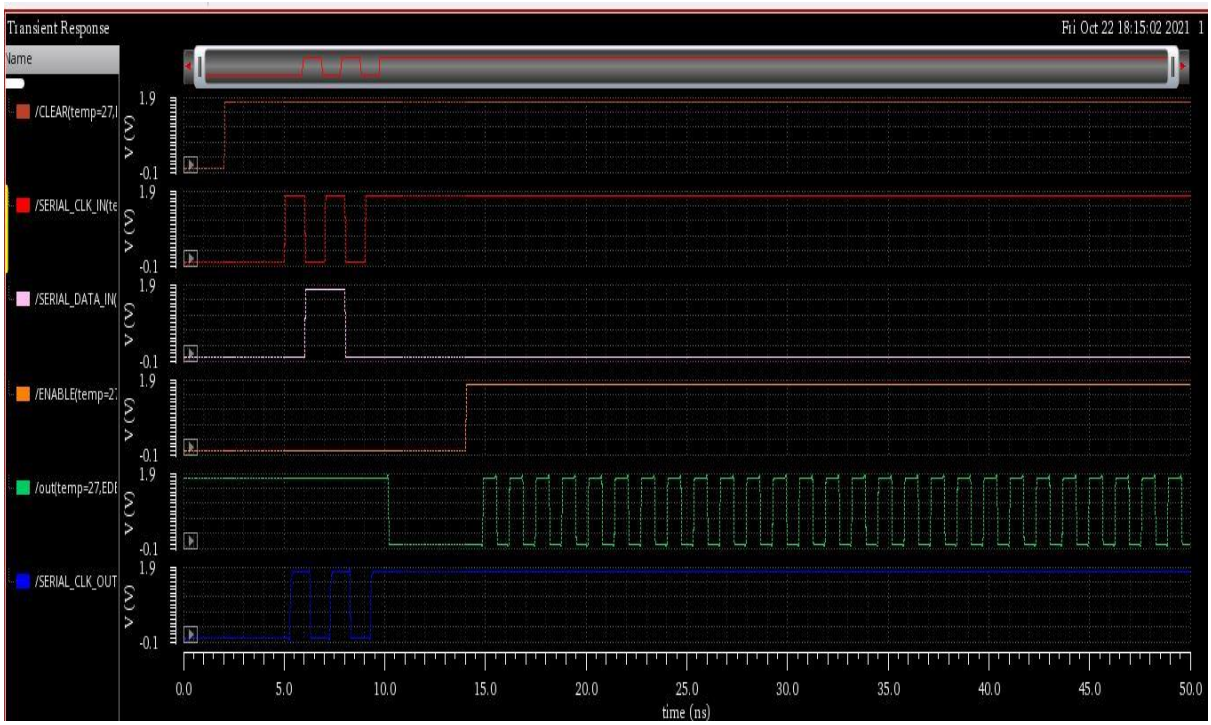

Figure 3-12 Spectre transient simulation of the ring oscillator

3.4 Programmable Frequency Divider

The type D logic flip-flop Figure 3-13, is a very versatile circuit. It can be used in many applications where an edge-triggered circuit is needed. In one application, this logic or digital circuit provides a very simple method of dividing an incoming pulse train by a factor of two.

The divide-by-two circuit uses a type D flip flop logic element. By inputting the pulse train into the clock circuit and connecting the $\bar{Q}$ output to the D input, you can take the output at the D-type Q terminal.

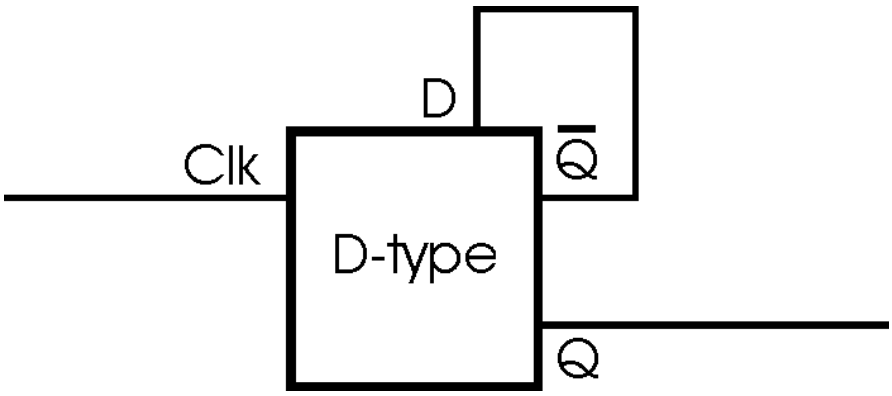

Figure 3-13 D-type frequency divide by two circuit

The circuit works in a simple way. The incoming pulse train serves as the clock for the device, and the data applied to the D input is then clocked through to the output. To see exactly how the circuit works, it is worth examining what happens in each phase of the waveforms shown in

Figure 3-14. Let us assume the situation where the Q output is level '1'. This means that the $\bar{Q}$ output is at '0'. This data is clocked through to the Q output on the next positive edge of the incoming pulse train at the clock input. At this point, the output changes from a '1' to a '0'. At the next positive clock pulse, the data at the $\bar{Q}$ output is clocked through again. Since it is now a '1' (unlike the Q output), this is transmitted to the output and the output changes state again.

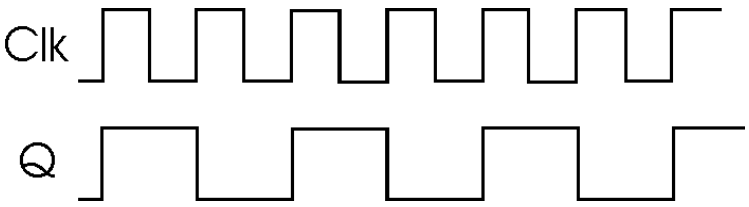

Figure 3-14 Division by 2

The output of the circuit changes states only on the positive edges of the incoming pulse clock. Each positive edge occurs once per cycle. However, since the D-type output requires two state changes to complete a cycle, this means that the output of the D-type circuit changes at half the rate of the incoming pulse current. In other words, it is divided by two.The frequency divider used in our clock generator is as shown in Figure 3-15 the corresponding layout in Figure 3-16.

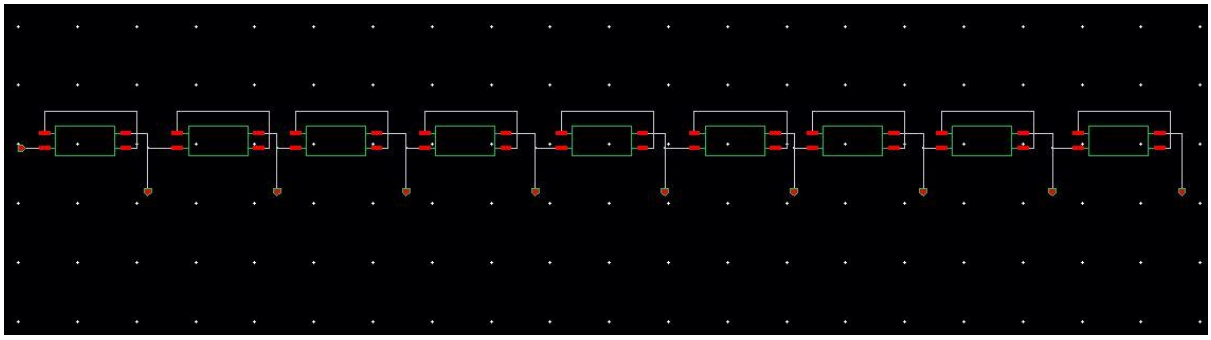

Figure 3-15 Frequency Divider Schematic

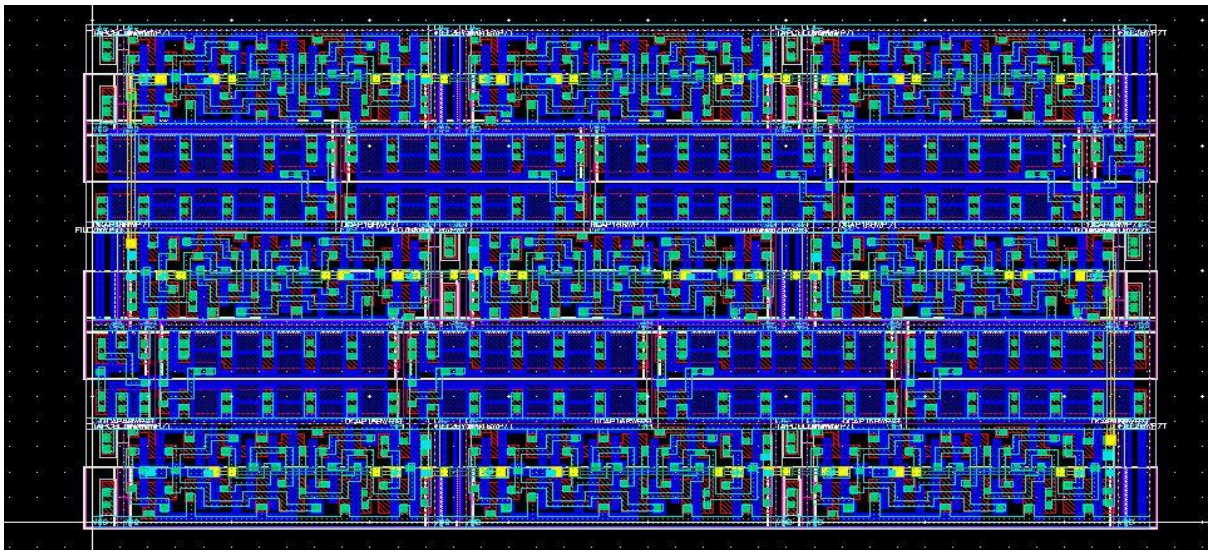

Figure 3-16 Frequency Divider Layout

Table 3.4 describes the 9 frequencies generated by the frequency divider for the four-clock frequency generated by the ring oscillator.

Frequency (MHz)	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6	Stage 7	Stage 8	Stage 9
1353	676.5	338.25	169.12	84.56	42.28	21.14	10.57	5.28	2.64
763	381.5	190.75	95.37	47.68	23.84	11.92	5.96	2.98	1.49
551	275.5	137.75	68.87	34.43	17.21	8.60	4.30	2.15	1.07
449.3	224.65	112.325	56.16	28.08	14.04	7.02	3.51	1.75	0.87

Table 3-4 Frequency Division by the 9 stages

3.5 Programmable Multiplexer

This is a combinational circuit with many data inputs and a single output that depends on control or selection inputs. For N input lines, log n (base2) selection lines are required, or we can say that for 2^n input lines, n selection lines are required. Multiplexers are also known as "data n selector, parallel to serial convertor, many to one circuit, universal logic circuit". Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain time and bandwidth.

Figure 3-17 is the symbol of the 3-to-1 multiplexer used in our design and table 3.5 truth table of the multiplexer

Figure 3-17 3×1 Multiplexer

S0	S1	Z
0	0	I0
1	0	I1
0	1	I2

Table 3-5 Truth table of 3×1 Multiplexer

As we have 9 stages, we use 4 3-to-1 MUXs to get the output, and to make it programmable we have used the same serial in parallel out circuit explained in section 3.1.4, with 10 bits. The schematic and layout are as shown in Figure 3-18 and Figure 3-19 respectively.

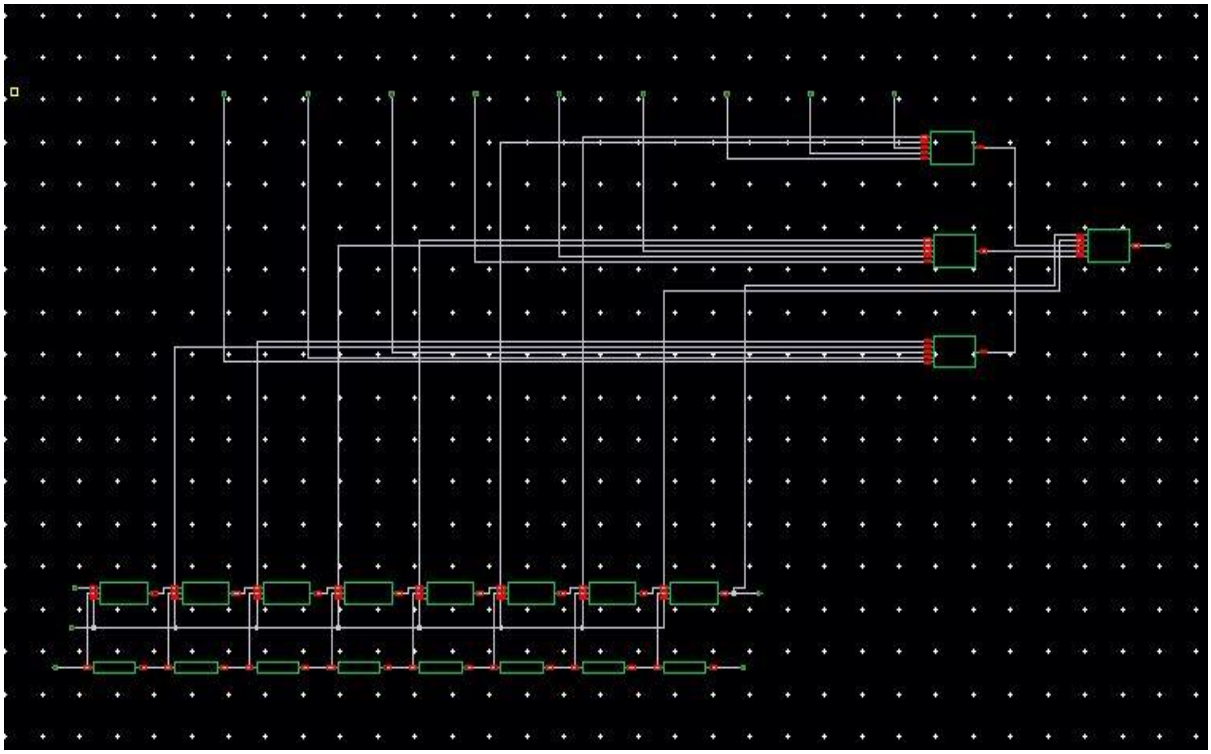

Figure 3-18 Schematic Diagram

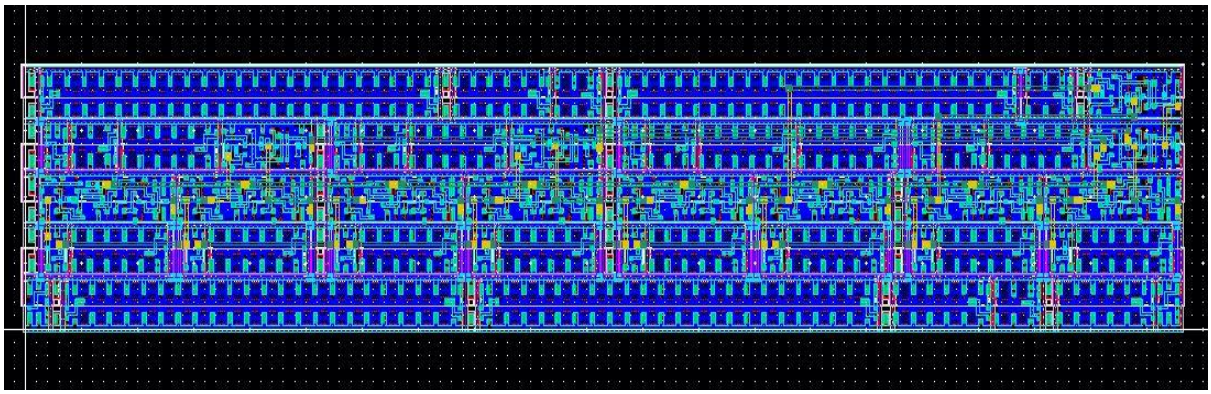

Figure 3-19 Layout of the programmable MUX

With the above configuration, we were able to select the reference clock and output clock signal from the frequency divider. For the ADC clock, we can select stages 4, 5, or 6 of the frequency divider, because they provide valid ADC clock frequencies for all settings of the programmable ring oscillator. This was implemented using as shown in Figure 3-20 and the corresponding layout is shown in Figure 3-21.

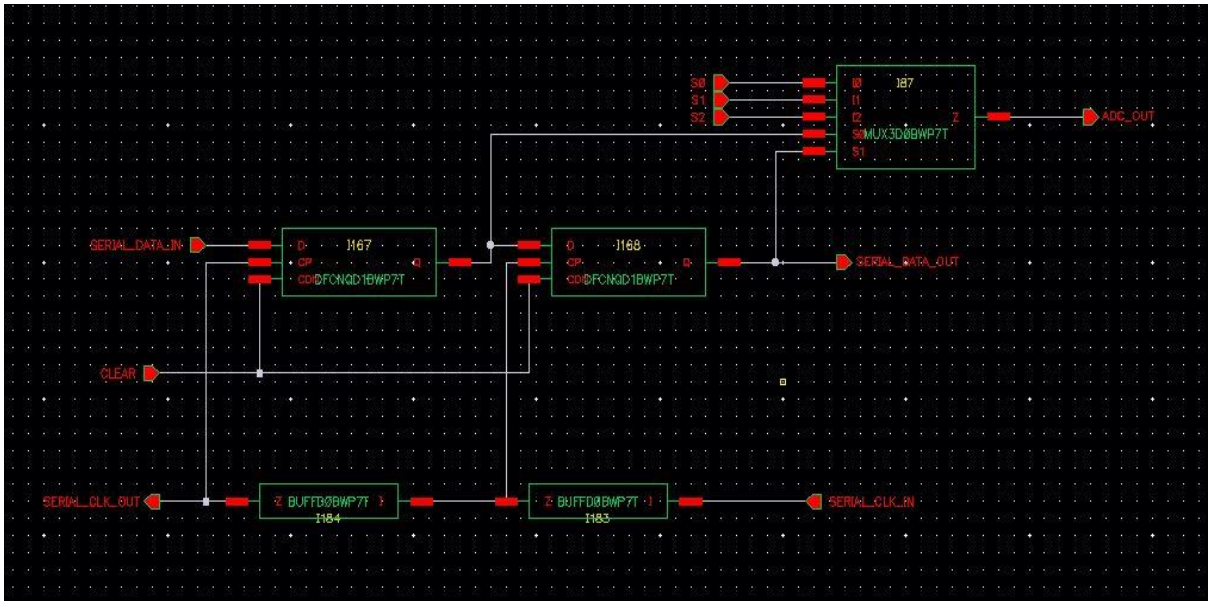

Figure 3-20 ADC MUX schematic

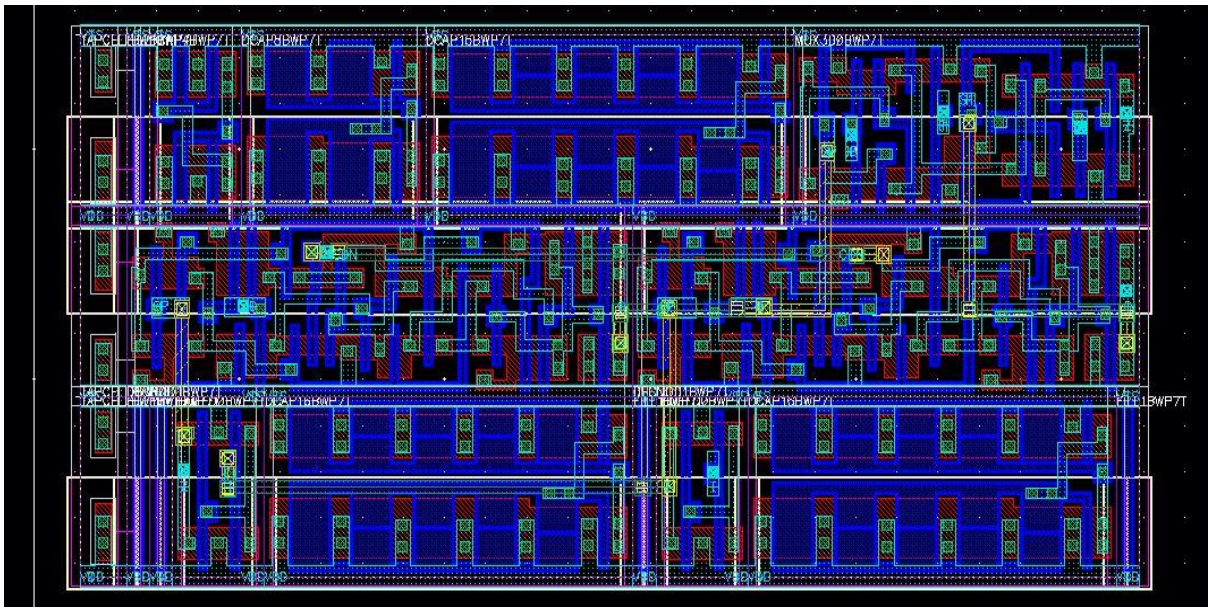

Figure 3-21 ADC MUX layout

The programmable frequency divider in the schematic clock generator is used to produce the reference clock signal, the non-overlapping clock signals for the sensor chip, and the clock for the ADCs of the sensor chip. Figure 3-22, Figure 3-23 shows the schematic and layout of the programmable frequency divider respectively, where Table 3-6 is the pin descriptions.

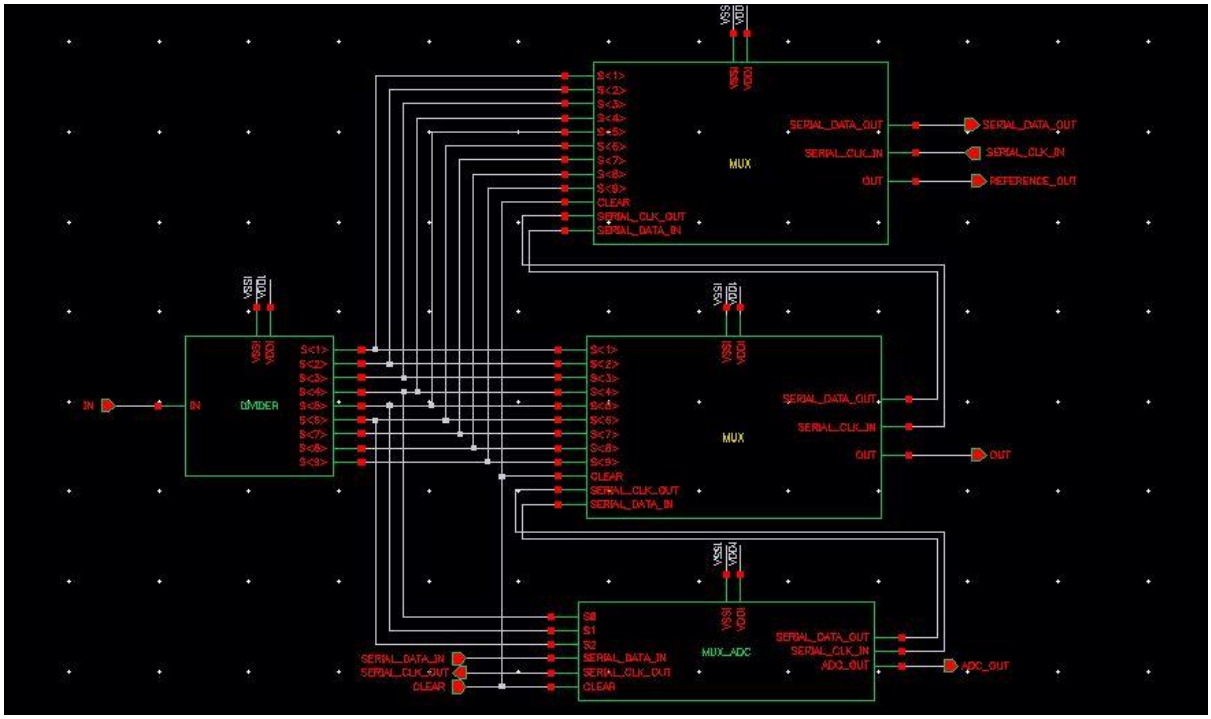

Figure 3-22 Schematic of the programmable frequency divider

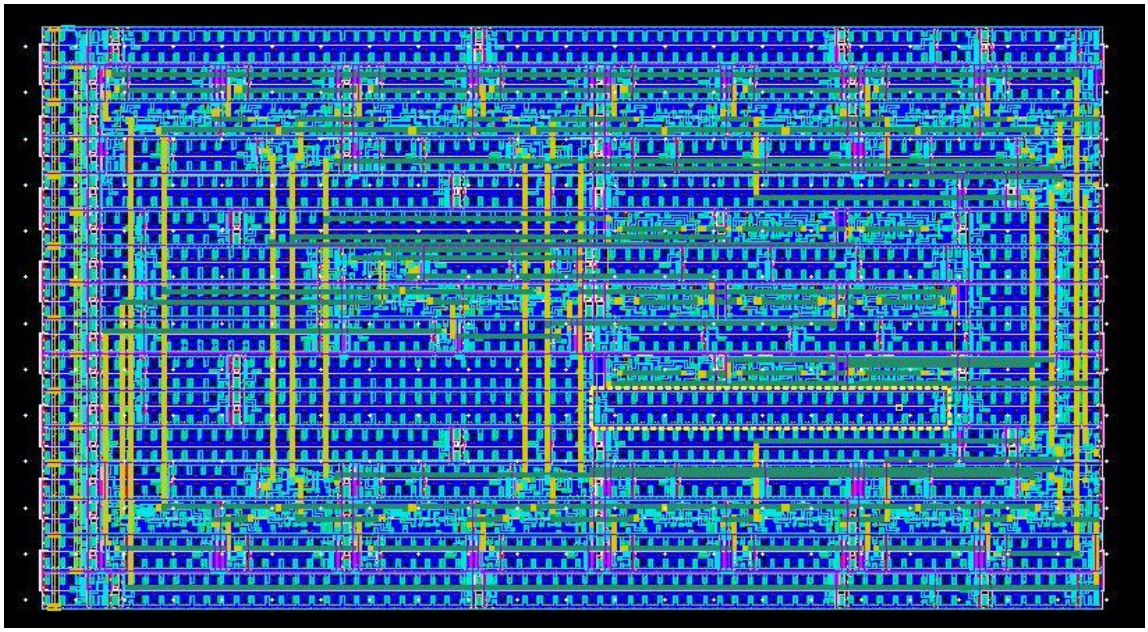

Figure 3-23 Layout of the programmable frequency divider

No.	Pin	Description
1	VDD	Supply Voltage (1.8 V)

2	VSS	Ground (0 V)
3	SERIAL_CLK_IN	Clock signal input for FIFO
4	SERIAL_DATA_IN	Data input for FIFO
5	IN	Input clock signal from ring oscillator
6	SERIAL_DATA_OUT	Data output for FIFO
7	SERIAL_CLK_OUT	Clock signal output from FIFO
8	OUT	Selected output clock signal
9	ADC_OUT	Output clock signal for ADC
10	REFERENCE_OUT	The clock signal to measure the frequency
11	CLEAR	To rest the SIPO

Table 3-6 Pin Description

	Ring oscillator Bits	ADC Bits	Clock Out	Reference Clock
Bits	001	01	00000000	00000001
Frequency	676.5 MHz	54.96 MHz	676.5MHz	338.25 MHz

Table 3-7 Serial data input for the programmable frequency divider

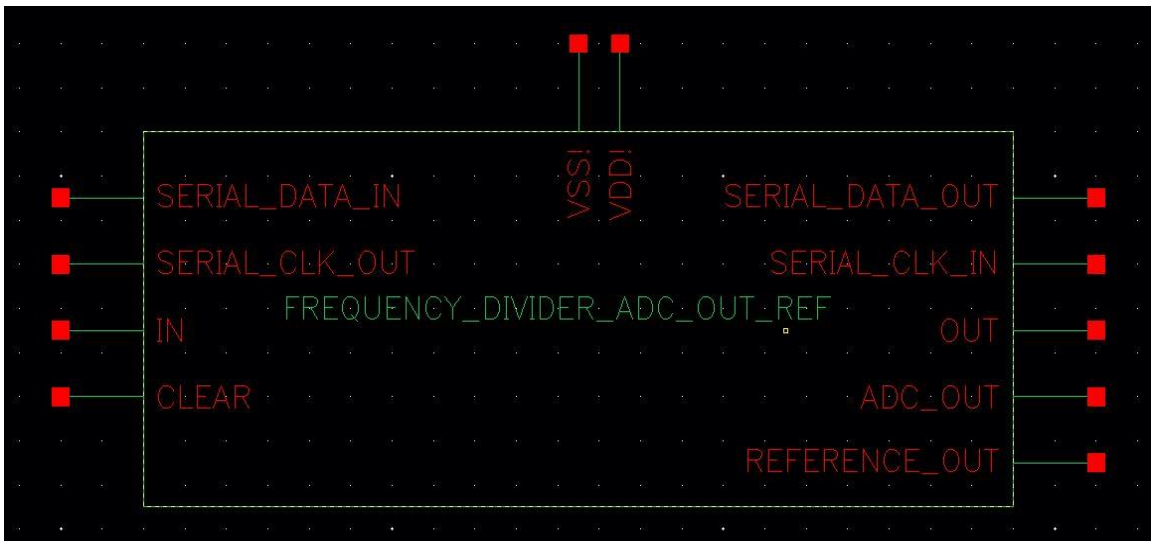

Figure 3-24 Symbol of the programmable frequency divider

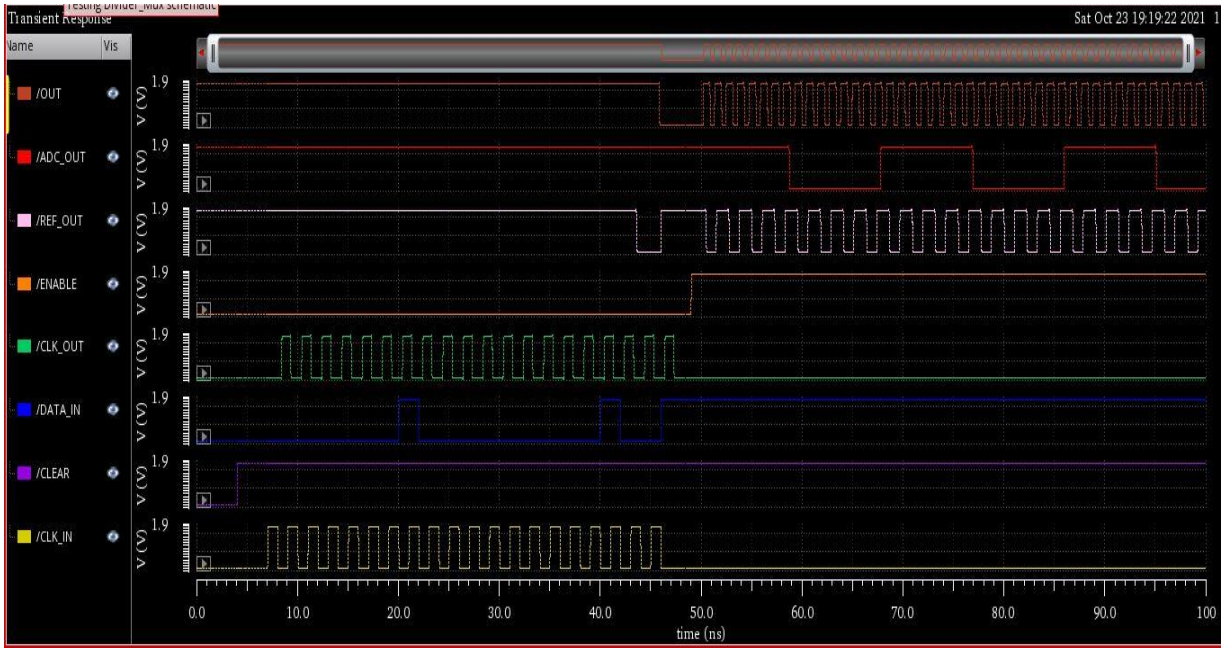

Figure 3-25 Spectre simulation

4 Chapter 4

In this chapter, we will discuss the programmable delay line and the pass transistor optimization technique.

4.1 Clocking Scheme

A clock signal can be combined with a control signal that turns the clock on or off for a particular part of the circuit. This is often used to save power by effectively turning off parts of a digital circuit when not in use. Based on the number of phases, they can be divided into single-phase clocks and multi-phase clocks, i.e., two-phase, or four-phase clocks.

Most modern synchronous circuits use only a single-phase clock; they transmit all clock signals on effectively one line. In synchronous circuits, a "two-phase clock" refers to clock signals distributed on 2 wires, each with non-overlapping pulses. Traditionally, one wire is referred to as "phase 1" or "φ1" and the other wire carries the signal "phase 2" or "φ2". The two-phase clock is of great importance in sequential circuits. Certain ICs require external generation of two-phase clock signals, while some ICs have integrated two-phase clock generation on-chip so that only a single-phase clock input was required, which simplified the system design [34]. The difference in phase angle between the two clock signals depends on the application. Since the two phases are guaranteed not to overlap, gated latches rather than edge-triggered flip-flops can be used to store state information if the inputs of the latches on one phase depend only on the outputs of the latches on the other phase.

Since a gated latch requires only four gates compared to six gates for an edge-triggered flipflop, a two-phase clock can result in a design with a smaller total number of gates.

The conventional circuit is shown in Figure 4-1[35]. The input clock signals CLK' and its inverse CLKn' are converted into two nonoverlapping clock phases Φ1 and Φ2. It consists of a pair of cross-coupled NAND gates which are used to achieve the non-overlap of the two

output signals. The NAND gates, together with two inverters connected to their outputs, define the length of the "dead" time,

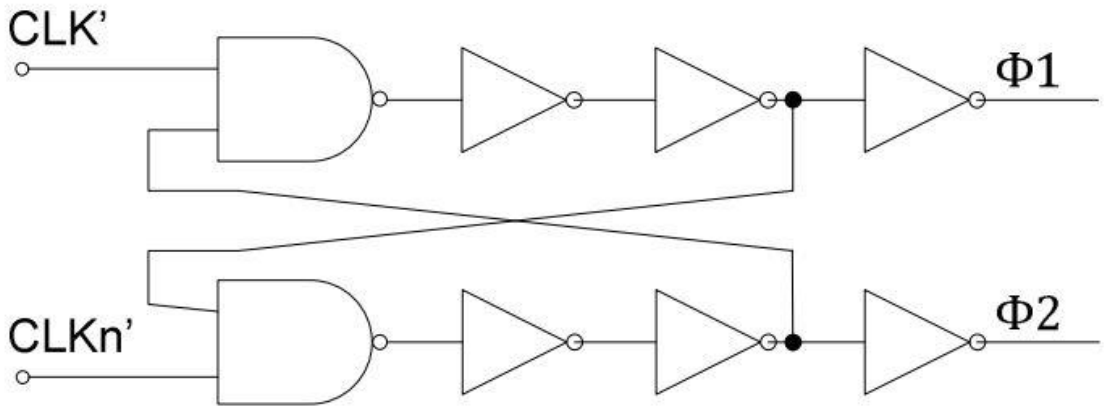

Figure 4-1 Conventional two-phase clock generator

i.e. the time when both clock phases are in the low state. In addition, the inverters determine the drive capability of the phase generator. To maximize the available settling time for the circuit, in many applications the phase widths are widened by minimizing the non-overlapping duration.

4.2 Proposed Concept

The following CMOS18 circuit in Figure 4-2, generates 2 single-ended, non-overlapping clock signals CLK _T and CLK _D from a single-ended input clock signal provided by the pulse voltage source. The non-overlapping gap width is determined by the inverter chains after the NAND gates. Ideally, the input inverter should invert the input clock without delay. However, due to the finite gate delay of the inverter, the edges of the inverted input clock CLK _InB ("B": bar, indicates the inverted logic value) are slightly delayed compared to the edges of the input clock. As a result, the pulses from CLK _T and CLK _D would have different duty cycles. With a true symmetrical differential input clock (CLK _In, CLK_InB) this asymmetry can be canceled. This is solved by inserting a transmission gate in the CLK_InB clock path, so that it matches the delay of the inverter. Detailed implementation is explained in section 4.3.

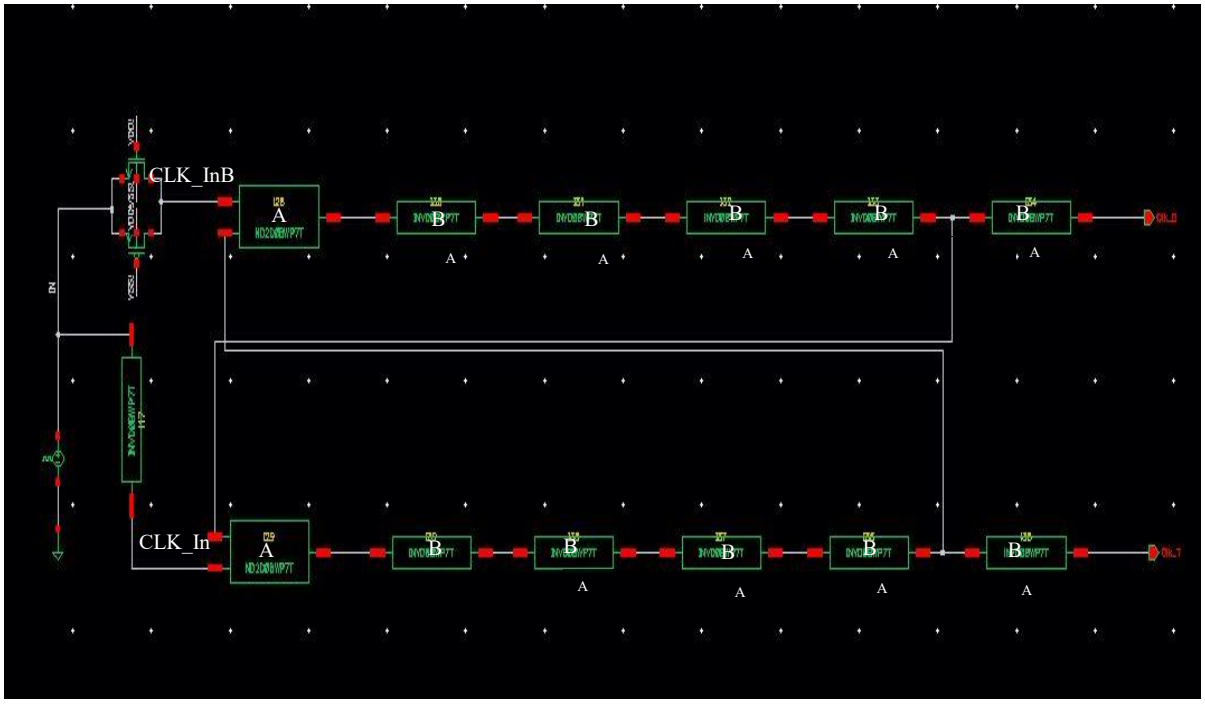

Figure 4-2 Non overlapping clock generator. A: NAND, B: Inverter.

The biosensor chip must receive differential, non-overlapping clocks (CLK _T, CLK _TB) and (CLK _D, CLK _DB), where CLK _TB and CLK _DB are the exact inverse of CLK _T and CLK _D, respectively. In this way, the net high-frequency clock components entering the chip are exactly zero. This is important to avoid high-frequency return paths through bond pads other than the clock pads.

Since we need fully differential clocks, the entire clock generator is made fully differential, starting with the programmable ring oscillator explained in section 3.1.

A discrete set of fixed, predefined, non-overlapping gaps between CLK _T and CLK _D can be made with longer inverter chains after NAND gates, with selectable taps after inverter pairs. Since the inductance of the clock generator's wire bonds can distort the clock pulses somewhat, we need to be able to select the gaps over a wider range, with constant relative accuracy. This can be achieved by a logarithmic distribution of the fixed delays, e.g. dt, 2×dt, 4×dt, 8×dt, etc.

The 2 inverters at the outputs are connected to buffer to have a higher drive strength because they must drive the drive larger transistors of the output amplifiers and the wire capacitances between them.

The schematic is shown above (Figure 4-2) is only conceptual. We still need to design the fully differential version with optimized drive strengths for all gates. Here we need to find a good

balance between small/large gates with wide/narrow statistical distributions of gate delays and low/high power dissipation.

The selectable delay path length explained in chapter 3 can also be used with Figure 4-2 to achieve different delay selections. So that each selection will give a different delay due to the inverter number changes, thereby we can separate the CLK_T, CLK_D without a cross-talk. Figure 4-3 is a zoomed section of the full circuit, showing 3 delay selection paths. Each path produces its own delay, which is increasing as we go from left to right.

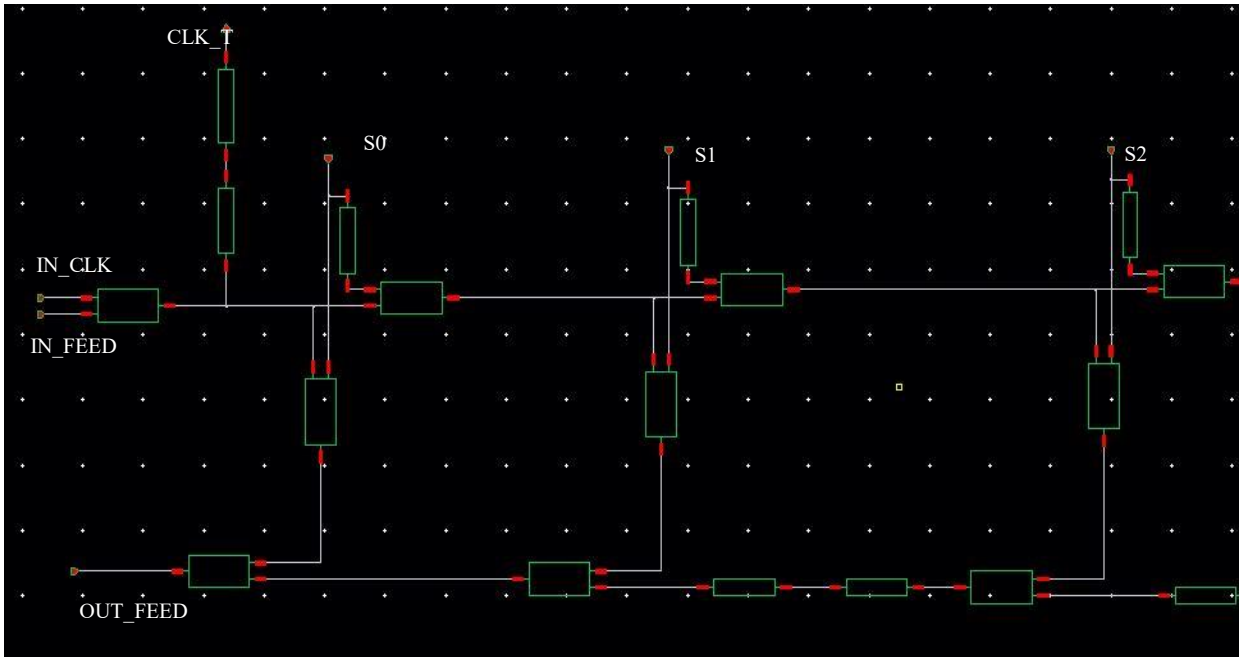

Figure 4-3 Close up section of CLK_T branch

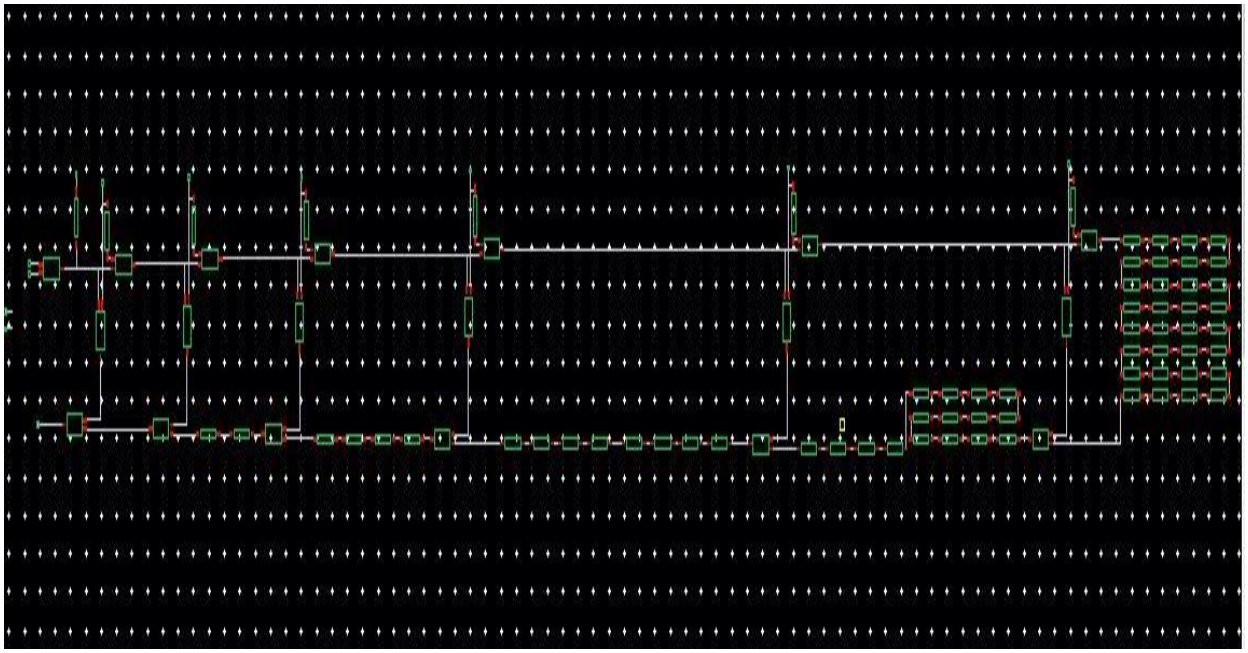

Figure 4-4 Full programmable delay path of the CLK_T branch

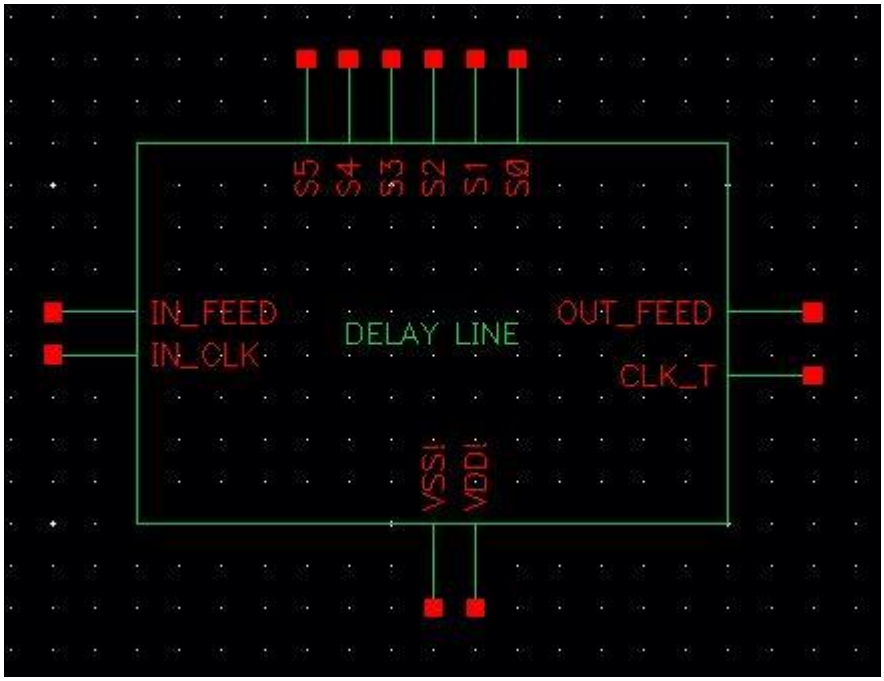

Figure 4-5 Symbol of the programmable delay path of figure 4.4

Figure 4-4 shows the complete path of CLK_T with the feedback (OUT_FEED) to the CLK_D section (the CLK_D section is same as in figure 4.4).

As mentioned in chapter 3 we can store the selection bits using serial in parallel out shift register. We implemented a 6-bit programmable non-overlapping clock signal as shown in Figure 4-6. The corresponding layout is shown in Figure 4-7

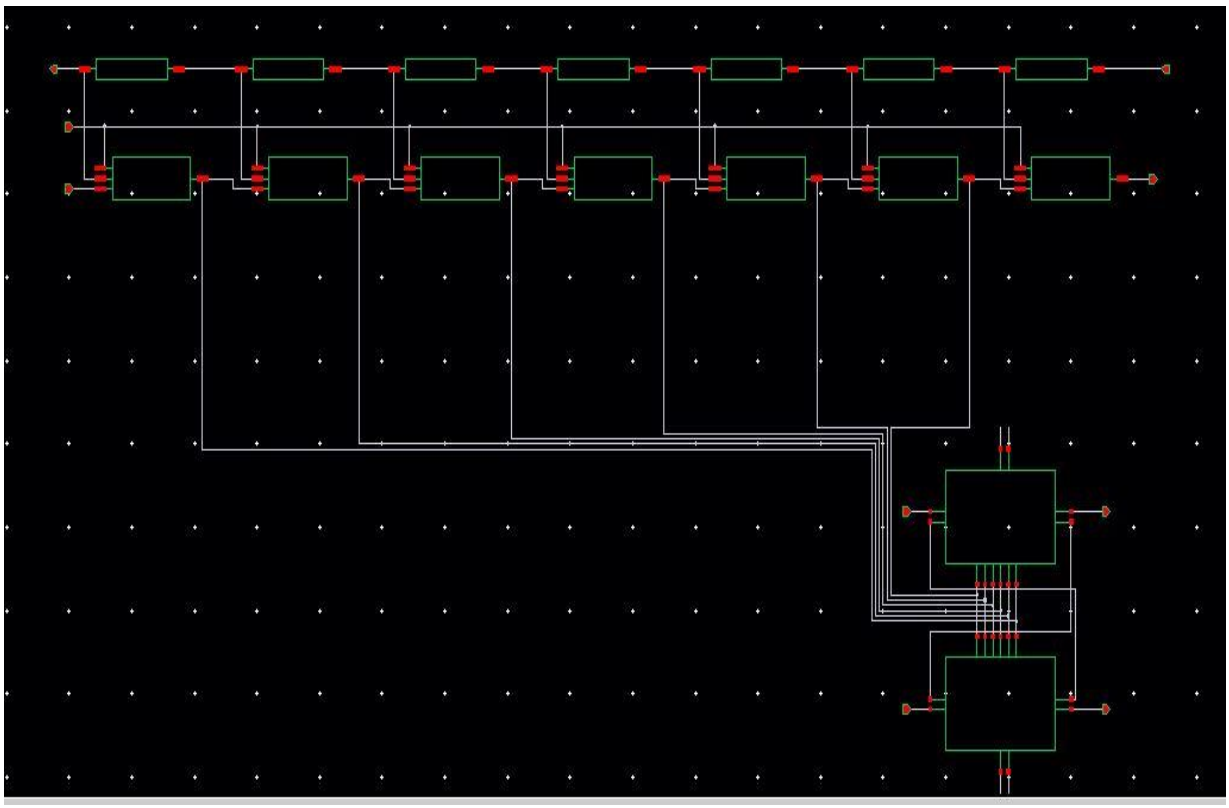

Figure 4-6 Schematic of Programmable non-overlapping clock generator

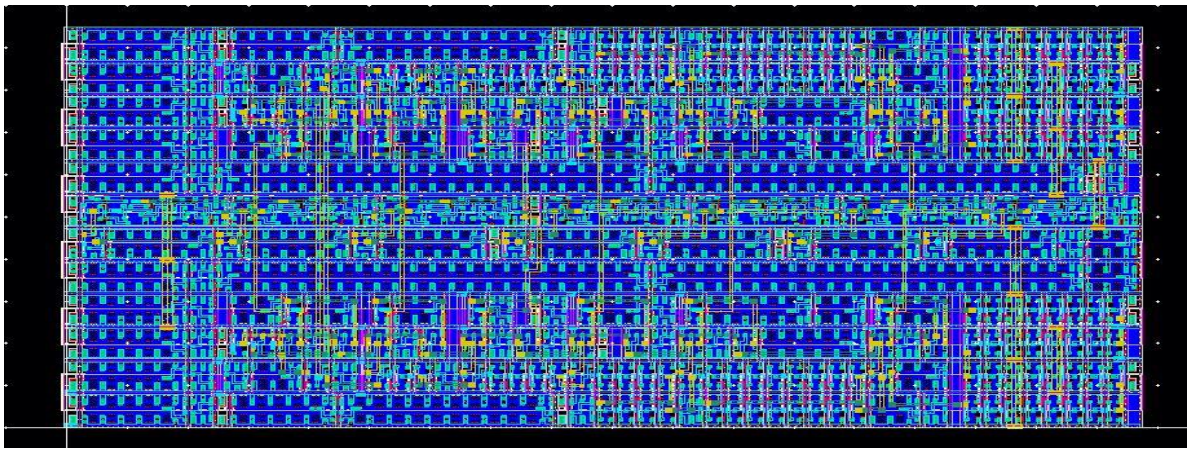

Figure 4-7 Layout of Programmable non-overlapping clock generator

The symbol, pin description, and the delays produced by each delay are shown in Figure 4-8 and Figure 4-9, and in Table 4-1 and Table 4-2.

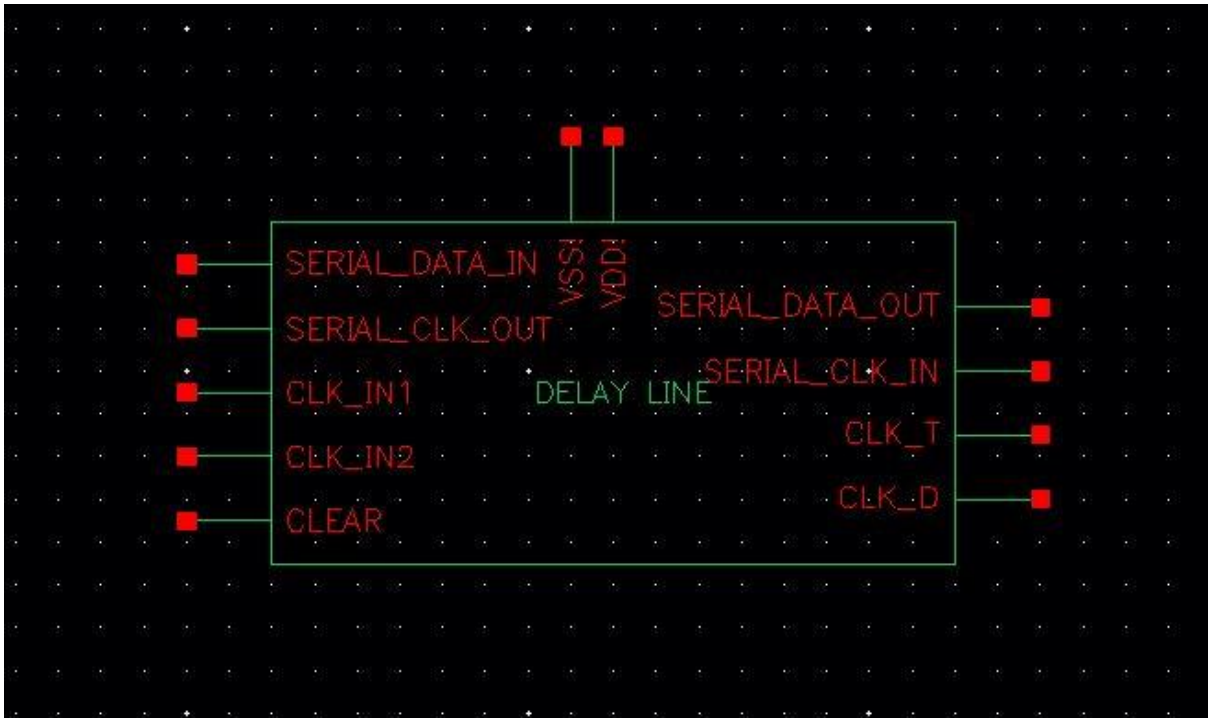

Figure 4-8 Symbol of Programmable non-overlapping delay line

No.	Pin	Description
1	VDD	Supply Voltage (1.8 V)
2	VSS	Ground (0 V)
3	SERIAL_DATA_IN	Data input for FIFO
4	SERIAL_CLK_IN	Clock signal input for FIFO
5	CLK_IN1	OUT1 from pass gate
6	CLK_IN2	OUT2 from pass gate

7	SERIAL_DATA_OUT	Serial data output from FIFO to read
8	CLK_T	Non-overlapping output clock signal
9	CLK_D	Inverted non overlapping output clock signal
10	CLEAR	RESET the FIFO
11	SERIAL_CLK_OUT	Clock signal output from FIFO

Table 4-1 Pin Description of Programmable non-overlapping clock generator

Selection bits S5S4S3S2S1S0	Schematic Delay	Layout Delay
000001	161.28 ps	204.00 ps
000010	243.99 ps	321.26 ps
000100	391.37 ps	515.00 ps
001000	578.41 ps	758.93 ps
010000	883.00 ps	1.15 ns
100000	1.384 ns	1.80 ns
000000	2.217 ns	2.87 ns

Table 4-2 Delays obtained by each path selection

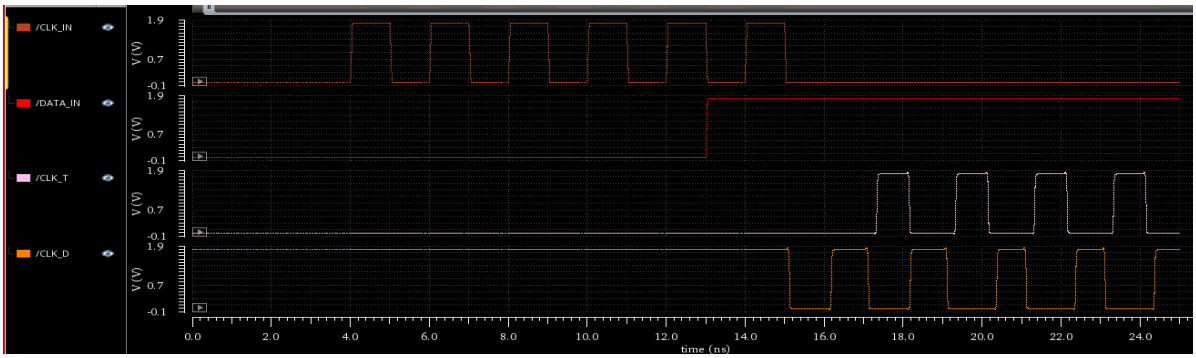

Figure 4-9 Spectre Simulation for the Delay Line

4.3 Transmission Gate

The two clock signals given to the programmable non-overlapping clock generator must be symmetric. However the inverter causes a delay in CLK_In when compared with the CLK_In B. This asymmetric can be solved by adding a transmission gate in the CLK_In B path.

A transmission gate (TG) is an analog gate similar to a switch that can conduct in either direction or be inhibited by a control signal. It is a CMOS-based switch in which PMOS passes a strong 1 but a weak 0, and NMOS passes a strong 0 but a weak 1. Both PMOS and NMOS operate simultaneously.

In principle, a transmission gate consists of two field-effect transistors in which, unlike many conventional discrete field-effect transistors, the substrate (bulk) terminal is not internally connected to the source terminal. The two transistors, an n-channel MOSFET and a p-channel MOSFET are connected in parallel, but only the drain and source terminals of the two transistors are connected. Their gate terminals are connected via a NOT gate (inverter) to form the control terminal.

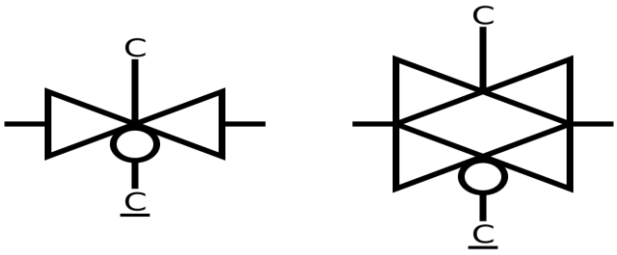

Figure 4-10 Symbol of transmission gate

Two variations of the "bow-tie" symbol (Figure 4-10) are commonly used to represent a transmission gate in circuit diagrams.

Unlike discrete FETs, the substrate terminal is not connected to the source terminal. Instead, the substrate terminals are connected to the respective supply potential to ensure that the parasitic substrate diode (between the source/drain and substrate) is always reverse biased and

thus does not affect the signal flow. Thus, the substrate terminal of the p-channel MOSFET is connected to the positive supply potential and the substrate terminal of the n-channel MOSFET is connected to the negative supply potential.

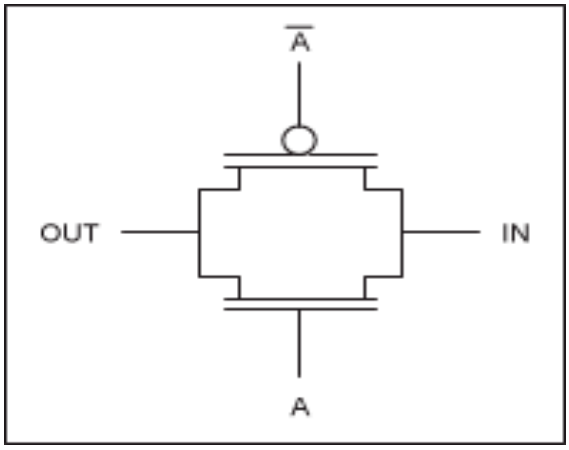

Figure 4-11 Circuit of transmission gate

When the voltage at node A (Figure 4-11) is a logic 1, the complementary logic 0 is applied to node A_Bar, allowing both transistors to conduct and pass the signal between IN at OUT. When the voltage at node A is a logic 0, the complementary logic 1 is applied to node A_Bar, turning off both transistors and forcing a high impedance between nodes IN and OUT.

Optimization of the transmission gate is done using the parametric analysis tool of the spectre Table 4-3.

	Length	Width	Fingers
NMOS	180nm	0.905u	3
PMOS	180nm	1.035u	4

Table 4-3 Transmission Gate Sizing

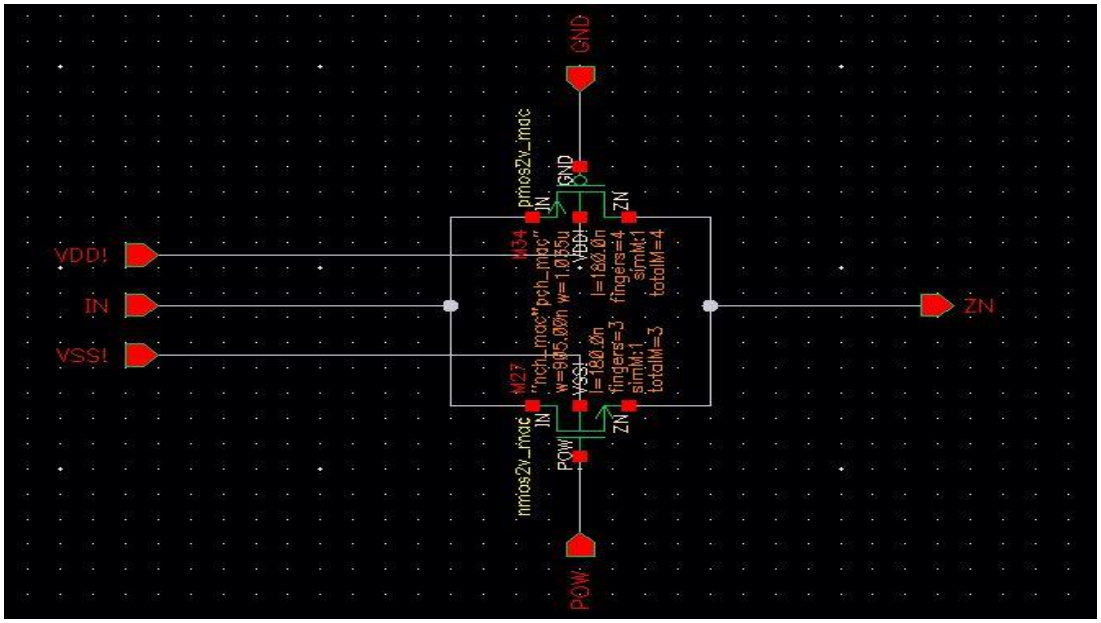

Figure 4-12 Circuit of transmission gate for a delay line

To have a standard design of digital circuits, the transmission gate layout was built and merged with the other standard cells.

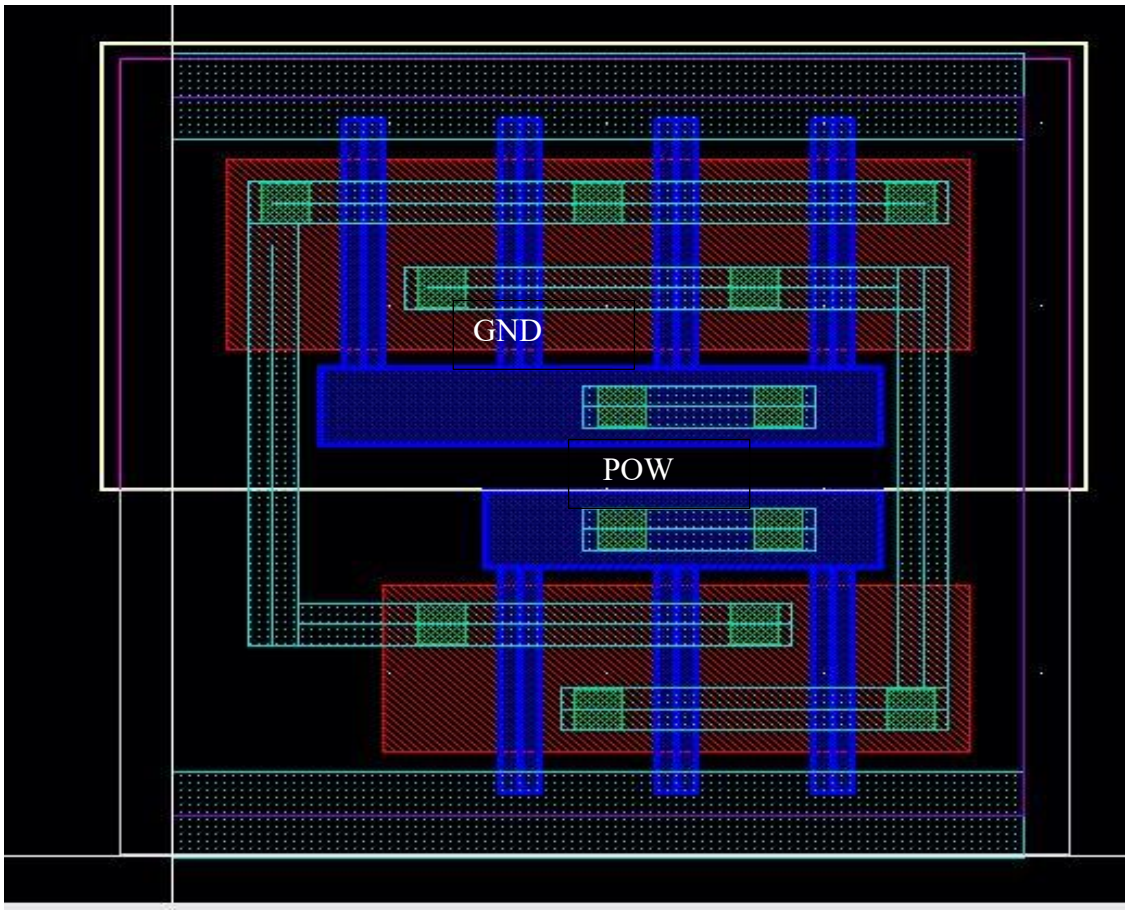

Figure 4-13 Circuit of transmission gate for the delay line

The POW, GND are connected permanently to a GTIE cell to avoid the gate breakdown due to the spikes in supply voltage.

4.4 Level Shifter

A level shifter, also called a logic level shifter or voltage level shifter in digital electronics, is a circuit used to translate signals from one logic level or voltage domain to another, to allow compatibility between ICs with different voltage requirements, such as TTL and CMOS [36-37]. Modern systems use level shifters to bridge domains between processors, logic, sensors, and other circuitry. In recent years, the three most common logic levels have been 1.8 V, 3.3 V, and 5 V, although levels above and below these voltages are also used.

The VLSI technology enables the realization of complex System on Chip (SoC) designs, where different parts of a system such as analog and digital circuits and passive components are integrated in a single chip. In such SoCs, different parts of the chip are operated at different voltages to achieve an optimal speed/power balance, and it is very common to have two or more voltage domains on a single chip [38-40]. For communication between different parts of a chip, operating at different supply voltages, level shifters are required to convert the logic signal from one voltage level to the other. In addition, level shifters are also required at the interface between the pad ring and the chip core where low voltage logic signals are switched from the chip core to the high voltage level at which the pad ring operates [41].

4.4.1 Cross-coupled rectifier

The biosensor chip requires non-overlapping clock signals with amplitude in the range 0.7 to 1.2 V. We need an amplifier circuit to shift the logic amplitude voltage of 1.8V to a variable VT (0.7-1.2V). This amplitude voltage must be adjustable in 50mV steps. The Figure 4-14 shows cross-coupled rectifier circuit.

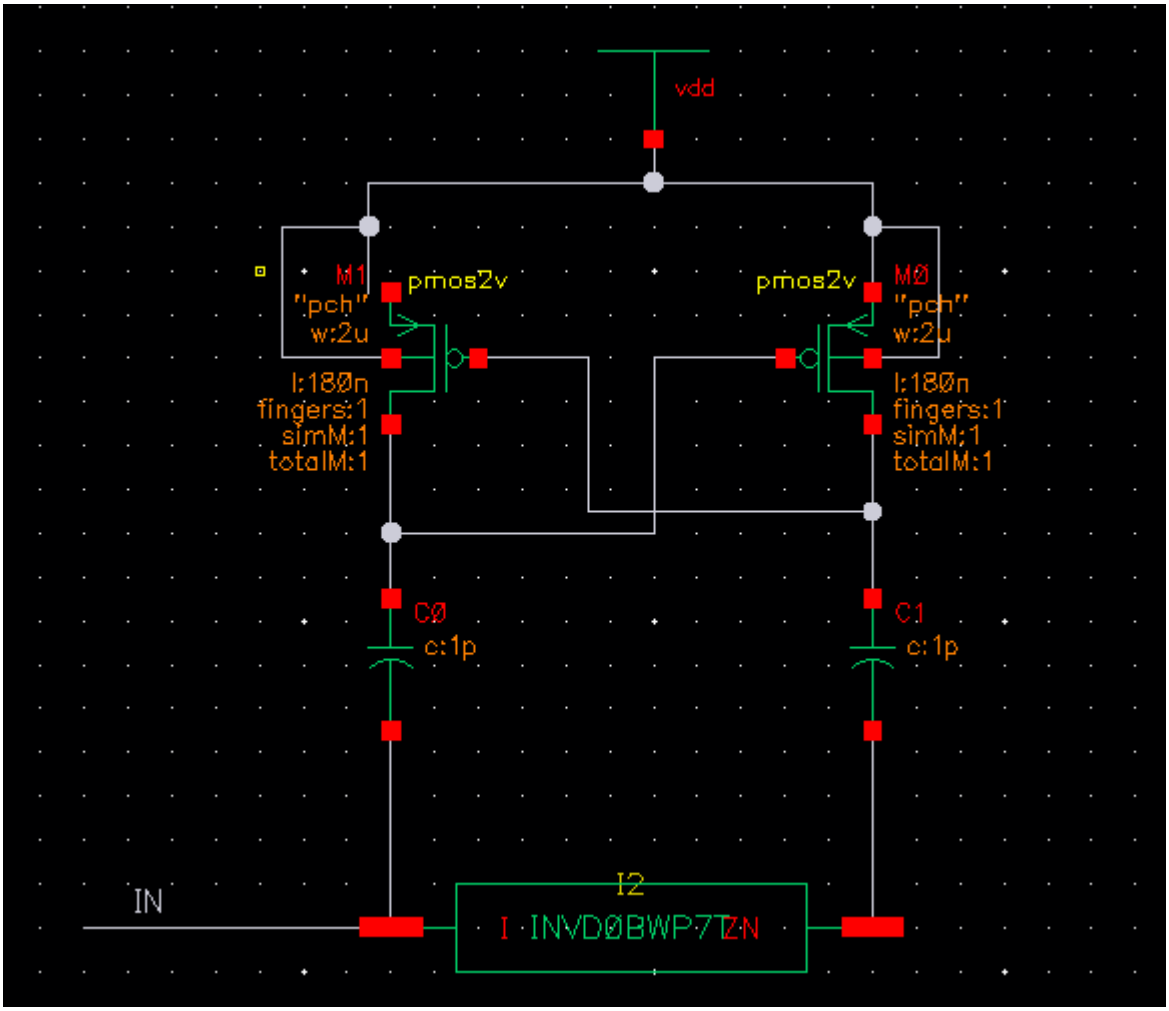

Figure 4-14 Cross-coupled rectifier circuits

At IN, the oscillation amplitude is given to the input. The inverter inverses the signal and the two capacitors copy it to the cross-coupled PMOSTs, which act as switches to clamp their drain volages to vdd. So, when one switch is closed the other one is open. This way it acts as a rectifier and it produces a level-shifted clock signal with and amplitude proportional to the input amplitude. With this consideration we have build the output stage amplifier of the clock generator to shift the output pulse amplitudes from 1.8V to 0.7-1.2V. From the cross-coupled rectifier circuit, instead of rectification we give voltage VT at vdd in Figure 4-14 and switch the output from VT and the oscillation voltage 1.8V with a capacitive division (PMOS input capacitance and C1). If we change VT the positive voltage of the oscillation will follow VT. The gate of the PMOS is copied to the output nodes. Instead of only using an inverter, which causes a delay in one branch, which would affect high frequency operation of the biosensor chip, we balance the clocking with a transmission gate (see Figure 4-15).

4.5 Output Stage Amplifier

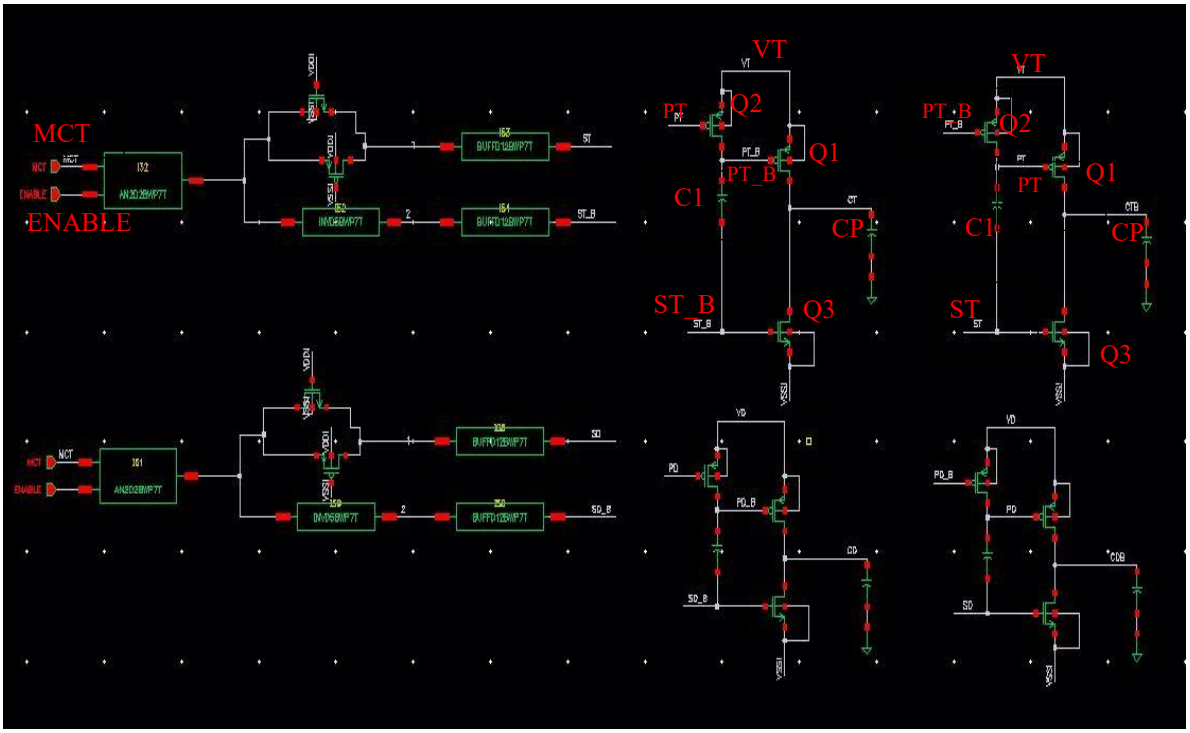

Figure 4-15 Output Stage Amplifier

The working of the output stage in Figure 4-15 is as follows. When the clock signal ST_B goes from low to high the potential PT_B of the transistor Q1 is lifted to a higher potential. The gate PT of the transistor Q2 is driven from the other output stage of clock ST, ensuring the voltage PT_B is clamped at voltage VT. At this moment Q1 is not conducting. When ST_B falls from high to low the capacitor C1, by capacitive division, pulls the gate voltage down by an amount proportional to the 1.8V logic input amplitude. The gate of Q1 varies with VT and the overdrive of the Q1 is same. Q1 is in conducting stage. CP is the output capacitance of the transmission line to the sensor chip. The circuit is optimized for Cp 1pF and the values transistor are as shown in Table 4-4

	Length	Width	Fingers
PMOS(Q1)	180nm	4u	21
PMOS(Q2)	180nm	4u	5
NMOS(Q3)	180nm	4u	5

Table 4-4 Output stage amplifier sizing

Figure 4-16 shows the clocks CT and CT_B for a load capacitance CP = 1pF.

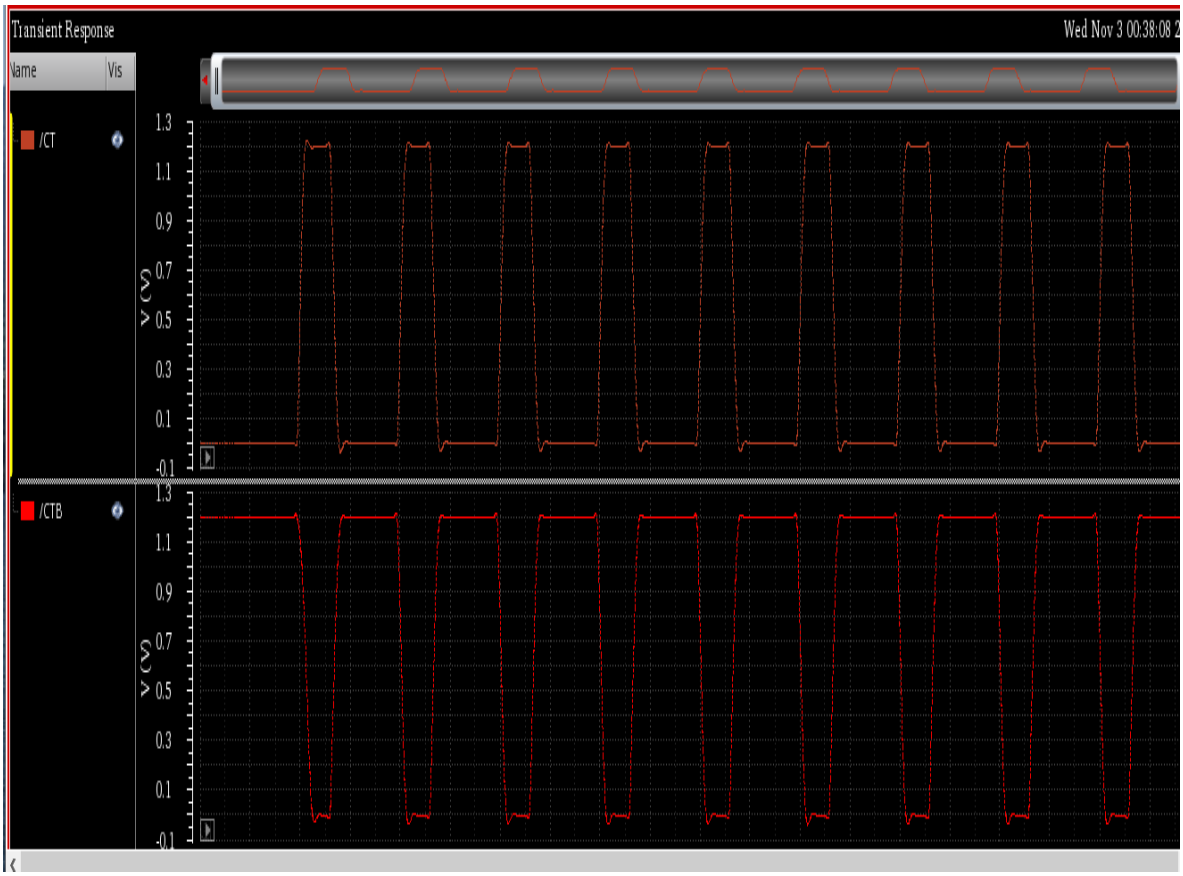

Figure 4-16 Spectre Simulation of Output Stage

The Layout and Symbol of the output stage is shown in Figure 4-17 and Figure 4-18 respectively.

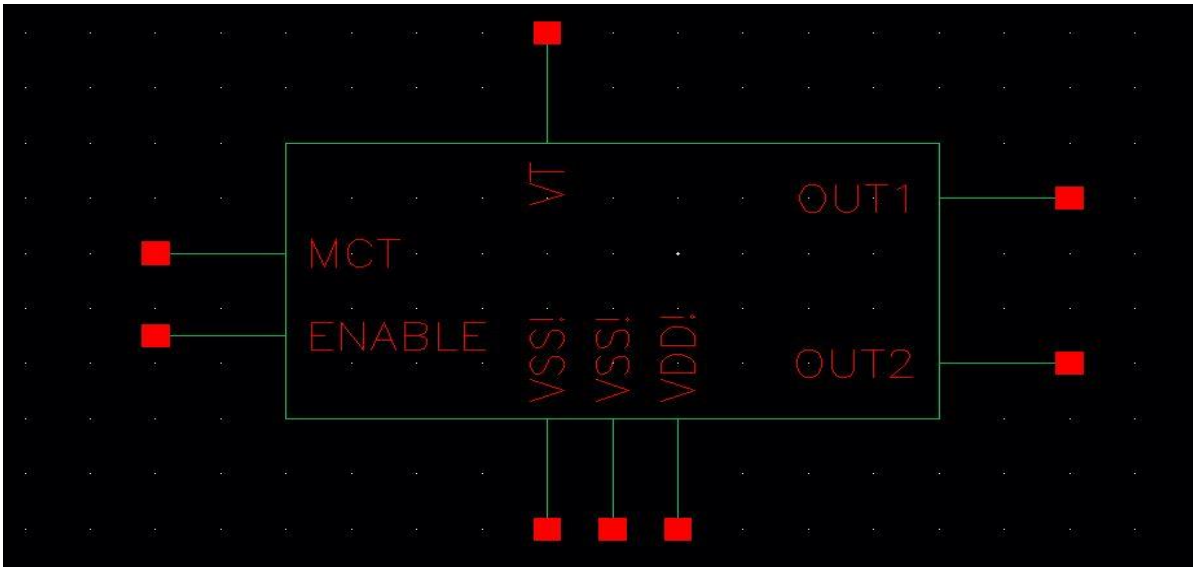

Figure 4-17 Symbol of output amplifier

No.	Pin	Description
1	VDD	Supply Voltage (1.8 V)
2	VSS	Ground (0 V)
3	VT	Supply Voltage (.7V -1.2V)
4	MCT	Input clock signal at 1.8 V
5	OUT1	Output clock signal range
6	OUT2	Inverted Output clock signal range
7	ENABLE	The pin should be switched from low to high and held constant

Table 4-5 Pin Description Output Amplifier

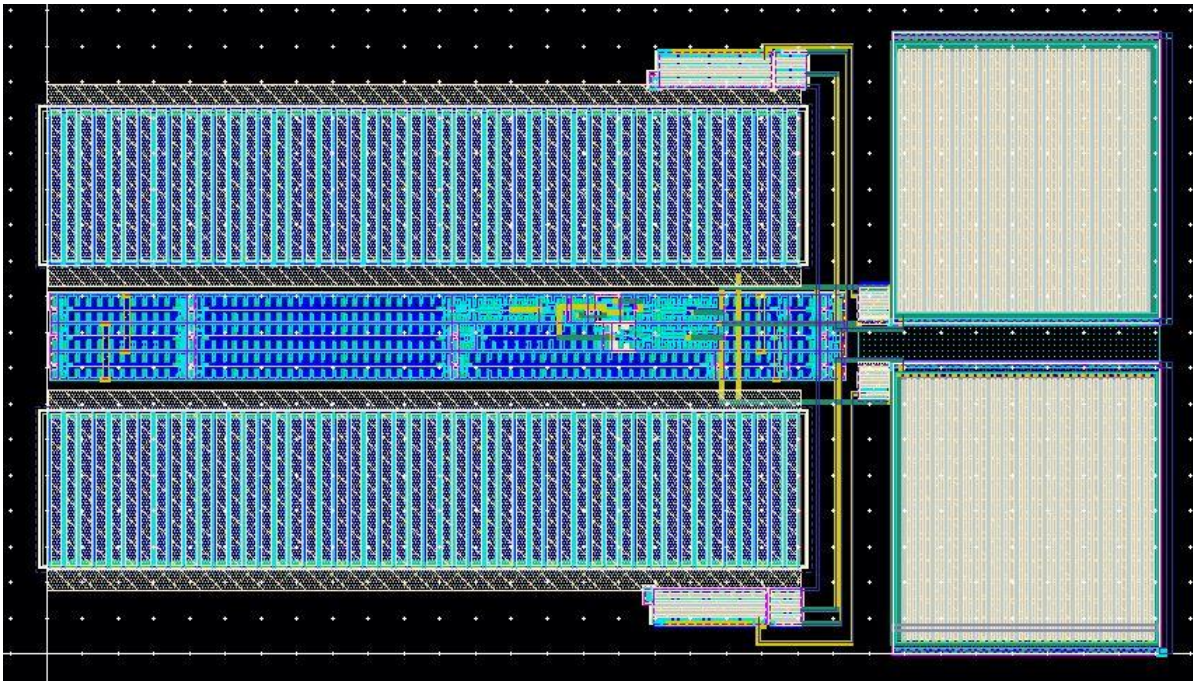

Figure 4-18 Layout of Output Stage Amplifier

5 Chapter 5

The final circuit and the ESD considerations for the clock generator are explained in this chapter.

5.1 Clock Generator

From the block diagram of the clock generator the circuit is implemented, Figure 5-1. Each block has the functional specifications explained in chapter 2.

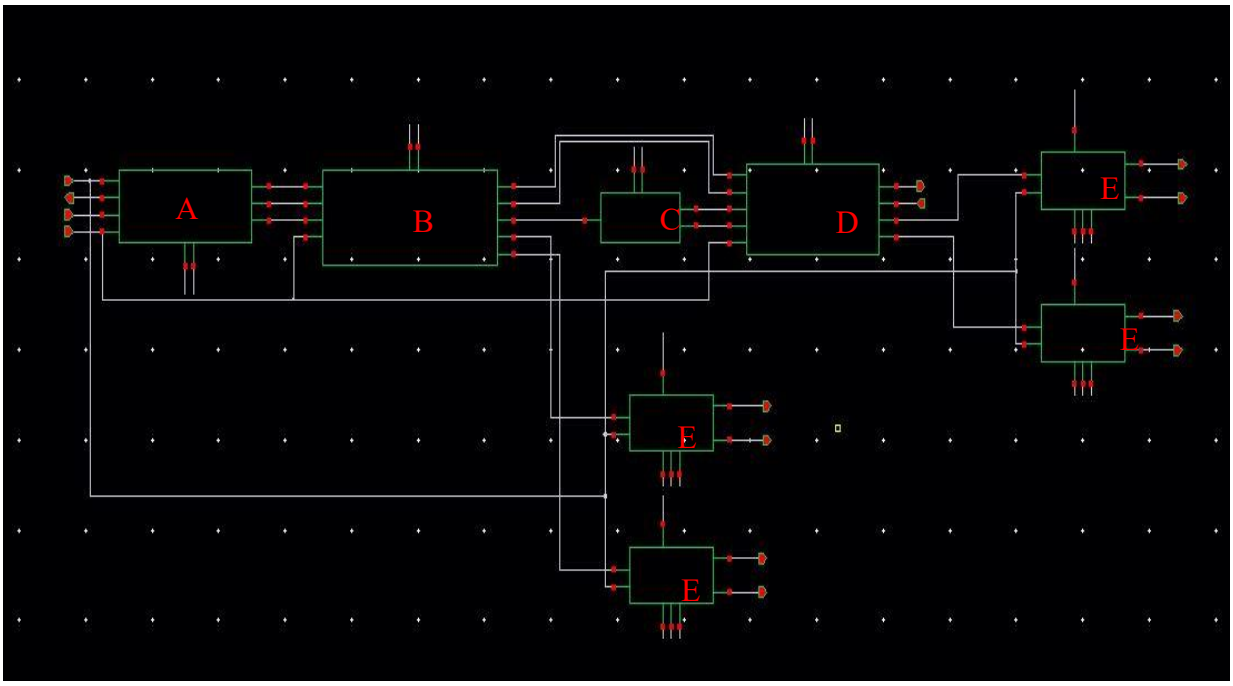

Figure 5-1 Schematic diagram of clock generator. A: Ring Oscillator, B: Programmable Frequency Divider, C: Transmission Gate, D: Non-overlapping Clock Generator, E: Output stage Amplifier

The symbol and pin descriptions are given in Figure 5-2 and Table 5-1.

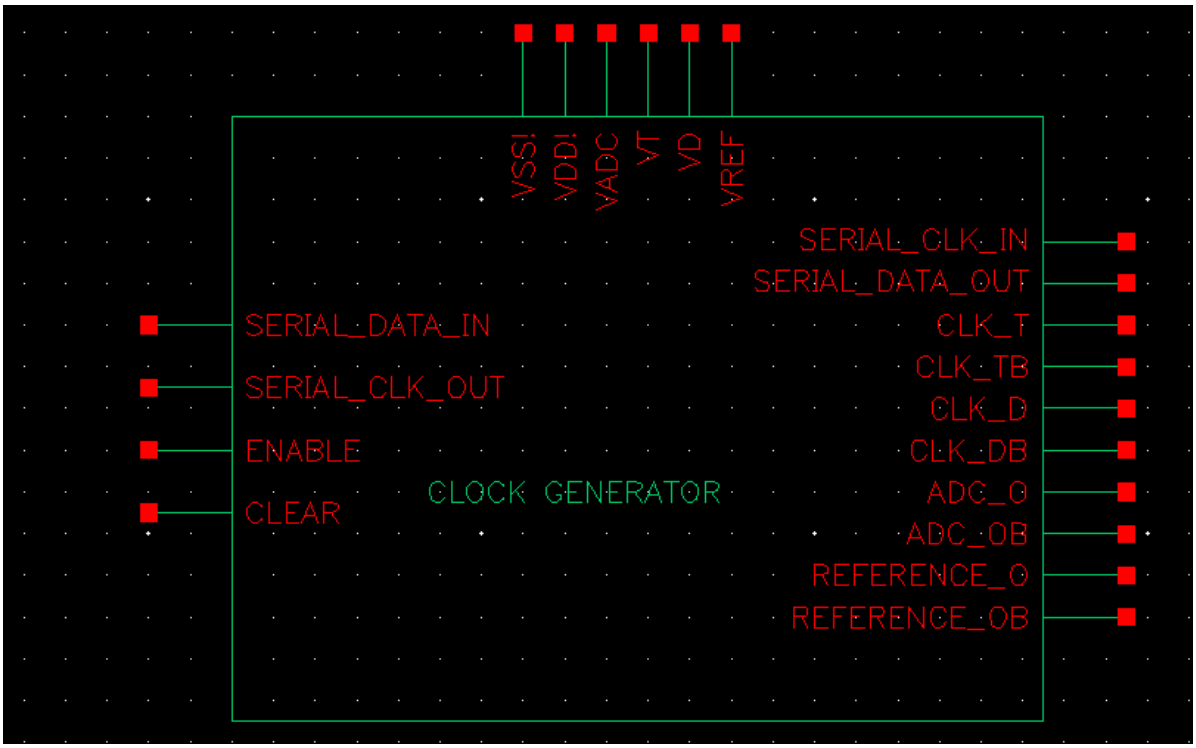

Figure 5-2 Symbol of the clock generator

No.	Pin	Description
1	VDD	Supply Voltage (1.8 V)
2	VSS	Ground (0 V)
3	VT,VD,VADC,VREF	Supply Voltage (.7V -1.2V)
4	SERIAL_CLOCK_IN	Clock signal input for FIFO
5	SERIAL_CLOCK_OUT	Clock signal output from FIFO

6	SERIAL_DATA_IN	Data input for FIFO
7	SERIAL_DATA_OUT	Serial data output from FIFO to read
8	ADC_O	The output clock signal for ADC ranges
9	ADC_OB	The inverted output clock signal for ADC ranges
10	CLK_D	Output clock signal range
11	CLK_DB	Inverted Output clock signal range
12	CLK_T	Output clock signal range
13	CLK_TB	Inverted Output clock signal range
14	REFERENCE_O	The clock signal to measure the frequency
15	REFERENCE_OB	Inverted clock signal to measure the frequency
16	CLEAR	Reset the FIFO
17	ENABLE	Start the clock generator

Table 5-1 Pin Description of Clock Generator

During the layout of the clock generator (Figure 5-3), it was taken care to place the output stages that generate the output clock signals CLK_T, CLK_D, CLK_TB, CLK_DB close to the bond pads, to avoid distortion of high-frequency components in long wires. The wires to the output stages are made wide enough to avoid electromigration. Electromigration is the transport of material caused by the gradual movement of ions in a conductor due to momentum transfer between conducting electrons and diffusing metal atoms. The effect is important in applications where high direct current densities are used, such as in microelectronics and related structures. As the structure size decreases in electronics, such as integrated circuits (ICs), the practical importance of this effect increases. The current density of metal layer 1-5 is 1mA/um. The maximum current flowing through this path is 4mA. Also, the currents are split in 2 or more parallel paths so that we can avoid using single very wide layer of metal.

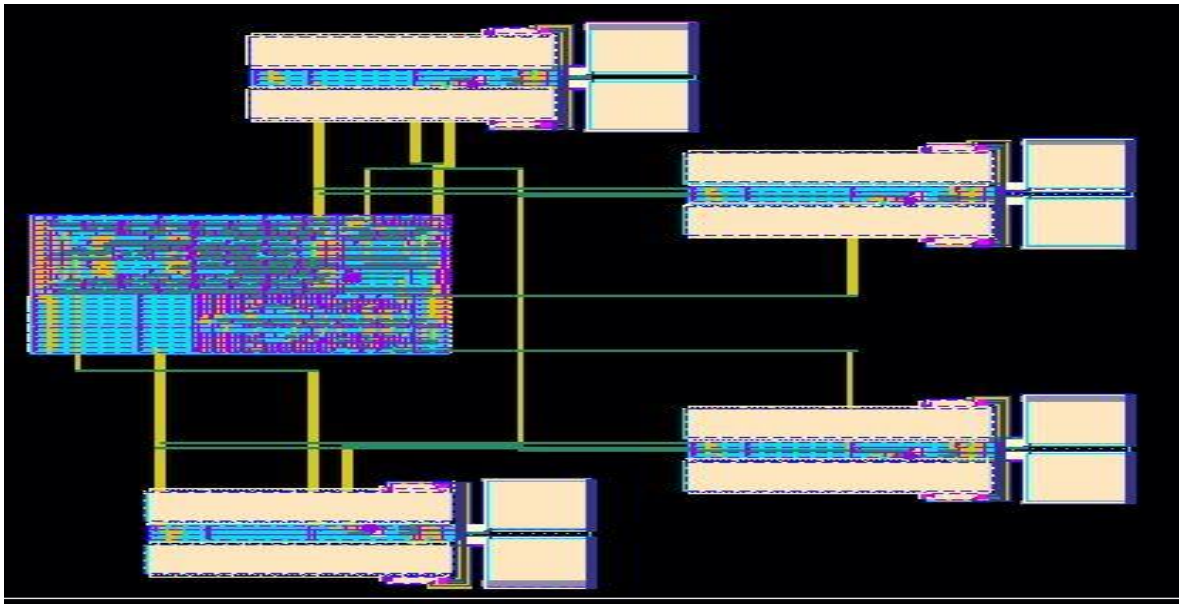

Figure 5-3 Layout of the clock generator

In post-layout simulation runs, high-quality non-overlapping output clock signals with frequencies from 1 MHz to 676 MHz is generated. The Figure 5-4 shows the final post layout simulation

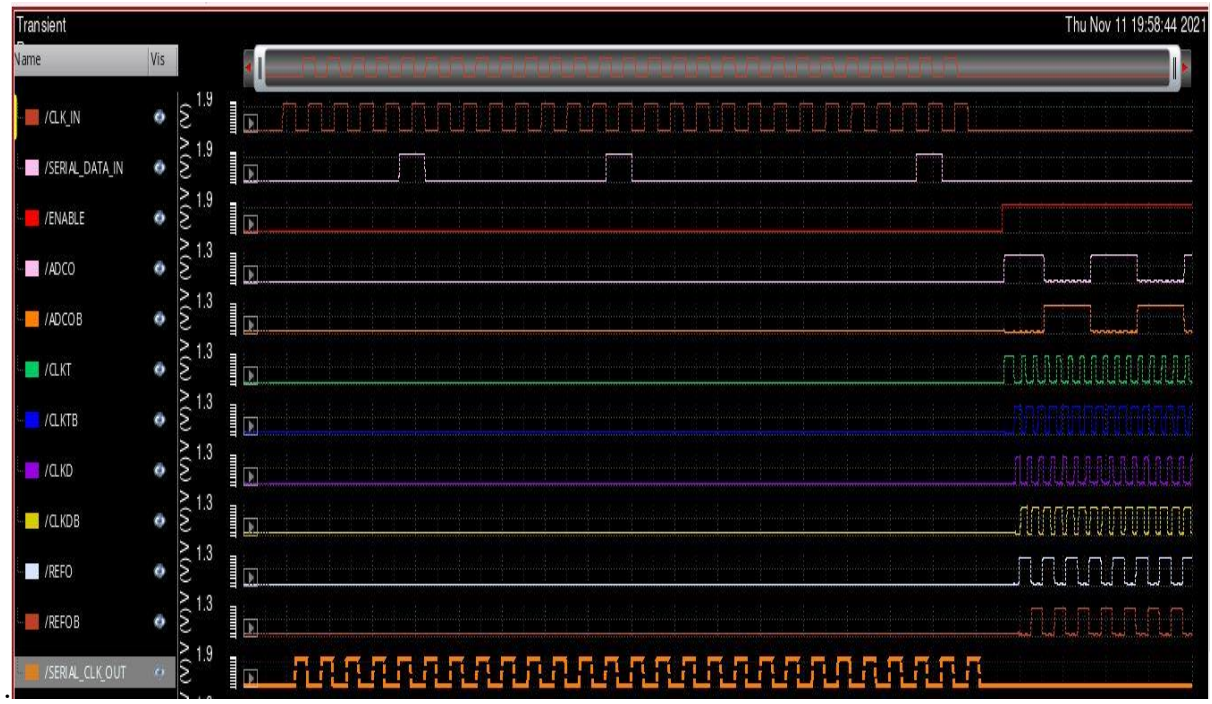

Figure 5-4 Final simulation

The clock generator was tested at 500MHz with different load capacitances and bond wire inductances. The generated clock signals are shown in Figure 5-5 to Figure 5-10.

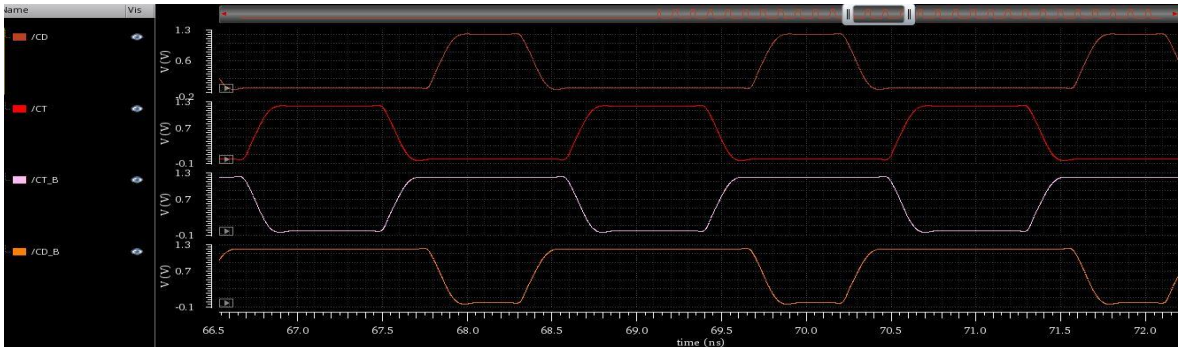

Figure 5-5 Output waveforms for 1 nH and 1 pF

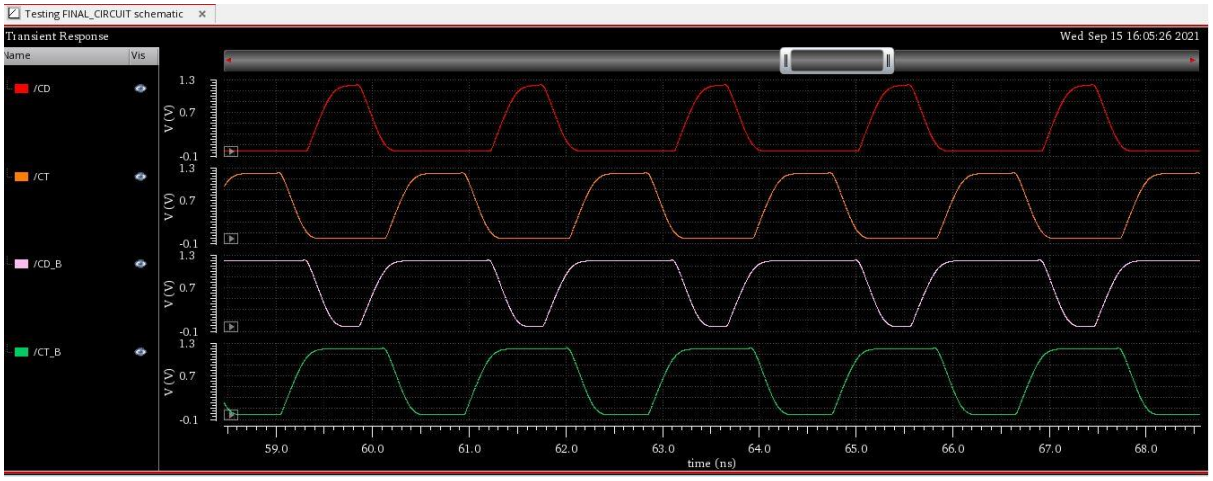

Figure 5-6 Output waveforms for 1 nH and 2 pF

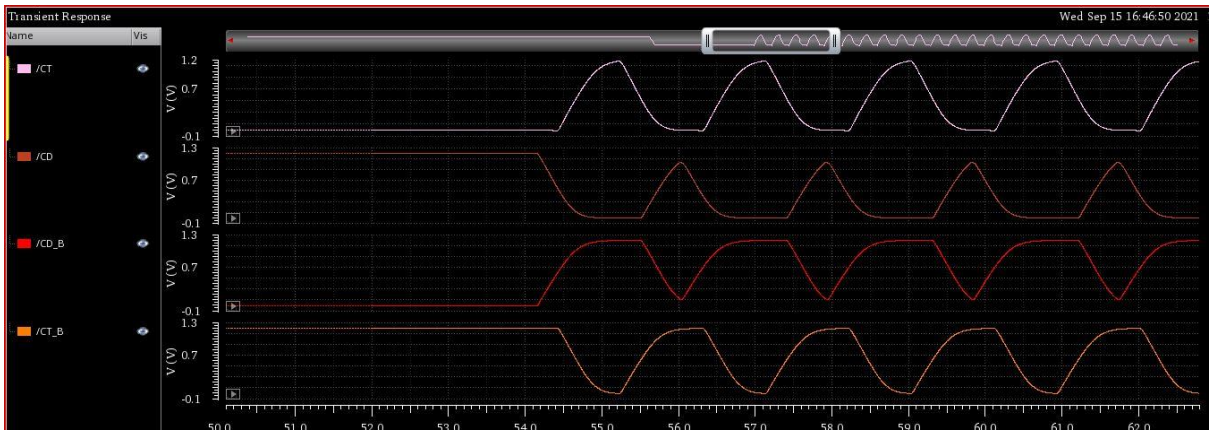

Figure 5-7 Output waveforms for 1 nH and 4 pF

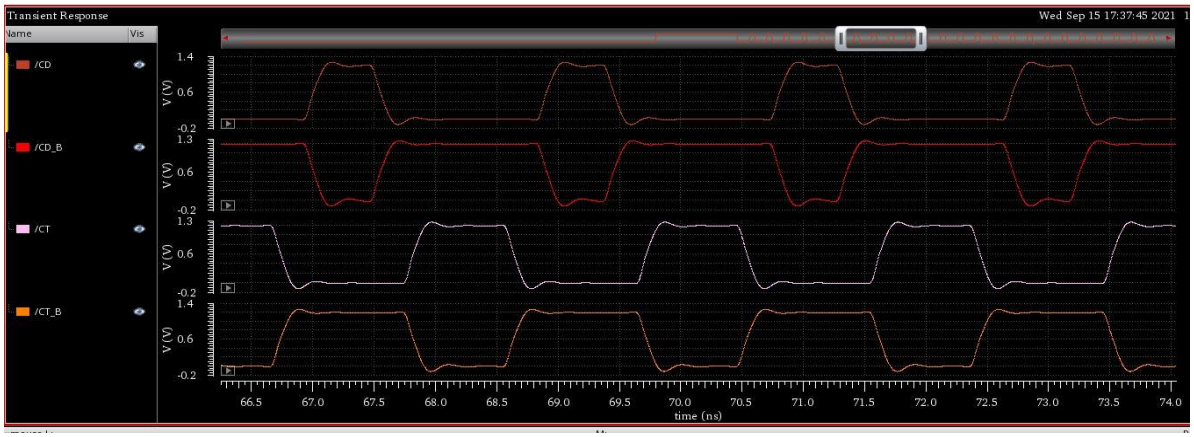

Figure 5-8 Output waveforms for 2 nH and 1 pF

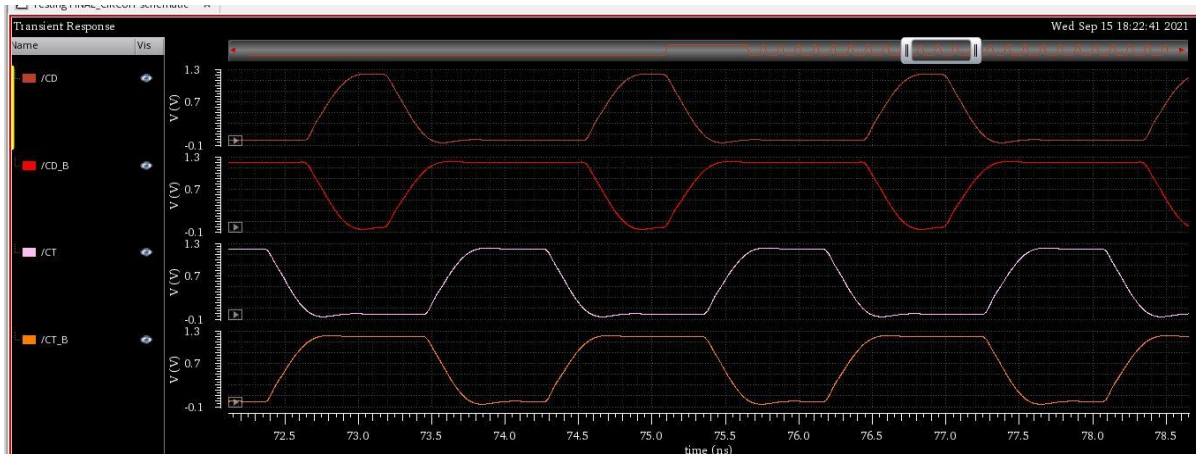

Figure 5-9 Output waveforms for 2 nH and 2 pF

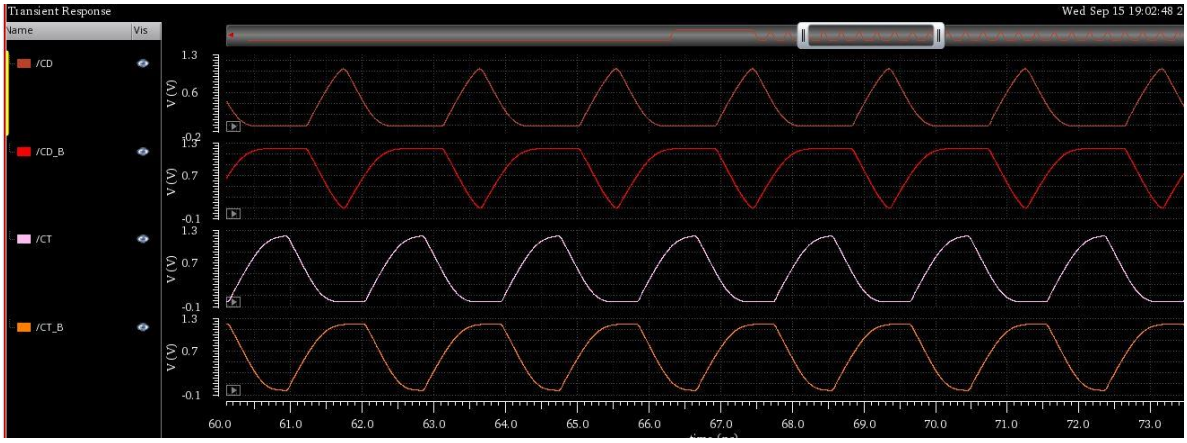

Figure 5-10 Output waveforms for 2 nH and 4 pF

From the figures it is evident that we can optimize the pulse edges playing with capacitance (C) and inductance (L). As we increase the C and L we get triangular pulses which are still useful as the sensor chip has triggers which can interpret for high and low. This is achievable because we can vary the pulse amplitude. The sensor chip is not completely resistive input as

the power dissipation will be too much. So, working with C and L is better. They can also cancelled each other with their complex terms.

5.2 Electrostatic discharge protection

Electrostatic discharge protection (ESD) is critical in advanced nodes to protect CMOS circuits from effects amplified by shrinking transistor dimensions and oxide film thicknesses. On the other hand, due to the growing size of System-on-chips (SoCs) and the number of transistors they contain, the protection tests of ESD are consuming more and more runtime and memory. Developers face increasing challenges in verifying ESD protection requirements and interconnect strength, not only at the intellectual property (IP) and large block level but to verifying the entire chip. New tools and techniques are easing the burden of ESD verification and improving product reliability.

Anyone who has ever walked across a carpet and gotten a shock when touching a doorknob knows exactly what an ESD event is. In an integrated circuit (IC), an ESD event typically induces electrical currents on the order of 0.1-10 amps, lasting between 10^{-6} and 10^{-3} seconds, dissipating powers on the order of 10-100 Watt. ESD Protection methods dissipate these ESD currents through unpowered devices (ESD protection devices) along intended ESD discharge paths while clamping the voltage at a safe level, preventing degradation of the function of the protected equipment.

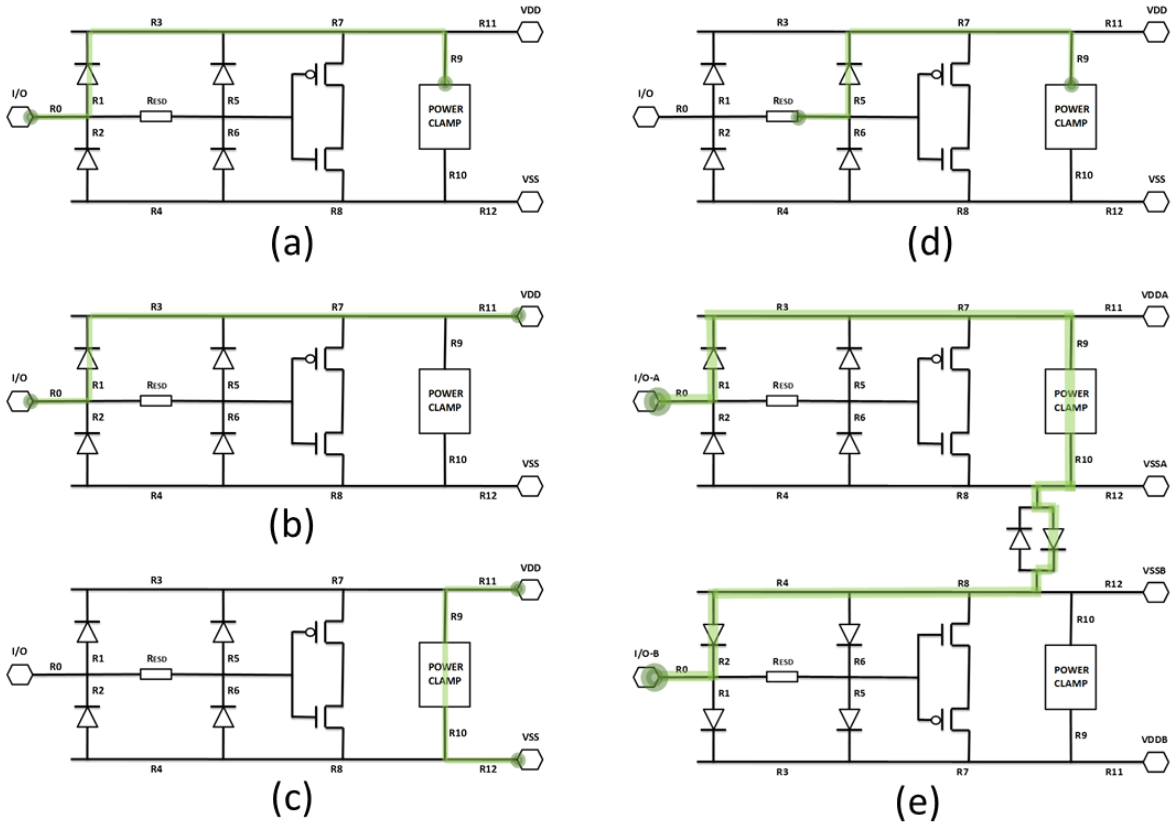

Figure 5-11 Common ESD protection schemes

Typical ESD protection systems are shown in Figure 5-11. The common ESD discharge paths (highlighted in green) run between:

a. I/O pin and power clamp
b. I/O pin and power pin
c. Power pin and ground pin
d. ESD resistor and power clamp
e. I/O pin and I/O pin

In layouts (a)-(d), the I/O pad is protected by pull-up and pull-down diodes, an ESD resistor, and secondary ESD diodes. A power clamp is connected between the supply bus VDD and the ground bus VSS. In layout (e), a pair of a back-to-back (B2B) connected diodes is used to connect the VSSA and VSSB ground busses of two power domains [43].

In TSMC 180nm, the Bond pads are divided into two categories

- Power pads
- Signal pads

There are two different types of power pads :

- IO pads, including PVDD3A and PVSS3A, pad ring voltage of 3.3V (i.e., IO voltage).
- Corepad, including PVDD3AC and PVSS3AC, pad ring voltage of 1.8V (i.e., core voltage), where C is core.

Similarly, signal pad falls into two categories:

- IO pad, called PDBXA, with a pad ring voltage of 3.3V (i.e. io voltage);
- Corepad, called PDBXAC, with a pad ring voltage of 1.8V (i.e. core voltage), where C stands for core, X can be 1, 2, or 3, and stands for 3 pads with different sized parasitic capacitors.

The features of bond pads used are shown in Table 5-2

Pads	Port to core	Port to Pad	Power & Ground	Purpose
PVDD3AC	AVDD	TACVDD	TACVDD, VSS	Power source for both analog macro and analog I/O power rail (voltage is the same as the pre-driver voltage of Digital I/O)
PVSS3AC	AVSS	AVSS	TACVDD,VSS	Ground provider used with PVDD3AC power cell

Table 5-2 Bond pad features

In addition to the ESD protection provided by the pads, secondary ESD is required if a MOS gate or drain is to be connected to a pad. This extra protection can be applied using the circuit in Figure 5-11, where a resistor is in series with a PMOS protection device to power and an NMOS protection device to ground.

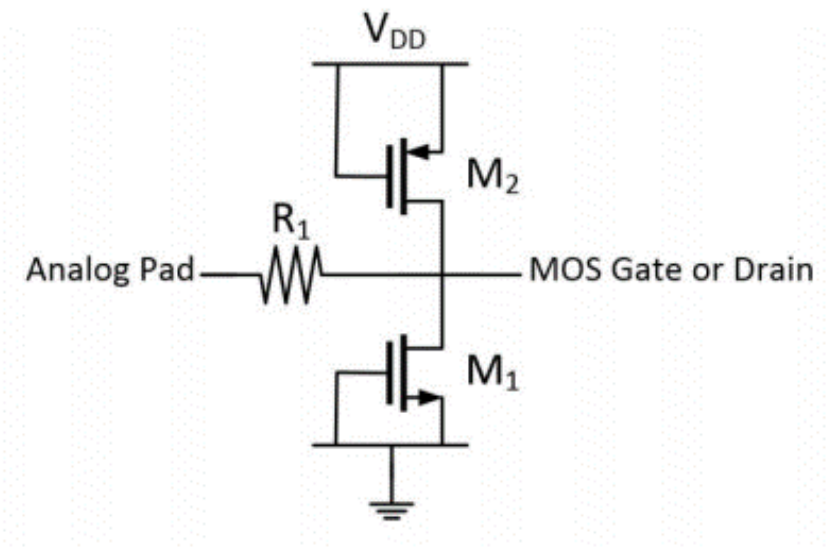

Figure 5-12 Secondary ESD protection

From the standard I/O library we used Dual-Driving Regular I/O Cell with Schmitt Trigger Input and Enable-Controlled Pull-Up Resistor -PDDW1216SCDG as the digital pin Figure 5-13. By setting the programmable pins to proper values we can achieve the input/output-only purpose pins.

Table 5-3 shows the functions of each pins.

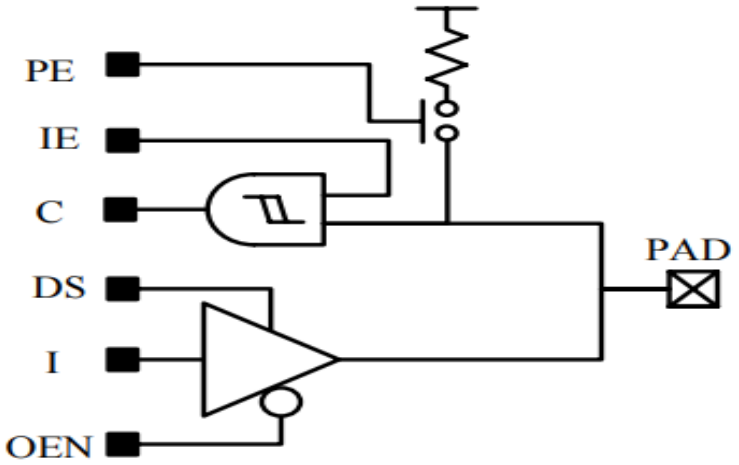

Figure 5-13 Digital Pin PDDW1216SCDG

DS	Drive Select	Tie to VDD or Ground
PE	Pull Enable	Tie to VDD or Ground
IE	(Input Enable) to enable the path from PAD to C	Tie to VDD or Ground
OEN	(Output Enable) to enable the path from I to PAD	Tie to VDD or Ground

Table 5-3 Programmable pins to control the I/O

5.3 Conclusion

In this thesis project, a non-overlapping clock generator chip for frequencies up to at least 500 MHz has been proposed and designed in the TSMC 180nm technology node. The post layout simulations shows that the clock generator can produce frequencies from 1 MHz to 676 MHz. This will help the biosensing measurements suffering less from false signals caused by non-specific binding of molecules to the nanoelectrodes. The new chip also overcome the distortion of clock pulses in the previous control system due to non-optimal impedance matching conditions and crosstalk in the long clock wires.

Along with frequency generation the clock signals are coarsely programmable i.e. pulse width, non-overlap delay, and low & high voltage levels. The chip also generates an ADC clock signal of 14 MHz to 47 MHz for the 8 on-chip ADCs of the sensor chip. In addition a reference clock signal is generated for clock frequency calibration.

5.4 Future work

The project was completed during the COVID-19 pandemic, which was a major main constraint. Due to the situation, technical support could not be given as originally planned. This led to some limitations in development of the project. Therefore, the non-overlapping clock generator for the unique Pixelated Capacitive Biosensor chip still has many possibilities for further improvement.

One of them, the frequency divider in the current chip, is using the divide by two method. The digital frequency dividers give discrete clock frequencies. For the lower frequencies, this isn’t

an issue, because the ratios N/(N+1) of neighboring clock frequencies can be close to 1 for large division ratios N. But, for small N, especially for N = 1, we need to interpolate between the discrete steps. This is why we need the programmable ring oscillator. E.g. if N = 1 and N =2 give nominal frequencies of 500 MHz and 250 MHz, respectively, for an input frequency of 1 GHz, then we must cover intermediate frequencies between 250 and 500 MHz by fine-tuning the programmable ring oscillator. However, there are frequencies we still can't produce. This can be improved by a phase lock loop (PLL) to have fine tuning range. This would also allow replacing the ring oscillator by a more accurate and stable quartz crystal clock generator, taking away the need for external calibration of the output clock frequency.

When looking at the delay line, we see that it contains many inverters. This consumes quite some chip area. And, it makes it difficult to keep all signal wires short. If they get too long, they will have increased parasitic capacitance, which can disturb the symmetry between the CLK_T and CLK_D parts, or the logarithmic distribution of the non-overlapping delays. In addition, long wires can pick up cross-talk from other lines. Therefore, it makes sense to look for ways to reduce the number of inverters, e.g. by using current-starved delay gates.

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Appendix

Matlab Code

The code below is used to generate the SERIAL DATA IN for the clock generator. The data include frequency and delay selection.

```
%Ring Oscillator
prompt = 'Enter the seletion bit of ring oscilators from 1 to 4\n';
x = input(prompt);
if x == 1
   n = 000;
   r = sprintf( '%03d', n );
   disp (r);
elseif x == 2
   n = 001;
   r = sprintf( '%03d', n );
   disp(r);
elseif x == 3
   n = 010;
   r = sprintf( '%03d', n );
   disp(r);
elseif x == 4
   n = 100;
   r = sprintf( '%03d', n );
   disp(r);
else
   disp('Error');
end

%Frequency Divider Reference Clock
```

```
prompt = 'Enter the number of division for frequency divider of Reference clock from 1 to 9\n';
y = input(prompt);
if y == 1
    n = 00000000;
    rf = sprintf( '%08d', n );
    disp (rf);
elseif y == 2
    n = 0000001;
    rf = sprintf( '%08d', n );
    disp(rf);
elseif y == 3
    n = 00000010;
    rf = sprintf( '%08d', n );
    disp(rf);
elseif y == 4
    n = 01000000;
    rf = sprintf( '%08d', n );
    disp(rf);
elseif y == 5
    n = 01000100;
    rf = sprintf( '%08d', n );
    disp(rf);
elseif y == 6
    n = 01001000;
    rf = sprintf( '%08d', n );
    disp(rf);
elseif y == 7
    n = 10000000;
    rf = sprintf( '%08d', n );
    disp(rf);
elseif y == 8
    n = 10010000;
    f = sprintf( '%08d', n );
    disp(f);
```

```
else
   disp('Error');
end

%Frequency Divider
prompt = 'Enter the number of division for frequency divider from 1 to 9\n';
y = input(prompt);
if y == 1
   n = 00000000;
   f = sprintf( '%08d', n );
   disp (f);
elseif y == 2
   n = 0000001;
   f = sprintf( '%08d', n );
   disp(f);
elseif y == 3
   n = 00000010;
   f = sprintf( '%08d', n );
   disp(f);
elseif y == 4
   n = 01000000;
   f = sprintf( '%08d', n );
   disp(f);
elseif y == 5
   n = 01000100;
   f = sprintf( '%08d', n );
   disp(f);
elseif y == 6
   n = 01001000;
   f = sprintf( '%08d', n );
   disp(f);
elseif y == 7
   n = 10000000;
   f = sprintf( '%08d', n );
```

```
    disp(f);
elseif y == 8
    n = 10010000;
    f = sprintf( '%08d', n );
    disp(f);
elseif y == 9
    n = 10100000;
    f = sprintf( '%08d', n );
    disp(f);
else
    disp('Error');
end
%ADC
prompt = 'Enter the stageof ADC from 1 to 3\n';
ad = input(prompt);
if ad == 1
    n = 00;
    adc = sprintf( '%02d', n );
    disp (adc);
elseif ad == 2
    n = 01;
    adc = sprintf( '%02d', n );
    disp(adc);
elseif ad == 3
    n = 10;
    adc = sprintf( '%02d', n );
    disp(adc);
else
    disp('Error');
end

%Delay Line
prompt = 'Enter the delay increasing from 1 to 6 \n';
de = input(prompt);
```

```
if de == 1
    n = 000000;
    d = sprintf( '%06d', n );
    disp (d);
elseif de == 2
    n = 000001;
    d = sprintf( '%06d', n );
    disp(d);
elseif de == 3
    n = 000010;
    d = sprintf( '%06d', n );
    disp(d);
elseif de == 4
    n = 000100;
    d = sprintf( '%06d', n );
    disp (d);
elseif de == 5
    n = 001000;
    d = sprintf( '%06d', n );
    disp(d);
elseif de == 6
    n = 010000;
    d = sprintf( '%06d', n );
    disp(d);
 else
    disp('Error');
end
a1=num2str(r);
b1=num2str(adc);
c1=num2str(f);
d1=num2str(rf);
e1=num2str(d);
data_a = strcat(e1,d1,c1,b1,a1);
fprintf('serial_data_in %027s \n', data_a );
```