POLITECNICO DI TORINO

Master's Degree in analog and power electronics design

Master's Degree Thesis

Integration of digital potentiometers in analog circuits

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Summary

The implementation of digital potentiometers in analog circuits allows the designer to perform a series of functionalities which are nearly impossible to achieve in the traditional scope, with analog potentiometers. This is possible because digital potentiometers usually work in close relationship with microcontrollers, which drive the potentiometers with streams of bit that indicate in a unique way the "position" of the wipers. The microcontrollers have the possibility to menage information in a sophisticated way, so that the external command can be processed, making the circuit they are controlling programmable. A clear example of the advantages of this design is the possibility of recalling pre-sets in audio circuit, for instance, the different setting of an equalisation network in a hi-fi system can be achieved exploiting the memory capability of the microcontrollers that drives the potentiometer inside the circuit itself. These capabilities of a digital control circuit on an analog process derives from the fact that the digital potentiometers are the transducer from a digital information to an analog one, being them very similar in their functioning to DACs (digital to analog converters). The difficulty of the substitution of the digital devices in place of the analog ones is embedded in the fact that the use of the first ones is prone to a series of setbacks, which in some cases can be solved just with a different choice of the commercial device, whilst in some other it requires the design of a proper modified circuit. The problems related to the potentiometers substitution basically are related to two different aspects: the restricted range available for the voltages at the terminal of the digital potentiometers and the injection of zipper noise into the signal path.

The aim of the present thesis is to show how it is possible to overcome the above mentioned problems. To do so, an analysis of some representative analog circuit is required, in order to have an as precise as possible measure of the voltages, currents and powers related to the analog potentiometers in the traditional circuits. This is fundamental in order to perform a correct choice of the type of digital devices suitable for a particular substitution, as well as a correct supply of the chosen ones, eventually modifying the original circuit in order to adapt it to the new necessities. The related chapter presents the analysis of some basic circuits, which result very general in their simplicity. For instance, considering operational

amplifiers, the simple inverting and non-inverting topologies are studied, followed by a more complicated instrumentation amplifier, which offers an example of a slightly different work condition for the potentiometer. Some transistors-based circuits are then discussed pointing out also the differences in the approach with respect to an op-amp circuit, followed by an analysis of some important oscillators, whose functioning heavily depends on potentiometers.

Once the preliminary discussion is finished, the thesis gets to the heart of the digital potentiometer subject. A first overview of their functioning principle and structure is performed in order to pointing out what are the characteristics of this devices that limits the most the action of the designer. The theoretical analysis continues presenting both supply and noise issues and an overview of some possible hardware solutions. The integration of digital potentiometer into the circuit of a non-inverting amplifier is theoretically performed and discussed at this point as an application of the theory presented till this point. Concerning, instead, the noise rejection method, an audio output muting system is presented in four different versions (exploiting different devices, e.g. JFET or opto-coupler) as well as some more sophisticated technique such as the zero-crossing-window technique.

To effectively explore some of the solutions that can be introduced to deal with the digital in place of analog substitution a prototyping board has been designed. This board is able to work in conjunction with a pre-existent board designed by Carlo Sorasio at the LAA Custom[1] laboratory. The PCB designed implements some of the representative circuits previously discussed with the digital potentiometers and it is designed so that it can operate in different way accordingly to the desire of the user by means of jumpers that patch the circuits as wanted. This modularity is important to properly show what are the choices and the parameters that can be tweaked inside the different solutions in order to understand what the most convenient topology for a certain circuit is.

In Figure 1 a picture of the physical prototype have been reported. Notice the two different board mounted one on top of the other: the bottom black one is the one specifically designed for the purpose of this thesis and implement the analog part, while the green one is the already existent one that implement the digital control (with four potentiometers on board).

The results of the measurements obtained are then reported to notice what are the critical issues of each solution, for example the trade-off between the noise rejection and the bandwidth in transparent mode is crucial for some topologies. In Figure 2 an example of the measurements done is produced: the signal at the output of one of the muting circuit analysed (*JFET-parallel*) in muting mode for the same topology with one or two stages of attenuation. In Figure 2 also

[1]Link to the main page of the brand: `https://www.laa-custom.com/`.

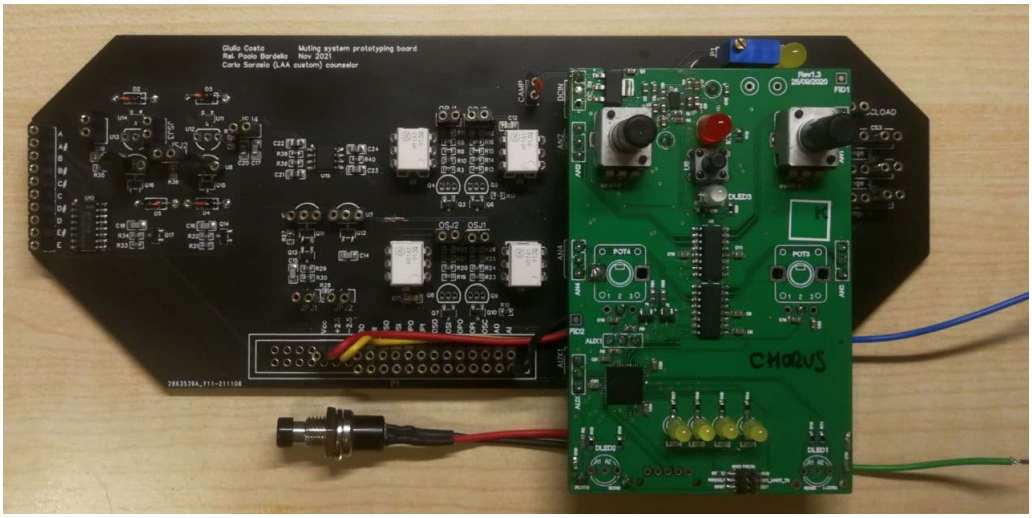

Figure 1: Experimental board photograph.

the envelope calculated for each wave are plotted. This type of measurements is useful to calculate the amplitudes of the different signal, evaluate the attenuation performances and finally compare the results obtained. This procedure allows to evaluate each circuit and give an idea of the convenience of each one.

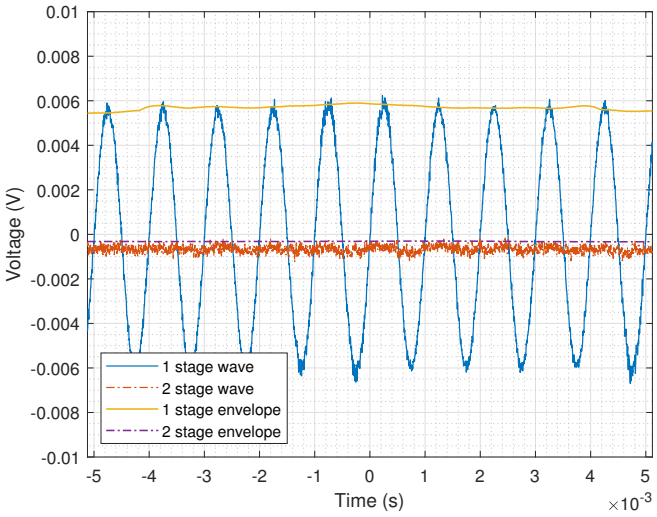

Figure 2: Example of a *JFET-parallel* muting circuit waveforms in mute condition with an input signal of amplitude 1 V at 1 kHz. Notice the different amplitudes of the residual output signal for solutions with one or two stages.

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Chapter 1

Preliminary analysis

The aim of this chapter is to identify the most common and representative analog circuits in which analog potentiometers are traditionally implemented, such as amplifiers, oscillators, filters and general passive networks. The analysis proposed in this chapter aims to give the basic knowledge for what concerns the electrical quantities related to the potentiometer. This will introduce the concepts of voltage ranges, current rates, power stresses, handled by the traditional potentiometer; so that the substitution of the analog device, with the digital one, can be done wisely. The analysis of the circuits included in this chapter are not meant to be the more deep and complete ones, since a standard approach to the circuit is generally sufficient to establish the limits and ranges that the device handles. The following sections form the basis from which the successive chapters will be developed.

1.1 Amplifiers

One of the most frequently encountered circuit class in analog design is the amplifier. Their analysis seems unavoidable, since, for example, amplifiers are part of conditioning circuit for sensors, basic block for audio and signal communication and manipulation, part of the drivers of many actuators, part of closed loop systems. In many cases, the amplifier is designed in such a way that it can be controlled by the users, from the external of the device, in at least one of its characteristics, which often results to be the gain. Controlling the gain is often done by varying the value of a resistor inside the circuit exploiting a potentiometer. This means that this class of circuit falls *in toto* into the discussion here developed.

The type of amplifier is traditionally determined on the nature of the signal in-coming at the input port and on the one of the out-coming signal[1]; so that the

[1]The terminology comes from the assumption that the amplifier is modelled as a *two-port*

traditional four classes are identified: *voltage*, *current*, *transimpedance*, *transresistance* amplifiers, depending on the nature of source and load. The most common genre is the voltage one [1], even though the other classes are well present in general.

The two port definition leads to some considerations about the definition of the properties of the ports themselves. The input one usually exhibits a passive behaviour and so it is normally modelled with an impedance (in case of an analysis which neglect the inductive capacitive effects, simply a resistance, R_{in}). The output port is related to the nature of the amplifier: in case of a voltage amplifier the output port will be driven by a voltage controlled voltage source (comprehensive of its output impedance). This is precisely the idealised model exploited to analyse the operational amplifier based circuit, in which the active device (namely the op-amp) is considered as a voltage amplifier. Also the linearised models (small signal models) of transistors are circuit defined starting from a two-port approach and it will be used.

The amplifier stages in general can be implemented in a very large number of different ways depending on the specific purpose. In this context the main classification of voltage amplifier is done by considering the nature of the active device exploited. Just to give a structure to the discussion, a class can be identified as the one that uses op-amp, another is the BJT based one, *ecc.*

For sure, the differences between the devices that characterise different classes of amplifiers make the analysis of the latter totally independent the one from the other. This holds even if some procedures are common to all the solutions: for instance the distinction between a linear and a saturation region of operation. The differences between the two will be well investigated in the following, but, to begin with, an analytic major difference relays in the strongly different active device circuital model.

The analysis of some basic amplifier circuit solutions aims to provide some examples of how to proceed even when more complex designs are considered.

1.1.1 Op-amp based stages

The op-amp can be used to design audio amplifiers in a very straightforward way, at least at a first level of complexity. Two basic different topologies are involved, namely the inverting configuration and non-inverting one. The simplicity of these topologies is directly related to their generality and so they become crucial during the development of this analysis. The procedure to analyse this two circuits is basically the same but, even if it can in principle lead to quite similar results, also some non-negligible differences need to be to pointed out.

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device.

Also, the analysis of the electrical quantities of the potentiometer of an instrumentation amplifier is discussed in order to present a more complex circuit example. In the following a frequency independent analysis is developed, since this is the basis of all the designs.

Inverting op-amp amplifier

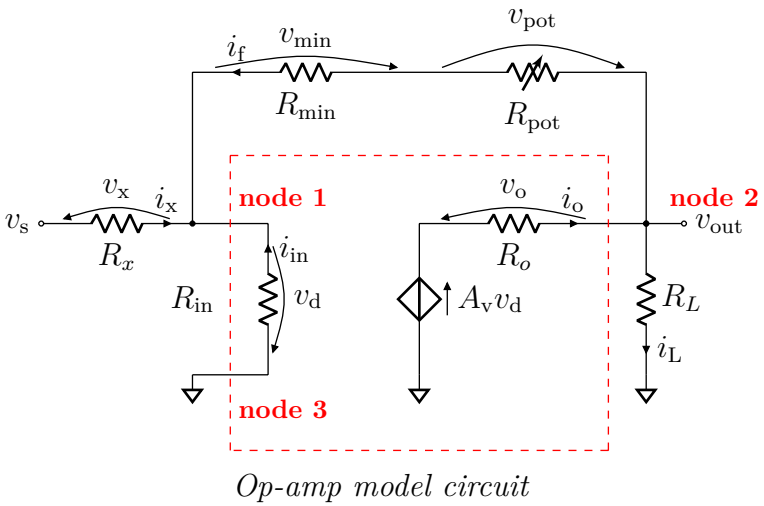


Figure 1.1: Basic op-amp based inverting amplifier circuit

For the analysis of the circuit above (Figure 1.1) two independent meshes and the two corresponding KVLs can be exploited. For sake of brevity, in the following calculations, the dependence of the variables with respect to time will not be made explicit in the notation, but the fact that the input signal $v_s(t)$ injected at the input of the circuit is a time dependent signal is natural; so all the other quantities exhibit a time dependence too. This assumption does not impact on the following first analysis because it will be carried on by neglecting all reactive effects, since the aim of this first discussion is to reach expressions for the rating of the electrical quantities. Another way to see this is that the analysis here performed involves a signal whose frequency falls into the *band* of the amplifier.

- The first mesh, above mentioned, is the input one:

$$v_s - v_x + v_d = 0 \tag{1.1}$$

  v_s is the input voltage so it has to be consider as a datum. Now consider v_x and write it as a function of v_d (the differential input voltage) and v_L (the

output voltage).

$$\begin{aligned} v_\mathrm{x} &= R_\mathrm{x} i_\mathrm{x} = R_\mathrm{x}(-i_\mathrm{in} - i_\mathrm{f}) = \\ &= -R_\mathrm{x}\left(\frac{v_\mathrm{d}}{R_\mathrm{in}} + \underbrace{\frac{v_\mathrm{L} + v_\mathrm{d}}{R_\mathrm{f}}}_{v_\mathrm{f}/R_\mathrm{f}}\right) = \\ &= -\frac{R_\mathrm{x}}{R_\mathrm{f}} v_\mathrm{L} - R_\mathrm{x}\left(\frac{1}{R_\mathrm{in}} + \frac{1}{R_\mathrm{f}}\right) v_\mathrm{d} \end{aligned} \tag{1.2}$$

In which the KCL equation at the inverting input node (node 1), and the feedback mesh across input, feedback itself and output have been exploited. Now Eq.1.2 can be substituted into Eq.1.1, which, recollecting some terms and moving the known term to the right hand side looks like follow:

$$\left[1 + R_\mathrm{x}\left(\frac{1}{R_\mathrm{in}} + \frac{1}{R_\mathrm{f}}\right)\right] v_\mathrm{d} + \frac{R_\mathrm{x}}{R_\mathrm{f}} v_\mathrm{L} = -v_\mathrm{s} \tag{1.3}$$

Eq.1.3 can be rewritten by defining, for sake of simplicity, the two equivalent conductances (G_fL is used in the following, but it is already defined here):

$$G_\mathrm{fin} := \frac{1}{R_\mathrm{in}} + \frac{1}{R_\mathrm{f}} \tag{1.4}$$

$$G_\mathrm{fL} := \frac{1}{R_\mathrm{L}} + \frac{1}{R_\mathrm{f}} \tag{1.5}$$

So that Eq.1.3 writes

$$\left[1 + R_\mathrm{x} G_\mathrm{fin}\right] v_\mathrm{d} + \frac{R_\mathrm{x}}{R_\mathrm{f}} v_\mathrm{L} = -v_\mathrm{s} \tag{1.6}$$

Now, the aim is to find another independent equation in v_L and v_d to construct a linear system that can be solved in these two unknowns.

- To do this, the output mesh KVL equation has to be written.

$$A_\mathrm{v} v_\mathrm{d} - v_\mathrm{o} - v_\mathrm{L} = 0 \tag{1.7}$$

This equation has a similar structure compared to Eq.1.1, in which only the term v_o, the voltage drop across the output resistance of the non-ideal op-amp, has to be re-written in order to make only v_d and v_L appear in the expression. To do this the KCL at the output node (node 2) and the Ohm's low are used.

$$
\begin{aligned}
v_\mathrm{o} &= R_\mathrm{o} i_\mathrm{o} = R_\mathrm{o}(i_\mathrm{L} + i_\mathrm{f}) = \\
&= R_\mathrm{o}\left(\frac{v_\mathrm{L}}{R_\mathrm{L}} + \underbrace{\frac{v_\mathrm{L} + v_\mathrm{d}}{R_\mathrm{f}}}_{v_\mathrm{f}/R_\mathrm{f}}\right) = \\
&= \frac{R_\mathrm{o}}{R_\mathrm{f}} v_\mathrm{d} + R_\mathrm{o}\left(\frac{1}{R_\mathrm{L}} + \frac{1}{R_\mathrm{f}}\right) v_\mathrm{L}
\end{aligned} \tag{1.8}
$$

Following the same procedure as before, Eq.1.8 is substituted into Eq.1.7 (also the definition of G_fL in Eq.1.5 is exploited).

$$
\left[A_\mathrm{v} - \frac{R_\mathrm{o}}{R_\mathrm{f}}\right] v_\mathrm{d} - \left[1 + R_\mathrm{o} G_\mathrm{fL}\right] v_\mathrm{L} = 0 \tag{1.9}
$$

Now we have two equations (Eq.1.6 and Eq.1.9) in two variables and so they can construct a 2 by 2 linear system[2], whose matrix formulation is the following one.

$$
\boldsymbol{M}\boldsymbol{x} = \boldsymbol{b} \tag{1.10}
$$

In which we define the matrix $\boldsymbol{M}$ and the constant term vector b as follow

$$
\boldsymbol{M} := \begin{bmatrix} \left(1 + R_\mathrm{x} G_\mathrm{fin}\right) & \dfrac{R_\mathrm{x}}{R_\mathrm{f}} \\ A_\mathrm{v} - \dfrac{R_\mathrm{o}}{R_\mathrm{f}} & -\left(1 + R_\mathrm{o} G_\mathrm{fL}\right) \end{bmatrix} \tag{1.11}
$$

$$
\boldsymbol{b} := \begin{pmatrix} -v_\mathrm{s} \\ 0 \end{pmatrix} \tag{1.12}
$$

The matrix resulting from this analysis looks pretty symmetric in its construction and at this point can be useful analyse this system, before solving it, in order to prove that, by making some common approximation, the usual inverting characteristic gain can be found.

To this aim, let's consider the following approximations:

[2]Theoretically this system definition is not correct, because the circuit will most likely introduce some distortion, hence exhibiting a non-linear behaviour. Indeed a non-linear system can not be investigated through a linear system, but the equation above are correct. The swerve is in the model we introduce for the op-amp: in this equivalent circuit the op-amp parameters does not show any limitation from the power supply or the *common mode voltage*. In other words, this equivalent circuit holds only for an op-amp working in linear conditions. The introduction of the non linearity will be taken into account at a later stage.

- $A_\mathrm{v} \to \infty$: the internal open loop gain is infinite.
- $R_\mathrm{in} \to \infty$: the input resistance is infinite in the ideal op-amp.
- $R_\mathrm{o} \to 0$: the output resistance of the ideal op-amp is null.

Keep aside, for now the first approximation on the open loop gain of the amplifier, consider just the second and third. This widely used approximations are strictly related one to the other from a circuital point of view and these also imply that v_d, differential input voltage, is vanishing.

Let's apply this simplifications onto the matrix $\boldsymbol{M}$ entries expressions: once the new entries have been derived making use of limits, the following matrix is obtained.

$$\boldsymbol{M'} := \begin{bmatrix} -\left(1 + \dfrac{R_\mathrm{x}}{R_\mathrm{f}}\right) & \dfrac{R_\mathrm{x}}{R_\mathrm{f}} \\ A_\mathrm{v} & -1 \end{bmatrix} \tag{1.13}$$

Since the constant term vector $\mathbf{b}$ remains untouched during this procedure, the classical inverting op-amp solution can be derived by solving the new approximated system $\boldsymbol{x} = \boldsymbol{M'}/\boldsymbol{b}$. From the second line of the matrix, the relation $v_\mathrm{d} = v_\mathrm{L}/A_\mathrm{v}$ is easily obtainable and substituted into the first line. Consider now the approximation on the open loop gain, $A_v \to \infty$, so that the following equation can be written.

$$\underbrace{\frac{\left(1 + \dfrac{R_\mathrm{x}}{R_\mathrm{f}}\right)}{A_\mathrm{v}} v_\mathrm{L}}_{\approx\, 0} + \frac{R_\mathrm{x}}{R_\mathrm{f}} v_\mathrm{L} = -v_\mathrm{s}$$

$$v_\mathrm{L} = -\frac{R_\mathrm{f}}{R_\mathrm{x}} v_\mathrm{s} \tag{1.14}$$

The Eq.1.14 is the well known inverting amplifier relation, so the ideal case is an approximation of the more general one discussed here. Still relying on the simplification of the ideal case it is useful to already derive the quantities related to the potentiometer.

Exploiting the KVL with the input, feedback and output voltage drop we can obtain the following equations.

$$\underbrace{\cancelto{0}{-v_\mathrm{d}}}_{ideal\ case} + v_\mathrm{f} - v_\mathrm{L} = 0 \tag{1.15}$$

$$v_\mathrm{f} = v_\mathrm{L}$$

$$v_\mathrm{f} = -\frac{R_\mathrm{f}}{R_\mathrm{x}} v_\mathrm{s} = -\frac{R_\mathrm{min} + R_\mathrm{pot}}{R_\mathrm{x}} v_\mathrm{s} \tag{1.16}$$

From Eq.1.16 it is obvious that if the R_{pot} increases also the voltage across the feedback increases (mimicking the output voltage). But this voltage is not the one across the potentiometer, because the v_{f} drop includes also the one across R_{min}. To better understand this point, the current through the feedback is found. Since R_{min} and R_{pot} are in series, this current is equal both for R_{min} and R_{pot}; so making use of Eq.1.16.

$$i_{\mathrm{pot}} = \frac{v_{\mathrm{f}}}{R_{\mathrm{f}}} = -\frac{\cancel{R_{\mathrm{min}} + R_{\mathrm{pot}}}}{R_{\mathrm{x}}\cancel{(R_{\mathrm{min}} + R_{\mathrm{pot}})}} v_{\mathrm{s}} = -\frac{v_{\mathrm{s}}}{R_{\mathrm{x}}} \tag{1.17}$$

So the Ohm's law can be used to express the voltage drop across the potentiometer resistance.

$$v_{\mathrm{pot}} = R_{\mathrm{pot}} i_{\mathrm{pot}} = -\frac{R_{\mathrm{pot}}}{R_{\mathrm{x}}} v_{\mathrm{s}} \tag{1.18}$$

Consequently, the dissipated power expression for the potentiometer comes straightforward.

$$\begin{aligned} p_{\mathrm{pot}} = v_{\mathrm{pot}}^{\mathrm{RMS}} i_{\mathrm{pot}}^{\mathrm{RMS}} &= \left(-\frac{R_{\mathrm{pot}}}{R_{\mathrm{x}}} v_{\mathrm{s}}^{\mathrm{RMS}}\right)\left(-\frac{v_{\mathrm{s}}^{\mathrm{RMS}}}{R_{\mathrm{x}}}\right) = \\ &= \left(\frac{v_{\mathrm{s}}^{\mathrm{RMS}}}{R_{\mathrm{x}}}\right)^2 R_{\mathrm{pot}} \end{aligned} \tag{1.19}$$

This is a linear relation in terms of the potentiometer resistance, but, as shown in the following, this relation is quite different from the more accurate one, even if under certain condition, it can provide good approximations.

Naturally, following the same steps, without simplification, it is possible to find an expression of $v_{\mathrm{L}}(v_{\mathrm{s}})$, which is more complicated but also more precise. The following derivation is still valid, anyway, only in the linear region of operation. So from the second row of the system (defined by the matrix $\boldsymbol{M}$) we can write the following expression of $v_{\mathrm{d}}(v_{\mathrm{L}})$.

$$v_{\mathrm{d}} = \frac{1 + R_{\mathrm{o}} G_{\mathrm{fL}}}{A_{\mathrm{v}} - \dfrac{R_{\mathrm{o}}}{R_{\mathrm{f}}}}(v_{\mathrm{L}}) \tag{1.20}$$

Substituting this expression in the first row of the system, a final expression for

v_L is found.

$$\frac{\Big[1+R_\mathrm{x}G_\mathrm{fin}\Big]\Big[1+R_\mathrm{o}G_\mathrm{fL}\Big]}{A_\mathrm{v}-\dfrac{R_\mathrm{o}}{R_\mathrm{f}}}v_\mathrm{L}+\frac{R_\mathrm{x}}{R_\mathrm{f}}v_\mathrm{L}=-v_\mathrm{s}$$

$$\frac{R_\mathrm{f}\Big[1+R_\mathrm{x}G_\mathrm{fin}+R_\mathrm{o}G_\mathrm{fL}+R_\mathrm{o}R_\mathrm{x}G_\mathrm{fin}G_\mathrm{fL}\Big]+R_\mathrm{x}\Big[A_\mathrm{v}-\dfrac{R_\mathrm{o}}{R_\mathrm{f}}\Big]}{R_\mathrm{f}\left(A_\mathrm{v}-\dfrac{R_\mathrm{o}}{R_\mathrm{f}}\right)}v_\mathrm{L}=-v_\mathrm{s} \tag{1.21}$$

From which the output voltage is expressed as function of the input voltage, defining an equivalent open loop gain for the op-amp: $A'_\mathrm{v}=A_\mathrm{v}-R_\mathrm{o}/R_\mathrm{f}$.

$$v_\mathrm{L}=-\frac{R_\mathrm{f}A'_\mathrm{v}}{R_\mathrm{x}A'_\mathrm{v}+R_\mathrm{f}\Big[1+R_\mathrm{x}G_\mathrm{fin}+R_\mathrm{o}G_\mathrm{fL}+R_\mathrm{o}R_\mathrm{x}G_\mathrm{fin}G_\mathrm{fL}\Big]}v_\mathrm{s}$$

$$v_\mathrm{L}=-\frac{R_\mathrm{f}}{R_\mathrm{x}+R_\mathrm{f}\dfrac{\Big[1+R_\mathrm{x}G_\mathrm{fin}+R_\mathrm{o}G_\mathrm{fL}+R_\mathrm{o}R_\mathrm{x}G_\mathrm{fin}G_\mathrm{fL}\Big]}{A'}}v_\mathrm{s} \tag{1.22}$$

$$=-\frac{R_\mathrm{f}}{R_\mathrm{x}+\dfrac{\epsilon}{A'_\mathrm{v}}}v_\mathrm{s}\quad\text{where} \tag{1.23}$$

$$\epsilon=R_\mathrm{f}\Big[1+R_\mathrm{x}G_\mathrm{fin}+R_\mathrm{o}G_\mathrm{fL}+R_\mathrm{o}R_\mathrm{x}G_\mathrm{fin}G_\mathrm{fL}\Big] \tag{1.24}$$

In Eq.1.22, the expression that multiplies the input signal is the one for the overall gain, in which the equivalent open loop gain has been recollected both from denominator and numerator. This make visible again the fact that if we consider the limit of the expression for $A_\mathrm{v}\to\infty$, so that also $A'_\mathrm{v}\to\infty$, the gain collapses into the ideal inverting op-amp amplifier one.

To derive the potentiometer expressions also in this more accurate framework the initial KVL is the same of the ideal case (Eq.1.15) with the only difference that, now, the v_d term is not null but is given by the expression of Eq.1.20.

$$-v_\mathrm{d}+v_\mathrm{f}-v_\mathrm{L}=0 \tag{1.25}$$

Substituting in the latter expression Eq.1.22, a complicated formulation for i_f can finally be found in the form of a rational function on the independent variable

R_f. Since $i_\mathrm{pot} = i_\mathrm{f}$, the potentiometer current can be found with the translation $R_\mathrm{f} = R_\mathrm{pot} + R_\mathrm{min}$.

$$i_\mathrm{pot}^\mathrm{real}(R_\mathrm{f}) = \frac{\dfrac{R_\mathrm{o}}{A'_\mathrm{v}} + \left(1 - \dfrac{\theta_{2\mathrm{n}}}{A'_\mathrm{v}}\right) R_\mathrm{f}}{\dfrac{\theta_{2\mathrm{d}}}{A'_\mathrm{v}} + \left(\dfrac{\theta_{1\mathrm{d}}}{A'_\mathrm{v}} + R_\mathrm{x}\right) R_\mathrm{f} + \dfrac{\theta_{0\mathrm{d}}}{A'_\mathrm{v}} R_\mathrm{f}^2} v_\mathrm{s} \tag{1.26}$$

In the latter expression, the following definitions have been introduced in order to keep the expression tight:

$$\theta_{2\mathrm{n}} = 1 + \frac{R_\mathrm{o}}{R_L}$$

$$\theta_{2\mathrm{d}} = R_\mathrm{o} R_\mathrm{x}$$

$$\theta_{1\mathrm{d}} = R_\mathrm{o} R_\mathrm{x} \left(\frac{1}{R_\mathrm{L}} + \frac{1}{R_\mathrm{in}}\right) + R_\mathrm{o} + R_\mathrm{x}$$

$$\theta_{1\mathrm{d}} = 1 + \frac{R_\mathrm{o}}{R_\mathrm{L}} + \frac{R_\mathrm{x}}{R_\mathrm{in}} + \frac{R_\mathrm{o} R_\mathrm{x}}{R_\mathrm{L} R_\mathrm{in}}$$

The expression for v_pot is obtained again by multiplying the i_pot current and the potentiometer resistance. This means that the polynomial at the numerator of Eq.1.26 raises its order by one unit. Consequently the power dissipated by the potentiometer is an even more complicated rational function with a polynomial of the third order at the numerator and a polynomial of the fourth order at the denominator.

Observing Eq.1.26, notice that the limit of this current, when the open loop gain is approaching infinite, is the ideal one found in Eq.1.17, as expected.

On the contrary, with respect to what usually happens, the study of these functions is not so useful. To justify that, consider the limits of the previous functions are not supported by any physical counterpart, since no saturation effects are taken into account, and for larger values of gain the amplifier will most-likely enter the saturation region. This topic will be developed in the following, because it is fundamental to consider those non-linearities in order to evaluate the electrical quantities related to the analog potentiometer.

To proceed in the discussion it is now evident the need of a comparison between the results obtained by considering an ideal circuit or a more realistic one. An error evaluation can prove that, depending on the values of the element of the circuit, it is not mandatory to consider a complete model, but that an ideal one can be sufficient. Evaluating some reasonable values for the op-amp parameters and for

the circuit elements[3] is possible to estimate the error committed by considering, in the successive calculations, the ideal op-amp model with respect to the more precise one just exploited above. The results is a very small error principally due to the fact that the open loop gain of the op-amp is much larger than the terms between square bracket in Eq.1.22, renamed ϵ as in Eq.1.24 for sake of clearness.

The error, evaluated as follow, is showing that, for the calculation in the following, it is usually sufficient to consider the ideal expressions. Clearly the worse the performance of the op-amp are, the more important the differences between the two results become. Since the potentiometer ideal current depends only on R_{x} and v_{s}, the trend of the error varying R_{pot} is the same as the real current (fractional function).

$$\delta_{\mathrm{i}}(R_{\mathrm{f}}) = \frac{i_{\mathrm{pot}}^{\mathrm{real}}}{i_{\mathrm{pot}}} = \frac{R_{\mathrm{x}}\dfrac{R_{\mathrm{o}}}{A'_{\mathrm{v}}} + R_{\mathrm{x}}\left(1 - \dfrac{\theta_{2\mathrm{n}}}{A'_{\mathrm{v}}}\right)R_{\mathrm{f}}}{\dfrac{\theta_{2\mathrm{d}}}{A'_{\mathrm{v}}} + \left(\dfrac{\theta_{1\mathrm{d}}}{A'_{\mathrm{v}}} + R_{\mathrm{x}}\right)R_{\mathrm{f}} + \dfrac{\theta_{0\mathrm{d}}}{A'_{\mathrm{v}}}R_{\mathrm{f}}^2} \tag{1.27}$$

Clearly, since the v_{pot} and the p_{pot} expressions are obtained through a multiplication which is the same for both the ideal and real cases, so the errors are exactly the same.

$$\frac{i_{\mathrm{pot}}^{\mathrm{real}}}{i_{\mathrm{pot}}} = \delta_{\mathrm{i}} = \frac{v_{\mathrm{pot}}^{\mathrm{real}}}{v_{\mathrm{pot}}} = \delta_{\mathrm{v}} = \frac{p_{\mathrm{pot}}^{\mathrm{real}}}{p_{\mathrm{pot}}} = \delta_{\mathrm{p}} \tag{1.28}$$

Looking at Figure 1.2 it is evident that the error increases with the potentiometer resistance in a more than linear way. it is convenient to plot the curves against the real gain value (as done in Figure 1.3), since the gain (at least at this point of the discussion) is the relevant quantity from the user point of view. This trend is almost linear, with a less than linear region for low values of gain which corresponds to the almost flat region in Figure 1.2. The important consideration in this discussion is that even considering an high ideal gain (greater than 100 times) and so an high R_{pot} resistance, the error remains well below 0.1%, for all the fundamental potentiometer electrical quantities . Finally, if the ideal expressions are considered to calculate the current through, the voltage across and the power dissipated by the potentiometer, the calculation will be much simpler without compromising the results.

The discussion carried on till now holds in linear conditions, which is not guaranteed *a priori* in any of the common amplifier circuit. So it is crucial to

[3]In order to estimate the errors and to obtain results comparable with the real devices the following suggested values have been used: $A_{\mathrm{v}} = 80\,\mathrm{dB}$, $R_{\mathrm{o}} = 500\,\Omega$, $R_{\mathrm{in}} = 10\,\mathrm{M}\Omega$, $R_{\mathrm{x}} = 1\,\mathrm{k}\Omega$, $R_{\mathrm{f}} = R_{min} + R_{pot}$ in which $R_{\mathrm{min}} = 1\,\mathrm{k}\Omega$ and $R_{pot} \in [0\,\mathrm{k}\Omega, 100\,\mathrm{k}\Omega]$, $R_{\mathrm{L}} = 50\,\mathrm{k}\Omega$

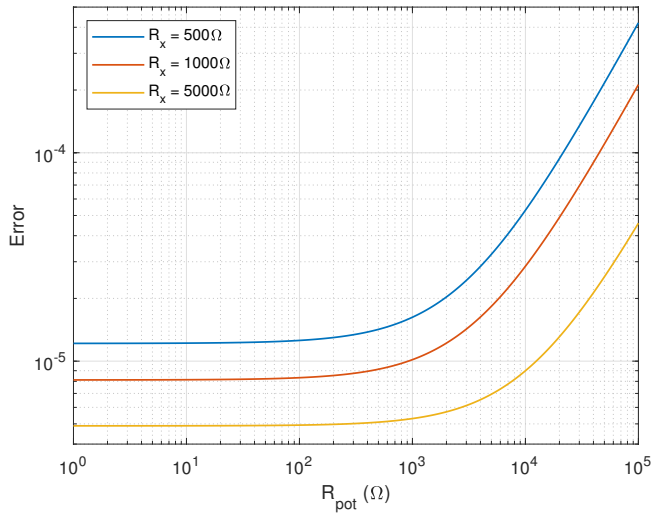


Figure 1.2: Plot of the error computed by considering the real op-amp model or the ideal one, versus the potentiometer value. Curve traced for three different values of R_{x}, so for three different ranges of gain ($R_{\mathrm{pot}} \in (0, 100\,\mathrm{k}\Omega]$).

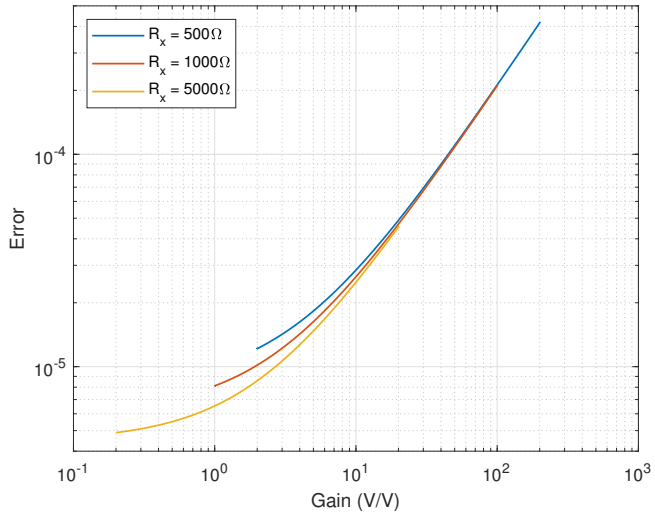


Figure 1.3: Plot of the error computed by considering the real op-amp model or the ideal one, versus the gain (real) of the circuit. Curve traced for three different values of R_{x}, so for three different ranges of gain ($R_{\mathrm{pot}} \in [0, 100\,\mathrm{k}\Omega]$).

include the effect of non-linearity into the calculation. The distortion is introduced by the op-amp, since, in some specific conditions, the active devices (namely integrated transistor) that constitute the operational amplifier itself, are driven out

of the usual operating region. Because the transistor are intrinsically non-linear devices (quadratic or exponential referring to MOS or BJT respectively), naturally the op-amp circuit has a non linear behaviour too.

Typically the mechanisms that bring the op-amp into saturation are not easy to model mathematically, since they rely on many different parameters of the internal integrated circuit. In the previous discussion we introduced a model in which the internal circuit of the op-amp is modelled introducing a circuit based on two networks: an input one (that models the input of the op-amp, namely the R_{in} resistance between the inputs) and an output one (the non-ideal generator). This procedure has the advantage of masking the complex networks present in the integrated circuit, in particular the relations between the output voltage and the power supply. Moreover, this approach can still be applied, just introducing some modification, in the saturation region of operation.

So it is possible to assume, for instance, that if the output voltage hits certain specific voltages (positive V_{OH} or negative V_{OL}), it will be clamped at these values until the input signal will return into a range for which the output voltage decreases into the available range. Usually, for bipolar op-amp, $V_{\mathrm{OH}} < V_{\mathrm{CC}}$ by a quantity which is the sum of typically two diode forward voltage drop (same for $V_{\mathrm{OL}} > V_{\mathrm{EE}}$)[4]:

$$v_{\mathrm{L}} \in [-V_{\mathrm{OH}}, V_{\mathrm{OL}}] \tag{1.29}$$

When saturation occurs, the op-amp is no more able to control v_{d} accordingly to v_{L} and the basic assumption, previously discussed, used to solved the op-amp circuit, $v_{\mathrm{d}} \approx 0$ is completely lost [1]. When the op-amp is in saturation the output behaves as a voltage source and this fact can be exploited to re-design the circuit in Figure 1.1 in saturation condition, as follow.

The solution of this circuit is straightforward by applying the *Millman's theorem* to the input node. This is made possible by recalling the definition $R_{\mathrm{f}} = R_{\mathrm{min}} + R_{\mathrm{pot}}$ and the fact that the load is in parallel with a voltage source (so it does not appear in this calculation).

$$-v_{\mathrm{d}} = \frac{\dfrac{V_{\mathrm{OH}}}{R_{\mathrm{f}}} + \dfrac{v_{\mathrm{s}}}{R_{\mathrm{x}}}}{\dfrac{1}{R_{\mathrm{f}}} + \dfrac{1}{R_{\mathrm{in}}} + \dfrac{1}{R_{\mathrm{x}}}} \tag{1.30}$$

[4]To avoid the limiting introduced by the power supply levels, further reduced by a consistent quantity (for LM741 this is around 2 V [2]), a common optimisation is the use of rail to rail op-amp. Also the values at which the output voltage is clamped depend on the output impedance of the amplifier and the saturation voltage of the output transistor of the final stage [3]. Here, the discussion is kept above these details and a simple limitation, lower than the supply swing, is consider for simplicity.

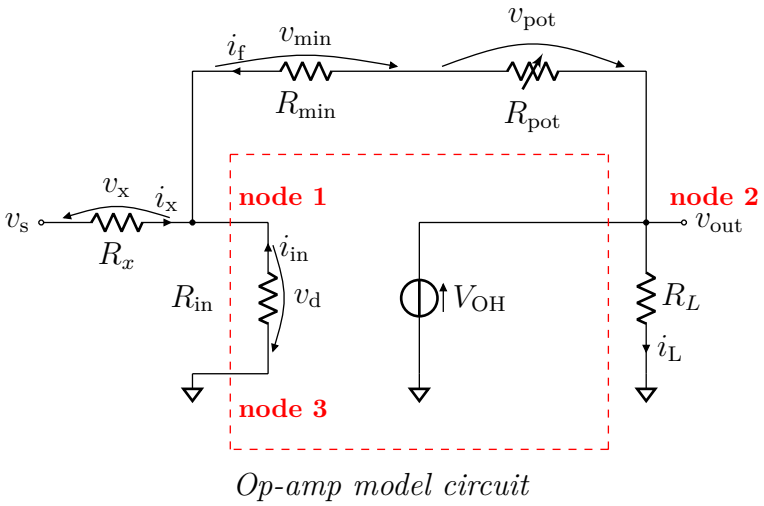


Figure 1.4: Basic op-amp based inverting amplifier circuit in positive saturation condition.

The Eq.1.30 can be re-written as it shows in Eq.1.32 by defining a new conductance, in the same way of Eq.1.4 and Eq.1.5.

$$G_{\text{finx}} = G_{\text{fin}} + \frac{1}{R_{\text{x}}} = \frac{1}{R_{\text{in}}} + \frac{1}{R_{\text{f}}} + \frac{1}{R_{\text{L}}} \tag{1.31}$$

$$v_{\text{d}} = -\frac{V_{\text{OH}}}{R_{\text{f}} G_{\text{finx}}} - \frac{v_{\text{s}}}{R_{\text{x}} G_{\text{finx}}} \tag{1.32}$$

This equation is sufficient to draw the complete output voltage curve, the final v_{d} voltage and all the potentiometer quantities for the inverting configuration.

$$i_{\text{pot}}^{\text{sat}} = \frac{v_{\text{f}}^{\text{sat}}}{R_{\text{f}}} = \frac{V_{\text{OH}} + v_{\text{d}}}{R_{\text{f}}} = V_{\text{OH}} \left(\frac{1}{R_{\text{f}}} - \frac{1}{R_{\text{f}}^2 G_{\text{finx}}} \right) - \frac{v_{\text{s}}}{R_{\text{f}} R_{\text{x}} G_{\text{finx}}} \tag{1.33}$$

As before, the voltage is simply obtained by multiplying the current for the potentiometer resistance and for the square of the resistance in order to obtain the dissipated power. All the results obtained are plotted in the graph below.

In Figure 1.5 the solid lines are drawn for $R_{\text{pot}} = 3140\,\Omega$ that is a value of resistance for which the circuit works in linearity. The dotted lines, for $R_{\text{pot}} = 9954\,\text{k}\Omega$, for which the op-amp is driven out of linearity. When linearity holds, the output follows the input voltage and, due to the extremely high open loop gain, the input differential voltage is very small (hundreds of microvolt). Notice that when saturation occurs, the output voltage is kept constant at V_{OL} or V_{OH} while, since

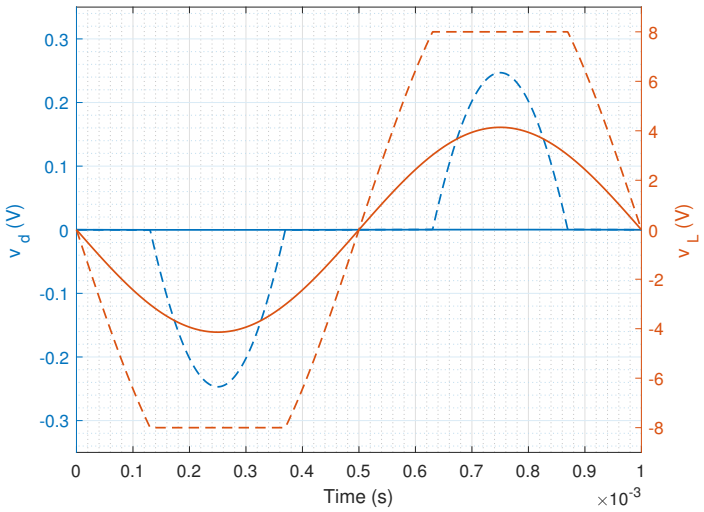


Figure 1.5: Inverting op-amp amplifier output voltage and input differential voltage, for a sinusoidal input signal of amplitude 1 V, for two different values of gain (for $R_{\text{pot}} = 3140\,\Omega$ (blue) and $R_{\text{pot}} = 9954\,\Omega$ (red)).

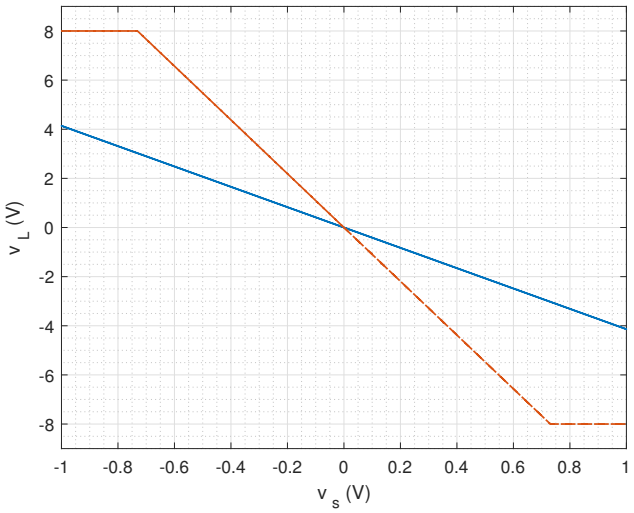


Figure 1.6: Inverting op-amp amplifier input-output characteristic. The two traces are plotted for the same R_{pot} values of the previous graph (Figure 1.5)

the input differential voltage and output voltage are no more related as before, now v_{d} is free to vary, following v_{s}.

Figure 1.6 present the transfer characteristic of the inverting amplifier circuit. it is evident that, for lower resistance of the potentiometer, the characteristic is a

straight line whose slope, *i.e.* the gain, is constant, while for large values of R_{pot} saturation occurs and the characteristic flattens. The higher the gain, the faster the circuit exits linearity and the characteristic looks vertical around 0 V input.

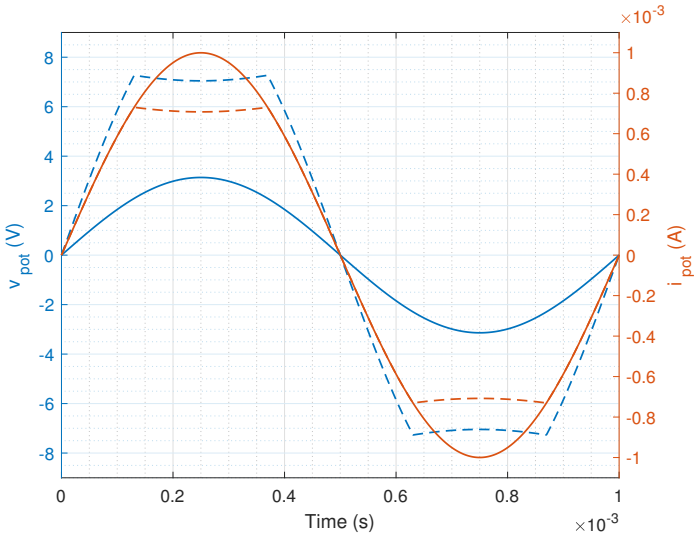


Figure 1.7: Current and voltage of the potentiometer, both in linearity and saturation condition. Dotted traces refer to a saturation condition, while the continuos ones refer to a linear condition (the two values of R_{pot} for which the graph is plotted are the same of Figure 1.5).

With Figure 1.7 the potentiometer quantities are introduced. Here are reported the voltage and the current, superimposed, both in linear and in saturation conditions. As before the dotted lines are referred to the saturation condition, and it is possible to notice how the clipping condition is not reflected from the output voltage in to the potentiometer voltage, due to the fact that the differential voltage, in saturation, is no more negligible, and it contributes consistently in the related mesh (Eq.1.25).

In Figure 1.8 the instant power dissipated by the potentiometer, calculated as the product between the voltage and the current is reported. As expected, for a sinusoidal (periodical) input, the power function exhibits a double frequency periodicity and this holds also in saturation. As a consequence of the distortion in both current and voltage of the potentiometer, also the power curve is affected by distortion when the op-amp is driven out of linearity. In any case, for normal values of the component of the circuit, the amount of power dissipated by the potentiometer is fairly low[5]: below 10 mW.

it is useful to also plot the maximum value (peak value) of voltage across the

[5]Referring to standard lumped element circuit.

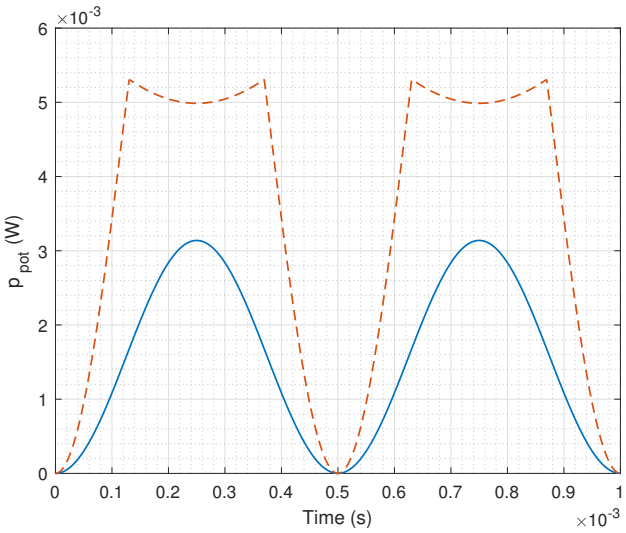


Figure 1.8: Power dissipated by the potentiometer, both in linearity and saturation condition (same values for R_{pot} of Figure 1.5, the dotted line refers to the saturation condition, the solid one refers to the linear condition).

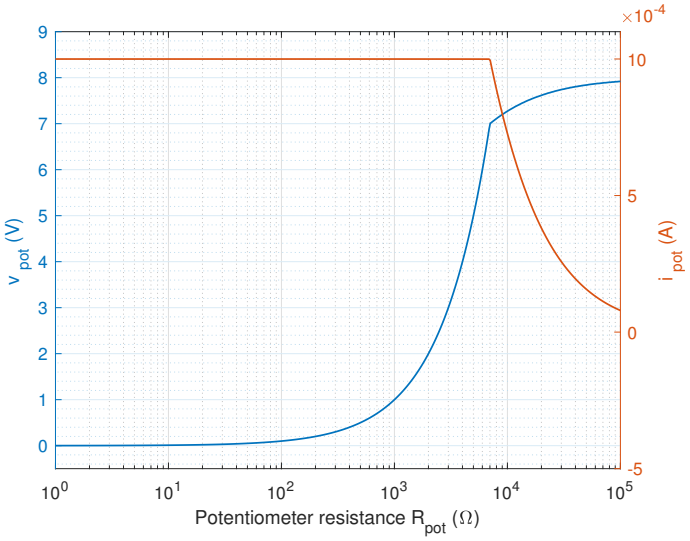


Figure 1.9: Maximum values of voltage and current for the potentiometer drawn against the potentiometer value.

potentiometer along one period of the wave, for each value of the potentiometer resistance. From a design prospective consider that the swing handled by R_{pot} is twice the peak value. When linearity holds, the potentiometer peak voltage increases linearly (Figure 1.9), while the current peak is kept constant. This also

means that the power in this region increases with the resistance in a linear way. In fact, looking at Figure 1.10, which is a double logarithmic plot, this part of the power graph looks like a straight line. After saturation region is entered the peak current drops faster than how the voltage increases, so the power decreases too, almost linearly.

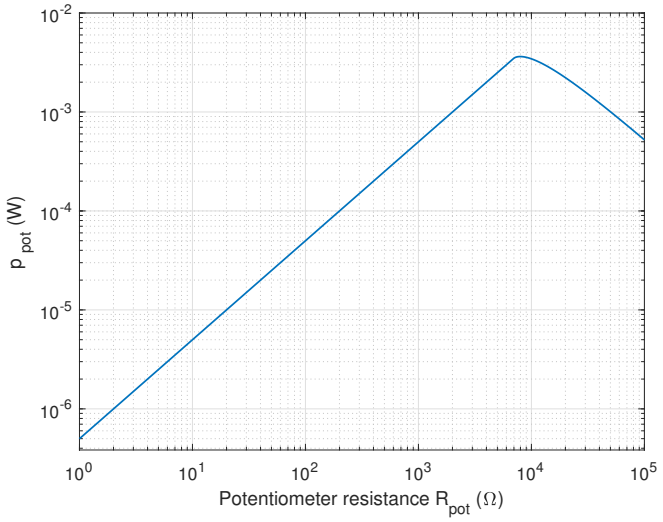


Figure 1.10: Power dissipated by the potentiometer versus the potentiometer value.

The power plotted in (Figure 1.9) is calculated as follow. Since the power for a resistor under periodic regime is given by Eq.1.34, the substitution is straightforward; thank to the fact that the potentiometer resistance is assumed to be constant during each gain's step.

$$\begin{aligned} p_{\text{pot}} &= R_{\text{pot}} \left[i_{\text{pot}}^{\text{RMS}} \right]^2 = \\ &= R_{\text{pot}} \frac{1}{T} \int_0^T i_{\text{pot}}^2(t) dt = \\ &= R_{\text{pot}} \frac{2}{T} \int_0^{T/2} i_{\text{pot}}^2(t) dt \end{aligned} \tag{1.34}$$

Non-inverting op-amp amplifier

The procedure exploited to study the non-inverting topology is in every aspect similar to the one carried on for the inverting circuit. Clearly the electrical connections of some components have been modified and so the equation are not the same (so as the results), but their structure is similar. In this section as well,

the analysis does not involve any frequency dependence or reactive effect, although the signal considered is time variant.

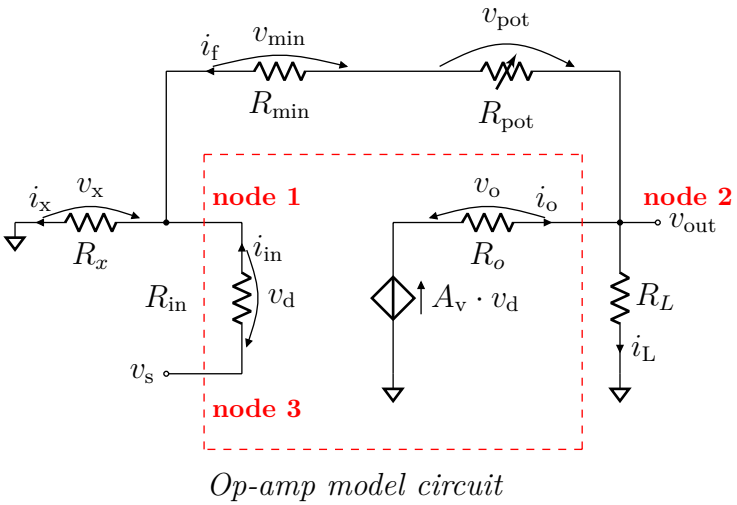


Figure 1.11: Basic op-amp based non-inverting amplifier circuit.

The circuit in Figure 1.11 is a topology in which the input signal is injected into the non inverting input of the amplifier and the gain is controlled (ideally) by the feedback resistor $R_f = R_{pot} + R_{min}$ and the inverting input resistor R_x connected to ground. As done before, it can be analysed by considering two meshes (KVL) and a few other straightforward equation, so that a two by two linear system, analogous to the inverting topology one, can be written and solved for v_d and v_L. As already seen for the inverting topology, linearity is assumed to begin with, and saturation effects will be taken into account later. Consider the input and output mesh as the two fundamental KVL equations to write the system.

$$\begin{cases} v_s - v_d - v_x = 0 \\ A_v v_d - v_o - v_L = 0 \end{cases}$$

The two voltages v_x and v_o can be re-written in terms of the unknown v_d and v_L and the input voltage v_s by exploiting the two KCL below (at node 1, Eq.1.35 and 2, Eq.1.36 respectively) and the overall feedback mesh involving v_f (Eq.1.37).

$$i_x = i_{in} + i_f = \frac{v_d}{R_{in}} + \frac{v_f}{R_f} \tag{1.35}$$

$$i_o = i_L + i_f = \frac{v_L}{R_L} + \frac{v_f}{R_f} \tag{1.36}$$

$$v_f = v_L + v_d - v_s \tag{1.37}$$

Some algebra leads to the following system of equations, given in the usual matrix form $\mathbf{Mx} = \mathbf{b}$ (where $\mathbf{x}$ is the unknown vector).

$$\boldsymbol{M} := \begin{bmatrix} \left(1 + R_{\mathrm{x}} G_{\mathrm{fin}}\right) & \dfrac{R_{\mathrm{x}}}{R_{\mathrm{f}}} \\ A_{\mathrm{v}} - \dfrac{R_{\mathrm{o}}}{R_{\mathrm{f}}} & -\left(1 + R_{\mathrm{o}} G_{\mathrm{fL}}\right) \end{bmatrix} \tag{1.38}$$

$$\boldsymbol{b} := \begin{bmatrix} \left(1 + \dfrac{R_{\mathrm{x}}}{R_{\mathrm{f}}}\right) \\ -\dfrac{R_{\mathrm{o}}}{R_{\mathrm{f}}} \end{bmatrix} \tag{1.39}$$

The matrix $\boldsymbol{M}$ in Eq.1.38 is equal to the one of the inverting topology previously studied; so the same definitions have been used for what concerns the equivalent open loop gain A'_{v}, and the two conductances G_{fin} and G_{fL} (Eq.1.4 and 1.5). The differences relay on the known vector $\boldsymbol{b}$, in which the second entry is no more null, but, more importantly, in which the first entry shows an opposite sign with respect to the inverting case. This fact is basically what makes the two topologies being complementary for what concerns the phase of the amplified signal.

$$v_{\mathrm{L}} = \frac{(R_{\mathrm{f}} + R_{\mathrm{x}}) + \dfrac{R_{\mathrm{o}}\left(1 + R_{\mathrm{x}} G_{\mathrm{fin}}\right)}{A'_{\mathrm{v}}}}{R_{\mathrm{x}} + \dfrac{R_{\mathrm{f}}\left(1 + R_{\mathrm{x}} G_{\mathrm{fin}}\right)\left(1 + R_{\mathrm{o}} G_{\mathrm{fL}}\right)}{A'_{\mathrm{v}}}} v_{\mathrm{s}}$$

Taking into account the definition of ϵ given in Eq.1.24 the final expression for v_{L} can be re-written as follow.

$$v_{\mathrm{L}} = \frac{(R_{\mathrm{f}} + R_{\mathrm{x}}) + \dfrac{R_{\mathrm{o}}\left(1 + R_{\mathrm{x}} G_{\mathrm{fin}}\right)}{A'_{\mathrm{v}}}}{R_{\mathrm{x}} + \dfrac{\epsilon}{A'_{\mathrm{v}}}} v_{\mathrm{s}} \tag{1.40}$$

Eq.1.40 can be easily approximated for $A_{\mathrm{v}} \to \infty$, in order to obtain the well known ideal case for the non-inverting amplifier. Since $A_{\mathrm{v}} \to \infty$ implies $A'_{\mathrm{v}} \to \infty$ the approximated expression results as follow.

$$v_{\mathrm{L}} = \left(1 + \frac{R_{\mathrm{f}}}{R_{\mathrm{x}}}\right) v_{\mathrm{s}} \tag{1.41}$$

As done for the inverting amplifier, consider the approximated equation to come up with some manageable expression for the potentiometer quantities. Clearly the

infinite open loop gain condition leads also to the nullification of the differential voltage.

$$i_{\text{pot}} = \frac{v_{\text{f}}}{R_{\text{f}}} = \frac{v_{\text{L}} - v_{\text{s}}}{R_{\text{f}}} = \\ = \left(1 + \frac{R_{\text{f}}}{R_{\text{x}}}\right) v_{\text{s}} - v_{\text{s}} = \frac{v_{\text{s}}}{R_{\text{x}}} \tag{1.42}$$

This is the same expression obtained for the inverting topology with the opposite sign, so both voltage and current of the potentiometer are the same in absolute value for inverting and non-inverting configuration.

$$v_{\text{pot}} = \frac{R_{\text{pot}}}{R_{\text{x}}} v_{\text{s}} \tag{1.43}$$

$$p_{\text{pot}} = i_{\text{pot}}^{\text{RMS}} v_{\text{pot}}^{\text{RMS}} = \left(\frac{v_{\text{s}}^{\text{RMS}}}{R_{\text{x}}}\right)^2 R_{\text{pot}} \tag{1.44}$$

Obviously the power dissipation is identical since the product of voltage and current with the same sign will results always in a positive power dissipation.

Introducing saturation into the analysis, in the very same way seen for the inverting topology, leads to the same substitution in the circuit of a fixed voltage generator in place of the voltage controlled one. Again solving this circuit for v_{f}

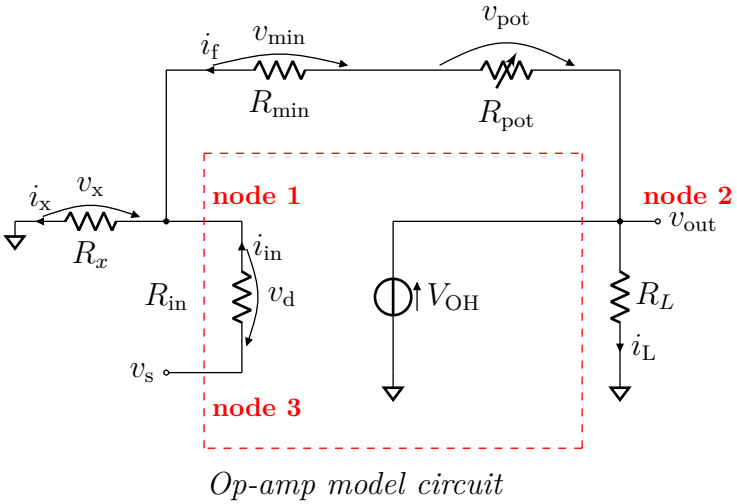


Figure 1.12: Basic op-amp based non-inverting amplifier circuit in positive saturation condition.

is a straightforward procedure since it implies the *Millman theorem* and a simple KVL. Notice that the *Millman theorem* is useful to find the inverting input voltage

with respect to ground (labeled as v_N), then a simple mesh across v_s, v_d and v_N is sufficient to get the result.

$$v_N = \frac{\frac{v_s}{R_{in}} + \frac{V_{OH}}{R_f}}{\frac{1}{R_f} + \frac{1}{R_{in}} + \frac{1}{R_x}} = \frac{v_s}{R_{in}G_{finx}} + \frac{V_{OH}}{R_f G_{finx}} \tag{1.45}$$

Substituting in the mesh it is possible to derive the v_d voltage in positive saturation condition. To obtain the expression for negative saturation condition it is sufficient to substitute the constant voltage V_{OH} with V_{OL}.

$$v_d = v_s - v_N = \left(1 - \frac{1}{R_{in}G_{finx}}\right) v_s - \frac{V_{OH}}{R_f G_{finx}} \tag{1.46}$$

The graph below, Figure 1.13, reports the final solutions for v_L and v_d for two values of gain[6], for which in one case linearity holds and and in the other (dotted trace) saturation is encountered. Notice the similarity with respect to the inverting topology case: in both situations amplification is linear till the V_{OH} or V_{OL} limits are reached by the output voltage. At that point the output of the op-amp is kept constant meanwhile the input differential voltage exceeds its linear, almost negligible, normal level, tracking the input source voltage. It turns out that without considering in any case fundamental properties of the amplifiers, *e.g.* input impedance, the same amplification factor and input-output relation can be obtained from both the topology, except for a phase inversion.

The input-output characteristic, shown in Figure 1.14, makes evident the first difference between the two topologies: the phase inversion. The characteristic in this case shows a positive slope, which leads to positive output voltage for positive input voltage. For what concerns the other properties of this curve, they are completely analogous. The higher the gain, the higher the slope of the linear central region of the characteristic, and saturation occurs in the same way. One difference is that in the inverting topology a minimum resistance, R_{min}, that set the minimum feedback resistance when the potentiometer is set to a null resistance position is mandatory in order to prevent the output voltage to vanish even for input source voltage different from zero (namely avoiding vanishing gain). Depending on applications, a common choice is to set $R_{min} = R_x$, so that at the minimum position for the potentiometer the amplifier works as a buffer. For the non-inverting case, this is not strictly required since if the feedback resistance is taken to be null a common buffer topology is already obtained without any addition. This is clear looking at

[6]The two values of R_{pot} for which the results are plotted are the same of the inverting topology: 3140 Ω and 9954 Ω.

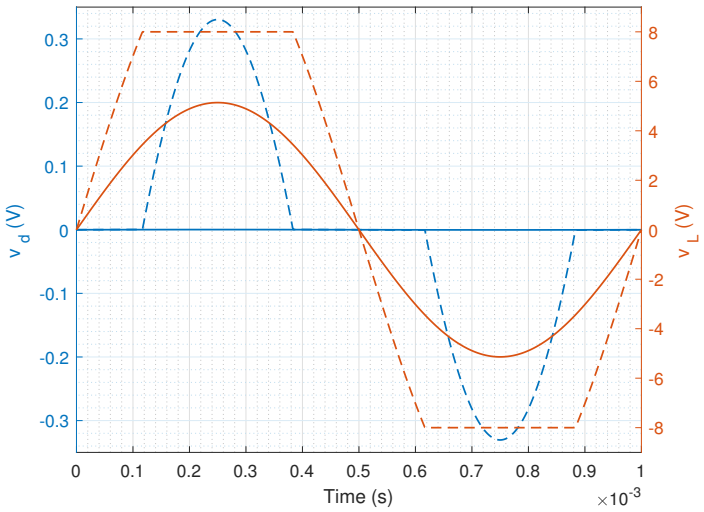


Figure 1.13: Non-inverting op-amp amplifier output voltage and input differential voltage, for a sinusoidal input signal of amplitude 1 V, for two different values of gain (for $R_{\text{pot}} = 3140\,\Omega$ (blue) and $R_{\text{pot}} = 9954\,\Omega$ (red)).

the gain expressions: in Eq.1.23, if $R_\text{f} \to 0$ the output voltage vanishes, while from Eq.1.40 the limits of the gain is one. For the inverting stage the following limits hold.

$$\text{Since} \qquad \lim_{R_\text{f}\to 0} \epsilon \to \infty \qquad \text{so} \qquad \lim_{R_\text{f}\to 0} -\frac{R_\text{f}}{R_\text{x} + \dfrac{\epsilon}{A'_\text{v}}} = 0 \tag{1.47}$$

For what concerns the non-inverting topology.

$$\lim_{R_\text{f}\to 0} \frac{(R_\text{f} + R_\text{x}) + \dfrac{R_\text{o}\,(1 + R_\text{x} G_\text{fin})}{A'_\text{v}}}{R_\text{x} + \dfrac{\epsilon}{A'_\text{v}}} =$$

$$\lim_{R_\text{f}\to 0} \frac{\dfrac{R_\text{o} R_\text{x}}{A'_\text{v}} \dfrac{1}{R_\text{f}}}{\dfrac{\epsilon}{A'_\text{v}}} = \lim_{R_\text{f}\to 0} \frac{R_\text{o} R_\text{x}}{\cancel{A'_\text{v}}} \frac{1}{R_\text{f}} \frac{\cancel{A'_\text{v}}}{\epsilon}$$

Recalling the definition of ϵ it results that the limits of $R_\text{f}\epsilon$ for $R_\text{f} \to 0$ is nothing but $R_\text{o} R_\text{x}$, so that the final result below it is straightforward.

$$\lim_{R_\text{f}\to 0} \frac{(R_\text{f} + R_\text{x}) + \dfrac{R_\text{o}\,(1 + R_\text{x} G_\text{fin})}{A'_\text{v}}}{R_\text{x} + \dfrac{\epsilon}{A'_\text{v}}} = \frac{R_\text{o} R_\text{x}}{R_\text{o} R_\text{x}} = 1 \tag{1.48}$$

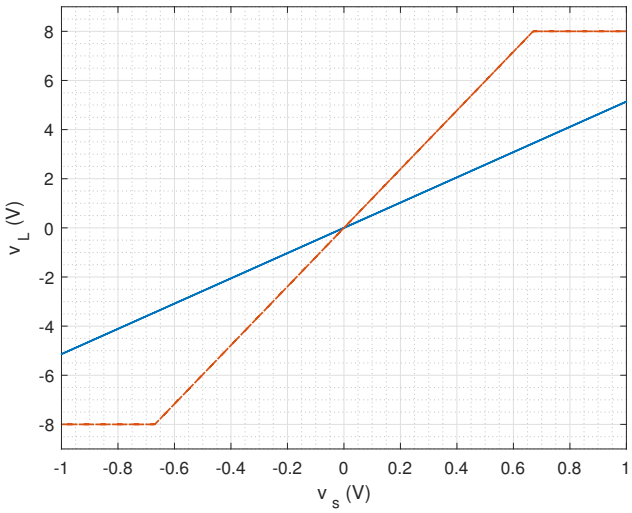


Figure 1.14: Non-inverting op-amp amplifier input-output characteristic. Blue line refers to the linear condition ($R_{\text{pot}} = 3140\,\Omega$) while the red one refers to a saturation condition ($R_{\text{pot}} = 9954\,\Omega$)

For what concerns the potentiometer current and voltage refer to Figure 1.15. Again, the situation is very similar to the one already shown for the inverting topology. In this case also the phase of the voltage is the same as the input source one, this means that it is the same of the inverting topology, since in that case the output voltage and the potentiometer voltage are opposite in phase. As it is noticeable comparing Figure 1.15 and Figure 1.7, the input source voltage has a greater effect on the potentiometer voltage and current in the saturation condition, since in the inverting case the v_{pot} exhibits a deep on the top of the waveform, while for the non-inverting topology, the top of the waveform results (almost) flat. This will have an impact on the dissipated power. The instantaneous dissipated power (Figure 1.16) has peak values similar in the two cases, slightly higher than the ones in Figure 1.8 for the inverting case, but the fact that the voltage has deeps in the inverting case means that the RMS level of voltage and current are lower than in the case of the non-inverting topology. Still, the trend of the curves is the same.

Also for what concerns the peak values of voltage and current, the plot resulting for the non-inverting topology is very similar to the previous homologous one. The difference is in the saturation region, in which the shape of the curves are not equal even if the general phenomenon is the same and so the traces are still close one to the other.

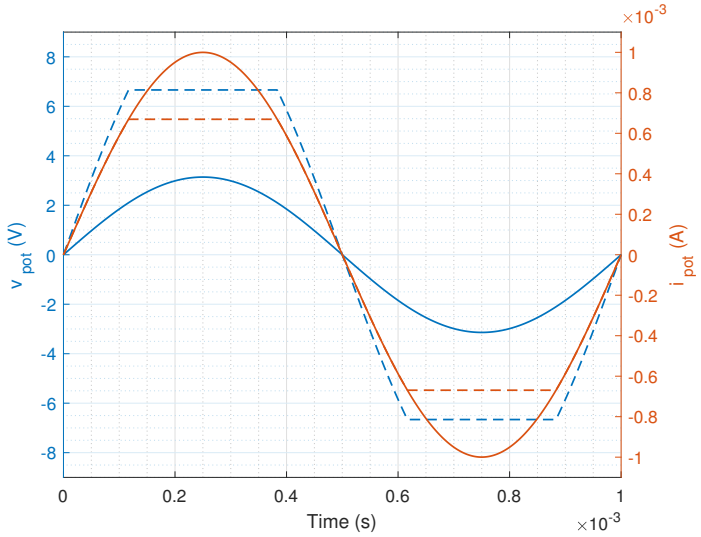


Figure 1.15: Current and voltage of the potentiometer, both in linear (blue) and saturation (red) condition (same values for R_{pot} of Figure 1.13).

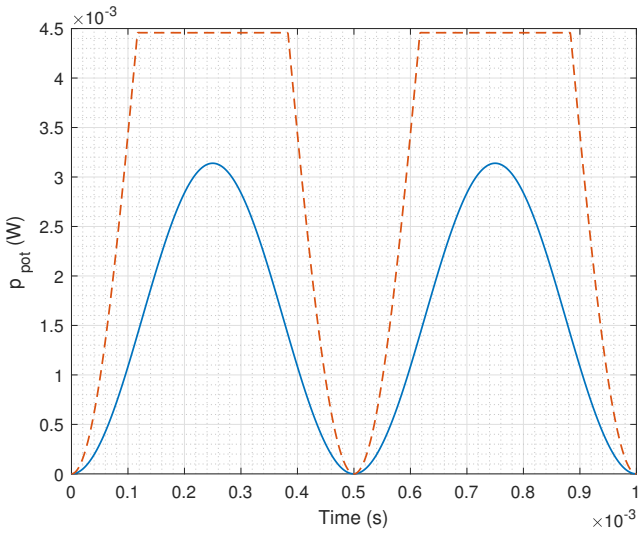


Figure 1.16: Power dissipated by the potentiometer, both in linear (blue) and saturation (red) condition (same values for R_{pot} of Figure 1.13).

Comparison between the inverting and non-inverting topologies

To end up the analysis of this two fundamental stages it worth the report of the peak voltage and current graph and the power dissipated one in a single graph for both inverting and non-inverting topology. This allows a direct comparison of the

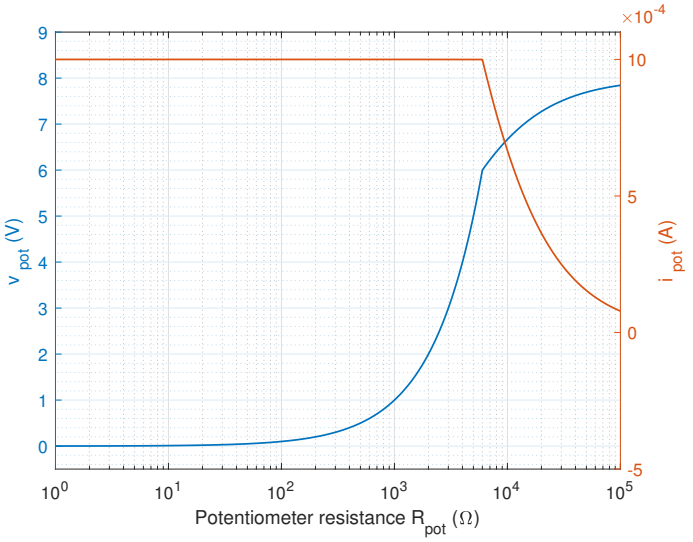


Figure 1.17: Maximum values of voltage and current for the potentiometer drawn against the potentiometer value.

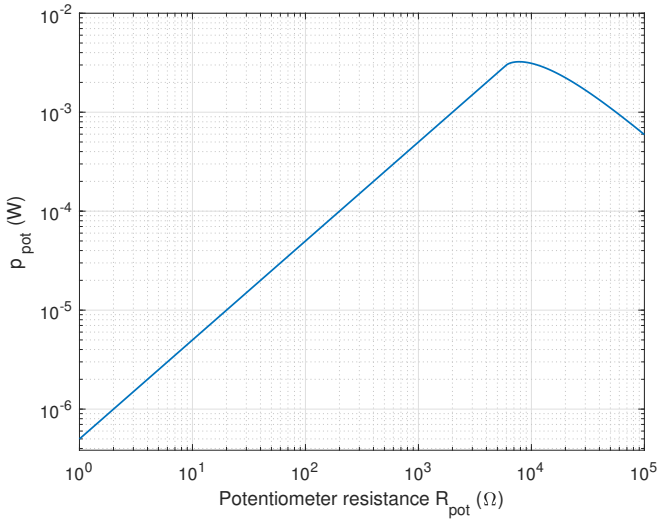


Figure 1.18: Power dissipated by the potentiometer drawn against the potentiometer value.

two situations.

In Figure 1.19, the differences in the way the circuit enters the saturation are evident: the inverting configuration enters saturation for slightly larger values of R_{pot}, due to the different expression of the gain. Also for increasing values of R_{pot}, even deeper in saturation, the potentiometer voltage tend to saturate at the V_{OH} (or V_{OL} depending on the sign of the specific half-wave). So the current will

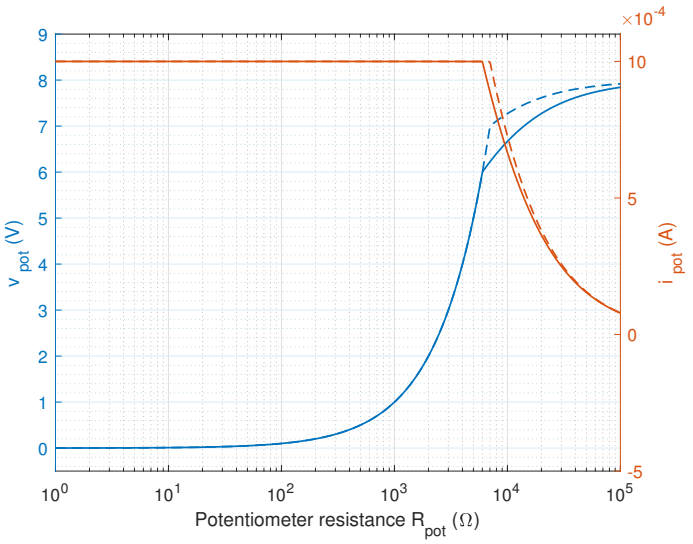


Figure 1.19: Peak values of current and voltage reported against the potentiometer resistance. dotted traces refers to the inverting topology, solid ones for non-inverting circuit.

decrease accordingly (considering the *Ohm's law*), since while the voltage across the potentiometer tends to a constant value, its resistance still increases. The fact that the inverting configuration enters saturation at a later stage results in a less steep curve towards the limiting value, compared to the non-inverting one.

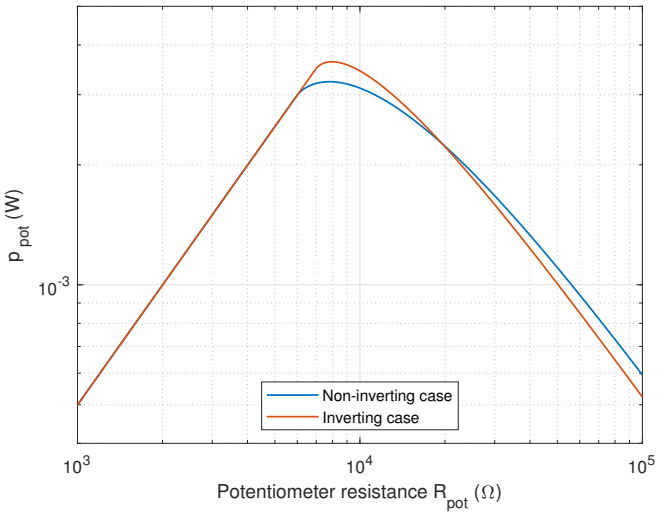


Figure 1.20: Power dissipated by the potentiometer reported against the potentiometer value for the two different topologies. The plot is reported just for the upper portion of the potentiometer range, since below that the two traces have a difference which is negligible.

This differences in the trend of the voltage and current peak values are reflected by the dissipated power (related to the RMS quantities). The two power curves are reported in Figure 1.20.

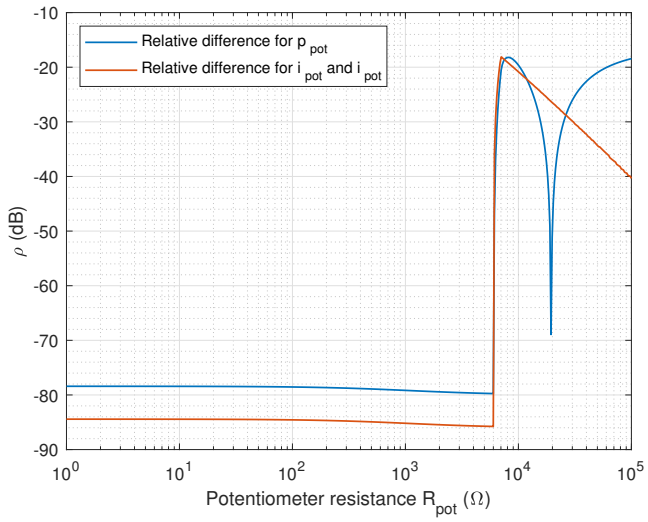


Figure 1.21: Relative difference of inverting e non-inverting topologies, for what concerns the potentiometer voltage and current and dissipated power.

Finally, in Figure 1.21, the relative differences between the two topologies potentiometer dissipated power is reported, with the same quantity related to the peak current and voltage. it is visible how much in linearity the two configurations can be interchangeable in terms of potentiometer stresses and parameters (such as voltage swing at its terminals). The saturation region is entered with an abrupt jump of the difference, since the non-inverting topology will stay in linearity still for a little portion of the potentiometer range. So the two power curves (and the corresponding voltages and currents) splits around that point and, because the inverting power curves drops faster than the non-inverting one, after the peak, there is an intercept point. This results in a "notch" in the relative difference plot.

Instrumentation amplifier

The instrumentation amplifier is a circuit whose aim is to increase some performances of a difference amplifier [1]. The advantage of the simple difference amplifier is its simplicity, beside, its gain performances are poor (≤ 10), so as the CMMR ($\leq 85\,\mathrm{dB}$) and noise performance ($20\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ to $50\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$) [4]. Furthermore, the most important point is that the input impedance of the difference amplifier is relatively low ($\approx 10\,\mathrm{k\Omega}$ to $\approx 100\,\mathrm{k\Omega}$) and this limits its implementation where low impedance source are involved [4]. The difference amplifier is visible on the

right of the red dotted line in Figure 1.22 and it represents the second stage of the instrumentation amplifier.

Considering each input in a single ended way[7], the previous resistance writes with the expressions below [4], in which the common assumptions $R_1^{\text{up}} = R_1^{\text{dwn}}$ and $R_2^{\text{up}} = R_2^{\text{dwn}}$ have been considered.

$$R_{\text{in}}^{\text{dwn}} = \frac{R_2 + R_1}{2} \tag{1.49}$$

$$R_{\text{in}}^{\text{up}} = 2\frac{R_2 + R_1}{2R_2 + R_1} R_1 \tag{1.50}$$

Notice that, to obtain this result, the ideal op-amp approximation as already been assumed.

To improve the difference amplifier topology, the basic circuit (on the right of the red dotted line in Figure 1.22) is preceded by an *input stage* (on the left of the red dotted line in Figure 1.22), which buffers the input signal. The input stage in Figure 1.22 is implemented with two more op-amps, to whom the input signals are connected on the non-inverting input. This means that the input impedance of the amplifier is much larger than before, being the impedance of the op-amp input very high (especially for MOS or JFET solution). In simple difference amplifier (here second stage) this is not true because the inputs are connected to resistor and not directly to op-amp inputs. This property is very important because allows the amplifier to work as expected on the differential mode, even in the presence of high common mode voltage. This property make the instrumentation amplifiers particularly suitable for test and measurement application (hence the name).

A quick analysis of the complete circuit is here performed, starting assuming a linear condition. Consider, to begin with, the difference amplifier second stage alone, and the voltage between the inputs of OA_3 and ground.

$$\underbrace{v_{\pm}}_{\text{referred to } OA_3} = v_+ = v_- = v_{\text{R}_2^{\text{dwn}}} = v_{\text{o}}^{\text{dwn}} \frac{R_2^{\text{dwn}}}{R_1^{\text{dwn}} + R_2^{\text{dwn}}} \tag{1.51}$$

so that, the current through the resistor R_1^{up} is easily derived using *Ohm's law*.

$$i_{R_1^{\text{up}}} = \frac{v_{\pm} - v_{\text{o}}^{\text{up}}}{R_1^{\text{up}}} = \left(v_{\text{o}}^{\text{dwn}} \frac{R_2^{\text{dwn}}}{R_1^{\text{dwn}} + R_2^{\text{dwn}}} - v_{\text{o}}^{\text{up}} \right) \frac{1}{R_1^{\text{up}}} \tag{1.52}$$

The mesh across the feedback resistor, R_2^{up}, it is useful to find the output voltage expression. Notice, again, that the condition of an infinite impedance input for the

[7] Considering the purpose of this amplifier, the analysis of this circuit is often done exploiting a differential approach.

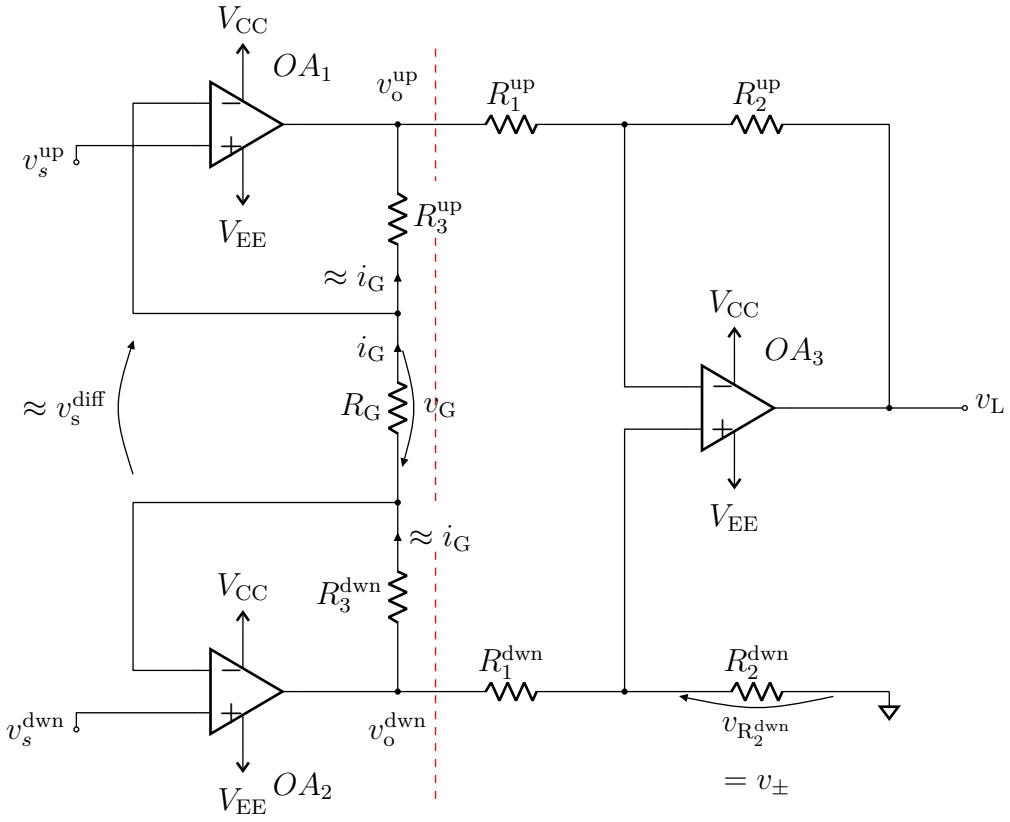


Figure 1.22: Basic instrumentation amplifier. The red dotted line separate the input stage from the core difference amplifier.

op-amp is here used.

$$\begin{aligned} v_L &= v_\pm + R_2^{up} i_{R_1^{up}} \\ &= v_o^{dwn} \frac{R_2^{dwn}}{R_1^{dwn} + R_2^{dwn}} + \frac{R_2^{up}}{R_1^{up}} \left(v_o^{dwn} \frac{R_2^{dwn}}{R_1^{dwn} + R_2^{dwn}} - v_o^{up} \right) \\ &= v_o^{dwn} \frac{R_2^{dwn}}{R_1^{dwn} + R_2^{dwn}} \left(1 + \frac{R_2^{up}}{R_1^{up}} \right) - \frac{R_2^{up}}{R_1^{up}} v_o^{up} \\ &= \frac{R_2^{up}}{R_1^{up}} \left(v_o^{dwn} - v_o^{up} \right) \end{aligned} \tag{1.53}$$

At this point the difference between the two first op-amps has to be derived. To this aim, the presence of a *gain resistor* R_G, is crucial. If the input differential voltage of each op-amp is null (ideal op-amp), then the input differential signal (v_s^{diff}) is also the voltage between the point n_{up} and n_{dwn} and ground (a part from

a minus sign).

$$v_{\mathrm{G}} = v_{n_{\mathrm{dwn}}} - v_{n_{\mathrm{up}}} = v_{\mathrm{s}}^{\mathrm{dwn}} - v_{\mathrm{s}}^{\mathrm{up}} = -v_{\mathrm{s}}^{\mathrm{diff}} \tag{1.54}$$

So the current through R_{G} can be easily find and so the current through all the R_3^{up}, R_{G} and R_3^{dwn} series (since no current is flowing in the op-amps input).

$$i_{\mathrm{G}} = \frac{v_{\mathrm{G}}}{R_{\mathrm{G}}} = -\frac{v_{\mathrm{s}}^{\mathrm{diff}}}{R_{\mathrm{G}}} \tag{1.55}$$

so the difference $v_{\mathrm{o}}^{\mathrm{dwn}} - v_{\mathrm{o}}^{\mathrm{up}}$ is found as follow.

$$\begin{aligned} v_{\mathrm{o}}^{\mathrm{dwn}} - v_{\mathrm{o}}^{\mathrm{up}} &= i_{\mathrm{G}} \left(R_{\mathrm{G}} + R_3^{\mathrm{up}} + R_3^{\mathrm{dwn}} \right) \\ &= -v_{\mathrm{s}}^{\mathrm{diff}} \frac{R_{\mathrm{G}} + 2R_3}{R_{\mathrm{G}}} = -v_{\mathrm{s}}^{\mathrm{diff}} \left(1 + \frac{2R_3}{R_{\mathrm{G}}} \right) \end{aligned} \tag{1.56}$$

Finally, combining Eq.1.53 and Eq.1.56 the overall input-output relation is obtained. In the latter equation, the assumption $R_3^{\mathrm{up}} = R_3^{\mathrm{dwn}} = R_3$, which is very often satisfied, has been exploited.

$$v_{\mathrm{L}} = -\frac{R_2^{\mathrm{up}}}{R_1^{\mathrm{up}}} \left(1 + \frac{2R_3}{R_{\mathrm{G}}} \right) v_{\mathrm{s}}^{\mathrm{diff}} \tag{1.57}$$

This final expression is the starting point to discuss another common characteristic of the instrumentation amplifier, which is important for the purpose of this text. Since the gain can be controlled by the resistor combination of the difference stage, but also by the resistor R_{G}, this means that the output stage resistor can be trimmed by the manufacturer and a single resistor (namely R_{G}) can the made accessible and variable from the external for the user[8]. In this framework, the voltage and current expressions related to R_{G}, the potentiometer, are already been found (Eq.1.54 and 1.55 respectively). Then, in periodic regime, the power is derived.

$$p_{\mathrm{G}} = v_{\mathrm{G}}^{\mathrm{RMS}} i_{\mathrm{G}}^{\mathrm{RMS}} = \frac{\left(v_{\mathrm{G}}^{\mathrm{RMS}} \right)^2}{R_{\mathrm{G}}} = \frac{\left(v_{\mathrm{s}}^{\mathrm{diff,RMS}} \right)^2}{R_{\mathrm{G}}} \tag{1.58}$$

Having the potentiometer in he position shown above (R_{G}) is important, because in this way the device will result as part of the input mesh, so that its voltage takes a role in the input KVL. This is where the input, not yet amplified, voltage has a predominant role, compared to the output voltage and this usually results in a more restricted voltage range for the potentiometer.

[8]For integrated instrumentation amplifier solution.

This result is valid in linear condition only. As for the previous topology, the successive step is to introduce the non-ideality and so the possibility for saturation to occur. A way to do this is to substitute to the three op-amps their real model and considering the voltage controlled voltage source as a fixed voltage source when the V_{OH} or V_{OL} limits are exceeded. Unfortunately, this way of proceeding (implemented before) here is not suitable. Since the complexity of the circuit is increased, the solution by hand of the entire network has become exceedingly complex[9]. In this situation a simulation software[10] is useful and can really speed up the entire analysis process[11].

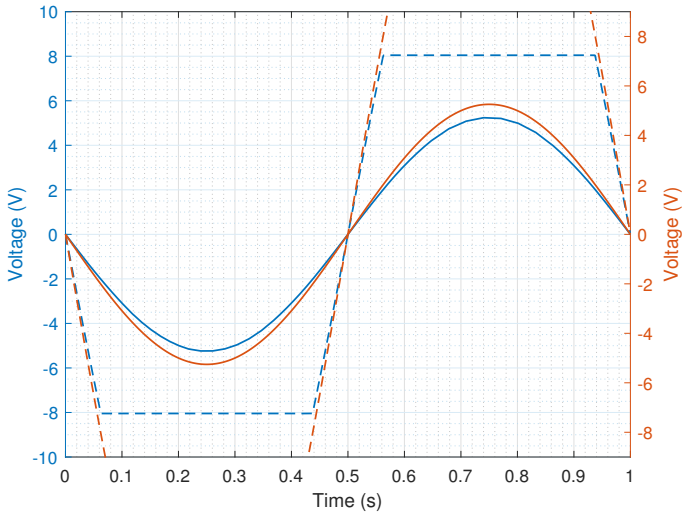


Figure 1.23: Output voltage for the instrumentation amplifier in Figure 1.22, for an input signal of 1 V peak-to-peak. On the left axis (blue), the LTspice simulation waveforms are plotted. On the right axis (orange), Eq.1.57 results are traced. Solid lines are for linear condition, dotted ones for saturation region.

In Figure 1.23 the output voltage is reported. In linear condition, notice the difference between the ideal solution and the simulation's one, clearly due to the neglected input and output impedances as well as the finite open-loop-gain. This discrepancy explodes when saturation is encountered, since the ideal model does

[9]Another source of trouble in this situation is that the active device that could possibly enter saturation are three. So that, following the previous procedure, not knowing *a priori* which of the three op-amp saturate, the possibilities to be explored at totally six (one for every combination). Even if some hypothesis can bring to simplifications, basically, it does not worth it.

[10]LTspice has been used.

[11]Values used for the simulation of the circuits in Figure 1.22 are the following: all op-amps are $OP07$, all fixed resistors are 10 kΩ, input signal is a 1 V peak-to-peak sine wave.

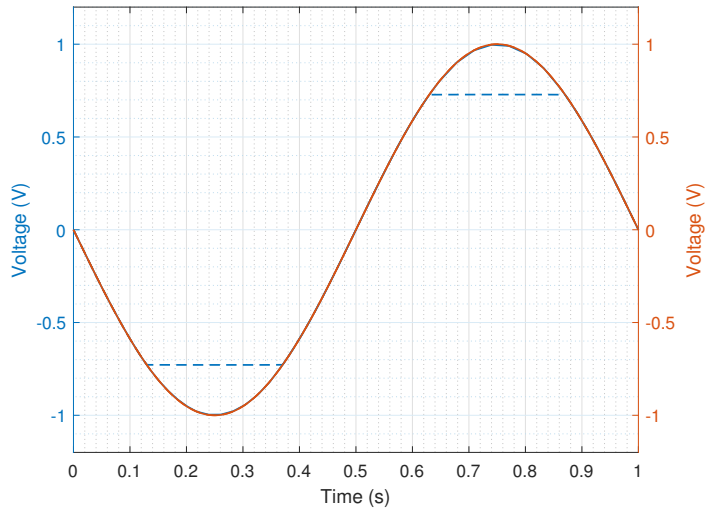


Figure 1.24: Potentiometer voltage v_{G} for the instrumentation amplifier in Figure 1.22, for an input signal of 1 V peak-to-peak. On the left axis (blue), the LTspice simulation waveform are plotted. On the right axis (orange), Eq.1.57 results are traced. Solid lines are for linear condition, dotted ones for saturation region.

not predict it: the dotted orange trace exceed the graph limits to reach its perfect sine shape maximum and minimum. In every aspect this behaviour is the same already discussed.

In Figure 1.24 the voltage across the potentiometer is plotted with the same scheme implemented for v_{L}. Interestingly enough, the saturation condition implies a reduction of the peak voltage across the potentiometer which increases with the saturation is strength. Since Eq.1.54 is well satisfied also considering the ideal component, the maximum voltage applied to the potentiometer is the peak value of the input signal in linear condition or less if saturation is entered. The current i_{G} through the potentiometer can be simply calculated dividing the voltage in Figure 1.24 by the potentiometer resistance. Accordingly the power dissipated is related to the RMS value squared of that waveform divided by the potentiometer resistance. These last quantities are reported in Figure 1.25 for different values of R_{pot}.

In Figure 1.25 the graph is reported not for the entire sweep of the potentiometer but only for the portion in which the linear condition is met. At the left of red point, the saturation region is entered and the blue line is not a good approximation anymore. The power, for higher values of gain, does not increase as before, since the RMS values of both voltage and current ($v_{\mathrm{pot}}^{\mathrm{RMS}}$ and $i_{\mathrm{pot}}^{\mathrm{RMS}}$) become lower than the ones of a perfect sine.

For what concerns the potentiometer substitution in the following chapters, the

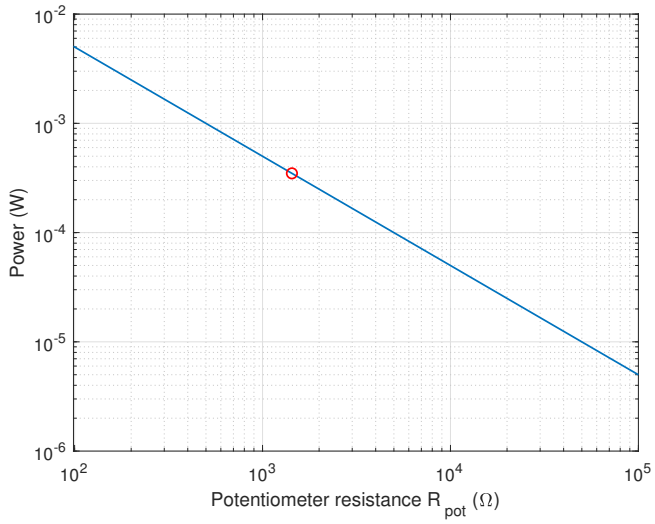


Figure 1.25: Potentiometer dissipated power p_{pot} for the instrumentation amplifier in Figure 1.22, for an input signal of 1 V peak-to-peak.

voltage swing across the device, at least not larger than the input signal range, is much more restricted with respect to what happens for the two preceding amplifiers. Indeed, it partially simplifies the discussion about the digital substitution at least for what concerns the supply of the digital device (and its permissible swing at the terminal).

1.1.2 Transistor based stages

Transistors are the basic component of electronics, also at the base of the more complex devices discussed above, the op-amps. The analysis and discussion of some representative examples of transistors based circuit is absolutely unavoidable in this context. An extremely large number of circuit can be implemented using transistors, *e.g.* they can build acceptable performances amplifier with a very few components (clearly including potentiometers). This make the choice of the examples quite difficult at a first sight.

From a circuital point of view, transistors can be represented as controlled current sources. Depending if they are bipolar or field-effect devices the control quantity of the controlled current source changes: current for the firsts, voltage for the seconds. Around this vary basic concept, the accurate models that describe the transistors' behaviour are built including non-linear elements and so they can be very hard to solve.

While op-amps are common also because of their relatively simple use (at least at a first level of complexity), this is not more true for transistor circuit. Even if

very simple circuits can be implemented exploiting transistors, their understanding requires more knowledge in comparison to equivalent op-amp solutions, also because op-amps are often treated as "black box" devices. To prove that consider the bias (quiescent) point selection problem. When op-amps are used in linear region, so all voltages fall into their permissible region, no bias calculation is required. When transistors are involved a certain attention to the quiescent (*Q point*) selection is mandatory, since the circuit parameters (such as gain) depend on that. Actually, this is

For what concerns amplifiers, some very simple solutions can be found in the literature. As already said, amplifiers can be of different type depending on the nature of the input and output quantities. Often, as a first approach to the transistor circuits, the common emitter amplifier configuration is presented. This amplifier can be controlled in several ways by a potentiometer and in the following an emitter (source) degeneration technique is discussed.

Another way to control transistors amplifier is to modify (again exploiting the potentiometers) the feedback network that a lot of configurations make use of. Feedback is an important concept which can improve the performance of an amplifier in several aspect (gain stability over frequency, input and output impedances, noise sensitivity). This solution forces the introduction of important approximated techniques to calculate the parameter of the circuit and so a feedback amplifier example is presented.

The heavy mathematical complexity of the more accurate models makes the circuit solution in which these models are involved not feasible by hand. Since, sooner or later, in the calculation, a non-linear system has to be solved, the analysis by hand is not worth from the beginning. These models obviously include saturation effects, but a more simple analysis can be done when they are driven in linear region of operation (saturation region for field-effect transistors).

Another commonly used circuit, the buffer, implemented as a common collector (drain) topology is here omitted because its functioning usually does not depend on any variable resistance element; so it does not fit the topic sufficiently well. Despite the fact that the present chapter is dedicated to the amplifier circuit, a regulated DC supply circuit is discussed here, because of its relevance to the transistor behaviour and potentiometer implementation analysis.

Common emitter (source) topology

For sake of completeness, it is important to remember that the procedure for solving (in general) transistor circuits by hand, consists in doing a preliminary analysis of the working (Q) point and then, through a linearisation, to use some Q-dependent parameters to solve the circuit. In dong this it appears clear that the solution found is valid only in linear, *small signal*, condition, which are already affected by

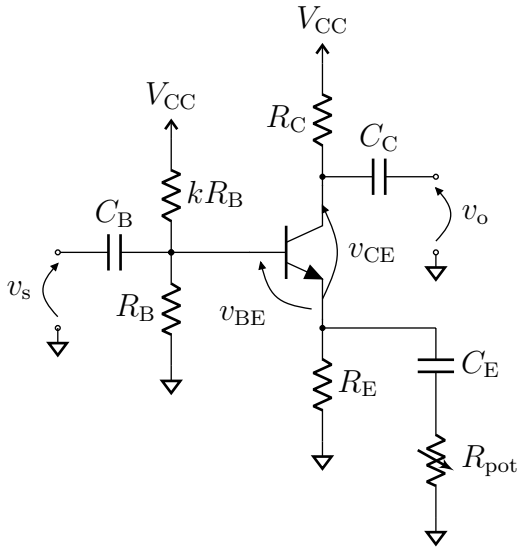


Figure 1.26: BJT common emitter amplifier with voltage divider implemented bias and bypass capacitor network controlled gain.

some usual simplification. Despite the heavy ideality of the entire procedure, under the hypothesis step by step introduced, the results can still be quite interesting, also because they give some very useful insights to the functioning of the circuit and on the effect of the various components on it.

Theoretically an immediate accurate way of proceeding would be to substitute a sufficiently good model for the active device and simply looking for a solution of the circuit (as done for the op-amps' topologies). In the present case, this would mean to substitute the *Ebers–Moll* model of the BJT in the schematic in Figure 1.26. Unfortunately, the accuracy and completeness of the results are paid with the difficulties of the mathematical solution: the *Ebers–Moll* model is intrinsically non-linear, since it contains two diodes (for the emitter-base and base-collector junction modelling). This implies that an approximated solution (easily feasible with a calculator) has to be performed, actually making pointless almost all the calculations made by hand[12].

So a more usefull way of proceeding is to assume a region of operation of the circuit (in this case active forward, so linear region) and approximate the component

[12]Notice that a solution of the circuit exploiting the *Ebers-Moll* model does not require a bias point calculation, since the latter is mandatory only if a linearisation is performed (so an approximation) through the small signal equivalent circuit. The accurate non linear model already "permits" the derivation of the solution in any region of operation.

behaviour so that the solution of the circuit becomes easier. A discussion of what happens when non-linear behaviours are to be considered will be done in the following.

To calculate the working point of the BJT in Figure 1.26 it is sufficient to perform a *Thévenin equivalent* of the circuit portion seen from the base towards the left (not considering the time varying generator, so disconnecting the C_{B} capacitor practically). So that a V_{eq} and an R_{eq} will permit the redraw of the circuit accordingly to the following definition:

$$\begin{cases} V_{\mathrm{eq}} = V_{\mathrm{CC}} \dfrac{R_{\mathrm{B}}}{R_{\mathrm{B}} + kR_{\mathrm{B}}} = V_{\mathrm{CC}} \dfrac{1}{k+1} \\ R_{\mathrm{eq}} = R_{\mathrm{B}} \parallel kR_{\mathrm{B}} = R_{\mathrm{B}} \dfrac{k}{k+1} \end{cases}$$

This equivalent circuit on the left permits the simple solution of a mesh (KVL, Eq.1.59) on the input branch, passing across the emitter-base junction, finishing on the emitter resistor[13]

$$V_{\mathrm{eq}} - R_{\mathrm{eq}} I_{\mathrm{B}} - V_{\mathrm{BE}} - R_{\mathrm{E}} I_{\mathrm{E}} = 0 \tag{1.59}$$

In the latter equation some quantities can be re-written in order to find a simple linear equation in I_{B}, bias base current. Since the BJT is assumed to be in linear condition the base-emitter voltage drop is the one that can be measured across an on-state diode. So V_{BE} can be approximated with a known value around 0.6 V. For what concerns the emitter current, it can be written as the base current multiplied by a factor, which is $\beta_{\mathrm{F}} + 1$, where β_{F} is the common-emitter current gain (considered as a constant datum[14])

$$\begin{aligned} V_{\mathrm{eq}} - R_{\mathrm{eq}} I_{\mathrm{B}} - V_{\mathrm{BE}} - R_{\mathrm{E}} \left(\beta_{\mathrm{F}} + 1\right) I_{\mathrm{E}} &= 0 \\ I_{\mathrm{B}} = \frac{V_{\mathrm{eq}} - V_{\mathrm{BE}}}{R_{\mathrm{eq}} + \left(\beta_{\mathrm{F}} + 1\right) R_{\mathrm{E}}} & \end{aligned} \tag{1.60}$$

Eq.1.60 for the bias base current is the one from which all the other quantities involved in the bias calculation are derived. Immediately the two other fundamental

[13]Clearly, being in DC conditions means also that the bypass capacitor make visible to the emitter, in terms of bias, only the resistor R_{E} to ground.

[14]The actual model of the real device is much more complex and it makes almost all quantities inter-dependent and not constant. But at least at a first level of approximation, β_{F} can be considered a constant.

currents are written as

$$I_{\mathrm{C}} = \frac{\beta_{\mathrm{F}} \left(V_{\mathrm{eq}} - V_{\mathrm{BE}}\right)}{R_{\mathrm{eq}} + \left(\beta_{\mathrm{F}} + 1\right) R_{\mathrm{E}}} \tag{1.61}$$

$$I_{\mathrm{E}} = \frac{\left(\beta_{\mathrm{F}} + 1\right) \left(V_{\mathrm{eq}} - V_{\mathrm{BE}}\right)}{R_{\mathrm{eq}} + \left(\beta_{\mathrm{F}} + 1\right) R_{\mathrm{E}}} \tag{1.62}$$

This will easily permit a calculation of the V_{CE} voltage which must satisfy an inequality related to the initial assumption of the region of operation. When the linear region is entered the emitter-base junction is forward bias so $V_{\mathrm{BE}} \approx 0.6\,\mathrm{V}$, while the base-collector junction is reversed bias, so that $V_{\mathrm{BC}} < 0\,\mathrm{V}$. This implies that, in linear condition, the emitter-collector voltage has to be positive: $V_{\mathrm{CE}} > 0\,\mathrm{V}$.

To briefly see what happens when the condition is missed, it is useful to consider the base voltage divider (formed by R_{B} and kR_{B}) as a variable divider. Sometimes, in place of the two resistor, a real *bias potentiometer* is used to make possible to trim the working point as wanted. In the following plot (Figure 1.27), this method is implemented, so that the Spice[15] simulation will show all the region of operation accordingly to the potentiometer sweep[16].

When the lower resistor is too small with respect to the upper one, the BJT is off, so that both I_{B}, I_{C} and I_{E} are null. If no current is flowing in the emitter resistor, the emitter is at $0\,\mathrm{V}$, so the voltage V_{BE} grows as the base voltage respect to ground increases. When V_{BE} reaches the emitter-base junction turn on voltage the current begin to flow into the base, so the collector to emitter current does. This implies that the voltage drops across emitter and collector resistors increase and the negative feedback action introduced by R_{E} make the linear region increment of I_{B} linear too (instead of exponential).

This situation is maintained until the voltage drop across R_{C} grows enough to put the BJT in saturation region. In saturation, the collector to emitter current is no more related to the base current, the *transistor effect* is lost and the current I_{C} is almost constant around the saturation value, $I_{\mathrm{C}}^{\mathrm{sat}}$. Since, the saturation region is entered when both emitter base and collector base junctions are forward biased, the mesh across those voltages make evident the V_{CE} is almost null.

$$V_{\mathrm{CE}} + \underbrace{V_{\mathrm{BC}}}_{\approx\ 0.6\,\mathrm{V}} - \underbrace{V_{\mathrm{BE}}}_{\approx\ 0.6\,\mathrm{V}} = 0 \qquad \rightarrow \qquad V_{\mathrm{CE}} \approx 0 \tag{1.63}$$

[15]The model of the BJT used is the 2N3904: .model 2N3904 NPN(IS=1E-14 VAF=100 Bf=300 IKF=0.4 XTB=1.5 BR=4 CJC=4E-12 CJE=8E-12 RB=20 RC=0.1 RE=0.1 TR=250E-9 TF=350E-12 ITF=1 VTF=2 XTF=3 Vceo=40 Icrating=200m mfg=NXP).

[16]Looking at the schematic of Figure 1.26, the potentiometer substitution for bias purposes results in a lower resistor $R_{\mathrm{B}}^{\mathrm{dwn}} = xR_{\mathrm{pot}}^{\mathrm{TOT}}$, while the upper resistor becomes $R_{\mathrm{B}}^{\mathrm{up}} = R_{\mathrm{pot}}^{\mathrm{TOT}}(1-x)$.

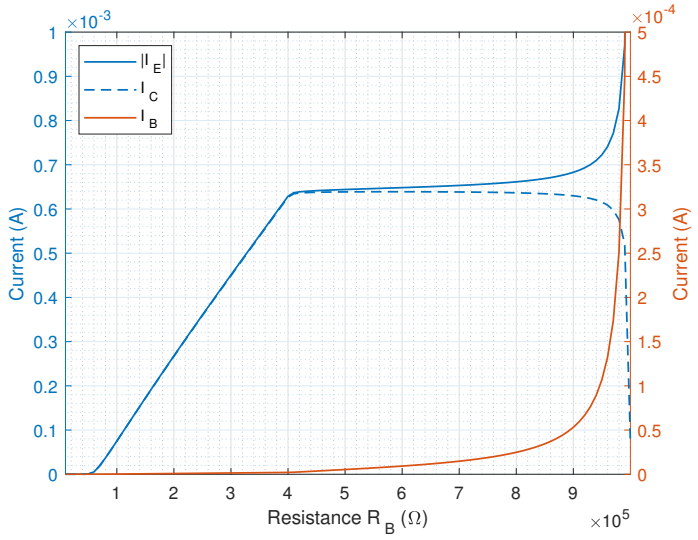


Figure 1.27: Bias current traced for the circuit in Figure 1.26.

In real devices, the residual V_{CE} voltage when saturation occurs is not null, *i.e.* $V_{\mathrm{CE}}^{\mathrm{sat}} \approx 0.2\,\mathrm{V}$ as visible in Figure 1.28; then it decreases slowly from $V_{\mathrm{CE}}^{\mathrm{sat}}$ to practically a null voltage. The voltages involved (V_{BE} and V_{CE}) are reported in Figure 1.28. Notice the almost linear initial increment of V_{BE}, while the collector is still at V_{CC} and the emitter is still at reference, so that $V_{\mathrm{CE}} = V_{\mathrm{CC}}$. When the BJT turns on, the V_{BE} flattens while the V_{CE} start decreasing linearly with the current increment, accordingly to the *ohms law*. Then, the saturation is reached and the two voltages enter again a constant portion of the characteristic again.

Basically, this method of proceeding is approximated since it consider V_{BE} constant as if, in the on state of the BJT, the junction between emitter and base was a constant V_γ forward voltage drop diode. This is not true, since, as visible in Figure 1.28, the V_{BE} is absolutely not constant. Still, this a good approximation when the region of operation is far from the transition between one region and the other.

As an example, consider the following values for the circuit in Figure 1.26.

- $R_{\mathrm{E}} = 3.9\,\mathrm{k}\Omega$
- $R_{\mathrm{C}} = 10\,\mathrm{k}\Omega$
- $R_{\mathrm{B}} = 68\,\mathrm{k}\Omega$
- $k = 235/34$ so that $kR_{\mathrm{B}} = 470\,\mathrm{k}\Omega$
- For the BJT consider $\beta_{\mathrm{F}} = 300$

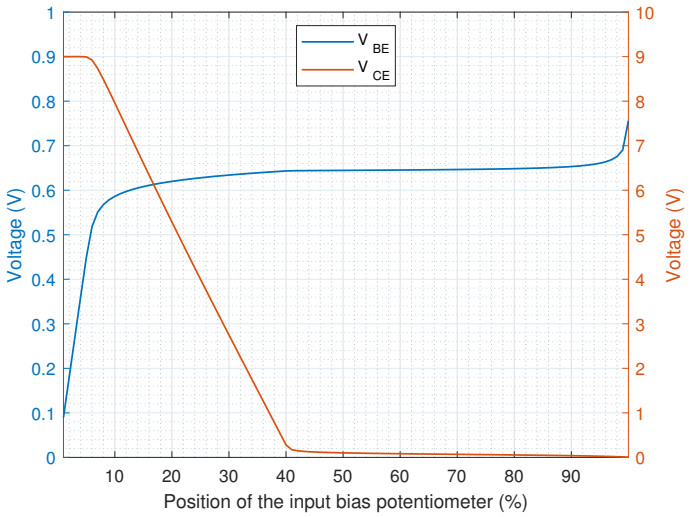


Figure 1.28: Bias voltages traced for the circuit in Figure 1.26.

- $V_{CC} = 9\,\text{V}$

Using Eq.1.60, Eq.1.62 and Eq.1.61, plus the mesh across the output side to calculate di V_{CE}, the values in Table 1.1, first column. The more precise values have been calculated with LTSpice simulator (second column), for comparison. The

Quantity	approximated	LTspice
I_B	435.8 nA	409.7 nA
I_C	130.7 µA	130.9 µA
I_E	131.2 µA	131.3 µA
V_{BE}	0.6 V	0.623 V
V_{CE}	7.181 V	7.173 V

Table 1.1: Comparison table for the approximated bias values and the simulated ones.

values are close enough to consider the approximation satisfying. These values are to be used in order to calculate the linear circuit parameters. These parameters are calculated as a result of a Taylor expansion around the working point of the more complex curves describing the current and the voltages.

Before the final solution of the equivalent small signal circuit, the *hybrid parameters* equivalent circuit is presented, as well as the expressions for the parameters themselves.

From the equivalent circuit above, it is possible to derive two equations, from which the parameters definition can be written directly. This equivalent model

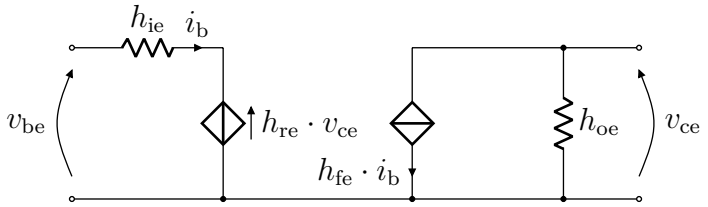


Figure 1.29: BJT small signal equivalent circuit drawn exploiting the *hybrid parameters*.

is exactly an application of the two ports element theory, in which the *hybrid* denomination means that, in the two equation system (Eq.1.1.2), one expression is a voltage mesh (KVL), while the other is a current sum at a node (KCL).

$$\begin{cases} v_{\mathrm{be}} = h_{\mathrm{ie}} i_{\mathrm{b}} + h_{\mathrm{re}} v_{\mathrm{ce}} \\ i_{\mathrm{c}} = h_{\mathrm{fe}} i_{\mathrm{b}} + h_{\mathrm{oe}} v_{\mathrm{ce}} \end{cases}$$

Since all this quantities are small signal variations (small characters), if an overall voltage or current is held constant, the corresponding small signal quantity is null. So that the following definitions can be written, directly from Eq.1.1.2.

$$h_{\mathrm{ie}} := \left.\frac{v_{\mathrm{be}}}{i_{\mathrm{b}}}\right|_{v_{\mathrm{ce}}=0,\ v_{\mathrm{CE}}=const.} \tag{1.64}$$

$$h_{\mathrm{re}} := \left.\frac{v_{\mathrm{be}}}{v_{\mathrm{ce}}}\right|_{i_{\mathrm{b}}=0,\ i_{\mathrm{B}}=const.} \tag{1.65}$$

$$h_{\mathrm{fe}} := \left.\frac{i_{\mathrm{c}}}{i_{\mathrm{b}}}\right|_{v_{\mathrm{ce}}=0,\ v_{\mathrm{CE}}=const.} \tag{1.66}$$

$$h_{\mathrm{oe}} := \left.\frac{i_{\mathrm{c}}}{v_{\mathrm{ce}}}\right|_{i_{\mathrm{b}}=0,\ i_{\mathrm{B}}=const.} \tag{1.67}$$

Since the curves that describe i_{B}, i_{C} and v_{CE} are complicated, a set of common assumption is consider to have a more direct passage from DC to AC small signal domain.

To begin with, the *forward current gain* $h_{\mathrm{fe}} = \beta_0$, which in general is different from β_{F} since the latter is the ratio of the collector and base current in DC, which is a function of the base current itself. To avoid the duty of extrapolate a derivative calculation from experimental measure, often the $\beta_0 = \beta_{\mathrm{F}}$ assumption is taken.

The *input resistance* h_{ie} can be extrapolated directly from a Taylor expansion

of the Ebers-Moll equation that give the current i_C[17]. In doing that, neglecting terms of the order grater than one, it results the following expression:

$$i_c = \frac{I_C}{V_T} V_{be} \;\rightarrow\; \beta_0 i_b = \frac{I_C}{V_T} V_{be}$$
$$h_{ie} = \frac{\beta_0 V_T}{I_C} = \frac{V_T}{I_B} \; . \tag{1.69}$$

With the values previously evaluated this input resistance is evaluated to be $h_{ie} = 59.66\,\mathrm{k}\Omega$.

Usually the *reverse voltage ratio* h_{re} is so small that its contribute to the input mesh ($h_{re} \cdot i_b$) is usually negligible. However, its value is around $h_{re} \approx 10^{-4}$.

The output admittance h_{oe} is related to a commonly used parameter called *Early's voltage*, which encapsulates the information of "how greater is the slope of the I_C current". So a good transistor has a large *Early's voltage* so that the current generated by the controlled current source is not "wasted" into the parallel admittance, but it will be entirely delivered to the load. The *Early's voltage* is usually denoted with the symbol V_A and it enters the output admittance's expression as

$$h_{oe} = \frac{I_C}{V_A} \; . \tag{1.70}$$

In our example it results that $h_{oe} = 1.307\,\mu\Omega^{-1}$.

At this point the complete circuit can be re-written accordingly in order to be solved. If the analysis is done inside the band of the amplifier, the capacitor has to be consider short or open circuit accordingly (in the current example, the bypass capacitor on the emitter has to be consider as a short). The constant generators have to be switched off, while the small signal variation in input has to be turned on. These considerations are resumed in the circuit in Figure 1.32 which is the one to be solved.

[17] In this model, the collector current has the expression as follow

$$i_C = I_S \left[\left(e^{v_{BE}/V_T} - e^{v_{BC}/V_T} \right) - \frac{1}{\beta_R} \left(e^{v_{BC}/V_T} - 1 \right) \right] \tag{1.68}$$

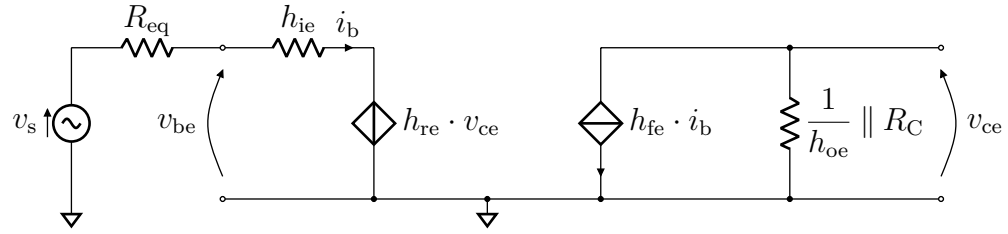


Figure 1.30: BJT common emitter amplifier small signal circuit.

Solving the system derived for the latter circuit, the following results are found.

$$\begin{cases} v_{\text{ce}} = v_{\text{s}} \left[\dfrac{1}{h_{\text{re}} + \dfrac{R_{\text{eq}} + h_{\text{ie}}}{h_{\text{fe}} \left(h_{\text{oe}}^{-1} \parallel R_{\text{C}} \right)}} \right] \\ i_{\text{b}} = \dfrac{1}{h_{\text{fe}}} \left[\dfrac{1}{h_{\text{re}} \left(h_{\text{oe}}^{-1} \parallel R_{\text{C}} \right) + R_{\text{eq}} + h_{\text{ie}}} \right] v_{\text{s}} \end{cases}$$

In order to be assumed as good approximations, the small signal condition has to be satisfied, hence, whatever the curve of v_{ce} is, it must remain inside the interval between V_{CC} and $V_{\text{CE}}^{\text{sat}}$ (not changing the region of operation of the BJT).

After this discussion about the amplifier itself, the potentiometer topics rises again. To control the gain of the amplifier, at least five options come immediately in mind involving one potentiometer placed in different points of the circuit. The first two will be discussed in the following and concern the positioning of a volume potentiometer either at the front or after the amplifier. The basic difference of the two possibilities is that, assuming that proper decoupling capacitor have been inserted, the reduction of the outcoming signal at the output does not affect in any way the functioning of the amplifier. While, supposing an input signal large enough that at full volume the amplifier exits the small signal approximation (or even changes the operating region), the input volume control can be useful to keep the amplifier in the proper region, on the contrary with respect to the output volume control.

The third option is similar to the classic volume control: instead of putting an R_{C} resistor on the collector and decoupling the volume control, the potentiometer itself is placed between the supply and the collector. Clearly the total resistance of the potentiometer has to be the same of the other cases' R_{C} resistance, but, from the external, the behaviour of the circuit is exactly the same as the output volume solution. For what concerns the voltage swing across the potentiometer the input volume solution obviously has the peak to peak swing of the input signal, which

usually is not large (also because of the constrain on the small signal condition). The other two solutions, instead, support large swings, since the collector voltage can vary from $V_{\mathrm{CE}}^{\mathrm{sat}} \approx 0.2\,\mathrm{V}$ (limit of the saturation region) up to V_{CC} (limit reached with the interdiction region). These three solutions do not affect directly the gain of the core amplifier, since they act exclusively on the input or output signals.

Two other common solutions are much more conservative from the potentiometer prospective. One consists in putting a potentiometer in place of the emitter resistor ($R_{\mathrm{pot}} = R_{\mathrm{E}}$) and connecting the bypass capacitor to the central tap of the potentiometer. The gain is maxed when the potentiometer tap is shorted to the emitter, so that the AC equivalent circuit looks as depicted in Figure 1.26, with the emitter connecting to ground (again, just for the variations, since the DC bias is not modified). The gain is at its minimum when the potentiometer is in the opposite position, so that, introducing negative feedback, the emitter resistor shows the same value both for the bias and the AC equivalent circuit and it is equal to the total value of the potentiometer. This method has the advantage that the potentiometer sees always a voltage at its fixed terminals which is almost constant around the bias value. This is true in small signal conditions (for other region of operation, the voltage across the potentiometer increases but always limited to the peak to peak swing of v_{s}[18]).

The last solution here introduced is to place a potentiometer in a variable resistor configuration in series with the bypass capacitor (between ground and the second terminal of the capacitor). With this arrangement the situation is similar to the previous case; the only difference appears when the small signal condition is violated: the voltage ripple is centred around zero volts and not around the emitter voltage bias value. But also in linear condition the constant contribution due to the bias voltage is dropped out by the bypass capacitor, so that in this configuration the voltage across the potentiometer can be hundred of time smaller than with the output volume solutions. The latter solution is the one shown in Figure 1.26.

These same solutions can be implemented without significant modification, exploiting other families of transistors, namely JFET and MOSFET as immediate alternatives.

Series-feedback pair amplifier

The circuit here discussed is an example of how the negative feedback theory can be exploited to obtain large stable gain at least from a relatively simple circuit with

[18]This is because the potentiometer voltage is part of the input mesh (KVL) in which also v_{BE} appears. v_{BE} is almost constant when the BJT is in an on state and far from the knee of the characteristic. In this way, from the KVL, it is possible to see that v_{s} is translated of a quantity v_{BE} on the emitter.

discrete transistors instead of op-amps[19]. The following is also a good example of how, using different types of transistors in the same circuit, some advantages can be reached because of the intrinsic differences of each family exploited. In this case the first stage of amplification is implemented with a JFET[20], so that the input impedance of the amplifier is vary large and in particular much larger than the one obtained with a BJT first stage. This is because the BJT is a current controlled device, while the FET transistors in general are voltage controlled devices. On the other hand, BJTs has a much larger gain with respect to JFETs, so the second voltage amplifier stage is a PNP BJT stage, providing the voltage gain needed to make the feedback system work as intended. The third stage is a common collector buffer.

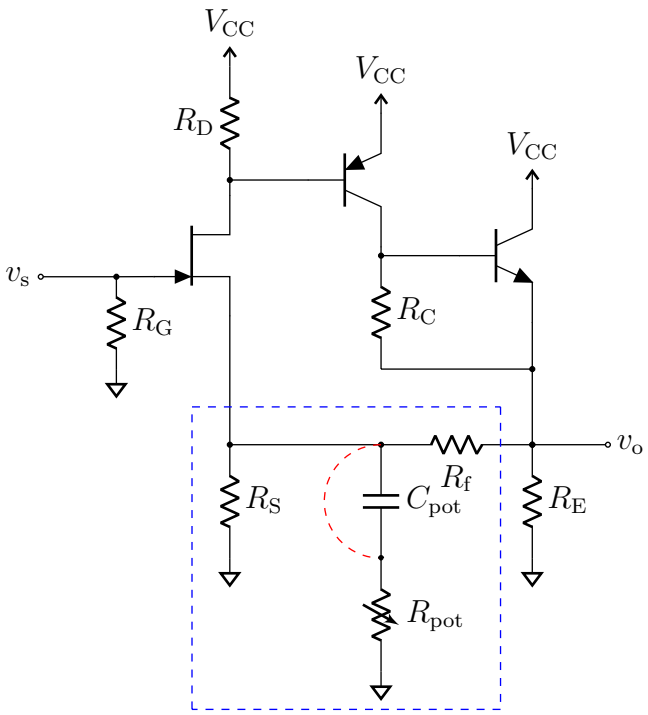


Figure 1.31: Series-feedback amplifier circuit. The red arc indicates that, for in band signals, the capacitor C_{pot} is equivalent to a short circuit. The blue dotted box isolate the feedback network β, the rest of the circuit forms the A, main high gain amplifier, block.

[19] As done in the previous sections.

[20] In this position also a MOS device can be used with similar performances. The bias of the gate would be rearranged because of the opposite sign of the threshold voltage between MOS and JFET transistors.

The bias calculation follows basically the same steps of the previous topology: a guess on the region of operation is done and, *a posteriori*, the validity of the results obtained is verified. For sake of brevity the results of a LTspice simulation are reported in Table 1.2 and Table 1.3. The results below are calculated exploiting the following values: $R_G = 100\,M\Omega$, $R_D = 2.1\,k\Omega$, $R_C = 10\,k\Omega$, $R_E = 22\,k\Omega$, $R_f = 3.3\,k\Omega$, $R_S = 1.035\,k\Omega$, $C_{pot} = 47\,\mu F$[21], $R_{pot} = [10\,\Omega \div 5\,k\Omega]$.

V_{GS}	V_{DS}	I_D
$-1.338\,V$	$7.075\,V$	$279.1\,\mu A$

Table 1.2: JFET bias values for the circuit in Figure 1.31.

V_{BE} or V_{EB}	V_{CE} or V_{EC}	I_B	I_C	I_E
$0.585\,V$	$3.654\,V$	$-337\,nA$	$-69.6\,\mu A$	$69.9\,\mu A$
$0.658\,V$	$4.312\,V$	$3.735\,\mu A$	$1.158\,mA$	$-1.162\,mA$

Table 1.3: BJTs bias values for the circuit in Figure 1.31. The first raw is referred to the PNP second stage transistor, the second one to the NPN output transistor.

The quantities reported are compatible with linear (for BJT) or saturation (for JFET) operating region so that the equivalent small signal circuit can be drawn. Consider that all the previous discussions concerning the parameter to use hold here, but, in addition to that, it is useful to remember that no difference stands between the small signal equivalent of PNP and NPN BJTs (the difference is only in the bias verse of currents and voltages). Furthermore, the JFET equivalent circuit is introduced as a voltage controlled (infinite input impedance approximation) current source.

Considering the classic theory of feedback, the circuit here discussed is a voltage (series-shunt) amplifier because the negative feedback is taken in parallel from the output signal and is connected to the source of the JFET common source amplifier (so it is not connected to the same point where the input signal is). Once the type of feedback configuration is clarified, identifying the A and β blocks results as an easy task: so that the common source, common emitter and common collector stages fall in the A inner amplifier block, while R_f, R_{pot} and R_S form the feedback network.

$$A_F = \frac{A}{1+\beta A} \quad \rightarrow \quad \lim_{A\to\infty} A_F = \frac{1}{\beta} \tag{1.71}$$

[21] Pay attention that also the input signal has been decoupled through a sufficiently large capacitor, in order to not affect the simulation done in the following.

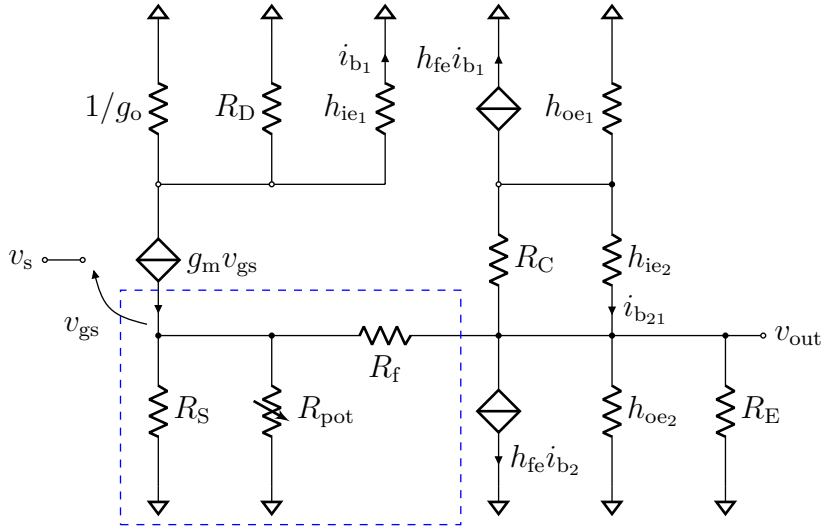


Figure 1.32: Small signal equivalent circuit of the amplifier in Figure 1.31. The dotted blue box points out the β feedback network.

If, exploiting the equivalent small signal circuit, the open loop gain will result high enough, the Eq.1.71 holds and an easy approximated value of the gain can be calculated. The exact solution of the equivalent circuit for this purpose is not immediate and it requires a certain amount of experience, but, at least intuitively, the approximation can be taken assuming that the JFET common source and mostly the PNP common emitter stages provide a sufficiently large amount of gain. If this is assumed the analysis of the β feedback network is quick: applying a test voltage generator (V_2^{test}) to the output port, the port one voltage is calculated (V_1^{test}), and β is nothing but their ratio.

$$\beta = \frac{V_1^{\text{test}}}{V_2^{\text{test}}} \tag{1.72}$$

Applying a V_2^{test}, V_1^{test} is found by considering the *Ohm's law* as follow.

$$V_1^{\text{test}} = V_2^{\text{test}} \frac{R_S \parallel R_{pot}}{R_f + R_S \parallel R_{pot}} \quad \rightarrow \quad \beta = \frac{R_S \parallel R_{pot}}{R_f + R_S \parallel R_{pot}} \tag{1.73}$$

Making the reciprocal of the latter expression, the simple approximation of the gain is found.

$$A_F \approx 1 + \frac{R_F}{R_S \parallel R_{pot}} \tag{1.74}$$

So that the ideal gain, obtainable only for $A \to \infty$, exploiting Eq.1.71 has the following expression.

$$A_{\mathrm{F}}^{\mathrm{ideal}} = 1 + \frac{R_{\mathrm{F}}}{R_{\mathrm{S}} \parallel R_{\mathrm{pot}}} \tag{1.75}$$

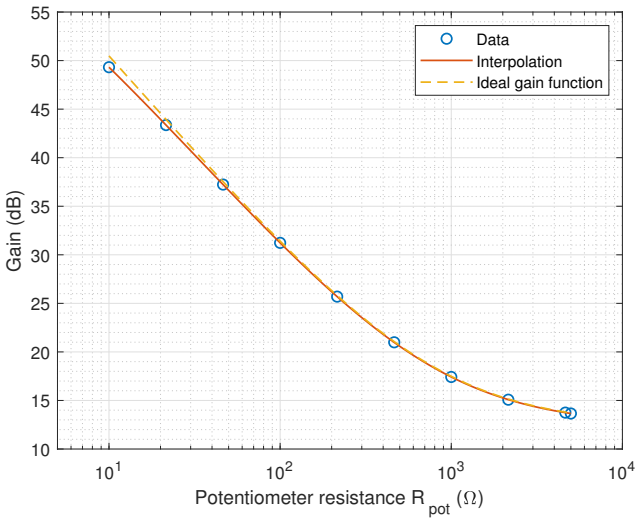


Figure 1.33: Gain curve for the series-pair feedback amplifier.

Simulating the resulting output voltage for a range of R_{pot} different values (here from $10\,\Omega$ up to $5\,\mathrm{k}\Omega$) it is possible to evaluate a curve representing the error between the ideal gain in Eq.1.75 and the simulated one. In Figure 1.33, the simulated gain result is plotted as well as the ideal function; the gain error can be calculated as:

$$\epsilon = \frac{\left| A_{\mathrm{F}}^{\mathrm{ideal}} - A_{\mathrm{F}}^{\mathrm{real}} \right|}{A_{\mathrm{F}}^{\mathrm{ideal}}} \ . \tag{1.76}$$

The divergence of the two curve is minimal in the decibel scale, which tends to compress the traces at high values of gain, but it is clear from Figure 1.34 that this error it is not negligible at high gain range. From the current simulation it results that to an ideal gain value of 50 dB corresponds a real gain of 48.895 dB, which in linear scale results in an error of approximately 11.94 %. Still, this approximation is quite good for low gain rages, for which the gain error stays well below 2 %, before it starts to increase linearly with R_{pot}.

To see what are the behaviours of voltage, current and power of the potentiometer resistance is useful a practical conceptual approximation of the circuit. Since the

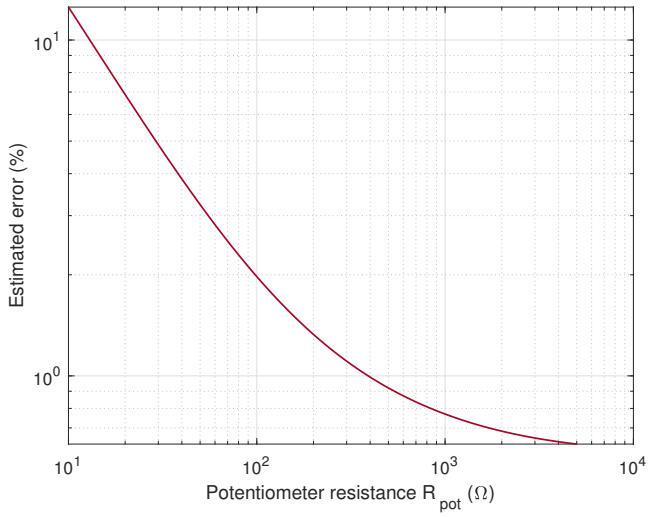


Figure 1.34: Gain error of the series-pair feedback amplifier between ideal and simulated curves.

circuit involves a negative feedback and the overall structure is non inverting (notice that the signal passes through two inverting stages and a non inverting one) an artificial op-amp can be superimposed on the circuit. The output of the op-amp is placed on the output emitter node, while, being the amplifier non inverting the input is connected directly on the non-inverting input. The β network remains outside the op-amp, making clear the analogy with the non inverting amplifier topology. Looking at this simplification Figure 1.35 and considering the classical

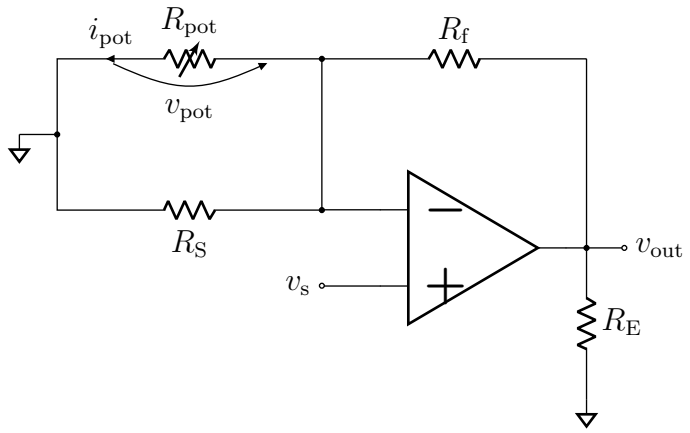


Figure 1.35: Intuitive equivalent circuit of the BJT feedback amplifier as it can be visualised for simplifying the calculations.

assumption taken in the op-amp based circuit, the quantities on the potentiometer are easily found. Notice that this artificial substitution becomes more legitimate the higher the open loop gain becomes. Looking at the input mesh the following expressions are derived.

$$v_{\text{pot}} = v_{\text{s}} \tag{1.77}$$

$$i_{\text{pot}} = \frac{v_{\text{s}}}{R_{\text{pot}}} \tag{1.78}$$

$$p_{\text{pot}} = v_{\text{pot}}^{\text{RMS}} i_{\text{pot}}^{\text{RMS}} = \frac{\left(v_{\text{s}}^{\text{RMS}}\right)^2}{R_{\text{pot}}} \tag{1.79}$$

Also, this expression is important because it tells that the swing across the potentiometer is limited in a range which is usually narrow, since the input voltage is kept small in order to exploit the linear region of the BJTs transistor (well below $2V_{\text{T}}$, where $V_{\text{T}} = k_{\text{B}}T/q$ is the thermal voltage). The latter expressions hold in linearity. As done before, the saturation situation is investigated by considering the output of the circuit as saturated at a high or a low constant voltage level (V_{OH} or V_{OL} respectively). Exploiting the *Millman's theorem* the voltage expression across the potentiometer can be found[22]:

$$v_{\text{pot}} = \frac{\dfrac{V_{\text{OH}}}{R_{\text{f}}} + \cancelto{\approx 0}{\dfrac{v_{\text{s}}}{R_{\text{in}}^{\text{A}}}}}{\dfrac{1}{R_{\text{f}}} + \cancelto{\approx 0}{\dfrac{1}{R_{\text{in}}^{\text{A}}}} + \dfrac{1}{R_{\text{S}} \parallel R_{\text{pot}}}} \; . \tag{1.80}$$

By multiplying numerator and denominator by R_{f} a quite simple and useful expression is written:

$$v_{\text{pot}} = \frac{\dfrac{V_{\text{OH}}}{R_{\text{f}}}}{\dfrac{1}{R_{\text{f}}} + \dfrac{1}{R_{\text{S}} \parallel R_{\text{pot}}}} = \frac{V_{\text{OH}}}{1 + \dfrac{R_{\text{f}}}{R_{\text{S}} \parallel R_{\text{pot}}}} = \frac{V_{\text{OH}}}{A_{\text{F}}^{\text{ideal}}} \; . \tag{1.81}$$

Current and power are defined in the usual way and are derived from the latter expression. In Figure 1.36 the potentiometer voltage is traced, for the ideal approximated case and the simulated, more accurate, one. Notice that in real case the linear to saturation transition is smooth and not abrupt as in the ideal one. Moreover, the neglected term, depending on the input voltage in saturation, contributes so that instead of a perfectly flat saturated value, the trend of the input signal is maintained through a factor of $R_{\text{f}}/R_{\text{in}}^{\text{A}}$.

[22]Where the term $R_{\text{f}}/R_{\text{in}}^{\text{A}}$ is consider much smaller than 1.

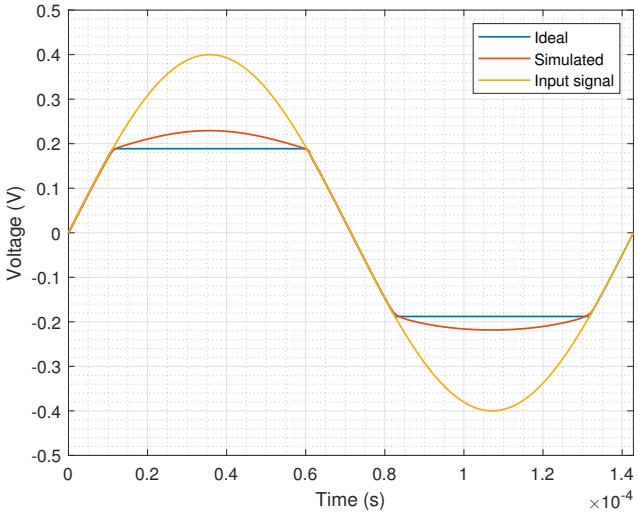


Figure 1.36: Potentiometer voltage for the circuit of the series-shunt amplifier presented.

Regulated DC supply (with feedback)

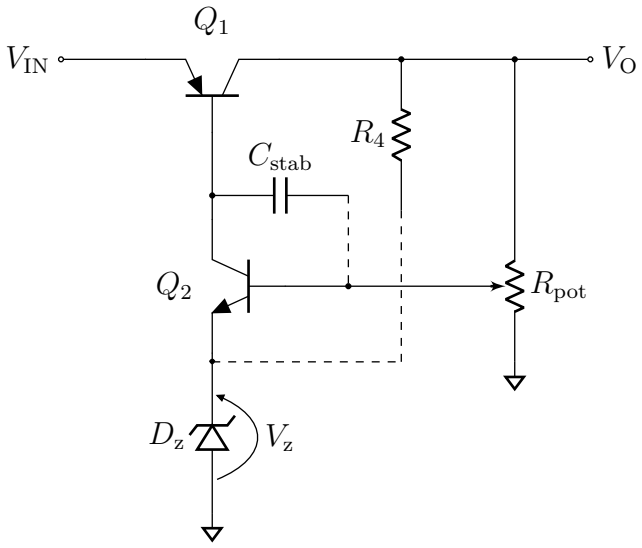


Figure 1.37: Simple voltage regulator.

The regulated DC supply constitutes an example of feedback circuit in which the potentiometer is subjected to a very different scale of voltage and current swing. While in the previous circuit, whose aim was to amplify signals, the potentiometer

was decoupled from the DC component through a capacitor, here the situation is reversed. The voltage regulator purpose is to generate a specific DC voltage from a higher source. To do this, the base (command) current of transistor Q_1 is controlled by the transistor Q_2, which is "sampling" the output voltage, establishing a negative feedback. When the output voltage v_{O} increases, the emitter base voltage of Q_2 increases too, through the voltage divider formed by the potentiometer. This make Q_2 increasing its collector current. A simple KCL at the base of Q_1 shows that the current increase for Q_2 makes the base current of Q_1 to decrease, facing it to supply less current to the load.

Some further details can be introduced, such as a bias resistor for the zener diode, connected from its cathode to the output voltage in order to stabilise its current and so the controlling voltage v_{BE_2}. Another improvement is related to the variation circuit. A capacitor placed between base and collector of Q_2 creates a local feedback low pass filter (through the *Miller effect*) which prevents the circuit to get into oscillation:

$$V_{\mathrm{pot}} = V_{\mathrm{O}} \tag{1.82}$$

$$I_{\mathrm{pot}} = \frac{V_{\mathrm{O}}}{R_{\mathrm{pot}}} \tag{1.83}$$

$$P_{\mathrm{pot}} = V_{\mathrm{pot}} I_{\mathrm{pot}} \ . \tag{1.84}$$

In this case the quantities are consider as constant, so the RMS values of voltage and current are not useful for the power calculation, on the contrary with respect to the previous cases[23].

In Figure 1.38 the output voltage is reported for different position of the control potentiometer. it is evident that the transistor Q_1 is always turned on, since the maximum voltage at the output is approximately equal to the input one minus a diode drop, which is the drop across the emitter base junction. When the potentiometer middle tap is below a certain voltage the transistor Q_2 is off and the feedback loop is broken so that the voltage is constant at the maximum output. When the potentiometer central tap reaches a voltage which is approximately one diode drop above the zener diode voltage V_{Z}, Q_2 is switched on and the output voltage approximately follows an inverse linear relation versus the potentiometer position.

$$V_{\mathrm{O}} \approx a + \frac{b}{x} \tag{1.85}$$

[23]Namely, for time-constant signal the RMS value coincide with the value of the signal itself. In the present case: $v_{\mathrm{pot}}^{\mathrm{RMS}} = v_{\mathrm{pot}} = const.$ (same for the current).

In Figure 1.39 the simulated current curve is reported, superimposed to the

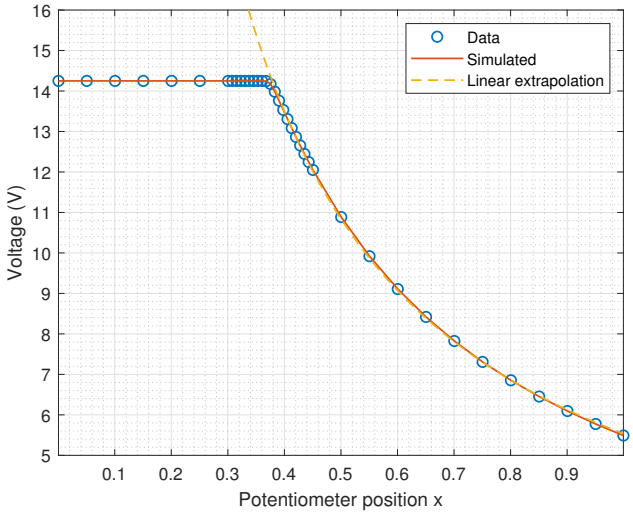


Figure 1.38: Output voltage v_O for the DC voltage regulator in Figure 1.37 traced varying the potentiometer position.

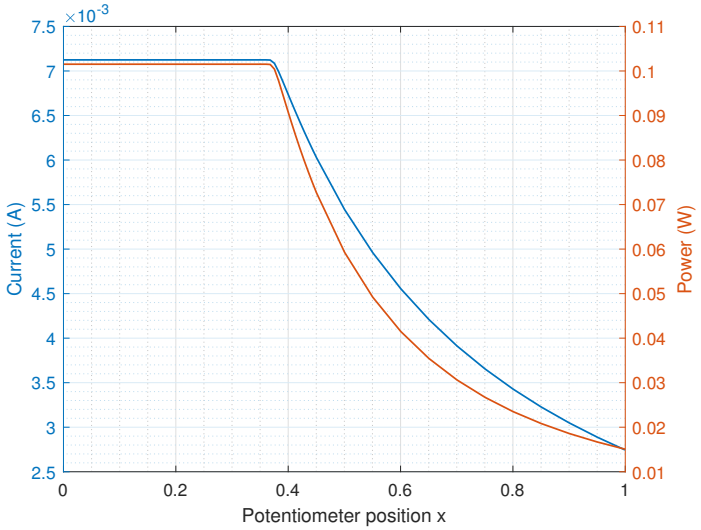


Figure 1.39: Potentiometer current i_{POT} and dissipated power p_{POT}, for the DC voltage regulator in Figure 1.37 traced varying the potentiometer position.

dissipated power. Since the current is derived from the voltage by means of a constant factor (potentiometer resistance), the trends of the curves are the same. This does not hold for the power curve, which, being the product of the two, shows

a different curvature:

$$\begin{cases} V_{\text{pot}} \approx a + \dfrac{b}{x} \\ \\ I_{\text{pot}} \approx \dfrac{\left(a + \dfrac{b}{x}\right)}{R_{\text{pot}}} \end{cases} \qquad \Longrightarrow \qquad P_{\text{pot}} \approx \frac{\left(a + \dfrac{b}{x}\right)^2}{R_{\text{pot}}} \ ,$$

it is clear that the higher curvature of the power curve is due to the higher order of the rational function that appears in the power expression.

1.2 Oscillators

Oscillator circuits are embedded in many electronics design since they are needed in every situation a timing of some sort is required. Not only in the obvious case of function generators, but also in a large number of different circumstances, as in case of instrumentation devices (*e.g.* oscilloscopes, frequency counter), oscillators are at the core of the functioning principle of the device. This made the knowledge on this family of circuit very wide, making very difficult to choose some representative case to be presented here.

It is evident that, because of their ubiquity, the discussion of a substitution of the traditional analog potentiometer with more flexible digital devices is of absolute interest.

In literature there is a very large number of circuits that provide an oscillation of some sort (*i.e. periodic output wave*). Some classifications can be made based on the type of oscillation provided, for instance, discriminating the shapes of the output waveform (*e.g.* square, sine, sawtooth, *ecc.*) or looking at the frequency band of the circuit (*e.g.* LFO, RF oscillator, *ecc.*). The subdivision used in this text is based on the mechanism that provide the oscillation itself. For example, a family of oscillator circuit exploits the charging and discharging properties of a reactive element (*relaxation oscillator*), another one is based on the usage of a positive feedback of a properly phase shifted signal back to the input of an amplifier (*phase-shift oscillator*). Also digital system are well presented in this field of electronics with interesting solutions, as well as design which involves piezoelectric material, in particular crystal element (*crystal oscillator*).

To begin with, a fairly simple relaxation oscillator is presented. Then a more conceptually complicated circuit, the *Wien-bridge* oscillator, is commented, both because its capital importance in electronics history and its impressive performances despite its apparent simplicity. Another particular case of phase-shift solution is then presented to give an idea of the variety of possible circuit derived from the same idea.

Furthermore, a look at the digital implementation of various kind of waveform generators (*e.g.* PWM) is not discussed here, since often, in that type of circuit, some sort of microcontroller is involved, making the direct implementation of digital potentiometer less powerful compared to the complete mastery of the firmware development. Also crystal oscillator are not discussed, despite their importance, since typically the frequency of the oscillation produced is not made variable directly acting on the core crystal circuit (which is fixed at a specific f_0 by the type of the crystal involved), but making use of PLL or other circuit which can divide or multiply that fixed frequency.

1.2.1 Relaxation oscillator

The relaxation oscillators have, generally, the advantages of a good level of simplicity and a low cost. Clearly they show some drawbacks at a practical implementation: their frequency behaviour is not well predictable[24], and in general they are not as precise as requested by some application. The working principle of a relaxation

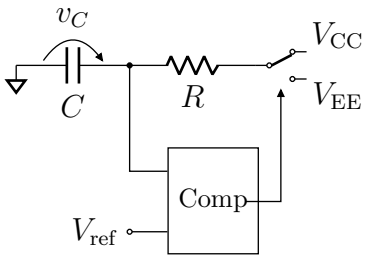


Figure 1.40: Principle schematic of a relaxation oscillator.

oscillator is schematised in Figure 1.40. The idea is that, at the time instant $t = 0$, the switch is in the position shown and the capacitor C charges through resistor R with a time constant $\tau = RC$. when the voltage across the capacitor reaches the level V_{ref} the comparator makes the switch to commutate, so that, if $V_{\text{EE}} = -V_{\text{CC}}$, the capacitor is now discharged. The hysteresis needed in the comparator block in order to have a capacitor voltage that swings in an appropriate interval is generated in a very simple way, also solving the problem of having a switch and an actuator: all this stuff can be solved with the usage of a single op-amp. When the supply is turned on, the op-amp output is forced either to V_{OH} or V_{OL} so that the voltage v_{sq} is forced either to an high or low voltage. Keeping in mind that an op-amp in saturation condition can be modelled as a voltage source (as seen in the previous

[24]Especially in cases in which integrated *Schmitt trigger* devices are used, because they have thresholds with large tolerances.

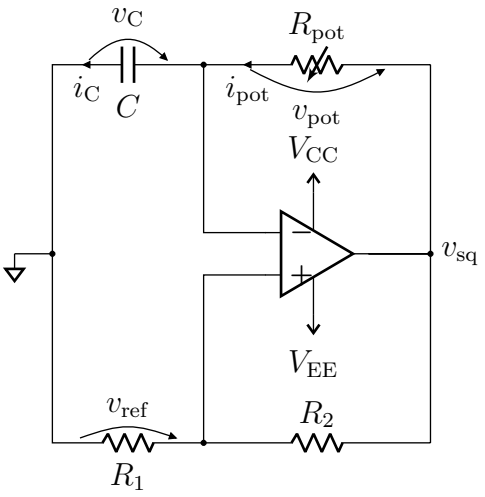


Figure 1.41: Op-amp (comparator) based schematic of a simple relaxation oscillator.

chapter), it is possible to see that the capacitor C will start to charge (if an initial positive saturation is assumed). This implies that the voltage v_C increases while, on the other branch, the voltage v_{ref} remains constant at a voltage determined by the voltage divider formed by R_1 and R_2. In this situation v_{ref} is positive and v_C is lower, since it is increasing starting from a null voltage; this maintains the op-amp output at the positive saturation level. When $v_C = v_{ref}$ the comparator switches its output to the negative saturation voltage so that, now, the capacitor discharges and the reference voltage sign is negative (with the same magnitude). From here the oscillation is stationary and the period is ideally stable. A simple proof leads to the expression of the period of oscillation.

Consider the stationary condition. The semi-period in which the capacitor discharges corresponds to an exponential decrease of the voltage v_C, which, in general, can be expressed as:

$$v_C = v_\infty - (v_\infty - v_0)\, e^{-t/\tau} \ . \tag{1.86}$$

In this case, the initial voltage of the decreasing exponential $v_0 = v_C(t = 0)$ is the reference voltage when the output of the comparator is at the positive saturation level v_{ref}^{up}. The limit value, for $t \to \infty$, v_∞ is the output voltage v_{sq}, which, being in the discharging phase, is the negative saturation level V_{OL}. The time constant of the exponential is clearly given by the product of capacitance and resistance: $\tau = R_{pot}C$. Substituting these values into Eq.1.86, the following expression is written:

$$v_C = V_{OL} - (V_{OL} - v_{ref}^{up})\, e^{-t/\tau} \ . \tag{1.87}$$

Now, consider the time instant in which the exponential will reach the $v_{\text{ref}}^{\text{dwn}}$ voltage, in which the comparator will commutate on the positive level again. This interval is exactly half of a period and it can be easily found by inverting the latter expression:

$$v_{\text{ref}}^{\text{dwn}} = V_{\text{OL}} - (V_{\text{OL}} - v_{\text{ref}}^{\text{up}})\, e^{-T/2\tau}$$

$$\frac{V_{\text{OL}} - v_{\text{ref}}^{\text{dwn}}}{V_{\text{OL}} - v_{\text{ref}}^{\text{up}}} = e^{-T/2\tau} \ .$$

The logarithm properties leads to a final general expression for the period of the oscillation:

$$T = 2\tau \ln\left[\frac{V_{\text{OL}} - v_{\text{ref}}^{\text{up}}}{V_{\text{OL}} - v_{\text{ref}}^{\text{dwn}}}\right] \ . \tag{1.88}$$

This is a general expression which can be simplified considering some common assumption which can be easily matched. To begin with, consider the to saturation levels of the comparator as equal in absolute values: $V_{\text{OL}} = -V_{\text{OH}}$. Also, it is useful to express the reference voltages as functions of the output voltage, through the voltage divider formed by R_1 and R_2. Putting these definitions together, Eq.1.88 can be rewritten as follow, and then further simplified exploiting some algebraic steps:

$$T = 2\tau \ln\left[\frac{-V_{\text{OH}} - \dfrac{R_1}{R_1+R_2}V_{\text{OH}}}{-V_{\text{OH}} + \dfrac{R_1}{R_1+R_2}V_{\text{OH}}}\right] = 2\tau \ln\left[\frac{1 + \dfrac{R_1}{R_1+R_2}}{1 - \dfrac{R_1}{R_1+R_2}}\right] =$$

$$= 2\tau \ln\left[1 + 2\frac{R_1}{R_2}\right] \ . \tag{1.89}$$

A further common assumption is that the voltage divider is designed to generate a reference voltage which is half the output voltage. This implies that the two resistance R_1 and R_2 are equal, so that the expression of the period will simplify further as:

$$T = 2RC \ln(3) \approx 2.2RC \ . \tag{1.90}$$

The waveforms involved in these computations are reported in Figure 1.42, where the oscillation of v_{C} across the capacitor is plotted for a period and a half, in stationary condition. The important voltage level are traced, so that the $[v_{\text{ref}}^{\text{dwn}}$ to $v_{\text{ref}}^{\text{up}}]$ range is visible. The discharging phases of the capacitor are plotted in blue, while the charging phases are in red; also, the extrapolation of the charging and discharging exponentials have been reported with the dotted trace. Since the v_{C} voltage changes

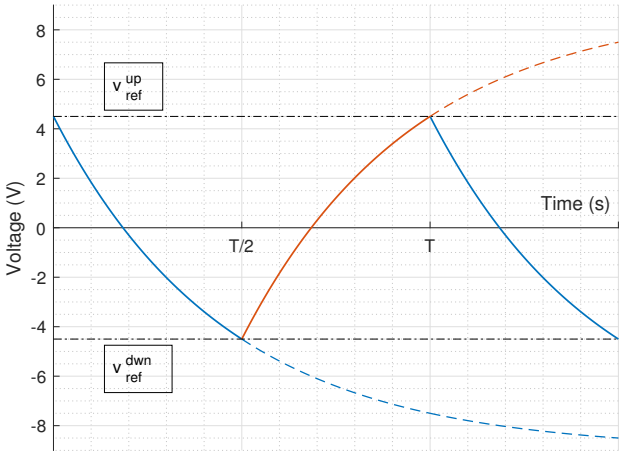


Figure 1.42: v_C oscillation for the circuit in Figure 1.41, under the assumption discussed above: $V_{OL} = -V_{OH}$ and $R_1 = R_2$.

direction every semi-period, the latter are just mathematical extrapolation plotted for sake of clarity.

In the next graph, Figure 1.43, the output voltage v_{sq} of the oscillator is reported. As expected this voltage swings between larger voltage limits, since the comparator forces its output at the highest or lowest voltage possible for a certain supply.

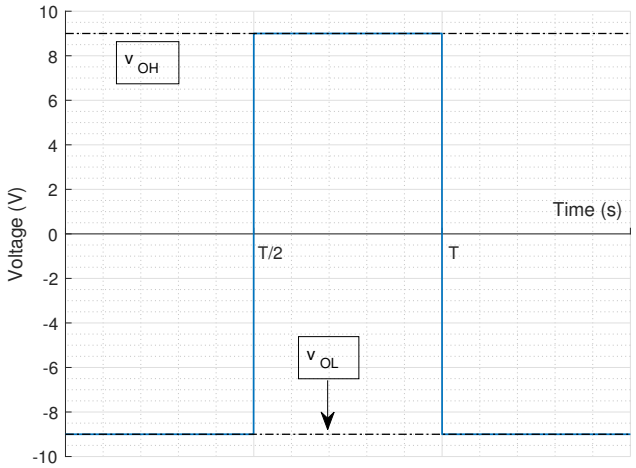


Figure 1.43: Output voltage v_{sq} oscillation for the circuit in Figure 1.41, under the assumption discussed above: $V_{OL} = -V_{OH}$ and $R_1 = R_2$.

Looking at Eq.1.89, different ways to control the period (namely the frequency) can be identified. Usually the possibility of varying the capacitance is discarded, since variable capacitor are expensive, huge and they offer a more restricted range of variability. Substantially, the resistor R, in series with the cap, is a good candidate and normally is the solution implemented, since a simple potentiometer connected as a variable resistor works fine here. Sometime, a selector is inserted in order to make possible to choose different values of capacitance and making available different consecutive ranges of frequency. In Figure 1.44 there is a graph showing the frequency of the output voltage versus the resistance R. Because the period of oscillation is directly proportional to the time constant τ, the relation between frequency and resistance is inverse linear $f(x) = 1/x$.

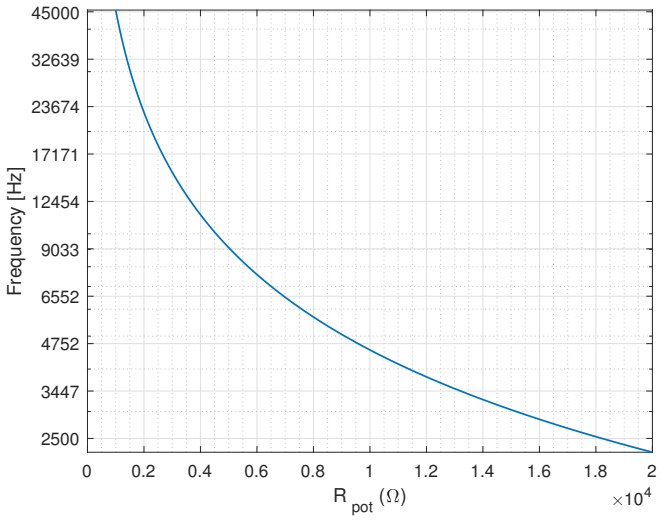


Figure 1.44: Frequency of oscillation plotted against the potentiometer resistance.

Another interesting consideration is related again to the expressions of the period in Eq.1.89. The shape of the exponential is controlled by the time constant τ, while the frequency itself can be controlled both by τ and the ratio R_1/R_2. To begin with, consider a specific region of the graph in Figure 1.43, *e.g.* the first semi-period. Supposing to increase τ (increasing R_{pot}), so that the shape of the exponential around that specific area previously considered approximates a line, this would increase the period, because of the τ increment, but the period of oscillation can be made equal to the initial case by simply rescaling properly the voltage reference of the comparator through the ratio R_1/R_2. In Figure 1.45 the voltage across the capacitor is reported for different combinations of R and R_1, so that the output frequency is constant at 1 kHz. Notice the different slopes of the exponential, for different values of R_1. This solution makes possible to exploit the circuit to actually

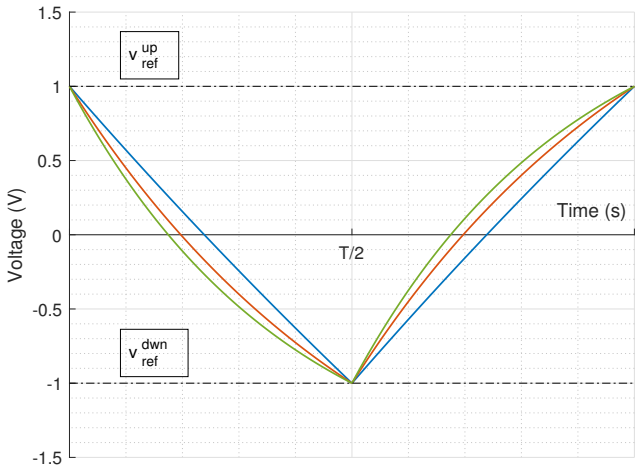


Figure 1.45: v_C plot normalised to the corresponding absolute values of the reference voltage, for different choices of the values pair (R_{pot} and R_1) that give the same output frequency. In blue $R_{pot} = 274.24\,k\Omega$ and $R_1 = 1\,k\Omega$, in red $R_{pot} = 57.21\,k\Omega$ and $R_1 = 6.982\,k\Omega$, in green $R_{pot} = 39.034\,k\Omega$ and $R_1 = 13\,k\Omega$.

generate two different waveform at a time: a square-wave at the comparators output and a triangle-wave at the capacitor terminals. Furthermore, the square-wave output has a fixed amplitude, due to the fact that, at every commutation, the op-amps output is forced always at the same levels, while the triangular wave has a different amplitude because the latter is nothing but the upper and lower reference voltage difference (which in this case are varying to maintain the triangular shape). Another point is that the usage of the triangular output of the circuit has to be done through a buffer (or amplifier with high input impedance), in order to avoid a current loss from the flux that charges and discharges, each cycles, the capacitor.

In traditional implementation of the circuit, the varying amplitude of the triangular output is a problem because it is very difficult to think to a solution to make it stable at the external. In the world of digital potentiometer this situation can be solved by simply increasing the resources: one potentiometer is the main frequency controller (R_{pot} in the circuit of Figure 1.41), a second one is the one controlling the shape of the triangular output (replacing R_1) and a third *automatically* controls the gain of the buffer/amplifier after the triangular output. This is feasible because all the three potentiometers can be controlled simultaneously, and accordingly to each other, by the microcontroller, allowing the external user to only deal with one control (namely the frequency knob).

In Figure 1.46, the voltages across the frequency potentiometer (R_{pot}) and the *shape control* potentiometer are traced for two different pairs of R_{pot} and R_1

values[25].

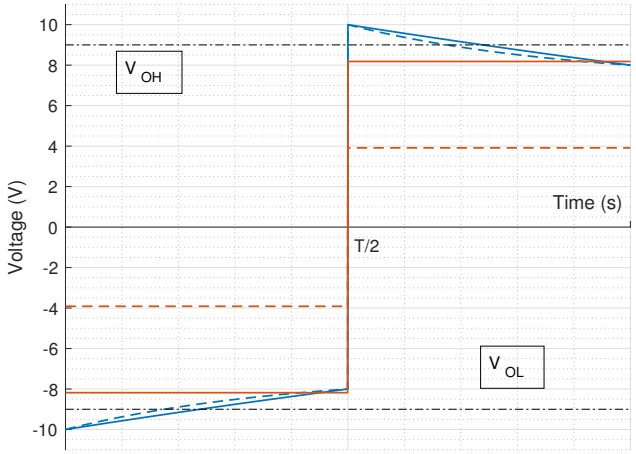


Figure 1.46: Potentiometer voltages: in blue $v_{\mathrm{R_{pot}}}$, in red $v_{\mathrm{R_1}}$. The solid traces refer to the values pair $R_{\mathrm{pot}} = 274.24\,\mathrm{k\Omega}$ and $R_1 = 1\,\mathrm{k\Omega}$, while the dotted ones refers to the choice $R_{\mathrm{pot}} = 39.034\,\mathrm{k\Omega}$ and $R_1 = 13\,\mathrm{k\Omega}$.

1.2.2 Phase-shift oscillator - *Wien bridge*

The Wien-bridge oscillator is a circuit which provides a sinusoidal output, based on a very different principle with respect to the relaxation circuit previously seen. In this circuit, the functioning principle is the usage of a feedback network around an amplifier, so that the *Barkhausen criteria* can be satisfied. Consider a circuit composed of a main amplifier block A and a feedback network β, as depicted below (Figure 1.47).

The *Barkhausen criteria* says that in order to make the circuit have a stable oscillation, the following conditions have to be satisfied.

- At $t = 0$, when the oscillation is not started yet, there's the trigger condition:

$$\begin{cases} |A(j\omega) \cdot \beta(j\omega)| > 1 \\ \arg\left[A(j\omega) \cdot \beta(j\omega)\right] = 0 \end{cases}$$

[25] One of them is a feasible choice, since it corresponds to a slope of the v_{C} exponential almost constant.

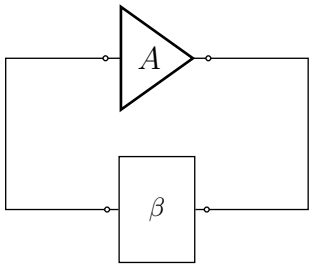


Figure 1.47: Op-amp (comparator) based schematic of a simple relaxation oscillator.

- In steady state condition, the following equations have to be satisfied:

$$\begin{cases} |A(j\omega) \cdot \beta(j\omega)|=1 \\ \arg\left[A(j\omega) \cdot \beta(j\omega)\right]=0 \end{cases}$$

The first set of conditions clearly comes from the fact that the system has to be unstable at the beginning, otherwise there would be no reason for the circuit to change its initial equilibrium state. Typically the temperature noise fluctuations are sufficient to trigger the oscillation, since for the unstable system, a minimal displacement from the initial state is sufficient to make it change state. When the oscillation is started the amplitude increases, but it has to be controlled in order to keep it stable henceforth. This implies that, typically, the amplification factor of the A block is reduced, in order to equal the losses in magnitude due to the feedback network at the oscillation frequency.

The following circuit is the *Wien bridge* oscillator, which uses an op-amp (in this case, but other solutions are feasible) with the non inverting feedback connected through the β network. The inverting feedback is connected with the usual voltage divider that is present in the non-inverting amplifier, providing the needed gain.

At this point the complication due to the change of constrains in the *Barkhausen criteria* for the amplitude of the closed loop gain arises. The lower resistor of the voltage divider is put in series with a JFET, which act as a variable resistor driven by a envelope generator, forming an automatic gain control (ACG) network. When the oscillation is not started yet both gate and source of the JFET are at the reference voltage, so that the control voltage is $v_{\mathrm{GS}} = 0$. Since the threshold voltage of the transistor is negative, a current flows into the drain making the resistance seen from the drain towards ground (R_{ch} resistance of the channel) low. Defining the resistance seen from the inverting input to ground $R_{\mathrm{x}} = v_{-}/I_{\mathrm{D}}$, the situation described above implies that $R_{\mathrm{x}} \approx R_{\mathrm{min}}$.

When the oscillation starts, the envelope network R_{D}, D_1, R_τ and C_τ make the voltage at the gate of the JFET to decrease, making v_{GS} to approach the threshold.

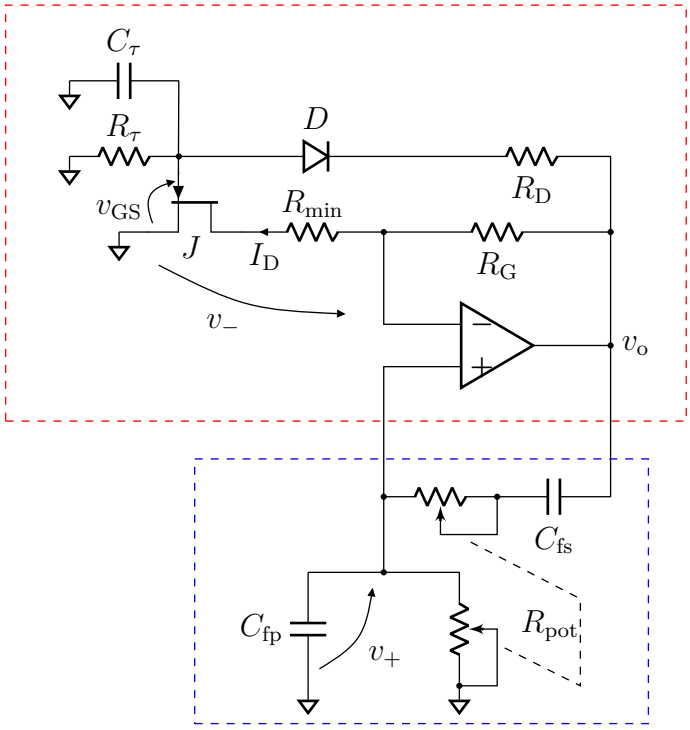


Figure 1.48: Op-amp based *Wien-bridge* oscillator with JFET based ACG. In the red box, the A block is pointed out (equipped to satisfy the *Barkhausen critiria*), in the blue box the β feedback network is shown.

This will reduce the current and so it will increase the channel resistance, reducing the gain of the non-inverting type feedback ($R_{\mathrm{x}} = R_{\min} + \underbrace{R_{\mathrm{ch}}}_{\text{large}}$).

The phase condition for the *Barkhausen criteria* can be expressed as follow. Consider also two normal and useful simplification: $C_{\mathrm{fs}} = C_{fp} = C$ and the equality of the two resistances of the dual gang potentiometer.

$$\angle\left[A(j\omega)\beta(j\omega)\right] = \angle\left\{\left(1+\frac{R_{\mathrm{G}}}{R_{\mathrm{x}}}\right)\left[\frac{\left(\frac{-j}{\omega C}\right) \parallel R_{\mathrm{pot}}}{\left(\frac{-j}{\omega C}\right) \parallel R_{\mathrm{pot}} + \left(\frac{-j}{\omega C}\right) + R_{\mathrm{pot}}}\right]\right\} =$$

$$= \angle\left\{\frac{j\omega R_{\mathrm{pot}} C}{\left(1-\omega^2 R_{\mathrm{pot}}^2 C^2\right) + 3j\omega R_{\mathrm{pot}} C}\right\} \tag{1.91}$$

The numerator is purely imaginary, so that its phase is $\pi/2$. The argument of the denominator is found using the arctangent, and the phase function approaches $\pi/2$ for frequencies that tend to zero, and $-\pi/2$ for the high frequencies range. This

means that there is a frequency for which the phase shift across the loop equals zero. This means that the imaginary part of the ratio in the latter expression is null. Without any calculation, it is sufficient to notice that, if the real part of the denominator vanishes, the resulting ratio is purely real:

$$\text{If} \quad \left(1 - \omega^2 R_{\text{pot}}^2 C^2\right) = 0 \quad \rightarrow \quad \angle\left[A(j\omega)\beta(j\omega)\right] = \angle\left[\frac{1}{3}\right] = 0 \tag{1.92}$$

The phase shift is null only for the oscillation frequency $f_0 = 1/2\pi RC$.

Looking at the magnitude *Bode diagram* of the transfer function of the β block (Figure 1.49), the attenuation of the network can be evaluated around -9.542 dB. If, in stationary condition, the amplifier will show exactly an opposite amplification factor, the oscillation can be sustained.

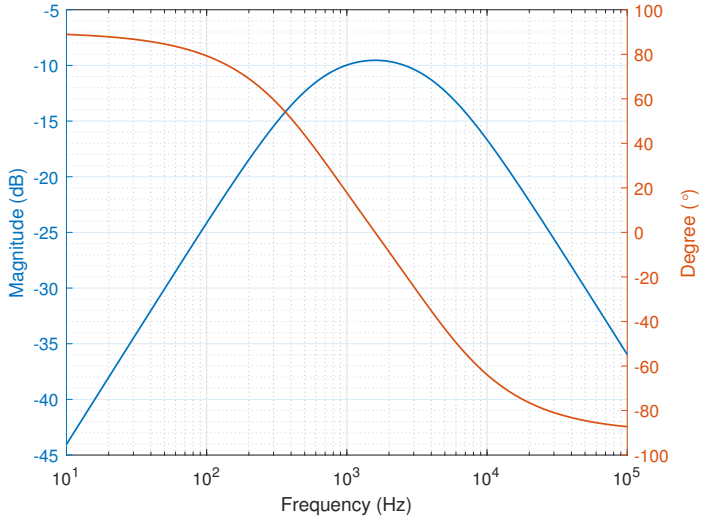


Figure 1.49: β positive feedback network transfer function bode plot. Notice the zero degree crossing point, for which the maximum of the magnitude curve reaches its maximum.

In reality, the ACG network has a delay response of some sort, in other words, the variation of the channel resistance due to a variation of the output amplitude takes some time to occur, as in every feedbacked system. This means that, even if the oscillation appears perfectly stable, the apparent stability is a dynamic equilibrium condition. Below, some important quantities in the wien-bridge oscillator are plotted: output voltage (Figure 1.51) and JFET channel resistance (Figure 1.50).

In Figure 1.50 the dotted line represents the mean values of resistance for $t \rightarrow 0$ (yellow) and after the trigger of the oscillation (red). The fact that these are mean values means that, as explained before, the equilibrium condition is dynamic. Notice also that the glitches in the trace are due to numeric issues: in practice the

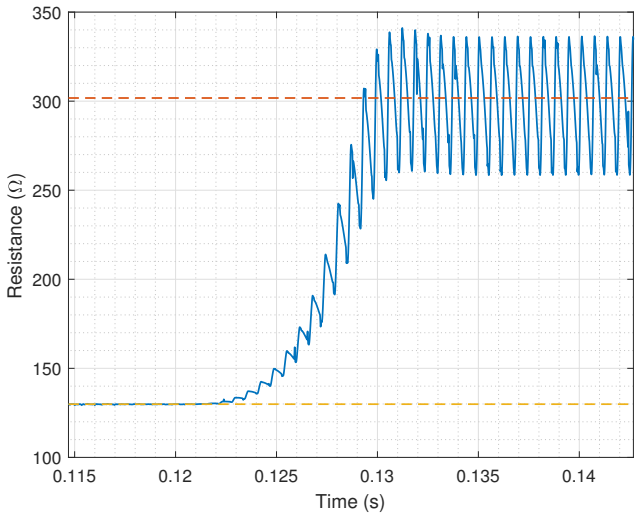


Figure 1.50: Channel resistance of the JFET, simulated for the period of time around the trigger of the oscillation.

resistance is calculated as a ratio of quantities that crosses the zero value almost simultaneously, and the ratio of such small quantities can lead to some glitches.

The *Barkhausen criteria* on the loop gain magnitude can be verified exploiting the values obtained with the simulation for the JFET channel resistance mean value

$$R_{\mathrm{x}} = R_{\mathrm{ch}} + R_{\mathrm{min}} = 301{,}8\Omega + 4700\Omega = 5001{,}8\Omega$$

$$A_{\mathrm{ol}} = 1 + \frac{R_{\mathrm{G}}}{R_{\mathrm{x}}} \approx 3 \approx 9.54 \text{ dB}$$

where A_{ol} is the gain of the non inverting amplifier. Consider the circuit in Figure 1.48 with the following values: $R_\tau = 4.7\,\mathrm{k\Omega}$, $R_{\mathrm{min}} = 4.7\,\mathrm{k\Omega}$, $R_{\mathrm{G}} = 10\,\mathrm{k\Omega}$, $R_{\mathrm{D}} = 560\,\Omega$, $R_{\mathrm{pot}} = 10\,\mathrm{k\Omega}$, $C_\tau = 470\,\mathrm{nF}$, $C_\tau = 470\,\mathrm{nF}$, $C_{\mathrm{fs}} = C_{\mathrm{fp}} = 10\,\mathrm{nF}$. For the diode the 1N4148 model has been used while the 2N3819 for the JFET and OP07 (with $V_{\mathrm{CC}} = 9\,\mathrm{V}$ single supply with virtual reference) have been considered for the active devices involved. With these values the output of the circuit is a sinusoidal wave of around 6.8 V peak to peak, whose zero level is referred to the virtual ground (4.5 V), and a total harmonic distortion THD = 1.198190%. The trigger transition is reported in Figure 1.51 The output voltage of the oscillator is a fairly good sine wave, as visible in Figure 1.51. The envelope of the oscillation is reported with the dotted lines above and below the output traces, making evident the initial exponential-like growth of the oscillation and then its damping accordingly to the parallel increase of the JFET channel resistance.

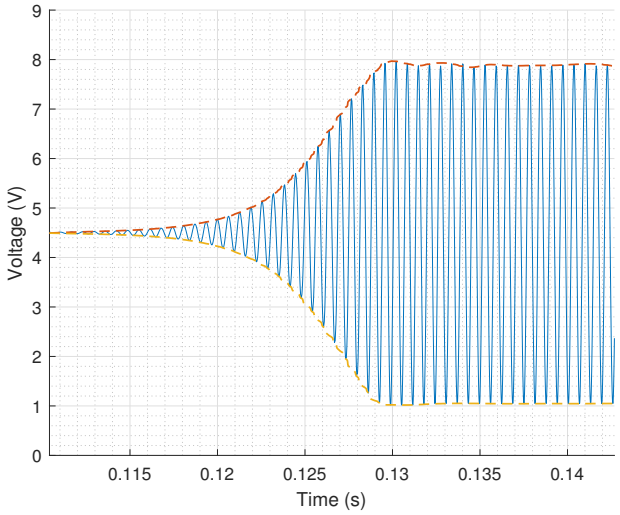


Figure 1.51: Output voltage of the *Wien-bridge* oscillator.

For what concerns the potentiometer, the situation is a little bit different from what seen till now. The β network time constant, given by the product $R_{\text{pot}}C$, has this form (for which the discussion above is valid) if the two resistances and the two capacitors are equal and this holds also when they vary. So, in traditional circuit, the capacitor were matched and placed as fixed capacitor, while the potentiometer implemented were a dual-gang type, so that the condition on the equality of the resistances were matched automatically for every position of the pot from the external (save for tolerances). In the case of digital potentiometer the situation is tackled by exploiting two digital pot (or more compact solution, *e.g.* two potentiometer in on package), driven appropriately by the microcontroller, so that the condition is matched via software easily.

As usual, the voltage (Figure 1.52) and current across each potentiometer are calculated. The voltages across the potentiometers are proportional to the output voltage, but since, at every frequency, the output amplitude is always the same, the voltages across the potentiometers are constant through their swings. This makes the current to follow a linear decrease with the increasing resistance. Hence the current plot is not interesting since it is derived simply from the voltage one through the Ohm's law. The current peak in steady-state condition is $I_{\text{peak}} = 0.161$ A.

1.2.3 Phase-shift oscillator - A different solution

In this subsection a different solution of a phase-shift oscillator is presented. In this circuit the amplifier block is implemented with a BJT common emitter stage, while

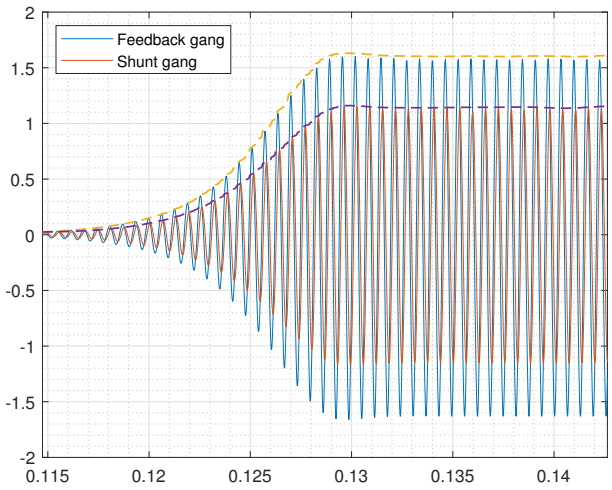


Figure 1.52: Potentiometer voltage for the wien-bridge oscillator. The two traces refer to the two gangs of the dual potentiometer.

the feedback network is formed with a cascade network of identical RC cells. The circuit is smaller than the *Wien-bridge*, since no automatic gain control is needed, but it is more complicated to investigate because of the interaction between the two blocks. This is because the input impedance of the amplifier in the *Wien-bridge* case is extremely high, while in the present solution the BJT base shows an impedance which usually is in the tens of kiloohm range. The input impedance is therefore interacting with the β network through a loading effect. Moreover, this loading effects go even further, since the input output impedances of each block interact with each other quantities and so the hand calculation implies necessarily some simplification, which have to be carefully discussed.

Without going too deep inside the functioning of the circuit of Figure 1.53, basically the RC cells network has a transfer function that introduce a phase rotation of totally 180°. This phase rotation has to be summed with the further rotation introduced by the inverting amplifier which is again 180°. This fact makes the circuit closed loop function satisfy the *Barkhausen criteria*, for what concerns the phase. The gain of the amplifier is then choose in order to satisfy the stationary condition requirements.

This non-ideality of the circuit causes its have poor performances, at least in the example chosen. The values reported are meant to build an LFO with a range of some hertz: $R_{\mathrm{C}} = 15\,\mathrm{k\Omega}$, $R_{\mathrm{f}} = 2.2\,\mathrm{M\Omega}$, $R_{\mathrm{s1}} = R_{\mathrm{s2}} = 220\,\mathrm{k\Omega}$, $C_1 = C_2 = C_3 = 1\,\mu\mathrm{F}$, while the potentiometer has to be a dual gang $100\,\mathrm{k\Omega}$. For the values reported, the output voltage is shown in: Figure 1.54. As visible, the output waveform is a

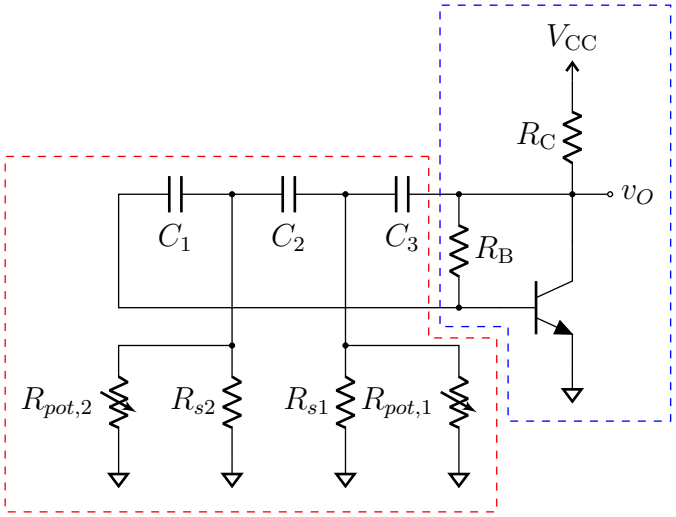


Figure 1.53: Common emitter BJT based *phase-shift* oscillator. In the blue box, the A block is pointed out, in the red box the β feedback network is shown.

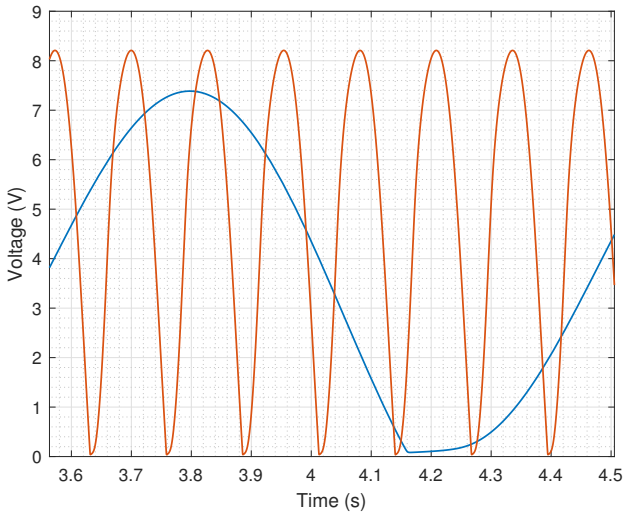


Figure 1.54: Output voltage of the phase-shift oscillator in Figure 1.53. The blue trace is the one obtained for the highest value of the potentiometer gangs resistances (100 kΩ), namely the lowest frequency. The red one is obtained for $R_{\mathrm{pot},1} = R_{\mathrm{pot},2} = 0\,\Omega$.

distorted sine shape function. The highest and lowest possible frequencies waves, obtainable with the values listed earlier on (respectively at 1.1 Hz and 7.9 Hz), have similar shapes. Even if they look similar the total harmonic distortion calculation points out that the wave with higher frequency is more distorted than the slowest:

$\text{THD}_{\text{low}} = 6.15\%$, $\text{THD}_{\text{high}} = 20.70\%$. Also, the fact that the high frequencies waves have a larger peak to peak value, hence the peaks of the waves are closer to the interdiction and saturation boundaries for the BJT, contributes to this behaviour of the THD.

In Figure 1.55 the FFT simulation results are reported for the to limiting cases.

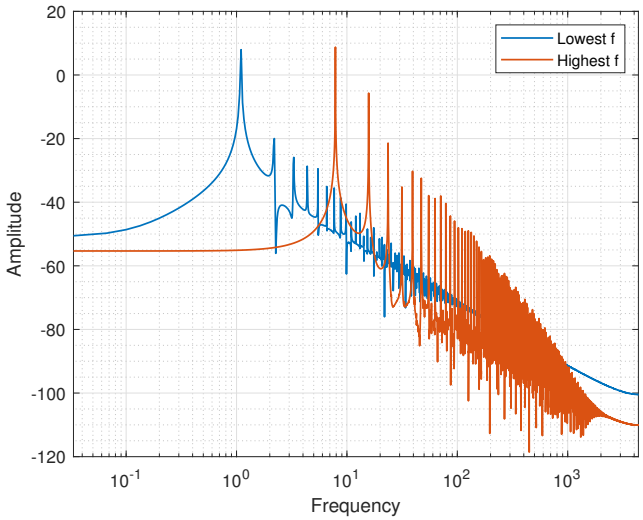


Figure 1.55: Output voltage of the wien-bridge oscillator.

The voltages across the gangs of the potentiometer are difficult to derive mathematically, since they are different, being the two gangs connected to different cells of the β network. The amplitude of the waves across each gang varies going from 0 V, when the potentiometer is turned to the highest frequency position, up to a maximum value, when the potentiometer is turned the other way. As visible in Figure 1.56, the wave peak to peak value across $R_{\text{pot},1}$ is around 2.6 V, while for $R_{\text{pot},2}$ is around 835 mV, at the same frequency of the output voltage and centred around 0 V since they are decoupled from the BJT stage.

The fact that the gang of the two which is closer to the base sustains a lower peak to peak voltage comes from the fact that the β network attenuates the signal magnitude going from one cell to the next one, whilst it also rotates its phase.

1.3 A note on passive network and other noticeable circuits

To end this chapter, a final brief look at the passive network is done, because of its possible relevance in the following of the text. Passive networks of resistive and

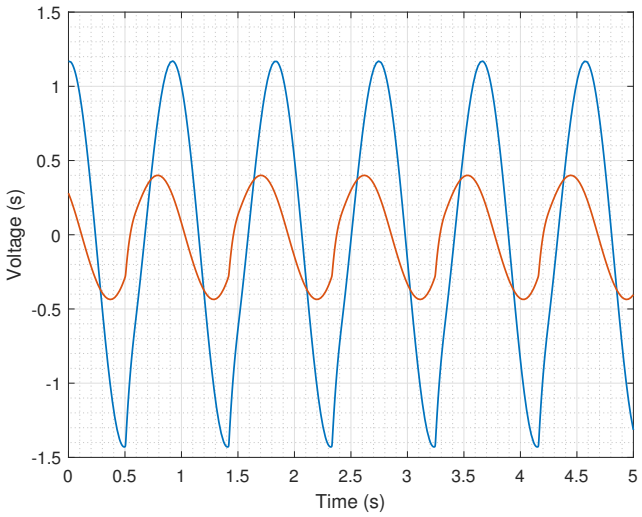


Figure 1.56: Dual gang potentiometer voltage for the phase shift oscillator in Figure 1.53. The blue line refers to the potentiometer gang closer to the BJT collector, so after the first β cell. The red trace is the one of the second gang, closer to the BJT base, after the second cell.

reactive elements are common in electronics and they usually accomplish signal manipulation tasks. A common example of this is the *volume control* potentiometer, set as a simple voltage divider between the signal source and the reference. From its simplicity, it appears clear that a complete analysis to find the voltage and current ranges across the potentiometer is unnecessary. Generalising to any resistive network, the implementation of this circuits with digital potentiometer usually does not present the need of any particular design, since being them passive the voltages inside the network do not exceed the limit of the input signal. In other words, the voltage across each terminal of each potentiometers is smaller than the one at the input of the network. This does not mean that is easy to predict what are the voltage and current ranges for a certain element of the network (it depends on the network obviously), but that upper bound is easily predictable.

Other, especially in audio circuits, largely used passive networks are the *equalisation* blocks. The latter usually are subscribed to the filter family which often results to include active solution (with op-amps or transistors, consider, for example, the very famous *Baxandall equalisation control* in Figure 1.58) and since this fact, they can be treated in the same way of the amplifiers shown in the previous sections, from the potentiometer prospective at least. The only big difference in this case is that the frequency at which the calculation is done is extremely important: since they are filter networks, they are supposed to work differently at different frequencies, so the voltage across a potentiometer inside the network can vary significantly, passing from a particular frequency to another.

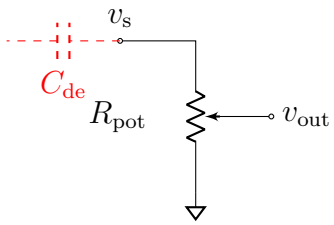


Figure 1.57: Common volume control solution implemented as a potentiometer voltage divider towards reference (in red, a possible decoupling capacitor is shown).

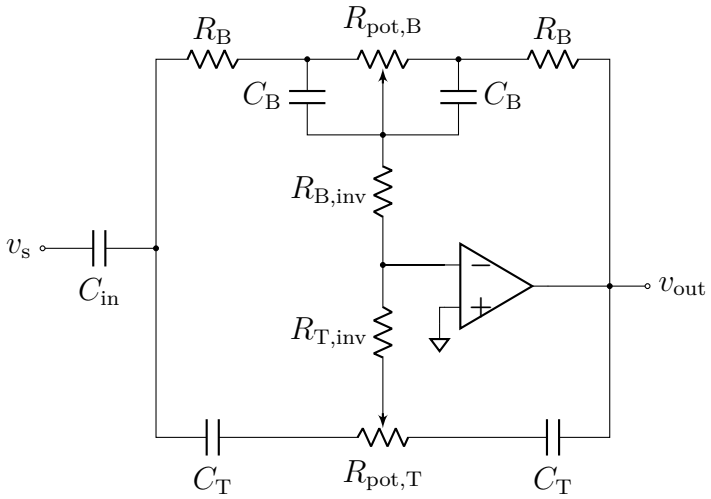


Figure 1.58: *Baxandall tone control.* This network is based on a negative feedback configuration, in which, comprehensive of the potentiometers, the passive network is put in the negative feedback of an op-amp (in this solution, but clearly not just op-amp solution can be implemented).

The latter warning is part of a generalisation for which an amplifier can be seen just as an active filter which, basically, affects (amplifies) any frequency in the same way, inside the band.

Also saturation effects can be treated in the same exact way seen for the amplifier.

Chapter 2

Voltage supply issue - possible solution

In the present chapter the supply related issues and possible solutions are presented as well as all the fundamental concept of digital potentiometer construction. To do this, a first presentation of the digital potentiometer is done, with a particular focus on the parameters which are fundamental in the discussion related to the powering. Moreover, the topics of non-idealities is presented, *e.g.* discussing the terminal resistances and capacitances. Then, to apply the above theory, a circuit design example is done considering a non-inverting operational amplifier circuit. This allows the discussion of the majority of the digital potentiometer integration design challenges.

2.1 The digital potentiometer - An overview

The digital potentiometer is a device that reproduces the behaviour of a traditional potentiometer exploiting a voltage divider constituted by a series of N equal resistors and a network of switches able to connect one node of the divider to the wiper external terminal of the device. The device is digital because, at the core, the switch network is controlled by a stream of bit which is unique for every node of the divider. In Figure 2.1 a possible generic block diagram of a digital potentiometer is shown. The resistor string can usually count a number of steps around 32 at least, up to 1024 elements. An immediate thing to notice about this block diagram is that this structure is exactly the one of a *resistor-string DAC* [4]. In fact the two devices have a lot in common at least from the conceptual point of view. In principle, in the DAC functioning, the resistor string is fed by a constant voltage and the output is the voltage at the node selected by the CMOS selector, through the wiper in a certain clock cycle. If the frequency of the output analog signal the

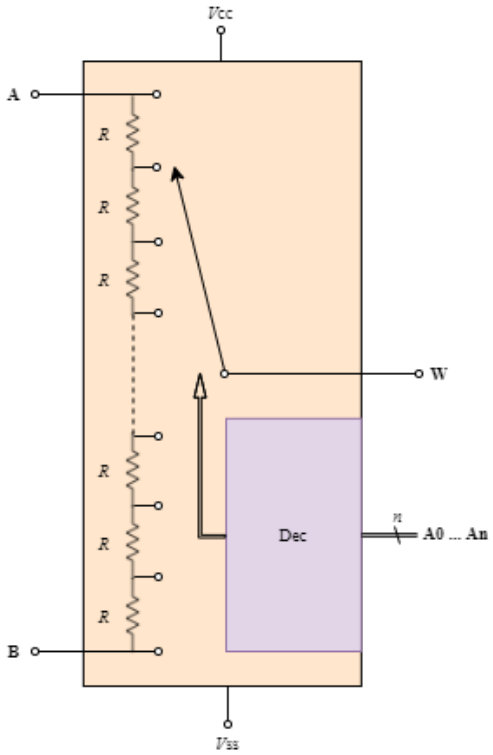


Figure 2.1: Most basic possible block diagram of a digital potentiometer.

DAC is producing is sufficiently lower than the clock one, the resulting waveform is sufficiently smooth. In the potentiometer implementation, the situation is in some sense "reversed": the device is crossed by the signal. In other way it's possible to say that in the DAC case the flux of information is going from the input digital stream, through the device, into the analog wiper output, whilst in the potentiometer, the flux of information is going from some of the resistor string terminals to another one (for instance from A, B to W, looking at Figure 2.1) and the CMOS network is just a control block.

This direct link between DAC and digital potentiometer is evident looking at some typical parameters of these devices, which results as common to both.

A first parameter whose introduction results completely natural is the *resolution* of the potentiometer. Still lying on a common semantic field to both the devices, the resolution is the number of distinct analog levels corresponding to the different digital words [5]. Sticking to the definition just given, sometimes the number of bits of the digital command is also used as resolution definition, in fact a simple logarithm function relates the apparently different definitions: $n = \log_2 N$. Concerning the potentiometer, the resolution is the number of possible position of the equivalent analog device and it is usually given as the number of bits in

the controlling code n. Independently on how the resolution can be defined, the resolution meaning is related to the number of resistors (and nodes) of the internal divider. The smallest voltage step that the potentiometer can resolve is given by the expression below.

$$v_{\mathrm{r}} = \frac{v_{\mathrm{A}} - v_{\mathrm{B}}}{N} \tag{2.1}$$

where v_{A} and v_{B} are the voltages of the A and B terminal of the potentiometer measured with respect to ground. Notice that the denominator is N since the top terminal of the first resistor and the lower terminal of the last resistor are used for the top and bottom connection A and B respectively.

For digital potentiometer, as well as for DAC (or ADC), some important error-related parameters are defined: *integral non-linearity* (INL) and *differential non-linearity* (DNL). Consider the DAC case because of the fact that its functioning offers a more intuitive basis for the explanation of the latter parameters. INL and DNL are linked to the concept of the function that relates the input code to the analog output voltage, which ideally would be a straight line. The INL is defined as the deviation of the output voltage from the theoretical one obtained for a certain input code [5]. Therefore, INL is a function of the code, but usually it is given as a single value which is the maximum of the INL function (Figure 2.3). The DNL is defined as the deviation in analog step sizes from the one theoretically obtained for a difference of one LSB (v_{r}). A visualisation of the DNL is shown in Figure 2.2.

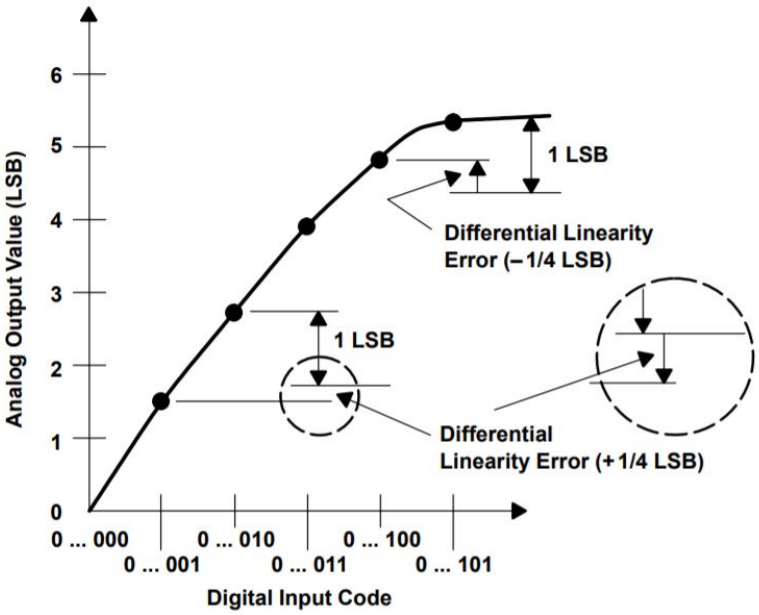


Figure 2.2: DAC DNL error representation [6].

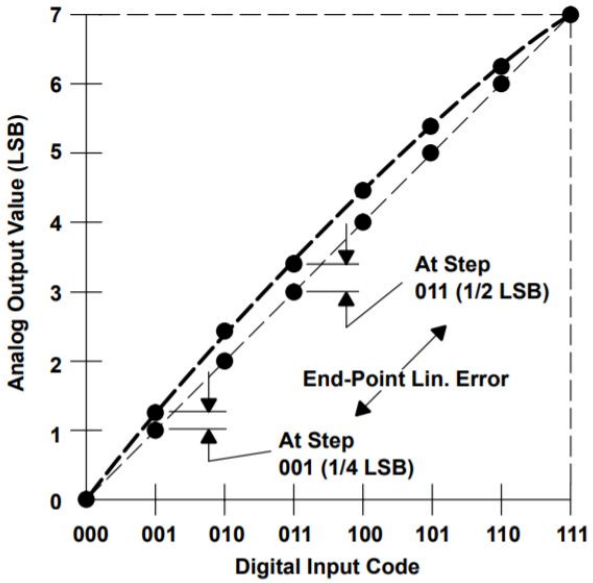


Figure 2.3: DAC INL error representation [6].

The straight line that describes the ideal behaviour can be defined as the line that connect the initial and final point of the characteristic or the one that fits the characteristic in the best way. The latter option appears as the most appropriate one in the digital potentiometer field, since in this situation the taper of the potentiometer (discussed later) can be different from linear. Related to the DNL, another parameter is introduced: the *monotonicity*. Since the DNL is a measure of how much, at a certain input code, the difference between the two consecutive output voltage deviates from the one corresponding to 1 LSB, if it results greater than 1 LSB the slope of the characteristic is no more unique. This means that there could be an input code for which a variation corresponding to an increase of the wiper voltage corresponds instead to a decrease.

Two others error can be identify as figure of merit of the digital potentiometers, even if they are more relevant for DAC applications, the *gain* and the *offset*. The offset error for a DAC is the difference between the actual output voltage an the theoretical one, specified at the null input code, usually the one that should refer to a 0 V output. in other words, it is not guaranteed that when the code is set to be de smallest value, also the output is null (Figure 2.4). For what concerns potentiometer application, in many cases, this error is not so important (and so it is often not reported in the datasheets) because it is normally much smaller than the absolute value of the potentiometer swing: the LSB order of magnitude. For example an offset of one LSB on a 256 steps potentiometer, with 1 V applied at its terminal is less the 4 mV (ł0.4%). Moreover, often the potentiometers control the

circuit through the ratio of the resistances realised on the two sides of the wiper, actually making the offset negligible.

The gain error "is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero" [6]. For the potentiometers (and the DAC) it is measure as the analog difference at full scale code. So it can be that the transfer function is not a perfect straight line, but it can undergoes a sort of "saturation effect" for which an input corresponding to the maximum code value does not result in the expected analog value (Figure 2.5).

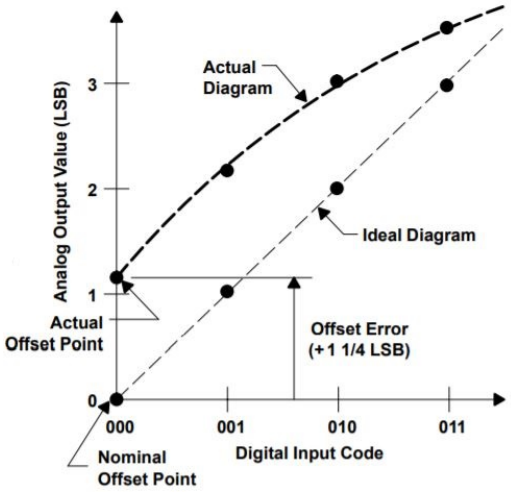


Figure 2.4: DAC offset error representation [6].

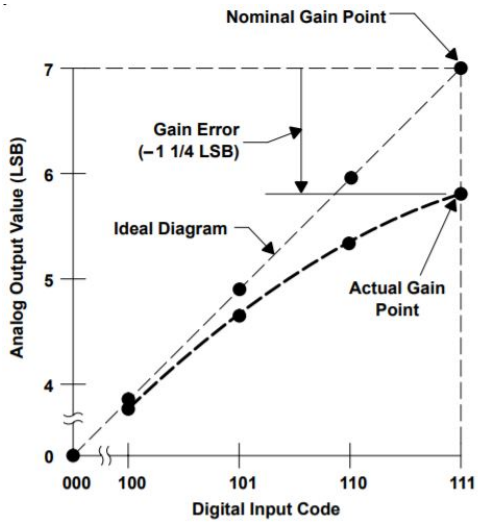


Figure 2.5: DAC gain error representation [6].

This errors on the characteristic are reflected directly on the voltages when the potentiometer is used. So it is evident that this parameters (reported in the datasheets) are fundamental.

A parameter which is always present in the digital potentiometer datasheets is the *nominal resistor tolerance*, defined as follow:

$$\epsilon_{TOL} = \frac{\Delta R_{\mathrm{AB}}}{R_{\mathrm{AB}}} \tag{2.2}$$

In Eq.2.2, ΔR_{AB} is the resistance measured between the two fixed terminals A and B, whilst R_{AB} is the nominal one. This parameter is usually quite high, *e.g.* between $\pm 20\%$ and $\pm 55\%$ [7] [8] [9], so it has consequences on the design of the circuit involving digital potentiometer[1]. In particular, this limitation on the R_{AB} is avoided trying to design circuit in which the quantity controlled by the potentiometer depends only on a ratio of resistances and not on their absolute value. This concept will be explained better in the following section when a design is presented. Related to the tolerance, in case of devices containing more than one potentiometer in the same package (dual, quad, *ecc.*) also the matching tolerance between each potentiometer in the same case is given. Usually this value is much lower than the tolerance on the absolute value of R_{AB}, *e.g.* 1% at maximum. But usually, this value is much lower than the single percentage point: around 0.1% or 0.2% [10] [8].

An important parameters always present in the digital potentiometer datasheet is the *resistance temperature coefficient*, Tem_{co}. This parameter indicates what is the percentage drift of the resistance for a variation in temperature of one degree (normally using Celsius degree unit). The lower is this coefficient, the more stable the potentiometer is for any variation of temperature, which can occur, obviously, for many reasons on electronic board (for instance at least because of the self eating phenomenon that affects every device). The Tem_{co} is a linear coefficient in the sense that it is referred to linear variations even if in reality the response is much more complicated and it would require a higher order polynomial fitting. In principle, it can be negative or positive, indicating a lowering or a rising of the R_{AB} resistance in presence of an increase of temperature. typically it is positive, between tens to hundreds of ppm/°C, but it can varies a lot with the potentiometer position assuming negative values, even if the typical one is positive. This is the case of the AD5243/AD5248 (Analog devices), for which the typical value is 35 ppm/°C, but the actual range is much more sever (Figure 2.6, Figure 2.7).

[1]This values of tolerance are common also for the analog potentiometer, so the considerations done for designing circuit controllable with ratio of resistances instead of absolute values holds also for the traditional design.

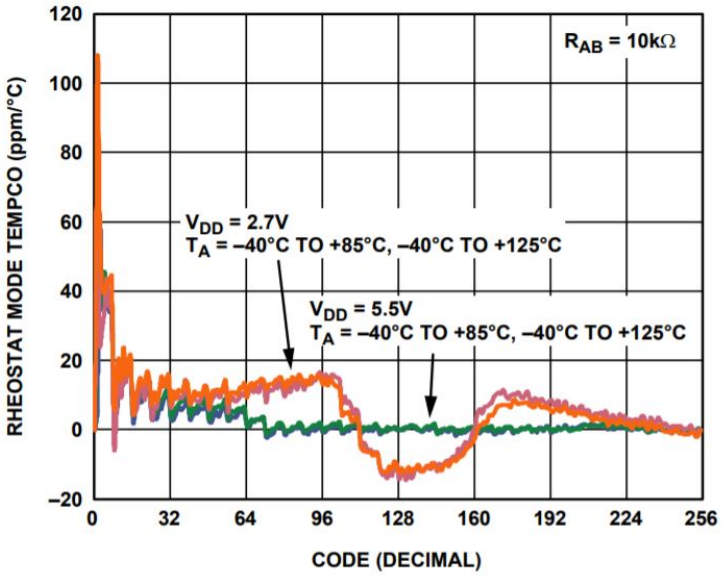


Figure 2.6: Temperature coefficient related to the potentiometer resistance R_{AB}, useful when the device is operating in the rheostat mode [9].

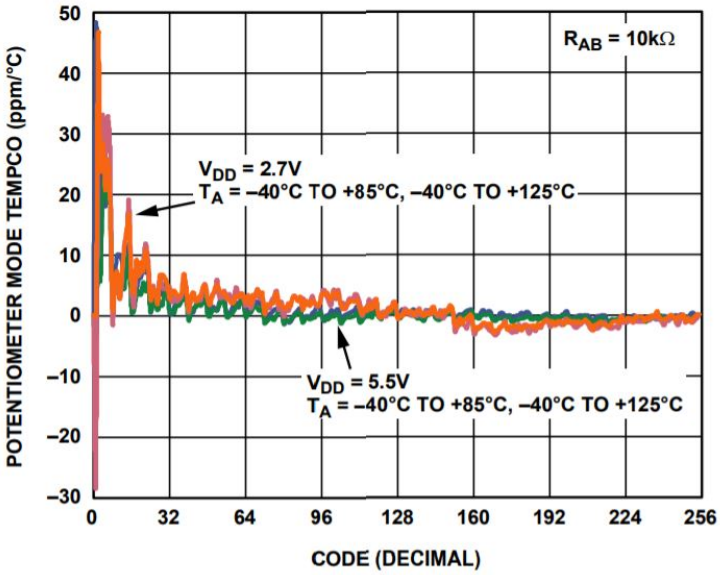


Figure 2.7: Temperature coefficient related to the voltage divider, useful when the device is operating in the potentiometer mode, in which the ratio of the upper and lower resistance of the divider is important [9].

Clearly, the devices considered are not ideal since they have connections and terminations that exhibit parasitic resistances and parasitic capacitances (usually parasitic inductances are negligible at a first level of approximation). In this prospective a circuital model of the digital potentiometer can be drawn and used in simulations to avoid the rising of bandwidth issues. All datasheets report the resistance and capacitance of each potentiometer terminal (this holds also for the digital input and output terminal of the device), so that the schematic in Figure 2.8 can be exploited.

Each terminal A, B, W is loaded with a capacitance towards ground, a series resistance and a series inductance. The impact of each parasitic element is very different from the other ones because they rise from different phenomena. In particular, a first source of parasitic effects, which can not be avoided is the bonding wire system that links the pad on the die to the lead of the package, allowing the access to the circuit itself from the external. The bonding wires are typically a source of series inductance and series resistance, since the usually have a low diameter over length ratio. The effects of parasitic inductances usually impact the performances at high frequencies, because of their interaction with the current spikes due to commutation in the digital circuit. However, in the context of digital potentiometers, the parasitic inductance of the terminal is not influential, since the bandwidth of the devices is limited by the parasitic capacitance and resistance well before the rise of the inductance's effect.

The parasitic capacitance and resistance of the terminals are much more effective since they are primarily due not to the bonding system but to the intrinsic architecture of the potentiometer circuit. Consider the wiper, ideally it is connected always (no matter the position of the ideal potentiometer) to a node of the resistor divider string. The selector is constituted by a series of many transmission gate, each connected to a node and to the wiper, so that a decoder on the digital input command can close one transmission gate at a time. So, the major contribution to the wiper resistance is in effect given by the on-state resistance of the transmission gate. These gates are required in order to ensure a good analog behaviour of the potentiometer, since the signal has to be transferred properly in both directions and with any level inside the permissible range. The R_{ON} resistance leads to a value for the wiper resistance which usually varies between $70\,\Omega$ and $400\,\Omega$. The resistances of the other two terminals is usually a little bit lower but it is in the same range of values. This is because the potentiometers usually have some additional functions such as the possibility to isolate and disconnect the terminals, hence some other switches are present also between the ideal digital potentiometer fix terminals and the external connection.

A first approximated yet powerful set of parasitic elements also include the capacitances shown by the terminals. They are given by the capacitance of the lead areas involved in the bonding system, but mostly by the junction capacitances

of the gates inside the chip. Their value is usually between 30 pF and 120 pF.

The combined effect of the parasitic limits the bandwidth of the device. The −3 dB bandwidth is usually at least of some tens of kilohertz up to the megahertz range. In any case, the BW is usually way more than sufficient for audio application whilst it is not even closer to the radio frequency field, from which, not coincidentally, the digital potentiometers are substantially excluded.

To complete the non-idealities of the terminals, also the leakage current at each of them is given in the datasheets. This current is usually much lower with respect to the one related to the analog signals involved, *e.g.* a few nanoampere.

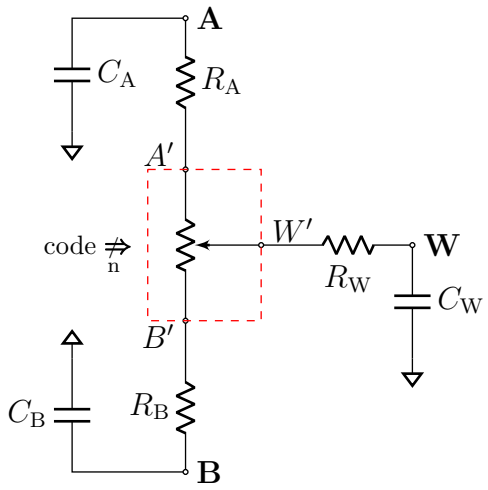


Figure 2.8: Digital potentiometer model that includes for each terminal a parasitic resistance and a parasitic capacitance. In the red dotted box, the ideal digitally controlled potentiometer is pointed out.

A very important aspect of the potentiometers which has a huge impact on the design is their supply. As any other active device the digital potentiometer has to be supplied with the right voltage (which must have a sufficient current capability). Based on the following aspect potentiometers are divided into two species: a "traditional" one and a "high swing" category. In the usual digital potentiometer, the analog voltage at the terminal has to be confined into the device supply, *e.g.* 0 V to V_{DD} or V_{SS} to V_{DD}. The high swing category includes potentiometers that have a more sophisticated switching network, able to let the resistor string work at a voltage which is independent from the digital supply. This means, for instance, that the analog signals at the potentiometer terminals can range from ±18 V while the device is supplied with a standard 0 V to 5 V range. An example can be the case of the MCP41HVX1 (Microchip): the analog voltage at the terminals (V_A, V_B, V_W) can swing inside the analog supply rails (from V_{EE} to V_{CC}) and these rails can

be an high ±18 V while the digital supply is in the range from from 2.7 V to 5.5 V and can be centred at any level inside the analog supply. This fact will result as one of the important aspect to be considered when an analog circuit is converted from analog to digital control.

Also, as for any digital circuit, the protocol and timing characteristics of the device are reported. The discussion of these parameters is not performed here, since they exceed the purpose of this text. It is sufficient to notice that, almost all the commercialised devices communicate via a I^2C or via an SPI protocol. Still the switching time between one position and another one is important in the following of the essay. This is usually in the range of a few hundreds of nanoseconds up to a few microseconds. T

he potentiometers are evolving continuously and many of the contemporary devices exhibit additional functionalities. One of the improvements is related to the possibility of storing and in general managing in a more complicated way the digital external command. This fact is directly linked to the possibility of including embedded memories inside the potentiometer chip so that the device can be programmed, without exploiting only the controller capabilities. For example, the AD5232 offers two potentiometers in one package, which can work each with its own memory (EEMEMx block), so that when a certain position is given by the controller (through the serial interface), the setting can be stored into the corresponding memory "executing an EEMEM save operation". This setting will be automatically loaded into the RDACx register at the device power-on. In Figure 2.9 the block diagram of the AD5232 is reported.

Another interesting possibility made available in many digital potentiometers is the shutdown command. Commonly denoted by $\overline{\text{SHDN}}$, is an active low asynchronous signal which disconnect the A terminal and connect the wiper W to the terminal B, without changing the content of the register RDAC that normally controls the position of the potentiometer. This feature will by of particular interest in the following of the thesis.

2.2 Potentiometers supply

Each digital potentiometer, whether high swing or not, needs to be supplied in the correct way. The values required are reported into the datasheet in terms of a permissible range of values according to the different working modalities of the device. Hence, a supply network is required and it has to be always evaluated on the basis of some figures of merit, first of all its output voltage stability with respect to the variation of input voltage or output current. The stability with respect to the output current is related to the capability of the circuit of not suffering of loading effect when a circuit is actually supplied by the voltage source circuit involved.

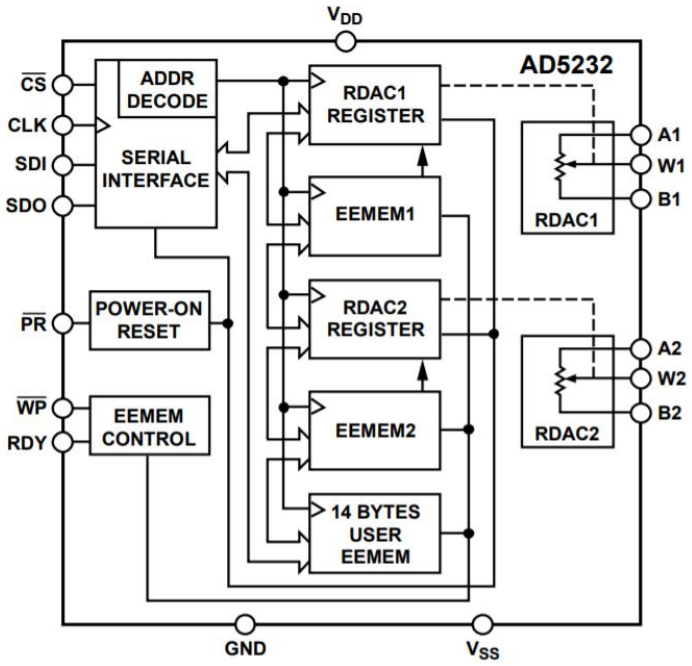


Figure 2.9: AD5232 functional block diagram.

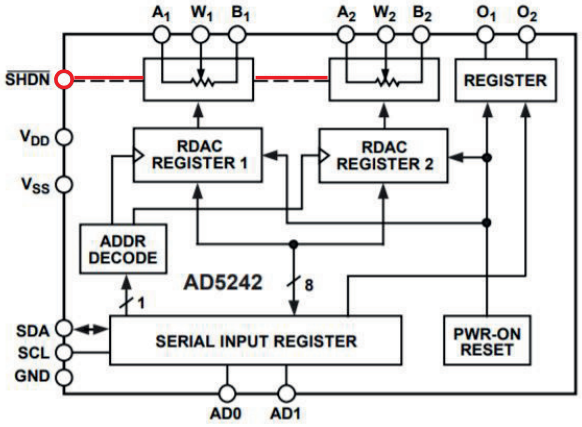


Figure 2.10: AD5242 functional block diagram, with the $\overline{\text{SHDN}}$ input pointed out in red.

This aspect can be evaluated with the calculation of the output impedance of the circuit.

Being the supply discussed a voltage source, its *Thévenin equivalent* circuit can be calculated. From the latter it results evident that a loading effect is more heavy when the voltage partition induced by the divider formed by the Thévenin equivalent impedance (alias the output impedance) and the load is significant.

The rejection of the input voltage variation is more difficult to be evaluated and normally its study exploits simulations and direct measurements. Notice that, this parameter is usually given in decibel in the form of an attenuation, so that an ideal circuit would have infinite rejection, but on the contrary, in some cases, precisely the capability of "tracing" the input voltage can be desirable.

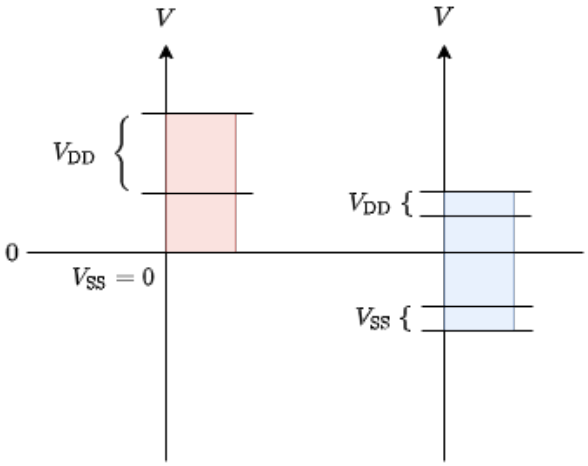


Figure 2.11: Logic representation of the single (left) or dual (right) supply functioning for the digital potentiometer. The curly brackets indicate the ranges of each level.

Many devices offer the possibility of a single or dual operation (see Figure 2.11), so that, in cases of not-high-swing potentiometers, the signals at the terminals can vary around 0 V or a fixed offset. If the potentiometer is operating in a single supply mode the signal has to be referred to a "virtual ground" V_{BB}: a voltage properly chosen and generated which is half of the V_{DD} voltage, in order to maximise the possible dynamic of the device. The permissible voltage range for the analog terminal is given referred to the supply levels[2] and from it, the virtual reference from the signal can be calculated. In the case of the AD5241/5242, for example, the permissible range is exactly from V_{SS} to V_{DD}, so that the following equation can be written:

$$V_{BB} = V_{SS} + \frac{V_{DD} - V_{SS}}{2} = \frac{V_{SS} + V_{DD}}{2} = \overline{(V_{SS}, V_{DD})} \tag{2.3}$$

The techniques used to generate the virtual reference voltage can be many, a simple solution is the one reported here (Figure 2.13). This solution has the advantage of generating a reference voltage which is continuously varying with the

[2]it is not guaranteed, that it is exactly the interval V_{SS} to V_{DD}, it could be less. Again, the datum is reported in every datasheet.

V_{DD} supply. This means that if, for any reason, the potentiometer undergoes a supply fluctuation, the reference of the signal will follow it, maintaining the correct relation between the signal reference itself and the potentiometer permissible swing at the terminals. In this scenario the decoupling of the DC component generated to make the potentiometer work correctly is mandatory, in order to not alter the operating point of other regions of the circuit. This holds unless the reference of the circuit itself is already elevated to a certain V_{BB}, for example in the case of single supplied operational amplifier based circuits.

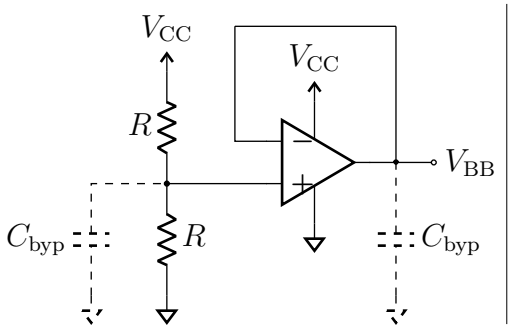


Figure 2.12: Virtual reference voltage generator. The dotted capacitors are usually inserted for a better frequency response.

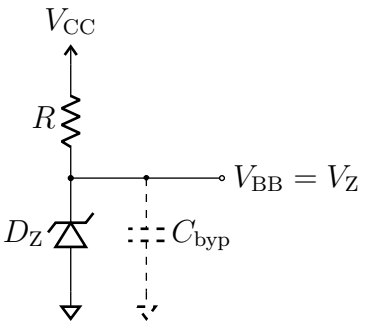


Figure 2.13: Zener diode voltage reference generator, with optional (dashed) filter capacitor.

In this solution, the op-amp buffers the $V_{BB} = V_{CC}/2$ voltage generated by the voltage divider on the left, offering a relatively low impedance voltage source on the right. Clearly, in the circuit, the performances of the amplifier are crucial as well as the power consumption added by the resistive divider dissipation (which can be kept acceptably low exploiting high values resistor, *e.g.* $\approx 500\,\mathrm{k\Omega}$ with a $9\,\mathrm{V}$ supply gives a dissipation of $324\,\mu\mathrm{W}$.

A simpler solution is the Zener diode one, which has the great advantage of using the less components possible (just one resistor and one diode, on the very least). But it has the disadvantage of not being adaptive, in the sense that, being the reference voltage equal to the voltage imposed by the Zener diode, it can not "follow" any variation of the supply. This can make the reciprocal distance between V_{BB} and V_{CC} vary, eventually causing some temporary reduction of the possible dynamic of the signal, even maintaining a correct supply of the potentiometer. The Zener diode solution presents a very low output impedance (since it derives from the parallel of the inverse of the Zener diode conductance and the R bias resistance). But in many cases also the output impedance of a standard operational amplifier is sufficient, for what concerns the virtual reference generation useful for the current discussion.

Many other parameters are involved in the design of a good supply especially

when high powers are involved. In the context here explored, the power consumption involved is low because of the relatively low current demand of the potentiometers. The situation is a bit different for what concerns the microcontroller operation. The microcontroller usually fulfils a huge set of other operation more than just driving the potentiometers, which indeed it is not an operation which demands huge resources to a standard controller (such as the ones belonging to the STM32L45 family). If the circuit design goes beyond the simple control of the potentiometers, clearly the power consumption can increase, bringing with it also the heat's management topic.

2.2.1 Consideration on a complex system

In a real application, the possible supplies needed can be many and with different requirements. Consider a design in which an analog circuit is controlled with digital potentiometers, implying the use of a microcontroller. In this situation at least three different supply voltages can be needed as can be seen in the following block diagram (Figure 2.14).

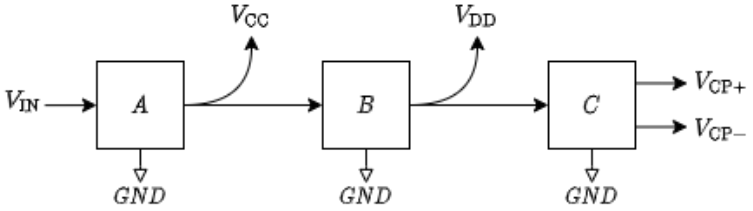


Figure 2.14: Logic representation of a possible supply cascading chain for a complete system.

In the above diagram a incoming voltage is properly scaled in order to generate the analog supply V_{CC} which usually has to be greater than the digital devices' one, in order to having available a proper dynamic. Then, in a sort of chain, other power supply unit are placed to generate the remaining digital supply voltages. In this block diagram example the supply of the microcontroller and the supply of the potentiometers are supposed different, so that a proper V_{DD} is generated for the controller by the block B. Whilst, supposing dual supply for the potentiometers, the block C is introduced.

Actually, the diagram can look more complicated or less, depending in the demand of the circuit allocated. It can be, for instance, that the supply of controller and potentiometers coincide, and in this case the C block is not needed. Or, a dual voltage for the analog circuit can be required, involving the design of an inverter block in parallel of A. Further more, a virtual ground reference is added when single supply operation is involved at least for one of the circuit supplied

(similar to the case of the diagram above, Figure 2.14). The fundamental point here is that a proper choice of the regulation block is absolutely crucial. Depending on the nature of the input voltage V_{IN} the A block choice varies in order to make the output voltage V_{CC} remains constant. If V_{IN} is the unregulated voltage coming form a rectifier section a switching converter circuit can be needed (buck or boost). On the contrary also a simple protection (to prevent inverse polarity connection or similar) can be sufficient, eventually in conjunction with a filter section. An important topics related to the powering of circuits in which different supplies are needed is the managing of different ground planes, especially when analog and digital block are mixed. Being the operation of the digital circuits unavoidably linked to the pulsating absorption or injection of current's spikes into the ground plane, the problem of the injection of currents into it rises. This can cause noise into the analog circuits that are close to the perturbation point, because they can be sensitive to reference's fluctuations. This problem is usually solved (at least in a good approximation) with the correct design of a "star" ground scheme.

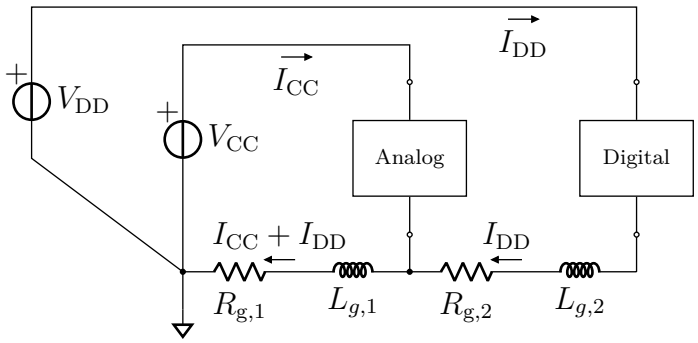


Figure 2.15: Wrong ground connection for mixed circuit.

"the digital return current modulates the analog return current (top figure). The ground return wire inductance [$L_{\mathrm{g},1}$ and $R_{\mathrm{g},1}$] *and resistance is shared between the analog and digital circuits, and this is what causes the interaction and resulting error."* [11] This scheme is usually done by designing a dedicated plane for the analog ground connections and one for the digital, with a connection between the two realised with a thick trace in a single point (the star ground point). Talking again about the general block diagram of Figure 2.14, many different circuits are commercially available. When a down scaling of an incoming higher voltage is needed, usually a more simple LDO (low drop out) regulator is sufficient. In cases a negative voltage for dual operation is needed, inverters are available as well as DC-DC converter in case of lower voltages that have to be converted to higher ones. In the following sections, two designs are presented, in order to show two very different approaches, dictated by the circuit requirements.

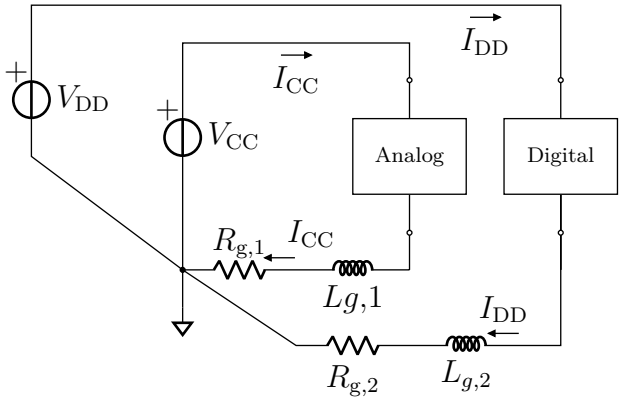


Figure 2.16: Correct ground connection for mixed circuit.

2.2.2 Practical example - Discrete series-pass linear voltage regulator

The circuit shown in Figure 2.17 is discussed in the book "The Art of Electronics" [4]. It represent a good example of a circuit still relatively simple but that is able to fulfil a considerable set of functionalities.

The current (whose AC component is filtered by the capacitor C_{byp}) flowing in R_1 and R_2 is sufficient to bias the Zener diode in the correct working point such that its voltage is almost constant at a certain value V_{Z}. At the output of the op-amp, the transistor Q_1 is placed inside the negative feedback loop of the amplifier, so that the current demanded by the load is not provided by the op-amp itself, but it flows through the transistor allowing a much higher current rating. This is because the op-amp output current is multiplied by the β of Q_1 Notice that the heat generated by this transistor has to be properly sunk, in order to prevent damages. The resistor divider formed by R_3 and R_4 generates the loop feedback voltage that is brought back to the amplifier's input to be compared to V_{Z}.

The circuit is equipped with an *over-current* protection composed by the transistor Q_2 and the sense resistor R_{sns}. The current flowing in R_{sns} determines the command voltage V_{BE} of Q_2, such that, when it is under a certain threshold, Q_2 stays off, when it exceeds that threshold, Q_2 turns on and begin to subtract current from the base of Q_1, limiting it. Hence, also the current exiting the emitter of Q_1 decreases when Q_2 is on, eventually closing the negative feedback that avoid problems related to short circuits at the output. The current threshold at which the *over-current* protection enters in action is decided by the value of the resistor R_{sns}, so it can be finely chosen. *E.g.* a $6.2\,\Omega$ for a maximum current of 100 mA.

The present circuit also offers an *over-voltage crowbar* protection, which prevent a certain load to demand a supply high than a certain threshold. The over-voltage

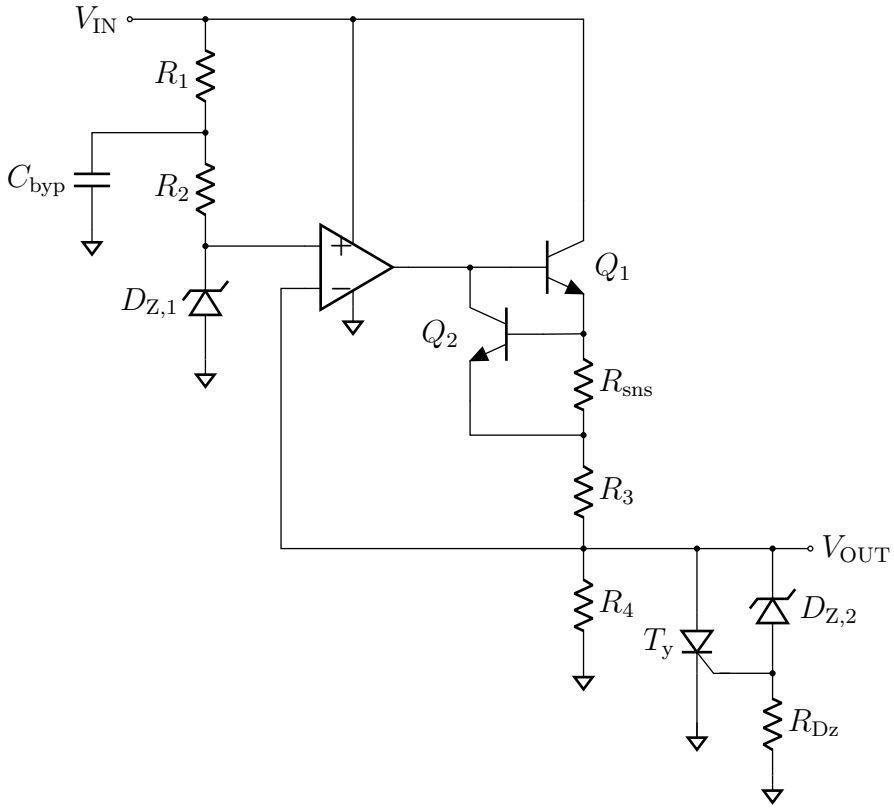


Figure 2.17: Discrete component series-pass linear voltage regulator.

threshold is determined by the series of $D_{\mathrm{Z},2}$ and R_{Dz}: when the voltage exceed the normal operating voltage of the Zener the latter establishes a fix $V_{\mathrm{Z},2}$ voltage at its terminals. So that when the output voltage exceeds the quantity $V_{\mathrm{Z},2} + V_{\mathrm{ON,ty}}$ (with $V_{\mathrm{ON,ty}}$ being the gate to cathode turn on voltage for the thyristor), the thyristor turns on, hence providing a low impedance path for the output current (short circuit). This situation pushes the regulator in a current limiting condition with the output grounded by the thyristor, it is anyway a good rule of thumb to insert a fuse in path of the current to prevent any further failure.

This type of design is implemented in situations in which the maximum output current reaches the ampere or so, implying dissipation for Q_1 up to a value around 20 W.

2.2.3 Practical example - LM27762 inverter

The present design is a lower power solution, practical when devices like the digital potentiometers are involved, since it has the advantage of producing a dual supply

(low voltage) and it is very compact, because of the low number of components required.

The LM27762 is a low-Noise dual output integrated charge pump and LDO. Designing with this type of components is relatively simple, since they generally require a few external component because all the control is implemented on the integrated circuit. To achieve the charge pump operation and voltage inversion the device exploit a complex internal network including switches' arrays and a 2 MHz oscillator. The fact that the oscillation that clocks the internal pump is at such a high frequency with respect to the audio limit is important, because this means that it can be completely removed from the output voltage, avoiding disturbances.

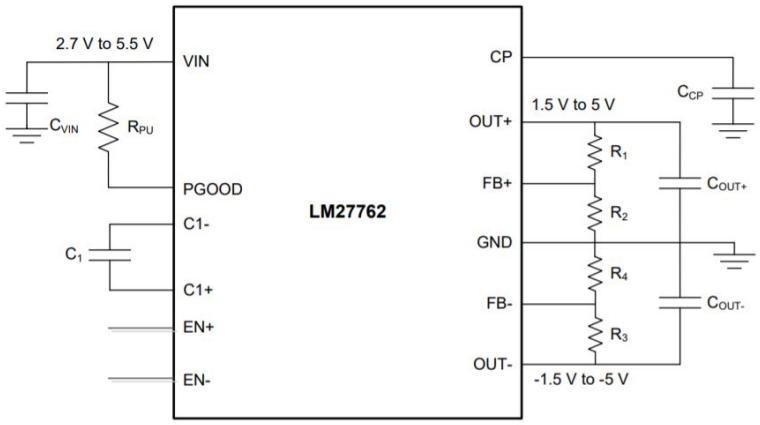


Figure 2.18: Texas Instrument LM27762 datasheet suggested circuit.

The output voltage can be set independently for the positive or negative output, with the voltage divider composed by R_1, R_2 or R_3, R_4 respectively (Eq.2.4 and Eq.2.5). The range of these outputs is $\pm 1.5\,\mathrm{V}$ to $\pm 5\,\mathrm{V}$ with an input voltage that has to be larger than 2.7 V and smaller than 5.5 V. The output capacitors are there for bypass purpose.

$$V_{\mathrm{OUT}}^{\mathrm{neg}} = -1.2\,\mathrm{V}\left(1 + \frac{R_3}{R_4}\right) \tag{2.4}$$

$$V_{\mathrm{OUT}}^{\mathrm{pos}} = 1.2\,\mathrm{V}\left(1 + \frac{R_1}{R_2}\right) \tag{2.5}$$

The external capacitor C_1 and C_{CP} and C_{IN} are the capacitor the work in conjunction with the internal charge pump CMOS switches. The values of the (ceramic) capacitor CP is usually chosen in the microfarad range (4.7 µF or so) and has to be slightly increased if the application requires a current flow which is closer to the rating of the device. The input capacitor C_{IN} is closely related to the C_{CP} because it is the reservoir that allows a quick transfer of charges from the

input to the charge pump output (so same values and characteristic of C_{CP} are required). The third external capacitor that is related to the charge pump is the "flying" capacitor C_1, which is in charge of transferring the input charges (from C_{IN}) to the output (to C_{CP}). If the values of this capacitor is chosen too small the device can exhibit some trouble in regulating the voltage at high current, whilst its value has not to be chosen too large otherwise the ripple at the output of the pump can increase. Usually the value is chosen around 1 µF or less (for larger current)[3].

The pin labelled as PGOOD, EN+ and EN− are terminals related to the control and monitoring operation of the correct functioning of the device. The enable pins EN+ and EN− control the functioning of the positive LDO and negative charge pump and LDO: when they are low (voltage lower than 1.2 V) the outputs of the device are force to ground via an internal 50 kΩ resistor. They have to be connected to a high voltage in order to enable the output. The "power good" pin instead, is an open collector active low terminal from which the user can monitor the functioning of the device. For instance, according to the datasheet, it is left to a high level, by the device itself, if one of the two output drops below 95% of the target voltage (outputs enabled). This is a useful feature: if for example the signal PGOOD is sensed by the microcontroller as an interrupt, so that a sort of "low power failure" flag can block the functioning of the system properly. Notice that while the enable pins are only inputs, from the LM27762 prospective, the power good pins is an open collector output, so it have to be connected to a proper pull-up resistor R_{PU} to the positive V_{IN} voltage.

2.3 Digital integration in an op-amp based amplifier

In the present section, the previously discussed problems and solutions for supply of the digital potentiometers lead to a first digital in place of analog substitution. The circuit chosen to this purpose is a non-inverting op-amp based amplifier, whose functioning has been discussed in chapter 1. The simplicity of the circuit in Figure 2.19 allows the discussion to focusing on the potentiometer functioning, still exploring a practically useful and feasible implementation.

To avoid the impact of the large tolerance on the absolute value of the potentiometer on the gain, the digital device is not exploited as a rheostat in the feedback of the amplifier, but it is placed across the inverting input. Consider a potentiometer with absolute value equal to $R_{\mathrm{pot}} \pm \Delta R_{\mathrm{pot}}$. Consider a new parameter x, variable from 0 to 1, which indicates the position of the wiper. According to this,

[3]Notice that C_1 has not to be polarised (electrolytic for instance), otherwise it will undergoes a reverse bias condition.

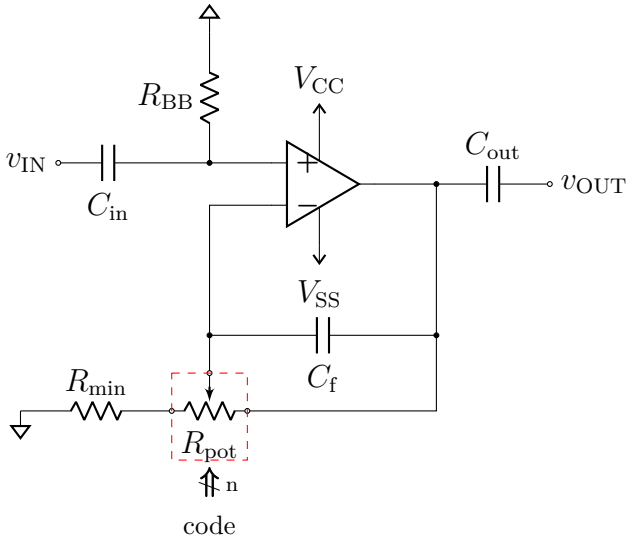


Figure 2.19: Non-inverting op-amp based amplifier, with digital potentiometer control.

if the potentiometer is placed as in Figure 1.11, the approximated[4] gain expression would be the following one:

$$A_v = -\frac{x\,(R_{pot} \pm \Delta R_{pot})}{R_{min}} \tag{2.6}$$

As visible from Eq.2.6, the absolute error on the potentiometer resistance is directly reported on the gain, reducing the predictability of this parameter and the reproducibility of the circuit itself.

If the potentiometer is wired as in Figure 2.19, the expression of the gain changes. Keeping into account the definition given for x, the portion of potentiometer resistance that falls between the inverting input and output can be expressed as $x\,(R_{pot} \pm \Delta R_{pot})$, while the one that goes from the inverting input to ground turns out to be $(1-x)\,(R_{pot} \pm \Delta R_{pot})$. With this assumption, the gain's expression can be rewritten.

$$\begin{aligned} A_v &= 1 + \frac{x\,(R_{pot} \pm \Delta R_{pot})}{(1-x)\,(R_{pot} \pm \Delta R_{pot})} = \\ &= 1 + \frac{x}{1-x}\frac{R_{pot} \pm \Delta \cancel{R_{pot}}}{\cancel{R_{pot}} \pm \Delta R_{pot}} = 1 + \frac{x}{1-x} = \frac{1}{1-x} \end{aligned} \tag{2.7}$$

[4]Neglecting the operational amplifier non-idealities.

Comparing Eq.2.6 and Eq.2.7 it is evident the absence of the $R_{\text{pot}} \pm \Delta R_{\text{pot}}$ term in the latter. The comparison of the two obtained gain curves, for the rheostat mode and the divider one are reported in Figure 2.20. Moreover, the curve that describes the gain with respect to x is changed because of the different dependence on the parameter x, but this is a minor issue. The curve shape is not a major problem for two independent reasons. Firstly, in a large portion of the usable range of the potentiometer, approximately from 0% to 75% of the "rotation", the curve has substantially a linear behaviour, which is comparable to the trend of the rheostat mode. Secondly, a different taper of the potentiometer can always be eventually modified via software. Another obvious difference is the fact that

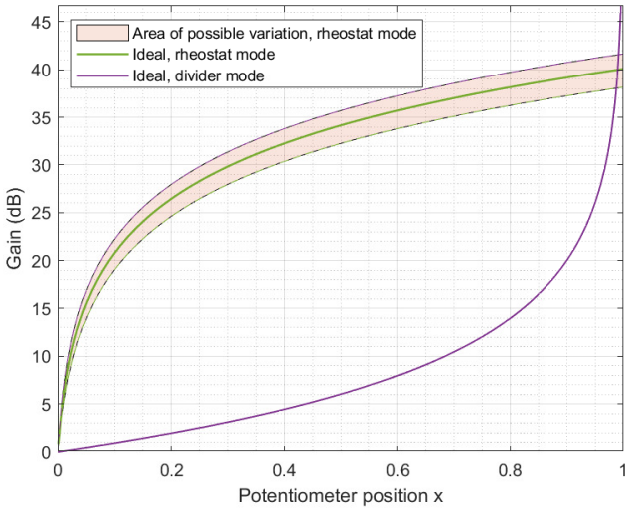


Figure 2.20: Approximated gain of the non-inverting amplifier for different position of the potentiometer. Notice the shaded area, in which a tolerance of 20% on R_{pot} makes the gain unpredictable, around the ideal value.

the two curves have the central region of the x variation which results in very different gain levels. This situation can be fixed placing two resistors one between the potentiometer and the op-amp's output and the other between the other fixed potentiometer terminal and ground. These additional resistors limit the action of the potentiometer: the feedback one unsure a gain value at the minimum position grater than one, practically introducing an offset for the violet curve in Figure 2.20, the other resistor (labelled as R_{min} in the circuit of Figure 2.19) limits the maximum value of gain, preventing the circuit to enter instability or distortion operating regions. The values of these two resistor has to be chosen wisely in according to the R_{pot} and the specifications of the circuit.

The circuit shown here assumes that the digital potentiometer is supplied in the correct way as well as that the op-amp has sufficient dynamic available to amplify

correctly the incoming signal. Anyway, two decoupling capacitor C_{in} and C_{out} have been inserted in order to make any potential DC component at the external of the circuit not affect the operation of the amplifier. This permits a supply of the amplifier completely independent on what are the DC domain outside the decoupling. In particular, if the virtual reference has to be inserted, in case of a single supply functioning $V_{\text{SS}} = 0\,\text{V}$, the resistor R_{BB} has not to be connected to ground, but to this virtual reference. Its value is to be determined, in order to have a negligible attenuation of the signal into the band (allowing to neglect the loading effect with the source impedance) and at the same time to obtain the correct cut-off frequency of the amplifier band (notice that C_{in} and R_{BB} form a high pass filter).

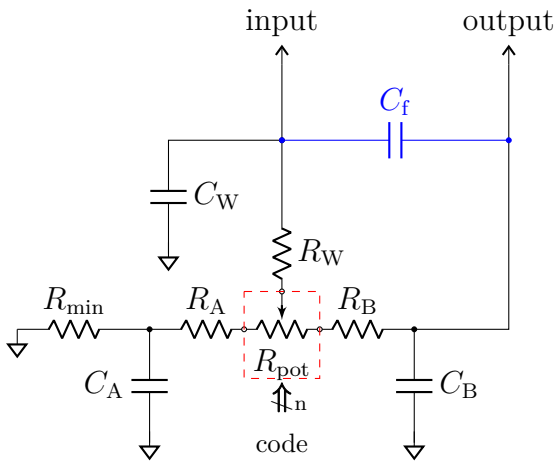


Figure 2.21: Isolated feedback network of the circuit in Figure 2.19 with the parasitic inserted. The red dashed box points out the ideal digital potentiometer, whilst in blue is drawn the low pass feedback capacitor.

In Figure 2.21 the feedback network of the circuit above (Figure 2.19) has been re-drawn considering the parasitic elements introduced by the potentiometer. An exact solution of the circuit in Figure 2.21 is not so manageable, since the at least three capacitances involved make the analysis very heavy. In principle the *Millman's theorem* can be exploited to calculate the voltage at the ideal internal wiper tap, from which the *Ohm's law* leads to the output voltage calculation. In Figure 2.22 the results of a spice simulation are reported using the following values $C_{\text{A}} = C_{\text{B}} = 45\,\text{pF}$, $C_{\text{W}} = 60\,\text{pF}$, $R_{\text{A}} = R_{\text{W}} = R_{\text{B}} = 200\,\Omega$, $R_{\text{min}} = 1\,\text{k}\Omega$ and $R_{\text{pot}} = 100\,\text{k}\Omega$[5].

[5]The decoupling and biasing components remaining are not considered as fundamental, because

In this situation the position of the potentiometer is crucial, because of the usually large absolute value of the potentiometer compared to the parasitic resistance one. Sticking to the previous definitions, when $x = 0$ the amplifier works substantially as a buffer, and the effect of the parasitic is not relevant in the sense that they only imply a low pass filter action at very high frequencies. Same behaviour is the one obtained for $x = 1$. With this value the gain is maximised and also in this condition the transfer function of the circuit is the one of an amplifier superiorly limited by a $-20\,\mathrm{dB/dec}$ low pass filter (so of the first order) at high frequencies.

The serious behaviour happens in between the two positions. When $x \approx 0.5$, the magnitude of the transfer function in the Bode plot exhibits a resonance peak. The peaking behaviour can appear similar to the one of a second order filter, at a first sight, but this is not because the slope of the magnitude after the peak is still $-20\,\mathrm{dB/dec}$, not $-40\,\mathrm{dB/dec}$. So the behaviour at high frequencies is still the one of a simple low pass filter. This is because the complicated summation and cancellation of poles and zeros that generates the peak is making the effect of only one of the capacitor to be dominant at high frequencies.

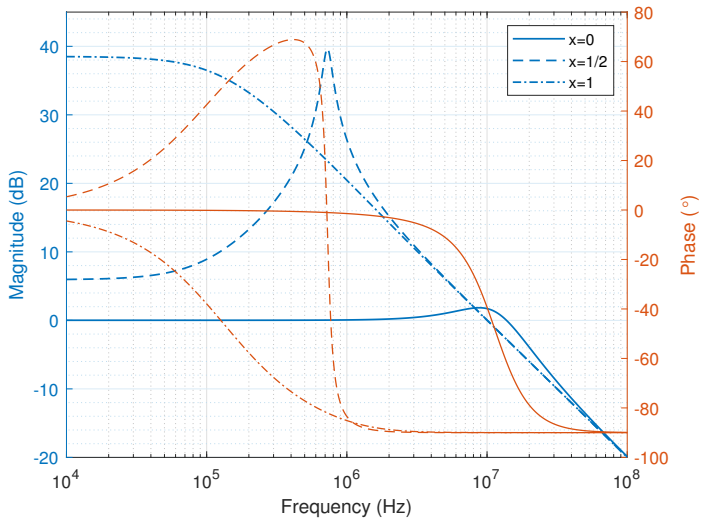


Figure 2.22: Bode plot for the circuit in Figure 2.21 without the capacitor C_f. In orange, on the right axis the phase response is plotted, while on the right the there is the magnitude response in blue.

To compensate the unstable response at high frequencies, the capacitor C_f is introduced. In practice, the cut-off frequency of this low-pass filter is determined, in a first approximation, by the interaction between C_f and the parallel to it portion

their value can be chosen in order not to influence in any way the following discussion.

of resistance $x\,(R_{\text{pot}} \pm \Delta R_{\text{pot}})$. For high gain levels the cut-off point moves towards lower frequencies (filtering more of the possible noise amplified at high frequencies) and it moves towards higher frequency for low gain levels. The progression of this cut-off point is linear with respect to the position of the potentiometer, again if the interaction between the other capacitance in the circuit is neglected. The zero, at even higher frequencies with respect to the pole, introduced by C_{f} behaves in the same way. The value of C_{f} is to be chosen so that the attenuation introduced at the peak's frequency is enough. The new response is visible in Figure 2.23. Further more, implementing a capacitor $C_{\text{f}} = 47\,\text{pF}$, the resulting dominant cut-off frequency with maximum gain is around 23 kHz (just above the audio limit).

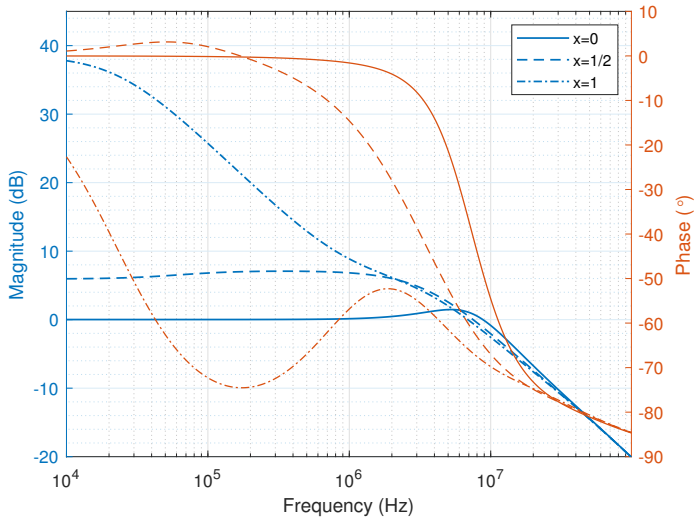


Figure 2.23: Bode plot for the circuit in Figure 2.21 without the capacitor C_{f}. In orange, on the right axis the phase response is plotted, while on the right the magnitude response is shown in blue.

From the potentiometer prospective the important point is that at high frequency operation, the parasitic elements introduced by the digital potentiometer have to be considered to properly stabilise the circuit, avoiding out-band instability.

Chapter 3

Noise issue - possible solution

The design of the amplifier discussed in the previous section brings the continuation of the present text directly to the second important issue related to analog integration of digital potentiometer. The fact that the potentiometer proceeds in its sweep by finite steps leads to a series of considerations. Firstly the gain curves in Figure 2.20 are not continuos curve, but they are the sequence of a large number (number of steps of the potentiometer N) of tiny steps, that directly reflects the quantised nature of the potentiometers. Usually this is a minor issue, in the sense that the refinement offered by a 256 steps potentiometer is usually sufficient, at least in audio applications. Furthermore the major problem that rises in an application as the previously discussed is related to the time interval around the commutation between a certain position and the next one (when the new stream is updated into the RDAC register).

3.1 Zipper noise theory and ground perturbation noise

Consider a sine waveform amplified by a circuit such as the one of Figure 2.20. Supposing to have an analog potentiometer with resolution $n = 5$ bit (or equivalently $N = 2^{\mathrm{n}} = 32$[1]). Furthermore, the values of R_{min} is chosen to be zero, for sake of simplicity in this explanation. The gain is expressed by Eq.2.7, in which x represent the position of the potentiometer. In the previous sections, the position x was plotted as a continuos variable, but in case of a digital potentiometer this is

[1]This resolution is low, but it is appropriate for demonstrating the problem here introduced.

obviously incorrect. So the relation that stands between x and the bit stream, the digital command, is the one in Eq.3.1

$$x = \frac{\#\text{ of the step}}{N} \tag{3.1}$$

From this relation is possible to see the granularity of the gain curve.

$$A_{\text{dg}} = \frac{\dfrac{\#\text{ of the step}}{N}}{1 - \dfrac{\#\text{ of the step}}{N}} \tag{3.2}$$

Consider a situation in which an analog potentiometer is used to control the gain of the present circuit and it is rotated so that A_{ag} varies from 1 to 3, in a certain period of time. A possible analog gain curve is represented in Figure 3.1 with the blue trace. Instead, the digital control situation with the above introduced 5 bit potentiometer produce the orange curve of Figure 3.1, through Eq.3.2. In this plot it is evident the difference in the transition between the two solution.

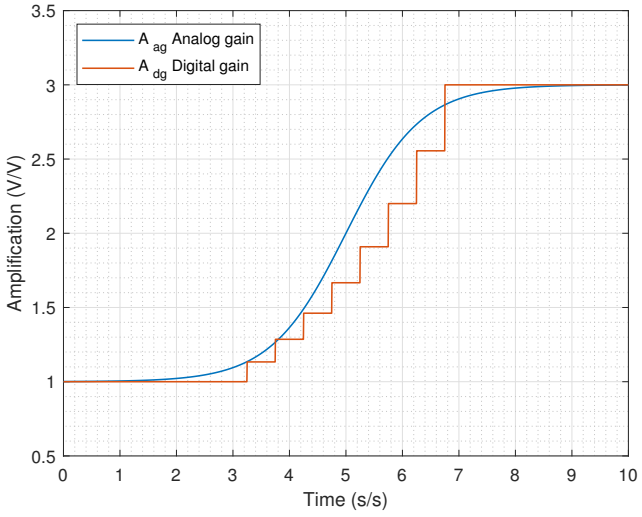


Figure 3.1: Plot of the gain curve, for a transition between unitary gain to a value of 3, for both analog (blue) and 5 bit digital (orange) implementation. The time axis is normalised to the period of the wave in Figure 3.2

It is now important to see the impact of such curves on the amplified signal. The output of the circuit is simply the product of the input signal and the gain expression, so, in the analog case, a continuos output is expected, whilst for the digital implementation, the steps in the gain curve result in discontinuities on the output voltage. As it is visible in Figure 3.2 and in the zoom of Figure 3.3,

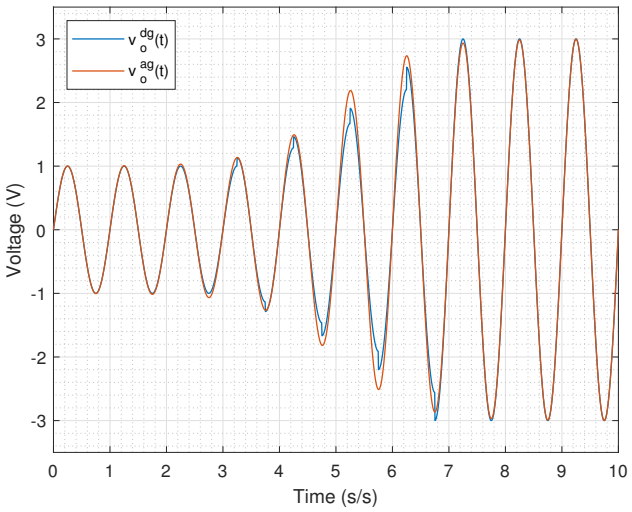


Figure 3.2: Output waveforms of the circuit discussed. v_{o}^{ag} is the analog output and v_{o}^{dg} is the discontinuous digital voltage.

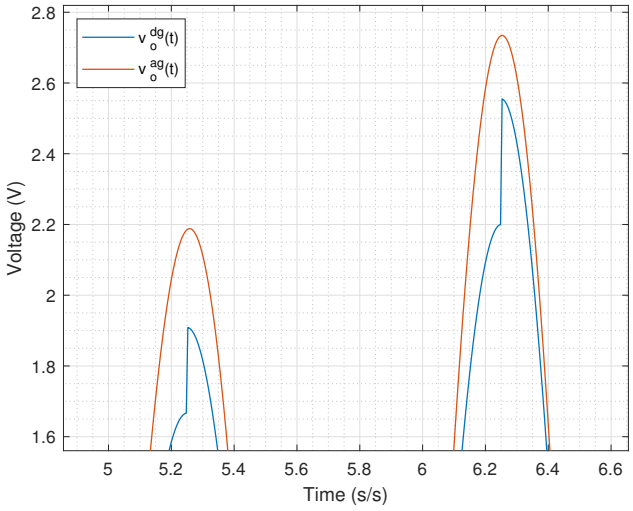


Figure 3.3: Same plot of Figure 3.2 zoomed around a central portion of the gain variation.

the discontinuities corresponding to the gain steps are quite noticeable. This is a situation in which the gain is not commutated immediately from one level to the other, so the steps are one for every code in between the initial and final position. This is because the process depicted is typical of those situation in which an external user operates a fine control from the external. The flux of information goes from a traditional potentiometer, set as a voltage divider between V_{DD} and

ground, to the microcontroller which senses the wiper voltage with one of the on board ADC. Then the microcontroller updates the command stream of the digital potentiometer. Since this entire chain is very fast compared to the usual human perception, the result is that during a manual sweep of a command the controlled quantity varies through many steps as above shown.

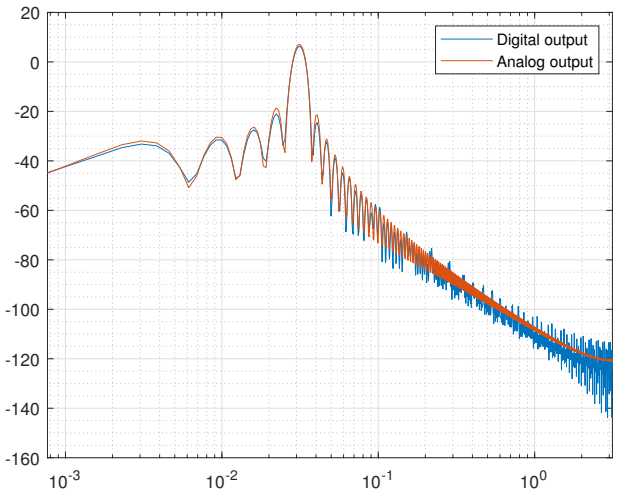


Figure 3.4: FFT results for the signals in Figure 3.2 through a *Kaiser* windowing. The plot has been drawn with smaller traces in order to make visible the differences in the harmonic content also at higher frequency.

The FFT of the two signals is shown in Figure 3.4, exploiting a *Kaiser* windowing. It is visible that, even if the digitally controlled signal exhibits an higher noise level at higher frequencies, substantially the two signals has similar characteristic. The THD values of the two signals are $\text{THD}_{\text{dg}} = 0.0574\%$ and $\text{THD}_{\text{ag}} = 0.0485\%$, and the THD of the analog output is not null because of the variable envelope due to the gain variation.

Yet there is another important source of noise in the circuit, due to the potentiometers. The issue is related to the injection of current in the ground plane in correspondence of the discontinuities already introduced by the intrinsic behaviour of the digital devices. Even if a ground planning that involves the separation of the two planes is a good way to attenuate the noise coming from digital commutation, this is not yet sufficient. Moreover, the commutation itself can generate some glitches in the signal directly at the nodes from and towards the selector move. The solution to these problems is a big part of the digital integration process.

In the case of the discontinuities introduced by the granularity of the potentiometer, there is the possibility of acting directly on the source itself of the possible noise. In case of a superposition of noise onto the output signal through the

reference plane or from the commutation elements, the source of noise is due to the commutation of the digital block of the potentiometer and it can not be eliminated at the source. This noise injection process is therefore avoidable only through a very accurate ground plane design, in which the simple separation of the two plane is mandatory but not sufficient or through muting systems of the output.

3.2 Zipper noise solution - *Zero-crossing-window* detection

The method here presented is capable of reducing in an efficient way the discontinuities introduced in the signal by the digital selection of the wiper position. The idea at the base of this circuital solution is the following one. If the signal that undergoes the injection of noise is periodic and decoupled, the waveform (whatever it is) exhibits a intercept point with the 0 V level, which is also periodic[2]. Thinking about the amplification operation of a circuit, it multiplies by a certain constant (at a given frequency) the incoming signal, actually modifying the amplitude of the wave. There is only one point of the wave which remains untouched during this operation and it is the point for which the wave voltage is null.

The zero-crossing point remains at the level it is for any value of amplification possible. This means that if the step in the gain curve is time-wise coincident with the wave zero value crossing instant, the resulting amplified waveform is again continuos.

In the following image (Figure 3.5) the instants in which the commutations of the selector inside the potentiometer have been rigidly translated till they have superimposed the zero-crossing point. As it appears clear, the discontinuities disappear, because they are hidden in the zero-crossing point. The solution is intuitively simple, but at the same time it is not so straight forward to be implemented practically. The core idea of the practical implementation is the following one, and it requires one more assumption. The potentiometer must have some sort of synchronization input or in general strobe signal that enables the reading of the command string. For example in the AD5292, the $\overline{\text{SYNC}}$ input is normally kept high and its falling edge triggers the loading into the register of the input stream on the subsequent falling edge of the clock.

This is mandatory because the zero-crossing window method works exactly on the level of this $\overline{\text{SYNC}}$ strobe. In the following block diagram (Figure 3.6) the situation is explained. Notice that the $\overline{\text{SYNC}}$ input arrives from the AND gate,

[2]This is valid in general, also when the reference of the signal considered is not the ground of the circuit.

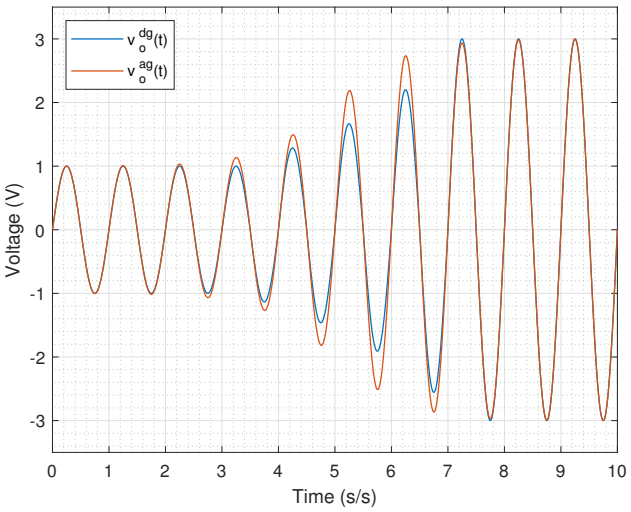


Figure 3.5: Same plot of Figure 3.2 zoomed around a central portion of the gain variation.

whose output results from the microcontroller synchronisation strobe ($\mu\overline{\text{SYNC}}$) and the output of the zero-crossing window detector.

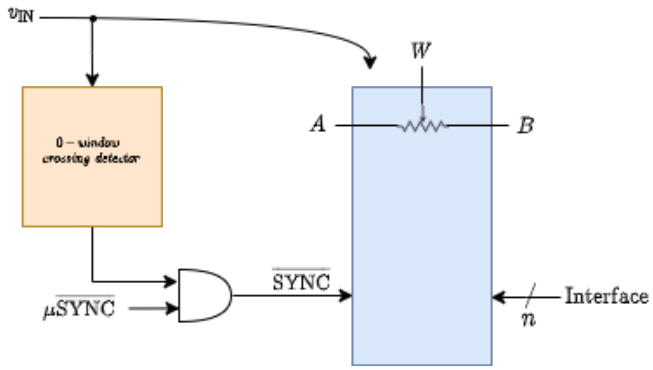


Figure 3.6: Block diagram of a zero-crossing window application.

If the potentiometer does not support this operation an alternative is the use of a chip select terminal ($\overline{\text{CS}}$, $\overline{\text{CE}}$) which can be used with comparable results, despite the different functions fulfilled in the digital circuit of the potentiometer, by this signal.

The zero-crossing window detector block is the analog circuit that is able to receive an input signal and giving as output a digital level, which is asserted only if the input function is crossing the zero level. In fact, is impossible to detect an exact point, also because ideally, if this could be done, the output signal of the detector

would be a Dirac delta. The real implementation involves a window comparator, in practice a circuit whose output is asserted if and only if the input function is inside a certain region around the zero level.

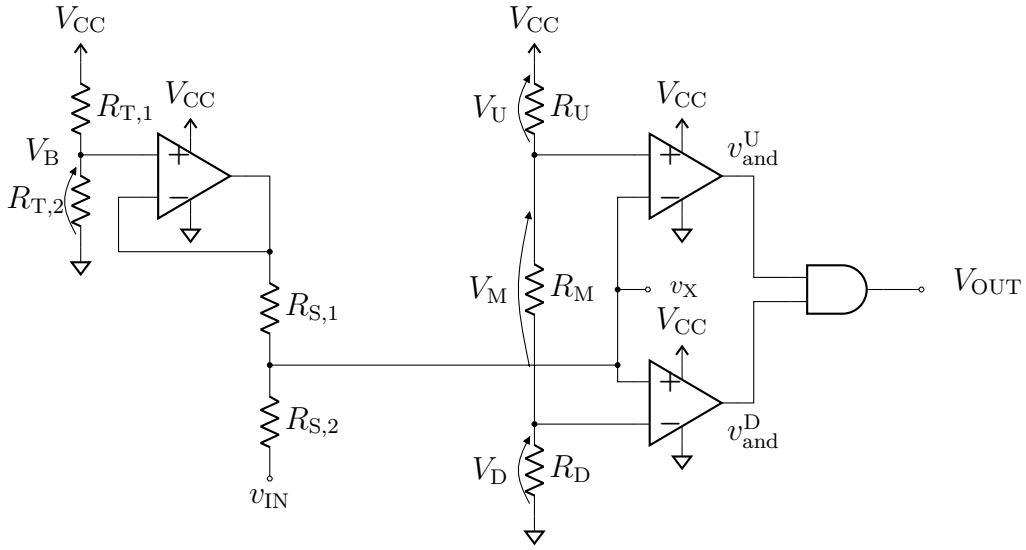


Figure 3.7: Zero-crossing window detector circuit.

In the circuit shown in Figure 3.7 three op-amps have been used in order to generate the correct information. Consider just the two op-amps on the right. The current flowing in the divider composed by R_U, R_M and R_D fixes the voltage of the non inverting (upper) op-amp input and the one of the inverting (lower) op-amp.

$$V_D = \frac{R_D}{R_U + R_M + R_D} V_{CC} \tag{3.3}$$

The voltage at the non-inverting input of the upper op-amp is given by $V_D + V_M$ or alternatively $V_{CC} - V_U$

$$V_M + V_D = \frac{R_D + R_M}{R_U + R_M + R_D} V_{CC}. \tag{3.4}$$

Because the two op-amps on the right don't have any feedback from the output to the input their output can be either at the positive or negative supply rail. In this way they work as comparators and considering all the possibilities that stand for the position of the voltage v_X with respect to the thresholds above calculated, the following cases can be discussed.

1. If $v_X < V_D$, the input differential voltage of the lower op-amp is negative so $v_{and}^D = 0\,V$ which is the logic low value. While the first upper op-amp has

an input differential voltage which is positive so that $v_{\text{and}}^{\text{U}} = V_{\text{CC}}$. The v_{OUT} resulting from the and operation is therefore equal to 0 V.

2. If $v_{\text{X}} > V_{\text{U}}$, the behaviour of each op-amps is reversed. The input differential voltage of the lower op-amp is positive, so that $v_{\text{and}}^{\text{D}} = V_{\text{CC}}$ which is the logic high level. While the first upper op-amp has an input differential voltage which is negative so that $v_{\text{and}}^{\text{U}} = 0\,\text{V}$. The v_{OUT} resulting from the and operation is again equal to 0 V.

3. If $V_{\text{D}} < v_{\text{X}} < V_{\text{U}}$ the two op-amps both have a positive differential voltage, so that the inputs of the and port are both high and so $v_{\text{OUT}} = V_{\text{CC}}$ indicating that the incoming signal has a value inside the window determined by the thresholds V_{D} and V_{U}.

Clearly the resistors that generate the thresholds have to be chosen properly, since their values determine the amplitude and offset (with respect to the 0 V reference) of the window in which the condition for the synchronisation is considered to be matched. Supposing a single supply solution (as the one in Figure 3.7), the centre of the window is chosen exactly on the middle level of the interval $[V_{\text{CC}},\ 0\,\text{V}]$. This condition is matched assuming $R_{\text{U}} = R_{\text{D}}$ and considering the power dissipated by the series, overall the value of these resistors have to be chosen high (hundreds of kΩ).

Another motivation for having the value of R_{U} and R_{D} high is that the size of the window is determined by the third central resistor of the divider, through the following equation:

$$V_{\text{M}} = \frac{R_{\text{M}}}{R_{\text{U}} + R_{\text{M}} + R_{\text{D}}} V_{\text{CC}} \tag{3.5}$$

If R_{U} and R_{D} are large, R_{M} can be chosen in the hundreds of ohm range. For example, considering $V_{\text{CC}} = 3.3\,\text{V}$, $R_{\text{U}} = R_{\text{D}} = 100\,\text{k}\Omega$ and $R_{\text{M}} = 806\,\Omega$ with 0.1% tolerance, the window has the following characteristics: dimension of $V_{\text{M}} = 13.246\,\text{mV}$ and centre at $V_{\text{centre}} = 1.65\,\text{V}$ with 0.2% tolerance.

The voltage v_{X} is the voltage derived from the input signal through some manipulation (rescaling and translation). This is because it is fundamental that when the input signal v_{IN} equals zero, the corresponding v_{X} is exactly at the centre of the window. Consider an input signal referred to 0 V and with a peak-to-peak voltage of 20 V. A possible solution is to insert a voltage divider to restrict the range of the input signal: a ten to one ratio for the resistors $R_{\text{S},1}$ and $R_{\text{S},2}$ will generate a v_{X} with a peak-to-peak voltage of approximately 1.82 V[3]. For instance

[3]The value of this ratio is chosen considering the estimated amplitude of the input signal.

consider $R_{S,1} = 9.09\,\text{k}\Omega$ and $R_{S,2} = 90.9\,\text{k}\Omega$ with 0.1% tolerance. This voltage can be easily managed inside the dynamic of the comparators.

Moreover, this is not yet sufficient, since, ideally, an offset V_{centre} of 1.65 V has to be summed to this signal. In Figure 3.7 this is done by connecting the bottom of the input divider to fixed the low impedance source, formed by the buffer (op-amp on the left) and the divider $R_{C,1}$ and $R_{C,2}$. Choosing $R_{C,1} = 27.4\,\text{k}\Omega$ and $R_{C,2} = 33.2\,\text{k}\Omega$ (0.1% tolerance) the voltage V_B equals 1.808 V. This is not yet the offset of v_X since this voltage is just the reference of the input divider. Looking at the latter in the opposite direction with respect to what has been done for the varying input v_{IN}, the offset is finally given as follow[4]:

$$V_{\text{centre}} = \frac{R_{S,2}}{R_{S,1} + R_{S,2}} V_B = 1.644\,\text{V} \tag{3.6}$$

This value is sufficiently close to the desired one, so that a complete simulation of the circuit can be done exploiting the values discussed.

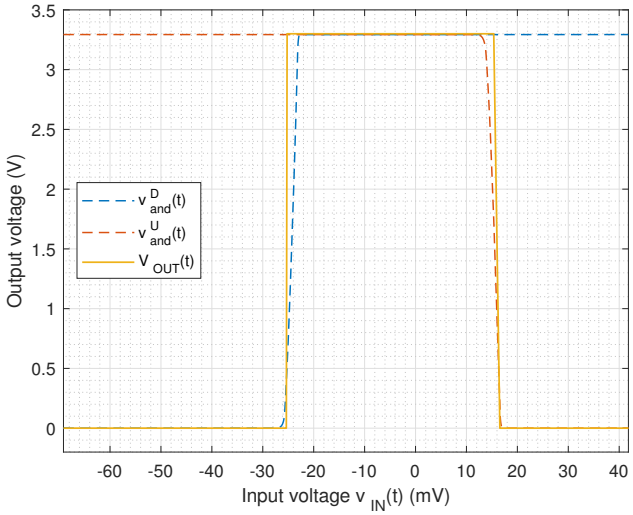


Figure 3.8: Simulation results for the circuit of Figure 3.7.

In Figure 3.8 the characteristic $V_{OUT}(v_{IN})$ has been reported as well as the output voltage ad the comparators output. Notice that the values of the resistor involved in this circuit are crucial, and so they can be tailored in conjunction with the amplifier and comparator used. In particular, while the fix threshold resistors R_U, R_M and R_D can be chosen considering only the size of the window and the

[4]This can be done exploiting the superposition theorem.

power dissipation, a good design choice can be to replace resistor $R_{T,2}$ with a precision trimmer. This is because $R_{S,2}$ and $R_{S,1}$ are not crucial (v_X must swing well beyond the limits of the window, but its exact amplitude is not crucial), whilst the centre voltage of the window (determined by the left most divider of Figure 3.7) is very important: few percentage of variation can shift the zero-crossing point of the input signal, outside the window.

For the simulation reported the linear technology RH1498M has been used for all the three active devices. This is a rail-to-rail input and output op-amp, so that it can swing the output signal to be sent to the AND gate from 0 V to V_{CC} (here chosen at 3.3 V) ensuring good noise margins. Clearly, the precision of the *zero-crossing window* method is determined by the efficiency of this detector circuit. This circuit has to be as fast as possible in commutating when the window is entered or left, and also it has to shown a reasonably restrict window, because the far from the zero-crossing the selector movement is done, the noisier the output of the analog circuit will result.

The circuit must be fast for the following reason. Consider an audio signal with frequency $f_{sig} = 1\,\text{kHz}$ and a zero-crossing window centred at 0 V with amplitude $\Delta V_W = 10\,\text{mV}$. The time that the signal takes to pass thorough the window (t_W) is given by the following formula[5]:

$$t_W = \frac{\Delta V_W}{2\pi f_{sig}} = \frac{10}{\pi}\mu\text{s} \approx 3.183\,\mu\text{s} \tag{3.7}$$

Now, the $\overline{SYNCH}$ has to be asserted in a time range sufficient to allow the microcontroller to commutate the position of the switch. Hence that the active elements chosen for realising the circuit discussed have to be fast enough so that their propagation delays summed don't violate the constrain imposed by the time t_W (t_{par} indicates the delay due to the parasitic capacitance on the voltage divider network and connection in general).

$$2t_{AND} + t_{COMP} + t_{par} \ll t_W - t_{\mu C} - T_{1rmpot} \tag{3.8}$$

So it is evident that a trade-off between signal-to-noise ratio of the output analog signal and time constrains (related to the size of the window) has to be found in order to match the specifications.

There are a few devices, such as the Maxim Integrated DS1882, which already have on board the *zero-window-crossing* detector circuit, whose action can be enabled or disabled through the setting of a configuration register. Indeed, as visible in Figure 3.9, the pointed out device is not the most basic one, since it offers

[5]Since a small region around 0 V is considered, a simple linear approximation can be used, without committing any limiting error: $sin(x) \approx x$.

almost all the features of interest for normal applications: memory, *zero-window-crossing* detection, independent analog and digital supplies.

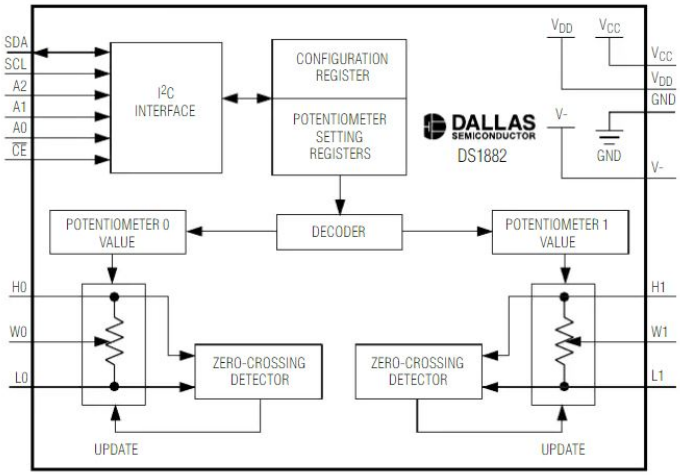


Figure 3.9: Block diagram of the AD1882 (Maxim Integrated) in which is visible the *zero-window-crossing* detector block is visible a the bottom. Its output is already labelled as an "update" command sent to the potentiometer selector.

3.3 Noise solution - output muting

From what has been reported in section 3.1, it results that the distortion problem caused by a sudden change in the slope of the signal (steps) produces an increment of the THD, enforcing the harmonic content of the signal. Yet, the increment can be quite small and if the disturb introduced are acceptable, depending on the application, the inserting of a *zero-crossing-window* detector circuit can result not completely justified. Still the noise introduced by the commutation (and not the step) in the signal is still a major problem. The following proposed systems are variation on a "brute force" technique which can, till in many cases, be effective.

The idea is that, if the source of noise can not be eliminated by acting on some particular parameter of the process (such as the timing of the commutation, as previously done), a possible solution is in the direct manipulation of the output signal. In this case the idea is to isolate the output voltage when a commutation is occurring, preventing it to perturb the circuitry that follows. At the bottom of this idea is the fact that, for example in audio design, the human hearing is not capable of sense variation in the waveform listened such as small muting window, so a muting of the circuit output is not influencing the final perception of the overall system. In Figure 3.10 the functioning principle of the muting system is

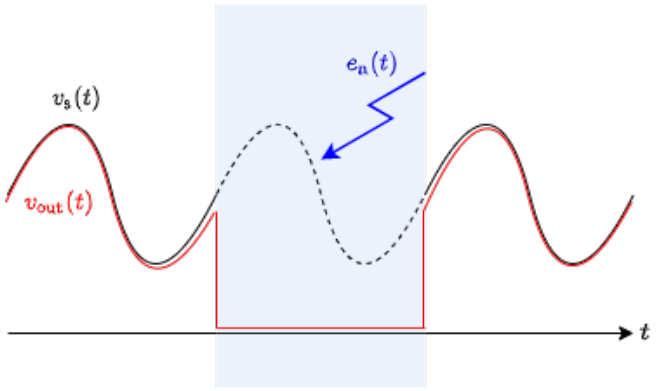


Figure 3.10: Functioning principle of the muting system.

provided. Still thinking at this level of complexity three important figure of merit of the muting circuit can be realized. One is the *transparency* of whatever circuit fulfils the muting operation when the circuit operates in the normal way. It is evident that the muting circuit has to be the more un-effective as possible on the output signal, in order to limiting as much as possible the possible increase of the distortion.

The second evident parameter of the circuit is the *attenuation* when the muting operation is on. It has to be as higher as possible, in absolute value and it is usually expressed in decibel, because this means that the signal is made null as well as the noise.

This parameters are related to the level of the signal, the other intuition that comes from observing Figure 3.10 is what are the time interval that the circuit need to intervene. The problem of the timing is divided into two parallel aspects: the time that that takes between the receiving of the muting command and the effective action on the signal and the time that is required by the signal to effectively go from a certain level to the standby value.

Depending on the type of circuit exploit to achieve the muting function this parameters vary a lot, and the meeting with the specifications can require some further modification of the circuit. In the following section some of the possible muting systems are discussed in more details.

3.3.1 FET switch

The intrinsic functioning of the muting circuit involves some sort of switches. They can be realised exploiting many different component or devices, but the most immediate choice is the transistor. In the following, a JFETs based solution is presented, considering that, with a little effort, the majority of the developed situations can be applied also to BJTs, MOSFETs or others.

Before starting to analyse the circuits themselves it is useful to review the JFET functioning itself. Basically the transistor core behaviour, the controlled current generator principle is common to all transistors but what changes is the nature and mode of the control. In the JFET the control is in voltage, since practically no current flows into or out from the gate, on the contrary to what happens in BJT designs. This makes JFET and MOSFET similar and in fact the both exploits a unipolar channel control process to fulfil their functions.

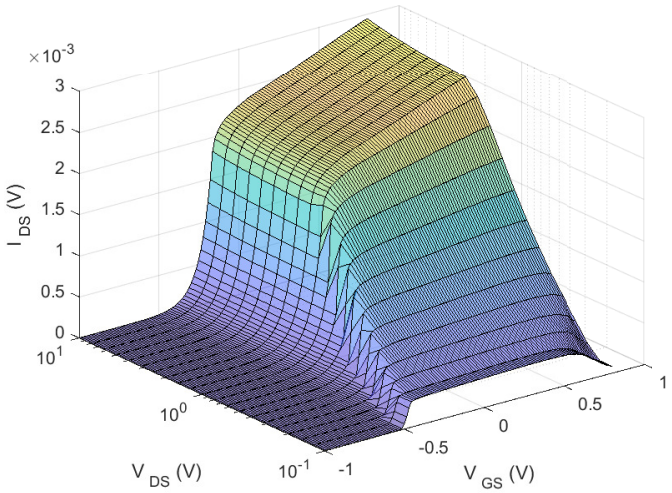


Figure 3.11: J201 characteristic with V_{DS} from almost 0 V to 10 V and V_{GS} from -1 V to 0.8 V.

In Figure 3.11 the characteristic of the J201 JFET is presented. The dependence of the drain current on the gate to source voltage is quadratic, when the saturation region is entered. But in fact, in our discussion, the curve traced by the current in every region is not so important, since only two operating regions matter: the off state and the saturation one.

Since in off state no current flows through the drain, the connection to this terminal looks as an open circuit, so an open switch. When the device is on, for high values of V_{GS}, the current flows through the channel and the equivalent circuit seen from the drain node is modelled with a resistance of value $R_{\mathrm{DS}} = V_{\mathrm{DS}}/I_{\mathrm{DS}}$.

Because the current increases with the control voltage the temptation is to make the gate to source voltage be much greater than zero in on state, in order to minimise the on-resistance. This can not be done, since even if slightly positive values of V_{GS} are manageable be the JFET, it quickly exits its normal operation when the gate junction is forward biased. This happens when V_{GS} exceed a certain slightly positive value, such as 0.6 V or a bit more. In any case a good rule of

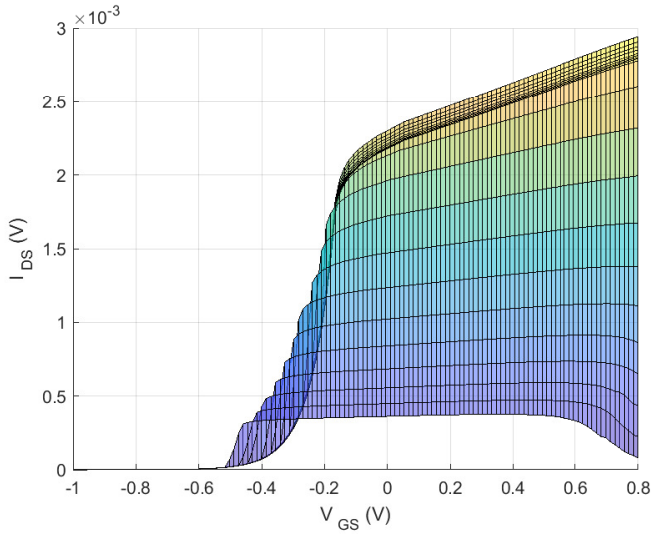


Figure 3.12: J201 characteristic view from the V_{GS} axis.

thumb is not to exceed the saturation current I_{DSS}.

This means that the control voltage used in the circuit has to toggle between two values: $V_{\mathrm{off}} \ll V_{\mathrm{PO}}$ (*e.g.* $V_{\mathrm{off}} = -3\,\mathrm{V}$ for the J201), which must ensure a completely off condition for the switch, and $V_{\mathrm{on}} \approx 0\,\mathrm{V}$ which allows a good amount (with respect to I_{DSS}) of current flows through the channel, without breaking the gate junction.

As in bipolar technology, both NPN and PNP transistor are possible, also for the JFET there is the possibility to implement n-channel JFET or p-channel JFET, with opposite characteristics. As discussed in the following, both type can be used in the same design in order to increase the performance of the circuit.

Essentially, in the following sections, the two types of JFET muting circuit are presented. This is because the specification can be reached, with some slightly difference, either placing the switch (normally closed) in series with the signal to interrupt the flux of information, or placing the switch in parallel (normally open) to the signal in order to shunt to ground the line when the muting is required.

Series configuration

In the *series-JFET* muting circuit, the switch is placed in series with the signal, so that when it is off the flux of information is interrupted. The choice of the type, n-channel or p-channel, of JFET to be exploited depends on the voltages that are available for the switching command. The driver in Figure 3.13 is important since it is very common that the microcontroller can not generate a signal with a sufficiently large swing in order to make the JFET go from an off state to an on

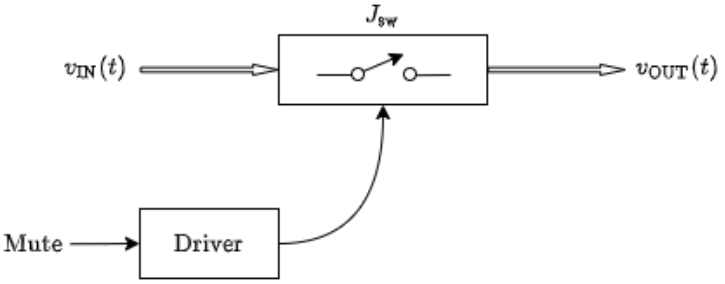


Figure 3.13: Simple *series-JFET* muting circuit block diagram.

state.

Supposing that the microcontroller can generate voltages up to its high supply level, *e.g.* 3.3 V. The driver whose output controls the gate of the JFET can be implemented in many different ways, a good figure of merit are the high input impedance, so that the voltage of the microcontroller is not stressed by loading effect. Usually a simple transistor stage whose input is connected to the *Mute* command is sufficient, as visible in the following schematic.

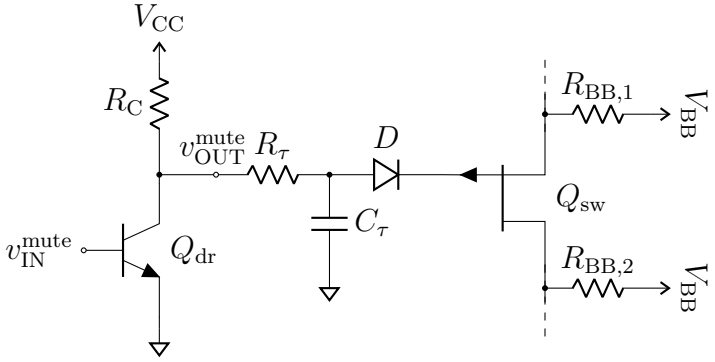


Figure 3.14: Driver circuit for a JFET switch.

Looking at the circuit in Figure 3.14, the input is the signal coming from the microcontroller. When v_{IN}^{mute} is low, the command voltage of the transistor Q_{dr} is null so that also its base current is null. If its base current is null, the transistor is off and also its collector current is null. This means that the collector voltage equals the supply voltage of the stage: $v_{OUT}^{mute} = V_{CC}$, because the result of the *Ohm's law* applied to the resistor R_C. Considering the channel of the JFET at the reference voltage, the command voltage of Q_{sw} is high ($v_{GS} = V_{CC}$). Being the JFET a p-channel device, it is off, disconnecting the two channel terminal as an open switch.

If the input command $v_{\text{IN}}^{\text{mute}}$ is high (at 3.3 V) the transistor is in saturation region and $v_{\text{OUT}}^{\text{mute}} = V_{\text{CE}}^{\text{sat}} \pm 0.2\,\text{V}$. If the threshold voltage is larger than this value of $V_{\text{CE}}^{\text{sat}}$ (condition which is usually easly satisfied) Q_{sw} is on, closing the contact.

The one pole low pass filter, formed by R_τ and C_τ, is inserted for stability purpose: it eventually smooths spikes and noise. Usually its cut-off frequency is chosen high, in order to not limiting the response of the driver too much. The diode is present to ensure that no current will start to flow out from the gate (p-channel) even if the command voltage would exceed a too low threshold for which the gate source junction conducts.

The critical point, at least as a first sight, of the circuit of Figure 3.14 is the fact that the correct driving of the switch controlling the gate voltage is not sufficient to ensure the conductivity of the channel because the voltage at the source of the device can vary arbitrarily with signal injected. Still looking at the p-channel JFET and considering the off state, it can happen that the peak of the signal oscillating around the bias voltage drops below a certain threshold, turning on the device. This situation is avoided if the signal injected has a peak voltage not larger than a certain level (exploiting the mesh across the gate)

$$\text{Off} - \text{state} \qquad \Longleftrightarrow \qquad \begin{cases} v_{\text{s,pk}} < V_{\text{BB}} - V_{\text{th}} \\ V_{\text{IN}}^{\text{mute}} = 0 \end{cases} \tag{3.9}$$

When instead the voltage $V_{\text{IN}}^{\text{mute}}$ is high and the driver is pulling down the voltage at the gate of the p-channel JFET. The voltage on the gate has to be low enough to ensure that the device will always be on. Again this is not entirely predictable because it depends on the peak value of the signal.

To ensure a better transparency of the switch when it is closed, a proper solution is to consider the implementation of a transmission gate. In a transmission gate, the correct transfer of the information between input and output is achieved with the use of a complementary type device in parallel with the first. This implies that even if the signal swing can drive one of the two JFET into a wrong operating region, the other will ensure the overall functioning of the switch.

Considering the transmission gate of Figure 3.17 some considerations can be done on the resistance offered by the switch to the transit of the signal in on state, R_{ON}. The voltage $V_{\text{BB}} = V_{\text{CC}}/2$ elevate the signal, adding an offset by means of which the negative peaks of the signal end up around the 0 V level[6]. Considering the on situation with $V_{\text{ctrl}} = V_{\text{CC}}$ and $v_{\text{in}} \approx -V_{\text{BB}}$, so that $v_{\text{IN}} \approx 0\,\text{V}$. The following

[6]The assumption introduced here is that the signal amplitude is such that v_{in} does not exceed the supply limits.

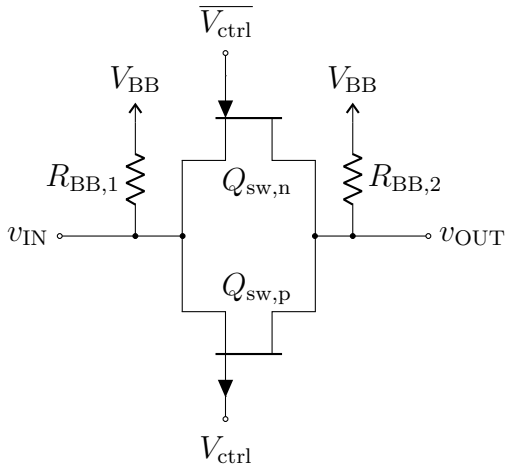


Figure 3.15: Transmission gate used to increase the performance of the muting *JFET-series* circuit. Notice the opposite polarity command given by the drivers the the complementary couple.

command voltages can be written:

$$v_{\text{GS}}^{\text{P}} = V_{\text{CC}} - v_{\text{IN}} = V_{\text{CC}} - V_{\text{BB}} - v_{\text{in}} \approx V_{\text{BB}}$$
$$v_{\text{GS}}^{\text{N}} = 0\,\text{V} - v_{\text{IN}} = -V_{\text{BB}} - v_{\text{in}} \approx 0\,\text{V}$$

The p-channel JFET is therefore switched off, because of the negative peak value reached by the time dependent component of v_{IN}. This means that the resistance of the gate is the on-resistance of one JFET only, and particularly the one of the n-channel when it is driven well above the threshold voltage, so it is low.

Considering now a voltage v_{IN} that rises towards V_{CC}, the transistor $Q_{\text{sw,n}}$ shifts gradually to a less conductive state being its command voltage lower, so the R_{ON} grows gradually too. Reached a certain level (still below V_{BB}) the p-channel JFET turns on and the overall resistance is given by the parallel channel resistance of the two contemporary on devices. So the R_{ON} decreases again stops to increase, till the n-channel JFET, exceeded a certain level above V_{BB}, start again to decrease accordingly to the p-channel device behaviour that is completely analogous to the one of $Q_{\text{sw,n}}$.

So the behaviour of the gate is strictly dependent on the particular level of the thresholds V_{PO} of the two devices. They have to be as symmetric as possible in order to offer an as uniform as possible resistance to the signal. Furthermore it is important that the two devices have a threshold which is greater than V_{BB} in absolute value, so that their behaviour ensure a superposition such that at least one device is well turned on for every v_{IN} value. In Figure 3.16 the resistance offered to the signal is reported as a function of the input voltage, for different

values of V_{PO}. Notice the two peaks of resistance corresponding to the turn on of the complementary device. The curves are asymmetric because of the differences between the models of the two devices, if they where exactly identical, not only the position but also the values of the maxima would be symmetric with respect to the middle point of the horizontal axis.

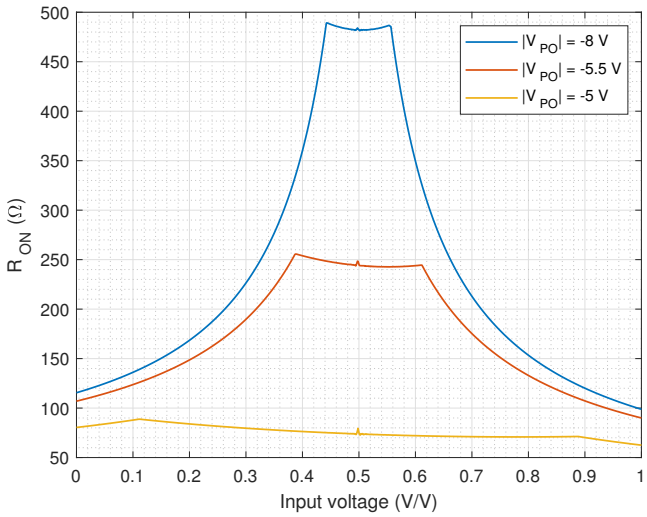


Figure 3.16: Simple *series-JFET* muting circuit block diagram.

Discrete transistors have worse matching characteristic with respect to the integrated solution. So it could be necessary to implement a second identical stage after the first one, in order to reach the desired attenuation with the switch open. Hence the overall circuit can become more and more complicated. In Figure 3.17 a complete possible implementation is provided. Figure 3.18 shows the driver block for the circuit of Figure 3.17, the inverter block is placed to get the complementary signal for the second driver. This inversion can be achieved in many different ways, substantially the requirement is that it has to be done as quickly as possible in order to not delayed too much the action of $\overline{V_{\mathrm{ctrl}}}$ with respect to V_{ctrl}.

Parallel configuration

The second possibility using JFET switches is the parallel connection topology, most commonly implemented in discrete form. In this circuit the switch works in a complementary way with respect to what happens in the series connection: the JFET is placed in parallel with the signal, so it has to be normally off and it provides a low impedance path R_{ON} to ground for the signal when the muting action is commanded.

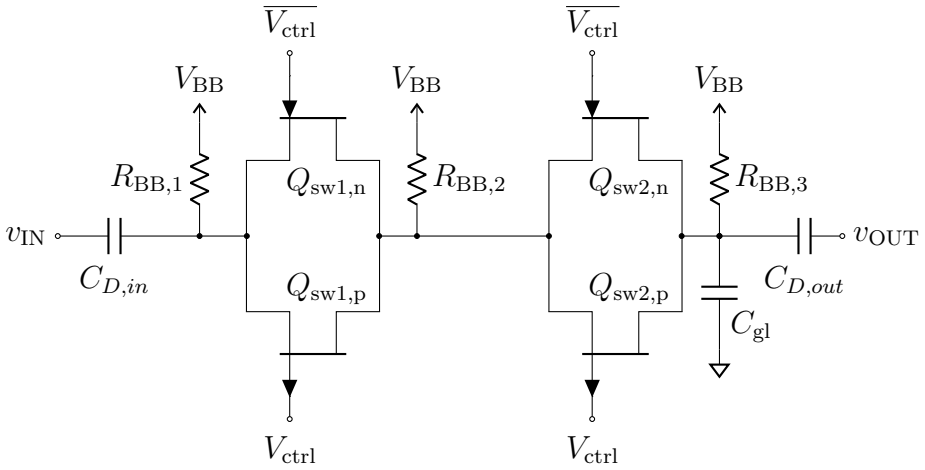


Figure 3.17: *JFET-series* muting circuit, with two stages.

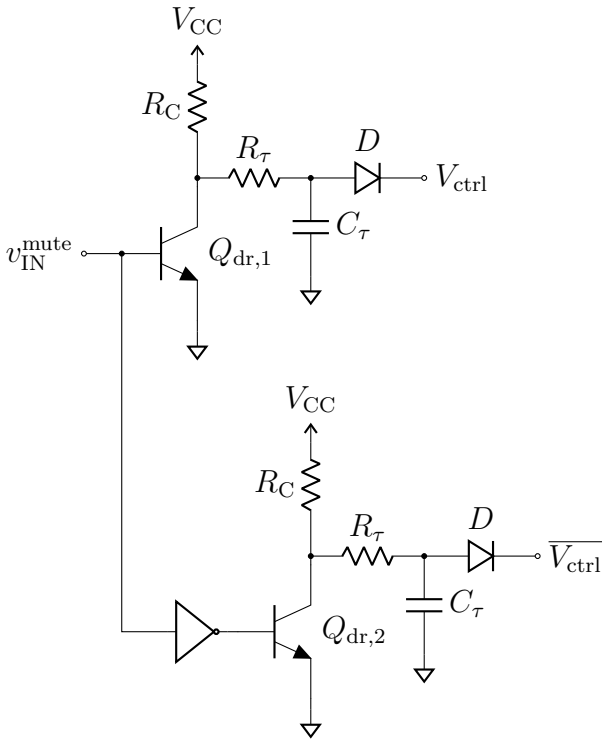


Figure 3.18: 2 stage *JFET-series* muting circuit driver.

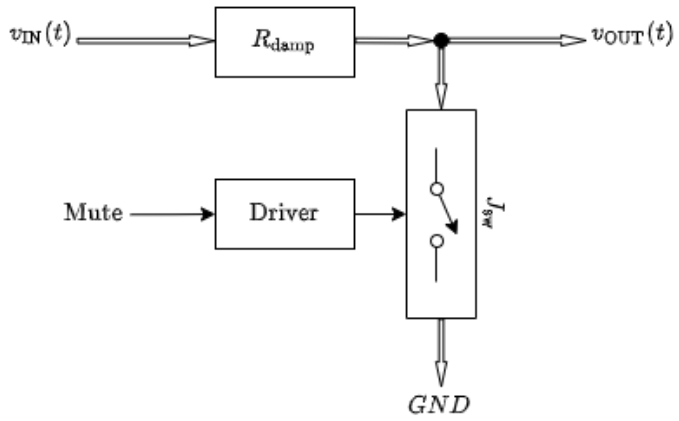


Figure 3.19: Simple *parallel-JFET* muting circuit block diagram.

From the functional prospective, the new block inserted in Figure 3.19 with respect to the diagram in Figure 3.13 is the R_{damp}. Its necessity is understandable considering the switch in an on state. If the JFET is on, its equivalent circuit can be represented as a resistor of value R_{ON}, this means that the input output relation of the overall muting circuit is the one of a voltage divider:

$$v_{\text{OUT}} = v_{\text{OUT}} \frac{R_{\text{ON}}}{R_{\text{ON}} + R_{\text{damp}}} \quad , \tag{3.10}$$

so that the attenuation in mute condition is the following one:

$$A_{\text{mute}} = 20 \log_{10} \left(\frac{R_{\text{ON}}}{R_{\text{ON}} + R_{\text{damp}}} \right) \tag{3.11}$$

So it is evident that in order to have an effective muting system it is essential that $R_{\text{damp}} \gg R_{\text{ON}}$, and this can be achieved by simply exploiting a resistor in series before the node at which the switch is connected. The value of this resistor has to be larger than a few kiloohm, depending also on how good is the behaviour of the JFET.

The driver block is absolutely analogous to the previous one and absolves to the same purpose. Considering a digital command with levels 0 V and 3.3 V, if the driver is identical to the one of Figure 3.14 the gate voltage of the p-channel JFET ends up to be at 9 V and ≈0.2 V respectively. The specie of the JFET is p because, being the threshold of the p-channel JFET larger than zero (the best solution in this case is that $V_{\text{PO}} \approx V_{\text{CC}}/2$ or a little less), the V_{GS} voltage is directly sufficient as it is to fully determine (at least in a first approximation) the behaviour of the device. If the source is at reference (as in Figure 3.20) the command voltage is directly found by looking at the command voltage at the output of the driver, so

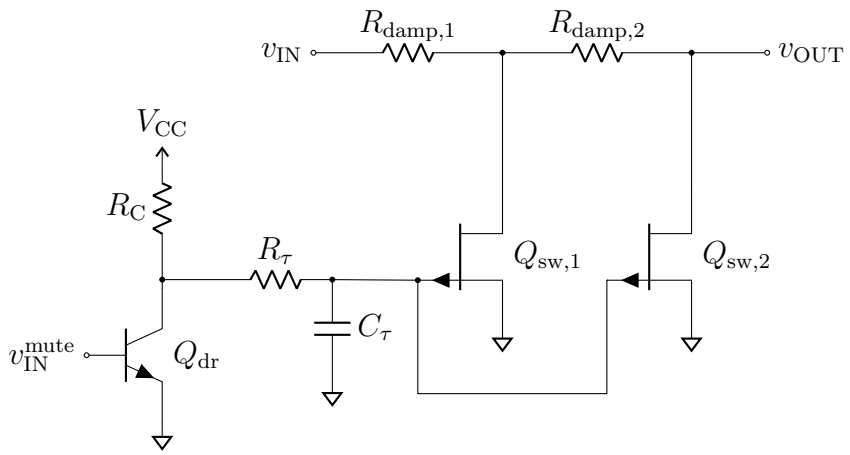


Figure 3.20: 2 stage *parallel-JFET* muting circuit.

when $V_{\text{IN}}^{\text{mute}}$ is low, the gate of the p-channel JFET is high and the switch is open, so that the mute circuit is not affecting the signal. Vice versa, if $V_{\text{IN}}^{\text{mute}}$ is high, the gate is approximately at 0 V, the switch is closed and the mute circuit is engaged.

If n-channel JFET were used, the muting circuit would have been always activated, since the gate to source voltage would never be lower than the threshold, which is negative. In addition to that, the following fact stands. With a gate to source voltage null, depending on the distance from the threshold, the JFET is on in a still safe region, with a V_{GS} voltage near V_{CC}, the device is surely broken since the gate connection has already started to let a large amount of current flow.

The great advantage of the parallel configuration against the series one is that in this case the command voltage of the device is decoupled from the varying incoming signal, which is arbitrary. If V_{GS} in on condition is sufficiently high, the signal oscillations (so the variation of source to drain voltage V_{DS}) are not sufficient to drive the JFET outside the ohmic region. This is a more simple to reach condition in comparison to the one in which the signal directly impacts the control voltage V_{GS} (*series-JFET* muting circuit) and this is the reason why there is no need for transmission gates.

Frequency responses of the JFET muting circuits

Especially when high frequency signals are involved, a topic which has to be discussed is the frequency response of the muting system when it is in transparent condition.

In the series configuration, the decoupling capacitors introduce an high pass action, which can be avoided only if a previously virtual reference is given, for

example through a single supplied op-amps based circuit. Anyway, their interference can be made negligible in the band of the device by wisely choosing their value according to the one of $R_{\mathrm{BB,1}}$ (for $C_{\mathrm{D,in}}$) and the load one.

A quite precise small signal model circuit for the muting circuit can be written, even it is quite heavy to solve and practically it soon gets useless by hand. The small signal model circuit has to be derived from the large signal model in the right operating region. The following circuit is indicated as muting system with one single cell; than multiple stage system can be derived by adding more identical sub-circuits.

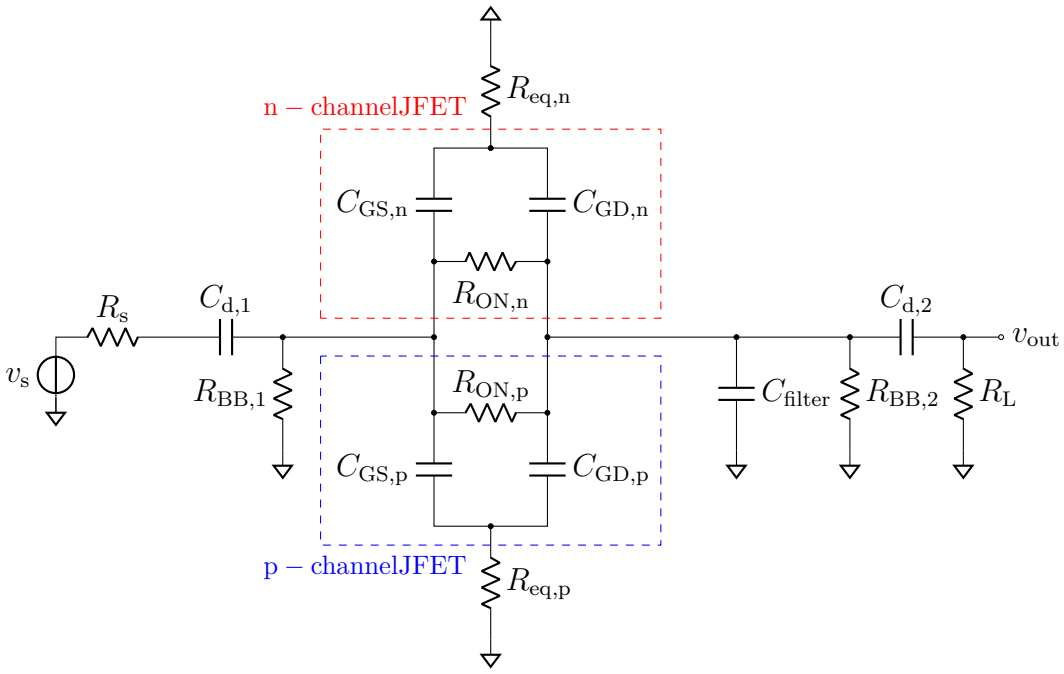


Figure 3.21: Small signal model of a single stage *series-JFET* muting circuit.

In the circuit in Figure 3.21 the on state model of the JFET switches are build with the resistance which models the channel of the device ($R_{\mathrm{ON,n/p}}$) and the two capacitances between the gate terminal and the entries of the channel ($C_{\mathrm{GS,n/p}}$ and $C_{\mathrm{GD,n/p}}$). Notice that the small signal equivalent circuit of p-channel and n-channel devices is identical. The unique difference in the remaining part of the circuit is the capacitor C_{filter} which acts as a low pass filter that avoids the presence of glitches, when the commutation between different states occurs.

The two resistances $R_{\mathrm{eq,n/p}}$ are the *Thévenin equivalent* resistances that are seen from the gates of the switches. Because the circuit above is drawn when the transparent condition holds, the equivalent voltage generator is switched off in the

small signal circuit, so that $R_{\mathrm{eq,n/p}}$ are grounded. Basically the following relations hold:

$$R_{\mathrm{eq,n/p}} = R_\tau + R_\mathrm{C} \parallel \frac{1}{h_{oe}}$$

The response of the circuit has a dominant low pass pole at high frequencies, whose cut-off frequency is fix by the series resistances $R_{\mathrm{ON,n}} \parallel R_{\mathrm{ON,p}} + R_\mathrm{s}$ and the filter capacitor C_{filter}. After this pole the magnitude response drops with a slope of $-20\,\mathrm{dB/dec}$, till it flattens to a specific level according to the values of the four capacitances $C_{\mathrm{GS,n/p}}$ and $C_{\mathrm{GD,n/p}}$. Since the devices are almost symmetric these capacitances are closed to each other in value.

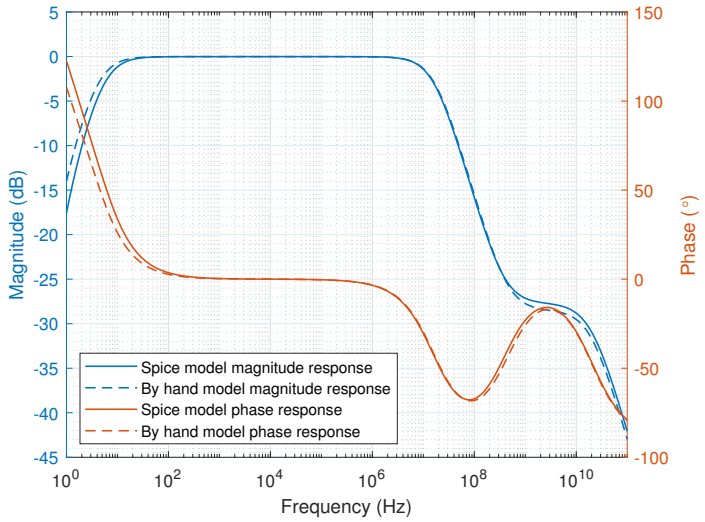


Figure 3.22: Comparison between the Bode plot obtained for a complete Spice model simulation or a simulation done by exploiting the circuit in Figure 3.21. Values are given in the text.

The by hand model solution plotted in Figure 3.22 has been drawn considering the circuit of Figure 3.21 and inserting values for the components that make the results of the simulation being consistent with the trace of the complete Spice model chosen as reference. To do this the following values have been used:

- $R_\mathrm{s} = 2.2\,\Omega$.
- $R_{\mathrm{eq,n/p}} = 50\,\mathrm{k}\Omega$, considering an $R_\mathrm{C} = 56\,\mathrm{k}\Omega$, an $R_\tau = 1\,\mathrm{k}\Omega$ and that the parallel between $R_{\mathrm{eq,n/p}}$ and $1/h_{oe}$ is dominated by the external resistor. Anyway, this resistance has a very little impact on the response with respect to the other elements, so its value is not crucial.

- $R_{\mathrm{BB},1/2} = R_{\mathrm{L}} = 1\,\mathrm{M}\Omega$.
- The channel resistances $R_{\mathrm{ON,n/p}} = 180\,\Omega$.
- The capacitances of the JFET model around a few pF: $C_{\mathrm{GS,n/p}} = C_{\mathrm{GD,n/p}} = 4\,\mathrm{pF}$.
- $C_{\mathrm{filter}} = 100\,\mathrm{pF}$

The values above are in line with the possible actual value of the sophisticated model: for instance the JFET model capacitances are higher for the J175 p-channel JFET chosen in the accurate simulation for which $C_{\mathrm{GS,p}} = 9\,\mathrm{pF}$ $C_{\mathrm{GD,p}} = 6.5\,\mathrm{pF}$. These values are twice the ones used in the less accurate model, but at the same time the model of the n-channel J201 (used in the simulation) shows the following values $C_{\mathrm{GS,p}} = 1\,\mathrm{pF}$ $C_{\mathrm{GD,p}} = 1\,\mathrm{pF}$, so that, on average, the results are close. If the last mentioned values are used, the discrepancy between the two responses at high frequencies reduces furthermore.

The parallel configuration can undergo the same procedure. In this case the situation is much simpler because of the different position of the switches. In transparent condition the signal only sees the extremely high resistance of the switched off channel (which can be approximated with an open circuit) and the $C_{\mathrm{GD,p/n}}$ capacitance connected to the gate, from which the *Thévenin equivalent* resistance and the $C_{\mathrm{GS,p/n}}$ capacitance go to ground. Also in this case a glitch filter capacitor has been added (C_{filter}). The derived small signal circuit is therefore the one in Figure 3.23. Also in this case a comparison between two simulations, the

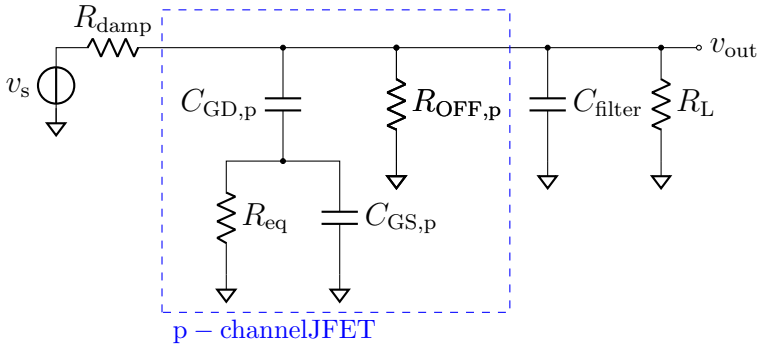


Figure 3.23: Small signal model of a single stage *parallel-JFET* muting circuit.

first done exploiting an accurate Spice model and the other one using this model present a quite successful result. The values used for the less accurate small signal model are the following:

- $R_{\text{damp}} = 10\,\text{k}\Omega$ which is considered as comprehensive of the signal source resistance, supposing the latter small compared to R_{damp}.
- $R_{\text{eq,p}} = 50\,\text{k}\Omega$ exploiting the same consideration as before.
- The capacitances of the JFET model around a few pF: $C_{\text{GS,p}} = 4\,\text{pF}$ and $C_{\text{GD,p}} = 9\,\text{pF}$ (very closed to the Spice model values).
- $R_{\text{eq,p}} \to \infty$, since the JFET is switched off the ensure transparency to the signal.
- $C_{\text{filter}} = 33\,\text{pF}$.
- $R_{\text{L}} = 1\,\text{M}\Omega$.

Exploiting these values the plot below is reported, making evident the simplification also in the shape of the response: a simple dominant low-pass filter, controlled by the R_{damp} and C_{filter}.

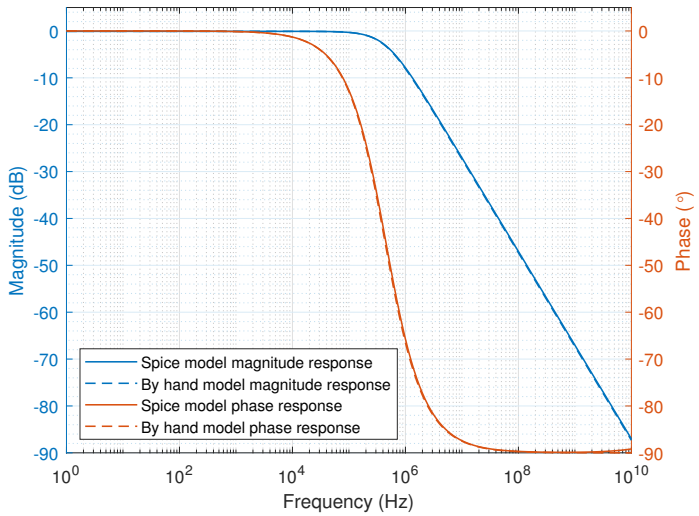


Figure 3.24: Comparison between the Bode plot obtained for a complete Spice model simulation or a simulation done by exploiting the circuit in Figure 3.23 with proper values.

An important difference between the two responses is that the cut-off frequency of the parallel configuration is pushed around a decade below in frequency with respect to the series case. This is because of the much larger resistance in series with the signal (in this case R_{damp} is nearly ten times R_{ON}) in the parallel configuration, in order to ensure a sufficient attenuation in muting operation. Anyway, also if the the response of the series configuration exhibits a zero after the cut-off, its action is limited, since the attenuation with respect to the passing band level is already

important and also because after it, as visible in the more accurate response, a new pole damps the response.

3.3.2 Optocoupler

The methods to implement an electronic switch are various, JFET transistor are one of these, but the exact same topologies can be realised basing the circuit on other devices. One alternative is represented by the use of *optocoupler*, technically, a device that is able to transfer electrical signals between to circuits, maintaining them isolated. This is possible thanks to the particular behaviour of semiconductors electrically light.

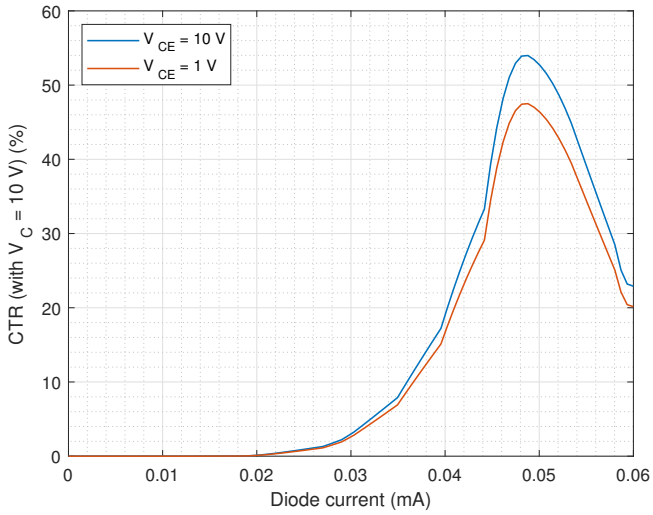


Figure 3.25: *Current transfer ratio* of an optocoupler. Derived from the Spice model of the H11A1.

On the input side of the optocoupler there is a light-emitting-diode, with an exponential characteristic in the ideal case, in practice some losses intervene making the curves approximate a straight line, far away from the knee point. The output side is a bipolar photo-transistor, whose base is sensible to the light. Hence, also the output characteristic is heavily non-linear. The parameter that is the most interesting for the development of the discussion is not dependent only on the optoisolator: the resistance seen from the collector of the photo-transistor to ground is evaluable through the *Ohm's law* as follow:

$$R_{\mathrm{CE}} = \frac{V_{\mathrm{CE}}}{I_{\mathrm{C}}} = \frac{V_{\mathrm{CE}}}{CTR \cdot I_{\mathrm{D}}}$$

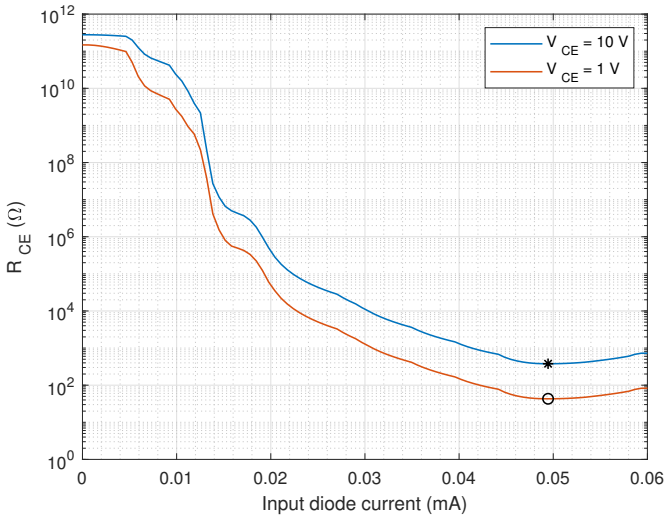


Figure 3.26: Resistance seen from the collector to ground (emitter grounded) for the H11A1. The two points point out the minima of the resistance curves: the lowest R_{CE} is equal to 378.5 Ω (for $V_{\mathrm{CE}} = 10\,\mathrm{V}$) and 43 Ω (for $V_{\mathrm{CE}} = 1\,\mathrm{V}$).

So it is evident that the voltage at the collector plays an important role in this calculation. In the previous equation, the *current transfer ratio* CTR has been used, being the parameter that relates the output to the input current (visible in Figure 3.25).

In the applications below, the voltage at the collector is often determined by the signal, so it is almost impossible to predict what would be the exact values of the equivalent R_{CE} resistance. The point here is that it is important to ensure a correct amount of input current in order to have an R_{CE} smaller than a certain maximum value.

Series configuration

The series (and also parallel) configuration is identical, from the block diagram prospective, to the JFET solution because the position of the switch is identical, independently on the device that implements the switching functionality.

To provide a decent amount of attenuation, also in this case two identical stages have been placed in sequence. In the present case, since the conductivity of the devices depends on the light incident on the base of the phototransistor, the circuit is much simpler than the JFET solution one, since the signal at the emitter terminal has a much lower impact on the state of the device. In practice this means that there is no need for topologies equivalent to the transmission gate in some sort, or other techniques.

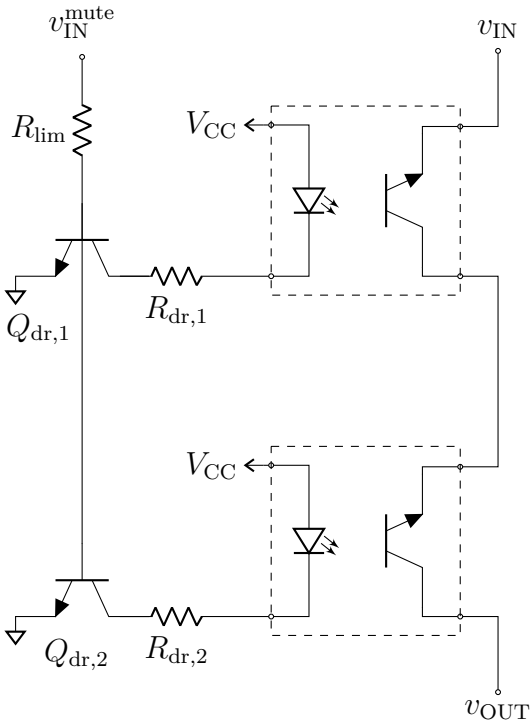


Figure 3.27: 2 stage *series-optocoupler* muting circuit.

The circuit in Figure 3.27 is a possible implementation of a two stage *series-optocoupler* muting circuit. One important difference between this solution and the previous (JFET based) one is that in the field-effect-transistor circuit the gate does not sink any current. This reflects into a driver circuit which has not to make any effort in supplying any current to the switch. On the contrary, the optocoupler is controlled in current and so the driver of the switch has to be a current, in place of a voltage, driver. The modification is easily done by connecting the switch in series with the transistor driver instead of in parallel.

The muting command is applied to the base of the driver as usual and the collector of the *npn* transistor is connected to the diode anode of the coupler with a current limiting resistor. Notice that this low side solution can be replaced with an high side *pnp* based one with the same results. Since the on state current needed to obtain a sufficiently low resistance at the output of the coupler can easily sit in the range between 10 mA and 30 mA, it is better to allocate for each optocoupler its own driver. In general, if the estimated dissipation grows, then a parallel connection of resistors and/or transistors can be implemented eventually correcting their values.

Parallel configuration

The parallel counterpart of the circuit in Figure 3.27 is the one in Figure 3.28. As seen in the JFET dedicated section, the insertion of the resistors $R_{\text{damp},1}$ and $R_{\text{damp},2}$ is necessary for obtaining the desired attenuation when the switches are closed. Similarly to the *series-optocoupler* solution the drivers are current sink, but also the current source solution is possible. The freedom that is present in optocoupler circuit in choosing the driver circuit is due to the fact the the optocoupler are devices which galvanically isolate the two branches of circuit they are connected to.

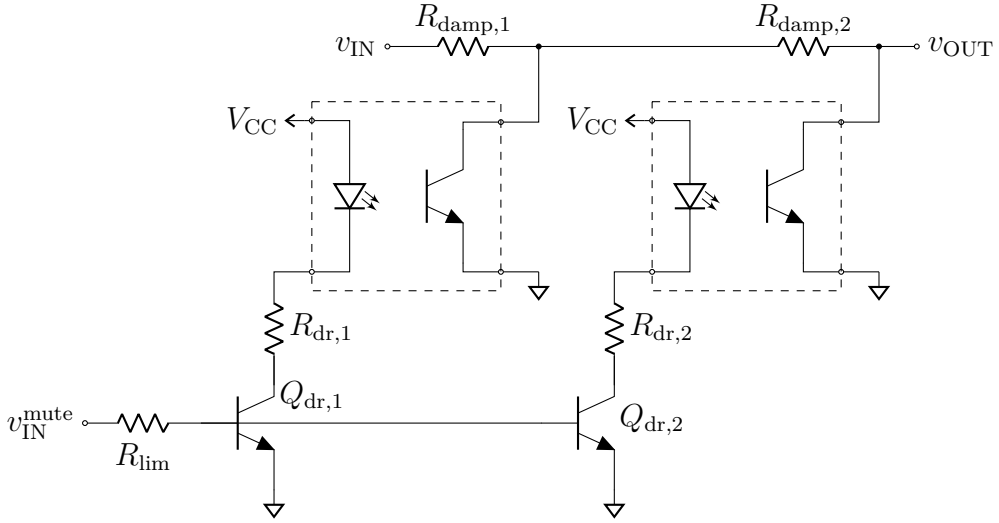


Figure 3.28: 2 stage *parallel-optocoupler* muting circuit.

Since, in this configuration, the switches are closed only when the muting command is given, an advantage of the parallel connection with respect to the series one is evident. The current needed to activate the optocoupler in the proper way flows only when the command signal $v_{\text{IN}}^{\text{mute}}$ is high, so that in normal operation no power is dissipated to maintain the on state. In the series configuration, the transparent condition is obtained with the switch closed, so the normal situation is with the internal LED always on. This means that if the muting circuit stays activated for 50% of the time, the two solutions are nearly equivalent, but, if the muting command is given only for short period of time (as it is likely to occur), the series configuration ends up to waste a noticeable amount of power.

Frequency response of the Optocoupler muting circuits

It is quite useful to analyse the frequency responses of the muting circuits in transparent condition, as done for the JFET circuit. To do so a dynamic model of

the optocoupler is needed, including its the parasitic elements. In this model, the diode driver side of the component is completely negligible because of the galvanic isolation between the two circuits.

In the majority of the datasheets, the parameters reported are the input capacitance (diode side, C_{D}) and the output collector to emitter capacitance C_{CE}. Whilst the C_{D} is relevant for computing the response time of the control driver, the latter is the most important in this case. The circuit below (Figure 3.29) is the resulting small signal circuit, considering the most relevant parasitic elements. The usual glitch filter capacitor C_{filter} has been added.

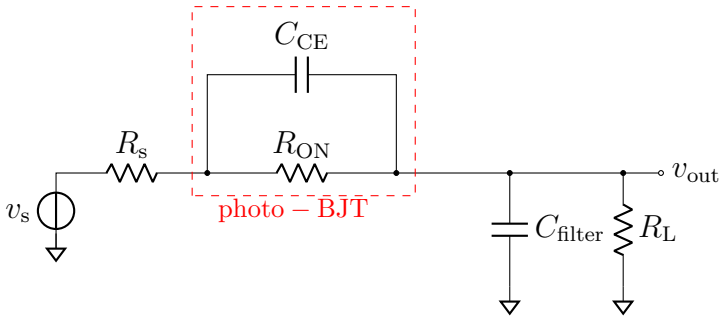


Figure 3.29: Small signal model of a single stage *series-optocoupler* muting circuit.

The resulting response is a magnitude curve that, for low enough frequencies, is dominated by the resistive voltage divider realised by R_{s}, R_{ON} and the load R_{L}. Since usually this ratio is quite close to 1 ($R_{\mathrm{s}} + R_{\mathrm{ON}} \ll R_{\mathrm{L}}$) the attenuation in band is usually quite low in absolute value. For frequencies high enough, so that the reactance shown by the two capacitors is much smaller than each resistances in parallel to them, the output is again the result of a voltage divider, but this time done considering the ratio of the capacitances C_{CE} and C_{filter}. In between the two regions a portion of the curve with a slope of $-20\,\mathrm{dB/dec}$ is present and its length is determined by the interaction between the two capacitances and the channel resistance, which controls the frequency of the cut-off.

The values found for the C_{CE} capacitance in order to make the two curves match is much higher than the average of the one written in the datasheets.

In the parallel configuration the values for the collector to emitter capacitance found in the datasheets and the Spice model results match quite well. This is because no other effects, such as *Miller effects* modifies the value of capacitance seen from the node at which the switch is connected.

As is visible in Figure 3.31, the phototransistor in off state can be simply modelled with an open circuit, still with the main C_{CE} capacitance in parallel towards ground. This configuration leads to the introduction of a single dominant low pass filter, since the parasitic capacitance will sum to C_{filter}. Since usually

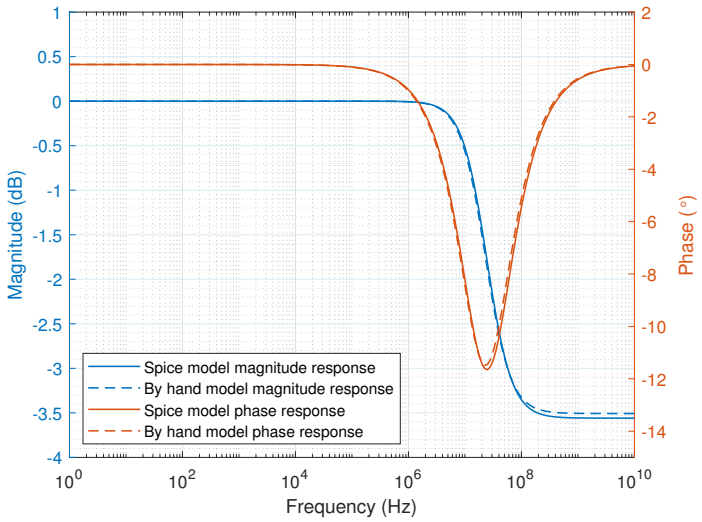


Figure 3.30: Bode plot for the circuit in Figure 3.29 with the result of a more accurate Spice model, for comparison.

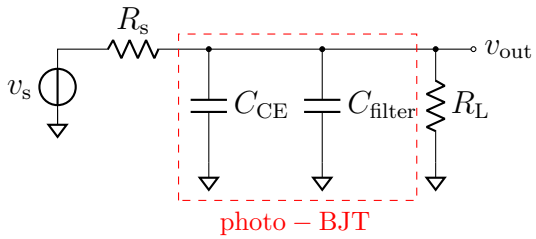


Figure 3.31: Small signal model of a single stage *parallel-optocoupler* muting circuit.

$C_{filter} \gg C_{CE}$ and being the resistance R_{damp} noticeable, this two elements are the one that determine the response of the circuit.

The values given by the datasheets make the two curves match perfectly in this case, also because the value itself of C_{CE} is not fundamental in determining the position of the dominant pole.

Anyway, all this frequency behaviours occur for very high frequencies, *e.g.* above one MHz and this holds both for JFET or optocoupler circuit and both for series or parallel configurations. So at least in audio application the band requirements of the circuit are easily matched. The choice between this four circuits seen till now depends on the resources available but in general is better to avoid the series configuration. The parallel design is usually more easily controllable and predictable, moreover it does not require more complicated solutions such as the transmission

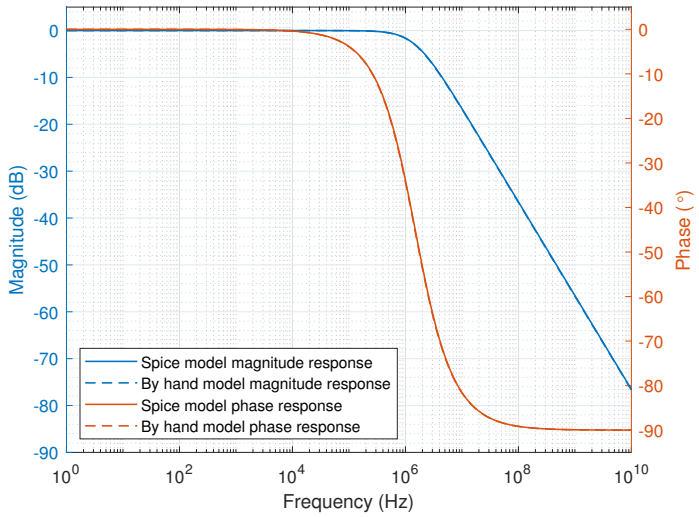


Figure 3.32: Bode plot for the circuit in Figure 3.31 with the result of a more accurate Spice model based one.

gate design.

In any case, both for series and parallel configuration, but more critically for the parallel one, a high impedance load is required. This is because the loading effect has a serious action on the frequency responses: for instance in the parallel configuration the R_{damp} resistors will drop the level of the signal if the load has not a sufficiently high impedance. This situation make advisable the use of a signal buffer after the muting system. The buffer does not require the integration of potentiometer, since it is fixed in gain, hence it is not a source of noise and can follow the muting system.

3.3.3 Other switching solution - Relay, other transistor, SS analog switch

To exploit the switching function different devices can be considered. In the previous sections two of them have been mentioned and explored, JFET and optocoupler, but at least two others deserve a mention.

BJT A third possible solution is the use of other types of transistors, for instance BJT. In every aspect the possible circuits are very similar to the JFET one: still a driver is needed to correctly force the device in the proper region. Also in this case a parallel configuration followed by a buffer is the more reliable solution, compared to the series one. The principle difference with respect to the JFET circuit is in

the driver design. Because the BJT are controlled in current instead of voltage, one more stage in the driver is usually needed. In a block diagram prospective the situation is a circuit in which not only a voltage translation block is present, as already seen (to amplify the V_{DD} digital supply swing to the higher V_{CC} analog supply one), but also a voltage to current transducer is placed.

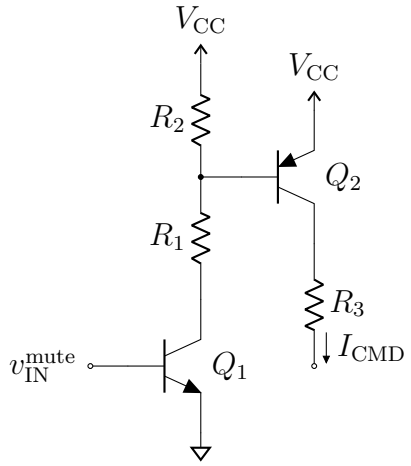


Figure 3.33: Driver circuit for a *parallel-BJT* muting circuit.

In Figure 3.33 Q_1 is the usual voltage driver, but its collector is not directly connected to the switch, instead the drop on the resistor R_2 controls the current source Q_2. This PNP transistor generates the current that drive the switch through the limiting resistor R_3. Despite this difference the circuits are analogous, also from the frequency response point view. In practice in place of the channel to gate capacitances, C_{GS} and C_{GD}, the C_{BC} collector to base and C_{BE} emitter to base capacitances are present. In addition to that the emitter to collector capacitance C_{CE} is noticeable. As a matter of fact, the situation is not changed and in this field a simple Spice simulation can give good insights into the frequency behaviour of the stage.

Relay This solution is completely different from the previous ones, since the relay is an electro-mechanical switch. This component can ensure an almost perfect either isolation or connection of the circuit output, because, once the switch is stable in one position, the path of the signal is granted only by metal element, no resistances of any sort are involved[7]. Similarly to the optocoupler circuit, the

[7]Technically the resistance of the metal part of the switch that conduct the signal is present, but usually this is extremely small compared to the transistors' one: it is usually smaller than $1\,\Omega$

isolation between the driver and signal branches of the circuit is ensured.

Traditional relays are usually much more bulky than transistor, so normally they are not involved in design in which the room available for the component is important. Moreover, also this solution require a proper driver, in this case it must be able to energise the solenoid of the relay, through a sufficient current flux.

The parasitic elements introduced by an electro-mechanical switch are almost negligible in comparison to the ones introduced by electronic switches. In particular the series resistance can easily sit below $1\,\Omega$, making the exploitation of these devices absolutely tempting. A downside of this choice is the possible introduction of spikes and glitches due to the physical movement of the mechanical parts, which are either in series or in parallel[8] to the signal itself. In the datasheet the capacitance across the terminal of the switch when it is open is reported, even if normally it is below the pF.

An important fact is related to the timing characteristic of the devices. Normally two different intervals are given: the *operating time*, measured from when the coil begin to energise to the moment in which the last[9] mechanical operation is finished and the *release time*, measured from the instant in which the supply is disconnected from the coil and the moment in which the last mechanical operation terminates. This two intervals depend on the complexity of the device under test, but normally they do not exceed a few ms (*e.g.* 3 ms at maximum)

Analog multiplexer For what concerns the transmission gate solution presented in the JFET muting circuit section, there is an already implemented solution that exploits exactly this principle. On the market, many types of analog multiplexers or switches are present. These devices present at least two terminals, for the input, output, eventually bidirectionally, and a third control terminal. Their usage is very simple in principle and they usually present very low series resistances. For instance the CD4066 (a very common chip) has on board four independent single pole single through switches. The R_{ON} of the switches increases with the supply voltage (which must be in the interval with respect to the V_{SS} terminal, from 3 V to 18 V, from -0.5 V to 20 V for the absolute maximum ratings) and also with temperature. For a supply of 15 V the resistance R_{ON} shows the same curve of Figure 3.16 with peak values around 100 V at 125 °C. So if they are used in the right conditions these analog switches can be extremely handy, and the acceptable performances are ensured by the fact that the CMOS technology design is in this

[8]Consider that if the configuration is parallel, probably a limiting resistor in series with the grounded terminal is needed in order to prevent the output of the preceding circuit being grounded, for instance damaging the output of an op-amp.

[9]In case the device contains multiple sections.

case tailored to fulfil the analog preservation requirements, on the contrary with respect to generic discrete parts. In Figure 3.34 two versions of the transmission gate symbol are visible, with the input and output on the horizontal line and the control on the top pin.

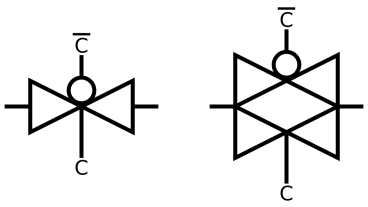


Figure 3.34: Transmission gate symbol. Normally the complementary control signal is internally generated, so that only one control has to be send to the gate.

3.4 Noise solution - Shutdown

In some cases it is possible to implement a muting circuit directly exploiting the functionalities available on board of some potentiometers. In particular some of them are provided with a dedicated pin, called *hardware shutdown* $\overline{\text{SHDN}}$, whose function is normally disabled. When the signal at this terminal is a logic false (in many case this condition corresponds to a high voltage level since the signal is active low) the potentiometers terminal are normally connected. When $\overline{\text{SHDN}}$ is commutated to a low logic level, one terminal (A for instance) is disconnected from the externally accessible pin and the other one (say B) is connected directly to the wiper W.

This is the natural implementation of a muting system, if B is connected to ground and A is the terminal from which the signal is injected into the device. The important condition *sine qua non* the *shutdown* method can be implemented is the fact that the potentiometer can not be in any position of the circuit. To make sure that the operation is efficient, the ideal situation is the one of a potentiometer used as a voltage divider at the output of the circuit, as in Figure 1.57 (eventually without any other potentiometer involving circuit after it along the signal's path). If the potentiometer is used as a voltage divider as in Figure 2.19 the shutdown method does not operate as intended, since the gain of the amplifier is commutated between a value, set by the potentiometer and 1, when the shutdown is activated[10].

[10]This holds if the terminal connected to the amplifier output is consider as the B terminal. In the opposite case the shutdown command will immediately drive the amplifier in saturation

A great advantage of this muting method is the fact there is no need for a driver able to control a switch of any sort, because the isolation is ensured directly by the internal circuit of the potentiometer. Hence, the signal coming from the microcontroller is sufficient to enable or disable the operation. This is also commonly ensured by the fact that the supply of the digital part is clearly common to both the microcontroller and digital potentiometer.

condition.

Chapter 4

Experimental results

A practical implementation in a realistic system is needed, in order to evaluate the previously theoretically discussed solution. This approach allows also a direct comparison of the different alternatives, for example concerning the muting circuits, based on direct measurements of their performances. This is done considering that some hints given in the previous sections hold in any case and so they are not discussed here even if they are used. For instance, the control of an amplifier gain with the ratio of the two resistances seen from the wiper instead of exploiting the absolute value of the potentiometer is considered in the following. The experimental system specifically designed for this purpose is composed by two separate boards: one is the one dedicated to the digital control, the other is the board containing the analog circuits to be implemented and discussed. These two boards are connected with headers and a few of external connection are made accessible externally to facilitate the measurements operations. The measurements to be taken are related to the fundamental characteristic of the circuits involved, for instance gain and bandwidth of an amplifier, or the attenuation of a muting circuit in off state. This data will lead to the possibility of a synoptic comparison of the different possibilities. The experimental set up will include the board and some basic electronic laboratory devices such as power supply, oscilloscope, signal generator.

4.1 Digital control

The digital control board has been developed by Carlo Sorasio (for LAA Custom[1]) and it houses a microcontroller (STM32L451xx) and two quad digital potentiometers, plus all the electronics that this main components require, for example the power supply block.

[1] `https://www.laa-custom.com/`

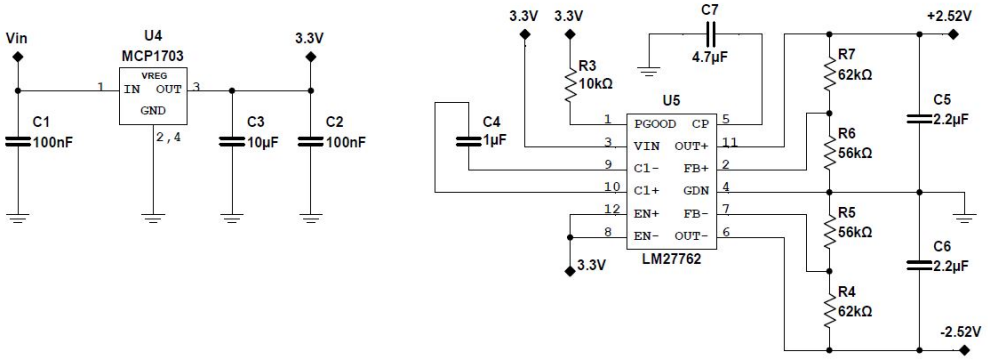


Figure 4.1: Power supply circuit for the digital board: 3.3 V and dual ±2.5 V generator.

In Figure 4.1 the supply portion of the circuit is reported. The V_{IN} terminal is connected to a header from which the supply has to be injected. From this external supply, a first block generates a stable 3.3 V using a MCP1703, which implies that V_{IN} must meet two conditions: $V_{\text{IN}} > 2.7\,\text{V}$ and $V_{\text{IN}} > V_{\text{drop}}^{\text{MAX}} + V_{\text{OUT}}^{\text{MAX}}$ [12]. This means that in this application $V_{\text{IN}} > 4.4\,\text{V}$. In the present experiments, the supply of the two boards is set to 9 V. The second block is a charge pump, that provides two regulated output voltages: at +2.5 V and -2.5 V. The chip used is the LM27762, whose basic circuit has been discussed in section 2.2.3.

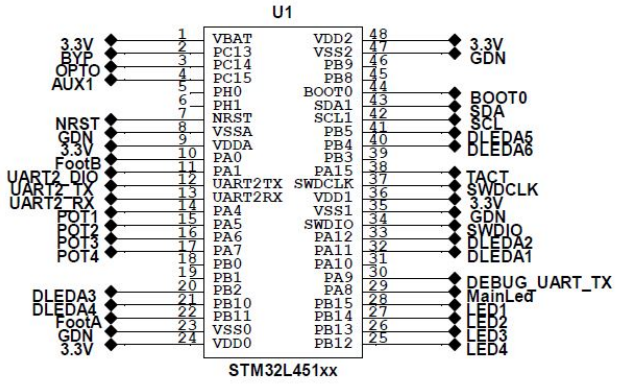
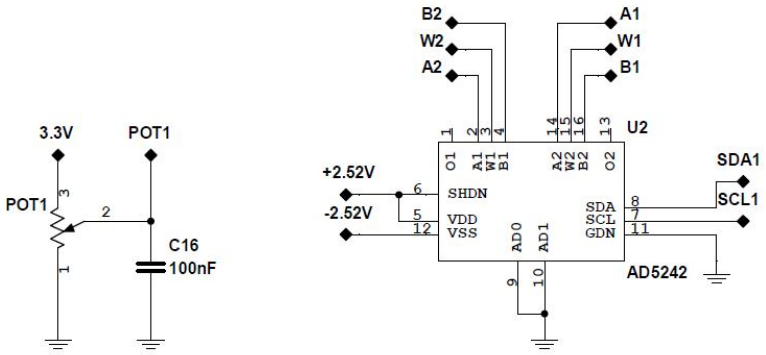


Figure 4.2: Microcontroller connection.

In Figure 4.2 the microcontroller connections are shown. The supply connection to the positive and reference terminal of the supply are not consider now but they are visible anyway. The board is configured to fulfil many tasks so that for example the possibility of controlling the behaviour of the circuit with a UART line, or also the possibility of re-loading the firmware of the microcontroller. The first functionality is related to the pin numbers 11 (UART2_DIO), 12 (UART2_TX)

and 13 (UART2_RX) whilst the second one is linked to the use of the pin 7 (NRST), 30 (DEBUG_UART_TX), 34 (SWDIO) and 37 (SWCLK). Namely this connections are made accessible from the external of the board through some dedicated headers on which also a supply connection is made (GND and 3.3 V).

The communication with the digital potentiometers is done with the SPI protocol through the pins 43 (SDA) and 42 (SCL). But the system in this case is set up in a more complicated way. The digital potentiometers are controlled in the way seen above, but the value given by the microcontroller is determine from the external in two different ways. The four available digital potentiometers (two per each chip) are associated to the voltage at four each corresponding inputs of the microcontroller: 14 (POT1), 15 (POT2), 16 (POT3), 17 (POT4). The voltage on these four pins is continuously sensed by the microcontroller that drive the potentiometers accordingly. This organisation allows the external user to interact in different ways with the device: either with an analog potentiometer connected as a voltage divider with the wiper sent to the microcontroller input or simply with an external voltage control. In this thesis, an important signal to be considered is the one labelled as OPTO because it is the signal that command the muting system. To facilitate the experiments this signal is not brought directly to the analog board, instead this connection is left open so that also an external signal can drive the muting circuits.



(a) Analog control to the microcontroller.

(b) Digital potentiometer connection.

Figure 4.3: Potentiometer arrangement on the digital control board. On the left the analog potentiometer used for external control of circuit. This type of control has been prepared for all the four digital potentiometers, then, if the direct voltage control is desired, the connection is simply soldered to the central pin of the analog omitted potentiometer. On the right there is the digital potentiometer connection. The configuration shown is duplicate for the other AD5242.

Potentiometer 1 and 2 are driven by an analog potentiometer voltage divider as

visible in Figure 4.3. The capacitor from wiper to ground is there for noise purposes, in order to stabilize the voltage at the microcontroller input. Potentiometers 3 and 4 are controlled by an external voltage directly connected to the microcontroller inputs.

The connection to the digital control board are the 9 V and reference supply fundamental to the functioning of the system, but, in addition to that, also the ± 2.5 V are taken from the digital board where the charge pump operates, and made available on the analog board for the op-amps supply. In the very same way, the 3.3 V is brought to the inverter, used to generate the complementary muting command. Clearly the ladder resistor chain connections of the digital potentiometer are brought to the analog board in order to be used in the circuits discussed in the following.

4.2 Analog board - amplifier

The analog board has been specifically designed to work in conjunction with the digital control above overviewed. In Figure 4.4 a photograph of the complete two board system is shown. The green board is the digital control dedicated one, while the black below is the analog circuit one which is described in the following. The green wire on the right is the connection for the muting command voltage. All the connections left open are visible in correspondence of the female header, so that they can be arranged as wanted using jumpers. Notice the red and yellow and black wires that bring the dual supply and the reference from the control board and make it available on the analog board. The momentary switch connected on the bottom of the image can be used to switch between the four different presets that can be stored into the microcontroller. The major difficulties in the realisation of this set up has been represented by the managing of all the different connection between the planes and some errors have been recovered through the process.

The first circuit implemented is the one in Figure 2.21 with the following values: $C_{\mathrm{IN}} = C_{\mathrm{OUT}} = 100\,\mathrm{nF}$, $R_{\mathrm{BB}} = 620\,\mathrm{k\Omega}$, $R_{\mathrm{min}} = 1\,\mathrm{k\Omega}$. C_{f} was left changeable by the user, in order to allow for bandwidth comparisons in the different possible configurations (with and without C_{f}, and with different values of this capacitor).

The main difference with respect to the circuit of Figure 2.21 is that another potentiometer has been put as a volume control after the op-amp stage, in the configuration of Figure 1.57. This is always in a prospective for which the aim of the measurements set is to give a basis for a comparison between different solutions. Being the configuration non-inverting, the minimum gain is one, obtained when

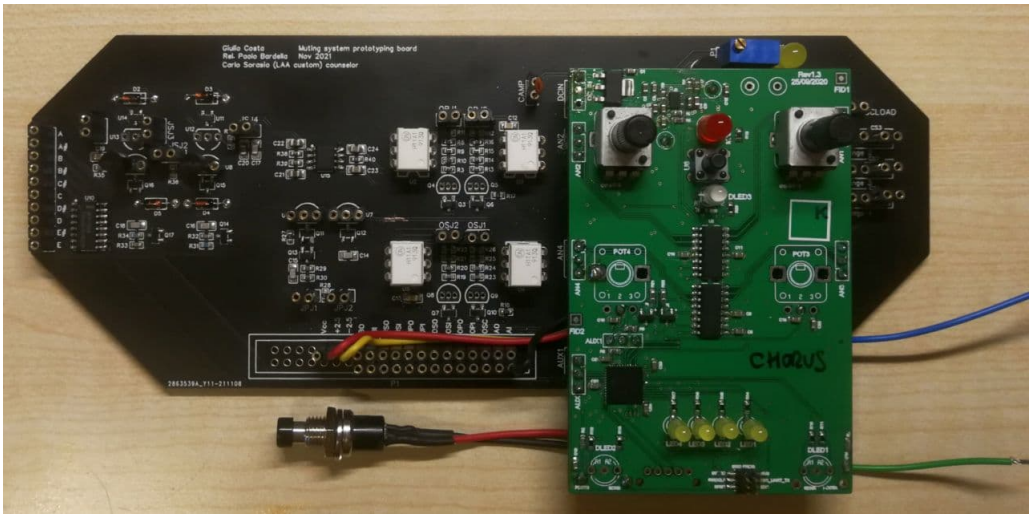


Figure 4.4: Experimental board photograph.

the resistance of the divider is all on the inverting input to ground side:

$$A_{\mathrm{v}}^{\mathrm{min}} = 1 + \frac{0}{R_{\mathrm{pot}} + R_{\mathrm{min}}} = 1\,\mathrm{V\,V^{-1}}$$

$$A_{\mathrm{v}}^{\mathrm{MAX}} = 1 + \frac{R_{\mathrm{pot}}x}{R_{\mathrm{min}} + R_{\mathrm{pot}}(1-x)} = 101\,\mathrm{V\,V^{-1}} \approx 40\,\mathrm{dB}\ .$$

So it is evident that, with an input signal whose amplitude is 10 mV, for example, the output signal will remains in the dynamic of the op-amp of choice, the OPA2134. Because the margin of linearity for high impedance load are $V_{\mathrm{SS}} + 0.5\,\mathrm{V}$ and $V_{\mathrm{CC}} - 1.2\,\mathrm{V}$ [13], a 1.01 V amplitude signal is correctly amplified. The op-amp starts to saturate the output voltage for input signals of amplitude 12.87 mV if the gain is maximised. Therefore, for an input signal of amplitude 50 mV the gain potentiometer placed in the feedback loop can drive di op-amp into saturation if it exceeds a certain threshold. The potentiometer placed after the amplification stage as a voltage divider has no effect on the operation of the amplifier. So if the designer is able to ensure that the input signal has not an amplitude sufficient to make the op-amp to saturate (or similarly, that for the largest input signal amplitude, the gain of the amplifier is not able to drive the op-amp into saturation) any variation of the potentiometer in any range of its swing is allowed. To ensure the linearity, the solution with the potentiometer in the feedback has to be limited in its range by a proper R_{min} resistor[2].

[2]Notice that R_{min} has always to be included into the design in order to make the ratio in the gain expression being limited. This avoid unwanted behaviour.

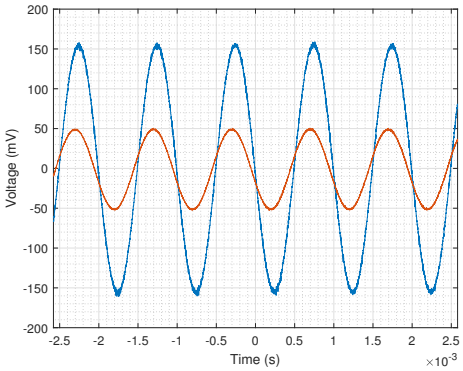
The capacitor C_{in} and C_{out} are present for decoupling purpose, when the op-amp is for example single supplied and a virtual reference is needed (connected to R_{BB}). In this case also a third decoupling capacitor is needed between the feedback and ground, in series with R_{min}. In this case the signal is referred to 0 V and the op-amp is dual supplied, so theoretically the decoupling capacitors are useless, but if they are sized in a way so that they not impact the bandwidth of the amplifier they can be included to reduce the response in DC. The new expression for the gain is the following one, simply derived from Eq.2.7 with the introduction of R_{min}.

$$A_{\text{v}} = \frac{1}{1 - x + \dfrac{R_{\text{min}}}{R_{\text{pot}}}} \tag{4.1}$$

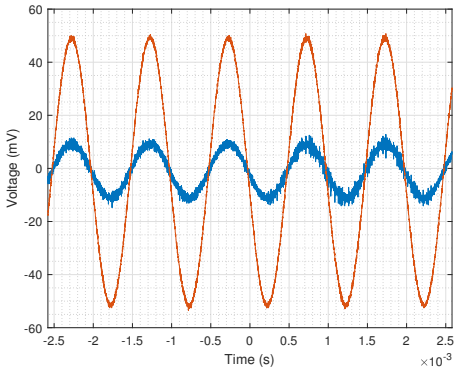
The resistors solder onto the board, are Yageo SMD 0603 at 1% tolerance [14], while the capacitors are MuRata SMD 0805 at 10% tolerance [15]. The transistors are J175 (p-channel, Onsemi [16]) and J201 (n-channel, Fairchild [17]), while the op-amps are OPA2134 (Texas Instrument [13]). In the following, the voltages measured across the potentiometers in different conditions are reported. These measurements have been taken with the Analog discovery 2, an *"high performance, all-in-one USB oscilloscope & instrumentation system"*[3]. For what concerns the feedback inserted potentiometer, in this case, since a limiting resistor R_{min} is inserted, the voltages across its terminals must not be measured with respect to ground. In Figure 4.5 left, the voltage at the output side terminal of the potentiometer is reported (yellow trace), while the blue trace is the input waveform. The first trace is also the output voltage of the amplifier (considering negligible the effect of the decoupling capacitor) and it is reported for a value of gain that still preserve the linear condition (with a 50 mV peak input sinusoidal signal). Clearly the linear condition implies that the difference between the inverting and non-inverting inputs of the op-amp is negligible and so $v_{\text{W}} \equiv v_{\text{in}}$.

The voltage drop on the resistor R_{min} coincides with the voltage at the third remained terminal of the potentiometer and it is variable with the gain, in accordance

[3]The oscilloscope of the Analog Discovery 2 is a 2 channels, 14-bit, 100 MS/s (mega-sample per second), with a bandwidth of 30 MHz, input impedance of 1 MΩ and a permissible voltage range of ±25 V. Also the input signals have been generated with the Analog discovery; the signal generator is a 2 channels, 14-bit, 100 MS/s, 12 MHz bandwidth, output impedance of 1 MΩ and a maximum output amplitude of ±5 V. Also the network analyser has been used and it works in conjunction with the oscilloscope, with a frequency range from 1 Hz to 10 MHz and frequency steps from 5 to 1000. `https://digilent.com/reference/test-and-measurement/analog-discovery-2/reference-manual`



(a) Voltages v_{out} (blue) and v_{in} (red).



(b) Voltages v_{min} (blue) and v_{in} (red).

Figure 4.5: On the left, the input and output voltage of the amplifier are plotted for a gain of approximately $3\,\text{V}\,\text{V}^{-1}$. On the right, the input and R_{min} resistance voltage are reported for a value of gain of approximately $17.38\,\text{V}\,\text{V}^{-1}$, the different value of gain with respect to the left plot is done in order to make the drop on R_{min} more visible. The measurements have been taken with the Analog Discovery 2 (Digilent).

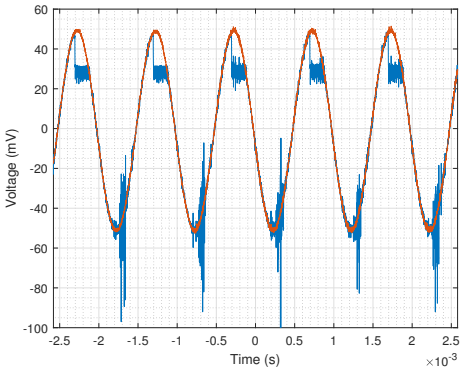
with the following expression:

$$v_{\text{min}} = v_{\text{inv}} \frac{R_{\text{min}}}{R_{\text{min}} + (1-x)R_{\text{pot}}} \ . \tag{4.2}$$

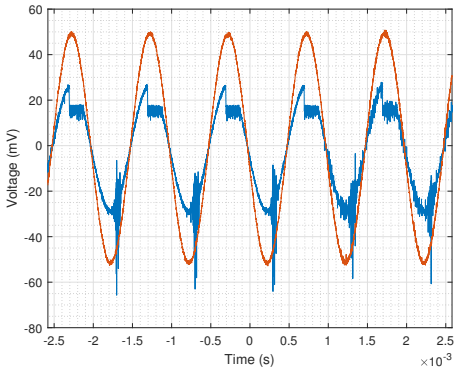
The voltage on the minimum resistor is the result of the voltage divider formed by R_{min} and the portion of potentiometer on this side of the inverting input node. So for increasing gain, $x \to 1$, the voltage $v_{\text{min}} \to v_{\text{inv}}$. In Figure 4.5 right, as expected, the blue trace representing the v_{min} voltage is smaller, since for a gain $A_{\text{v}} = 17.38$ the corresponding value of x is 0.9425 which, once it is substituted into Eq.4.2, gives an amplitude for v_{min} equals to 7.41 mV (still considering a 50 mV peak input signal).

This situation changes completely in saturation condition, when the output voltage clamps and so the potentiometer output terminal voltage and the inverting input voltage with respect to ground (followed by v_{min} through the voltage divider). Figure 4.6, both left and right, refer to a saturation condition. Notice that for this high gain values ($44\,\text{V}\,\text{V}^{-1}$) $x \approx 1$ and $v_{\text{min}} \approx v_{\text{inv}}$. In this particular saturation condition the characteristics of the op-amp are crucial. In fact, the clamp in the inverting input voltage and R_{min} voltage are only on the top portion of the wave, so it is clear that the upper rail of the op-amp below linearity is preserved is lower in absolute value than the one of the negative side. This is confirmed by the OPA2134 datasheet [13].

In Figure 4.7, the voltages across each terminal of the potentiometer are reported as well as the current entering each terminal. In doing this the op-amp is considered



(a) Voltages v_{out} (blue) and v_{in} (red).



(b) Voltages v_{min} (blue) and v_{in} (red).

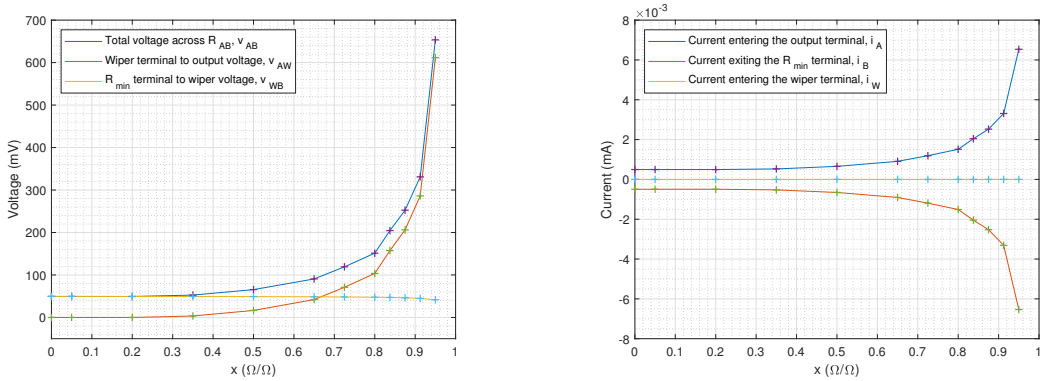
Figure 4.6: On the left, the input and inverting input voltage of the amplifier are plotted for a theoretical gain of approximately $44\,\text{V}\,\text{V}^{-1}$. On the right, the input and R_{min} resistance voltage are reported for the same value of gain. The still lower peak value of v_{min} with respect to the inverting input voltage is due to the fact that the theoretical gain is not maxed yet. The measurements have been taken with the Analog Discovery 2 (Digilent).

ideal and so the current flowing into the wiper terminal of the potentiometer is null, being it in series with the inverting input of the op-amp. The curves reported refer to peak values of the waveforms (both for voltages and currents). The power dissipated is calculated in a very simple way and it is referred to the RMS values (which are quick derived assuming that in linearity a sinusoidal input produces a sinusoidal output). It is reported in Figure 4.8 for different values of x. Since

$$P_{\text{pot}} = V_{\text{A}}^{\text{RMS}} I_{\text{A}}^{\text{RMS}} + V_{\text{B}}^{\text{RMS}} I_{\text{B}}^{\text{RMS}} + \underbrace{V_{\text{W}}^{\text{RMS}} I_{\text{W}}^{\text{RMS}}}_{\approx 0} = \\ = \left(V_{\text{A}}^{\text{RMS}} - V_{\text{B}}^{\text{RMS}}\right) I_{\text{A}}^{\text{RMS}} = V_{\text{AB}}^{\text{RMS}} I_{\text{A}}^{\text{RMS}} \,, \tag{4.3}$$

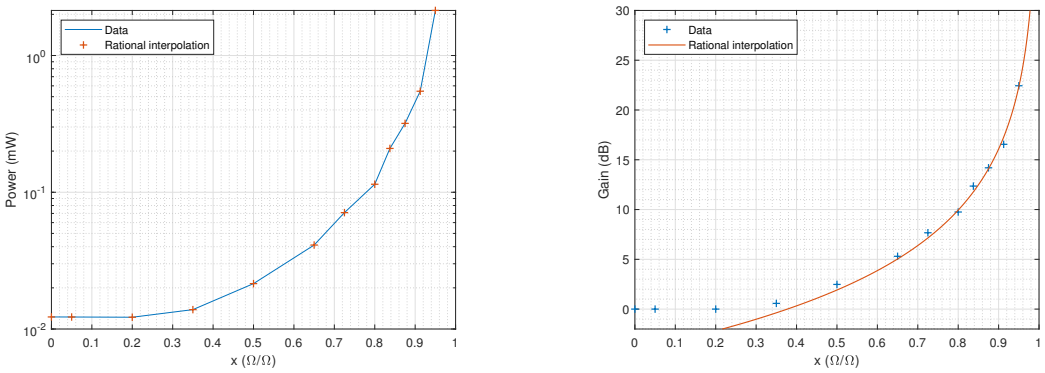
the power is calculated and reported for sake of completeness because the power dissipated is very small and completely safe for the devices involved. All the previous plots refer to linear conditions. Clearly the voltage at each terminal of the potentiometer remains inside the potentiometer's available dynamic since the two devices (op-amp and digital potentiometer) are fed with the same supply (dual $\pm 2.5\,\text{V}$). In this way the saturation of the op-amp occurs always before the dynamic limits of the potentiometer are reached, protecting it.

The other solution is more straightforward. The voltage at the B terminal is always null with respect to the reference since it is grounded. The voltage at the upper terminal A is the output voltage of the amplifier, which in this case has a fixed gain, whilst the wiper terminal voltage is the A one reduced accordingly to the voltage divider position. The situation is more simple because whatever the



(a) Voltages V_{AB}, V_{WB}, V_{WA}. **(b)** Currents I_{A}, I_{W}, I_{B}.

Figure 4.7: On the left, the peak values of the voltages across each terminal combination of the potentiometer (V_{AB}, V_{WB}, V_{WA}) for different values of the x parameter. On the right, against the same parameter x, the corresponding terminal currents are plotted.



(a) Dissipated power P_{pot}. **(b)** Gain curve A_{v}.

Figure 4.8: On the left, the dissipated power is plotted for different values of the x parameter. On the right, against the same parameter x, the gain data points are plotted with a possible interpolating rational function of the form $1/(1-x)$.

amplitude of the input signal and gain combination is the output signal is always limited by the op-amp rails. So it does not matter if the amplifier is working in linearity or not, the terminal A voltage (which is always the largest one) swings at maximum in an interval which results to be $[-2\,\mathrm{V}, 1.3\,\mathrm{V}]$[4].

[4]Considering the OPAx134 specifications for a $10\,\mathrm{k}\Omega$ load[13]. In this case the saturation seems to occur later because of the much grater load impedance, still maintaining its asymmetry.

It's interesting to demonstrate that the power dissipated by the potentiometer exploited as a volume control is constant with x, a feature that can result useful. Consider the definition just used, involving the sum of the dissipation at the ports of the component, and use it:

$$\begin{aligned} P_{\text{pot}} &= v_{\text{A}}^{\text{RMS}} i_{\text{A}}^{\text{RMS}} + v_{\text{B}}^{\text{RMS}} i_{\text{B}}^{\text{RMS}} + v_{\text{W}}^{\text{RMS}} i_{\text{W}}^{\text{RMS}} = \\ &= \frac{(v_{\text{out}} - v_{\text{W}})_{\text{RMS}}^2}{(1-x)R_{\text{pot}}} + \frac{v_{\text{W,RMS}}^2}{xR_{\text{pot}}} \ . \end{aligned} \tag{4.4}$$

In Eq.4.4 the power calculation is done as the sum of the dissipated power on the two resistors forming the divider. The upper one holds the drop from the output of the op-amp v_{out} to the wiper, while the second term is the one related to the portion of resistance from the wiper to ground. In the following calculation the following fact is used: the RMS value of a difference of sinusoid with same frequency and phase and different amplitude is equal to the difference of the peak values divided by $\sqrt{2}$. Re-writing Eq.4.4 as follow a nice result is reached:

$$\begin{aligned} P_{\text{pot}} &= \frac{1}{2R_{\text{pot}}} \left[\frac{(\hat{v}_{\text{out}} - \hat{v}_{\text{W}})^2}{(1-x)} + \frac{\hat{v}_{\text{W}}^2}{x} \right] = \\ &= \frac{1}{2R_{\text{pot}}} \left[\frac{\hat{v}_{\text{out}}^2 (1-x)^{\cancel{2}}}{\cancel{(1-x)}} + \frac{x^{\cancel{2}} \hat{v}_{\text{out}}^2}{\cancel{x}} \right] = \\ &= \frac{1}{2R_{\text{pot}}} \left[\hat{v}_{\text{out}}^2 - \cancel{x\hat{v}_{\text{out}}^2} + \cancel{x\hat{v}_{\text{out}}^2} \right] = \\ &= \frac{\hat{v}_{\text{out}}^2}{2R_{\text{pot}}} \ . \end{aligned} \tag{4.5}$$

In the above steps, according to the definition of x, the fact that $v_{\text{W}} = xv_{\text{A}} \equiv v_{\text{out}}$ is used. Moreover, the $\hat{}$ symbol indicates the peak value af the quantity below it. Notice that the expression of Eq.4.5 does not depend on the x parameter. The measured value is $P_{\text{pot}} \approx 8.45\,\mu\text{W}$.

An important part of the analysis of the amplifier is concerning the bandwidth. The experimental set up considered in this thesis includes the Analog Discover 2, which can also be used as a network analyser, which allows the user to directly visualise the *Bode plot*. As visible in Figure 4.9 the not compensated response presents a resonance peak approximately at 430 kHz. The other two traces in the figure above are plotted for values of C_{f} belonging to different decades. For the smallest capacitance value ($C_{\text{f}} = 47\,\text{pF}$), the magnitude plot presents a dominant pole around 35 kHz and, as is it evident looking after the plateau of the simultaneously introduced zero, the resonance is well attenuated. This behaviour is not maintained for higher values of C_{f}: an unexpected new resonance occurs, indicated

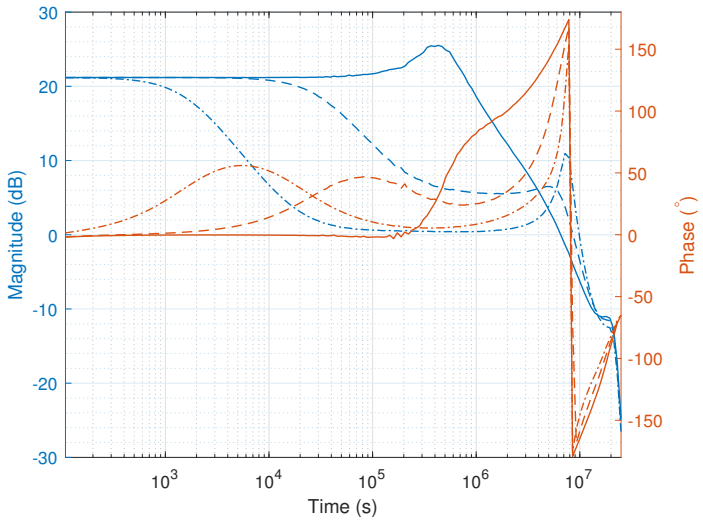


Figure 4.9: High frequencies portion of the response of the amplifier with different values of C_f: solid no C_f present, dotted $C_\mathrm{f} = 47\,\mathrm{pF}$, dot-solid $C_\mathrm{f} = 1\,\mathrm{nF}$.

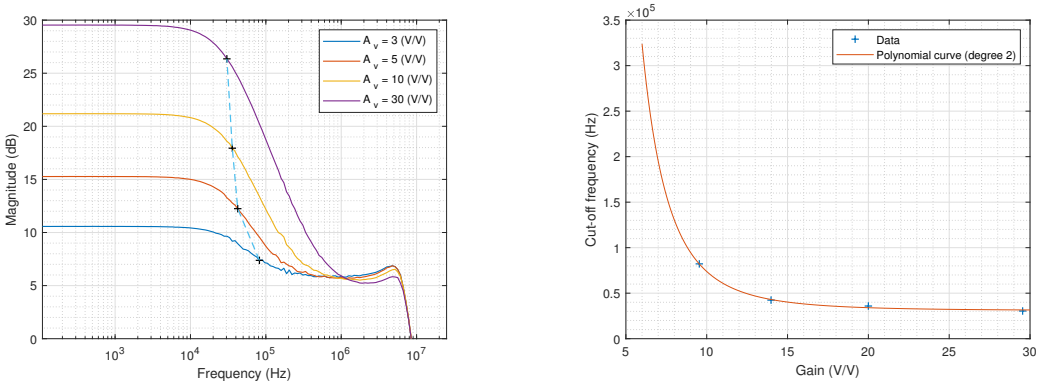
by the sharp peak around 8 MHz on the dot-solid magnitude trace. This happens because the action of the pole introduced by C_f is completely compensated by the combined zero. So even if the new cut-off frequency for $C_\mathrm{f} = 1\,\mathrm{nF}$ is around 1.82 kHz the new resonance at 8 MHz is important.

So, a C_f capacitor in the feedback of the op-amp is needed in order to limit the band of the amplifier, but its capacitance has to be small enough to make the new resonance rise. A value of a tens of picofarad is sufficient.

Further more the cut-off frequency of the amplifier is not fixed, since it depends on the coupling between the capacitor and the portion of potentiometer resistance in the feedback of the amplifier, so practically it depends on the gain. Figure 4.10 shows the drift of the cut-off frequency imposed by C_f with the gain. For low gain values (less than 6 dB for instance) the difference between the level inside the passing band and the level of the plateau after the zero is too small to consider the C_f pole a proper dominant cut-off point. This causes a quick increase of the cut-off frequency with the decrease of the gain, because the well above second pole is detected instead of the C_f one.

4.3 Muting circuits

This section of the results' report is dedicated to the muting circuit explained in the previous chapter. Substantially two important aspects are investigated: the attenuation and transparency performances in on and off mode respectively as well



(a) Dissipated power P_{pot}.

(b) Gain curve A_{v}.

Figure 4.10: On the left, the Bode diagram for four different values of gain is reported with the band cut-off point of the various response pointed out (with same $C_{\text{f}} = 47\,\text{pF}$). On the right, the same cut-off points are plotted against the gain instead of the frequency.

as the frequency response in transparent mode. The attenuation and transparency properties can be evaluated with the oscilloscope, observing the levels of the signals, whilst the frequency response can be evaluated with the network analyser tool of Waveforms (Digilent software, using the Analog Discovery 2).

4.3.1 JFET based

Series configuration

Starting with a more simple configuration in which just one stage is implemented (with respect to the schematic in Figure 3.18 and Figure 3.17) a good insights of the performances of the circuit is already visible. Then the same exact measurements can be taken adding first the complementary branch to obtain the transmission gate and Furthermore the second stage. This allows a direct comparison of the possible modification on the same topology, enlightening the possible advantages.

Following this procedure the measure of the attenuation inside the passing band can be compared for the solution with one stage, with or without transmission gate, and the two stages transmission gate one. The signals reported in Figure 4.11 are filtered through a moving window mean whose size is 6 samples. This is necessary because of the low level signals considered are also prone to the noise injection in the experimental environment, exhibiting a lower signal to noise ratio with respect to larger waves. Considering the peak level of the signals obtained, an evaluation of the attenuation (Ψ) for each case can be done.

- For a single stage solution, without transmission gate: $\Psi = -36.5\,\text{dB}$.

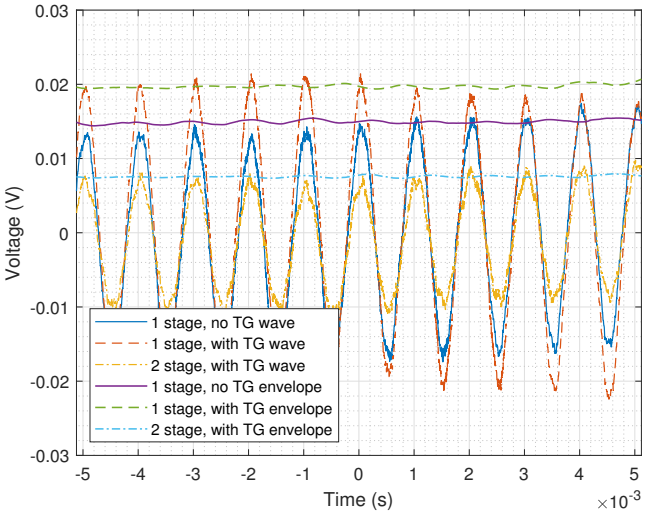


Figure 4.11: *JFET-series* muting circuit waveforms in off state for solutions with different number of stages (or transmission gate implementation) and with an input sinusoid of 1 V peak.

- For a single stage solution, with transmission gate: $\Psi = -34.1\,\text{dB}$.
- For a double stage solution, with transmission gate: $\Psi = -42.4\,\text{dB}$.

These results are reasonable because, with respect to the most simple case, a transmission gate adds an impedance (the off n-channel) in parallel to the already existent one. So the difference in decibel indicates that the transmission gate solution attenuate less than the simplest solution by a factor which is near to $\sqrt{2}$. Adding a second transmission gate solution means that the impedance added in this next case is put in series with the first stage one, making the attenuation stronger.

For what concerns the attenuation in band (Figure 4.12), when the muting circuit is disabled, the same procedure is implemented. The way in which the impedances added and subtracted changing the number of stage or the transmission gate implementation works on the attenuation is the same. In this case, the values of attenuation are so similar that in practice no difference is noticed using one solution or the other.

- For a single stage solution, without transmission gate: $\Psi = -0.149\,\text{dB}$.
- For a single stage solution, with transmission gate: $\Psi = -0.142\,\text{dB}$.
- For a double stage solution, with transmission gate: $\Psi = -0.169\,\text{dB}$.

In this series configurations, the limiting of the band at high frequencies is not crucial, considering implementations below a few megahertz, despite the presence

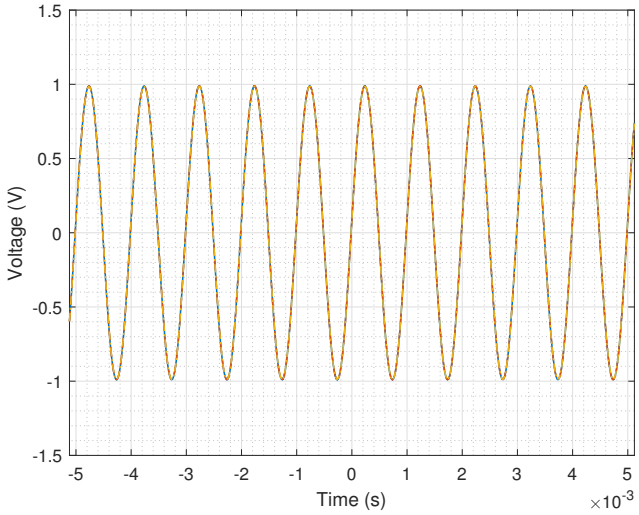


Figure 4.12: *JFET-series* muting circuit waveforms eith the system disabled for different solutions and with an input sinusoid of 1 V peak. Notice that it is impossible to appreciate differences in the order of tens of millivolt on this scale.

of the glitch filter capacitor C_{gl} at the output of the system. So it is more useful trying to measure the band in the low frequency region, where the decoupling capacitors act as well as the possible load effect at the output. For the following measurements a load of 22 kΩ is used.

As visible in Figure 4.13 the variation is almost null, because in this situation the dominant pole at low frequencies is associated to the external load resistance. The poles associated to the two first decoupling capacitors and relative biasing resistors are placed around a decade below (approximately at 5 Hz).

Parallel configuration

A seen in the previous chapter, the parallel configuration of the muting circuit based of JFET switches is a lot simpler in terms of operation and size of the circuit. Despite this reduction, its performances are in general comparable or superior with respect to the series configuration.

In Figure 4.14 the output waveforms for a single or double stage solution are reported considering an input sine wave of amplitude 1 V. According to the measure of their amplitudes the attenuation can be evaluated:

- For a single stage solution: $\Psi = -44.9\,\text{dB}$.
- For a double stage solution: $\Psi = -70.0\,\text{dB}$.

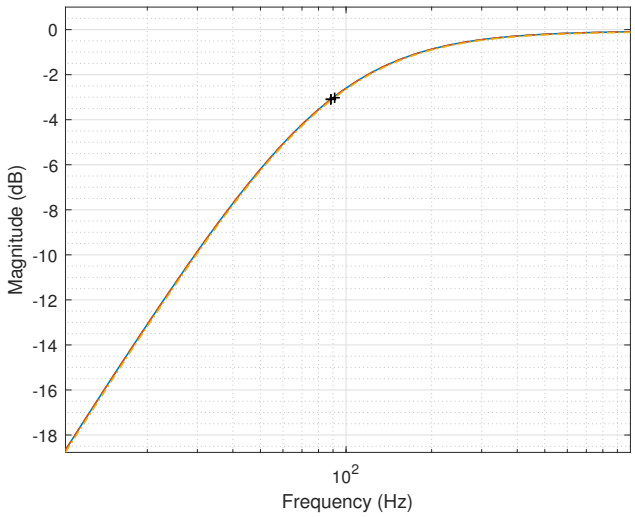


Figure 4.13: *JFET-series* muting circuit Magnitude Bode diagram around the lower cut-off frequency. The cut-off point (at $-3\,\mathrm{dB}$) is marked with a black "+" for all the three traces, which look absolutely equivalent.

With one single stage the attenuation is already very good, a bit higher in absolute value than the two stages series configuration (the most complicated one). With the two stages parallel solution the attenuation increases impressively, so that the signal is detected hardly when hidden in the noise floor of the system. In fact, still observing Figure 4.14, it can be noticed that the envelope (from which the amplitude is derived) detected is practically the amplitude of the noise. So it is clear that the performances in muting condition are absolutely preferable especially facing the hardware simplification involved. This is because the voltage divider formed by the resistor R_{damp} and the impedance seen "looking into" the drain of an on JFET is quite unbalanced. Supposing, for sake of simplicity, a resistance R_{ON} for the JFET of $100\,\Omega$, with a resistor $R_{\mathrm{damp}} = 10\,\mathrm{k}\Omega$ the attenuation is theoretically of $-40\,\mathrm{dB}$. Hence, considering the measurements above for the single stage option, the resistance of the on JFET can be estimated as

$$\Psi = 20\log_{10}\left(\frac{R_{\mathrm{ON}}}{R_{\mathrm{damp}} + R_{\mathrm{ON}}}\right)$$

$$R_{\mathrm{ON}} = R_{\mathrm{damp}}\frac{10^{\Psi/20}}{1 - 10^{\Psi/20}} = 10\,\mathrm{k}\Omega\frac{10^{-44.9/20}}{1 - 10^{-44.9/20}} \approx 57\,\Omega \tag{4.6}$$

which is a plausible value.

Consider now the transparent condition. In this situation the channel resistance seen from the drain of the JFET is extremely high so that the voltage divider

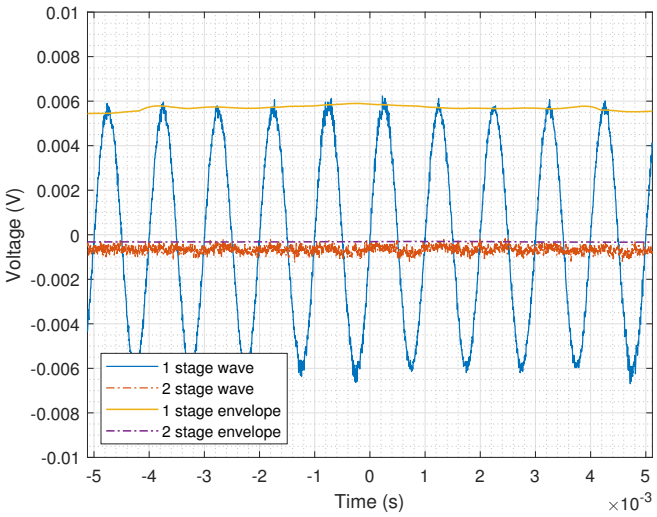
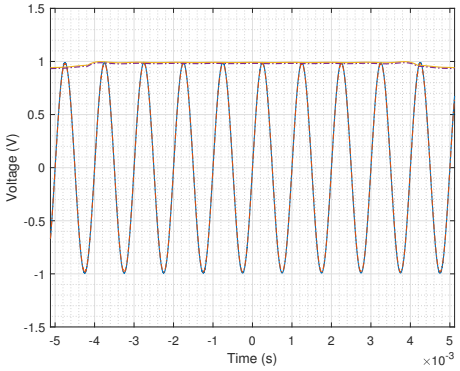
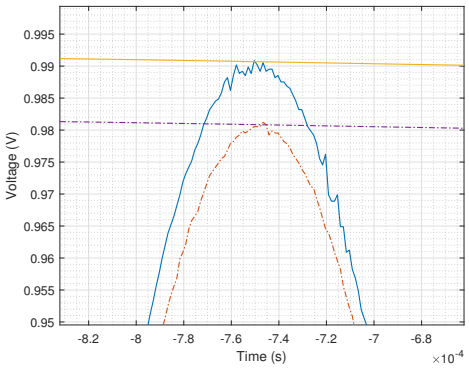


Figure 4.14: *JFET-parallel* muting circuit waveforms in mute condition with an input signal of amplitude 1 V.



(a) Output waveforms in transparent condition.



(b) Zoom of the plot on the left, around one of the central peak.

Figure 4.15: Output voltages in transparent condition (at 1 kHz, inside the passing band), with the envelopes detected for one and two stages solutions. On the right, a zoom of one portion of the plot is visible, in order to make more clear the difference between the two different solutions. The amplitude of the input signal is of 1 V.

condition is reversed. The divider factor of the stage in transparent condition is close to one, but anyway it attenuates the signal in a visible way. Considering the

input impedance of the oscilloscope high enough[5], the little attenuation visible is to be addressed only by the muting system.

Summarizing,

- For a single stage solution: $\Psi = -0.11\,\text{dB}$.
- For a double stage solution: $\Psi = -0.19\,\text{dB}$.

The values above confirm a greater attenuation in transparent condition for the two stage solutions. The difference between the two levels is 0.08 dB, so a difference between the two amplitudes is around 1%. These values are slightly larger than in the case of the *JFET-series* solution for the same testing condition, but the values are so close that the advantage of having a better transparency performance (at expense of an hardware complication) is completely negligible.

On the contrary with respect to the series configuration, the parallel one does not require a DC bias to fulfil its functioning, so no decoupling capacitors are needed at the input or at the output. This means that the bandwidth of the system is practically flat up to the DC, making the analysis of the response useless in the low frequency region.

Looking at the upper portion of the spectrum, the response is clearly dominated by the low pass action introduced by the coupling between the glitch filter capacitor C_{gl} added on the output of the system and the resistor R_{damp} constituting the voltage divider series element. Knowing this, it is evident that whatever the cut-off frequency of the single stage configuration is, the one of the double stage has to be at a frequency which is half the first one. This is because the resistance in series with the signal in the two stages circuit is approximately twice the one in the single stage. In Figure 4.16 the situation for the two possible solutions of parallel configuration is reported. The black "+" marks the −3 dB point with respect the passing band, which are localised respectively at 98.6 kHz and 193.6 kHz. A quick calculation proves the previous considerations about the cut-off frequency:

$$\frac{f_{\text{c}}^{2\text{ stage}}}{f_{\text{c}}^{1\text{ stage}}} \approx 1.9634 \tag{4.7}$$

which means that the cut-off frequency of the double stage solution is less than 2% far from the factor of 2.

In the upper frequency region this fact represents the only disadvantage of the parallel configuration in comparison with the series one. Clearly a trade-off between disturb suppression and frequency response can be found depending on the specification of the system to be designed.

[5]The input impedance of the oscilloscope is in the order of magnitude of the megaohm, so compared to the value of R_{damp} it is practically ineffective.

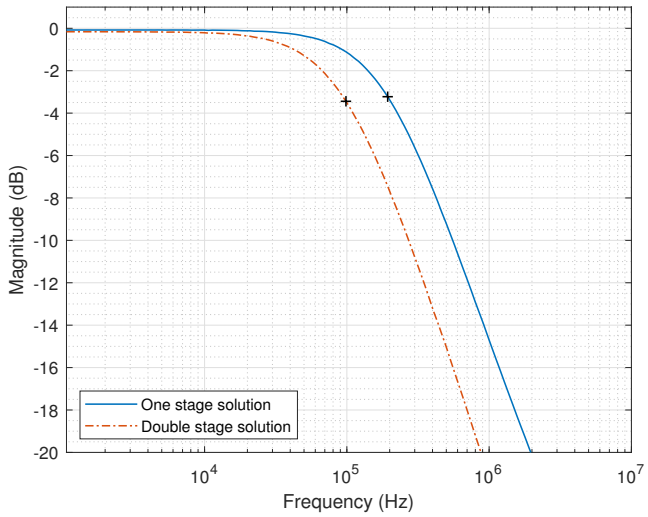


Figure 4.16: *JFET-parallel* muting circuit response in transparent condition. The plot represents the upper portion of the magnitude Bode diagram around the cut-off.

4.3.2 Optocoupler based

The optocoupler based muting circuits exploit a different component to fulfil their purpose but fundamentally they can be evaluated on the same basis of the JFET ones. So in the following sections the two complementary configuration of optocoupler muting circuits are analysed with the same process just implemented, with some more considerations on the turn on characteristic of the optoisolator itself.

Series configuration

The basic considerations have to be repeated on how the circuits works in muting conditions. The plot in Figure 4.17 is the analogous of Figure 4.11. As expected the two stages solution attenuates more the signal because it puts more impedance in series on the signal path. But comparing the peak levels of these waves to the one of the JFET series solution it is visible that the performances of the optocoupler system are worst.

- For a single stage optocoupler system $\Psi = -27.9\,\text{dB}$.
- For a double stage optocoupler circuit $\Psi = -31.5\,\text{dB}$.

Looking at the calculated values above, it results that the two stages optocoupler solution (which is the more effective of the two) attenuates the signal 2.6 dB less than the less effective JFET one (single transmission gate configuration).

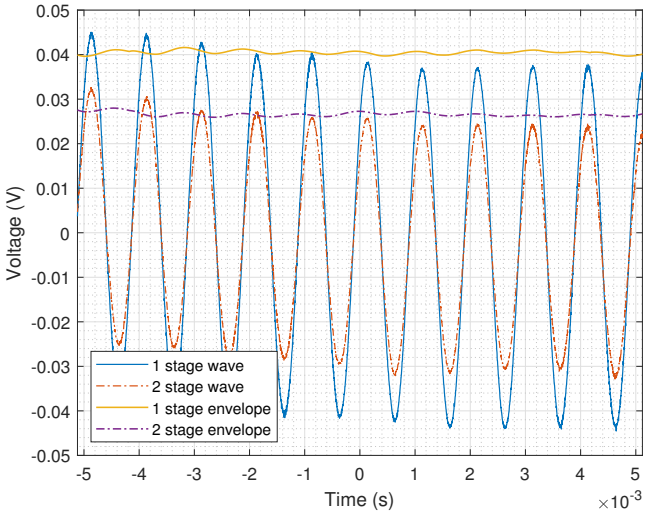


Figure 4.17: *Optocoupler-series* muting circuit waveforms in off state for solutions with different number of stages and with an input sinusoid of 1 V peak.

The discussion about the transparent condition is more interesting than the one concerning the mute state because of the analysis on the state of the driver. Recalling the circuit in Figure 3.27, a consideration can be done tracing the mesh across the input of the driver (one of the two, the other in parallel is not crucial).

$$V_{\mathrm{IN}}^{\mathrm{mute}} - R_{\mathrm{lim}} I_{\mathrm{B}} - V_{\mathrm{BE}}^{\mathrm{ON}} = 0 \tag{4.8}$$

Eq.4.8 is written in static condition, but a variation of $V_{\mathrm{IN}}^{\mathrm{mute}}$ can still be considered by supposing that it varies slowly in time. Hence, practically in the experimental set-up, a voltage control formed by a potentiometer and a resistor (as visible below, Figure 3.27) has been prepared and connected to the command node, and some measurements of the $V_{\mathrm{IN}}^{\mathrm{mute}}$ have been taken.

The direct solution of the circuit in Figure 4.18 involves a non linear equation, hence it is not feasible by hand. Qualitatively, starting with the potentiometer at the ground extreme, the voltage across the base-emitter junction is null and Q_{dr} is off. Turning up the potentiometer, the situation remains the same (Q_{dr} off) until the transistor starts to conduct the current. The voltage $V_{\mathrm{IN}}^{\mathrm{mute}}$ does not increase linearly, as before, because the more the voltage at the base of Q_{dr} grows, the more the base conduct current (exponentially) and this has an effect on the $V_{\mathrm{IN}}^{\mathrm{mute}}$ itself.

This fact has an impact on the muting circuit, because the ability of the driver to sink (or source) current is directly linked to the behaviour of the phototransistor inside the optocoupler. In order to be turned on in a sufficiently strong way, a good amount of current has to flow in the collector. In the following plot (Figure 4.19)

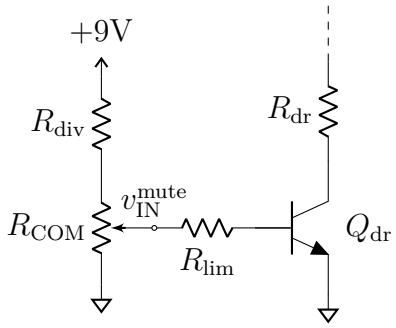
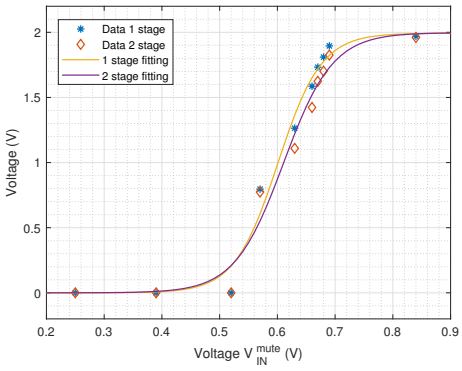
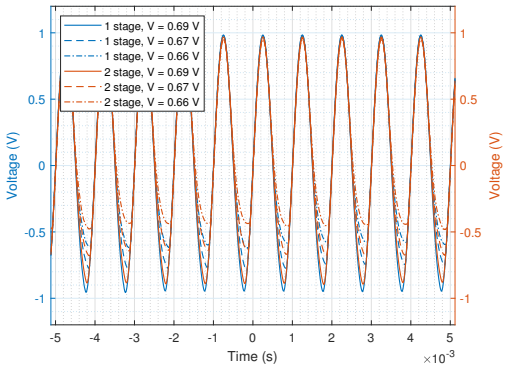


Figure 4.18: Driver circuit for an *optocoupler-series* muting circuit.

the peak to peak voltage of the output signal in transparent condition has been measured for different positions of the potentiometer R_{COM} and plotted against the corresponding values of $V_{\text{IN}}^{\text{mute}}$. Below a certain threshold, when the BJT is off, the signal at the output is (almost) null. Around the 0.6 V the transistor turns on and the signal start to pass through the optocoupler since the LED inside it is starting to emit photons. When the saturation condition is reached, after a complete turn on, the amplitude of the output signal is constant because the resistance exhibited by the phototransistor is not decreasing any more.



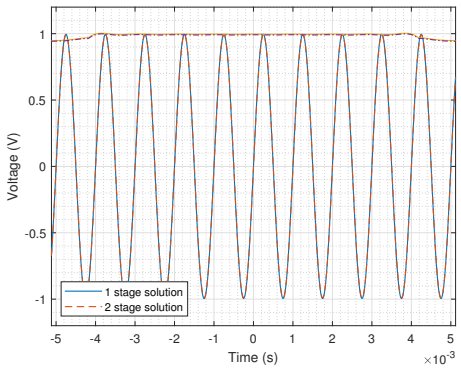
(a) Peak to peak voltage of the output signal against the vommand voltage $V_{\text{IN}}^{\text{mute}}$



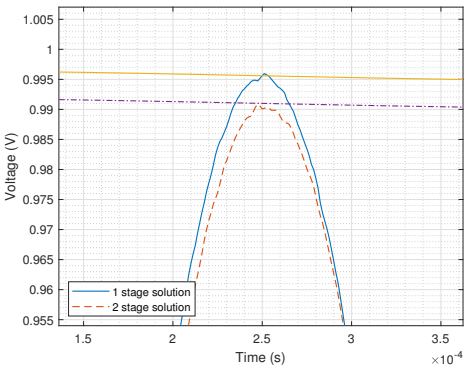
(b) Output voltage for the single and double stage solution for three different levels of command.

Figure 4.19: Transparent behaviour of the *optocoupler-series* circuit around the edge of the turn on region of the driver, with an input signal of 1 V peak.

Ensuring a correct transparent condition the measure of the attenuation in band can be carried on. Exploiting the peak value measured using the envelope detection,



(a) Output waveforms in transparent condition.



(b) Zoom of the plot on the left, around one of the central peak.

Figure 4.20: Output voltages in transparent condition (at 1 kHz, inside the passing band), with the envelopes detected for one and two stages solutions. On the right, a zoom of one portion of the plot is visible, in order to make more clear the difference between the two different solutions. The amplitude of the input signal is of 1 V. Notice that for a two stage solution, for the same value of $V_{\mathrm{IN}}^{\mathrm{mute}}$, the performances are worst because the series element are doubled.

te following attenuation in transparent condition have been calculated:

- For the single stage circuit: $\Psi = -0.030\,\mathrm{dB}$.
- For the double stage circuit: $\Psi = -0.071\,\mathrm{dB}$.

These values of attenuation are absolutely important, since they are a order of magnitude smaller (in absolute value) than the one for the JFET solutions. The huge disadvantage of the series configuration based on optocoupler is that to keep the transparent condition a big amount of power has to be delivered both by the driver and the switch, in comparison to what happens in the JFET circuit. In the JFET circuit the switching element control port does not draw any current, so the power is dissipated only in the driver section. Considering the JFET series two stage transmission gate configuration, the main dissipated power contributions are given by the resistor R_{C} and by the transistor $Q_{\mathrm{dr},1}$ (the other one is off because the complementary commands)[6]. In the optocoupler counterpart the main contributions come from the driver transistor, by the limiting resistor in series with the collector and by the optocoupler LED himself. Moreover, the final dissipated power for the optocoupler circuit is twice the value obtained considering the components above, because the two stages have to be driven contemporarily

[6]For the designator of the components consider the schematic in Figure 3.18.

on. Doing these steps, it results that the optocoupler circuit series solution sink an order of magnitude more than the JFET based one: 45.68 mW against 5.67 mW. Hence a slightly improvement in the transparency is paid with a significant increase of energy demand.

For what concerns the frequency response analysis, similarly to the JFET parallel circuit, no decoupling capacitances are present since no bias for the optocoupler is needed. Again, this means that the interesting limitations in the band happens in high frequencies region. The two different cut-off point have been marked with the

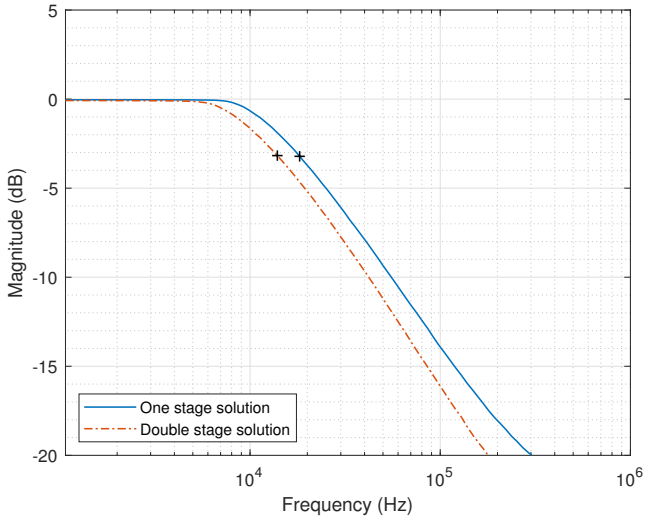


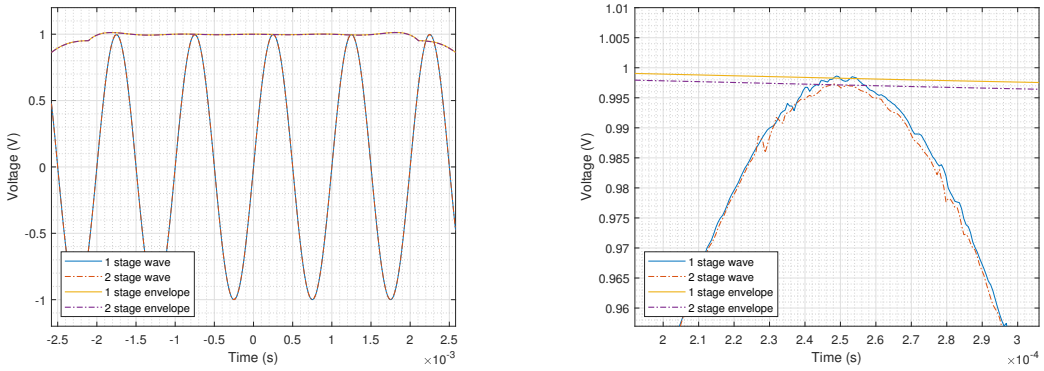
Figure 4.21: *Optocoupler-series* muting circuit magnitude Bode diagram around the high frequencies cut-off point.

black crosses in Figure 4.21. For the two stages solution, more resistance is localised in series with the signal, making the cut-off point drop with respect to the single stage circuit, similarly to what has been presented before. Anyway, the highest cut-off frequency is not twice the other because of the non-idealities involved in the real circuit: 18.3 kHz and 13.9 kHz respectively. The frequencies involved are much lower than the one of the other solution. The trade-off involving the glitch filter capacitor placed at the output of the circuit (100 pF in this case) could still be a direction to explore to increase the band. In any case it is unlikely that the high frequencies performance of the *series-JFET* can be reached exploiting this component.

Parallel configuration

The parallel configuration does not show for the optocoupler solution the same hardware advantage against the series one, as it occurred for the parallel configuration implemented with JFET with respect to the series JFET one. This holds even if the results obtained with the current implementation present an unexpected difficulty.

Start considering the transparent condition, since in this situation the results are in every aspect comparable with the previous one (Figure 4.22). In off condition



(a) Output waveforms in transparent condition.

(b) Zoom of the plot on the left, around one of the central peak.

Figure 4.22: Output voltages in transparent condition (at 1 kHz, inside the pass band), with the envelopes detected, for the one and two stages solutions. On the right, a zoom of one portion of the plot is visible, in order to clarify the difference between the two different solutions. The amplitude of the input signal is 1 V.

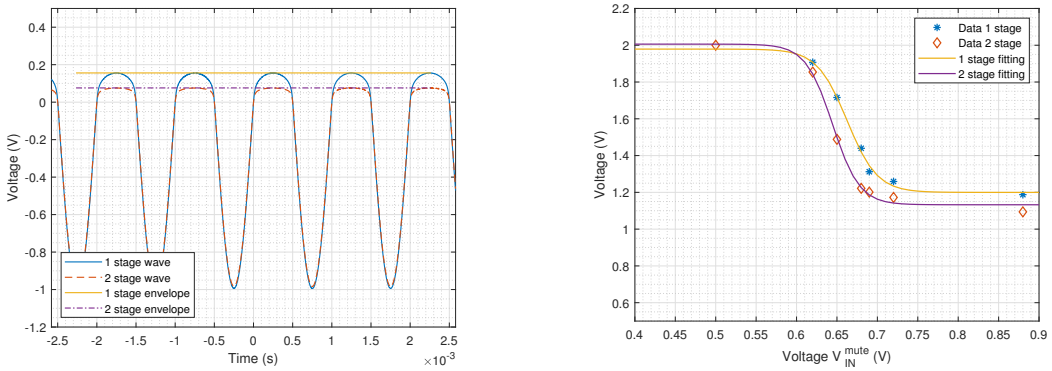
the photo-BJT contained in the optocoupler is well approximated with an open circuit so that the following attenuation can be calculated:

- For a single stage solution: $-0.017\,\mathrm{dB}$.
- For a double stage solution: $-0.026\,\mathrm{dB}$.

So, compared to all the three solutions seen till now, the *optocoupler-parallel* system exhibits a smaller difference in transparent condition between solutions with one or two stages. This difference is an order of magnitude smaller (in decibel) than the mean of the other previous cases. Anyway, this datum on its own does not mean that the circuit works particularly well with respect to the others, the absolute values of the attenuation are just absolutely good.

In muting condition a particular situation occurs. In the plot of Figure 4.23 the output waveforms for one or two stages solutions have been reported showing that

with the same command exploited for the series configuration only the positive half of the wave has been cut. On the right of Figure 4.23 the peak to peak amplitude of the output signal has been plotted for the two possible solutions in correspondence of different measured values of the $V_{\text{IN}}^{\text{mute}}$ voltage. As it is evident, from the transparent condition on the left of the graph, when the driver is still turned off, the peak to peak amplitude is 2 V, as for the input signal. When the transition region is passed (around the 0.65 V) the curve would tend to 0 V. This is not because the lower half wave is practically untouched. In fact the peak to peak voltage at the output is a bit higher than the input amplitude value (1 V). This situation can be recovered in two different ways: either increasing the input



(a) Output waveforms in transparent condition.

(b) Zoom of the plot on the left, around one of the central peak.

Figure 4.23: Output voltages in transparent condition (at 1 kHz, inside the passing band), with the envelopes detected for one and two stages solutions. On the right, a zoom of one portion of the plot is visible, in order to make more clear the difference between the two different solutions. The amplitude of the input signal is of 1 V. Notice that for a two stage solution, for the same value of $V_{\text{IN}}^{\text{mute}}$, the performance are worst because the series element are doubled.

command voltage (namely forcing the driver to push the optocoupler further into conduction) or by making a simple modification in the circuit of Figure 3.28. The second solution is preferable, since it does not stress the driver more and it consists in mirroring one of the two optocoupler respect to the horizontal line, so that the shunt branch to ground is not entering the collector of the phototransistor and exiting from the emitter but exactly the opposite. In this way one half of the wave is shunted by the first optocoupler, while the second stage cut the other half wave.

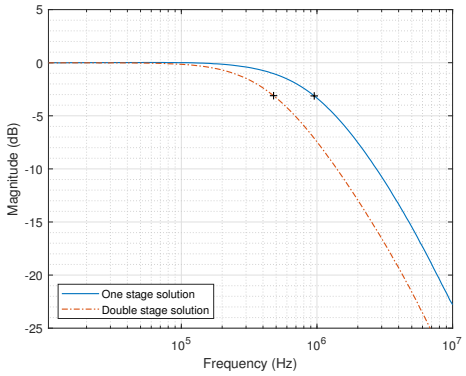
This solution implies that the two stages *optocoupler-parallel* circuit is instead a one stage, because the muting action is brought separately for different portion of the wave by the two stages. To really have a two stage effect on the output signal four optocouplers have to be used.

Supposing to have a symmetric action by the two opposite stages (this is not absolutely true but it is a good approximation at this point), the attenuations can be evaluated starting from the peak values of the output positive half wave in Figure 4.23 left.

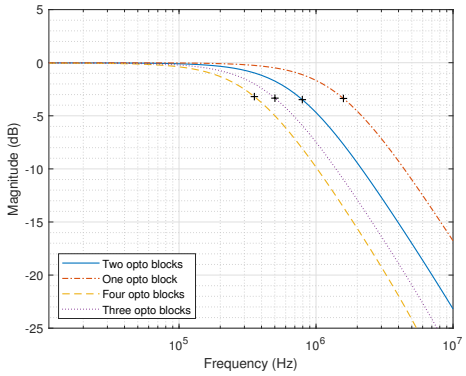
- For a full wave single stage (or two optocoupler blocks) solution: $\Psi = -16.1\,\mathrm{dB}$.
- For a full wave double stage (or four optocoupler blocks) solution: $\Psi = -22.4\,\mathrm{dB}$.

These values are the lowest (in absolute value) obtained till now, facing a clear hardware complication. Hence the performance of this circuit in muting conditions are not evaluated as good.

For what concerns the frequency response, as for the previous cases, what is important is the high frequencies cut-off determined by the coupling between the glitch filter capacitor and the damping resistors $R_{\mathrm{damp,n}}$. In Figure 4.24 (left) the



(a) *Optocoupler-series* muting circuit magnitude Bode diagram around the high frequencies cut-off point.



(b) *Optocoupler-parallel* frequency response Spice simultion for one, two, three or four optocoupler blocks.

Figure 4.24: *Optocoupler-parallel* frequency response report.

same behaviour seen for the *JFET-parallel* configuration is noticeable. The one stage solution has a frequency cut-off which is practically twice the double stage one, since the series resistance is doubled accordingly. The cut-off for a one block circuit is at $f_{\mathrm{c}}^{1,\mathrm{st}} = 955\,\mathrm{kHz}$, while for a two blocks circuit is $f_{\mathrm{c}}^{2,\mathrm{st}} = 479\,\mathrm{kHz}$. Notice also that the considerations made before on the fact that more stages have to be put in series with opposite connection with respect the other to obtain an even effect on the waveform's portion is not violated by the measurements here commented from the Bode diagram. This is because in off condition the characteristics of the optocoupler do not really matter and only the number of R_{damp} resistors (number

of stages) is crucial. From a Spice simulation, in fact, it results that the division of the frequency cut-off for an increasing number of stages is maintained (Figure 4.24 right).

4.3.3 Comparison

In this section, a direct comparison of the four different main topology results is presented in order to give a more precise overview of the situation. Firstly a series of tables with the results for the same characteristic are shown, clearly reporting these for the different four circuit studied (Table 4.1 and Table 4.3). Then a "score" for each circuit is given based on the performances obtained considering each single characteristic. The respective summations of these scores brought to a list which contains the circuits, from the most overall convenient to the less one. It is extremely important that these considerations are not meant to be absolute, because they depend on the scores given that are not an absolute system of evaluation. Moreover, in every specific application a certain requirement can exclude some of the circuits involved, beyond the theoretical considerations. These scores are given in Table 4.2 and Table 4.4.

	Single (dB)	Double (dB)
JFET-series	-34.1	-42.4
JFET-parallel	-44.9	-70.0
Opto-series	-27.9	-31.5
Opto-parallel	-16.1	-22.4

(a) Mute condition performances

	Single (dB)	Double (dB)
JFET-series	-0.142	-0.169
JFET-parallel	-0.11	-0.19
Opto-series	-0.030	-0.071
Opto-parallel	-0.017	-0.026

(b) Trasparent condition performances

Table 4.1: Attenuation derived measurements for all the different possibilities. For the *JFET-series* configurations, only the two complete with transmission gate are here considered (this holds for the following tables too).

In Table 4.1 the attenuation performances in decibel are collected, so that an order and a score can be given to the eight total combinations obtained considering the one and the two stages configurations for four circuit.

	Value (dB)	Score
Opto-p (1 stg)	-16.1	8
Opto-p (2 stg)	-22.4	7
Opto-s (1 stg)	-27.9	6
Opto-s (2 stg)	-31.5	5
JFET-s (1 stg)	-34.1	4
JFET-s (2 stg)	-42.4	3
JFET-p (1 stg)	-44.9	2
JFET-p (2 stg)	-70.0	1

(a) Mute condition scores

	Value (dB)	Score
JFET-p (2 stg)	-0.19	8
JFET-s (2 stg)	-0.169	7
JFET-s (1 stg)	-0.142	6
JFET-p (1 stg)	-0.11	5
Opto-s (2 stg)	-0.071	4
Opto-s (1 stg)	-0.03	3
Opto-p (2 stg)	-0.026	2
Opto-p (1 stg)	-0.017	1

(b) Trasparent condition scores

Table 4.2: Attenuation scores. The "p" suffix stands for "parallel" and the "s" stands for "series".

The following tables refer to the frequency performances of the muting circuits. With respect to the attenuation report, this one is more susceptible to heavy changes, in the sense that the choice of some components directly affect the high or low cut-off point; while for the attenuation, only a load impedance change produces visible changes. The problem of noise rejection is only partially solved

	Single (kHz)	Double (kHz)
JFET-series	> 1000	> 1000
JFET-parallel	98.6	193.6
Opto-series	18.3	13.9
Opto-parallel	955	479

(a) High frequency cut-off point.

	Single (Hz)	Double (Hz)
JFET-series	5	5
JFET-parallel	0	0
Opto-series	0	0
Opto-parallel	0	0

(b) Low frequency cut-off point.

Table 4.3: Bandwidth performances.

by inserting a filter capacitor. To avoid the restriction of the band caused by this element (especially in the parallel configurations that use some R_{damp} resistor) the

implementation of a buffer can be used. A voltage buffer between the output of the muting circuit and the filter capacitor can be used, eventually decoupling the output impedance of the circuit from the capacitance. If a more precise limiting of the band is needed, the implementation of a second order filter can be considered.

In the following table the scores for the bandwidth performances are given.

	Value (kHz)	Score
Opto-s (2 stg)	13.9	8
Opto-s (1 stg)	18.3	7
JFET-p (1 stg)	98.6	6
JFET-p (2 stg)	193.6	5
Opto-p (2 stg)	479	4
Opto-p (1 stg)	955	3
JFET-s (1 stg)	$> 1\,\text{MHz}$	2
JFET-s (2 stg)	$> 1\,\text{MHz}$	2

(a) High frequency cut-off scores.

	Value (Hz)	Score
JFET-s (2 stg)	5	2
JFET-s (1 stg)	5	2
JFET-p (2 stg)	0	1
JFET-p (1 stg)	0	1
Opto-s (2 stg)	0	1
Opto-s (1 stg)	0	1
Opto-p (2 stg)	0	1
Opto-p (1 stg)	0	1

(b) Low frequency cut-off scores.

Table 4.4: Bandwidth performances scores.

To give a final evaluation of the convenience of the circuits above, a final score to each of them has to be given considering the hardware complexity and power dissipation estimation. For what concerns the dissipated power also a qualitative evaluation can be done at this level, considering that accordingly to the polarity of the switch and so to the state that the driver has to occupy the consumption can very a lot. For instance, a JFET-parallel circuit is implemented with p-channel JFET so to keep the transparent condition the voltage at the gates has to be high, in order to be high the BJT driver has to sink no current, so it is switched off and the power consumption can be consider null (for that stage). Considering an application in which the transparent condition is the most common with respect to the muting one, this is a circuit that consumes much less than the series counterpart.

It is important to notice that the evaluation of the hardware complexity is not done with some kind of measurements. An intermediate score (the HW column in Table 4.5, left) is given considering the number of driver, with a penalty if two, and the number of switching devices. Hence, for example, the *series-JFET* circuit shows two drivers and four transistors, so it receives a score of $2 \cdot 2 + 4 = 8$. For what concerns the power, the transparent condition is considered as the normal one, so the circuits with the driver switched off in this state are at the lowest dissipation possible (0). Than the other values are weighted with the number of contemporary on drivers involved. The values obtained are then put into a rank as done for the other characteristics.

	HW	Score
JFET-s (2 stg)	8	4
JFET-s (1 stg)	6	3
JFET-p (2 stg)	4	2
Opto-s (2 stg)	4	2
Opto-p (2 stg)	4	2
Opto-p (1 stg)	3	1
JFET-p (1 stg)	3	1
Opto-s (1 stg)	3	1

(a) Hardware complexity scores.

	Power	Score
Opto-s (2 stg)	4	4
JFET-s (2 stg)	2	3
Opto-s (1 stg)	2	3
JFET-p (1 stg)	1	2
JFET-s (1 stg)	0	1
JFET-p (2 stg)	0	1
Opto-p (2 stg)	0	1
Opto-p (1 stg)	0	1

(b) Power consumption scores.

Table 4.5: Hardware complexity and power consumption scores.

At this point, for each circuits, the final evaluation can be done by summing the different scores obtained. Clearly, with the method followed, the best circuit is the one that gains the lowest score.

	Results
Opto-p (1 stg)	16
Opto-p (2 stg)	18
JFET-p (1 stg)	18
JFET-s (1 stg)	18
JFET-p (2 stg)	19
JFET-s (2 stg)	20
Opto-s (1 stg)	24
Opto-s (2 stg)	25

Table 4.6: Final score table.

It is clear that the rank in Table 4.6 has to be combined with the single design requirements. Furthermore, the single characteristic score can be evaluated with different weights with respect the others in the final summation in order to make one of the particular aspect be more relevant.

As understandable from Table 4.6 the most convenient topology is a single stage parallel optocoupler based circuit. It combines a good level of attenuation despite its hardware simplicity with an optimal isolation in transparent conditions. Moreover, it does not consumes an excessive amount of power even if it is based on an optocoupler device.

Chapter 5

Conclusion

The integration of digital potentiometer into analog circuits has been overviewed considering some key circuits such as different types of amplifier. The most relevant design problems related to the integration have been presented with a particular focus on voltage supply and noise issues. Some possible solutions have been commented and some of them have been also tested by means of a dedicated board, realised specifically for the purpose, to be used in conjunction to a pre-existent circuit (designed by LAA Custom). The results obtained show that the process of integration is not a straight forward procedure, despite its initial apparent simplicity.

A systematic approach to the topic is hard to be found in the literature. Hence, the present work represents a basis for the author for a more in depth and complete investigation of the subject. On the other hand it is directly connected to the practical implementation of digitally controlled analog circuits, such as amplifiers or dedicated muting circuits.

The hope of the author is that this work could represent just the beginning of more complex experiments in this field, which represents, indeed, an important aspect of the evolution of the electronics.

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