Master Thesis

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Superconducting Devices in Silicon

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Abstract

Superconducting qubits have shown great prospects for quantum computing applications but the scalability of the circuits made of these devices faces major challenges. The classical superconducting transmon qubits, which make up the largest quantum processors today, are controlled through a magnetic flux and so are limited by the cross talking between qubits and the large amount of current required to tune all these magnetic fluxes. The gatemon geometry seems to overpass these issues. Gatemons are based on a new kind of device called JoFET that is a field effect transistor (FET) with a superconducting source and drain. The idea is to use the S/N/S junction of the FET as a Josephson junction in which we can tune the super-current amplitude thanks to a gate voltage. Besides solving the two previously raised issues, the large-scale implementation of such a technology requires its compatibility with large-scale fabrication processes. To do so, we want to engineer a CMOS compatible JoFET.

This report focuses on the superconducting PtSi - Si interfaces physics and fabrication for the purpose of making a silicon based CMOS compatible JoFET. PtSi is well known in the CMOS industry and has a relatively high superconducting critical temperature (Tc around 1K), thus it is a good candidate for that purpose. The main challenge for JoFET design is the maximization of the super-current that can flow through it because it is deeply linked to the performances of the resultant gatemon qubit. The amplitude of this super-current will be conditioned by the transparency of the S/N (PtSi/Si) interface and this report mainly focuses on this issue. We measured the very low temperature electrical behavior of PtSi/Si junctions made with the CMOS quasi-industrial facilities of the CEA-Leti in order to bring some elements to guide the engineering of the PtSi/Si JoFet fabrication process.

Résumé

Les qubits supraconducteurs se sont montrés très prometteurs pour l'implémentation des futurs ordinateurs quantiques, mais la fabrication de puce contenant un très grand nombre de ces qubits fait face à d'importants défis. Les qubits supraconducteurs qui sont aujourd'hui majoritairement utilisés pour le calcul quantique, les transmons, sont pilotés via un flux magnétique et sont donc limités par le « cross-talk » et l'importance du courant nécessaire à leur contrôle. La géométrie gatemon semble outrepasser ces problèmes. Les gatemons sont basés sur un nouveau type de dispositif appelé JoFET qui n'est rien d'autre qu'un transistor à effet de champ (FET) dont la source et le drain sont supraconducteurs. L'idée est d'utiliser la jonction S/N/S du FET comme une jonction Josephson dans laquelle on est capable de piloter l'amplitude du super-courant grâce à une tension de grille. En plus de résoudre les deux challenges exposés précédemment, ces dispositifs doivent être compatibles avec la fabrication à grande échelle. Pour ce faire, nous devons développer des JoFET compatibles avec les technologies CMOS.

Ce rapport se concentre sur la physique et la fabrication des interfaces entre PtSi supraconducteur et silicium dans l'objectif de fabriquer un JoFET compatible avec les technologies CMOS. Le PtSi est bien connu dans l'industrie CMOS et a une température supraconductrice critique (Tc) relativement haute (environ 1K), ainsi il semble être un bon candidat. Le principal défi à relever dans le développement d'un JoFET est la maximisation du super-courant qui peut le traverser car cette grandeur sera fortement liée aux performances du qubit gatemon qui en découlera. L'amplitude de ce super-courant est conditionnée par la transparence de l'interface S/N (PtSi/Si), ce rapport discute largement ce point. Nous avons mesuré le comportement électrique à très basse température de jonctions PtSi/Si fabriquées sur les lignes quasi-industrielles du CEA-Leti dans le but d'apporter de nouveaux éléments au développement du procédé de fabrication des JoFET en PtSi/Si.

Sommario

L'implementazione di superconduttori qubit nei computer quantistici ha mostrato un enorme potenziale e viene considerata il futuro per tali applicazioni, sebbene la fabbricazione di chip contenenti un numero sufficentemente elevato di qubit rappresenti ancora una grande sfida tecnologica. I superconduttori qubit che oggi sono maggiormente utilizzati per il calcolo quantistico, i transmons, sono gestiti attraverso un flusso magnetico e sono quindi limitati dal cosiddetto "cross-talk" e dalla quantità di corrente elettrica necessaria al loro impiego. La geometria di Gatemon sembra superare questi vincoli. I gatemon si basano su un nuovo tipo di dispositivo chiamato JoFET, ovvero un transistor a effetto campo (FET) dotato di source e drain superconduttori. L'idea è di utilizzare la giunzione S/N/S del FET come giunzione Josephson in cui l'ampiezza della supercorrente può essere controllata da una tensione di gate. Oltre a risolvere tali sfide tecnologiche, questi dispositivi devono essere compatibili con la fabbricazione su larga scala. Per riuscire in ciò, è necessario sviluppare JoFET che siano compatibili con le tecnologie CMOS.

Il presente lavoro si concentra sulla fisica e la fabbricazione di interfacce superconduttore PtSi - Silicio, sviluppate con l'obiettivo di fabbricare un JoFET compatibile con CMOS. Il PtSi è ben noto nell'industria CMOS e sembra essere un buon candidato in quanto presenta una temperatura critica di superconduttività (Tc) relativamente alta (circa 1K). La sfida principale nello sviluppo di un JoFET è massimizzare la supercorrente che può fluire attraverso di esso, in quanto tale ampiezza sarà fortemente legata alle prestazioni del qubit gatemon risultante. L'ampiezza della supercorrente è condizionata dalla trasparenza dell'interfaccia S/N (PtSi/Si) e in questo lavoro il tema è stato ampiamente studiato attraverso la misura del comportamento elettrico a temperature molto basse delle giunzioni PtSi/Si, fabbricate sulle linee quasi-industriali del CEA-Leti al fine di fornire nuovi elementi per lo sviluppo del processo di fabbricazione del PtSi/Si JoFET.

Contents

Introduction

For more than a century, we know that quantum mechanics is a fundamental pillar of nature laws. However, computer algorithms that are one of the most important tools we use to calculate, model and simulate the nature are not governed by quantum mechanics rules, we usually label them "classical computing". In the 80s, some physicists, led by Richard Feynman, came up with the idea of a quantum computer [1]. They proposed to use quantum superposition and quantum entanglement to engineer a new way of processing information. This new computation method is based on quantum bits, these quanta of information play a role similar to that of the classical bits. A qubit is a two level quantum system so that we can define two fundamental states usually written $|0\rangle$ and $|1\rangle$, these two states compose the basis of the two-dimensional Hilbert space that describes the system. In other words, the qubit state can be $|0\rangle$, $|1\rangle$ or any quantum superposition of theme. The potential power of a quantum computer comes from the size of its computational space, it grows as 2^n where n is the number of qubits while in a classical computer it grows linearly with the amount of transistors. Today, the most advanced quantum circuits are made of a few tens of those qubits. Thus, scalability is required to increase the power of the first quantum circuits that are tested all over the world and to finally reach the performance that we are waiting for. Indeed, quantum computers open up wonderful prospects in many domains such as drug synthesis, meteorological simulation, material science or simply to model some complex quantum systems that challenge the most powerful classical supercomputers.

Theoretically, a quantum computer can even emulate the behavior of a classical computer and so overtake the later in every domain but this statement does not take into account the inherent analog nature of quantum computers. The weakness of quantum computing comes from the propagation of the errors. Indeed, these systems are noisy and errors quickly becomes their worst enemy as soon as the calculation implies many steps (ie. many logic gates). To face this issue, correction algorithms have been developed and the key to override this question appears to be the multiplication of physical qubits. The correction codes imply logical qubits made of many noisy physical qubits. Thus, the need for scalability prevails even more and stands beside the need for high performance qubits.

In that context, many technologies are explored to handle these challenges. Among them, we can name the most famous ones: ion traps, quantum dots and superconducting qubits. The work presented here will focus on the later. Superconducting qubits have shown great prospects for scalability and proofs of concept such

as Sycamore [2] or Zuchongzhi [3] paves the way to large superconducting quantum circuits. The CEA, and especially the Grenoble division, is part of the world top laboratories working on these topics. The close collaboration with the CEA-Leti permits to build bridges between the fundamental researches and the future industrial implementations of these technologies. This internship is in the framework of a project involving booth the CEA-Pheliqs laboratory and the CEA-Leti in order to link fundamental research and industrial challenges. The aim of the project is to couple one the most advanced quantum computing technologies with the industrial most known processes: complementary metal oxide semiconductor (CMOS). In other words, we want to build superconducting qubits using CMOS facilities in order to greatly improve the scalability of this kind of systems. This report and my internship are part of this long term project just as the PhD I will start in the fall 2021.

This report focuses on what I learned and did during this 6 months internship at the CEA-Pheliqs laboratory in the LaTEQS research group. The first section focuses on the theoretical background that I acquired and that is needed to understand the main issues of this research topic. All the path from superconductivity to superconducting qubit is discussed. The second section deals with the state of the art of this domain and more specifically the advantages of the gatemon geometry and the recent breakthroughs about it. The third section describes the experimental techniques used in this work. The principle of a dilution refrigerator and the TLM measurements are discussed. The fourth section looks after all the measurements of the PtSi/Si junctions (made at the CEA-Leti) done during the internship. Then the road-map of the project is presented before a short focus on the internship organization.

1 Theoretical background

1.1 Superconductivity

Superconductivity can appear in some material below a critical temperature Tc and a critical magnetic field Hc. A zero resistance and a perfect diamagnetism that means the expulsion of any magnetic field characterize this phenomenon. H. Kammerlingh Onnes and G. Holst discovered superconductivity in 1911 when they cooled down a mercury sample and succeed in measuring its superconducting transition at $T_c = 4.2K$ (Fig 1). Mercury was the first of a long list of superconducting materials that will be found later on. Meissner and Ochsenfeld brought the second amazing characteristic of superconductor to light in 1933 when they showed the expulsion of an applied magnetic field. This phenomenon, now called the Meissner effect, is actually a consequence of the zero resistivity.

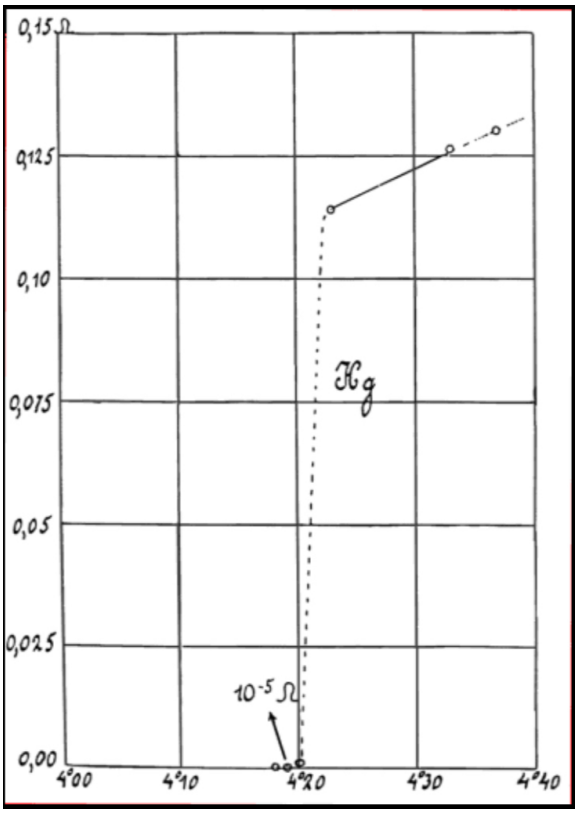


Figure 1: H. K. Onnes' plot of the resistivity of Hg at low temperature showing its superconducting transition (1911). From [4].

1.1.1 London equations

In 1935, Fritz and Heinz London proposed a first phenomenological model [5]. The London equations came from a very classical physics. The first London equation is:

$$\frac{\partial j}{\partial t} = \frac{ne^2}{m}E \tag{1.1}$$

Its derivation is based on Newton's second law applied to a density of superconducting electrons n that are moving without any friction. It describes the effect of an electric field E over such a super-current density j. From this first equation, we can find the second one using the Maxwell-Ampère equation:

$$\Delta \times j = -\frac{ne^2}{m}B \tag{1.2}$$

where B is an applied magnetic field. This simple model permit to explain remarkably well the Meissner effect [6] by giving us the London penetration depth:

$$\lambda_L = \sqrt{\frac{m}{\mu_0 ne^2}} \tag{1.3}$$

An applied external magnetic field vanishes exponentially inside a superconductor with a characteristic length λ_L.

1.1.2 Pippard

In 1953, Pippard introduced a non-local relation between the current density and the magnetic field [7] to overpass the London description weaknesses which cannot explain some experiments. The idea is to introduce a coherence length ξ that is the characteristic length of the super-current density variation when a magnetic field is applied. The key point is to focus on the electrons around the Fermi level $\pm k_B T_c$. These electrons will be the only one relevant around the Tc and the energy interval that we consider can be translated to a length through the Heisenberg uncertainty principle to finally get a coherence length:

$$\xi \propto \frac{\hbar \nu_F}{k_B T_c} \tag{1.4}$$

where ν_F is the Fermi wave length.

1.1.3 Ginzburg-Landau

In 1950, the Ginzburg-Landau theory uses the second order phase transition theory from Landau and a wave description of the superconducting electron density as order parameter. We consider a normal phase and a superconducting phase that are separated by an energy corresponding to the critical magnetic field:

$$g_0^N - g_0^S = \frac{\mu_0 H_c^2}{2} \tag{1.5}$$

Ginzburg and Landau give us the following equation to describe the free energy of the transition:

$$f = \alpha|\psi|^2 + \frac{\beta}{2}|\psi|^4 + \frac{1}{2m}|(-i\hbar\nabla - 2eA)\psi|^2 + \frac{h^2}{8\pi} \tag{1.6}$$

where α and β depends on the temperature and are experimentally determined, e is the electron charge, m the electron mass, B the magnetic field and A the vector potential. ψ is the order parameter; its square amplitude gives the superconducting electronic density. By minimizing this phase transition free energy expression with respect to A and the order parameter, we can express the super-current density and get the superconducting critical temperature. Taking a uniform order parameter we find back the London description. Also, the Ginzburg-Landau theory reintroduce the previously defined coherence length and the penetration depth λ, we commonly use the Ginzburg-Landau parameter $\kappa = \frac{\lambda}{\xi}$.

1.1.4 Abrikosov

In 1957, Abrikosov proposed two categories of superconductors using the Ginzburg-Landau parameter to discriminate them [8]. The first superconductors discovered were all type I, meaning that their coherence lengths were greater than their penetration depths. Abrikosov supposed the existence of type II superconductors for which the GL parameter is greater than one. Such materials should show a second order transition with two critical fields. Between these two critical fields, the applied field is not completely expelled anymore and penetrates the materials forming Abrikosov vortexes; each one holds a flux quantum $\phi_0 = h/2e$. These magnetic vortexes have been observed for the first time in 1967. Another important characteristic is the electron mean free path, indeed for very clean materials the coherence length and the penetration depth will be the same as discussed previously but when the electronic mean free path becomes shorter, i.e. in the dirty limit, we get

$$\xi^2 = \xi_0 l \tag{1.7}$$

$$\lambda^2 \approx \lambda_0^2 \frac{\xi_0}{l} \tag{1.8}$$

with l the electronic mean free path. Furthermore, a consequence of this is the fact that a type I superconductor can become a type II (superconducting Si:B for instance).

1.1.5 BCS

It is in 1957, that Bardeen, Cooper, and Schrieffer (BCS) established a strongest microscopic theory [9], this theory will become the classical description of superconductivity. This work, that lead to a Nobel Prize in 1972, assumes that in a superconductor, electrons are paired because of interactions with the crystal and being paired they behave as bosons. Thus, these pairs of opposite wave vectors and spins are condensed in a fundamental state separated from the classical fermionic states by an energy gap Δ. This energy gap can be understood as the pair breaking energy. All these pairs form a fundamental state described by a wave function having as coherence length the previously discussed ξ.

One of the main results of the BCS theory is the relation between the superconducting gap at 0K $\Delta(0)$ and the critical temperature of the superconductor Tc:

$$\Delta(0) = 1.76 k_B T_c \tag{1.9}$$

Even more interesting, BCS gives us the value of the superconducting gap Δ with respect to the temperature. When T is close to T_c we get:

$$\frac{\Delta(T)}{\Delta(0)} \approx 1.74 \sqrt{1 - \frac{T}{T_c}} \tag{1.10}$$

1.2 Andreev reflection

We will now focus on the interfaces between a normal conductor and a superconductor, this kind of hybrid structure plays a central role in superconducting quantum circuits. For superconductors, the BCS theory tells us that there is a gap in the electronic density of states around the Fermi level and gives us the size of this gap. Thus, when an electron inside this energy gap comes from the normal conductor side and impinges the interface, it cannot be simply transmitted since there is no available state in the superconducting side of the junction to host him. Thus two different scenarios can occur inside the gap:

- The electron is simply reflected (i.e. specular reflection).

- The electron is reflected as an hole with the opposite momentum and a Cooper pair is created on the superconducting side. This process is called Andreev reflection.

The probabilities of each of these phenomena are derived in an article published in 1982 by Blonder, Tynkham and Klapwijk (BTK) [10]. The BTK probabilities depend on the size of the superconducting gap and the height of the barrier at the interface. For the barrier, we usually use a parameter Z linked to the transparency T as follows:

$$T = \frac{1}{1+Z^2} \tag{1.11}$$

From this probabilities we are able to express the current that we should measure at the interface with respect to the bias V we impose (for voltages lower than Δ/e):

$$I_{NS} = G_{NN}\frac{1+Z^2}{e}\int_{-\infty}^{+\infty}[1+A(\epsilon,Z,\Delta)-B(\epsilon,Z,\Delta)][f_F(\epsilon-eV)-f_F(\epsilon)]d\epsilon \tag{1.12}$$

where f_F is the Fermi-Dirac distribution function, G_{NN} is the conductance of the same junction if we replace the superconductor by a normal metal, A and B are the probabilities for Andreev reflection and specular reflection respectively. The first thing we understand is that when the probability of Andreev reflection is low then the current crossing the interface will also be low. But, if the Andreev reflection are maximized, then the conductivity is doubled compared to the normal one. This Andreev current is at the origin of the Josephson effect that we will talk about later.

The BTK model permits to plot the conductance versus bias for a given barrier height and temperature as it is done figure 2 for different barrier height Z at T=50mK and where Γ is the Dynes parameter.

The Dynes parameter as been proposed for the first time in 1978 by R. C. Dynes [11], it is an additional imaginary part to the energy that changes the density of states used in the BTK current calculation.

$$\rho(E,\Gamma) = \rho(E - i\Gamma) \tag{1.13}$$

where Γ is the Dynes parameter. It permits to express the presence of some available states inside the gap due to some defects for instance.

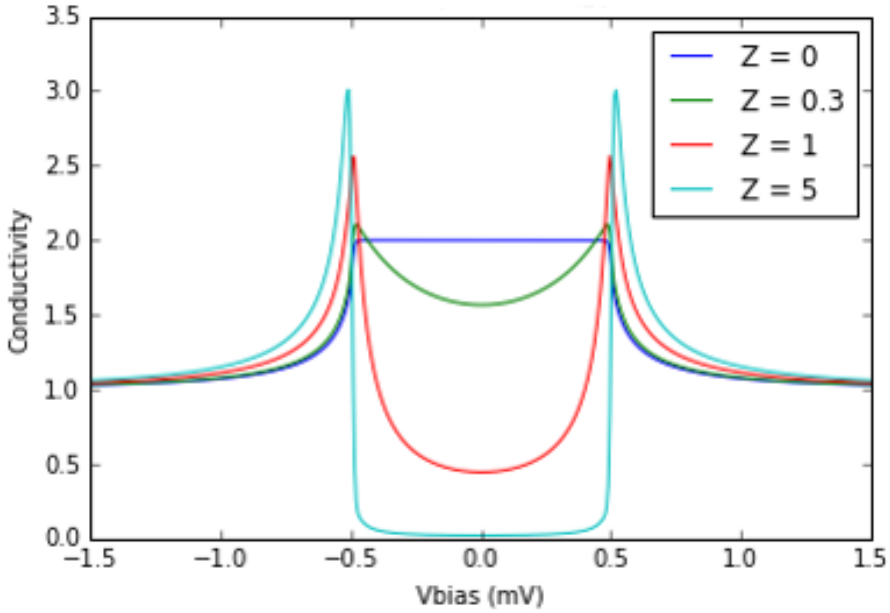


Figure 2: Conductivity of a superconductor/semiconductor junction with respect to its bias plotted for different interface barrier heights ($\Delta = 500\mu eV$, $\Gamma = 0.03\Delta$ and $T = 50mK$). The conductance peaks at the edges of the gap are called "coherence peaks".

1.3 Josephson effect

In 1962, using the BCS theory, B. D. Josephson described the flow of a super-current through a new kind of device called Josephson junction (JJ) [12]. Under this name we should distinguish two device families.

The first one is made of two superconducting electrodes separated by a thin isolating barrier (SIS junction). If the barrier is thin enough the Cooper pairs flowing in the superconducting electrodes can tunnel across the junction.

Later, the Josephson effect is observed in devices made of two superconducting electrodes separated by a "weak link", it can be a normal metallic or semiconducting barrier (SNS junction). In this case, super-current can cross much larger links. By proximity effect, superconducting like behavior is induced in the "weak link". It is the consequence of the previously discussed Andreev reflections. A succession of coherent Andreev reflections inside the "weak link" may induce the presence of

so-called Andreev bound states (ABS). These ABS can carry a finite suppercurrent across the SNS junction and make it a JJ. The main property of this process is its phase coherence, which is linked to the diffusion properties of the "weak link" and the quality of the SN interfaces [13].

The work of B. D. Josephson raises two effects, the DC Josephson effect and the AC Josephson effect. The DC Josephson equation gives a relation between the phase difference between the two superconductors ϕ and the Copper pair super-current I_S flowing through the junction:

$$I_S = I_C sin(\phi) \tag{1.14}$$

where I_C is the critical current. Furthermore, the second Josephson relation describes the time dependence of the phase ϕ with respect to the bias V of the JJ:

$$\frac{\partial \phi}{\partial t} = \frac{2eV}{\hbar} \tag{1.15}$$

We can simply deduce from these two formulas that when we apply a bias V to the Josephson junction, the super-current will oscillate as follows:

$$I(t) = I_C sin(\frac{2e}{\hbar} Vt + \phi_0) \tag{1.16}$$

making the device a perfect voltage to frequency converter and a great way to measure the conductance quantum $2e/\hbar$, this is the AC Josephson effect. The frequency of these oscillations is called the Josephson frequency. From this, we can derive:

$$V = \frac{\hbar}{2eI_C cos(\phi)} \frac{\partial I}{\partial t} = L(\phi) \frac{\partial I}{\partial t} \tag{1.17}$$

and we define the Josephson inductance L_J:

$$L(\phi) = \frac{L_J}{cos(\phi)} \tag{1.18}$$

The energy of such a junction can be derived by considering the bias voltage and the super-current expressions. Doing so we get:

$$E_J(\phi) = \int_0^t V I_S dt = -E_0 cos(\phi) \tag{1.19}$$

where $E_0 = \hbar I_C / 2e$ is the Josephson energy.

1.4 Superconducting quantum interference devices (SQUID)

The Josephson Effect paves the way to many applications; one of the greatest examples is the superconducting quantum interference devices (SQUID). Such a device is composed of two Josephson junctions placed in a superconducting loop (Fig 3). In

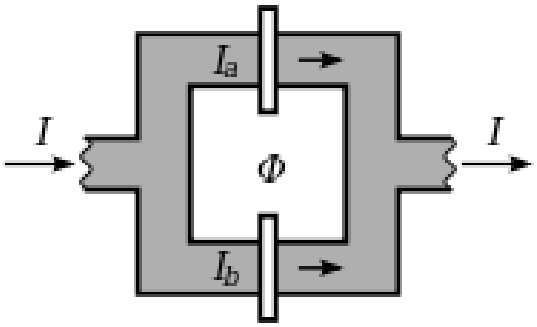


Figure 3: Schematic of a SQUID made of two Josephson junctions placed in a superconducting loop

such a loop the Aharonov-Bohm effect tells us that the phase shift $\Delta\Phi_B$ between an electron rotating clockwise and an other one rotating anticlockwise induced by an external magnetic field ϕ is written:

$$\Delta\Phi_B = \frac{2\pi\phi}{\phi_0} \tag{1.20}$$

where ϕ_0 is the flux quantum. Furthermore, the total phase shift inside the loop has to be a multiple of 2π:

$$\Delta\Phi_B + 2\Delta\Phi_J = 2\pi n \tag{1.21}$$

with $\Delta\Phi_J$ the phase shift for one JJ (considering the two JJ identical). Thus, if the critical current of the two JJ is identical then we can write the current crossing the SQUID as follows:

$$I = I_C sin(n\pi - \frac{\pi\phi}{\phi_0}) \tag{1.22}$$

This behavior permits to measure magnetic field much smaller than ϕ_0 thanks to a SQUID.

1.5 Superconducting qubit

Classical computation is based on an elementary quantum of information called bit. A bit can takes values: zero or one. Starting from this basic element, we can encode all the information we want and process it. However, one limitation of this principle is the classical representation of the elementary information that have to be 1 or 0 even if we know for decades that nature does not really work like that.

We came to the idea of encoding this quantum of information into a two level system that follows the quantum mechanics rules. To do so we can think about spins of electrons or photons but here we will focus on quantum oscillators. A quantum harmonic oscillator can be in several eigenstates defined by specific energies (not a continuum of levels as in a classical harmonic oscillator) (Fig 4a).

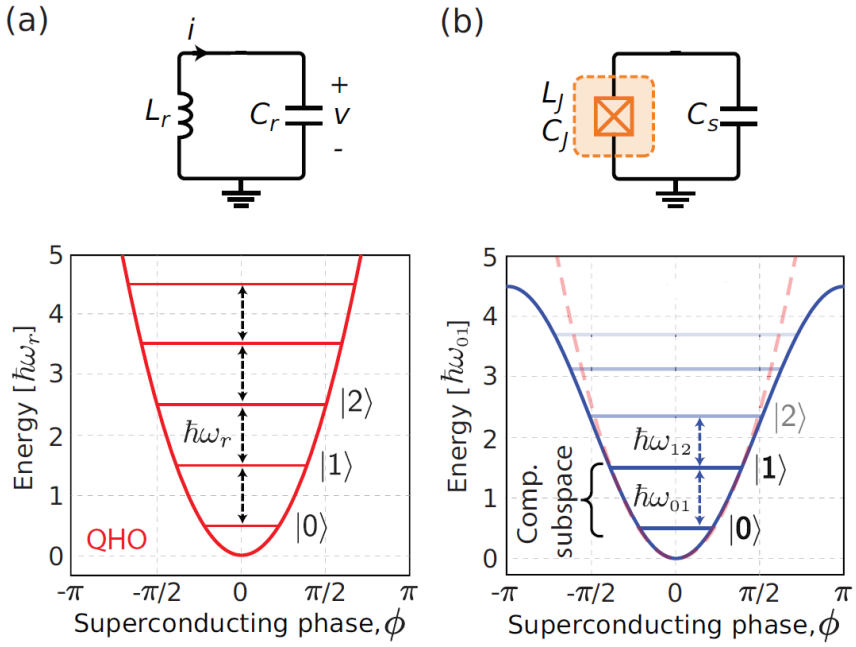


Figure 4: (a) Circuit for a quantum harmonic oscillator made of a capacitor in parallel with an inductance, the eigenstates of the system are equidistantly spaced. (b) Circuit for quantum anharmonic oscillator, the Josephson junction replaces the inductance and introduces the non linearity. The eigenstates are not anymore equidistantly spaced and we can define a computational space over the two lowest energy levels. From [14].

To make a qubit we will build such an oscillator and choose two of the possible eigenstates that will become our 0 and 1 states. The question is now how to build this device. A classical way to build a harmonic oscillator is the so-called LC circuit made up of a capacitor and an inductance. By cooling down this circuit, we show off its quantum behavior, it means that the energy states are now discretized. The issue is that the energy gap between two eigenstates is always the same and this makes impossible to know in which state the system is. Therefore, we need to introduce anharmonicity. To do so, a Josephson junction or a couple of JJ replace the classical inductance introducing non linearity and so anharmonicity in the oscillator. Indeed, a JJ behaves as a nonlinear inductance (Fig 4b). Then, we are able to define a computational space over the two lowest energy levels for instance.

1.6 From Cooper pair box to transmon qubit

The first superconducting qubit realized was a Cooper pair box (CPB). This device is composed of a superconducting island that is capacitively coupled on one side to a gate voltage and connected to a superconducting reservoir through a JJ on the other side. The energy of the system takes into account the Josephson energy E_J and the charging energy E_c of the island. The Hamiltonian of the system is as follows:

$$H = 4E_c(n - n_G)^2 - E_J cos(\phi) \tag{1.23}$$

Where ϕ is the phase difference across the JJ, n is the number of Cooper pairs in the island and $n_G = C_G V_G/2e$ is the reduced gate charge. On the figure 5 we plot the firsts energy levels of this system with respect to the gate charge, we observe that a small E_J ($\leq E_C$) opens a gap near the degeneracy points between the fundamental and the first excited states. By increasing the E_J/E_C ratio, the energy levels are flattened and finally when $E_J/E_C = 50$ we quit the CPB regime to enter into the transmon regime. The charging energy induced by Coulomb blockade phenomena does not any more predominate. In the transmon regime the two first energy levels are separated by $E_{01} = \sqrt{8E_J E_C}$. The main advantage of the transmon over the CPB is its lower sensitivity to charge noise. Indeed, the increase of the ratio E_J/E_C induces an exponential decrease of the sensitivity toward charge noise. However, we should keep in mind another phenomenon: the charge energy is the origin of the anharmonicity of the system but only linearly so a good controllability of the qubit stills reachable.

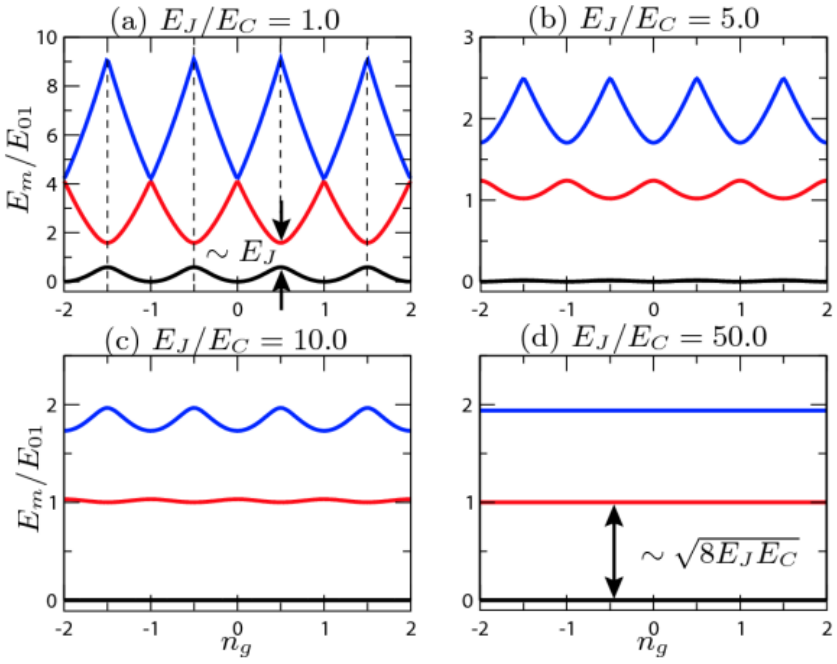


Figure 5: Energy spectrum of the three first levels of the CPB Hamiltonian as function of the reduced gate charge for different values of the ration between the Josephson energy and the charging energy. From [15].

1.7 Gatemon

In a superconducting qubit, it is essential to be able to tune the energy levels of the system, especially E_{01} that characterize the transition between the two first states. To do so we can tune the Josephson energy E_J, in classical transmon devices it is done through the phase modulation of the JJ (as shown in equation 1.19). A magnetic flux is applied thanks to a superconducting current line. This technique has a drawback: the integration of a large number of current lines is a barrier for complex quantum processors integration.

To solve this issue, another geometry have been proposed: the "gatemon". Here, the idea is to tune the Josephson energy by tuning the current flowing through the JJ (and so E_J in 1.19). To achieve this, the weak link between the two superconductors is made of a semiconductor and thanks to a gate voltage, we modulate its carrier concentration (Fig 6). The new JJ based device is actually a field effect transistor with a superconducting source and drain and is called a "JoFET" (Joseph-

son field effect transistor). Such implementations have been done multiple time in particular using Al source and drain and a channel made of InAs but never by using silicon [16][17].

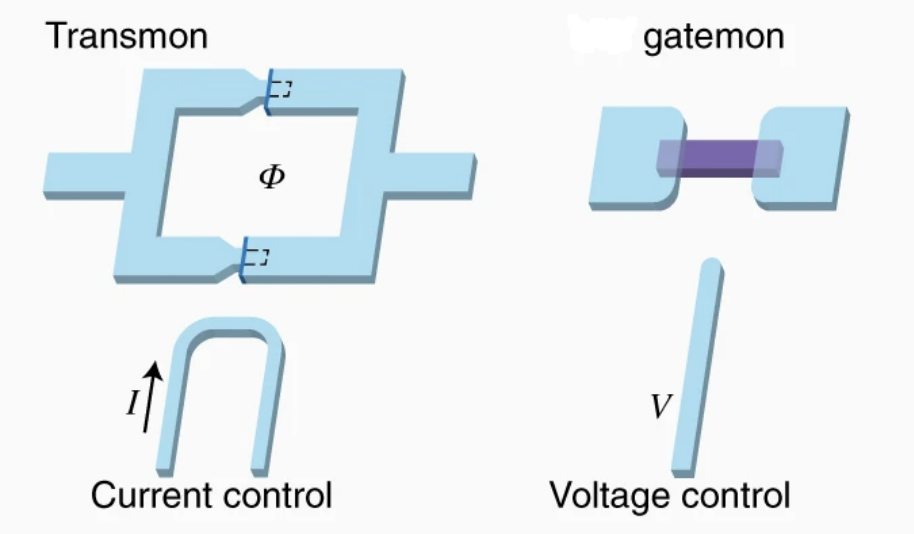


Figure 6: Left side: classical transmon where E_J is tuned through a magnetic flux. Right side: gatemon composed of superconducting source and drain and a semiconducting channel, E_J is tuned by a capacitive modulation of the channel conductivity and so of the Josephson current. From [18].

2 State of the art devices

We saw in the previous section one way to store quantum information: superconducting qubits. Among these superconducting qubits we choose to focus on the gatemon geometry for various reasons we will firstly expose. Then we will focus on the state of the art gatemon made of Al/InAs junctions. Finally, we will discuss recent work on PtSi/Si gatemon done in the LaTEQS team.

2.1 Benefits of the gatemon geometry

The first main advantage of this implementation is its metal oxide semiconductor field effect transistor (MOSFET) like architecture. Indeed, a gatemon can be seen as a simple MOSFET with superconducting source and drain. This greatly facilitates its integration in large scale designs. The complete switch of the gatemon takes also advantage of its MOSFET like behavior, as a matter of fact, the channel conductance can be modulated over several orders of magnitude. This point addresses one of the main drawbacks of transmons just as the switching time that is also greatly improved in gatemons. Last but not least, gatemons are driven through a gate voltage whereas transmon are driven through a magnetic flux and so require a current control. Thus, gatemons gets simpler to integrate and consume less power, which is a crucial challenge for the future large scale quantum circuits.

2.2 State of the art InAs gatemon

For almost a decade, people are trying to build gatemons because of these great prospects but the main challenge is to engineer the interface between the superconductors and the semiconducting channel. As discussed in the previous section, the Josephson effect comes from the Cooper pairs transfer across the channel thanks to Andreev reflections. To successfully occur, these Andreev reflections need a very transparent interface to ensure coherent travel across the junction. The quality of the semiconductor-superconductor (Sm-S) interface will be the whole point. Recent fabrication breakthroughs permitted to produce very high quality Al/InAs interface (thanks to in situ aluminum epitaxy over InAs [16]) and most of the current working gatemons are made with this technology (Fig 7).

2.3 Silicon based gatemon

This internship is part of an even more challenging project since its aim is to reach sufficiently transparent interfaces to build a qubit but using complementary metal

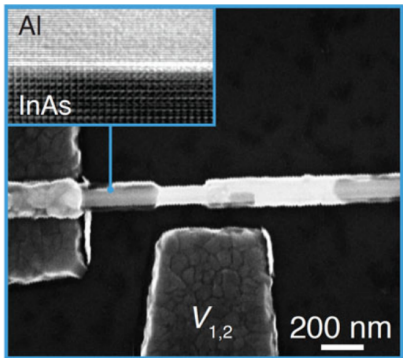


Figure 7: Scanning electron micrograph of a gated semiconducting weak link Josephson junction inside a gatemon. From [19].

oxide semiconductor (CMOS) technologies. Indeed, since these processes are the most widespread and known, the path to widely reproducible gatemon qubit will probably go through CMOS. Thus, our goal is to build a silicon based gatemon. The next question will be the choice of the CMOS compatible superconductor that need to show a highly transparent interface with silicon. We focus on silicides ($PtSi$, V_3Si) and superconducting silicon.

During the past 3 years, Tom Vethaak shown that V_3Si can be overtaken by $PtSi$ mainly because of process considerations. He also measured induced superconductivity in the channel of $PtSi/Si$ Josephson field effect transistors (JoFET) and shown the gate control of this induced superconductivity by tuning the Schottky barrier width. These measurements have been done on 30 years old devices produced at that time to investigate $PtSi$ Schottky barrier transistors, their geometry is shown on figure 8. As shown figure 9, the differential conductance is zero inside the superconducting gap for gate voltage $|V_G| < 3V$ and coherence peaks are observed at the gap edges. These features are the consequence of the discontinuity of the density of states on the superconducting $PtSi$ contacts. By applying a large gate voltage we observe a non zero differential conductance around zero bias which indicates the appearance of an Andreev current.

The aim of this internship is to look at the fabrication of high quality $Si/PtSi$ interfaces at the CEA Leti quasi-industrial platform. Furthermore, superconducting silicon have been studied for a few years and seems to be well appropriate for high quality interface Sm-S junctions [21][22][23]. We will investigate this option during the next few years with the partnership of the C2N Lab in Saclay.

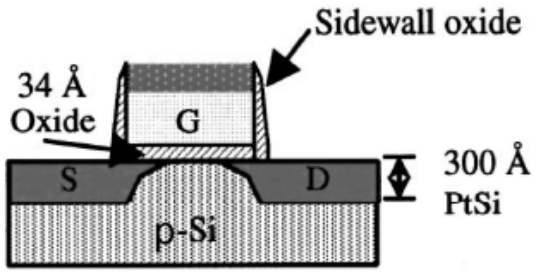
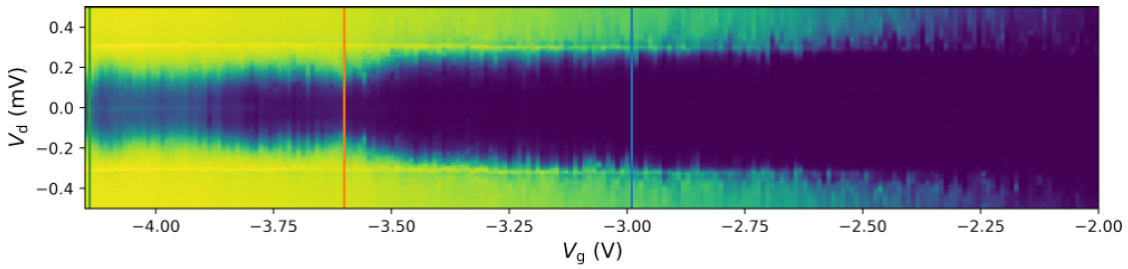
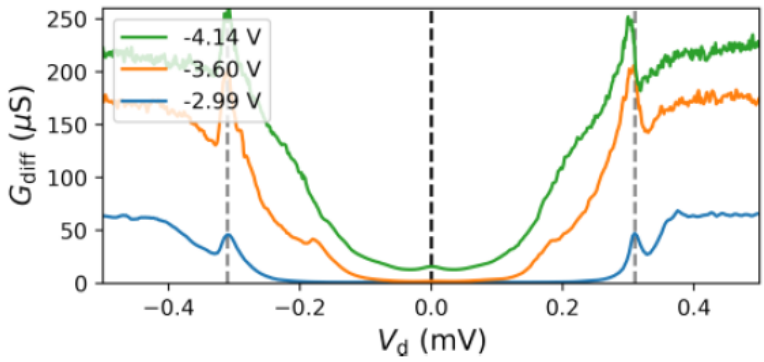


Figure 8: Schottky barrier PtSi/Si transistor from the 90's used to test if Andreev current can flow through it. From [20].



(a)



(b)

Figure 9: (a) Differential conductance map of the PtSi Schottky barrier transistor where the gate voltage and drain/source voltage are scanned. (b) 3 cut lines highlighting the appearance of the coherence peaks first and then of the non zero sub-gap conductance when a sufficient gate voltage is applied. From [20].

3 Experimental techniques

Now that we defined the point we want to focus on: the transparency of the interface between superconducting PtSi and silicon. The first thing we need is to cool down our samples while measuring them. To do so, we will use a dilution fridge. In this section, the cryogenic setup will be first discussed before going on a technique called transverse length measurement (TLM) that will permit us to precisely characterize those PtSi/Si interfaces.

3.1 Dilution fridge

All around the world, dilution fridges gained a foothold in laboratories as soon as researchers need to study physical phenomena at very low temperature. The dilution refrigerator principal was first proposed by London in the early 50's and London, Clark and Mendoza did the first demonstration in the 60's. Then, during the next decade, this technology have been introduced in many laboratories and permits now to reach very low temperature up to 2mK.

Even if many technological improvements have been done until today, the physical principal that gives the cooling power remains the same. The dilution implies the two isotopes of helium:

- ^{4}He that is the isotope commonly found in nature as a co-product of gas extraction for instance.
- ^{3}He that is much more challenging to find on earth and is mostly produced thanks to the tritium beta decay that occurs in stored nuclear warhead or in dedicated installations [24].

These two isotopes are very different since ^{4}He is a boson whereas ^{3}He is a fermion and, very interesting for our purpose, ^{4}He becomes superfluid (superfluid names fluids that show a transition toward a zero viscosity state) below 2.17K when ^{3}He does below 2mK.

The cooling principle is based on the ^{3}He-^{4}He phase diagram presented on figure 10. The crucial point is that below the tri-critical point at 0.87K the ^{3}He-^{4}He mixture presents a two-phase region surrounded by a "concentrated phase" where ^{3}He is dominant and the "dilute phase" where the ^{4}He dominates. Thus, in the mixing chamber, where the cooling power is produced, these two phases stand. The concentrated phase, being lighter because ^{3}He has a lower mass than ^{4}He, floats over the dilute phase. All the process consist in extracting ^{3}He atoms from the dilute

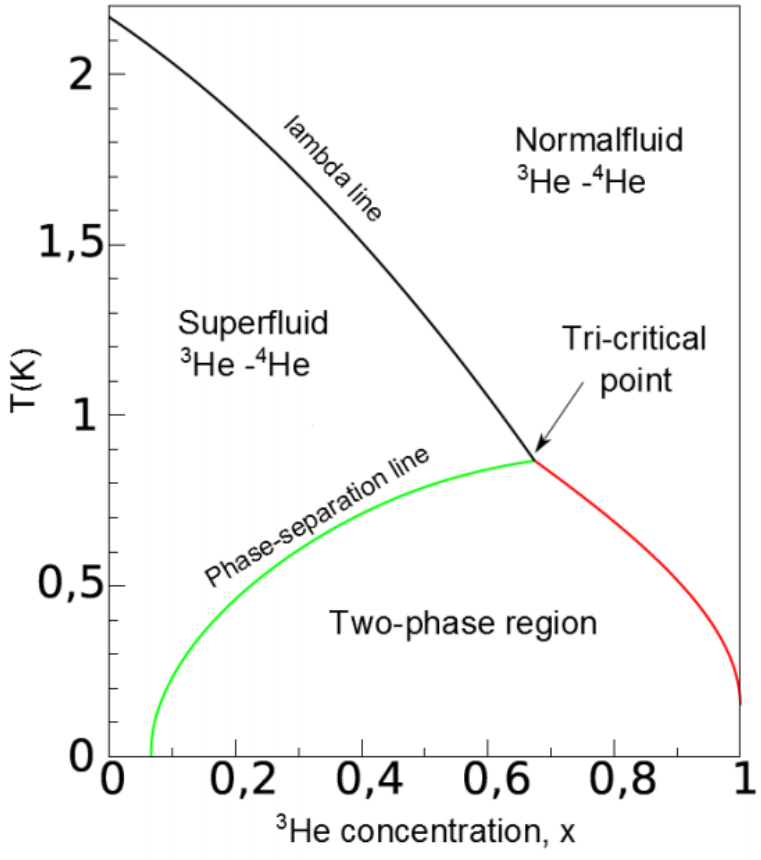


Figure 10: Phase diagram of the ^{3}He/^{4}He mixture at saturate vapor pressure. We notice the separation into two phase below a tri-critical point. From [25].

phase to put them in the concentrated one. Doing so, the phase diagram tells us that the mixture will be cooled down. The cooling power is produced at the interface of the two phases.

The figure 11 describes the working principle of a wet dilution fridge. The first cooling step is the cooling down from room temperature to 4.2K by plunging the system into a liquid ^{4}He bath. Then, by pumping over a ^{4}He pot we get a first cooling power permitting to reach 1K thanks to a Joule-Thomson expansion. This first cooling step permits to condensate the ^{3}He that is injected toward the mixing chamber, more precisely toward the concentrated phase that floats over the dilute one inside the mixing chamber. Here, the goal is to extract some ^{3}He atoms from the dilute phase. To do so, the dilute phase is pumped toward the still, which is warmer

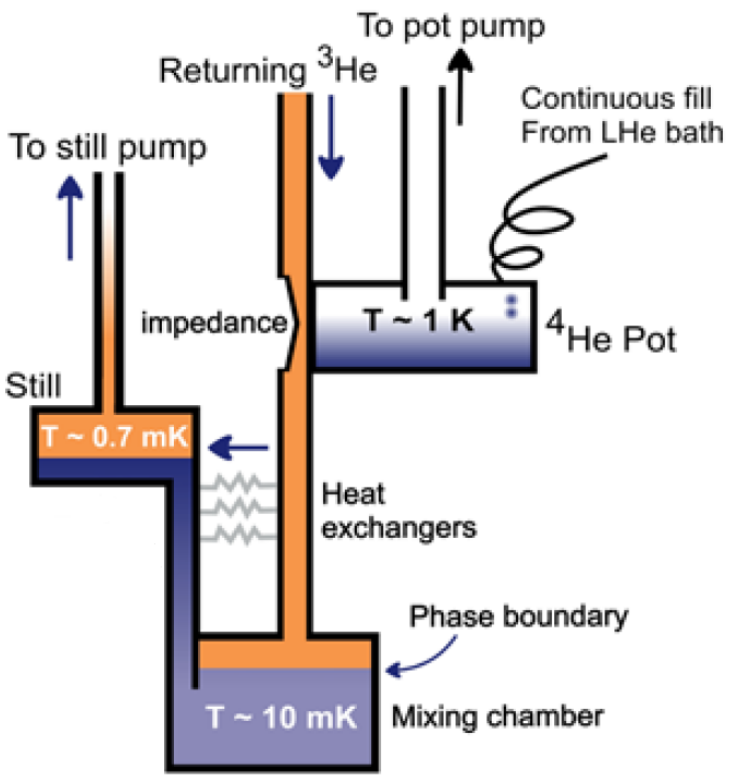


Figure 11: Schematic description of a wet dilution fridge composed of a 1K pot, a mixing chamber and a still. From [26].

(about 700mK). In the still, the pressure and temperature implies a continuous evaporation of the ^{3}He, the gaseous phase present in the still is pumped, and the loop is closed. During all that process a small part of the ^{3}He from the dilute phase in the mixing chamber migrates to the still and is finally added to the concentrated phase. Doing so and because of the previously discussed phase diagram (Fig 10), a cooling power is produced at the interface of the dilute phase and the concentrated phase inside the mixing chamber.

3.2 Transverse length measurements (TLM)

The aim of the internship is to study the electrical behavior of superconductor-semiconductor interfaces. To do so, we have fabricated structures made of a doped silicon channel with two PtSi contact plugs. From such devices, we have to extract

the resistance of one $PtSi - Si^+$ interface while measuring the resistance of the whole device. A method is to build devices (as shown figure 12) with variations in the silicon channel length L and width W from one device to the other. The total

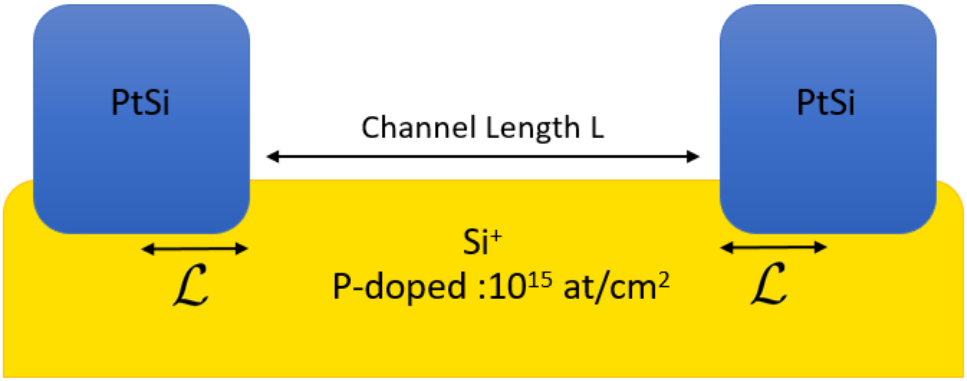


Figure 12: Schematic representation of the kind of TLM device we use to study the electrical behaviour of the PtSi/Si junctions.

resistance R_{tot} of such a device is written as follows, where Rc is the $PtSi - Si^+$ contact resistance and $Rs(Si^+)$ the silicon channel sheet resistance:

$$R_{tot} = 2Rc + \frac{L}{W} Rs(Si^+) \tag{3.1}$$

By plotting R_{tot} as a function of L/W we can extract the silicon sheet resistance of the channel Rs and the contact resistance of the junctions Rc by simply doing a linear regression. Then we want to extract the interface resistance between the superconducting PtSi and the Si channel. We define $\mathcal{L}$ the length of the contact involved in the current transport. We assume that the current density is uniform along this length $\mathcal{L}$ and we neglect the resistance of the bulk PtSi. Rb is the interface surface resistance (expressed in $\Omega.\mu m^2$) and Rs is the sheet resistance of the silicon underneath the contact. From geometric considerations we get:

$$Rc = \frac{Rb}{W\mathcal{L}} + \frac{\mathcal{L}}{W} Rs \tag{3.2}$$

$\mathcal{L}$ is derived by considering its optimum to minimize Rc:

$$\frac{\partial Rc}{\partial \mathcal{L}} = 0 \Leftrightarrow \mathcal{L} = \sqrt{\frac{Rb}{2Rs}} \tag{3.3}$$

By combining 3.2 and 3.3, we finally get an expression of the contact resistance:

$$Rb = \frac{2W^2Rc^2}{9Rs} \tag{3.4}$$

Additionally, we have another type of devices, named Kelvin crosses. These are made of a doped silicon bottom electrode and a metallic perpendicular top electrode, the two electrodes are linked by a PtSi plug similar to those present in the TLM devices (see Fig. 13). In that case the four wires measurement gives access directly to Rc.

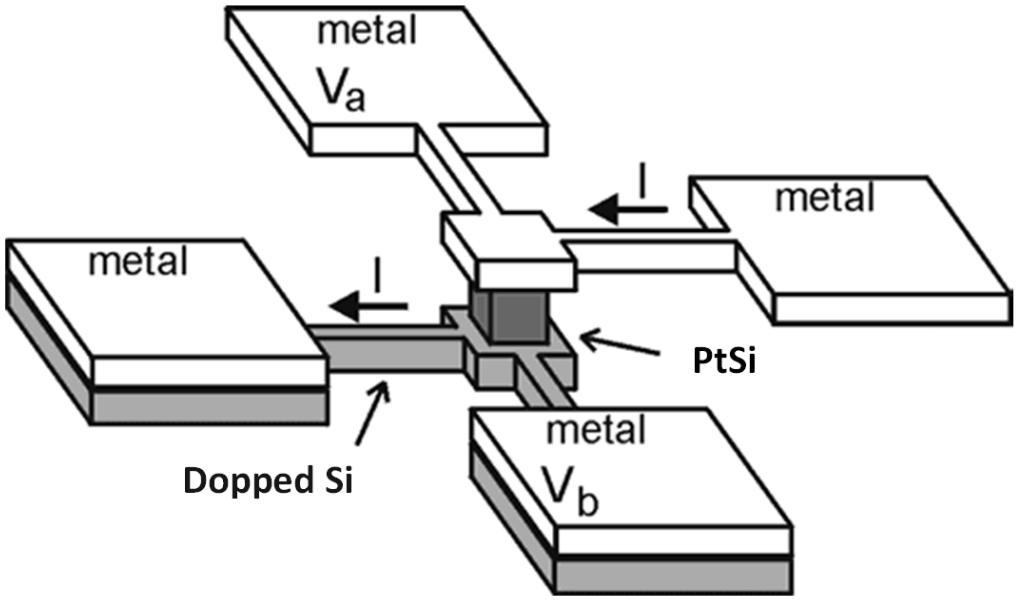


Figure 13: Schematic representation of the Kelvin crosses used to measure the $PtSi-Si^+$ interface resistance.

4 PtSi/Si junctions

Our goal is to reach a demonstration of a silicon based Josephson junction industrial fabrication; here the PtSi-Si junctions are explored. Thus, thanks to a collaboration with the CEA Leti, we can experiment our process flow in order to define the right way to produce high quality PtSi-Si Josephson junctions. We can also rely on the growth and material science expertise at the Leti that permits to combine all the required skills for the success of the project. This section will first deal with the fabrication of TASP wafers before exposing the TLM measurements at room temperature and at very low temperature followed by the I-V measurements done at very low temperature including also Kelvin cross devices.

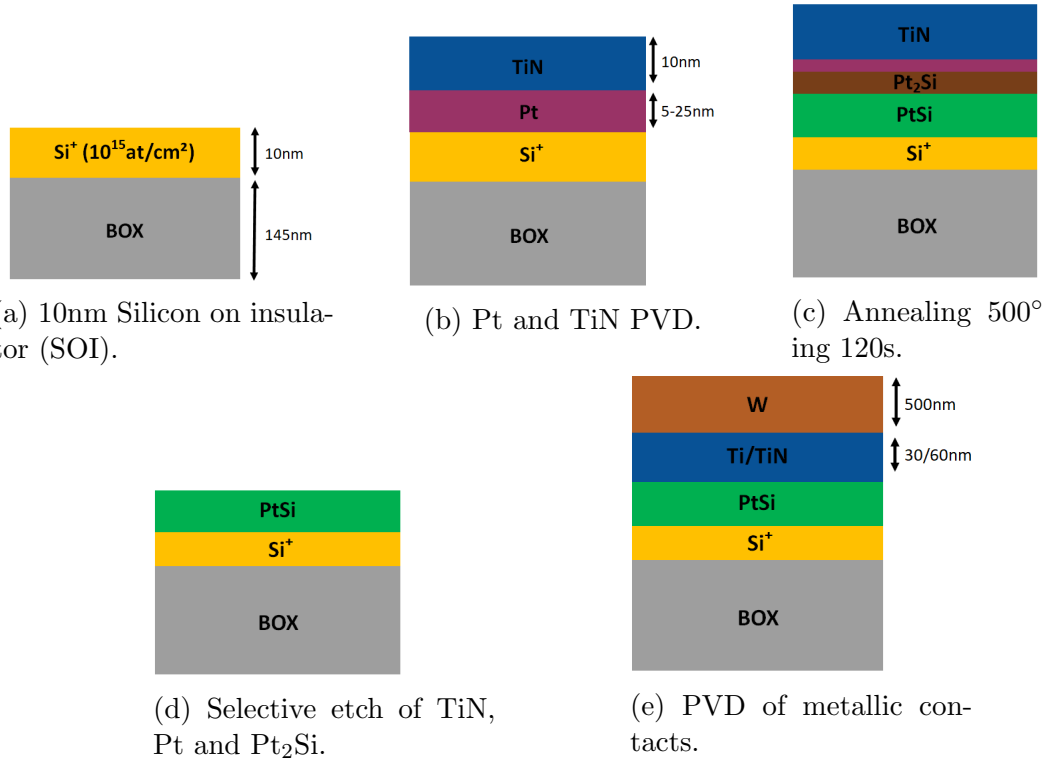
4.1 Fabrication process

TASP wafers are silicon on insulator (SOI) wafers p-doped at $10^{15} at/cm^2$ (10nm thick Si layer on a 145nm BOX) (Fig. 14a) on which TLM and Kelvin cross patterns are firstly optically lithographed. After some plasma cleaning, a Pt thin film is deposited by physical vapor deposition (PVD). The Pt thickness varies from 5nm to 25nm over 5 different wafers (table 1). Then a TiN protection cap is deposited by the same way in order to protect the platinum during the following annealing step (Fig. 14b). The annealing is processed at 500°C during 120s (Fig. 14c). The TiN and the non-reacted Pt are then selectively etched (Fig. 14d). Finally, metallic contacts are added (Fig. 14e).

Wafer	Pt deposition	Annealing
W07	5nm	500°C 120s
W09	10nm	500°C 120s
W10	15nm	500°C 120s
W11	20nm	500°C 120s
W12	25nm	500°C 120s

Table 1: Split table for TASP wafers, all of them are 10nm SOI.

The formation of PtSi is a two step process. In the first temperature range, between 200°C and 300°C, platinum atoms diffuse into the silicon layer and a Pt_2Si phase appears. Then, at higher temperatures, between 300°C and 500°C, the silicon atoms diffuse into the Pt_2Si phase and form a PtSi phase. Finally, 1nm of platinum deposited on silicon can result in a 2nm PtSi layer.



(a) 10nm Silicon on insulator (SOI).

(b) Pt and TiN PVD.

(c) Annealing 500°C during 120s.

(d) Selective etch of TiN, Pt and Pt_2Si.

(e) PVD of metallic contacts.

Figure 14: Process flow of the PtSi/Si junctions fabrication.

One of the main challenges in this process is the fully consumption of the Pt_2Si phase. To consume the Pt_2Si phase, some silicon atoms have to diffuse toward this phase but the limiting parameter can be the quantity of silicon that is actually available for the process. This limitation can simply come from the lack of silicon, here we use SOI wafer with a 10nm silicon layer over the BOX. To solve this issue, the important parameter is the amount of platinum that is deposited on the silicon layer. For instance, if the stoichiometry is well respected (1 atom of silicon for 1 atom of platinum), the formation of the Pt_2Si intermediate phase should consume all the Pt and half of the Si while the diffusion of Si atoms in Pt_2Si will consume all the Pt_2Si to form a pure PtSi layer. Furthermore, all the platinum deposited besides the silicon patterns can diffuse toward it so taking the Pt thickness in consideration is not always enough.

The 5 wafers are then tested with an automatic probe station at room temperature. These measurements tell us that only the wafer W07 (5nm Pt deposited) for both TLM and Kelvin crosses and W09 (10nm Pt deposited) for Kelvin crosses

seems to show a good silicidation. The following studies will focus on these 2 wafers.

4.2 TLM

The principle of TLM, previously explained, is applied here to a set of devices from W07 composed of two PtSi plugs separated by a doped silicon channel. The size of the PtSi/Si contact is 0.35x1.25μm. To begin with, we processed a bunch of 4 wires resistance measurements for various channel dimensions at room temperature with a probe station. Then, plunging the device into liquid helium we did the same at 4K. The measurements are plotted figure 15.

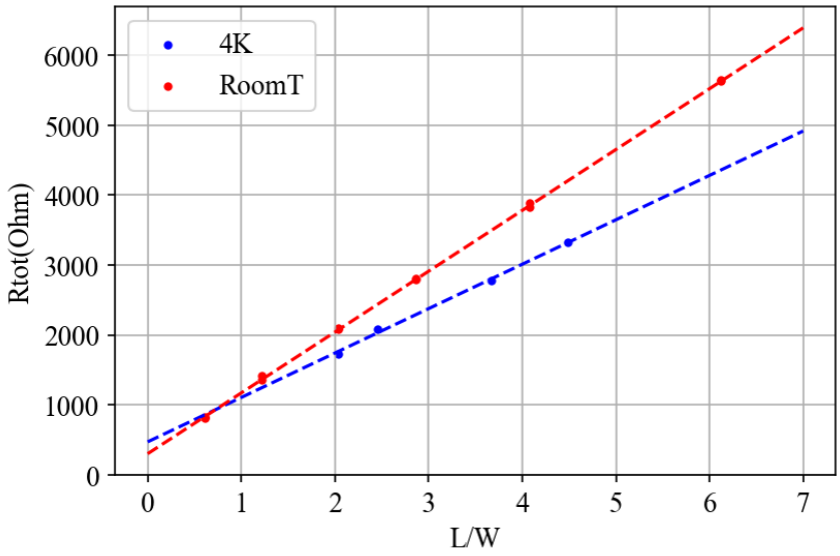


Figure 15: TLM resistance measurements for a 0.35x1.25μm PtSi/Si contact from W07 at room temperature and at 4K. Linear fits are done (dotted lines).

As shown eq. 3.1, we get a linear relation between the resistance of the device and the L/W ratio (dimensions of the channel). We deduce from these fits the silicon sheet resistance and the contact resistance between the PtSi and the Si listed in the table 2.

Two remarks about this result:

- This sheet resistance corresponds to a resistivity of $8,7.10^{-4}\Omega.cm$ at room temperature which is consistent with the doping level ($10^{21}at/cm^2$). The highly

Temperature	Rs(Si^+)	Rc
300K	870Ω	150Ω
4K	635Ω	235Ω

Table 2: Sheet resistance of the Si^+ channel Rs and PtSi/Si contact resistance Rc from W07 (0.35x1.25μm contacts).

doped silicon should behave as a metal and this is what we observe, its resistivity decreases with the temperature. The first order phenomena is the freezing of the crystal and so the reduction of phonons/electrons interactions. This classical interpretation also tells us that the resistivity should saturate at some point when all the phonons/electrons interactions have disappeared and only the defects of the crystal are the origin of the remaining resistivity.

- The contact resistance increases while the temperature decreases. Here, the first order phenomena is linked to the Schottky barrier present at the interface. The thermally activated electronic transport across this barrier is reduced by the cooling down and the tunneling of electrons across the barrier remains a source of conductance even at very low temperature.

The same kind of measurements is done at very low temperature by using a dilution fridge. We kept the same PtSi/Si contact size and measured the zero bias resistance of 4 devices at temperatures between 75mK and 700mK. For the sack of clarity, these TLM data are represented on figure 16a for only five of those temperatures.

Firstly, we notice that the origin of these TLM linear fits increases while the temperature decreases. Indeed the contact resistance rises at very low temperature because of the superconducting gap opening in PtSi. The contact resistance is extracted and plotted figure 16b. This phenomena will be more deeply discussed in section 4.3.

Secondly, the TLM lines on figure 16a seem to be parallel but actually they do not. The sheet resistance of the silicon channels, which corresponds to the slope of these lines, is plotted figure 16c. We notice that the resistivity of the highly doped silicon does not decrease any more with temperature or even saturate, as its quasi-metallic behavior should predict. To explain this we may rely on a positive correction of the resistivity in disordered electronic systems at very low temperature called weak localization [27]. The classical Drude model takes in consideration the individual diffusive motion of each electrons to derive its probability to cross the conductor. At

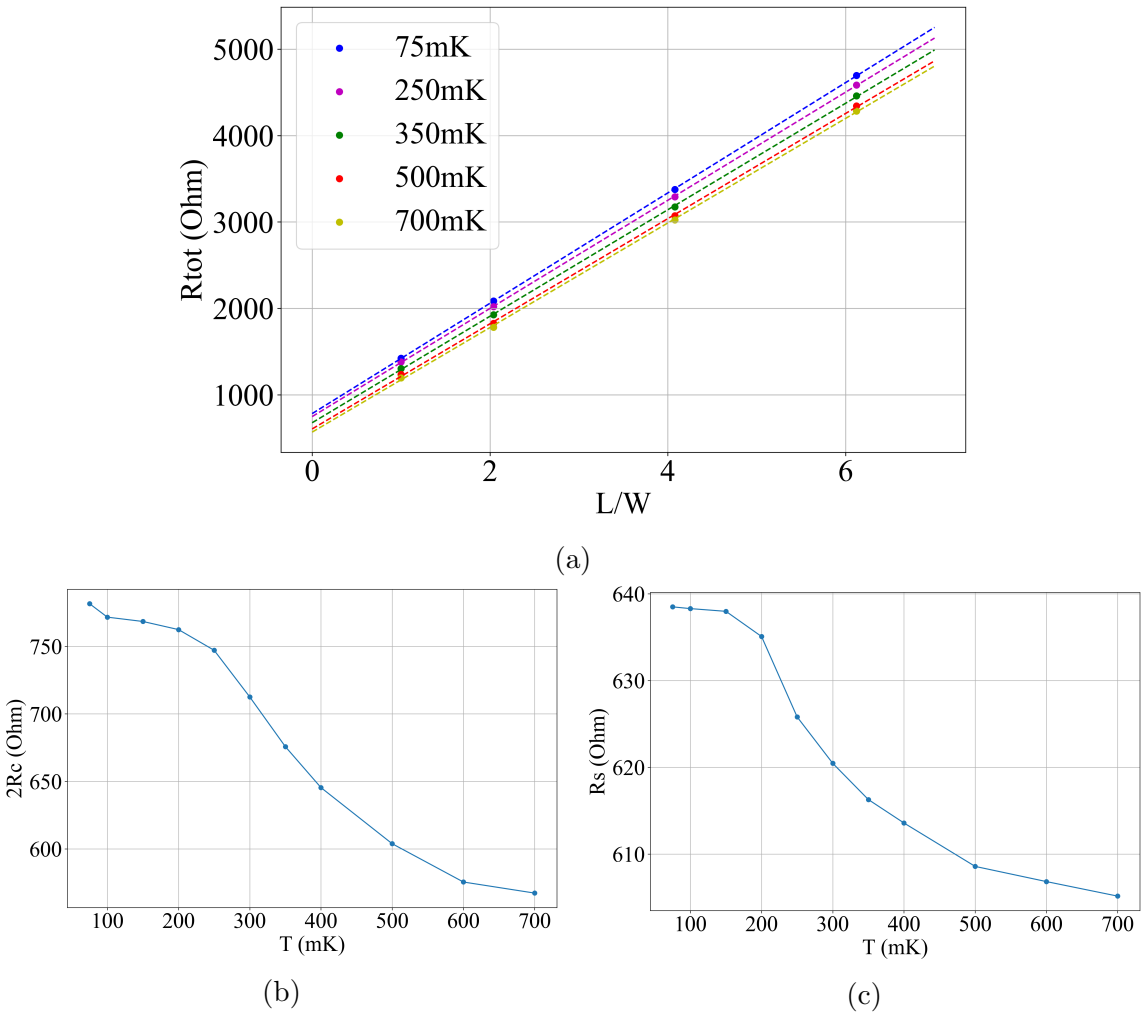


Figure 16: (a) The total resistance of devices with different channel dimensions is plotted for different temperatures. The TLM method is applied thanks to linear fits (dotted lines). (b) From the TLM linear fits origin, we extract the contact resistance at the PtSi/Si interface for various temperature. (c) The sheet resistance of the channel silicon is also deduced from TLM and plotted with respect to temperature.

very low temperature, some quantum effects have to be considered and a correction term is added to the Drude model. The electron can follow different paths and we have to look at the interferences that can occur between these paths. Doing so, we understand that the wave function describing the electron can experience localization due to these interferences. This phenomenon results in a reduction of the probability

for the electron to cross the conductor and so an increase in resistance. The saturation of the phenomenon below 150mK may be the consequence of a saturation of the electronic temperature of the system that may be no more perfectly coupled to the phonons temperature measured by our thermometer. One should carry out some magnetoresistance measurements to test these hypothesis.

4.3 I-V measurements

Knowing the sheet resistance of the silicon channel, we are now able to study the electrical behavior of the PtSi/Si interfaces. We will measure the resistivity of the same samples but this time we will also bias the devices with a DC current. The goal is to scan the differential resistance of the junction over all the PtSi superconducting gap and outside. The measurements are processed at very low temperature in a dilution fridge. A four wires measurement technique is used. The device is biased by a DC current I_{DC} and an AC current δI_{AC} is sent through the device thanks to a lock-in amplifier. The voltage across the device is measured with a differential amplifier while the DC biasing I_{DC} is ramped up. The lock-in amplifier extracts the AC voltage δV_{AC} across the device and a voltmeter measures the DC voltage bias V_{DC}. The differential resistance of the device is deduced from:

$$R_{diff} = \frac{\delta V_{AC}}{\delta I_{AC}} \tag{4.1}$$

After measuring the TLM devices, we will do the same measurements on Kelvin crosses. The silicidation process have been the same. The differences come from the geometry that may influence the junction growth. These crosses are made of a simple PtSi/Si interface without any silicon channel.

4.3.1 TLM devices

The results obtained on three different TLM devices at different temperatures are shown figure 17.

The resistance of one PtSi/Si interface R_C is extracted thanks to our knowledge about the silicon channel conductivity:

$$R_C = \frac{R_{diff} - R_{Si}(T)}{2} \tag{4.2}$$

Where R_{diff} the complete device differential resistance and R_{Si} the silicon channel resistance. The same way we extract the bias of one interface V_C using the following

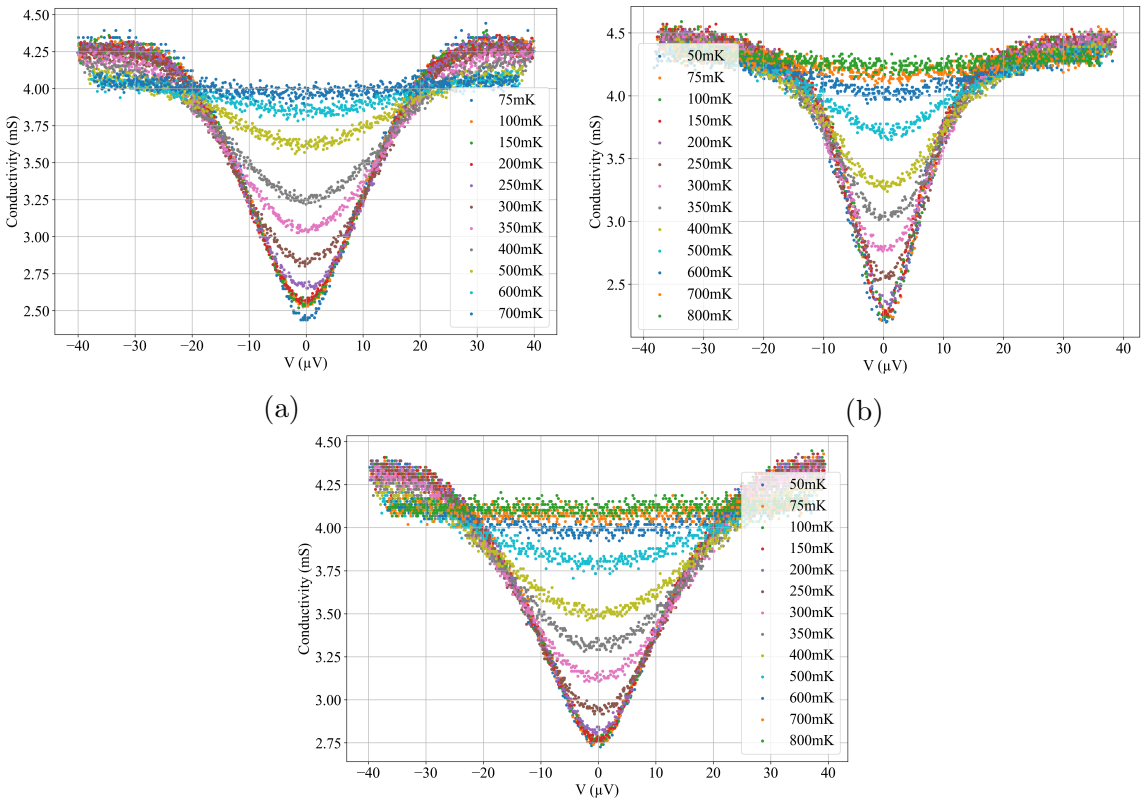


Figure 17: Differential conductance of a single PtSi/Si interface with respect to its voltage biasing. The measurements are shown here for 3 different TLM devices from W07: (a):RB0C1#3 (b):RB0C1#6 (c):RB0C1#2. While the sample are cooled down the zero bias conductivity drops and a conductivity gap opens before saturating around 200mK.

formula:

$$V_C = \frac{V_{DC} - I_{DC} R_{Si}(T)}{2} \tag{4.3}$$

Where V_{DC} the complete device bias and I_{DC} the DC bias current flowing through the device.

The first observation is the appearance of a conductance gap at lower biasing and that this gap disappears when the temperature get close to 700mK. This seems to be the consequence of the phenomena previously discussed in section 1.2. Indeed, at very low temperature the PtSi becomes superconducting and so a gap in its

density of states appears. This gap reduces the amount of charge carrier available for crossing the interface and so increases the resistance of the junction. From this understanding, we should deduce two things:

- The critical temperature of the PtSi layer present in our device is around 700mK. This result is in accordance with what have been previously measured for thin PtSi layers [20][25].
- Knowing the Tc of the PtSi layer, the BCS theory gives us the size of the superconducting gap as shown eq. 1.9. With Tc=700mK we get a superconducting gap $2\Delta \approx 200\mu eV$.

Knowing the theoretical superconducting gap of the PtSi layer we try to fit our measurements with the BTK model discussed in the section 1.2. We can obtain fits as the one shown figure 18, here the I-V measurement of the device RB0C1#2 TASP6/6 done at 250mK is fitted with the BTK model using the following parameter: barrier height Z=3, Dynes parameter $\Gamma = 1.9\mu eV$ and superconducting gap width $2\Delta = 15.4\mu eV$. A few remarks about this fit have to be done:

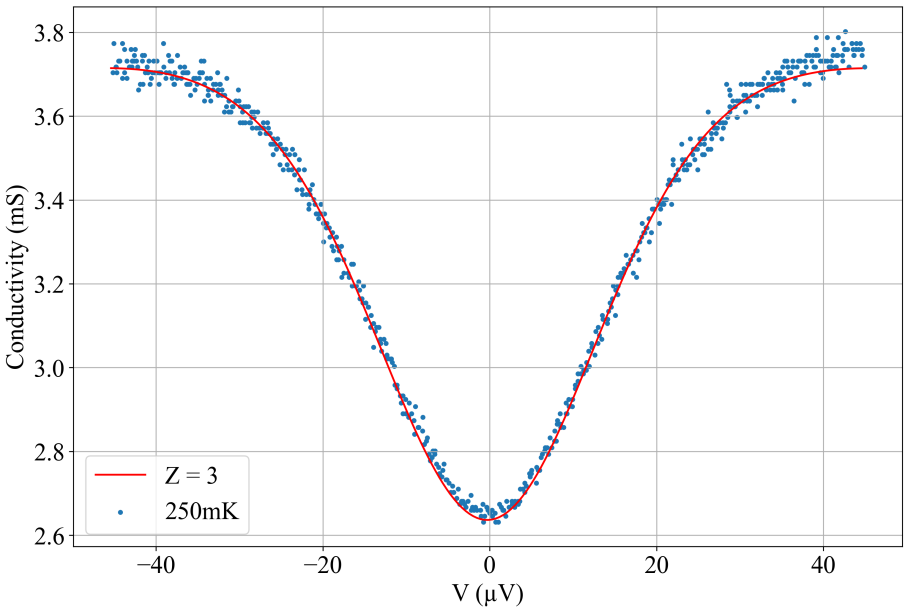


Figure 18: I-V measurement of RB0C1#2 W07 at 250mK and its BTK fit with the following settings: Z=3, $\Gamma = 1.9\mu eV$, $\Delta = 7.7\mu eV$.

- First of all, we have to be careful with this kind of fit since four different

parameters enter into account (temperature, barrier height, gap width, Dynes parameter). Indeed we observe that different sets of parameters can match one single measurement. So the fit shown figure 18 have to be seen as an indicative information but can not permit to determine by itself the parameters that characterize the interface. This observation is especially true when we do not see any coherence peak and when the gap is very smooth.

- Secondly, this fit gives us a gap $\approx 15\mu eV$ which is way below what BCS tells us for a Tc between 700mK and 1.1K (classical values for PtSi layer made with a similar process). Furthermore, a 15.4μeV superconducting gap would corresponds to a Tc around 50mK and should imply an opening of the gap in the I-V measurements at a much lower temperature. (Also, even if we do not trust the fit, observing the I-V curve we cannot imagine a gap Δ greater than 40μeV which corresponds to a Tc around 250mK so the gap width stills not coherent with the appearance of the zero bias conductivity drop as soon as the temperature is below 700mK.)

Thus we understand that this fit does not permit to determine the size of the gap. Another classical way to determine this Δ is simply to take the distance between the top of the two coherence peaks, this distance should be about the value of 2Δ. The issue for this set of measurements is that we do not observe any coherence peak, the reason may be the crystallographic disorder at the interface. All the challenge of the fabrication is actually here. To check this guess, some additional analysis should be done. For instance an X-ray photoelectron spectroscopy (XPS) could give us some decisive information about the chemical composition at the interface: Is the transistion between Si and PtSi sharp or smooth ? Is their some other phases at the interface ?

Moreover, we observe a kind of temperature saturation. Indeed, below 200mK, cooling down the device does not influence any more its behavior. This may not be the consequence of an electronic temperature saturation inside our device (due to a lack of filtration in the electrical setup for instance) since the phenomena have been observed on two different dilution fridges and measurement setups.

4.3.2 Kelvin crosses

Kelvin cross devices are made of a single $PtSi - Si^+$ junction, the structure provides 4 terminals that allows four wires measurements.

Wafer W07

We reproduce the same kind of measurements but with Kelvin crosses. This patterns come from the same wafer W07 as the previously discussed TLM devices and so the silicidation process have been exactly the same. Here, the devices are composed of one single PtSi/Si junction without any Si channel. The measurements are process on 3 devices that differ by the area of their interfaces. We measure their resistances thanks to the same four wires setup. The I-V curves we obtained for 3 of those devices are shown figure 19.

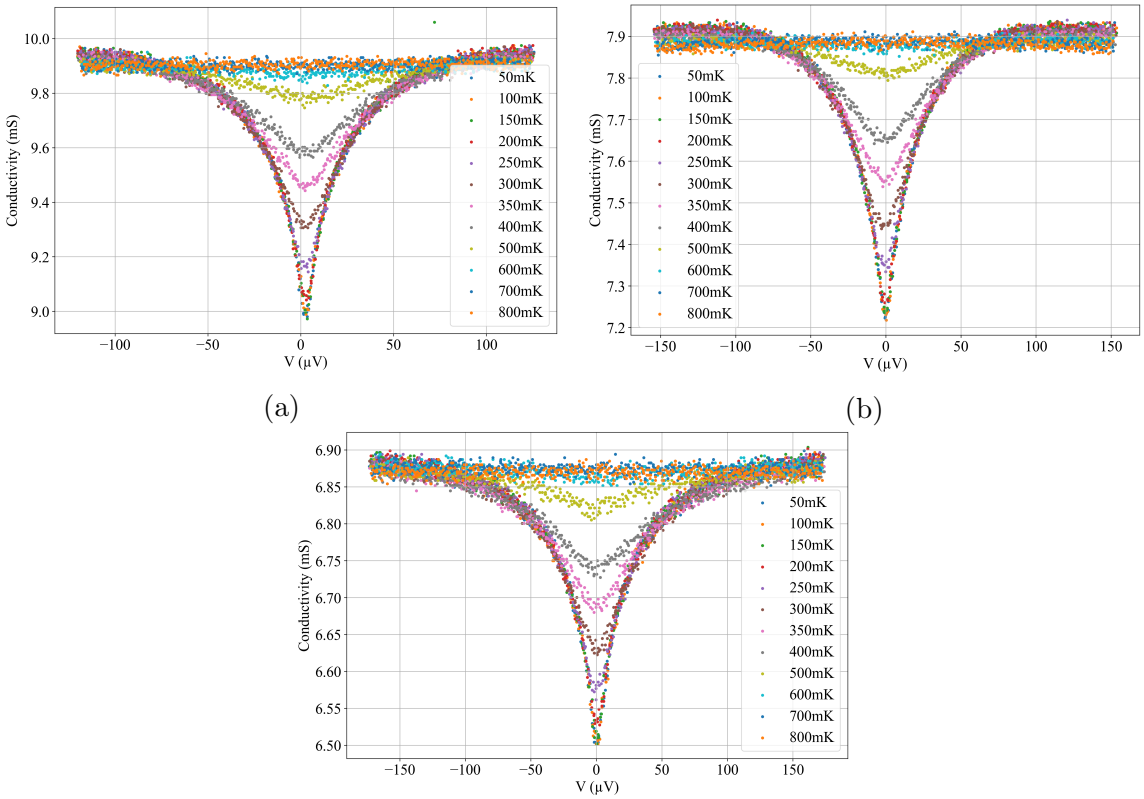


Figure 19: Differential conductance of a PtSi/Si interface with respect to its voltage biasing. The measurements are processed on 3 different Kelvin cross devices from W07 with 3 different contact areas: (a) KA0C1#1 6x6μm (b) KA0C1#2 5x5μm (c) KA0C1#3 4x4μm. While the sample are cooled down the zero bias conductivity drops and a conductivity gap opens before saturating around 200mK.

First of all, we notice that their is a linear relation between the normal con-

ductance of these devices and the area of the PtSi/Si interfaces. Just as for the TLM devices, we cannot easily determine the location of the coherence peaks so it is hard to extract the size of the gap. However, we observe that the Kelvin crosses show much sharper gaps with very narrow conductivity minimums around zero bias.

Wafer W09
The wafer W09 room temperature measurements shown that Kelvin crosses were well processed so we did the same measurements using these devices. Here the Pt deposition before annealing was 10nm (it was 5nm for W07) so the thickness of the PtSi layer should be greater if the amount of Pt was the limiting parameter for the PtSi growth on W07. The I-V curves we obtained for 3 of those devices are shown figure 20.

The depth of the conductivity gap measured on the W09 Kelvin crosses is in average 3 times those measured on the W07 for the same contact sizes. Also, the width of these gaps is about 1.5 times greater on the W09 devices.

An other interesting feature we observe is the appearance of smooth bumps at the edges of the gap on the figure 20c. These bumps could be interpreted as small coherence peaks and so indicate a behavior closer to the BTK predictions for a superconductor-semiconductor junction. Also, looking at the position of those pseudo peaks (dash blue lines) we can estimate the width of the superconducting gap: $2\Delta \approx 290\mu eV$. This value corresponds to a critical temperature $Tc \approx 950mK$ (according to eq. 1.9). This Tc is pretty close to the classical bulk PtSi Tc which is usually around 1K.

These observations could be the consequences of a sharper transition, at the interface, from the superconductor density of states to the metallic one. The W09 junctions behavior is maybe closer to the well known behavior of the conductivity at a bias sharp interface between a superconductor and a metal. If so, it means that the induced superconductivity in the silicon channel is weaker and so that the interfaces built on W09 are less transparent.

4.4 Conclusion

At the sight of these observations, it is hard to conclude about the actual structure of the junctions built on the CEA-Leti quasi-industrial facilities. However, the temperature dependence of the gap opening and the first marks of coherence peaks support the presence of a superconducting PtSi layer. Furthermore, to understand the electrical behavior variations previously exposed we should look at the crystallographic

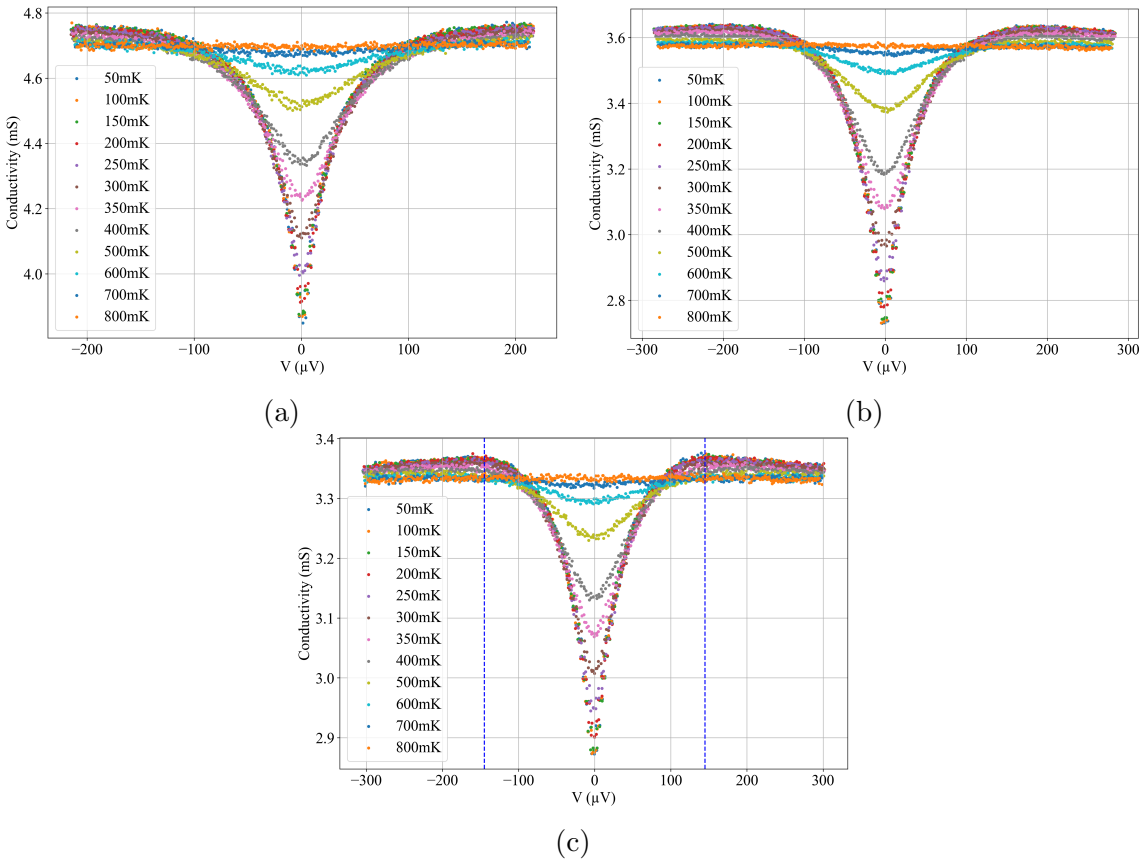
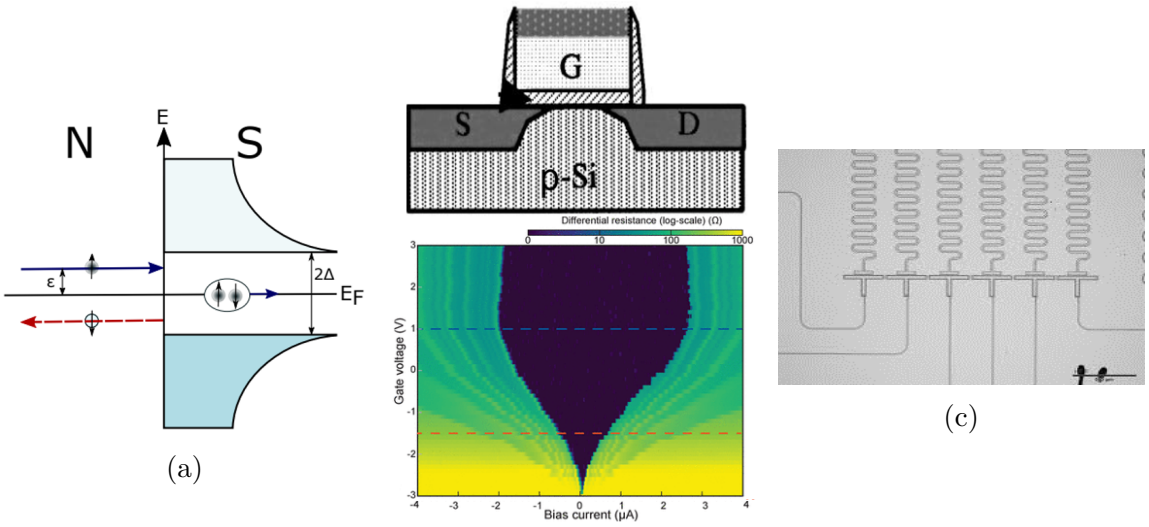


Figure 20: Differential conductance of a PtSi/Si interface with respect to its voltage biasing. The measurements are processed on 3 Kelvin cross devices from W09 with 3 different contact areas: (a) KA0C2#1 3x3μm (b) KA0C1#2 5x5μm (c) KA0C1#3 4x4μm, the conductance maximums are highlighted by the dashed lines.

and chemical characteristics of the interfaces. An XPS could give us some crucial information just as a tunneling electron microscopy (TEM) coupled with a focus ion beam preparation of the samples in order to look at the structure of the junction.

5 Road-map for future investigations

All the work presented here will be continued in the framework of my PhD in the LaTEQS team at the CEA-Pheliqs laboratory. The goal of the project is to reach the implementation of a silicon based gatemon qubit. As discussed in this report, the first step is to develop a reproducible process for the fabrication of silicide/silicon junction. During the past 3 years, Tom Vethaak studied a few silicide that were candidate for this kind of junction (V_3Si, $CoSi_2$ and $PtSi$). The PtSi/Si junction were studied thanks to some old Schottky barrier transistor fabricated at the CEA-LETI during the 90s. These devices showed very promising behaviors [20].



(a)

(b)

(c)

Figure 21: The road-map of the PhD project is made up of 3 main goals. (a) The first part will focus on the realization of highly transparent PtSi/Si junction with quasi-industrial facilities available at the CEA LETI. The goal is to maximize the rate of Andreev reflection at the interface between the superconductor side (S) and the semiconductor side (N). Electrons pair themself into Cooper pairs so they can tunnel across the superconductor. (b) Having a high quality interface, we will build a JoFET in which we should be able to tune the super-current. As shown here, the gate voltage permits to modulate the super-current amplitude in this Al/InAs based device from [28]. (c) Finally, we will build a quantum an-harmonic oscillator coupled to a resonator in order to have a complete gatemon qubit as it have been done here with Al/InAs based gatemon by [16].

The logical follow-up is to look at the process to fabricate such junction and to try to improve their transparency, the topic of my master thesis is precisely in this framework. The so called TASP wafers that we measured were a first try to build PtSi/Si junctions on the quasi-industrial 300nm facilities of the CEA-LETI. As reported here, this process of silicidation is not completely satisfying and the transparency of the interfaces have to be improved since it is a key point for the gatemon quality. Thus, the study and the improvement of these junctions and their fabrication in collaboration with the CEA-LETI will be the first goal of the coming PhD thesis (Fig 21a).

Being able to build high quality PtSi/Si interfaces, we will try to make Josephson field effect transistors with them. It will consist in a classical MOSFET for which the source and the drain are made of superconducting PtSi. A challenge here will be to induce a super-current across the silicon channel. To do so, the coherence of the Cooper pairs have to be ensured over all the channel and the transparency of the interfaces will play a major role in it. Then, having such a super-current, we will try to tune it through a gate voltage. The idea is quite the same as in a classical MOSFET, we modify the density of carrier inside the channel as well as the interfaces schottky barrier and so we tune the super-current that flows through the channel. Once we are able to do that we build the first silicon based JoFET (Fig 21b).

The final step, which is a more long range goal, is to make it a true gatemon qubit. Thus, we will have to couple this JoFET to a capacitor in order to build a quantum anharmonic oscillator. Then, we would like to be able to write and read this qubit in order to study its properties and finally see if this kind of device could be a great answer to the scalability issues encountered by every quantum computing technologies (Fig 21c).

6 Internship organization

Beyond the scientific results, a major objective was to train myself to all the experimentation techniques that I encountered and to the processing of the resultant data. Besides this experimental skills, these 6 months allowed me to acquire the theoretical knowledge that are required to work on these topics. All these aspects of the internship are at least as important as the scientific results presented here and their diversity is reflected in the Gantt chart of the internship conduct (Fig. 22). A cost estimation of the main expenses linked to this work is presented table 3.

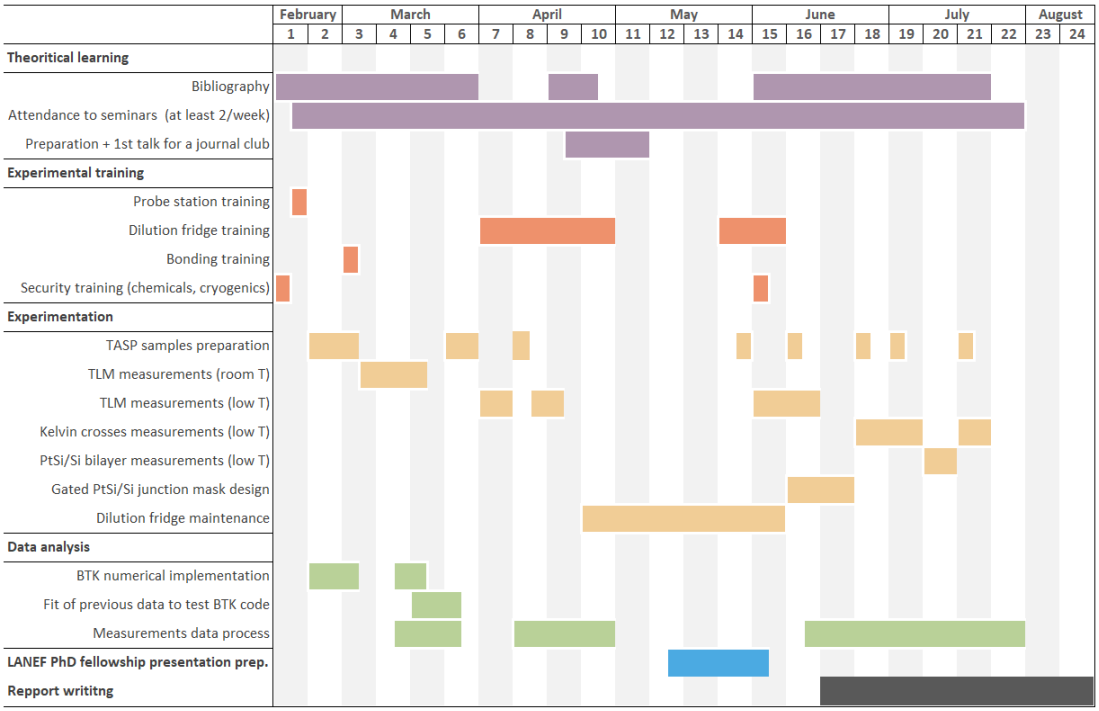


Figure 22: Gantt chart of the internship conduct.

Expenditure item	Description	Cost
Liquide Helium for dilution fridges	12x100L ($\approx$ 6 €/L)	7.2 k€
Dilution fridge use	4 months on 20 years old setups at 200 k€	3.3 k€
Wage	Total paid by the employer	9 k€
Total	Other fees are marginal	19.5 k€

Table 3: Estimation of the main expenses of the internship.

Conclusion

During this internship, I focused on the feasibility of silicon-based Josephson junction in a CMOS compatible technology. The long-term goal being the implementation of those Josephson junctions in JoFETs to ultimately build CMOS compatible and silicon based superconducting gatemon qubits. The superconductor we selected for these junctions is PtSi, this choice have been done considering the work previously achieved especially by T. Vethaak in the LaTEQS team [20]. Thus, this Master thesis aims to study the electrical behavior of PtSi/Si junctions made on the quasi-industrial CMOS facilities at the CEA-Leti.

The first section exposes the theoretical background required to understand the key issues of the project. The foundation of superconductivity, the Josephson Effect, the SQUID as well as the superconducting qubits are presented. Doing so, the frame of the project is laid out. Then, this framework is even more precisely depicted in the second section. The advantages of the gatemon geometry are explained and the recent work on this technology is shown. The third section goes into the experimental techniques that have been set up during the internship by focusing on the dilution fridge and the TLM principles. These tools are used to process the measurements exposed in the fourth section where the fabrication process of the junctions and their electrical behavior are discussed. These studies reveal the need for deeper analysis about the very structure of these junctions that can be done thanks to other tools as XPS for instance. Finally, the fifth section tells us about the road map for future investigations scheduled for the PhD thesis that will follow the internship and some details about the internship organization are given in the sixth section.

To finish with, one should keep in mind the major challenge of this work: the enhancement of the transparency at the superconducting-semiconducting interface. This point is probably a milestone in the race toward scalable CMOS silicon gatemon. PtSi could be the key just as superconducting highly doped silicon (Si:B) or even a combination of booth in order to get on one hand the strong superconductivity of PtSi (relatively high Tc) and in the other hand the very transparent interface that a Si:B/Si should provide.

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Glossary

BCS Bardeen, Cooper and Schrieffer gave their names to the theory of superconductivity they proposed in 1957.

BTK Blonder, Tynkham and Klapwijk proposed in 1982 the BTK model that describes the electronic transport at a superconducting - normal metal interfaces.

CMOS Complementary Metal Oxide Semiconductor is the most common fabrication technology for electronic devices.

CPB A Cooper Pair Box is a charge qubit made of a gated superconducting island coupled to a superconducting reservoir through a JJ.

Dynes parameter In 1978, Dynes proposed to add the eponymous parameter inside the density of state used in the BTK model in order to express the presence of states inside the gap.

Gatemon Is a superconducting qubit where the Josephson energy is modulated through a gate voltage.

JJ A Josephson Junction is made of two superconductors separated by a weak link through which Cooper pairs can tunnel.

JoFET A Josephson Field Effect Transistor is a key component of the gatemon qubit and basically a JJ where the weak link is capacitively coupled to a gate in order to modulate the amount of super-current that flows through it.

Kelvin Cross Design geometry that permits a four wire measurement of a SN junction.

MOSFET A Metal Oxide Semiconductor Field Effect Transistor is the basic component of every CMOS circuit and is made of a source and a drain separated by channel whose conductivity is modulated by a gate voltage.

Qubit Is a quantum two level system that stores the smallest information unit in quantum computing.

Shottky barrier Is a potential energy barrier that can appear at a metal-semiconductor junction equivalent to the difference between the metal work function and the semiconductor electron affinity.

SNS Superconductor - Normal metal - Superconductor junction.

SQUID A Superconducting Quantum Interference Device is made of two JJ placed in a superconducting loop, the current flowing through these JJ depends on the magnetic flux that flows through the loop.

Tc Is the critical temperature of a superconductor, in other words the temperature below which the material is superconducting.

TEM Transmission Electron Microscopy is a microscopy technique where the electrons are transmitted through a ultra-thin sample, it permit to observe the crystallographic structure of the sample.

TLM Transverse Length Measurement is a design and a measurement technique that permits to extract the channel sheet resistance and the interfaces resistances of a SNS junction.

Transmon Is a type of superconducting charge qubit designed to reduce the charge noise by increasing the ratio E_J/E_C.

XPS X-ray photoelectron spectroscopy is a technique to process a surface chemical structure analysis of a sample.