POLITECNICO DI TORINO

Master degree course in Mechatronic Engineering

Master Degree Thesis

High Energy Eensity DC-DC Converter for a Thermoelectric Generator

Supervisors
prof. Marcello Chiaberge
prof. Dario Gandini

Candidate
Leonardo Zio
ID: 277739

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Abstract

Energy saving is becoming more and more important as it allows for less pollution and reduces the economic cost. To achieve energy saving we can either reduce the amount of energy used or increase the efficiency of our system. This study deals with the second option, in particular, we want to increase the efficiency of the car. We can improve it by reusing the energy from the heat of the exhaust pipe, which would otherwise be wasted. This is not a trivial task since converting thermal energy into a usable source of energy is difficult, in fact in today's cars the thermal energy from the exhaust pipe is unused. This can be achieved by using a thermoelectric generator (TEG) and a DC-DC converter. The TEG is based on the Seebeck effect and it transforms thermal energy into electrical energy. In order to use this electrical energy in any useful way, we have to regulate the output voltage of the TEG. Here is where the DC-DC converter comes into play. In our application the output voltage will be used to charge the battery of the car. This whole system will reduce the alternator's work, thus reducing fuel consumption and reducing the emissions.

The aim of the thesis is to design and prototype a DC-DC converter with V_{in}=0-60V and V_{out}=13.5V with an input power up to 300W. A single PCB should be designed with all the needed parts: power, measures, microcontroller, supplies and communication interface.

The final prototype was successfully tested. The tests confirmed that the board works as it was designed to work, maintaining an excellent efficiency (>95% in almost all working points). All the other parts (measures, supplies, etc.) work well too.

Contents

Acronyms

ADC Analog to digital converter.

CAN Controller area network.

CCM Continuous conduction mode.

DAC Digital to analog converter.

DCM Discontinuous conduction mode.

EMI Electromagnetic interference.

ESR Equivalent series resistance.

GND Ground.

GPIO General purpose input/output.

JTAG Joint test action group.

MOSFET Metal–oxide–semiconductor field-effect transistor.

NIBB Non-inverting buck boost.

PCB Printed circuit board.

RMS Root mean square.

TEG Thermoelectric generator.

Introduction

Energy saving is becoming more and more important as it allows for less pollution and reduces the economic cost. To achieve energy saving we can either reduce the amount of energy used or increase the efficiency of our system. This study deals with the second option, in particular, we want to increase the efficiency of the car. Internal combustion engines have a low efficiency. Only abut 25% of the energy produced by the fuel combustion is used for the vehicle operation, the remaining 75% is wasted as heat, as shown in figure 1.1. We can improve this situation by reusing the energy from the heat of the exhaust pipe, which would otherwise be wasted. This is not a trivial task since converting thermal energy into a usable source of energy is difficult, in fact in today's cars the thermal energy from the exhaust pipe is unused. This can be achieved by using a thermoelectric generator (TEG) and a DC-DC converter. The TEG is based on the Seebeck effect and it transforms thermal energy into electrical energy. The output of the TEG is an unregulated voltage ranging form 0V to 60V, depending on the temperature difference ΔT on the input side. In order to use this electrical energy in any useful way, we have to regulate the voltage. Here is where the DC-DC converter comes into play. The DC-DC converter is a device that takes as an input an unregulated voltage and outputs a precise voltage. In our application the output voltage will be used to charge the battery of the car. This whole system will reduce the alternator's work, thus reducing fuel consumption and reducing the emissions.

Aim of the Thesis

The TEG is designed and provided by Magneti Marelli. The aim of this thesis is to design and realise a fully functional DC-DC converter (power part and control part) that allows a thermoelectric generator to charge an automotive battery with nominal voltage $12V$.

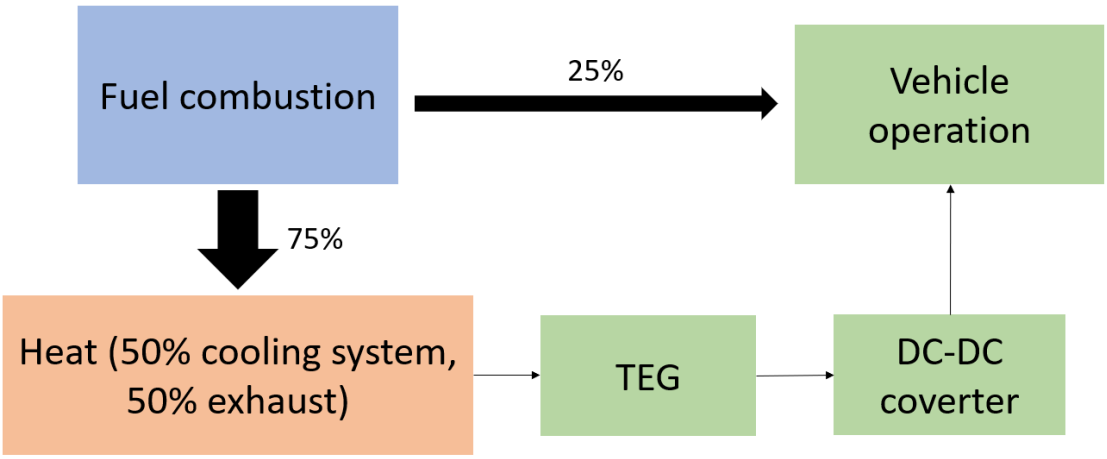


Figure 1.1: Fuel combustion energy diagram

Thesis Structure

This thesis is structured in chapters.

1. Introduction.
2. DC-DC Converters: various DC-DC converter topologies will be presented, choosing the most suitable for our application.
3. NIBB Design: practical design of the chosen DC-DC converter in all of its parts.
4. PCB Design: PCB design of the DC-DC converter.
5. Testing: testing of the prototype PCB.
6. Conclusion.

1.1 Thermoelectric Generator

A TEG is a device which transforms thermal energy into electrical energy. Its working principle is based on the Seebeck effect. What we are mainly interested in are the characteristics of the generator's output, which will be the converter's input. The TEG's output characteristics were found performing some tests and computing the interpolations with the collected data. We find the curves in figure 1.2, figure 1.4, figure 1.3.

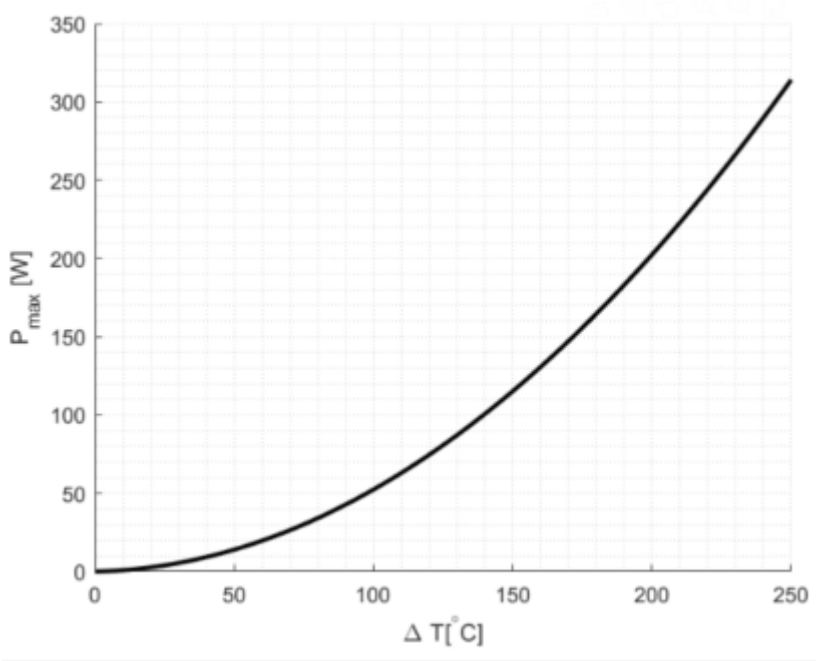


Figure 1.2: Maximum output power

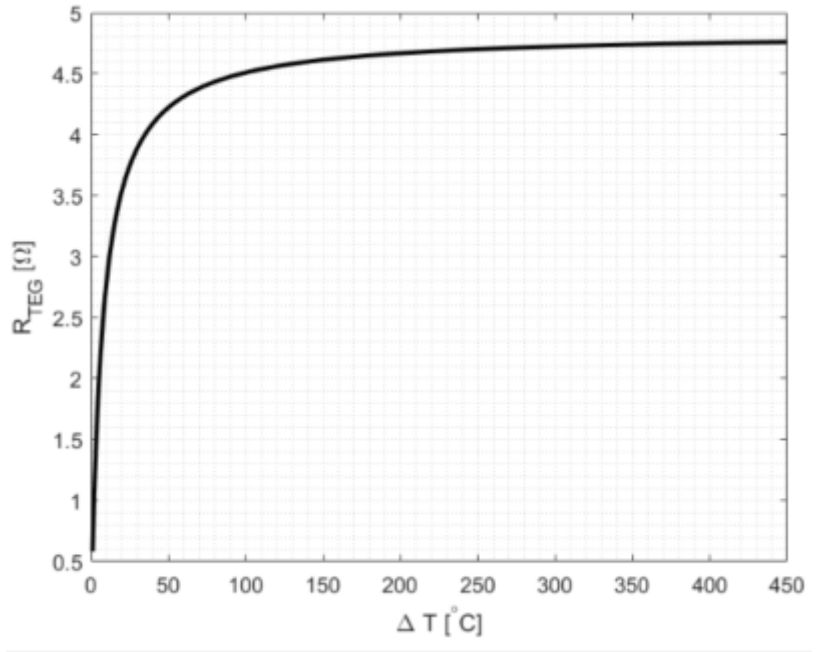


Figure 1.3: output resistance of the TAG

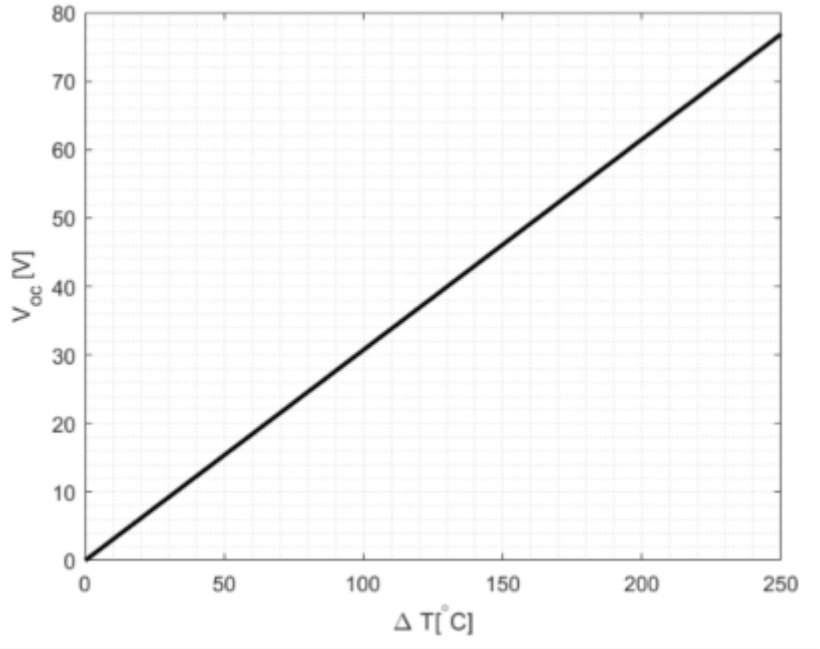


Figure 1.4: Open circuit output voltage

Where:

- P_{max} is the maximum available output power at a given ΔT
- R_{TEG} is the output resistance of the TEG
- V_{oc} is the output open circuit voltage

From the Maximum power transfer theorem we know that to obtain the maximum power from the TEG, the converter's input resistance should match the TEG's output resistance, and so we will have

$$V_{mp} = \frac{V_{oc}}{2} \tag{1.1}$$

Where V_{mp} is the TEG's output voltage in maximum power condition.

Given all the above information we can compute the curve that correlates P_{max} and V_{mp}. Once the correlation is found, we slightly raise the coefficients so that we will have a safety margin while designing the converter. The result can be seen in figure 1.5.

$$P_{max} = 0.4 \cdot V_{mp}^2 + 0.35 \cdot V_{mp} \tag{1.2}$$

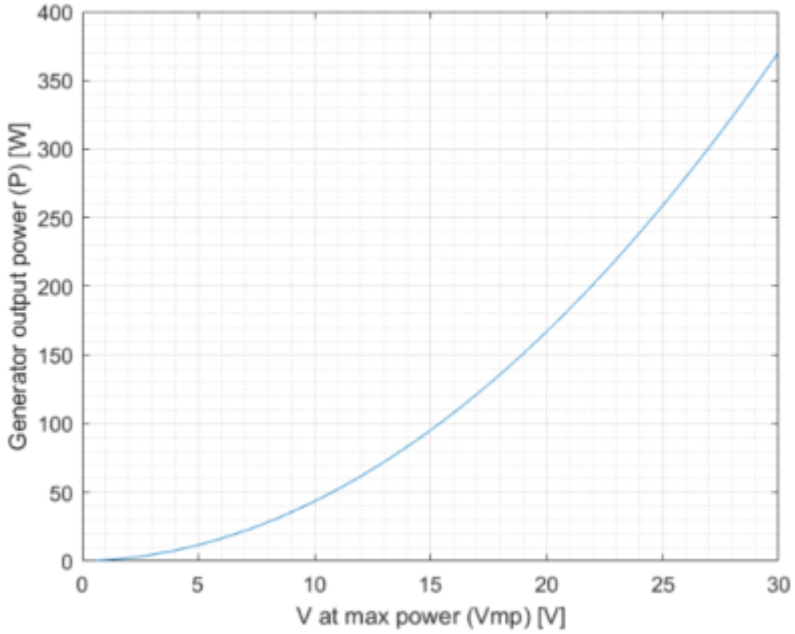


Figure 1.5: TEG's maximum power and output voltage correlation

DC-DC Converters

The aim of this thesis is to design and realise a DC-DC converter that allows a thermoelectric generator (TEG) to charge an automotive battery with nominal voltage $12V$. In this chapter we will see a brief explanation of the TEG, followed by a comparison of the possible topologies of DC-DC converters that could be used for the described purpose and finally a detailed description of the chosen topology, the non-inverting buck boost (NIBB).

2.1 Suitable DC-DC Converter Topologies

In section 1.1 we have seen that the input voltage of our converter will be approximately between 0 and 60 volts. On the other side of the converter there will be an automotive battery with nominal voltage $12V$, this means that we have to select a converter that can work both as a step-up and a step-down converter. There are 4 converter topologies that are normally used in these situations: the inverting buck-boost, the non-inverting buck-boost, the single-end primary inductor converter (SEPIC) and the cascade boost and buck which can be seen in figures 2.1, 2.2, 2.3 and 2.4 respectively.

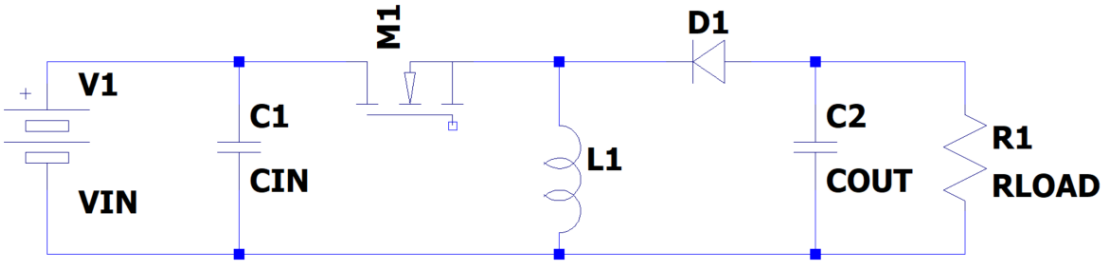


Figure 2.1: Inverting buck-boost

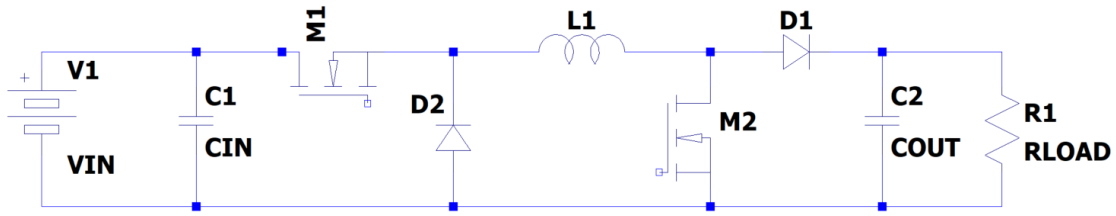


Figure 2.2: Non-inverting buck-boost

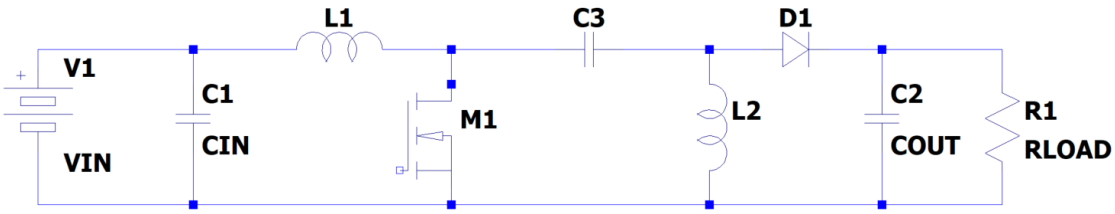


Figure 2.3: SEPIC

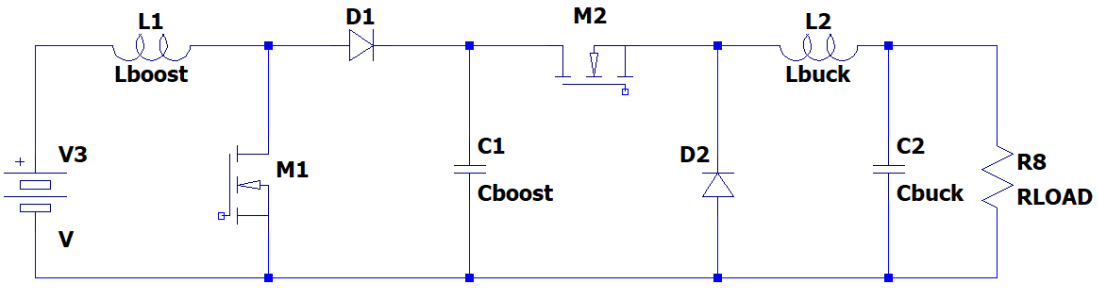


Figure 2.4: Cascade boost and buck

We have to discard the inverting buck-boost because, as the name suggests, its output voltage has inverse polarity with respect to the input voltage, which in our application is not desired.

The main drawback of the SEPIC is that it has an additional inductor and capacitor, which take a lot of space, dissipate power ad raise the cost. On the other hand the NIBB has ad additional diode and transistor, which don't take much space, but can dissipate a lot of power if they are switching. The cascade boost and buck works similarly to the NIBB, but it has a lot more components, so it is discarded.

Fortunately, as we will see in section 2.2, in our application, the NIBB rarely switches both transistors in the same switching period, so its major disadvantage becomes a minor problem. Given the simple magnetic component, higher power density and lower power loss relative to SEPIC we will choose the NIBB as the DC-DC converter for our application.

Topology	Number of passive components	Number of active components	Output polariry
inverting buck-boost	3	2	inverse
non-inverting buck-boost	3	4	direct
SEPIC	5	2	direct
cascade boost buck	4	4	direct

Table 2.1: Comparison between topologies

2.2 Non-inverting Buck-Boost

To improve efficiency we will use a NIBB with four switches instead of two, where the diodes are replaced by transistors.

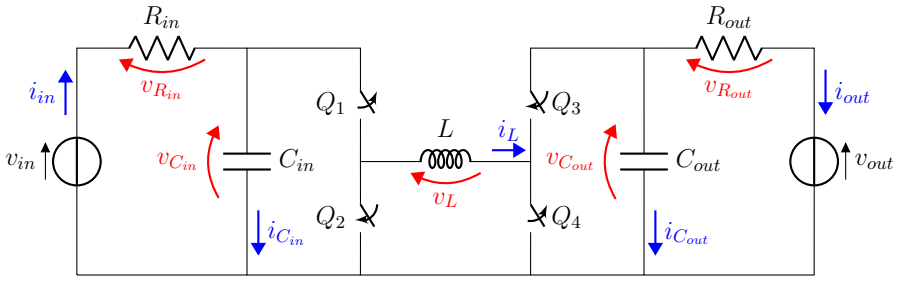


Figure 2.5: Non-inverting Buck Boost with 4 switches

Since we have to charge a $12V$ battery we set $V_{out} = 13.5V$.

Buck Mode and Boost Mode

To understand the NIBB working principle we can divide the converter in the buck leg (two transistors on the left) and the boost leg (two transistors on the right). We will refer to D_{buck} as the duty cycle of the buck leg and D_{boost} as the duty cycle of the boost leg, having that:

- when $D_{buck} = 100\% \implies$ Q1 is always ON, Q2 is always OFF

- when $D_{boost} = 100\% \implies$ Q4 is always ON, Q3 is always OFF

It is easy to see that if we set $D_{boost} = 0\%$ then Q3 acts as a short circuit and Q4 as an open circuit and the converter becomes a simple buck converter (this operating mode will be referred as buck mode), as can be seen in figure 2.6. The buck mode is used when $V_{in} > V_{out}$.

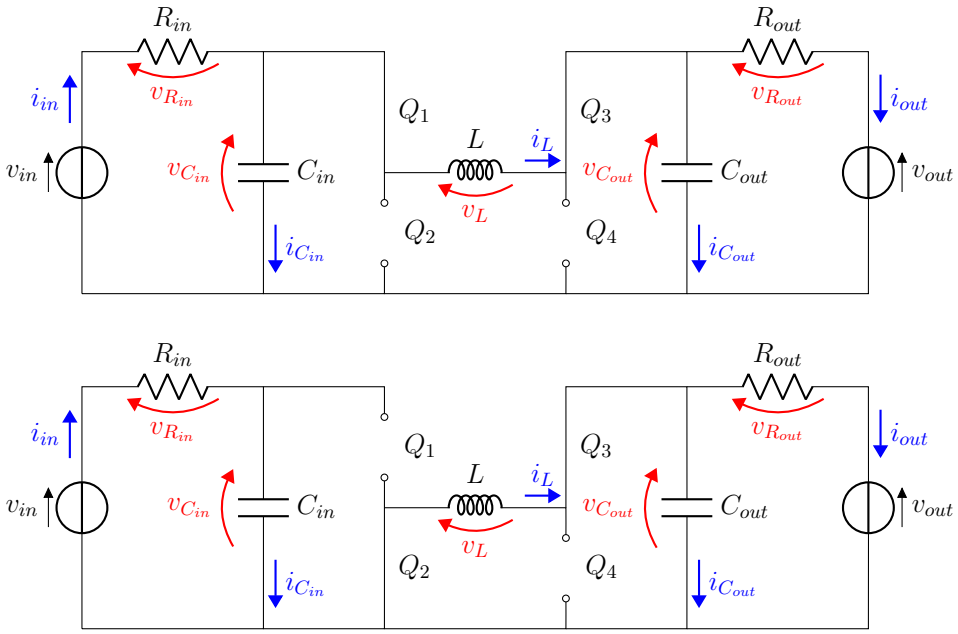


Figure 2.6: Buck mode switching, $D_{boost} = 0\%$

On the other hand if we set $D_{buck} = 100\%$ then Q1 acts as a short circuit and Q2 as an open circuit and the converter becomes a simple boost converter (this operating mode will be referred as boost mode), as can be seen in figure 2.7. The boost mode is used when $V_{in} < V_{out}$.

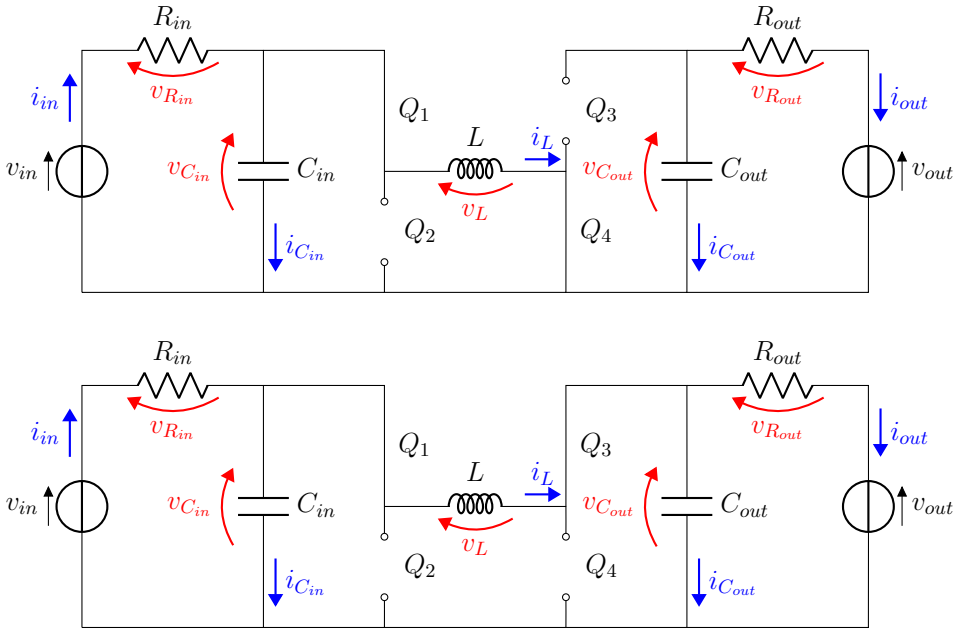


Figure 2.7: Boost mode switching, $D_{buck} = 100\%$

Using the volt-second balance technique and assuming that we are in continuous conduction mode (CCM), we can find the relation between V_{in}, V_{out} and the duty cycle in both buck and boost mode.

N.B.: the assumption of CCM is correct since we will design the converter to operate in CCM.

$$D_{buck} = \frac{V_{out}}{V_{in}} \tag{2.1}$$

$$D_{boost} = 1 - \frac{V_{in}}{V_{out}} \tag{2.2}$$

While deriving equations 2.2 and 2.1 it is assumed that there is no power loss. We have calculated also the case where there are power losses and it turns out that the two duty cycles were practically equal to the ideal case, so we decided to stick with the ideal duty cycles to simplify the analysis.

Buck-Boost Mode

We have analysed the two cases where $V_{in} < V_{out}$ and $V_{in} > V_{out}$, we can't extend the buck mode and the boost mode to the cases $V_{in} \leq V_{out}$ and $V_{in} \geq V_{out}$ because of the limitations in maximum and minimum allowable

duty cycles, so we have to introduce a new mode for the case $V_{in} \approx V_{out}$ which is called buck-boost mode.

In this mode both legs are switching and we can model the converter as a cascade of a buck and a boost converter, so to compute the duty cycle we just multiply the attenuation of the buck with the gain of the boost. One of the two legs will always be "passive", in the sense that its duty cycle will be constant, while the other leg will be the one regulating the output to the desired voltage. There will be two expression of duty cycle in the buck-boost mode, depending on which leg is the active one.

$$D_{buck(B-B)} = \frac{V_{out}}{V_{in}}(1 - D_{boostmin}) \tag{2.3}$$

$$D_{boost(B-B)} = 1 - \frac{V_{in}}{V_{out}} D_{buckmax} \tag{2.4}$$

Where $D_{buckmax}$ and $D_{boostmin}$ are the maximum and minimum achievable duty cycles and they depend on several factors, such as the switching frequency, the dead time, the type of transistor etc. A good estimation is $D_{buckmax} = 0.95$ and $D_{boostmin} = 0.05$.

We will have that when:

- $V_{out} - p < V_{in} \leq V_{out} \implies D_{buck} = D_{buckmax} = 0.95$ and $D_{boost} = D_{boost(B-B)}$
- $V_{out} < V_{in} \leq V_{out} + p \implies D_{boost} = D_{boostmin} = 0.05$ and $D_{buck} = D_{buck(B-B)}$

Where p defines the extent of the buck-boost mode and is set to $p = 2V$.

With the buck-boost mode defined we have a clear picture of all the working points. A graphical representation of the duty cycles is present in figure 2.8.

Mode	Input voltage
Boost	$V_{in} \leq 11.5V$
Buck	$V_{in} > 15.5V$
Buck-Boost	$11.5V < V_{in} \leq 15.5V$

Table 2.2: Modes summary

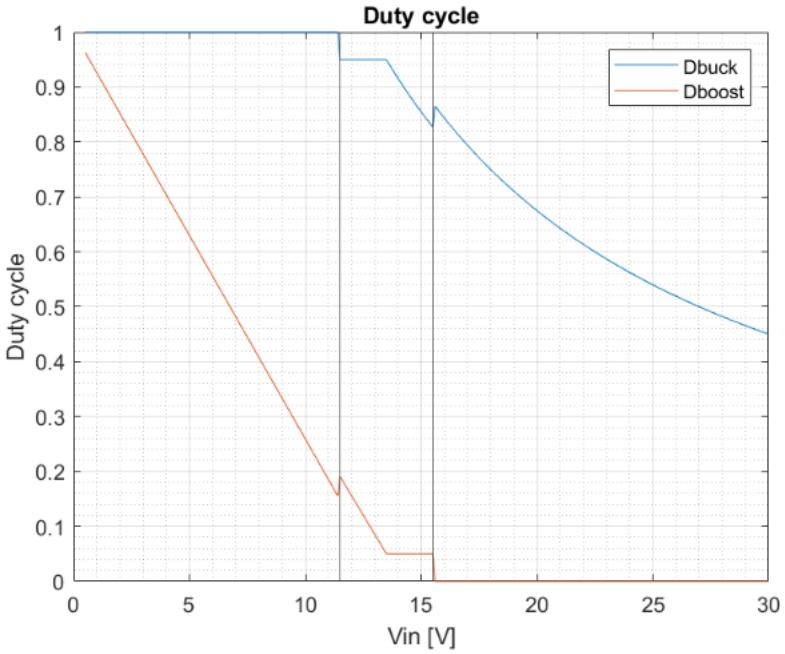


Figure 2.8: Duty cycles

Non-Inverting Buck-Boost Design

It was determined that the NIBB is the best converter choice for our application and its general working principle was explained. In this chapter we will see all the steps needed to design a full NIBB converter, this includes the following parts:

- Power stage
  - Power components
  - Efficiency estimation
  - Drivers
- Measure stage
  - Current measure
  - Voltage measure
- Control
  - Microcontroller
  - Communication circuits
  - Fault detection
- Supplies

In this chapter we will refer to the converter's input voltage as V_{mp}, as this is the output voltage of the TEG in the maximum power condition.

3.1 Power Stage

This section will present how the power components are chosen, followed by an estimation of the efficiency and finally a discussion on the driver's circuit and its component selection.

3.1.1 Power Components

To properly choose the power components some Matlab scripts were written to perform all the calculations and display the graphs.

Inductor and Switching Frequency

To properly choose the inductor we have to calculate:

- Inductance
- Average and RMS current
- Maximum inductor current

The minimum allowable inductance is calculated based on which current mode we want to have in our converter (DCM or CCM), we chose CCM. Since the converter will work both like a boost and a buck, we have to choose an inductor which will guarantee that we stay in CCM in both modes. For the buck we need:

$$L > \frac{R_o(1 - D_{buck})}{2f_{sw}} \tag{3.1}$$

And for the boost we need:

$$L > \frac{R_o(1 - D_{boost})^2 D_{boost}}{2f_{sw}} \tag{3.2}$$

Where $R_o = \frac{V_{out}}{I_{out}}$ is the load resistance and it changes in every working condition.

Running the Matlab script the figure 3.1 is created.

We can see that if the switching frequency is low, then the minimum inductance is high. This is a problem since we don't have commercial inductors with high inductance and high saturation current. Given that in our application the inductor current will be pretty high we have to use a switching frequency high enough that allows us to find a commercial inductor that has

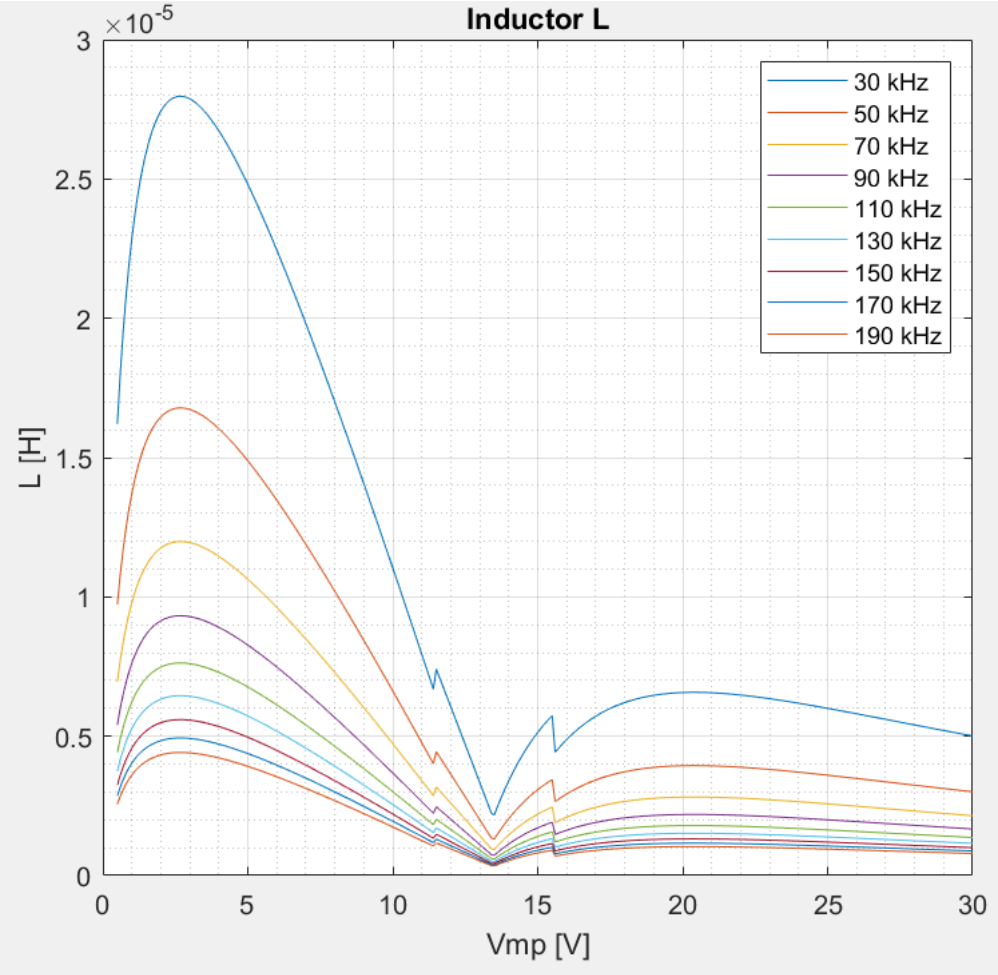


Figure 3.1: Minimum inductance to stay in CCM for all the frequencies

a high enough saturation current. A good compromise between switching frequency and minimum inductance is $f_{sw} = 150kHz$. The curve for this switching frequency is shown in figure 3.2. The maximum of the curve is $5.6\mu H$, so we choose an inductance of $L = 10\mu H$.

The average inductor current is needed to properly select the inductor and the RMS current is needed to calculate the losses. Given that we will use the converter in CCM, the average current is approximately equal to the RMS current since the ripple is relatively small. To calculate the average current we need a different expression for each working mode.

$$I_{LbuckRMS} \approx I_{Lbuckave} = I_{out} \tag{3.3}$$

$$I_{LboostRMS} \approx I_{Lboostave} = I_{in} \tag{3.4}$$

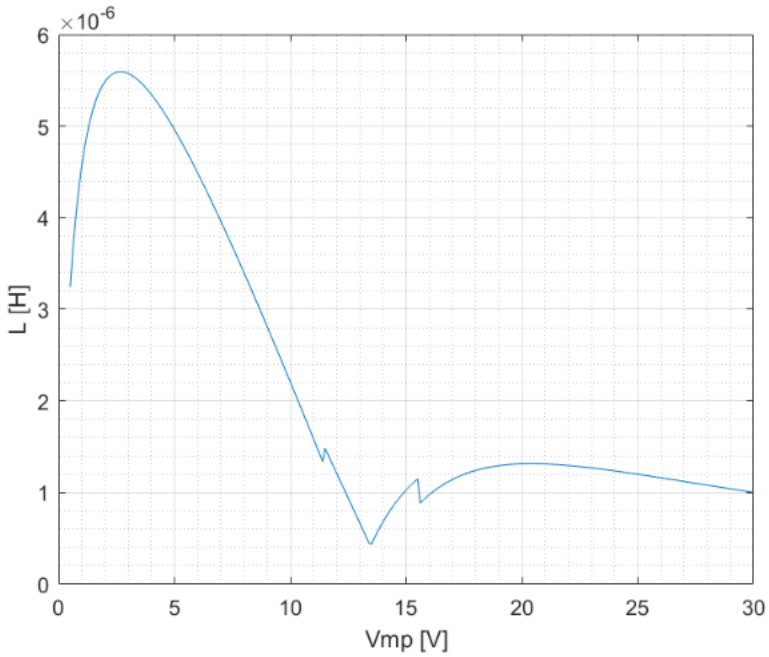


Figure 3.2: Minimum inductance to stay in CCM

$$I_{Lbuck(B-B)RMS} \approx I_{Lbuck(B-B)ave} = \frac{I_{out}}{1 - D_{boostmin}} \tag{3.5}$$

$$I_{Lboost(B-B)RMS} \approx I_{Lboost(B-B)ave} = \frac{I_{in}}{D_{buckmax}} \tag{3.6}$$

Combining the four equations we find the graph in figure 3.3.

The maximum inductor current is needed to properly select the inductor and avoid saturation and it's also the maximum current going through the transistors. Its the sum of the average current and half the ripple current.

$$I_{Lbuckmax} = I_{Lbuckave} + \frac{\Delta I_{buck}}{2} \tag{3.7}$$

$$I_{Lboostmax} = I_{Lboostave} + \frac{\Delta I_{boost}}{2} \tag{3.8}$$

$$I_{Lbuck(B-B)max} = I_{Lbuck(B-B)ave} + \frac{\Delta I_{buck(B-B)}}{2} \tag{3.9}$$

$$I_{Lboost(B-B)max} = I_{Lboost(B-B)ave} + \frac{\Delta I_{boost(B-B)}}{2} \tag{3.10}$$

Where:

$$\Delta I_{buck} = \frac{(V_{mp} - V_{out}) D_{buck}}{f_{sw} L} \tag{3.11}$$

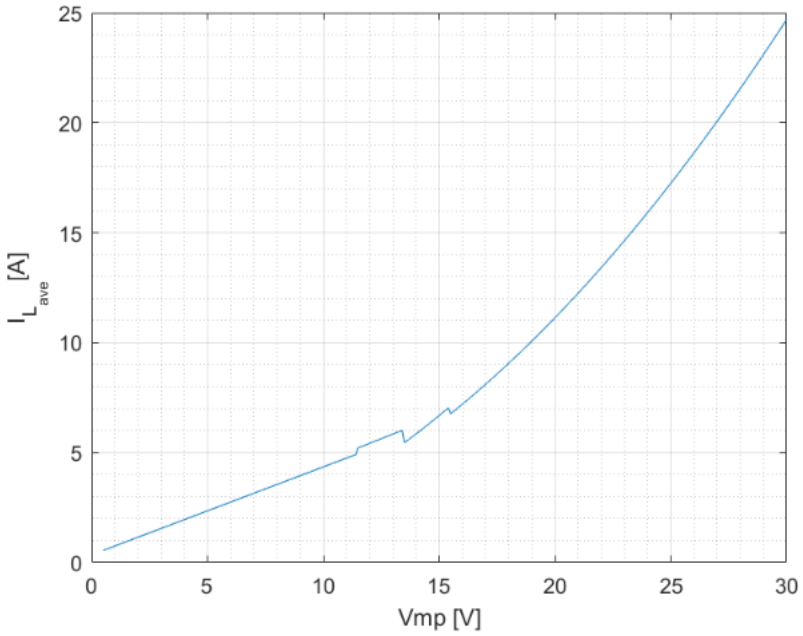


Figure 3.3: Average inductor current

$$\Delta I_{boost} = \frac{V_{mp} D_{boost}}{f_{sw} L} \tag{3.12}$$

$$\Delta I_{buck(B-B)} = \frac{V_{out}(V_{mp} - V_{out}(1 - D_{boostmin}))}{f_{sw} L V_{mp}} \tag{3.13}$$

$$\Delta I_{boost(B-B)} = \frac{V_{in}(V_{out} - V_{mp} D_{buckmax}))}{f_{sw} L V_{out}} \tag{3.14}$$

Combining the four equations we find the graph on figure 3.4.

Considering all the calculated parameters a good inductor choice is the MPX1D2213L100 from Kemet.

Input Capacitor

To choose the input capacitor we have to specify the working voltage, which is in this case the open circuit output voltage of the generator (60V). Furthermore we have to specify the maximum RMS current that goes through the capacitor. We expect this current to have its maximum during the buck mode.

$$I_{CinRMS} = \begin{cases} I_{out}\sqrt{\frac{V_{out}}{V_{mp}}(1 - \frac{V_{out}}{V_{mp}})} & \text{buck mode} \\ \frac{\Delta I_{boost}}{\sqrt{12}} = \frac{V_{mp} D_{boost}}{f_{sw} L \sqrt{12}} & \text{boost mode} \end{cases} \tag{3.15}$$

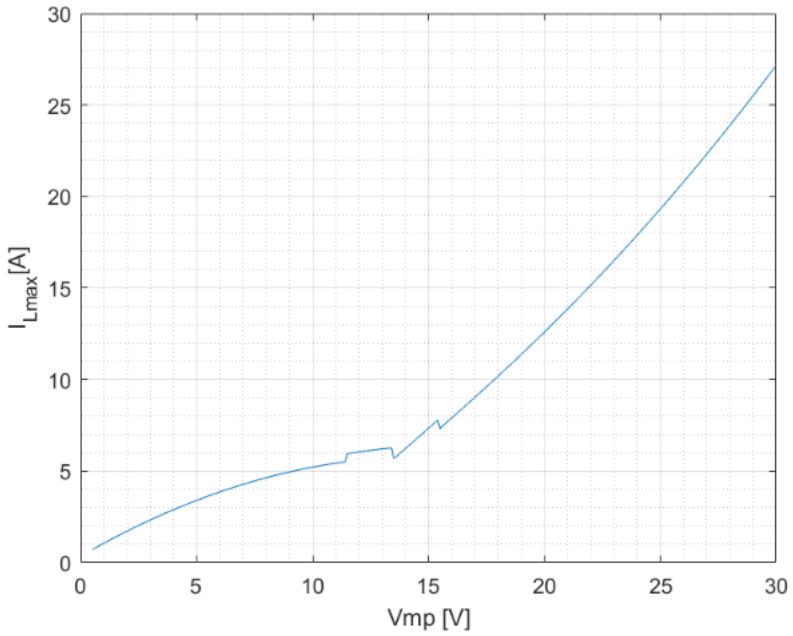


Figure 3.4: Maximum inductor current

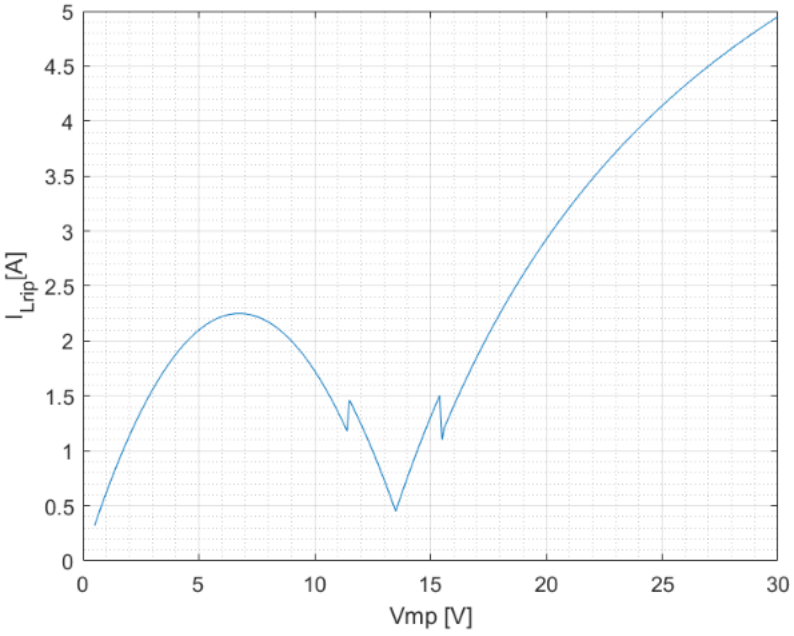


Figure 3.5: Inductor peak to peak current ripple

Since in the buck-boost region we don't know the exact capacitor RMS

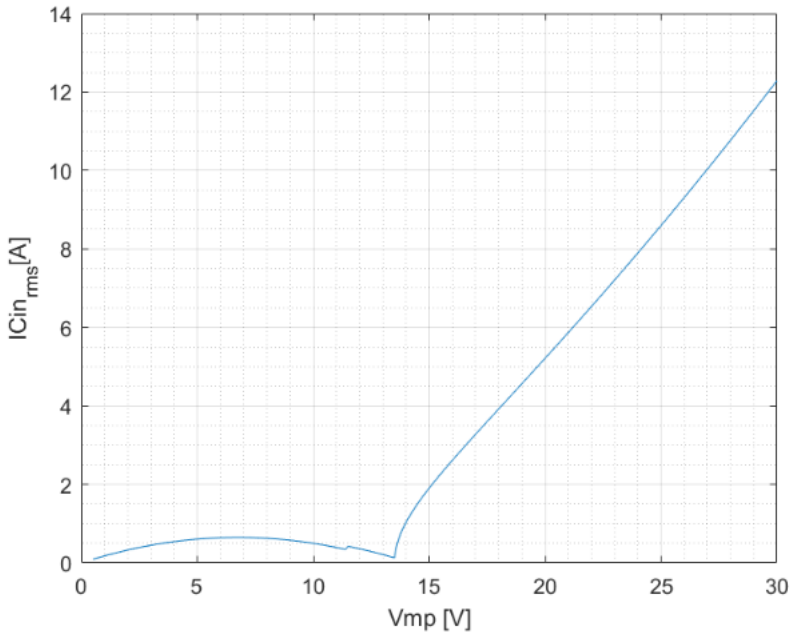


Figure 3.6: Input capacitor RMS current

current we can estimate it. We will use the same formula as the buck mode when we have $V_{out} + p > V_{mp} > V_{out}$ because in this region the boost duty cycle is very low. We will use the same formula as the boost mode when we have $V_{out} - p < V_{mp} < V_{out}$ because in this region the buck duty cycle is very high.

Since 12A of current is quite high we have to have many capacitors in parallel to distribute the current. We choose to use ceramic capacitors since they are much smaller compared to electrolytic capacitors and have smaller ESR. One 1210 ceramic capacitor can bear between 1A and 2A of current, so we will place 10 ceramic capacitor in parallel. Furthermore a $390\mu F$ electrolytic capacitor is added to increase the capacitance since ceramic capacitors have small capacitance ($4.7\mu F$ each). A series + parallel configuration shown in figure 3.7 is used for the capacitors for safety reasons, to avoid a short circuit of the input if one of the capacitors brakes; unfortunately this quadruples the number of capacitors. Two resistors are added to discharge the capacitors if the input is disconnected. The resistors are used also to ensure that the voltage drop on each of the two series capacitors is equal.

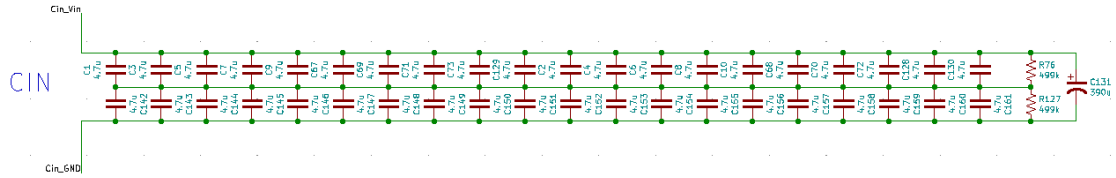


Figure 3.7: Input capacitors

Output Capacitor

To design the output capacitor we have to specify the working voltage, which is in this case the output voltage $V_{out} = 13.5V$. Furthermore we have to specify the maximum RMS current that goes through the capacitor. We expect this current to have its maximum during the boost mode. We have extended the formulas for buck and boost mode also for the buck-boost mode, as it was explained for the input capacitor.

$$I_{CoutRMS} = \begin{cases} I_{out}\sqrt{\frac{V_{out}}{V_{mp}} - 1} & \text{boost mode} \\ \frac{\Delta I_{buck}}{\sqrt{12}} = \frac{(V_{mp} - V_{out})D_{buck}}{f_{sw}L\sqrt{12}} & \text{buck mode} \end{cases} \tag{3.16}$$

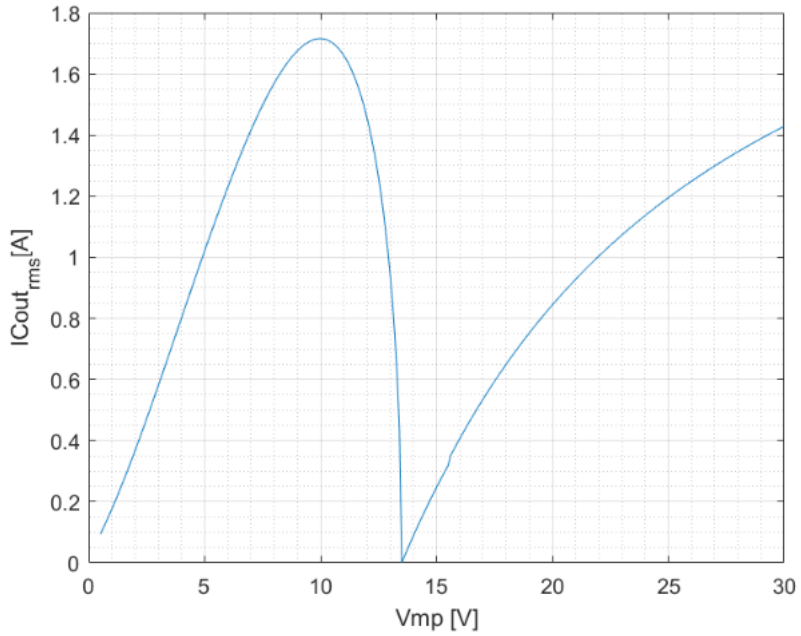


Figure 3.8: Output capacitors RMS current

Although the $I_{CoutRMS}$ is much smaller than the I_{CinRMS}, as can be seen in figure 3.8, it was decided to put the same number of capacitors also for C_{out}, mainly due to three reasons:

1. Symmetry between input and output
2. Having more capacitors in parallel reduces the total ESR improving efficiency
3. A bigger output capacitance reduces the output voltage ripple

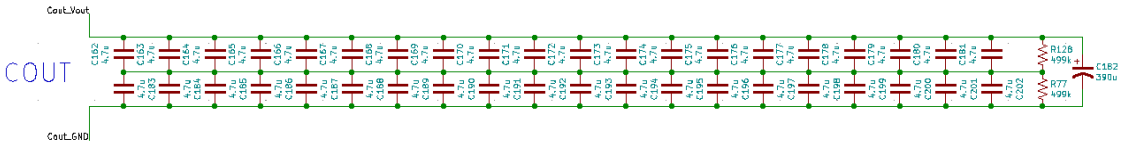


Figure 3.9: Output capacitors

Transistor Choice

To choose the transistors there are some criteria to respect:

1. To be available on the market
2. To have a D-PAK package
3. To be a MOSFET
4. To be rated for $V_{ds} > 60V$ and $I_d > 50A$

A list of possible candidates is:

- FDB035N10A
- TK160F10N1L
- IPB180N08S4-02
- PSMN3R8-100BS

To choose the best MOSFET between the candidates an efficiency analysis were performed, choosing at the end the transistor which had the smaller losses. To perform such analysis a Matlab script was written. Te calculated losses were the following:

MOSFET	Ron [mΩ]	Coss [pF]	Ciss [pF]	Qg [nC]
FDB035N10A	3	3100	5500	90
IPB180N08S4-02	2.2	6000	10000	128
TK160F10N1L	2.5	2500	10000	122
PSMN3R8-100BS	3.5	1000	10000	170

Table 3.1: MOSFETs' parameter comparison

- **Conduction losses** - appear when the transistor is ON and are caused by the R_{on} resistance of the MOSFET.

$$P_{cond} = I_d^2 R_{on} \tag{3.17}$$

  Where I_d is the drain current.

- **Switching losses** - appear every time a transistor changes its state from ON to OFF and vice versa.

$$P_{sw} = \frac{V_{ds} I_d}{2}(t_r + t_f) f_{sw} \tag{3.18}$$

  Where V_{ds} is the drain to source voltage, t_r and t_f are the rise time and fall time of the MOSFET and were calculated as suggested by [7] and [2].

- **Gate drive losses** - are the losses that accounts for the energy required to charge and discharge the gate capacitance.

$$P_{gatedrive} = Q_g V_{driver} f_{sw} \tag{3.19}$$

  Where Q_g is the total gate charge, V_{drive} is the voltage that drives the MOSFET's gate.

- **Output capacitance losses** - are losses due to the output capacitance C_{oss} charge and discharge.

$$P_{Coss} = \frac{1}{2} C_{oss} V_{ds}^2 f_{sw} \tag{3.20}$$

- **Dead time losses** - occur during the dead time. The dead time is the time during which both transistors in one leg (high and low side)

are OFF to prevent shoot through current. During the dead time both transistors are OFF, but the body diode of the low side transistor will conduct and dissipate power.

$$P_{dt} = V_d I(t_{swon} + t_{swoff}) \tag{3.21}$$

Where V_d is the body diode forward voltage, $t_{swon} + t_{swoff}$ is the total minimum dead time, which is the time to switch OFF plus the time to switch ON the MOSFET.

- **Reverse recovery losses** - losses due to the MOSFETs' body diode reverse recovery.

$$P_{rr} = Q_{rr} f_{sw} V_{ds} \tag{3.22}$$

Where Q_{rr} is the reverse recovery charge of the body diode.

Of course not all the losses are present at all times, for example in buck mode, the conduction losses of Q4 are equal to zero since this transistor is always OFF. The following considerations are made by taking into account which losses does every transisor have at any given input voltage. Running the Matlab script it turns out that the best choice is the FDB035N10A from ON-semiconductors. In figure 3.10 we can see all the losses relative to this transistor. The graph accounts for the different operating modes and also for the fact that we have four transistors. In figure 3.11 we can see the combined losses for each of the four transistors.

Shunt Resistor

The shunt resistor will be introduced in this part because it introduces some non-negligible losses, even if its not strictly functional to the power part, but more to the measure part. The shunt resistor is used to measure the currents inside the converter and it works by transforming the current into a voltage that is then sensed by the measuring circuit. This information is then used for the control. Three shunt resistors were placed in order to measure the input, the output and the inductor currents.

For the input and output currents a 0.001Ω resistor was chosen. For the inductor current a 0.01Ω resistor was chosen. Why the inductor current shunt is bigger will be explained later in the Measure section of this chapter. For the shunt selection care must be taken because we have to make sure that the selected shunt can dissipate the power coming from the high currents.

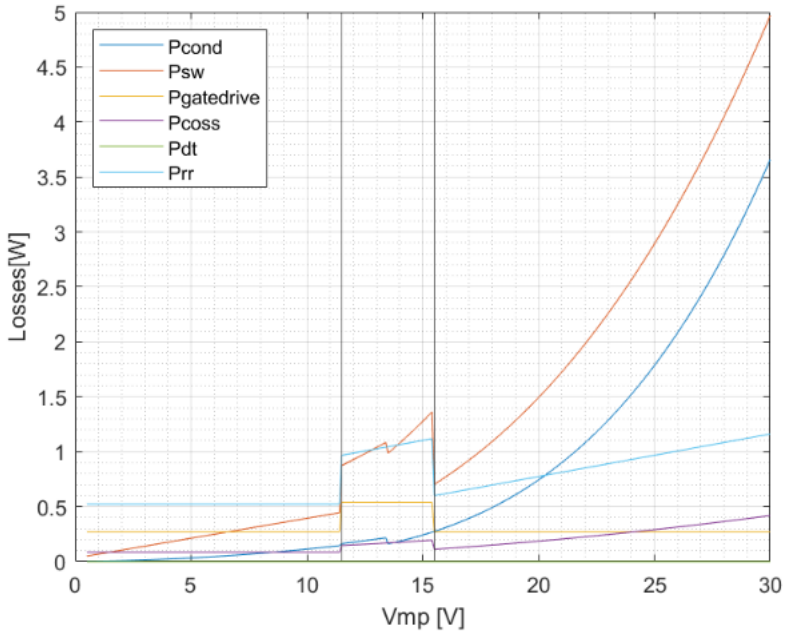


Figure 3.10: MOSFET losses

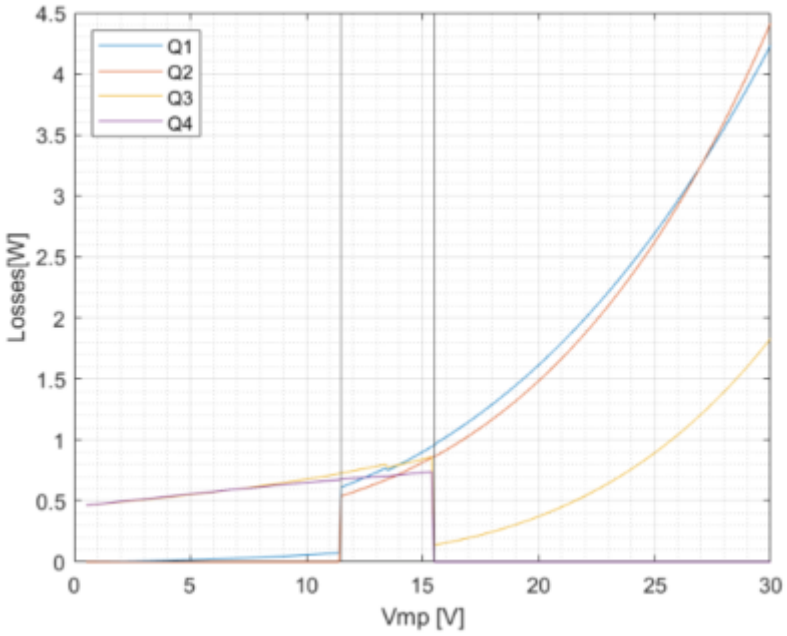


Figure 3.11: Losses for each MOSFET, where Q1, Q2, Q3, Q4 are the one in figure 2.5

Other Components

In figure 3.12 the full power stage circuit schematic is shown. There are some components that have not been discussed yet:

- **Low side shunt** - there are two 0Ω shunt resistors, that can be replaced with 0.001Ω resistors if we want to take low side measures.
- **Exposed pads** - there are 5 pairs of exposed pads, a wire will be placed in between them to connect them, allowing a current probe to be placed to measure various currents in the circuit.
- **Snubber** - two snubber circuits were predisposed so that if we see that there are strong oscillations during testing we can dampen them by placing a resistor and a capacitor.
- **Voltage divider** - there are two voltage dividers, one on the input side and one on the output side. They are used to take the voltage measures.

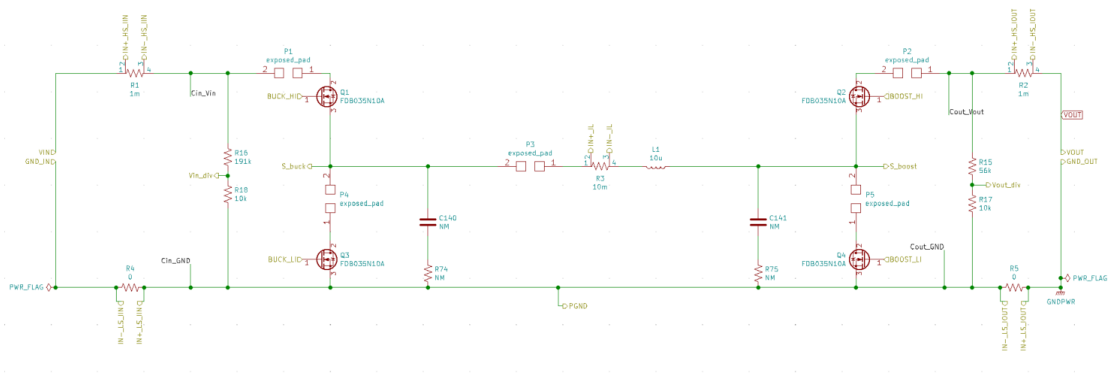


Figure 3.12: Power stage schematic

Name	Value	MPN	Manufacturer
MOSFET	/	FDB035N10A	ON Semiconductor / Fairchild
Shunt resistor	1mΩ and 10mΩ	HCS2512FT1L00 and WSHM2818R0100FEA	Stackpole Electronics Inc and Vishay Dale
Input/output capacitors	437μF	GRM32ER71K475KE14L and UBY1K391MHL1TO	Murata Electronics and Nichicon
Inductor	10μH	MPX1D2213L100	Kemet

Table 3.2: Power components summary

3.1.2 Efficiency Estimation

Once the components have been chosen, we can proceed with an efficiency estimation. The transistor losses had already been discussed, let's see now the other causes of losses:

- **Inductor losses** - the main inductor losses are the conduction losses

$$P_L = I_{LRMS}^2 ESR_L \tag{3.23}$$

- **Capacitor losses** - the main capacitor losses are the conduction losses

$$P_C = I_{CRMS}^2 ESR_C \tag{3.24}$$

  The ESR_C of the selected input and output ceramic capacitors (GRM32ER71K475KE14L) can be estimated as 0.004Ω at $150kHz$

- **Shunt resistor losses** - conduction losses of the shunt resistors

$$P_{shunt} = I^2 R_{shunt} \tag{3.25}$$

A graph with all the main losses is shown in figure 3.13. Once the losses

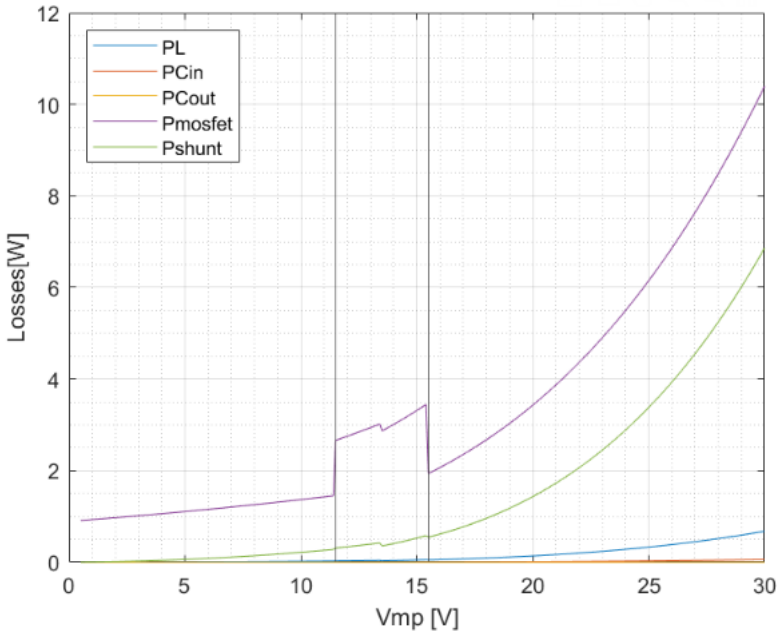


Figure 3.13: Main losses in the NIBB

have been calculated it is easy to estimate the converter's efficiency with the following formula. The result is shown in figure 3.14.

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} \tag{3.26}$$

It is interesting to notice two things:

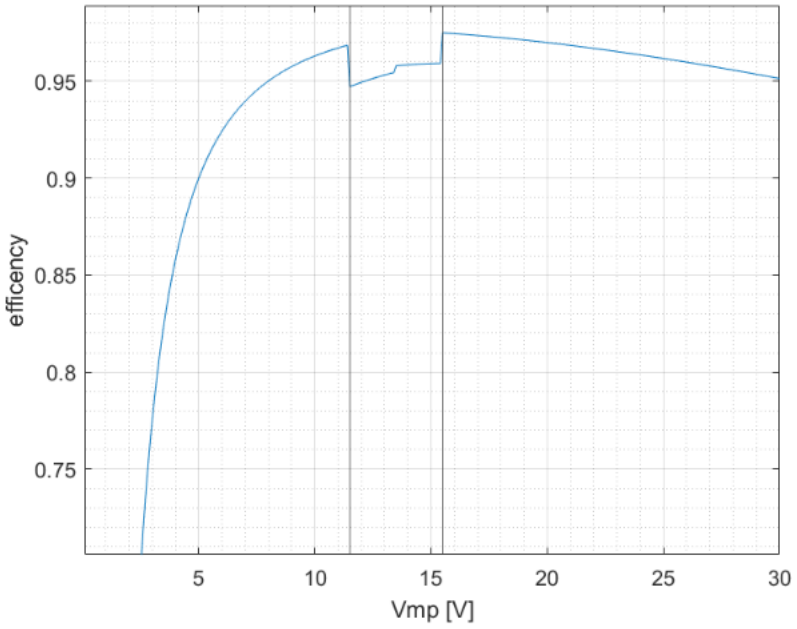


Figure 3.14: Estimated converter's efficiency

1. It's probably a good idea not to use the converter for $V_{mp} < 4V$.
2. The efficiency drops in the buck-boost region due to the fact that all 4 transistors are switching.

3.1.3 Drivers

The drivers are the last remaining component that has to do with the power stage of the converter, as it tells the MOSFETs when to turn ON and OFF. When the NIBB converter is working in buck or boost mode, the driver is required to deliver a 100% duty cycle. This is not a trivial task when the 100% duty cycle is required for the high side MOSFET. In conventional drivers the high side driver is able to drive the high side MOSFET using the bootstrap technique. The problem is that the bootstrap can't be used for

the 100% duty cycle, because the bootstrap capacitor needs to be charged periodically, and this can't happen when the transistors are not switching.

To solve this issue an isolated supply and an isolated driver are required. The isolated supply replaces the bootstrap capacitor because it can provide the constant voltage that is needed to achieve 100% duty cycle. The chosen driver is a half bridge isolated driver, the UCC21320 from Texas Instruments. Since we have four transistors in the NIBB we need two half bridge drivers, one for each leg and three isolated power supplies, one for each high side MOSFET and one for the two low side MOSFETs. The driver circuit of the buck leg is shown in figure 3.15. the Circuit for the boost leg driver is identical.

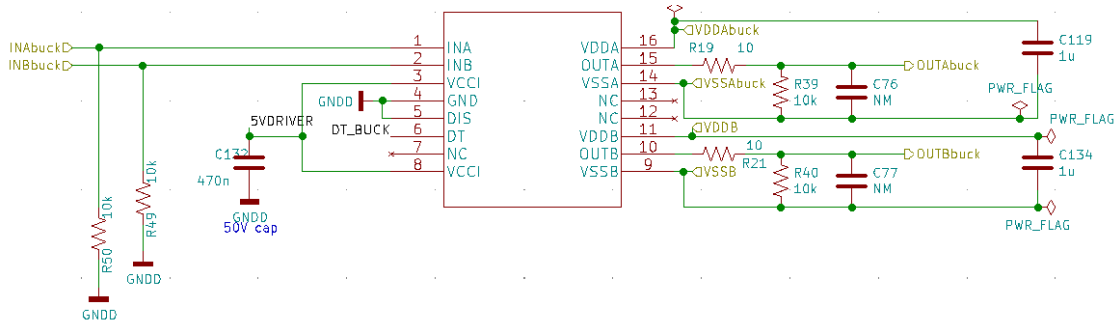


Figure 3.15: Driver circuit

The left part of the circuit in figure 3.15 is the power part, the one connected to the power stage of the NIBB (gates and reference voltages). The resistors R19 and R21 are used to control the current going in the gate. Care must be taken in selecting this two components because the current going through them is not small (usually >1A) and so they have to have an adequate power rating. On the left side of the figure we have the control part of the circuit, we can see the two inputs that come from the microcontroller, INA and INB.

An interesting feature of this driver is that we can set a hardware dead time. This is done by placing a resistor between the DT pin on the driver (pin number 6) and ground. The value of the resistance determines the length of the dead time. This feature can be particularly helpful because it lowers the work that the microcontroller has to do, freeing some computational power. In figure 3.16 the small circuit that permits to enable or disable this feature is shown (if the DT pin is connected to the 5V the feature is disabled). The microcontroller decides if enable it or not through the command Dead_Time_Buck. If Dead_Time_Buck is high then the NMOS

turns ON, connecting the gate of the PMOS to GNDD, turning it ON.This will connect the 5V to the DT pin on the driver, disabling the hardware dead time function. If Dead_Time_Buck is low, the opposite happens and the hardware dead time of approximately $200ns$ will be enabled.

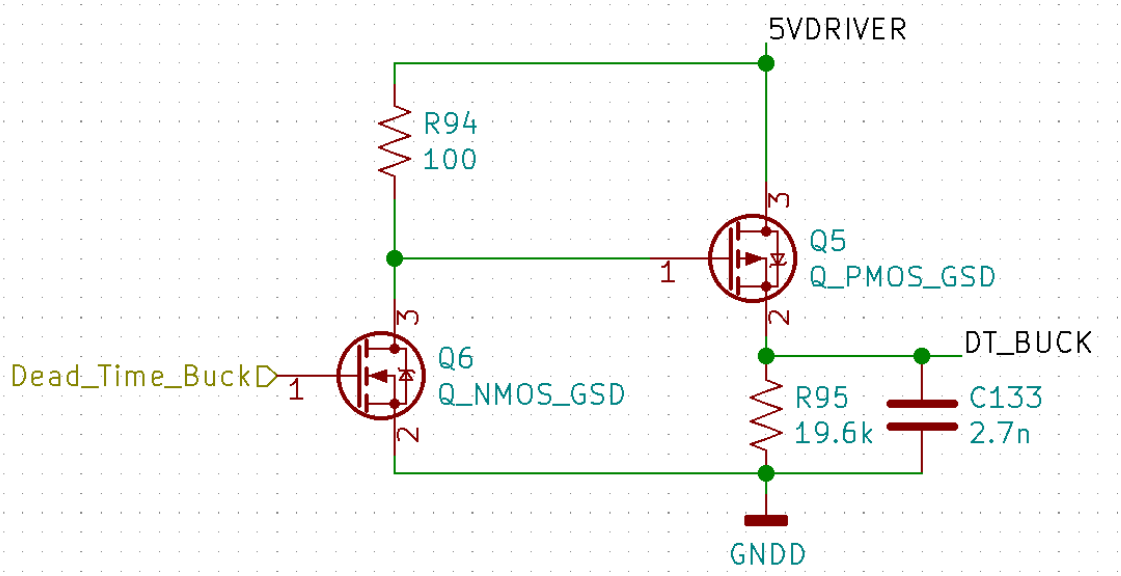


Figure 3.16: Dead time enabling circuit

3.2 Measure Stage

This section will present how the measure stage of the NIBB was designed. The measure stage is probably the most delicate part of the whole NIBB, because even a few millivolts can make the difference between a usable measure and an unusable measure. Particular care must be taken in both the theoretical design and PCB design.

The measures are fed to the microcontroller and are used to control the NIBB. In total five measures are taken:

1. Input current
2. Output current
3. Input voltage
4. Output voltage

5. Inductor current

The inductor current is the only one that is not strictly necessary because in the chosen control strategy it will be estimated given the other four parameters, but it can still be very useful so we will measure it anyway.

3.2.1 Current Measure

Input and output currents

The full current measuring circuit (a part from the shunt) is shown in figure 3.17. To measure the currents a shunt resistor is used for each measure. The shunt resistor transforms the current into a voltage that is then sensed by a sensor. Given that the shunt resistors are high side, the sensor is chosen so that it can tolerate e big common voltage. For the input and output currents the sensor is the INA240 form Texas Instruments. The sensor has a gain that amplifies the small voltage drop on the shunt resistor. The output of the sensor is then attenuated by a voltage divider from a full scale of 5V to a full scale of 3V, which is the admissible input voltage of the microcontroller's analog inputs. After the voltage divider there is a filter that filters the measure, removing the noise.

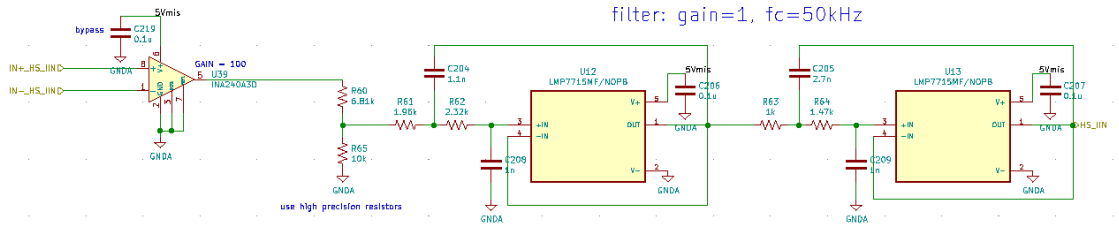


Figure 3.17: Input and output current measuring circuit

The main goal of the filter is to filter out the switching noise of the converter, which is at $150kHz$. A fourth order Bessel filter with cutting frequency around $50kHz$ was chosen. A Sallen-Key configuration was used as it gives the best performance when the gain is 1. Higher filer order was avoided due to space limitations on the PCB. A critical parameter to take into considerations during the filter design is the phase lag. The phase lag has to be very small, because if it is too big the measure becomes useless for the control.

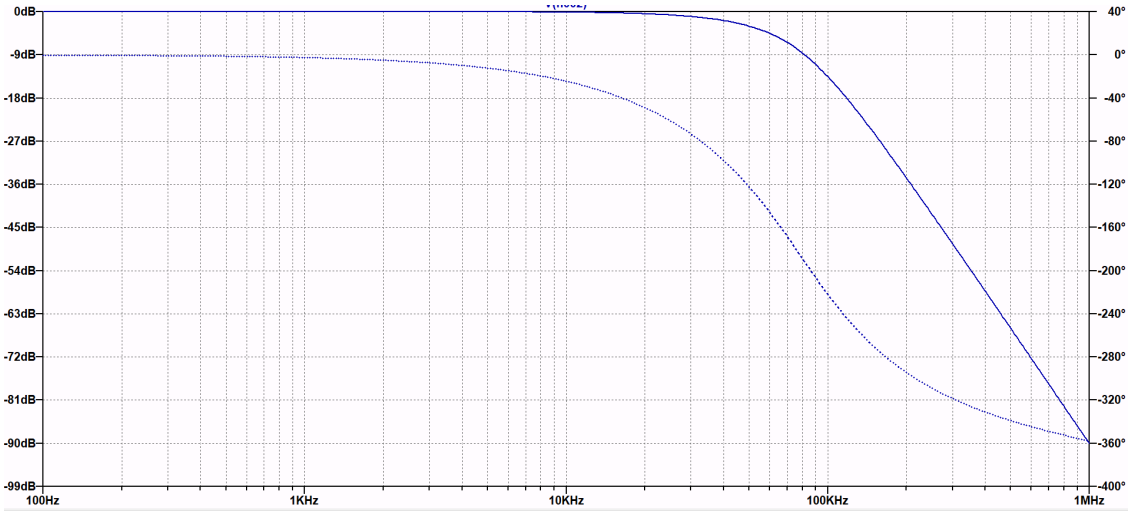


Figure 3.18: Second order filter bode diagram; phase in dotted line, magnitude in straight line

Inductor current

A very similar approach to the one seen for input and output currents was used. The measuring circuit is shown in figure 3.19 and is composed by a shunt resistor, an RC filter, a sensor, a voltage divider and an active filter.

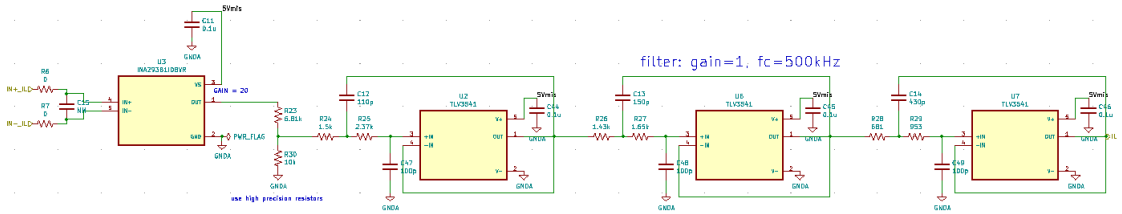


Figure 3.19: Input and output current measuring circuit

There are three differences with respect to the circuit for input and output currents: the shunt resistor, the sensor and the filter. The shunt resistor for the inductor current is 10 times bigger, 0.01Ω. The reason for this is the parasitic inductance of the shunt. Given that the inductor current is a big AC current, even a small parasitic inductance can cause big problems. To illustrate the problem let's look at the figure 3.21. We have a 0.001Ω shunt resistor with a $3nH$ parasitic inductance. From the figure 3.21b we can see that the waveform of the voltage across the shunt (green) resistor is nowhere near the inductor current waveform (red). This is a huge problem since the

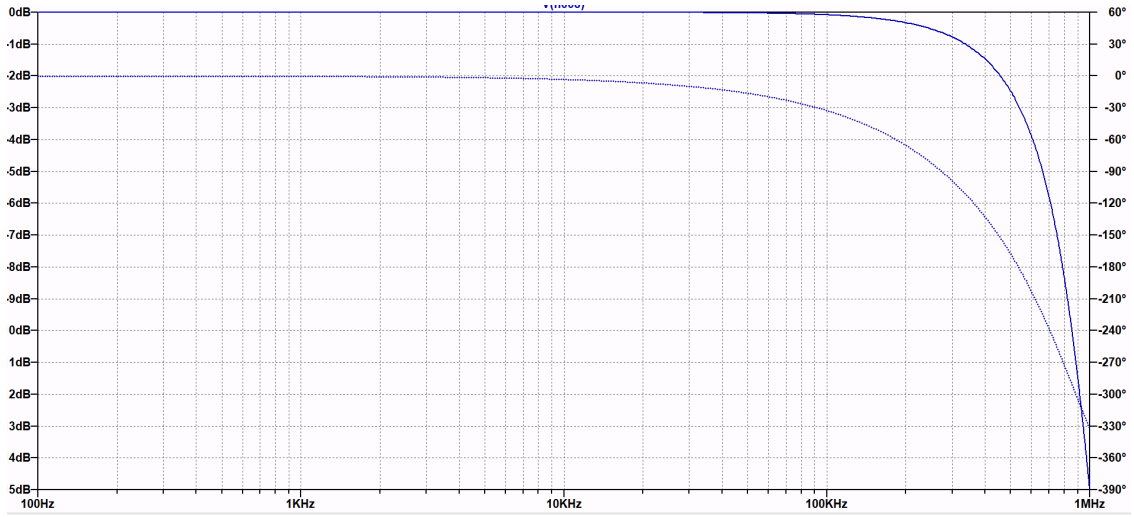
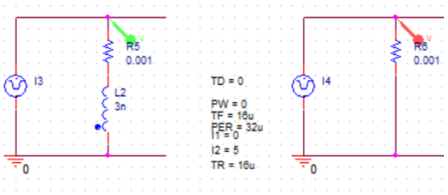
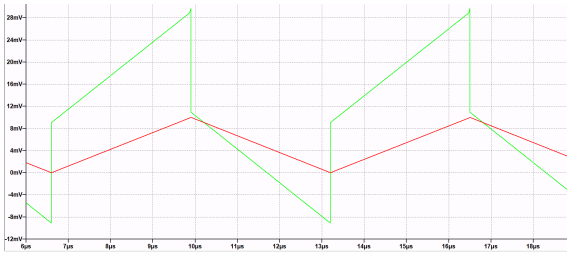


Figure 3.20: Third order filter for I_L measure bode diagram; phase in dotted line, magnitude in straight line

sensor will pick up the distorted waveform.



(a) Simulation circuit for the inductor current



(b) Simulated shunt resistor voltage

Figure 3.21: Inductor current simulation

There are two solutions to this problem, which were both adopted in the final NIBB design:

1. Use a bigger value for the shunt resistor in order to minimize the parasitic inductance effect.

2. Use an RC filter that will compensate the zero introduced by the RL circuit, restoring the original waveform.

The drawback of increasing the shunt resistance is that the dissipated power will be increased.

The sensor is a different sensor with respect to the input and output current measuring circuit. The sensor is different because the INA240 bandwidth is too small, so it was replaced with the INA293.

The filter for the inductor current measure is a sixth order Bessel filter with a cutting frequency of $500kHz$. The importance of a small phase lag still applies.

3.2.2 Voltage Measure

The voltage measuring circuit is shown in figure 3.22. The circuit is composed by a voltage divider that brigs the voltage down from V_{in} and V_{out} to 3V, which is the admissible input voltage for the microcontroller analog inputs and a filer, which is the same of the input and output current measuring circuits and the same considerations apply.

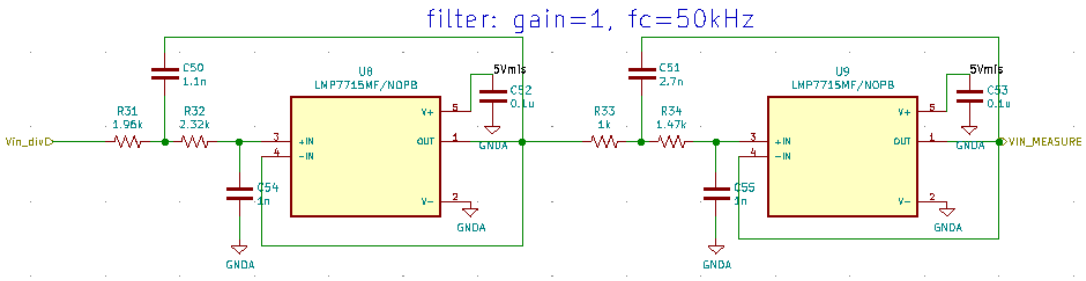


Figure 3.22: Input and output voltage measuring circuit

3.3 Control

This section will present all the circuits that are connected to the microcontroller, that are: the microcontroller circuit itself, all the communication circuit that are used by the board to communicate with the external world and the fault detection circuit that is used to detect an overcurrent or an undervoltage situation.

3.3.1 Microcontroller Circuit

The employed microcontroller is the TMS320F28379DPTP from Texas Instruments. We will see all of its parts one by one in the following subsections.

Supply

The microcontroller needs two power supplies: 1.2V and 3.3V. All the power supply pins are shown in figure 3.23. As we can see, each pin has to have a bypass capacitor, the capacitance is the one suggested by the microcontroller's datasheet.

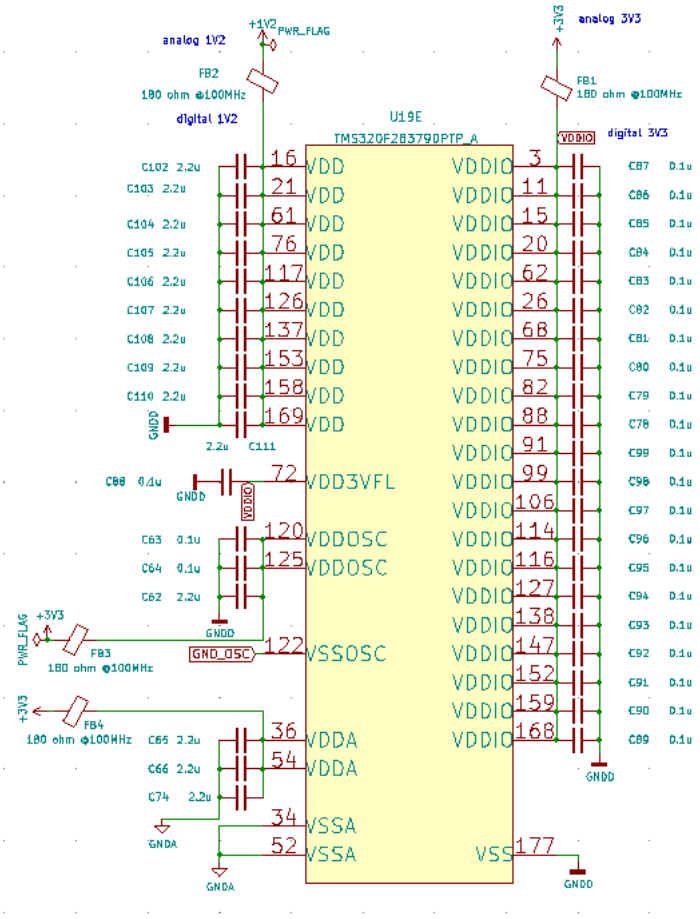


Figure 3.23: Microcontroller's supply circuit

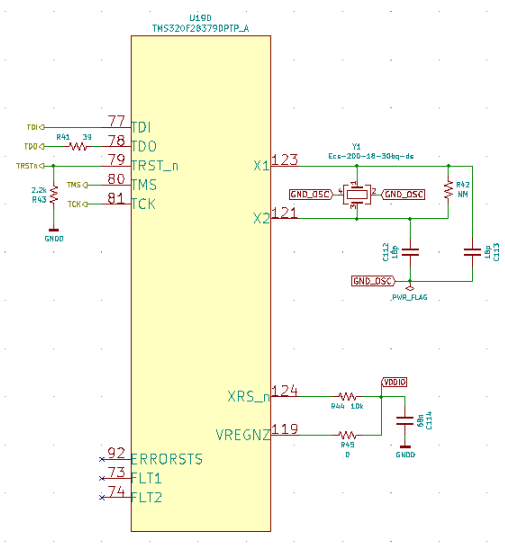
We can see that there are three different grounds: analog ground GNDA, digital ground GNDD and crystal oscillator ground GND_OSC. This is because we want to protect the analog and crystal circuits from the noisy digital circuit. This is possible by having different ground planes on the PCB that are then connected between them in a single point. This ensures that the noisy digital return currents travels only on the GNDD and do not affect the other grounds.

To improve the quality of the power supply we introduce ferrite beads

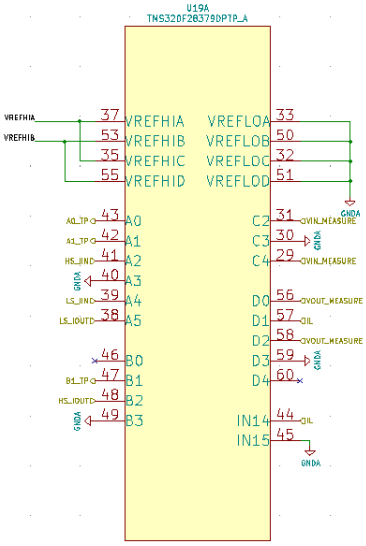
(FB1, FB2, etc.) in series with the power supply, forming a π filter with the capacitors. A ferrite bead is a "special inductor" that is very good at blocking high frequency noises. Relative to general inductors, ferrite beads have a high resistance component and low Q value, allowing to eliminate high frequency noise by transforming it into heat.

Analog Section

In figure 3.24a we see the JTAG and crystal oscillator circuits which are done following the datasheet recommendations. The JTAG is an industry standard that allows the programming and debugging of the microcontroller and uses a 14 pin connector. The crystal oscillator is needed to set the clock of the microcontroller.



(a) Microcontroller's JTAG and crystal oscillator circuit



(b) Microcontroller's analog input circuit

Figure 3.24: Microcontroller's analog circuits

In figure 3.24b we see all the connections to the microcontroller's ADCs and DACs. Here we have all the measures of current and voltage that we have discussed before, connected to the ADCs. The pins are selected based on the sampling order of the ADCs. We have four ADCs (A, B, C, D), each of them have several input channels (A0, A1, A2, ...). The channels with the same number are sampled in the same time instant, for example channels A2, B2, C2 and D2 are sampled in the same instant. To have all the main

measures ($I_{in}, I_{out}, V_{in}, V_{put}$) taken at the same instant we put them on the same number (A2, B2, C2 and D2).

In order for the analog part of the microcontroller to work properly we have to provide a 3V reference signal. This is done by the circuit in figure 3.25, we have a precise regulator that transforms the 5V into 3V, followed by two voltage followers. The reference voltage is connected to the microcontroller through the pins 37, 53, 35 and 55.

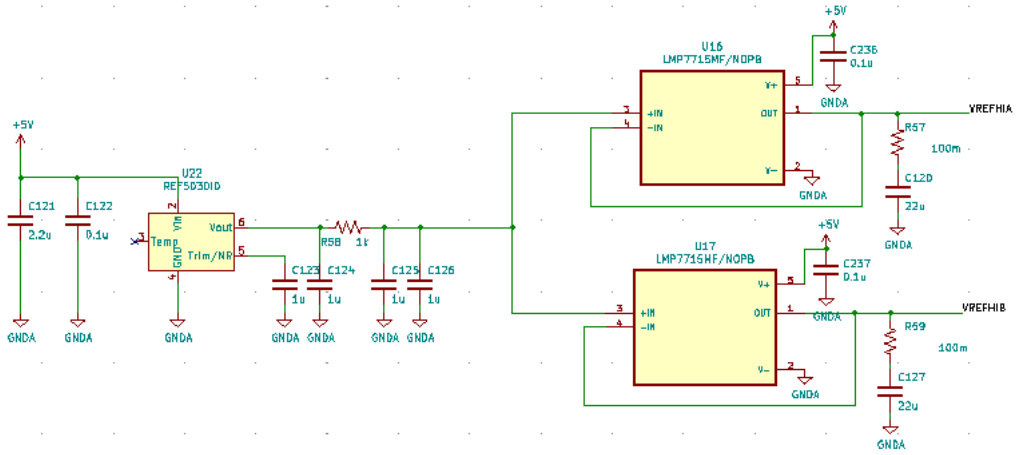


Figure 3.25: Reference voltage signal circuit

The fault detection circuit shown in figure 3.26 is used to detect an input current overcurrent, an input voltage undervoltage and an output voltage undervoltage. It is very useful in order to stop the NIBB in case of a fault preventing to damage the NIBB or any external components. On the left side of the circuit there is a 3V reference. In the middle there are 3 comparators, one for each fault, which compare the 3V reference with the measured quantity. On the right side all the comparators' output converge into an OR gate which's output is then connected to a microcontroller's GPIO.

Digital Section

The digital section of the microcontroller is shown in figure 3.27. The GPIO pins are internally connected in groups of 32

- Group A: GPIO0-GPIO31
- Group B: GPIO32-GPIO63
- Group C: GPIO64-GPIO95

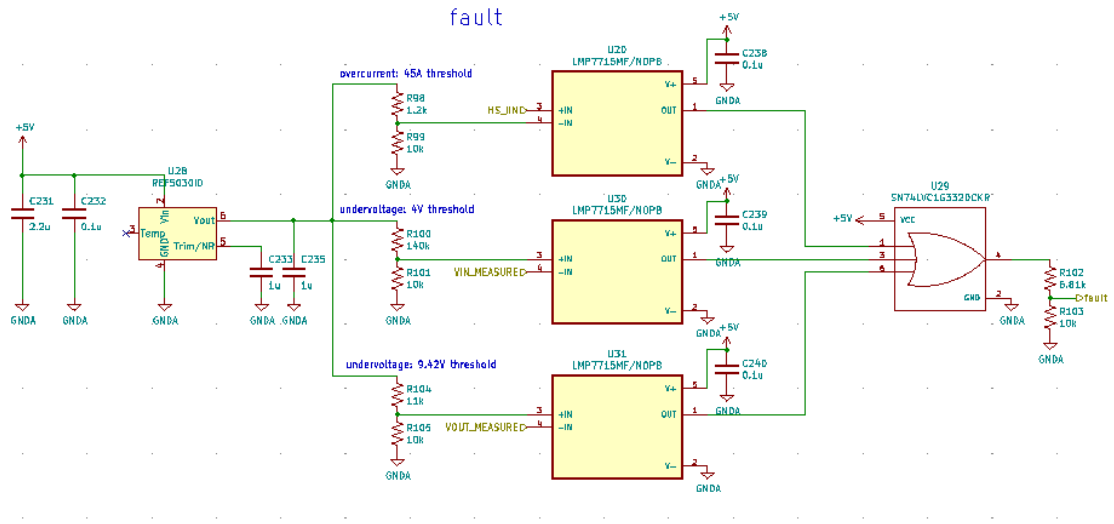


Figure 3.26: Fault detection circuit

- Group D: GPIO96-GPIO127
- Group E: GPIO128-GPIO159
- Group F: GPI160-GPIO168

Each group is assigned to one of the two CPUs. We chose to assign group A and B to the CPU1 and group C to the CPU2.

The most important GPIOs are the following:

- GPIO0-GPIO3: are special GPIOs that are able to provide PWM signals for the drivers that will drive the MOSFETs.
- GPIO30-GPIO31: are used for the CAN.
- GPIO43-GPIO44: are used to select if the dead time will be hardware or software.
- GPIO72, GPIO84: are used for the startup procedure.

3.3.2 External Connections

In this section we will take a look to all the circuits used to communicate with the board and all the connectors used to interact with the board.

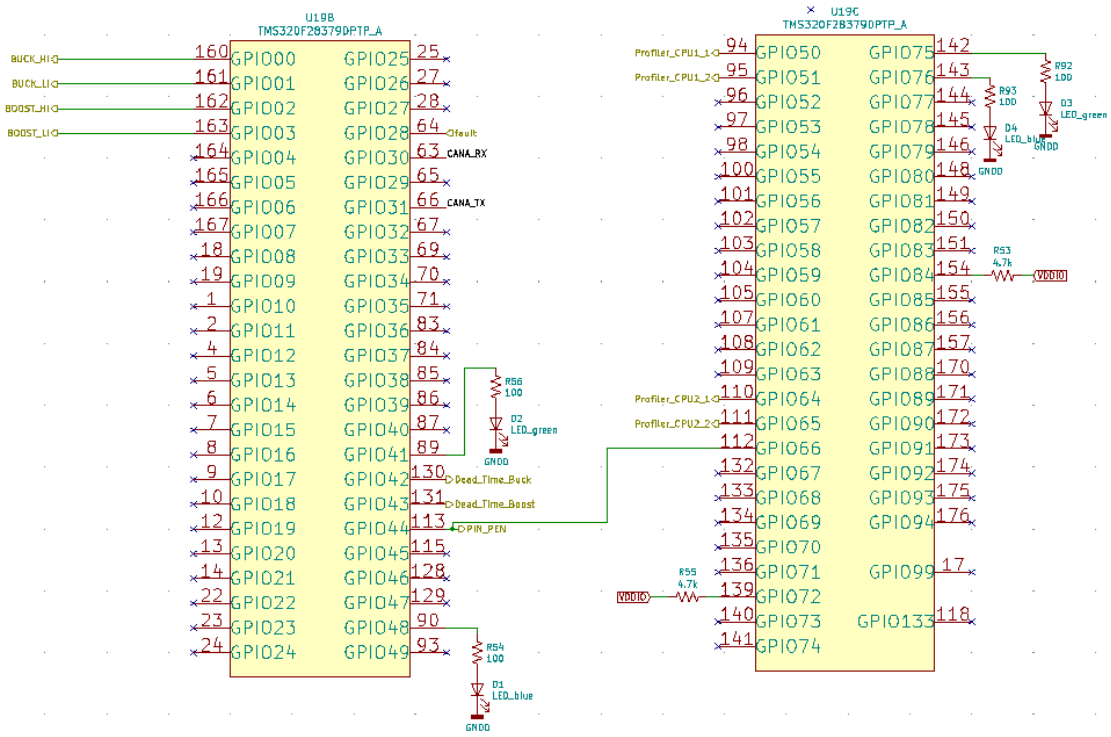


Figure 3.27: Microcontroller's digital section

CAN

The Controller Area Network (CAN) is a serial communication protocol used in automotive applications. It is designed to work also in very noisy and difficult environments. To use it we have to have an external module, figure 3.28, connected to the microcontroller. All the components are chosen following the datasheet suggestions. The R46 resistor is especially important since it provides the impedance matching.

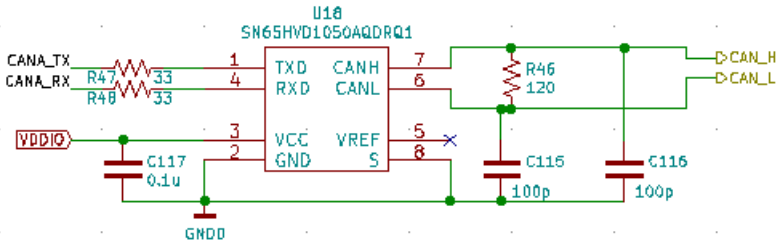


Figure 3.28: CAN transceiver module circuit

The CANH and CANL pins are then connected to a DB9 connector, figure 3.29, that is used to communicate with the external world.

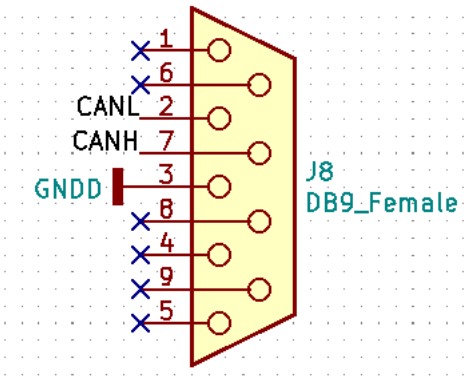


Figure 3.29: CAN DB9 connector

JTAG

The JTAG is an industry standard that allows the programming and debugging of the microcontroller and uses a 14 pin connector, the connections to the connector are shown in figure 3.30.

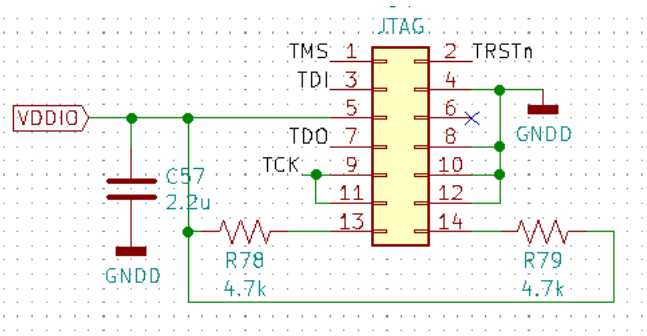


Figure 3.30: JTAG 14 pin connector

Test Points

Test points (figure 3.31) are placed on the PCB to allow an easy measure with the oscilloscope probe. Test points for the for the following quantities are placed on the PCB:

- Profiler1 CPU1

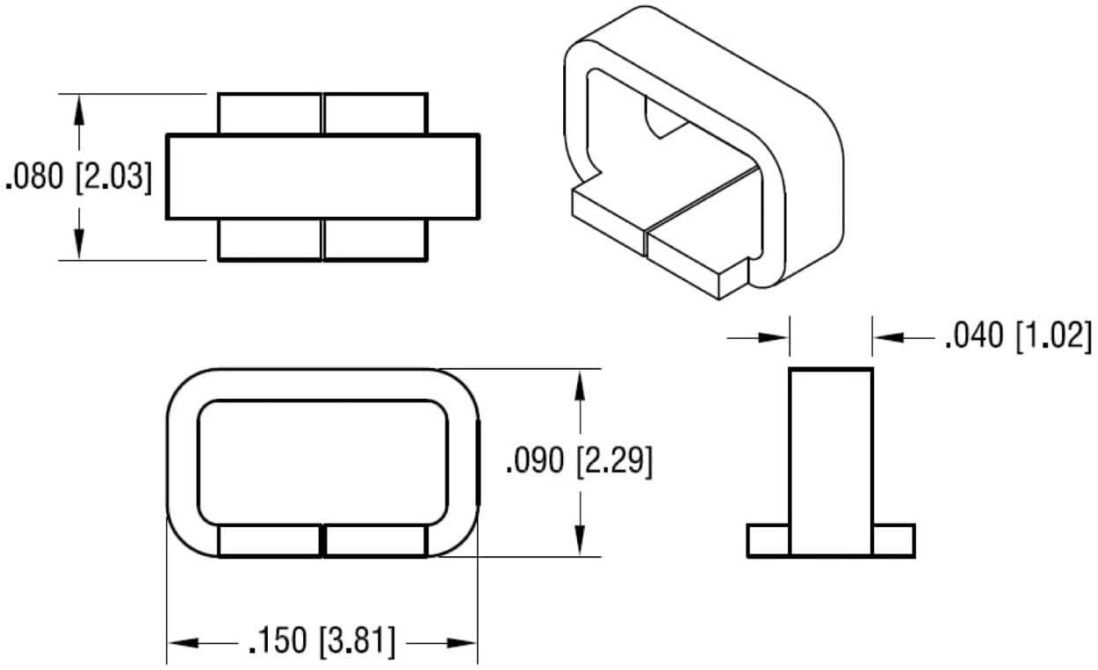


Figure 3.31: Test point

- Profiler2 CPU1
- Profiler1 CPU2
- Profiler2 CPU2
- ADC A0
- ADC A1
- ADC B1
- High side I_{out}
- High side I_{in}
- Low side I_{out}
- Low side I_{in}
- Inductor current
- Input voltage

- Output voltage

3.4 Supplies

There are many different power supplies needed to properly run a NIBB converter, every active component needs to be properly supplied, this includes: the operational amplifiers, the sensors, the microcontroller, the drivers, the CAN module and so on.

On the NIBB board there are six power supplies in total:

- 5V: for all the analog circuitry.
- 3.3V: for the microcontroller.
- 1.2V: for the microcontroller.
- three isolated 12V: for gate driving.

As we will see in the chapter on the PCB design, all the supplies are on a separate board. This is mainly because power supplies modules are very difficult to find on the market in this moment due to a limited stock availability. So it has been decided to design the power supplies in the last days in order to be sure that all the components were actually present on the market and so the best choice was to design them on a separate board that will then be connected to the main NIBB board. Furthermore in this way the supply board can also be used in different projects since it contains some universally used voltages.

5V, 3.3V and 1.2V

These three power supplies were realized using the modules of the LMZM23601 family from Texas Instruments. The design is pretty simple as it requires just few capacitors to use as C_{in} and C_{out} and couple of resistors for the feedback path. In figure 3.32 the 1.2V power supply circuit is shown, the ones for 3.3V and 5V are very similar. The main difference is that the input voltage for the 5V and 3.3V supplies is the NIBB output voltage (13.5V), meanwhile the input voltage for the 1.2V supply is 5V. This is because due to duty cycle limitations, the LMZM23601 accepts up to 14V input voltage when the output voltage is 1.2V.

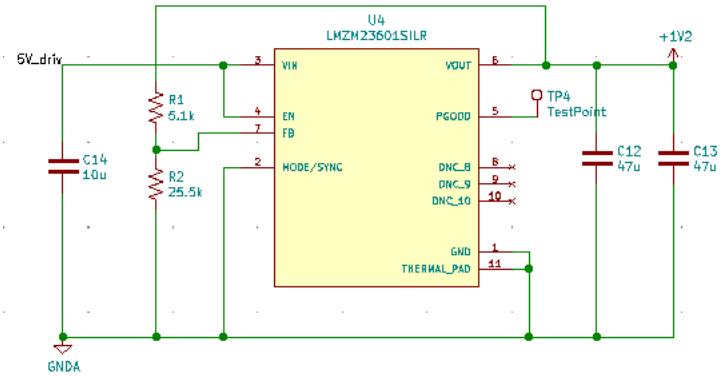


Figure 3.32: 1.2V power supply circuit

Because the power supplies should be very precise, especially for the measuring circuits, an additional filter (figure 3.33) was added to the input voltage of the 5V and 3.3V power supplies. This filter is also used to decouple the power ground from the analog ground.

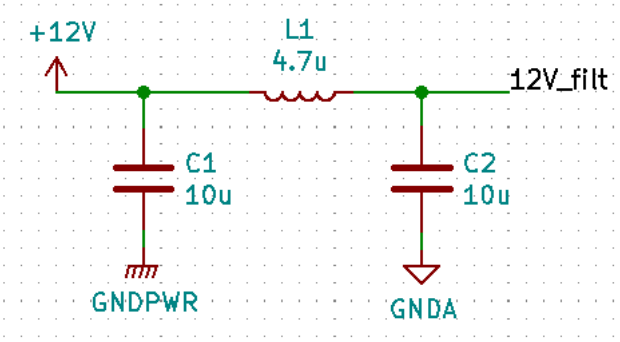


Figure 3.33: 12V filter

12V Isolated Power Supplies

There are three 12V isolated power supplies used as gate to source voltage by the drivers to drive the MOSFETs. We need three different 12V isolated power supplies because we have three different source voltages. The two low side MOSFETs share the same source voltage, meanwhile high side MOSFETs don't and their source voltage are the two switching point voltages.

For the design of the isolated power supplies the SPBW03F-12 module was used. This module takes as input a voltage between 9V and 36V and

outputs 12V. The circuit is shown in figure 3.34. The capacitor on the input pins is used as a bypass capacitor.

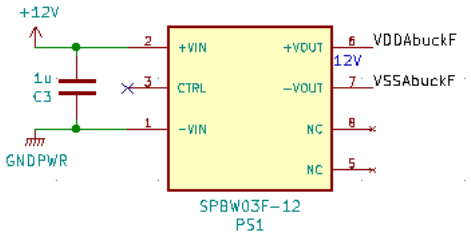


Figure 3.34: 12V isolated power supply circuit

PCB Design

Once the theoretical design and the schematic have been completed, it is time for the PCB design. A good PCB design can be the difference between a perfectly working board and a non working one. During this thesis three PCB were developed:

1. Measure board.
2. NIBB board.
3. Supplies board.

There are several general rules useful to develop any PCB, those rules were used in the design of all three of the boards.

- Any current loop should be minimized to minimize electromagnetic interference (EMI), especially the high current loops.
- Place decoupling and bypass capacitors near the pins of the interested integrated circuit (IC).
- Use ground and power planes, these are crucial to reduce noise and interference, help to maintain the same GND or power potential across the whole board, dissipate heat and mechanically strengthen the board.
- Be aware of the minimum trace width, especially for the high current traces. Not doing so can cause overheating or even melted traces.
- Try to avoid vias as much as possible. Vias will increase the trace inductance and break power and ground planes.
- Do not place copper planes (such as ground planes) under inductors.

- If you have a digital and an analog part on your board, it can be useful to use two separate ground planes and connect them in a single point. This topic is still very discussed in the PCB designer community, so the reader should be aware that this is not always the best solution.
- Avoid routing two traces parallel and near to each other for a long distance to avoid crosstalk.
- Do not introduce 90 degree angles while routing traces.

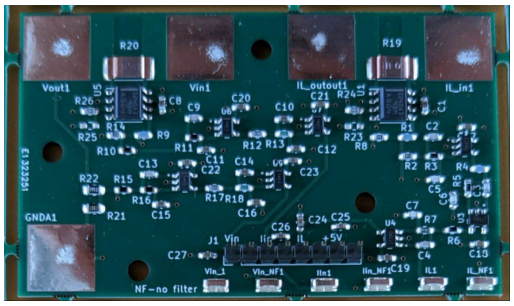
4.1 Measure Board

The measure circuits are the most delicate circuits in the NIBB. For this reason it was decided that it would be a good idea to design a separate board with just the measuring circuits, to test them before proceeding with the design of the main NIBB board. Another reason to design a separate board was to have a measuring board that could be used in other future projects. The circuit present on the board is the same described in the chapter 3.2. This turned out to be a great idea since some critical flaws were found on the measuring board. The flaws were then corrected on the main NIBB board. The measure board is the one in the figure 4.1 and the lessons that we learned were:

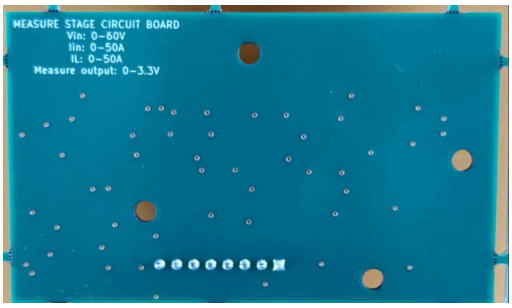
1. The chosen operational amplifier (OPA388) was not good since it is a chopper amplifier.
2. The parasitic inductance in the 0.001Ω resistor is a big problem.
3. The INA240 current sensor has a bandwidth that is too small to measure properly the inductor current.
4. The power supply for the measuring stage has to have very small ripple.

To solve these issues the following things were done:

1. Substitute the OPA388 with a LMP7715 which is a high bandwidth precision operational amplifier.
2. As discussed in the design chapter, use a 0.01Ω shunt resistor and an RC filter for the inductor current measure.
3. Use a higher bandwidth sensor (INA293-1MHz bandwidth).



(a) Measure board PCB, front



(b) Measure board PCB, back

Figure 4.1: Measure board PCB

4. Use a separate 5V power supply just for the analog circuits.

The board presents five exposed pads that are used to connect the board to the circuit that we want to measure. The three pads on the left are used to connect the voltage and the input and output currents (lower bandwidth). The two pads on the right are used to connect the inductor current (higher bandwidth). On the bottom we can see there are pin headers and testing point (the same testing points that we saw in figure 3.31). The test points include all the measures before and after the filter, so we can see what effect does the filer have. In figure 4.2 we have the input/output current measuring circuit schematic and the position of the test points are highlighted.

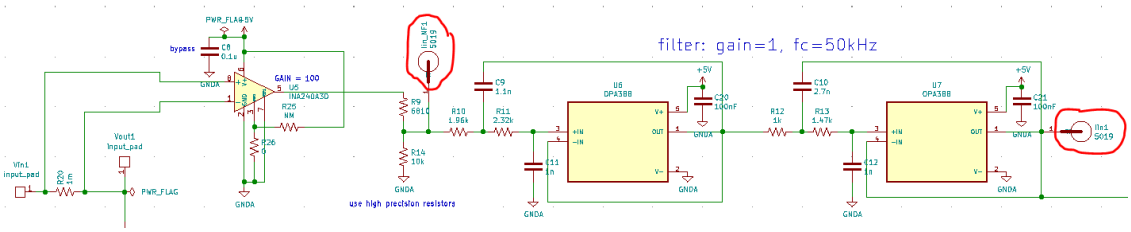


Figure 4.2: Test point location on the measure board

In figure 4.3 we can see the PCB layout design. It is a 4 layer layout. The yellow plane is the GND plane, underneath it we have the 5V power plane. On the top side we have red signal traces and the bottom side is empty so that the board can be placed on a hard surface without worrying about it getting damaged.

The most crucial point in this board design is the shunt resistor to sensor connection. Since every milliohm counts, if the connection is not made properly the measure will be wrong. In the figure 4.4 there is an example of good

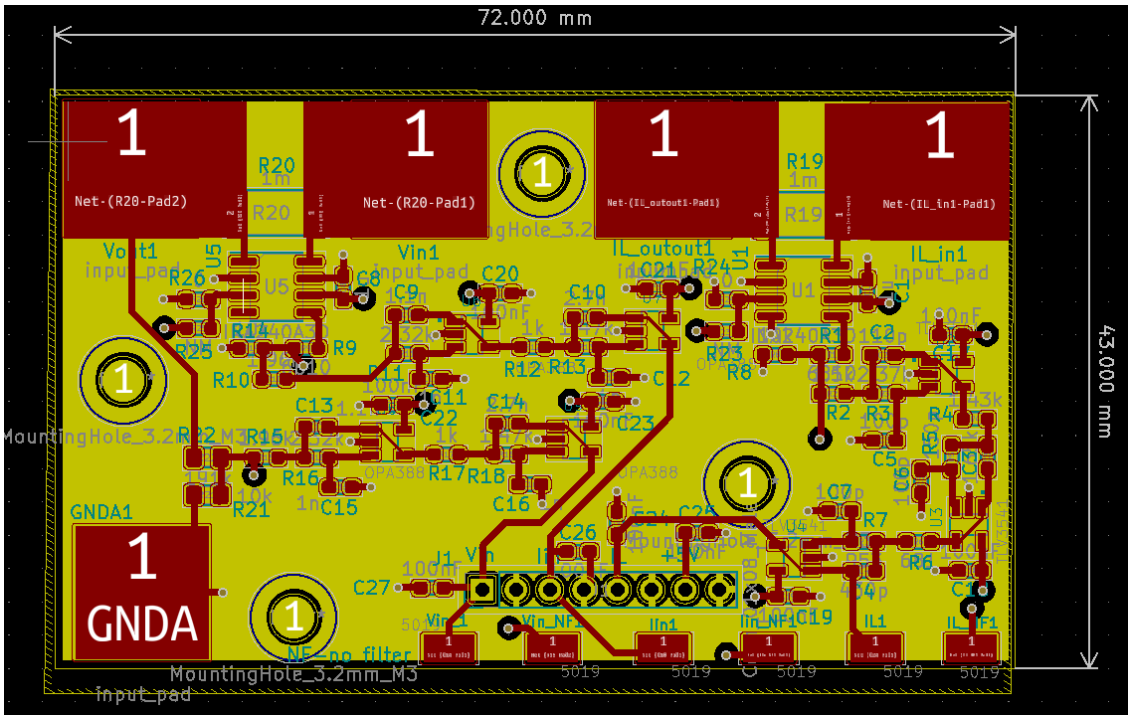


Figure 4.3: Measure board PCB layout

and bad shunt resistor connection. The connection on the right is wrong because the high current passing through the trace will create an additional voltage drop that will be picked up by the sensor.

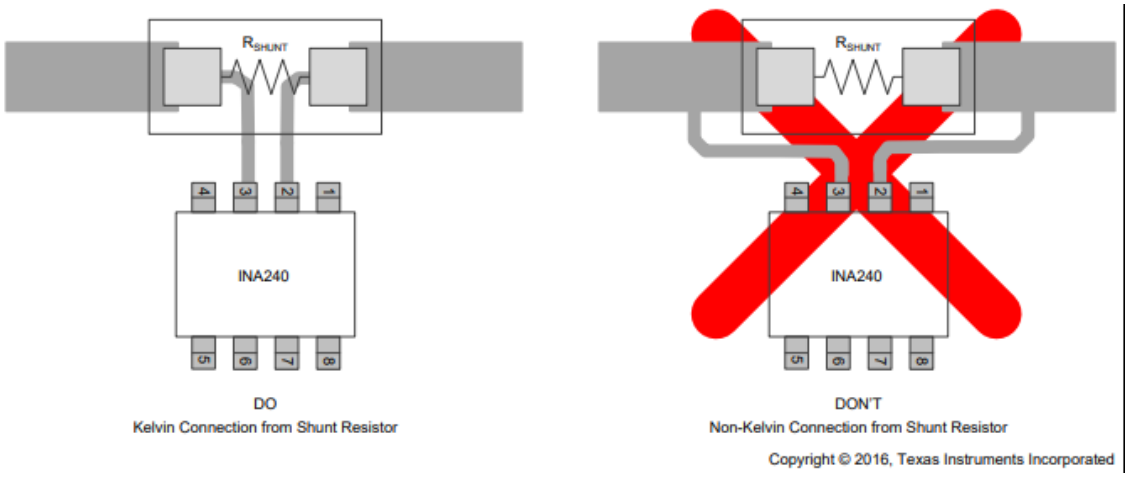


Figure 4.4: Correct shunt resistor connection, image taken from [10]

Another interesting thing to observe is the connection between the exposed

pads and the shunt resistor. We can see that they are very wide. This is because we expect a big current to pass between the exposed pads and through the shunt resistor and we need large traces to bear that current and properly dissipate the generated heat.

4.2 NIBB Board

The NIBB board is the main board of this thesis. The board can be subdivided in 4 areas:

1. Power.
2. Measures.
3. Drivers.
4. Microcontroller.

There is also a fifth component that is crucial for the correct operation of the NIBB, which are the supplies. As said before the supplies will be present on a separate board that will be connected to this board through some connectors.

The areas should be placed on the PCB following some design guidelines:

- The trace from the drivers to the MOSFETs should be as short as possible to minimize the parasitic inductance.
- The trace from the shunt to the sensor should be short to minimize the error.
- We have to have 3 grounds: digital (GNDD), analog (GNDA) and power (GNDPWR) connected between them in a single point.
- Each area has to be placed on top of the respective ground plane.

Given the above restriction, the best layout that was found is the one in figure 4.5. This layout allows to have the driver and the measure circuits near the power stage, furthermore it allows a direct connection between the drivers and the microcontroller and a connection between the measure stage and the microcontroller through the bottom layer of the PCB, shielding these traces from the power traces that are on the top layer with the help of the ground planes that are in the inner layers.

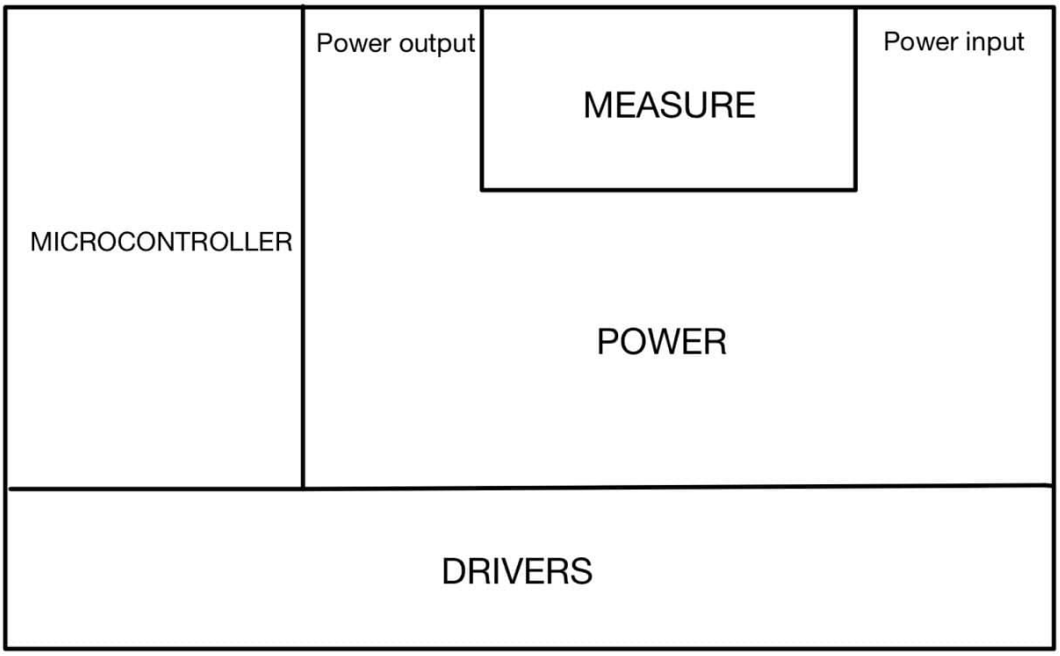


Figure 4.5: PCB general layout

4.2.1 First Layer

On the first layer (top layer) almost all the components are placed and the majority of connections are made. From the figure 4.6 we can see all the areas that we talked above.

The power stage is U-shaped, we can see that is pretty symmetrical. All the traces here are quite wide to be able to bear high currents. We can see that below the MOSFETs there are many vias. These vias are thermal vias and help to remove the heat from the MOSFETs, spreading it to the other layers and to the heatsink that will be connected below the board. We can see the two holes (the two big yellow dots), which are the holes for the heatsink's screws. All the traces that go to a different layer present many vias to improve conductivity. From figure 4.7 we can see an improved shunt resistor connection. This is the best shunt resistor connection (according to [15]), because it optimally decouple the power stage from the measuring stage.

On the left we can see the microcontroller area, where we have the microcontroller itself on the bottom and above it we have the reference voltage

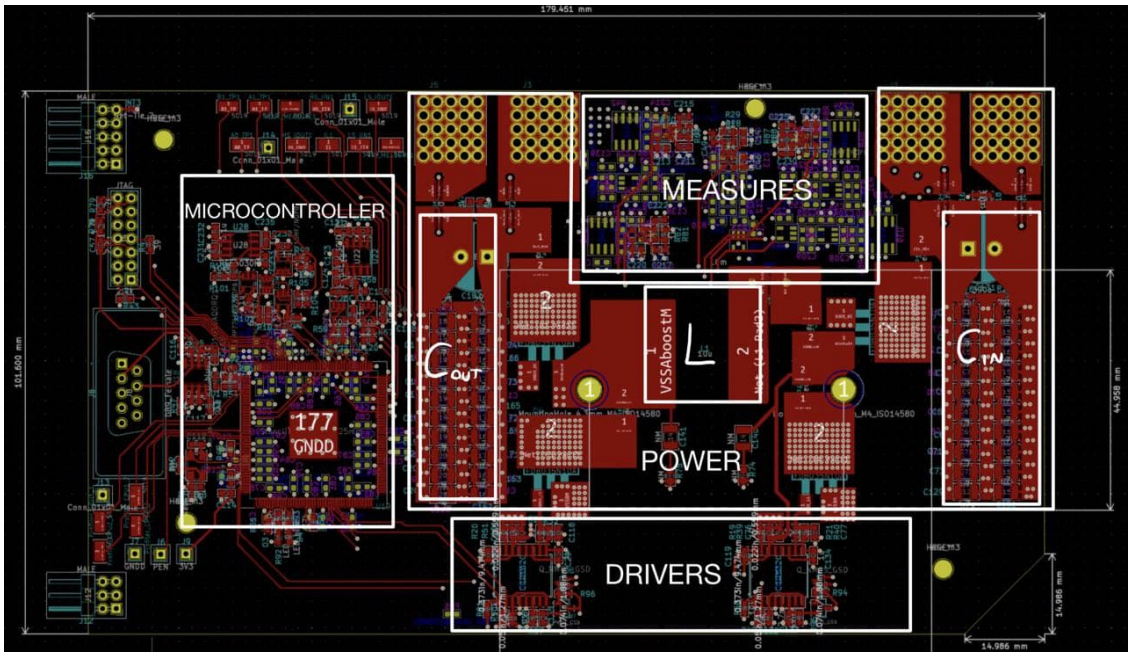


Figure 4.6: Layer 1 of the NIBB PCB

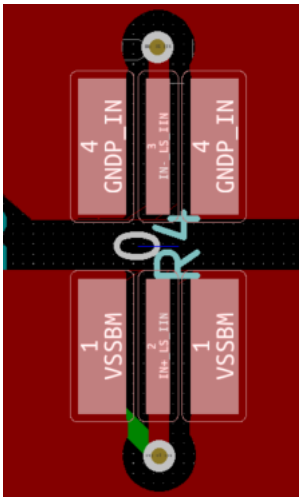


Figure 4.7: Improved shunt resistor connections

circuit and the fault circuit. On the left side of the microcontroller there are the CAN transceiver and the crystal oscillator circuit. All the bypass capacitors for the microcontroller are placed below the microcontroller as this is the most close position. The GPIOs on the microcontroller that we saw in figure 3.27 are selected so that the GPIO pins are physically close to the

thing that they are connected to. This allows to route the traces more easily and allows to have a tidier layout. Some examples of this are:

- The GPIOs that output's the driver signals are on the bottom of the microcontroller, near to the drivers.
- The analog inputs are on the top right, near to the measuring circuits.
- The JTAG pins are on the top left, near the JTAG connector.

On the far left of the board and on the top left we have all the connectors, shown in more detail in figure 4.8. The CONNECTOR 1 and CONNECTOR 2 are the two connectors used to connect the NIBB PCB to the power supply PCB. CONNECTOR 1 has:

- 1.2V
- 3.3V
- 5V
- GNDPWR
- 12V
- GNDA

CONNECTOR 2 has the three isolated voltages needed to produce the V_{gs} to drive the MOSFETs. CONNECTOR 1 and CONNECTOR 2 are pin header connectors with the pins bent at 90 degrees, so we can easily connect the supply board near to the NIBB board.

4.2.2 Second Layer

The second layer, figure 4.9, is an inner layer. Here we have the following ground and power planes:

- 5V for the fault circuit and for the reference volt circuit.
- 5V for the measure circuit.
- 3.3V for the microcontroller.
- 1.2V for the microcontroller.

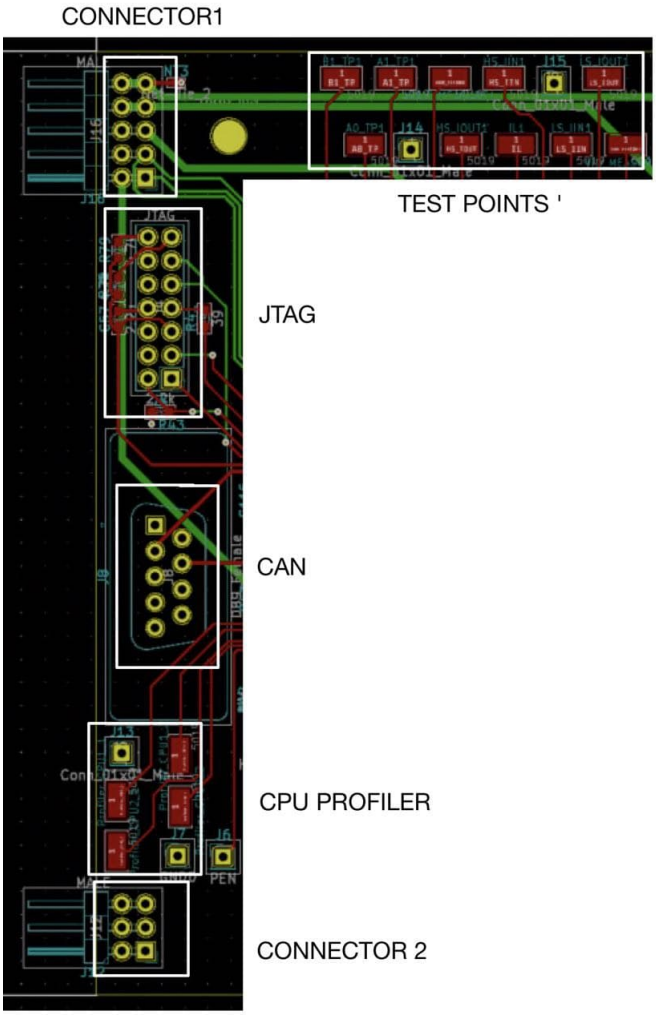


Figure 4.8: Connectors on the NIBB PCB

- GNDPWR

In addition to that, we can see that on the bottom there are the traces that connect the CONNECTOR 2 to the drivers.

The GNDPWR was placed on the second layer to block as much as possible the noise coming from the switching power traces on the top layer. Furthermore, we need a continuous GNDA plane that extends from the microcontroller to the measure circuit. The placement of the GNDPWR plane one the second layer and of the GNDA plane on the third layer (figure 4.11) allows this to happen. Furthermore placing the GNDA plane between the GNDPWR and the signal traces fatherly improves noise immunity. A cross

section of the power stage of the PCB is shown in figure 4.10.

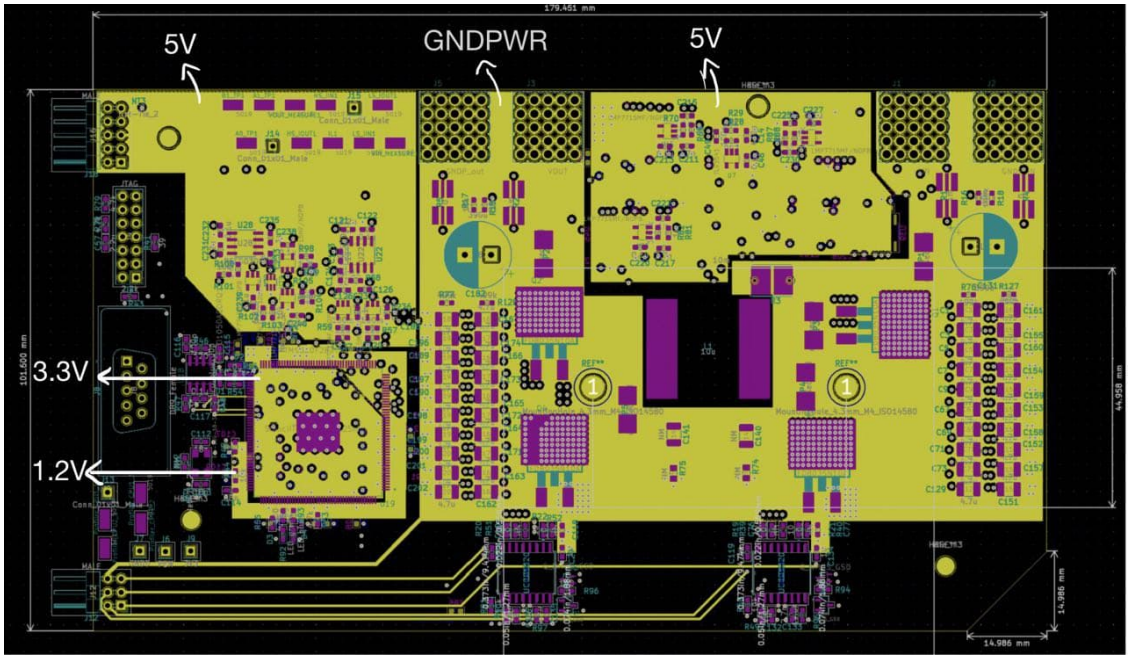


Figure 4.9: Layer 2 of the NIBB PCB

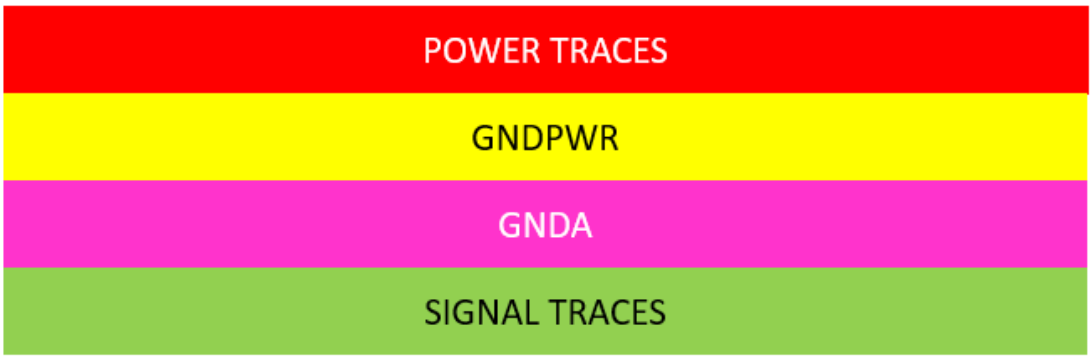


Figure 4.10: PCB cross section under the power stage

Another interesting thing to point out is the spacing of the vias. We can see that for example on the input and output capacitors on the GNDPWR plane or on the 3.3V plane. The vias are spaced so that the plane that they pass through is unbroken as much as possible. This allows the currents that travel on these planes to take the shortest path without creating big current loops that would increase EMI.

4.2.3 Third Layer

The third layer is dedicated to the ground planes:

- The digital ground plane.
- The analog ground plane.
- The crystal oscillator ground plane.

It is crucial that the ground plane is below every component and trace that is referred to it, an example of this is shown in figure 4.12 where the GND_OSC plane extends all the way to the right, where the traces connect to the microcontroller. This is due to two reasons. The first is that this will reduce EMI, the second is that if a trace is outside the ground plane, the return current will not be able to travel directly underneath the trace. This will create a current loop that will cause interference.

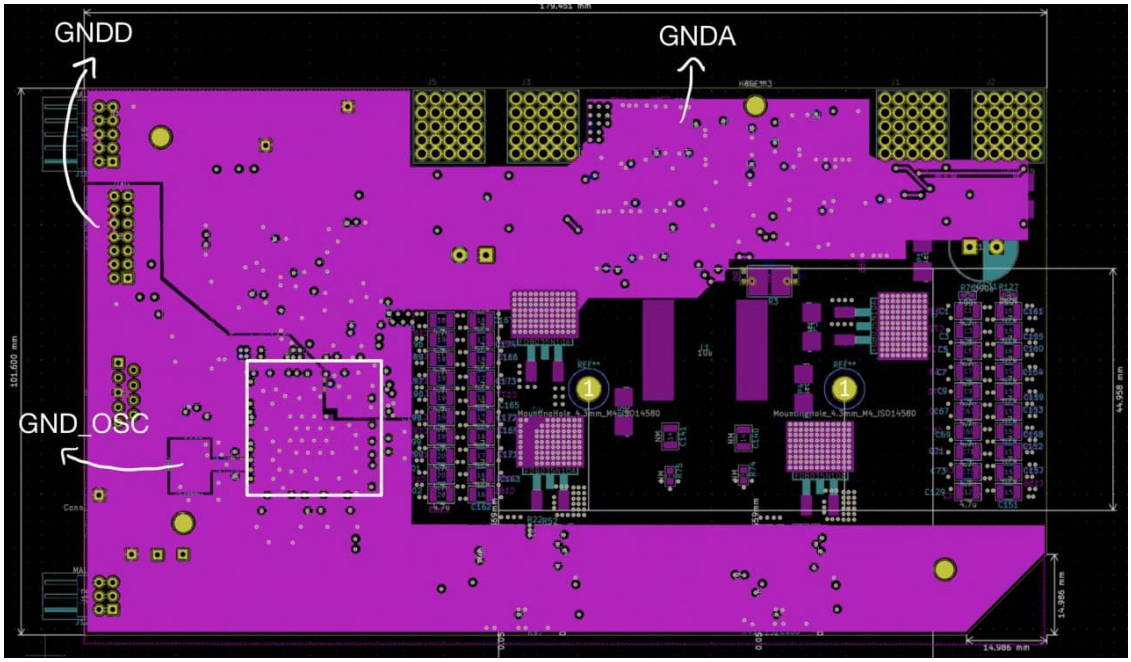


Figure 4.11: Layer 3 of the NIBB PCB

In figure 4.11 the microcontroller footprint is highlighted with a white square. We can see that underneath the microcontroller there are both the GNDA and GNDD planes. This is due to the fact that the microcontroller has both a digital and an analog part and thus needs a connection to both the planes.

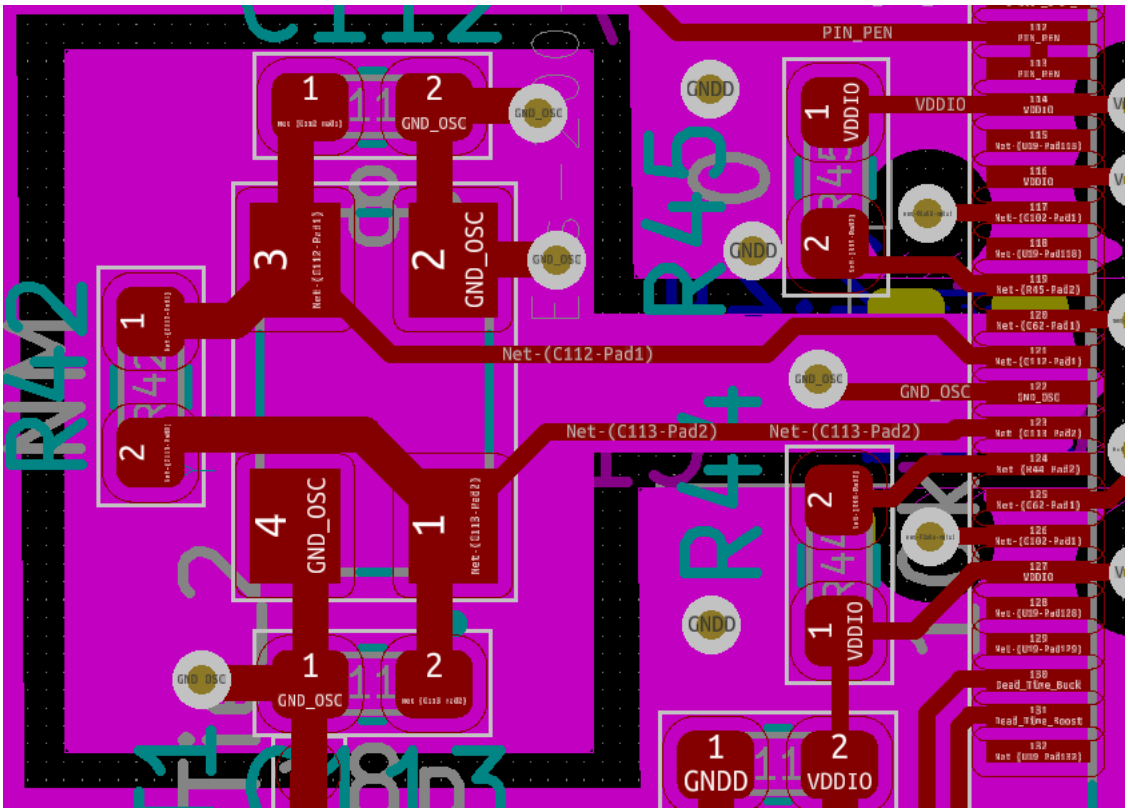


Figure 4.12: Crystal oscillator circuit with relative GND

4.2.4 Fourth Layer

The fourth layer is the bottom layer of the PCB. On this layer we have almost all of the measuring circuit components, half of the C_{in} and C_{out} capacitors, all the microcontroller's bypass capacitors and many traces. In figure 4.13 all the traces that brings the measures from the measuring circuit to the microcontroller are highlighted. In figure 4.13 we can also see the thermal copper zones, one of them is highlighted on the bottom right. The thermal copper zones are copper zones that are connected to the MOSFET's thermal pad through many vias. These zones help to distribute the heat over a large area. Thanks to the fact that the zones are on the bottom layer, they will be in contact with the heat sink, helping the heat dissipation.

In figure 4.14 we can see all the power traces that are on the bottom layer. The top one are used to bring the 12V and the GNDPWR to the supply board. The ones in the middle are used to bring the 3.3V and 1.2V supplies to the microcontroller and are connected to the two planes that we saw on

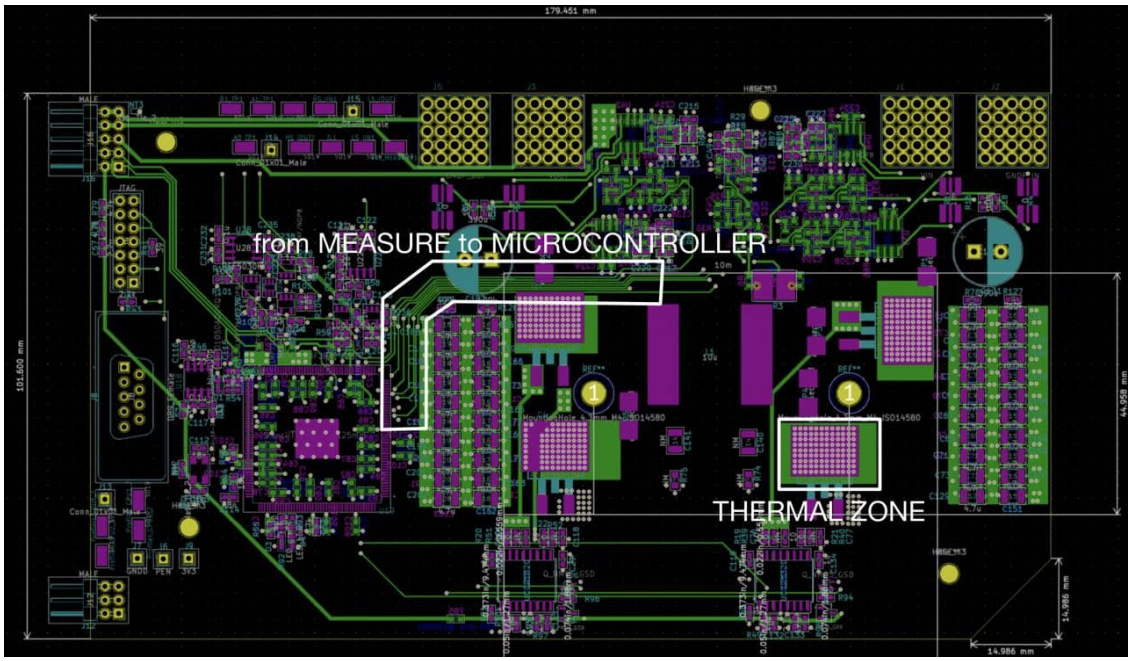


Figure 4.13: Layer 4 of the NIBB PCB

the second layer. The bottom trace, the longer one, is the trace that brings the 5V supply to the drivers. All these power traces are thicker than normal signal traces and are between $0.5mm$ and $0.8mm$ wide. In figure 4.14 also the traces that go from the drivers to the MOSFETs' gates are shown. These traces are $0.8mm$ wide and are connected to the components through many vias, this is because we want to minimize the parasitic inductance and also because there will be a relatively high current going through them.

The ferrite beads that were discussed in section 3.3.1 are connected in series with these traces. Each supply trace has its own ferrite bead. The ferrite beads are placed near to the noisy component in order to isolate the noise from the rest of the board. An example of this can be seen in figure 4.15 where the drivers circuit is shown. The ferrite is highlighted on the bottom left corner.

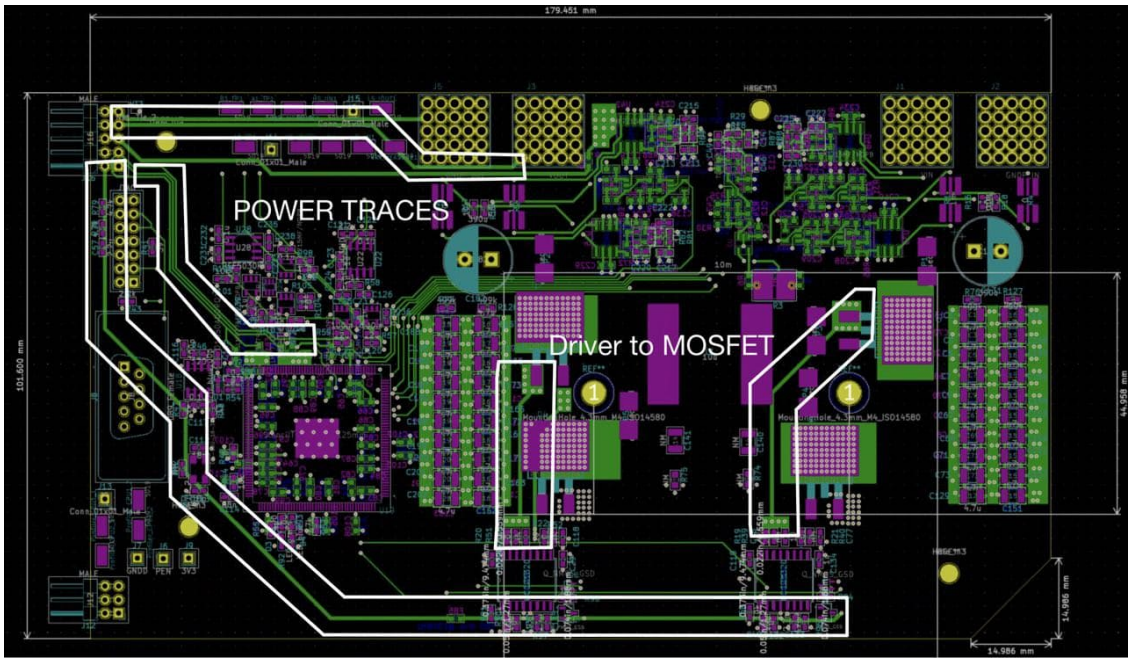


Figure 4.14: Layer 4 of the NIBB PCB, power traces

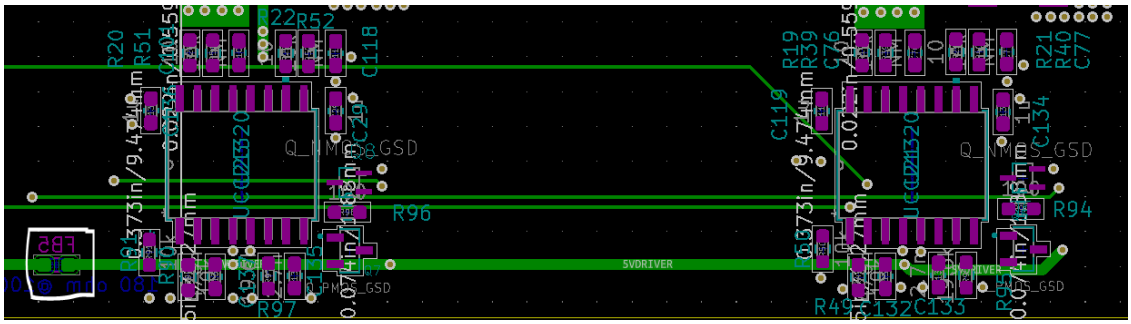


Figure 4.15: Ferrite bead placement in the drivers circuit

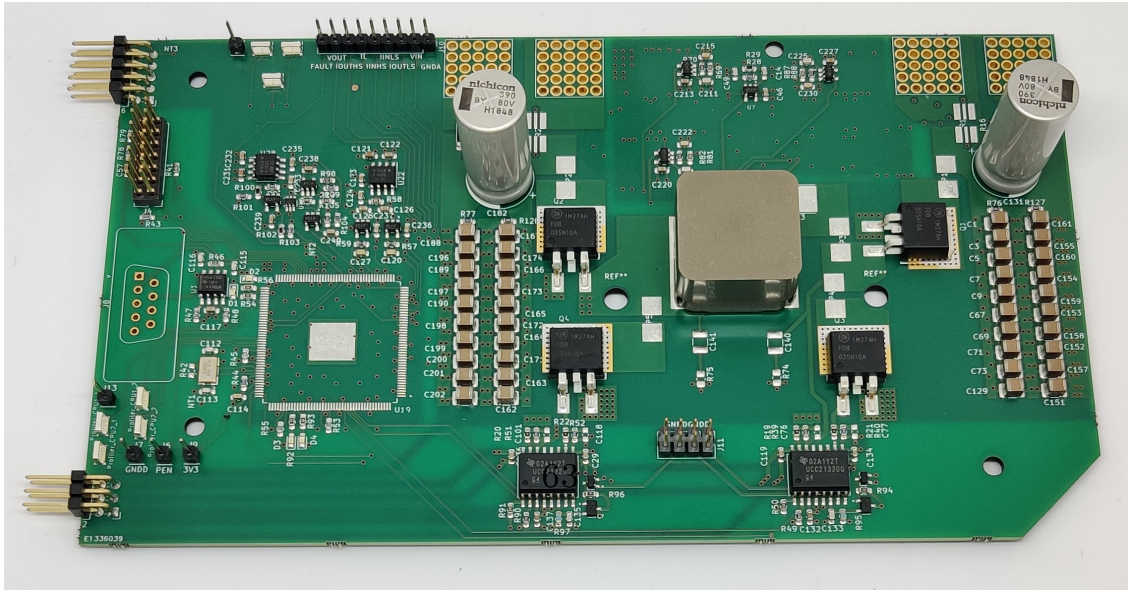


Figure 4.16: Front of the NIBB PCB

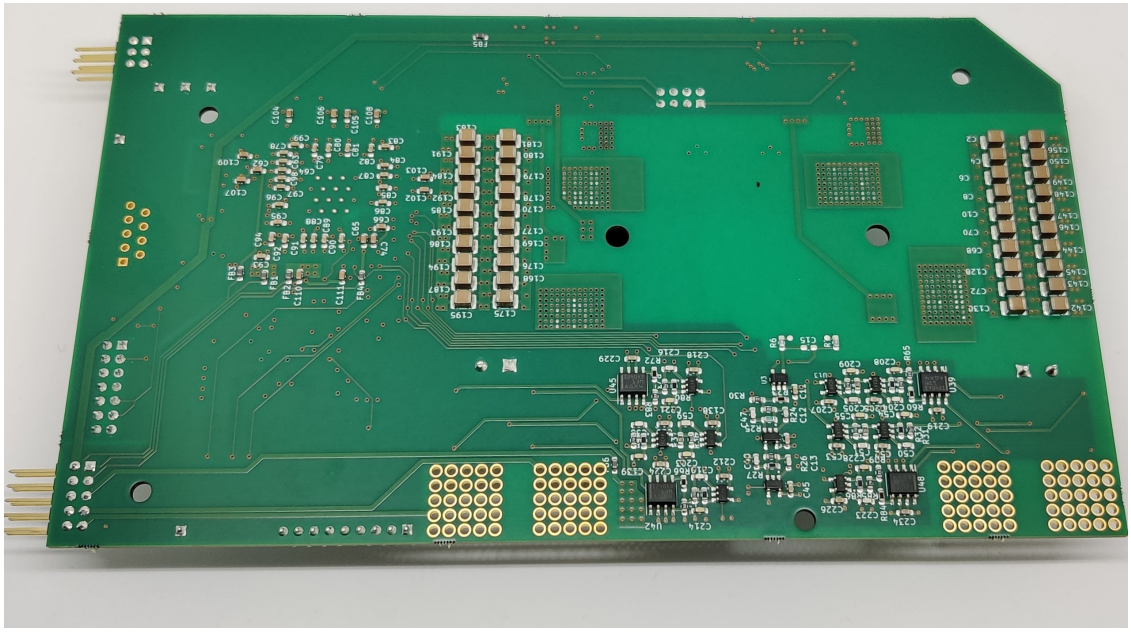


Figure 4.17: Back of the NIBB PCB

4.3 Supply Board

As said many times all the supplies are located on a separate PCB, the supply board. The supply board is connected to the NIBB board through pin headers. The two design requirements for this PCB were:

1. The connectors have to be at the same distance that are on the NIBB board, so we can connect them.

2. The board should be as narrow as possible.

The input voltage for all the power supply modules is the output voltage of the NIBB. This voltage enters the supply board through the left connector visible in figure 4.18. This voltage gets filtered through a π-filter, which's inductor is on the bottom left corner, before entering the 5V and 3.3V regulators. As already said in the design chapter, the 1.2V regulator takes as an input the 5V instead of 12V.

On the left side of the board there are the 5V, 3.3V and 1.2V circuits, on the right side there are the isolated power supplies.

Since there were 2 pins for the 5V supply, it was decided to implement two different 5V supplies. One for the digital part of the NIBB (the drivers) and one for the analog part of the NIBB (measure circuit, fault circuit, reference

voltage circuit). This was done to ensure a less noisy power supply for the analog part of the circuit.

Layer 1 and 2

On layer 1 we have the majority of connections, meanwhile on layer 2 we have the GNDA plane that extends till the middle of the board and on the right side we have the return path of the isolated supplies output. We can see that the forward path of the isolated power supplies output on the layer 1 is directly above the return path, minimizing the current loop area.

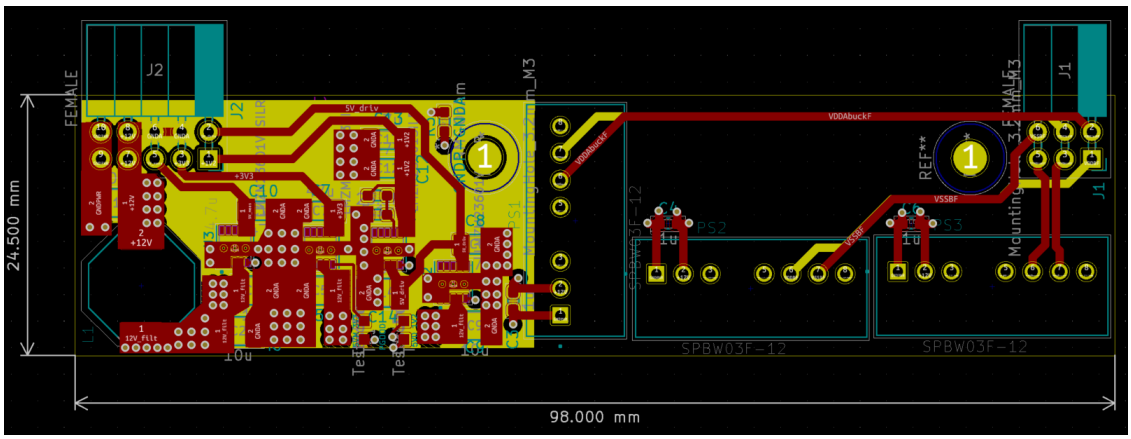


Figure 4.18: Layer 1 and 2 of the supply board

On layer 1 all the connections for the 5V, 3.3V and 1.2V modules are made using copper areas instead of traces to increase conductivity and heat dissipation. The ground connections are made with several vias for the same reason.

On the first layer we also have a 0Ω no mount resistor where we can connect a 0Ω resistor if we want to connect the GNDPWR and the GNDA plane.

Layer 3

In figure 4.19 the third layer is shown. This layer contains just the GNDPWR plane that is used by the isolated power supplies.

Layer 4

On layer 4 we have one big and one small copper area. The big one is the 12V copper area which is used by the isolated power supplies. The smaller

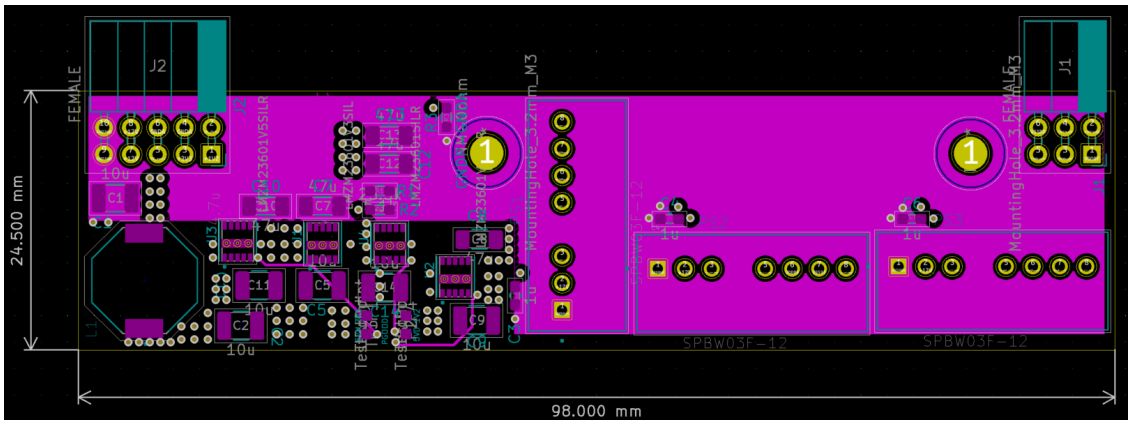


Figure 4.19: Layer 3 of the supply board

one is the copper area for the filtered 12V, which is, once again, used by the 5V and 3.3V circuits.

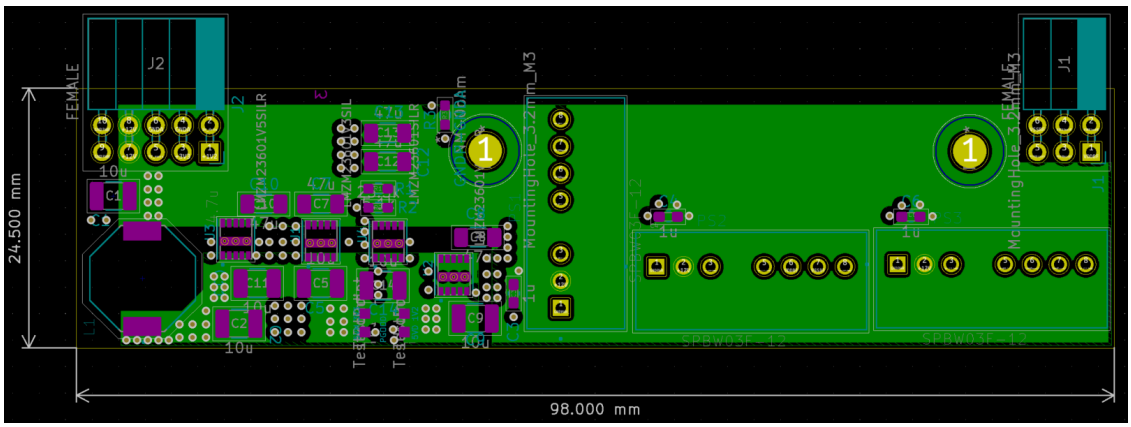


Figure 4.20: Layer 4 of the supply board

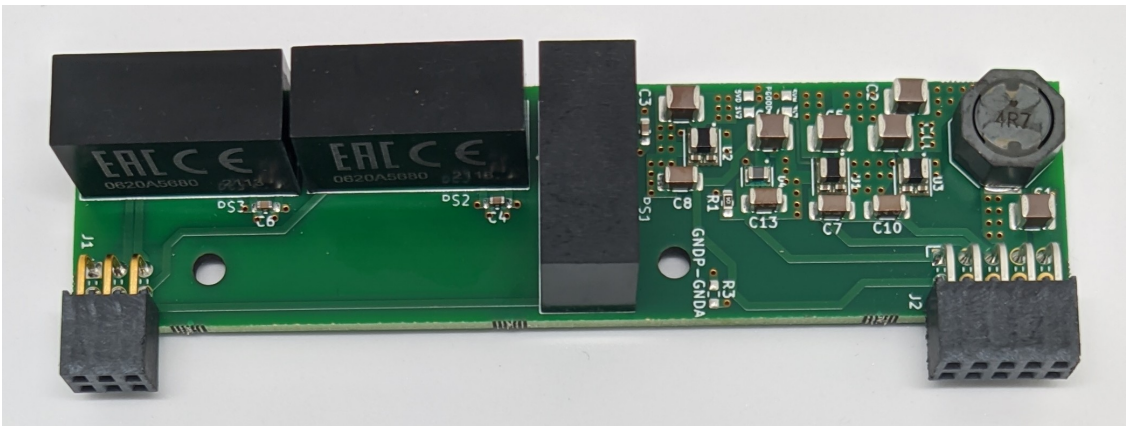


Figure 4.21: Front of the supply PCB

Testing

All the testing was done in open loop, having as V_{in} a voltage coming from a generator and as load either a 1Ω or a 3Ω resistor. The 5V supply and the supply for the drivers were coming from the supply board, confirming that it works perfectly. The testing bench is shown in figure 5.1. We have two generators, MCH-305D-II from MCH Instruments and the CPX400D from AIM-TTI Instruments, and the oscilloscope, Wavesurfer 434 from LeCroy.

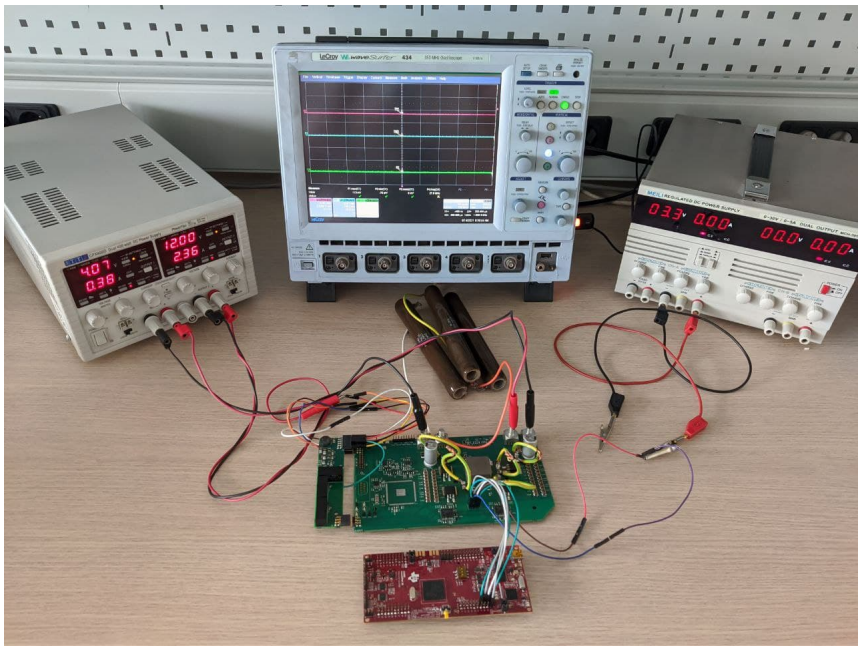


Figure 5.1: Testing bench

5.1 Power Stage Test

The power stage was tested in all the three modes: buck, boost and buck-boost. During the testing the efficiency was recorded for many different working points. In figure 5.2, 5.3 and 5.4 the three typical DC-DC converter waveforms are shown.

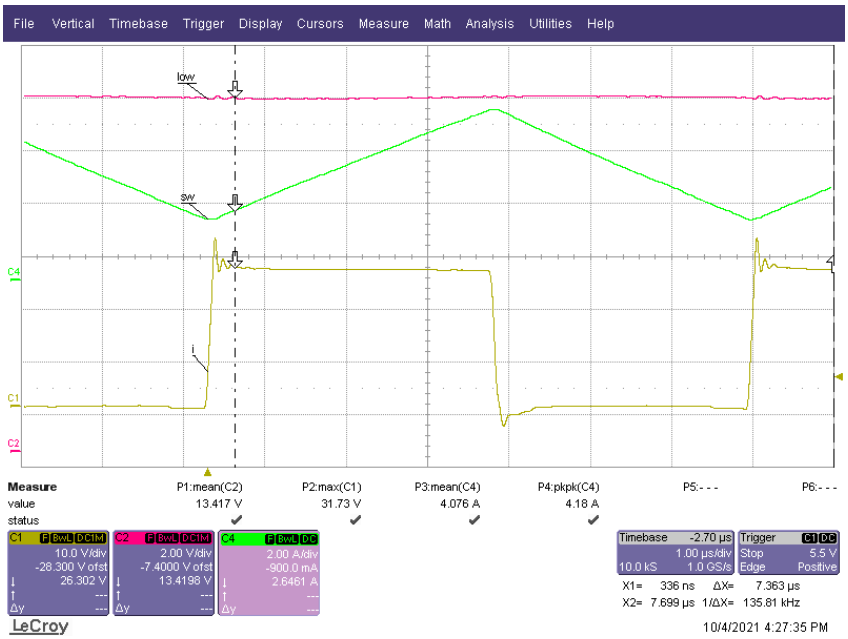


Figure 5.2: Buck mode typical waveforms: pink - V_{out}, yellow - switching node voltage, green - inductor current. Taken at $f_{sw} = 150kHz$ and $V_{in} = 26.3V$

We have:

- pink - V_{out}.
- yellow - switching node voltage.
- green - inductor current.

A snubber was applied to reduce the ringing on the switching node voltage.

The efficiency tests were performed using the setup shown in figure 5.5. We have:

- yellow - V_{in}.
- pink - V_{out}.

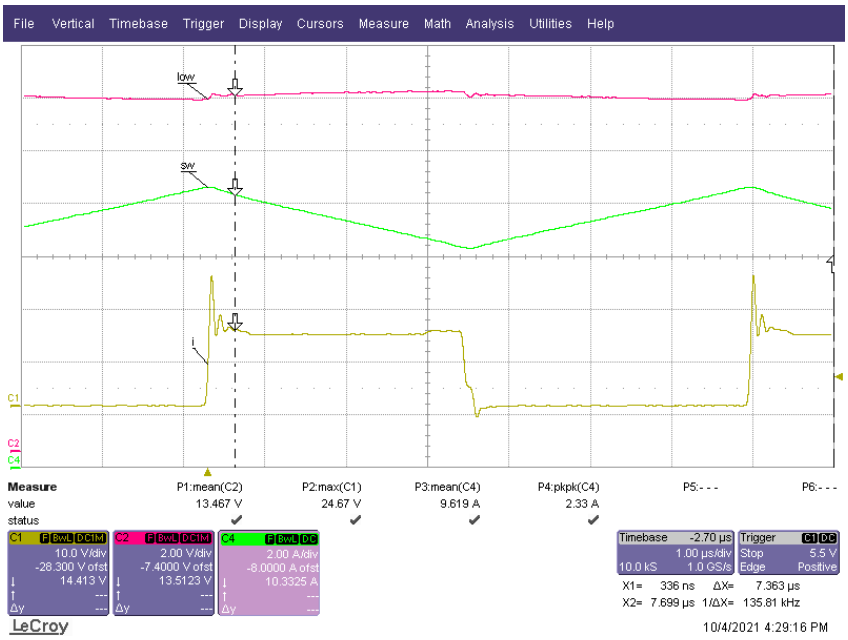


Figure 5.3: Boost mode typical waveforms: pink - V_{out}, yellow - switching node voltage, green - inductor current. Taken at $f_{sw} = 150kHz$ and $V_{in} = 6.7V$

- blue - I_{in}.
- green - I_{out}.

This setup allows us to quickly measure the efficiency in all the chosen working points by entering the mean value of the four variables in an excel file. After performing some tests, the found efficiency curve was compared with the theoretical efficiency curve that we calculated in the initial design steps. The efficiency tests were performed with a 3Ω load and so at a constant output power of 58W.

From the figure 5.6 we can see that the calculated efficiency matches pretty well the actual efficiency of the converter when we are not using a snubber. This is because during the calculations we didn't take into consideration the snubber losses. Moreover in some cases the measured efficiency is even better than the calculated one. As expected we can see that in the buck-boost mode the efficiency drops by some percents due to the fact that all the four transistors are switching and thus the switching losses increase. Overall we can say that the efficiency of the converter is very good given the fact that most of the time it will operate in buck mode, having an efficiency

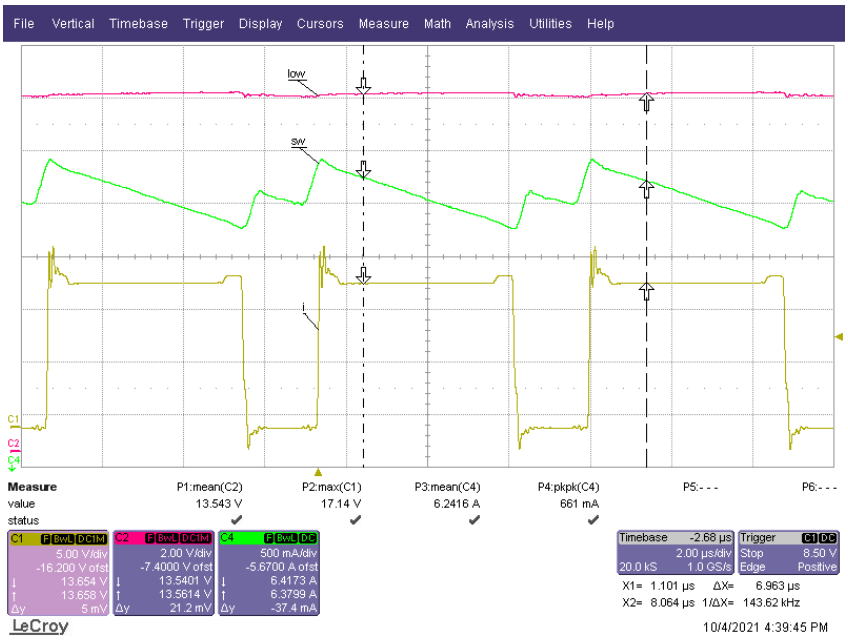


Figure 5.4: Buck-boost mode typical waveforms: pink - V_{out}, yellow - boost switching node voltage, green - inductor current. Taken at $f_{sw} = 150kHz$ and $V_{in} = 14V$

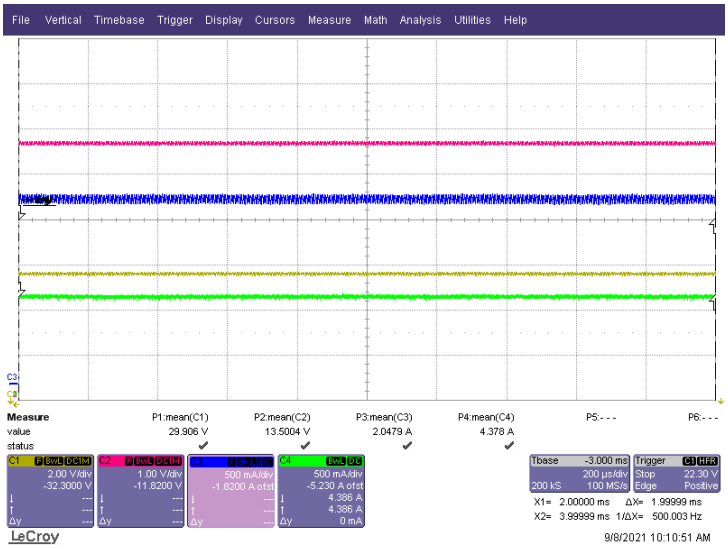


Figure 5.5: Efficiency measure oscilloscope setup: yellow - V_{in}, pink - V_{out}, blue - I_{in}, green - I_{out}. Taken at $f_{sw} = 150kHz$ and $V_{in} = 29.9V$

$> 97\%$. When we added the snubber to the NIBB, the efficiency dropped, as expected. To maintain a good efficiency and sill have the benefits of the

snubber we can use a bigger resistor in the snubber, but the oscillations will get a little bit worse, or we can use a different and more sophisticated snubber circuit that will guarantee both good dampening and good efficiency.

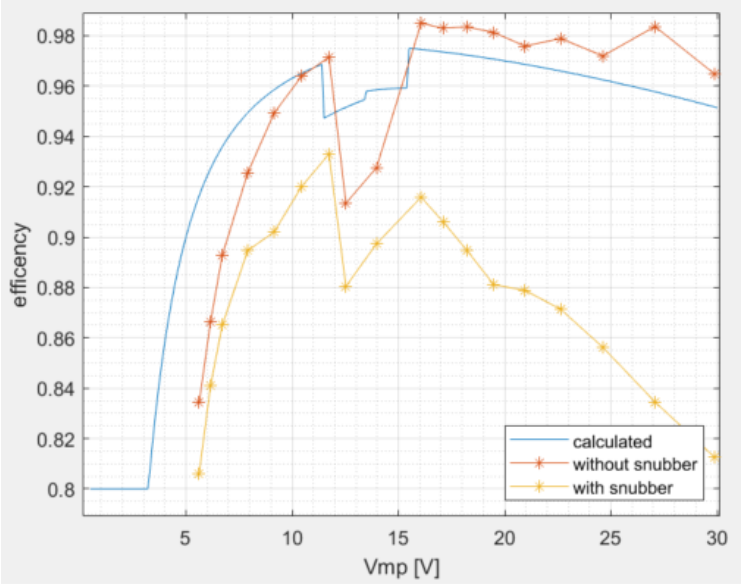


Figure 5.6: Efficiency curves: blue - calculated efficiency, orange - measured efficiency without snubber, yellow - measured efficiency with snubber

Efficiency measures were performed also for other frequencies, the results are shown in figure, 5.7. All the measures in this figure are performed with the snubber. The efficiency drops with the increase of the frequency because the switching losses increase.

The last efficiency measure was performed with a variable load to simulate the TEG's output power. Unfortunately we had just 1Ω resistors and so we couldn't simulate exactly the TEG's output power, The employed power is shown in fugure 5.8b. Results of the efficiency testing are shown in figure 5.8a

The input and output ripple of current and voltage was checked in several working point, changeing frequency, operating mode and duty cycle. The results are reported in table 5.1. We can see that at 30kHz the ripple increases significantly,this is because with a 3Ω resistor the NIBB was working in DCM. Furthermore it is interesting to note how the ripple increases with the decrease of the switching frequency.

Some tests were performed on the MOSFETs to see how high are their

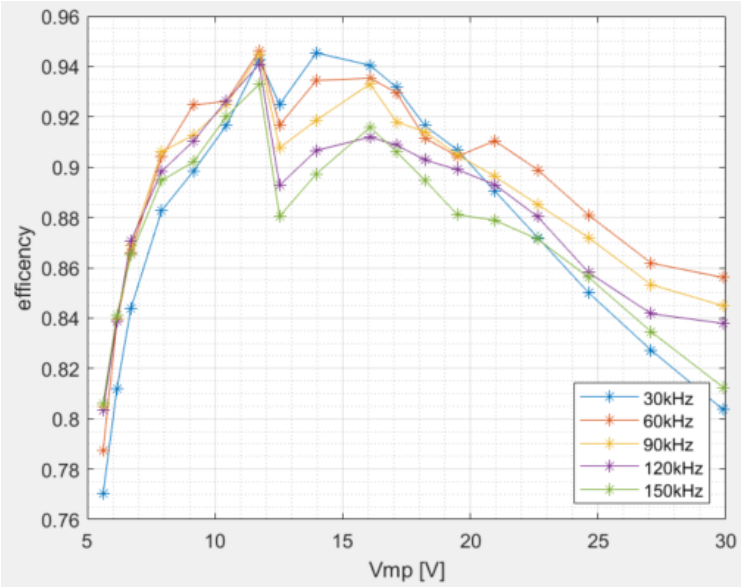
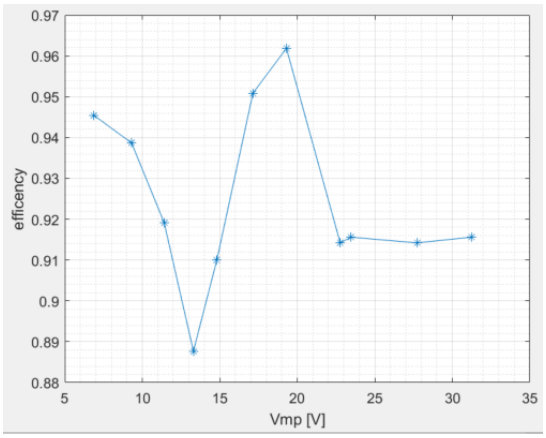
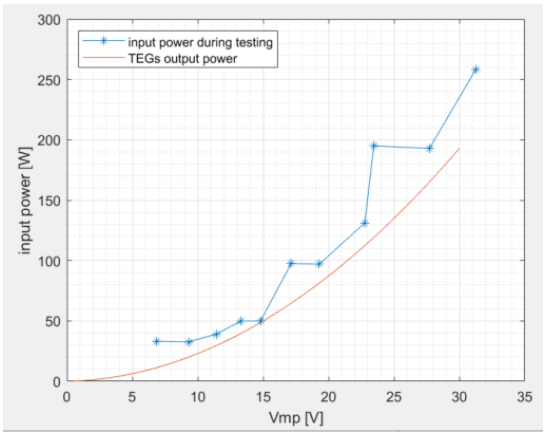


Figure 5.7: Efficiency curves at different switching frequencies, all performed with a snubber



(a) Efficiency curve approximating TEG's output power



(b) NIBB's input power used during the efficiency testing (blue) VS actual TEG's output power (orange)

Figure 5.8: Testing the NIBB's efficiency simulating the real TEG output power curve, $f_{sw} = 150kHz$

actual losses. The quantities that were measured were V_{ds} and I_{ds}. By multiplying these two quantities we can find the instantaneous value of the sum of the following losses: conduction losses, switching losses, reverse recovery

f_{sw}	**MODE**	**DUTY**	V_{in} **ripple [mV]**	V_{out} **ripple [mV]**	I_{in} **ripple [mA]**	I_{out} **ripple [mA]**	**% ripple** V_{out}
150KHZ	BUCK	0.5	772	169	36	15	1.25
150KHZ	BUCK	0.8	604	103	25	8	0.76
150KHZ	B-B	0.9/0.35	448	228	21	23	1.69
150KHZ	BOOST	0.5	147	276	16	33	2.04
150KHZ	BOOST	0.7	187	417	15	46	3.09
120KHZ	BUCK	0.5	733	182	50	23	1.35
120KHZ	BUCK	0.8	592	109	34	12	0.81
120KHZ	B-B	0.9/0.35	427	256	37	33	1.90
120KHZ	BOOST	0.5	162	306	19	48	2.27
120KHZ	BOOST	0.7	200	484	22	64	3.59
90KHZ	BUCK	0.5	644	230	68	42	1.70
90KHZ	BUCK	0.8	579	152	58	22	1.13
90KHZ	B-B	0.9/0.35	405	306	41	48	2.27
90KHZ	BOOST	0.5	198	378	37	71	2.80
90KHZ	BOOST	0.7	230	551	35	96	4.08
60KHZ	BUCK	0.5	539	375	134	87	2.78
60KHZ	BUCK	0.8	536	220	103	42	1.63
60KHZ	B-B	0.9/0.30	417	335	72	63	2.48
60KHZ	BOOST	0.5	266	442	95	107	3.27
60KHZ	BOOST	0.7	314	644	81	144	4.77
30KHZ	BUCK	0.5	798	874	467	224	6.47
30KHZ	BUCK	0.8	546	422	320	105	3.13
30KHZ	B-B	0.9/0.30	510	447	236	114	3.31
30KHZ	BOOST	0.5	547	590	361	160	4.37
30KHZ	BOOST	0.7	521	787	326	214	5.83

Table 5.1: Output and input voltage and current ripple in different working points

charge losses and deadtime losses. Then by averaging the found quantities we can find the average power loss for each transistor. These testes were performed for f_{sw}=30kHz, 60kHz, 90kHz, 120kHz, 150kHz. For each switching frequency four tests were performed, two in buck mode and two in boost mode. In table 5.2 the results are reported. We can see how the measured losses decrease with the increase of the frequency. Htis is due to the decrease of the switching losses. Another interesting thing to notice is that despite the low frequency, the losses increase for the 30kHz switching frequency. This is due to the fact that with this switching frequency the converter was working in DCM.

5.2 Switching Performance

Some tests were performed to evaluate the switching performance. In figure 5.9 we have the full switching chain:

- blue - PWM signal coming from the microcontroller.
- yellow - driver's output signal that goes to the MOSFET's gate.

FREQUENCY	MODE	DUTY	LS/HS	CALCULATED LOSS [W]	MEASURED LOSS [W]
150kHz	BUCK	0.5	LS	1.59	2.35
150kHz	BUCK	0.8	LS	1.03	1.58
150kHz	BOOST	0.5	LS	1.15	1.90
150kHz	BOOST	0.7	LS	1.59	2.13
150kHz	BUCK	0.5	HS	1.59	1.28
150kHz	BUCK	0.8	HS	1.03	1.50
150kHz	BOOST	0.5	HS	1.15	1.53
150kHz	BOOST	0.7	HS	1.76	1.00
120kHz	BUCK	0.5	LS	1.66	2.40
120kHz	BUCK	0.8	LS	0.99	1.48
120kHz	BOOST	0.5	LS	1.17	1.91
120kHz	BOOST	0.7	LS	1.82	2.10
120kHz	BUCK	0.5	HS	1.66	1.44
120kHz	BUCK	0.8	HS	1.02	1.40
120kHz	BOOST	0.5	HS	1.17	1.87
120kHz	BOOST	0.7	HS	1.64	1.16
90kHz	BUCK	0.5	LS	1.64	2.03
90kHz	BUCK	0.8	LS	0.97	1.49
90kHz	BOOST	0.5	LS	1.18	2.09
90kHz	BOOST	0.7	LS	1.89	2.96
90kHz	BUCK	0.5	HS	1.64	1.28
90kHz	BUCK	0.8	HS	1.00	1.55
90kHz	BOOST	0.5	HS	1.18	1.71
90kHz	BOOST	0.7	HS	1.69	1.34
60kHz	BUCK	0.5	LS	1.53	1.90
60kHz	BUCK	0.8	LS	0.95	1.31
60kHz	BOOST	0.5	LS	1.21	1.67
60kHz	BOOST	0.7	LS	1.96	2.48
60kHz	BUCK	0.5	HS	1.53	1.22
60kHz	BUCK	0.8	HS	0.98	1.59
60kHz	BOOST	0.5	HS	1.21	1.67
60kHz	BOOST	0.7	HS	1.75	1.32
30kHz	BUCK	0.5	LS	1.48	2.89
30kHz	BUCK	0.8	LS	0.89	1.59
30kHz	BOOST	0.5	LS	1.26	1.68
30kHz	BOOST	0.7	LS	2.09	2.25
30kHz	BUCK	0.5	HS	1.48	5.82
30kHz	BUCK	0.8	HS	0.93	2.65
30kHz	BOOST	0.5	HS	1.26	2.53
30kHz	BOOST	0.7	HS	1.86	1.25

Table 5.2: MOSFETs' calculated loss VS measured loss. LS=low side transistor, HS=high side transistor

- pink - NIBB switching node voltage.

Thanks to this image we can calculate the delay introduced by the driver. The delay introduced by the driver is highlighted in figure 5.10a and is equal to 42ns. The delay that we see in figure 5.10b is the delay between the switching voltage and the driver signal. We can see that the switching voltage goes low before the driver signal is changed from low to high. This is due

to the dead time. During the deadtime the switching node is connected to ground through the body diode of the low side MOSFET and so as soon as the high side MOSFET goes OFF, the switching node goes low.

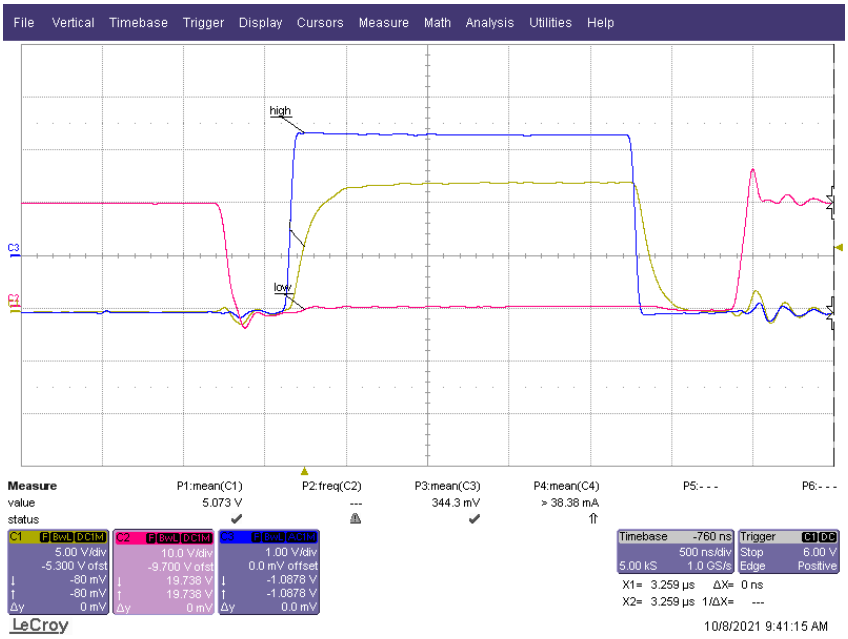
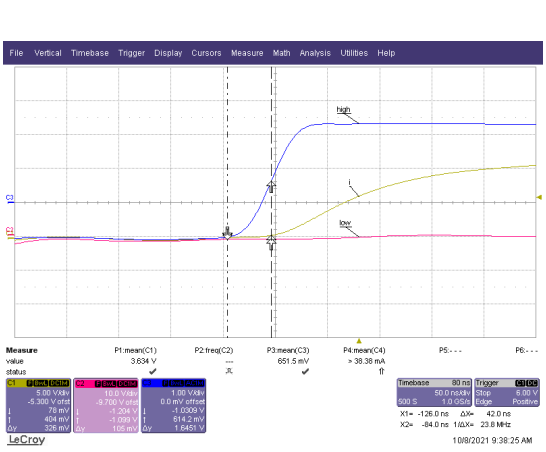


Figure 5.9: Switching chain signals: blue - PWM signal coming from the microcontroller, yellow - driver's output signal that goes to the MOSFET's gate, pink - NIBB switching node voltage

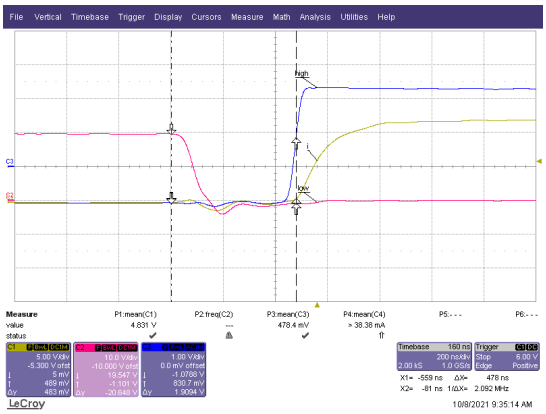
We performed a test to evaluate the correct functioning of the hardware deadtime circuit. To do so we sent to the driver a PWM signal from the microcontroller that had a deadtime $< 200ns$. Given that the selected hardware deadtime is 200ns, the driver ignored the deadtime of the signal sent by the microcontroller, imposing the deadtime set by the hardware deadtime. In figure 5.11 we can see the results of this test, we have:

- yellow, green - PWM signals sent from the microcontroller to the driver.
- pink, blue - PWM signal sent from the driver to the MOSFETS' gates.

We can see that the hardware deadtime works correctly as the delay between the pink and blue signals is approximately 200ns.



(a) Delay between microcontroller signal and driver output



(b) Delay between switching node voltage and driver signal, that is equal to the deadtime

Figure 5.10: Switching signals: blue - PWM signal coming from the microcontroller, yellow - driver's output signal that goes to the MOSFET's gate, pink - NIBB switching node voltage

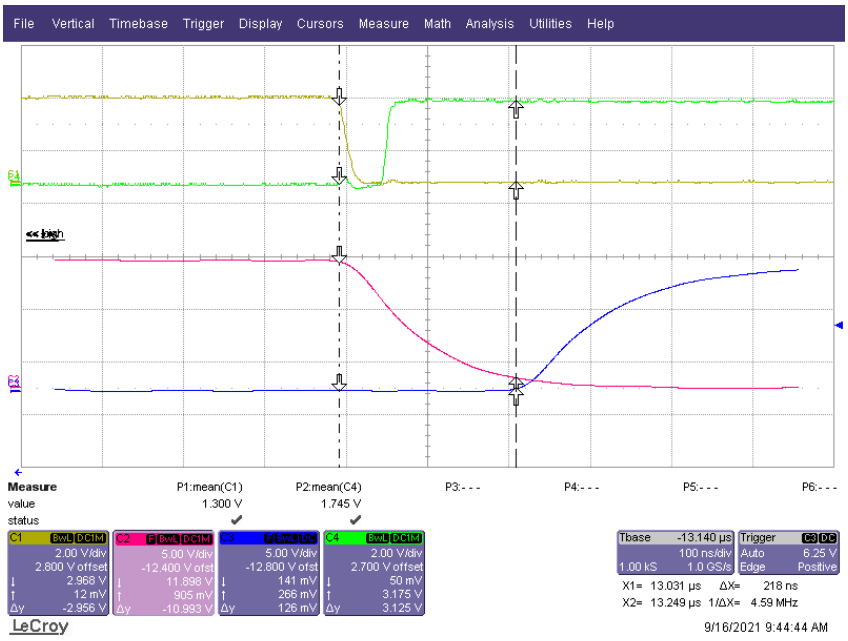


Figure 5.11: Hardware deadtime test: yellow, green - PWM signals sent from the microcontroller to the driver, pink, blue - PWM signal sent from the driver to the MOSFETS' gates

The last test performed on the switching chain was the one needed to

estimate the the minimum deadtime that would prevent the shoot through current. From the figure 5.11 we can see that a safe deadtime would be around 300ns.

5.3 Measure Stage Test

The measuring stage of the NIBB was tested by comparing the true value of the quantity that we are interested in with the value coming from the measuring stage. The true value was multiplied with the gains (of the amplifiers) and the attenuation (of the voltage divider) present in the measuring stage before comparing it with the value coming from the measuring stage. To make this concept more clear let's make ad example. The I_{in} measured with the oscilloscope probe is 17.02A. The I_{in} measuring circuit tells us that I_{in} has a value corresponding to 1.03V. Now, if we want to compare the two quantities we have to convert the true value in the following way:

$$I_{in} \cdot R_{shurnt} \cdot G_s \cdot G_d = 17.02A \cdot 0.001\Omega \cdot 100 \cdot \frac{10000}{10000 + 6810} = 1.01V \quad (5.1)$$

Where $R_{shurnt} = 0.001\Omega$ is the shunt resistor, $G_s = 100$ is the current sensor gain and $G_d = \frac{10000}{10000+6810}$ is a voltage divider. Comparing the two quantities of 1.01V and 1.03V we see that we have a relative error of 1.7%. In the tables 5.3, 5.5 and 5.6 we see all the performed tests. The compensating gain is a gain that can be implemented in the microcontroller to improve the measure and is calculated as $\frac{calculatedQuantity}{measuredQuantity}$.

Iin true [A]	**Iin measured** [V]	**Iin calculated**[V]	**compensating gain**	**relative error**
1.000	0.075	0.059	0.793	0.261
2.000	0.135	0.119	0.881	0.135
3.000	0.196	0.178	0.911	0.098
4.010	0.257	0.239	0.928	0.077
5.000	0.315	0.297	0.944	0.059
8.030	0.497	0.478	0.961	0.040
10.970	0.673	0.653	0.970	0.031
14.040	0.856	0.835	0.976	0.025
17.020	1.030	1.012	0.983	0.017
19.950	1.200	1.187	0.989	0.011

Table 5.3: I_{in} measuring circuit test

Looking at 5.3 we see that the measure becomes more precise as the current increases and so the relative error is not constant. As we can see from figure

Iout true [A]	**Iout measured** [V]	**Iout calculated**[V]	**compensating gain**	**relative error**
1.000	0.060	0.059	0.991	0.009
2.000	0.128	0.119	0.930	0.076
3.000	0.175	0.178	1.020	0.019
4.000	0.232	0.238	1.026	0.025
6.000	0.356	0.357	1.003	0.003
8.040	0.474	0.478	1.009	0.009
11.030	0.650	0.656	1.009	0.009
14.010	0.830	0.833	1.004	0.004
17.000	1.008	1.011	1.003	0.003
20.040	1.190	1.192	1.002	0.002

Table 5.4: I_{out} measuring circuit test

Vin true [V]	**Vin measured** [V]	**Vin calculated** [V]	**compensating gain**	**relative error**
5.000	0.250	0.249	0.995	0.005
10.020	0.497	0.499	1.003	0.003
15.000	0.741	0.746	1.007	0.007
20.000	0.988	0.995	1.007	0.007
25.000	1.233	1.244	1.009	0.009
30.000	1.480	1.493	1.008	0.008

Table 5.5: V_{in} measuring circuit test

5.12 this is caused by an offset error. Unfortunately we couldn't test the sensor for currents above 20A as this is the generator's current limit. Knowing the value of the offset error we can easily compensate for it, increasing the accuracy of the measure, especially for the low current measures. From the output current measures we see that the sensor is more accurate in this case, the error does not change very much changing the output current.

Analysing table 5.5 we see that the voltage measures are very good also for low voltages and that the error and compensating gain are constant. This is because the only error here is the one introduced by the voltage divider resistors, which is constant. This is a good news because if we implement the compensating gain in the microcontroller we can increase the accuracy even more. For the data shown in 5.6 regarding the measure of V_{out} the same considerations apply. An example of the measuring circuit output can be seen in figure 5.16, where we have the actual V_{out} in yellow and the measured output voltage in pink. We can see that the measuring circuit follows pretty closely the true output voltage dynamic.

Let's now analyse the most problematic measuring circuit, the one for the inductor current. Two test were performed both at a switching frequency of 30kHz, one with the RC filter and one without the RC filter. In figure 5.17

Vout true [V]	Vout measured [V]	Vout calculated [V]	compensating gain	relative error
9.000	1.340	1.364	1.018	0.017
11.000	1.630	1.667	1.022	0.022
13.000	1.930	1.970	1.021	0.020
13.500	2.000	2.045	1.023	0.022
15.030	2.230	2.277	1.021	0.021

Table 5.6: V_{out} measuring circuit test

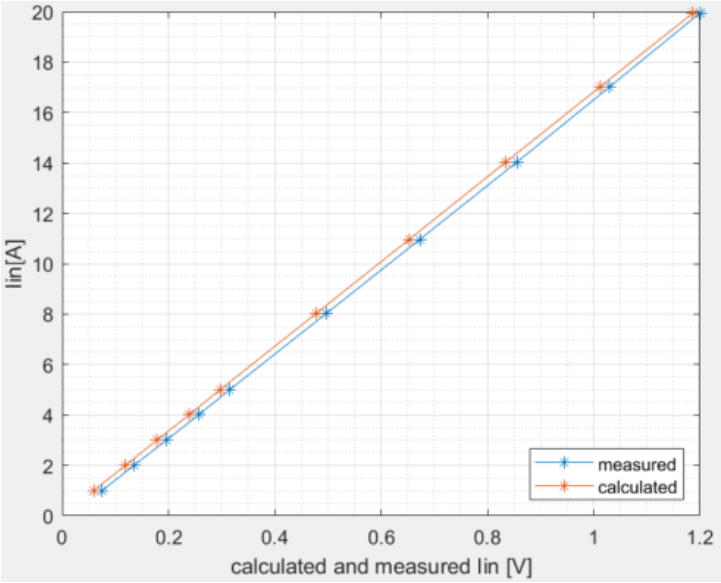


Figure 5.12: I_{in} measuring stage characteristic

we have in yellow the waveform coming from the measuring circuit and in blue the true inductor current coming form the oscilloscope probe. In figure 5.18 we have in yellow the waveform coming from the measuring circuit but this time the RC filter is applied.

It is clear that the RC filter makes the waveform much better, confirming its the theoretical utility. In both the situations, with and without filter we see a drop in the voltage when the inductor current changes slope. This is probably due to the sensor that is not able to handle well a big $\frac{dv}{dt}$ and the only way to solve it would be to change the sensor. This issue with the sensor becomes even more evident if we perform a test increasing the switching frequency. Apart from this problem, the measured quantity magnitude is correct.

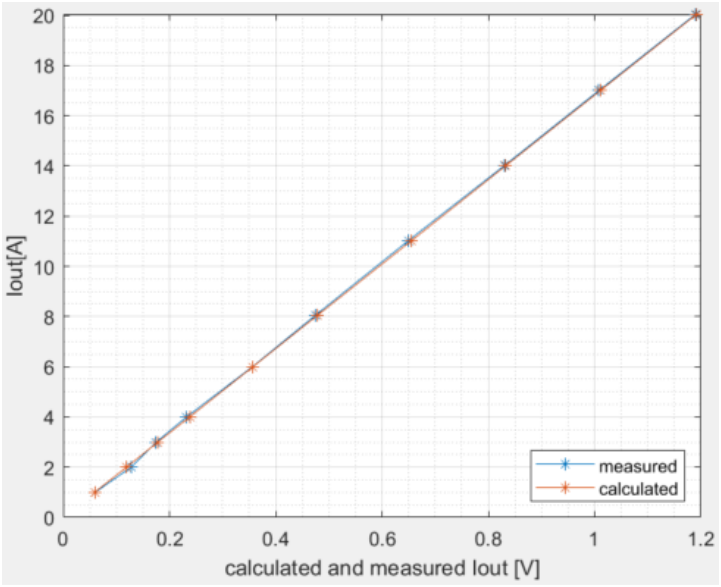


Figure 5.13: I_{out} measuring stage characteristic

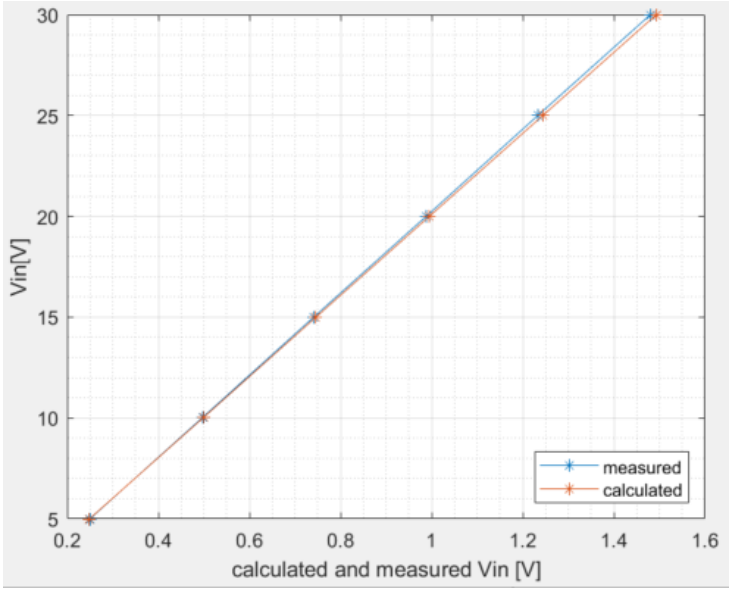


Figure 5.14: V_{in} measuring stage characteristic

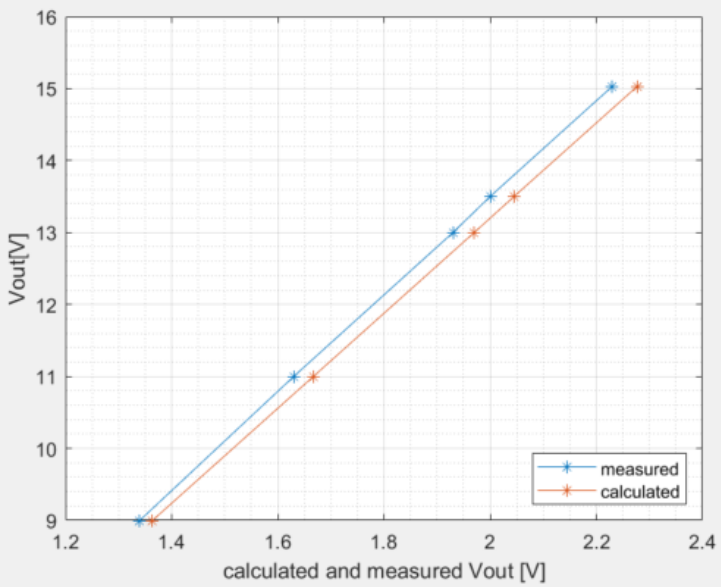


Figure 5.15: V_{out} measuring stage characteristic

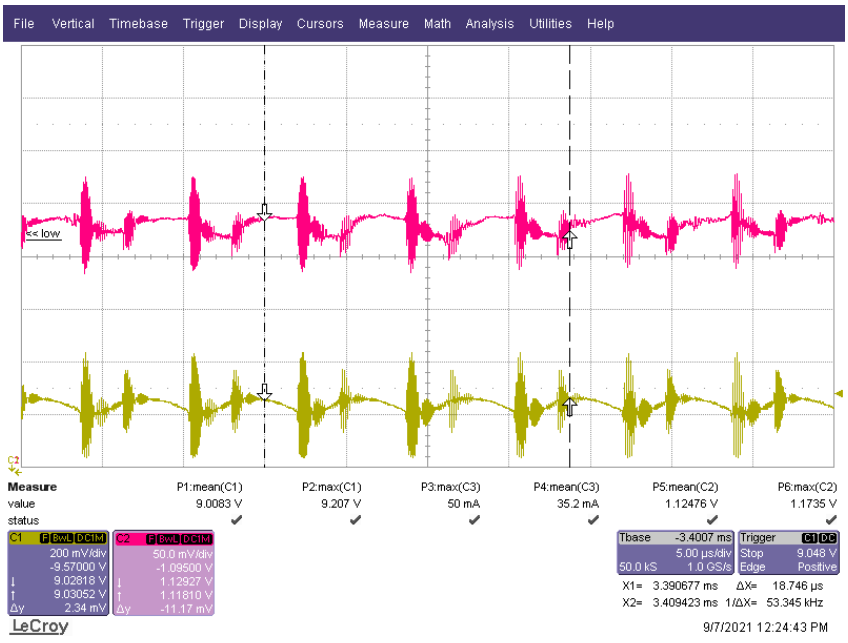


Figure 5.16: pink: V_{out} measure circuit output, yellow: true V_{out}

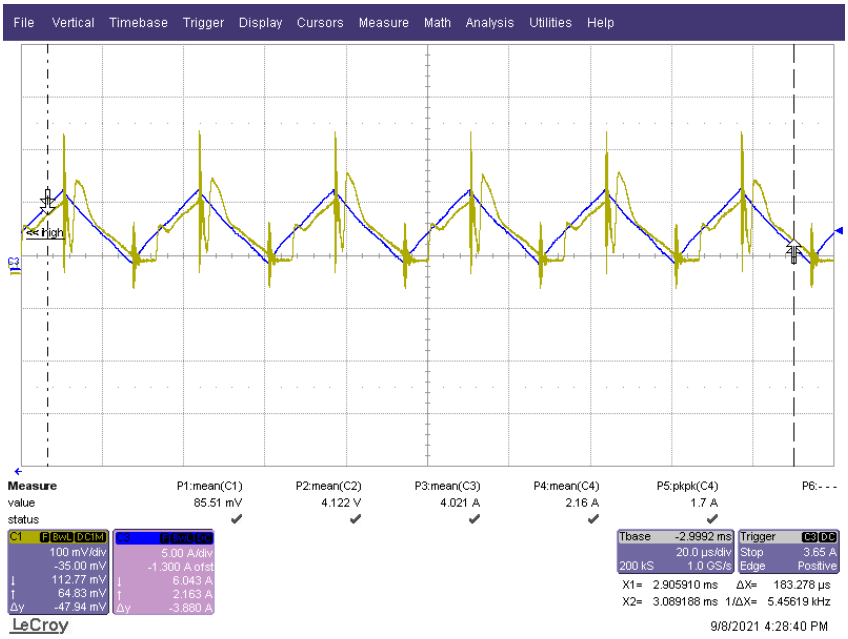


Figure 5.17: Inductor current measure **without** RC filter

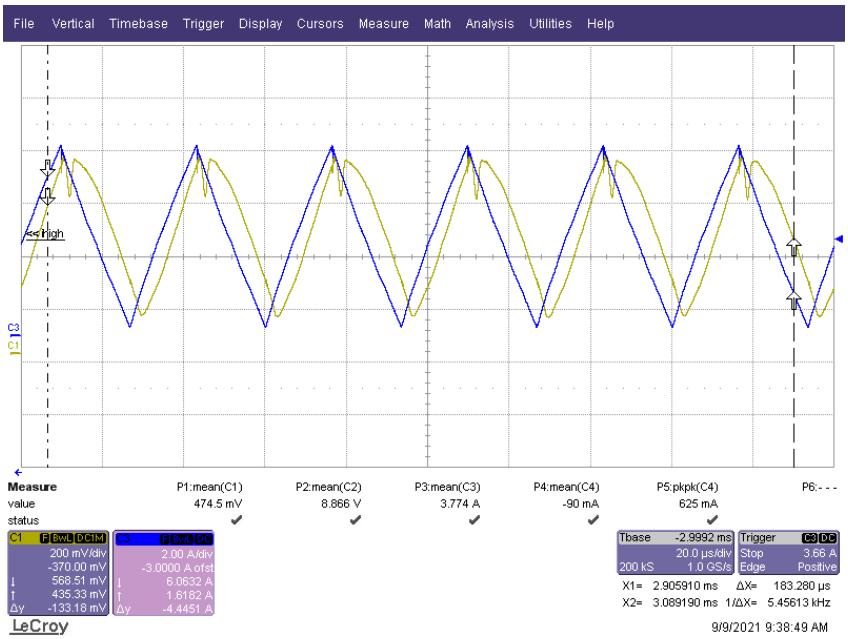


Figure 5.18: Inductor current measure **with** RC filter

Conclusion

In this thesis all the steps to design and realise a NIBB PCB were shown. A non-inverting buck-boost was successfully designed, prototyped and tested. The comparison between the laboratory tests and the initial design calculations was very good, showing that the design process was carried out with care and that the design choices were correct.

Nonetheless the NIBB board can be further improved. For example by putting all the components of the supply board on the NIBB board, thus making a single functioning PCB. Another possible improvement could be made on the inductor current measuring circuit by replacing the used sensor with a sensor that can better handle high dv/dt, and possibly by increasing the shunt resistor. A last possible improvement is to use a more efficient snubber circuit to increase the overall NIBB efficiency.

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