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Master's Degree in Nanotechnologies for ICTs

Electrical Characterization of Hex-SiGe Nanowires

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Abstract

The semiconductor industry has required a significant increase in energy efficiency and computational performance of the electronic devices for decades. This results in the search for low-power, high-frequency devices. To meet these demands it was necessary to replace the electrical signals with photonic signals. One of the possible candidates are group III-V semiconductor materials, which can efficiently emit light, but they are not CMOS compatible, so their integration with Si chips is very expensive. Ge-rich SiGe alloys grown in the hexagonal crystal structure showed a direct bandgap nature. SiGe compounds are epitaxially grown in the hexagonal phase by MOVPE on thin hexagonal GaAs nanowires, that act as templates. The result is a hex-GaAs core surrounded by a hex-SiGe shell in a GaAs/SiGe core/shell nanowire configuration. While it is difficult to engineer the growth of this novel material, it has been proven to efficiently emit light and it is CMOS compatible as well. Thus, it could revolutionize the optoelectronics industry, replacing group III-V semiconductor materials.

Despite the promising experimental results obtained regarding this novel material, many of its electrical, mechanical and optical properties still need to be investigated. The purpose of this thesis is the electrical characterization of hexagonal Ge-rich SiGe alloys carried out in the well-equipped BRNC cleanroom facility of IBM Research Europe. Previous attempts highlighted some issues in its development, including the difficulty in obtaining ohmic contacts at the metal-semiconductor interface. For this reason, one of the main objectives of this project is the investigation of the current-voltage characteristics performed on the material to analyze the occurrence of Schottky potential barriers. From this analysis arises the need to highly dope the metal-semiconductor contact areas by solid-state diffusion to overcome the potential barriers due to the tunnel effect in order to obtain ohmic contacts. In addition, from resistivity measurements it is possible to estimate the doping concentration in the material to verify the effectiveness of the process. Furthermore, some annealing tests highlighted the interference by arsenic impurities coming from the GaAs core in the nanowires during solid-state diffusion doping. This required etching the GaAs core from the nanowires in order to analyze the results of the process on the SiGe shells without additional interference.

To mum and dad
who always believed in me

A mamma e papà
che hanno sempre creduto in me

Contents

Acronyms

ALD	Atomic Layer Deposition
APT	Atom Probe Tomography
BCB	Bisbenzocyclobutene
BHF	Buffered Hydrofluoric Acid
DFT	Density Functional Theory
DMSO	Dimethyl Sulfoxide
EBL	Electron Beam Lithography
EDS	Energy-Dispersive X-ray Spectroscopy
FIB	Focused Ion Beam
FLP	Fermi Level Pinning
GDS	Graphic Design System
HF	Hydrofluoric Acid
IPA	Isopropyl Alcohol
MA	Methacrylic Acid
MIBK	Methyl Isobutyl Ketone
MOCVD	Metal Organic Chemical Vapor Deposition
MOVPE	Metal Organic Vapor Phase Epitaxy
MSM	Metal-Semiconductor-Metal
NW	Nanowire
PECVD	Plasma Enhanced Chemical Vapor Deposition
PMMA	Poly Methyl Methacrylate
RIE	Reactive Ion Etcher
RTA	Rapid Thermal Annealing
SB	Schottky Barrier
SBH	Schottky Barrier Height
SE	Secondary Electrons
SEM	Scanning Electron Microscope
SNMS	Secondary Neutral Mass Spectrometry
TEM	Transmission Electron Microscope
TLM	Transmission Line Measurement
VLS	Vapour-Liquid-Solid

Chapter 1

Introduction

Ever since the invention of the first transistor, semiconductor materials played a fundamental role in the exponential growth of technology. In particular, two elements of group IV, silicon and germanium, were distinguished among others by their excellent electrical properties. Furthermore, with the advent of metal-oxide-semiconductor field-effect transistors, the need for a high quality oxide allowed silicon to excel over germanium. The exponential growth of the electronics-based semiconductor industry led to the miniaturization of electronic devices in order to maximize data processing and transfer speeds and minimize energy consumption. These improvements digitized the entire telecommunications system, but at the same time it required processing a huge amount of data.

To process a huge amount of data it is necessary to further increase the speed of electrical devices, but this results in additional energy consumption. To reduce energy consumption the size of the devices should be further reduced. However, over the past years, microelectronics devices has reached its fundamental physical limit and the resistance and capacitance that characterize the electrical interconnections of integrated circuits severely limit their speed and power. Low-power electronics are looking for new technologies capable of replacing the von Neumann architecture, while the interconnections issue has been overcome by replacing electronic signals with photonic signals, generating optoelectronics. Using photons instead of electrons to transfer information means a significant reduction in energy consumption and at the same time an increasing in the operating frequencies.

Initially, several attempts were carried out to achieve silicon- or germanium-based optoelectronic devices able to efficiently emit light. The main advantage of the elements of group IV is their compatibility with CMOS technology as regards the materials integration and the temperatures used in the manufacturing processes. However, silicon and germanium are indirect bandgap semiconductors by nature, because they normally crystallize in the cubic phase. This means that they cannot efficiently emit light unless properly engineered. Nevertheless, all attempts made to achieve this goal produced other drawbacks that did not allow this technology to diffuse in the fast development of the semiconductor industry. For this reason, group III-V semiconductor materials have established themselves in optoelectronics.

Their main advantage is the direct band gap of some of their compounds which allows them to efficiently emit light. Furthermore, they are characterized by high electron mobility, so they can operate at high frequencies, and their band gap can be engineered by varying the stoichiometry of their ternary and quaternary compounds. However, group III-V semiconductor materials are very difficult to integrate with the silicon chip making the process extremely expensive and hard to integrate on a large scale.

As anticipated, both silicon and germanium crystallize in the cubic phase by nature, resulting to be indirect bandgap semiconductors. However, under suitable conditions, both silicon and germanium can grow in the hexagonal crystal phase. The study of their band diagrams shows that hexagonal germanium is a direct bandgap semiconductor, while hexagonal silicon remains an indirect bandgap semiconductor. Therefore, hexagonal germanium has the potential to be the CMOS compatible light source which the semiconductor industry is looking for. Nevertheless, pure hexagonal germanium shows a radiative recombination lifetime much higher than III-V group semiconductor materials. This means that this direct bandgap material is characterized by a low light emission efficiency, that cannot be competitive with III-V compounds. However, theoretical studies suggested that Ge-rich hexagonal SiGe alloys maintain the direct band gap, which can be tuned by tuning the germanium content, and show a low radiative recombination lifetime, slightly higher than III-V group semiconductor materials. For these reasons, Ge-rich hex-SiGe alloys could be the ideal candidate for silicon photonics because it can be easily integrated with CMOS technology and it is characterized by a high light emission efficiency.

Proving and realizing the growth of this novel material has been the goal of the SiLAS project, an Horizon 2020 FET-Open project, over the past 4 years (2017-2020). The results obtained from both the growth and the characterization of hex-SiGe are very promising, and will be discussed in Section 1.1. The final goal is to realize an electrically pumped SiGe nanolaser and to create a path for CMOS integration. This aim will be carried out for another 4 years (2021-2025) by the OptoSilicon project, an Horizon 2020 FET-Open project. Both the projects are managed by Eindhoven University of Technology and partnered with University of Oxford, Friedrich Schiller University Jena, Johannes Kepler University Linz, IBM Research and Technical University of Munich. The research carried out by this thesis falls between these two projects. Its goal is the electrical characterization of this novel material, as will be discussed in Section 1.2. As hex-SiGe is a novel material, its electrical, mechanical and optical properties are still largely unknown. The project is carried out in the group of Material Integration for Nanoscale Devices at IBM Research Europe. In particular, the manufacturing process is developed in the well-equipped BRNC cleanroom facility.

1.1 The SiLAS project

The aim of the SiLAS project was to investigate and grow a novel material capable of replacing III-V group semiconductor materials for on-chip and chip-to-chip communication by light in optoelectronics. The most promising material for this role is SiGe in the hexagonal crystal phase. This section describes the results obtained from the growth process of the material and from its optical characterization. In addition, the advantages of hex-SiGe which make it a suitable candidate for being CMOS compatible and efficiently emitting light are discussed.

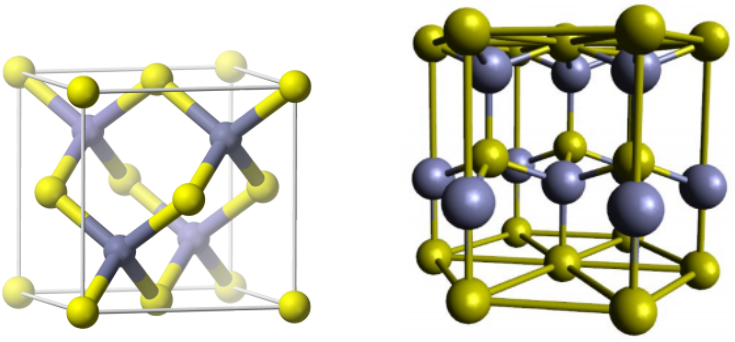
1.1.1 $Si_{1-x}Ge_x$ crystalline structure

The thermodynamically stable crystal phase of both silicon and germanium is the cubic crystalline structure, that means that this is the crystal phase these elements assume by nature. For this reason, the semiconductor industry has exploited cubic silicon for decades to make electronic devices. The cubic crystalline structure in the elemental form of silicon and germanium is also called diamond (D). The crystal phase of the materials describes the microscopic atomic arrangement that it assumes and plays a fundamental role in the definition of its electronic and optical properties, because it defines the periodic potential that acts on the electrons. In the cubic phase, silicon and germanium are both indirect bandgap semiconductors, therefore they cannot emit light efficiently if not properly engineered, but also in this case they would show disadvantages that would not allow them to be implemented as substitutes for III-V group semiconductor materials in optoelectronics. As anticipated, the hexagonal phase of these two elements is not energetically favored in nature, but under suitable growth conditions it can occur. In this case the crystalline structure of the material is called lonsdaleite (LD). Hex-Ge is a direct bandgap semiconductor, but its radiative recombination lifetime is too high to be competitive with the III-V group emission light efficiency, as will be explained in detail below.

Like silicon and germanium in their elemental forms, the SiGe compound also grows in the cubic phase by nature. The cubic phase of the SiGe compound is called zincblende (ZB) and it is depicted in Figure 1.1a. Although obtaining the hexagonal phase in this compound is extremely difficult, under suitable process conditions it is possible to achieve it. Since hexagonal Ge is a direct bandgap semiconductor, a hex-SiGe alloy with sufficient Ge content can assume a direct bandgap nature, but with a sufficiently low radiative recombination lifetime to be competitive with III-V group semiconductor materials. The hexagonal phase of the SiGe compounds is called wurtzite (WZ) and it is shown in Figure 1.1b. Achieving a high crystal quality wurtzite SiGe is the aim of the SiLAS project. The names of the four crystal phases described above are summarized in Table 1.1.

1.1.2 GaAs/SiGe core/shell epitaxial growth

Over the past decades, several methods have been tried to grow silicon and germanium in the hexagonal phase. The most promising were the vapour–liquid–solid



(a) (b)

Figure 1.1: Crystal structure schematics of **(a)** cubic (zincblende) and **(b)** hexagonal (wurtzite) group IV semiconductor compounds [1].

Table 1.1: Group IV semiconductors crystal phases.

	Cubic	Hexagonal
Elemental	Diamond (D)	Lonsdaleite (LD)
Compound	Zincblende (ZB)	Wurtzite (WZ)

(VLS) nanowire growth and the strain induced crystal transformation. The VLS method consists in the growth of nanowires by chemical vapor deposition. The crystal grows through direct adsorption of a gas phase onto a solid surface, catalyzed by a liquid phase. The strain induced crystal transformation method aims to achieve a different crystal phase from a crystalline material due to the application of strain. These methods work, but only for growing small volumes of crystalline materials. Furthermore, the crystalline quality provided by these techniques is poor and risks introducing crystalline defects into the material that could alter its electrical and optical properties.

On the other hand, a high crystalline quality can be achieved by the crystal transfer method. It consists in the transfer of the hexagonal crystal phase of a hexagonal nanowire core template to the group IV shell by epitaxial growth. This technique takes advantage of the easier growth of some materials in the hexagonal phase to transfer their crystalline structure to compounds that are thermodynamically more disadvantaged to grow in the hexagonal phase. However, it is important that the lattice mismatch between the core template and the shell is minimized. Therefore, it is necessary to select the suitable material for each shell. The material used for the growth of hexagonal Ge that best suits its lattice constant is GaAs, which is energetically more favored to grow in the hexagonal phase than Ge, while the one most suitable for the growth of hexagonal Si is GaP. It has been proven that the lattice mismatch between Ge-rich hex-SiGe alloys and hex-GaAs is low enough to allow the growth of these compounds while maintaining the same core template as for hex-Ge. A high lattice mismatch between the core and the shell would induce strain in the shell, generating lattice defects in the growing material.

The crystal transfer method is the technique implemented by Elham M. T. Fadaly et al. [2] in the context of the SiLAS project to grow Ge-rich hex-SiGe alloys. The process flow, depicted in Figure 1.2, starts by patterning gold micro-disks on a GaAs substrate by electron beam lithography. The gold is evaporated on the patterned resist, then excess metal is removed by lift-off. The Au micro-disks act as catalyst for the growth of thin wurtzite GaAs nanowires by vapour-liquid-solid method. The nanowires grow in the hexagonal phase only if the contact angle of the gold droplets is approximately of 90°. The growth of crystalline GaAs/SiGe core/shell nanowires is carried out by the metal-organic vapor phase epitaxy (MOVPE) technique. The metal-organic precursor for gallium is trimethylgallium (TMGa), while the one for arsenic is arsine (AsH3). When the growth of the wurtzite GaAs core nanowires is completed, the gold droplets are removed by wet chemical etching. Finally, the thin wurtzite GaAs nanowires act as template for epitaxial growth of hex-SiGe shell by MOVPE. The implemented gas precursors in this process are disilane (Si2H6) for Si and germane (GeH4) for Ge.

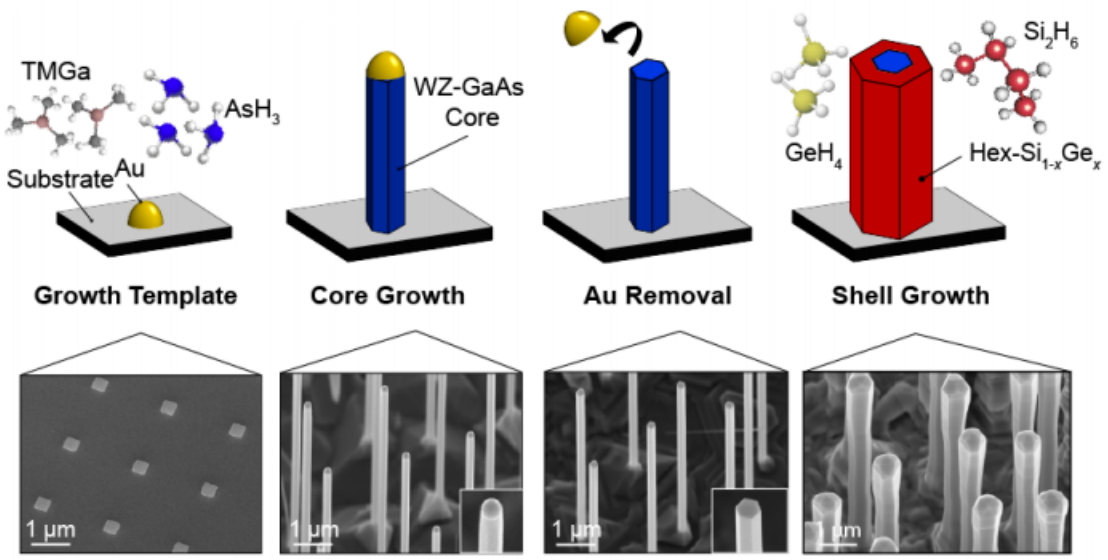
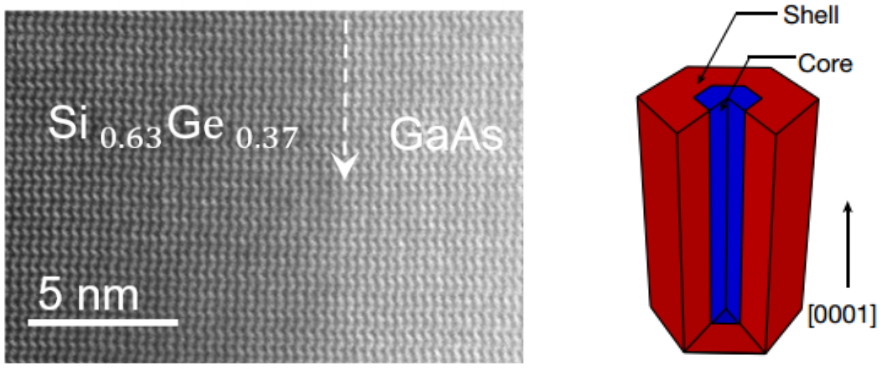


Figure 1.2: Schematic illustration of the nanowire growth process, correlated with SEM images [2].

The high crystal quality of the hex-SiGe shell is proven by TEM analysis as showed in Figure 1.3a. The final result is a thin wurtzite GaAs core surrounded by a hex-SiGe shell, as depicted in Figure 1.3b. Some As impurities coming from the GaAs substrate during thermal annealing processes may be responsible for n-type doping of the SiGe shell.

1.1.3 Tunable direct band gap and high emission efficiency

The results obtained from the optical characterization of hex-SiGe are reported in an article published in *Nature* by Elham M. T. Fadaly et al. [3] in April 2020. As anticipated in the previous chapter, both silicon and germanium in the cubic crystal phase are characterized by an indirect bandgap nature, that results in a

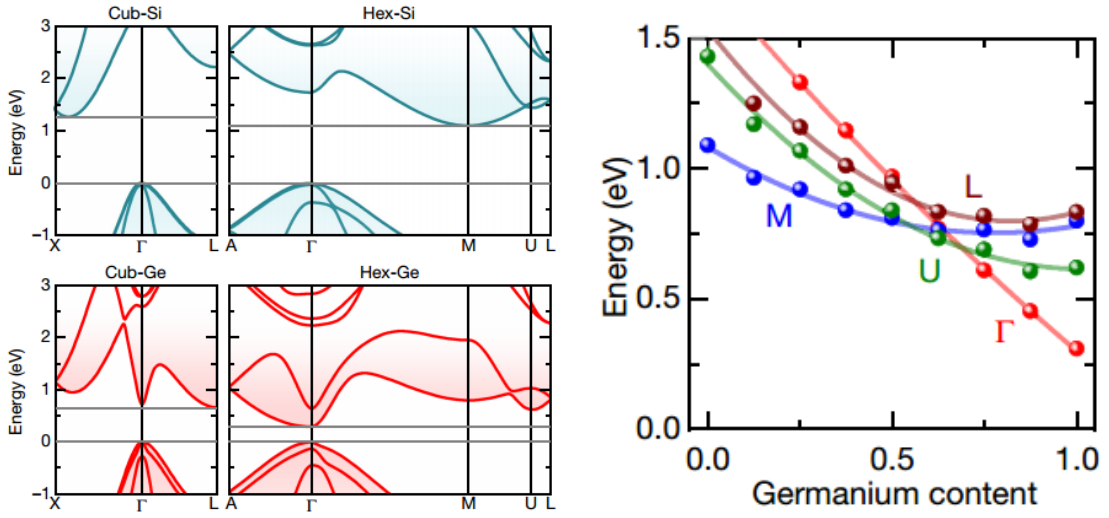


(a) (b)

Figure 1.3: **(a)** High resolution HAADF-STEM images of the crystal structure of $Si_{0.63}Ge_{0.37}$ confirming the hexagonal crystal structure grown on wurtzite GaAs nanowire cores [1]. **(b)** Schematic illustration of the hexagonal GaAs/SiGe core/shell nanowires [3].

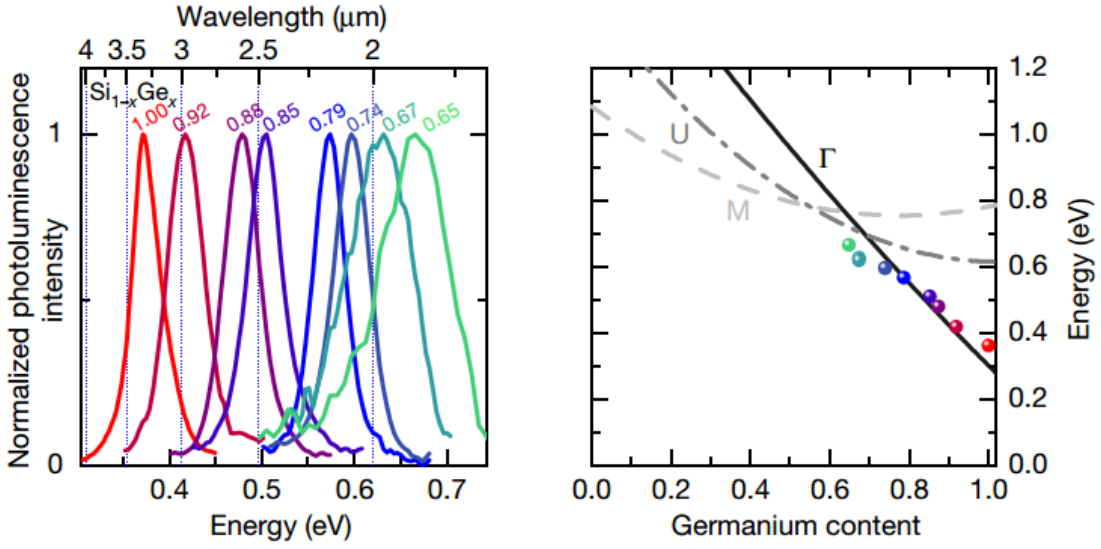
low light emission efficiency. However, these semiconductor materials can grow in the hexagonal crystal phase in particular conditions. The band structures of both cubic and hexagonal Si and Ge are reported in Figure 1.4a. As cub-Si, hex-Si is an indirect semiconductor material because the lowest conduction-band minimum is situated at the high-symmetry M-point, while the Γ-point is only a local conduction-band minimum. On the contrary, the lowest conduction-band minimum of hex-Ge is situated at the Γ-point, resulting in a direct bandgap semicondutor. This suggests that Ge-rich hex-SiGe alloys show a direct bandgap nature. Density functional theory (DFT) can be implemented to theoretically calculate the band structure of hex-SiGe alloys. The energies of the high-symmetry points in the band structure of the hex-SiGe alloys vs the germanium content are reported in Figure 1.4b. The semiconductor alloys show direct bandgap nature when the lowest conduction-band minimum is situated at the Γ-point. As it can be observed from the graph, if the germanium content exceeds 0.65, the band gap of the hex-SiGe alloys is direct. Therefore, not only Ge-rich hexagonal SiGe alloys have a direct band gap, but it is also tunable in energy, by tuning the Ge content. Theoretical predictions of DFT are experimentally proven by photoluminescence spectroscopy for different Ge contents. The energies of the direct band gaps measured by this analysis perfectly agree with the theory, as reported in Figure 1.5. The emission wavelength is tunable between 1.8 µm and 3.5 µm, that makes Ge-rich hexagonal SiGe alloys suitable for optical communications.

The wavelength tunability of hex-SiGe is not the only advantage of the alloys. Pure hexagonal germanium, despite having a direct band gap, cannot replace III-V group semiconductor materials because its radiative recombination lifetime is several orders of magnitude higher than its competitors, especially at low temperatures, resulting in a very low light emission efficiency. The calculated radiative lifetimes of hexagonal SiGe alloys with different Ge content for different temperatures are reported in Figure 1.6a. As it can be clearly seen, the higher the Ge content, the lower the radiative recombination lifetime. This suggests that a high germanium con-



(a) (b)

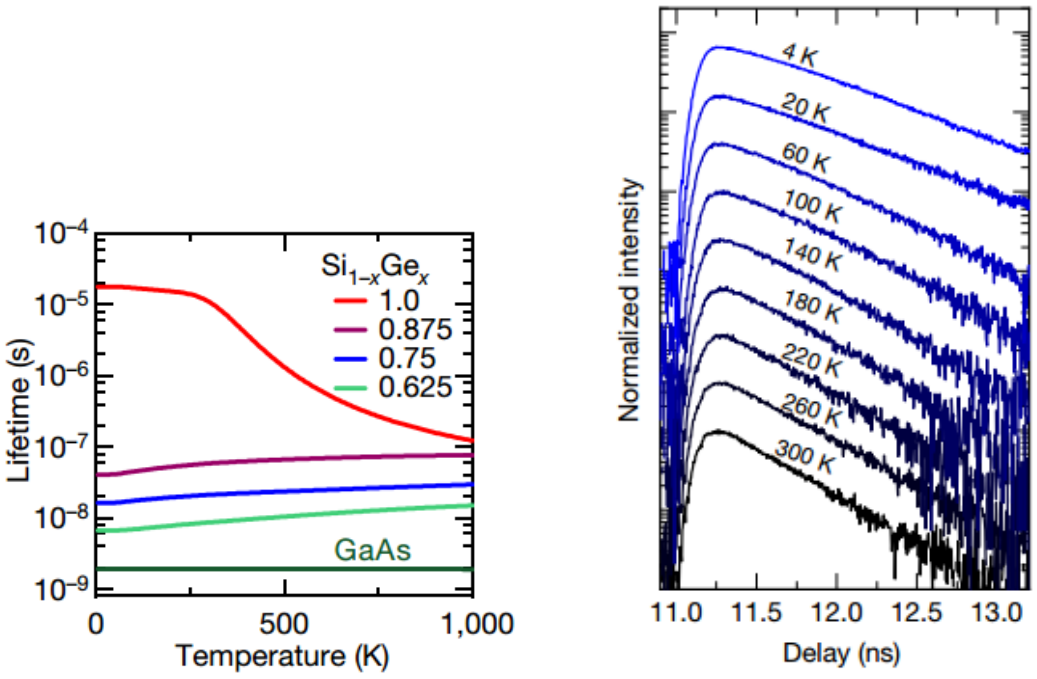
Figure 1.4: **(a)** Band structures of cub-Si, hex-Si, cub-Ge and hex-Ge based on DFT calculations [3]. **(b)** Minimum conduction-band energies for the selected high-symmetry points Γ, M, L and U as a function of the Ge content in the hex-$Si_{1-x}Ge_x$ [3].



(a) (b)

Figure 1.5: **(a)** Tunability of the photoluminescence spectra for different compositions [3]. **(b)** Comparison of the measured peak energies as a function of the Ge content with the calculated emission band minima [3].

tent results in a high light emission efficiency. The radiative lifetime of hex-SiGe with a high germanium content, but low enough that the band gap is still direct, is slightly higher than that of GaAs, an excellent III-V group light emitter. The radiative recombination lifetime of hex-$Si_{0.20}Ge_{0.80}$ has been experimentally measured by time-resolved photoluminescence spectroscopy, as shown in Figure 1.6b. This alloy shows sub-nanosecond radiative recombination lifetime even at the very low temperature of 4 K, and low temperature dependence.



(a) (b)

Figure 1.6: **(a)** Radiative recombination lifetime of different hex-$Si_{1-x}Ge_x$ compositions compared to the radiative recombination lifetime of cub-GaAs [3]. **(b)** Time-resolved photoluminescence lifetime measurements of hex-$Si_{0.20}Ge_{0.80}$ recorded at different temperatures [3].

In conclusion, the combination of the direct band gap, the wavelength tunability and the sub-nanosecond radiative recombination lifetime makes Ge-rich hexagonal SiGe alloys suitable for replacing III-V group semiconductor materials in optoelectronics. Furthermore, hex-SiGe is CMOS compatible, so it could be the best candidate for on-chip communication by light. For these reasons, the aim of the OptoSilicon project is to design and realize an electrically pumped SiGe nanolaser.

1.2 Scope of the thesis

As described in the previous sections, hex-SiGe is an excellent candidate for on-chip communication by light, because it is CMOS compatible and an efficient light emitter. However, it is a novel material, so many of its electrical, mechanical and optical properties still need to be investigated. The aim of this thesis is the electrical characterization of Ge-rich hex-SiGe alloys. As discussed in Section 1.1, SiGe compounds are epitaxially grown in the hexagonal phase by MOVPE on thin wurtzite GaAs nanowires, that act as templates. The result is a hex-GaAs core surrounded by a hex-SiGe shell in a GaAs/SiGe core/shell nanowire configuration.

To electrically characterize this semiconductor material it is first necessary to transfer the nanowires from the growth substrate to a new clean substrate. After that, the nanowires can be electrically contacted, so it is necessary to design and manufacture metal contacts. However, the hexagonal morphology of the nanowires and their thickness makes this process difficult to realize, because the surface first needs to be planarized. Then, the metal is evaporated and the process is completed by lift-off. Finally, the electrical characterization of hex-SiGe is carried out by two- and four-wire measurements. Previous attempts highlighted the difficulty in achieving ohmic contacts. This happens because, when the metal is deposited on the semiconductor material, a potential Schottky barrier arises. The potential barrier at the metal-semiconductor interface prevents electrons from flowing easily, causing a high contact resistivity. As a consequence, the power dissipation turns out to be very high. For this reason, the primary objective of this thesis is to engineer the contacts in order to achieve an ohmic behavior. Two-wire measurements will be functional to investigate the current-voltage (I-V) characteristics in order to establish whether the contact assumes an ohmic character or not. The resistivity of hex-SiGe is calculated by four-wire measurements, then the carrier concentration in the material can be estimated by that value.

Below is a brief description of the content of each chapter.

Chapter 2 deals with the fundamental theoretical concepts for understanding the following experimental chapters.

Chapter 3 describes in detail the general process flow for the design and manufacture of metal contacts on hexagonal GaAs/SiGe core/shell nanowires which will also be used in the more advanced manufacturing processes in the following chapters.

Chapter 4 reports the first two- and four-wire measurements performed on the hex-SiGe nanowires and compares the results obtained with and without planarization of the surface before evaporating the metal contacts.

Chapter 5 aims to fit the experimental data collected by I-V measurements to estimate the height of the potential Schottky barriers and lays the groundwork to overcome the Fermi level pinning issue.

Chapter 6 investigates the annealing limit temperature and time combinations that the GaAs/SiGe core/shell nanowires can tolerate before melting and deals with a possible way to obtain ohmic contacts by the diffusion of nickel into the SiGe shell.

Chapter 7 demonstrates the possibility to achieve ohmic contacts between the Ni metal contacts and the SiGe shell by phosphorus solid-state diffusion doping after selectively etching the GaAs core over the SiGe shell to avoid interference during the doping process, then the resistivity values of P-doped hex-SiGe are extrapolated by four-wire measurements.

Chapter 8 concludes the thesis analyzing the main issues encountered during the experimental work and laying the foundations for future developments of this technology.

Note to the reader The GaAs/SiGe core/shell nanowires analysed in this thesis are provided by the Eindhoven University of Technology. Their hex-SiGe shells are composed by 20% silicon and 80% germanium. In particular, two different batch of nanowires are measured: sample H06794 and sample H06793. The GaAs core thickness of both the samples measures 100 nm, while the SiGe shell thickness and the nanowires length differ. Sample H06794 has thicker shells of about 60 nm and longer nanowires of about 6 µm, while sample H06793 has thinner shells of about 40 nm and longer nanowires of about 8 µm. In the first part of the thesis nanowires from sample H06794 are used. When nanowires from sample H06793 will be used, in Chapter 7, it will be further specified.

Chapter 2

Fundamentals and methods

2.1 Metal-semiconductor junction

As anticipated in Section 1.2, the aim of this thesis is the electrical characterization of hexagonal GaAs/SiGe core/shell nanowires. It is mainly based on two- and four-wire measurements. From two-wire measurements it is possible to obtain current-voltage (I-V) characteristics, which are fundamental not only for determining the contact resistance, but also for analyzing the type of contact obtained. What determines a good contact is the quality of the interface between two materials. This does not only concern the contact area, but also the type of materials involved. A contact between two metals is more conducive to the transit of electrons from one side of the interface to the other. Unlike this, the flow of charges between a metal and a semiconductor is generally determined by drift and diffusion currents, as is the case for a p-n junction. For this reason, two types of electrical conduction can be established at the interface: ohmic contacts or Schottky contacts. The type of contact is determined by the combination of metal and semiconductor. What distinguishes ohmic contacts is the absence of space charge at the interface between metal and semiconductor. As a consequence, no voltage drop occurs at the interface. In this case, the current-voltage characteristic exhibits ohmic behavior for both voltage polarizations, both positive and negative, i.e. the I-V measurement shows a linear trend. Generally, this type of contact is obtained technologically by a high doping concentration around the contact area of the semiconductor side [4]. This results in a symmetrical current–voltage curve obeying Ohm's law [5].

2.1.1 Rectifying behavior

The ohmic behavior is easy to describe, but also difficult to achieve technologically between metal and semiconductor at the nanoscale. Generally, rectifying behavior is more likely to be observed from current-voltage measurements. This is the name of the I-V characteristic resulting from a Schottky contact. A Schottky contact behaves similarly to a p-n junction. They differ because in a p-n junction the depletion region extends to both sides, while in a metal-semiconductor junction the space charge region originates only in the semiconductor side. The metal can inject free charges

into the semiconductor, or vice versa, but the free charge density in the metal is high enough to reduce the space charge region to zero. The rectifying behavior can prevail on the ohmic behavior both for n-type and p-type metal-semiconductor junctions. In the first case, the Schottky contact is observed when the semiconductor electron affinity is lower than the metal work function, while the latter case generates a rectifying behavior if the sum of the semiconductor band gap and electron affinity is higher than the metal work function [6]. Depending on the type of semiconductor, electrons or holes are injected into the metal, respectively. The resulting depletion region is not electrically neutral and the charge of one type is prevalent. As a consequence, a potential barrier is formed at the interface [4]. Electrons and holes are subjected to this potential barrier, called Schottky barrier, which is responsible for the rectifying behavior at the metal-semiconductor junction. To overcome this potential barrier, free charges need an additional voltage drop, such as the turn-on voltage of a diode. The ohmic character is obtained when this barrier tends to zero, that is when the work function of the metal and the electronic affinity of the semiconductor coincide. Therefore, since the goal is to obtain a good metal-semiconductor contact for the electrical characterization of the nanowires, the Schottky barrier must be reduced to zero, to avoid that the space charge region introduces a large parasitic resistance. The parasitic resistance is due to the additional potential energy that the charges need to overcome the barrier. If the material is used to implement electrical devices, this side effect could cause undesired power consumption. In low power electronics this consumption would prevent such devices from being used.

2.1.2 Schottky barrier height

The purpose of this thesis is to analyze the current-voltage characteristics obtained from two-wire measurements on electrically contacted nanowires. Since the nanowires are composed of semiconductor material, each metallic contact manufactured on them generates a metal-semiconductor junction, i.e. a Schottky contact, if they are not properly processed before evaporating the metal. Each nanowire will be contacted by four wires, as explained in detail in Chapter 3, therefore the two-wire measurements will involve some pairs of contacts among the four available. This means that for each measurement, two Schottky contacts are involved, not just one, arranged in a metal-semiconductor-metal (MSM) configuration. Also, they are connected back to back. Thus, the system can be described by a pair of diodes connected back to back with a resistance in series between the two representing the resistance of the portion of nanowire, as depicted in Figure 2.1.

Figure 2.1: Two Schottky barriers connected back-to-back with series resistance [4].

If the second contact was ohmic, it would be possible to study a single Schottky

contact, and then analyze the parameters that characterize it, simply by characterizing the charge transport process with the equation that describes a Schottky diode. However, in this thesis the objective is to analyze the Schottky barriers to understand how to obtain ohmic contacts, therefore the problem of the back to back connected Schottky diodes cannot be overcome before this study. In the equation that describes the transport of charges through the nanowire and the two contacts, it is therefore necessary to take into account both the junctions at the same time. The I-V characteristics obtained from the two-wire measurements will reflect this trend. Furthermore, considering the two barriers characterized by the same parameters would be an error. The variability connected to the manufacturing process makes the height of the two Schottky barriers and the other related parameters to be different from each other. This difference is related to the interfacial chemistry and the local defects [6]. In this case the system can be described as back to back connected asymmetric Schottky diodes.

The electrical transport mechanism that regulates the flow of free charges at each interface can be described with thermal emission, as in a common Schottky diode. This charge transport is so called because the electrons that take part in the current flow cross the potential barrier by means of the thermal energy. The metal-semiconductor junction before physical contact can be described by Figure 2.2. This figure shows the typical band diagram of a metal and an n-type semiconductor before they are brought into contact. From now on, only the case of an n-type semiconductor will be treated since SiGe nanowires are characterized by a predominance of donors. However, similar considerations can be developed for a p-type semiconductor.

According to the Schottky–Mott rule, the SB height can be defined as [7]:

$$\phi_{SB} = \phi_m - \chi_s \tag{2.1}$$

where ϕ_{SB} is the SB height for electrons injection, ϕ_m is the metal work function and χ_s is the semiconductor electron affinity, as reported in Figure 2.2.

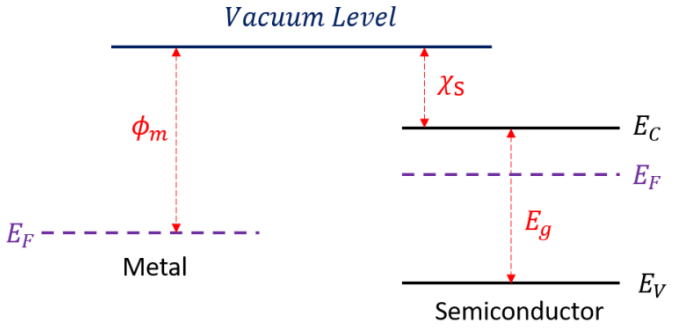


Figure 2.2: Typical band diagram of a metal and an n-type semiconductor before they are brought into contact [6].

When no external voltage is applied to the back to back connected asymmetric Schottky diodes, the system is in equilibrium, so the energy band diagram can be depicted by Figure 2.3a. Considering that the two Schottky junctions are back to back connected, when a voltage is applied to one of the two sides of the system,

one of the two diodes is forward biased, while the other one is reverse biased. The resulting energy band diagram is shown in Figure 2.3b.

As previously mentioned, when the Schottky barrier width is much smaller than the mean free path of an electron, the current transfer through the interface is usually described by the thermionic emission [5]:

$$I_1 = I_{s1}\left[e^{\frac{qV_1}{kT}} - 1\right] \tag{2.2}$$

$$I_2 = -I_{s2}\left[e^{-\frac{qV_2}{kT}} - 1\right] \tag{2.3}$$

where $V_{1,2}$, $I_{1,2}$ and $I_{s1,2}$ are the voltage drops, the currents and the reverse saturation currents at the contacts 1 and 2, respectively, q is the electron charge, k is the Boltzmann constant and T is the temperature. The sum of the voltage drops at the two contacts V_1 and V_2 and on the nanowire resistance will be indicated by V, while the total current flowing through the two junctions equal to I_1 and I_2 will be pointed out as I. When a voltage is applied to the system, the total current is limited by the reverse saturation current of the reverse biased junction.

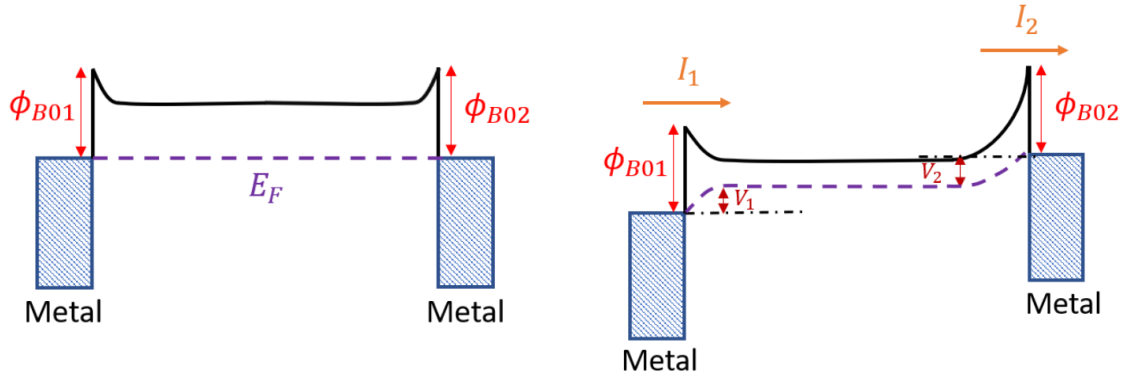
The reverse saturation current assumes the same expression like in a common Schottky diode:

$$I_{s1,s2} = S_{1,2}A_R T^2 \exp\left(-\frac{\phi_{B1,2}}{kT}\right) \tag{2.4}$$

where $S_{1,2}$ and $\phi_{B1,2}$ are the contact areas and the Schottky barrier heights at the contacts 1 and 2, respectively, while A_R is the effective Richardson constant [8]:

$$A_R = \frac{4\pi m k^2 q}{h^3} = 1.20173 \times 10^6 \text{ A m}^{-2} \text{ K}^{-2} \tag{2.5}$$

where m is the mass of an electron and h is Planck's constant.



(a) (b)

Figure 2.3: Energy diagram of a semiconductor with two Schottky junctions at the contacts for **(a)** equilibrium condition and **(b)** when an external potential is applied to the left contact [6].

Taking into account the voltage drop on the nanowire resistance, the total voltage drop assumes the following expression [4]:

$$V = V_1 + V_2 + RI \tag{2.6}$$

and substituting V_1 and V_2 with the expressions for the inverse saturation currents reported in Equation 2.2 and Equation 2.3, one obtains:

$$V = \frac{kT}{q} \ln\left(\frac{I}{I_{01}} + 1\right) - \frac{kT}{q} \ln\left(-\frac{I}{I_{02}} + 1\right) + RI \tag{2.7}$$

that is the closed-form equation for the V-I characteristic. However, the goal is to find a valid expression for the I-V characteristics, in order to fit the curves and obtain accurate estimates of the unknown parameters, such as the height of the Schottky barriers. A closed-form expression for $I = I(V)$ can only be obtained if the resistance of the nanowire is neglected. According to numerical simulations carried out by Zuo Wang et al. [5], the effect of the series resistance on the I-V characteristics is relevant only if the potential barriers are very low. From the electrical characterization measurements and numerical simulations it will be noticed that the Schottky barriers are high enough to make the effect of the potential drop on the fitted curves negligible. For this reason, the resistance of the nanowire will be neglected in this thesis, in order to find a closed-form expression for the I-V characteristics.

Considering that:

$$I = I_1 = I_2 \tag{2.8}$$

and the approximate expression for the total voltage drop:

$$V = V_1 + V_2 \tag{2.9}$$

after some calculations, reported by A. Grillo [6] and omitted in this discussion for the sake of conciseness, one can find:

$$I = \frac{2I_{s1}I_{s2}\sinh\left(\frac{qV}{2kT}\right)}{\left(I_{s1}e^{\frac{qV}{2kT}} + I_{s2}e^{-\frac{qV}{2kT}}\right)} \tag{2.10}$$

However, this expression does not take into account the non-ideality factors at the junctions that can affect the thermionic emission. By numerically simulating this equation, the trend shown in Figure 2.4a is obtained, where the current saturates due to the reverse saturation current of the reverse biased junction. This concavity around the origin of the axes cannot be compared to the measured I-V characteristics, as it will be discussed in Section 5.2. To describe the correct trend of the measured I-V curves, it is necessary to introduce the ideality factors $n_{1,2}$ in the exponential term of the reverse saturation currents in Equation 2.4. This factor includes in the equation all the non-idealities that make the SBH dependent on the voltage drop applied at the junctions [6]:

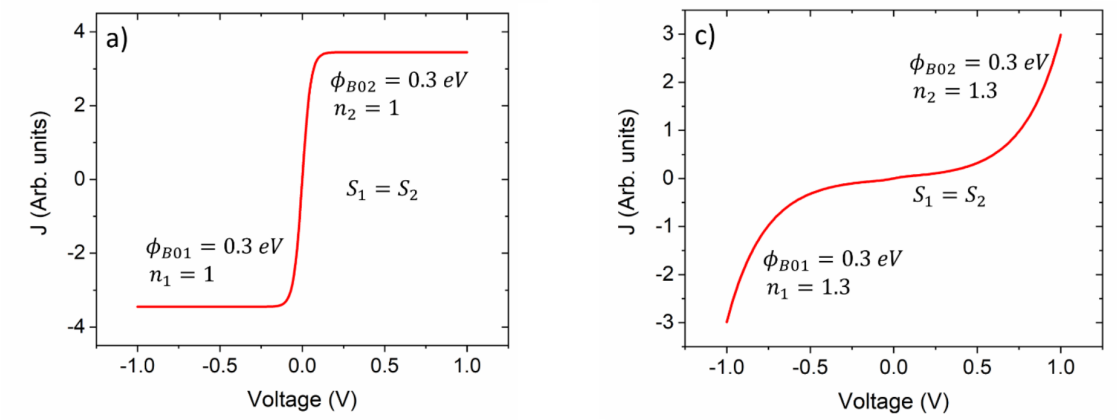
$$\phi_{B1,B2}(V) = \phi_{B01,B02} \pm eV_{1,2}\left(1 - \frac{1}{n_{1,2}}\right) \tag{2.11}$$

where $\phi_{B01,B02}$ are the ideal SBHs at zero bias. The ideality factors are defined as:

$$\frac{1}{n_{1,2}} = 1 \pm \frac{\partial \phi_{B1,B2}}{e \partial V_{1,2}} \tag{2.12}$$

so, they can assume values in the range $[1, +\infty)$, where $n_{1,2} = 1$ represents the ideal case. Non-idealities can be introduced by organic impurities, crystal defects, thin oxidation layers or image-force barrier lowering.

As mentioned by S. M. Sze [9], in a metal-semiconductor rectifying junction, the barrier height is a function of the applied bias because a charge carrier in the semiconductor near the junction experiences two forces, one arising from the field in the space-charge depletion layer, as previously explained, the other from the image charge induced in the metal, which is the image-force barrier lowering effect. This effect consists in the accumulation of image charges in the metal as carriers approach the metal-semiconductor interface, which causes the potential barrier to get lower. This results in a barrier height dependent on the applied voltage (Equation 2.11), because the higher the external voltage, the more intensive the accumulation of image charges at the interface. To conclude, when the SBH depends on the external applied voltage, the I-V characteristics assume the concavity depicted in Figure 2.4b, which faithfully reproduces the trend of the I-V curves obtained from two-wire measurements.



(a) (b)

Figure 2.4: Numerical simulation of Equation 2.10 describing the thermionic emission in two back-to-back connected Schottky diodes. **(a)** I-V characteristic for metal-semiconductor junctions with the same barrier height, $\phi_{B01} = \phi_{B02} = 0.3\,\text{eV}$, the same junction area $S_1 = S_2$ and perfect ideality ($n_1 = n_2 = 1$). The current saturates to the reverse saturation current of the reverse-biased diode. **(b)** I-V characteristic for $\phi_{B01} = \phi_{B02} = 0.3\,\text{eV}$, areas $S_1 = S_2$ and ideality factors $n_1 = n_2 = 1.3$. The ideality factor is due to the image-force barrier lowering effect [6].

2.1.3 Fermi level pinning

In the previous section, the Schottky–Mott rule has been reported in Equation 2.1. However, this rule describes an ideal case, because in most metal-semiconductor

junctions the height of the Schottky barrier does not depend on the metal work function.

Generally, a metal-semiconductor Schottky contact reaches equilibrium by migrating electrons from the semiconductor to the metal. This flow leaves ionized donors behind that produce a potential barrier that opposes the further migration of electrons. However, this happens in an ideal Schottky contact.

On the contrary, the presence of a high density of surface states at the metal-semiconductor interface, with energies within the semiconductor band gap, can trap a large amount of charges. This happens because, generally, most of the interface states are located below the Fermi level, so they have a high probability to be filled by electrons. When the contact is formed and the band bending occurs, some of the surface states that were originally filled by electrons get pushed up above the Fermi level. For this reason, they will probably release electrons which will migrate in the metal side, considering that the metal has lower energy. This electrons contribute to achieve thermal equilibrium. If the density of surface state is very high, the amount of electrons generated by their emptying is comparable or greater than the electrons migrating from the conduction band. In the latter case the electrons migrating from the surface states to the metal could be enough to reach equilibrium. This means that, irrespective of the doping density, the same equilibrium state will always be reached, where the Fermi level position is determined mainly by the surface states energies. So, in this situation, the Fermi level is fixed to the energies where the surface states density peaks. This phenomenon is called Fermi level pinning and it is detrimental for metal-semiconductor contacts. When it occurs, the Schottky barrier height does not depend on the metal work function anymore, so changing metal is not sufficient to obtain ohmic contacts. The band diagram of the current situation is shown in Figure 2.5.

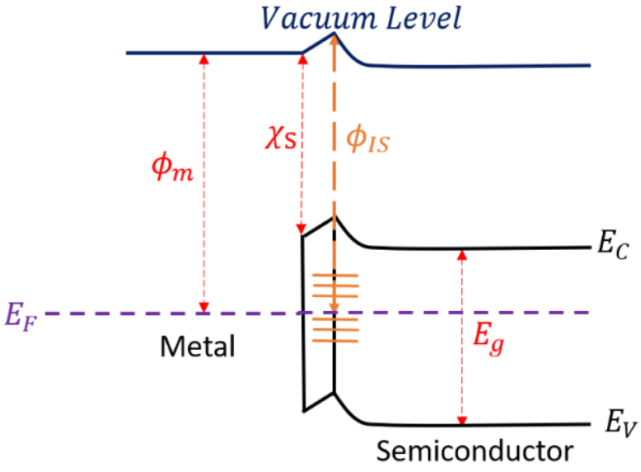


Figure 2.5: Band diagram of a metal-semiconductor junction where a high-density of interface states occurs. The Fermi level is pinned at the semiconductor interface states energies, ϕ_{IS}, and the SB height is independent of the metal work function [6].

When FLP occurs, the expression for the SBH expressed in Equation 2.1 is replaced

by [6]:

$$\phi_{SB} = (S \cdot \phi_m - \chi_s) + (1 - S)\phi_{IS} \tag{2.13}$$

where:

$$S = \frac{\partial \phi_{SB}}{\partial \phi_M} \tag{2.14}$$

is the Schottky pinning factor. It can assume values in the range $[0, 1]$. $S = 0$ means that the SBH is independent of the metal work function.

2.2 Transfer length method

As explained in Section 2.1, a Schottky barrier at the metal-semiconductor interface introduces a high contact resistance, which consequently causes high power consumption. This is due to the potential barrier generated by the space charge region in the semiconductor side. On the contrary, if this barrier is negligible or if the junction has been engineered by heavy doping, an ohmic contact can be established. However, an ohmic contact does not necessarily make the contact resistance negligible. In low-power electronics it is necessary to minimize every possible power consumption source. For this reason, it is useful to measure the contact resistance in order to minimize it.

In four-point measurements, the contact resistance of the device is negligible because it is bypassed by the two inner probes, which are crossed by an almost zero current. To measure the contact resistance it is instead necessary to perform two-wire measurements. An alternative solution to obtain more accurate measurements is to use four probes, but also including contact resistances. In this way, the contact resistance between the probes and the metal tracks is neglected, but the metal-semiconductor contact resistances between the device and the metal tracks are taken into account.

2.2.1 Contact resistance

Considering the device structure depicted in Figure 2.6 and assuming ohmic contacts at the metal-semiconductor junctions, the resistance between the points A and B can be divided into three different components: the resistance of the metallic conductor Rm, the contact resistances Rc, and the semiconductor resistance $Rsemi$. Thus, the total resistance can be written as:

$$R_T = 2R_m + 2R_c + R_{\text{semi}} \tag{2.15}$$

The contact resistances and the semiconductor resistance are generally much higher than the metal resistance, that is a good conductor, so Rm can be neglected without committing a large relative error.

Neglecting the metal resistance and writing the semiconductor resistance in terms of its sheet resistance:

$$R_{semi} = R_S \frac{L}{W} \tag{2.16}$$

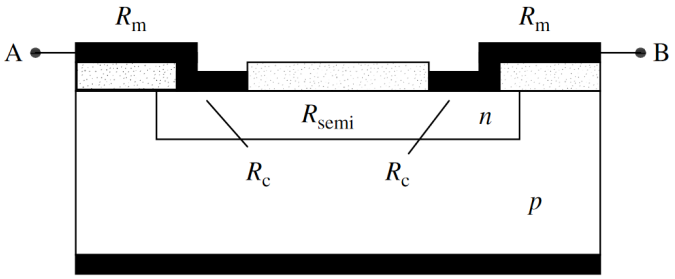


Figure 2.6: A schematic diagram showing two contacts to a diffused semiconductor layer, with the metal resistance, the contact resistances and the semiconductor resistance indicated [7].

the total resistance can be expressed as:

$$R_T = \frac{R_S}{W} L + 2R_C \tag{2.17}$$

This is the equation that describes a straight line as a function of the semiconductor's length. It is characterized by a slope of $\frac{R_S}{W}$ and intersects the y-axis at $2R_C$, in the limit of a zero-length semiconductor, as shown in Figure 2.7. This allows to extrapolate the contact resistance from simple two-wire measurements. It is sufficient to manufacture pairs of contacts on the semiconductor at known and different distances, keeping all the other parameters the same, such as the contacts width W and the contacts area A_C, as depicted in Figure 2.8. Then, the total resistance values of each pair of contacts can be measured and plotted in the graph. By a linear fit of the measured data, the straight line is generated and the unknown parameters can be extrapolated. In this way, not only the metal-semiconductor contact resistance R_C is obtained, but also the sheet resistance R_S of the semiconductor.

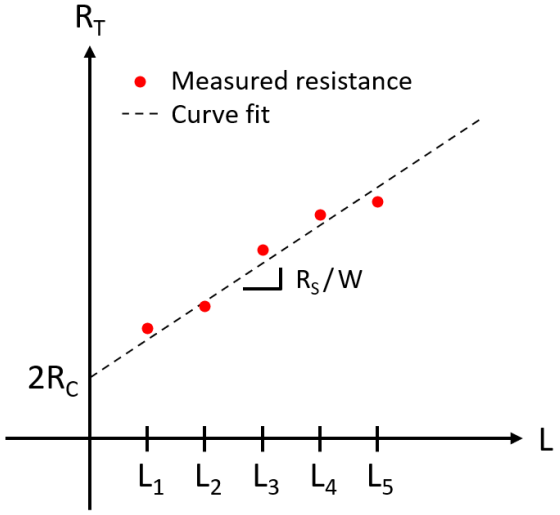


Figure 2.7: Total resistance as a function of the semiconductor's length. The contacts resistance can be extrapolated from the intersection of the fitted line with the y-axis, while the slope of the line provides the semiconductor's sheet resistance.

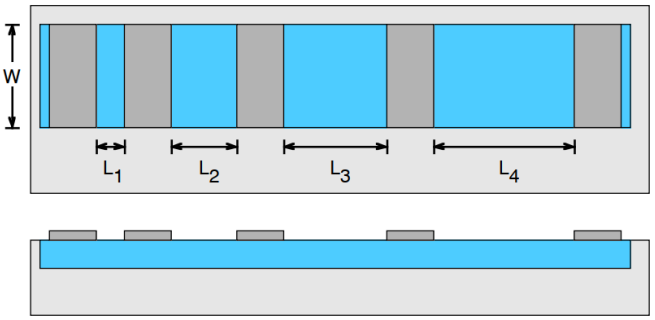


Figure 2.8: Typical arrangement for a TLM test pattern. An array of contacts is manufactured over the semiconductor region. The contacts are placed at different lengths, while keeping the width and the contacts area the same. Resistance measurements between each pair of contacts can be used to construct the TLM graph.

2.2.2 Contact resistivity

From contact resistance measurements it is possible to obtain an estimate of the power dissipated due to the metal-semiconductor interface, but it does not provide precise information on the quality of the contact. Therefore, in order to compare the contact quality with other materials or with different contact areas, it is useful to calculate the contact resistivity from the resistance values.

Contact resistance is defined as:

$$R_C = \rho' \frac{\Delta x}{A_C} \tag{2.18}$$

where Δx is a small region around the contact interface and ρ' is the resistivity associated to the volume defined by $A_C \cdot \Delta x$, as shown in Figure 2.9. However, the contact resistivity is reduced to an infinitesimal distance from the contact interface, that means:

$$\rho_C = \lim_{\Delta x \to 0} (\rho' \Delta x) = R_C A_C \tag{2.19}$$

thus its unit of measurement is $\Omega \cdot \mathrm{m}^2$.

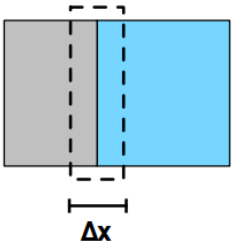


Figure 2.9: Schematic of a small region around the contact. The definition of contact resistivity assumes that $\Delta x \to 0$.

This simplified description is based on the assumption that the current flows perpendicularly to the interface between the metal and the semiconductor and uniformly

over the entire contact area. However, the situation is different if the contacts are placed above the planar semiconductor, because the current flow is no more uniform over the entire contact area, so this results in $A_C \neq W \cdot L$. The current flow is maximum at the inner edge of the contact, as depicted in Figure 2.10, while it decays nearly exponentially with the distance when it moves away from the inner edge: this phenomena is called *current crowding*. The current is reduced to $1/e$ at the characteristic length L_C, also said transfer length [7]:

$$L_T = \sqrt{\frac{\rho_C}{R_S}} \tag{2.20}$$

The transfer length can be thought of as that distance over which most of the current transfers from the semiconductor into the metal or from the metal into the semiconductor. This parameter gives the name to the adopted method since it is called *transfer length method*.

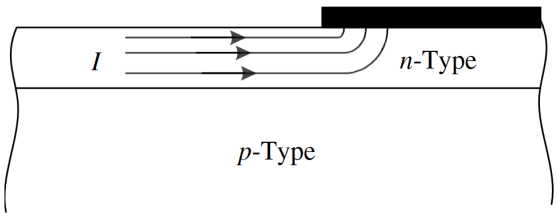


Figure 2.10: Current crowding phenomena. The current flow is maximum at the inner edge of the contact, while it decays nearly exponentially with the distance from there.

Thus, the effective contact area turns out to be $A_C = W \cdot L_T$ and from Equation 2.19 and Equation 2.20 the contact resistance can be rewritten as:

$$R_C = \frac{\rho_C}{L_T W} = \frac{R_S L_T}{W} \tag{2.21}$$

Finally, the total resistance results to be:

$$R_T = R_{semi} + 2R_C = R_S \frac{L}{W} + 2\frac{R_S L_T}{W} = \frac{R_S}{W}(L + 2L_T) \tag{2.22}$$

The equation for the total resistance written in this form suggests that the fitting line intersects the x-axis at a distance equal to $-2L_T$ from the origin, as reported in Figure 2.11.

To sum up, the transfer length method consists in the manufacturing of an array of metal contacts on a planar semiconductor. The TLM graph can be constructed by fitting the total resistance values measured on couples of contacts at different distances. If the width and the distances of the contacts are known, it is straightforward to extrapolate the other parameters from the graph. The sheet resistance R_S is obtained by the slope of the fitting line, the contact resistance R_C is extrapolated from the vertical intercept, while the transfer length L_T from the horizontal intercept. Since all these parameters are known, the contact resistivity can be calculated:

$$\rho_C = R_C L_T W \tag{2.23}$$

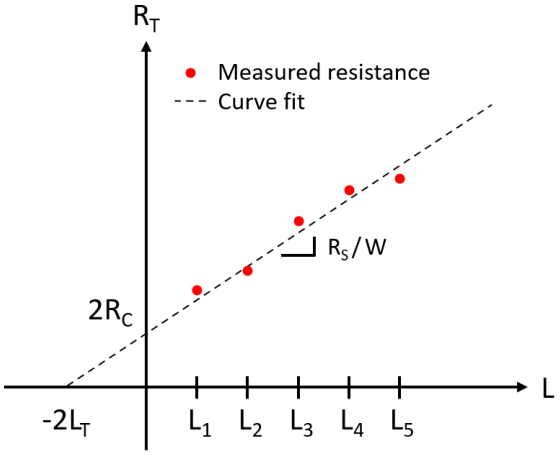
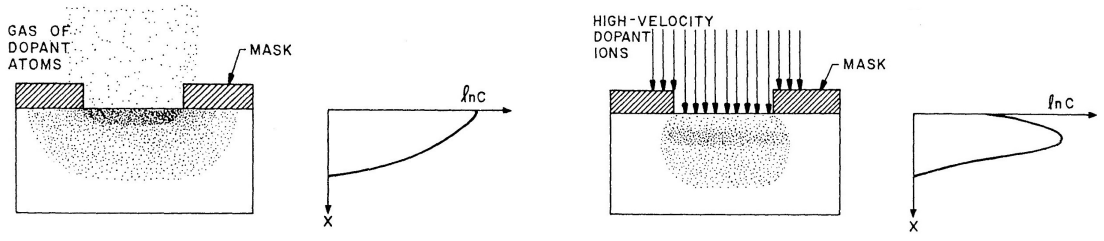


Figure 2.11: Total resistance as a function of the semiconductor's length. The horizontal intercept provides the transfer length.

2.3 Doping by diffusion

A key aspect of semiconductors is the possibility of modulating their electrical and optical properties by intentionally introducing a controlled amount of impurities, the dopants. Two main techniques exist for semiconductors doping: diffusion and ion implantation. They are implemented according to the doping profile that one wants to achieve. Generally, diffusion is more suitable for deep doping profiles, while ion implantation is implemented to achieve shallow junctions. Also, the concentration peak of dopants resulting from diffusion is generally at the surface, while ion implantation allows to achieve deeper concentration peaks, as shown in Figure 2.12. Then, the temperature required for dopants diffusion is higher than the one needed to recover the crystalline structure by annealing after ion implantation. Furthermore, doping by diffusion can be performed according to two different methods: vapor-phase and solid-state diffusion. The difference is not only in the implemented phase of the dopants, but also in the resulting doping profiles, because the two mechanism are regulated by different boundary conditions. However, in both cases, the doping concentration decreases from the surface to the bulk of the semiconductor and the diffusion time and temperature are key parameters for the resulting doping distribution.



(a) (b)

Figure 2.12: Doping profiles resulting from **(a)** diffusion and **(b)** ion implantation [10].

Dopants diffusion is induced by a concentration gradient. The impurities randomly move from a region of higher concentration to a region of lower concentration. This phenomenon is influenced by different parameters, such as temperature, concentration gradient, type of dopant and substrate's crystalline structure. Dopants can diffuse through the crystalline lattice of the substrate until a concentration gradient exists or the temperature is high enough to provide the sufficient energy for doping diffusion. The most common atomic diffusion mechanisms in a crystal lattice are the vacancy-mediated and the interstitial-assisted diffusion mechanisms. If the temperature of the crystalline structure is sufficiently high, the atoms of the lattice can acquire enough energy to leave the crystal site creating a vacancy. As a consequence, there is a consistent probability that the diffusing impurities start to occupy that free space: in this case the diffusion mechanism is said to be vacancy-mediated, as illustrated in Figure 2.13a. Otherwise, if the impurity atoms move in-between the atoms of the crystal lattice, the phenomenon is called interstitial-assisted diffusion mechanism, as pictured in Figure 2.13b. Generally, vacancy-mediated diffusion is slower than interstitial-assisted diffusion since the concentration of vacancies is low.

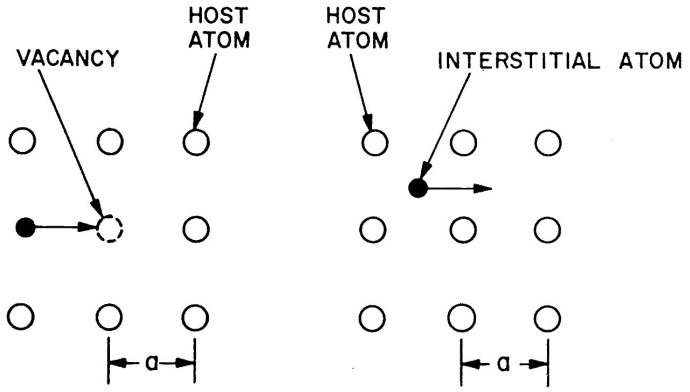


Figure 2.13: Illustration of the dopants diffusion mechanisms through the crystal lattice atoms: **(a)** vacancy-mediated and **(b)** interstitial-assisted diffusion mechanisms [10].

The flux of dopants diffusing through the crystal lattice is related to the concentration gradient by the diffusion coefficient, also said diffusivity, according to Fick's First Law of diffusion:

$$F = -D\frac{\partial C}{\partial x} \tag{2.24}$$

where D is the diffusion coefficient, C is the dopant concentration, and x is the penetration distance. As anticipated before, the driving force of diffusion is the dopant concentration gradient. The negative sign means that the dopants tend to diffuse from a region of higher concentration to a region of lower concentration.

Furthermore, in the absence of a dopant source, the law of conservation of matter, which relates the time derivative of the dopant concentration with the gradient of the flux, must hold:

$$\frac{\partial C}{\partial t} = -\frac{\partial F}{\partial x} = \frac{\partial}{\partial x}\left(D\frac{\partial C}{\partial x}\right) \tag{2.25}$$

This equation is referred to as Fick's Second Law of diffusion:

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} \tag{2.26}$$

The diffusion coefficient is not a constant, but it is function of the temperature, as follows:

$$D = D_0 e^{-\frac{E_a}{kT}} \tag{2.27}$$

where D_0 denotes the diffusion coefficient extrapolated for infinite temperature and E_a stands for the Arrhenius activation energy.

The activation energies for vacancy diffusion are generally higher than for interstitial diffusion because, for interstitial diffusion, E_a is related to the energy required to move a dopant atom from one interstitial site to another, while, for vacancy diffusion, E_a is related to the sum of the energies required for the formation of vacancies in the crystal lattice and for the occupation of the sites by the dopant atoms. This is the reason why vacancy diffusion is slower than interstitial diffusion, because a higher activation energy results in a lower diffusion coefficient, that means a slower diffusion process.

The doping profile resulting from the Fick's Second Law is defined by the initial and boundary conditions. Two different situations can occur: the concentration of dopants at the surface is kept constant or the total dose of dopants that can diffuse into the substrate is fixed. The first situation is generally related to the vapor-phase diffusion, because the concentration of dopant atoms in the gas is kept constant and the impurities continue to diffuse into the substrate without decreasing of the surface concentration. This means that the longer the time the higher the diffused dose. On the other hand, solid-state diffusion is generally governed by the second situation, because a fixed amount of dopants is deposited on the substrate and is subsequently diffused into the bulk by thermal annealing.

Constant surface concentration

To find a solution to the Fick's Second Law when the dopant concentration at the surface is kept constant, it is necessary to define one initial condition and two boundary conditions. The initial condition states that the dopant concentration into the substrate is initially zero:

$$\mathrm{C(x, 0)} = 0 \quad \mathrm{x} > 0 \tag{2.28}$$

Then, a general boundary condition that states that at infinite depth the dopant concentration is always zero must be imposed:

$$\mathrm{C}(\infty, \mathrm{t}) = 0 \quad \forall \mathrm{t} \tag{2.29}$$

Finally, it is necessary to define a boundary condition that takes into account that the dopant concentration at the surface is constant at every time:

$$\mathrm{C}(0, \mathrm{t}) = \mathrm{C}_s \quad \forall \mathrm{t} \tag{2.30}$$

where C_s is the surface concentration.

The solution of the differential equation that satisfies the initial and boundary conditions involves the complementary error function:

$$C(x,t) = C_s \operatorname{erfc}\left\{\frac{x}{2\sqrt{Dt}}\right\} \tag{2.31}$$

where $\sqrt{Dt}$ is the diffusion length.

The resulting doping profile is exhibited in Figure 2.14a. A longer time or a higher diffusion coefficient results in a deeper diffusion. The maximum dopant concentration is located at the surface and it is constant with time. To obtain the total dose of diffused dopants it is sufficient to integrate the doping distribution over the entire depth:

$$Q(t) = \int_0^\infty C(x,t)dx = 2C_s\sqrt{\frac{Dt}{\pi}} \tag{2.32}$$

Constant dose

When the total amount of dopants that can diffuse into the substrate is fixed, the initial condition reported in Equation 2.28 and the boundary condition reported in Equation 2.29 are still valid. However, it is necessary to define a new boundary condition that takes into account that the total amount of dopants is constant:

$$\int_0^\infty C(x,t)dx = S \tag{2.33}$$

where S is the total amount of dopants per unit area.

Solving the Fick's Second Law differential equation according to the initial e boundary conditions, one obtains:

$$C(x,t) = \frac{S}{\sqrt{\pi Dt}} \exp\left\{-\left(\frac{x}{2\sqrt{Dt}}\right)^2\right\} \tag{2.34}$$

that is a Gaussian distribution.

The resulting doping profile is showed in Figure 2.14b. A longer time or a higher diffusion coefficient results in a deeper diffusion, as in the previous case, and the maximum dopant concentration is still at the surface. However, the surface dopant concentration is no more constant with time:

$$C_s(t) = \frac{S}{\sqrt{\pi Dt}} \tag{2.35}$$

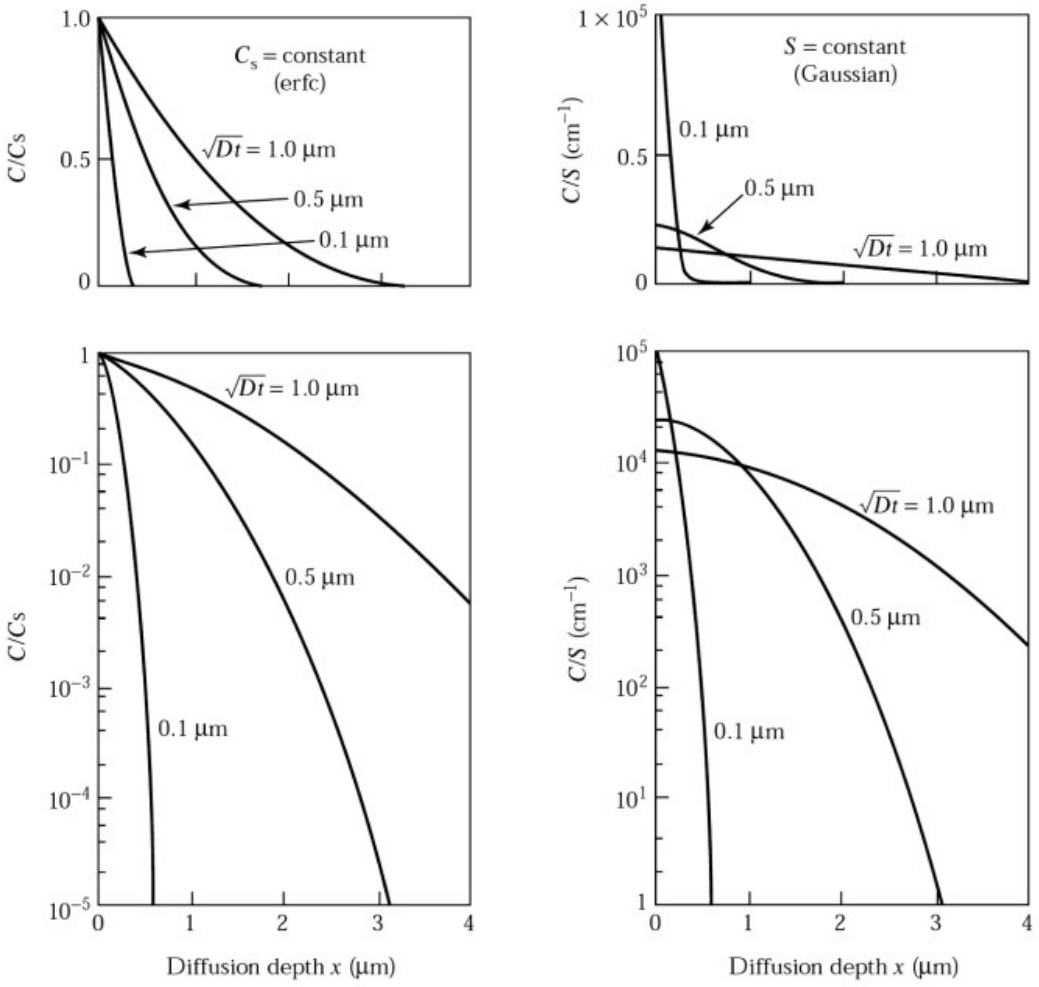


Figure 2.14: Diffusion profiles on linear and logarithmic scales for **(a)** normalized complementary error function and **(b)** normalized Gaussian function versus distance for successive diffusion times [10].

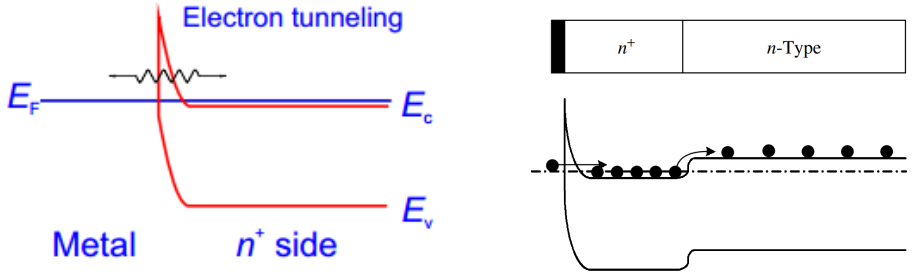
2.3.1 Ohmic contacts by n+ doping

The main purpose to implement doping by solid-state diffusion in this thesis is to establish ohmic contacts. Doping can influence the contacts behavior by reducing the depletion region in the semiconductor. This action makes a positive contribution even if the Fermi level is pinned to the energies where the surface states density peaks. This consequence cannot be taken into account by the Schottky theory as discussed in Section 2.1, because it neglects the quantum tunnel effect. However, the tunnel effect can highly enhance the electrons flow through the metal-semiconductor interface. The thinner the energy barrier the more the tunnel crossing of the barrier is favoured. Increasing the semiconductor doping level makes the barrier thinner:

$$x_d = \sqrt{\frac{2\varepsilon_s}{qN_d}V_{bi}} \tag{2.36}$$

where x_d is the depletion region width, ε_s is the dielectric constant of the semiconductor, q is the elementary electron charge, N_d is the donors concentration and V_{bi} is the built-in potential.

As a consequence, increasing the semiconductor doping level, the tunnel effect is improved and the contact behavior becomes ohmic, as depicted in Figure 2.15.



(a) (b)

Figure 2.15: Band diagram of a highly doped metal-semiconductor junction. The higher the doping concentration, the thinner the depletion region, the thinner the potential barrier. A thinner barrier enhances electron tunneling, generating ohmic contacts [7].

2.4 Experimental techniques

This section briefly describes the physical principles governing the experimental techniques implemented in this thesis, from fabrication to characterization, indicating the tools used. The parameters set on each instrument are described in the following chapters each time they are adopted.

2.4.1 Fabrication techniques

Reactive ion etching

Reactive-ion etching (RIE) is a dry etching technique, that means the etchant comes from a gas source. In particular, the name of this technique suggests that the implemented gas source is a plasma, which can remove material from a substrate by chemical reactions. The plasma is composed by reactive ions or free radical species, generated by electron bombardment. The electrons are accelerated by an electromagnetic field generated by a parallel plate capacitor. It consists of two parallel electrodes in a low pressure chamber, one of them is grounded, while the other one is connected to a RF power supply. The RF power supply provides the plasma generation by a cascading process, while the DC biased applied between the two electrodes is responsible for the directionality of etching, because the ions are accelerated towards the wafer platter.

Compared to plasma etching, reactive-ion etching provides higher anisotropy because of the directionality of the ions bombardment. This means that the plasma does not only etch the target by chemical reactions, but also by physical bombardment. The DC bias accelerating the ions towards the target is typically due to asymmetric electrodes. In order to enhance the chemical reactions that occur in the process chamber, the gas generating the plasma must be specifically selected according to the material which has to be etched. The tool adopted for this thesis is the *Oxford PlasmaPro NPG 80*. Its wafer platter is made of graphite and it can reach a maximum RF power of 300 W.

Electron beam lithography

Electron beam lithography (EBL) operates with the same purpose of photolithography, but the light source is substituted by an electron beam source. The purpose of lithography is to transfer a desired pattern into a polymer layer spun on a substrate, called resist. In particular, electron beam lithography needs special electron-sensitive resists that react to a focused electron beam. The desired layout is designed by a CAD software and converted into a GDS file, that will be used to transfer the necessary information to the writing tool. The main advantage of EBL compared to photolithography is the possibility to directly write on the resist without needing to generate a mask. This makes it very expensive, but also versatile and customizable. The other great advantage is the resolution, that is much higher than photolithography, because the wavelength of the wave-like electrons is much shorter than light, so that diffraction is negligible.

The resolution of the tool is limited by the alignment procedure, whose aim is to align the desired pattern to the substrate alignment marks. The substrate can be exposed by the focused electron beam in two different ways: raster scan consists of scanning the entire substrate with the electron beam, shutting off the beam where the exposure is not required, while vector scan exposes only the areas where the exposure is required. The last technique is faster, but it can expose some undesired areas because the electron beam is never shut off. The *Vistec EBPG 5200+* is the tool used in this thesis. It can reach a sub-8nm resolution and the electron beam source is a Schottky thermal field emitter.

Electron beam evaporation

Electron beam evaporation is a physical vapor deposition (PVD) technique. Unlike chemical vapor deposition, physical vapor deposition consists in the deposition of gas molecules onto a cooler substrate by condensation and not by chemical reactions. It is generally adopted for metal deposition. It consists of a low pressure double-chamber, divided into a process chamber and a source chamber. The source chamber contains the crucibles hosting the source materials. In electron beam evaporation the evaporating agent is an electron beam generated by a heated tungsten filament. The filament is heated until thermionic emission of electrons occurs. The advantage of electron beam evaporation compared to thermal evaporation is that the crucible is kept at low temperature, so no contaminants are introduced in the source materials. Furthermore, the electrons generated by thermionic emission are deflected from the tungsten filament to the source material by an electromagnetic field, so no contaminants are introduced in the source material from the filament, too. Different metals can be evaporated subsequently, without breaking the vacuum, because more than one crucible are mounted in the source chamber. The source materials are evaporated so that they can reach the process chamber and condensate on the substrate, mounted upside down on a cold plate. When the plate is inserted or removed from the tool, the vacuum is broken only in the process chamber to speed up the process and to prevent the source chamber from being contaminated.

The advantage of electron beam evaporation is the high deposition rate and the low adopted temperatures if compared with CVD techniques. However, the deposition is highly directional, so the resulting conformality is quite poor. The conformality can be increased by heating the holder plate, but not every tool has this feature. Also, not every material can be evaporated, so this technique is mainly used for the deposition of metals. The e-beam evaporator used in this thesis is the *Evatec BAK501 LL*. It disposes only of a cold plate.

Atomic layer deposition

Atomic layer deposition (ALD) is a chemical vapor deposition (CVD) technique. Its purpose is the atomically controlled thin films deposition. ALD can deposit metals, semiconductors and insulators. The source material is deposited by chemical reactions with the substrate from a gas phase. It generally uses high temperatures to enhance the chemical reactions and low pressures to minimize contamination. The

peculiarity of this technique is the alternation of two or more gaseous precursors that are introduced into the chamber in sequence. Between one gas and the next, the chamber is purged of an inert gas. The gases are selected so that at each pulse the reaction is self-limiting. When an atomic layer of one of the precursors has reacted over the entire surface, the reaction is self-limited. The same happens for the next gas. At the end of a cycle the reaction of the first gas can be repeated.

Unlike evaporation, the great advantage of ALD is the high conformality. Furthermore, it is possible to operate with a very fine control on the thickness of the deposited layer by setting the desired number of cycles. However, this technique is very slow. The tool adopted in this thesis is the *Oxford FlexAL ALD*.

Plasma enhanced chemical vapour deposition

Plasma enhanced chemical vapour deposition (PECVD) is a chemical vapor deposition technique. Similarly to ALD, it can deposit metals, semiconductors and insulators. The source material is deposited by chemical reactions with the substrate from a gas phase. It generally uses low pressures to minimize contamination. In contrast to ALD, in plasma enhanced chemical vapour deposition the precursors are present simultaneously in the reactor. This makes the deposition thickness more difficult to control and the conformality poorer than ALD. If the holder plate is heated, the adsorbed reactants can migrate along the surface increasing the conformality. The precursors must be selected accordingly to the desired chemical products.

As the name suggests, the energy required for the chemical reactions is provided by the plasma generated by the gas precursors. The plasma is generally generated by a RF power supply. Unlike RIE, the plasma does not favor the etching of the material, but it supplies the energy necessary for the chemical reactions to take place at the surface of the target. The RF power supply is applied to a couple of electrodes. One of the electrodes is grounded. The accelerated electrons collide with the gaseous atoms generating ions. The energy supplied by the plasma allows to reduce the temperature in the reaction chamber and increases the deposition rate. However, plasma can damage the deposited layer. The *Oxford PlasmaPro 100 PECVD System* is the tool used for this thesis.

Rapid thermal annealing

Rapid thermal annealing is a manufacturing process consisting in heating a substrate at high temperatures for a short time. Different heating sources can be adopted by this technique like high intensity lamps or lasers. The purpose of this method can be dopant diffusion, dopant activation, metal reflow, chemical vapor deposition, thermal oxidation and so on. The temperature ramp can be very steep, but in this case it is possible to cause an overshoot. The temperature can be controlled by a pyrometer or a thermocouple. The inert gases introduced into the chamber during the process can be chosen accordingly to the reactivity with the materials present in the chamber. The furnace adopted for this thesis is the *Annealsys AS-one 150*.

2.4.2 Characterization techniques

Profilometer

A profilometer is a characterization tool used to measure the thickness of the surface's roughness. Two types of profilometers exist: contact and non-contact. The contact (mechanical) mode probes the surface's profile by a stylus, while the non-contact (optical) mode exploits light's interference to measure the surface's roughness. The surface is scanned by the stage or the probe movement. The *Dektak 6M* is used for this thesis. It is a stylus profilometer with a 1nm vertical resolution.

Scanning electron microscopy

A scanning electron microscope (SEM) uses a focused electron beam to analyse the sample. The first great advantage in comparison with an optical microscope is the much higher resolution, due to the extremely low wavelength of electrons. Furthermore, SEM is characterized by larger depth of field and it can extrapolate additional information by the signals generated by the collisions of the electrons with the sample. It can be exploited not only for topographical and morphological information, but also for compositional and crystallographic characterization. Sample preparation is simpler than a TEM and it can scan large samples. However, high energy electrons can damage biological samples or charge up insulating surfaces.

Different signals are generated by the interaction of the electrons with the sample. The two main information signals are backscattered electrons (BSE) and secondary electrons (SE), collected by different types of detectors. The first category of electrons are emitted by elastic interactions, that means that the incident electrons are deflected by the specimen atomic nucleus with high energies. During the collision they lose a negligible amount of energy, but they are deflected of a wide angle. Measuring the intensity of this signal provides useful compositional information, because the elements with higher atomic numbers have more positive charges on the nucleus, that means that more electrons are backscattered producing a more intensive backscattered signal. They are generally detected by a solid state detector (SSD). The result is contrast due to the atomic number of the elements in the SEM images. The secondary electrons are characterized by lower energies because they are generated by inelastic interactions with the electrons of the atoms of the sample. They can only escape from a small region of the material surface because of their low energy, so they can provide topographic information with a nanometer resolution. They are generally detected by an Everhart–Thornley (ET) detector. BSE also provide topographic information, but characterized by a lower resolution than SE, because they have larger energies, so their interaction region is larger. To sum up, from the backscattered electron image, clear information on the composition of the sample can be obtained, while in the secondary electron image, the roughness morphology can be analysed. The SEM used for this thesis is the *Hitachi SU8000*. Other signals can be generated by the interaction of the incident electrons with the sample: x-rays, Auger electrons, cathodoluminescence, transmitted electrons that can provide other types of information.

Energy-dispersive x-ray spectroscopy

Energy-dispersive x-ray spectroscopy (EDS or EDX) is a characterization technique obtained by the combination of an additional detector with a scanning electron microscope. The analysed signal is generated by the interaction of the incident electrons with the atoms of the specimen. When an inner shell electron is displaced by collision with an incident electron, an outer shell electron may fall into the inner shell to reestablish the charge balance in its orbitals. The ionized atom returns to ground state by the emission of an x-ray photon. The energy of the emitted photon is characteristic of the jump made by the electron between the energy levels of the orbitals of the affected atom. For this reason this signal is called characteristic x-ray signal. Measuring the energy possessed by that photon it is possible to establish which element emitted it. The deceleration of high-energy electrons generates an additional continuous background signal that is called Bremsstrahlung or continuum x-ray signal. This constitutes a background noise that must be carefully removed from the analysed signal. The x-ray detector adopted for this thesis is the *Oxford Instruments X-Max*.

Semiconductor Device Parameter Analyzer

For the electrical characterization of the devices in this thesis the *Keysight B1500A semiconductor device parameter analyzer* has been used. It is an all-in-one device characterization analyzer supporting IV, CV, pulse/dynamic IV and more. The mainframe and plug-in modules enable characterization of most electronic devices, as well as materials, semiconductors, and active/passive components [11]. Two- and four-wire measurements have been carried out with it to measure current-voltage characteristics and resistivity. Triaxial cables have been used for low noise measurements to connect the parameter analyser to the probe station. The probe station consists of a movable stage, adjustable probes and an optical microscope. The tips of the electrical probes are made of tungsten and are characterized by a diameter of 5 µm.

Physical Property Measurement System

For the electrical measurements in temperature of the devices in this thesis the *Quantum Design PPMS DynaCool* has been used. The PPMS DynaCool uses a single two-stage pulse tube cooler to cool both the superconducting magnet and the temperature control system, providing a low vibration environment for sample measurements. It offers continuous low temperature control and precise field and temperature sweep modes [12]. The tool can operate in the temperature range of 1.8 K–400 K and can generate magnetic fields up to 9 T.

Chapter 3

Process flow

In this chapter the general process flow for the electrical contacting of the hexagonal GaAs/SiGe core/shell nanowires is described. Each section is focused on one of the main processing steps in this regard. The general issues involving each step are analyzed in detail and the different tests carried out to set the most suitable tools parameters are reported. Additional steps that cannot be applied at every run, and their related issues, will be explained in the following chapters whenever necessary.

Before reporting the detailed description of the main processing steps, a brief summary of the manufacturing process is provided in the following paragraphs as depicted in Figure 3.1.

Substrate cleaning Before the deposition of the SiGe nanowires on the SiO_2 substrate, it is necessary to perform a cleaning step to improve their adhesion to the surface and to prevent them from moving during the next processing steps. In particular, a first step consists in removing the dust particles with an N_2 gun, then the substrate is treated with an O_2 plasma to eliminate the organic impurities.

Nanowires deposition Now that the substrate is cleaned, the nanowires can be transferred from the chip they grew up on to the new chips to be processed. Cleanroom paper is used to do the transfer.

Surface planarization If the metal for the electrical contacts was deposited on the bare nanowires, a gap would be created between the nanowires and the substrate which would make the contact hard to establish. Therefore, a benzocyclobutene-based polymer with excellent planarization properties is spun onto the chip surface to fill the gap.

Reactive ion etching The benzocyclobutene-based polymer could partially cover the nanowires decreasing the chances of making electrical contacts when the metal is deposited. Reactive ion etching must be performed to reduce the polymer thickness and uncover the nanowires.

Resist spinning A double layer of positive electron-sensitive photoresist is spun on the substrate. The underlying layer is made of PMMA/MA 33%. This co-polymer is characterized by 3-4 times higher sensitivity than PMMA 950k, the second layer. It is typically used as an undercut layer for lift-off applications in a bi-layer scheme along with PMMA 950k.

Electron beam lithography The bi-layer resist is exposed by electron beam lithography in those areas where the polymer needs to be removed to deposit the metal contacts. The design is customized for every chip in order to align the metal contacts to the randomly deposited nanowires.

Resist development The resist areas exposed by the electron beam are removed from the substrate by MIBK:IPA 1:2 developer. The development step terminates when the chip is rinsed in IPA.

Contacts areas cleaning Before the deposition of the metal contacts, it is necessary to clean the nanowires surface. The residual organic impurities are etched away by an O_2 plasma asher, while the thin SiO_2 barrier grown on the surface of the nanowires due to the air exposure is removed by BHF wet etching.

Metal evaporation The metal for the electrical contacts is deposited on the patterned resist by means of an electron beam evaporator. Initially, Ti is used as an adhesion layer before the evaporation of Au, then Ni will substitute Ti as a reservoir for metal diffusion.

Lift-off The coated substrate with the bi-layer resist and the deposited metal films is immersed in heated DMSO for a short period until the resist is stripped off. Then, the substrate is rinsed in IPA to remove the residual polymer. After this final step, the metal left on the substrate is patterned according to the desired design.

3.1 Nanowires deposition

The hexagonal GaAs/SiGe core/shell nanowires are grown on a GaAs substrate by crystal transfer method as explained in Section 1.1. They are arranged vertically on the substrate at the end of their growth, so they must be transferred to a new substrate to be electrically contacted. The new substrate is composed by a 120 nm SiO_2 layer on a Si wafer for electrical isolation. However, the SiO_2 layer also generates some issues. First, charge-up effects could occur during SEM imaging because of the isolation from the substrate, generating some artifacts. Then, a too long HF etching process could affect the SiO_2 layer, causing undesired over-etching. The wafer is patterned with tungsten markers for subsequent EBL alignment, then it is diced into 10 mm chips.

Before transferring the nanowires on the new substrate, it is important to treat the surface with an O_2 plasma to ensure that all the organic impurities are eliminated.

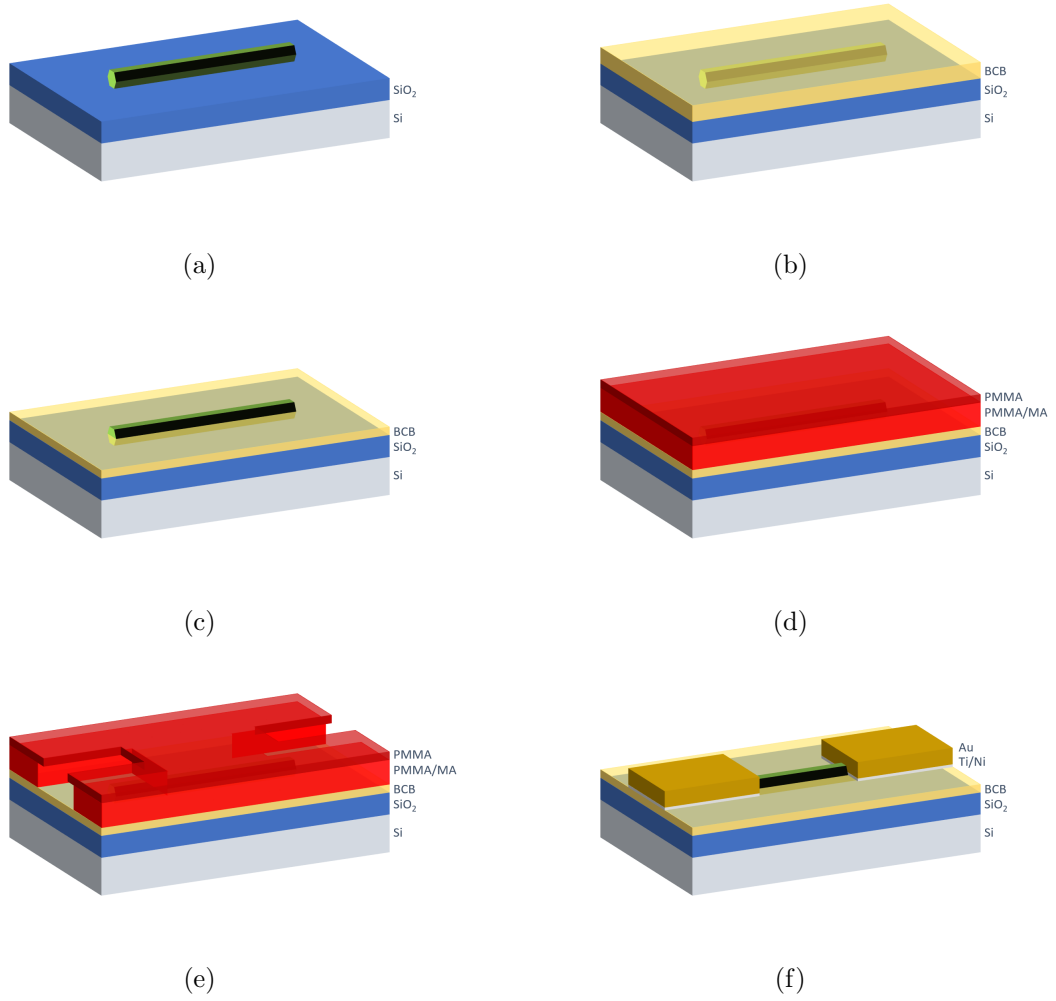
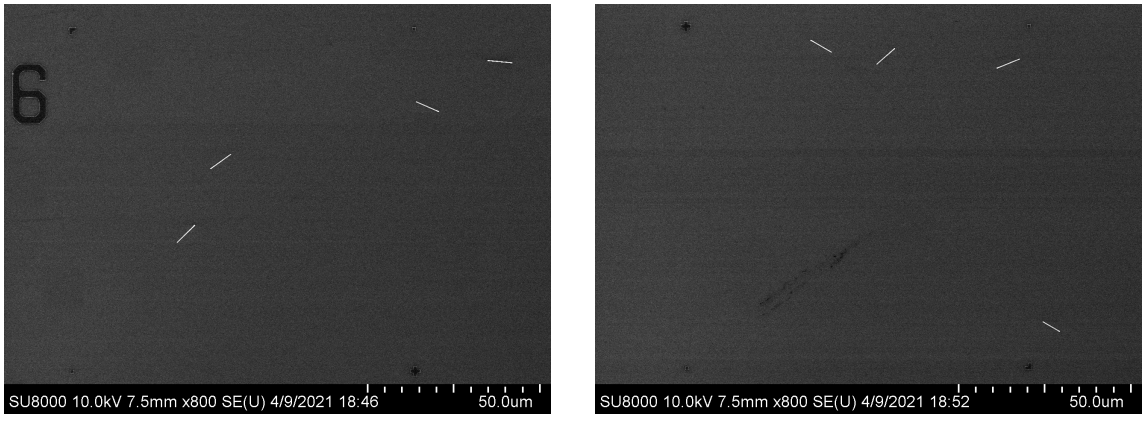


Figure 3.1: Schematics of the general process flow for the electrical contacting of the hexagonal GaAs/SiGe core/shell nanowires. **(a)** Nanowires deposition. **(b)** Surface planarization with a benzocyclobutene-based polymer. **(c)** Partial reactive ion etching of the benzocyclobutene-based polymer. **(d)** Double layer positive electron-sensitive photoresist spinning. **(e)** Electron beam lithography and resist development. **(f)** Metal evaporation and lift-off.

This step enhances their adhesion to prevent them from moving during the next treatments. A 200 W O_2 plasma for 60 s is sufficient for this purpose. At this point, cleanroom paper is used to carry out the transfer sliding it first on the bunch of nanowires and then on the clean chip. A small area in the center of the chip is highlighted by larger tungsten markers for deposition. It is important to collect the nanowires from the edges of the original substrate because the central ones generally show crystalline defects due to stacking faults. The deposited nanowires are shown in Figure 3.2.

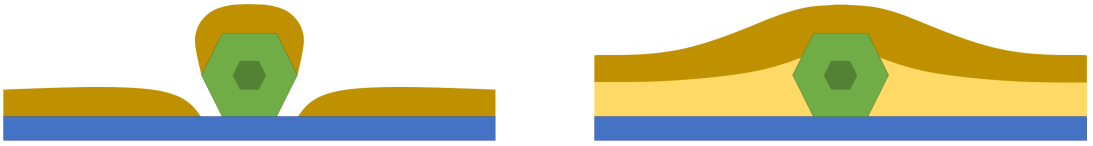


(a) (b)

Figure 3.2: SEM images of the nanowires lying on the substrate after transferring. The tungsten markers are useful for EBL alignment.

Now that they lie on the surface of the chip, it is useful to capture SEM images of the nanowires together with a couple of tungsten markers. This mapping images will be overlapped with the GDS file of the chip template in order to align the markers and to mark the positions of the nanowires. Knowing their positions, it is possible to design the metal contacts. This process is repeated for every chip as the nanowires are distributed randomly.

If the metal was evaporated on the bare nanowires, their thickness and their hexagonal morphology would cause a bad coverage. Their average diameter is 220 nm, while the targeted metallization thickness ranges from 100 nm to 150 nm. If the surface was not planarized before depositing the metal, gaps would be created in the metal tracks, as shown in Figure 3.3a, which would translate into open contacts. A preliminary test without substrate planarization is performed in Section 4.1 in order to analyse this issue and find an appropriate solution to solve it. This bad coverage is mainly due to the low conformality of the evaporation process because of the shadow effect of the hexagonal morphology of SiGe. The growth rate of the evaporated material is dependent on the flux density of the gas molecules, that tends to zero in the shadowed areas. Another factor that reduces the conformality is the cold substrate of the evaporator, which prevents molecules from migrating after being adsorbed on the surface. This issues can be solved by planarizing the surface before the metal deposition as shown in Figure 3.3b. In this thesis, the high degree of planarization of benzocyclobutene-based polymers is exploited to solve this problem. Section 3.2 will explain in detail which polymer has been chosen and how it is implemented.



(a) (b)

Figure 3.3: Schematic cross-section of the SiGe nanowires showing the effect of planarization before metal deposition. **(a)** If the metal was evaporated on the bare nanowires, the shadow effect of their hexagonal morphology would cause a bad coverage, generating some gaps in the metal tracks. **(b)** A polymer with excellent planarization properties con solve this issue, enhancing the conformality of the evaporated metal layer.

3.2 Benzocyclobutene-based polymers

The Dow Chemical Company developed a class of benzocyclobutene-based polymers with excellent properties for microelectronic fabrication. Two main series of polymers were commercialized: the non-photosensitive CYCLOTENE^{TM} 3000 series and the CYCLOTENE^{TM} 4000 series. The latter is composed by photosensitive negative resins, that means that the exposed areas are cross-linked and the polymers is not removed by development.

This thesis focuses on the CYCLOTENE^{TM} 3000 series, that is a class of low dielectric constant resins obtained by the partial polymerization of B-staged bisbenzocyclobutene (BCB) monomers. The properties that make this family of polymers suitable for this project are the low temperature cure and the excellent degree of planarization. The formulation selected for the planarization of the substrate after the deposition of the NWs is the CYCLOTENE^{TM} 3022-35. It has been chosen because of the low viscosity (14 cSt @ 25 °C) that allows a low thickness range (1.0-2.4 µm) when spin-coated [13]. In addition, the thickness range can be further reduced by diluting the polymer with Mesitylene solvent.

The first step for planarization consists in the surface preparation. The datasheet of CYCLOTENE^{TM} products suggests that the substrate to be coated should be free of inorganic particles, organic residues and other contaminants because particles and residues cause coating defects and may lead to adhesion problems. A treatment into the O_2 plasma asher should be sufficient to solve the issue, but this step is skipped because it has been already done before the deposition of the NWs to improve their adhesion to the substrate. Numerous tests proved that the adhesion of the BCB to the substrate is sufficiently good. Furthermore, vapor prime adhesion promoters developed for photoresists (HMDS) should be avoided because do not work well with the CYCLOTENE^{TM} family of resins [13]. Some solutions with different ratios of CYCLOTENE^{TM} 3022-35:Mesitylene have been mixed and spun at different rotational speeds for 40 s onto the substrate to tests the resulting thickness range. After spin-coating, it is necessary to thermal cure the resins to let the solvent evaporate and to enhance the polymers cross-linking. This step is performed into a convection oven at 300 °C for 30 min. This process parameters should be sufficient

for the complete solidification of the BCB as can be deduced from Figure 3.4. In addition, the NWs do not get damage by such a low temperature, so this step is process compatible.

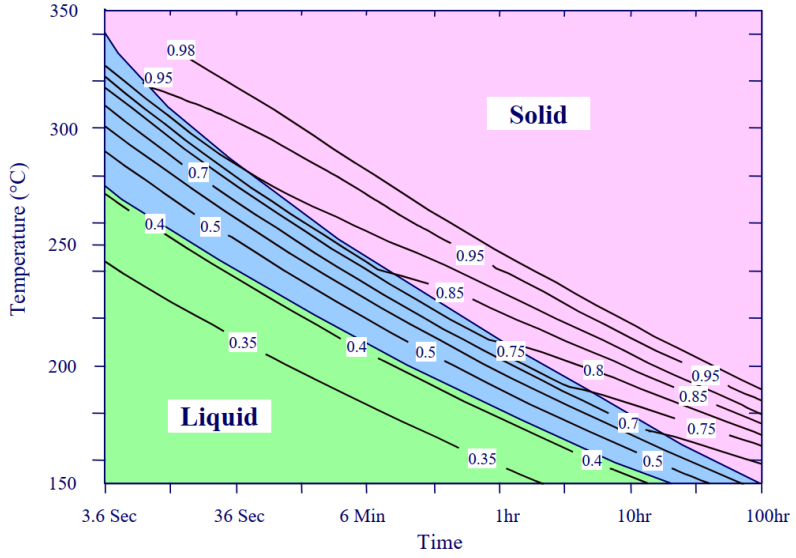


Figure 3.4: The extent of BCB cure as a function of temperature and time [13].

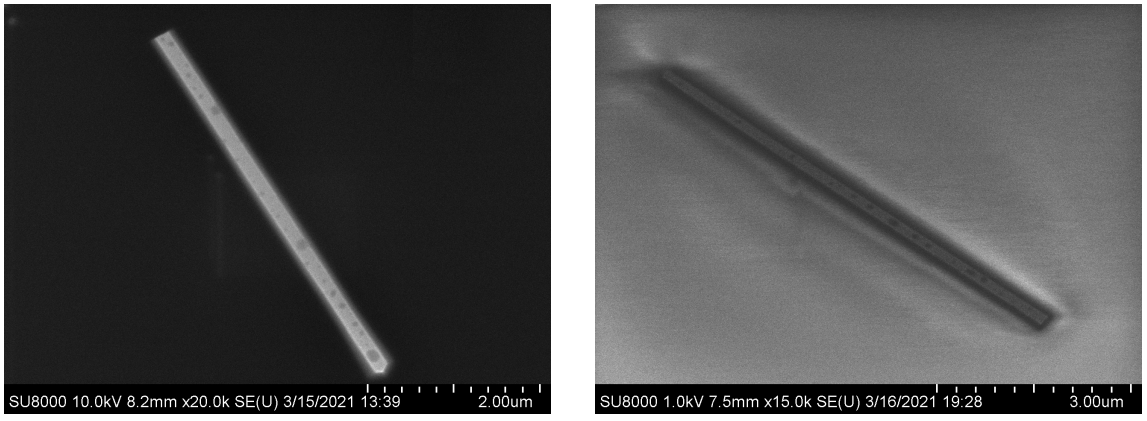
After thermal curing, the thickness of the cross-linked polymers can be measured by a profilometer. The values reported in Table 3.1 have been obtained by the central area of dummy chips, assuming a uniform thickness of the BCB. Some variations can be due to the variability of the process step or to the edge beads, if the chips are very small. A thickness of about 120 nm is the target for a good planarization of the chip surface, considering that the average NWs diameter is 220 nm. This means that the more suitable mixing ratio for this purpose is 1:2 CYCLOTENE^{TM} 3022-35:Mesitylene spun at 3000 rpm for 40 s. The excellent planarization properties of BCB are showed in Figure A.1. For a feature thickness of the order of a few hundreds on nanometers, a planarization ratio of nearly 1 should be easily obtained, but it should also be considered that the polymer film thickness is of the same order of magnitude.

Table 3.1: Thickness after cure into a convection oven at 300 °C for 30 min versus 40 s spin speed for different mixing ratios.

CYCLOTENE^{TM} 3022-35:Mesitylene	Spin Speed (rpm)	Thickness (nm)
2:3	3000	278 ± 1
2:3	4000	252 ± 1
2:3	5000	221 ± 1
1:3	3000	083 ± 1
1:3	5000	073 ± 1
1:2	3000	122 ± 1

3.3 Reactive Ion Etching

As described in Section 3.2, the CYCLOTENE^{TM} 3000 resins series is characterized by low temperature cure and excellent planarization properties. However, two opposite issues could occur during the polymer spinning. If the thickness of the spun polymer film was too low, the degree of planarization would not be sufficient to obtain good metal contacts. On the other hand, to ensure a sufficient degree of planarization, it is necessary to increase the BCB thickness, but a new problem arises in this case. A thin layer or some droplets of the polymer resin could cover the NWs' surface during spin-coating (Figure 3.5a), because the BCB tends to accumulate near obstacles due to centrifugal and electrostatic forces, as clearly shown in Figure 3.5b. Considering that BCB is an insulating material, the electrical contacts cannot be correctly established if some droplets are still present at the metal-semiconductor interface during the metal deposition. For this reason, it is necessary to etch away the excess material.



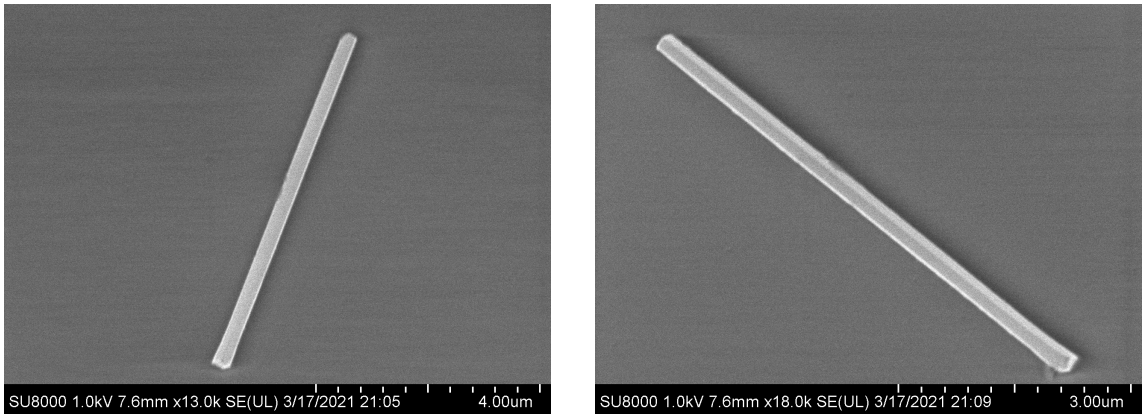
(a) (b)

Figure 3.5: SEM images showing the issue of the NWs covered by BCB. **(a)** Some polymer droplets could stand between the metal and the semiconductor materials, breaking the electrical contacts. **(b)** The resin accumulates at the edges of obstacles during spin-coating, a clear advantage for planarization.

To etch away a small portion of the spun and hard baked BCB, a Reactive Ion Etcher has been implemented. Before operating on the real chips, some tests was performed on dummy chips to set the most suitable parameters. The aim was to obtain a good etch rate while preserving a low chip-to-chip variability. The higher the etching time, the lower the etched thickness variability. It must also be considered that benzocyclobutene is a silicon containing polymer. This means that the etch rate would be extremely low if a silicon etching gas precursor was not included in the RIE recipe, because silicon would accumulate on the surface during the etching of the polymer. Good gas precursors for silicon etching are SF_6 and O_2, because SF_6-O_2 mixtures can react with Si to produce the volatile SiF_4 [14]. On the contrary, the etch rate of BCB with 100% oxygen is extremely low because of the inability to convert silicon into the volatile SiF_4, quickly leading to a silicon rich surface, as reported by *Sandia National Laboratories* [15]. The same laboratories did additional

tests with different SF_6-O_2 mixing ratios in order to obtain a calibration curve for the BCB etch rate, as reported in Figure A.2, and to estimate the contribution of SF_6 as a gas precursor. They found an optimal etching rate with the addition of 10% SF_6. However, this project is focused on SiGe NWs. SF_6 should be removed to preserve the integrity of the SiGe crystalline structure and the hexagonal morphology of the NWs. This results in a very low etching rate, but still reasonable considering that in this case it is sufficient to etch away a few tens of nanometers.

The first tests were performed under the following conditions: RIE power of 20 W, O_2 flow rate of 50 SCCM, SF_6 flow rate of 5 SCCM, chamber pressure of 50 mTorr, temperature of 20 °C. The average BCB etch rate resulted in 10 nm/min. If SF_6 took part to the etching process, 2 min would be sufficient to etch a sufficient portion of the polymer surface. However, SF_6 was removed by the RIE recipe to avoid damaging the SiGe NWs. The SF_6 flow rate was reduced to 0 SCCM, while all the other parameters remained the same. This results in an average etch rate slightly greater than 1 nm/min. Therefore, to sufficiently etch away the BCB, the process time was set to 20 min, resulting in an average etched thickness of 20 nm. To increase the etching rate, the RIE power could be increased, but this would result in a higher process variability. Considering that the thickness of the features involved is of the order of tens of nanometers, it is preferable to keep a lower power. The final result is reported in Figure 3.6.



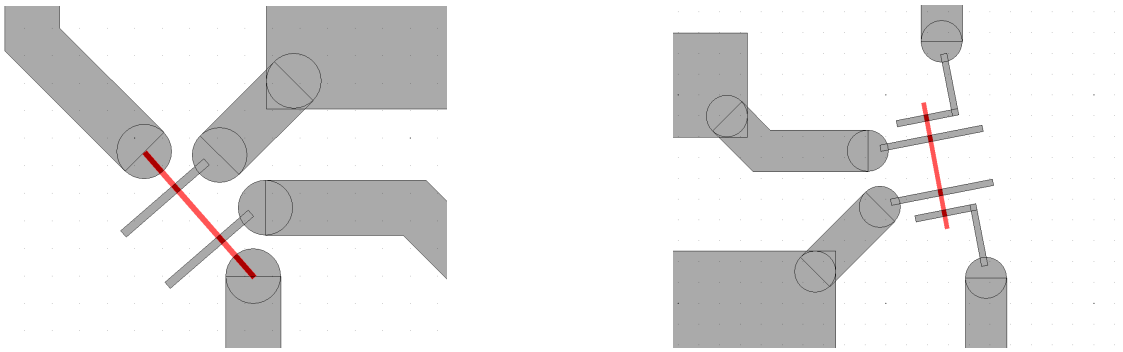
(a) (b)

Figure 3.6: SEM images of the NWs after BCB partial etching. **(a)** The polymer droplets have been completely etched away. **(b)** The darker area is due to the hexagonal morphology of the NWs, because the image is composed by SE, but the bright edges clearly show the absence of polymer on the top surface of the NW.

3.4 Electron beam lithography

Now that the surface with the nanowires is planarized, the metal contacts design must be transferred to the chip substrate. Electron beam lithography is chosen for this task because every chip needs a customized design since they are distributed randomly. As anticipated in Section 3.1, the SEM images captured after the deposition are overlapped with the GDS file. In order to mark the correct position of some

nanowires, the tungsten markers on the SEM images are aligned to the markers on the digital file and the positions are outlined. The metal pads for the subsequent electrical characterization are designed as close as possible to the chip's edges to make the bonding with an external holder easier. Then, metallic tracks connect the metal pads to the four-wire contacts on the nanowires. The metal contacts are designed to minimize the issues due to slight misalignments. The first proposed design aims to overlap the contacts with the nanowires even if large misalignments occur, as showed in Figure 3.7a. When higher accuracy has been achieved during the alignment process, it was possible to improve the design so that all the contact areas were the same, as depicted in Figure 3.7b. This is very useful to obtain good contacts resistivity measurements with the TLM method, as explained in Section 2.2.

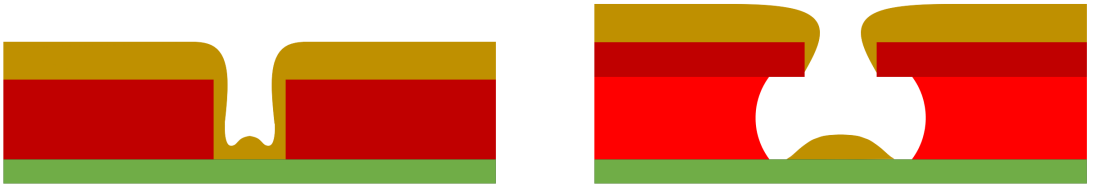


(a) (b)

Figure 3.7: GDS file design showing the metal contacts in four-wires configuration. **(a)** First design aiming to minimize the misalignment issue. **(b)** Improved design characterized by four equal contacts areas for contacts resistivity measurements.

Then, the substrate is spin-coated with an electron-sensitive photoresist to transfer the digital design to the physical chip. It is important to take into consideration that the metal will be patterned with the lift-off technique. This means that by stripping away the resist the metal could also be removed if this step is not done correctly. Spinning a single layer of photoresist could cause the metal to deposit as a single continuous film, as depicted in Figure 3.8a. In this case, the metal would peel-off completely during the lift-off process. A double layer configuration could solve this problem. If the upper layer sticks out over the lower layer, the evaporated metal splits due to the shadow effect caused by this layout, as shown in Figure 3.8b.

For this reason, a double layer of positive electron-sensitive photoresist is spun on the substrate. The underlying layer is made of PMMA/MA 33%. It is a co-polymer of poly methyl methacrylate and a methacrylic acid. It is typically used as an undercut layer for lift-off applications in a bi-layer scheme along with PMMA 950k, the second layer, because it is characterized by 3-4 times higher sensitivity. PMMA950k is a positive tone resist which has been used for decades in e-beam lithography applications. It consists of long polymer chains (MW 950,000 g/mol) that upon irradiation from the electron beam undergo chain scission rendering fragments with lower molecular weight that can be dissolved/removed by the developer [16]. To increase the adhesion of the resist to the substrate it is suggested to perform a 180 °C



(a) (b)

Figure 3.8: Schematic cross-section comparing single and double layer resist effect on metal evaporation. **(a)** A single layer of resist could cause the metal to deposit as a single continuous film. **(b)** A bi-layer scheme let the evaporated metal split due to the shadow effect.

dehydration step on the hotplate for 5 min. The first layer is spun at 5000 rpm for 40 s to obtain a thickness of about 300 nm, suitable for a metal thickness ranging from 100 nm to 150 nm. Then, the resist is subjected to a 180 °C post apply bake on the hotplate for 5 min to allow the excess solvent to evaporate. The second layer is spun at 3000 rpm for 40 s to obtain a thickness of about 140 nm, sufficient to produce a shadow effect during the metal evaporation. Finally, the same post apply bake is repeated as before.

After resist spin-coating, the chip is submitted to the electron beam lithography. The self-alignment is done by means of special tungsten markers previously sputtered for this purpose. Then, the exposure dose is adjusted to $\sim$420 µC/cm^2. The exposed areas are subjected to polymer chain scission, so they will be dissolved by development.

Finally, the double layer photoresist is developed in MIBK:IPA 1:2. The chip is immersed in a baker containing the mixture and rotated clockwise and counterclockwise in order to enhance the process. 60 s are sufficient to obtain a good development of the resist, without leaving residues in the exposed areas. Then, the chip is rinsed in IPA for 30 s and dried with an N_2 gun. The result is checked under an optical microscope to ensure a complete development. If there are any residues left, this process is prolonged. An example of the final result of a by-layer resist scheme for lift-off applications is shown in Figure A.3.

3.5 Metallization

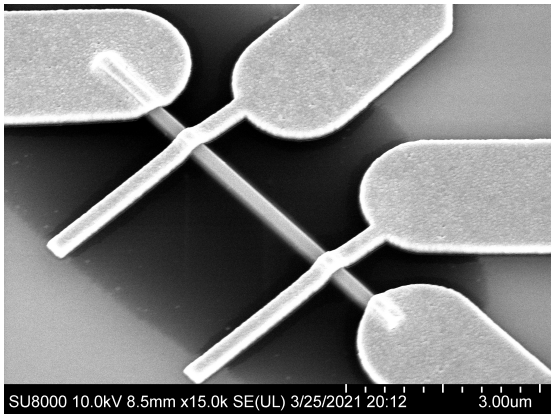
After the resist development, some organic residues may have remained on the surface of the nanowires. This could reduce the contact area during metallization. For this reason, it is useful to perform a chip cleaning by oxygen plasma, as also suggested by E. Stern [17]. It sufficient to set the O_2 plasma asher at 200 W for 30 s. A small amount of resist is etched away, but this is not enough to invalidate the lift-off process. However, during the evaporation of the metal, another factor could invalidate the metal contacts. This is due to the undesired growth of a thin silicon oxide layer on the surface of the nanowires due to the exposure of the chip to the air. 6 s of BHF wet etching are sufficient to remove the thin oxide barrier without

damaging the SiO_2 substrate, considering an etching rate of $\sim$1.2 nm/s.

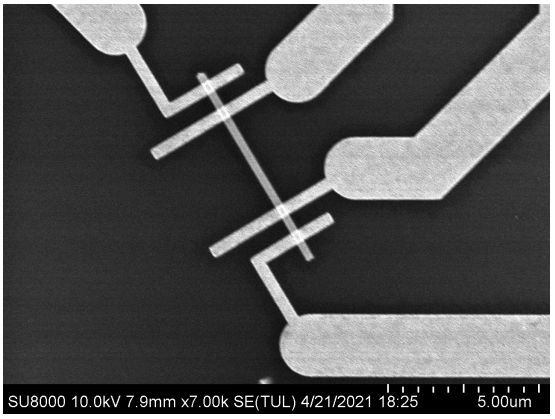
At this point, the chip is ready for metal evaporation. It is loaded into the vacuum load chamber and the process can start. It is important to considered that the plate is cold, so the metal that is deposited on the surface cannot migrate, as explained in Section 3.1. To mitigate this problem, the plate rotates at 10 rpm in order to guarantee the best possible conformality. The metal chosen for the contacts is Au, due to its low resistivity and excellent passivation properties. However, before evaporating gold, Ti or Ni are deposited. On the first chips 150 nm of Au were evaporated on 10 nm of Ti. The titanium is an adhesion layer for gold. Later, titanium was replaced by nickel. 50 nm of Ni below 50 nm of Au provide a reservoir for nickel diffusion. If the chip is annealed at a sufficiently high temperature, nickel can diffuse across the surface of the nanowires. An alloy of NiSiGe can favor the depinning of the Fermi level and reduce the Schottky barrier, or even give rise to ohmic contacts, as explained in Section 6.2. The electron beam evaporator is set to deposit 0.1 nm/s of Ti and 0.2 nm/s of Ni and Au.

The last step of the entire process is the metal lift-off. This method is implemented instead of wet etching because it is easier to perform. Considering that different metals are evaporated on the same chip and by chip to chip, it would be necessary to use different selective and specific chemicals and optimize the wet etching process for each metal. On the contrary, lift-off can be repeated in the same way whatever the metals deposited. Furthermore, a lift-off metallization of the contacts must be performed because subjecting the NWs to metal etchants could be detrimental to their properties [18]. However, this method also introduces some disadvantages. Lift-off is generally characterized by lower resolution than wet etching, because it highly depends on the coverage of the evaporated metal. Furthermore, it is much more likely that some metal or resist impurities will remain on the chip at the end of the process. Finally, The resist thickness should be 2 or 3 times higher than the deposited metal thickness.

The coated substrate with the bi-layer resist and the deposited metal films is immersed in DMSO for a short period until the resist is stripped off. DMSO is a strong solvent, but to enhance its effect it is useful to heat it in the hotplate at 110 °C. Also, sonication cannot be used to aid the lift-off because it may remove NWs from the chips [18]. A pipette can be used to spray the chip with the solvent to speed up the process. When all the resist has been stripped away, the substrate is rinsed in IPA to remove the residual polymer. After this final step, the metal left on the substrate is patterned according to the desired design, as shown in Figure 3.9. The physical design can be compared with the digital design in Figure 3.7.



(a)



(b)

Figure 3.9: SEM images of the nanowires when the metallization for four-wires contacts is completed. **(a)** The darker area shows the accumulation of BCB near the edges of the nanowire. **(b)** Design characterized by four equal contacts areas for contacts resistivity measurement.

Chapter 4

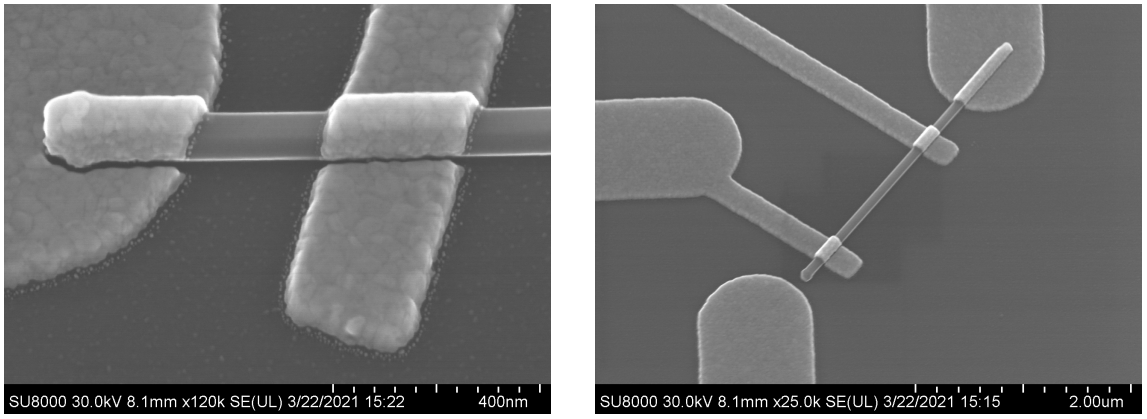
First-run devices

The purpose of this chapter is to highlight the importance of each step of the manufacturing process. Initially, the results obtained from the incomplete process are analyzed, which means without the planarization step. Having acknowledged that this process is fundamental for the success of metallization, the first results obtained from the complete process are presented. From two-wire measurements it is immediate to realize the arising of Schottky barriers from the metal-semiconductor junctions. Then the resistivity values of the nanowires are extracted from the measurements obtained from the four-wires configuration and the SEM. Finally, an electrical characterization in temperature is proposed and possible improvements in this regard are indicated.

4.1 Without BCB planarization

The metal contacts on the first chip were intentionally manufactured without using the BCB for planarizing the substrate with the nanowires, as explained in Section 3.2. This was done to analyze the extent of the problem and to determine which was the most suitable thickness of the polymer for an optimal result. As expected, the gap created between the substrate and the surface of the nanowire due to the shadowing effect during the metal evaporation process is too large to allow successful metal contacts. This is clearly observable from Figure 4.1a, where the broken metal track is shown at the junction between the two parts. It should also be noticed that in this first manufacturing process 10 nm of Ti covered by 60 nm of Au were deposited. Titanium acts as an adhesion layer, therefore its thickness is sufficient, but to increase the chances of success it is convenient to increase the thickness of gold. In the next section the improved thickness of gold will be reported. Finally, as shown in Figure 4.1b, the alignment process needs to be improved to achieve four successful contacts on the same nanowire. As explained in Section 3.4, the alignment is done by superimposing the captured SEM images with the GDS files during the design of the contacts. Therefore, the misalignment may be due to the low resolution of the images. In the following chips the misalignment will be reduced to the minimum, so as to never exceed the margin allowed for achieving contacts.

This improvement was possible thanks to some tricks in capturing SEM images, related to the orientation and the zoom of the images. The electrical results are not reported because none of the nanowires could be contacted due to the issues described above. All two-wire measurements showed open circuits.



(a) (b)

Figure 4.1: SEM images showing the first run issues. **(a)** The lack of planarization by means of BCB makes the metal traces to break because of the gaps created between the substrate and the surface of the nanowires. **(b)** The alignment process fails if the resolution of the images superimposed to the GDS file is not high enough.

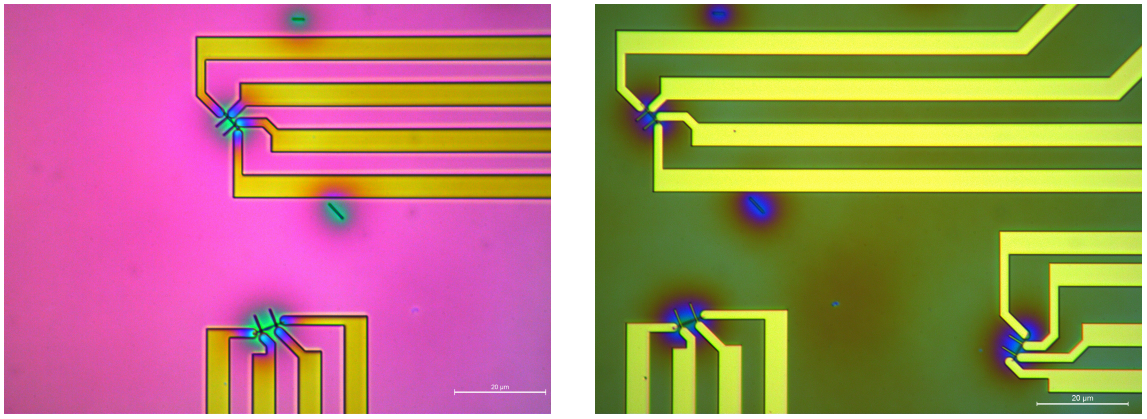
4.2 With BCB planarization

Considering the results obtained without the use of BCB, as described in the previous section, it has been decreed that the planarization of the substrate is essential for the success of the metal contacts. Therefore, the first electrical characterization results obtained following the complete manufacturing process are presented here. The thickness of the deposited Ti is 10 nm as in the previous case, but the Au thickness has been increased to 150 nm. In this way, the probabilities of the metal trace breaking between the surface of the nanowire and the substrate decrease considerably.

As can be seen from Figure 3.9a obtained with the SEM, BCB accumulates more at the edges of the nanowires because it encounters an obstacle during spinning. This behavior enhances the planarization of the substrate, because the higher the obstacle, the higher the thickness of the polymer. This effect is not only visible in the SEM, but it is sufficient to observe the samples under the optical microscope to notice it, as clearly visible in Figure 4.2.

4.2.1 Two-wire measurements

The most immediate type of electrical characterization that can be performed on the nanowires is the two-wire measurement of the current-voltage characteristic. Based on the trend of the data collected, it is possible to determine whether the metal-semiconductor electrical contact is characterized by a rectifying or ohmic behavior.



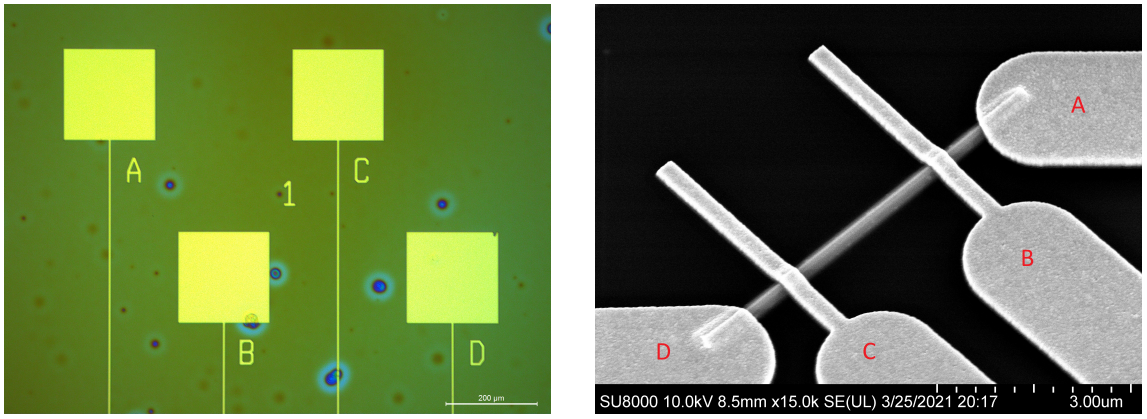
(a) (b)

Figure 4.2: Optical microscope images highlighting the accumulation of the BCB at the edges of the nanowires **(a)** after resist development and **(b)** after metal lift-off.

The first one is characterized by a high resistance around the origin, i.e. below the threshold voltage if the metal-semiconductor junction is described as a Schottky diode. This rectifying behavior is clearly shown in Figure 2.4 and will be compared with the trend obtained from the measured curves. The effect is more pronounced if the ideality factor introduced in Section 2.1.2 differs from 1. On the contrary, the result produced by an ohmic contact is characterized by a linear trend of the IV characteristic. In this case, the contact resistance can be measured by linear interpolation of the collected data.

The procedure for measuring the current-voltage characteristics is described in this section and repeated in the same way for all the chips produced. It consists in contacting the metal pads manufactured on the chip with sharp tungsten tips characterized by a diameter of 5 µm at the probe station. Each metal pad is connected to one of the four contacts on each nanowire. A letter is associated with each of the four pads. The pair of letters describing the two-wire measurement performed is shown on the plot of the IV characteristic to distinguish the pair of contacts it concerns. The correspondence of the pads with the electrical contacts on the nanowires is shown in Figure 4.3. On each chip eight nanowires are contacted. Each nanowire is associated with a number from one to eight, also reported in the legend of the plot.

Electrical measurements are made by the Agilent B1500A Semiconductor Device Parameter Analyzer. IV sweeps are performed taking into account that the nanowires could burn if the applied voltage or current is too high. After carrying out some tests, the maximum voltage applied to the nanowires has been set to $\pm 2\,\mathrm{V}$. The compliance set on the current is 10 µA. This means that the maximum current that can flow throw the nanowires during measurements is the value set by compliance. Beyond that value, the current saturates to the maximum value. The results are reported in Figure 4.4. The most relevant pair of contacts is AD, because the other two contacts are those needed for four-wire measurements. However, for the measurement of the contact resistivity, it will be necessary to exploit all the reported



(a) (b)

Figure 4.3: Correspondence of **(a)** the metal pads with **(b)** the metal-semiconductor contacts on each nanowire.

couples to fulfill the requirements of TLM. Thus, it is useful to check the behavior of all couples. Also, before the design improvement, the contact area is highly variable from one to another. This introduces a high variability between one pair of contacts and the others. The variability is quite high even between one nanowire and another as regards the same pair of contacts. This is due to the variability of the contact area from a microscopic point of view during the manufacturing process. This factor will be reduced by replacing titanium with nickel in the next chips. B and C are the contacts that show a higher resistance because they are characterized by a smaller area. However, all measured cases are characterized by rectifying behavior, as expected from a non-engineered metal-semiconductor junction.

4.2.2 Four-wire measurements

Another useful measure obtainable from the electrical characterization of nanowires is their resistivity. It is useful not only to know the conductivity of the novel Hex-SiGe semiconductor, but also to compare the resistivity of the intrinsic material with that of the doped material. Furthermore, knowing the carrier concentration vs resistivity curve, traceable through Hall effect measurements, it is possible to know the doping density from resistivity measurements.

In the same way the current-voltage measurements were obtained, four-wire resistivity measurements are also achieved by Agilent B1500A. The four-wire measurements allow to remove the high resistance of the metal-semiconductor contacts in order to measure only the resistivity of the semiconductor. A current ranging from $-10\,\mu A$ to $+10\,\mu A$ is passed through the nanowire from contact A to contact D. This values corresponds to the compliance for IV measurements. In that range 400 voltage values are sampled. The voltage is measured between contact B and contact C, so as not to measure the resistance of the wires and contacts that connect these two points to the measurements tool. Resistance values are defined as the inverse of the best-fit linear approximation to the IV plot [17]. A selection of the data is done before the linear fit. Data ranges that deviate too far from linearity are excluded.

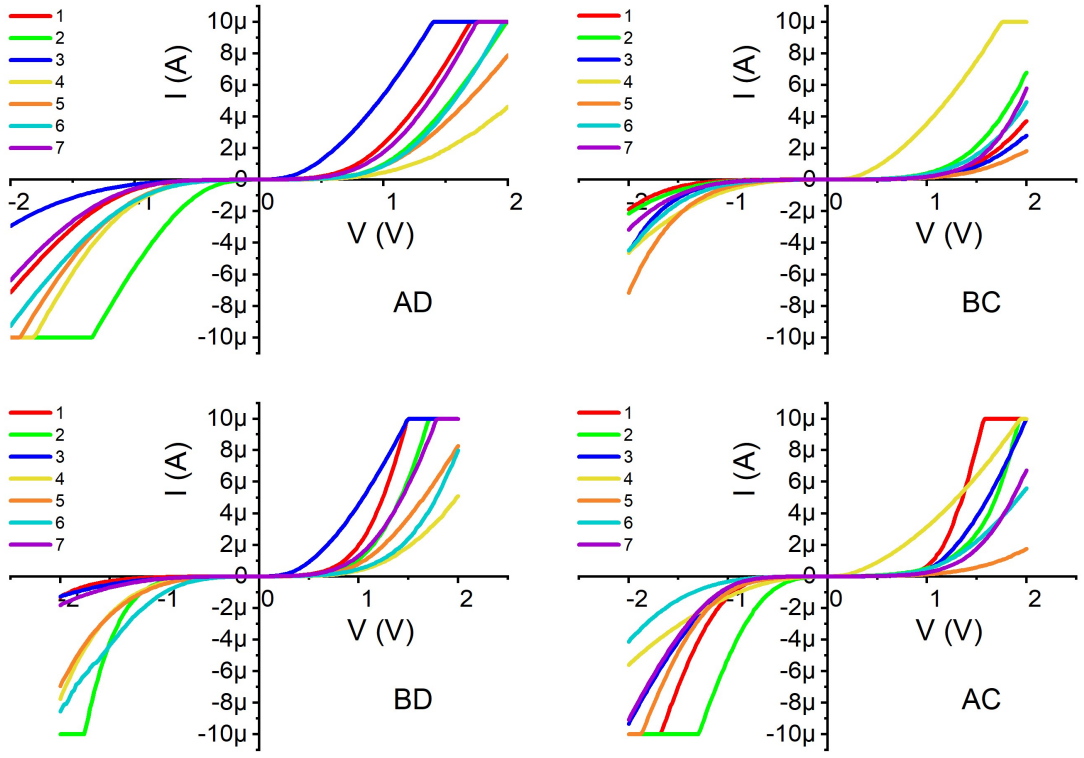


Figure 4.4: Current-voltage characteristics obtained by two-wire measurements of Ti/Au metal-semiconductor contacts. The rectifying behavior is clearly distinguishable in all curves. The legend shows the numbers of the nanowires, while the couple of letters indicates the couple of contacts taken into consideration in each plot.

In this way the resistance values of the nanowires are obtained. However, the resistance of the nanowires is not useful to electrically characterize them because the data obtained are not comparable. In order to compare the data with each other it is necessary to calculate the resistivity of the nanowires. Thus, additional data is needed, namely the length and diameter of the nanowires. The main source of uncertainty is introduced by these measures, which are obtained at the SEM. The results obtained are shown in Figure 4.5. Most nanowires have an average diameter of about 220 nm. The variability of these data is low because their diameter is similar. However, the nanowires have hexagonal rather than circular morphology. This introduces an approximation that varies as the diameter of the circles surrounding the measured hexagons varies. For this reason, the nanowires that have a diameter that is very different from the average one are characterized by resistivity values that are not comparable with the other ones, so they must be excluded. The values obtained fall within the resistivity range between silicon and germanium as reported in literature. They are closer to the resistivity of germanium, as one would expect considering that they are composed of 80% germanium and 20% silicon. However, it must also be taken into account that the resistivity values of semiconductors strongly depend on the carrier concentration.

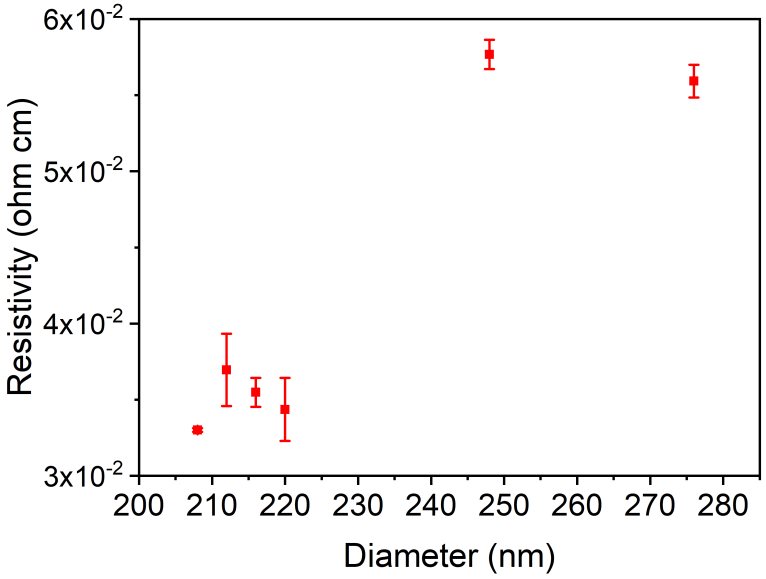


Figure 4.5: Resistivity values calculated by four-wire and SEM measurements performed on Hex-SiGe nanowires as grown.

4.3 Temperature sweep

The behavior of the metal contacts is further investigated through a temperature analysis. From the two-wire measurements it is expected to notice an increase in the height of the Schottky barriers as the temperature decreases. To carry out the measurements, the sample was prepared to be mounted on the instrument. The chip

was placed on a holder and fixed with a colloidal resin. After that, the chip pads were contacted to the holder pads by wire bonding. The wires are made of aluminum. The holder pads are connected to pins that mount on the measuring tool. Then, the holder is mounted in the PPMS DynaCool to sweep the temperature from 300 K to 50 K. In this temperature range the current-voltage characteristics are measured step by step. The obtained results are reported in Figure 4.6.

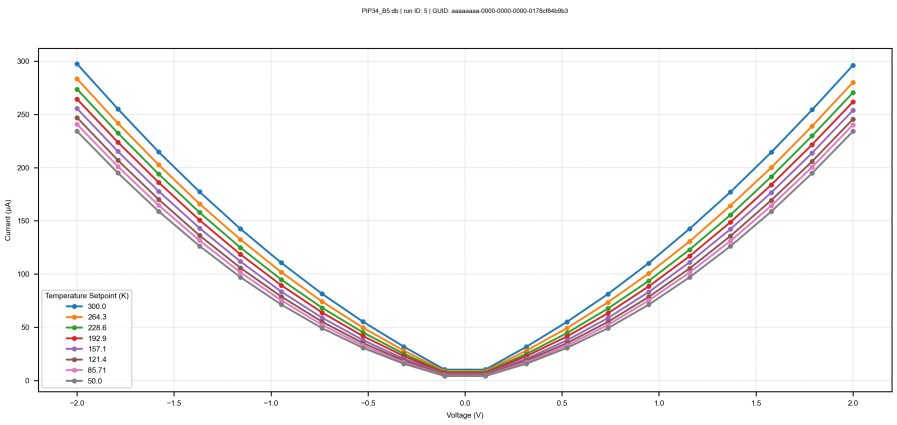


Figure 4.6: Temperature analysis of current-voltage characteristics obtained by two-wire measurements of Ti/Au metal-semiconductor contacts. The lower the temperature, the higher the contacts resistance. As the temperature decreases, the thermionic emission at the metal-semiconductor junction decreases, because the thermal energy of the electrons is not sufficient to overcome the Schottky barriers.

As expected, the Schottky barriers increase as the temperature decreases. To better explain this phenomenon, it is necessary to consider the main source of electronic transport through the metal-semiconductor junction: the thermionic emission. Since the probability that an electron overcomes the potential barrier increases as the thermal energy possessed by the charge increases, if the temperature decreases the thermal energy of the electron decreases. If it decreases, consequently the current flowing through the junction decreases as well, and the resistance increases. The thermal characterization is even more useful if performed on an ohmic contact. In this way, it is possible to establish which is the operating temperature of the device as the temperature decreases. There is a limit temperature at which the ohmic contact assumes a rectifying behavior because the electrons do not have enough energy to overcome the potential barrier anymore. That temperature establishes the operating range of the device.

Chapter 5

Schottky barriers height

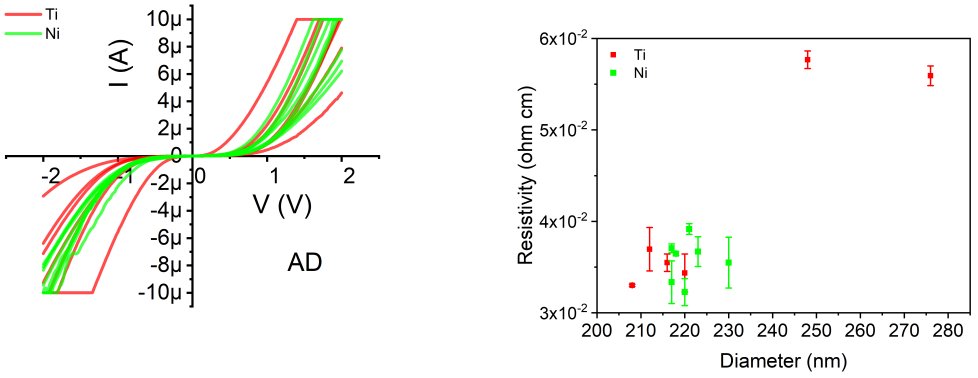
In Section 2.1 the formation of Schottky barriers at the metal-semiconductor interfaces has been treated from a theoretical point of view. The goal of this chapter is to experimentally measure the height of the Schottky barriers. Knowing the Equation 2.10, which relates current and voltage at the junction, the aim is to fit the experimental data obtained from the I-V measurements to estimate the height of the potential barriers. Also, to verify that Fermi level pinning occurs, the same two-wire measurements are repeated with contacts made of different metals. If Fermi level pinning does not occur, then changing the metal should also change the work-function of the metal and consequently vary the height of the potential barriers. On the contrary, if the height of the Schottky barriers does not depend on the work function of the metal it means that it is necessary to find a further solution for Fermi level depinning from the energies where the surface states density peaks.

5.1 Comparison between Ti and Ni contacts

As explained in the introduction of this chapter, different metals have been implemented for the metal contacts to analyze the Fermi level pinning issue. Some contacts consist of 10 nm of Ti and 150 nm of Au, while the others are composed of 50 nm of Ni covered by 50 nm of Au. However, what characterizes the contact behavior is only the interface between Ti or Ni and SiGe. If no Fermi level pinning occurs, the height of the potential barrier depends on the Ti or Ni work function.

Before estimating the height of the Schottky barriers, a comparison between the two and four wire measurements obtained from the Ti/Au and Ni/Au contacts is reported. From Figure 5.1a it can be clearly seen that the variability of the I-V curves between the nanowires is lower in the case of Ni contacts. Less variability means greater reproducibility, therefore greater reliability in the results, which is very useful for comparing measurements obtained on different chips and with different processes. Looking at the resistivity graph in Figure 5.1b, it can be noticed that the variability in this case is similar to the previous case. This is due to the fact that during the four-wire measurements the contribution of the metal contacts is removed, therefore the variation of the metal does not impose a variation in the

measurement obtained.



(a) (b)

Figure 5.1: Comparison between Ti/Au and Ni/Au contacts as regards **(a)** the current-voltage characteristics and **(b)** the resistivity of the nanowires.

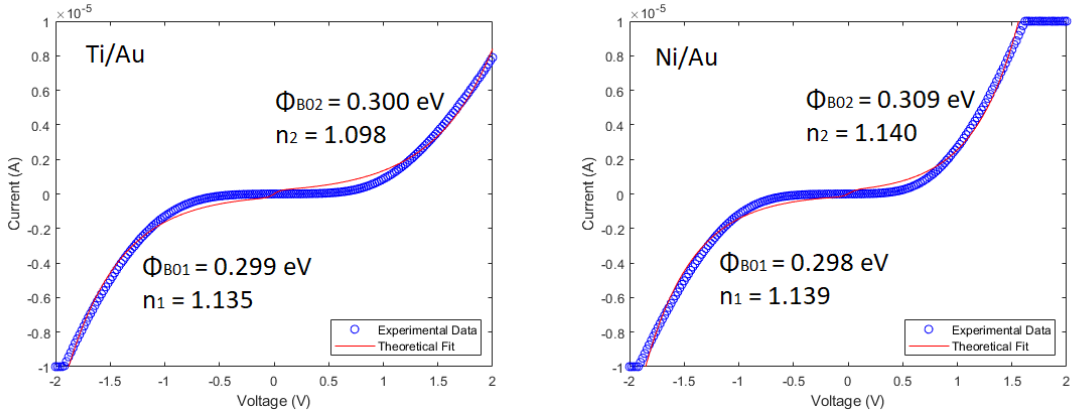
5.2 SBH and Fermi level pinning

To obtain an estimate of the height of the Schottky barriers it is sufficient to fit the current-voltage curves obtained from the two-wire measurements with the equation that regulates the current flow at the metal-semiconductor junction. Equation 2.10 describes the current-voltage relationship across the back-to-back connected asymmetric Schottky diodes, but does not take into account the non-ideality factors that make the height of the potential barriers dependent on the applied voltage. Therefore, as explained in Section 2.1, it is necessary to insert Equation 2.11 inside the first one, otherwise the concavity of the curve is opposite to that investigated.

The equation depends on three parameters that define the shape of the I-V curves. These parameters affect the reverse saturation current, which is the limiting factor for the current that can flow through the junctions. Since the two diodes are back to back connected, when one diode is forward biased the other one is reverse biased. Therefore, it is the reverse biased diode that makes the current to saturate at high voltages. As a consequence, the current is limited by the contact area and the height of the potential barrier, which are the limiting factors of the reverse saturation current. A larger contact area lets more current flow, so the reverse saturation current increases as the contact area increases. On the contrary, as the potential barrier increases, the flow of electrons becomes more difficult, this means that the higher the barrier, the lower the inverse saturation current. Furthermore, the decrease in current is exponential with respect to the height of the Schottky barrier. The third factor that affects the trend of the I-V curves is the ideality factor. It defines the concavity of the curve around zero. It is essential to obtain a good fitting.

To prevent the fitting error from being too large, the parameters to be estimated were limited to reasonable intervals before performing the computation. The contact area can be estimated from the SEM images. It turns out to be about $2 \times 10^{-13}\,\mathrm{m}^2$,

but it must be taken into account that there could be gaps between the metal and the semiconductor that could reduce the contact area. Furthermore, the hexagonal morphology of the nanowires could cause further errors. The ideality factor has been limited to assume valid values, which means values greater than 1. However, values slightly greater than 1 are sufficient to obtain a suitable result. Finally, the height of the potential barriers has been limited to a very wide range because it is difficult to be estimated a priori.



(a) (b)

Figure 5.2: I-V characteristics for **(a)** Ti/Au and **(b)** Ni/Au contacts. The blue circles represent the experimental data, while the red lines are the fitting curves from Equation 2.10, with the SB heights and the ideality factors as fitting parameters.

Figure 5.2 shows the I-V characteristics of two devices whose contacts are made of different metals. The curves obtained from the thermionic emission equation are superimposed on the experimental data, demonstrating the good fitting. The contact area is assumed to be equal because the manufacturing process is the same for both the chips. The heights of the Schottky barriers and the ideality factors result to be $\phi_{B01} = 0.299\,\text{eV}$, $n_1 = 1.135$, $\phi_{B02} = 0.300\,\text{eV}$, $n_2 = 1.098$ for the nanowires contacted by Ti/Au and $\phi_{B01} = 0.298\,\text{eV}$, $n_1 = 1.139$, $\phi_{B02} = 0.309\,\text{eV}$, $n_2 = 1.140$ for the nanowires contacted by Ni/Au. However, from the literature the Ti work function is 4.33 eV, while Ni has a work function of 5.35 eV. It is clear that the Schottky-Mott rule reported in Equation 2.1 does not yield an accurate estimate of the barriers' heights, because from the experimental results the heights of the potential barriers obtained by varying the metal should differ much more than that. This can only mean that the Fermi level is pinned at the interface states energies. As a consequence, it is not sufficient to change metal for the contacts to obtain an ohmic behavior, but it is necessary to highly dope the contacts areas, as it will be explained in Chapter 7.

A good fitting was obtained by narrowing step by step the intervals of the parameters that define the equation, according to a non-linear least squares method, that minimizes the sum of the squared residuals. To evaluate the goodness of the fit, the coefficient of determination, also called R-squared, and denoted by R^2, was evaluated. R-squared is a statistical measure of how close the data are to the fitted

regression line, that is the curve that best fits the data. The data are denoted by y_i, while $\bar{y}$ is their mean. In addition, their associated fitted values are pointed out as $\hat{y}_i$.

First, it is necessary to defined the sum of squares (SSR) and the total sum of squares (SST), respectively:

$$SSR = \sum_i (\hat{y}_i - \bar{y})^2 \tag{5.1}$$

$$SST = \sum_i (y_i - \bar{y})^2 \tag{5.2}$$

Then, the coefficient of determination can be expressed as:

$$R^2 = \frac{SSR}{SST} \tag{5.3}$$

This parameter gives an estimation of how successful the fit is in explaining the variation of the data. Generally, the higher the R-squared value, the better the model fits the data, in a range between 0 and 1. The accounted value for the Ti/Au contacts is 0.989, while the value for the Ni/Au contacts is 0.988.

Chapter 6

Thermal annealing tests

In the previous chapter the Schottky barrier height has been estimated and it has been verified that Fermi level pinning occurs. The aim of this chapter is to lay the groundwork for Chapter 7, which will deal with obtaining ohmic contacts in a controlled manner. However, before doing that, it is very useful to perform some annealing tests for three main reasons: to check which is the melting temperature of hexagonal SiGe, which is the limit temperature below which the material does not suffer damage to the crystalline structure and finally which is the effect of temperature on the core/shell structure in terms of inter-diffusion between SiGe and GaAs. In addition, some annealing tests at lower temperatures were also carried out to evaluate the effect of Ni diffusion on the character of the contacts.

6.1 Carrier concentration estimation

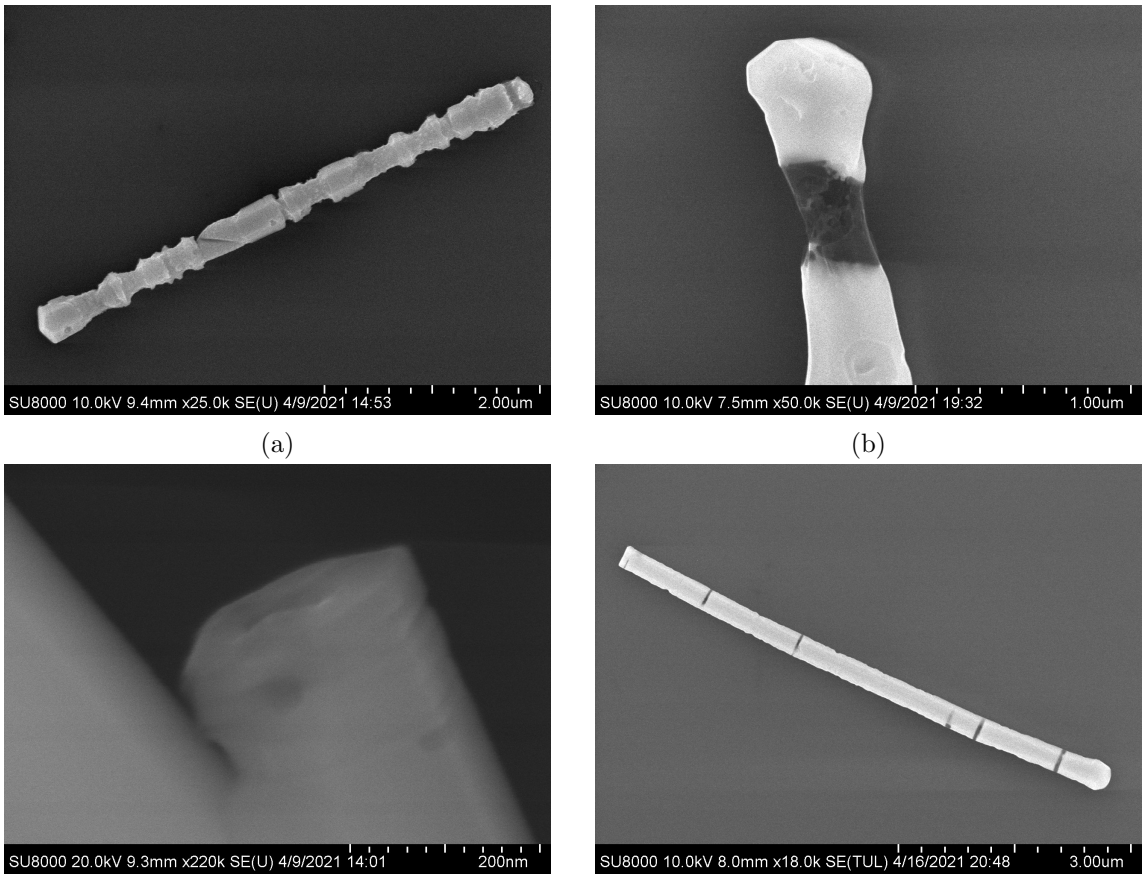
Considering that hexagonal SiGe is a novel material, no data are available regarding its melting temperature or the temperature at which the crystal lattice gets damaged or assumes the cubic phase. However, considering that the nanowires used in this thesis are composed of 80% germanium, the melting point should be located in the melting temperatures range of silicon and germanium tending to that of germanium. Figure A.4 shows the transition curve between solid and liquid phases of cubic $Si_{1-x}Ge_x$ binary alloys. The curve that defines the melting points is well fitted by the following equation [19]:

$$T_s \approx 1412 - 738x + 263x^2 \,(^\circ\mathrm{C}) \tag{6.1}$$

where T_s is the melting temperature and x is the germanium content.

It is easy to calculate that the melting temperature of cubic SiGe alloys should range between 1412 °C and 937 °C. For this reason, some preliminary tests are carried out from high temperatures to lower temperatures for different annealing times to check which is the most suitable temperature and time combination not to damage the hexagonal SiGe crystalline structure. This is done by rapid thermal annealing using Ar and H_2 as inert gases. The response of the annealing tests is verified by SEM

analysis and is reported in Figure 6.1. By SEM images it can be argued whether the lattice is damaged or not and whether crystal defects arise or not. At 900 °C for 6 s (Figure 6.1a) and at 850 °C for 600 s (Figure 6.1b) hexagonal SiGe, differently from cubic SiGe, looks melted. This phenomenon will be further investigated in the next chapter, after GaAs core wet etching. The hexagonal SiGe without the GaAs core will result undamaged even at 900 °C for 6 s. This means that SiGe alone does not melt at 900 °C, but the intensive inter-diffusion of SiGe with GaAs heavily damages the nanowires' morphology. At 850 °C for 6 s (Figure 6.1c) and at 800 °C for 600 s (Figure 6.1d) the nanowires do not look melted, but their crystalline structure is damaged, so the temperature still need to be decreased.



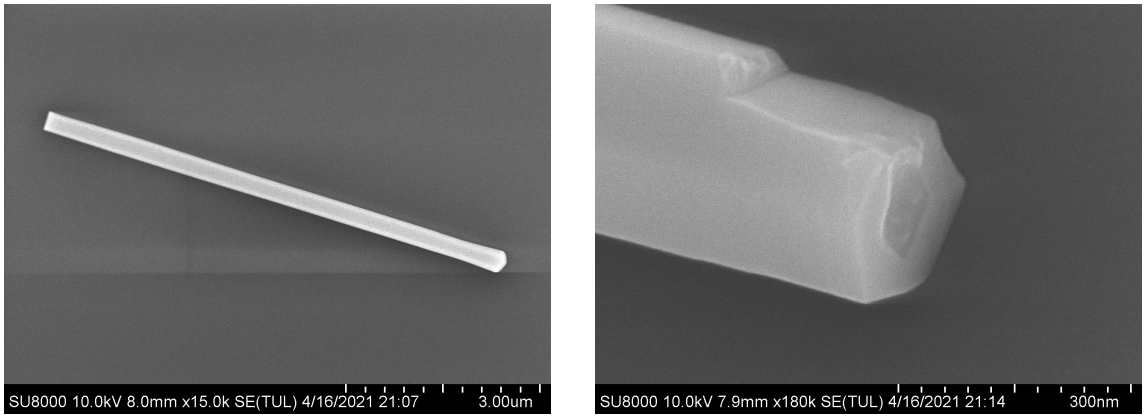
(a) (b)

(c) (d)

Figure 6.1: SEM images resulting from annealing tests for different temperature and time combinations: **(a)** 900 °C 6 s, **(b)** 850 °C 600 s, **(c)** 850 °C 6 s, **(d)** 800 °C 600 s.

Maintaining the temperature at 800 °C, but decreasing the annealing time to 6 s, the hexagonal morphology of the SiGe nanowires is undamaged and there are no visible damages to their structure, as clearly visible by Figure 6.2. Then, the annealed nanowires have been electrically characterized to analyse the effect of the temperature on the electrical properties of the material and on the behavior of the metal contacts.

Unexpectedly, from two-wire measurements the metal contacts turn out to be ohmic, as shown in Figure 6.3. As explained in Section 2.3.1, increasing the semiconductor



(a) (b)

Figure 6.2: SEM images resulting from the 800 °C 6 s annealing test.

doping level makes the depletion region thinner. As a consequence, also the potential barrier at the metal-semiconductor interface becomes thinner. This effect enhances the electrons tunneling through the barriers and the contacts assume an ohmic behavior. However, to increase the semiconductor doping concentration it is necessary to introduce dopant impurities into SiGe. These dopants have not been introduced by external, but the contacts result to be ohmic after rapid thermal annealing. This consequence is probably due to the combination of two different effects: the thermal activation of As impurities that have been trapped in SiGe during the nanowires growth process, as explained in Section 1.1, and the net doping concentration at the contacts interfaces resulting from the thermal diffusion of As impurities from the GaAs core of the nanowires. Dopants activation means electrical activation of the dopants wherein free electrons are released when dopant atoms move into substitutional lattice sites, increasing the carrier concentration. As regards the thermal diffusion of dopants from the GaAs core, it introduces a higher carrier density at the metal-semiconductor interfaces that enhances the electrons tunnel effect leading to ohmic contacts.

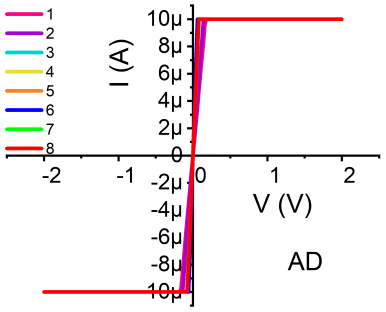
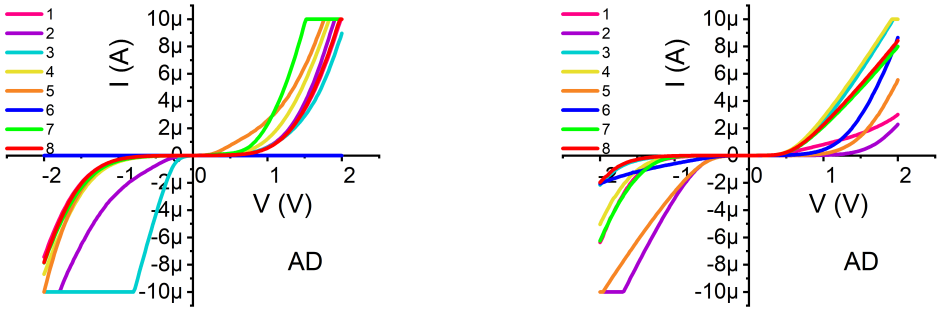


Figure 6.3: Current-voltage characteristics obtained by two-wire measurements of Ni/Au metal-semiconductor contacts carried out on 800 °C 6 s annealed GaAs/SiGe core/shell nanowires. The behavior of the metal-semiconductor junctions is ohmic.

Considering that the I-V characteristics behavior is ohmic, the TLM method described in Section 2.2 can be carried out to estimate the contact resistivity. The contact resistivity measures $1.32 \times 10^{-6}\,\Omega\,\mathrm{cm}$, that is a very low value, but in trend with other results reported in literature. This value will be compared with the contact resistivities resulting by solid-state diffusion doping in Figure 7.15.

Finally, other annealing tests have been performed to find out whether a lower temperature is sufficient to obtain ohmic contacts or not. Both at 750 °C for 6 s (Figure 6.4a) and at 700 °C for 6 s (Figure 6.4b) the I-V characteristics still show a rectifying behavior, meaning that the the resulting thermal diffusion of dopants is not sufficient.



(a) (b)

Figure 6.4: Current-voltage characteristics obtained by two-wire measurements of Ni/Au metal-semiconductor contacts carried out on **(a)** 750 °C 6 s and **(b)** 700 °C 6 s annealed GaAs/SiGe core/shell nanowires.

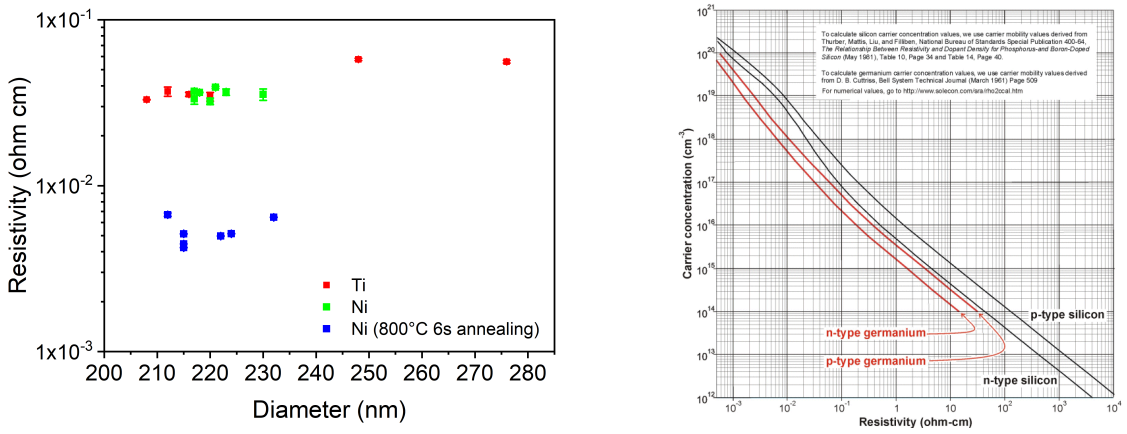
Table 6.1 reports a summary of the results obtained by the annealing tests for different temperature and time combinations.

Table 6.1: Results carried out by annealing tests on GaAs/SiGe core/shell nanowires.

	6 s	600 s
900 °C	Melted	
850 °C	Damaged	Melted
800 °C	Ohmic	Damaged
750 °C	Rectifying	
700 °C	Rectifying	

As for contact resistivity, also the resistivity of SiGe decreases after rapid thermal annealing. Figure 6.5a compares the resistivity measured before and after 800 °C 6 s annealing. It has been reduced by one order of magnitude. The resulting resistivity measures $5 \times 10^{-3}\,\Omega\,\mathrm{cm}$. The resistivity value is useful for the estimation of the carrier concentration in the semiconductor. By Hall effect measurements it is possible

to extrapolate carrier concentration vs resistivity curves. As for the melting temperature, also the carrier concentration vs resistivity curves are unknown for hexagonal SiGe, because it is a novel material, so no data are available in literature. However, data collected by silicon and germanium can provide useful information. The graph depicted in Figure 6.5b reports the carrier concentration vs resistivity curves for both n-type (P-doped) and p-type (B-doped) silicon and germanium. Hall effect measurements have not been carried out on hexagonal SiGe, but the curves calibrated for germanium should provide a good estimation for the carrier concentration in the novel material. By this curves the carrier density before annealing is of the order of $10^{17}\,\mathrm{cm}^{-3}$. It was expected to be slightly higher, considering that a higher density of As impurities should be introduced in SiGe by the GaAs substrate during the high temperature growth process, as can be deduced by the atom probe tomography (APT) characterization of hex-$Si_{0.25}Ge_{0.75}$ nanowires reported in Figure 6.6. By the APT characterization, the incorporation of approximately 200 ppm of As impurities is observed in the entire SiGe shell, while the Ga concentration quickly drops to a value close to the noise level. This means that the estimated low carrier concentration is probably due to the inactive dopants. After the rapid thermal annealing the carrier concentration increases, resulting to be of the order of $10^{18}\,\mathrm{cm}^{-3}$.



(a) (b)

Figure 6.5: **(a)** Resistivity values comparison between GaAs/SiGe core/shell nanowires before and after 800 °C 6 s annealing. **(b)** Carrier concentration vs resistivity curves obtained by Hall effect measurements for both n-type (P-doped) and p-type (B-doped) silicon and germanium [20, 21].

This can be explained looking at the diffusion coefficients of As and Ga into the germanium crystal lattice. By the graph in Figure 6.7a the Ga diffusivity into germanium appears to be a few orders of magnitude lower than that of As at 800 °C. As a consequence, during rapid thermal annealing, the dose of As impurities diffusing from the GaAs core into SiGe is much higher than that of Ga. The result is a net doping density dominated by As atoms. Furthermore, it is known that doping diffusion increases exponentially with temperature. Figure 6.7b reports the As content into a Ge thin film introduced by a GaAs substrate at different temperatures.

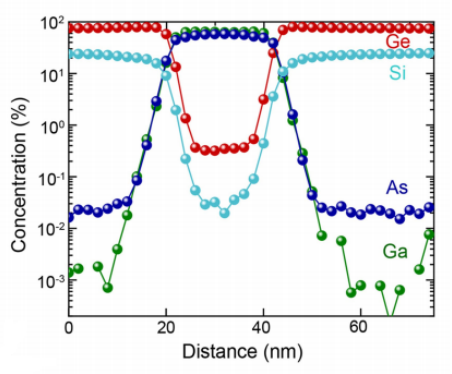
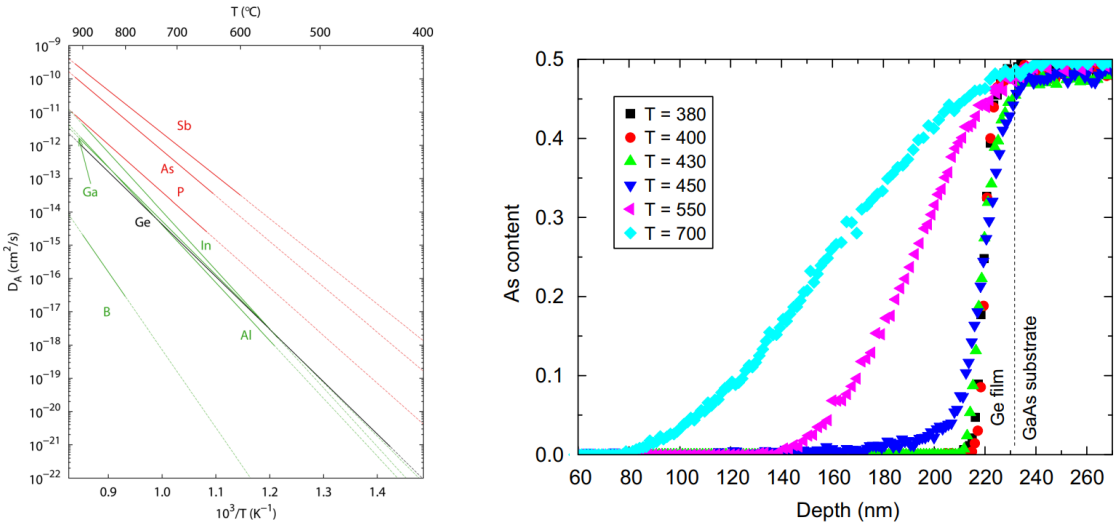


Figure 6.6: Atom probe tomography characterization of hex-$Si_{0.25}Ge_{0.75}$ nanowires showing the atomic species concentration as a function of the radial distance across the core/shell structure [2, 3].

It is easy to observe that As doping can penetrate through the germanium crystal lattice for hundreds nanometers at 700 °C. This means that As can penetrate from the GaAs core to the nanowires' external surface, where the metal contacts are established. This is a further proof that explains the ohmic behavior of the metal-semiconductor contacts. Moreover, the higher the distance from the GaAs core, the lower the compensation of As impurities by Ga atoms, because Ga requires longer time to penetrate deeply.



(a) (b)

Figure 6.7: **(a)** Diffusion coefficients of the n-type dopants (red lines): phosphorus (P), arsenic (As), and antimony (Sb) in Ge compared to Ge self-diffusion and to the p-type dopants (green lines): boron (B), aluminum (Al), gallium (Ga), and indium (In). Each solid line spans the range of the respective experimental results, and the corresponding dashed line indicates an extrapolation to lower and higher temperatures [22]. **(b)** SNMS profiles for As into Ge layer for Ge/GaAs epitaxy at different temperatures [23].

6.2 Nickel diffusion

In Chapter 5, nickel was used in place of titanium to check if Fermi level pinning occurred. However, it can also act as a reservoir for Ni diffusion into SiGe. The aim of this section is to verify whether Ni diffusion can be exploited to obtain ohmic contacts or not. The contact resistivity achieved with this method will be compared with the values obtained by solid-state diffusion doping in Chapter 7.

Metal contacts composed by 50 nm of Ni covered by 50 nm of Au were achieved for this purpose. It is necessary that the nickel layer is thick enough so that the reservoir does not run out during the diffusion process in order to obtain a good result. The Ni diffusion is performed by means of rapid thermal annealing. During this process two main phenomena occur: the inter-diffusion between Ni and SiGe and the formation of NiSiGe. They are both responsible to alleviate the Fermi level pinning, so Ni diffusion is a good candidate to obtain ohmic contacts. The formation of NiSiGe at the interface between Ni and SiGe by RTA is proven by Xiong-Xiong Du et al. [24]. First, they deposited Ni on SiGe by sputtering, then they annealed the samples at 400 °C for 30 s. The results are verified by TEM analysis, as shown in Figure A.5, where the mono-crystalline NiSiGe layer is formed between Ni and SiGe. Finally, the contact resistivity has been proven to be much lower than before.

As regards the purpose of this thesis, the first objective is to investigate which is the most suitable temperature range combined with an annealing time of 6 s. The first attempt was made with a temperature of 300 °C, but the electrical characterization following the process produced only open contacts. This means that the diffusion of nickel occurred too quickly, completely emptying the metal reservoir and producing voids between the Au layer and the SiGe surface. A second test was made with a temperature of 280 °C, but it did not produce notable results. Considering that the Schottky barriers were still present, the diffusion of nickel was not sufficient to alleviate the Fermi level pinning. Therefore, the ideal temperature should be in the range between these two limiting temperatures. Indeed, a promising result was obtained by an annealing temperature of 290 °C. The majority of the Schottky contacts turned into ohmic contacts. However, the randomness of the I-V curves reported in Figure 6.8 makes it difficult to analyze the obtained data.

The randomness of the I-V curves is due to the irregularities created between Au and SiGe during nickel diffusion. Some cavities are formed during emptying of the Ni reservoir, so the path taken by the current turns out to be random. The cross sectional area of the conducting material differs between one contact to another, so also the contact resistivity shows the same behavior. The morphology of nickel after diffusion is depicted in Figure 6.9.

Measurable results have been obtained at 288 °C for 6 s. The contact resistivity has been obtained by TLM method on the I-V curves shown in Figure 6.10 and it measures $3.47 \times 10^{-3}\,\Omega\,\mathrm{cm}$. However, the contact resistivity results to be still too high to be competitive with the value obtained by the 800 °C 6 s annealing of the GaAs/SiGe core/shell nanowires. These values will be compared with the contact resistivities resulting by solid-state diffusion doping in Figure 7.15.

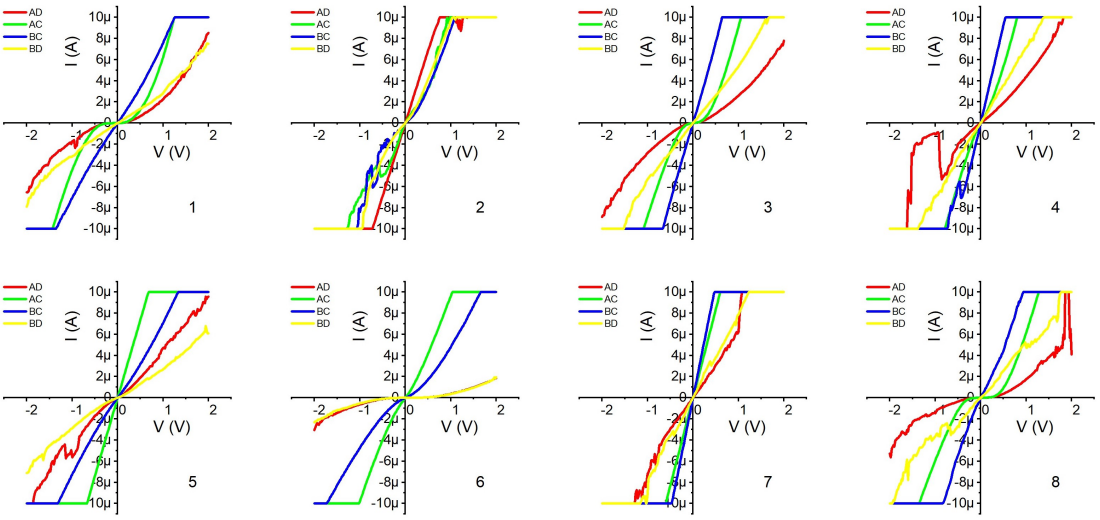
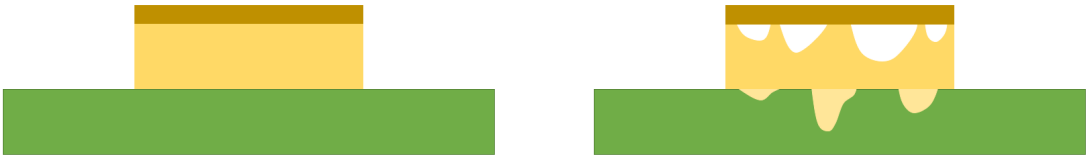


Figure 6.8: Current-voltage characteristics obtained by two-wire measurements of Ni/Au metal-semiconductor contacts after 290 °C 6 s Ni diffusion. The randomness is due to the irregularities created between Au and SiGe during nickel diffusion.



(a) (b)

Figure 6.9: Schematic cross-section of the Ni diffusion process into the SiGe layer **(a)** before and **(b)** after rapid thermal annealing.

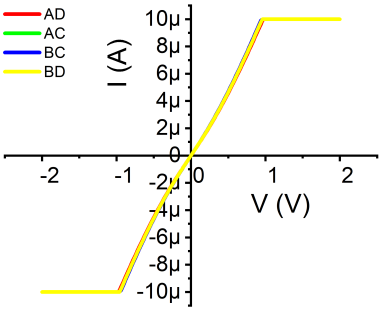


Figure 6.10: Current-voltage characteristics obtained by two-wire measurements of Ni/Au metal-semiconductor contacts after 288 °C 6 s Ni diffusion.

Chapter 7

Ohmic contacts

This is the last chapter that concludes the thesis and completes the main purpose of this project: obtaining ohmic contacts at the metal-semiconductor interface to minimize the contact resistivity and, consequently, the power dissipation, as well as analyzing the electrical response of the novel material to the doping process. The previous chapters have been fundamental in achieving this goal. It was necessary to analyze the reasons for the rising of Schottky barriers at the metal-semiconductor junctions to find a way to reduce or overcome them. Furthermore, the annealing tests have been useful to define the temperature range at which dopants have a diffusion coefficient high enough to present a remarkable response, but at the same time not to melt or damage the crystalline structure of the nanowires. Finally, during the annealing tests it turned out to be necessary to etch the GaAs core away to avoid that it interfered with the results during the thermal annealing process for dopants diffusion. As a consequence, the first aim of this chapter is to pursue the most proper way to etch the GaAs core away from the core/shell nanowires' structure. Then, the doping by diffusion process will be investigated in order to achieve ohmic contacts by reducing the thickness of the Schottky barriers. Finally, the contact resistivity will be measured and compared with the previous results to ensure the effectiveness of the method employed.

7.1 GaAs core etching

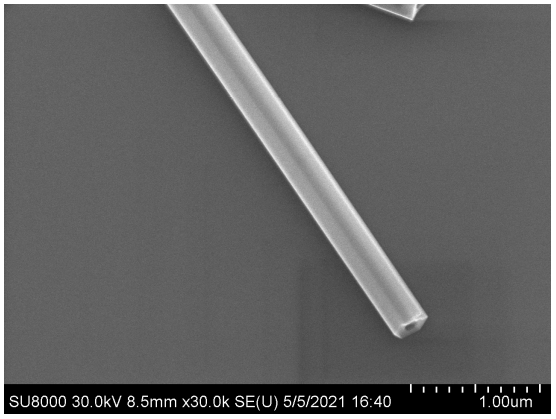
In Section 6.1 it has been demonstrated that As and Ga impurities from the core of the GaAs/SiGe core/shell nanowires can diffuse into SiGe if thermally annealed increasing the doping concentration. This phenomenon is useful for obtaining ohmic contacts, that is the aim of this thesis, but it depends on the GaAs core. The ultimate goal is to grow hex-SiGe substrates without the presence of the GaAs core, that is necessary for the growth process of the material. Therefore, it is necessary to manage the doping process from outside, without relying on the presence or not of the GaAs core.

As a consequence, the etching of the GaAs core from the nanowires' structure is a necessary step to analyse the effect of doping by diffusion without the interference

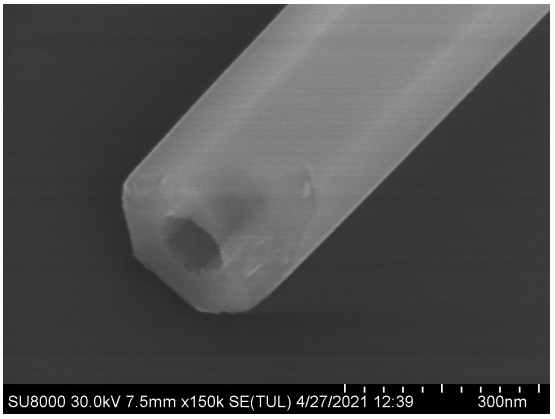
of As and Ga dopants during rapid thermal annealing. However, it is necessary to selectively etch the GaAs core over the SiGe shell. Peroxide solutions have been demonstrated to etch III-V group semiconductor materials, but in this case they must be excluded because they would oxidize SiGe, damaging its structure. An effective solution for the selective wet etching of GaAs over SiGe has been refined by A. Turala et al. [25]. They immersed the samples in a bromine-methanol solution having a bromine concentration of 1%, whose molecular formula is $Br_2 - CH_2OH$. This solution is a well known non-selective etchant for nearly all III-V semiconductors able to selectively etch III-V materials over Ge. The reported average rate of bromine-methanol towards III-V materials is of 1 µm/min. The same process is repeated and the same bromine concentration is achieved to etch the GaAs core of the nanowires. Due to the volatility of bromine, the solution mixture is covered during the etching and no agitation is used in order to minimize bromine evaporation. However, the etching rate results to be much lower than 1 µm/min. The reason is that the etching does not take place over the entire surface of the core, because much of the surface is covered by the SiGe shell. As a consequence, the etching rate decreases with time, because the diffusion of bromine-methanol becomes more and more difficult as the core is etched. Also, one of the sides of the nanowire is capped, otherwise the time to completely etch the core would be less than half. So, the average etch rate results to be about 58 nm/min. Furthermore, considering that the SiGe shell is about 60 nm thick, while the nanowires are about 6 µm long, the required selectivity between GaAs and SiGe etch rates is supposed to be much higher than 100, otherwise the SiGe shell would be completely etched during the GaAs core etching. This requirement is not easy to achieve, so it is necessary to stop the etching process as soon as the core has been completely etched. If the nanowires are immersed for too long, the bromine-methanol solution can start to etch the SiGe shell at one end of the nanowires. If the nanowires are too long to avoid this side effect before the GaAs complete etching, it is necessary to exclude the damaged portion of the nanowires from electrical contacting.

This issue is pointed out by the results obtained from two different batch of nanowires. Sample H06794 is characterized by nanowires with an average length of 6 µm and an average shell thickness of 60 nm. As mentioned in the previous paragraph, these geometrical parameters require a GaAs/SiGe etch selectivity much higher than 100. Short nanowires with thick SiGe shells offer a double advantage: (1) the shorter are the nanowires, the shorter is the time needed to completely etch the GaAs cores, and (2) the thicker are the SiGe shells, the longer is the time needed to completely etch them, so (1+2) a lower selectivity is sufficient to completely etch the GaAs cores without completely etch the SiGe shells. Figure 7.1 proves that the selectivity provided by the bromine-methanol solution is high enough to completely etch the GaAs cores of this batch of nanowires without completely affect the SiGe shells, that still appear to be thick enough to be further processed. On the other hand, sample H06793 provides 8 µm long nanowires with 40 nm thick shells. The time needed to completely etch the GaAs cores increases more than linearly as the nanowires length increases, because the etching process is limited by the bromine-methanol diffusion. The GaAs/SiGe selectivity required by this sample is higher than 200. If

the bromine concentration or the etching time are not perfectly calibrated, the SiGe shells risk to be completely etched or pierced. Also, the variability that affects the length of the nanowires or the thickness of the shells can heavily decrease the yield of the etching process. The nanowires that have been affected by an excessive damage during this process are shown in Figure 7.2. Some of the nanowires have been only damaged on one side, so they can still be contacted on the remaining portion, while the other nanowires must be excluded. This results in a very low yield, as it will be further discussed in Section 7.4.

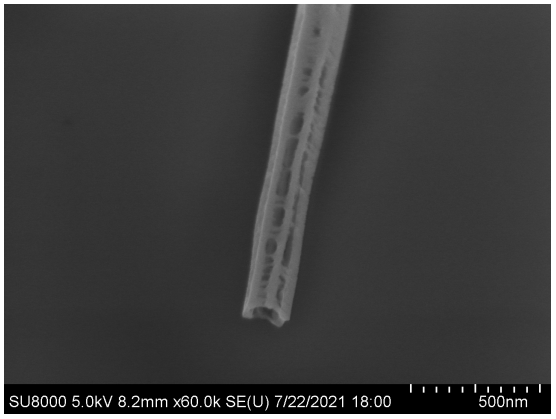


(a)

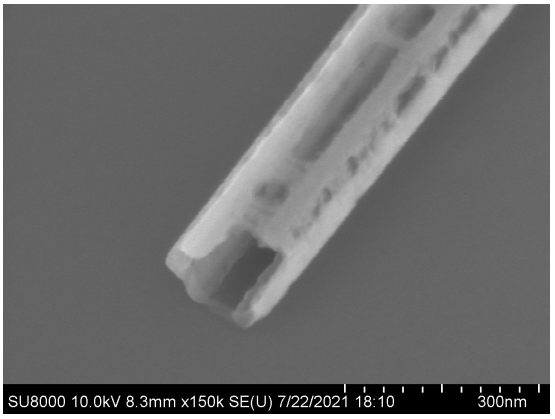


(b)

Figure 7.1: SEM images of the thick nanowires (sample H06794) after 60 min etching by bromine-methanol (time required to completely etch the GaAs cores of these short nanowires).



(a)

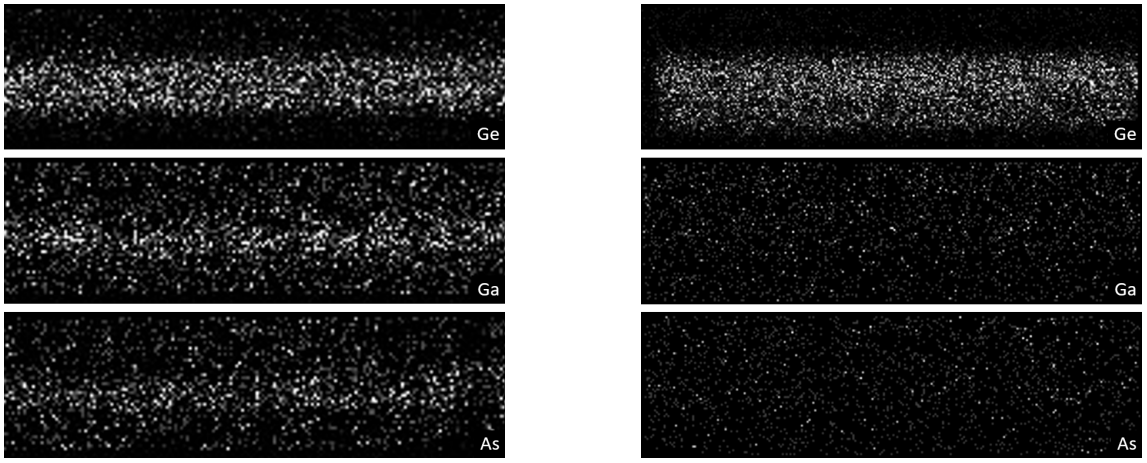


(b)

Figure 7.2: SEM images of the thin nanowires (sample H06793) after 150 min etching by bromine-methanol (time required to completely etch the GaAs cores of these long nanowires). The SiGe shells appear over-etched.

Energy-dispersive X-ray spectroscopy is employed in order to verify the complete success of the core etching, because a simple SEM analysis does not provide a clear result. The elements pointed out by EDS are Ge, As and Ga. The shells of the nanowires are made of 80% germanium and 20% silicon, but Si could not be distinguished by the signal coming from the Si substrate, while arsenic and gallium are the

elements that compose the GaAs core. First, GaAs/SiGe core/shell nanowires are analysed in order to have a reference for comparison before and after etching. These results are reported in Figure 7.3a, where it is possible to notice not only the signal coming from the entire Ge shell, but also both the signals coming from Ga and As, composing the GaAs core. Then, the same analysis is performed after immersing the nanowires in the bromine-methanol solution for the time it takes to completely etch the core. The process is completed when EDS provides the result depicted in Figure 7.3b. The signals coming from Ga and As are no longer distinguishable by noise, that means that the etching process has been completed.

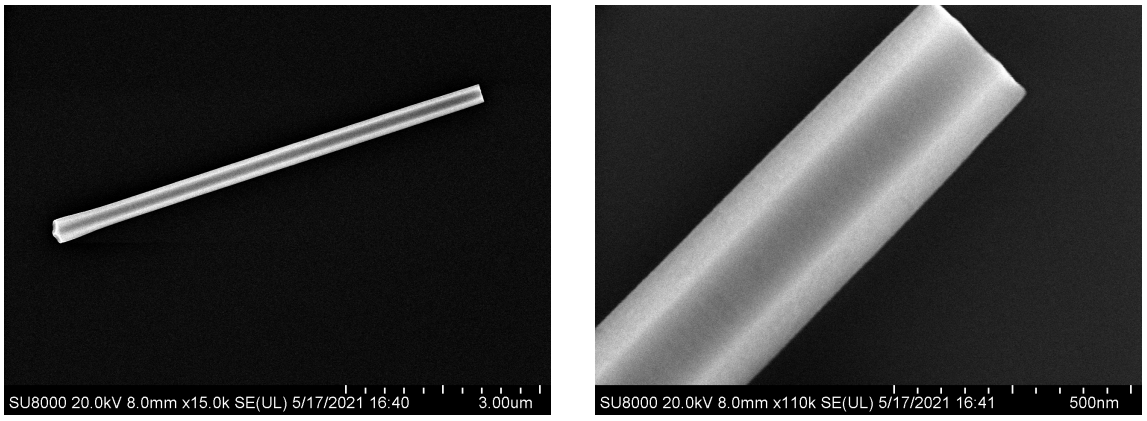


(a) (b)

Figure 7.3: Energy-dispersive X-ray spectroscopy of Ge, Ga and As in the GaAs/SiGe core/shell nanowires **(a)** before and **(b)** after core etching.

After GaAs core etching, some annealing tests have been carried out by rapid thermal annealing to compare the thermal stability of the nanowires without the GaAs core with the results obtained by the annealing tests performed on the nanowires with the GaAs core, as reported in Section 6.1. The thick nanowires (sample H06794) with the GaAs core did not survive neither at 850 °C for 6 s nor at 800 °C for 600 s. Differently, the thick nanowires (sample H06794) without the GaAs core can survive at 900 °C for 6 s, as shown in Figure 7.4, so they appear thermally more stable than the nanowires with the GaAs core, and the crystalline structure of the SiGe shell after rapid thermal annealing is confirmed to still be hexagonal by STEM analysis along the [0001] direction, as reported in Figure 7.5. The higher thermal stability is probably due to the impossibility of SiGe to interdiffuse with GaAs: if the Ge atoms cannot diffuse into the GaAs core, the SiGe shell structure is less affected by the annealing process. On the other hand, the thin nanowires (sample H06793) without the GaAs core start to decompose even at lower temperature than the thick nanowires (sample H06794) with the GaAs core. As demonstrated in Figure 7.6, the thin NWs decomposed at 720 °C for 300 s. This is probably due to the fragility of the SiGe shell after the etching process, which turns out to be very thin. However, the first annealing tests performed on the thin nanowires have been carried out by metal-organic chemical vapour deposition (MOCVD) in a H_2 and As atmosphere with the purpose of vapor-phase diffusion doping, so it is not really correct to compare

them with the previous results. For this reason, the thin nanowires have also been subjected to rapid thermal annealing tests which confirmed that they are more fragile than the thick nanowires since they melted at 750 °C for 300 s. Nevertheless, it should be noted that no annealing data is available on the thick nanowires for the same temperature and time combinations to directly compare the different results, so it needs further investigation.



(a) (b)

Figure 7.4: SEM images of the thick nanowires (sample H06794) without the GaAs core after 900 °C 6 s rapid thermal annealing.

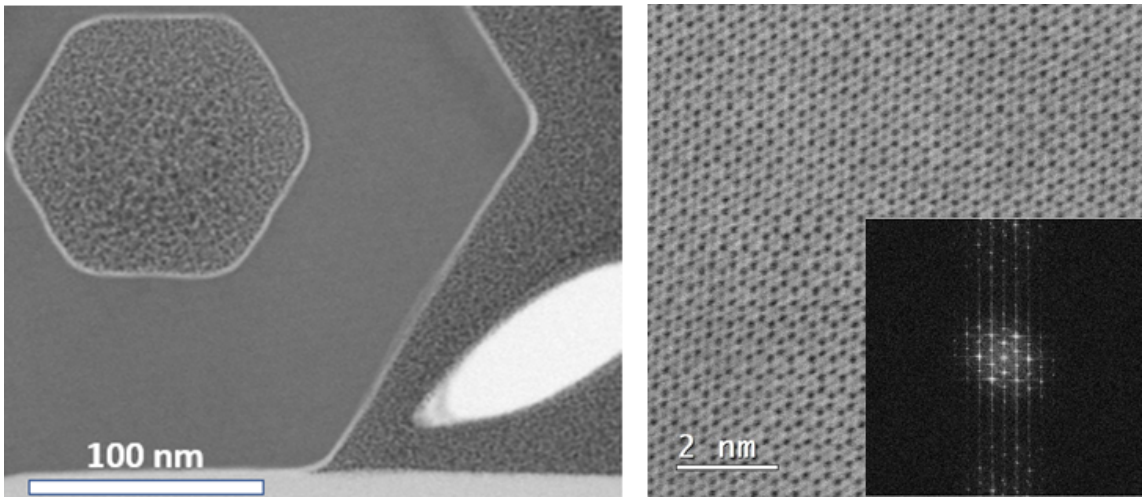
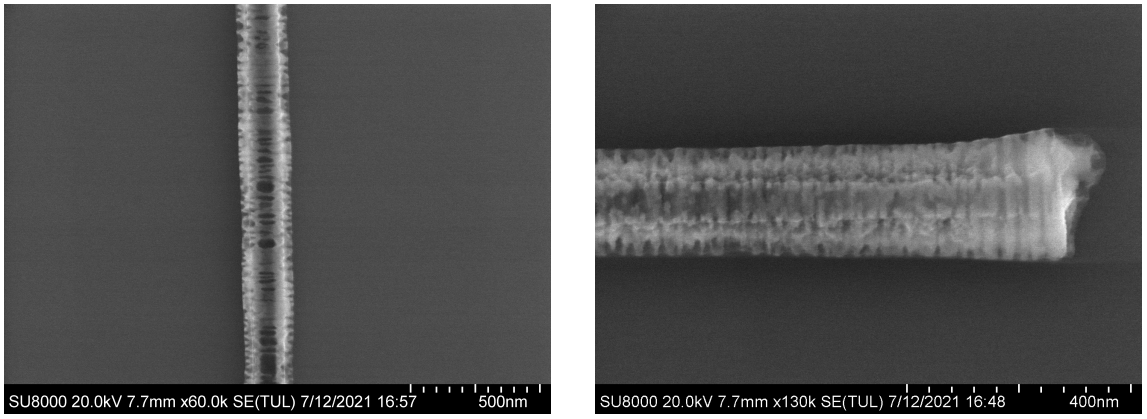


Figure 7.5: STEM images of the thick nanowires (sample H06794) without the GaAs core after 900 °C 6 s rapid thermal annealing highlighting the preserved hexagonal crystalline structure along the [0001] direction.

7.2 Doping by solid-state diffusion

Once the GaAs core has been selectively etched over SiGe, it cannot interfere with the external doping process anymore. In this section, the process flow that aims at the solid-state diffusion is described in details. Then, the obtained results are analysed by the electrical characterization of the doped nanowires.



(a) (b)

Figure 7.6: SEM images of the thin nanowires (sample H06793) without the GaAs core after 720 °C 300 s MOCVD thermal annealing.

7.2.1 Process flow

In order to dope the SiGe shell of the nanowires, some additional steps need to be added to the general process flow described in Chapter 3. The additional steps are depicted in Figure 7.7 and they will be described one by one in the following lines. Initially, the nanowires are deposited on the SiO_2 substrate as usual. Then the GaAs core is etched over SiGe, as reported in the previous section.

The next step consists in depositing a thin layer of SiO_2 by atomic layer deposition. Plasma enhanced ALD is used for this purpose because of its precise film thickness control, high uniformity and conformality. As a consequence, an equally thick SiO_2 layer grows on the entire exposed surface of the nanowires. The purpose of this silicon oxide layer is to work as a hard mask for solid-state diffusion, because it has to be stable despite the high temperatures necessary for the dopants to diffuse within the SiGe. A polymeric resist would completely melt if exposed to high temperatures during rapid thermal annealing. The effectiveness of the silicon oxide layer as a diffusion mask will be further investigated in Section 7.3. During the process, about 60 nm of SiO_2 are deposited on the surface of the nanowires. The material is grown at 300 °C, the chamber pressure is about 10 mTorr and an RF power measures 250 W. The flow rates of the metal and non-metal precursors are 100 SCCM for $[(CH_3)_2 N]_3 SiH$ and 50 SCCM for O_2, respectively, while the flow rate of Ar, that is employed as purge gas, measures 100 SCCM. The entire process requires 200 cycles to be completed.

After the deposition of the silicon oxide layer, it is necessary to pattern it in order to obtain a suitable mask for doping by diffusion. 370 nm of PMMA 950K are spun on the substrate as a photoresist for electron beam lithography. The resist is exposed in order to open the contacts areas that need to be doped. However, some of the nanowires are completely exposed. This nanowires will be completely doped, so their resistivity values will provide a useful estimation of the doping concentration. After the development of the resist, the SiO_2 is etched by BHF where the polymer has been exposed. The results of this first steps are reported in Figure 7.8.

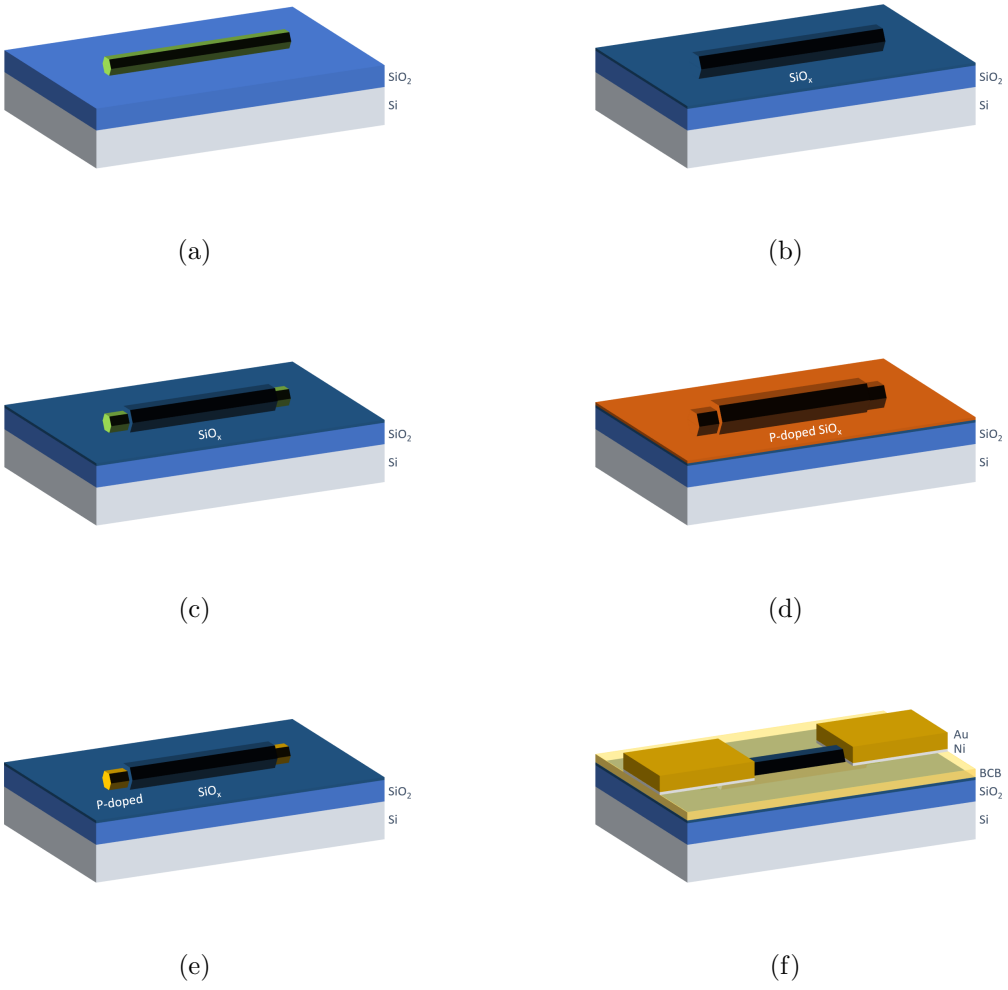
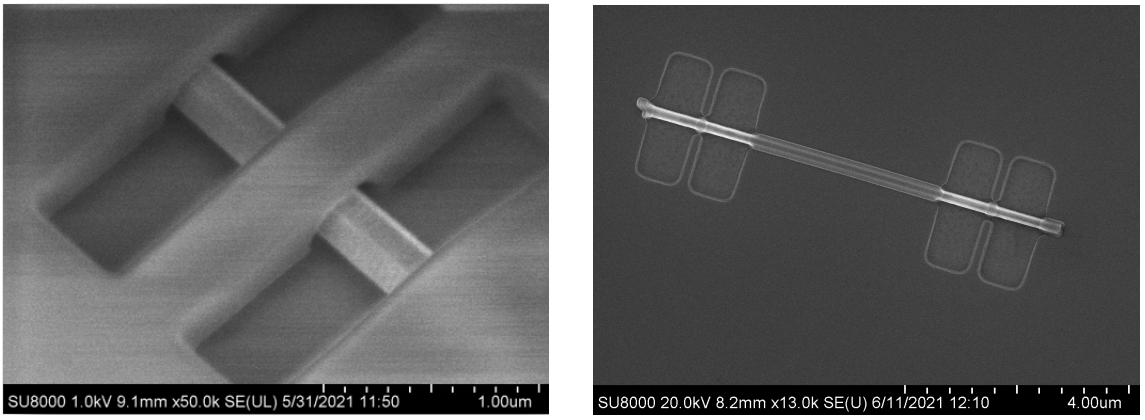


Figure 7.7: Schematics of the process flow for doping by solid-state diffusion of the SiGe nanowires after GaAs core etching. **(a)** Nanowires deposition. **(b)** Plasma enhanced atomic layer deposition of a SiO_2 diffusion mask. **(c)** Contacts opening by BHF after resist patterning by electron beam lithography. **(d)** Plasma enhanced chemical vapor deposition of a P-doped SiO_x layer followed by rapid thermal annealing for phosphorus diffusion into SiGe. **(e)** P-doped SiO_x removal by BHF. **(f)** Surface planarization followed by metal evaporation and lift-off.



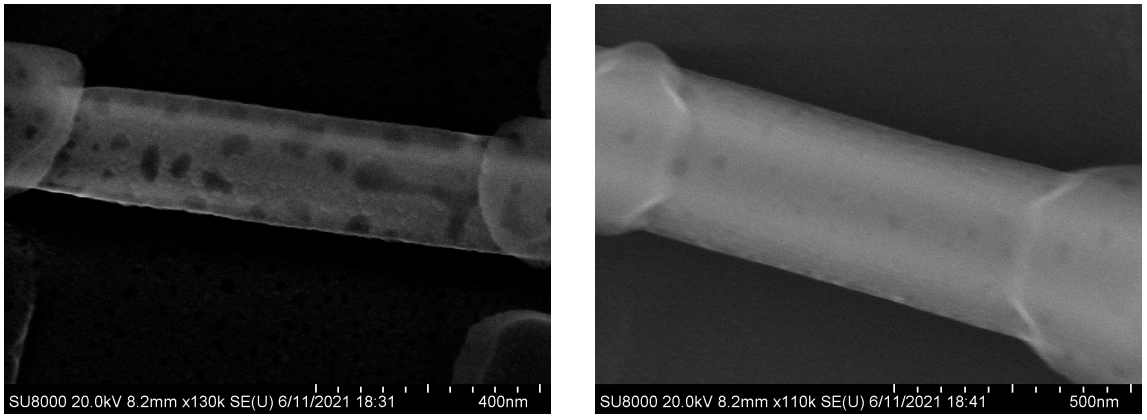
(a) (b)

Figure 7.8: SEM images showing the patterned SiO_2 diffusion mask **(a)** before and **(b)** after removing the resist.

At this point the SiO_2 hard mask for doping by diffusion is patterned. The next steps consist in the solid-state diffusion itself, as anticipated is Section 2.3. The deposition of a fixed dose of dopants is performed by PECVD. The selected dopant is phosphorus, that is a well-known n-type dopant for Si and Ge. Phosphorus atoms are deposited as impurities in P-doped SiO_x. The deposited scheme is composed by two layers. The first layer consists in P-doped SiO_x, while the next one is a SiO_x capping layer. The aim of the capping layer is to avoid outer diffusion during the thermal annealing process for phosphorus diffusion. If the phosphorus leakage is limited by the capping layer during the rapid thermal annealing, a high concentration of P atoms diffuse into the SiGe shell, resulting in a higher doping concentration. The deposited thickness of the two layers measures 20 nm each. This result is obtained at 300 °C, 150 mTorr and 20 W of RF power. The P-doped layer is grown by infusing 150 SCCM of SiH_4, 700 SCCM of N_2O and 50 SCCM of PH_3, while the capping layer is deposited with the same conditions except for the phosphine flux that is turned off. The aim of the solid-state diffusion is to heavily dope the contacts areas for a thickness of a few nm, so 20 nm of P-doped SiO_x can be approximated to an infinite reservoir for phosphorus diffusion, considering that the P concentration in SiO_x is of the order of $10^{20}\,cm^{-3}$.

The parameters that most influence the doping concentration at the interface between the P-doped SiO_x and the SiGe and the penetration depth within the hexagonal crystalline structure are the temperature and the time during rapid thermal annealing. As reported in Equation 2.27, the diffusion constant of phosphorus grows exponentially with the temperature, so increasing the temperature also increases the dopant dose diffused during the annealing process. However, the temperature should not exceed the limit beyond which the nanowires melt or get damaged, as discussed in Section 7.1. When the temperature limit has been reached, the most suitable way to increase the diffused dopant dose is to increase the annealing time. The experimental results obtained by different temperature and time combinations will be reported in Section 7.4, while the images of the nanowires after the deposition of P-doped SiO_x by PECVD and the solid-state diffusion process by RTA are shown

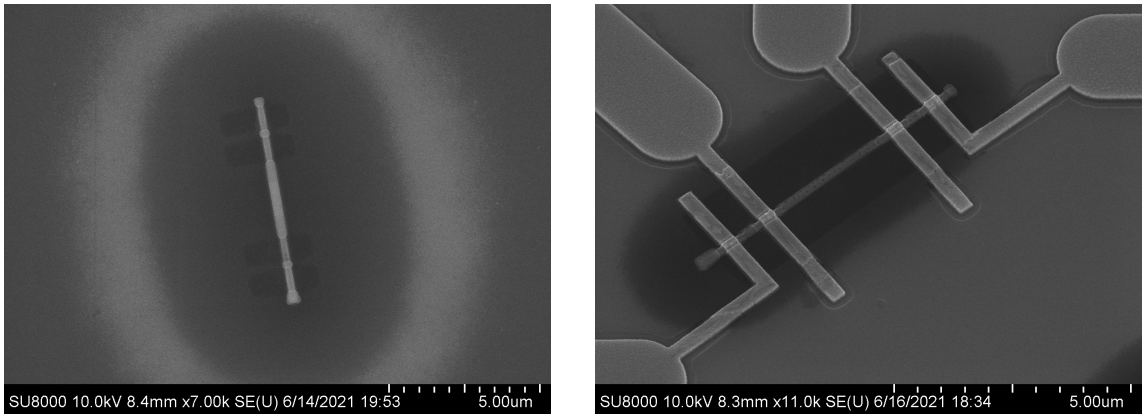
in Figure 7.9a for the sample annealed at 850 °C for 30 s and in Figure 7.9b for the sample annealed at 800 °C for 30 s.



(a) (b)

Figure 7.9: SEM images of the resulting nanowires after the deposition of P-doped SiO_x by PECVD and the solid-state diffusion process by RTA for **(a)** 850 °C 30 s and **(b)** 800 °C 30 s thermal annealing.

After the solid-state diffusion by rapid thermal annealing, the P-doped SiO_x is etched from the substrate by BHF. Finally, the common steps described in Chapter 3 complete the process, that consist in the planarization of the substrate by means of BCB, as shown in Figure 7.10a, and the metallization of the contacts as reported in Figure 7.10b.



(a) (b)

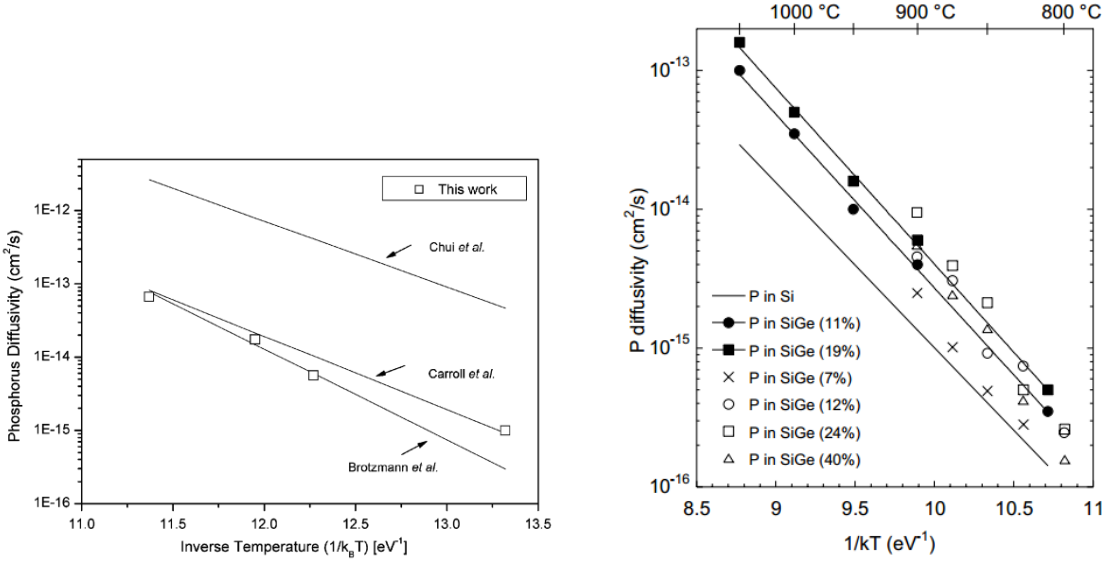
Figure 7.10: SEM images showing the nanowires **(a)** after the substrate planarization and **(b)** after the metallization of the contacts during the solid-state diffusion process.

7.3 SiO_2 diffusion mask

As anticipated in the previous section, a thin SiO_2 layer is conformally grown on the surface of the SiGe shell by ALD as a hard mask for solid-state diffusion. The thickness of the silicon oxide layer is about 60 nm. Then, the layer is patterned by

BHF etching to open the contacts areas which need to be doped in order to obtain ohmic contacts. However, the diffusivity of phosphorus into SiO_2 should be much lower than into SiGe so that the SiGe shell can achieve a sufficiently high doping concentration at the contacts areas without the phosphorus impurities being able to penetrate through the entire silicon oxide layer during the diffusion process. As hexagonal SiGe is a novel material which needs to be further investigated, no data about the diffusivity of phosphorus into this material are available in literature. Therefore, the most suitable approach to estimate its diffusivity is to define an interval within which this value can range.

Whereas this thesis deals with SiGe nanowires with 80% germanium content, the diffusivity of phosphorus in this material should be very close to that of germanium. P-diffusion in Ge is mainly mediated by vacancies. Its activation energy is 2.07 eV, which yields an attractive potential between the P-vacancy pair resulting in a large diffusion coefficient of P in Ge [26]. The diffusion coefficient of P in Ge is of the order of $10^{-12}\,\mathrm{cm}^2/\mathrm{s}$ at 800 °C as reported in Figure 7.11a. On the other hand, the diffusion coefficient of P in Ge-rich SiGe alloys is greatly suppressed compared to that of P in Ge [26], because the diffusion mechanism of phosphorus in silicon is different than in germanium. Recent experiments have suggested that for intrinsic P diffusion in Si, the interstitial-assisted diffusion mechanism dominates, combined with a vacancy-mediated diffusion mechanism [27]. The combination of these two effects results in an overall increase in P diffusivity with Ge content. The diffusion coefficient of P in cubic SiGe with 40% germanium content is of the order of $10^{-16}\,\mathrm{cm}^2/\mathrm{s}$ at 800 °C as reported in Figure 7.11b. The observations made so far suggest that the diffusion coefficient of phosphorus in hexagonal Ge-rich SiGe at 800 °C should range in the interval delimited by the reported values. As a consequence, 800 °C should be sufficient to introduce a high concentration of dopant deep enough to generate ohmic contacts and reduce the resistivity of the nanowires.



(a) (b)

Figure 7.11: Phosphorus diffusivity in **(a)** cubic Ge [28] and **(b)** cubic SiGe [29].

On the contrary, solid-state diffusion of phosphorus through silicon dioxide is quite slow and often negligible. K. Shimakura et al. [30] report a diffusivity of P in SiO_2 of $3 \times 10^{-18}\,cm^2/s$ at 800 °C as can be extracted by Figure 7.12. The resulting diffusion length of phosphorus in silicon dioxide is of a few nanometers at 800 °C for more than 1 h, that is a time much longer than the ones exploited for solid-state diffusion of phosphorus in this thesis. As a consequence, 60 nm of SiO_2 are highly sufficient to completely mask the diffusion of phosphorus in silicon germanium.

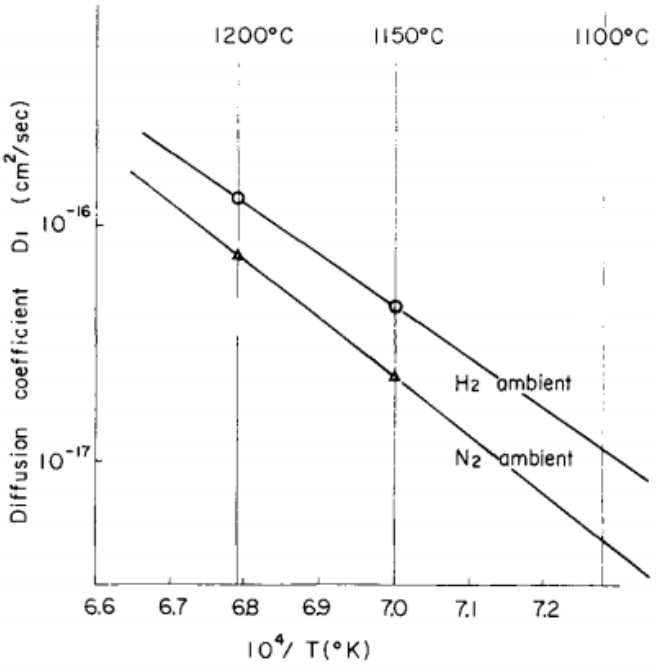


Figure 7.12: Phosphorus diffusivity in SiO_2 [30].

7.4 Electrical characterization

Once the solid-state diffusion doping has been completed, it is possible to perform the electrical characterization on the doped nanowires, by both two- and four-wire measurements. The most of the nanowires are only doped at the contacts areas in order to obtain ohmic contacts, while a few of them are entirely doped in order to measure their reduced resistivity. Both the contact resistivity and the SiGe resistivity obtained by phosphorus doping of the nanowires without the GaAs core will be compared with the results obtained by rapid thermal annealing of the nanowires with the GaAs core in Section 6.1, which are doped by a net doping concentration of arsenic impurities coming from the GaAs core.

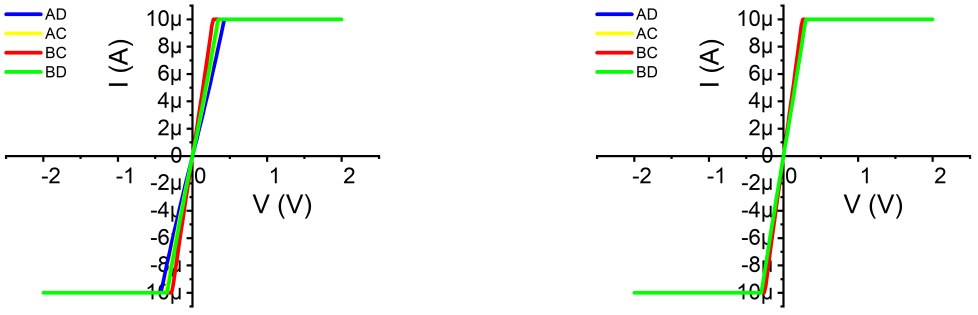
As explained in Section 7.1, the thick nanowires (sample H06794) without the GaAs core appear to be thermally more stable than the same nanowires with the GaAs core. They do not look affected by 900 °C 6 s rapid thermal annealing, so temperatures below this limit can be exploited to drive phosphorus impurities into the SiGe shell during the solid-state diffusion process. The first two essays have been performed at 850 °C for 30 s and at 800 °C for 30 s. The aim of the high temperatures

is to introduce a high concentration of dopants, because the diffusivity of impurities increases exponentially with the temperature. The time controls the diffusion depth, so 30 s are sufficient to obtain a high phosphorus concentration for a few nanometers into the SiGe shell at high temperatures. The nanowires still covered by the P-doped SiO_x after rapid thermal annealing are shown in Figure 7.9. The silicon oxide shell of the nanowires annealed at 850 °C for 30 s (Figure 7.9a) looks rough and covered by dark spots. A further SEM analysis reveals that the dark spots are due to holes or damage in the SiGe shell. This means that the thermal stability of the nanowires without the GaAs core decreases if the SiGe shell is covered by a SiO_x shell during the rapid thermal annealing. This may be due to the thinning of the SiGe shell during the etching process of the GaAs core, that makes it very fragile, so that the mechanical strain induced by the SiO_x shell due to the high temperatures is sufficient to generate holes in the SiGe shell. In addition, both the growing process of the nanowires and the etching process of the GaAs cores are responsible for variability of the SiGe shell thickness. It results in a high variability in the outcome of the solid-state diffusion process, because the thermal stability of the SiGe shells highly depends on their thickness, as previously explained. This causes a significant decrease in the yield of the doping process, for both two- and four-wire measurements, because the thinner shells are more subjected to damage at the high temperatures for solid-state diffusion. The silicon oxide shell of the nanowires annealed at 800 °C for 30 s (Figure 7.9b) appears less damaged. The dark spots indicating holes in the SiGe shell are fewer and smaller than the ones on the nanowires annealed at 850 °C for 30 s. The reason is that at lower temperatures the SiGe shell is more stable, so it is less damaged during the solid-state diffusion process.

The presence of holes in the SiGe shell introduces two major issues, due to the variability that characterize them during their formation. First, the contact resistivity is measured by TLM. This method requires that only the distance separating two contacts varies, while all the other geometric parameters should be kept the same. The mask that defines the pattern of the metal contacts in the evaporation process is the same for each contact. However, the variability of the holes that form on the SiGe shell introduces a high variability in the contacts areas from one contact to another, which results in a great uncertainty on the values extracted from the fit provided by the TLM method. Then, another issue introduced by the SiGe shell damage is the variability that affects the cross sectional areas of the nanowires. It is reduced both by the thinning of the SiGe shell during the GaAs core etching process and by the holes formation. However, only a TEM analysis would be able to estimate the cross sectional areas, but it is not feasible on a large number of nanowires, therefore it is not possible to obtain an accurate estimation. This results in large error bars on the resistivity values, because they are linearly dependent by the cross sectional areas.

From two-wire measurements it is possible to obtain the I-V characteristics to investigate whether the contacts turned into ohmic or not by the n+ doping, as explained in Section 2.3.1. From the analysis of the collected data results that some contacts are still Schottky, but many others have assumed an ohmic behavior. Contacts that are still Schottky are probably prevented from turning into ohmic due to a resid-

ual oxide barrier or due to defects at the metal-semiconductor interface that pins the Fermi level at the interface states energies. Most nanowires have some ohmic contacts, but only one nanowire per chip shows all four ohmic contacts, for both temperatures. Their I-V characteristics are reported in Figure 7.13a for the nanowire annealed at 850 °C for 30 s and in Figure 7.13b for the nanowire annealed at 800 °C for 30 s. Obtaining ohmic contacts from the solid-state diffusion process makes this method very promising for achieving this goal, however the low yield of nanowires with all four ohmic contacts suggests that the process still needs to be refined.



(a) (b)

Figure 7.13: Current-voltage characteristics obtained by two-wire measurements of Ni/Au metal-semiconductor contacts carried out on **(a)** 850 °C 30 s and **(b)** 800 °C 30 s annealed nanowires without the GaAs core. The behavior of the metal-semiconductor junctions is ohmic.

Another attempt has been carried out at lower temperature to increase the yield of ohmic contacts. As thin nanowires (sample H06793) has been employed, the temperature has been decreased a lot to avoid damaging them, as they withstand much lower temperatures. As the temperature was decreased to 600 °C, the time was increased to 300 s to ensure that the phosphorus impurities diffused deep enough to generate ohmic contacts. The yield of the contacts which turned into ohmic is much higher: most of the nanowires show all four ohmic contacts, as shown in Figure 7.14. However, reducing the temperature also reduces the peak doping concentration at the metal-semiconductor interface because the solid solubility of P into SiGe decreases. This results in a higher contact resistivity, which is in contrast with the aim of this thesis.

As anticipated, contact resistivities are extrapolated by the TLM method. The obtained results are reported in Figure 7.15. The TLM method can only be applied to ohmic contacts, so a reference value is not available, because bare nanowires produce Schottky barriers, but the ohmic contacts obtained by different methods can be compared. First of all, it can be stated that the contact resistivity that can be obtained from nickel diffusion is still too high if compared with the other values, despite the fact that the contacts turn into ohmic, as explained in Section 6.1. In the same section, the results obtained from the nanowires with the GaAs core were analyzed. As previously stated, the contact resistivity obtained by annealing these

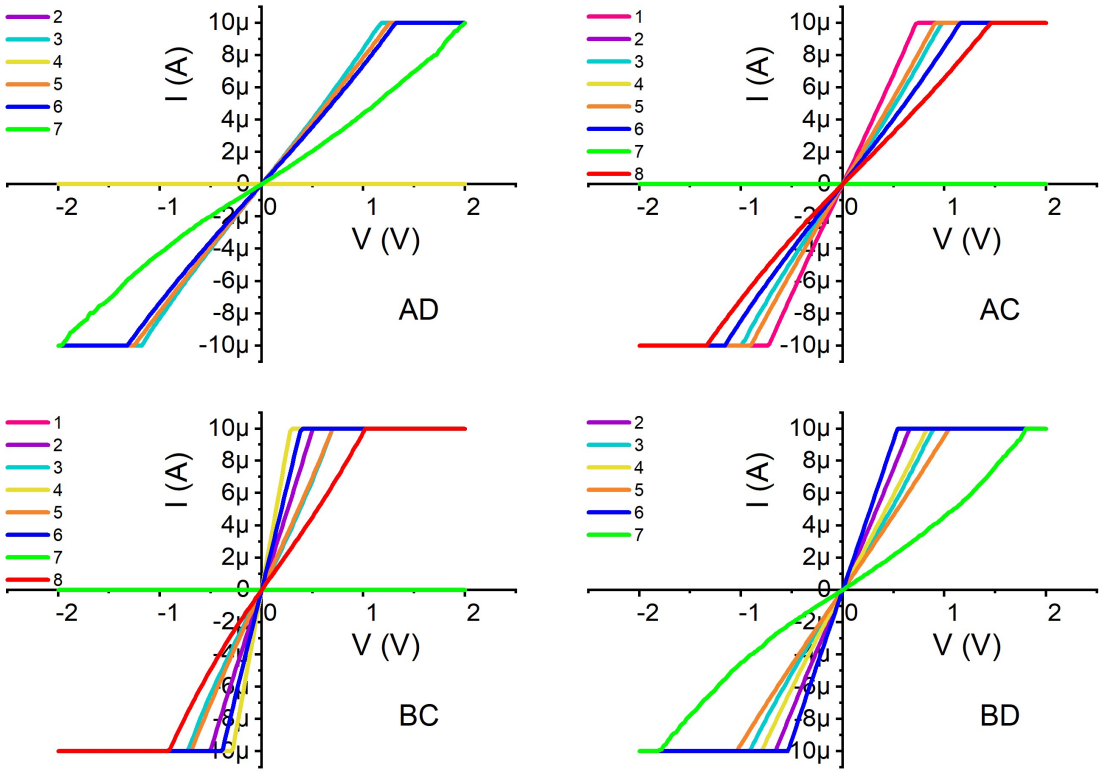


Figure 7.14: Current-voltage characteristics obtained by two-wire measurements of Ni/Au metal-semiconductor contacts carried out on 600 °C 300 s annealed nanowires without the GaAs core.

nanowires assumes very low values. The goal is to achieve an even lower contact resistivity by introducing the doping impurities by solid-state diffusion. As can be seen from the graph, the contact resistivity of the P-doped nanowires annealed at 850 °C for 30 s is even lower than the contact resistivity of the nanowires with the GaAs core, therefore this goal has been achieved. On the other hand, even if ohmic contacts have been achieved from the P-doped nanowires annealed at 600 °C for 300 s, the contact resistivity turns out to be still to high to be competitive with the previous results. Finally, the results obtained by the P-doped nanowires annealed at 800 °C for 30 s appear not to be in trend with the other ones. In particular, its contact resistivity turns out to be higher than expected. This could be due to an error introduced by the high variability affecting the contact areas, as explained above. The results obtained from the different combinations of diffusion temperature and time will be further compared below regarding the SiGe resistivity to come to a more accurate conclusion.

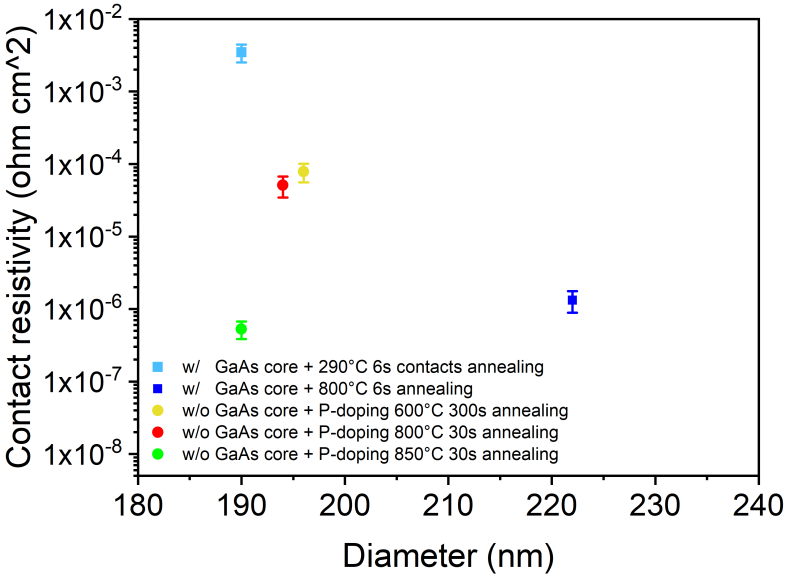


Figure 7.15: Contact resistivity values comparison between ohmic contacts obtained by different methods.

Four-wire measurements allow to measure the resistance of a portion of the SiGe shell. After that, the resistivity of the material can be calculated if the geometric parameters of length and cross sectional area are known. The distance between the two inner contacts of the four-wire measurements can be measured with high accuracy from the images captured by the SEM. On the contrary, the cross sectional area is extremely hard to estimate, because it cannot be visualized unless the nanowire is dissected. One way to measure it is to create a lamella with the FIB, but this would require a huge amount of time, because it would be necessary to repeat the process for each measured nanowire in order to have accurate results, since the thickness of the SiGe shell is characterized by high variability, worsened even more by the presence of holes following the annealing process.

The values obtained for the resistivity of the SiGe shell are reported in Figure 7.16. The cross sectional area of the nanowires with the GaAs core is easier to estimate because the diameter of the core can be measured during the growth process of the nanowires, while the diameter of the nanowires with the SiGe shell can be measured at the end of the process. As previously explained, the resistivity of the nanowires doped by the GaAs core by 800 °C 6 s annealing decreases of about one order of magnitude compared to the reference sample. Also in this case, as for the contact resistivity, the aim is to achieve an even lower resistivity by introducing the doping impurities by solid-state diffusion. The plotted resistivity values for the nanowires without the GaAs core has been calculated by the same cross sectional area as for the thick nanowires with the GaAs core (sample H06794). For this reason, they must be considered as upper limits, because these values are certainly overestimated.

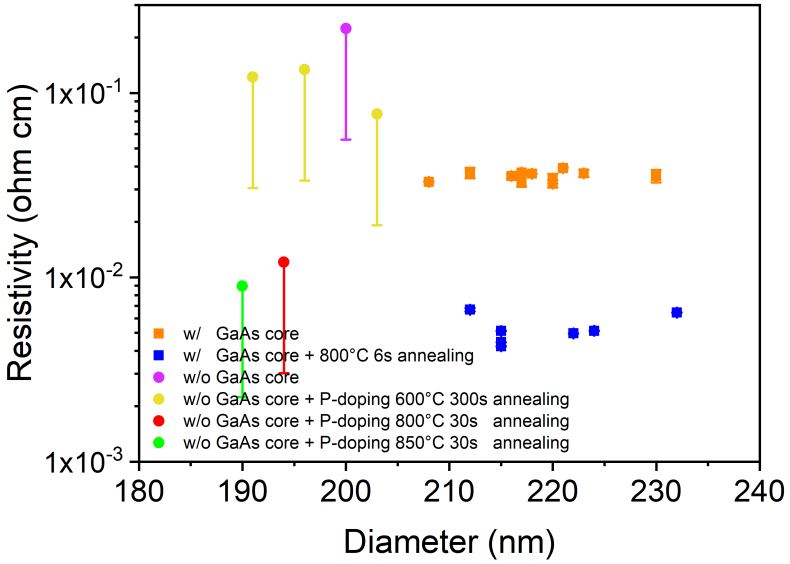


Figure 7.16: SiGe resistivity values comparison for different doping concentrations obtained by different methods.

The resistivity of the thick nanowires (sample H06794) without the GaAs core annealed at 850 °C for 30 s and at 800 °C for 30 s is overestimated because their SiGe shell has been thinned during the GaAs core etching process and because the formation of holes in the SiGe shell during the solid-state diffusion process has reduced their cross sectional area.

The resistivity of the thin nanowires (sample H06793) without the GaAs core annealed at 600 °C for 300 s is overestimated because their SiGe shell is thinner by growth and because it has been further thinned during the GaAs core etching process. The same considerations also apply to the thin reference nanowires without the GaAs core.

However, the cross sectional area resulting from these reductions cannot be measured. Therefore, a large error bar has been added to the graph to estimate the

range that these values could assume if properly corrected. The error bars extend only in one direction because the plotted values have to be considered upper limits. From these considerations it is clear that the resistivity of the nanowires annealed at 600 °C for 300 s has not taken a great advantage from the solid-state diffusion doping compared with the reference sample. This is also confirmed by the contact resistivity, where it can be seen that the doping concentration is sufficient to turn the contacts into ohmic, but it is still much lower than in the other samples. On the other hand, introducing the corrective factor that takes into account the reduced cross sectional area, the resistivity of the SiGe shell of the nanowires annealed at 850 °C for 30 s and at 800 °C for 30 s appears to assume values comparable or even lower than the nanowires doped by the GaAs core by 800 °C 6 s annealing. From a more detailed analysis, comparing these values with the contact resistivity data, it can be argued that the doping concentration of the sample annealed at 850 °C for 30 s is higher than the sample doped by the GaAs core, while the doping concentration of the sample annealed at 800 °C for 30 s is probably lower.

To conclude, high temperatures introduce a high doping concentration, but also risk damaging the thick nanowires, reducing the cross sectional area and consequently increasing the resistivity of the SiGe shell. On the other hand, low temperatures are suitable not to damage the thin nanowires, but the doping concentration introduced in the SiGe shell is not high enough to be competitive with the other samples. Therefore, the ideal situation is to use thick nanowires, to avoid damaging them at high temperatures or during the etching process of the GaAs core, but to keep the temperature low enough not to create holes or damage to the SiGe shell, despite the resulting doping concentration being lower than expected.

Chapter 8

Conclusion

This is the final chapter of the thesis, whose aim is to summarize the results obtained during the project and lay the foundations for its future developments. The aim of the project was the electrical characterization of the novel hex-SiGe semiconductor material, but its primary objective was to obtain ohmic contacts at the metal-semiconductor interface following the evaporation of the metal on the hex-SiGe nanowires for electrical contacting.

The first obstacle encountered for this purpose was the need to planarize the surface of the substrate where the nanowires were spun to avoid that a gap could be created in the metal contacts making them vain. The solution was the use of benzocyclobutene-based polymers that have an excellent degree of planarization and low curing temperature. This process required an initial effort to be optimized, but afterwards it was crucial to the success of subsequent processes and required few further revisions. It made it possible to perform two- and four-wire measurements on the nanowires, including temperature analysis. Regarding this, temperature measurements have only been performed on Schottky contacts until now. As proposed in the previous chapters, a possible future development is a temperature analysis performed on ohmic contacts to define the operating temperature of the devices below which the contacts turn out to assume a rectifying behavior.

Then, the measurement of the height of the Schottky barriers by fitting the I-V characteristics obtained from the two-wire measurements with the equation that describes the thermionic emission was fundamental to analyze their formation and the Fermi level pinning issue. This numerical analysis made it possible to evaluate the extent of the problem, to define the impossibility of varying the height of the potential barriers simply by changing the metal for the metallization of the contacts and laid the assumptions for the subsequent developments. Hence the idea of highly doping the contacts to turn their behavior into ohmic.

Before doping the contact areas between metal and semiconductor, annealing tests were carried out on thick nanowires with the GaAs core highlighting the problem of its interference. Arsenic impurities from the GaAs core diffused up to the surface of the SiGe shell during annealing, so it was necessary to selectively etch it.

Bromine-methanol solutions have been used for this purpose because they are able to selectively etch the GaAs core over the SiGe shell. The selectivity provided by these solutions is sufficiently high for the thicker and shorter nanowires, but it is too low for the thinner and longer nanowires. The shell of the latter is excessively damaged because at the end of the process it is too thin not to withstand the high temperatures needed for the solid-state diffusion doping process. This poses an obstacle to the doping process which forces to exclude the thin nanowires in favor of the thick ones in future applications. As it has been proven, they have a thicker shell at the end of the etching process which allows them to withstand higher temperatures and longer exposures.

However, the most troubled issue remains the annealing process, be it a limit temperature test or part of solid-state diffusion doping. Table 8.1 summarizes all the annealing tests carried out on thick (sample H06794) or thin (sample H06793) nanowires, with or without the core, covered or not by the solid-state diffusion SiO_x shell, performed by RTA or MOCVD, as described in the two previous chapters. As anticipated, the yield of the solid-state diffusion process was heavily reduced by the damage that the shells of the nanowires suffered during the annealing process, following the etching of the GaAs core by bromine-methanol solutions. Thick nanowires without the GaAs core appear thermally more stable than counterparts with the GaAs core. However, their stability is reduced if they are covered with the SiO_x shell during the solid-state diffusion process. The reduction of the thickness of their SiGe shell by the etching process of the GaAs core combined with the reduction of the cross sectional area due to the holes formed by the mechanical strain induced by the SiO_x shell reduces the yield of the process and makes the resistivity of the material difficult to calculate from four-wire measures.

The matter becomes even more complicated working with the thin nanowires. Their shell is so thin that, if the etching process of the GaAs core is too long, the risk that it will be completely damaged is very high, causing it to collapse. Nanowires in these conditions can not be analyzed anymore. Furthermore, even if their SiGe shell survives, it turns out to be so thin that it is difficult to process for solid-state diffusion, because they only withstand low temperatures. Even if it is possible to make the contacts ohmic, the doping density results to be very low compared with that of the thick nanowires.

Furthermore, it is difficult to compare the results obtained from thick nanowires with those obtained from thin nanowires. This happens because thin nanowires do not withstand high temperatures like thick nanowires, so it is necessary to increase the diffusion time of dopants to make the penetration depth sufficiently high. Such different combinations of time and temperature are incompatible, so only evaluative conclusions can be drawn. There is still no complete matrix of results that allows to exclude some solutions in favor of others. However, from the processes carried out on the solid-state diffusion, it is evident that the thin nanowires after the etching process of the GaAs core appear thermally less stable than the others. This suggests proceeding in future attempts with thick nanowires. It will be necessary to refine the parameters that control the doping process to prevent the SiGe shell of the nanowires

Table 8.1: Summary of the results carried out by annealing tests on thick (sample H06794) or thin (sample H06793) nanowires, with or without the core, covered or not by the solid-state diffusion SiO_x shell, performed by RTA or MOCVD. The ✓ symbol point out the survived nanowires, while the ✗ symbol highlight the damaged ones.

	6 s	30 s	300 s	600 s
900 °C	✗ Thick ✓ Thick w/o core			
850 °C	✗ Thick	✓ Thick w/o core + SiO_2 shell	✗ Thick w/o core + SiO_2 shell	✗ Thick
800 °C	✓ Thick	✓ Thick w/o core + SiO_2 shell	✗ Thick w/o core + SiO_2 shell	✗ Thick
750 °C	✓ Thick		✗ Thin w/o core + SiO_2 shell	
720 °C			✗ Thin w/o core (MOCVD)	
700 °C	✓ Thick			
650 °C			✓ Thin w/o core (MOCVD)	
600 °C			✓ Thin w/o core + SiO_2 shell	

from being damaged. In this way it will be possible to have a more precise estimate of the cross sectional area for the calculation of the resistivity of the material after doping, so as to be able to better compare it with the previous results.

The final purpose of the n-type doping is not just about obtaining ohmic contacts to minimize the power consumption in future electronic devices, but also to refine the solid-state diffusion process in order to generate the n-type region in a p-n junction. The objective of this junction is the generation of a light emitting diode. In this regard, doping by implantation tests with gallium impurities have also been conducted to constitute the p-type region. The results are promising, but the effort of this thesis aimed mainly at the n-type region because without ohmic contacts it would have been difficult to discern whether the I-V characteristics were due to the diode behavior or the Schottky contacts.

This purpose paves the way for future developments of this novel material. As previously stated, the direct band gap of Ge-rich hex-SiGe alloys, their high light emission efficiency and the tunability of their emission wavelength make them suitable candidates for laser emission in silicon photonics, but this has yet to be proven. The electrical characterization carried out in this project and the attempt to manufacture a p-n junction are fundamental steps for the realization of this purpose. This aim could open a pathway towards CMOS integrated Si-based light sources in the near future, that would revolutionize not only silicon photonics, but the entire semiconductor industry.

Appendix A

Supporting Figures

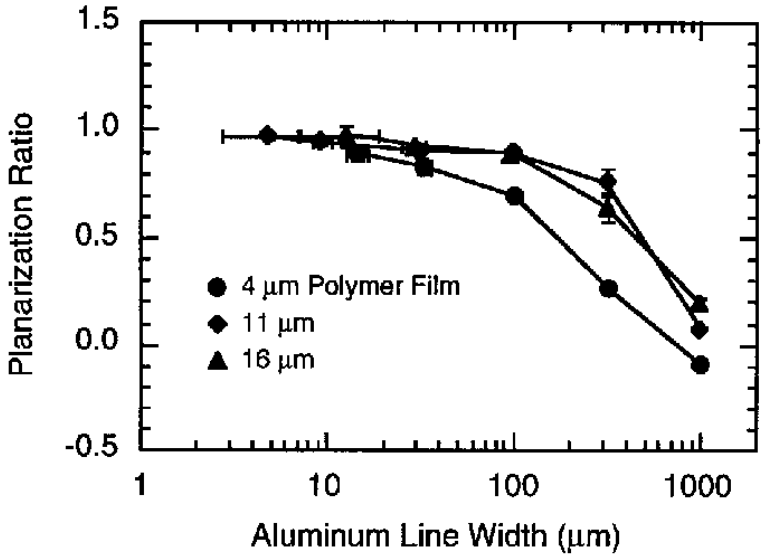


Figure A.1: Planarization ratio for dry etch grade BCB polymer as a function of aluminum line width (4 µm thick Al line) [31].

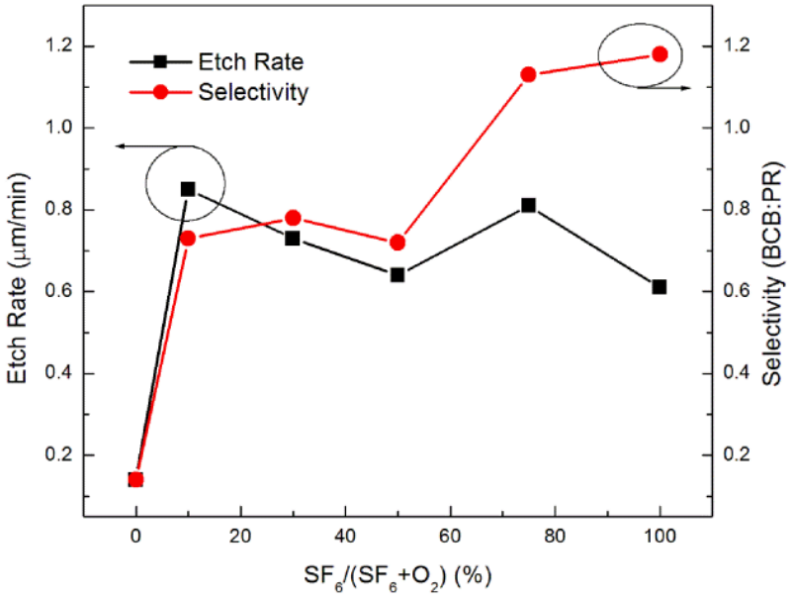


Figure A.2: BCB etch rate and BCB:PR etch selectivity for different $SF_6 - O_2$ mixing ratios etched in Inductively Coupled Plasma (ICP) Reactive Ion Etcher (RIE).The values are obtained setting the following parameters: ICP power of 300 W, RIE power of 300 W, pressure at 3 mTorr [15].

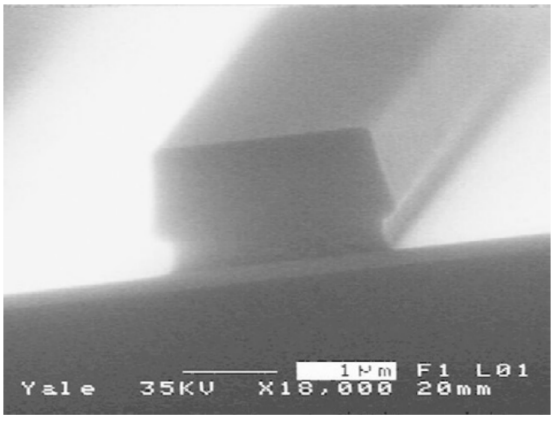


Figure A.3: Edge-on SEM image of the LOR/S1813 bilayer resist profile used for lift-off metallization [17].

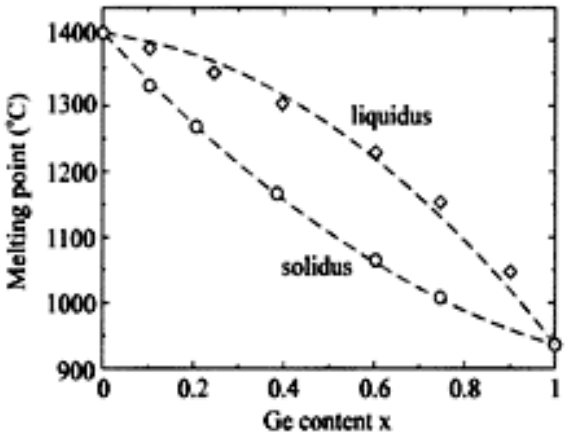


Figure A.4: Melting point of cubic SiGe alloys as a function of germanium content [19].

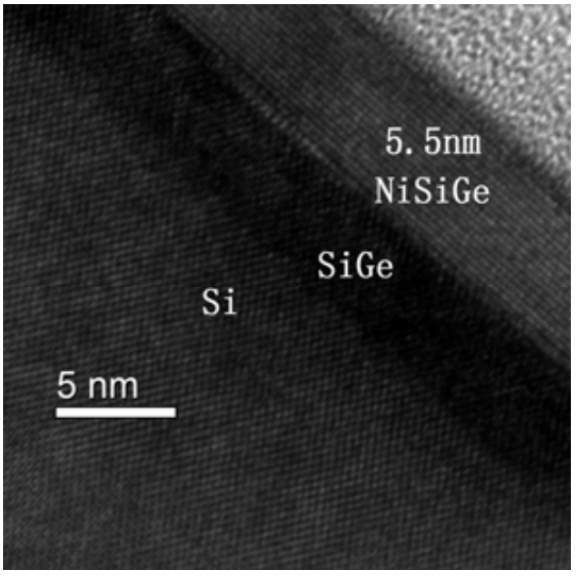


Figure A.5: TEM image of the nickel germano-silicide formed by rapid thermal annealing at 400 °C for 30 s with 5.5 nm nickel thickness at the interface between Ni and SiGe [24].

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Davide