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Master of Nanotechnologies for Integrated Systems
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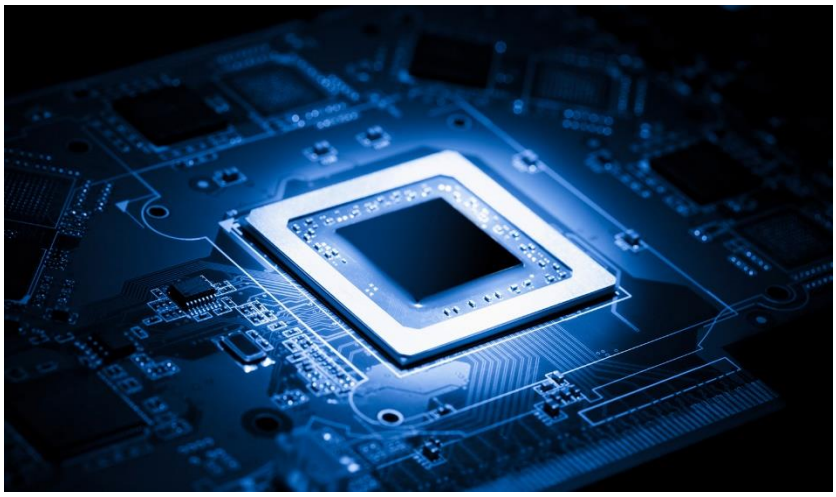
Design of a Clock and Data recovery circuit

from 10/02/2021 to 10/08/2021



Confidentiality: yes / no

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Table of content:

Figures:

Tables:

Glossary:

CDR : clock and data recovery
CML : current mode logic
PAM4 : Pulse Amplitude Modulation 4-level
NRZ : Non Return to Zero
DAC : digital-to-analog converter
VCO : Voltage controlled oscillator
LSB : less significant bit
DNL : Differential NonLinearity
BER : Bit Error Rate
PVT : Process Voltage and Temperature
MIM : Metal Insulator Metal
UI : Unit Interval
PTAT : Proportional to absolute temperature
BICMOS : BIpolar Complementary Metal–Oxide–Semiconductor
PSRR : Power supply rejection ratio
PM : Phase margin
V2I : Voltage to current converter
VCSEL : Vertical-Cavity Surface-Emitting Laser
ADC : Analog to Digital converter
TIA : TransImpedance Amplifier

Abstract:

1.1- English :

The communications became a real challenge in the 21th century, especially with new technologies. For a transmission process of data, the sender transforms it into an optical signal that will be recovered by a receiver. The transmitted data through the optical medium will be subject to distortion and noise. The optimal processing of the incoming data is subject to choosing a proper clock that will sample the incoming signal in order to faithfully recover it with less errors. This report presents the design of some blocks used in a clock and data recovery circuit (CDR) introduced by the module PAM4, which task is to recover the data and the clock sampling this data from the incoming signal.

1.2- French :

Les communications sont devenues un véritable défi au 21ème siècle, notamment avec les nouvelles technologies. Pour un processus de transmission de données, l'émetteur les transforme en un signal optique qui sera récupéré par un récepteur. Les données transmises via le support optique seront sujettes à la distorsion et au bruit. Le traitement optimal des données entrantes est soumis au choix d'une horloge appropriée qui échantillonnera le signal entrant afin de le récupérer fidèlement avec moins d'erreurs. Ce rapport présente la conception de certains blocs utilisés dans un circuit de récupération d'horloge et de données introduit par le module PAM4, dont la tâche est de récupérer les données et l'horloge utilisée pour échantillonner ces données à partir du signal entrant.

1.3- Italian :

Le comunicazioni sono diventate una vera sfida nel secolo scorso, soprattutto con le nuove tecnologie. Per un processo di trasmissione dei dati, il mittente lo trasforma in un segnale ottico che verrà recuperato da un ricevitore. I dati trasmessi attraverso il supporto ottico saranno soggetti a distorsione e rumore. L'elaborazione ottimale dei dati in ingresso è subordinata alla scelta di un opportuno clock che campiona il segnale in ingresso in modo da recuperarlo fedelmente con meno errori. Questo rapporto presenta il progetto di alcuni blocchi utilizzati in un circuito di clock e recupero dati introdotto dal modulo PAM4, il cui compito è recuperare i dati e il clock campionando questi dati dal segnale in ingresso.

1.Introduction:

Transmission of data starts by an electrical signal applied to a laser generating an optical signal (light) that will travel across a medium long distance, it will thereafter be received by a photodiode recovering back the initial electrical signal. During this process, the transmitted light may undergo attenuations due to the imperfections of the materials used for the medium, it may also get distorted and subjected to noise.

Clock and data recovery (CDR) is a circuit used to recover faithfully the data after being subject to the medium limitations. It basically uses the data to generate the proper clock to be injected to a FlipFlop in order to sample properly this incoming data. The CDR designed in this project will use PAM4 standards. Previous generations CDR used NRZ standards by coding the incoming signal in two levels (one bit logic): “0” and “1”, the PAM4 standards allows the coding of the signal in 4 levels (two bits logic): “00”, “01”, “10” and “11” allowing to double the throughput at the same incoming data rate.

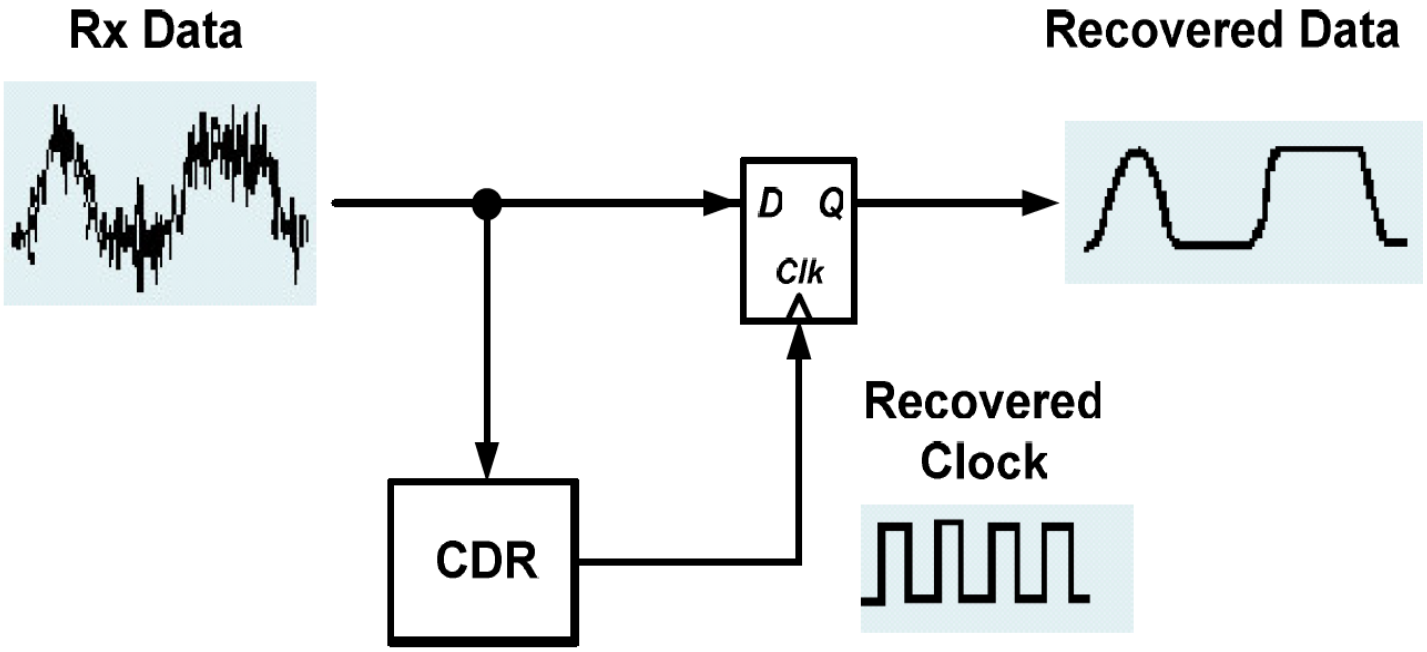


Figure 1: Clock and data recovery principle [1]

The goal of my internship is to help design different blocks that are used by the senior designers in the design of the clock and data recovery structure. In particular I have been involved in a digital-to-analog converter (DAC), a phase interpolator in two implementations, a bandgap reference and a voltage-to-current converter (V2I). I have also been involved with the layout of those blocks and others.

2.The company presentation:

Litrinium is an international company headquartered in Orange County, California, United states. I have been part of the design team in Sophia Antipolis in France. The main objective of Litrinium is to provide solution enabling ultra-high-speed networking. targeting signal transmission and reception markets. We can cite some of the core products for those applications like transimpedance amplifiers, laser drivers, clock and data recovery …

2.1 - Targeted markets:

- Data centres connectivity
- 5G wireless infrastructures
- Artificial Intelligence (AI)
- Internet-of-Things (IoT)
- Augmented Reality/Virtual Reality (AR/VR)

2.2 – Size of the company:

- The company was founded in 2016
- Headquartered in California (United states)
- 2 Other design centres, the first in Sophia Antipolis in France, and the second in Canada.
- Marketing centres in Japan, Taiwan, Singapore and China.
- 29 Employees
- Pre-revenue stage

3.Digital-to-analog converter (DAC):

3.1- The structure of the DAC

Clock and data recovery circuits use many digital-to-analog converters, in particular in the designed chip a digital engine generates an 8 bits digital word, that will be injected to the digital-to-analog converter generating a current increasing with this digital word. In what I have been involved with, this current will be used to bias a phase interpolator that starts from a reference clock (in terms of phase) generated by a VCO and will shift this clock with the digital word from 0 to 360 degrees.

The digital-to-analog converter implemented converts the injected digital code into a current, with a LSB of 5µA (increase of 5µA of the outputted current with increase of 1 in the digital word). The main motivation behind the choice of conversion in current is parasitics. A choice for example of a voltage-based DAC will lead to voltage drops through the parasitic resistance arising from routing, and therefore a loss of information.

My work on this DAC as an intern was to characterize this newly designed DAC, find solutions and try to optimize when the results violate the specification. The latter was only to get an increase of the current of 1LSB ± ½ LSB.

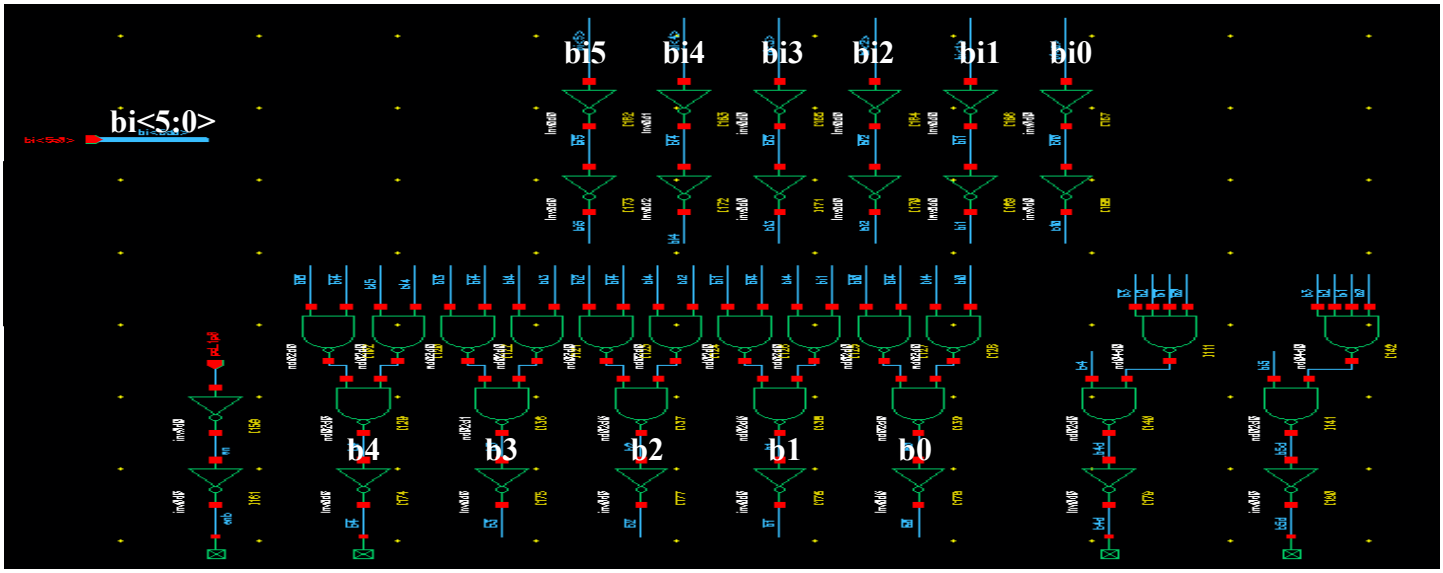
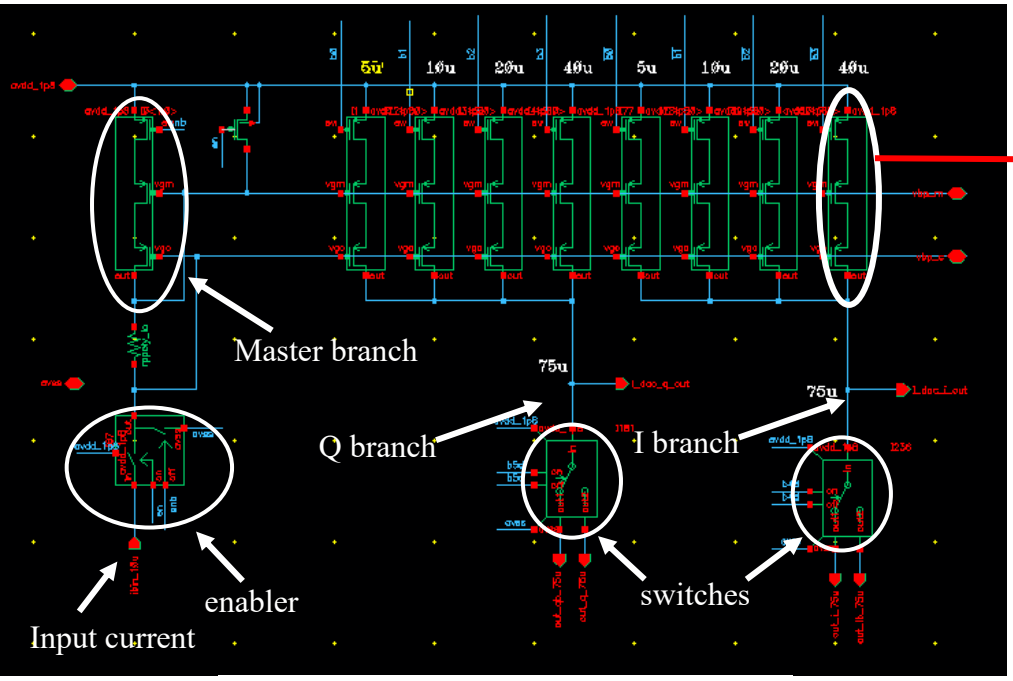


Figure 2: Logic part of the DAC

This part of the DAC in Figure 2 uses 6 bits of the 8 bits generated by the digital engine, those 6 bits are sufficient to perform the seeked operation of shifting. The first 4 bits (bi0, bi1, bi2 and bi3) are used as logic for switching the transistors used in the analog part of DAC that changes the current (Figure 3), the 2 last bits (bi4 and bi5) are used as logic for switching between the branches I, Ibar, Q and Qbar of the DAC and that will subsequently bias the phase interpolator.

In the multiple NAND branches, the operation that is performed in each branch is a XNOR operation of a bit with bi4 (for example $b0 = \overline{bi4 \otimes bi0}$ allowing us to switch from a quadrant to another (from I to Ib for example)

Figure 3 shows the analog part of the DAC consisting of multiple cells shown in figure 4, the top transistor acts as a switch to the bits generated by the logic part of Figure 2. The middle transistor acts as a current mirror, copying the input bias current from the master branch and finally the bottom transistor is a cascode for voltage mirroring for a better copy of the current by the current mirror when considering Early effect.



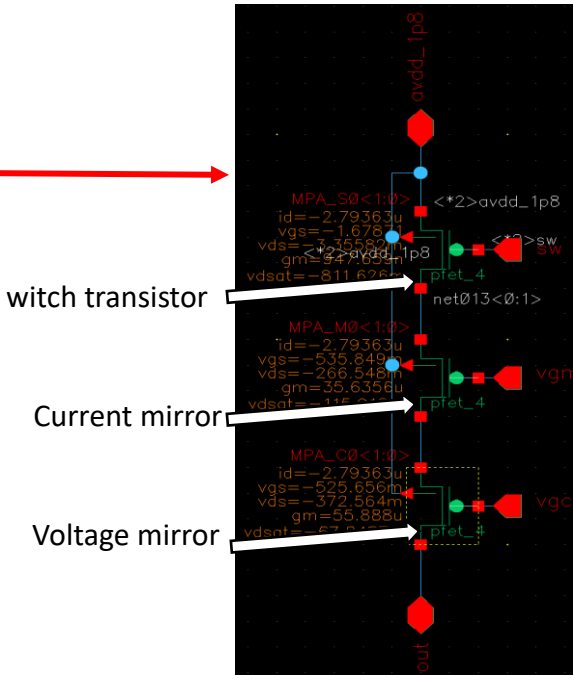


Figure 3: Analog part of the DAC

Figure 4: cells used in the DAC

Table1 shows the saturation of the current mirror transistor and the cascode in Figure 4 in PVT (refer to annex 9.1 for corner configurations) for the code 15 where all the transistors of the Q-branch are activated. Since all the transistor of this Q-branch are subject to similar conditions (same Vg, Vs and Id) we can limit ourselves to analyse only one Figure4 cell as the other cells will yield the same results. The specification is to have a saturation margin higher than 100mV ($V_{ds} - V_{ds_{sat}} < -100mV$).

Output	temp=-40	temp=110	Corner_fast_0	Corner_fast_1	Corner_fast_2	Corner_fast_3	Corner_slow_0	Corner_slow_1	Corner_slow_2	Corner_slow_3
sat_margin_dac_mirr	-155.4m	-126.6m	-147.7m	-122.2m	-153m	-127.8m	-166.4m	-141.3m	-174.2m	-148.1m
sat_margin_dac_casc	-593.7m	-525.1m	-657.2m	-604.1m	-901m	-853.3m	-336.6m	-337.3m	-733.8m	-663m

Table 1: DC Operating point of DAC's cells

3.2-Performances:

Figure 5 shows the functionality of the DAC, we have as expected a current increase with the digital word (ctrl_pi). As the load of the digital bits generated by the logic part is different for one bit to another, for example b3 drives 8 transistors while b0 drives only 1 transistor, this may cause the increase of the current to be slightly different for each code as the switching transistors will not switch in the same way, it will also cause some glitches as we will see later in the report when we will perform transient simulations. Figure 6 shows the step increase of the current in the Q-branch (derivative of Figure 5).

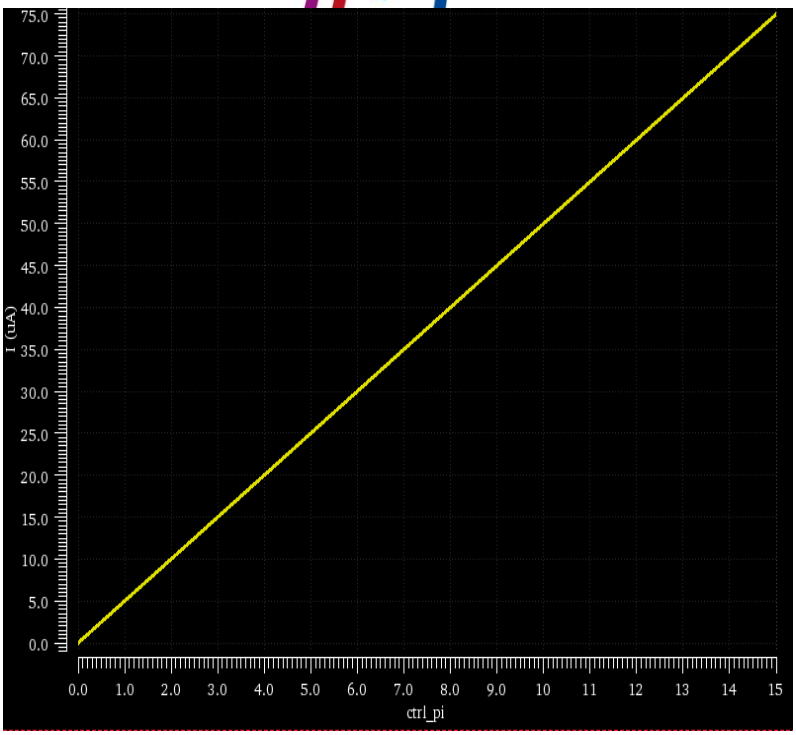


Figure 5: step increase of the current in Q-branch (digital code varying from 0 to 15)

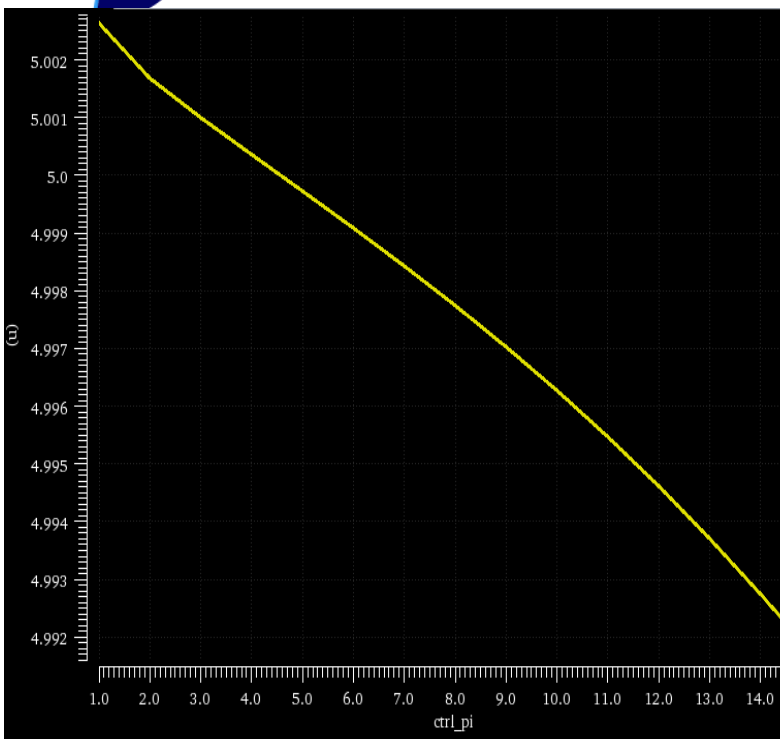


Figure 6: Step variation of the current in the Q-branch

As mentioned before, the specification is to have an increase within 1LSB ± ½ LSB, which is perfectly the case in Figure 6. To check this specification in PVT, we perform a Monte Carlo simulation and we calculate the DNL which is the derivative of the current minus the expected increase of 5µA. For the worst case of the code equal to 8, we have a mean of -2.507nA and a standard deviation 554.6nA, in consequent we are lower than ½ LSB for the **mean plus 3-sigma**.

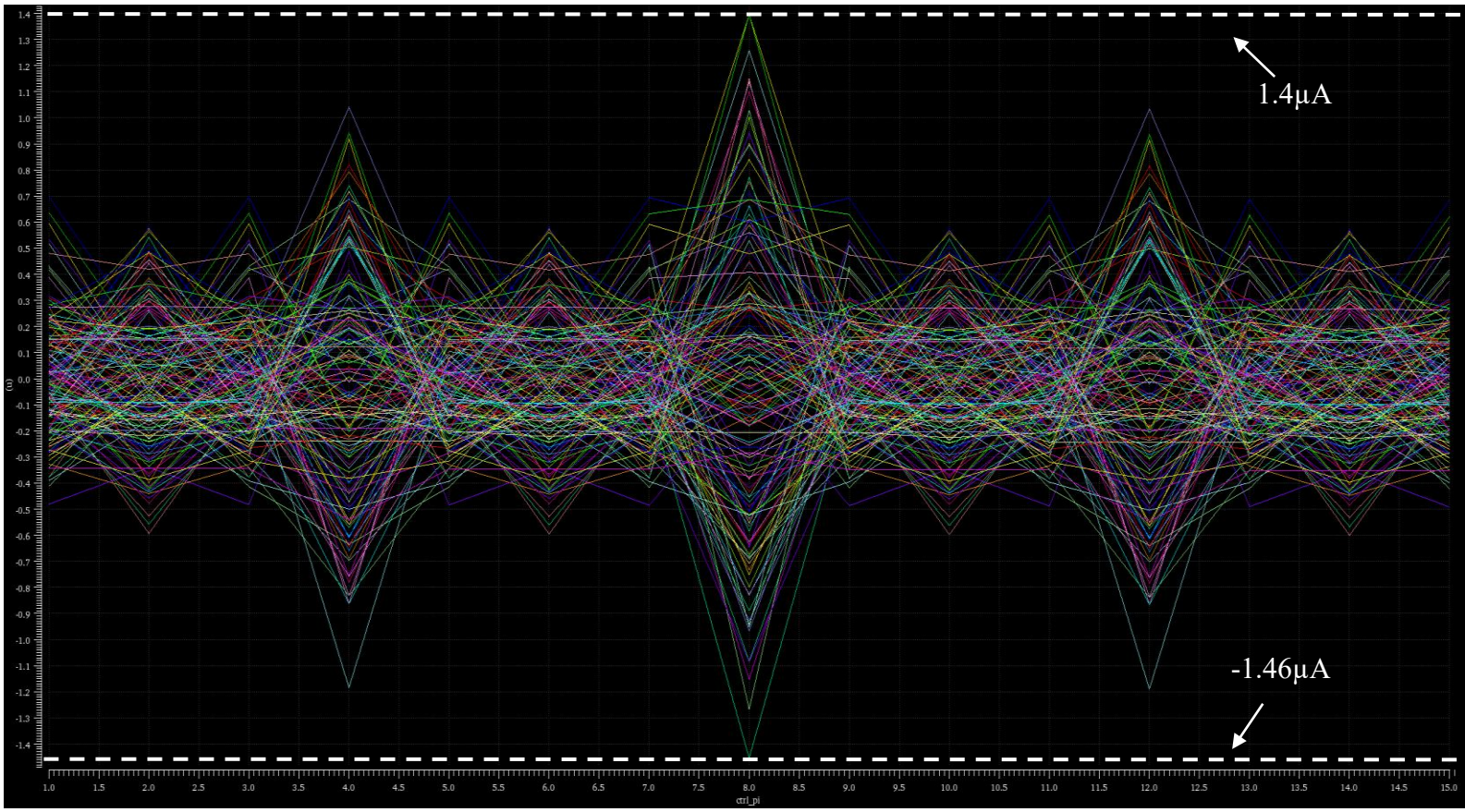


Figure 7: Monte Carlo results for the DNL of the DAC

4.Phase interpolator:

4.1- Introduction

The clock and data recovery structure has to be able to adapt itself in terms of the clock generated in order to sample the incoming data in an optimal position for less errors. For this reason, a phase interpolator is a circuit that helps shifting the phase of the generated clock using the DAC previously discussed.

In our phase interpolator, we will use a *polyphase filter* (not discussed in this report) that generates the four quadrature of phase (I, Q, $\bar{I}$ and $\bar{Q}$) when fed by a clock from a VCO. We will then try to mix the four phases with specific weights in order to get a specific phase, for example if we mix I and Q we will get an outputted clock phase between 0 and 90 degrees depending on the weights given to I and Q.

Interpolation is the technique of monitoring the tail current to get a specific result, in our case the tail current will create the weights.

4.2- Structure of the phase interpolator

Our phase interpolator consists of four npn bipolar differential pairs with a resistive load. The inputs of the differential pairs (ip = I positive (I), in = I negative ($\bar{I}$), qp = Q positive (Q) and qn = Q negative ($\bar{Q}$)) are the generated clocks through the polyphase filter.*

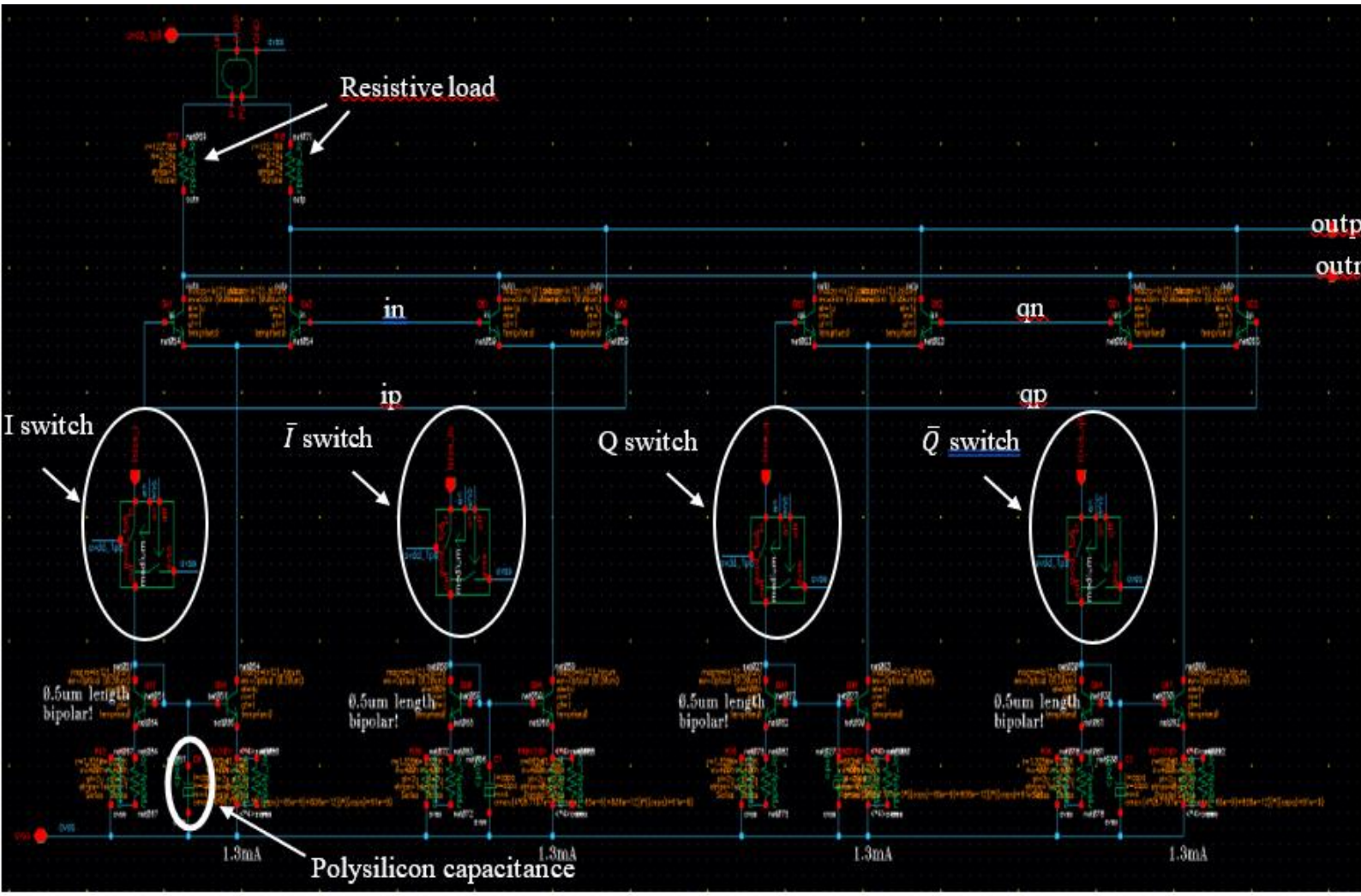


Figure 8: Structure of the phase interpolator

In this structure the tail current is generated by the previously designed DAC, the switches in Figure 3 will make through the logic of Figure 2, the switching of the tail current from I to $\bar{I}$ or the opposite or from Q to $\bar{Q}$ or the opposite depending on the digital word.

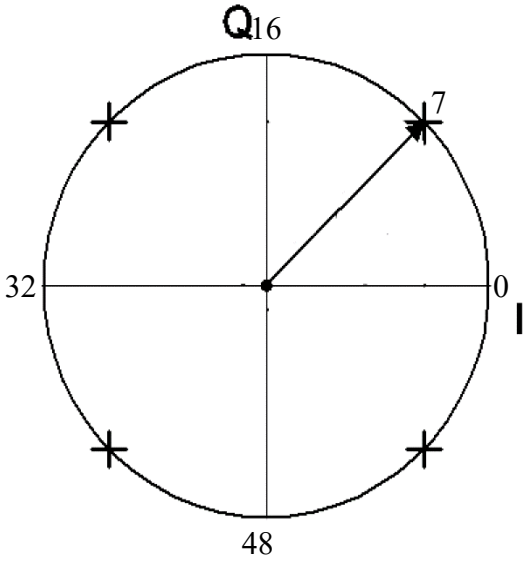


Figure 9: Performed phase shifting with the digital word

In small signal analysis the generated current through the bipolars is equal to $g_m V_{be}$, in this case in small signal their emitters are grounded (virtual ground) and we end up with $g_m V_b$. The summation of the two weighted clocks is performed in current domain and will allow us through proper weighting **to sweep an outputted clock from 0 to 360 degrees.** The choice of the bipolars for the differential pairs is motivated by their higher cutoff frequency with respect to MOS transistors allowing us to work at high frequencies, in this case we were working at **28GHz**, but also this choice was motivated by **the linear dependency of g_m in an intrinsic way with respect to I_c**. In the case of a MOS transistors differential pairs this linear behaviour of g_m would be valid only for some range of tail current where the differential pair is in weak inversion, otherwise in strong inversion g_m is proportionnal to the squar root of the drain current. As we are performing an interpolation, the tail current is varying and so the inversion region, this unwanted change will make in the case of strong inversion the phase shifting non linear.

4.3- Functionality:

The goal of this section is to show some results to validate the working of the circuit. Figure 10 shows the testbench used for the simulation. At this stage we simulated only the DAC and phaseshifter, the subsequent stages (red crosses) will not be taken into consideration in the simulation at this step and in particular the FlipFlop. We also simulated using an ideal differential clock generation circuit that will in advanced stages of the project be replaced by a VCO. Figure 11 shows the functionality of the phaseshifter: we can see that the phase of the outputted clock *ckp_shf* (clock positive shifted) is shifted accordingly with the digital word with respect to the input reference clock *ckp_inp*.

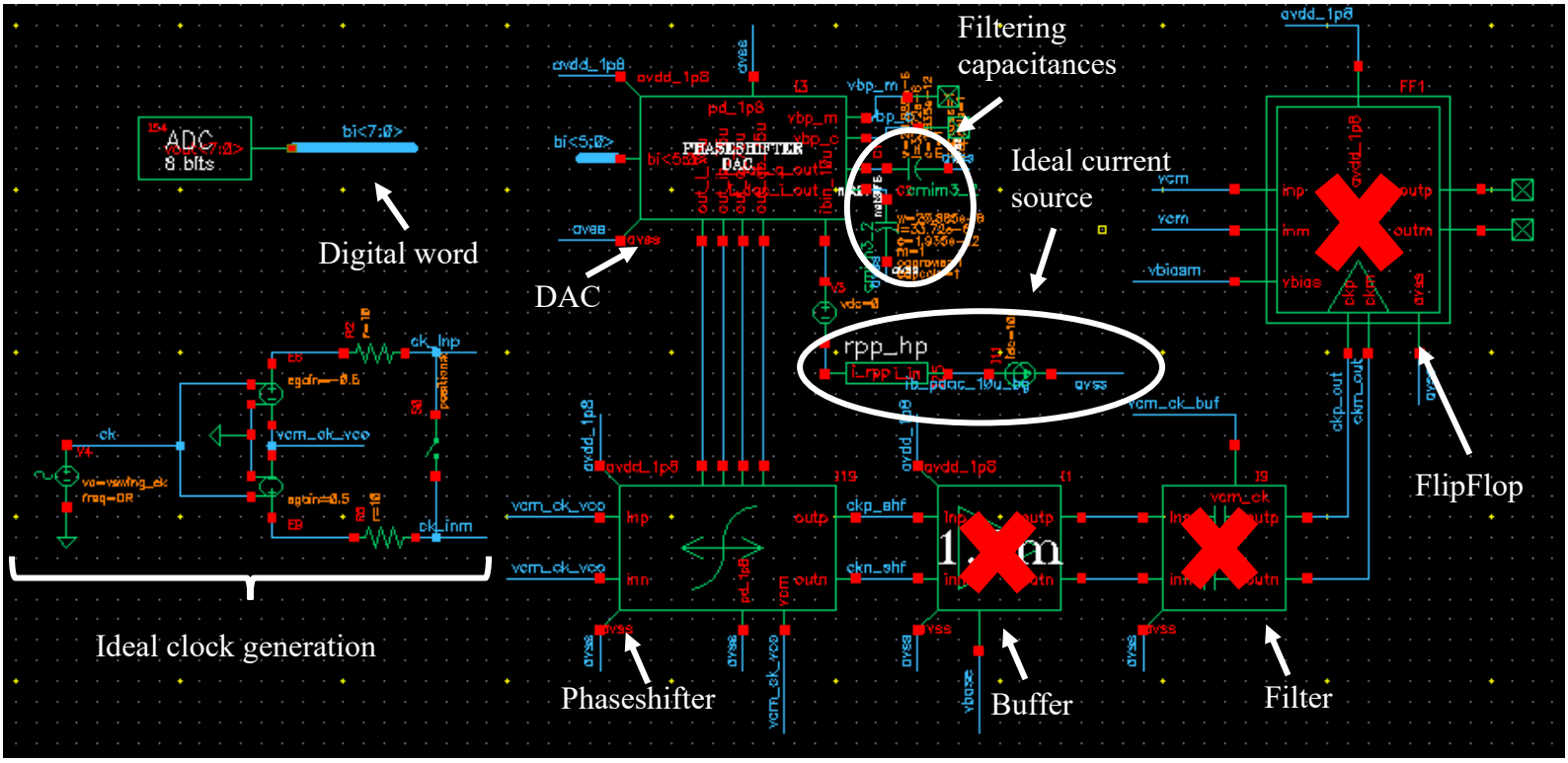


Figure 10: Testbench of the simulation

In Figure 11, we have only simulated the codes 0, 16, 32, 48 and 62 (code 63 overlaps with code 0) for ease of reading, for a simulation of all the codes (not plotted here) we can see the whole transition of the phase.

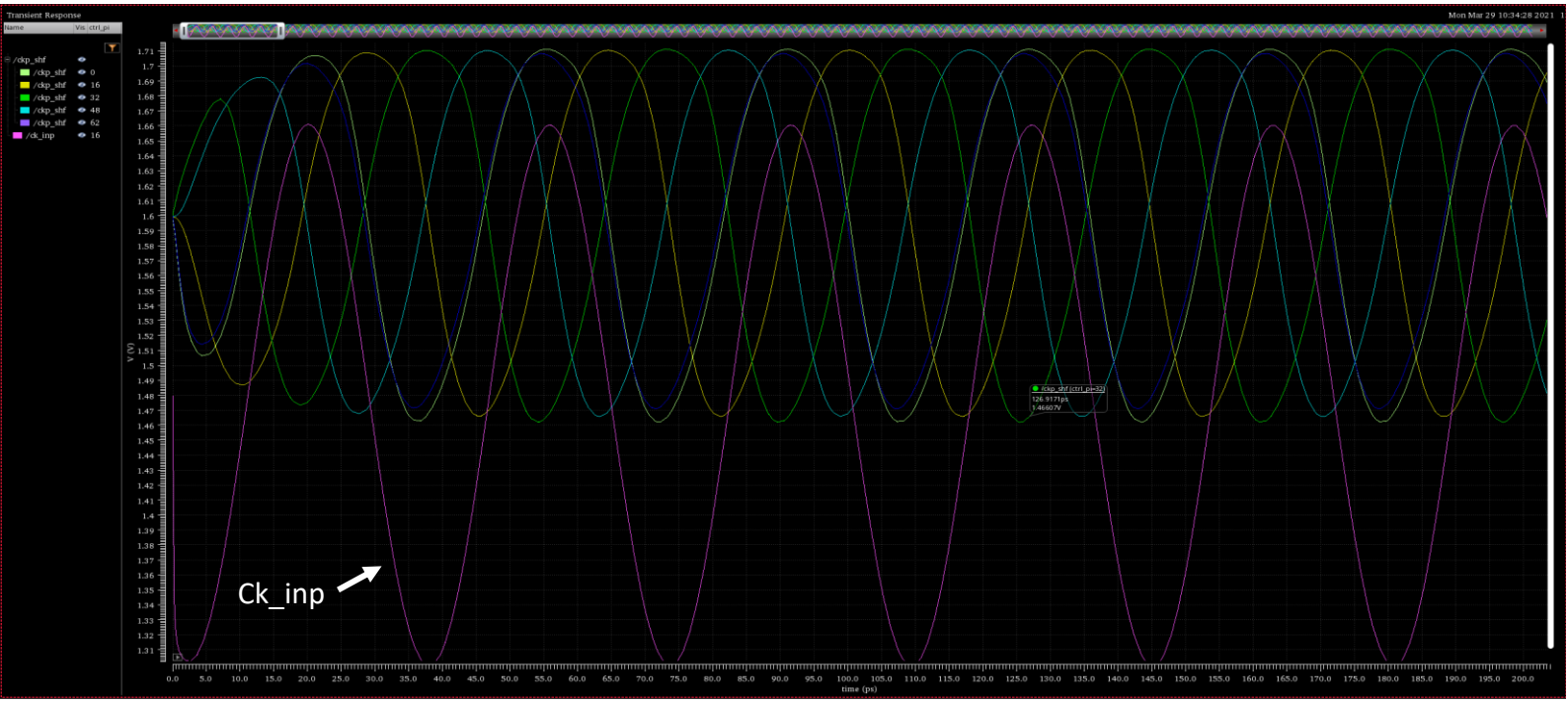


Figure 11: phase shifting of the clock

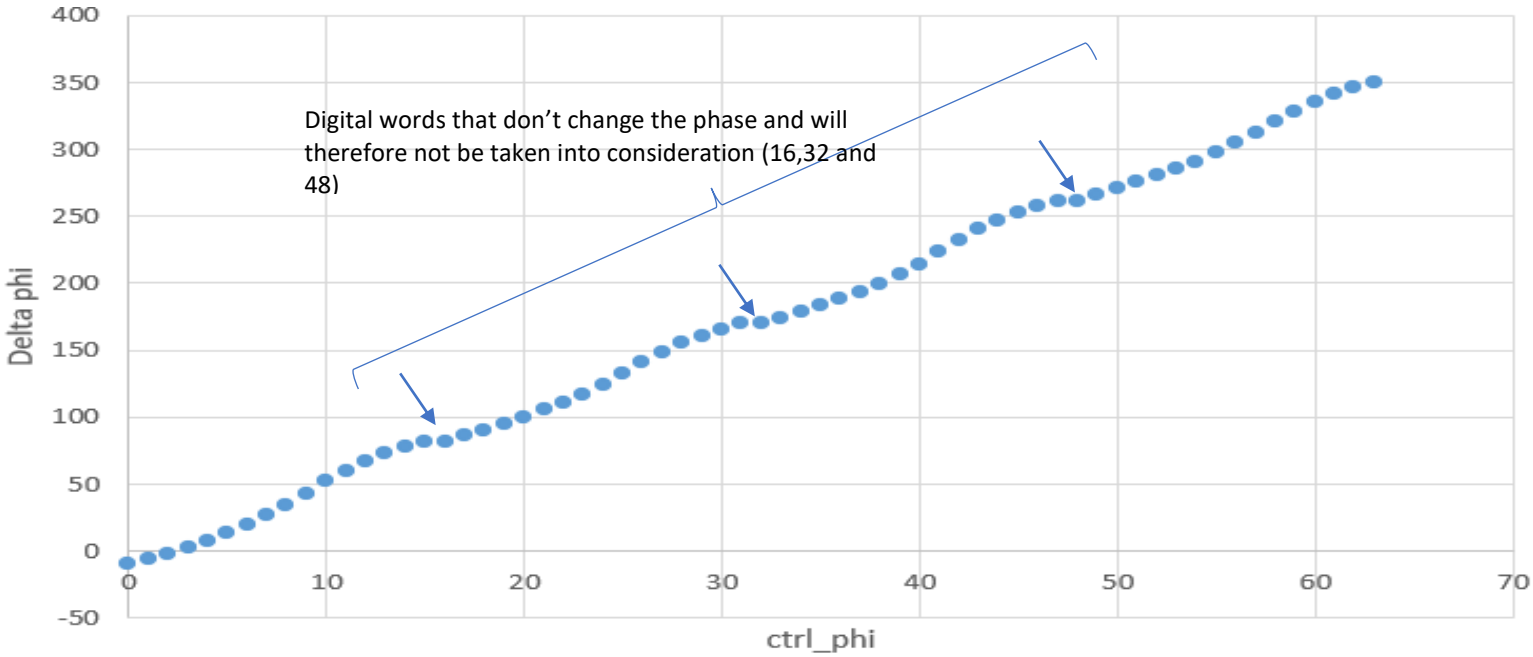


Figure 12: Measured phase (Delta phi) of the outputted clock

Figure 12 shows the measured clock shifting, the code 16,32 and 48 are intermediate code that doesn't contribute to change of the phase but are rather used to switch from one branch to the other: I to $\bar{I}$ or the opposite or from Q to $\bar{Q}$ or the opposite.

4.4- Glitches:

The DAC structure suffers from glitches due to asymmetry of loading as explained in section 3.2. Those glitches will result in a **temporary decrease of the current**, which can be problematic as the outputted clock will not be the correct one, in particular the sampled data through the Flipflop will be wrong and we'll increase and violate a harsh specification of the bit error rate (BER): number of errors of sampling per unit time.

The analysis of glitches and proposed solutions will be done in this section for the first quadrant (from code 0 to code 16) but by symmetry this will solve also the problem for the other quadrants. We have noticed ***two important glitches*** during this work.

4.4.1- Cause of the *first* glitches:

The first glitch arises when passing from code 7 to code 8 which translates in binary passing from 0111 to 1000. We also noticed glitches when passing from 3 to 4 (from 011 to 100) and from 11 to 12 (from 1011 to 1100), but the more pronounced one is from 7 to 8 as we change 4 bits.

We plotted in Figure 13 the tail current in the phaseshifter with its glitches, that arises from glitches from the DAC. As predicted the transition from 7 to 8 is the more pronounced one. We can notice that from code 0 to code 1, the current takes time to settle, this is because we are charging at this time the polysilicon capacitances added in the phaseshifter in order to help filtering the glitches (cf Figure 8).

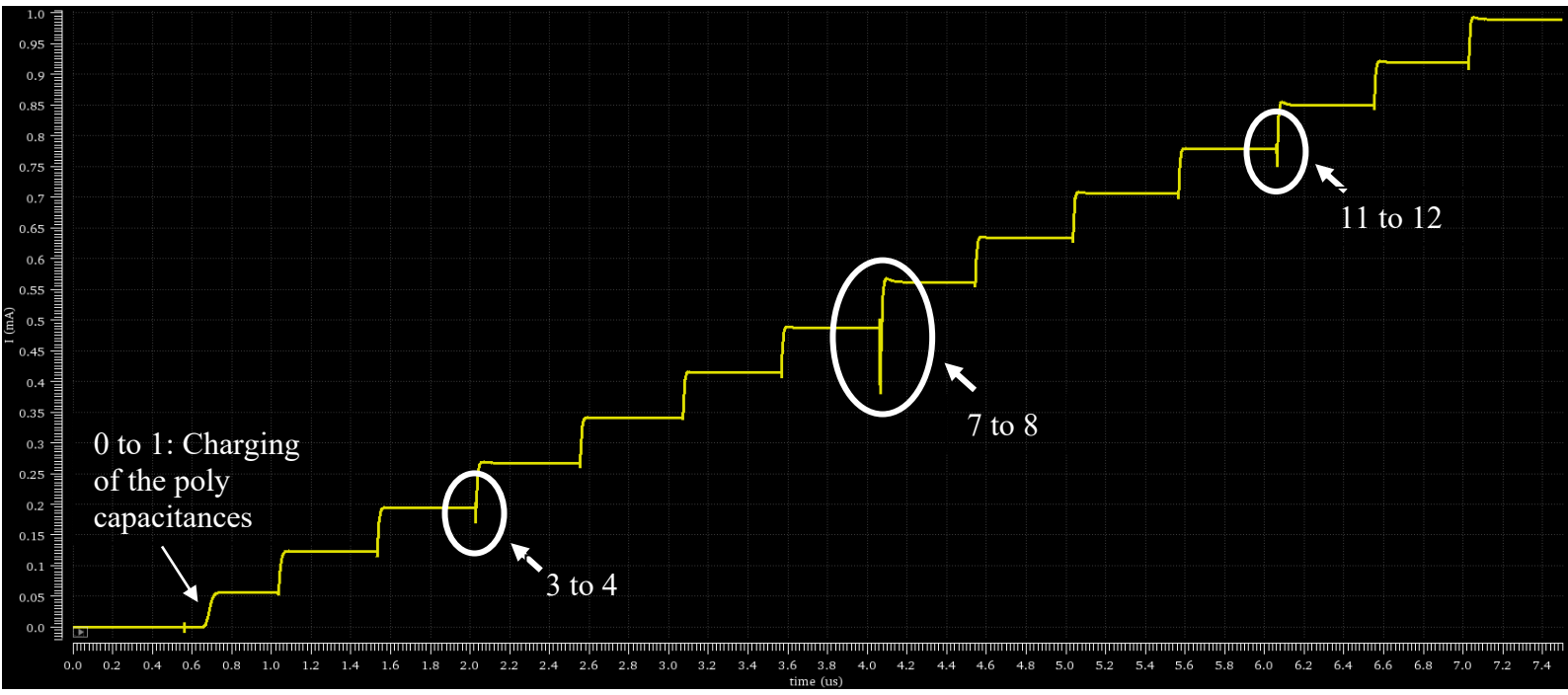


Figure 13: Glitches in the phaseshifter tails current

In figure 14, we show in more detail the transition of the switching bits from 7 to 8 (from 0111 to 1000). As we are dealing with PMOS transistors, their switching threshold voltage is $V_{dd} - V_{T_{pmos}}$ (V_g needs to be lower than $V_{dd} - V_{T_{pmos}}$ to conduct current). We assume for simplicity that V_T=0.4V (It is in general in this order of magnitude), as V_{dd}=1.68V, we set the cursor to highlight the transition to 1.28V. We can see from the graph a region where the outputted bits aren't the targeted ones and therefore leading to a glitch.

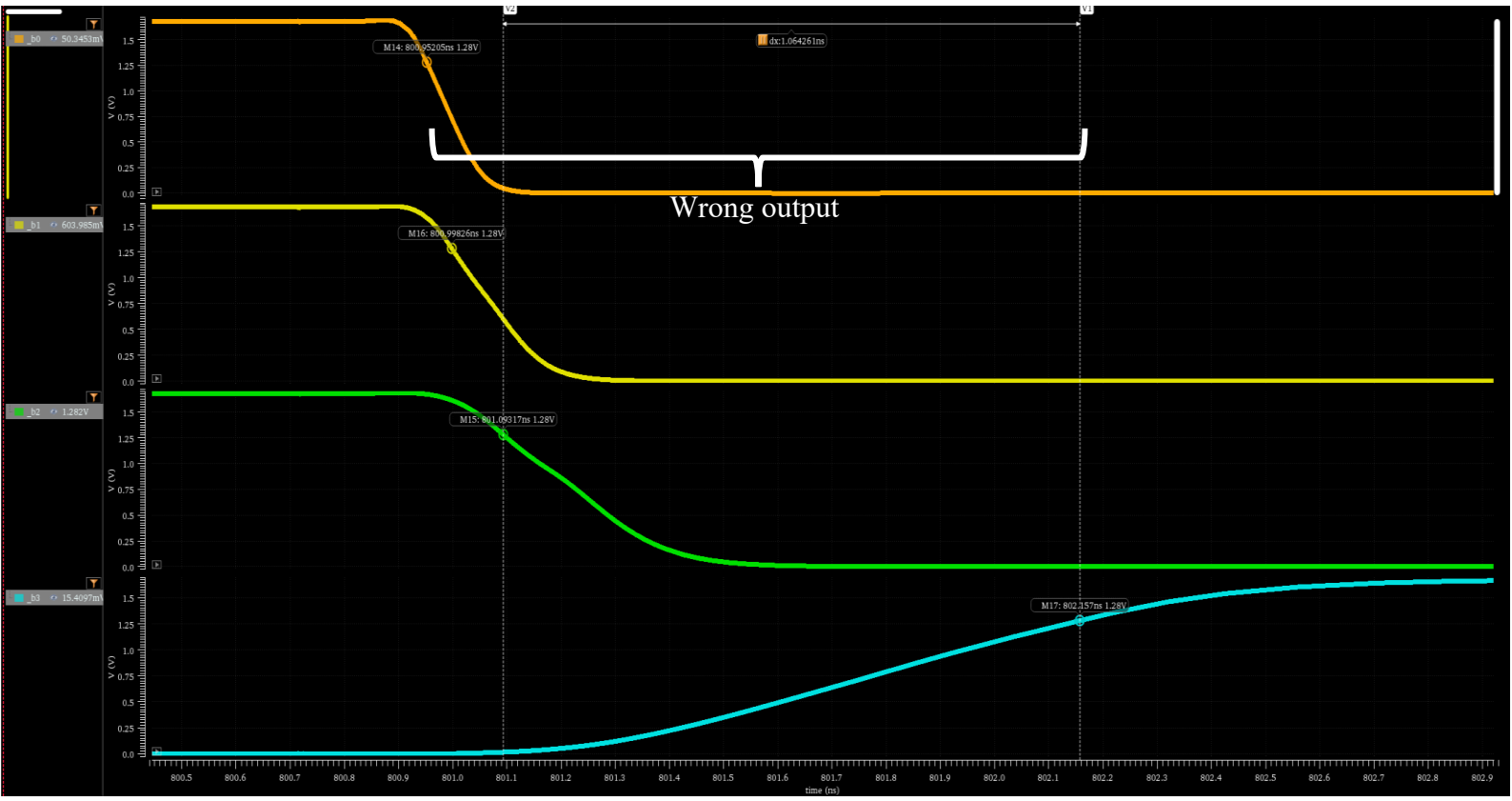


Figure 14: Cause of the glitch

As mentioned before, glitches become problematic when the resulting clock is not the targeted one, for that reason we put a specification of a height of the glitch lower than ½LSB.

In Table2, the simulation results for the nominal case and in PVT (please refer to section 9.1 for more information about the corners configuration) show red cases where the glitch is higher than ½ LSB = 50µA.

Output	Nominal	Corner_fast_0	Corner_fast_1	Corner_fast_2	Corner_fast_3	Corner_slow_0	Corner_slow_1	Corner_slow_2	Corner_slow_3
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
Iout_Q									
glitch_min	454.1u	492.4u	500.6u	496.6u	507.9u	397.8u	401u	382u	409.1u
glitch_min_time	4.016u	4.045u	4.003u	4.008u	4.063u	4.017u	4.023u	4.065u	4.015u
glitch	60.1u	98.31u	45.25u	99.15u	45.71u	83.6u	45.33u	105.5u	46.79u

Table 2: Glitch measurement results in PVT

4.4.2- Suggested solutions:

A first suggested solution to solve the problem of the glitches is to "boost" the switching bit b3, as it is according to Figure 14, the most limiting one. For that we referred to the *logical effort model*, which led us to increase the sizes of the gates gradually (depending on the type of the gates) in Figure2 for the branch of the bit b3, so that we get a faster response of the bit b3 in the sense of a faster transition.

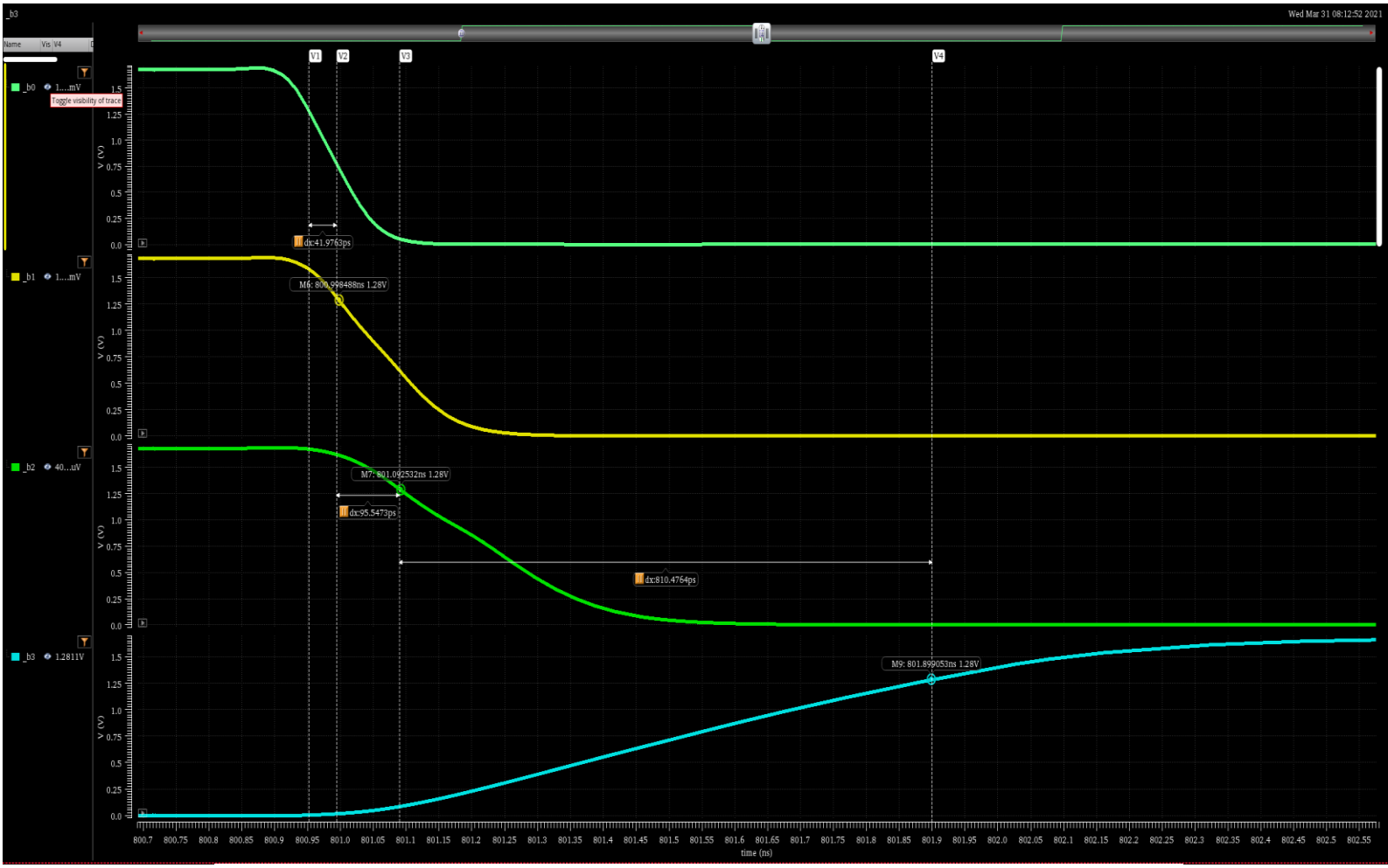


Figure 15: Transition times after increasing the sizes of the gates of b3 branch

The library of the used gates comprises cells of the same gates with different sizes. The best case consisted of changing the second NAND in b3 branch from NAND0 (the smallest NAND gate in the library) to NAND1 (a slightly bigger NAND gate). Figure 15, shows the results of this transition: we passed from 1.06ns delay between the thresholds of b2 and b3 to 810.47ps. This in simulation decreases the size of the glitch but not significantly as shown in tables 3 and 4. Therefore, we didn't investigate further this solution, but we had rather added more filtering capacitances shown in the final testbench in Figure 10. The sizes of those capacitances were determined by layout limitations, we chose the maximum size that can fit the layout we have. The goal of those filtering capacitance, is that during the glitch (wrong range of Figure 14), the voltage across this capacitance will drop and therefore it will start discharging itself, compensating the drop of the current. By descending in the hierarchy, we can see that the connecting way of those added capacitance will make them in parallel with the polysilicon capacitances in Figure 8. Knowing that we added MIM capacitances (for layout reasons) we ended up with the sizes 20,885µm× 33,72µm corresponding to 1,935pF (Table 4).

Output	Nominal	Min	Max	Corner_fast_0	Corner_fast_1	Corner_fast_2	Corner_fast_3	Corner_slow_0	Corner_slow_1	Corner_slow_2	Corner_slow_3
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
Iout_Ib											
Iout_Q											
glitch_min	491.8u	431.2u	542.5u	540.2u	524u	542.5u	530.8u	460.9u	431.2u	463.7u	438u
glitch_min_time	804.6n	803.5n	809n	803.5n	803.7n	805.2n	804.5n	806.8n	809n	807.5n	805.4n
glitch	25.04u	13.86u	53.41u	50.54u	22.01u	53.41u	22.94u	20.34u	13.86u	23.19u	17.05u

Table 3: Glitch measurement with NAND0 and added filtering capacitance configuration

Output	Nominal	Spec	Corner_fast_0	Corner_fast_1	Corner_fast_2	Corner_fast_3	Corner_slow_0	Corner_slow_1	Corner_slow_2	Corner_slow_3
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
Iout_Ib										
Iout_Q										
glitch_min	494.6u		542.8u	526.8u	545.2u	533.6u	463.8u	434.1u	466.1u	440.9u
glitch_min_time	804.2n		803.4n	803.7n	805.2n	804.5n	806.5n	809.1n	807.4n	805n
glitch	22.21u	< 50u	47.97u	19.16u	50.72u	20.17u	17.42u	10.95u	20.78u	14.14u

Table 4: Glitch measurement with NAND1 and added filtering capacitance configuration

The eye diagram of Figure 16 shows the resulting Jitter on the clock around the glitch in post-extraction. The jitter is about 8,376mUI (corresponding to 3.015 degree).

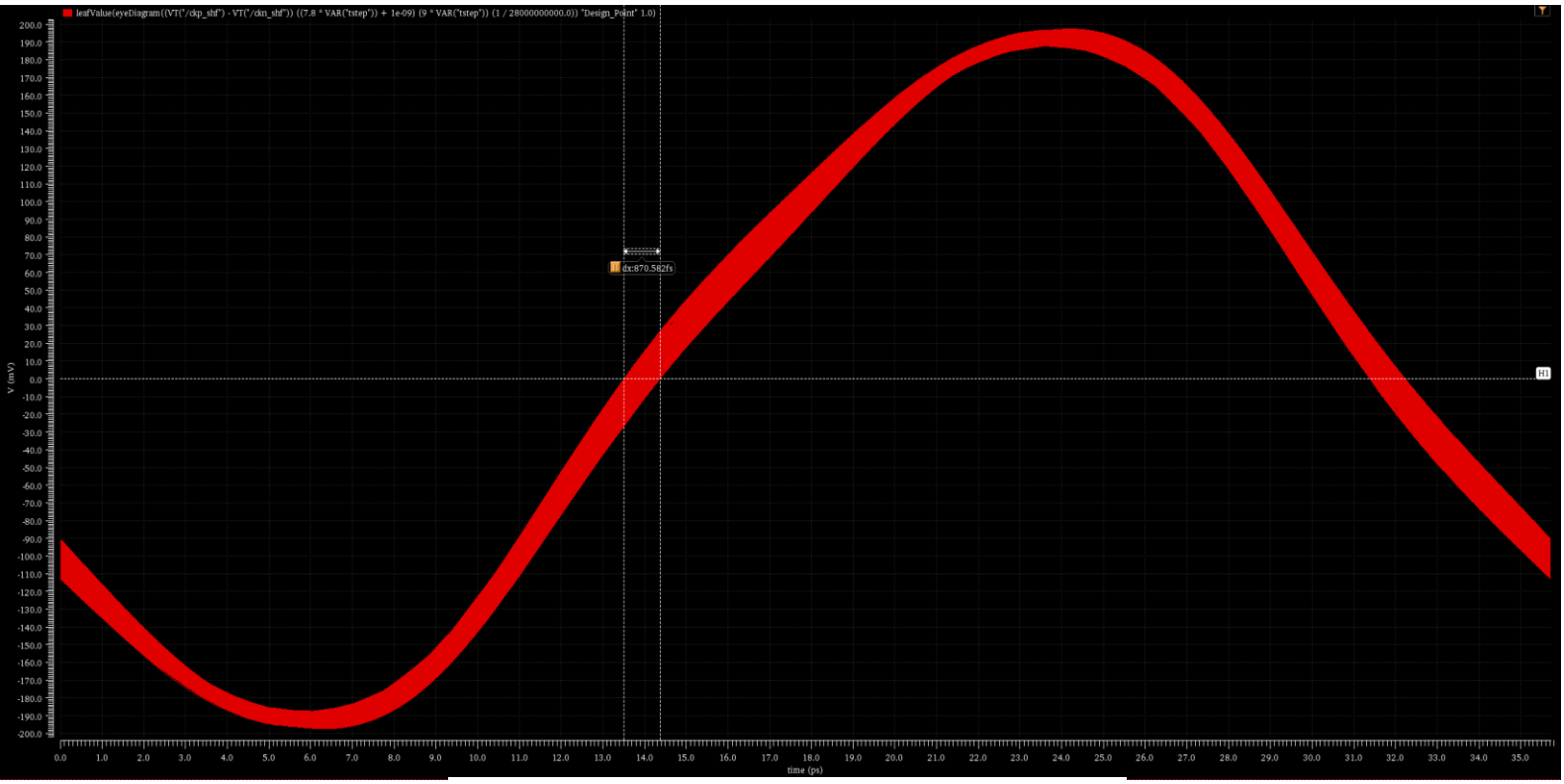


Figure 16: Eye diagram around the first glitch

4.4.3- Cause of the *second* glitches:

The second predominant glitch is seen during the transition from code 31 to 32 (from 011111 to 100000: we have 6 bits varying including bi5) for the branch I. The cause of this glitch is similarly to the previous one caused by an asymmetry of the load, in this case of bit bi4 (see Figure 2), but the process is slightly different.

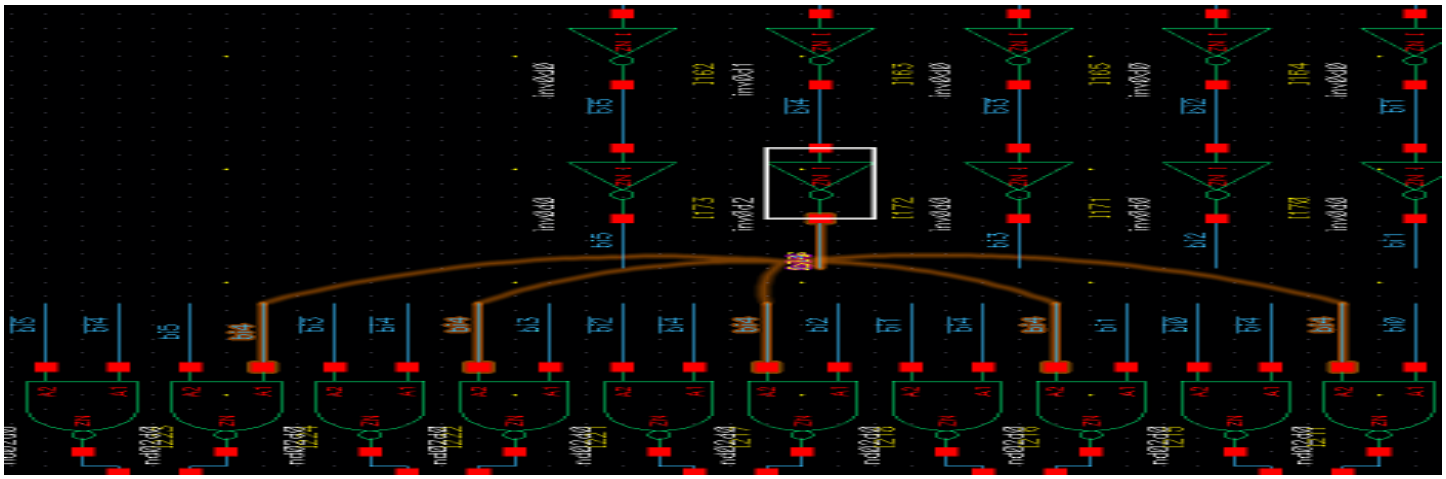


Figure 17: Load of the bit bi4

In Figure 18, we have plotted this glitch for the nominal corner, in this case it is of the order of 60µA and it is even worse for other corners as we see in Table 5. To Try to understand the origin of this glitch, we can take for example the NAND branch of Figure 17 or Figure 2 in the right, this branch as mentioned before performs the XNOR logic function between bi4 and bi0: b0 = $\overline{bi4 \otimes bi0}$, during the transition bi0 and bi4 go both from 1 to 0, but as bi0 is faster in terms of transition as it is loaded on only one switching transistor (therefore less gate capacitance to charge) we get the following scenario:

- Before the transition: b0 = $\overline{1 \otimes 1}$ = 1
- During the transition: b0 = $\overline{1 \otimes 0}$ = 0 (bi0 toggled faster than bi4), here we get the glitch.
- After the transition: b0 = $\overline{0 \otimes 0}$ =1

This representation can be performed for the other loading bits and we'll get the same reasoning and same result leading to the glitch.

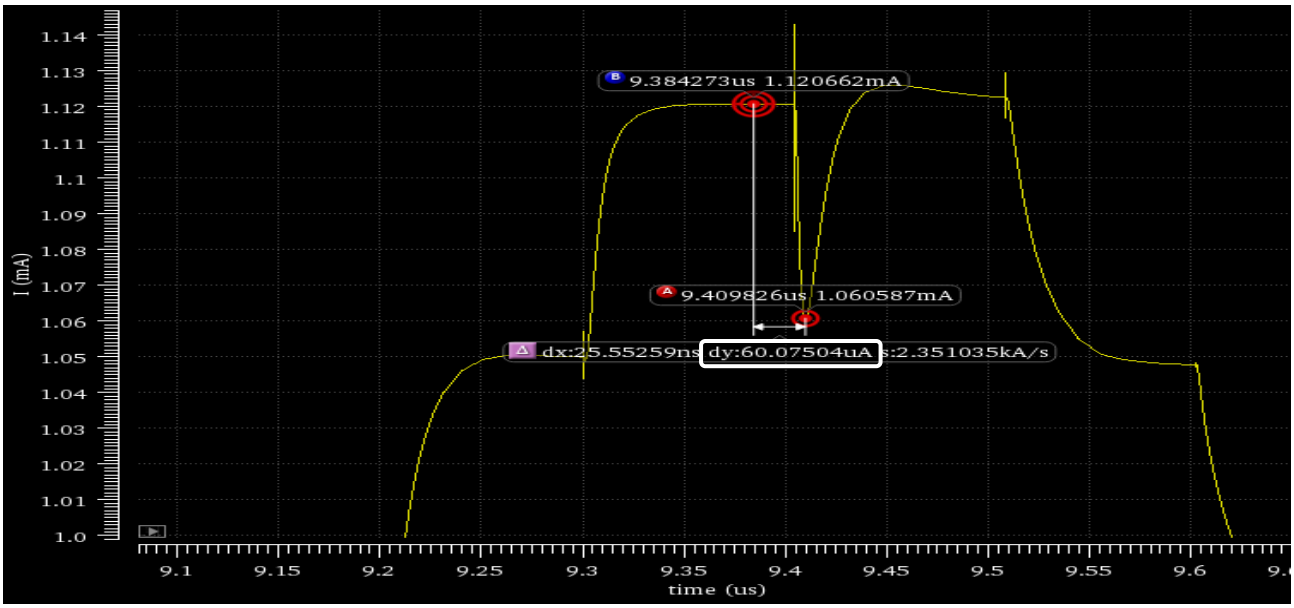


Figure 18 : Glitch in nominal corner

4.4.4- Solution to the *second* glitch:

Similarly to the first glitch, we have chosen to "boost" this time the path of the bit bi4, by increasing the size gradually of its inverters (the branch selected in Figure 17) using the inverters already available in the library with different sizes, in particular we used inv0, inv1 and inv2 (increasing sizes).
Tables 5,6 and 7 show the results of the given solution to this problem and we see that the configuration of Table 7 solved completely the problem

Nominal	Spec	Weight	Pass/Fail	Min	Max	Corner_fast_0	Corner_fast_1	Corner_fast_2	Corner_fast_3	Corner_slow_0	Corner_slow_1	Corner_slow_2	Corner_slow_3
1.061m				889.6u	1.223m	1.216m	1.137m	1.223m	1.157m	966.8u	889.6u	1.003m	925.4u
9.41u				9.407u	9.415u	9.408u	9.41u	9.408u	9.411u	9.408u	9.407u	9.412u	9.415u
60.1u	< 50u		fail	43.19u	123.4u	108.4u	81.76u	123.4u	90.01u	57.2u	43.19u	55.7u	43.91u

Table 5: Results of the glitch for inv0 for the first inverter and inv0 for the second one

Nominal	Spec	Weight	Pass/Fail	Min	Max	Corner_fast_0	Corner_fast_1	Corner_fast_2	Corner_fast_3	Corner_slow_0	Corner_slow_1	Corner_slow_2	Corner_slow_3
1.087m				905.6u	1.266m	1.266m	1.149m	1.246m	1.164m	997.4u	905.6u	1.016m	932.1u
9.407u				9.4u	9.418u	9.408u	9.41u	9.408u	9.408u	9.4u	9.418u	9.415u	9.409u
33.39u	< 50u		fail	26.54u	99.99u	58.64u	69.65u	99.99u	82.75u	26.54u	27.26u	42.78u	37.17u

Table 6: Results of the glitch for inv0 for the first inverter and inv1 for the second one

Nominal	Spec	Weight	Pass/Fail	Min	Max	Corner_fast_0	Corner_fast_1	Corner_fast_2	Corner_fast_3	Corner_slow_0	Corner_slow_1	Corner_slow_2	Corner_slow_3
eval err						eval err	eval err	eval err	eval err	eval err	eval err	eval err	eval err
1.07m				888.1u	1.279m	1.265m	1.16m	1.279m	1.181m	977.4u	888.1u	1.007m	918.5u
9.401u				9.4u	9.401u	9.401u	9.4u	9.4u	9.4u	9.401u	9.4u	9.401u	9.401u
1.118m				931.6u	1.334m	1.317m	1.205m	1.334m	1.224m	1.022m	931.6u	1.057m	967.6u
2.897u	< 50u		pass	685.8n	22.74u	6.841u	13.4u	11.5u	22.74u	685.8n	991.8n	1.369u	1.529u

Table 7: Results of the glitch for inv1 for the first inverter and inv2 for the second one

In Figure 19, we show the final layout of the DAC with all the previously discussed modifications. The added MIM capacitances were not displayed (hidden using the non-visible option of cadence) for sake of ease of reading, but they cover both all the DAC's layout.

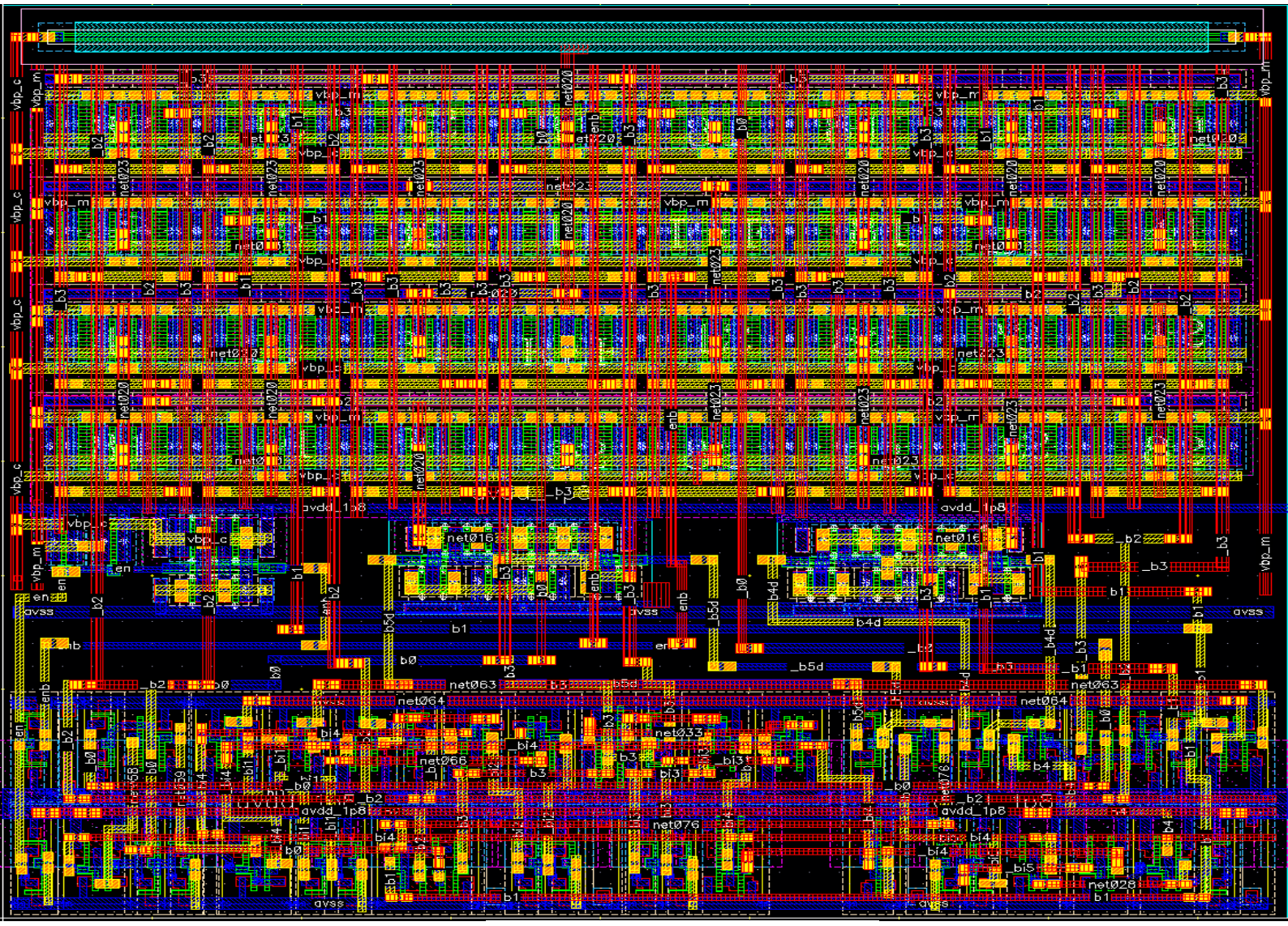


Figure 19: Final layout of the DAC

5.FlipFlop + phase interpolator:

5.1- Introduction:

The phaseshifter previously discussed will generate a clock that will be fed to a FlipFlop to sample a data. In Figure 10, the testbench uses after the phaseshifter a buffer for isolation, a filter to help with the glitches and then the clock is injected to the FlipFlop. As the targeted specification in terms of glitches has been met we don't need anymore the filter nor the buffer and an idea was to directly implement the FlipFlop with the phaseshifter.

5.2- Implementation:

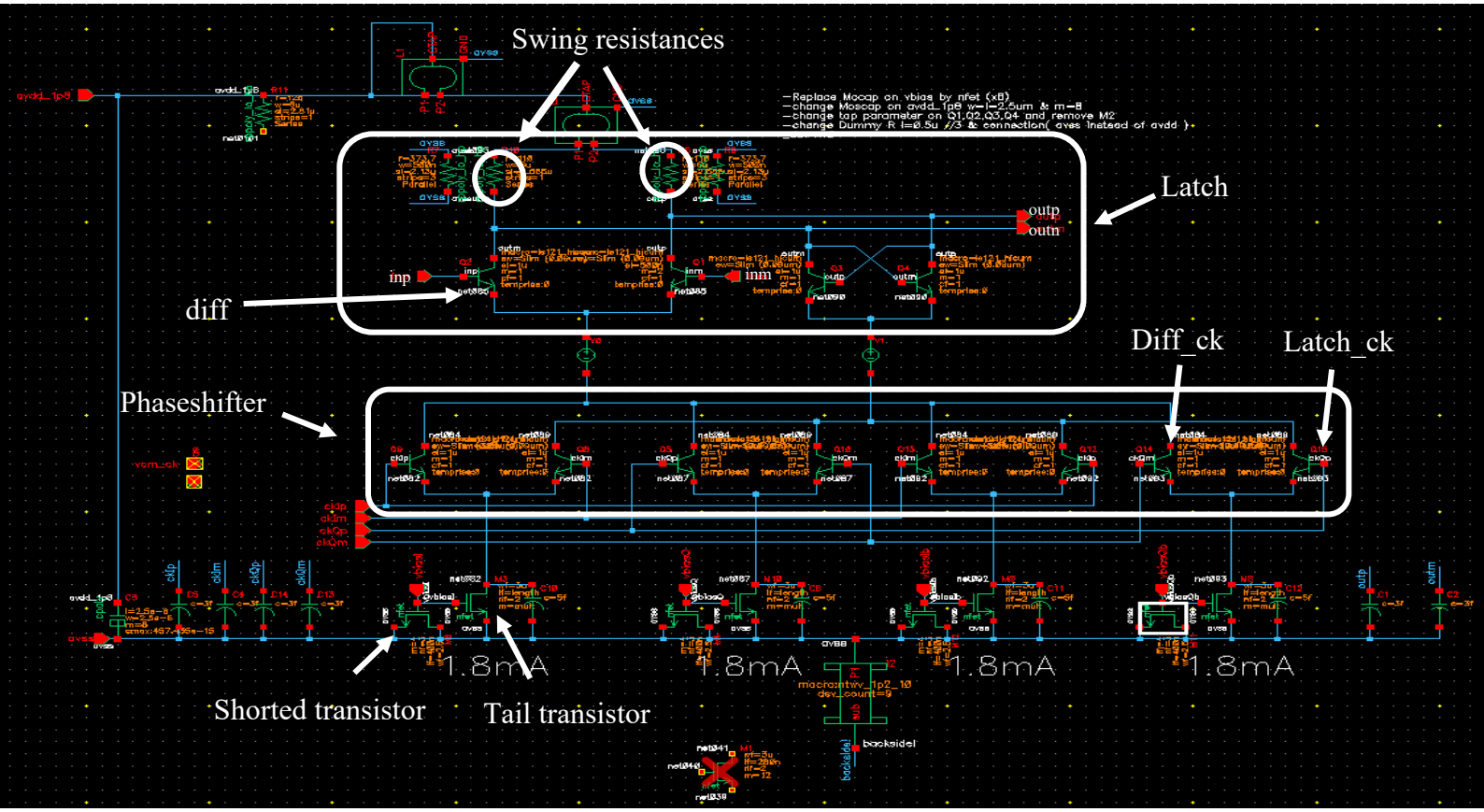


Figure 20: Latch + phaseshifter structure (with annotations for Table 8)

In Figure 20 we show the structure of the implemented latch + phaseshifter. Please refer to Annex 9.2 and annex 9.3 for theoretical demonstrations of the latch working principle and the testbench used for this structure. If we take the example where I and Q branches are activated with weights, the mixed current similarly to the phaseshifter discussed previously will generate a differential clock, That will for a half clock cycle act as a tail current for the differential pair of the latch allowing the input data to go to the output, for the other clock cycle where the regenerative feedback is activated we will keep the data originally computed by the differential pair in the previous half clock cycle, refer to Annex 9.3 for the demonstration.

Concerning the differential pair of the latch, if we take the situation where the positive input ***inp*** is high (inm low), we get outm = V_{dd}- RxI, and when inp is low outm = V_{dd}, therefore the output swing is RxI. The maximum current I is defined to be 1.8mA for speed purposes, and we want an output swing of 200mV therefore we chose a value of the swing resistances of 110Ω.
The use of the shorted transistors is mainly as filtering capacitances, as their drains and sources are tied to the ground along with the bulk, the oxide capacitance of those transistors to the ground is the targeted one.

5.3- Performances:

The phaseshifter in this implementation succeeds in performing exactly the same function as in the previous sections as shown in Figure 21.

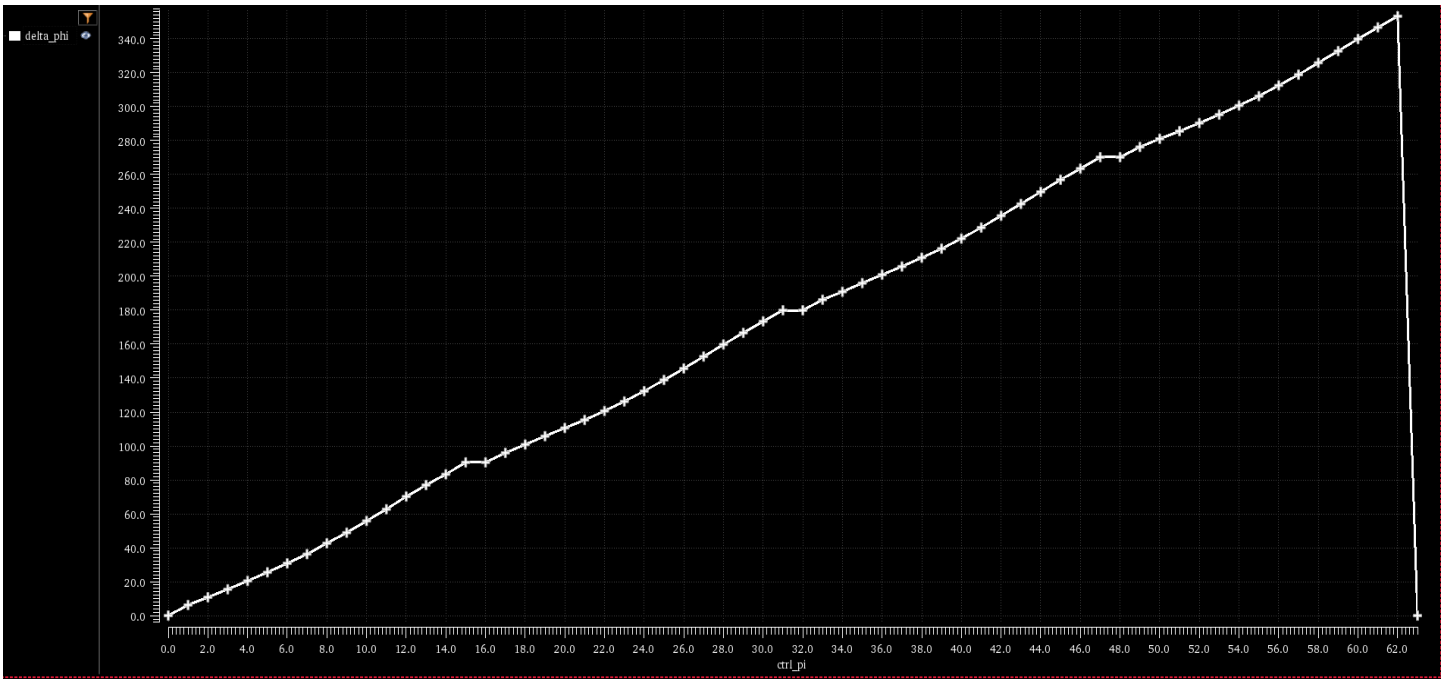


Figure 21: Latch + phaseshifter phase shifting

The main limitation of this structure is the saturation of the transistors, this problematic hasn't been discussed so far and in particular in the previous DAC and phaseshifter as it wasn't a real problem. For what concerns the MOS transistors, we want them to saturate and we set a target of 100mV of saturation margin for sake of robustness. For Bipolar transistors, we want a reverse biasing ($V_{cb} > 0$) of the collector-base pn junction, otherwise we'll get leakage of current to the base. As a "rule of thumb" $V_{be} \approx 0.6\,V$ and since $V_{ce} = V_{cb} + V_{be}$, we use directly V_{ce} for saturation measurement of the bipolar instead of V_{cb}, and the target would be to have $\boldsymbol{V_{ce} > 400mV}$. As the DAC outputs different values of current, we'll get different saturation cases. We'll limit our analysis in this report to the maximum current in one branch (1.8mA in a branch).

5.4- Operating point:

In the computation of the operating point, we used two tests: "switchedon" and "switchedoff" for full analysis. We included a boolean parameter « switched », high in switchedon and low in switched off. In switchedon, it will make the common mode of differential pairs of the phaseshifter changed by 100mV: increased by 100mV for the left bipolar (connected to the diff_pair, *satmargin_diff_ck in Table 8*) and decreased by 100mV for the right bipolar (connected to the latch, *satmargin_latch_ck in Table 8*) to mimic the real behaviour of a working differential pair having one transistor passing (we chose the left one) and the other transistor blocking. In the "switchedoff" test the Boolean parameter is low and the common mode is the same for both transistors of the differential pairs.

The most important transistors of this circuit are the bipolars of the differential pairs of the phaseshifter. As they are "sandwiched" between the latch and the tail transistor, their V_{ce} is the main concern as it may be

lowered. The tail transistors are also important as they copy the current but we will prioritize the bipolars. The strategy to get good saturation margin is to play on the sizes of the tail transistors and the common mode of the phaseshifter bipolars.

We know the formula of the drain current of a MOS transistor in saturation being: $I_d = \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)^2$, and since $V_{ds,sat} = V_{gs} - V_T$, having a drain current fixed (in this case equal to 1.8mA, increasing the width W or lowering the length of the transitor L, will make V_{gs} lower and so a lower $V_{ds,sat}$ allowing us to easily saturate the transistor. The limiting factor is that we cannot play on the length of the transistor L, as it is limited by the technology, but also a length at the limit of the technology will make the transistor parameters vary a ***lot in process***, therefore we chose to act on W. The drain of the tail transistors is a high-speed node; therefore, an exaggerated increase of W will ***limit the speed*** as it will increase the parasitic capacitances.

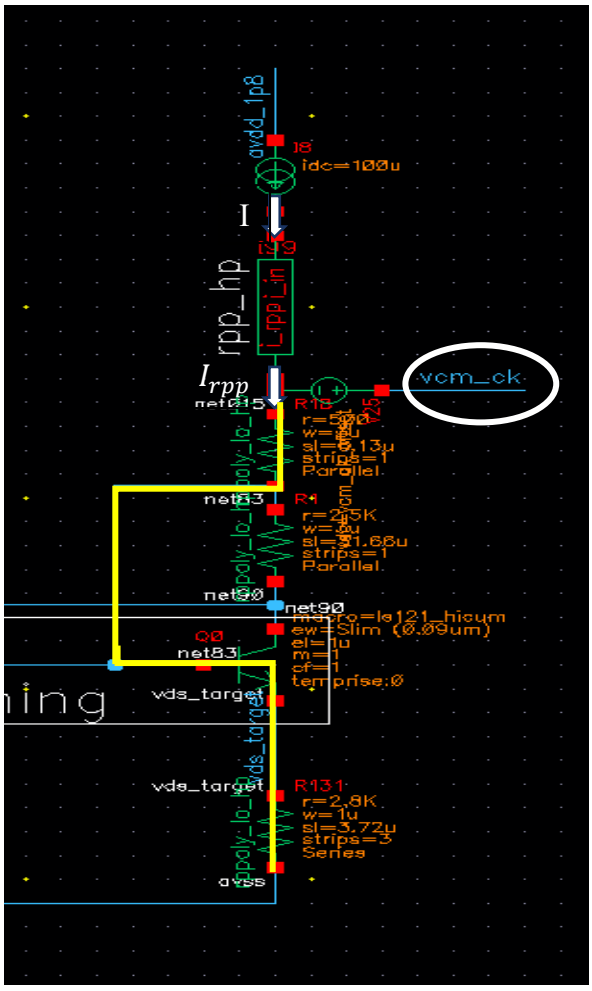


Figure 22: Common mode bias

Figure 22 shows a part of the biasing circuit used to generate biasing voltages for the cells. In particular, Figure 22 shows the branch generating the common mode vcm_ck of the bipolars of the phaseshifter. If we follow the yellow path, we have vcm_ck = $(R_{18} + R_{131})^* I_{rpp} + V_{be}$ (neglected bipolar base current). Being I an ideal current source: the cell rpp_hp generates a current $I_{rpp} = \frac{bandgap\ Voltage}{R_{poly}}$, with R_{poly} a polysilicon resistance of the rpp_hp cell, this modelizes the real current generated by the bandap cell that will be discussed in section 6, and we have the bipolar Q0 having the same size as the bipolars of the phaseshifter, please refer to annex 9.4 for more detail about the rpp_hp cell.
With this vcm_ck and assuming V_{be} doesn't vary too much (which is true, see the exponential curve of I_c as a function of V_{be}). We get a voltage at the drain node of the tail transistor in Figure 20 equal to $(R_{18}+R_{131})^*I = \frac{bandgap\ Voltage}{R}*(R_{18}+R_{131}) \approx 300mV$, and this doesn't vary too much in process, as the process variations of the resistances will be compensated by use of the ratio, and the bandgap voltage is initially designed to be robust againt PVT variations.

The purpose of this circuit is finally to have a voltage that is relatively ***constant with process*** on the drain of the tail transistor and that will allow to saturate it.

In the case we take higher resistances R_{18} and R_{131} for a better saturation of the tail transistor and therefore a higher drain voltage (emitter of the bipolars of the phaseshifter), we'll be limiting the V_{ce} of the bipolars of the phaseshifter and maybe violate the rule of 400mV, therefore we have a tradeoff of vcm_ck.

As mentioned, V_{be} of bipolars remains nearly constant and we approximate it to 0.6V depending on the technology used. Using this assumption, V_{ce} of the bipolars of the phaseshifter is equal to ***the difference between the common mode of the bipolars of the latch and vcm_ck***, we took this difference to be equal to 400mV.

Table 8 shows the saturation of the transistor, in "switchedoff" test, we see that the tail transistors are saturated but not with a good margin to help saturate diff_ck. In some corners for the test "switchedon", diff_ck violates the rule of 400mV, but this still allows to do its function and we can permit it as the rule of 400mV gives a high margin and it is the ideal case seeked.

	Output		temp=-40	temp=110	Corner_fast_0	Corner_fast_1	Corner_fast_2	Corner_fast_3	Corner_slow_0	Corner_slow_1	Corner_slow_2	Corner_slow_3
switchedon	satmargin_diff		853.3m	732.3m	852.7m	734.8m	852m	734.6m	878.4m	777.3m	877.5m	777.1m
switchedon	satmargin_diff_ck		355.3m	546.2m	357.6m	526.3m	583.3m	760.8m	322.9m	497.5m	544.1m	730.3m
switchedon	satmargin_latch_ck		537.6m	726m	540.9m	704.5m	770.4m	942.1m	500.1m	674.5m	726.4m	910m
switchedon	satmargin_tail_transistor		204m	49.93m	191.5m	61.73m	205.4m	66.87m	193.3m	41.64m	211.6m	48.33m
switchedon	satmargin_casc_master	Biasing transistors	181.5m	64.03m	126.7m	20.71m	126.8m	20.86m	235.4m	128.1m	235.5m	128.3m
switchedon	satmargin_mirr_master	Biasing transistors	185.3m	81.38m	190.5m	94.2m	190.4m	94.04m	180.8m	86.75m	180.6m	86.57m
switchedon	sat_margin_dac_mirr		-155.4m	-126.6m	-147.7m	-122.2m	-153m	-127.8m	-166.4m	-141.3m	-174.2m	-148.1m
switchedon	sat_margin_dac_casc		-593.7m	-525.1m	-657.2m	-604.1m	-901m	-853.3m	-336.6m	-337.3m	-733.8m	-663m
switchedoff	satmargin_diff		794.6m	666.2m	790.1m	667.5m	790.1m	667.4m	811.9m	707.6m	811.8m	707.5m
switchedoff	satmargin_diff_ck		439.7m	627.9m	438.4m	611.7m	678m	851.1m	396.8m	575.4m	636.3m	814.5m
switchedoff	satmargin_latch_ck		477.9m	650.6m	474.3m	633.7m	713.8m	873m	430.5m	595.6m	670m	834.7m
switchedoff	satmargin_tail_transistor		140.6m	2.094m	132m	9.5m	132.4m	9.974m	144m	158.6u	144.4m	836.5u
switchedoff	satmargin_casc_master	Biasing transistors	181.5m	64.03m	126.7m	20.71m	126.8m	20.86m	235.4m	128.1m	235.5m	128.3m
switchedoff	satmargin_mirr_master	Biasing transistors	185.3m	81.38m	190.5m	94.2m	190.4m	94.04m	180.8m	86.75m	180.6m	86.57m
switchedoff	sat_margin_dac_mirr		-155.4m	-126.6m	-147.7m	-122.2m	-153m	-127.8m	-166.4m	-141.3m	-174.2m	-148.1m
switchedoff	sat_margin_dac_casc		-593.8m	-525.2m	-657.2m	-604.2m	-901.1m	-853.4m	-336.7m	-337.4m	-733.9m	-663m

Table 8: Saturations of the transistors of the structure

6.Bandgap reference:

6.1- Introduction:

Up to what we have been discussing so far, we have been using an ideal current source injecting current to the cell rpp_hp to generate a bandgap-like current (a current with the form of $\frac{PVT\ independant\ voltage}{R_{poly}}$) in order to mimic the behaviour of the real cell generating current, the bandgap.

The bandgap is a cell generating current for the whole chip. In our implementation it generates 3 types of currents:

- **Bandgap current:** a current with the form of $\boldsymbol{I_{bg}} = \frac{PVT\ independent\ voltage}{R_{poly}}$ (R_{poly} varies by 7% in PVT).
- **Proportional to absolute temperature (PTAT) current:** a current increasing with temperature (with a positive derivative with respect to temperature)
- **Reference current:** a current with the form of $\boldsymbol{I_{ref}} = \frac{PVT\ independent\ voltage}{R_{ref}}$, with R_{ref} being an output resistance not varying in PVT (1% of variation in PVT).

The general idea behind a bandgap circuit is to generate a voltage that is PVT independent, it is often referred to *bandgap voltage* or *reference voltage*. In our implementation using BICMOS, we try to get the following formula:

$$\boldsymbol{V_{bg} = V_{be} + \alpha \times \Delta V_{be}}$$

V_{be} : base-emitter voltage of a bipolar transistor

ΔV_{be} : difference between two base-emitter voltages of two different bipolars

α : proportionality coefficient

By this formula we seek to add two opposite types of voltages, a *Complementary to absolute temperature* (CTAT) voltage V_{be} , that is to say a voltage decreasing with temperature (negative derivative with respect to temperature) and a *Proportional to absolute temperature* (PTAT) voltage ΔV_{be} (positive derivative with respect to temperature) with a coefficient of proportionality α so that we can adjust it to have an independent voltage V_{bg} with respect to temperature (derivative equal to zero).

We'll see during this section, that the process independency of V_{bg} comes from the coefficient α. The voltage supply independency will come from the fact that the supply voltage doesn't enter within the equation of V_{bg} , we will quantify this dependency later during this section using the *Power supply rejection ratio* (PSRR) quantity.

6.2- Bandgap cell:

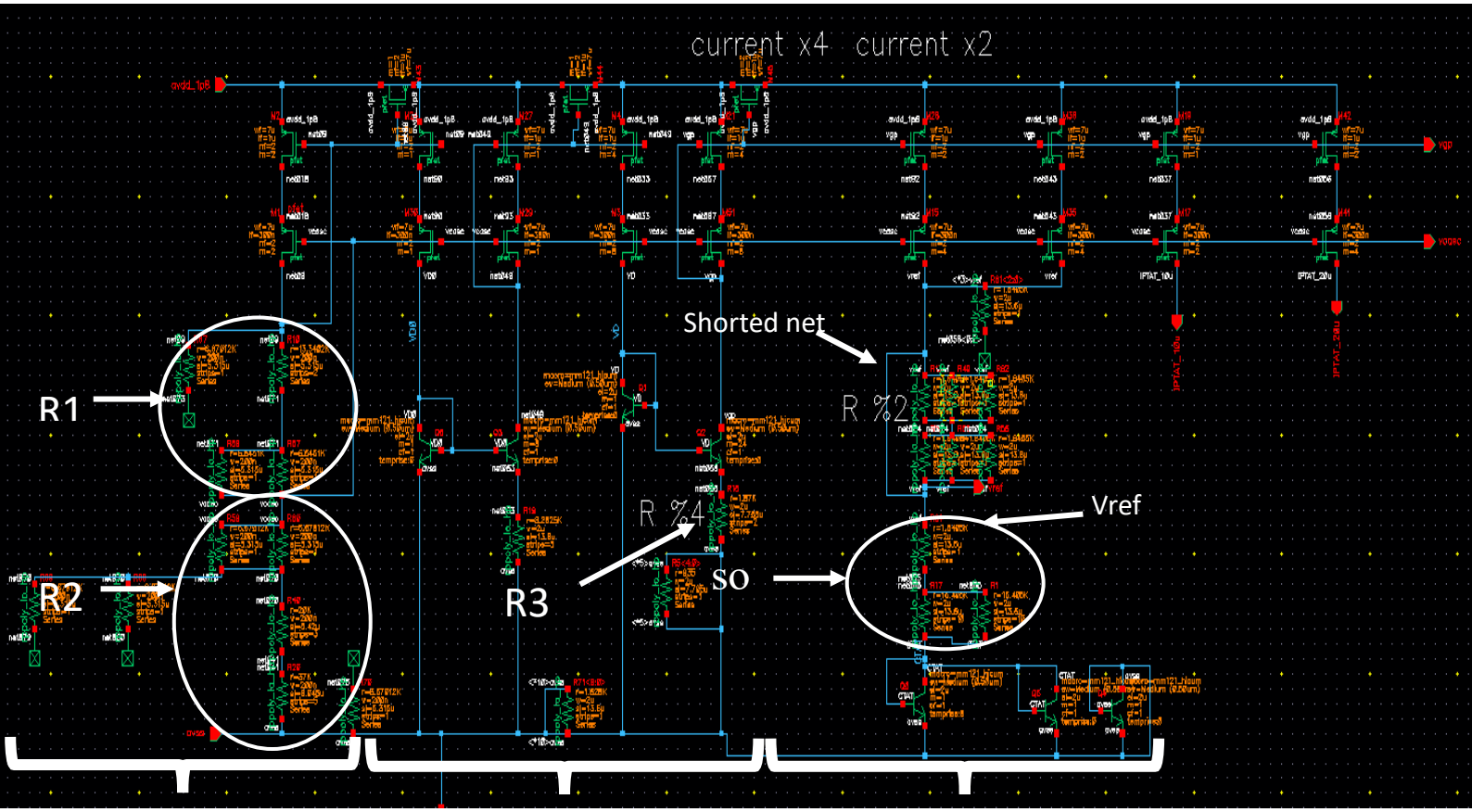


Figure 23: Bandgap reference cell

The bandgap reference cell is represented in Figure 23, it is composed of 3 parts:

- **Biasing branch:** In this branch we generate a current that is not significant for the rest of the analysis, it is used just to activate the circuit. The values of $R_1$and R_2 are chosen depending on the saturation of the transistors.
- **PTAT current branch:** In this branch we generate a current that is PTAT.

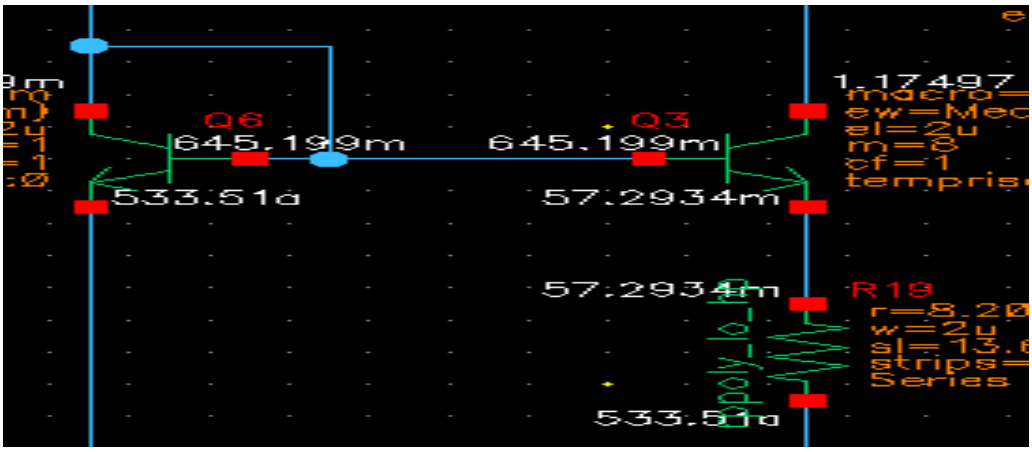


Figure 24: Zoom on the PTAT branch

1. The master branch of the current mirror, gives a base-emitter voltage $V_{be} = V_T \ln\left(\frac{I_s}{I_c}\right)$, and we see that we have a logarithmic dependency with respect to the collector current copied from the *biasing branch* that is highly dependent over the supply voltage V_{dd}, therefore we'll be getting a logarithmic attenuation of the supply voltage noise. We see that we have used two times this branch, the more we use the more we decrease the dependency over V_{dd}, however the PMOS current mirrors have a dependency over V_{dd}, a high variation on the supply will make the copy of the current less effective and we'll see a change of the current. Finally, the supply independency will not be carried by this branch and so we'll limit ourselves to two PTAT branches. We will see further in this report another cell for supply voltage immunity.
2. Using the slave branch and considering **m** the multiplicity of parallel bipolar transistors, we see that the current across the resistor is equal to:

$$I = \frac{\Delta V_{be}}{R} = \frac{V_T}{R}[ln(\frac{I_s}{I_c}) - ln(\frac{I_s}{m \times I_c})] = \frac{k_b T}{q \times R} ln(m)$$

We can see the linear behaviour of this current with respect to temperature, this will be the PTAT current generated by this bandgap cell.

- $\boldsymbol{V_{ref}}$ **branch:** The last PTAT branch generates a current $I = \frac{\Delta V_{be}}{R_3} = \frac{k_b T}{q \times R_3} ln(m)$, this current will be copied to the Vref branch flowing through $R_4$and a bipolar transistor in diode connected configuration and we get:

$$V_{ref} = V_{be} + \frac{R_4}{R_3}\Delta V_{be}$$

We see that the generated voltage has the formula cited during the introduction being $\alpha = \frac{R_4}{R_3}$. As we demonstrated $\Delta V_{be} = \frac{k_b T}{q} ln(m)$ is a PTAT voltage.

The bipolar transistor has intrinsically a base-emitter voltage that is CTAT, and it varies in a linear way with temperature. The slope of this variation depends on the technology, but in general $\frac{dV_{be}}{dT} \approx -2mV/K$. Figure 25 summarizes the idea behind the bandgap voltage cell of summing a PTAT and a CTAT voltage.

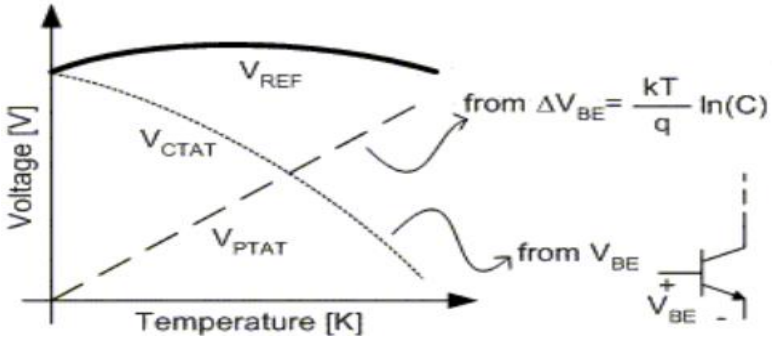


Figure 25: Bandgap cell principle [2]

6.3- Amplifier and bandgap current generator:

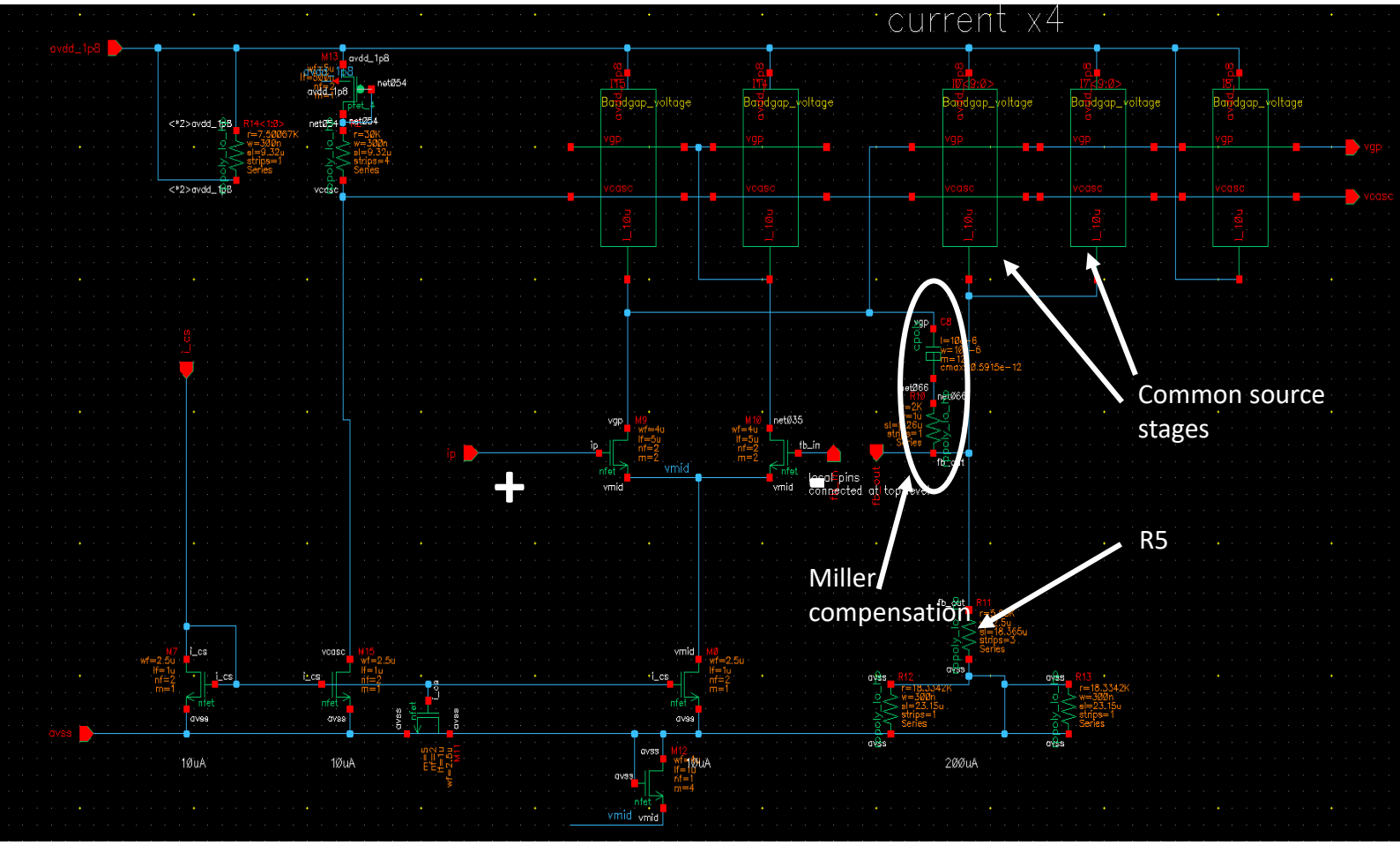


Figure 26: amplifier after the bandgap cell and bandgap current generator

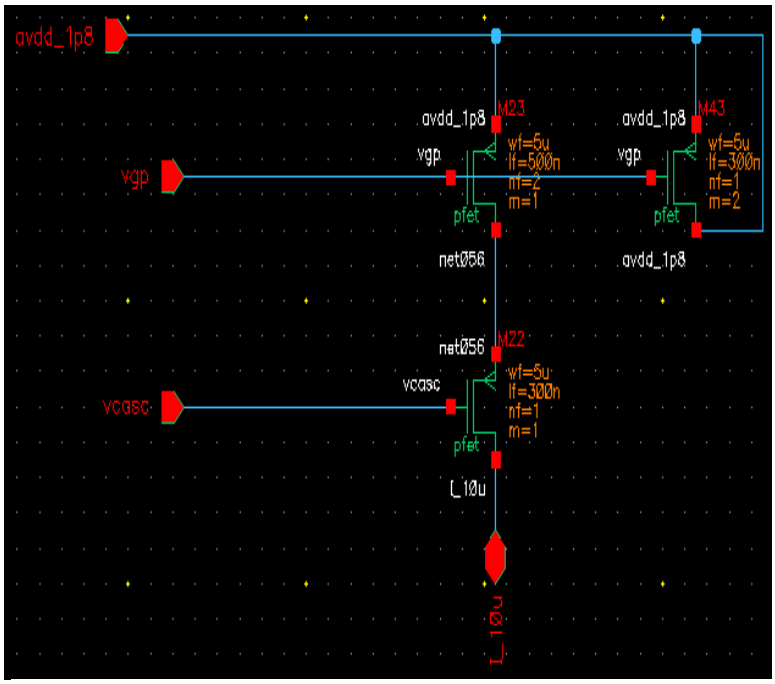


Figure 27: second stage of the bandgap amplifier

The generation of a bandgap current has to use an amplifier, we cannot directly feed the *reference voltage* directly into a resistance to get the $\frac{V_{ref}}{R_5}$ bandgap current targeted, this is because as the V_{ref} branch shown in Figure 23 is composed of resistances, having V_{ref} injected to a resistance to get the bandgap current will put the resistance R_5in parallel with R_4 and therefore lowering the latter's value and altering V_{ref}.

The V_{ref} generated is fed to a very high impedance, which is the gate impedance of the input of the amplifier in figure 27. In particular, V_{ref} is applied to the positive input of the two stages amplifier, while the negative input is connected to the output for a negative feedback in order to copy V_{ref} to the resistance R_5.

The second stage of the amplifier will be used also as a master of a current mirror to copy the generated current $\frac{V_{ref}}{R_5}$ to the different cells of the chip. The generated voltage vgp and vcasc in figure 27 will be fed to the slave branches of the current mirror for the bandgap current generation.

The cascode biasing branch in Figure 26 uses the same idea of "voltage tracking" of Figure 22. The voltage vcasc generated across the upper part of this branch is $V_{casc} = V_{dd} - V_{sg,pmos} - RI$ .The diode connected pmos transistor of this branch is matched with the cascode transistor of the other pmos current mirrors of this cell in terms of size, and as a "rule of thumb" we consider the V_{sg} of a MOS transistor not varying too much with current, this will lead us to a drain voltage of the current mirror (upper pmos transistor of figure 27) of $V_{dd} - RI \approx V_{dd} - 300mV$ letting the current mirrors in saturation and hopefully with a high saturation margin.

Finally, the reference current discussed in the introduction will be generated by the same process of the bandgap current. We will be also using for the reference current an amplifier but this time it will be connected to an external resistance. The main advantage of this resistance is that as it is external it doesn't vary too much with the process, it can typically deviate by 1% from the targeted value and so we get a more stable current.

6.4 – Power supply rejection ratio (PSRR):

The power supplies typically undergo some variations and oscillations, this can be detrimental to a circuit especially when seeking some precise values as for the bandgap or reference current. Therefore, we try to limit and immune ourselves against those variations. We define the *power supply rejection ratio* (PSRR) to

be the logarithm of the ratio between the variation of the outputted voltage and the variation of the power supply (or the inverse in some other textbooks):

$$PSRR = 20 \times log\left(\frac{\Delta V_{out}}{\Delta V_{dd}}\right)$$

We performed some AC analysis in order to quantify this power supply variation. As discussed in 6.2 section, the PTAT current branches of Figure 28 will provide a logarithmic attenuation of the collector current that is very dependent on the power supply, because a variation of the power supply will vary the current through R_1 and R_2. At the same time, a variation on the power supply will vary the source of the current mirrors, and so will affect the whole branch making its immunity against the power supply variation not so efficient.

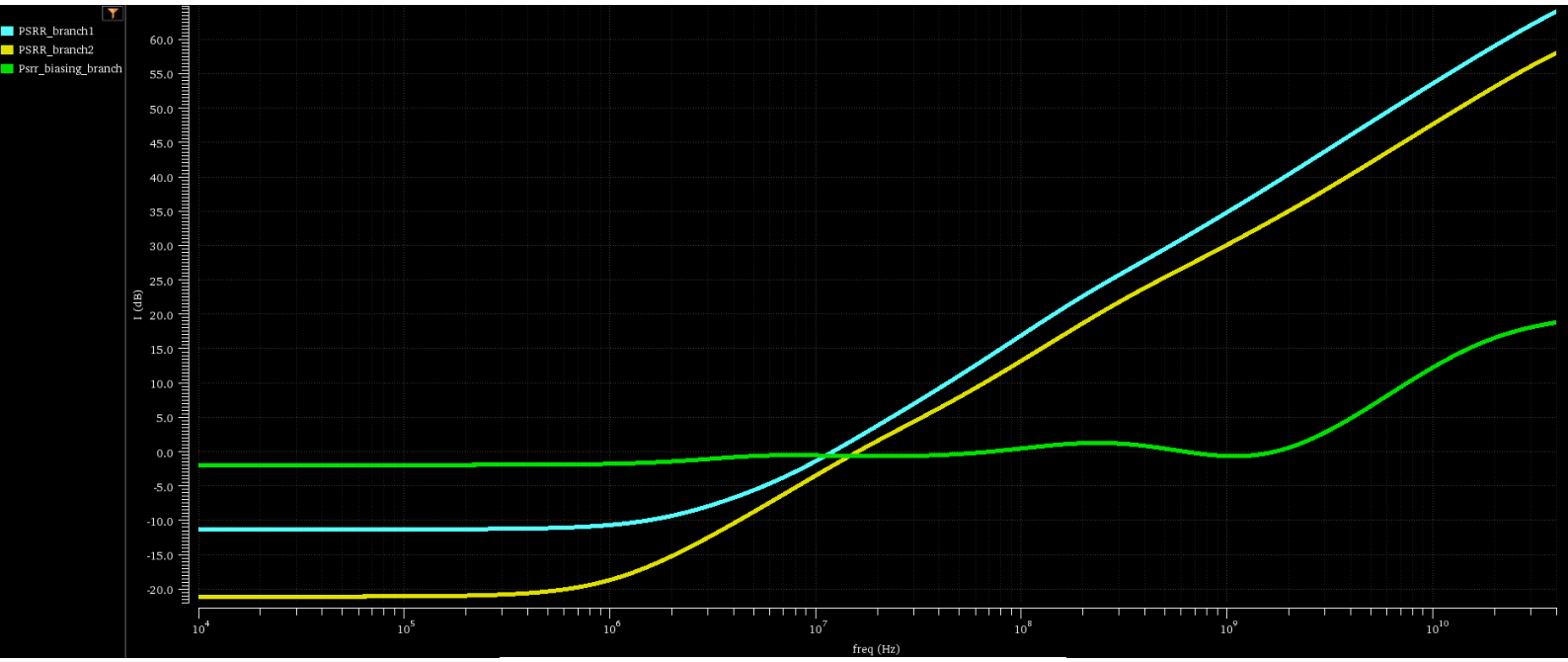


Figure 28: PSRR in the bandgap cell

In figure 28, we plot the PSRR throughout the branches of the bandgap cell having:

$$PSRR_{biasing.branch} = 20 \times log\left(\frac{\Delta V_{R_1+R_2}}{\Delta V_{dd}}\right)$$

$$PSRR_{branch_i} = 20 \times log\left(\frac{\Delta V_{base.branch_i}}{\Delta V_{dd}}\right)$$

With i=1 or 2 and considering their base voltage as the outputted voltage. We can see that the more we pass through the branches the lower is the PSRR, we can keep adding PTAT branches for higher immunity but this implies a higher area.

Originally, the bandgap has been designed with a *power supply regulator* that compensates the variations of the power supply using some feedback loops. We will try in this design to reach the same results of the regulator in terms of supply rejection, especially for the range of frequencies of interest, which is $[1MHz\ 10MHz]$. Alternatively, we use an RC low-pass filter. We tune the cut-off frequency to be lower than 1MHz so that filter start blocking the variations of the power supply starting from this frequency, for this reason, we chose values of the resistor and capacitor of: R=1MΩ and C=1pF and we get a cut-off frequency of:

$$\mathbf{f = \frac{1}{2\Pi\, RC} \approx 159.15kHz}$$

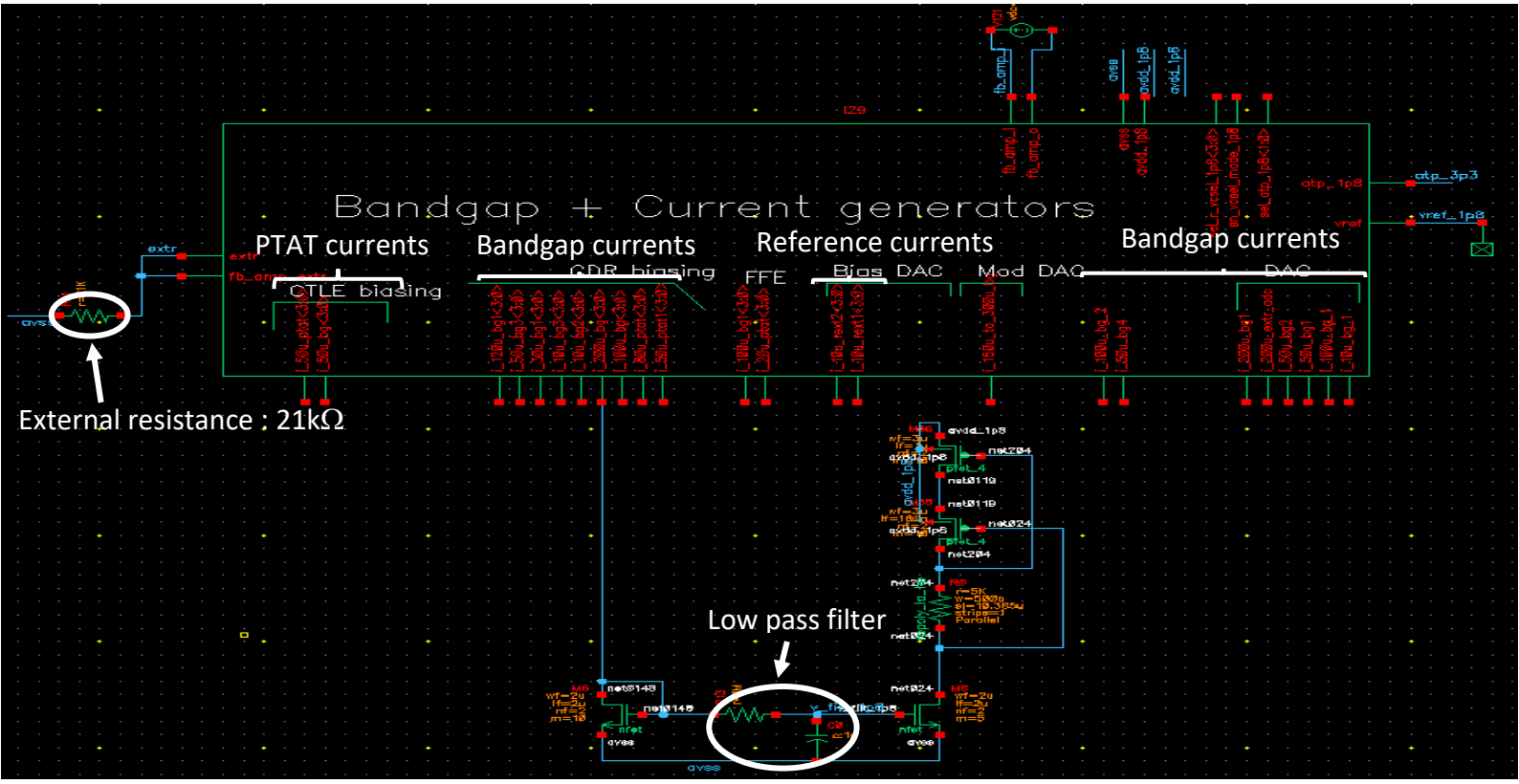


Figure 29: Top bandgap cell + amplifiers current generators + low pass filter

In Figure 30, we present the results of the PSRR with the regulator and the filter coloured in white and yellow respectively, the output voltage for PSRR calculation is the output voltage of the filter. We see that starting from the range of frequencies of interest $[1MHz\ 10MHz]$, we have a better rejection from the filter than from the regulator since we are below -40dB, an initial target that the regulator couldn't reach and has been replaced by the filter.

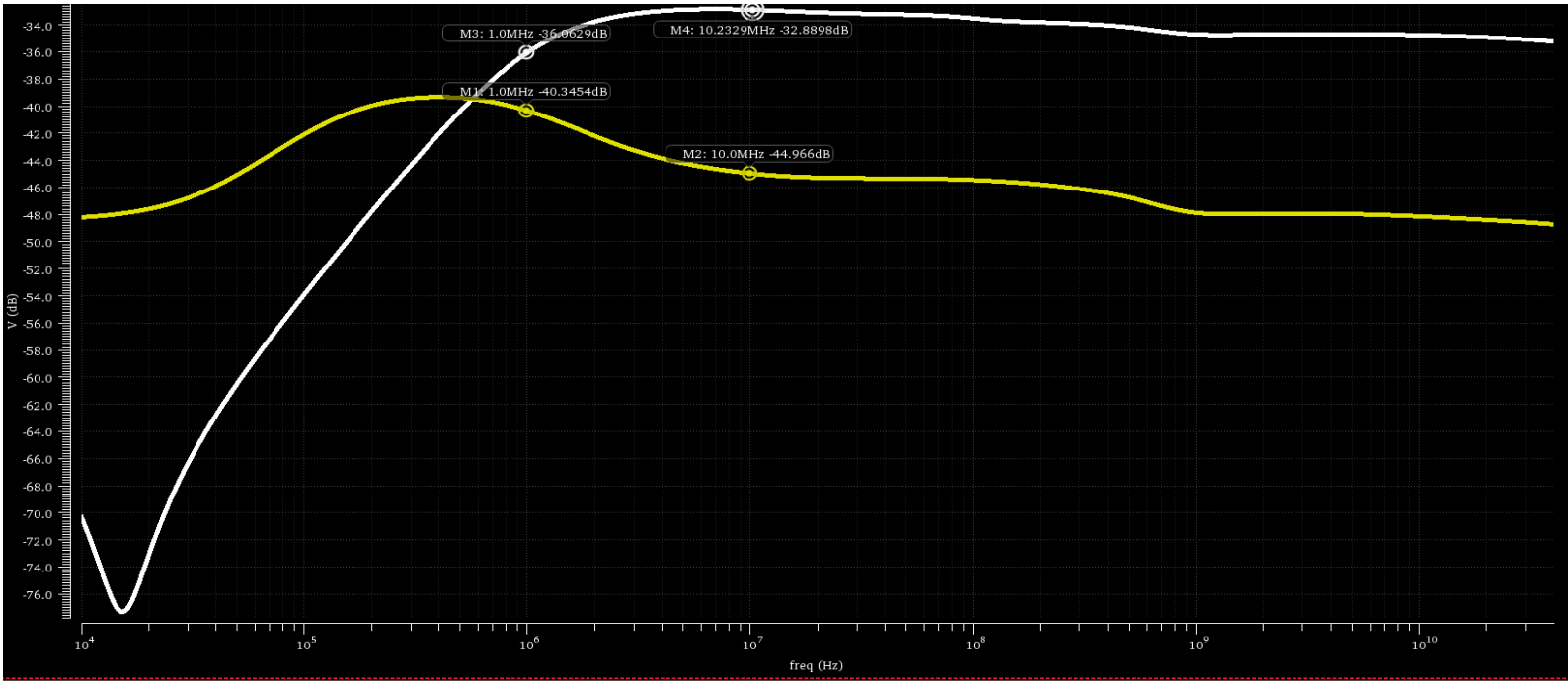


Figure 30: PSRR using the regulator (white) and using the filter (yellow)

Although the regulator performs a high rejection at low frequencies, it doesn't fulfil the specifications at the frequencies of interest, also the design of the regulator uses bulky components (bulkier multiple times than the filter).

6.4 – Layout of the bandgap:

6.4.1 – Parasitic resistances:

As discussed during the previous sections the values of the resistances are very important for the bandgap as they determine V_{ref} through R_3 and R_4 but also, they determine the values of the bandgap current through R_5.

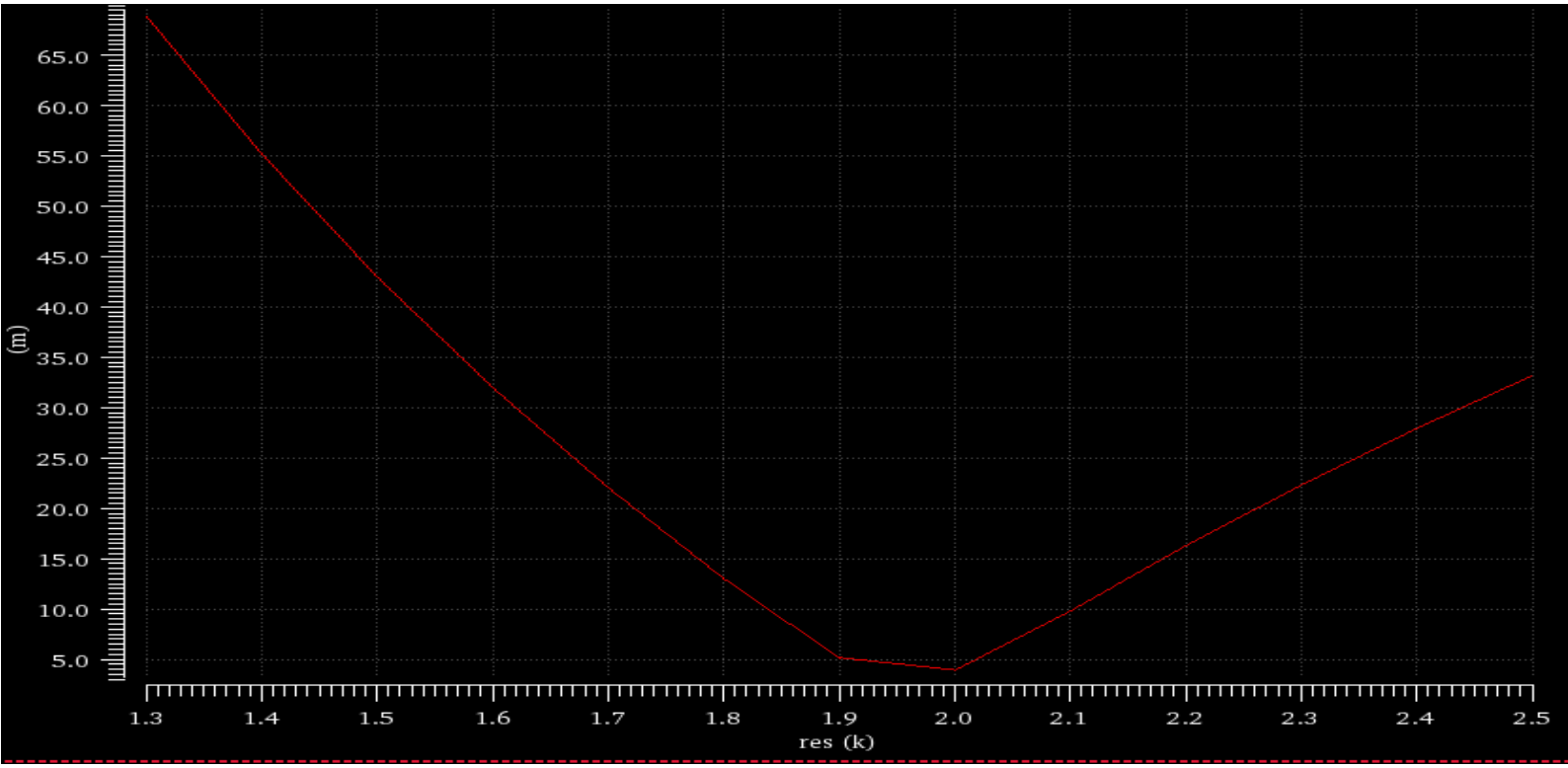


Figure 31: Variation of V_{ref} with R_3

As an example of important resistance, we can analyse the resistance R_3. We performed a sweep over temperature of $\mathrm{V}_{\mathrm{ref}}$ for values of R_3 within the range $[1.3k\Omega\ 2.5k\Omega]$ and we plot in figure 31 the difference of the extrema of $\mathrm{V}_{\mathrm{ref}}(T)$: max $(\mathrm{V}_{\mathrm{ref}}) - min\ (\mathrm{V}_{\mathrm{ref}})$, as a function of R_3. We can notice reaching a minimum around 1.9kΩ, motivating our choice for 1.87kΩ for R_3 (less dependency over temperature).

In Figure 31, we highlighted the importance of the values of the resistances to be precise. In the case of a bad layout, we will get some additional parasitic resistances that might alter the targeted values in schematic. To minimize parasitic resistance, we try to **shorten** as much as possible connections, route with wide metals ($R = \rho\frac{L}{W\times t}$, $\rho: electrical\ resistivity, L: length, W: width\ and\ t: thickness$), and finally maximize number of parallel vias to get lowered parallel vias resistances.

6.4.2 – Layout matching and Common centroid structure:

Analog layout requires often to have matched parameters of transistors: for differential pairs we want same V_{gs} for low voltage offset, for current mirrors we want same drain current…, to achieve this goal we adopt several matching techniques in order to have external variations affecting the transistors of interest in a symmetric way. The main external variations of interest are lithography variations, rotation (we try to have transistors to be matched laid in the same direction), process variations (mainly etching) and temperature gradients [3][4]. For that, matched transistors need to have same sizes and we try to make them surrounded by the same environment. A general formula of standard deviation of a particular parameter X (threshold voltage, β-parameter, drain current …) , has been proposed by scientist Pelgrom in 1989 [5] being expressed as: $\sigma_X^2 = \frac{A_X^2}{WL} + S_X^2 D^2$ with A_X *and* S_X being some process constants given by the foundry depending on the technology used, W and L are respectively the width and the length of the similarly sized matched transistors, and D is the distance between those transistors.

A general technique used in our layout is the common centroid structure, consisting of decomposing the transistors to be matched into equally sized fingers (small transistors fragments of a bigger transistor), the connections are then performed in such a way of a symmetric structure with the same "gravity centre". Taking the example of a gradient of temperature, we see from Figure 32 that it will affect equally the matched transistors A and B in common centroid structure, no matter the angle of the temperature source (even laterally).

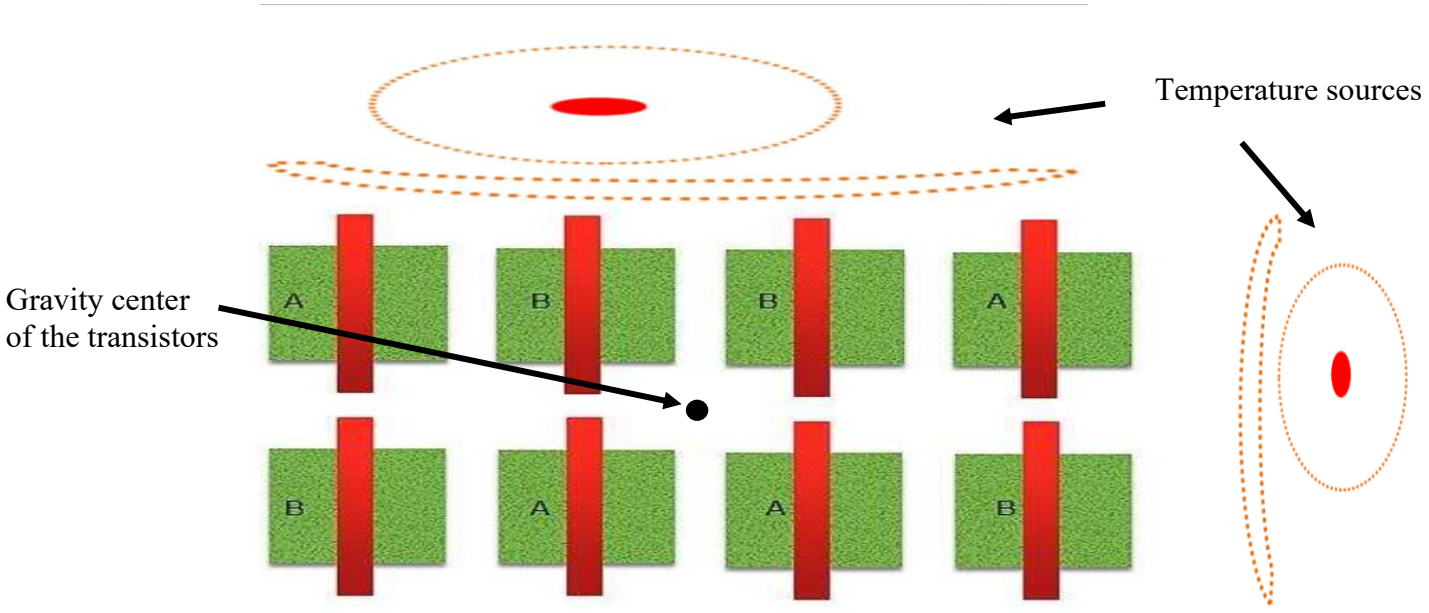


Figure 32: Example of a common centroid structure

We can notice that the transistors of the edge in Figure 32 don't "see" the same environment since they have a transistor on one side and nothing on the other side. To have a good matching (to have all transistors with the same environment) we add dummy transistors on the edges, those transistors are shorted to not draw current and are just laid for process matching.

A final consideration in a layout is to always use an even number of fingers, so that the matched transistors are symmetrical in terms of current flow. A more representative image of this idea is drawn in Figure 33.

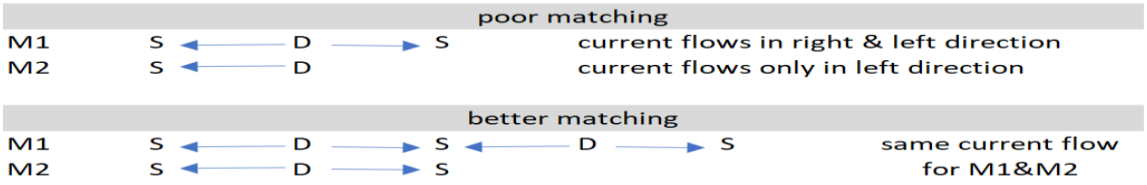


Figure 33: Current flow symmetry for matching

6.4.3 – Final layout of the bandgap:

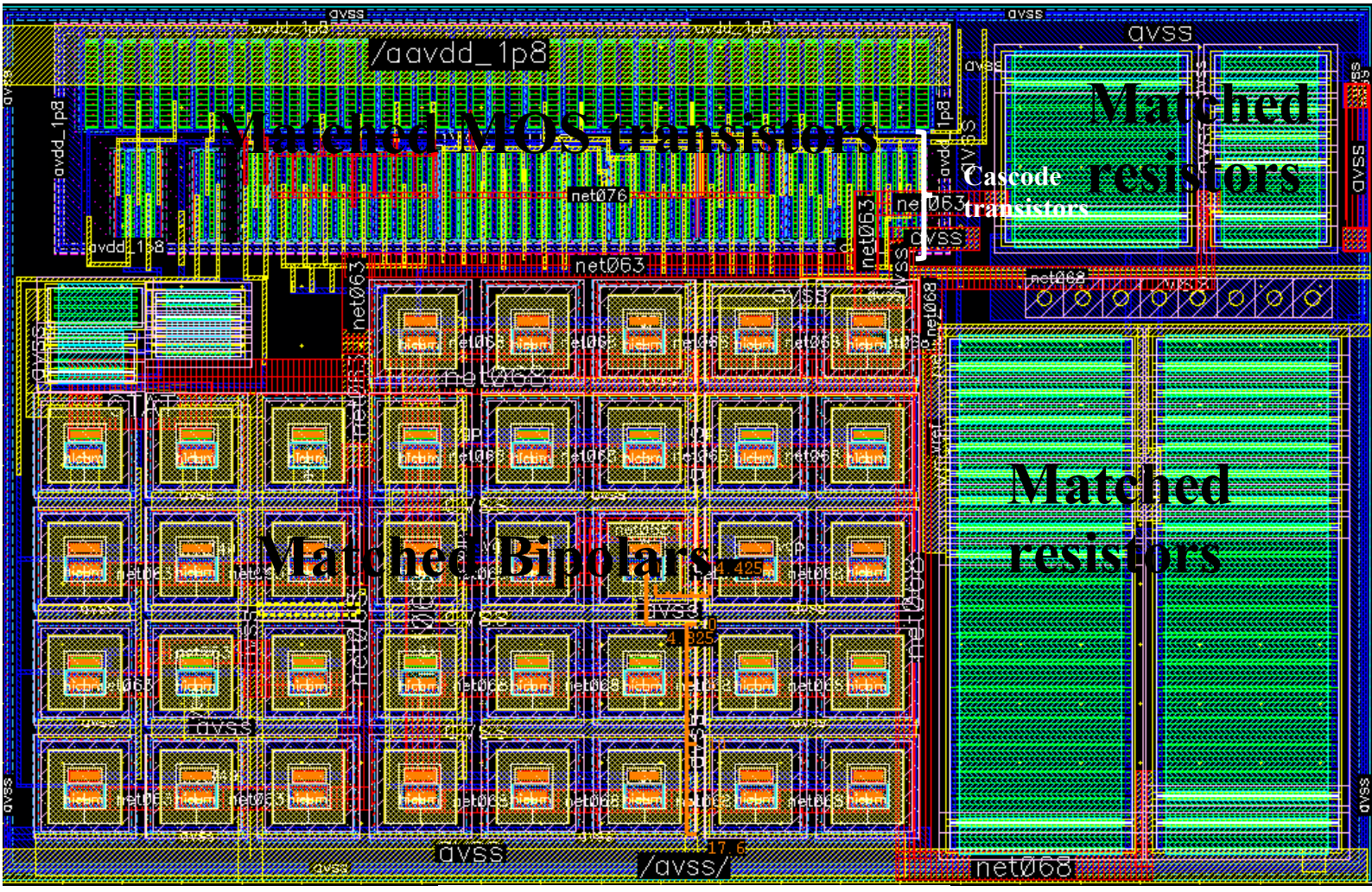


Figure 34: Final layout of the bandgap

Figure 34 shows the final layout of the bandgap with the previously discussed matching considerations. In Table 9, we report the results of the parasitic resistances at the node of important resistances due

to metal wiring and vias. We see that at maximum we have a resistance of 4.5Ω that wouldn't affect the circuit too much in terms of performances as we will see in the next section.

Net name	Wire resistances(Ω)	Via resistances(Ω)	Total resistance(Ω)
CTAT	3,732	0,282	4,014
Net055	0,124	//	0,124
Vref to R4	0,399	0,037	0,436
Net068 (worst path)	3,856	0,449	4,305
R18(1,87kΩ) to avss	0,213	//	0,213
Net063	3,399	0,893	4,292
R19(8,2025kΩ) to avss	0,116	//	0,116
Bipolar Q6 to avss	0,712	0,061	0,773
Bipolar Q1 to avss	1,101	Negligible	1,101

Table 9: Parasitic resistances at important nodes

6.5 – Schematic and post-extraction performances:

In this section, we will discuss the performances of the Bandgap for schematic and post extraction layout. We will be comparing two versions of the schematic with and without parasitics of bipolar (option to check within the schematic editor to include the parasitic of the bipolar). We will also be comparing two versions of the layout, a first version where we weren't severe in terms of layout considerations (less layout matching, asymmetrical routing on polysilicon…, please refer to annex 9.5) and a second version where we tried to improve and correct those layout rules (Figure 34).

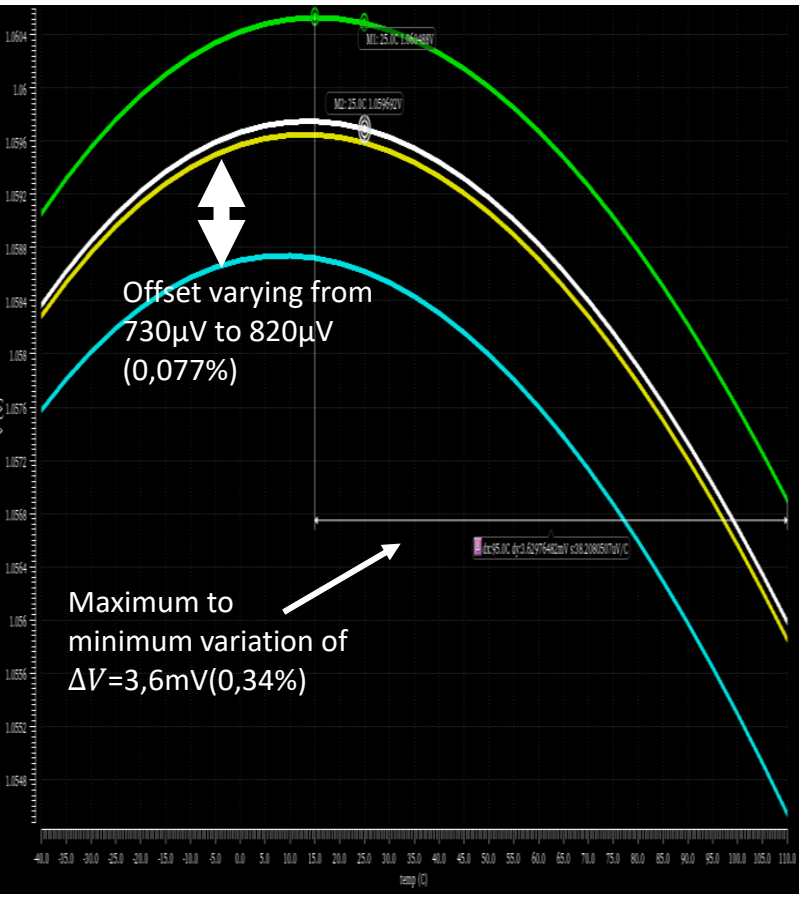


Figure 35: V_{ref} as function of temperature. Blue : new version's layout extraction, yellow : schematic without parasitic, white : schematic with parasitics and green : old version's layout extraction

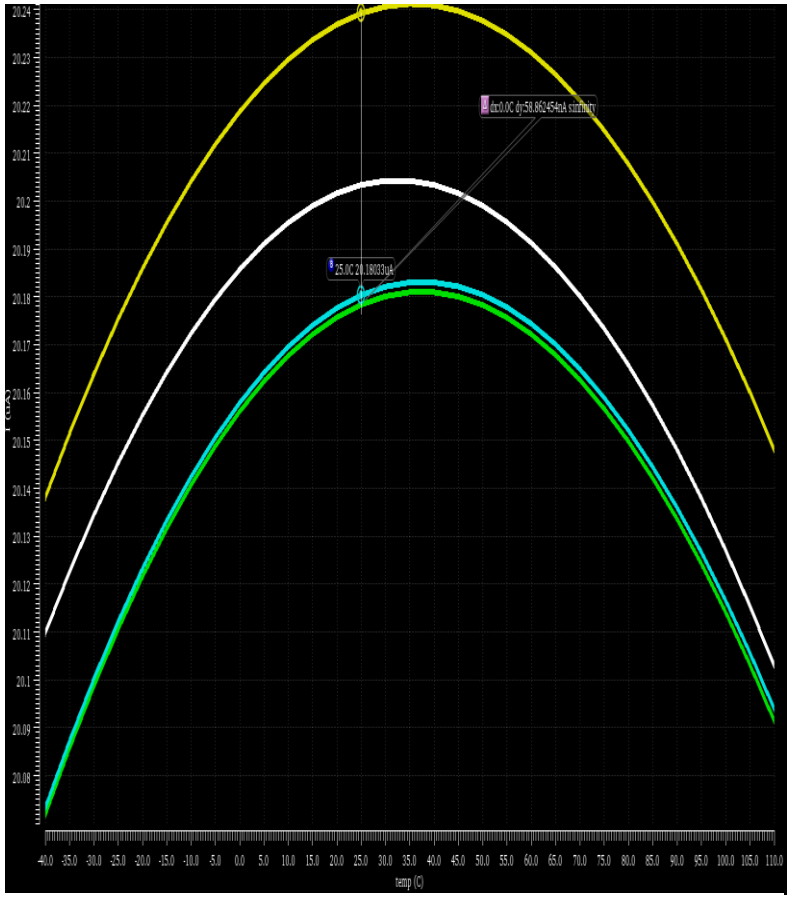


Figure 36: I_{bg} as function of temperature. Green: schematic without parasitics, Blue: schematic with parasitics, white : new version's layout extraction and yellow : old version's layout extraction

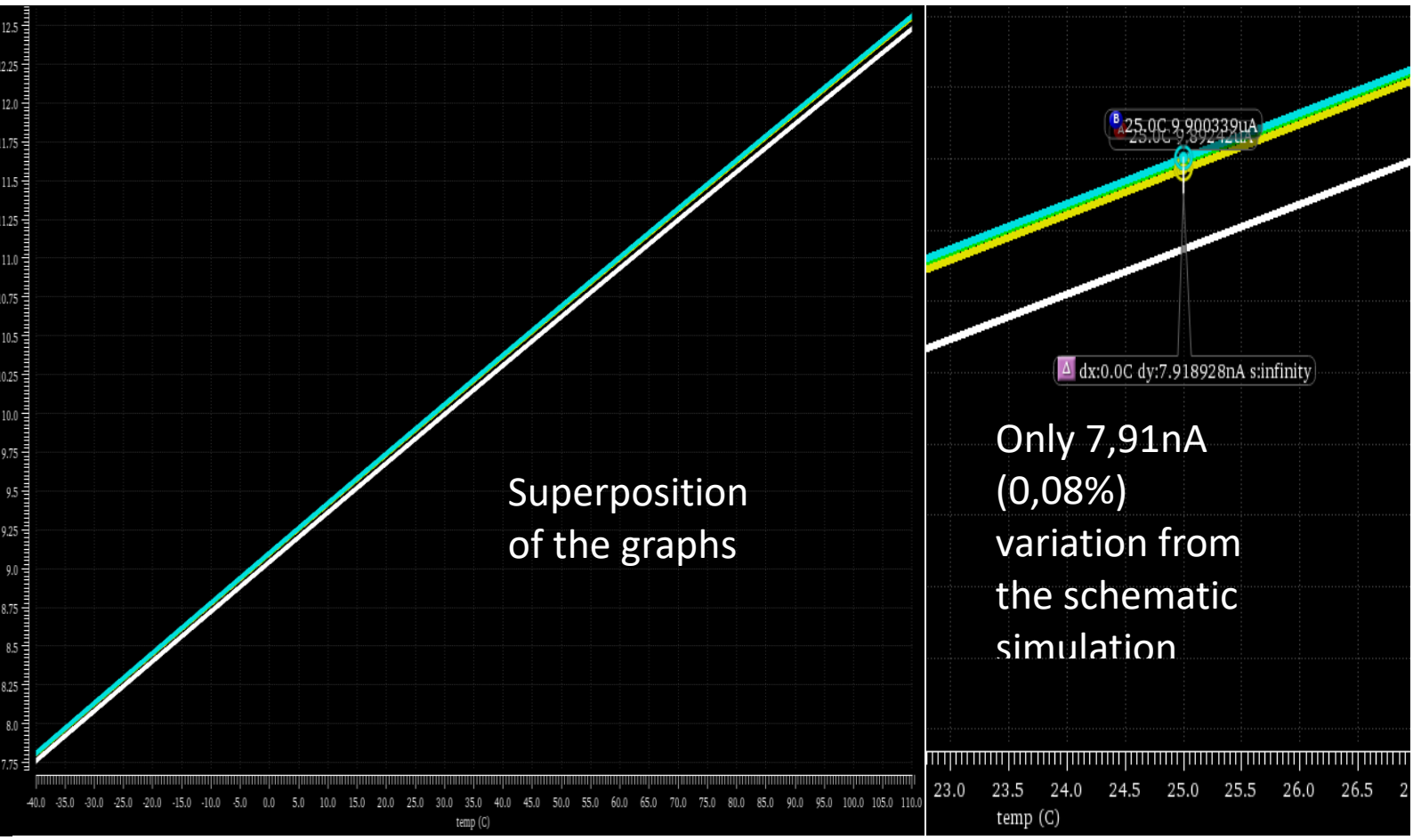


Figure 37: I_{ptat} as function of temperature. White: old version's layout extraction, yellow : new version's layout extraction, Green: schematic without parasitics (overlapped), Blue : schematic with parasitics

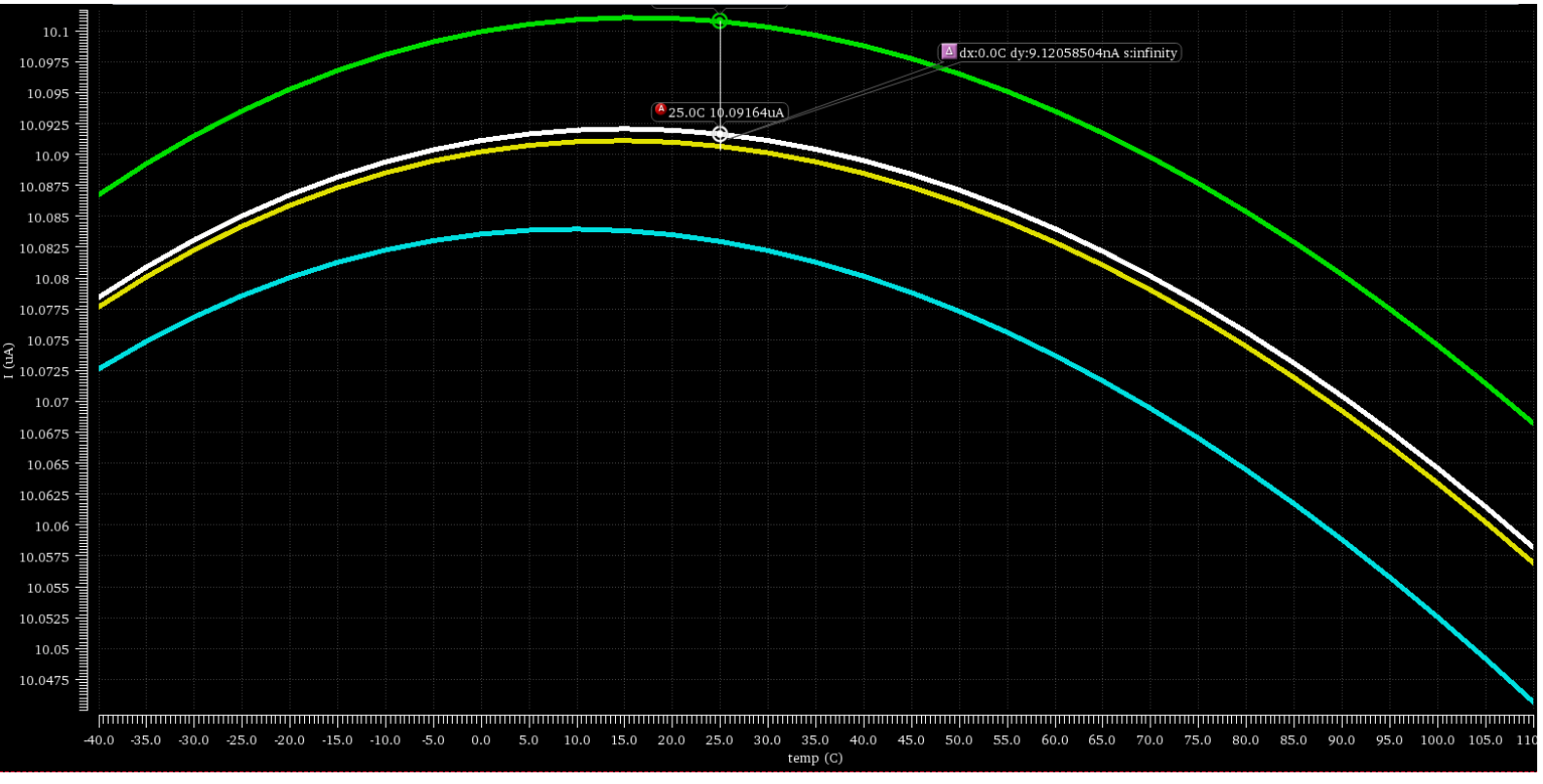


Figure 38: I_{ref} as function of temperature. Blue: new version's layout extraction, yellow: schematic without parasitic, white : schematic with parasitics and green : old version's layout extraction

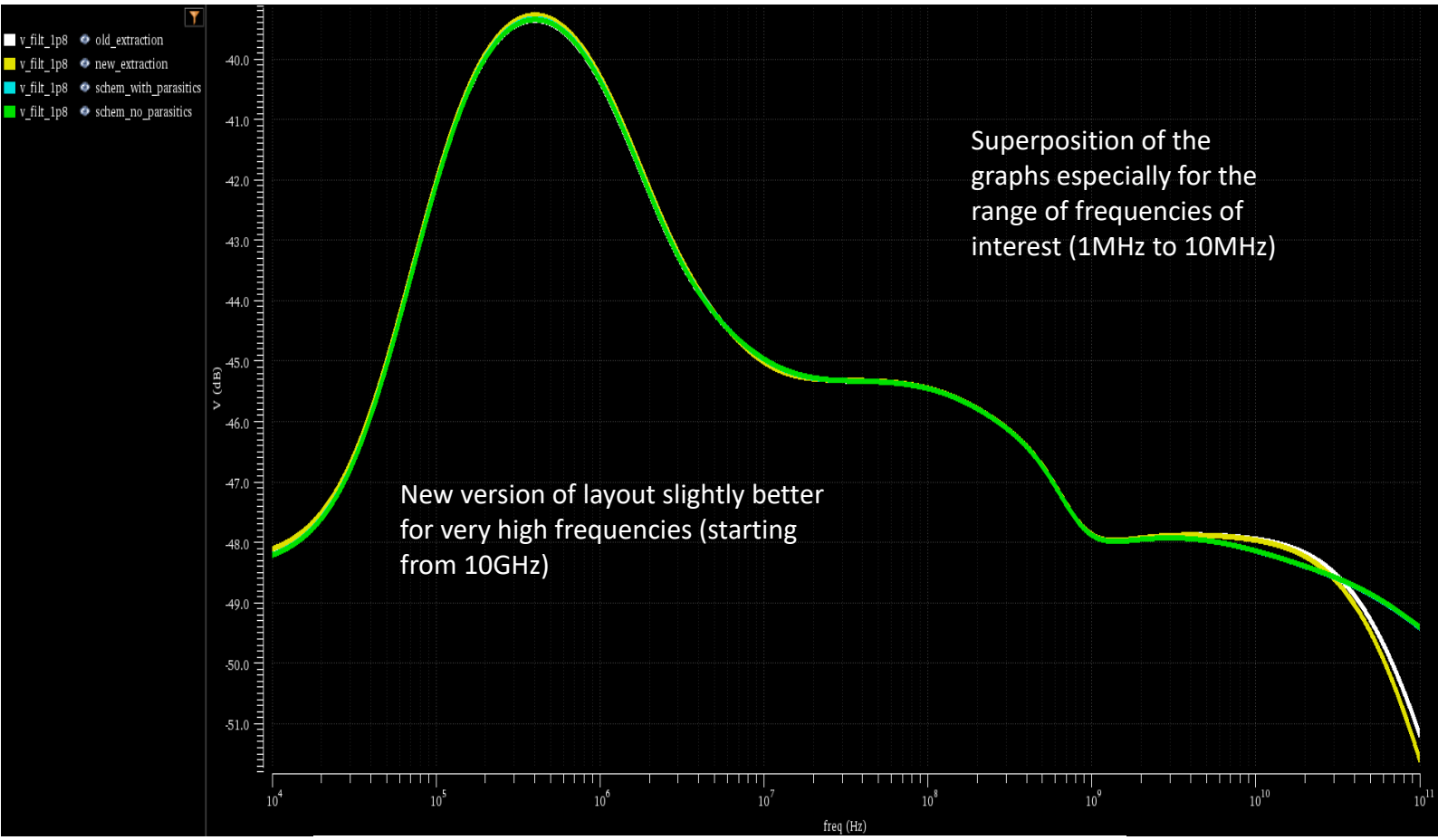


Figure 39: PSRR results for post layout extraction and schematic

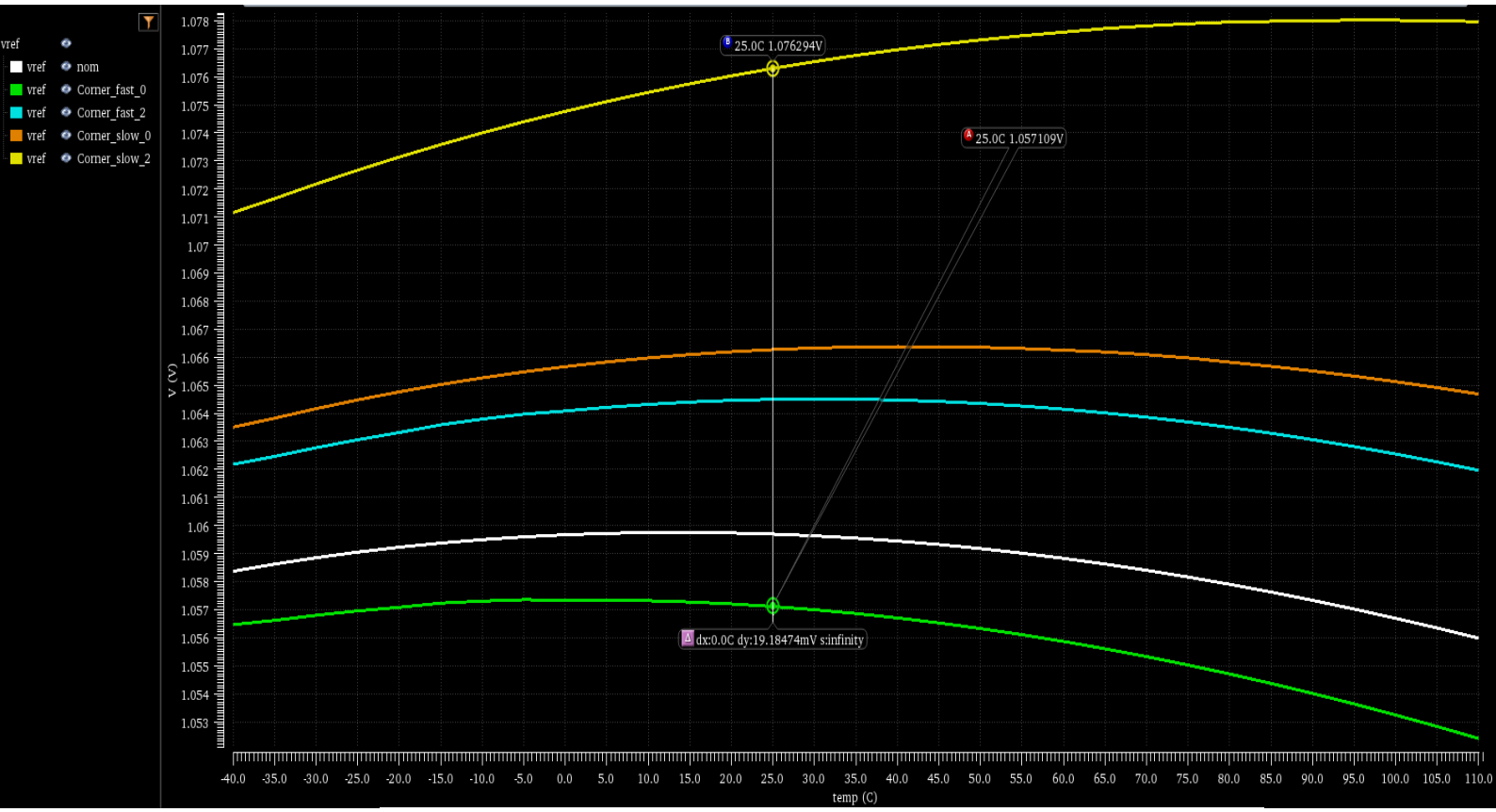


Figure 40: V_{ref} curves in schematic without parasitics in PVT

6.6 – Stability of the current generator amplifiers:

We reported in Figure 26, the generation of the current in the bandgap for which we used an amplifier for impedance isolation. The use of a two-stages amplifier ensures a high gain for the copy of the non-inverting input to the inverting input and isolates the load resistance from the output resistance of the amplifier, it is also designed this way to use the load of the second stage as a master branch current mirror. As two-stages amplifiers suffer from stability issues, we use a Miller compensation RC circuit to ensure stability.

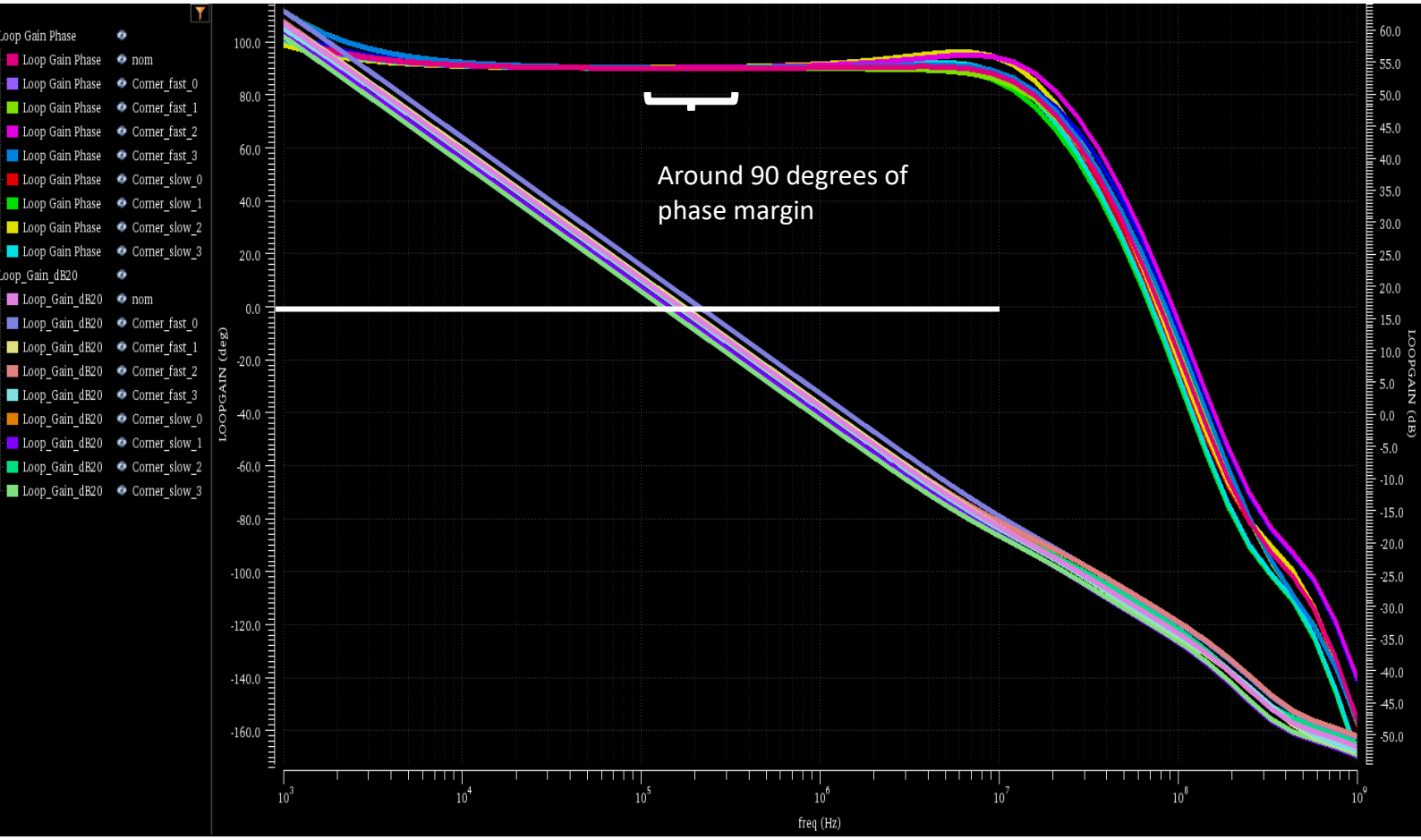


Figure 41: Gain and phase curves in PVT for stability check

In Figure 41, we see that the amplifier used for current generation is stable enough and robust. It has a phase margin of 90 degrees ensuring a good stability.

We also checked stability by injecting a step of current of different amplitudes to the feedback loop. We injected 1µA, 10µA and 50µA step of current. For a stable system, we expect the output voltage to recover its initial value quickly and without oscillations. On the opposite side, an unstable system may vary depending on the phase margin, the lower is the phase margin, the higher in amplitude will be the oscillations and the longer will be the time needed to recover the initial value of the output, for a phase margin close to zero, the system may diverge with oscillations without having the output recovering its value. In our case as shown in Figure 41, we have a phase margin: PM = 180- φ(0dB gain) = 90 degrees, which is optimal. As reported in Figure 43, we see that the output recovers its initial value without oscillations in approximatively 1µs.

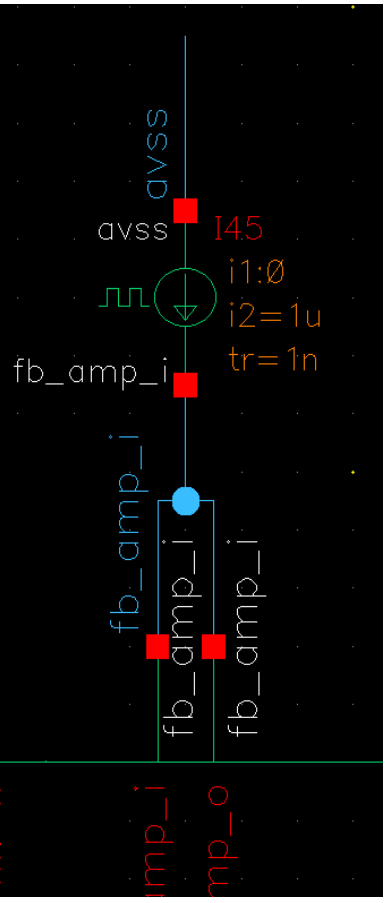


Figure 42: Configuration used for pulse injection

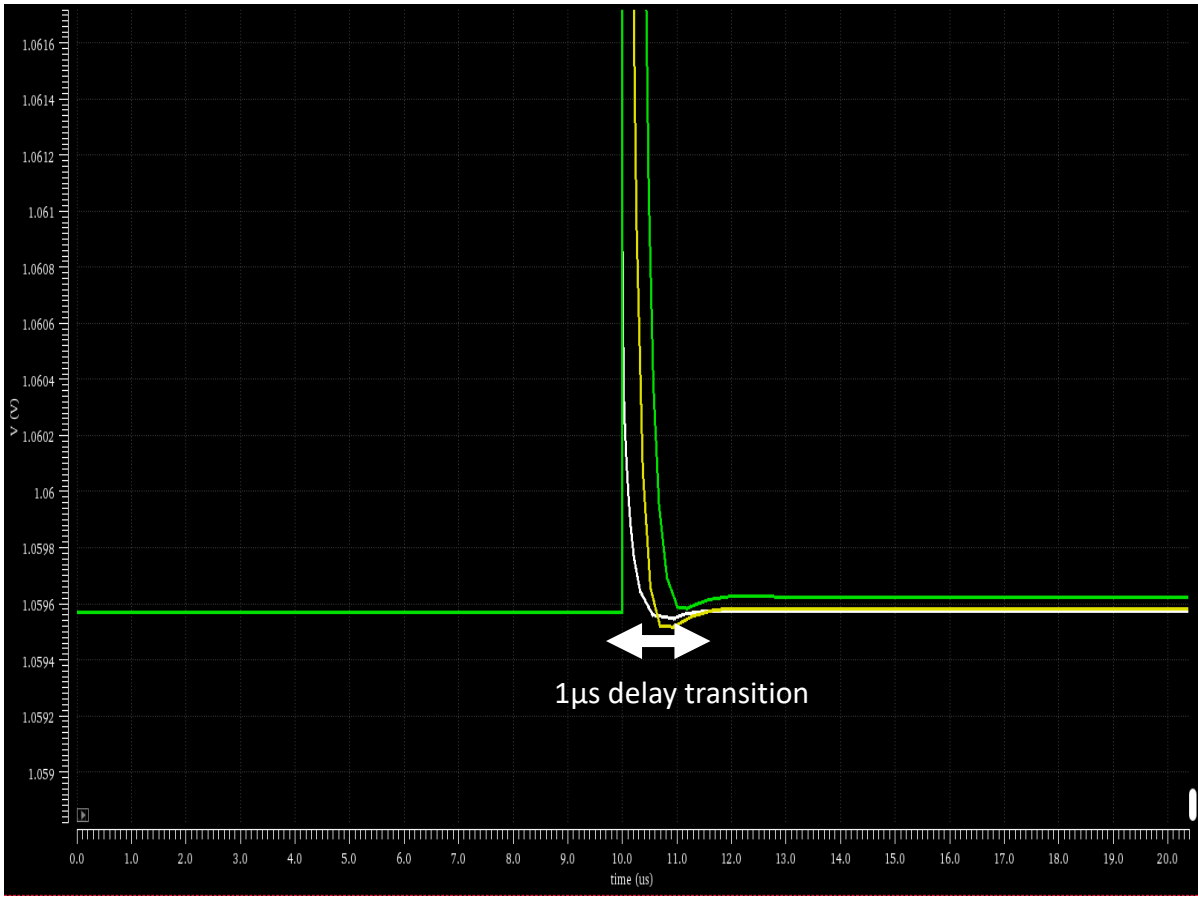


Figure 43: pulse injection for stability check results. White: 1µA pulse, yellow : 10µA pulse and green : 50µA pulse.

7.Voltage to current converter:

7.1. Introduction:

The clock and data recovery circuit designed in this project aims to receive a signal, reshape it after losses in the medium and then transmit it. In the transmission process, we use a laser that upon an electrical excitation, we get an optical response, in our project we chose a type of laser called the VCSEL laser (Vertical-Cavity Surface-Emitting Laser) and it has to be biased with the proper current for it to work in an optimal way. We call laser driver, the electrical circuit that will give this optimal current for the laser, ideally it is a constant current source with minimum noise.

A voltage to current converter circuit (V2I) is a circuit designed in order to convert an input voltage into an output current in linear way. In our project the voltage to current converter will be used to measure the input resistance of the VCSEL, as shown in figure 50, the VCSEL is modelled by its input resistance plus an ideal voltage source V_{th}. After generating defined currents by the VCSEL driver, we can solve the problem with two equations of two unknowns.

$$V_{VCSEL1} = R_{in}I_{VCSEL1} + V_{th}$$
$$V_{VCSEL2} = R_{in}I_{VCSEL2} + V_{th}$$

The current generated by the V2I will be injected to an Analog to digital converter (ADC), converting it into a digital output that will be treated to extract the value of the input resistance of the VCSEL.

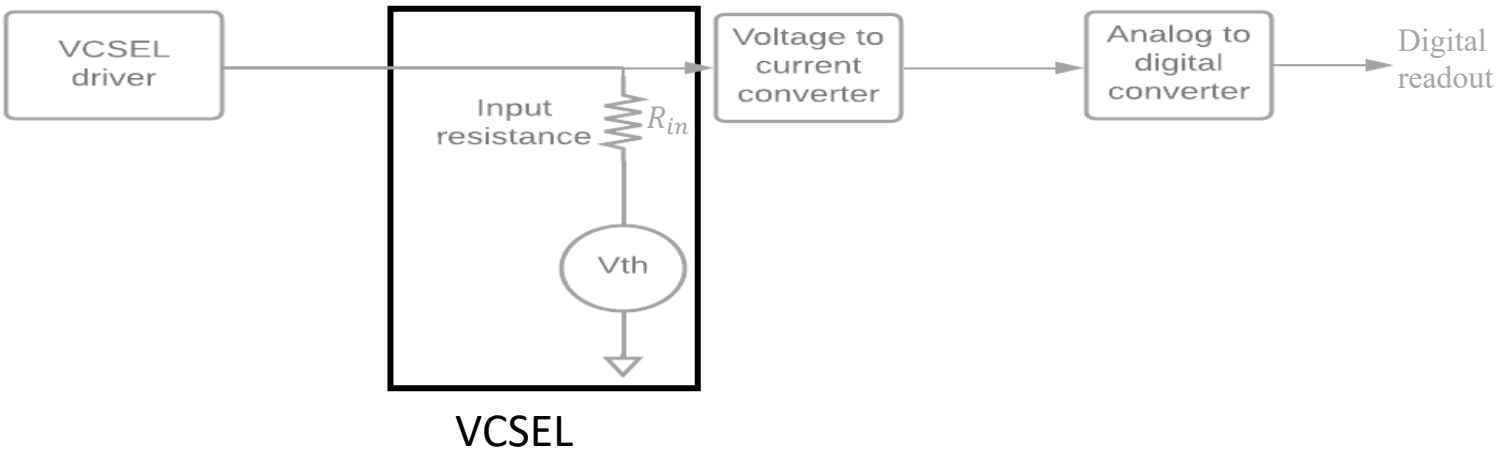


Figure 44: Block diagram of the use of the Voltage to current

7.2. Specifications:

The variable	Minimum	Typical	Maximum
Gain variation	-	-	5%
Output current	0µA (at 1,5V)	-	200µA(at 2,5V)
Output current at 1,5V(normalized to the input current)	0	-	0,5
Output current at 2,5V(normalized to the input current)	9,5	10	10,5

Main target

Table 10: Specifications of the V2I

The specifications in the output current were normalized to the input biasing current, so that the comparison is also performed with respect to this input current as it varies also in PVT. Further details will be given in section 7.4.

7.3. Suggested structures:

As this circuit was designed from scratch, we have discussed at the beginning several other structures, we displayed two of them in the annex 9.6.

The first structure to be proposed in annex 9.6.1 is the amplifier-current generator, used in the bandgap section, as this structure generates a current perfectly linear: $I_{out} = \frac{V_{in}}{R}$. This structure doesn't fit the needs of our implementation, as we have specifications to get an output current of 0µA when $V_{in} = 1.5V$ and a current of 200µA when $V_{in} = 2.5V$, we will not be able to nullify the current when the input voltage is at 1.5V. We can eventually have add a sink offset to nullify it, but solving the equations, this offset is about 300µA and that increases significantly the power consumption.

The second structure discussed in the annex 9.6.2 for the V2I, makes benefit of the mixing of currents one from a transistor in saturation and the other from a transistor in triode. The final result is a linear law of the output current with the input voltage. The main advantage is that we don't have anymore a resistance that are in general bulky and takes most area in a circuit. The main disadvantage making us discarding this structure, is its squared dependency with respect to the threshold voltage. The latter varies too much in PVT, therefore squaring it, will make the performances of our circuit vary too much in PVT and we wouldn't be able to meet the specifications.

The structure we decided to go for, is a source-degenerated differential pair (Figure 45): it is a differential pair for which we added a resistance at the source, the higher this resistance the more linear the circuit will be.

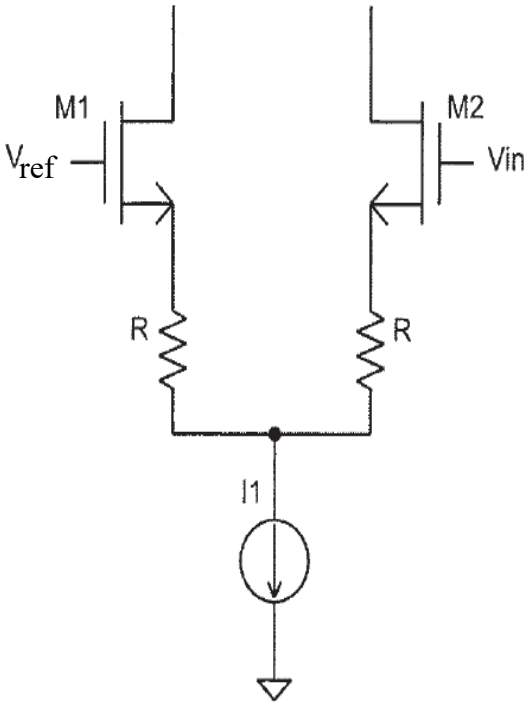


Figure 45 : source degenerated differential pair

As the specifications is to have 0µA when $V_{in} = 1.5V$ and a current of 200µA when $V_{in} = 2.5V$. We therefore compare the input voltage to a $V_{ref} = 2V$ so that we make the middle of the comparison (equal currents) at 2V of the input voltage. The current flowing through the transistor M2 is then copied to an output branch. The small signal analysis of the M2-branch gives:

$$\frac{i_{out}}{v_{in}} = \frac{g_m}{1+g_m \times R} \approx \frac{1}{R} \text{ for } g_m \times R >> 1$$

Therefore, the higher is R, the better will be the linearity as we will get higher $g_m \times R$. The drawback of this structure is the input swing as we have to take into account a voltage drop across the resistance R, but in the real implementation we've made sure to have all the transistors saturated.

The choice of an NMOS differential pair instead of a PMOS as shown in Annex 9.6.3 that we initially started with, was mainly motivated by the fact that the load of the differential pair is a cascoded current mirror for a better copy of the current, therefore when the PMOS transistors will be passing we'll be getting net010 and net013 in annex 9.6.3 at high voltages and so it would be more difficult to saturate the current mirrors.

7.4. Implementation of the structure:

In Figure 46, we show the implementation with an NMOS differential pair used. Here we don't have an issue of PMOS transistors passing high voltages, on the contrary it will help saturating the transistors of the Differential pair.

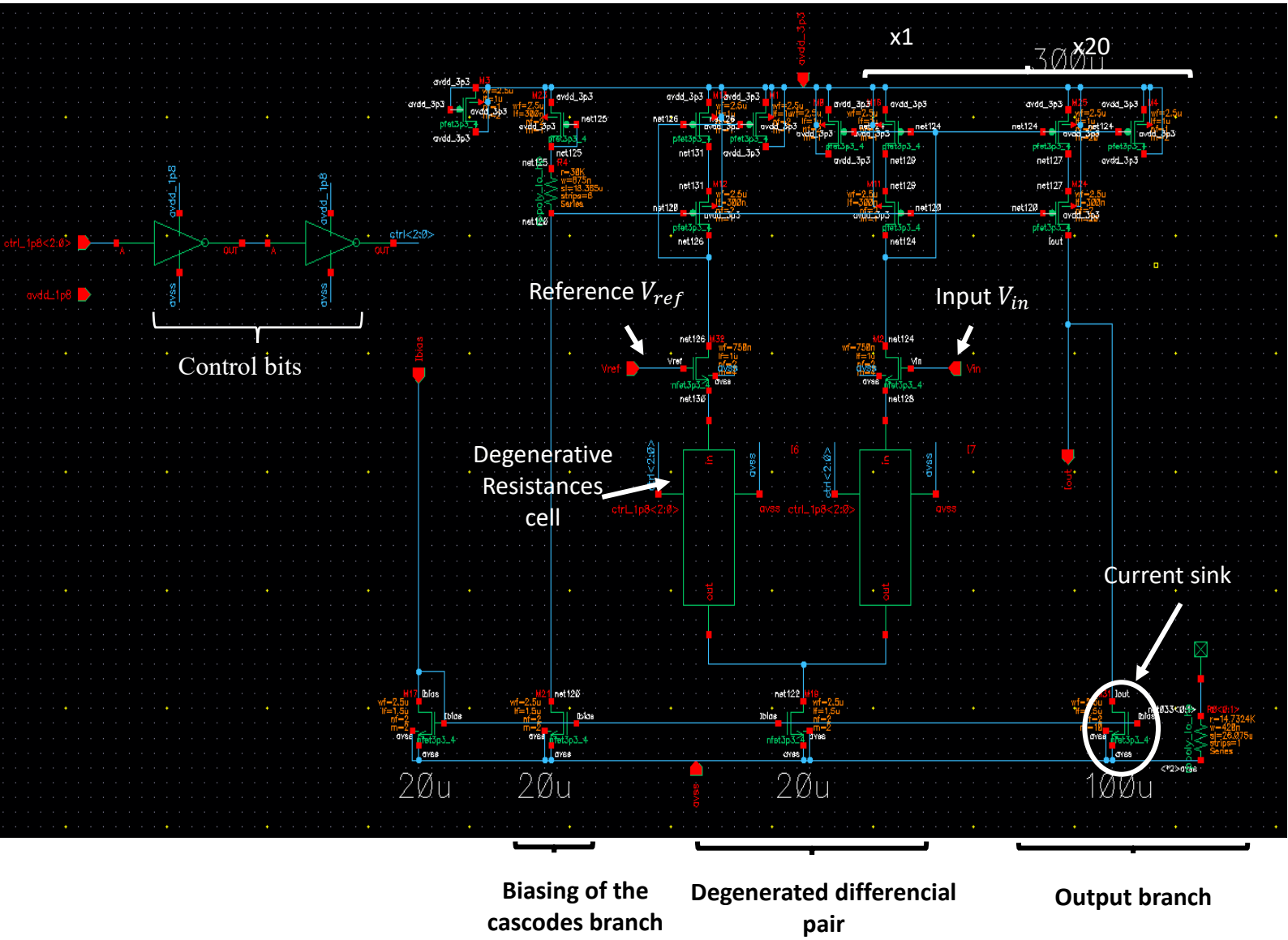


Figure 46: Implemented version of the V2I

The working of this circuit especially with the given specifications as we will see later depends highly on the value of the degenerative resistance, for this reason, it is highly recommended to have some debug solutions in case after the fabrication of the circuit in the lab, we need to vary the resistance. The control bits are injected to NMOS transistor switches used to tune the value of the degenerative resistance as shown in Figure 47. The resistance we'll be using during all the simulation is the 33kΩ+3.2kΩ = 36.2kΩ, and so a standard **code of 001**. Due to layout limitations, we couldn't afford more debug resistances. In Figure 48, we show the general behaviour of the circuit with without and with 5kΩ and 10kΩ degenerative resistances. We can see that the higher is the resistance the lower will be the gain and so a **greater range of linearity**, we therefore decided to increase the degenerative resistance to 36.2kΩ in order to be linear in the range of interest which is [1.5V 2.5V], this decision implies a non-zero current at 1.5V. To solve this problem, we use a current sink in Figure 46 to remove this offset.

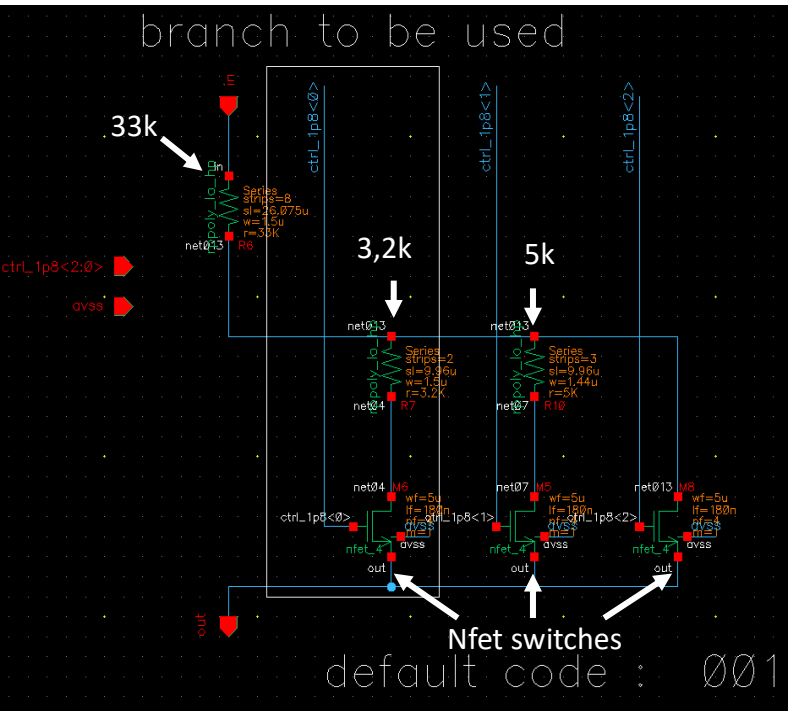


Figure 47: Degenerative resistances cell

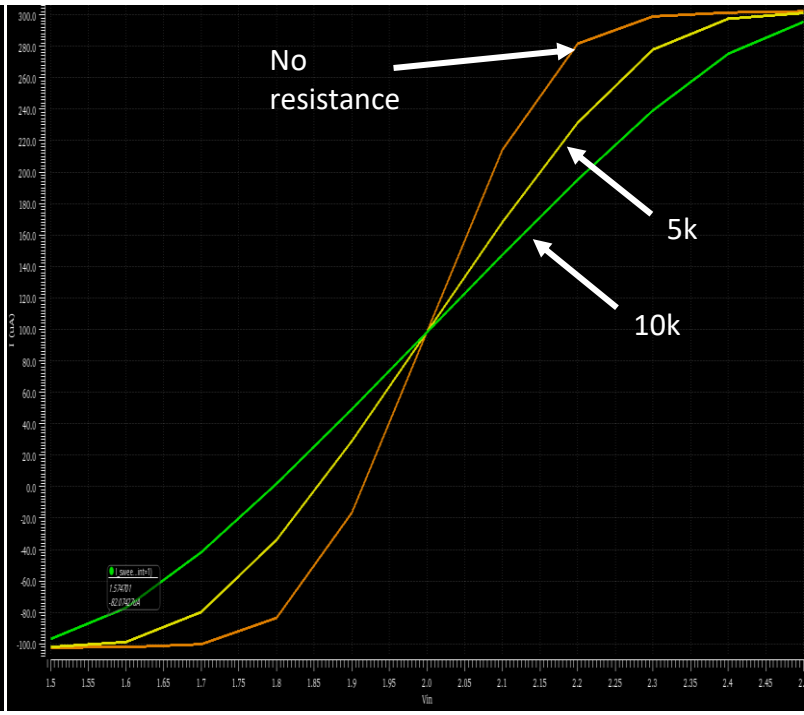


Figure 48: Output current vs resistance

Final parameters:

- *Input current, cascode biasing current and tail current: 20µA*
- *Degenerative resistance: 36,2kΩ*
- *Vin branch current at 1,5V: 5µA (copied 20 times to the output branch leading to 100µA)*
- *Vin branch current at 2,5V: 15µA (copied 20 times to the output branch leading to 300µA)*
- *Current sink: 100µA (to remove the offset of 5µA copied 20 times current generated at $V_{in} = 1.5V$)*

7.5. Performances:

In figure 49, we show the performances of the V2I in nominal, in particular, we see a 5.44µA current at 1.5V. Normalizing the latter to the input current 20µA, we get a ratio of 0.272 that respects the specifications in section 7.2 of a maximum ratio of 0.5. The same approach can be done to verify the specifications at a voltage of 2.5V.

We performed an AC simulation to calculate the DC gain, and plotted the variation of the gain knowing that it is the **derivative of the output current** with respect to the input voltage. **The gain variation** is calculated in percent, and we have as a specification that this variation should be **less than 5%.** We compute the gain variation using the following formula:

$$\textbf{Gain variation} = \frac{Max,deriv,I_{out} - Min,deriv,I_{out}}{DC\ gain}$$

We have a tradeoff between the gain variation and the output current:

High degenerative resistance → lower gain and mild variation of the gain → less gain variation, increase of output current at 1,5V and decrease of the output current at 2,5V.

The performances in PVT are summarized in Table 11, only fail the cross-corners fast_res_slow_mos where the resistances are configured on FAST and the MOS transistors are configured on slow (refer to annex 9.1 for the parameters of these corners). **For this configuration,** the value of the resistance is too high, making the gain very low that we have too much current at 1.5V output and low current at 2.5V. When confronted to this situation, we'll have to lower the resistance, and for that, we will use the code 100 that will discard the resistance 3.2kΩ and replace is by a wire (please refer to Figure 47).

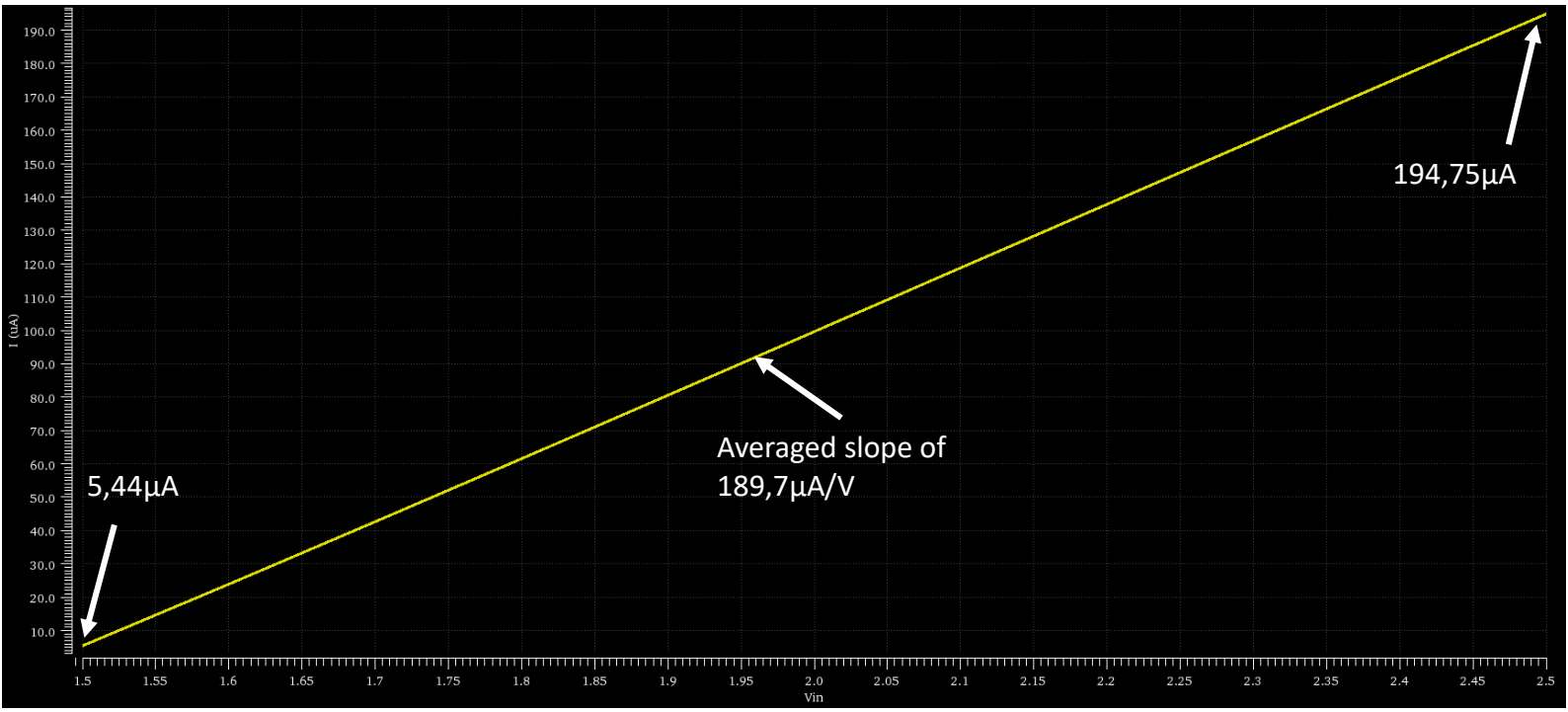


Figure 49: Output current vs V_{in}

Output	Nominal	Spec	Corner_fast_0	Corner_fast_1	Corner_fast_2	Corner_fast_3	Corner_slow_0	Corner_slow_1	Corner_slow_2	Corner_slow_3
gain_variation_p...	3.409	< 5	3.677	3.259	3.712	3.299	3.631	3.167	3.668	3.24
current_1.5_dc	272.5m	range -0.5 0.5	83.56m	434.9m	84.78m	436.1m	151.1m	496.2m	152.2m	497.2m
current_2.5_dc	9.754	range 9.5 10.5	9.942	9.668	9.949	9.679	9.779	9.524	9.786	9.535

ner_slowres_fastm(	ner_slowres_fastm(	ner_slowres_fastm(	ner_slowres_fastm(	orner_fastres_slowmos	ner_fastres_slowm	ner_fastres_slowm	ner_fastres_slowm
4.287	4.353	4.314	3.91	2.821	2.349	2.876	2.486
12.61m	360.7m	13.44m	361.4m	447.9m	777.1m	448.8m	777.9m
9.994	9.694	10	9.708	9.449	9.205	9.458	9.217

Table 11: Performances in PVT

The results of the simulation after lowering the resistance (use of the code 100) for the fast_res_slow_mos corners are reported in Table 12.

Output	Spec	eig	s/I	Mir	Ma	ner_fastres_slowmo	ner_fastres_slowmo	ner_fastres_slowmo	ner_fastres_slowmo
Filter	Filter	Filt	Fil	Fil	Fil	Filter	Filter	Filter	Filter
gain_variation_p...	< 5					3.666	3.085	3.711	3.147
current_1.5_dc	range -0.5 0.5					110.9m	477.6m	111.6m	478.2m
current_2.5_dc	range 9.5 10.5					9.814	9.524	9.823	9.538

Table 12: Results of the slow_res_fast_mos corners with the code 100

7.6. Layout:

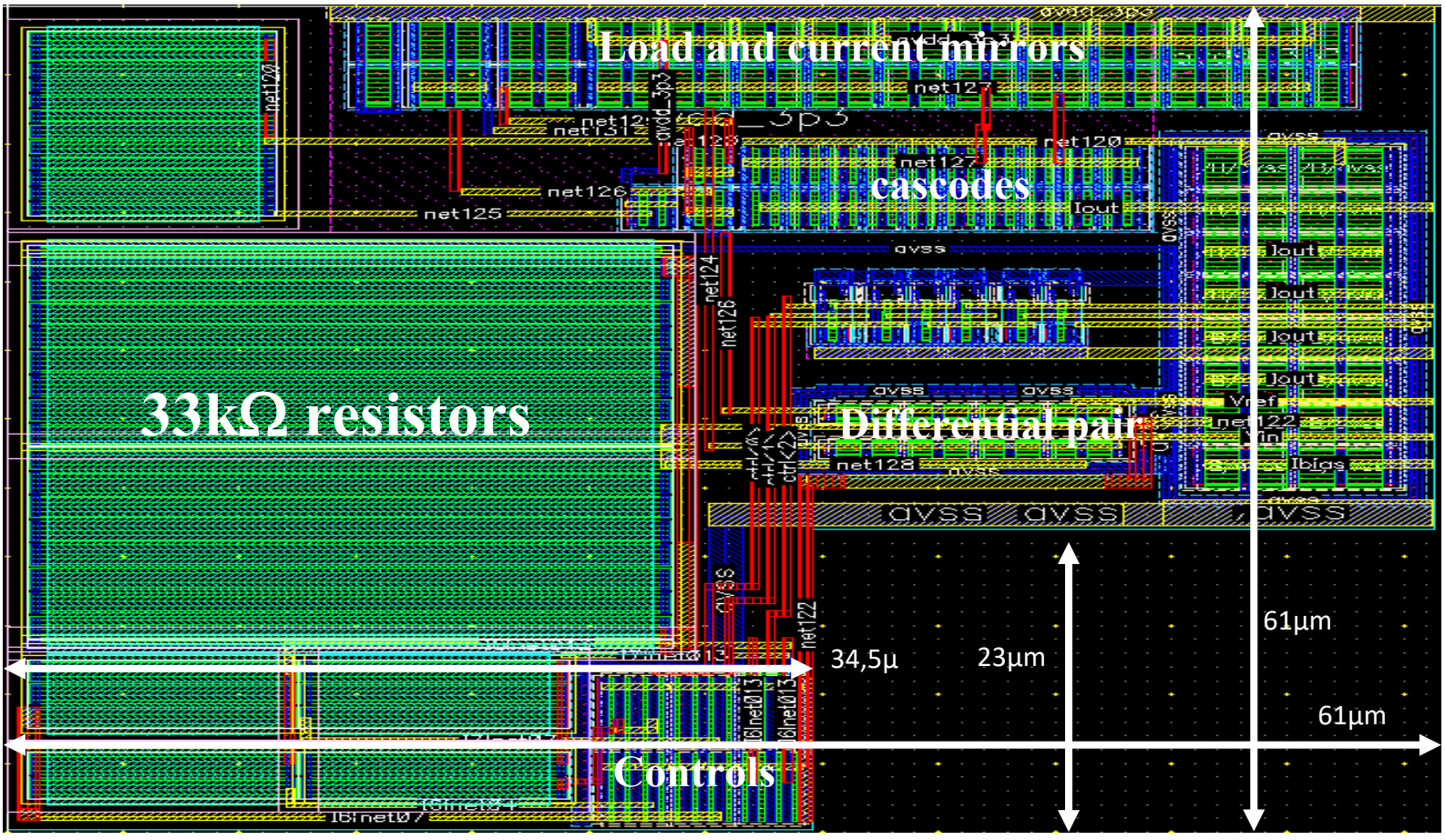


Figure 50: Layout of the V2I

The shape of the overall layout was specified by the top level, a square of 61µm x 61µm with rectangular hole of 26.5µm x 23µm.The layout of the V2I was performed taking into account similar considerations as for section 6.4.2. The resistances of 33kΩ being very important, were designed and laid out

with a high width (therefore a higher length) to limit its variations in PVT, and we also tried to make the widths of the connections as large as possible with a high number of vias to reduce the parasitic resistances.

We report in Table 13 the results of the post-extraction simulation, we have a slight violation of the specifications but acceptable at the corners slow1 and slow3. The final power consumption of the circuit was of 0.99mW in the best case and 1.393mW in the worst case.

Output	Nominal	Spec	Corner_fast_0	Corner_fast_1	Corner_fast_2	Corner_fast_3	Corner_slow_0	Corner_slow_1	Corner_slow_2	Corner_slow_3
gain_variation_p...	3.381	< 5	3.635	3.235	3.671	3.271	3.602	3.138	3.639	3.2
current_1.5_dc	278.3m	range -0.5 0.5	90.32m	441.1m	91.56m	442.4m	156.5m	501.1m	157.6m	502.1m
current_2.5_dc	9.757	range 9.5 10.5	9.946	9.671	9.954	9.682	9.782	9.525	9.789	9.536
			ner_slowres_fastm	ner_slowres_fastm	ner_slowres_fastm	ner_slowres_fastm	rner_fastres_slowmos	ner_fastres_slowm	ner_fastres_slowm	ner_fastres_slowm
			4.181	4.374	4.211	3.93	2.79	2.322	2.847	2.456
			17.23m	365.6m	18.09m	366.3m	453.9m	782.6m	454.9m	783.4m
			9.997	9.695	10.01	9.71	9.453	9.207	9.461	9.22

Table 13: Post extraction results of the V2I

8. Other layouts:

During this project, other top-level layouts were asked to be done. We performed the layout of some sub-cells of a Transimpedance Amplifier (TIA). The general succinct idea of a transimpedance amplifier is a circuit that converts current into a voltage, it is in this project placed subsequently to a photodiode that converts optical signal into a current, to get an output voltage.

The laid out sub-cells of the TIA were a bandgap reference circuits slightly similar to the one discussed in section 6 and a level-shifter circuit that converts supply voltage from 1.8V to 3.3V.

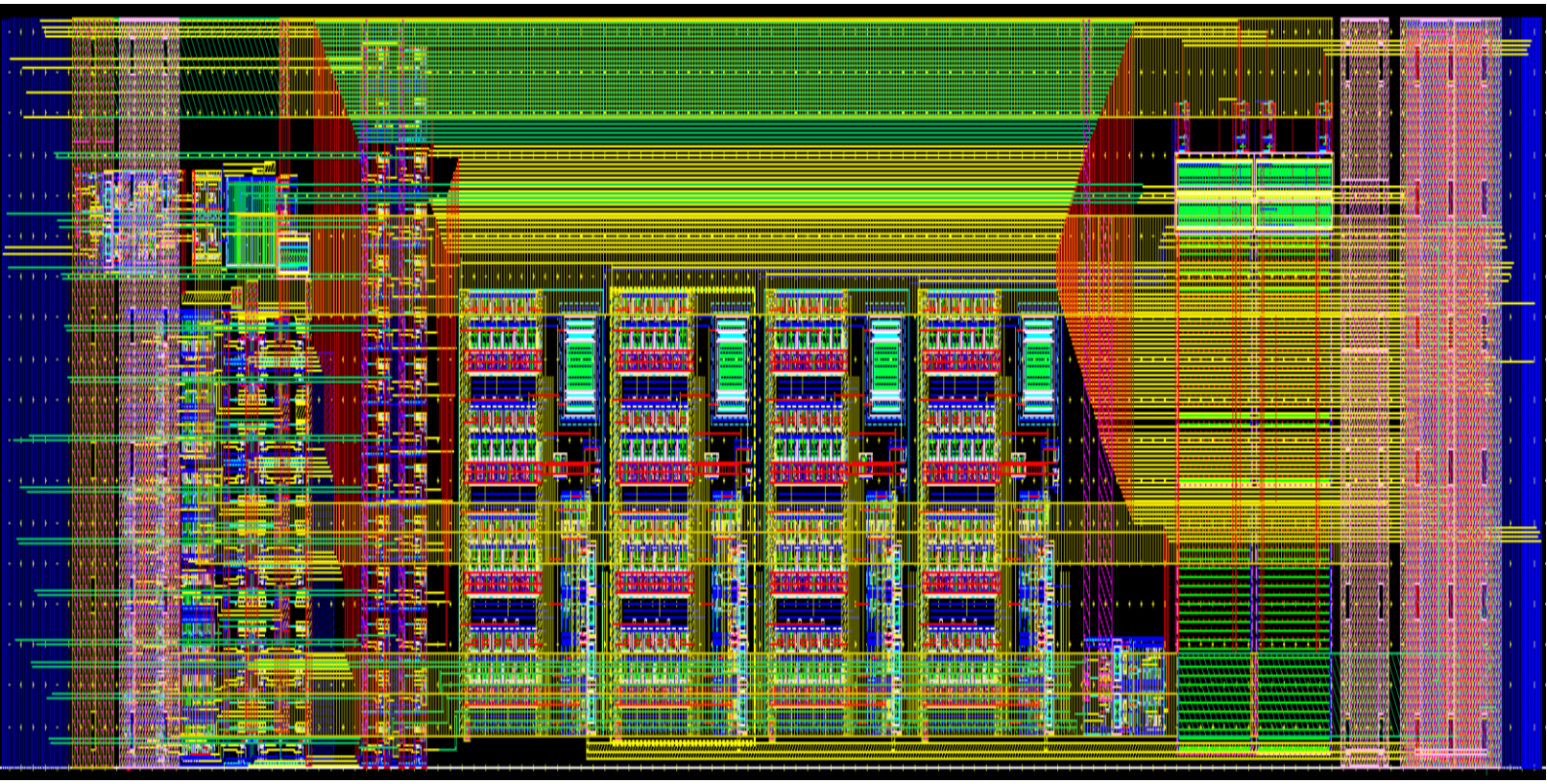


Figure 51: Layout of the level shifter

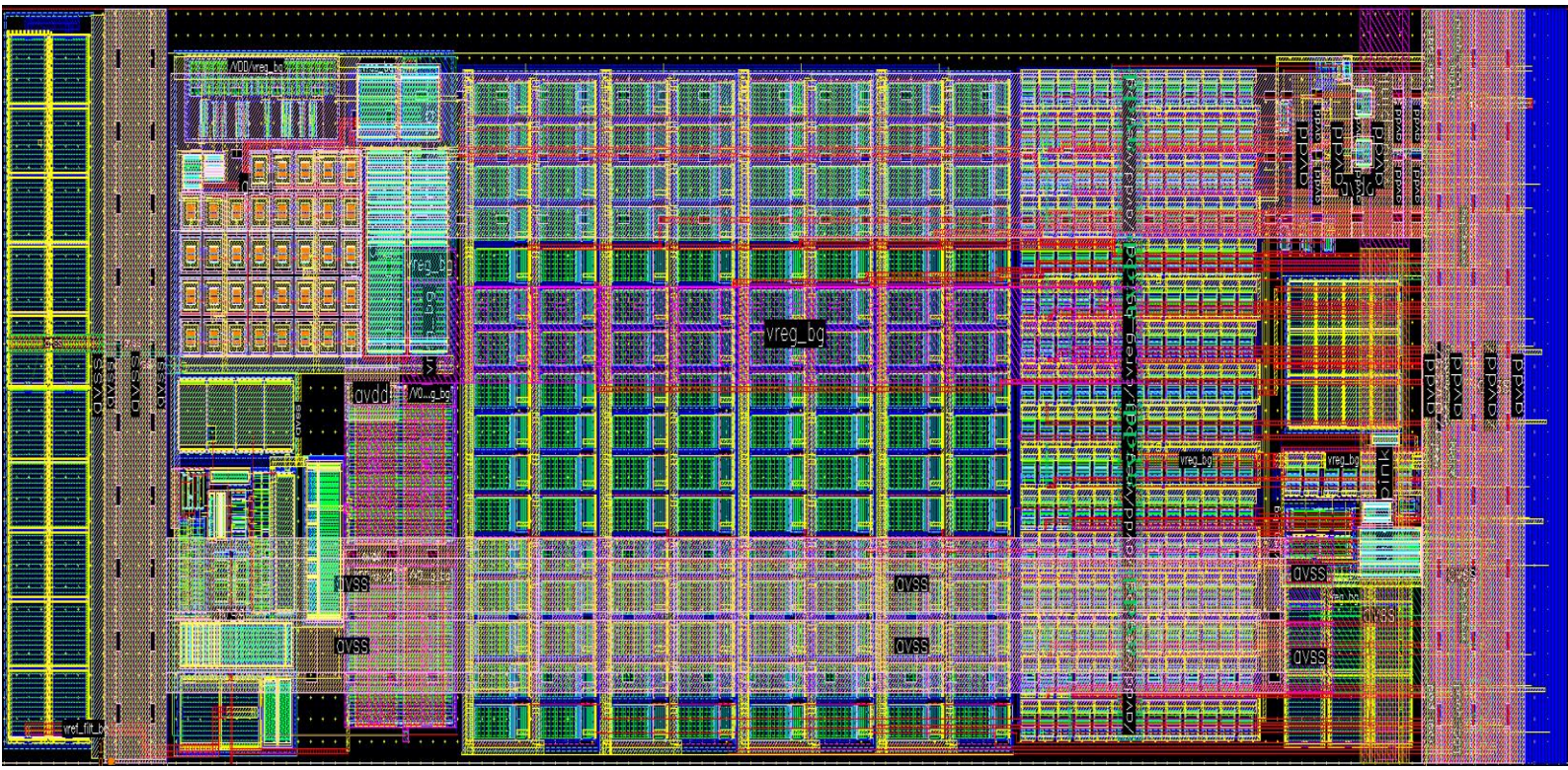


Figure 52: Top Layout of the bandgap of the TIA

The layouts presented in Figure 51 and Figure 52 were performed from scratch, we had some directives about the critical nodes in terms of parasitic resistance. As the level-shifter and the bandgap are DC circuits, we didn't have to take into account parasitic capacitances, even during the parasitic extraction by the simulator. Concerning the top bandgap of the TIA, it has similar components as the one presented in section 6, it has similar bandgap cell and amplifiers current generators, the only difference is the number of current mirror cells used to generate the needed current.

9.Annex:

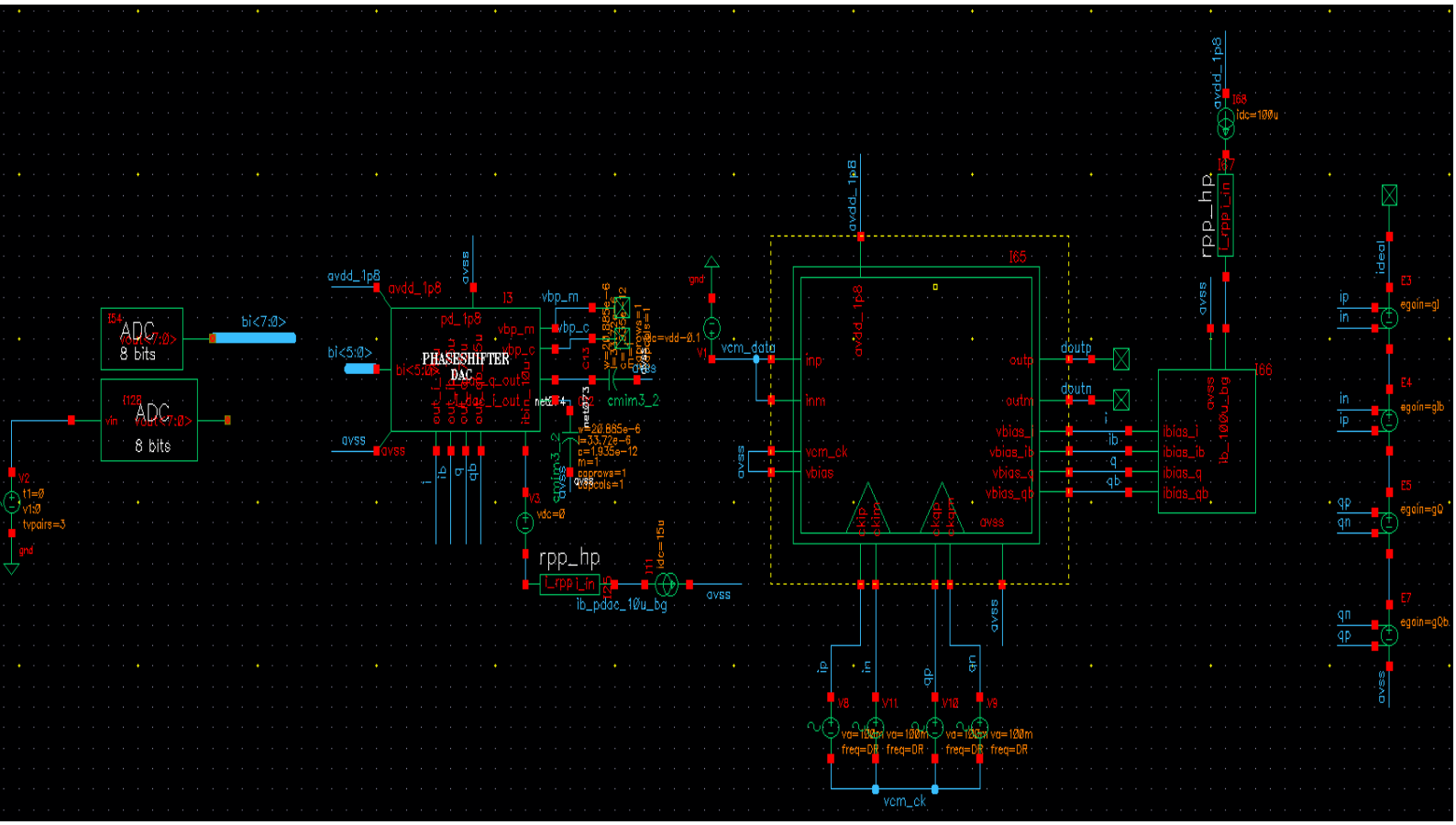
9.1-: Corners configuration

Parameter	Nominal	Corner_fast_0	Corner_fast_1	Corner_fast_2	Corner_fast_3	Corner_slow_0	Corner_slow_1	Corner_slow_2	Corner_slow_3
statistics.scs	params	params	params	params	params	params	params	params	params
diode_mod.scs	SS	SS	SS	SS	SS	SS	SS	SS	SS
cap.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
global.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
hppnp.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
hpvar.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
ind.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
mis.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
n1p8.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
n3p3_5p0.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
npn.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
p1p8.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
p3p3_5p0.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
rnw.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
rtin.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
npn_rth.scs	RTH	NO_RTH	NO_RTH	NO_RTH	NO_RTH	NO_RTH	NO_RTH	NO_RTH	NO_RTH
warnings.scs	NO	NO	NO	NO	NO	NO	NO	NO	NO
hvres.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
lvres.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
salres.scs	NOM	FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
sub.scs	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
circuit.scs	CIRCUIT	CIRCUIT	CIRCUIT	CIRCUIT	CIRCUIT	CIRCUIT	CIRCUIT	CIRCUIT	CIRCUIT
fet.scs	BSIM	BSIM	BSIM	BSIM	BSIM	BSIM	BSIM	BSIM	BSIM
vdd	3.3	3.14	3.14	3.46	3.46	3.14	3.14	3.46	3.46
temperature	27	-40	110	-40	110	-40	110	-40	110

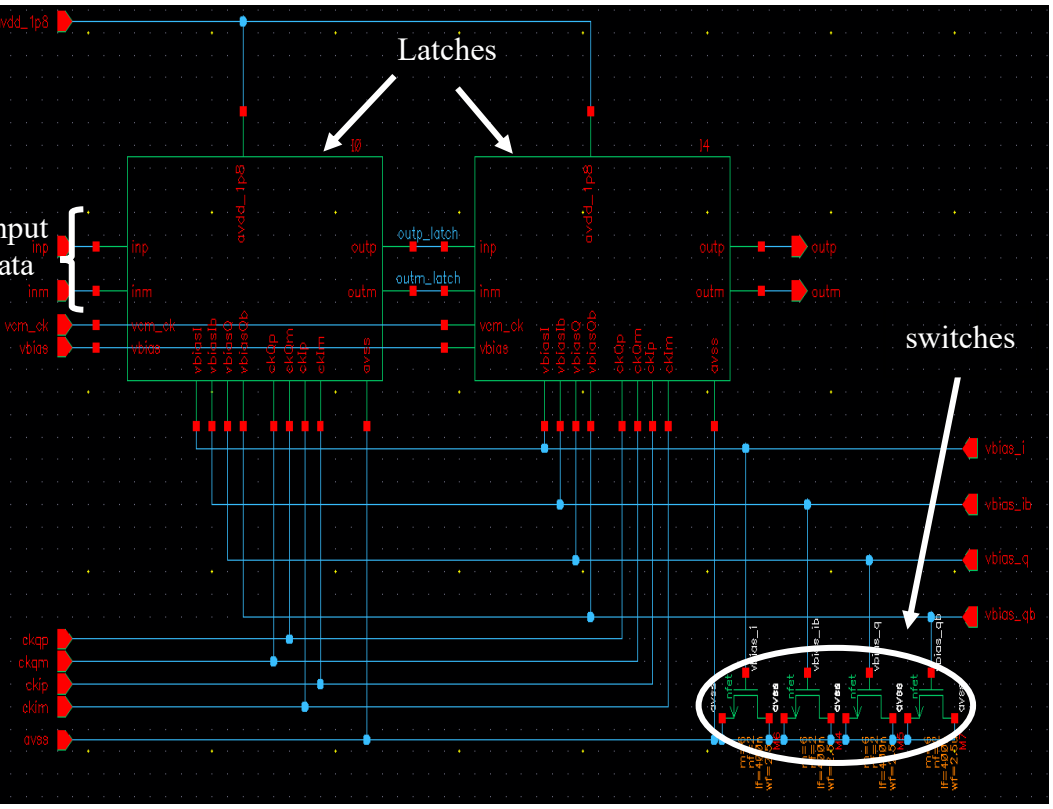
Corner_slowres_fastmos_0	Corner_slowres_fastmos_1	Corner_slowres_fastmos_2	Corner_slowres_fastmos_3	Corner_fastres_slowmos_0	Corner_fastres_slowmos_1	Corner_fastres_slowmos_2	Corner_fastres_slowmos_3
params	params	params	params	params	params	params	params
SS	SS	SS	SS	SS	SS	SS	SS
SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW
SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW
SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW
SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW
SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW
SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW
SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW
FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW
SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW
FAST	FAST	FAST	FAST	SLOW	SLOW	SLOW	SLOW
SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW
SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW	SLOW
NO_RTH	NO_RTH	NO_RTH	NO_RTH	NO_RTH	NO_RTH	NO_RTH	NO_RTH
NO	NO	NO	NO	NO	NO	NO	NO
SLOW	SLOW	SLOW	SLOW	FAST	FAST	FAST	FAST
SLOW	SLOW	SLOW	SLOW	FAST	FAST	FAST	FAST
SLOW	SLOW	SLOW	SLOW	FAST	FAST	FAST	FAST
DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
CIRCUIT	CIRCUIT	CIRCUIT	CIRCUIT	CIRCUIT	CIRCUIT	CIRCUIT	CIRCUIT
BSIM	BSIM	BSIM	BSIM	BSIM	BSIM	BSIM	BSIM
3.14	3.14	3.46	3.46	3.14	3.14	3.46	3.46
-40	110	-40	110	-40	110	-40	110

Configuration of the corners used

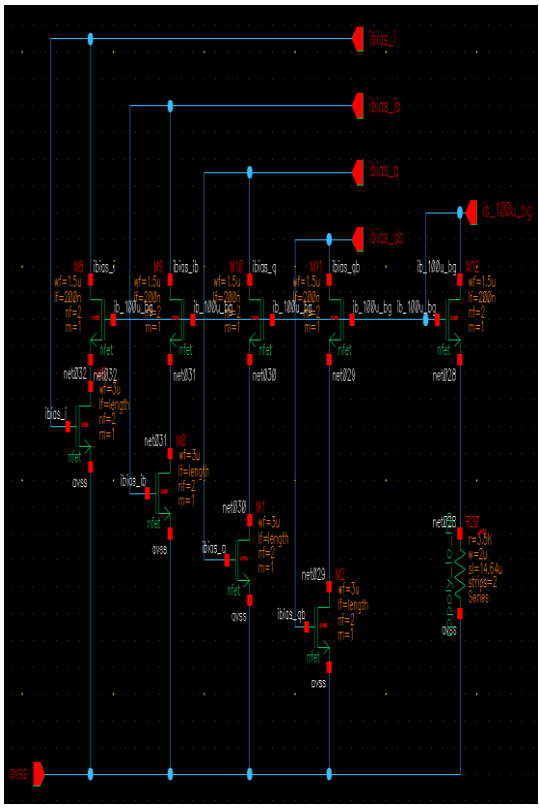
9.2-: FlipFlop + phase interpolator annex:



Testbench of the section 5

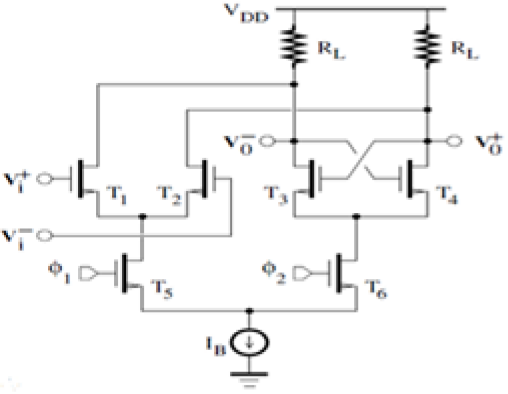


Flipflop structure

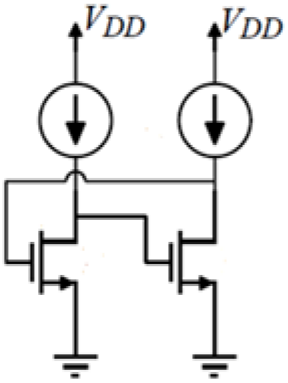


Biasing current mirror

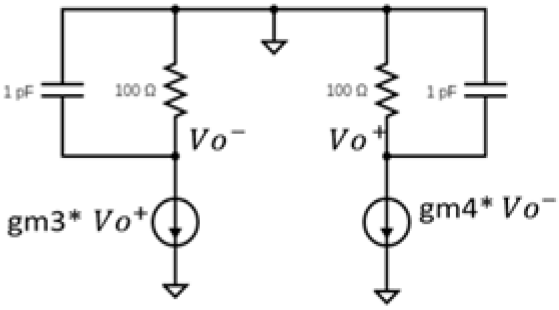
9.3-: Analog latch theory



Example of an NMOS latch



Simplified schematic of an NMOS latch



Small signal analysis of an NMOS latch

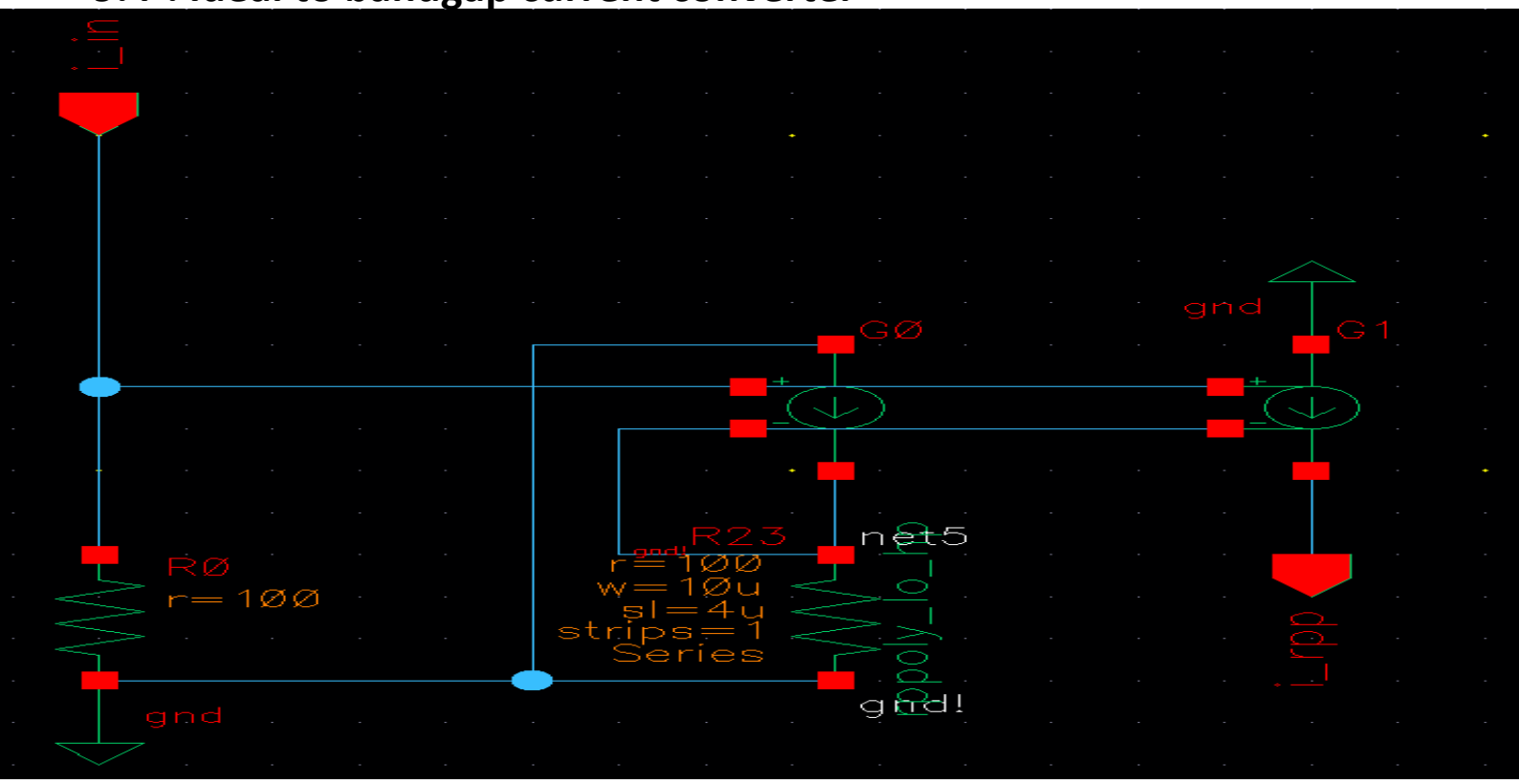
Analog latch schematic

When Φ1 is high, Φ2 is low and only the differential pair is activated and it computes the outputs voltages
When Φ2 is high, Φ1 is low and only the latch is activated, the drain parasitic capacitances of the transistors hold the last value of the output voltages and then the positive feedback is activated forcing one output to high level and the other to the low level

Using the small signal analysis get the following equations: $\frac{Vo^+}{R} + Vo^+sC + Vo^-g_{m34} = 0$ and $\frac{Vo^-}{R} + Vo^-sC + Vo^+g_{m34} = 0$

We define $V_d = Vo^+ - Vo^-$ we get V_dsC+ $(g_{m34} - \frac{1}{R})V_d$=0 leading to $V_d(t) = V_d(0)\exp(\frac{g_{m34} - \frac{1}{R}}{C} t)$.
The advantage of this structure is we get an exponential time-dependant expression of the gain equal to $\frac{V_d(t)}{V_d(0)} = \exp(\frac{g_{m34} - \frac{1}{R}}{C} t)$, the more we wait the greater is the gain until it saturates.
The speed of the latch depends on the factor $g_{m34} - \frac{1}{R}$ that should be positive, in general we choose g_{m34}R>>1
We can also increase Vd(0) to saturate quickly, in general Vd(0) is referred as *the sensitivity of the latch*, the higher Vd(0) the quicker we'll be "splitting" the output values, but this solution is in general not considered because to have it we should increase the sizes of T1 and T2 (to increase the gain and so $g_{m1,2}$), therefore we'll be having more parasitic capacitance affecting the speed of the circuit.

9.4-: Ideal to bandgap current converter



Ideal to bandgap current converter

The above cell allows conversion from of ideal current entering *i_in* input to a bandgap-like current outputted at *i_rpp*. Current outputted by a bandgap as discussed in section 6 can be formulated by: $I_{bg} = \frac{PVT\ independant\ voltage}{R_{poly}}$.

The cells G0 and G1 are voltage controlled current sources, those are ideal components converting voltage to a current with a gain. Here the gain has been chosen to be 10^4Siemens.

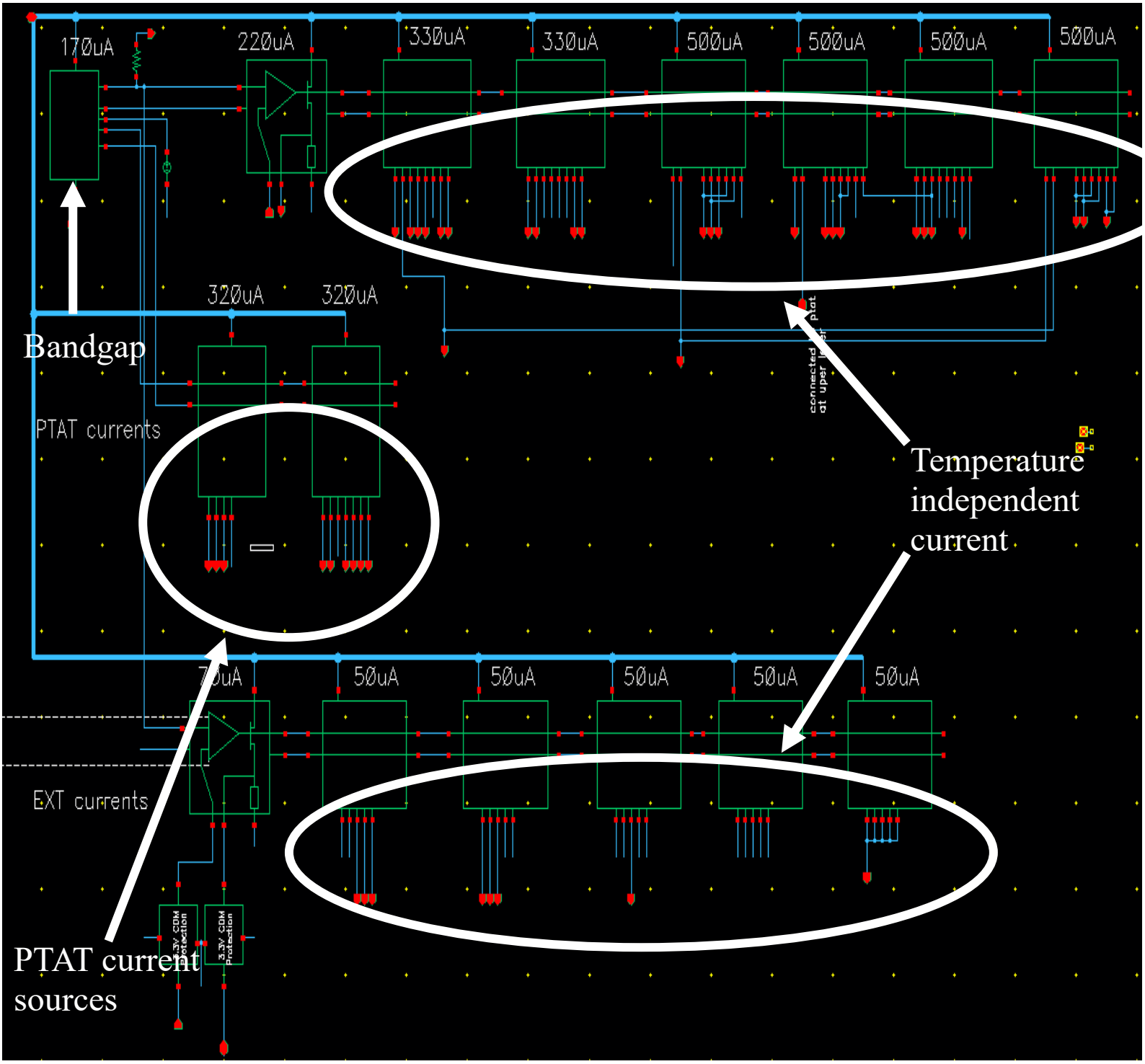
We annotate I : the ideal inputted current from i_in, I_{out} : the current outputted by G0 and G1, R : the ideal resistance R_0 equal to 100Ω and R_{poly} : the polysilicon resistance R_{23} equal to 100Ω.

We have: I_{out} = (RI-R_{poly} I_{out})×gain ➔ $I_{out} = \frac{\text{gain}\times RI}{1+\text{gain}\times R_{poly}} \approx \frac{RI}{R_{poly}}$ (assuming a high gain).

Finally, we get the targeted result and we can use this cell to simulate in PVT and Monte Carlo simulations

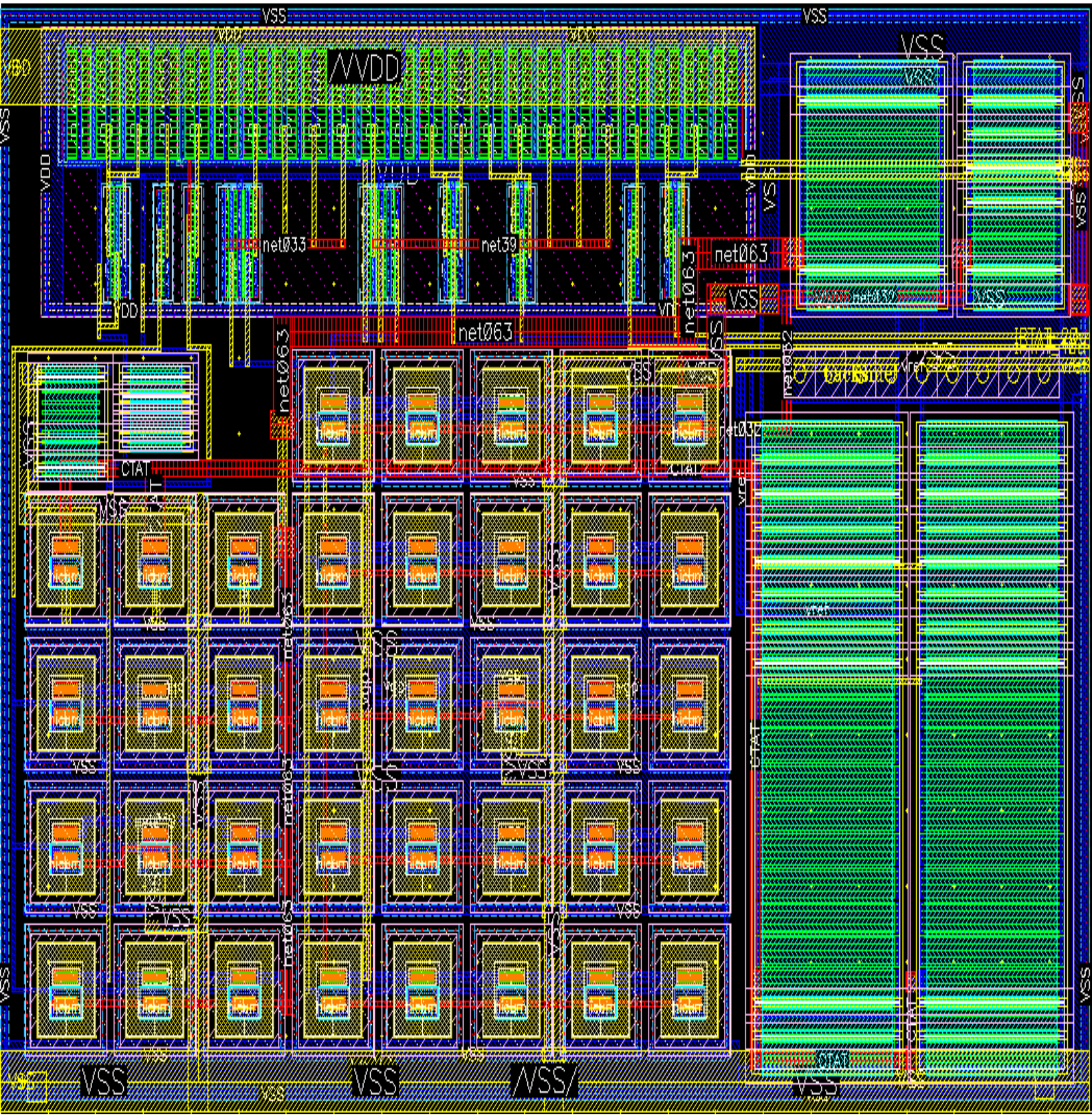
9.5-: Bandgap reference cell:

9.5.2-: First version of the bandgap layout



Top view of the bandgap cell

9.5.2-: First version of the bandgap layout

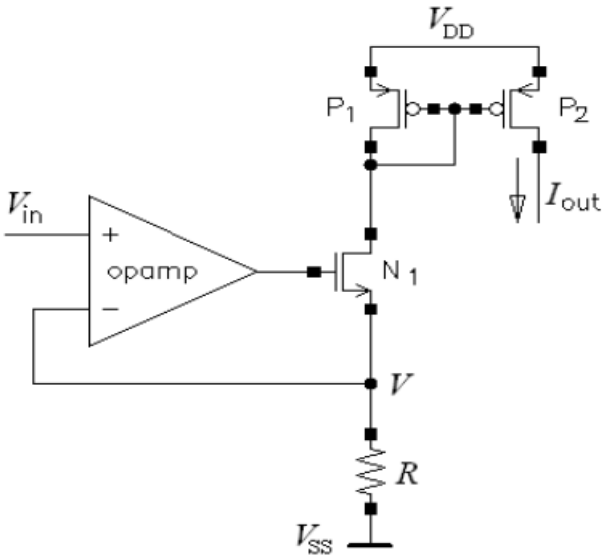


First version of the layout of the bandgap cell

9.6-: Voltage to current converter structures:

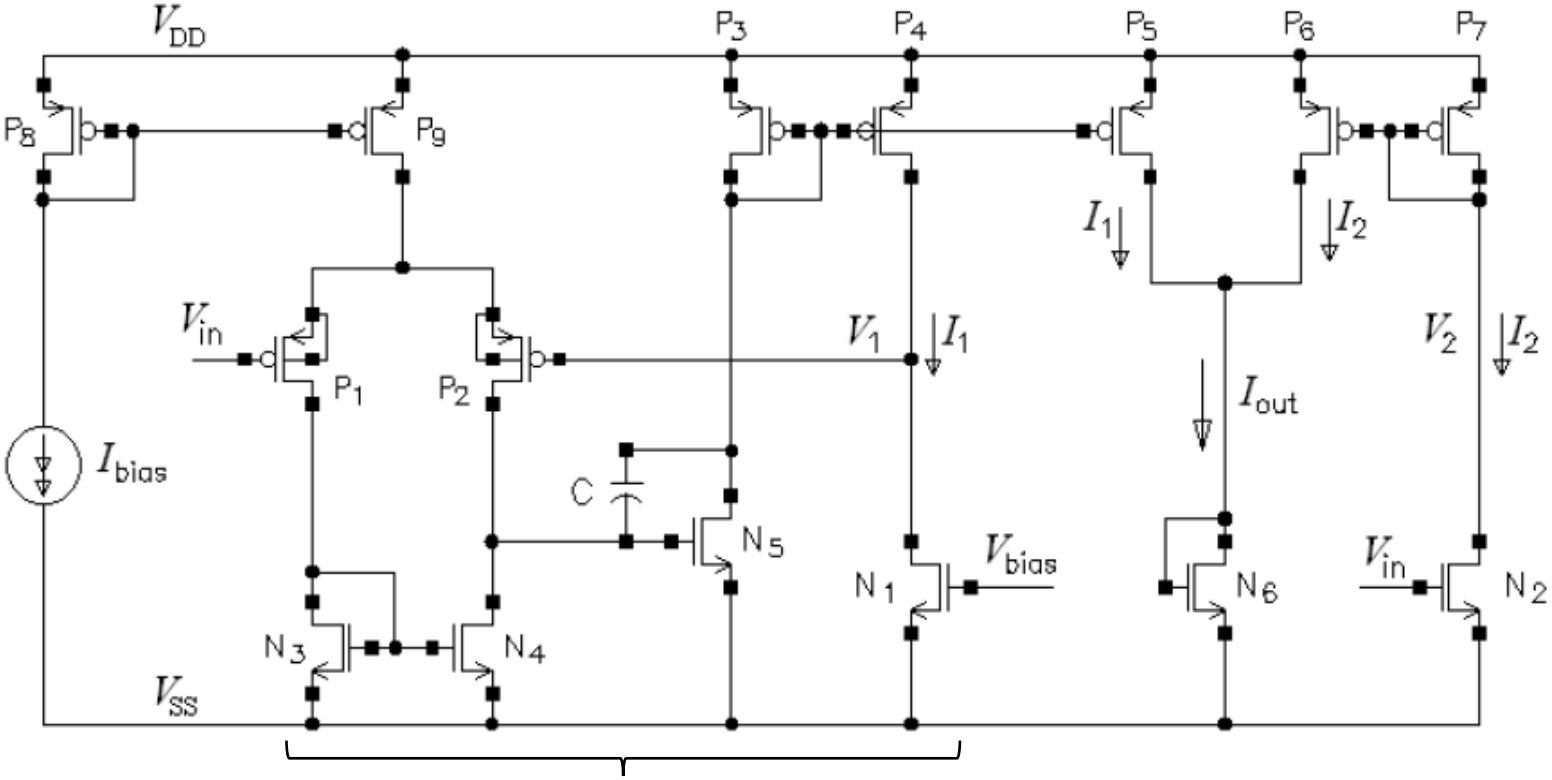
9.6.1: First proposed structure:

V_{in} is copied to the inverting input of the inverter, to the node V, generating a current across the resistance that will be copied to an output through transistor P_2 : $I_{out} = \frac{V_{in}}{R}$.



First proposed structure of the V2I [5]

9.6.2: Second proposed structure:



Three stages opamp

Second proposed structure of the V2I [5]

In this structure, the three stages OPAMP insures a voltage $V_{in} \approx V_1$. The transistor N_1 is pushed to tried having its gate voltage V_{bias} close to V_{DD}, this gives us a maximum value of V_{in} : $V_{in,max} = V_{bias} - V_{T,nmos}$, having N_1 in triode, it will act as a resistor and we'll have a very similar structure to the first proposed structure of the V2I. On the opposite side, N_2 is in saturation region to get a square-law relation of the drain current with respect to the input [5] and so V_{in} mustn't fall below the threshold voltage of N_2 : $V_{in,min} = V_{T,nmos}$. The output current of the V2I, is generated by mixing the drain current of N_1, $I_1, with$ the drain current of N_2, I_2.

$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}[2(V_{bias} - V_{T,nmos})V_{in} - {V_{in}}^2]$$

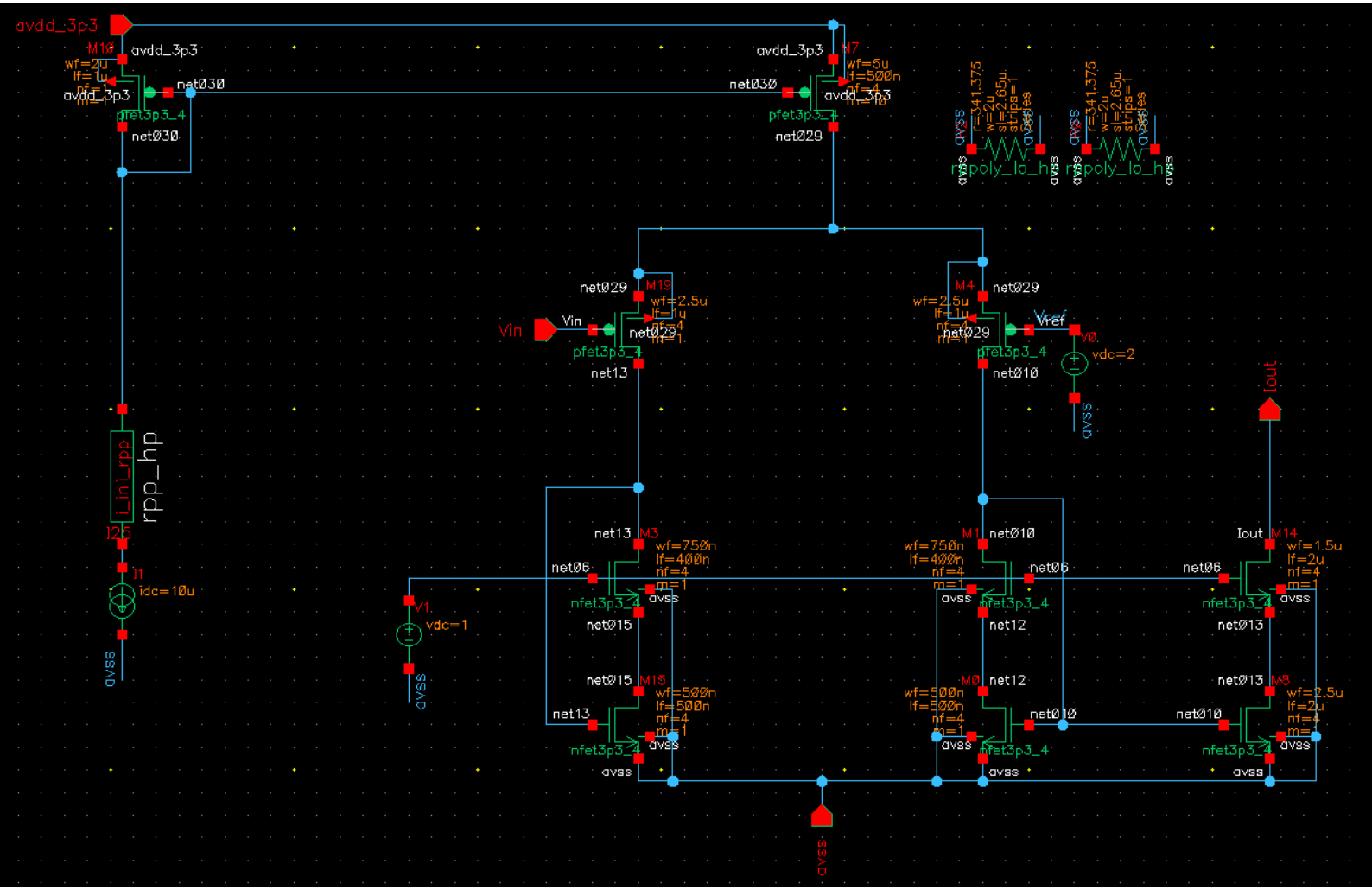
$$I_2 = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}[V_{in} - V_{T,nmos}]^2$$

Assuming the same size for $N_1$and N_2, $\frac{W_2}{L_2} = \frac{W_1}{L_1} = \frac{W}{L}$, we get the following output current:

$$I_{out} = I_1 + I_2 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{T,nmos}^2 + \mu_n C_{ox}\frac{W}{L}(V_{bias} - 2V_{T,nmos})V_{in} = \boldsymbol{I_0 + A \times V_{in}}$$

I_0 G

9.6.3: PMOS implementation of the chosen structure for the V2I

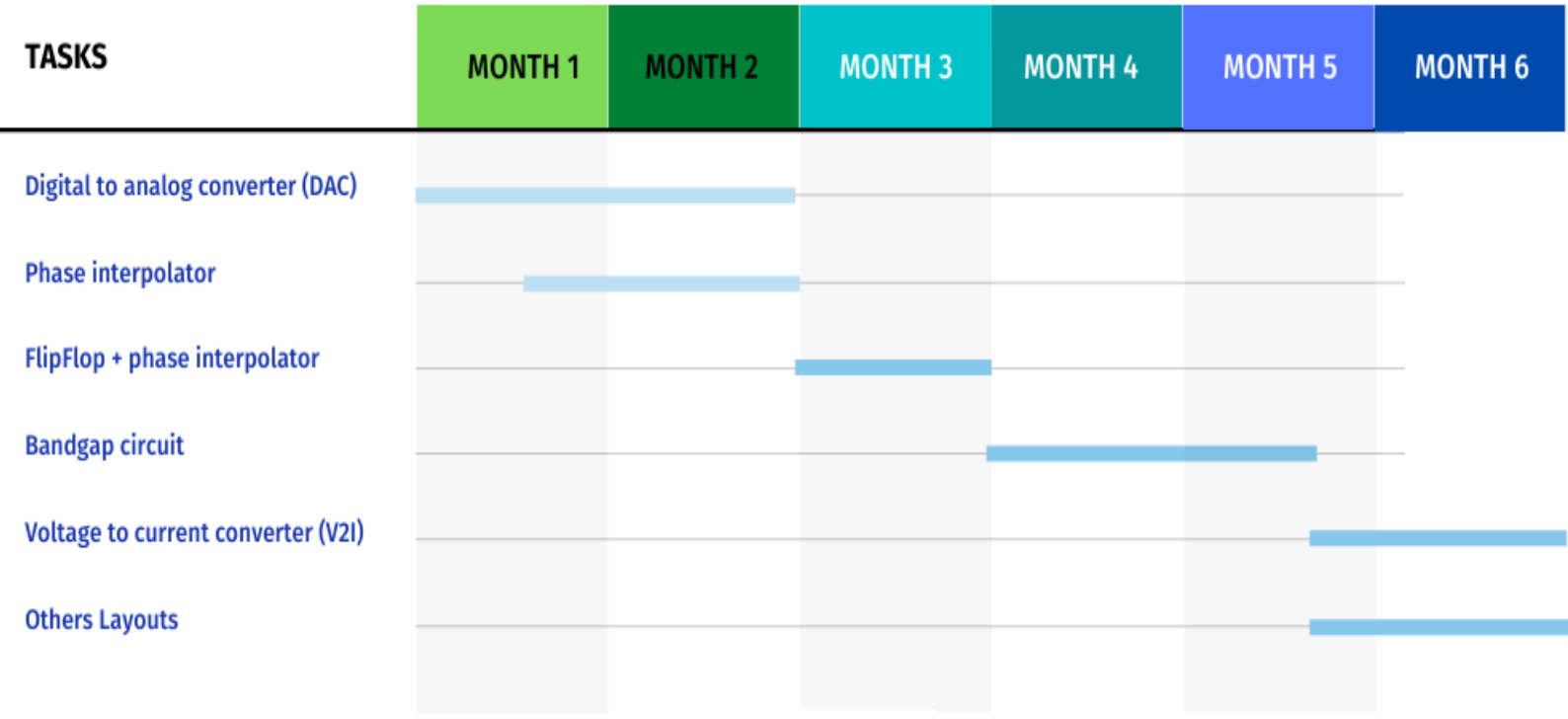


PMOS implementation of the chosen V2I structure

10.GANTT DIAGRAM

LITRINIUM

GANTT CHART



GANTT DIAGRAM

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