POLITECNICO DI TORINO

Master degree in Electronic Engineering

Master's degree Thesis

From FinFET to Nanosheet Si-SiGe GAAFET: fabrication process simulation and analysis

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Summary

The field-effect transistors are one of the building blocks of modern electronics. In the last 50 years, transistor technology had a noticeable development. According to Moore's law, the transistor dimensions became and continue to become very small: from the first MOSFET having a channel length of 20 μm in 1960 to the actual multigate devices (FinFET and GAAFET) with a channel length of a few nanometers. This continuous race is due to the increasing demand in electronic systems, not only for high integration density, but also for high performance and low power consumption.
In this context, this thesis aims to investigates, by means of physical simulations, multigates FETs. In particular, the work is divided into four parts. In the first part, the fabrication steps to realize a bulk FinFET are considered, in particular the various techniques used in each steps and why it is used that technique, the type of doping that changes in base of device type (n or p doping). Moreover the realization process of the FinFET differs not only for the doping type, but also for the material: instead of realizing source and drain with silicon, they are made with Silicon Carbide (SiC) in n-type finFET and with Silicon Germanium (SiGe) in p-type finFET. The choice of these materials is motivated by the fact that:

- SiC has a lattice constant that is smaller than the silicon one and this leads to a tensile stress in the channel which is in Silicon.
- SiGe has a lattice constant that is greater than the silicon one and this leads to a compressive stress in the channel.

The tensile and compressive stress causes an increase in electron an hole mobility, respectively.
The second part of the thesis consists on performing an electrical characterization of the two versions of the bulk FinFET by means of Sentaurus Device. For both types of FinFET is made a comparison between the case with and without stressed channel. Especially, it is underlined how the compressive (SiGe) and tensile (SiC) stress implies an increase in the mobility of the carriers and consequently in the ON current I_{on} and Subthreshold Swing (SS). In particular, it resulted an increment of about 20/30% in the Ion and a worsening of about 6% in the SS. In the third part, the effort spent in the bulk FinFET fabrication process is exploited to simulate the similar Gate-All-Around

FET fabrication process. Indeed, several steps are inherited from FinFET process. The main difference are the realization of alternating layers of silicon and silicon germanium, the introduction of silicon nitride inner spacer, and the subsequent etching of SiGe layers.
Also in this case the fabrication of non strained and SiC/SiGe strained version are simulated.
In addition, beside bulk GAAFET, also the fabrication process of a Silicon-On-Insulator (SOI) GAAFET is simulated.
And finally, in the last part of the thesis, the different versions are electrically characterized with Sentaurus Device and compared. Again an increment in the ON current is obtained in the comparison between non strained/strained channels and concerning the comparison between bulk and SOI version, an enhancement of Drain-Induced-Barrier Lowering (DIBL) is obtained.

Throughout this thesis, process simulations are performed in Sentaurus Process, electrical characterization with sentaurus Device and results are visualized with Sentaurus Inspect and post-processed in MatLab or MS Excel.
A brief tutorial on Sentaurus suite is presented at the end of the thesis.

In conclusion, the purpose of this thesis is twofold:

- highlight the importance of fabrication process simulations in a context where fabrication costs are becoming unaffordable and process variations dominant in devices performances;
- provide the advantages and disadvantages among the different device versions simulated and to demonstrate why nowadays there is a fervent push in substitute FinFET with GAAFET devices.

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CHAPTER 1

Introduction

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas[1].
According to Moore's law, the channel length of transistor should reduce by 50% every 6 years and its area should become 50% smaller every 3 years. But the more is the reduction of transistor and the more difficult it is to make a functional transistor. Below a certain size, it become impossible to manufacture a transistor with the traditional lithography process and, moreover, there are further issues: scaling the transistor leads to have Short Channel Effects (SCEs) and a reduction of gate oxide thickness that causes an increase of the leakage current. The consequences of the first one is the change of the threshold voltage value and a less strong electrostatic control of the channel; the SCEs can be limited by the use of a different technological choice. The second problem can be partially solved by introducing new gate oxide materials (e.g. Hafnium Oxide).
Initially, the transistors were planar. They were large enough to disregard the problems described previously.

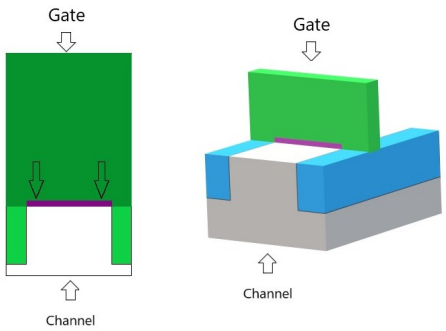


Figure 1.1:
Planar MOSFET (1 gate)

As manufacturing processes advanced, the transistors got smaller and smaller and, to avoid the troubles mentioned above, a three-dimensional configuration has been chosen. This configuration has channel's gate on three sides (three gates device), giving

it more surface area to electrostatically control the channel[2]. An example is the Fin Field-effect Transistor (FinFET).

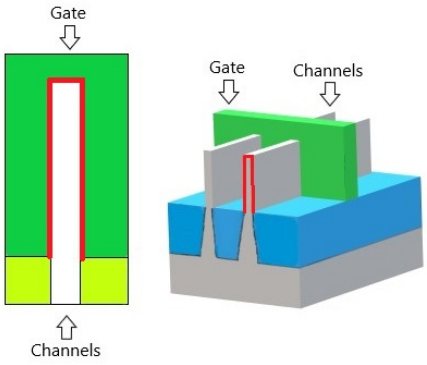
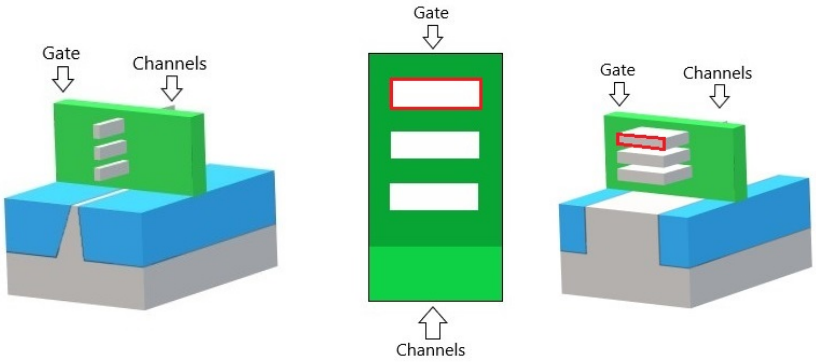


Figure 1.2:
FinFET (3 gates)

Until 3nm process node, FinFET presents the leakage current and other short channel problems under control. Beyond this point, new technologies are required to continue the further scaling step.
The development of three-dimensional configuration led to a structure in which the gate is completely surrounded. This structure is the Gate-All-Around FET (GAAFET) with nanowires or nanosheets.



(a) (b)

Figure 1.3: GAAFET (4 gates) (a) nanowires (b) nanosheets

The new Samsung's transistors are nanosheets. The stacking is vertical, with horizontal nanosheets, like a stack of printer paper, replacing the traditional fins[2]. According to Samsung, the advantages with respect to the FinFET are: [3]

- **Additional area is not required to improve speed:** Nanosheets can be stacked vertically instead of adding fins like with FinFETs.
- **Compatible with traditional FinFET Designs:** Designers can replace FinFETs without changing footprints.

- **Compatible with existing processes:** it shares the same process tools and manufacturing methodology as finFET.

1.1 Comparison between SOI and bulk technology

FinFET and GAAFET comes basically in two flavors, bulk and Silicon-On-Insulator(SOI). However, there are substantial differences as regard as the shape and the parasitic elements due to the different process flow.
The SOI-based flow consists of making the FET on the wafer's buried oxide layer, that allows to isolate the fins or the nanosheets from the silicon substrate and to better control their shape and size.
On the contrary, in the bulk silicon-based flow there is not a clear demarcation between the base of fin or nanosheet, therefore it is necessary the use of implanted wells and shallow-trench-isolation oxide to isolate the channel from electrical point of view. Moreover, the bulk wafer isolates it also from the thermal point of view; in the case of SOI one, this is not possible due to the BOX layer.

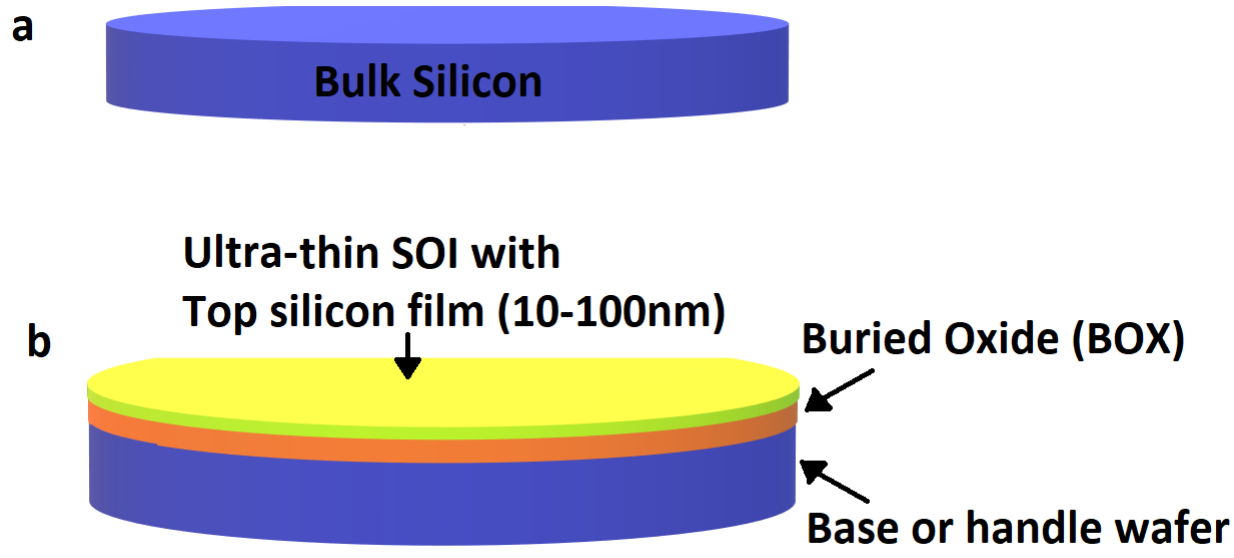
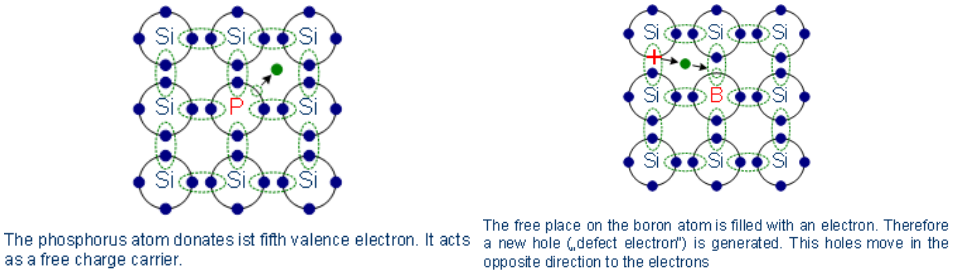


Figure 1.4: (a) BULK wafer (b) SOI wafer

CHAPTER 2

Fabrication process simulation of BULK FinFET

A fin field-effect transistor (finFET) is a type of non-planar transistor, or "3D" transistor[4], a multigate device. Its name derives from the fact that source/drain region forms fins on the silicon surface. The first FinFET was commercialized in the first half of 2010s and became dominant in the 14nm, 10nm and 7nm process nodes. A FinFET can be fabricated on SOI wafer or on bulk wafer. The SOI configuration has an insulating layer made of oxide between the fin and the silicon substrate. In the bulk configuration the fin is directly in contact with the silicon substrate.
As for MOSFETs, also for FinFETs there are two distinct types (n and p) according to the type of doping. The n-type finFET has n-type doped (e.g. Phosphorus) source and drain and the channel is doped with a p-type dopant (e.g. Boron); while in the p-type finFET is the opposite respect the previous case.
A n-type dopant is an element of V Group that adds extra valence electrons which are unbonded from individual atoms and in this way it realizes an electrically conductive n-type semiconductor. This dopant is also known as electron donor.
A p-type dopant is a III Group element. Doping silicon with it, there are holes in silicon lattice that are free to move. This element is also said electron acceptor and it makes an electrically conductive p-type semiconductor.



(a) (b)

Figure 2.1: ***Doping*** (a) *n-type* **donor** (b) *p-type* **acceptor**

In both finFET types, an improvement can be performed by using a SiC (n-type finFET) or a SiGe (p-type finFET) source/drain instead of a silicon one. This solution increases mobility of electrons and holes.

2.1 n-type BULK finFET

The fabrication of n-type BULK finFET consists of several steps. A 5 nm n-type finFET is taken into account. It has a channel length of 25 nm; a Phosphorus concentration of $2 \cdot 10^{20} cm^{-3}$ for source and drain; a Boron concentration of $1 \cdot 10^{15} cm^{-3}$ for the channel and one of $2 \cdot 10^{18} cm^{-3}$ for the substrate.

2.1.1 P-well implantation

Initially, a 10 nm silicon epitaxial layer is grown on a bulk wafer. Then a boron dose of $1 \cdot 10^{13} cm^{-2}$ is implanted with an energy of 30 keV and a Rapid Thermal Annealing (RTA) is performed at 1000°C (Figure 2.2).

The **Ion Implantation** is a method used for doping semiconductor. The implanter introduces the dopant atoms into the lattice at room temperature by means of the high kinetic energy generated by it.
High energy ions can damage the silicon lattice. A thermal annealing is required to avoid damages, in particular, a RTA is performed. In the semiconductor industry, rapid thermal annealing (**RTA**) is a semiconductor process step used for the activaton of the dopants and the interfacial reaction of metal contacts[5]. In the principle, the operation involves rapid heating of a wafer from ambient to approximately 1000-1500 K[5]. As soon as the wafer reaches this temperature, it is held for a few seconds and then finally quenched[5].

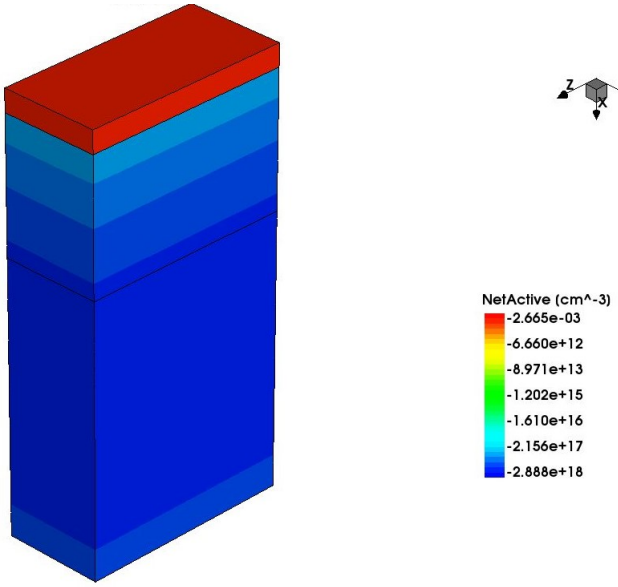


Figure 2.2: p-well implantation (*Boron concentration blue part*)

2.1.2 Fin fabrication with SIT

The **Sidewall Image Transfer** (**SIT**) is a technique used when there is the need to realize fins because it is impossible to make them with the photolithography due to hig aspect ratio and small pitch. The aspect ratio is equal to FH/FT, where FH is the fin height and FT is the fin thickeness.
The SIT required 6 steps:

1. The Silicon substrate is covered with 2.5 nm of SiO_2, 16.5 nm of Si_3N_4 and 19.5 nm of Silicon by deposition. The three layers are called **Buffer Oxide**, **Transfer Layer** and **Mandrel Layer** respectively.

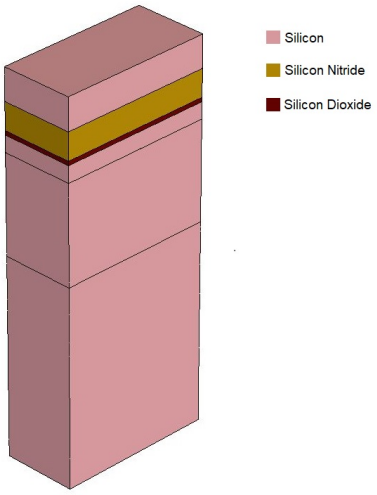


Figure 2.3: Mandrel Layer (Silicon), Transfer Layer (Nitride), Buffer Oxide (SiO_2)

2. The mandrel layer is modeled performing etching using mask and the photolithography at the maximum resolution.

3. The SiO_2 spacers are formed by performing an anisotropic etching and subsequently an isotropic overetch. This is the same method applied in CMOS process. The width of the spacers' base is lower than the maximum photolithograpy resolution because it depends only on the etching process and the aspect ratio of the mandrel.

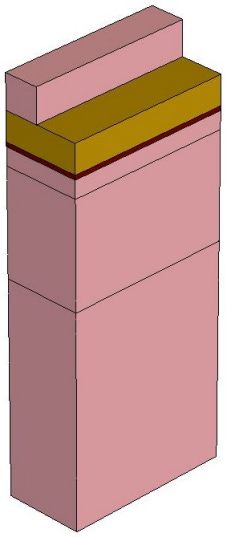


Figure 2.4: Mandrel

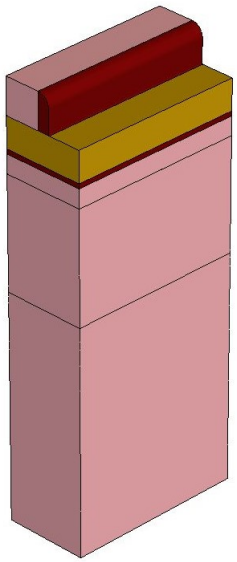


Figure 2.5: SiO_2 spacer

4. The mandrel is etched. The spacers are used as hardmask and then the transfer layer is also etched. In this way the Si_3N4 will be the hardmask for the fin etching.

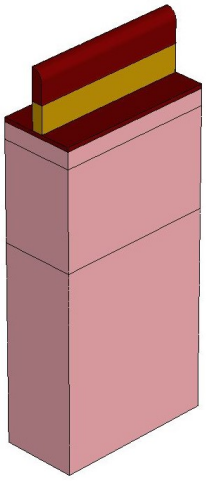


Figure 2.6: Mandrel and nitride etching

5. The nitride hardmask is necessary for the Silicon etching after removing spacers. So the fin is formed.

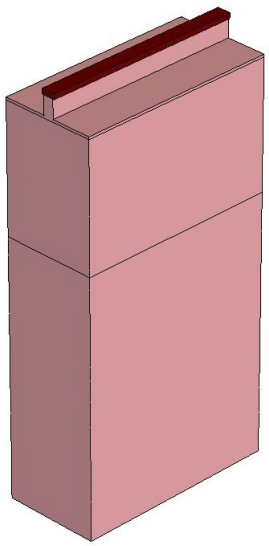


Figure 2.7: Fin Formation

6. Finally, the remaining oxide is etched.

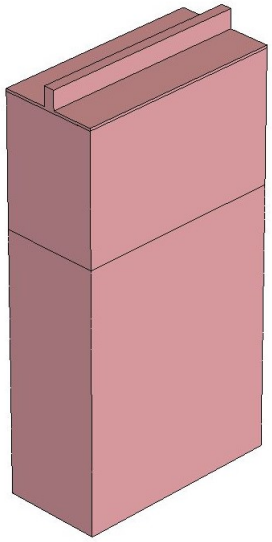
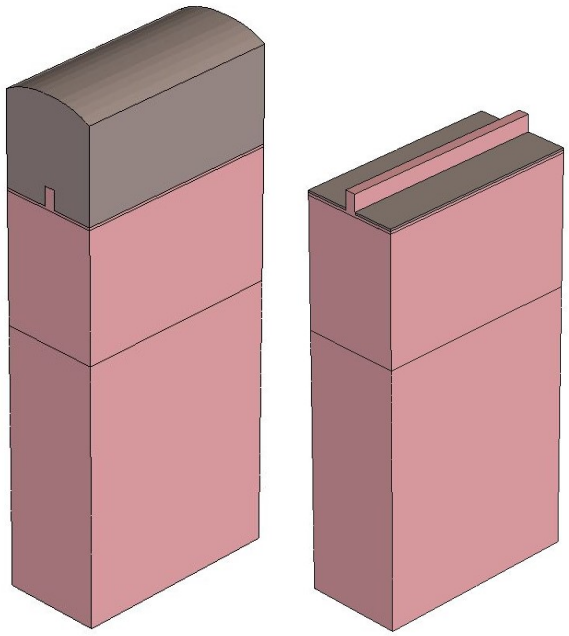


Figure 2.8: Fin after removing oxide

2.1.3 TEOS CMP

After the realization of the fin, the deposition and the etching of TEOS (figure 2.9).
The thetraethyl orthosilicate (**TEOS**) is a chemical compound with the formula $Si(C_2H_5O)_4$.

TEOS is deposited in a CVD system where wafers are first heated to a lower temperature than typical for dielectric films (Between 200°C – 500°C)[6]. Once the furnace reaches the proper temperature, a gaseous TEOS mixture distributes uniformly through the system, parallel to the wafers[6]. After distributing the gas evenly, radio-frequency energy between the gas and the surface of the wafers begins the deposition process[6]. Then the TEOS surface is smoothed by CMP process.



(a) (b)

Figure 2.9: TEOS *(grey)*: (a) Deposition (b) CMP

The Chemical Mechanical Polishing (**CMP**) or planarization is a process of smoothing surfaces with the combination of chemical and mechanical forces. It can be thought of as a hybrid of chemical etching and free abrasive polishing[7].

2.1.4 Thermal Oxidation

The fin is oxidized by exploiting thermal oxidation (figure 2.10).

The thermal oxidation is a process that consists in making oxide grow on the surface using the silicon present on it. The typical temperature range for oxidation is 900°-1100° C.

The generic equation is:

$$x^2 + Ax = B(t + \tau) \tag{2.1}$$

where

$$A = \frac{2D}{K} \quad B = \frac{2DC_0}{C_{ox}} \quad \tau = \frac{C_{ox}}{2DC_0}d_0^2 + \frac{C_{ox}}{KC_0}d_0$$

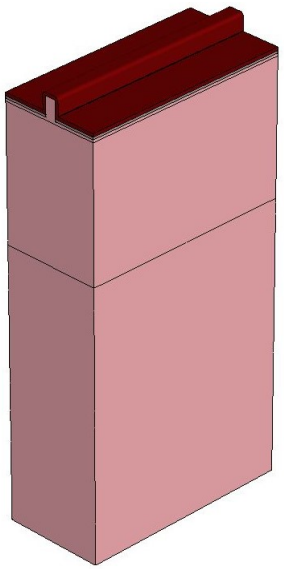


Figure 2.10: Thermal Oxidation

x is the thickness of the grown oxide; C_0 is the concentration of oxygen molecules in the atmosphere; C_{ox} is the concentration of oxidant in the new oxide; D is is the oxidant diffusivity; K is the chemical kinetic constant; d_0 is the thickness of the unwanted oxide that grows on the wafer; τ is the extra time due to the growth of the unwanted oxide. There are two types of thermal oxidation:

- *dry oxidation*: the silicon reacts with oxygen molecules. It is very slow and it is optimal for growing very thin layer, therefore in the general equation the x^2 term is neglected.
$$x \approx \frac{B}{A}(t+\tau) \tag{2.2}$$
- *wet oxidation*: the silicon reacts with water molecules. It is suitable for thick layer due to the growth rate that is 10 times faster than using dry oxidation. In this case the x term is neglected, so:
$$x^2 \approx \sqrt{B(t+\tau)} \tag{2.3}$$

Finally, the dry oxidation depends linearly with respect to time(t), while the wet one depends on $\sqrt{t}$.

2.1.5 Dummy gate

The aim of dummy gate is to favor the realization of source/drain extensions and the S/D epitaxial growth.
A layer of polysilcon is deposited on the fin and then etched through photolithography. The remains of polysilicon cover the central part of the fin.

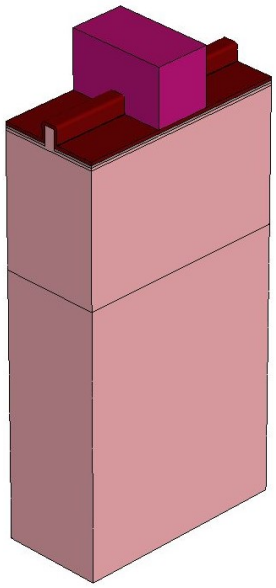


Figure 2.11: Dummy gate - Polysilicon (*violet*)

Using a mask, a thin oxide layer is formed on both sides of the dummy gate. Its thickness is 1 nm and it is called wall.

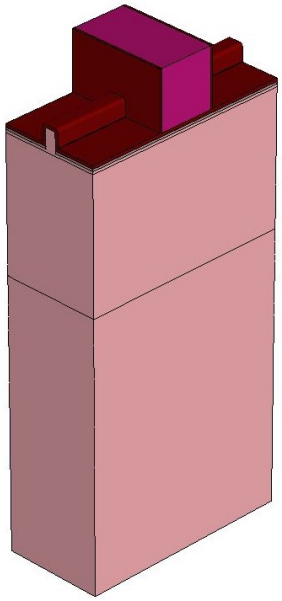


Figure 2.12: Oxide walls

Then the dummy gate is covered by a thick layer of photoresist and a $1 \cdot 10^{12} cm^{-2}$ dose of Phosphorous is implanted with an energy of 30 keV and a tilt angle of 10 degrees. Subsequently a RTA is performed (1000°C 0.1s) to activate the dopant.

The role of extensions is to limit the hot carrier injection phenomenon by reducing the electric field peak. This phenomenon can damage irreversibly the transistor because the threshold voltage can permanently change if there are too many electrons trapped into the gate oxide.

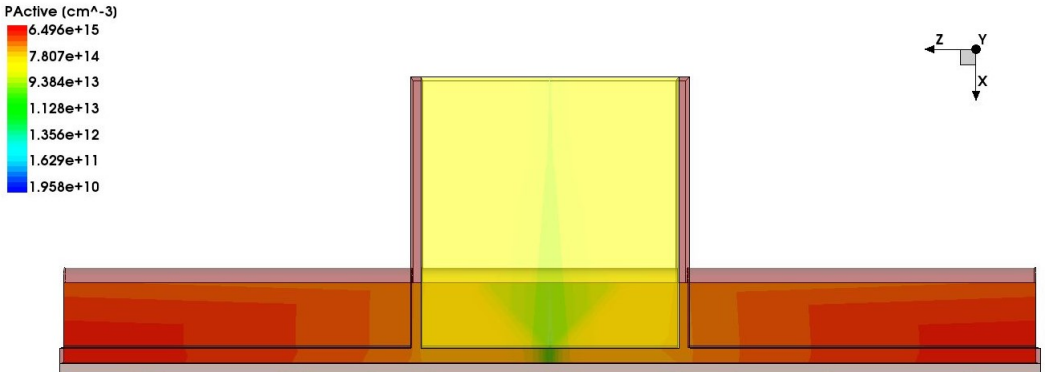


Figure 2.13: Phosphorous S/D extensions. Polysilicon and SiO_2 are in translucency

2.1.6 S/D Creation

Si_3N_4 spacers are realized to define source and drain. The spacers are formed in the same way as the SiO_2 ones in the SIT process (isotropic deposition, anisotropic echting plus isotropic overecthing).

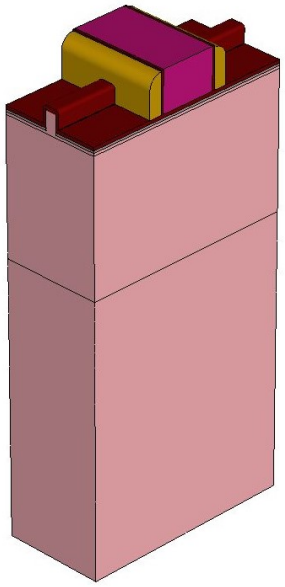


Figure 2.14: Si_3N_4 formation

Before creating source and drain, it is necessary to remove the silicon dioxide. To accomplish it, silicon carbonitride (SiCN) is employed as mask. Exploiting photolithography, it covers the dummy gate and it is used as mask.

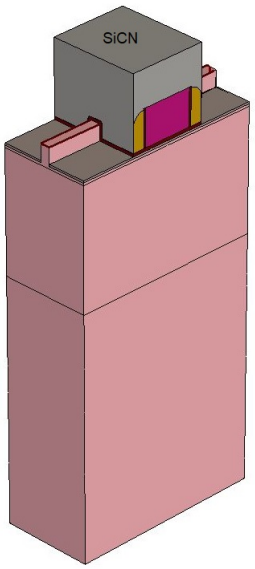
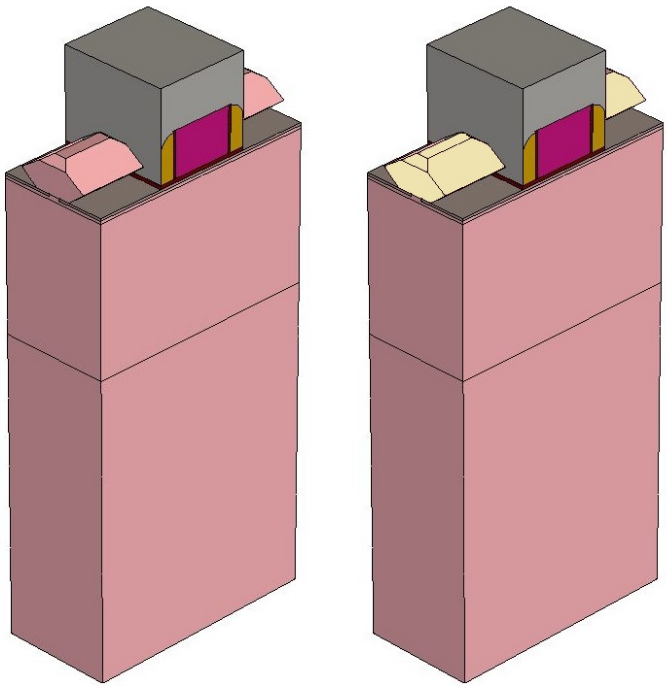


Figure 2.15: SiCN photolithography

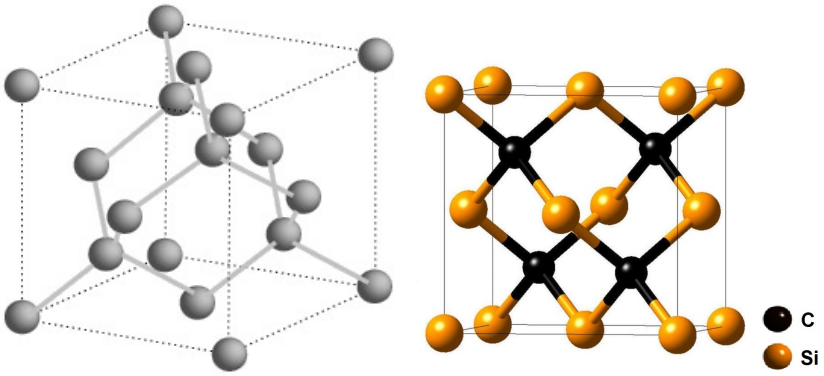
Once the oxide is removed, the exposed part of the fin is removed and epitaxial growth of the source and drain is performed. It is possible to have an epitaxial growth of n-doped ($2 \cdot 10^{20} cm^{-3}$ of phosphorus) Silicon or a growth of n-doped Silcon Carbide (figure 2.16).



(a) (b)

Figure 2.16: S/D epitaxial growth: (a)n++ Silicon S/D (b) n++ SiC S/D

Silicon Carbide The principal difference between the two types is the lattice spacing. The silicon lattice constant is 5.43 Å, while the SiC lattice constant is 3.073 Å. This disparity leads to a tensile stress on the channel and consequently the electron mobility increases.



(a) (b)

Figure 2.17: Lattice structure: (a)*Silicon* (b)*Silicon Carbide*

2.1.7 Silicidation and dummy gate removal

The SiCN is removed and a thin layer of Titanium is deposited on S/D and then the silicidation process begins. Titanium reacts with Silicon and it gives Titanium Silicide that is 1 nm thick. The unreacted Titanium is etched.

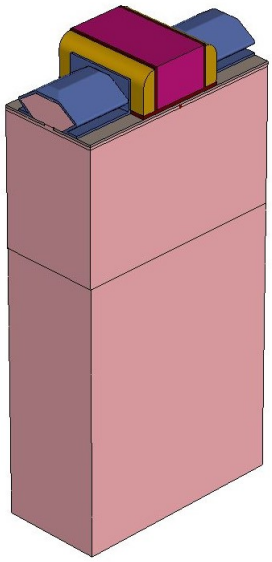


Figure 2.18: Silicidation - $TiSi_2$ (*lilac*)

The silicidation is necessary to reduce S/D contact resistance. The siicide materials have a resistivity comparable to the metal one ($\approx 1\mu\Omega \cdot cm$). In the table 2.1 is reported the resistivity value of the main silicide materials.

Silicide	**Resistivity**$[\mu\Omega \cdot cm]$
$TiSi_2$	13 - 16
$TaSi_2$	35 - 45
$MoSi_2$	90 - 100
WSi_2	70
$CoSi_2$	16 - 20
$PtSi_2$	28 - 35

Table 2.1: Resistivity of silicide materials

A 20 nm layer of Phosphosilicate glass (**PSG**) is placed on the all structure and then its surface is smoothed by using CMP in such a way as to remove the portion above the dummy gate (figure 2.19).

Finally the dummy gate is eliminated: using silicon dioxide as a mask, the polysilicon is etched and, subsequently, the removal of SiO_2 covering the gate is exploited (figure 2.20).

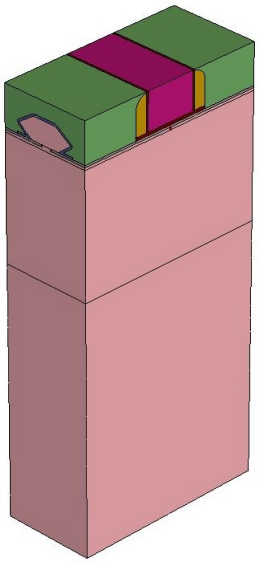


Figure 2.19: PSG(*green*) deposition and CMP

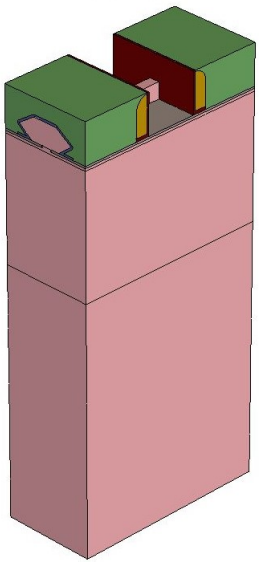


Figure 2.20: Dummy gate removal

2.1.8 Gate stack

The next step consists in thin thermal oxidation(1 nm) of the exposed part of the fin and a subsequent deposition of a thin layer(1 nm) of hafnium oxide. It is needed to avoid dielectric breakdown and leakage by quantum tunneling (figures 2.21 2.22).

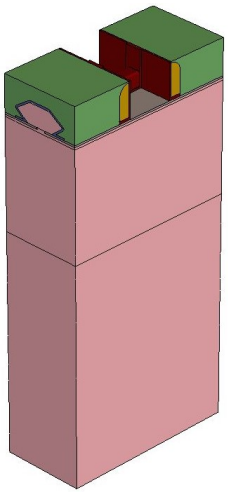


Figure 2.21: Gate thermal oxidation

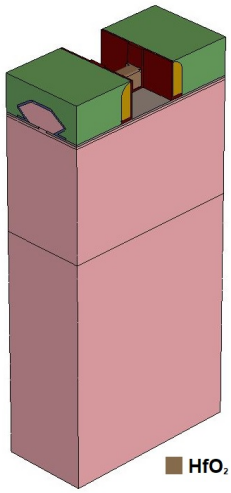


Figure 2.22: HfO_2 deposition

Moreover a high-K dielectric(HfO_2)/metal interface is formed to prevent parasitic phenomena such as gate poly depletion. Using the metal-interdiffusion technology (MIG), a stack is created. This stack consists in two layers of insulating materials (SiO_2, HfO_2) and three layers of conductor materials (TiN, TaN, TiAl).
$15\mathring{A}$ of titanium nitride, $15\mathring{A}$ of tantalum nitride and $20\mathring{A}$ of titanium aluminide are deposited on HfO_2.

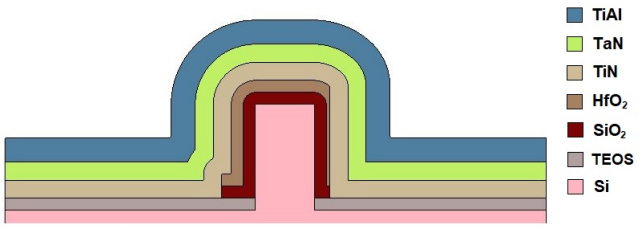


Figure 2.23: n-finFET Gate stack

The choice of the Ti and Al metals was made following two main criteria. These metals have:

- a low work function in vacuum in order to favor the nfinFET EWF[8],
- a free energy of metal-oxide formation lower than the one of SiO2 which enables the oxygen scavengingfrom the SiO_2 [8].

The EWF is the Effective Work Function thatis defined as the energy difference of the metal Fermi energy and the Si Conduction Band edge (the n-type barrier height, ϕ_n) plus the energy of the Si CB edge to the vacuum level (the Si Electron Affinity, $\chi_{Si} = 4.05$ eV) [9].

$$EWF = \chi_{Si} + \phi_n \tag{2.4}$$

2.1.9 Contacts

The stack is covered with tungsten and then the excess is etched by performing CMP to obtain the tungsten at a height less than that of the PSG of 1nm. The same is done with the Si_3N_4, the only difference is its height which is the same as the PSG.

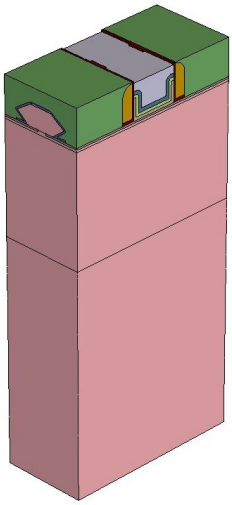


Figure 2.24: Tungsten(*grey*) deposition on gate stack

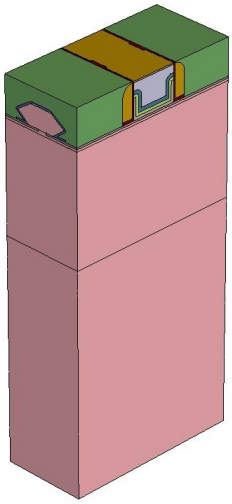


Figure 2.25: Si_3N_4 deposition on tungsten

The technique of self-aligned contact (SAC) is applied to form S/D contacts. SAC is used to prevent short circuits between drain and gate or source and gate. This technique consists in a partial removal of PSG at source/drain by using photolithography and etching. The created cavity is filled with the deposition of tungsten.
As regard as the gate contact, it is made with photolithography and subsequent etching of the nitride. Finally W deposition and CMP is exploited.

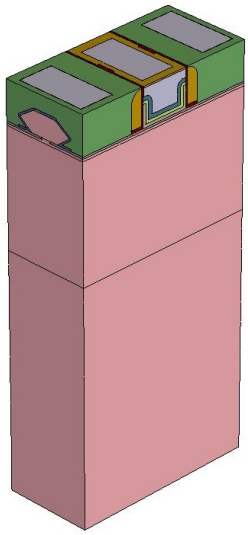


Figure 2.26: n-type BULK finFET

2.2 p-type BULK finFET

The necessary steps to fabricate a p-type BULK finFET is the same of the n-type one. The exceptions are:

- type of dopant for source/drain;
- type of dopant for the channel and the substrate;
- the use of silicon germanium instead of silicon carbide as stressed material.

In following section are described only the steps that differ from the n-type finFET. A 5 nm p-type finFET is taken into account. It has a channel length of 25 nm; a Boron concentration of $2 \cdot 10^{20} cm^{-3}$ for source and drain; a Phosphorus concentration of $1 \cdot 10^{15} cm^{-3}$ for the channel and one of $2 \cdot 10^{18}$ for the substrate.

2.2.1 N-well implantation

As in the case of n-type finFET, a 10 nm silicon epitaxial layer is grown on a bulk wafer, a 30 keV implantation of phosphorus with a dose of $1 \cdot 10^{13} cm^{-2}$ is performed and a subsequent RTA is exploited at 1000°C for 1s.

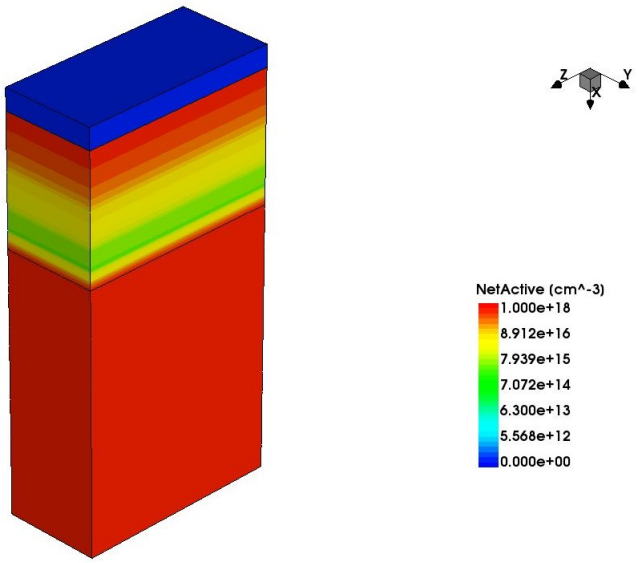


Figure 2.27: n-well implantation

After the n-well implantation, the fin is formed by applying the SIT technique. Then TEOS is deposited and etched with CMP process forming a shallow trench insulator. The exposed portion of the fin is oxidized by performing thermal oxidation.
A polysilicon dummy gate is created at the center part of the fin through photolithography and etching, and at its sides a thin wall (1 nm thick) is made.

2.2.2 S/D creation

The dummy gate is covered by a thick layer of photoresist and a 6 keV implantation is executed with a tilte angle of 10 degrees. The dose of the implanted dopant is $1 \cdot 10^{12} cm^{-3}$ and it is boron. Moreover, a RTA is done (1000°C 0.1s) to activate the dopant. S/D extensions are obtained.

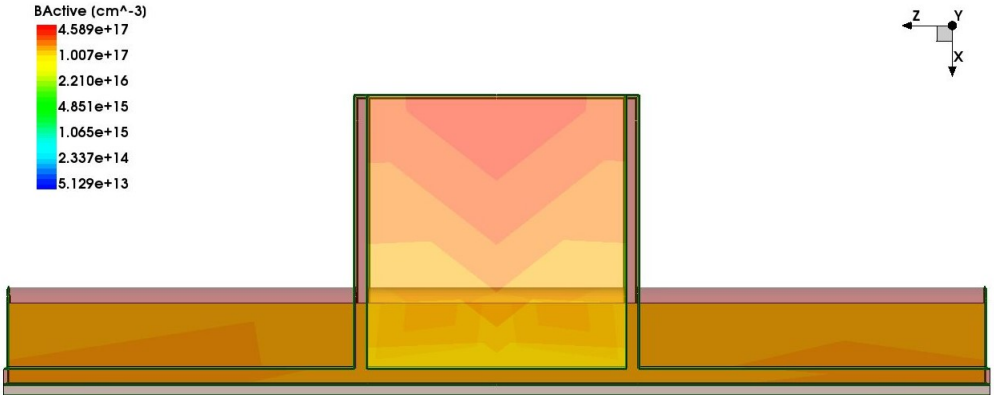
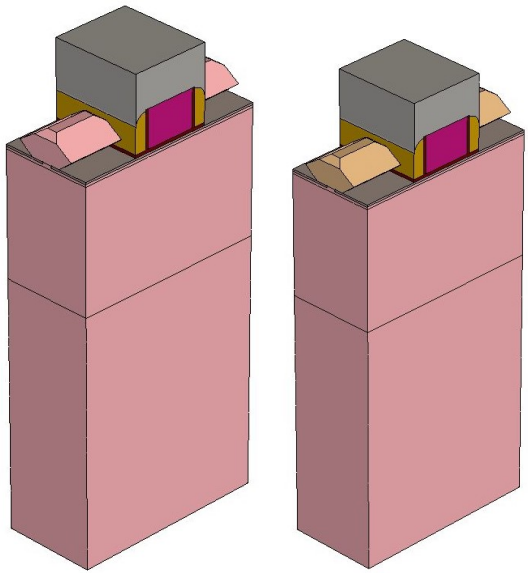


Figure 2.28: Boron S/D extensions. Polysilicon and SiO_2 are in translucency

Before the definition of the source and drain, Si_3N_4 spacers are realized near the oxide walls and the silicon dioxide is removed using silicon carbonitride as a mask. Subsequently the exposed part of the fin is etched and epitaxial growth of the source and drain is performed. A p-doped($2 \cdot 10^{20} cm^{-3}$ of boron) silicon or a p-doped silicon germanium can grow (figure 2.29).



(a) (b)

Figure 2.29: S/D epitaxial growth: (a)p++ Siliocn S/D (b) p++ SiGe S/D

Silicon Germanium The introduction of germanium in the silicon lattice leads to a change in the spacing between the atoms. As seen above, in the case of pure silicon the lattice constant is $5.43\mathring{A}$, while in SiGe it depends on the concentration of germanium: the lattice constant ranges from $5.43\mathring{A}$ (100% silicon) to $5.66\mathring{A}$ (100% germanium). So, increasing Ge concentration, a compressive stress increases on the channel and consequently the hole mobility increases.

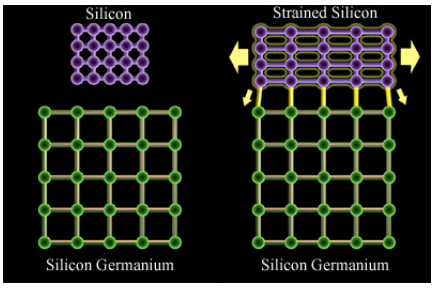


Figure 2.30: SiGe lattice structure and its effect on the Silicon

The SiCN is removed and the silicidation process is executed on S/D epitaxial layers using titanium as metal in the reaction with the silicon. The S/D areas are covered with PSG and then the CMP process is exploited in such a way to have it at the same height of the dummy gate. At this point, the dummy gate is etched using the SiO_2 as etch stop and, finally, the oxide is removed.

2.2.3 Gate stack

A stack in the gate area is realized through several step:

1. a thin layer (1 nm thick) is formed by performing dry thermal oxidation on the exposed part of the fin;
2. deposition of a HfO_2 layer with a thickness of 1 nm;
3. metal-interdiffusion technology is applied: four metal layer are deposited (TiN, TaN, TiN, TiAl)

Each metal layer has the thickness reported in the table 2.2.

Metal	**Thickness**[Å]
TiN	15
TaN	15
TiN	15
TiAl	20

Table 2.2: Thickness of the metals in the gate stack

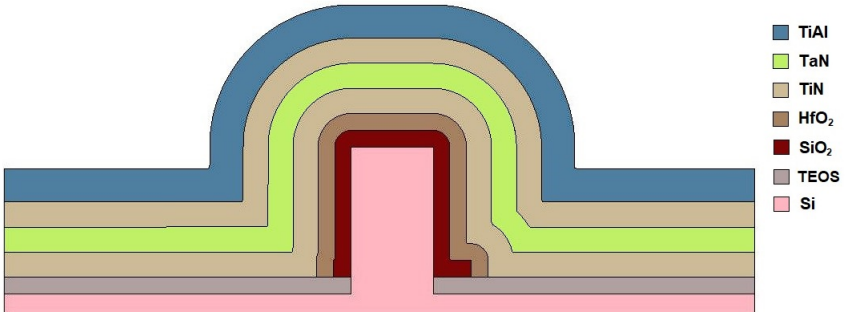


Figure 2.31: p-finFET Gate stack

2.2.4 Contacts

The stack is covered with tungsten and nitride as it happens in the case of n-type finFET. The PSG is partially etched: a cavity is formed. It is filled with tungsten: the S/D contacts are made. In the same way it happens for the gate contact: the Si_3N_4 is partially removed and W deposition and CMP are exploited.

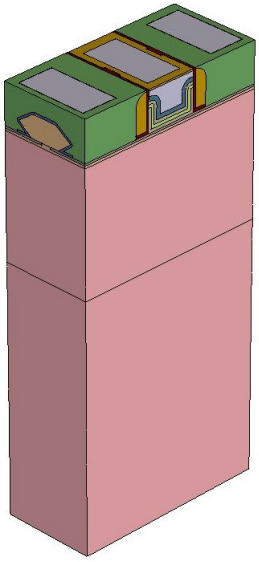


Figure 2.32: p-type BULK finFET

CHAPTER 3

Physical simulation of BULK FinFET

A An electrical device simulation of the two FinFET's types (realized previously) is made by using the software Synopsys Sentaurus Device, then the results are are visualized, post-processed, analyzed and finally compared with Sentaurus Inspect, Matlab and MS Excel. Through SDevice, the electron/hole mobility, the device stress and the Carbon/Germanium concentration are taken into account. In particular the analysis is focused on how the introduction of Carbon/Germanium influences the leakage current and the mobility of the device and consequently its Ion current.

3.1 Simulation models

The simulation of the two types of FinFET is made by means of a specific model for mobility, recombination and mechanical stress effect. The trans-characteristic Id-Vgs is derived from the combination of these models.

3.1.1 Mobility models

As regard as the calculation of the carrier mobility, several phenomena are taken into account. Normally the mobility is a function of the lattice temperature. In the case of doped materials the carriers scatter with the impurities, this leads to a degradation of the mobility.
The used models describe the mobility degradation due to the doping and the scattering with surface phonons and surface roughness and moreover they describe the degradation in high electric field.
In doped semiconductors, scattering of the carriers by charged impurity ions leads to degradation of the carrier mobility [10].

Masetti model As doping-dependent mobility model, the Masetti model is adopted. It follows the equation below:

$$\mu_{dop} = \mu_{min1} e^{-\frac{P_c}{N_{A,0}+N_{D,0}}} + \frac{\mu_{cost} - \mu_{min2}}{1 + \left(\frac{N_{A,0}+N_{D,0}}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{N_{A,0}+N_{D,0}}\right)^{\beta}} \tag{3.1}$$

The default values for each coefficients in the case the material is silicon are reported in table 3.1

Symbol	Electrons	Holes	Unit
μ_{min1}	52.2	44.9	cm^2/Vs
μ_{min2}	52.2	0	cm^2/Vs
μ_1	43.4	29.0	cm^2/Vs
P_c	0	$9.23 \cdot 10^{16}$	cm^{-3}
C_r	$9.68 \cdot 10^{16}$	$2.23 \cdot 10^{17}$	cm^{-3}
C_s	$3.43 \cdot 10^{20}$	$6.10 \cdot 10^{20}$	cm^{-3}
α	0.680	0.719	1
β	2.0	2.0	1

Table 3.1: Masetti model: default coefficients

In the channel region of the FinFET, the high transverse electric field forces carriers to interact strongly with the semiconductor–insulator interface. Carriers are subjected to scattering by acoustic surface phonons and surface roughness [10]. The chosen model that describe the mobility degradation caused by these effects is the Remote Phonon Scattering (RPS) model.

Remote Phonon Scattering model The RPS degradation mobility is obtained by the following equation:

$$\mu_{rps} = \frac{\mu_{rps0}}{\left(\frac{F_\perp}{10^6 V/cm}\right)^{\gamma_1} \left(\frac{T}{300K}\right)^{\gamma_2}} \tag{3.2}$$

The default values for each coefficients in the case the material is silicon are reported in table 3.2

Symbol	Electrons	Holes	Unit
μ_{rps0}	496.7	496.7	cm^2/Vs
γ_1	0.68	0.68	1
γ_2	0.34	0.34	1

Table 3.2: RPS model: default coefficients

In high electric fields, the carrier drift velocity is no longer proportional to the electric field, instead, the velocity saturates to a finite speed v_{sat} [10]. The High-Field Saturation model is the Canali model.

Canali model It derives from the Caughey-Thomas formula [11], but it has temperature-dependent parameters [12]:

$$\mu(F) = \frac{(\alpha+1)\,\mu_{low}}{\alpha + \left[1 + \left(\frac{(\alpha+1)\,\mu_{low} F_{hfs}}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}} \tag{3.3}$$

where μ_{low} is the low-field mobility. The exponent β is temperature dependent according to:

$$\beta = \beta_0 \left(\frac{T}{300K}\right)^{\beta_{exp}} \tag{3.4}$$

Instead, the velocity saturation v_{sat} is given by:

$$v_{sat} = v_{sat,0} \left(\frac{300K}{T}\right)^{v_{sat,exp}} \tag{3.5}$$

The driving force F_{hfs} is calculated as:

$$F_{hfs} = |\nabla \phi_n| \tag{3.6}$$

The default values for each coefficients in the case the material is silicon are reported in table 3.3

Symbol	**Electrons**	**Holes**	**Unit**
β_0	1.109	1.213	1
β_{exp}	0.66	0.17	1
α	0	0	1
$v_{sat,0}$	$1.07 \cdot 10^7$	$8.37 \cdot 10^6$	cm/s
$v_{sat,exp}$	0.87	0.52	1

Table 3.3: Canali model: default coefficients

3.1.2 Recombination models

The processes that exchange carriers between the conduction band and valence band are called recombination processes. In this analysis of the finFET, three types of recombination are used: *Shockley-Read-Hall*(SRH), *Auger* and *Band-to-Band tunneling*.

Shockley-Read-Hall Recombination It is a non-radiative recombination and it occurs when it is created a trap level within energy gap due to a defect in silicon lattice. The SRH recombination follows the model that implements the form below:

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p (n + n_1) + \tau_n (p + p_1)} \tag{3.7}$$

where:

$$n_1 = n_{i,eff} e^{\frac{E_{trap}}{kT}} \qquad p_1 = n_{i,eff} e^{\frac{-E_{trap}}{kT}}$$

E_{trap} is the difference between the defect level and and the intrinsic level. The silicon default value is $E_{trap} = 0$.
The τ_n and τ_p lifetimes are derived from the doping-dependent factor. The doping dependency is modeled with Scharfetter relation:

$$\tau_{dop} (N_{A,0} + N_{D,0}) = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_{A,0} + N_{D,0}}{N_{ref}} \right)^{\gamma}} \tag{3.8}$$

The default parameter for doping-dependent parameters are summarized in the table 3.4

Symbol	**Electrons**	**Holes**	**Unit**
τ_{min}	0	0	s
τ_{max}	$1 \cdot 10^{-5}$	$3 \cdot 10^{-6}$	s
τ_0	$1 \cdot 10^{-5}$	$3 \cdot 10^{-6}$	s
N_{ref}	$1 \cdot 10^{16}$	$1 \cdot 10^{16}$	cm^{-3}
γ	1	1	1
E_{trap}	0	0	eV

Table 3.4: Default parameters for doping-dependent SRH lifetime

Auger recombination It too is a non-radiative recombination. It happens when two electrons collide the vicinity of a hole which leads to a non-radiative recombination event. The energy and momentum is absorbed by the second electron [13]. The rate of band-to-band Auger recombination R_{net}^A is given by:

$$R_{net}^A = (C_n n + C_p p) \left(np - n_{i,eff}^2 \right) \tag{3.9}$$

with temperature-dependent Auger coefficients:

$$C_n (T) = \left(A_{A,n} + B_{A,n} \left(\frac{T}{T_0} \right) + C_{A,n} \left(\frac{T}{T_0} \right)^2 \right) \left[1 + H_n e^{-\frac{n}{N_{0,n}}} \right] \tag{3.10}$$

$$C_p(T) = \left(A_{A,p} + B_{A,p} \left(\frac{T}{T_0} \right) + C_{A,p} \left(\frac{T}{T_0} \right)^2 \right) \left[1 + H_p e^{-\frac{p}{N_{0,p}}} \right] \tag{3.11}$$

where $T_0 = 300$ K. There is experimental evidence for a decrease of the Auger coefficients at high injection levels [14]. This effect is explained as resulting from exciton decay: at lower carrier densities, excitons, which are loosely bound electron–hole pairs, increase the probability for Auger recombination. Excitons decay at high carrier densities, resulting in a decrease of recombination [10]. This effect is modeled by the terms $1 + He^{-n/N_0}$.
The default value of the coefficients for silicon are listed in table 3.5.

Symbol	**Electrons**	**Holes**	**Unit**
A_A	$6.7 \cdot 10^{-32}$	$7.2 \cdot 10^{-32}$	$cm^6 s^{-1}$
B_A	$2.45 \cdot 10^{-31}$	$4.5 \cdot 10^{-33}$	$cm^6 s^{-1}$
C_A	$-2.2 \cdot 10^{-32}$	$2.63 \cdot 10^{-32}$	$cm^6 s^{-1}$
H	3.46667	8.25688	1
N_0	$1 \cdot 10^{18}$	$1 \cdot 10^{18}$	cm^{-3}

Table 3.5: Default coefficients of Auger recombination model

Band-to-Band Tunneling It is a generation-recombination process and it occurs when an electron passes through the band gap from the valence band to the conduction band without the assistance of traps. There are several models that represent this phenomenon. In this case the **Hurkx model** is used. Its equation is:

$$R_{net}^{BB} = A \cdot D \cdot \left(\frac{F}{1V/cm} \right)^P e^{-\frac{BE_g(T)^{\frac{3}{2}}}{E_g(300K)^{\frac{3}{2}} F}} \tag{3.12}$$

where:

$$D = \frac{np - n_{i,eff}^2}{(n + n_{i,eff})(p + n_{i,eff})} (1 - |\alpha|) + \alpha \tag{3.13}$$

when $\alpha = -1$ D is negative and there is only a generation, whereas $\alpha = 1$ D is positive there is only a recombination; in the case $\alpha = 0$ there is a generation-recombination process. By default $\alpha = 0$.
The unit of coefficients are: $cm^{-3}s^{-1}$ for A and V/cm for B; P and α are dimensionless.

3.1.3 Mechanical stress models

Mechanical distortion of semiconductor microstructures results in a change in the band structure and carrier mobility. These effects are well known, and appropriate computations of the change in the strain-induced band structure are based on the deformation potential theory [15].
The calculation of mechanical stress is given by the combination of three models: the *Deformation Potential model*, the *Density of States model* and the *Piezoresistance Mobility model*.

Deformation Potential model For Silicon, Bir and Pikus [16] propose the following model in which three Δ_2 electron valleys, heavy-hole and light-hole are considered.

$$\begin{aligned} \Delta E_{C,i} &= \Xi_d \left(\varepsilon'_{11} + \varepsilon'_{22} + \varepsilon'_{33}\right) + \Xi_u \varepsilon'_{ii} \\ \Delta E_{V,i} &= a \left(\varepsilon'_{11} + \varepsilon'_{22} + \varepsilon'_{33}\right) \pm \delta E \\ \delta E &= \sqrt{\frac{b^2}{2}\left(\left(\varepsilon'_{11} - \varepsilon'_{22}\right)^2 + \left(\varepsilon'_{22} - \varepsilon'_{33}\right)^2 + \left(\varepsilon'_{11} - \varepsilon'_{33}\right)^2\right) + d^2\left(\varepsilon'^2_{12} + \varepsilon'^2_{13} + \varepsilon'^2_{23}\right)} \end{aligned} \tag{3.14}$$

where Ξ_d, Ξ_u, a, b, d are deformation potentials, i is the carrier band number and ε'_{ij} are the components of the strain tensor in the crystal coordinate system.
The equation written above corresponds to a simple form of linear deformation model. When there are ellipsoidal bands, the model could be expressed as:

$$\Delta E_i = \left[\Xi_d \bar{1} + \Xi_u \left\{\vec{e_i} \vec{e_i^T}\right\}\right] : \bar{\varepsilon'} \tag{3.15}$$

where:

- Ξ_d and Ξ_u are linear deformation potentials.
- $\bar{1}$ is a unit 3x3 matrix.
- $\bar{\varepsilon'}$ is the strain tensor in the crystal coordinate system.
- $\vec{e_i}$ is the unit vector parallel to the k-vector of the main axis of the ellipsoidal valley i.

The $:$ represents the dyadic product that is defined as $\bar{a} : \bar{b} = \sum_i \sum_j a_{ij} b_{ij}$.
Using a degenerate $k \cdot p$ theory at the zone boundary X-point, it is derived an additional shear term for the Δ_2 electron valleys [10]:

$$\Delta E_c = \Xi_d \left(\varepsilon'_{11} + \varepsilon'_{22} + \varepsilon'_{33}\right) + \Xi_u \varepsilon'_{ii} + \begin{cases} \dfrac{-\Delta}{4}\eta_i^2 & |\eta_i| \leq 1 \\ -\left(2|\eta_i| - 1\right)\dfrac{\Delta}{4} & |\eta_i| > 1 \end{cases} \tag{3.16}$$

where:

- $\eta_i = \dfrac{4\Xi_{u'}\varepsilon'_{jk}}{\Delta}$ is a dimensionless off-diagonal strain with $j \neq k \neq i$.
- ε'_{jk} is a shear strain component.
- Δ is the band separation between the two lowest conduction bands.
- $\Xi_{u'}$ is the deformation potential responsible for the band-splitting of the two lowest conduction bands.

Density of states model The effect of the strain leads to a change of the effective mass for both electrons and holes, and, consequently, an alteration of conduction band and valence band effective density-of-states(DOS).
As regard as the conduction band in silicon, it can be approximated as three Δ_2 valleys. Without stress, the DOS of each valley is:

$$N_{C,i} = \frac{N_C}{3}, \quad i = 1, 3 \tag{3.17}$$

where N_c is given by:

$$N_C\left(m_n, T_n\right) = 2.5094 \cdot 10^{19} \left(\frac{m_n}{m_0}\right)^{\frac{3}{2}} \left(\frac{T_n}{300K}\right)^{\frac{3}{2}} cm^{-3} \tag{3.18}$$

Applying a stress, there is a relative shift of the energy $\Delta E_{C,i}$ that is different for each Δ_2 valleys. Moreover, the presence of shear stress leads to large effective mass change for electrons. The stress-induced change of the effective DOS for each Δ_2-valley can be written as[10]:

$$N_{C,i} = \sqrt{\left(\frac{m_{t1,i}}{m_t}\right)\left(\frac{m_{t2,i}}{m_t}\right)\left(\frac{m_{1,i}}{m_1}\right)} \cdot \left(\frac{N_C}{3}\right) \tag{3.19}$$

Accounting for the change of the stress-induced valley energy $\Delta E_{C,i}$ and the carrier redistribution between valleys, the strain-dependent conduction-band effective DOS can be derived for Boltzmann statistics[10]:

$$N'_C = \gamma \cdot N_C \tag{3.20}$$

where:

$$\gamma = \frac{1}{N_C} \sum_{i=3}^{3} N_{C,i} e^{\dfrac{\Delta E_{C,min} - \Delta E_{C,i}}{kT_n}} \tag{3.21}$$

and:

$$\Delta E_{C,min} = min\left(\Delta E_{C,i}\right) \tag{3.22}$$

The total hole effective DOS mass for arbitrary strain in silicon is:

$$m'_p(T) = \left[m_{cc,1}^{3/2} e^{-\frac{E_3 - E_1}{kT}} + m_{cc,2}^{3/2} e^{-\frac{E_3 - E_2}{kT}} + m_{cc,3}^{3/2} \right]^{2/3} \tag{3.23}$$

where E_1, E_2 and E_3 are the ordered band edges for each of the three valence valleys, and $m_{cc,1}$, $m_{cc,2}$ and $m_{cc,3}$ are the carrier-concentration masses for each of the valleys given by:

$$m_{cc}^{3/2}(T) = \frac{2}{\sqrt{\pi}} (kT)^{-3/2} \int_0^\infty dE m_{DOS}^{3/2}(E) \sqrt{E} e^{-E/(kT)} \tag{3.24}$$

m_{DOS} is the energy-dependent DOS mass of each valley and it is equal to:

$$m_{DOS}^{3/2}(E) = \frac{\sqrt{2}\pi^2\hbar^3}{\sqrt{E}} \frac{1}{(2\pi)^3} \int_0^{2\pi} d\varphi \int_0^{\pi} d\Theta \sin(\Theta) \left[\left| \frac{\delta k}{\delta E} \right| k^2 \right]_{\varphi,\Theta,E} \tag{3.25}$$

The strain-dependent valence-band effective DOS is then calculated from[10]:

$$N'_V = \left(\frac{m'_p}{m_p} \right)^{\frac{3}{2}} N_V \tag{3.26}$$

Piezoresistance Mobility model The model is based on an expansion of the mobility enhancement tensor in terms of stress. The electron or hole mobility enhancement tensor follow the equation below:

$$\frac{\mu_{ij}}{\mu_0} = \delta_{ij} + \sum_{k=1}^{3} \sum_{l=1}^{3} \Pi_{ijkl} \sigma_{kl} + \sum_{k=1}^{3} \sum_{l=1}^{3} \sum_{m=1}^{3} \sum_{n=1}^{3} \Pi_{ijklmn} \sigma_{kl} \sigma_{mn} \tag{3.27}$$

where:

- μ_{ij} is a component of the electron or hole stress-dependent mobility tensor.
- μ_0 is the isotropic mobility without stress.
- δ_{ij} is the Kronecker delta function.
- σ_{kl} is a component of the stress tensor.
- Π_{ijkl} is a component of the first-order electron or hole piezoconductance tensor.
- Π_{ijklmn} is a component of the second-order electron or hole piezoconductance tensor.

The temperature and doping dependency of the piezoresistance coefficients is obtained by combining the following two equation[17]:

$$\pi_{ij} = -\Pi_{ij} \qquad \leftrightarrow \qquad \Pi_{ij} = -\pi_{ij} \tag{3.28}$$

$$\pi_{ijk} = -\Pi_{ijk} + \Pi_{ij}\Pi_{ik} \qquad \leftrightarrow \qquad \Pi_{ijk} = -\pi_{ijk} + \pi_{ij}\pi_{ik} \tag{3.29}$$

with these two equations[18]:

$$\begin{aligned} \Pi_{ij}(N,T) &= P_1(N,T)\,\Pi_{ij}(0,300K) \\ \Pi_{ijk}(N,T) &= P_2(N,T)\,\Pi_{ijk}(0,300K) \end{aligned} \tag{3.30}$$

- π_{ij} and π_{ijk} are components of the first-order and second-order piezoresistance tensors, respectively.
- $Pi_{ij}(0,300K)$ and $Pi_{ijk}(0,300K)$ are piezoconductance coefficients for low-doped silicon at 300 K.
- $P_1(N,T)$ and $P_2(N,T)$ are doping factors given by:

$$P_1(N,T) = \left(\frac{300K}{T}\right)\frac{F_{-1}(\eta)}{F_0(\eta)}$$

$$P_2(N,T) = \left(\frac{300K}{T}\right)^2\frac{F_{-2}(\eta)}{F_0(\eta)}$$

  $F_r(\eta)$ is a Fermi-Dirac integral of order "r" and η is the Fermi energy measured from the band edge in units of kT ($\eta_n = (E_{F,n} - E_C)/kT$ and $\eta_p = (E_V - E_{F,p})/kT$).

The mobility enhancement factor γ is applied to each individual mobility component. This factor is equal to:

$$\gamma = 1 + P_1(N,T)\frac{\Delta\mu_{low}}{\mu_{low,0}} \tag{3.31}$$

In high electric field, the mobility along the main directions is proportional to the saturation velocity. The stress-dependent saturation velocity is modeled in this way:

$$v_{sat,i} = v_{sat,0}\cdot\frac{1+\alpha\cdot t_i}{1+t_i} \tag{3.32}$$

where $v_{sat,0}$ is the stress-independent saturation velocity and α is saturation factor. By default $\alpha = 1$; for n-type finFET is 0.2, for p-type is 0.27.

3.2 n-type BULK finFET

An analytical study is performed on the n-type finFET previously realized with Sentaurus Process. The I_{ds}-V_{gs} trans-characteristic is obtained by computing the electrostatic

potential and the electron/hole density from the Poisson equation and electron and hole continuity equation.
The Poisson equation is:

$$\nabla \cdot \left(\varepsilon \nabla \phi + \vec{P}\right) = -q\left(p - n + N_D - N_A\right) - \rho_{trap} \tag{3.33}$$

While the continuity equations for carrier transport are:

$$\nabla \cdot \vec{J_n} = q\left(R_{net,n} - G_{net_n}\right) + q\frac{\delta n}{\delta t} \qquad -\nabla \cdot \vec{J_p} = q\left(R_{net,p} - G_{net_p}\right) + q\frac{\delta p}{\delta t} \tag{3.34}$$

The meaning of each parameter is:

- ε is electrical permittivity.
- $\vec{P}$ is the ferroelectric polarization.
- q is the elementary electronic charge.
- n and p are the electron and hole densities.
- N_D is the concentration of ionized donors.
- N_A is the concentration of ionized acceptors.
- $R_{net,n}$ and $R_{net,p}$ are the electron and hole net recombination rate.
- $G_{net,n}$ and $G_{net,p}$ are the electron and hole net generation rate.
- $\vec{J_n}$ is the electron current density.
- $\vec{J_p}$ is the hole current density.

These parameters derive from the combination of recombination, mobility and mechanical stress models.

3.2.1 Resulting data

After solving all equations and applying a voltage of 1 V between drain and source and a voltage of 1 V between gate and source, the resulting trans-characteristics for the unstressed and stressed n-type finFET are as follows in the figure 3.1.

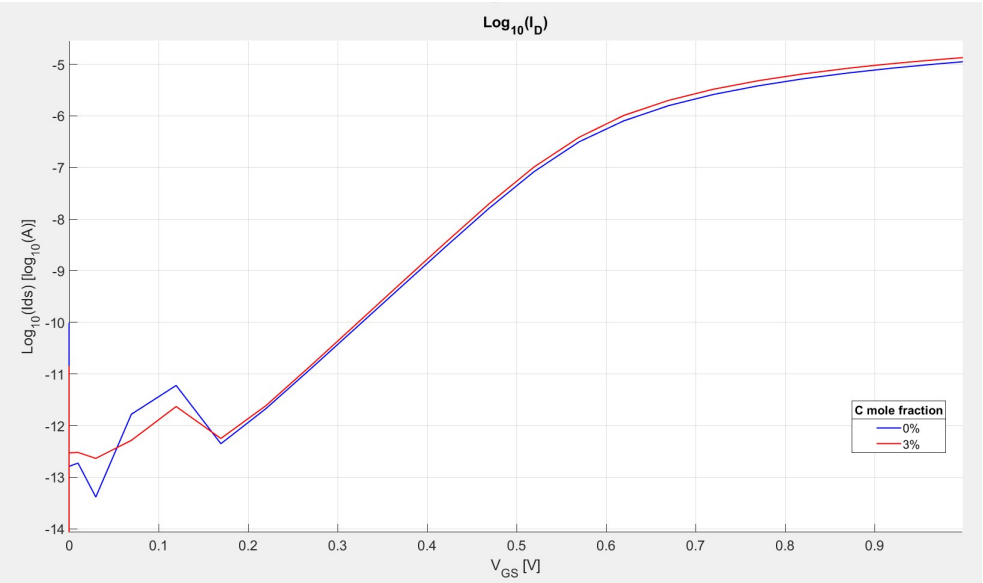


Figure 3.1: I_{ds}-V_{gs} characteristic of n-type finFET ($V_{ds} = 1V$, $V_{gs} = 1V$)

As it can be seen in figure 3.1, the I_{on} current calculated by SDevice at $V_{gs} = 1V$ is 11.24 μA for the case with only silicon and 13.52 μA for the case in which there is silicon carbide with a carbon mole fraction of 3%.
When there is a pure silicon (100% Si mole fraction), its density is about $5 \cdot 10^{22}$ $atoms/cm^3$[19]. Using a SiC with a carbon mole fraction of 3% means that the density of carbon is equal to the 3% of total density that is $0.03 \cdot 5 \cdot 10^{22}$ $atoms/cm^3 = 1.5 \cdot 10^{21}$ $atoms/cm^3$ and the density of Si corresponds to 97% of the total density ($4.85 \cdot 10^{22}$ $atoms/cm^3$). As explained in subsection 2.1.6 the introduction of SiC, instead of pure silicon, to made source and drain, generates a tensile stress on the channel due to the mismatch between the SiC and Si lattice constant. In figure 3.2 the difference type of stress is reported:

- the central part is the stress in the channel;
- the parts in which the green line has a drop are the S/D extensions;
- the side parts are the source and drain regions.

It can be observed that without lattice constant mismatch there is a constant stress of about $-1 \cdot 10^7$ Pa; with the mismatch, stress is no longer constant and changes from about $1 \cdot 10^9$ Pa in S/D region to about $-1 \cdot 10^9$ Pa in S/D extension region. The minus sign indicates the the stress is tensile, otherwise it is compressive.

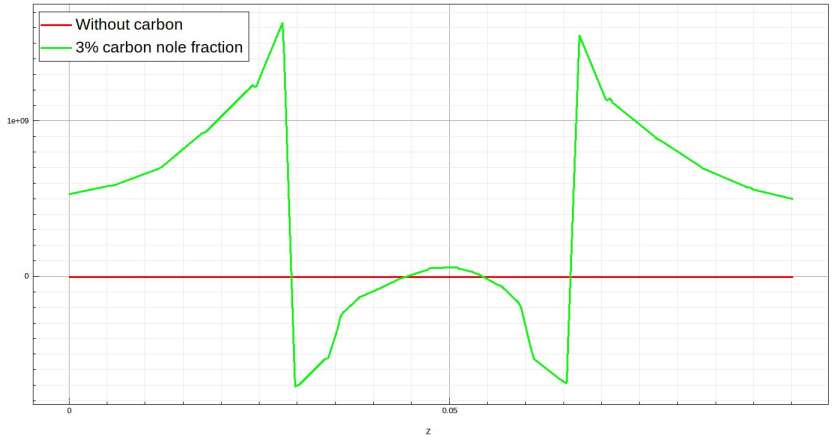


Figure 3.2: Stress along the channel: without SiC (*red line*), with SiC (*green line*)

The purpose of modifying the stress is that it leads to an increment in electron mobility in the channel. SDevice derives the electron mobility from the models described in section 3.1.

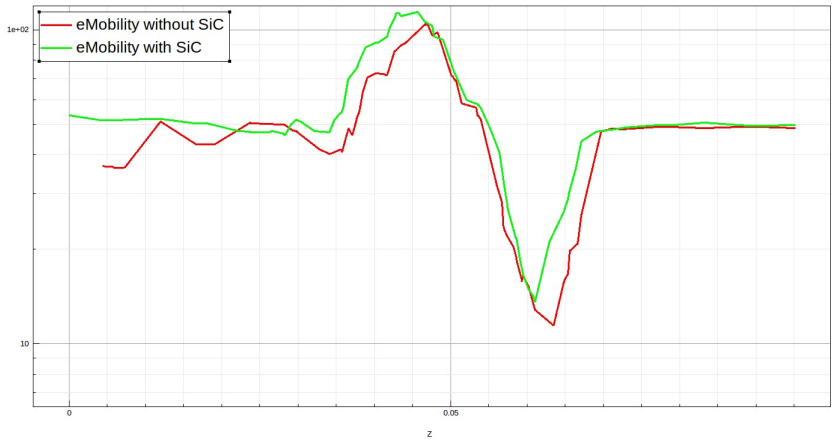


Figure 3.3: electron mobility along the channel: without SiC (*red line*), with SiC (*green line*)

Figure 3.3 shows an average increase in mobility of about 20% in the case with tensile stress in the channel. Indeed the I_{on} current is increased of 2.28 μA that is the 20.28% of 11.24 μA. This result is supported by the equation:

$$I_{ds,n} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{3.35}$$

where:

- μ_n is the electron mobility.
- C_{ox} is the gate capacitance and is given by the ratio between the permittivity ε_{ox} and the thickness t_{ox} of the silicon dioxide $\left(\frac{\varepsilon_{ox}}{t_{ox}}\right)$

- W is the width of the fin.
- L is the length of the fin.
- V_{gs} is the voltage between gate and source.
- V_{th} is the threshold voltage.

The resulting data are elaborated by Sentaurus Inspect in order to compute the threshold voltage (V_{th}) and the subthreshold swing (SS) for both cases. The SS indicates how easily a transistor can be turned off, in particular it determines how many Volts the gate voltage must vary to decrease/increase the subthreshold current ($I_{sub,V_{th}}$) by one order of magnitude. It is measure in mV/dec. The SS is given by:

$$SS = 2.3 \cdot V_T m \tag{3.36}$$

where:

- V_T is the thermal voltage and it is equal to: $\left(\frac{kT}{q}\right)$; k is the Boltzmann constant, T is the temperature and q is the charge of an electron.
- $m = 1 + \frac{C_{dep}}{C_{ox}}$. C_{dep} is the depletion region capacitance.

So, the minimum reachable value for SS is 59.8 mV/dec when m=1.
In the table 3.6 V_{th} and SS are reported for both cases:

C mole fraction	V_{th} **(V)**	**SS (*mV/dec*)**
0.00	0.684	63.65
0.03	0.671	63.02

Table 3.6: V_{th} and SS of unstressed and stressed n-type bulk finFETs

3.3 p-type BULK finFET

Considering the equations 3.33 and 3.34 and the models of the section 3.1, SDevice derives the I_{ds}-V_{gs} characteristics for each type of unstressed/stressed p-finFET. In particular the analysis is focused on how the threshold voltage and the Subthreshold Swing vary according to the variation of Germanium concentration and V_{ds}.
The range of V_{ds} taken into account is [0,-1] V, while the germanium mole fractions considered are:

- 0% (pure silicon - Si);
- 75% (silicon germanium - $Si_{0.25}Ge_{0.75}$);
- 100% (germanium - Ge).

3.3.1 Resulting data

Firstly, the trans-characteristic for the different three conditions of germanium concentration is obtained with $V_{ds} = -1V$ and $V_{gs} = -1V$ (Figure 3.4).

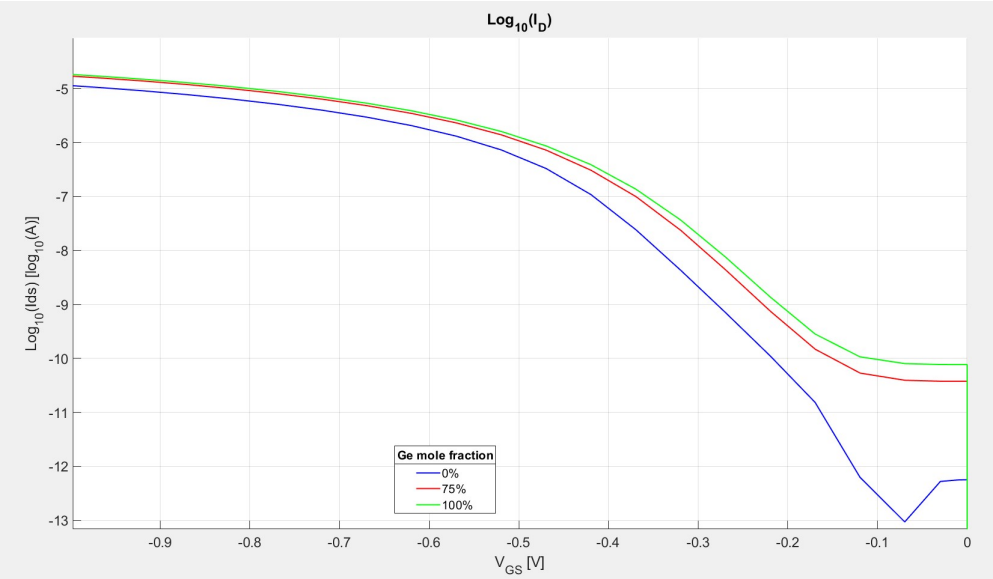


Figure 3.4: I_{ds}-V_{gs} characteristic of p-type finFET ($V_{ds} = -1V$, $V_{gs} = -1V$)

The I_{on} currents obtained are 11.39 μA for pure silicon case, 17.07 μA for $Si_{0.25}Ge_{0.75}$ case and 18.32 μA for Ge case.
In $Si_{0.25}Ge_{0.75}$ the silicon germanium density is the total silicon density ($5 \cdot 10^{22}$ $atoms/cm^3$) minus the 75% of $0.58 \cdot 10^{22}$ [20] that is $4.565 \cdot 10^{22}$ $atoms/cm^3$. In Ge, the density is $4.42 \cdot 10^{22}$ $atoms/cm^3$ [20].
These variation germanium concentration for source/drain material generate an increase/decrease in channel stress due to the the lattice constant mismatch (subsection 2.2.2). In figure 3.5 is represented how the stress changes according to Ge mole fraction:

- the central part illustrates stress in the channel;
- the side parts illustrate the source and drain regions.

Without lattice constant mismatch between channel and S/D region, the stress is constant and it is about $-1 \cdot 10^8$ Pa. With the changing of germanium mole fraction, there is a lattice mismatch that increments with the increase in Ge mole fraction. This results in a compressive channel stress that has a peak of about $4 \cdot 10^8$ Pa (100% mole fraction), while in S/D regions there is a stress of about $-2 \cdot 10^9$ Pa.

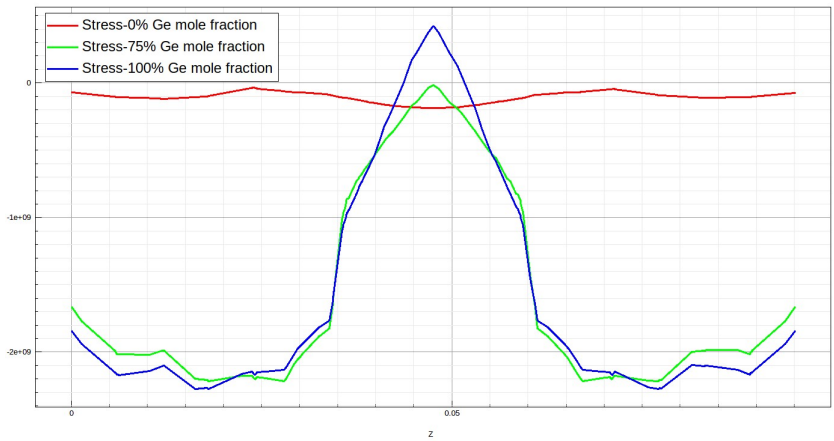


Figure 3.5: Stress along the channel: 0% Ge (*red line*), 75% Ge (*green line*), 100% Ge (*blue line*)

The compressive stress in the channel causes an increase in hole mobility.

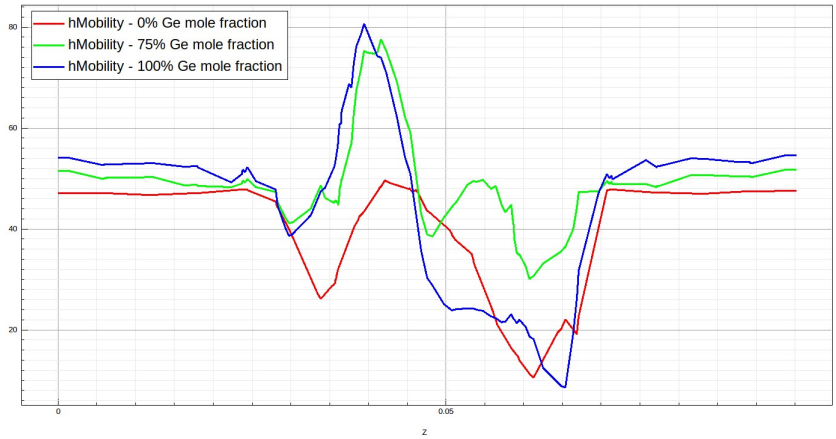


Figure 3.6: hole mobility along the channel: 0% Ge (*red line*), 75% Ge (*green line*), 100% Ge (*blue line*)

As it can be observed in figure 3.6, there is an average increase in hole mobility respect to unstressed case:

- of about 46% for $Si_{0.25}Ge_{0.75}$ device;
- of about 63% for Ge device.

These results are confirmed by the increment of the I_{on} currents: in one case the current increases of 5.68 μA that is approximately 49% of 11.39 μA; in the other case it increase of 6.93 μA that is 60.8% of 11.39 μA.
All is supported by the formula:

$$I_{ds,p} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(V_{gs} - V_{th}\right)^2 \tag{3.37}$$

where μ_p is the hole mobility.
These data are computed by Sentaurus Inspect to obtain V_{th} and SS for the three cases. In table 3.7 the value calculated are summarized. Increasing the Ge concentration the

Ge mole fraction	V_{th} **(V)**	**SS** (mV/dec)
0.00	-0.596	62.88
0.75	-0.571	66.68
1.00	-0.565	70.02

Table 3.7: V_{th} and SS of unstressed and stressed p-type bulk finFETs

V_{th} decreases in absolute value and the subthreshold swing gets worse. Another analysis is performed by varying the V_{ds} from 0 to -1 V and keeping constant V_{gs} at 1 V. The data generated by SDevice are then taken and reworked by MS Excel to understand how the threshold voltage and the subthreshold swing change as the V_{ds} varies in case with only silicon and in the case there is silicon germanium.
The V_{th}, as seen above, decreases in absolute value with SiGe; but this difference is less evident respect to the structure with only silicon when there are low voltages for V_{ds} (Figure 3.7).

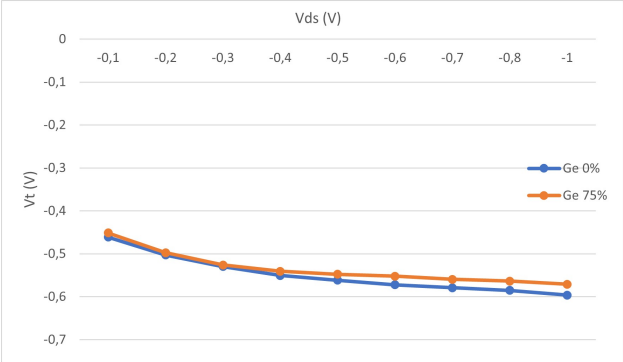


Figure 3.7: Variation of V_{th} as V_{ds} varies

As regard as the subthreshold swing (SS), the behavior is not similar in the two structures:

- it has a constant value of about 63 mV/dec for the unstressed device (blue line in figure 3.8);
- it has a value ranging between 62 mV/dec and 66 mV/dec for the stressed device and it increases as V_{ds} increases (orange line in figure 3.8).

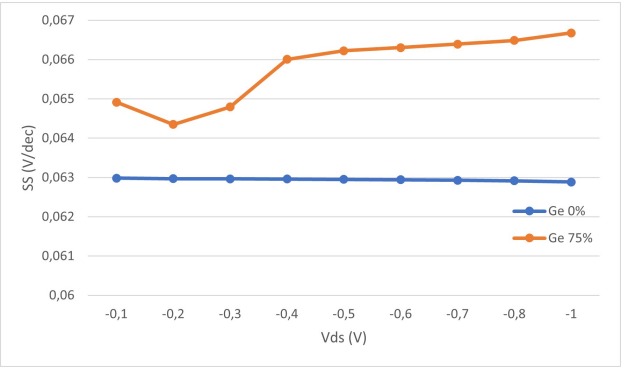


Figure 3.8: Variation of SS as V_{ds} varies

Finally, it can be observed that the absolute value of the I_{on} currents for both cases increase as V_{ds} increases and, at the same time, the difference between the two currents increases (Figure 3.9).

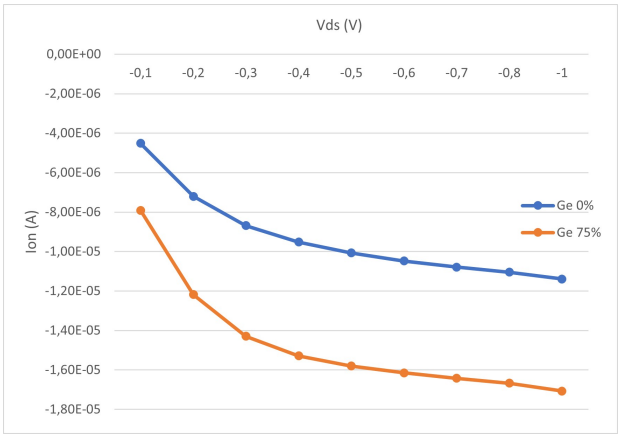


Figure 3.9: Variation of I_{on} as V_{ds} varies

The results obtained are shown in the table 3.8.

V_{ds} $(\boldsymbol{V})$	**Ge mole fraction**	V_{th} $(\boldsymbol{V})$	**SS** $(\boldsymbol{mV/dec})$	I_{on} (μA)
-0.1	0	-0.46123	62.983	-4.51
	0.75	-0.45127	64.913	-7.91
-0.2	0	-0.50296	62.970	-7.20
	0.75	-0.49765	64.349	-12.18
-0.3	0	-0.52961	62.964	-8.69
	0.75	-0.52601	64.794	-14.29
-0.4	0	-0.55067	62.959	-9.52
	0.75	-0.5406	66.006	-15.28
-0.5	0	-0.56144	62.952	-10.06
	0.75	-0.54761	66.223	-15.80
-0.6	0	-0.57208	62.943	-10.47
	0.75	-0.55220	66.305	-16.14
-0.7	0	-0.57923	62.931	-10.79
	0.75	-0.55939	66.392	-16.42
-0.8	0	-0.58413	62.914	-11.04
	0.75	-0.56372	66.489	-16.67
-1.0	0	-0.59639	62.884	-11.39
	0.75	-0.57082	66.679	-17.07

Table 3.8: Variation of V_{th}, SS, I_{on} as V_{ds} varies for unstressed and stressed p-type finFET

CHAPTER 4

Fabrication process simulation of Nanosheet GAA-FET

Formally, there are two types of Gate-All-Around FETs (GAAFETs): the typical GAAFETs called nanowires which have "thin" fins and the multi-bridge channel FETs (MBCFETs) called nanosheet which use "thicker" fins[21]. In both cases, the gate material surrounds the channel region on all sides: the name of this transistors derives from this type of structure.
The first GAAFETs are shown in 1988, so the main technology advantages are well known[21]. The structure of this type of transistor allows designers to optimize it with precision for high performance or low power consumption by adjusting channel width (effective width, W_{eff})[21]; larger sheets allow higher performances with higher power, while narrower sheets reduce the power consumption and the performances. To do something similar with finFETs, the engineers must use additional fins in order to improve the performances[21]. Moreover, GAAFET adjustments allow for an higher transistor density because different transistors can be used for several purposes.
As for MOSFETs and finFETs, also for GAAFETs there is a distinction according to the type of doping: a n-type GAAFET has n-type doped (e.g. Phosphorus) source and drain and the channel is doped with a p-type dopant (e.g. Boron); while in the p-type GAAFET is the opposite respect the previous case. As is done for the finFET, also for the two types of GAAFET an improvement can be obtained by using a SiC (n-type finFET) or a SiGe (p-type finFET) source/drain instead of a silicon one. This solution increases mobility of electrons and holes.

4.1 n-type Nanosheet GAAFET

The fabrication of p-type nanosheet (NS) GAAFET consists of several steps very similar to the finFET. Three type of GAAFET are taken into account:

1. A bulk GAAFET realized without Shallow Trench Insulation (STI)technique.

2. A bulk GAAFET made with STI.

3. A SOI GAAFET.

All these three types have a channel length of 14 nm; three sheets with width of 22 nm and height of 7 nm; a Phosphorus concentration of $2 \cdot 10^{21} cm^{-3}$ for source and drain; a Boron concentration of $1 \cdot 10^{15} cm^{-3}$ for the channel and one of $2 \cdot 10^{18} cm^{-3}$ for the substrate.

4.1.1 P-well implantation

A boron dose of $1 \cdot 10^{14}$ is implanted on a bulk wafer with an energy of 30 keV and a RTA is performed at 1000°C. As shown in figure 4.1, the variation in hue from blue to red represents the increase in the concentration of boron.

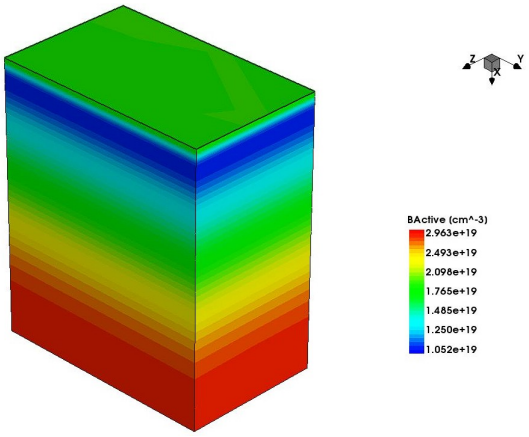


Figure 4.1: p-well implantation

In SOI version, after the implantation, a buried oxide layer (BOX) is grown through a wet thermal oxidation (figure 4.2).

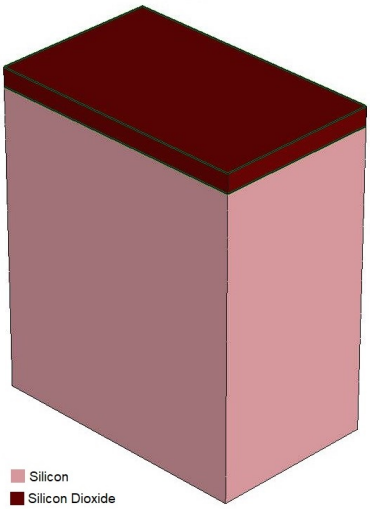
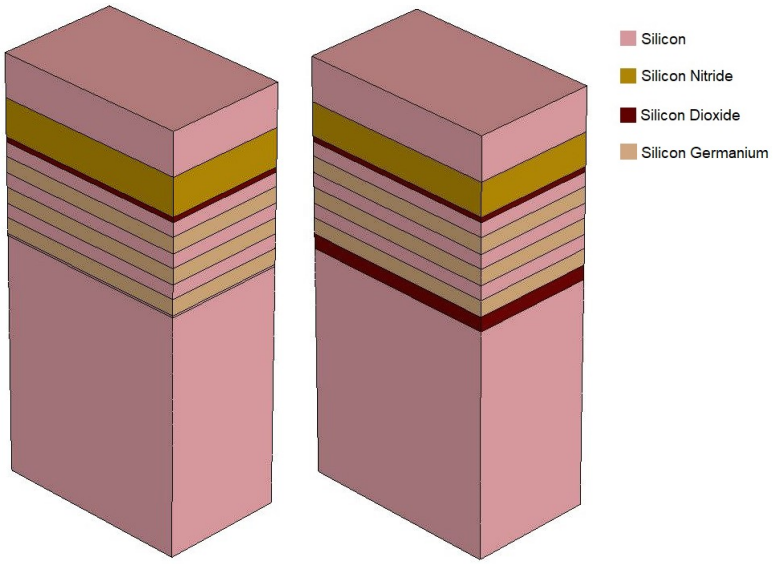


Figure 4.2: Buried oxide (*brown*)

4.1.2 Modeling of Si-SiGe layers using the SIT technique

The process to realized three layers of silicon is very similar to the steps made in subsection 2.1.2. As for finFET, it consists of 6 steps:

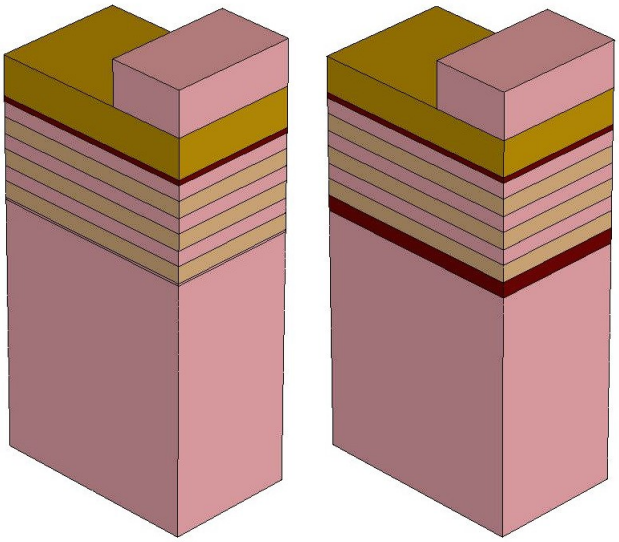
1. An alternating sequence of layers of silicon and silicon germanium (three layers of 8nm SiGe and three of 7nm Si) is deposited on the silicon substrate (or the box in case SOI) and then it is covered with 2.5 nm of SiO_2, 19 nm of Si_3N_4 and 21.5 nm of Si. The three layers are called **Buffer Oxide**, **Transfer Layer** and **Mandrel Layer** respectively (figure 4.3).



(a) (b)

Figure 4.3: Mandrel Layer (Silicon), Transfer Layer (Nitride), Buffer Oxide (SiO_2): *(a) bulk (b)SOI*

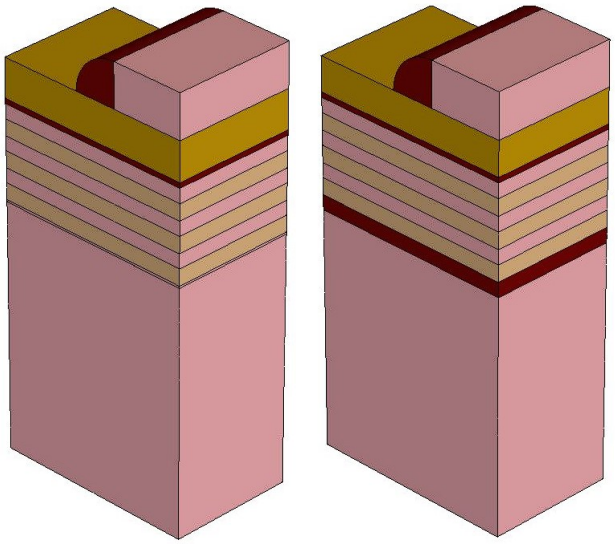
2. The mandrel layer is modeled by making etching using mask and photolithography (figure 4.4).



(a) (b)

Figure 4.4: Mandrel: *(a) bulk (b)SOI*

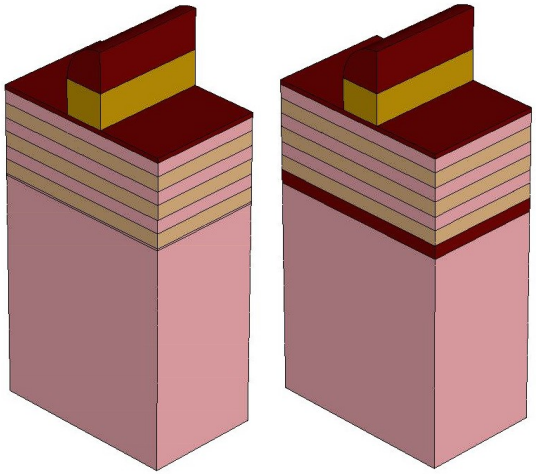
3. The silicon dioxide spacer are realized by performing an anisotropic etching and subsequently an isotropic overetch (figure 4.5).



(a) (b)

Figure 4.5: SiO_2 spacer: *(a) bulk (b)SOI*

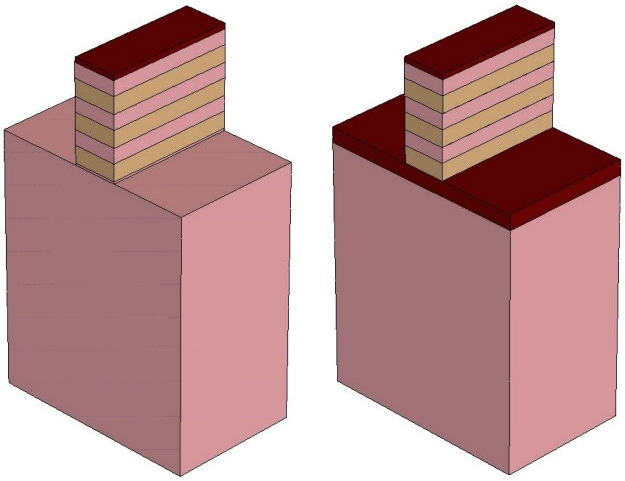
4. The mandrel is etched. The spacer becomes the hard mask for etching the transfer layer and, in turn, the residual nitride of the transfer layer becomes the hard mask for etching the sheets (figure 4.6).



(a) (b)

Figure 4.6: Mandrel and nitride etching: *(a) bulk (b)SOI*

5. The nitride hard mask is key element to form the Si-SiGe sheets. The part of silicon and silicon germanium not covered by Si_3N_4 is etched (figure 4.7).



(a) (b)

Figure 4.7: Sheets formation: *(a) bulk (b)SOI*

In case in which the bulk GAAFET has a STI, another etching process involves the two sides of the sheets (figure 4.8).

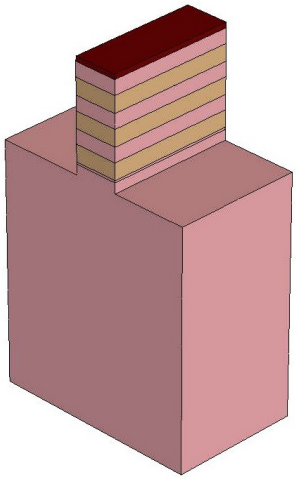
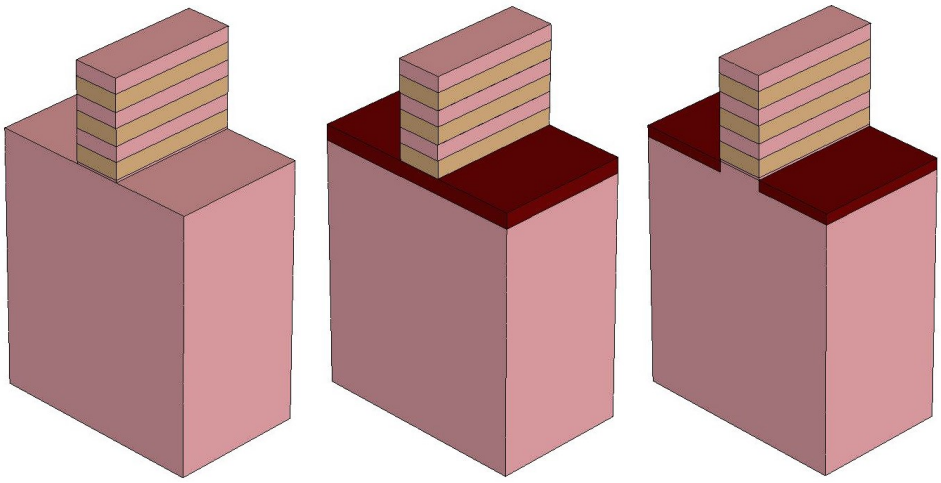


Figure 4.8: Etching of silicon substrate

6. Finally, the remaining oxide is etched (figure 4.9 (a) and (b)). In the case there is the STI, before etching the oxide, the part of the substrate, where the silicon was previously removed, is filled with silicon dioxide and the SiO_2 is removed by performing CMP (figure 4.9 (c)).



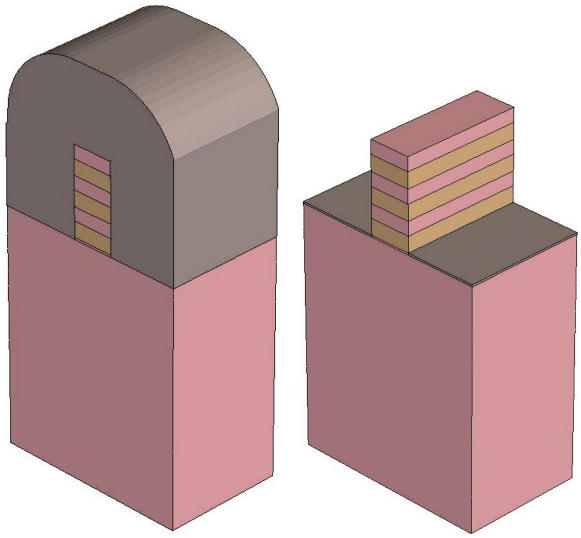
(a) (b) (c)

Figure 4.9: Sheets after removing oxide: *(a) bulk (b)SOI (c) bulk with STI*

The Shallow Trench Insulation is a necessary technique to prevent current leakage. It consists of: etching the exposed part of silicon forming a trench; fill the trench with silicon dioxide; removal of excess oxide by chemical mechanical polishing.
The following steps to made a n-type bulk GAAFET with and without STI and a n-type SOI GAAFET are the same; so, only steps of bulk nGAAFET without STI are taken into account.

4.1.3 TEOS CMP and thermal oxidation

TEOS (grey in figure 4.10) is deposited on all structure and then it is etched by CMP process (figure 4.10 (b)).



(a) (b)

Figure 4.10: TEOS *(grey)*: (a) Deposition (b) CMP

The Si-SiGe layers are oxidized by exploiting dry thermal oxidation (figure 4.11).

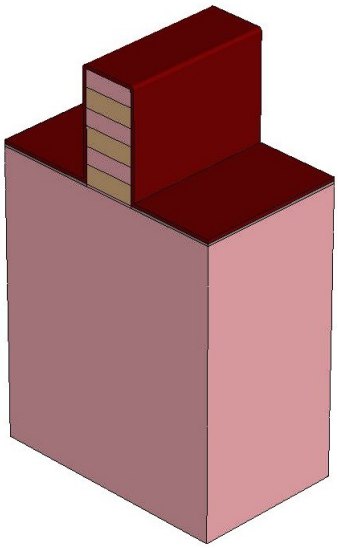


Figure 4.11: Thermal Oxidation

A 15 Å SiO_2 layer is formed on the Si-SiGe layers.

4.1.4 Dummy gate

The role of dummy gate is to mark the region where there will be the channel, and, as already seen in subsection 2.1.5, to favor the realization of source/drain extensions and the S/D epitaxial growth.
A layer of polysilicon is deposited on Si-SiGe layers and then removed by means of photolithogaphy only where it doesn't cover the central part of the layers (figure 4.12).

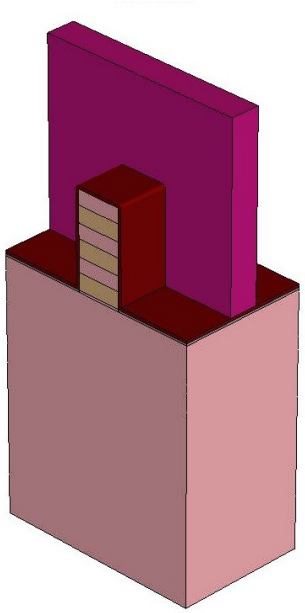


Figure 4.12: Dummy gate - Polysilicon (*violet*)

A thin oxide layer (2 nm) is made on both sides of the dummy gate. Also in this case, it is called oxide wall (figure 4.13).

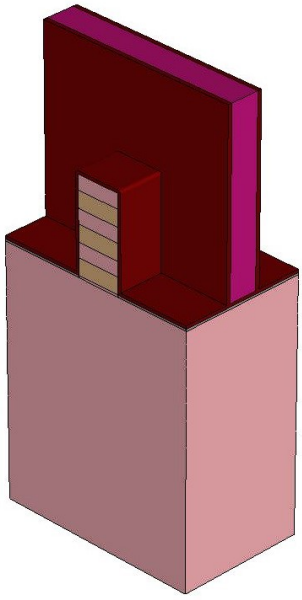


Figure 4.13: Oxide walls

The S/D extensions are realized by covering the dummy gate with a thick layer

of photoresist and implanting a $1 \cdot 10^9\ cm^{-2}$ dose of phosphorus with an energy of 4 keV and a tilt angle of 10 degrees. Subsequently a RTA is executed (1000°C 0.1s) to activate the dopant (figure 4.14).

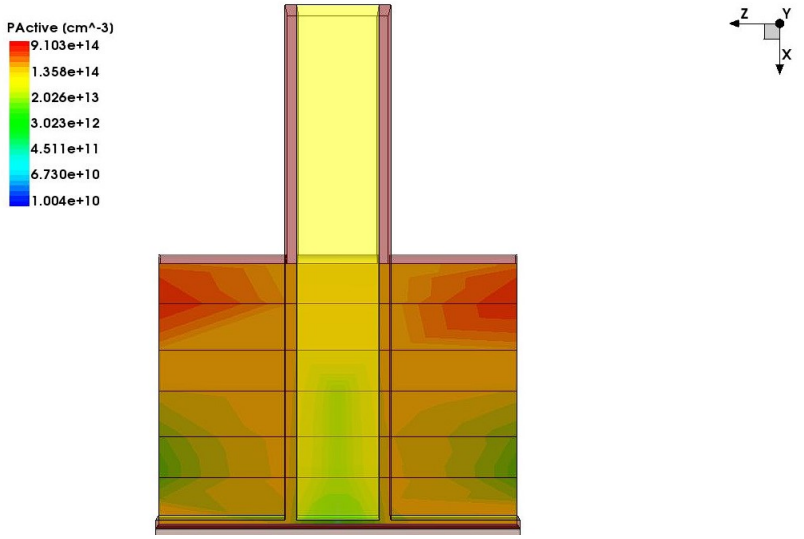


Figure 4.14: Phosphorous S/D extensions. Polysilicon and SiO_2 are in translucency

4.1.5 S/D creation

Si_3N_4 spacers are formed at the sides of wall in the following way: firstly, an isotropic deposition of nitride is made and then an anisotropic etching plus an isotropic overetching is performed (figure 4.15).

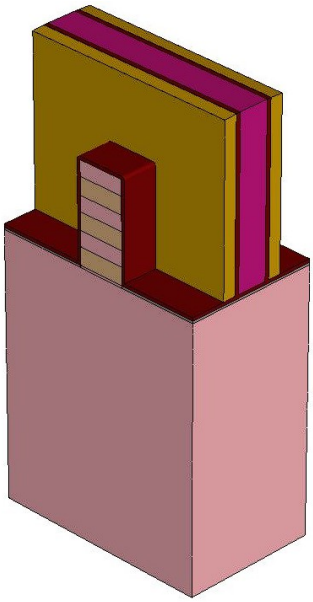


Figure 4.15: Si_3N_4 formation

Subsequently SiCN is used as hard mask to remove silicon dioxide: after having deposited the SiCN, only the part of the dummy gate is covered using photolithography and the exposed oxide is removed (figure 4.16).

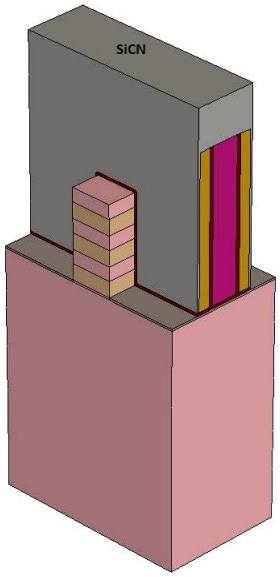


Figure 4.16: SiCN photolithography

Once the oxide is removed, an anisotropic etching is performed to also remove the exposed part of Si-SiGe layers. Furthermore, an isotropic etching on silicon germanium is exploited, forming grooves that are filled with silicon nitride and they are called inner spacer (figure 4.17).

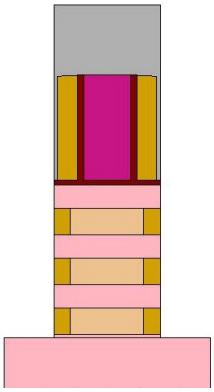
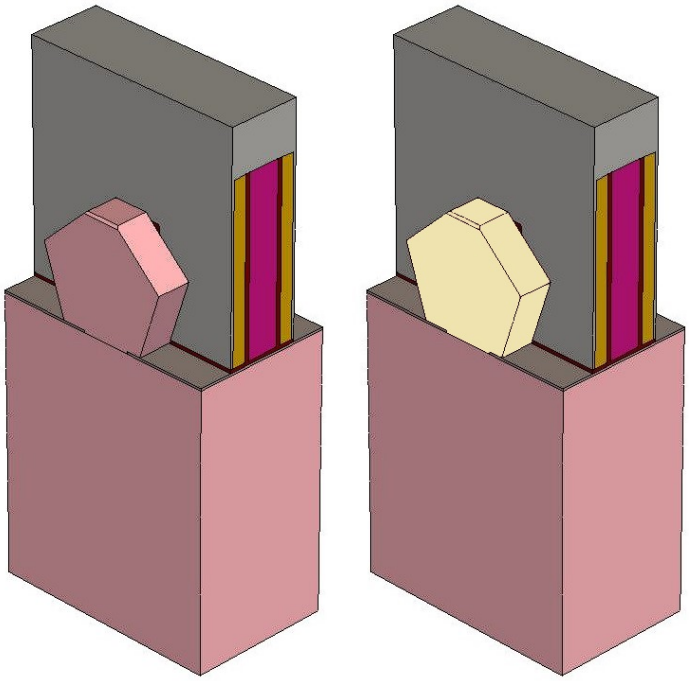


Figure 4.17: Inner spacers: cross section (*yellow part among the silicon*)

Inner spacer is crucial for reducing intrinsic capacitance and to improve dynamic performances[22].

Finally an epitaxial growth of n-doped($2 \cdot 10^{21} cm^{-3}$ of phosphorus) silicon is made to form source and drain. It can be possible to have silicon carbide instead of silicon for the reasons already explained in paragraph 2.1.6 (figure 4.18).



(a) (b)

Figure 4.18: S/D epitaxial growth: (a)n++ Silicon S/D (b) n++ SiC S/D

4.1.6 Silicidation and dummy gate removal

The SiCN is etched, the device is covered by titanium and then the silicidation process begins: titanium reacts with silicon and it gives a 1 nm layer of titanium silicide ($TiSi_2$). The unreacted titanium is removed (figure 4.19).

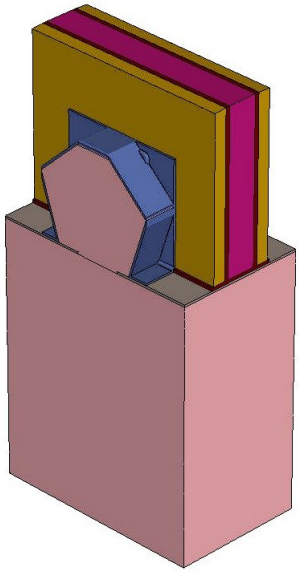


Figure 4.19: Silicidation - $TiSi_2$ (*lilac*)

The purpose of silicidation is already explained in subsection 2.1.7. The silicide materials have a resistivity comparable to the matal one (table 2.1).

The all structure is covered by PSG, and the surplus material is smoothed through CMP so that the portion of PSG above the dummy gate is removed (figure 4.20). Finally the dummy gate is eliminated: the polysilicon is etched using silicon dioxide as etch stop and, subsequently, also the SiO_2 covering the gate is etched and the SiGe layers are removed (figure 4.21).

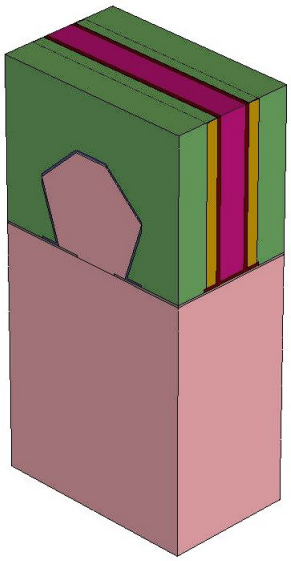


Figure 4.20: PSG(*green*) deposition and CMP

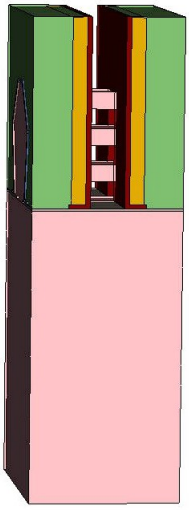


Figure 4.21: Dummy gate removal

4.1.7 Gate stack

A dry thermal oxidation of the exposed part of the sheets and a subsequent deposition of a thin layer (1 nm) of hafnium oxide (HfO_2) are performed to avoid dielectric breakdown and leakage current by quantum tunneling (figures 4.22 4.23).

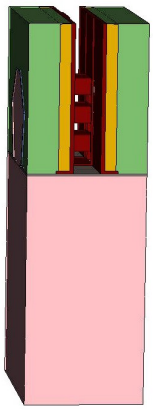


Figure 4.22: Gate thermal oxidation

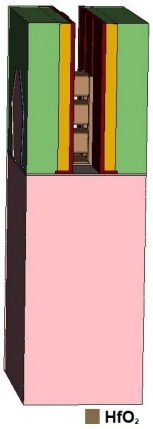


Figure 4.23: HfO_2 deposition

A stack is made exploiting the metal-interdiffusion technology (MIG). This stack is realized on the gate and it is formed by (figure 4.24):

- Two layers of insulating materials:
  - SiO_2;
  - HfO_2.
- Three layers of conductor materials:
  - 15$\mathring{A}$ of TiN;
  - 15$\mathring{A}$ of TaN;
  - 20$\mathring{A}$ of TiAl.

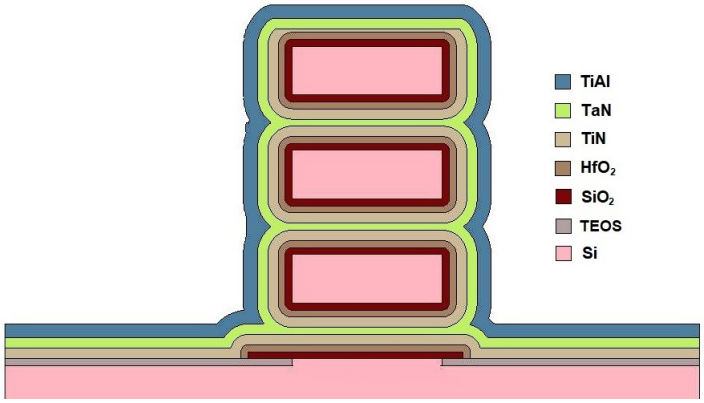


Figure 4.24: n-GAAFET Gate stack

The choice of TiAl is dictated by what has already been seen in the subsection 2.1.8.

4.1.8 Contacts

A thick layer of tungsten is placed on the stack and then it is smoothed by using CMP in such a way as to have the tungsten at a lower height of 1 nm than that of the PSG (figure 4.25). The 1 nm difference in height is compensated with nitride: a thick layer of Si_3N_4 is deposited and then etched by exploiting CMP (figure 4.26).

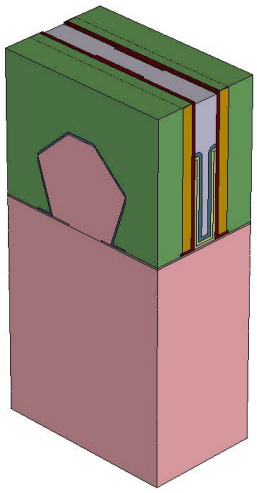


Figure 4.25: Tungsten(*grey*) deposition on gate stack

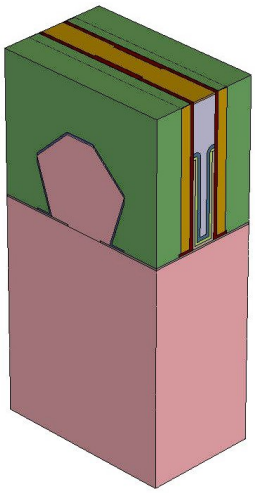
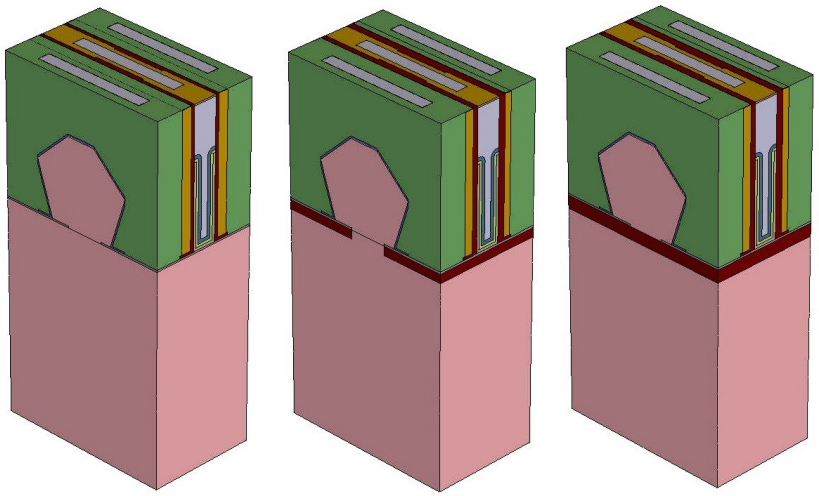


Figure 4.26: Si_3N_4 deposition on tungsten

Finally, the S/D contacts and gate contact are realized:

- the S/D contacts are formed by creating the cavity in the PSG in correspondence of source and drain by means of the SAC technique. Then the cavity is filled with tungsten.
- the gate contacts are made with photolithography and etching of the nitride and, finally, with W deposition and etching through CMP.

All three types of n-type NS GAAFET (bulk, bulk with STI, SOI) are shown in figure 4.27.



(a) (b) (c)

Figure 4.27: n-type nanosheet GAAFET: *(a) bulk (b) bulk with STI (c) SOI*

4.2 p-type Nanosheet GAAFET

The steps to fabricate a p-type NS GAAFET is very similar to the n-type. As for n-type GAAFET, three types are considered: bulk, bulk with STI and SOI. The main differences respect to the n-type case are:

- type of dopant for source/drain;
- type of dopant for the channel and the substrate;
- the use of silicon germanium instead of silicon carbide as stressed material.

The dimensions of the considered p-type GAAFETs are:

- 14 nm for channel length;
- 22 nm for sheet width;
- 7 nm for sheet height.

As regard as the doping concentration, the source and drain have a Boron concentration of $2 \cdot 10^{21} cm^{-3}$; the channel has a Phosphorus concentration of $1 \cdot 10^{15} cm^{-3}$; the substrate has a Phosphorus concentration of $2 \cdot 10^{18} cm^{-3}$.

4.2.1 N-well implantation

A 30 keV implantation of phosphorus with a dose of $1 \cdot 10^{12} cm{-}3$ is performed and a subsequent RTA is made at 1000°C for 1s. In figure 4.28, the increase in concentration of phosphorus is indicated by the variation of hue from blue to red.

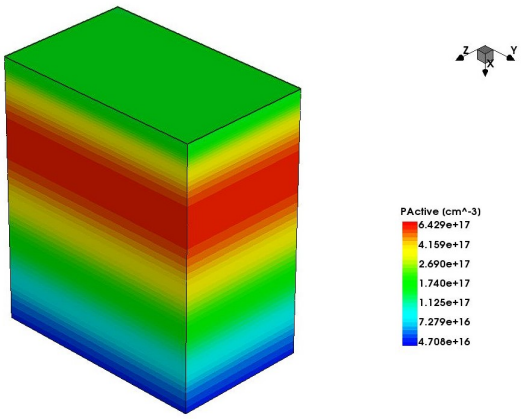


Figure 4.28: p-well implantation

In the following steps it proceeds as in the case of the n-GAAFET.

1. A thick layer of BOX is grown by using wet thermal oxidation (only SOI case).

2. Modeling of Si-SiGe layers through SIT technique (3 layers of Si 7 nm thick and 3 layers of SiGe 8 nm thick). In bulk with STI case, trenches are made at the sides of layers and the they are filled with SiO_2.

3. TEOS deposition and subsequent etching using CMP.

4. Dry thermal oxidation of the Si-SiGe layers.

5. Dummy gate and oxide walls formation.

4.2.2 S/D creation

The dummy gate is covered with photoresist and then the S/D extensions are realized: a $1 \cdot 10^{10}$ dose of boron is implanted with an energy of 6 keV and a 10 degrees tilt angle. A RTA (1000°C 0.1 s) is performed to activate the dopant (figure 4.29).

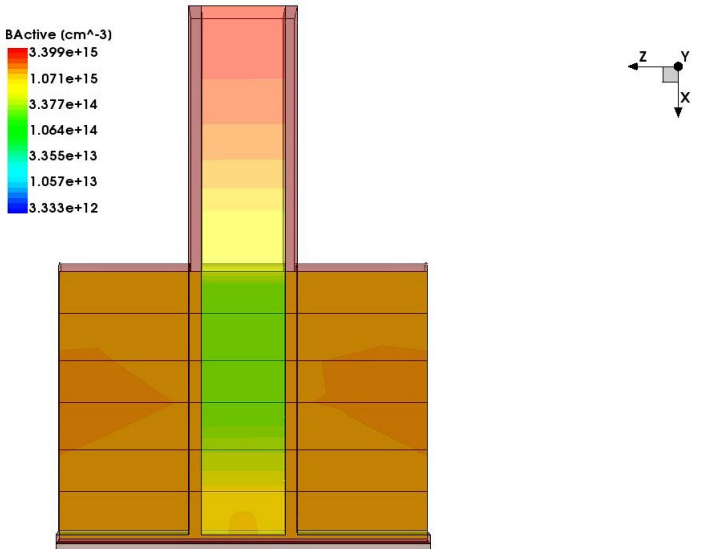
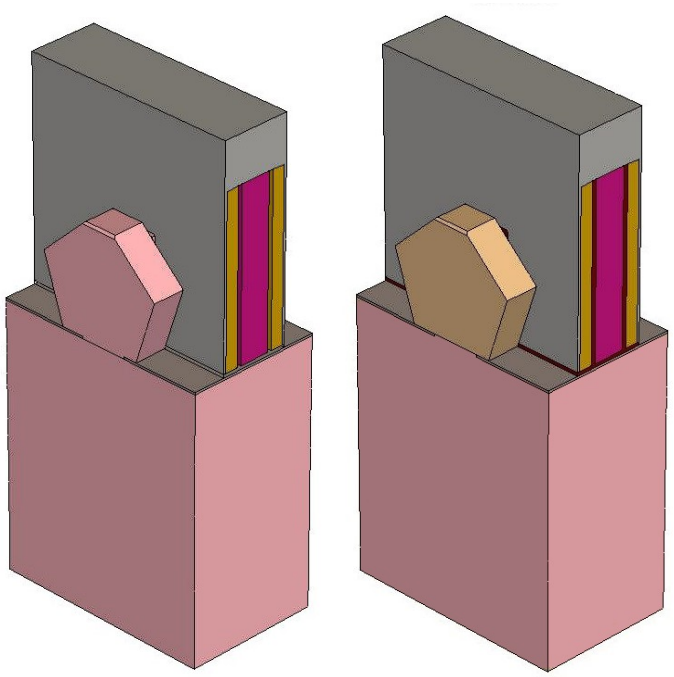


Figure 4.29: Boron S/D extensions. Polysilicon and SiO_2 are in translucency

Si_3N_4 spacers are created near the oxide walls. The SiCN is placed on the gate and the spacers: the exposed oxide and the Si-SiGe layers below it are removed. A SiGe isotropic etching is exploited to form the inner spacer filling the formed grooves with nitride. Where the Si-SiGe layers are removed, a of p-doped ($2 \cdot 10^{21} cm^{-3}$ of boron) silicon or a p-doped silicon germanium (in case of stressed device) is epitaxially grown (figure 4.30).



(a) (b)

Figure 4.30: S/D epitaxial growth: (a)p++ Silicon S/D (b) p++ SiGe S/D

The introduction of silicon germanium causes a change in silicon lattice as already explained in paragraph 2.2.2.
After S/D formation, the silicon carbon nitride is eliminated and the silicidation process is executed on S/D epitaxial layers using titanium as metal in the reaction with the silicon. The all structure is covered by PSG and then it is etched through CMP so that it has the same height of the dummy gate and it covers only the S/D areas. The dummy gate is etched using the oxide as etch stop and, subsequently, also the oxide is removed.

4.2.3 Gate stack

At this point, a stack (figure 4.31) in the gate area is realized as in the case of n-GAAFET, however there is an extra titanium nitride layer. The steps are as follows:

1. a thin layer (1 nm thick) is formed with dry thermal oxidation;
2. the oxide is covered by a layer of HfO_2 1 nm thick;
3. four layers of metal is deposited by exploiting MIG technology. The metals are, respectively, TiN, TaN, TiN, TiAl. The thickness for each layer are reported in table 2.2.

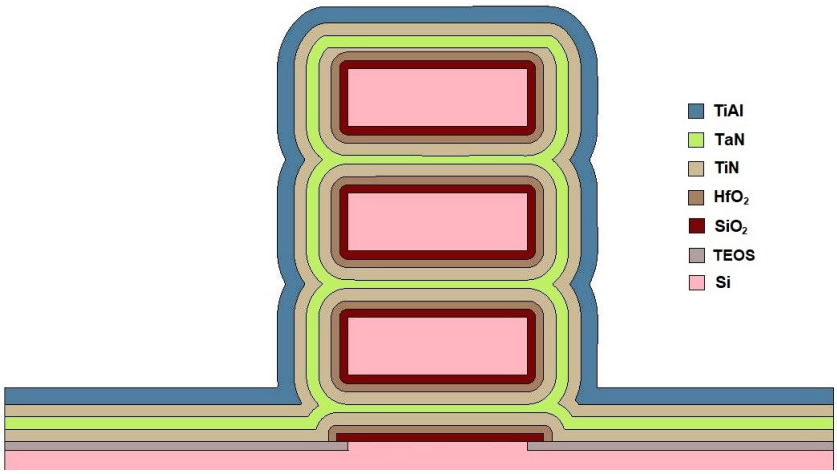


Figure 4.31: p-GAAFET Gate stack

4.2.4 Contacts

The tungsten covers the stack and then is etched in the same way as explained in subsection 4.1.8. The difference in height between PSG and W is compensated by deposition and CMP of nitride.
Finally the contacts are created. For S/D contacts two cavities in the PSG are formed by using SAC technique and then they are filled with tungsten. For gate contact Si_3N_4 is partially removed and then W deposition and etching by means of CMP are performed.

CHAPTER 5

Physical simulation of NS GAA-FET

A similar analysis to what as already seen in chapter 3 is done. Besides considering the advantage obtained from stress, it is observed how the behavior of subthreshold current varies according to the technology used (bulk, bulk with STI, SOI). So another parameter is introduced: Drain-Induced Barrier Lowering (DIBL). As technology scales the channel gets shorter, source and drain regions get closer to each other. When they are sufficiently close, an electrostatic coupling occurs between source and drain. So, when an high V_{DS} very close to power supply is applied, the energy barrier that prevents the flow of carriers through the channel becomes very low. At this point, even a small value of the gate-source voltage, with $0 < V_{GS} < V_{th}$, can completely flatten the energy barrier and allow a free flow of carriers in the channel. DIBL worsens as the doping level of the extensions increases.
The DIBL can be calculated as:

$$DIBL = -\frac{V_{th}^{DD} - V_{th}^{low}}{V_{DD} - V_{D}^{low}} \tag{5.1}$$

where V_{th}^{DD} is the threshold voltage when a drain voltage equal to the power supply is applied; V_{th}^{low} is the threshold voltage when a very low drain voltage is applied (0.05 V); V_{DD} is the power supply and V_{D}^{low} is the low drain voltage. The DIBL in measured in mV/V.

5.1 n-type Nanosheet GAA-FET

Initially , the analysis is focused on the differences between stressed and unstressed case for bulk and SOI technology. The variations of V_{th}, SS and DIBL are then considered as function of the thickness of buried oxide or of the oxide in trenches. Finally is made a comparison with bulk case and SOI case.

5.1.1 bulk NS GAAFET

Firstly, a simple n-type nanosheet GAAFET is considered. Solving Poisson and quantum correction equations, the I_{ds}-V_{gs} characteristic for stressed and unstressed devices is obtained. As for the finFET, also for the GAAFET, a drain voltage and a gate voltage of 1 V are applied. (figure 5.1).

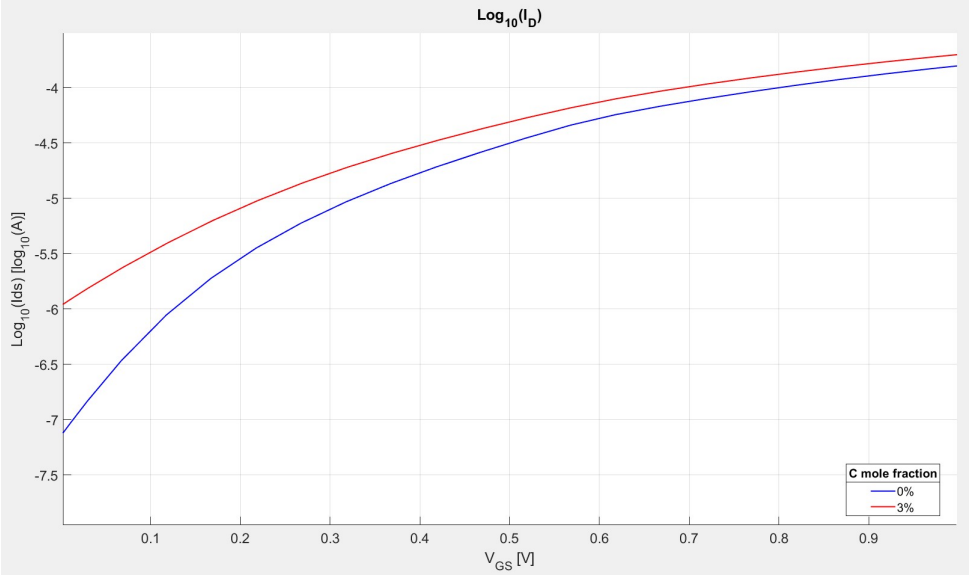


Figure 5.1: I_{ds}-V_{gs} characteristics of n-type bulk GAAFET ($V_{ds} = -1V$, $V_{gs} = -1V$)

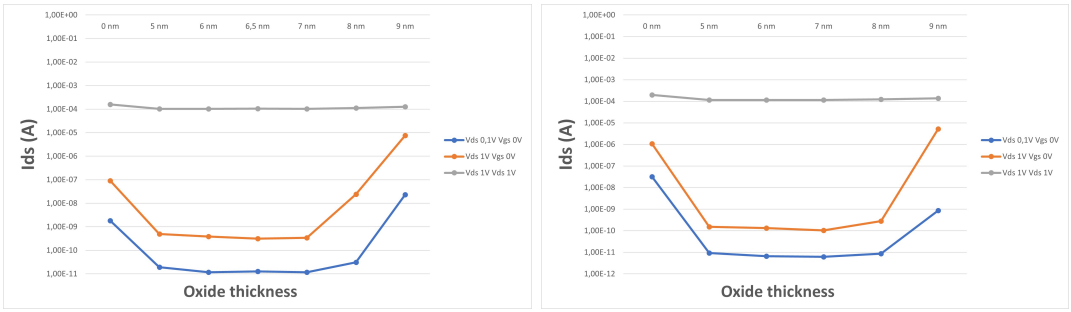
The I_{on} current at $V_{gs} = 1V$ is 157.44 μA for unstressed device and 198.93 μA for stressed device. Introducing $Si_{0.97}C_{0.03}$ source and drain, a tensile stress is induced in the channel and, consequently, an increase in mobility which leads to an increase in I_{on} current of about 26%. One reason why the difference in current is very high compared to the finFET is due to the fact that in this case three transistors (three nanosheets) are considered, while in the case of the finFET only one transistor (one fin) is considered.
Looking at figure 5.1, it is clear that the disadvantage of this structure is the high leakage current due to the "parasitic transistor" generated at top of the substrate. Furthermore in table 5.1 it can be seen how the SS is worse than the n-finFET case.

C mole fraction	V_{th} **(V)**	**SS** (mV/dec)	**DIBL** (mV/V)
0.00	0.479	91.91	-111.25
0.03	0.425	84.17	-129.65

Table 5.1: V_{th}, SS and DIBL of unstressed and stressed n-type bulk GAAFETs

To reduce the high leakage current, shallow trench insulator (STI) technique is adopted. It is considered various depth of STI and it is noted that the leakage current

begins to increase again form a certain depth onwards (figure 5.2). The more the depth increases, the more the stress generated by the oxide increases and the performance decreases[23]. The stress may affect the electrical device performance, like diode junction leakage and junction capacitance, in different ways. At the same time, the short channel behaviour may be compromised, due to the STI stress impact on the channel and well doping concentration [24].



(a) (b)

Figure 5.2: I_{ds} current at different V_{gs} and V_{ds}: (a) unstressed (b) stressed

The introduction of STI leads to a slight decrease in the I_{on}, while, as regard as the subthreshold current, it decreases by about two orders of magnitude before the effect of the stress due to STI prevails. The data for different depths of trench and for different voltages is reported in table 5.2.

			I_{ds} (μA)					
			V_{ds} 0.1 V	V_{gs} 0 V	V_{ds} 1 V	V_{gs} 0 V	V_{ds} 1 V	V_{gs} 1 V
STI depth	*unstressed*	0 nm	1.81E-03		0.0915		157.44	
		5 nm	1.94E-05		4.96E-04		102.23	
		6 nm	1.16E-05		3.9E0-04		103.66	
		7 nm	1.17E-05		3.38E-04		102.31	
		8 nm	3.10E-05		0.02397		112.16	
		9 nm	1.16E-05		7.557		125.70	
	stressed	0 nm	0.0318		1.068		198.93	
		5 nm	9.22E-06		1.51E-04		114.24	
		6 nm	6.66E-06		1.33E-04		115.51	
		7 nm	6.16E-06		1.04E-04		114.15	
		8 nm	8.61E-06		2.82E-04		121.91	
		9 nm	8.71E-04		5.198		138.21	

Table 5.2: I_{ds} at various STI depths and at different V_{ds} and V_{ds}

To better understand the subthreshold behavior, the DIBL is derived from equa-

tion 5.1:

- the threshold voltage when $V_{gs} = 1$ V and $V_{ds} = 50$ mV are applied (V_{th}^{low});
- the threshold voltage when $V_{gs} = 1$ V and $V_{ds} = 1$ V are applied (V_{th}^{DD});
- a drain voltage of 50 mV;
- a drain voltage of 1 V.

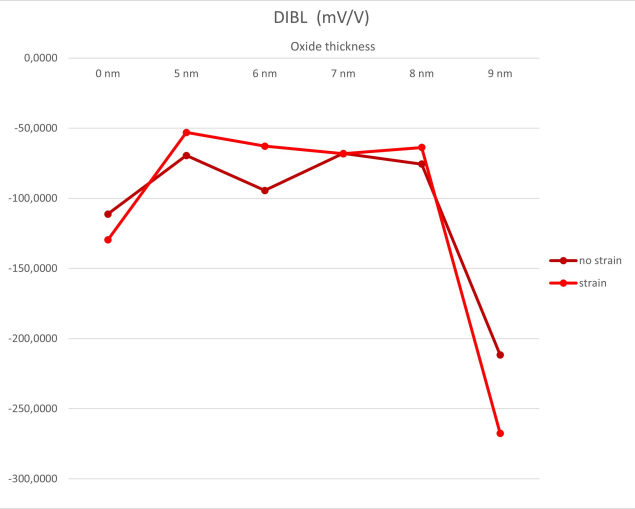


Figure 5.3: DIBL at different STI depths: unstressed case (*dark red line*), stressed case (*light red line*)

So, V_{th}^{low} and V_{th}^{DD} are calculated for stressed and unstressed case at different STI depths. From them derives the DIBL which, as expected, has a very low value in the absence of STI and higher values with a depth of the STI between 5 nm and 8 nm, and worsens with ever greater depths (figure 5.3). As regard as the subthreshold swing, it remains almost constant and then worsens dramatically with fairly consistent STI depths (figure 5.4).

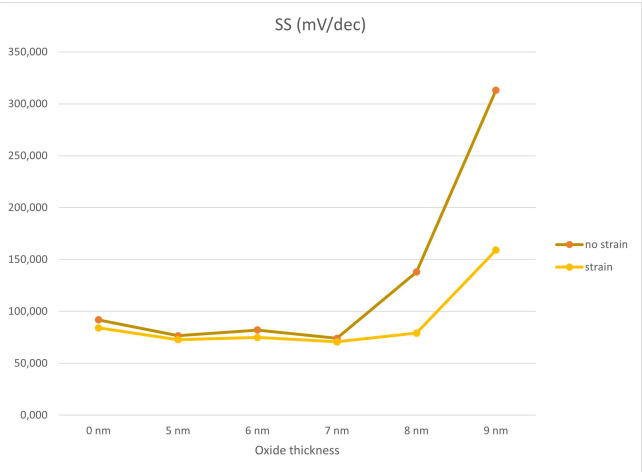


Figure 5.4: SS at different STI depths: unstressed case (*dark yellow line*), stressed case (*light yellow line*)

The results are reported in table 5.3.

	STI depth	V_{th}^{DD} (V)	V_{th}^{low} (V)	SS (mV/dec)	DIBL (mV/V)
unstressed	0 nm	0.479	0.373	91.91	-111.25
	5 nm	0.441	0.375	76.62	-69.42
	6 nm	0.471	0.381	82.07	-94.37
	7 nm	0.445	0.381	74.00	-68.04
	8 nm	0.451	0.379	138.00	-75.61
	9 nm	0.339	0.138	313.10	-211.64
stressed	0 nm	0.425	0.302	84.17	-129.65
	5 nm	0.429	0.378	72.72	-53.05
	6 nm	0.441	0.382	74.80	-62.76
	7 nm	0.444	0.380	70.73	-68.15
	8 nm	0.439	0.378	79.15	-63.74
	9 nm	0.630	0.376	158.98	-267.46

Table 5.3: V_{th}^{DD}, V_{th}^{low}, SS and DIBL at different STI depths

5.1.2 SOI NS GAAFET

Another solution to reduce the leakage current is the use of a Silicon-On-Insulator technology instead of a bulk one. In this case, only the unstressed device is considered. As previously done, the DIBL is calculated for different BOX thicknesses. So, V_{th}^{DD}, V_{th}^{low} at different oxide thickness are derived. As it can be observed in figure 5.5, as the oxide thickness increases, the DIBL tends to stabilize around -40 mV/V, while the while SS tends to slightly increase (figure 5.6).

Figure 5.5: DIBL at different BOX thickness

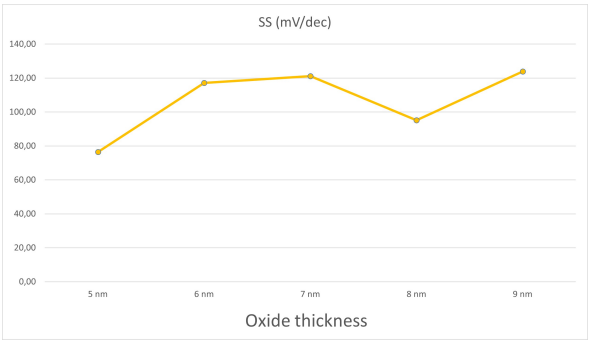


Figure 5.6: SS at different BOX thickness

The detailed results are reported in table 5.4.

	BOX thickness	V_{th}^{DD} (V)	V_{th}^{low} (V)	SS (mV/dec)	DIBL (mV/V)
unstressed	5 nm	0.419	0.358	76.45	-64.76
	6 nm	0.367	0.334	117.17	-35.37
	7 nm	0.383	0.341	121.12	-44.45
	8 nm	0.357	0.320	95.19	-39.27
	9 nm	0.340	0.299	123.90	-42.66

Table 5.4: V_{th}^{DD}, V_{th}^{low}, SS and DIBL at different oxide thicknesses

From this data, it is evident that the DIBL for SOI devices is better than that for bulk device, whereas in SS there are no relevant variations between the two types. Regarding the I_{on} current at various oxide thicknesses, there are no significant variations and it does not differ much from the bulk case (table 5.5).

BOX thickness	5 nm	6 nm	7 nm	8 nm	9 nm
I_{on} (μA)	109.82	112.97	118.91	114.37	117.72

Table 5.5: I_{on} in n-type SOI NS GAAFET varying the buried oxide thickness

5.2 p-type Nanosheet GAA-FET

The procedure to simulate the p-type NS GAA-FET is very similar to n-type one. The main difference is in the simulation of the stress: in n-type the stress is calculated manually without actually using SiC in SProcess and then the stress is inserted in SDevice. Instead in the p-type the SiGe is actually introduced in the simulation process and the stress is automatically calculated by SProcess and then transferred to SDevice. As for n-type, also for p-type the bulk and SOI technologies are considered.

5.2.1 bulk NS GAAFET

Intially the bulk GAA-FET without STI is considered, in particular the attention is focused on the stress due to different concentration of Ge. The I_{ds} - V_{gs} characteristics are derived for Si, $Si_{0.25}Ge_{0.75}$ and Ge source/drain (figure 5.7). A drain and gate voltages of -1 V are applied.

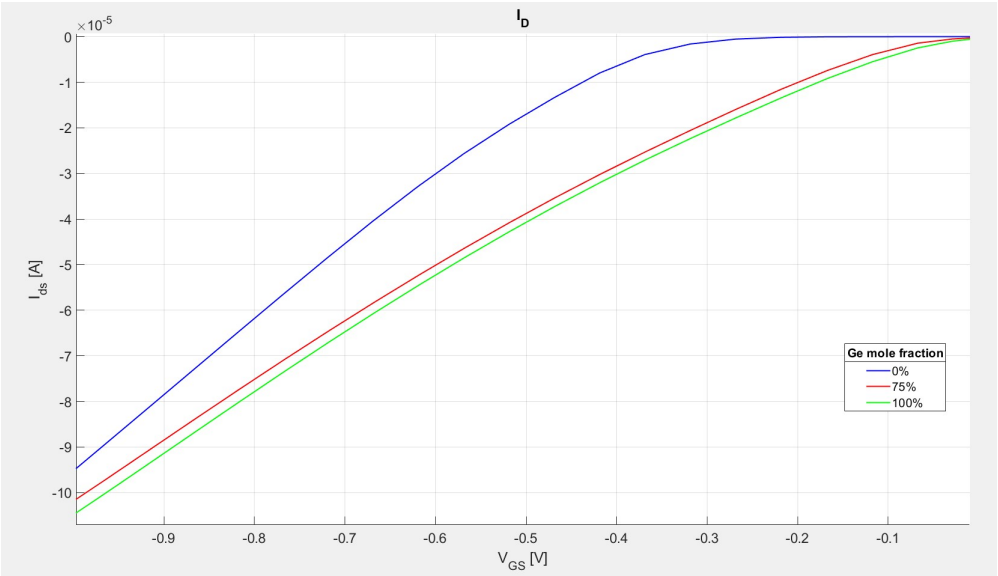


Figure 5.7: I_{ds}-V_{gs} characteristics of p-type bulk GAAFET ($V_{ds} = -1V$, $V_{gs} = -1V$)

There is an increase in I_{on} current of about 7% between unstressed device and stressed device with $Si_{0.25}Ge_{0.75}$; while the increase is about 10% between unstressed device and stressed device with Germanium. The three I_{on} currents with the respective V_{th}, SS and DIBL are reported in table 5.6.

Ge mole fraction	I_{on} (μA)	V_{th} $(\boldsymbol{V})$	**SS** $(\boldsymbol{mV/dec})$	**DIBL** $(\boldsymbol{mV/V})$
0.00	-95.22	-0.431	68.44	-107.7
0.75	-101.87	-0.242	74.92	-189.68
1.00	-104.85	-0.227	77.89	-195.36

Table 5.6: I_{on}, V_{th}, SS and DIBL for different Ge concentration in p-type bulk NS GAAFETs

As the Ge concentration increases, the SS and DIBL worsen. This happens because the germanium introduces impurities in silicon lattice.
As for bulk n-GAAFET, also for bulk p-GAAFET there is a "parasitic transistor" at top of the substrate that leads to have an high leakage current. The solution adopted to solve this problem is the introduction of the STIs with a depth of 7 nm. The improvement in the subthreshold behavior can be observed in figure 5.8.

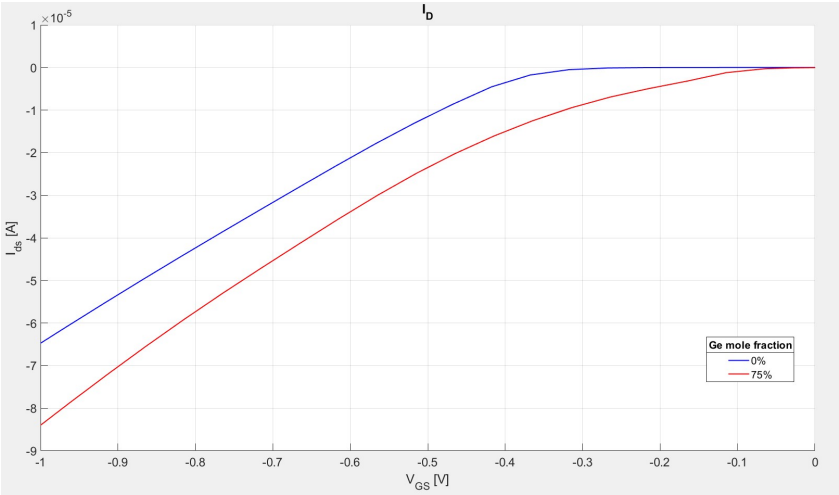


Figure 5.8: I_{ds}-V_{gs} characteristics of p-type bulk GAAFET with 7 nm STI depth ($V_{ds} = -1V$, $V_{gs} = -1V$)

The improvement is slightly visible in the DIBL values. SS remains almost unchanged, while the threshold voltage increases by about 150 mV in the stressed case (table 5.7).

Ge mole fraction	I_{on} (μA)	V_{th} (V)	**SS** (mV/dec)	**DIBL** (mV/V)
0.00	-64.75	-0.438	75.96	-101.18
0.75	-84.00	-0.399	69.90	-117.30

Table 5.7: I_{on}, V_{th}, SS and DIBL for stressed and stressed cases in p-type bulk NS GAAFETs with STI depth of 7 nm

On the contrary, the choice of inserting the STIs leads to a strong reduction of I_{on} current:

- 32% less for the unstressed case;
- 18% less for stressed case.

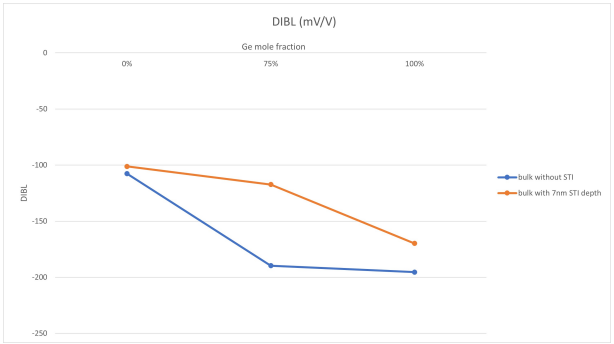


Figure 5.9: DIBL for bulk NS GAAFET with and without STI

5.2.2 SOI NS GAAFET

Another way to implement a p-type NS GAAFET is to use a silicon-on-insulator substrate instead of a bulk substrate. In particular the analysis focuses on p-type SOI NS GAAFET with a BOX 7 nm thick. The I_{ds}-V_{gs} characteristic is represented in figure 5.10

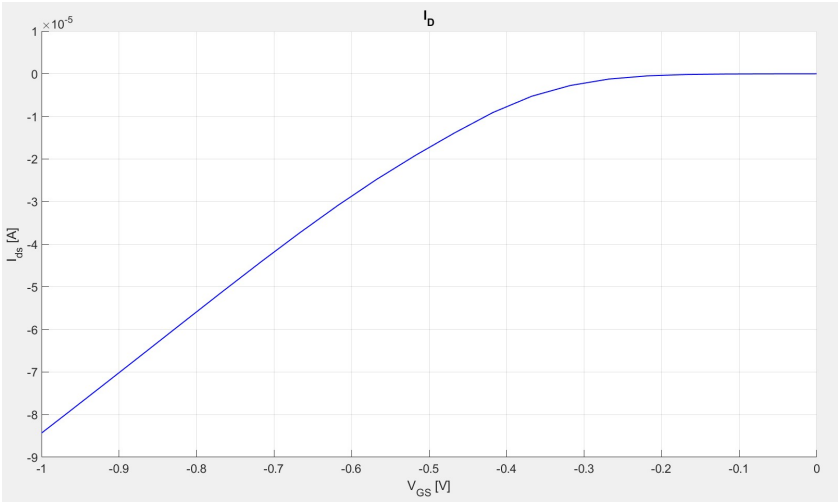


Figure 5.10: I_{ds}-V_{gs} characteristics of p-type SOI GAAFET with BOX 7 nm thick ($V_{ds} = -1V$, $V_{gs} = -1V$)

Respect to the bulk device, the SS slightly worsens, the DIBL remains almost the same and the threshold voltage slightly decreases: there is basically no clear difference. The parameters are reported in table 5.8.

I_{on} (μA)	V_{th} $(\boldsymbol{V})$	**SS** $(\boldsymbol{mV/dec})$	**DIBL** $(\boldsymbol{mV/V})$
-84.33	-0.410	104.07	-107.56

Table 5.8: I_{on}, V_{th}, SS and DIBL in p-type SOI NS GAAFETs with BOX 7 nm thick

CHAPTER 6

Synopsys Sentaurus TCAD Suite

Sentaurus is a suite of TCAD tools which simulates the fabrication, operation and reliability of semiconductor devices. The Sentaurus simulators use physical models to represent the wafer fabrication steps and device operation, thereby allowing the exploration and optimization of new semiconductor devices. The Sentaurus TCAD tools work seamlessly and can be combined into complete simulation flows in 2-D and 3-D. Sentaurus TCAD supports silicon and compound semiconductor technologies, covering a broad range of semiconductor applications[25].
Sentaurus TCAD Suite is composed by software divided into three main categories.

- Process simulation:
  - Sentaurus Process.
  - Sentaurus Topography.
- Structure editing:
  - Sentaurus Structure Editor.
- Device and interconnect simulation:
  - Sentaurus Device.
  - Raphael.
  - Sentaurus Interconnect

The framework of Sentaurus is foremd by:

- Sentaurus Workbench.
- Sentaurus Visual.
- Sentaurus Inspect
- Sentaurus PCM Studio.

6.1 Sentaurus Workbench

Sentaurus Workbench (SWB) is a complete graphical environment for creating, managing, executing, and analyzing TCAD simulations[25]. It has graphical user interface that allow to create project in which it is possible using the software of the suite. So in one project it can be simulate a process and, at the same time, simulate the device generated by the process simulation.

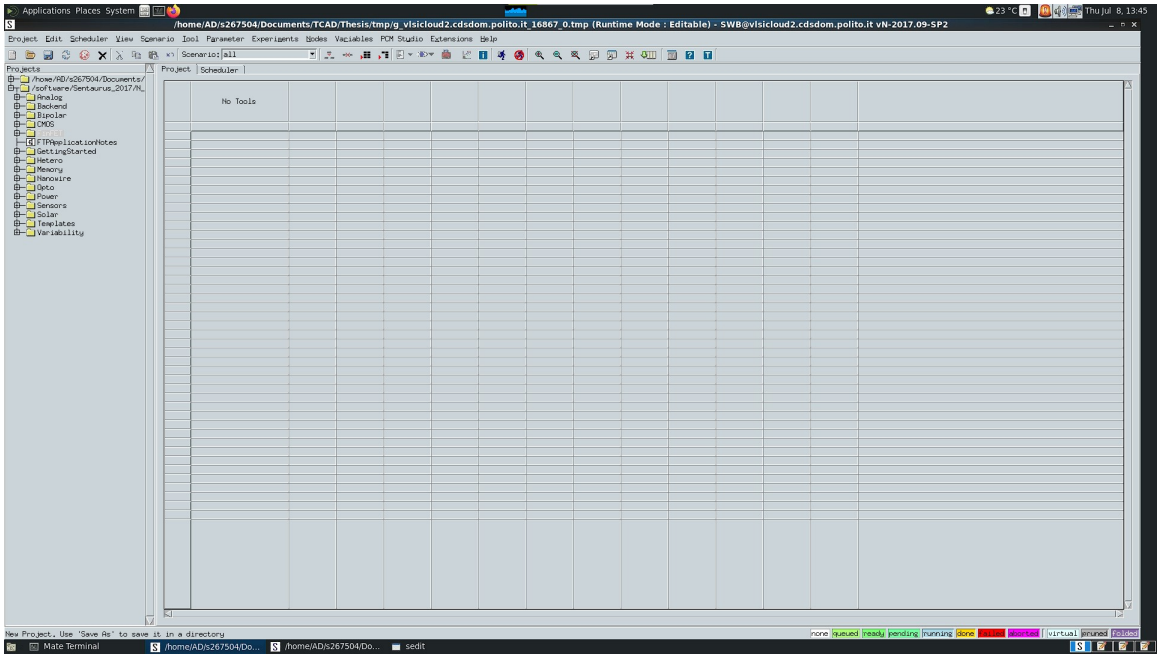
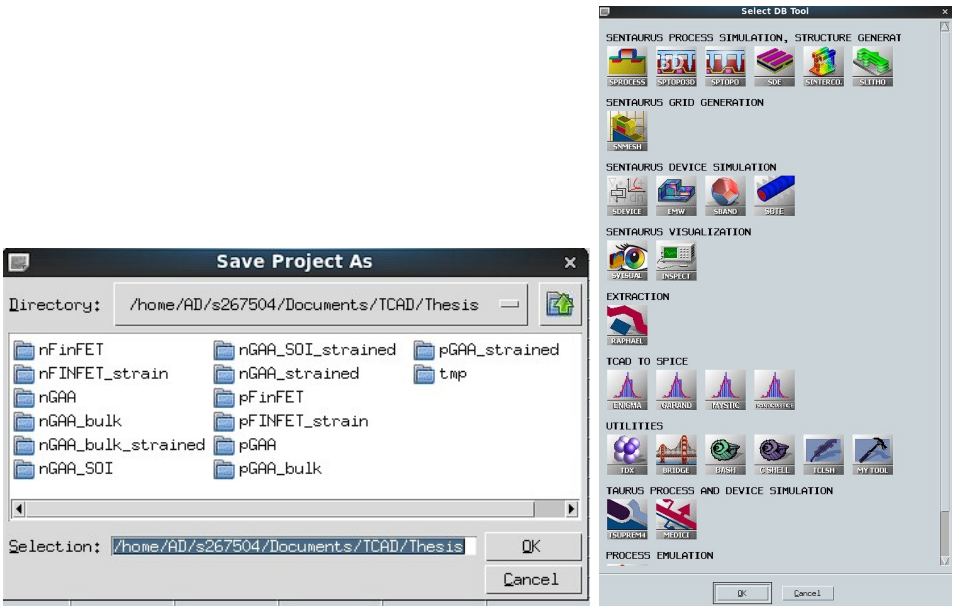


Figure 6.1: Sentaurus Workbench GUI

When the software is started, the screen in figure 6.1 appears. To create a new project it is necessary to select in the upper menu bar **Project** → **New** → **New Project**. Then **Project** → **Save As** → **Project** to save the project. After selecting the folder where to save it, to rename it simply add in the selection line: "/ + project name" (figure 6.2 (a)).
Now to choice what kind of software will be used, it is selected in the upper menu bar **Tools** → **Add**, a window is opened and then it need to select **Tools...**. At this point another window is opened (figure 6.2 (b)) and it can be possible to choice the software of the suite. Each rectangular is called 'node'.



(a) (b)

Figure 6.2: (a) Save project (b) Add tools

In this thesis each project is realized in the following order:

1. Fabrication of the device using Sentaurus Process.
2. Device simulation using Sentaurus Device.
3. Calculation of the parameters and printing of the graph with Sentaurus Inspect.

6.1.1 Sentaurus Process

Sentaurus Process (SProcess) simulates the fabrication steps in silicon process technologies in 2-D and 3-D[25]. With SProcess it is possible to simulate diffusion, deposition, thermal oxidation, etching, implantation, epitaxial growth, thermal annealing. Moreover it has a wide material database. Sentaurus Process computes all major sources of mechanical stress derived from volumetric changes, thermal and lattice mismatches, and deposited thin films. The complete stress history during processing can be simulated and the resulting stress field can be seamlessly exported to Sentaurus Device for evaluating its effect on electrical performance[25].
With right click on SProcess icon and selecting **Edit Input** → **Commands**, the file *sprocess_fps.cmd* is opened. In this file,the all commands to realize the device are written. The commands corresponding to the fabrication of the devices considered in this thesis are analyzed below.

```
math coord.ucs
```

```
math numThreads= 4

AdvancedCalibration
SiGe_and_Stress_Effect 1 1 1 0

# Set mechanical parameters
source mechParams.fps

pdbSet Mechanics EtchDepoRelax 0
pdbSet Grid MGoals Keep3DBrep 0

pdbSet Math flow 3D ILS.tolrel     1e-15
pdbSet Math flow 3D ILS.refine.sts 1

#The effect of germanium and stress on dopant diffusion is switched on
    by:
pdbSet Silicon SiliconGermanium.ConversionConc 1
pdbSet Silicon Skip.Parameter.Interpolation 0

# Stress/strain input - SD SiGe Mole Fraction
set GeMoleFraction @Ge_frac@
pdbSetBoolean Silicon Mechanics UpdateStrain 1
set iSMG    1.0                    ;# pMOS metal gate stress [GPa]
set iSsti   1.0                    ;# STI stress [GPa]

# USER-DEFINED PROCEDURES
source user_proc.fps
```

math coord.ucs is just a library declaration, while *math numThreads* indicates how many threads must be used during SProcess execution.
A more accurate calibration for Sentaurus Process has been performed by the Advanced Calibration team and is available using the command: *AdvancedCalibration*. The use of *Advanced Calibration* together with *SiGe_and_Stress_Effect* allows the defect-mediated interdiffusion of silicon and germanium.
The *source* command allows to place parameter settings in a separate file.
pdbSet and pdbSetBoolean are commands used to set parameter database, in particular[26]:

- *Mechanics EtchDepoRelax* if set to '0' the stress-rebalancing step after etchin or deposition is omitted.
- *Math flow 3D ILS.tolrel* and *Math flow 3D ILS.refine.sts* set to '1' indicate that the iterative linear solver (ILS) uses a STS3 mechanics solver for flow in 3D simulations
- *SiliconGermanium.ConversionConc* set to '1' and *Skip.Parameter.Interpolation* set to '0' enable the effect of germanium and stress on dopant diffusion (This commands are not used in unstressed and n-type devices).

- *Silicon Mechanics UpdateStrain* set to '1' enables the updating of the lattice spacing and the lattice mismatch strains during dopant redistribution.

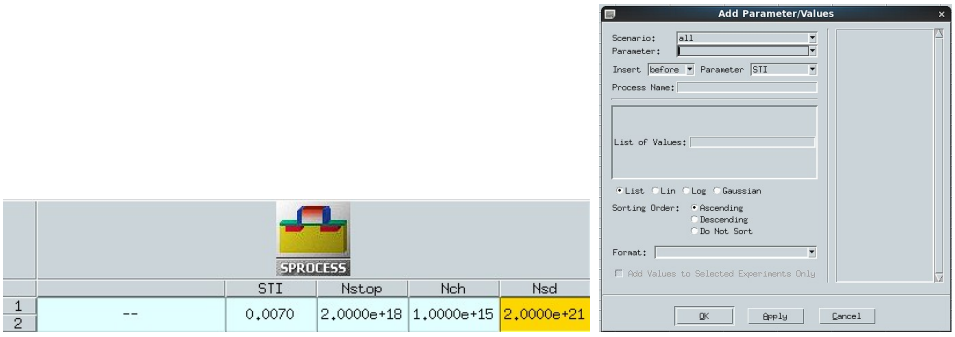
The *set* commands is used to define variables that can be used in the next commands by recalling them with the symbol '$'. For n-type devices these variables is slightly different:

```
# Stress/strain input - SD SiC Mole Fraction
set CMoleFraction @C_frac@
set iSMG    -1.0                    ;# nMOS metal gate stress [GPa]
```

Moreover for the case of devices with STI is added the command:

```
set STI @STI@
```

The value of variables with the symbol '@' means that the value is taken by the node under the column with the corresponding name in Senaturus Workbench (figure 6.3 (a)). Right click on the top of a column then **Add Parameter/Values** and a windows is opened (figure 6.3 (b)). In this windows it can be set the name of the parameter and its value.



(a) (b)

Figure 6.3: (a) Variables and its value in SWB (b) Adding variable

```
line x location= -70.0<nm> spacing= 1.0<nm> tag= SiTop
line x location= 20.0<nm> spacing= 5.0<nm>
line x location= 50.0<nm> spacing= 10.0<nm> tag= SiBottom

line y location= 0.0 spacing= 50.0<nm> tag= Left
line y location= 0.1<um> spacing= 50.0<nm> tag= Right

line z location= 0.0 spacing= 50.0<nm> tag= Back
line z location= 0.062<um> spacing= 50.0<nm> tag= Front

region SiStop xlo= SiTop xhi= SiBottom ylo= Left yhi= Right zlo= Back
   zhi= Front

init wafer.orient = { 0 0 1 }  flat.orient = { 1 1 0 } !DelayFullD
```

The *line* command specifies the position and spacing of mesh lines. With *tag* lines can be labeled for later reference by *region* command. Sentaurus Process uses the unified coordinate system (UCS)[26]:

- x has a downward direction, from the top to the bottom;
- y is perpendicular to the x-direction and lies along the wafer surface; y is in the lateral direction.
- z-direction is used for three dimensions, and the direction is given by X × Y.

region creates regions with a specified material using the coordinates defined with *line* command. The *init* command initialize a structure with a (001) wafer. When a 3D mask is used in an *etch*, a *deposit*, or a *photo* command, Sentaurus Process automatically extrudes the structure and the mesh into the appropriate dimension and copies the data. This delay of creating a full-dimensional structure can be switched off in the *init* command using the option *!DelayFullD*[26].

```
# Pwell

refinebox name= nw min= {-0.02 0 0.0} max= {0.03 0.11 0.17} xrefine=
   10<nm> yrefine= 50<nm> zrefine= 50<nm>
grid remesh

implant Phosphorus dose= 1e12<cm-2> energy= 30<keV> tilt= 30<degree>
   rotation= 0<degree>

implant Phosphorus dose= 1e12<cm-2> energy= 30<keV> tilt= 30<degree>
   rotation= 90<degree>

implant Phosphorus dose= 1e12<cm-2> energy= 30<keV> tilt= 30<degree>
   rotation= 180<degree>

implant Phosphorus dose= 1e12<cm-2> energy= 30<keV> tilt= 30<degree>
   rotation= 270<degree>
#####################################################################

# Thermal Annealing

diffuse temperature= 1000<C> time= 1<s>

struct tdr= n@node@_pGAA1;
```

The *refinebox* command sets the local grid parameters and performs a grid refinement using the MGOALS module; *min* and *max* limits the extent of the refinement box. Both arguments take a Tcl list of numbers defining the refinement box extent in the x-, y-, and z-axes. Moreover it is possible to assign a name to the refinement box and the *xrefine*, *yrefine* and *zrefine* commands define the element size in x-, y-

and z-direction[26]. To make the mesh changes in the refinement box take effect, *grid remesh* is used. With *implant*, a dose of Phosphorus of $1 \cdot 10^{12}$ is implanted with an energy of 30 keV and a title angle of 30 degrees. Four implantations are performed with a rotation difference of 90 degrees each to cover the entire 3-D structure. For n-well is used Boron instead of phosphorus. A thermal annealing step is executed at 1000°C for 1 second through the *diffuse* command. With *struct*, a tdr file containing the structure obtained until this point is saved. In SWB, the tdr file can be visualized with Sentaurus visual by right clicking on the desired node and then **Visualize** → **Sentaurus Visual (Select File...)**, now a window is opened and it is possible to choose the tdr file.

```
# BOX

diffuse temperature= 800<C> time= 5.2<min> H2O

struct tdr= n@node@_nGAA1;
```

In case of SOI device, the buried oxide grows with wet thermal oxidation activated by *H2O* in *diffuse* command. In this case the thermal oxidation is performed at 800°C for 5.2 minutes. A 6 nm layer of oxide is formed.

```
#deposit Si/SiGe layers

deposit material= {SiStop} type= anisotropic time= 1<min> rate=
   {0.001}
deposit material= {SiliconGermanium} type= anisotropic time= 1<min>
   rate= {0.008}
deposit material= {SiFin} type= anisotropic time= 1<min> rate= {0.007}
    region.name= Sich1
deposit material= {SiliconGermanium} type= anisotropic time= 1<min>
   rate= {0.008}
deposit material= {SiFin} type= anisotropic time= 1<min> rate= {0.007}
    region.name= Sich2
deposit material= {SiliconGermanium} type= anisotropic time= 1<min>
   rate= {0.008}
deposit material= {SiFin} type= anisotropic time= 1<min> rate= {0.007}
    region.name= Sich3
```

The *deposit* command is used to deposit new layer. The deposition uses in this thesis are: anisotropic, isotropic and fill. For the first two cases, it is necessary specify the duration of the deposition and how many um for each minute it deposits of that material. Instead for fill, it is indicated the x-coordinate up to which to deposit the material, the *coord* command is used. Moreover it is possible to give a name to the region formed with deposition. The *SiStop*, *SiFin*, *SiSD* and *SiGeSD* materials are defined in the file *mechParams.fps*. These materials are silicon, this difference is made only to distinguish the silicon of substrate, channel and source/drain.

```
# Nanosheet Production with SIT

deposit material= {Oxide} type= isotropic time= 1<min> rate= {0.0025}
deposit material= {Nitride} type= isotropic time= 1<min> rate= {0.019}
deposit material= {SiFin} type= isotropic time= 1<min> rate= {0.0215}

struct tdr= n@node@_pGAA2; # deposit mandrels, nitride, hardmask

mask name=fin left= 0<nm> right= 63<nm> back= -1 front= 0.17<um>
   negative

etch material= {SiFin} type= anisotropic time= 1<min> rate= {0.06}
   mask= fin

struct tdr= n@node@_pGAA3;

deposit material= {Oxide} type= isotropic time= 1 rate= {0.0215}
etch material= {Oxide} type= anisotropic time = 1 rate= {0.0215}
   isotropic.overetch= 0.001

struct tdr= n@node@_pGAA4; # Spacer formation

etch material= {SiFin} type= anisotropic time= 1<min> rate= {0.1}
etch material= {Nitride} type= anisotropic time= 1<min> rate= {0.1}

struct tdr= n@node@_pGAA5; # etch mandrels

etch material= {Oxide} type= anisotropic time= 1<min> rate= {0.0215}
etch material= {SiFin} type= anisotropic time= 1<min> rate= {0.008}
etch material= {SiliconGermanium} type= anisotropic time= 1<min> rate=
    {0.008}
etch material= {SiFin} type= anisotropic time= 1<min> rate= {0.008}
etch material= {SiliconGermanium} type= anisotropic time= 1<min> rate=
    {0.008}
etch material= {SiFin} type= anisotropic time= 1<min> rate= {0.008}
etch material= {SiliconGermanium} type= anisotropic time= 1<min> rate=
    {0.008}
etch material= {SiStop} type= anisotropic time= 1<min> rate= {0.001}

etch material= {Nitride} type= anisotropic time= 1<min> rate= {0.02}

struct tdr= n@node@_pGAA6; # Nanosheet formation

etch material= {Oxide} type= anisotropic time= 1<min> rate= {0.02}

struct tdr= n@node@_pGAA7;
```

etch removes an exposed layer of a specific material. The etching uses in this thesis are anisotropic, isotropic and cmp. For the first two cases, what has already been seen

above is valid. For cmp, it is very similar to the fill deposition, the difference being the removal, instead of deposition, of the material at a specified x-coordinate using *coord* command.
mask creates a mask then can be used in *etch*, *deposit* and *photo* commands. *left*, *right*, *back* and *front* specify the corners of a rectangle and the points inside the rectangle are considered masked by default. If *negative* command is used, the point outside the rectangle are considered masked.
For devices with STI the line *etch material= SiStop type= anisotropic time= 1<min> rate= {0.001}* is removed and the subsequent code become:

```
etch material= {SiFin} type= anisotropic time= 1<min> rate= {0.008}
etch material= {SiStop} type= anisotropic time= 1<min> rate= {$STI}

etch material= {Nitride} type= anisotropic time= 1<min> rate= {0.02}

struct tdr= n@node@_nGAA6; # nanosheet formation

deposit material= {Oxide} type= isotropic time= 1<min> rate= {0.1}
etch material= {Oxide} type= cmp coord= -0.07

struct tdr= n@node@_nGAA7; # STI
```

```
#TEOS

#--- Calculate intrinsic stress ---------------------------------
set iS    [expr ($iSsti * 1.0e10 * ( 1.0 - 0.16 ) / ( 1.0 - 2.0 * 0.16
    ))]
doping name=SxxSTI field=StressELXX depths= { 0 100 } stress.values= {
    $iS $iS }
doping name=SyySTI field=StressELYY depths= { 0 100 } stress.values= {
    $iS $iS }
doping name=SzzSTI field=StressELZZ depths= { 0 100 } stress.values= {
    $iS $iS }

mater add name= TEOS new.like=oxide

deposit material= {TEOS} type= isotropic time= 1<min> rate= {0.04}
   doping= { SxxSTI SyySTI SzzSTI }

struct tdr= n@node@_pGAA8;

etch material= {TEOS} type= cmp coord= -0.071

struct tdr= n@node@_pGAA9; #TEOS CMP
```

It is also possible to assign an expression to a variable instead of a value with command *expr* in square brackets. In this case the intrinsic stress due to TEOS is calculated. This stress is used in *doping* command. This command defined a doping

profile to which is possible to assign a name. This profile can be used for dopants, stress and mole fractions. Moreover, it allows a doping profile specification that can be used inside the deposit command to add doping and other fields to the newly deposited layer[26]. *mater add* creates a new material that there are not in the Sentaurus database. The default parameters of this new material are inherited from the material indicates by *new.like* command.

```
# SiO2 deposition

deposit material= {Oxide} type= isotropic time= 1<min> rate= {0.0015}

struct tdr= n@node@_pGAA10;

mater add name= SiCN new.like= SiliconCarbide
#########################################################################

#Dummy gate

deposit material= {Polysilicon} type= fill coord= -0.16

mask name= gate back= 24<nm> front= 38<nm>
mask name= gate_n back= 24<nm> front= 38<nm> negative

etch material= {Polysilicon} type= anisotropic time= 1<min> rate=
   {0.1} mask= gate

struct tdr= n@node@_pGAA11;

mask name= wall back= 22<nm> front= 40<nm> negative

deposit material= {Oxide} type= anisotropic time= 1<min> rate= {0.1}
   mask= wall
etch material= {Oxide} type= cmp coord= -0.16

struct tdr= n@node@_pGAA12; # SiO2 CVD on dummy gate wall
#########################################################################

# S\D extensions

#Cover dummy gate and nwell with photoresist
mask name= dummy back= 15<nm> front= 47<nm> negative

photo thickness= 1<um> mask= dummy

implant Boron dose= 1e10<cm-2> energy= 6<keV> tilt= 10<degree>
   rotation= 0<degree>
implant Boron dose= 1e10<cm-2> energy= 6<keV> tilt= 10<degree>
   rotation= 180<degree>
```

```
etch material= {Photoresist} type= anisotropic time= 1<min> rate= {3}
#########################################################################

# RTA

diffuse temperature= 1000<C> time= 0.1<s>

struct tdr= n@node@_pGAA13;
```

photo creates a photoresist layer of the specified thickness outside the mask. For n-type devices the implantation is made with phosphorous. Two rotations are used to create extensions between source and drain.

```
# Spacer

deposit material= {Nitride} type= isotropic time= 1<min> rate= {0.1}
   mask= dummy

etch material= {Nitride} type= anisotropic time= 1 rate= {0.11}
   isotropic.overetch= {0.01}
etch material= {Polysilicon} type= cmp coord= -0.149
etch material= {Oxide} type= cmp coord= -0.149

struct tdr= n@node@_pGAA14; # Spacer definition
#########################################################################

# S/D Creation

deposit material= {SiCN} type= isotropic time= 1<min> rate= {0.15}
   mask= dummy

etch material= {Oxide} type= anisotropic time= 1<min> rate= {0.2}
etch material= {SiCN} type= cmp coord= -0.17

struct tdr= n@node@_pGAA15; # SiCN deposition photolitography and
   etching

etch material= {SiFin} type= anisotropic time= 1<min> rate= {0.007}
etch material= {SiliconGermanium} type= anisotropic time= 1<min> rate=
    {0.1}
etch material= {SiFin} type= anisotropic time= 1<min> rate= {0.007}
etch material= {SiliconGermanium} type= isotropic time= 1<min> rate=
   {0.005}

deposit material= {Nitride} type= fill coord= -0.11
etch material= {Nitride} type= anisotropic time= 1 rate= {0.11}

EpitaxySD sd1 0.045 0.062 -0.013 0.013 0.045 0.03 0.004 0.005 0.006
   0.016 0.0151 55.0 -0.115 0.05
polyhedron list
```

```
insert polyhedron=sd1 replace.materials= { Gas } \
       new.material=SiGeSD new.region=SDepi
PolyHedronClear

EpitaxySD sd2 0.0 0.017 -0.013 0.013 0.045 0.03 0.004 0.005 0.006
   0.016 0.0151 55.0 -0.115 0.05
polyhedron list
insert polyhedron=sd2 replace.materials= { Gas } \
       new.material=SiGeSD new.region=SDepi
PolyHedronClear

sel SiGeSD  z=@Nsd@   name=Boron      store
sel SiFin   z=@Nch@   name=Phosphorus store
sel SiStop  z=@Nstop@ name=Phosphorus store


set NgeL [MoleFractionFields SiliconGermanium $GeMoleFraction]
set Nge [lindex $NgeL 5]
sel SiGeSD       z=$Nge     name=Germanium   store
sel SiFin        z=0    name=Germanium   store

diffuse temp=800 time=100.0e-3<s>

struct tdr= n@node@_pGAA16; # etching of the exposed N fins and Si
   epitaxy
```

EpitaxySD is a function defined in file *user_proc.fps* and it is a set of simpler commands such as *point* and *polygon*.
point create a point for polygon that is generated with *polygon* command. Finally with *insert polyhedron* command forms with the polygons previously defined the 3-D structure of the source and drain. In this case this structures are renamed "SDepi" and are made of SiGeSD.
With *sel* command are define the concentration of a specified chemical element in a determined material. For example in the code, a 'Nsd' concentration of boron is present in SiGeSD.
In p-type stressed devices, a concentration of germanium is attributed to the source and drain according to the Ge mole fraction. To activate these dopants, the *diffuse* command is used.

```
#--- Calculate intrinsic stress from C Mole fraction -----------------
#--- C11=165.7GPa C12=63.9GPa C44=79.6GPa for Silicon - 2% C
   negiligible
set iS    [expr (1.0 * ( 165.7 + 2 * 63.9 ) * 1e9 * 0.449 *
   $CMoleFraction )]
stressdata  SiSD  sxxi=$iS<Pa>  syyi=$iS<Pa>  szzi=$iS<Pa>

sel SiSD    z=@Nsd@   name=Phosphorus   store
sel SiFin   z=@Nch@   name=Boron store
```

```
sel SiStop  z=@Nstop@ name=Boron store

diffuse temp=1000 time=100.0e-3<s>
```

In n-type stressed devices, instead of defining a concentration of carbon that than causes lattice mismatch, the stress is mathematically calculated an then stored in the SiSD material.

```
# TiSi2 patterning

etch material= {SiCN} type= anisotropic time= 1<min> rate= {0.2}

mask name= f1 left= 0.021<um> right= 0.079<um> negative

deposit material= {TiSilicide} type= isotropic time= 1<min> rate=
   {0.001} mask= f1

etch material= {TiSilicide} type= cmp coord= -0.121

struct tdr= n@node@_pGAA17;
#########################################################################

# PSG deposition and CMP

mater add name= PSG
reaction name= PSGreaction mat.l= Phosphorus mat.r= Oxide mat.new= PSG
    new.like= oxide diffusing.species= {Oxide}

deposit material= {PSG} type= isotropic time= 1<min> rate= {0.2}

etch material= {PSG} type= cmp coord= -0.149

struct tdr= n@node@_pGAA18;
```

In this case the material PSG, which are not in the Sentaurus database, is added and defined as reaction between phosphorus and oxide and it takes the default parameters from oxide. To do this, the *reaction* command is used.

```
# Dummy Gate removal

etch material= {PolySilicon} type= anisotropic time= 1<min> rate=
   {0.2}

struct tdr= n@node@_pGAA19; # Dummy gate etching using SiO2 as etch
   stop layer

etch material= {Oxide} type= anisotropic time= 1<min> rate= {0.1} mask
   = gate_n
etch material= {SiliconGermanium} type= cmp coord= -0.07

struct tdr= n@node@_pGAA20; # SiO2 etching
```

```
#########################################################################

# Gate stack

mask name= gf0 left= 0.04 right= 0.065 back= 24.1<nm> front= 37.9<nm>
   negative

deposit material= {Oxide} type= isotropic time= 1<min> rate= {0.001}
   mask= gf0
etch material= {Oxide} type= cmp coord= -0.149

mask name= gf1 left= 0.039 right= 0.066 back= 24<nm> front= 38<nm>
   negative

deposit material= {HfO2} type= isotropic time= 1<min> rate= {0.001}
   mask= gf1
etch material= {HfO2} type= cmp coord= -0.118

struct tdr= n@node@_pGAA21; # Thermal oxidation of fins and HfO2
   deposition
#########################################################################

# MIG process

#--- Calculate intrinsic stress --------------------------------
set iS    [expr ($iSMG * 1.0e10 * ( 1.0 - 0.296 ) / ( 1.0 - 2.0 *
   0.296 ))]
doping name=SxxMG field=StressELXX depths= { 0 100 } stress.values= {
   $iS $iS }
doping name=SyyMG field=StressELYY depths= { 0 100 } stress.values= {
   $iS $iS }
doping name=SzzMG field=StressELZZ depths= { 0 100 } stress.values= {
   $iS $iS }

set iStn  [expr ($iSMG * 1.0e10 * ( 1.0 - 0.25 ) / ( 1.0 - 2.0 * 0.25
   ))]
doping name=SxxMGtn field=StressELXX depths= { 0 100 } stress.values=
   { $iS $iS }
doping name=SyyMGtn field=StressELYY depths= { 0 100 } stress.values=
   { $iS $iS }
doping name=SzzMGtn field=StressELZZ depths= { 0 100 } stress.values=
   { $iS $iS }

deposit material= {TiNitride} type= isotropic time= 1<min> rate=
   {0.0015} mask= gate_n doping= { SxxMGtn SyyMGtn SzzMGtn }
etch material= {TiNitride} type= cmp coord= -0.1185

mater add name= TaNitride
reaction name= TaN mat.l= Tantalum mat.r= Nitrogen mat.new= TaNitride
```

```
   new.like= Nitride diffusing.species= {Tantalum Nitrogen}

deposit material= {TaNitride} type= isotropic time= 1<min> rate=
   {0.0015} mask= gate_n
etch material= {TaNitride} type= cmp coord= -0.120

deposit material= {TiNitride} type= isotropic time= 1<min> rate=
   {0.0015} mask= gate_n doping= { SxxMGtn SyyMGtn SzzMGtn }
etch material= {TiNitride} type= cmp coord= -0.1235

struct tdr= n@node@_pGAA22; # TiN/TaN/TiN gate deposition

mater add name= TiAl new.like= Aluminum

deposit material= {TiAl} type= isotropic time= 1<min> rate= {0.002}
   mask= gate_n doping= { SxxMG SyyMG SzzMG }
etch material= {TiAl} type= cmp coord= -0.1255

struct tdr= n@node@_pGAA23; # TiAl deposition

deposit material= {Tungsten} type= isotropic time= 1<min> rate= {0.1}
   doping= { SxxMG SyyMG SzzMG }
etch material= {Tungsten} type= cmp coord= -0.148

struct tdr= n@node@_pGAA24; # W CVD and CMP

deposit material= {Nitride} type= isotropic time= 1<min> rate= {0.05}
etch material= {Nitride} type= cmp coord= -0.1489

struct tdr= n@node@_pGAA25; # W partial etch back, Si3N4 CVD and CMP

mask name= s left= 17<nm> right= 83<nm> back= 50<nm> front= 57<nm>
   negative
mask name= d left= 17<nm> right= 83<nm> back= 5<nm> front= 12<nm>
   negative

mask name= g left= 17<nm> right= 83<nm> back= 27.5<nm> front= 34.5<nm>
    negative

etch material= {PSG} type= anisotropic time= 1<min> rate= {0.05} mask=
    s
etch material= {PSG} type= anisotropic time= 1<min> rate= {0.05} mask=
    d

etch material= {Nitride} type= anisotropic time= 1<min> rate= {0.01}
   mask= g

deposit material= {Tungsten} type= isotropic time= 1<min> rate= {0.05}
    doping= { SxxMG SyyMG SzzMG }
```

```
etch material= {Tungsten} type= cmp coord= -0.1489

diffuse temp=450<C> time=1.0e-6<s> stress.relax

struct tdr= n@node@_pGAA26; # S/D contact and gate contact
```

Also for the metals in gate stack the stress is calculated and applied to them. Finally the strain is updated with the the *diffuse* command and *stress.relax* switches on relaxation of stresses during diffusion with an inert ambient[26].

```
deposit  Gas    type=fill  coord=-0.56

#--Change refinement strategy and remesh
   ------------------------------
##---------------Remeshing for device simulation--------##

# clear the process simulation mesh
refinebox clear
refinebox !keep.lines
refinebox clear.interface.mats
line clear

pdbSet Grid MGoals Keep3DBrep 0

# reset default settings for adaptive meshing
pdbSet Grid AdaptiveField Refine.Abs.Error 1e37
pdbSet Grid AdaptiveField Refine.Rel.Error 1e10
pdbSet Grid AdaptiveField Refine.Target.Length 100.0
# Doping based refinement
pdbSet Grid Adaptive 1

# Set high quality delaunay meshes
pdbSet Grid sMesh 1
pdbSet Grid SnMesh DelaunayType boxmethod
pdbSet Grid SnMesh DelaunayTolerance 5.0e-2
pdbSet Grid SnMesh CoplanarityAngle 179
pdbSet Grid SnMesh MaxPoints 500000
pdbSet Grid SnMesh MaxNeighborRatio 1e6

# Set the interface spacing
mgoals accuracy=1e-6
pdbSet Grid SnMesh min.normal.size 0.01
pdbSet Grid SnMesh max.box.angle.3d 179
pdbSet Grid SnMesh normal.growth.ratio.3d 8.0
# Which interfaces are to have interface meshes

refinebox interface.materials= {SiFin Oxide Oxide HfO2}
refinebox name= gate min= {-0.152 0.0 0.015} max= {-0.077 0.22 0.047}
   xrefine= 1<nm> yrefine= 2<nm> zrefine= 1.4<nm>
```

```
refinebox name= source min= {-0.152 0.0 0.0} max= {-0.071 0.22 0.015}
   xrefine= 10<nm> yrefine= 20<nm> zrefine= 20<nm>
refinebox name= drain min= {-0.152 0.0 0.047} max= {-0.071 0.22 0.062}
    xrefine= 10<nm> yrefine= 20<nm> zrefine= 20<nm>
grid remesh
```

Before moving on to analyzing the device with sentaurus Device, it is necessary performing a remesh. The time simulation depends on the mesh quality.

```
# Contact

contact point replace region= Tungsten_1.3.2 name= source
contact point replace region= Tungsten_1.3.1 name= drain

contact point replace region= Tungsten_1.1 name= gate

contact bottom name = substrate SiStop

struct tdr= n@node@_GAA !gas; # Final

exit
```

Finally the contact are defined for subsequent device simulation.

6.1.2 Sentaurus Device

Sentaurus Device (SDevice) simulates the electrical, thermal, and optical characteristics of silicon and compound semiconductor devices in 2-D and 3-D. In addition, Sentaurus Device enables the analysis of complex integrated circuit phenomena such as electrostatic discharge, latch-up, and single event upset[25]. As for SProcess also for SDevice there is a command file where all the commands are put. As seen in subsection 6.1.1, the command file is opened by right clicking on SDevice icon and selecting **Edit Input** → **Commands**. The name of the file is *sdevice_des.cmd*.
Before analyzing the devices, the materials not present in the sentaurus database must be defined in a file called *datexcode.txt*. New materials should be written as follows:

```
Materials {
  PSG {
        label   = "PSG"
        group   = Insulator
        color   = #74b36b, #d915b8
    }
}
```

where label is the name which is used to indicate the material; group indicates if the material is a insulator, a semiconductor or a conductor; color is the written in hexadecimal format, each pair of alphanumeric character indicates the quantity of red, green and blue. The color chosen for that material is visible in Sentaurus Visual. To define

the parameters for the new materials, it must be generated a file with extension *.par* in which inserting the material parameters and finally including this file in another file called "*sdevice.par*". In *sdevice.par* are included all *material.par* files and, moreover, it is possible to add other parameters for existing materials in the database.

The *sdevice_des.cmd* is divided in six sections:

1. File section.
2. Electrode section.
3. Physics section.
4. Plot section.
5. Math section.
6. Solve section.

Each section is explained by taking into account the code uses to simulate the devices of this thesis.

File Section

```
File
{
*INPUT FILES
Grid ="n@previous@_GAA_fps.tdr"
* physical parameters
Parameter = "sdevice.par"
*strain
Piezo= "n@previous@_GAA_fps.tdr"

**** OUTPUT FILES
* distributed variables
Plot = "n@node@_des.tdr"
* electrical characteristics at the electrodes
Current= "n@node@_des.plt"
}
```

Grid loads device geometry and mesh from the *tdr* file generated by SProcess.
Parameter takes the parameters from *sdevice.par* file.
Piezo extracts stress data for piezoelectric model from the *tdr* file generated by SProcess.
Plot saves in a *tdr* file spatially distributed simulation results according to what defined in Plot section.
Current saves in a *plt* file device currents, voltages, charges, temperatures, and times that can be visualized in a graph with Sentaurus Inspect.

Electrode Section

```
Electrode
{
* defines which contacts have to be treated as electrodes; initial
   bias
* & boundary conditions
{ name="source" Voltage=0.0 }
{ name="drain" Voltage=0.0 }
{ name="gate" Voltage=0.0 }
{ name="substrate" Voltage=0.0 }
}
```

The electrode section is used to define contacts and their initial voltage.

Physics section

```
Physics
{
Mobility( DopingDep
    Enormal( RPS InterfaceCharge(SurfaceName="S1") )
        HighFieldSaturation )
EffectiveIntrinsicDensity( BandGapNarrowing( OldSlotBoom ) NoFermi )
Recombination ( SRH(DopingDep) Auger Band2Band ( Model = Hurkx ) )
Piezo(
  Strain= LoadFromFile
  Model (
          DeformationPotential(ekp hkp minimum)
          DOS(eMass hMass)
    Mobility( hfactor(kanda sfactor=SBmob(Type=1)
   ApplyToMobilityComponents )
                          hSaturationFactor = 0.27
          )
  )
)
}

Physics (Region= "SDepi.1") {
  Aniso(eQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
  Aniso(hQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
}

Physics (Region= "SDepi.2") {
  Aniso(eQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
  Aniso(hQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
}

Physics (Region= "Sich1") {
  Aniso(eQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
```

```
  Aniso(hQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
}

Physics (Region= "Sich2") {
  Aniso(eQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
  Aniso(hQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
}

Physics (Region= "Sich3") {
  Aniso(eQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
  Aniso(hQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
}

Physics(Material="TiNitride") {
  Piezo( Stress=(0,0,0,0,0,0) )
}

Physics(MaterialInterface="HfO2/Oxide") {
  Traps (
    (FixedCharge Conc=1.0e12 Level EnergyMid=0.0 fromMidBandGap)
    (FixedCharge Conc=-1.0e12 Level EnergyMid=0.0 fromMidBandGap)
  )
}
```

In Physics section are inserted the commands regarding the behavior of the device, in particular are chosen the model with which the device simulation proceeds.
In the first part are put the models for mobility, recombination and stress that are applied to all device structure. The models take into account are the same describe in section 3.1. For n-type device is used *efactor* instead of *hfactor* and *eSaturationFactor = 0.2* instead of *hSaturationFactor = 0.27*.
In the second part are applied determined characteristics to only some region of the device: *Aniso* is used for defining anisotropic direction in crystal system; *Piezo(Stress=(0,0,0,0,0,0)* set the stress to 0 *Pa* in TiN; *Traps* gives the specification of traps with fixed charge and level distribution with a concentration of $1 \cdot 10^12$ at the interface between HfO_2 and oxide.

Plot section

```
Plot
{
* On mesh variables to be saved in the .tdr output file
*- Doping Profiles
Doping DonorConcentration AcceptorConcentration
*- Charge, field, potential and potential energy
SpaceCharge
ElectricField/Vector Potential
BandGap EffectiveBandGap BandGapNarrowing ElectronAffinity
```

```
ConductionBandEnergy ValenceBandEnergy
*- Carrier Densities:
EffectiveIntrinsicDensity IntrinsicDensity
eDensity hDensity
eQuasiFermiEnergy hQuasiFermiEnergy
*- Currents and current components:
eGradQuasiFermi/Vector hGradQuasiFermi/Vector
eMobility hMobility eVelocity hVelocity
Current/Vector eCurrent/Vector hCurrent/Vector
eDriftVelocity/Vector hDriftVelocity/Vector
*- SRH & interfacial traps
SRHrecombination
tSRHrecombination
*- Band2Band Tunneling & II
eBand2BandGeneration hBand2BandGeneration Band2BandGeneration
eAvalanche hAvalanche Avalanche
StressXX StressYY StressZZ StressXY StressYZ StressXZ
eMobilityStressFactorXX eMobilityStressFactorYY
   eMobilityStressFactorZZ
eMobilityStressFactorYZ eMobilityStressFactorXZ
   eMobilityStressFactorXY
hMobilityStressFactorXX hMobilityStressFactorYY
   hMobilityStressFactorZZ
hMobilityStressFactorYZ hMobilityStressFactorXZ
   hMobilityStressFactorXY
eTensorMobilityFactorXX eTensorMobilityFactorYY
   eTensorMobilityFactorZZ
hTensorMobilityFactorXX hTensorMobilityFactorYY
   hTensorMobilityFactorZZ
}
```

In Plot section are placed the data that are saved at the end of the simulation to the Plot file specified in File section.

Math section

```
Math
{
coordinateSystem { UCS }
-CheckUndefinedModels
Surface "S1" ( MaterialInterface="HfO2/Oxide")
AutoOrientationSmoothingDistance = -1
* use previous two solutions (if any) to extrapolate next
Extrapolate
* use full derivatives in Newton method
Derivatives
* control on relative and absolute errors
-RelErrControl
* relative error= 10^(-Digits)
```

```
Digits=5
* absolute error
Error(electron)=1e8
Error(hole)=1e8
* maximum number of iteration at each step
Iterations=100
* solver of the linear system
Method=ParDiSo
* display simulation time in 'human' units
Wallclock
* display max.error information
CNormPrint
* to avoid convergence problem when simulating defect-assisted
   tunneling
NoSRHperPotential
StressMobilityDependence=TensorFactor
RHSmin=1e-12
CheckRhsAfterUpdate
Number_of_Threads = 4
}
```

The Math section contains all the commands necessary to perform the calculations of the equations used in the solve section.
CoordinateSystem specifies the coordinate system that is used for explicit coordinates. The unified coordinate system (UCS) uses the convention of the simulation coordinate system as established by Sentaurus Process[10]. Drift-diffusion or hydrodynamic simulations activate the checking mobility models ConstantMobility and DopingDependence. This checking procedure can be switched off by the keyword - *CheckUndefinedModels*[10].
Surface defines a surface with name "S1" and it is the union of the interfaces HfO_2/Oxide.
By default, the switch from one parameter set to another when using auto-orientation occurs abruptly. To enable a smooth transition between different parameter sets, it must be specified a nonzero value for the auto-orientation smoothing distance. Specifying $AutoOrientationSmoothingDistance < 0$ uses the average interface vertex spacing as the smoothing distance[10].
Extrapolate actives linear extrapolation to predict the next solution based on the values of the previous solutions.
The *Coupled* command in Solve section activates a Newton-like solver over a set of equations. *Derivatives* command actives full derivatives, in this way Newton's iterations converge better.
Convergence of a solution in Sentaurus Device is determined by calculating and examining the following quantities at each Newton iteration[10]

- RHS norm is the norm of the right-hand-side (that is, the residual of the equations).

- Update error is a measure of the updates to the equation variables.

Moreover *Coupled* depends on:

- *Iterations* sets the default number of iterations for *Coupled* command.
- *Digits* are the number of relative error digits
- When *-RelErrControl* is set, if the error is < 1, the solution is considered converged.
- *Error* define the absolute error for hole and electron.
- if RHS norm is less than *RHSmin* the solution is considered converged.
- *CheckRhsAfterUpdate* forces Sentaurus Device to perform an additional check on the RHS norm after the update error criteria is satisfied. In this way the problems of convergence are reduced.

Method=ParDiSo selects the linear solver PARDISO.
The keyword *Wallclock* is used to display clock times rather than CPU times.
CNormPrint prints instance equation errors per Newton step.
The inclusion of defect-assisted tunneling may lead to convergence problems. The flag *NoSRHperPotential* avoids convergence problem when simulating defect-assisted tunneling.
StressMobilityDependence=TensorFactor activates stress tensor applied to low-field mobility. In this case, the dependency of saturation velocity on stress is given by $v_{sat,i} = v_{sat,0} \cdot (1 + \alpha \cdot t_i)$.
Number_of_Threads activates multithreading. In this case, four threads are used.

Solve section

```
Solve
{
* EQUILIBRIUM
Coupled(Iterations=100 LineSearchDamping=1e-4) { Poisson
   hQuantumPotential Contact }
Coupled(Iterations=100) { Poisson hQuantumPotential Contact }
* TURN-ON
* increasing VDS to goal
quasistationary (InitialStep = 0.010 MaxStep = 0.05 MinStep=1e-6
Goal {name= "drain" voltage = @Vds@}
)
{coupled {poisson electron hole hQuantumPotential Contact} }
* increasing VGS to goal
quasistationary (InitialStep = 0.010 MaxStep = 0.05 MinStep=1e-6
Goal {name= "gate" voltage = @Vgs@}
```

```
)
{coupled {poisson electron hole hQuantumPotential Contact} }
}
```

The Solve section describes the simulation. In this section the order of the commands is important. Indeed the commands are performed in order.
The *Coupled* command is used to solve a set of equations. The equations considered are the Poisson equation and the equations for quantum corrections. These equation are performed by specifying *eQuantumPotential* (for electrons) and *hQuantumPotential* (for holes). By default, the keywords *Contact* are not required because the Poisson equation also covers the contact domain. If only the Poisson equation is solved, no additional equations are added. Only if additional equations to Poisson appear in a Coupled statement, the contact equations are also added[10].
The *Quasistationary* command is used to ramp a solution from one boundary condition to another. In this commands it is necessary to define the initial step and the maximum and the minimum steps that the simulation can reach. *Goal* indicates on which contact the simulation is applied and which is the voltage at which the simulation must end.

6.1.3 Sentaurus Inspect

Sentaurus Inspect is a software that allows to print graph from the data generated by the other Sentaurus software. Moreover, it is possible to extrapolate parameters from graph such as threshold voltage and the subthreshold swing. Also in Sentaurus Inspect there is a command file. Its name is *inspect_ins.cmd*. To open it, it is necessary to right click on Sentaurus Inspect icon and then to select **Edit Input** → **Commands**. The code in the command file is written below.

```
set out_file n@previous@_des
proj_load "${out_file}.plt"

cv_createDS NO_NAME {n@previous@_des gate OuterVoltage} {
   n@previous@_des drain TotalCurrent} y

catch {open log.log w} log_file
set vt1 [f_VT TotalCurrent_drain]
puts $log_file "Threshold voltage = $vt1 V"
puts $log_file ""

cv_createWithFormula logcurve "log10((-1)*<TotalCurrent_drain>)" A A A
    A
cv_createWithFormula difflog "(-1)*diff(<logcurve>)" A A A A
set sslop [ cv_compute "1/vecmax(<difflog>)" A A A A ]
puts $log_file ""
puts $log_file "sub slop = $sslop A/V"
puts $log_file ""
```

```
ft_scalar VT $vt1
ft_scalar sslop $sslop

close $log_file
script_break
```

set is used in the same way of SProcess, it defines variables.
proj_load load file from which extrapolate data. In this case the data are taken from the *plt* file generated by SDevice.
cv_createDS creates a curve and then it is displayed. The first parameter is the name of the curve (NO_NAME); the second is the dataset on x-axis (OuterVoltage of gate); the third is the dataset on y-axis (TotalCurrent of drain); the fourth is an optional parameter that specifies the axis to use. In this way a trans-characteristic $I_{ds} - V_{gs}$ is realized.
catch memorizes in a variable a command (it is very similar to *set*). In this case *open log.log w* that means opening a the "*log.log*" file in write mode.
From *TotalCurrent_drain* is calculated the threshold voltage with *f_VT* commands and the value is stored in *vt1*.
Then the the value is written in "*log.log*" file with *puts* command. Quotes without anything indicates a blank line.
The SS is calculate by transforming the linear curve in logarithmic, then the first derivative is done and finally the reciprocal number of the maximum of the values on y-axis. For n-ype device there is no need to multiply by "-1". The value of SS is stored in "*log.log*" file.
cv_createWithFormula computes a new curve using the formula applied to the data of the argument curves within the given range. Setting the range to any nonnumeric value (for example, A) instructs Inspect to set no limit in the corresponding direction[27]. The first parameter is the name of the curve; the second is the expression, the third, fourth, fifth and sixth are, respectively x-min, x-max, y-min, y-max that indicate the range for which the formula is applied.
cv_compute computes a scalar using the formula. The first parameter is the formula; the second, third, fourth and fifth are, respectively x-min, x-max, y-min, y-max. It is very similar to *cv_createWithFormula*. *ft_scalar* exports the value of V_{th} and SS to table of Sentaurus Workbench.
The "*log.log*" file is closed with *close* command and *script_break* is used to not close the graph GUI of the curve created with *cv_createDS* command.

CHAPTER 7

Conclusions

The work of thesis is divided in two main topics. The first topic is dedicated to fabrication process to realize various types of finFETs and nanosheet GAAFETs. The similarity between the processes allows to switch from one device to another too much effort and to reduce production costs. In addition, the NS GAAFET grows in height allowing for greater density than finFETs [2].
The second topic is dedicated to the analysis of the devices' performances and their reliability. From the study of the currents, and parameters such as DIBl, SS and threshold voltage, it is evident that the novelty of NS GAAFET is to allow for better performance than finFETs and at the same time reduce the effects due to scalability. Low threshold voltage in NS GAAFET is an advantage to use this device in low power applications. Indeed, in NS GAAFET the V_{th} is about 200 mV lower than the finFET one.
Concerning the ON current, a significant performance improvement can be observed between finFET and GAAFET. In fact, it results an increase of a factor 10.
The introduction of other materials (carbon and germanium) influences the sub-threshold behavior as they introduce impurities into the crystal lattice of the silicon (the SS worsens), but at the same time improve the performance: there is an improvement of I_{on} of a minimum of 20% to a maximum of 60% . From this it can be concluded that the stressed versions are suitable for high performance applications.

7.1 Future Work

The popularity of mobile devices made possible by the VLSI circuits joined the needs of boosting computational power and energy efficiency [2]. The always-on-standby devices such as smartphones require ultra-low-power systems, keeping the industry searching for better transistors. An idea for a future work could be to scale even more the size of a GAAFET and consider all the resulting effects (manufacturing processes, short

channel effect ...).
With regard to standby consumption, the simulation of the devices is assuming an increasingly important role, especially in the analysis of subthreshold behavior.
On the other hand, even the preliminary step of simulating manufacturing processes is assuming an increasingly fundamental role as the continuous scaling process is leading to exaggerated manufacturing costs and increasingly impacting variations in the performance of integrated circuits.

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