POLITECNICO DI TORINO

MASTER'S THESIS

Analysis and development of a low-power Capacitive Power Transfer AC-DC adapter

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Abstract

The scientific context in with the thesis project takes place, is that of Capacitive Power Transfer (CPT) and power converters. Capacitive Power Transfer system is an emerging field in the area of Wireless Power Transfer (WPT) and appears as an alternative to the widespread Inductive Power Transfer (IPT) technology.
In recent decades, with the advent of vehicle electrification, the Wireless power transfer (WPT) area and in particular the CPT technology has once again become the subject of study for the benefits it could bring to the sector. As the area is still in its infancy, the first part of this thesis is dedicated to an extensive study on the literature available on the CPT and the basic operation of the system.

The main aim of the thesis, is to develop an AC-DC prototype adapter for low power applications.
One of the main problems of CPT technology can be identified in the low coupling capacitance between the plates of the capacitive interface. This turns out to be the main disadvantage in Wireless power transfer applications, in which the transmitting and receiving parts of energy are physically separated from each other. However, in the area of power converters it is not necessary to design the capacitive interface plates and therefore by using discrete capacitors it is possible to eliminate the problem of low coupling capacitance.
The operating principle of CPT is instead used to create a galvanically isolated converter through the use of discrete capacitors and thus avoiding the use of transformers.

All the work has been carried at Politecnico di Torino with the collaboration of STMicroelectronics Catania.

Thesis Outline

The thesis is divided in five main parts:

The first part is devoted to a brief introduction on the CPT technology, with particular emphasis on the structure of the system and an initial comparison with inductive power transfer(IPT), focusing attention on the advantages/disadvantages of the technology and main applications.

The second part concern the analysis of the circuit, highlighting all the equations and simplifications used to design the system.

The third part of the thesis exposes all the step used to find components values of the circuit following the design specifications and the equations found in previous section.

The fourth part expose illustrates the simulation results of the circuit, making a comparison between the ideal components simulation and real components simulation.

Last part presents the PCB layout of the board and the exprimental results obtained in the laboratory.
The conclusion about the achievement obtained and future development are finally presented.

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Chapter 1

Introduction

The theory of transferring power without wires was first formulated and demonstrated by Nikola Tesla in the early 1900's.
In the recent decade, the transfer of electricity without wires has been an important challenge for researchers.

The advantage of wired power delivery is that the system is widely used and well established. As this technlogy has been around for a long time highly efficient and reliable systems have been developed. Nowadays the wired technology is less expensive and can be used with every power level.
However, there are some drawbacks when it comes to the use of wired power. At higher power levels, the cables/power chords are heavy and expensive. Another problem of the cables is that they can be damaged. The possibility of electrical hazard caused due to rain, snow or humid environment is eminent [1].

Wireless Power Transfer (**WPT**) can provide convenient and safe solutions compared to wired methods.
Two methods of WPT have been developed: **Inductive Power Transfer** (**IPT**), **Capacitive Power Transfer** (**CPT**).

For almost a century wireless transfer of power has been carried out with the help of magnetics(coils and cores), hence the term inductive power transfer (IPT). The use of magnetics made the system versatile to transfer power across small and large air-gaps. IPT systems work on the principle of electromagnetic induction.

The CPT technology is the dual of the conventional IPT technology. The CPT system uses electric fields to transfer power. Historically, CPT was applied in low power applications to deliver power across an inherently small gap [1].

The block diagram of CPT and IPT systems is the same fig.1.1, the only differences can be identified in the coupling elements(capacitors for CPT and inductors for IPT) and in the compensation networks. Inductive matching networks are used in a CPT system and capacitive matching networks are used in IPT system to establish resonances with the coupler.

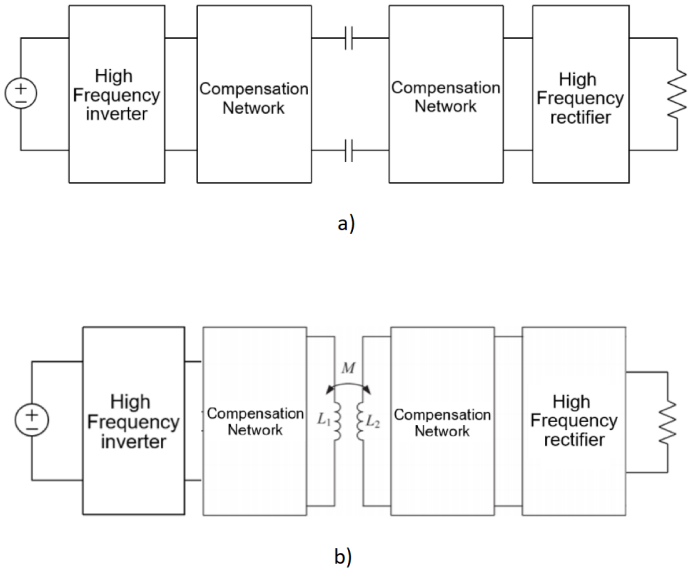

FIGURE 1.1: a) CPT typical structure. b) IPT typical structure

Currently, IPT is mostly favoured for short distance WPT beacuse of low frequency requirement and high power density.
Nevertheless, CPT systems are demonstrated recently delivering kWs of power allowing CPT to be considered for many applications.

Compared to the conventional IPT technology, the CPT system mainly has three advantages [2]:

- Negligible eddy-current loss
- Low cost and weight
- Good misalignment performance

First, in an IPT system, the high-frequency magnetic fields can generate eddy-current losses in the nearby metal, causing significant temperature rise in both low and high power applications.

However, in a CPT system, there is no concern about the eddy-current loss.

Second, in an IPT system, the inductive coupler contains two coils that work as a loosely coupled transformer. Since the coupling coefficient is usually very small, we need to increase the current circulating in the coils to transfer enough power. Considering the skin depth of the conductor at very high frequency, a large amount of Litz-wire is required to build the coils, which increases the system cost and weight. In addition, the conductive losses in the coil can be significant in high power application.
CPT does not require the use of ferromagnetic material (e.g. ferrites) to improve coupling. Instead of expensive Litz wire, low cost metal plates (typically aluminum plates) are utilized to establish the field. This leads to comparatively lower system cost and less weight than in IPT couplers, and allows miniaturization of CPT couplers for small-gap applications [2].

Third, the experimental results show that the CPT system has much better misalignment performance than the IPT system [2].

The recent CPT technology still needs a long way to mature, there are some limitations to overcome:

- Low power density
- Low efficiency
- Strong electric field emissions

The main drawback of the CPT system is low coupling capacitance between plates (typically in pF range), which requires frequency in MHz range to reduce the reactance of coupling capacitors. The power of switching inverters operating in MHz range is still limited to low kW and sub-kW range, and boosting that power it is an active area of research.

Second, the power loss in a CPT system mainly comes from the conductive loss and core loss of the compensation inductors. Since the switching frequency is usually higher than 1 MHz, the skin effect of the wire becomes apparent and extra losses can be induced. If the switching frequency increases even further, the power losses can be more significant.

Third, in an IPT system, the magnetic fields can be easily shielded by ferrite and aluminum plates, and the leakage fields to the surrounding area can be reduced below safety level. However, the electric field emission in a CPT system is difficult to be shielded, because the electric fields can easily pass

	CPT	IPT
Pros	low cost and weight Negligible eddy-current loss Good misalignment performance	High power density trasmission Higher efficiency Field emissions easily shielded
Cons	Low power density transmission Lower efficiency Strong electric field emissions	High system cost and weight Eddy-current losses

TABLE 1.1: CPT vs IPT

through metal [2].

All these pros and cons are summarized in the table 1.1.

1.1 Main Applications

WPT is applied across multiple domains. It is applied in consumer electronics (cellphone charging), transportation electrification (static and dynamic Electric Vehicles (EVs) charging), bio-medical implants (powering life-critical devices), unmanned vehicle charging (underwater and aerial), space power transfer (sending power from Space to Earth) [1].

Two main applications can be identified when we are talking about CPT:

- Electric vehicle charging: High power, Wireless power transfer
- Power adapter: middle power, Galvanic isolation

In **EV charging applications**, an example is shown in fig.1.2 , transmitter and receiver sides are separated and usually the system deals with high power levels. Therefore the metal plates of the capacitive interface needs to be designed in order to transfer a certain power.

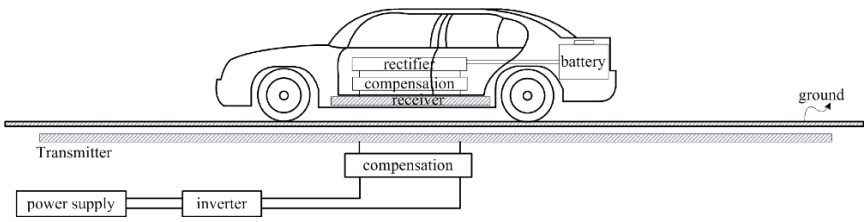

FIGURE 1.2: EV Charging with CPT

The design of the metal plates have to take into account not only the distance but also the problem of misalignment in order to ensure best efficiency and high transfer power.

In **Power adapter** application instead, the transmitter and receiver are in the same PCB/boards and the power is relatively low, for this reason the capacitive interface can be replaced with discrete capacitors. Galvanic isolation is obtained without using transformer or other types of Inductive methods.

The structure of the circuit and the design of it is the same for both applications, the only different procedure is in the particular case of adapter where the capacitive coupling interface does not need to be designed.

1.2 Thesis objectives

The main objective of the thesis work is to take advantage of CPT technology in order to implement a galvanically isolated power converter. Nowdays, the market of isolated power converters is dominated by inductive coupled solutions, where the use of transformers is inevitable. With capacitive coupling principle is possible to realize smaller and lighter converters that could replace, in the future, those based on transformers.
An isolated power converter isolates the input from the output by electrically and physically separating the circuit into two sections preventing direct current flow between input and output. A result of isolation is that each of the isolated circuits has its own return or ground reference.
There are several cases where an isolated power supply may be required or provide some benefit in an application, the main adavantage is safety compliance. For converters powered from high and potentially hazardous voltages(such as ac-dc converters powered from ac mains) isolation separates the output from dangerous voltages on the input.

The first part of this thesis is dedicated to an extensive study on the literature available on the CPT systems and the basic operation of the system.
The second part, on the other hand, is focused on the design, simulation and development of a 40W isolated AC-DC adapter using the CPT technology and based on the topology found in [3]. The input voltage is the rectified 50Hz 220V of the main which is converted to 20V of typical laptop adapters range. The idea is to verify the feasibility of the project and define a design methodology.

The objectives of the thesis can be therefore summarized into six points:

- Detailed study on Capacitive Power Transfer technology, highlighting the main advantages and disadvantages.
- Complete circuit analysis of a CPT system suitable for the design of 40W power adapter.
- Definition of a design methodology to derive all the components of the circuit.
- Performation of ideal and real components simulations in order to verify the correctness of equations.
- Design of the PCB layout.
- Experimental results

Chapter 2

CPT Technology

Capacitive Power Transfer(**CPT**) utilizes high frequency electric fields to transfer power. In fig. 2.1 is presented the general structure of a CPT system [2], that can be used for every application.

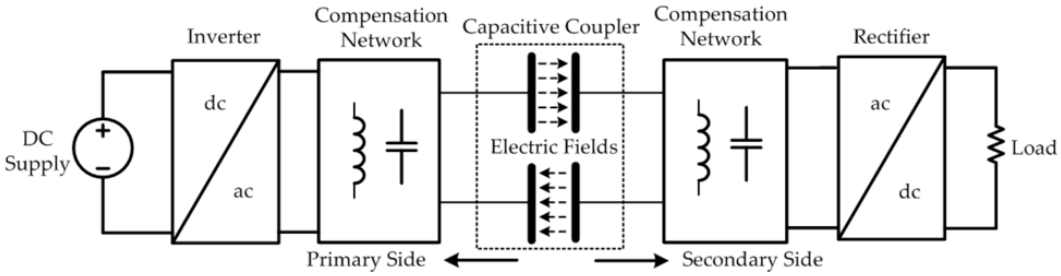

FIGURE 2.1: CPT Typical Structure [2]

Four main block can be identified:

- **Inverter**: converts DC into AC
- **Compensation networks**: both on the primary and secondary side, used for Input/Output matching and for allowing it works at the operational resonance.
- **Capacitive coupler**
- **Rectifier**: converts AC into DC, it is usually a 4-diodes full-wave rectifier, but active rectifiers can also be used to increase the efficiency.

A DC input voltage is converted to a high frequency AC voltage which is then supplied to two primary metal plates. When two secondary plates are placed close to them, an alternating electric field is formed between the plates thus the displacement current can 'flow' through.
As a result, power can be transferred to a DC Load via a rectifier without

direct electrical contacts.

All the discussion about the CPT of this chapter are made considering the general case in which the capacitive interface is not a discrete capacitor, and so the mutual capacitance is affected by design problems of misalignment and distance.
In the other chapters of the thesis, as it concerns the design of a low power adapter, all the issues about mutual coupling capacitance, misalignment and distance, related to the design of the capacitive coupler, will not be considered.

2.1 Fundamental Working Principle

The fundamental challenge in CPT comes from the tradeoffs between the **transfer distance**, **power**, and **efficiency**. Current CPT systems cannot achieve long distance, high power, and high efficiency simultaneously. Their performance is still not comparable with the IPT systems, so their application area has been limited. When the transfer distance reaches hundreds of mm, the coupling capacitance is small. This makes it difficult to achieve high power transfer efficiently, especially for electric vehicle charging applications.

If the transfer distance is increased, the coupling capacitance decreases and the switching frequency has to be increased to transfer sufficient power. However, the switching losses in active components, such as input inverter MOSFETs, increase with the frequency. Therefore, the overall efficiency is still limited.

To analyze its fundamental working principle, the structure of a CPT system can be further simplified as in Fig.2.2 [2].

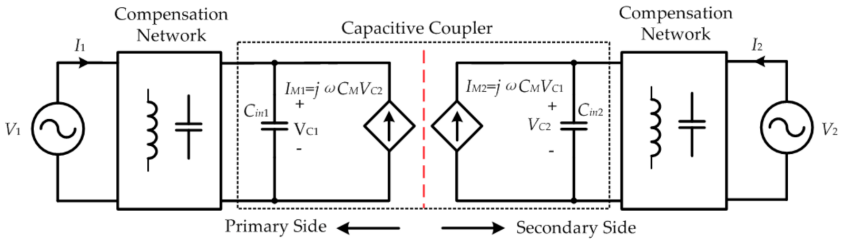

FIGURE 2.2: CPT system basic model

The input and output sides are represented by two sinusoidal sources V1 and V2, neglecting the high-order harmonics in the circuit.
The capacitive coupler is replaced by a voltage controlled current source that

depends on CM, the mutual coupling capacitance. In a capacitive coupler, there are multiple coupling capacitances between plates, which can increase the complexity of the working principle analysis.

The complex power S_{M1} absorbed by I_{M1} is expressed as:

$$S_{M1} = V_{C1} \cdot \overline{(-I_{M1})} = V_{C1} \cdot \overline{(-j\omega C_M V_{C2})}$$

S_{M1} is a complex power, including real and imaginary part defined as P_{M1} and Q_{M1}.
The primary voltage V_{C1} is selected as the reference phasor, and the phase difference of V_{C2} is defined as θ, resulting [2]:

$$V_{C2} = |V_{C2}|(\cos\theta + j\sin\theta) \tag{2.1}$$

$$S_{M1} = P_{M1} + jQ_{M1} = \omega C_M |V_{C1}||V_{C2}| \sin\theta + j\omega C_M |V_{C1}||V_{C2}| \cos\theta \tag{2.2}$$

$$\begin{cases} P_{M1} = \omega C_M |V_{C1}||V_{C2}| \sin\theta \\ Q_{M1} = \omega C_M |V_{C1}||V_{C2}| \cos\theta \end{cases} \tag{2.3}$$

the active power is further defined as $P_M = P_{M1} = P_{M2}$ and the reactive power $Q_M = Q_{M1} = -Q_{M2}$.

Therefore, in a practical system design, the phase angle theta can be designed to be closed to 90°. In this way, the reactive power circulating in the circuit is almost reduced to zero, and the corresponding conduction loss is also minimized.
Equation (2.3) shows also that the system power is proportional to the switching frequency ω, the mutual coupling capacitance C_M and the voltage V_{C1} and V_{C2} of the metal plate.

In fig.2.3 is reported the system power as function of the plate voltage and frequency considering the factor $\sin\theta = 1$, the $C_M = 10pF$ and $V_{C1} = V_{C2}$ [2].

2.2 Inverter

An Half bridge inverter is used to convert DC into AC. Figure 2.4 shows the topology of an half-bridge single phase inverter, where two large capacitors are required to provide a neutral point N, such that each capacitor maintains a constant voltage $v_i/2$.
It is clear that both switches S_+ and S_- cannot be on simultaneously because a short circuit across the dc link voltage source v_i would be produced.

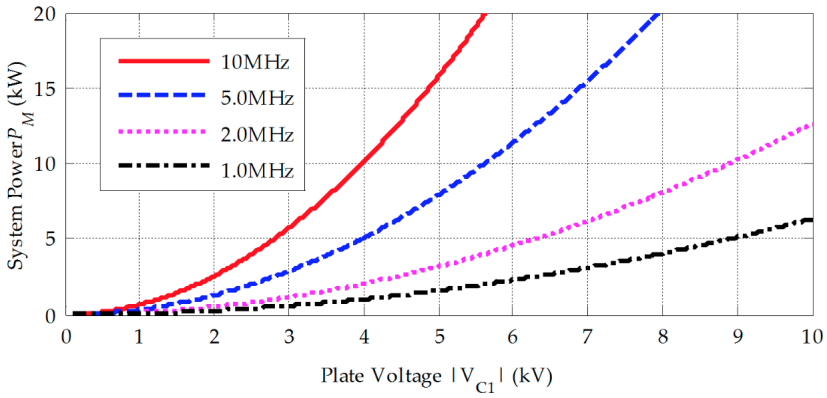

FIGURE 2.3: The maximum achievable system power P_M at different fs and $|V_{C1}|$ when $C_M = 10pF$

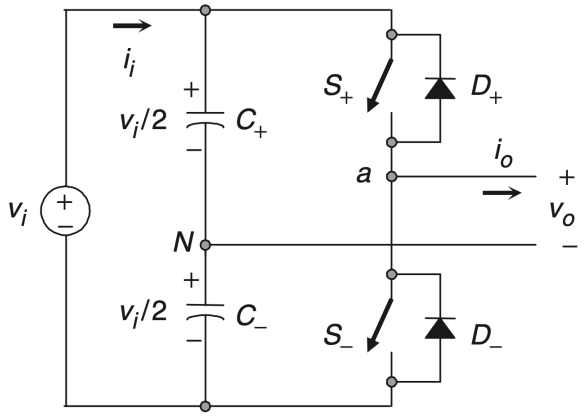

FIGURE 2.4: Single-phase half-bridge inverter

In order to avoid the short circuit across the dc bus and the undefined ac output-voltage condition, the modulating technique should always ensure that at any instant either the top or the bottom switch of the inverter leg is on.
The state of the switches S_+ and S_- are defined by the modulation technique. Since the working frequency of the circuit is in the MHz range, is convenient to use a square-wave modulation technique.

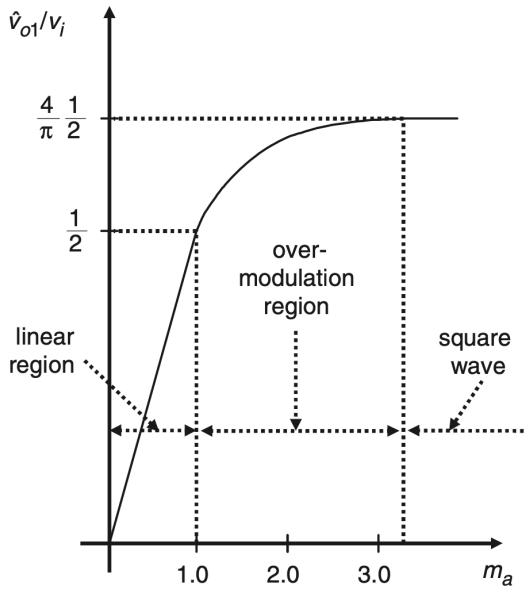

FIGURE 2.5: Modulation regions inverter

2.2.1 Square-wave Modulation Technique

In square wave modulation, both switches S_+ and S_- are on for one half-cycle of the ac output period.

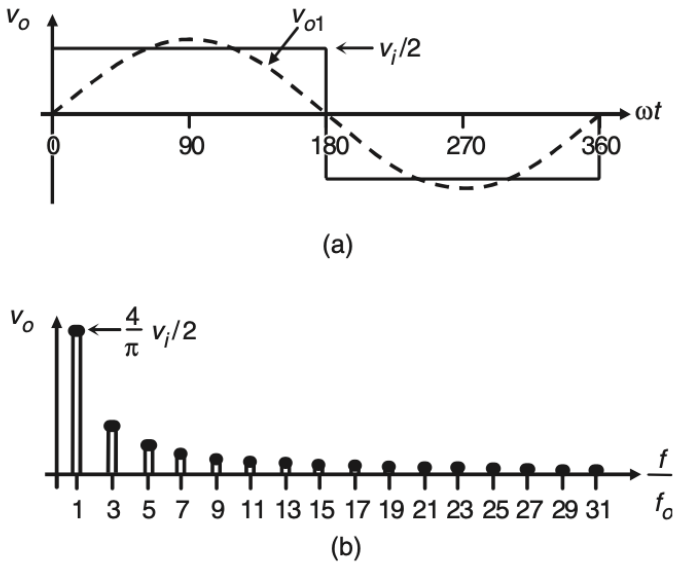

FIGURE 2.6: Square-wave modulation waveform

Fig. 2.6 shows the following: (a) the normalized ac output voltage harmonics are at frequencies h = 3, 5, 7, 9, . . ., and for a given dc link voltage; (b) the fundamental ac output voltage can be expressed in Fourier series:

$$v_o(t) = \sum_{k=odd}^{\infty} \frac{2}{k\pi} v_i \sin(\omega_k t) \tag{2.4}$$

Equation 2.4 states that the square wave can be decomposed into the sum of infinite sine waves, of different frequencies and amplitudes. In particular, it contains only odd harmonics terms.
Due to the selective nature of resonant circuits, all components besides the fundamental can be assumed to be filtered out. Therefore, all higher harmonics are neglected and the circuit waveforms are consequently assumed to be purely sinusoidal at the fundamental frequency.
The output of the inverter can be therefore modeled as a sinusoidal generator with a peak value equal to the one of its fundamental component(k=1):

$$\hat{v}_{o1} = \frac{2}{\pi} v_i \tag{2.5}$$

It can be seen that the ac output voltage cannot be changed by the inverter. However, it could be changed by controlling the dc link voltage v_i.

2.3 Compensation Network

The compensation network is probably the most important and critical block to be designed in a CPT circuit. It determines the power capabilities, the efficiency and the frequency properties of the system.
In full bridge/half bridge inverter based topology the compensation network should be a resonant circuit. It is composed by inductor and capacitor that gives rise to series or parallel resonances.
Some examples of different compensation networks are reported in this chapter [2].

2.3.1 Series L Compensation

In fig.2.7 is reported the simplest compensation network, composed by one inductor at the input and one at the output.

$L1$ and $L2$ are used at both primary and secondary sides to compensate the mutual capacitances C_{M1} and C_{M2}. To reduce the complexity of the secondary side the two inductors can be combined to one and placed at the

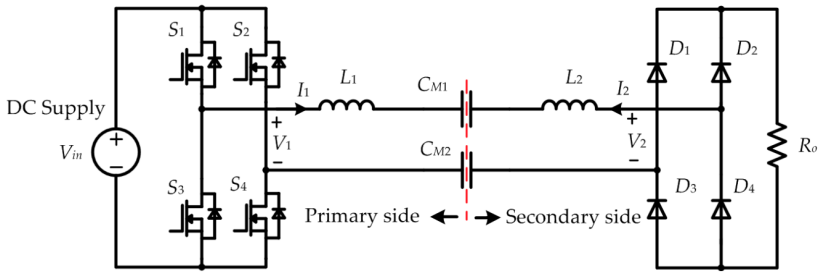

FIGURE 2.7: Series L compensation network

primary side.
The main disadvantages of this simple compensation network is its requirement on inductance size and its sensitivity with parameter variation. The inductors resonate directly with the mutual capacitance C_{M1}/C_{M2}, but the coupling capacitances can be relatively small (tens of pF) and are affected by problems of misalignment and distance of the metal plates.

$$\omega = \frac{1}{\sqrt{LC}}$$

As reported in the formula of the resonance, the smaller the capacitance value, the larger the inductance value and so bigger the inductors size. It is possible to reduce the inductor size increasing the working frequency of the system, but the sensitivity problems remains.

2.3.2 LC Compensation

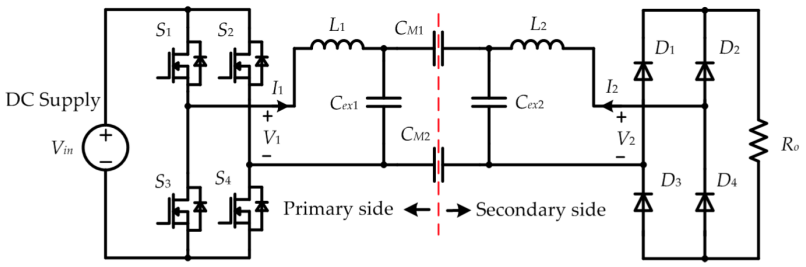

FIGURE 2.8: LC compensation network

In fig.2.8 is presented the LC compensation network. The parallel capacitors C_{ex1} and C_{ex2} are usually much larger than the mutual capacitances C_{M1} and C_{M2}, which dominates the equivalent capacitance of the network. The

inductor $L1$ and $L2$ resonate with the equivalent capacitances at the primary and secondary sides, respectively.
Since the capacitance increases, the required inductances $L1$ and $L2$ decreases, so as their size and volume. In addition, the resonance of the system is not sensitive to distance and misalignment variations in the capacitive coupler.

2.3.3 LCL Compensation

In fig.2.9 is presented the LCL compensation network.
The series inductances L_{s1} and L_{s2} compensate only parts of the mutual

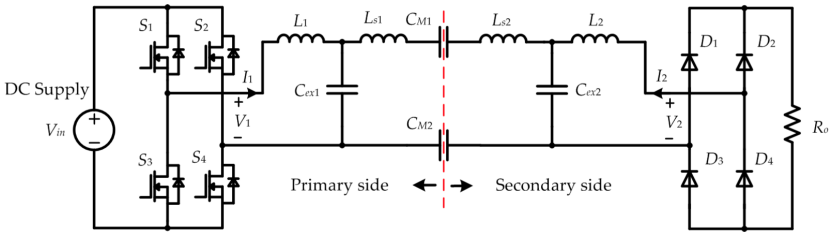

FIGURE 2.9: LCL compensation network

capacitances C_{M1} and C_{M2}, and the remaining parts are compensated by the LC network. It can provide the flexibility to tune the system power through designing the inductance ratio $L1/L_{s1}$, so as the ratio of $L2/L_{s2}$.
There is the same disadvantage of the L series structure(L_{s1} resonate with C_{M1}) and so high value of series inductances L_{s1} and L_{s2}.

2.3.4 LCLC Compensation

Two extra LC network L_{f1}-C_{f1} and L_{f2}-C_{f2} are used at the primary and secondary side to convert the voltage $V1$ and $V2$ into current sources for the resonant circuits. There are multiple resonances in the circuit, for example C_{f1} can resonate with both L_{f1} and $L1$, which are used to increase the voltage in the capacitive coupler for sufficient power transfer.

The system power can be regulated through circuit parameter design without affecting the coupling coefficient.
The disadvantage of this configuration is the complexity of the circuit, mainly due to the multiple resonances.
Since there are a lot of passive elements, also the system cost and weight is then increased and the losses on this components can reduce drastically the efficiency.

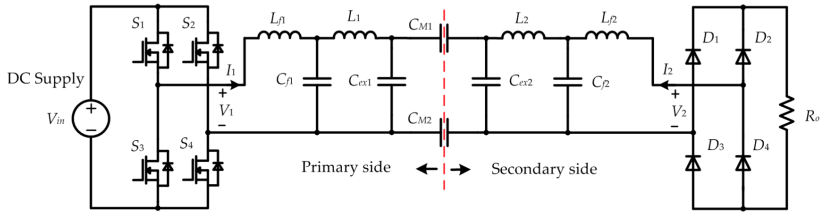

FIGURE 2.10: LCLC compensation network

2.4 Capacitive Interface

Different structures of capacitive couplers are explored so far to provide a high-power, efficient, and compact CPT design.
The capacitive coupler consists of multiple metal plates that are used to generate electric field to transfer power.
There are coupling capacitance between each pair of plates that determine the power transfer performance.
Since the goal of the thesis is to design a CPT adapter, discrete capacitors are used for the capacitive interface. In order to have a complete overview of the topic, some examples of capacitive interface structures are reported [2].

2.4.1 Two-Plate Structure

It is also called unipolar structure. The mutual capacitance between the two plates provides the path for the current to flow forward to the load, and a conductive path is then required to allow the current flowing back to the primary side.

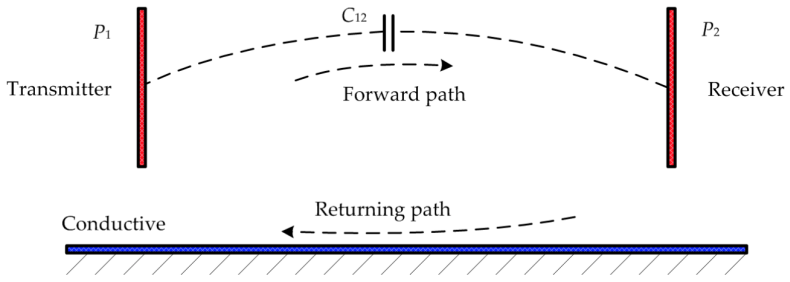

FIGURE 2.11: Two Plate(unipolar) structure [2]

The advantage of the two-plate structure is the simplicity. Can be applied both in short and long distance applications.

2.4.2 Four-Plate Parallel Structure

This is the most common way to realize a capacitive coupler, it can also be called a bipolar structure. As reported in fig.2.12, there is a coupling capacitance between each pair of plates, totally resulting in six capacitances: C_{13} and C_{24} are defined as main coupling capacitance [2].

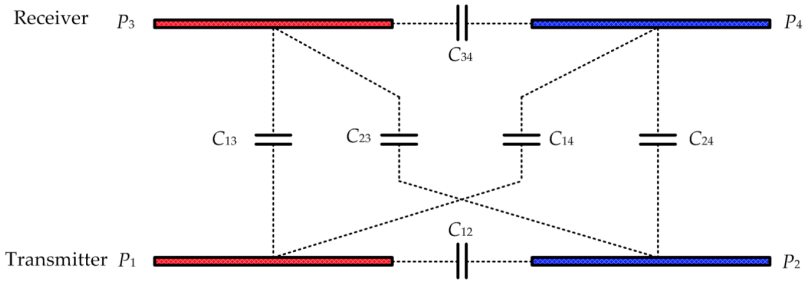

FIGURE 2.12: Four-Plate parallel structure [2]

When the plate are well-aligned and the plate distance is short, the main couplings dominate the capacitive model and the other coupling can be neglected to simplify the circuit analysis. However when the plate are misaligned and the plate distance is long, the cross couplings are relatively large and they need to be considered in the circuit analysis [2].

$$\begin{cases} C_M = \frac{C_{24}C_{13}-C_{14}C_{23}}{C_{12}+C_{24}+C_{14}+C_{23}} \\ C_{in1} = \frac{(C_{13}+C_{14})(C_{23}+C_{24})}{C_{12}+C_{24}+C_{14}+C_{23}} + C_{12} \\ C_{in2} = \frac{(C_{13}+C_{23})(C_{14}+C_{24})}{C_{12}+C_{24}+C_{14}+C_{23}} + C_{34} \end{cases} \tag{2.6}$$

Since the six-capacitance model is very complicated, the equivalent behavior source model(fig.2.13) is used to design the four-plate structure.

2.4.3 Four-Plate Stacked Structure

To increase the self-capacitances and eliminate the external capacitances, the primary plates P1 and P2 are placed closed to each other, similarly for P3 and P4.

The coupling model of this stacked structure is the same of the Four-plate parallel structure.

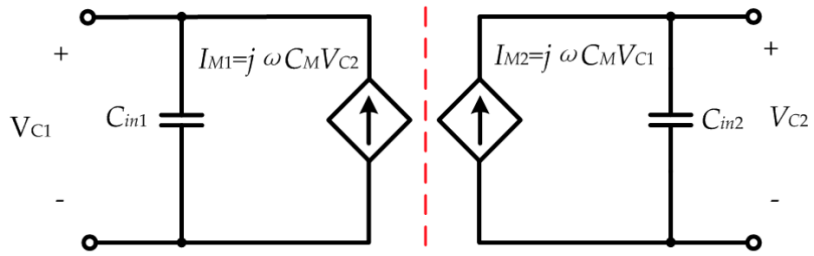

FIGURE 2.13: Equivalent source model of four-plate structure [2]

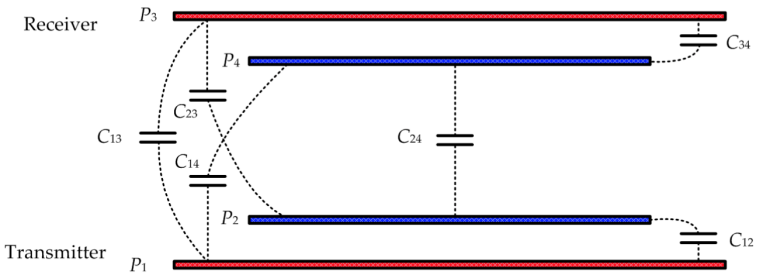

FIGURE 2.14: Four-Plate stacked structure [2]

Compared to the parallel structure, the stacked is more compact and robust to angular misalignment. However, one limitation is on the relatively small mutual capacitance. Since the structure is compact, C_{14} and C_{23} are increased. According to the equation (2.6) C_M is therefore reduced.

2.4.4 Six-Plate Structure

The plates P1, P2, P3, P4 work as active plates to transfer power, and the plates P5, P6 work as auxiliary plates to increase the equivalent self-capacitance and serve as electric field shielding.

2.4.5 Electric Field Repeater

Fundamental when the transfer distance need to be further increased. For example the four-plate structure(bipolar) can be used to realize a repeater system as shown in fig.2.16.

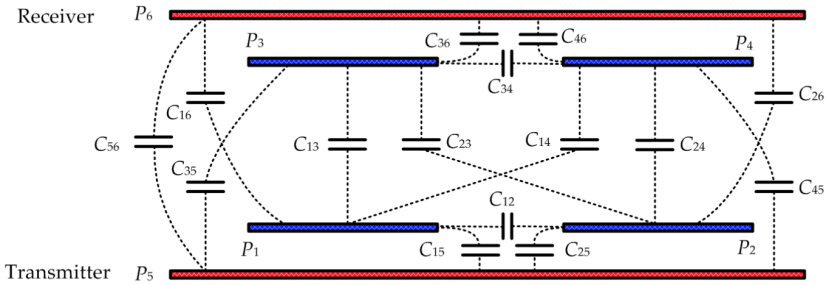

FIGURE 2.15: Six-Plate structure

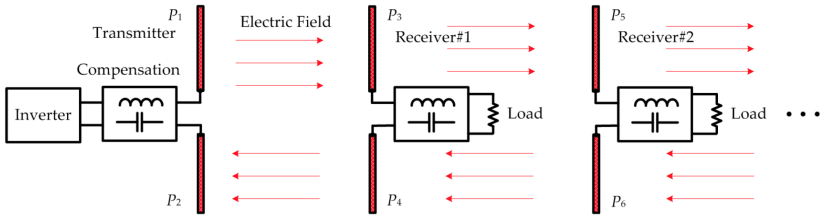

FIGURE 2.16: Electric field repeater system based on a four-plate structure

The most critical challenge in a repeater system is the transfer efficiency. Especially in a long-distance application, when the number of repeater stage increases, the power loss in the system could increase dramatically.

2.5 Rectifier

There are two types of single-phase full-wave rectifier, namely, full-wave rectifiers with center-tapped transformer and bridge rectifiers. In the CPT circuit considered in this thesis there is no possibility of a center-tapped configuration, for this reason a bridge rectifier topology should be used.

Employing four diodes instead of two, as shown in fig.2.17 it can be possible to provide full-wave rectification without using a center-tapped transformer. During the positive half- cycle of the transformer secondary voltage, the current flows to the load through diodes D_1 and D_2. During the negative half-cycle, D_3 and D_4 conduct.

The voltage and current waveforms of the bridge rectifier are shown in fig.2.18. During its conducting state, each diode has a forward current which

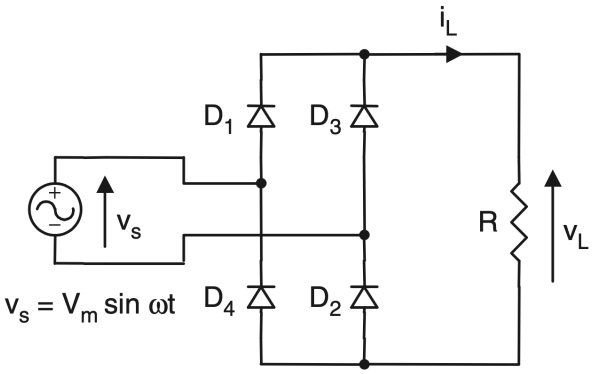

FIGURE 2.17: Bridge Rectifier

is equal to the load current and the peak inverse voltage of the diodes is equal to V_m during their blocking state.

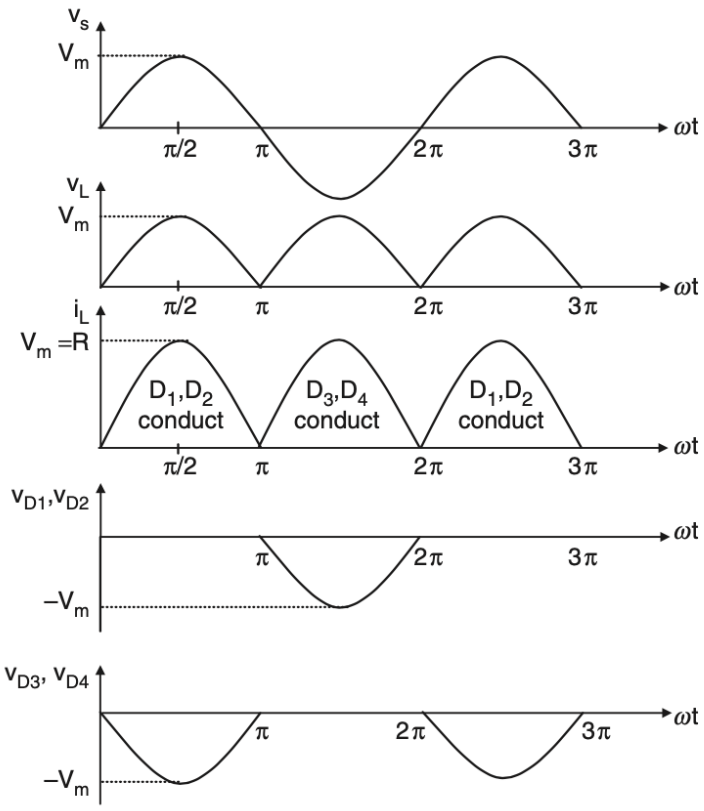

FIGURE 2.18: Voltage and current waveform of bridge rectifier

The average value of the load voltage v_L is V_{DC} and it is defined as:

$$V_{DC} = \frac{1}{T}\int_0^T v_L(t)\,dt = \frac{1}{\pi}\int_0^\pi V_m \sin\omega t\, d(\omega t) = \frac{2V_m}{\pi} \tag{2.7}$$

The root mean square value(RMS) can be calculated:

$$V_{LRMS} = \sqrt{\frac{1}{\pi}\int_0^\pi (V_m \sin\omega t)^2\, d(\omega t)} = \frac{V_m}{\sqrt{2}} \tag{2.8}$$

In order to reduce the output ripple it will be placed a capacitor in parallel to the load resistance R.

Chapter 3

Complete Circuit Analysis

This chapter of the thesis is devoted to the presentation and analysis of the CPT circuit used to design the power adapter. The final circuit that it will be analyzed is shown in fig.3.1 and it is based on the scheme proposed in [3].

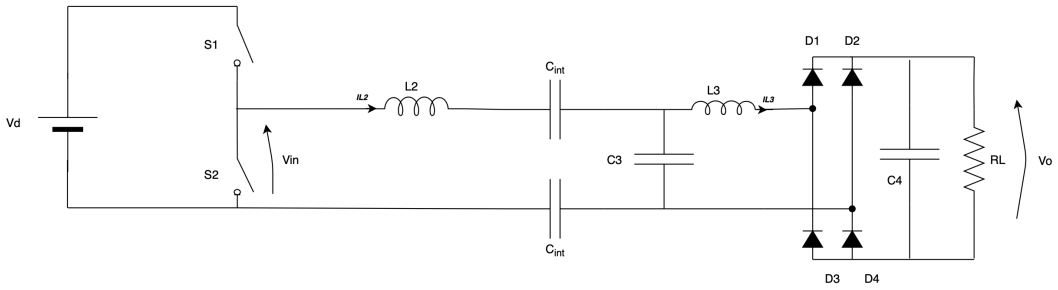

FIGURE 3.1: Final CPT scheme

In the next paragraphs the compensation network will be studied and all the equations useful for the design of the passive network will be derived. But some simplification will be made to understand and analyze its operation.

3.1 Simplifications

The simplified equivalent circuit is presented in fig.3.2, this is a simple linear circuit, which can be studied using standard AC analysis.
The simplifications implemented are briefly explained below.

3.1.1 Output voltage simplification

The first simplification is related to the output voltage of the inverter(correspond to the the input voltage of the compensation network) that is a square wave. As reported in the previous chapter equation(2.4), it can be approximated with a sinusoidal waveform neglecting all the higher harmonics and the peak value of the fundamental can be expressed as:

$$V_{in1} = \hat{V}_{in} = \frac{2V_d}{\pi} \tag{3.1}$$

3.1.2 Diode bridge simplification

The second simplification is related to the output section and in particular to the diode bridge rectifier and the load. They can be replaced with an equivalent AC resistance R_e(this simplification derive from the equivalence of power before and after the bridge (3.2)).

$$\begin{cases} P_o = R_e I_{oRMS}^2 = R_e \left(\frac{I_{opk}}{\sqrt{2}}\right)^2 = R_L I_o^2 \implies R_e = \frac{8}{\pi^2} R_L \\ I_{opk} = \overline{I_o} \frac{\pi}{2} \end{cases} \tag{3.2}$$

3.1.3 Compensation network simplification

The third simplification is in the capacitive interface C_{int}. The series combination of the two interface capacitances has been replaced by $C_2 = \frac{1}{2} C_{int}$.

The fourth simplification is the simple decomposition of the series inductor L_2 in L_{2a} and L_{2b}.

- L_{2a} compensates the reactance of the capacitive interface C_2.
- L_{2b}, along with L_3 and C_3 form the LLC network that define the circuit operation.

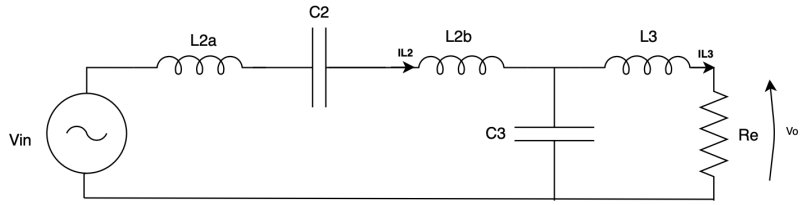

FIGURE 3.2: Simplification of the complete CPT scheme

3.2 Compensation Network Analysis

3.2.1 Resonances

The system works with two resonant networks that can reduce the switching losses in the power conversion circuit.
As indicated in fig.3.3 the first is in the N_2 network between L_{2a} and the equivalent capacitive interface C_2.

$$\omega = \frac{1}{\sqrt{L_{2a}C_2}} \tag{3.3}$$

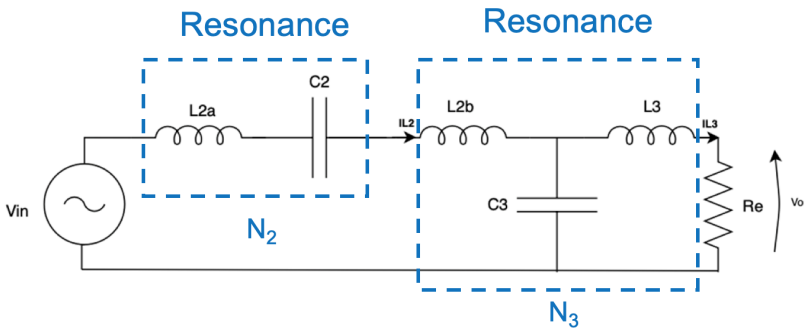

FIGURE 3.3: Resonances of network N_2 and N_3

The second in the network N_3 between C_3 and the parallel combination of

L_3 and L_{2b}.

$$\omega = \frac{1}{\sqrt{(L_{2b} \parallel L_3)C_3}} = \frac{1}{\sqrt{L_{comb}C_3}} \tag{3.4}$$

The circuit needs to be designed so that the two resonances occur at the same frequency [2].

$$\omega = \frac{1}{\sqrt{L_{2a}C_2}} = \frac{1}{\sqrt{L_{comb}C_3}}$$

3.2.2 Network Analysis

In this section the compensation network is analyzed in order to find a relationship between impedances, input and output voltages and currents. Since the system is studied under the first harmonic approximation, all current and voltage waveforms are considered to be sinusoids ringing at the resonant frequency. Therefore, the circuit analysis can be done using current and voltage phasors.

The impedances of inductors and capacitors can be written as:

$$Z_{L3} = j\omega L_3 \tag{3.5}$$

$$Z_{L2b} = j\omega L_{2b} \tag{3.6}$$

$$Z_{C3} = -\frac{j}{\omega C_3} \tag{3.7}$$

Supposing to work at the resonant frequency and to apply the resonant condition (3.3), the series impedance $L_{2a} - C_2$ can be approximated with a short circuit. With this simplification, fig.3.4, the input voltage V_{in} is applied to the LCL network N_3.
At this point the aim is to find the impedance seen by the generator Vin, in this way is possible to derive the current $I_{C2} = I_{L2} = \frac{V_{in}}{Z_{LCL}}$. Once I_{L2} has been calculated, the current I_{L3} can be found through the current divider formula.

The first step is to calculate the impedance of $R_e - L_3 - C_3$ network:

$$Z_{LC} = (Z_{L3} + R_e) \parallel Z_{C3}$$

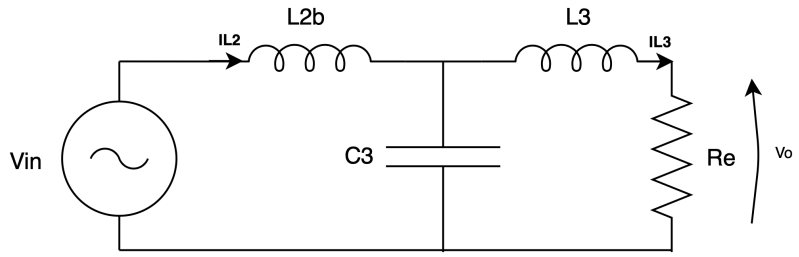

FIGURE 3.4: Simplification of the circuit at the resonant frequency

replacing (3.7) and (3.5):

$$Z_{LC} = \frac{(j\omega L_3 + R_e)\left(-\frac{j}{\omega C_3}\right)}{(j\omega L_3 + R_e) + \left(-\frac{j}{\omega C_3}\right)} = \frac{\frac{L_3}{C_3} - j\frac{R_e}{\omega C_3}}{R_3 + j\left(\omega L_3 - \frac{1}{\omega C_3}\right)} \tag{3.8}$$

The total impedance of the N_3 network:

$$Z_{LCL} = Z_{LC} + Z_{L2b}$$

replacing (3.8) and (3.6):

$$Z_{LCL} = \frac{\frac{L_3}{C_3} - j\frac{R_e}{\omega C_3}}{R_e + j\left(\omega L_3 - \frac{1}{\omega C_3}\right)} + j\omega L_{2b} \tag{3.9}$$

It is possibile to highlight the dependance on the equivalent inductance $L_{comb} = L_3 \parallel L_{2b}$ by multiplyng and dividing by $L_{2b} + L_3$. Substituting the resonance condition (3.4) some terms reduces to zero and the impedance is simplified to:

$$Z_{LCL} = \frac{j\left(\omega L_{2b} R_e - \frac{R_e}{\omega C_3}\right)}{R_e + j\left(\omega L_3 - \frac{1}{\omega C_3}\right)}$$

Multiplyng and dividing by the complex conjugate of the denominator and ordering the terms:

$$Z_{LCL} = \frac{R_e\left(\omega L_{2b} - \frac{1}{\omega C_3}\right)\left(\omega L_3 - \frac{1}{\omega C_3}\right) + R_e^2 j\left(\omega L_{2b} - \frac{1}{\omega C_3}\right)}{R_e^2 + \left(\omega L_3 - \frac{1}{\omega C_3}\right)^2} \tag{3.10}$$

Now it is possbile to divide the impedance in real and imaginary part and calculate magnitude and phase:

$$Re\{Z_{LCL}\} = \frac{R_e\left(\omega L_{2b} - \frac{1}{\omega C_3}\right)\left(\omega L_3 - \frac{1}{\omega C_3}\right)}{R_e^2 + \left(\omega L_3 - \frac{1}{\omega C_3}\right)^2} \tag{3.11}$$

$$Im\{Z_{LCL}\} = \frac{R_e^2\left(\omega L_{2b} - \frac{1}{\omega C_3}\right)}{R_e^2 + \left(\omega L_3 - \frac{1}{\omega C_3}\right)^2} \tag{3.12}$$

$$|Z_{LCL}| = \sqrt{Re\{Z_{LCL}\}^2 + Im\{Z_{LCL}\}^2} = \frac{R_e\left(\omega L_{2b} - \frac{1}{\omega C_3}\right)}{\sqrt{R_e^2 + \left(\omega L_3 - \frac{1}{\omega C_3}\right)^2}} \tag{3.13}$$

$$\angle Z_{LCL} = \arctan\left(\frac{Im\{Z_{LCL}\}}{Re\{Z_{LCL}\}}\right) = \arctan\left(\frac{R_e}{\omega L_3 - \frac{1}{\omega C_3}}\right) \tag{3.14}$$

The current through the capacitive interface C_2 can be expressed as:

$$|I_{C2}| = \frac{V_{in}}{|Z_{LCL}|}$$

Replacing the formula of the Z_{LCL} amplitude (3.13) previously calculated:

$$|I_{C2}| = V_{in}\frac{\sqrt{R_e^2 + \left(\omega L_3 - \frac{1}{\omega C_3}\right)^2}}{R_e\left(\omega L_{2b} - \frac{1}{\omega C_3}\right)} \tag{3.15}$$

To calculate the current I_{L3} it can be used the current divider formula, knowing $I_{C2} = I_{L2}$:

$$I_{L3} = I_{C2}\frac{Z_{C3}}{Z_{C3} + Z_{L3} + R_e} = I_{C2}F$$

Rename F the current divider factor:

$$F = \frac{\frac{-j}{\omega C_3}}{R_e + j\left(\omega L_3 - \frac{1}{\omega C_3}\right)} = -\frac{\frac{1}{\omega C_3}\left(\omega L_3 - \frac{1}{\omega C_3}\right) + j\frac{R_e}{\omega C_3}}{R_e^2 + \left(\omega L_3 - \frac{1}{\omega C_3}\right)^2} \tag{3.16}$$

Dividing this factor in real and imaginary part:

$$Re\{F\} = -\frac{\frac{1}{\omega C_3}\left(\omega L_3 - \frac{1}{\omega C_3}\right)}{R_e^2 + \left(\omega L_3 - \frac{1}{\omega C_3}\right)^2} \tag{3.17}$$

$$Im\{F\} = -\frac{\frac{R_e}{\omega C_3}}{R_e^2 + \left(\omega L_3 - \frac{1}{\omega C_3}\right)^2} \tag{3.18}$$

It is possibile to calculate the magnitude of the F factor:

$$
\begin{aligned}
|F| &= \sqrt{Re\{F\}^2 + Im\{F\}^2} \\
&= \frac{1}{R_e^2 + \left(\omega L_3 - \frac{1}{\omega C_3}\right)^2} \sqrt{\left(\frac{1}{\omega C_3}\left(\omega L_3 - \frac{1}{\omega C_3}\right)\right)^2 + \left(\frac{R_e}{\omega C_3}\right)^2} \\
&= \frac{1}{\omega C_3 \sqrt{R_e^2 + \left(\omega L_3 - \frac{1}{\omega C_3}\right)^2}}
\end{aligned}
\tag{3.19}
$$

At this point the amplitude of the current I_{L3} can be derived:

$$
|I_{L3}| = |I_{C2}||F|
$$

$$
\begin{aligned}
|I_{L3}| &= V_{in} \frac{\sqrt{R_e^2 + \left(\omega L_3 - \frac{1}{\omega C_3}\right)^2}}{R_e\left(\omega L_{2b} - \frac{1}{\omega C_3}\right)} \cdot \frac{1}{\omega C_3 \sqrt{R_e^2 + \left(\omega L_3 - \frac{1}{\omega C_3}\right)^2}} \\
&= V_{in} \frac{1}{\omega C_3 R_e\left(\omega L_{2b} - \frac{1}{\omega C_3}\right)}
\end{aligned}
\tag{3.20}
$$

With the expression of I_{L3} is possibile to derive all the quantities of the circuit and find the values of inductors and capacitors following the design specifications.
In the next paragraph it will be explained a simpler derivation of the output power expression.

3.2.3 Power analysis

The active power provided by the source is:

$$
P_{in} = V_{in}|I_{C2}| \cos\phi \tag{3.21}
$$

The power factor $\cos\phi$ can be calculated from the impedance triangle(3.5) as:

$$
\cos\phi = \frac{R}{Z}
$$

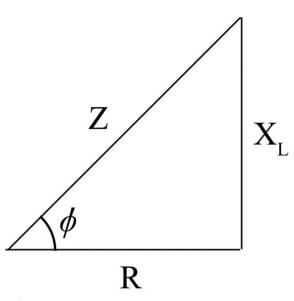

FIGURE 3.5: Impedance triangle

Using the expressions of Z_{LCL} previously calculated (3.11) and (3.13):

$$\begin{aligned}\cos\phi = \frac{Re\{Z_{LCL}\}}{|Z_{LCL}|} &= \frac{\dfrac{R_e\left(\omega L_{2b}-\dfrac{1}{\omega C_3}\right)\left(\omega L_3-\dfrac{1}{\omega C_3}\right)}{R_e^2+\left(\omega L_3-\dfrac{1}{\omega C_3}\right)^2}}{\dfrac{R_e\left(\omega L_{2b}-\dfrac{1}{\omega C_3}\right)}{\sqrt{R_e^2+\left(\omega L_3-\dfrac{1}{\omega C_3}\right)^2}}} \\ &= \frac{\left(\omega L_3-\dfrac{1}{\omega C_3}\right)}{\sqrt{R_e^2+\left(\omega L_3-\dfrac{1}{\omega C_3}\right)^2}}\end{aligned} \tag{3.22}$$

Now it is possibile to derive the power substituting in (3.21) the expressions (3.22) and (3.15):

$$\begin{aligned}P_{in} &= V_{in}^2\frac{\sqrt{R_e^2+\left(\omega L_3-\dfrac{1}{\omega C_3}\right)^2}}{R_e\left(\omega L_{2b}-\dfrac{1}{\omega C_3}\right)}\frac{\left(\omega L_3-\dfrac{1}{\omega C_3}\right)}{\sqrt{R_e^2+\left(\omega L_3-\dfrac{1}{\omega C_3}\right)^2}} \\ &= \frac{V_{in}^2}{R_e}\frac{\left(\omega L_3-\dfrac{1}{\omega C_3}\right)}{\left(\omega L_{2b}-\dfrac{1}{\omega C_3}\right)}\end{aligned} \tag{3.23}$$

Since C_3 is not an independent variable in the circuit, it can be substituited with the resonance expression (3.4):

$$P_{in} = \frac{V_{in}^2}{R_e}\left(\frac{L_3}{L_{2b}}\right)^2 \tag{3.24}$$

Considering all the components ideal(without losses), it is possibile to consider valid the expression $P_{in} = P_o$. It is important to note that the power is proportional to the ratio of the two inductors L_3 and L_{2b}.

Chapter 4

Design

The objective of this chapter is to describe a design procedure to calculate the passive components of the CPT system, according to the specifications reported in table 4.1. Under 10Ω load the system is expected to provide 40W of power. The input voltage V_d is the rectified voltage of the electric grid. The final circuit of fig.3.1 is, for clarity, shown again below.

In this design, it is considered each interface capacitor with a value of 2nF. Since the capacitive interface is made by two series capacitors $C_2 = 1nF$.

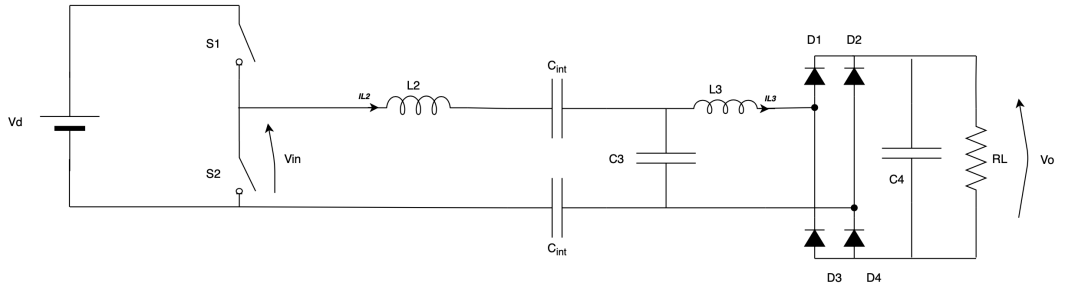

FIGURE 4.1: Final CPT scheme

P_{out}	40W
V_d	310V
f_{sw}	1MHz
C_2	1nF
R_L	10Ω

TABLE 4.1: Power Adapter Specification

Some other quantities derive directly from the specification, the output voltage and current:

$$V_o = \sqrt{P_{out} R_L} = 20V$$

$$I_o = \sqrt{\frac{P_{out}}{R_L}} = 2A$$

4.1 Power Adapter Design

In order to better understand the design procedure of the compensation network, a list of steps is indicated below:

1. Calculate L_{2a} with (3.3).
2. Calculate L_{2b} and L_3 with (3.24) and imposing a limitation on the capacitive interface voltage.
3. Calculate C_3 with (3.4).

4.1.1 Compensation Network

Following the specification in table 4.1 and substituting in the first resonance formula (3.3) it is possibile to derive the value of L_{2a}:

$$L_{2a} = \frac{1}{C_2 \omega^2} = \frac{1}{1nF(2\pi \cdot 1MHz)^2} = 25.33\mu H \tag{4.1}$$

From the equation (3.2) and (3.1) is possibile to derive:

$$R_e = \frac{8 \cdot 10\Omega}{\pi^2} = 8.10\Omega \tag{4.2}$$

$$V_{in} = \frac{2 \cdot 310V}{\pi} \approx 200V \tag{4.3}$$

As reported in equation (3.24), fixing the power determines the relationship between the inductors L_{2b} and L_3 but not their absolute values. It is still present one degree of freedom, a constrain should be added.
The idea is to limit the voltage of the capacitive interface C_2 imposing a $V_{C2} < 200V$.

$$\frac{L_3}{L_{2b}} = \sqrt{\frac{40W \cdot 2 \cdot 8.10\Omega}{(200V)^2}} = 0.127 \tag{4.4}$$

$$|V_{C2}| = |I_{C2}| \frac{1}{\omega C_2} \tag{4.5}$$

Using equation (3.15) and replacing (4.4) is possible to obtain:

$$\begin{cases} |V_{C2}| = V_{in} \dfrac{\sqrt{R_e^2 + \left(\omega L_3 - \dfrac{1}{\omega C_3}\right)^2}}{R_e\left(\omega L_{2b} - \dfrac{1}{\omega C_3}\right)} \dfrac{1}{\omega C_2} < 200V \\ \dfrac{L_3}{L_{2b}} = 0.127 \end{cases} \tag{4.6}$$

The values of L_3 can be found resolving the system or graphically as reported in fig.4.2:

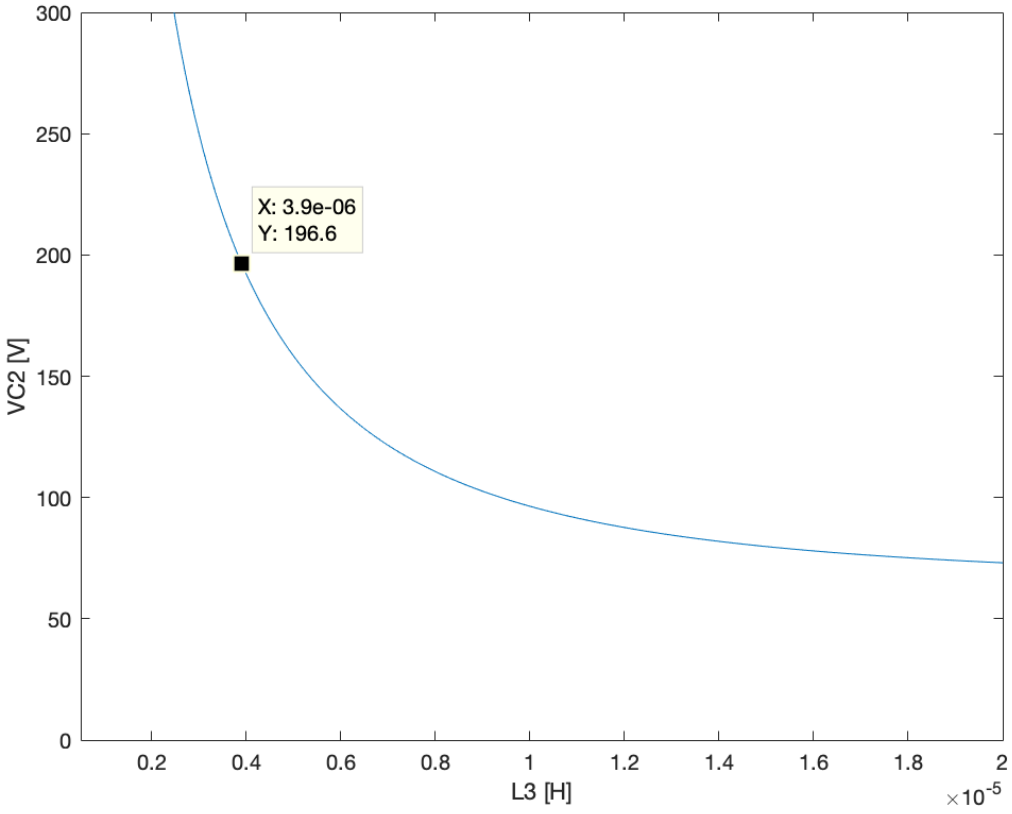

FIGURE 4.2: Graphical representation of (4.6), L_3 vs V_{C2}

It can be found the value of L_3 from the graph and then normalized to:

$$L_3 > 3.7\mu H \implies L_3 = 3.9\mu H \tag{4.7}$$

It is convenient to use a value of L_3 as small as possible for problems related to the size of L_2 inductor and so its losses. Since the ratio $\frac{L_3}{L_{2b}}$ is fixed, the greater is the value of L_3, the greater is the value of L_{2b} and consequently that of L_2.
At this point from the equation (4.4), the value of L_{2b} can be derived:

$$L_{2b} = 3.9\mu H \cdot 7.87 = 30.7\mu H \tag{4.8}$$

Since the inductor L_2 is the sum of L_{2a}(4.1) and L_{2b} as explained in the "Simplification" chapter:

$$L_2 = 25.33\mu H + 30.7\mu H = 56.03\mu H \implies 56\mu H \tag{4.9}$$

From the formula of resonance (3.4) is now possible to derive the C_3 capacitance:

$$C_3 = \frac{1}{(2\pi \cdot 1MHz)^2 \cdot 3.46\mu H} = 7.32nF \implies 6.8nF \tag{4.10}$$

All the components of the compensation network have been calculated, specifying their normalized values.

4.1.2 Rectifier

Three main parameters can be identified for the selection of the output rectifier diodes:

- Technology
- Peak inverse voltage
- Average forward current

In order to reduce the conduction losses, it is convenient to choose a Schottky diode. It has low voltage drop which implies a better efficiency of the system, while the lack of minority carriers (that must be extracted in the junction diodes before obtaining the interdiction) allows for high switching speeds and reduction of switching overshoots.

The peak inverse voltage V_{RRM} should be higher than the output voltage V_o=20V.

$$V_{RRM} > 20V$$

The average forward current I_F should be higher than half the output current $\frac{I_o}{2}$, since the output power P_o=40W, the output current is about 2A.

$$I_F > 1A$$

4.1.3 Half-Bridge MOS

The Half-bridge design consists in stating the requirements for the MOS devices:

- Drain-source voltage V_{DS}
- Drain current I_D
- Speed Q_g

The drain-source voltage should be greater than the input voltage V_d:

$$V_{DS} > 310V$$

The switching speed is directly related to the total gate charge Q_g and to the gate resistance R_g. Smaller Q_g implies smaller gate capacitance and therefore smaller time to charge it. A MOS transistor with a reasonably low value of Q_g should be selected.

At this point all the passive components of the CPT circuit are calculated and summarized in table 4.2.

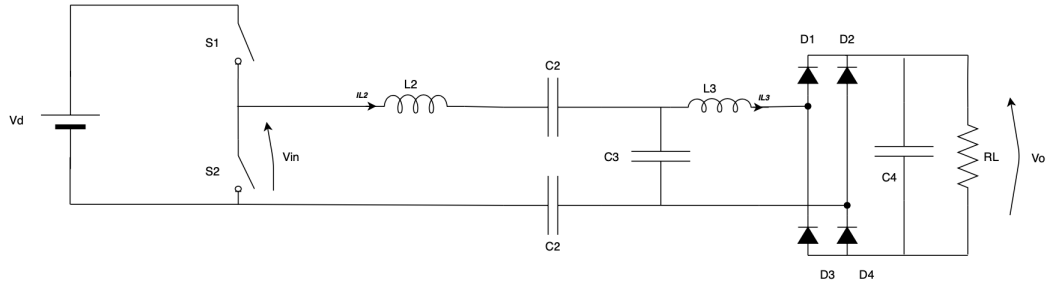

FIGURE 4.3: Final CPT scheme

$L2$	$56uH$
$L3$	$3.9uH$
$C3$	$6.8nF$
C_2	$1nF$
R_L	10Ω

TABLE 4.2: Final values passive components

4.2 Frequency Analysis

In this section the frequency behaviour of the circuit will be analyzed through simualtions with LTSpice. The simplified version of the circuit will be considered for the frequency simulations, the scheme, for clarity, is shown again fig.4.4.
The circuit topology that was analyzed and designed is a multiresonance system. Different combination of passive components can give rise to a resonance. It is possibile to study the frequency behaviour and to find the frequency points [5].

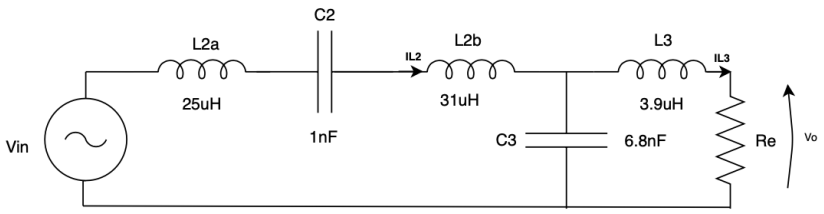

FIGURE 4.4: CPT simplified circuit

The frequency points are those values where the circuit can load constant-current or constant voltage without any external control loop.

Until now it has only been analyzed the output performance of one single resonance point without exploring whether the system has other resonance points or constant-current and constant-voltage output characteristics.

In the next subsection the constant-current and constant-voltage points will be indicated without going into detail with the procedure and equations that can be found in [5].

4.2.1 Constant-voltage point

The output voltage as a function of frequency is plotted in fig.4.6 for a different load conditions($R_e \approx 0.81 R_L$). It is possibile to note that there are two frequencies where the output voltage V_o is indipendent on the load. The first point around 650kHz and the second around 1MHz. The second point is exactly at the working frequency, this means that the designed circuit works as a voltage source.

Considering the simplified circuit of fig.4.5, the constant voltage mode of operation occurs when there is a simultaneous resonance between L_{2a}-C_2 and $L_{2b} \parallel L_3$ - C_3:

$$\begin{cases} \omega = \frac{1}{\sqrt{L_{2a}C_2}} = \frac{1}{\sqrt{(L_{2b} \parallel L_3)C_3}} \\ L_{2a} + L_{2b} = 56\mu H \end{cases}$$

Solving the system(using tab.4.2) it is possible to obtain a quadratic expression on L_{2a}, two values of inductance means two constant frequency points. This is consistent with what is plotted in fig.4.6:

$$\begin{cases} L_{2a} = 23.7\mu H \implies f \approx 1.03 MHz \\ L_{2a} = 62.7\mu H \implies f \approx 635 kHz \end{cases}$$

The frequency points are calculated substituting the L_{2a} values(found solving the system) in the resonant equation (3.3).

4.2.2 Constant-current point

The constant-current point can observed by plotting the output current as a function of frequency, for different load conditions, fig.4.8. It is possible to note that there is a single frequency where the output current I_o is indipendent on the load.

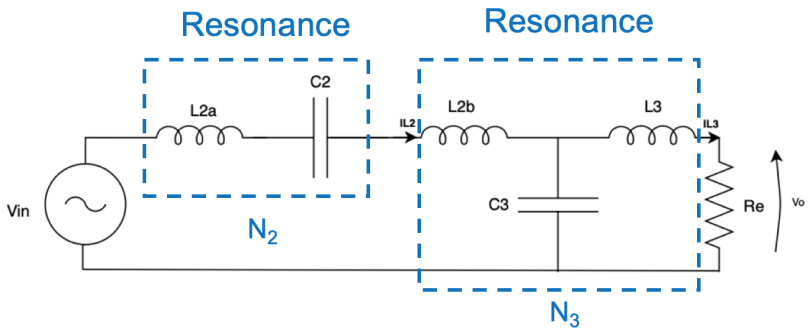

FIGURE 4.5: Constant-voltage resonances

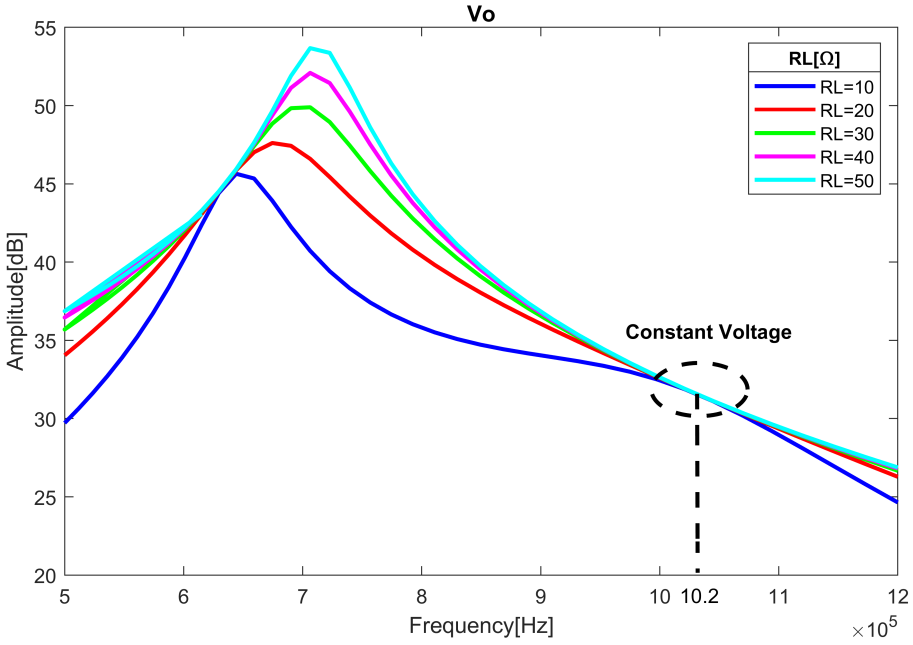

FIGURE 4.6: Output voltage frequency simulation, constant-voltage point

The constant current point occurs when L_{2a} resonates with C_2 and L_{2b} resonates with C_3(fig.4.7):

$$\begin{cases} \omega = \frac{1}{\sqrt{L_{2a}C_2}} = \frac{1}{\sqrt{L_{2b}C_3}} \\ L_{2a} + L_{2b} = 56\mu H \end{cases}$$

Solving the system above (using 4.2) it is possible to obtain a constant-current

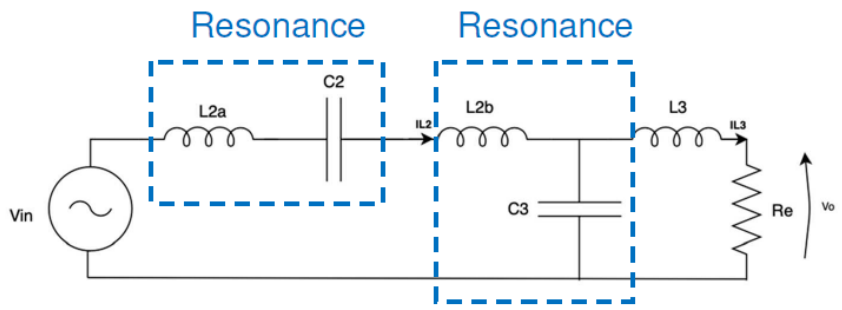

FIGURE 4.7: Constant-current resonances

frequency of about 720kHz. This value is consistent with the simulation of fig.4.8.

With the original design of the circuit and changing the working frequency to 720kHz it is possibile to work in the constant-current point.

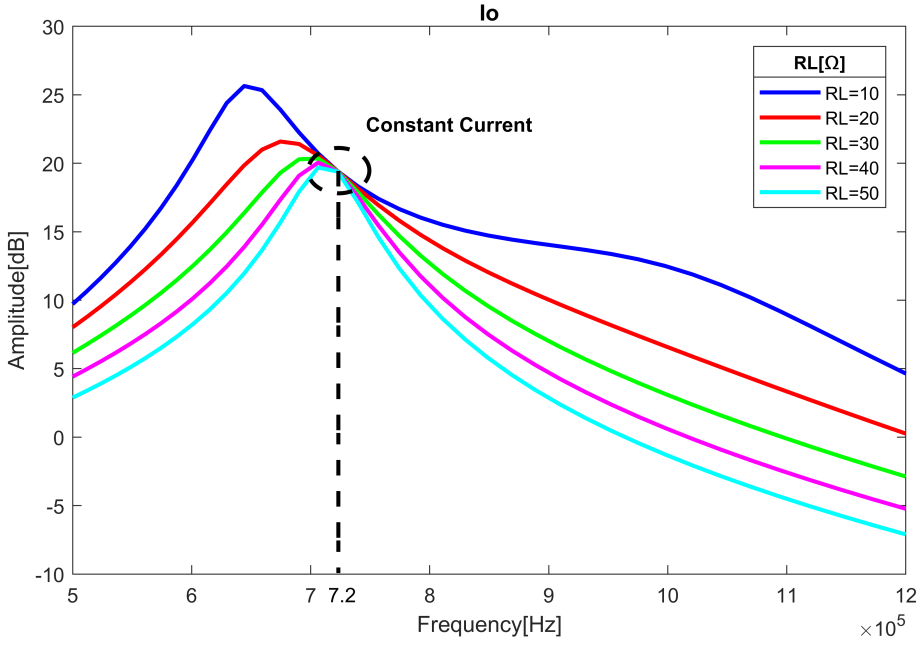

FIGURE 4.8: Output current frequency simulation, constant-current point

4.3 Synchronous rectifier

Synchronous rectifiers are also known as active rectifiers and they are used to improve the efficiency of diode rectifier circuits. The semiconductor diodes are replaced with actively controlled switches, usually power MOSFETs or BJT(fig.4.9).

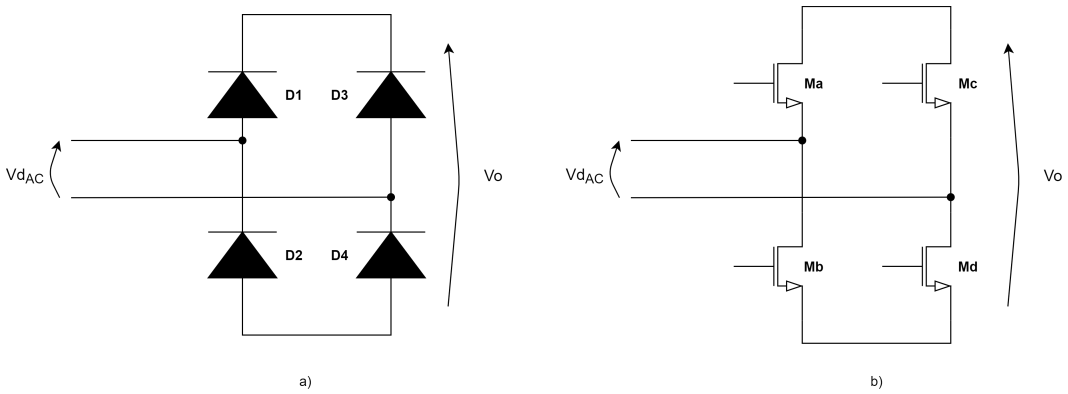

FIGURE 4.9: a)Diodes rectifier. b)Synchronous rectifier

The voltage drop of a standard p-n junction diode is typically 0.7 V - 1.7 V and 0.15 V - 0.5 V of a Schottky diode.
MOSFETs have a quasi-constant very low resistance when conducting, known as on-resistance R_{DSon}. The voltage drop across the transistor is then much lower, meaning a reduction in power loss and an increase of the efficiency.
The issue of efficiency is even more noticeable when using low voltage converters. With low voltage and high current levels the voltage drops introduced by diodes become unacceptable and synchronous rectifier techniques become essential.

The disadvantage of active rectification is that it require additional control circuits to ensure the devices turn on synchronously. The control circuitry is usually composed by comparators which sense the input AC(Vd_{AC}) and trigger the MOSFET at the correct times: turn on at ZVS(Zero Voltage Switching) and turn off, as the current reverses.

Another important reason to adopt an active rectification for the project is the possibiliy to control the output voltage and to implement in the future a closed loop control system.
In order to ensure the proper commutation(ZVS) to MOSFETs, the C node

of the complete circuit schematic 6.3 is used by the comparator to detect the drain-source voltage of the M6 transistor(4.10). The output of comparator

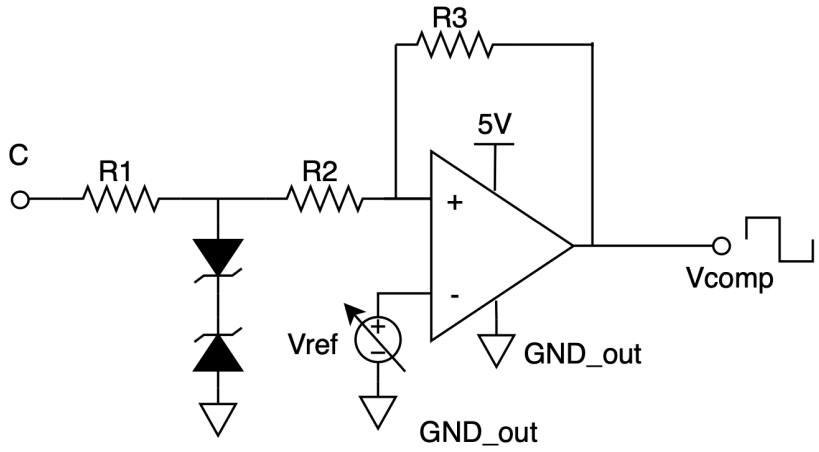

FIGURE 4.10: Synchronous rectifier comparator circuit

is an high signal whenever drain voltage of M6 is greater than the source voltage(connected to ground). Having digitalized the node C voltage, it is possible to ensure ZVS for all the MOSFETs of rectifier. The variable voltage generator Vref is another degree of freedom that can be used to anticipate the output of comparator in order to reduce the delay accumulated by gate drivers and comparator.

Chapter 5

Simulation Results

5.1 Ideal components simulations

The next project step is to verify the equation found in the previous chapters with simulations. Below are presented the simualtion results using ideal components, neglecting the main power dissipation of inductors and real MOS transistors.
All the simulations are performed with the SPICE-based LTspice software.

In fig.5.1 is presented the complete circuit that has been simulated. V_d is the rectified voltage of 310V, L_2, L_3 and C_3 form the ideal compensation network and R_L is the load resistance. C_{out} in parallel with R_L is the smoothing capacitor able to reduce the ripple of the output voltage and current.

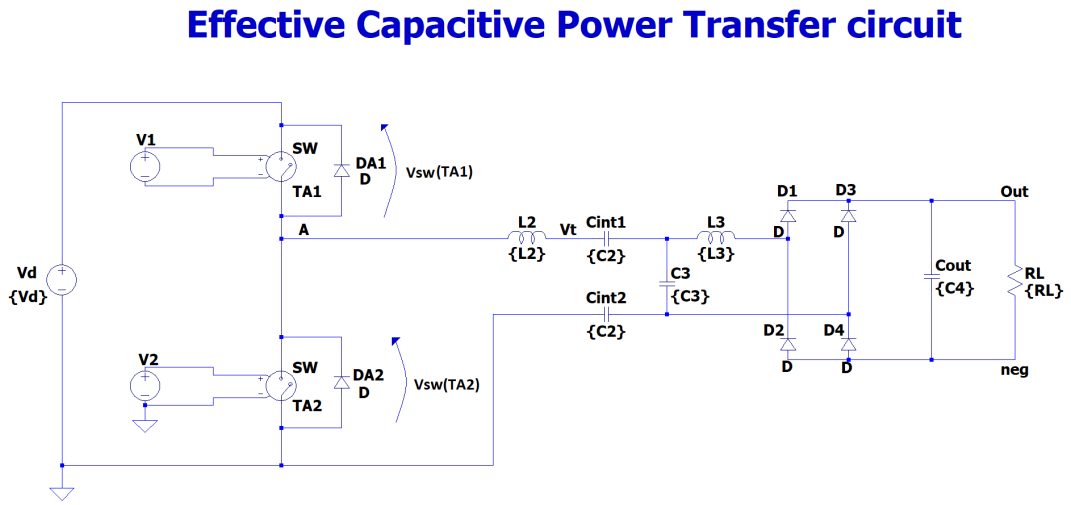

FIGURE 5.1: LTspice ideal simulation schematic

MOS transistor of half-bridge are substituted with ideal switch SW(with a ON resistance of 10mΩ) controlled by V_1 and V_2 in order to guarantee a square wave modulation.
As shown in fig.5.2, V_1 and V_2 signals have a period T_p of 1us, a delay T_d of 500ns and a T_{on} of 470ns, in this way a dead time of 30ns is taken into account.
In parallel to the ideal switches are needed freewheeling diodes because there is an inductive load. $DA1$ and $DA2$ can be omitted when real simulation are performed since in real MOS transistor the source-drain diode is intrinsically present.

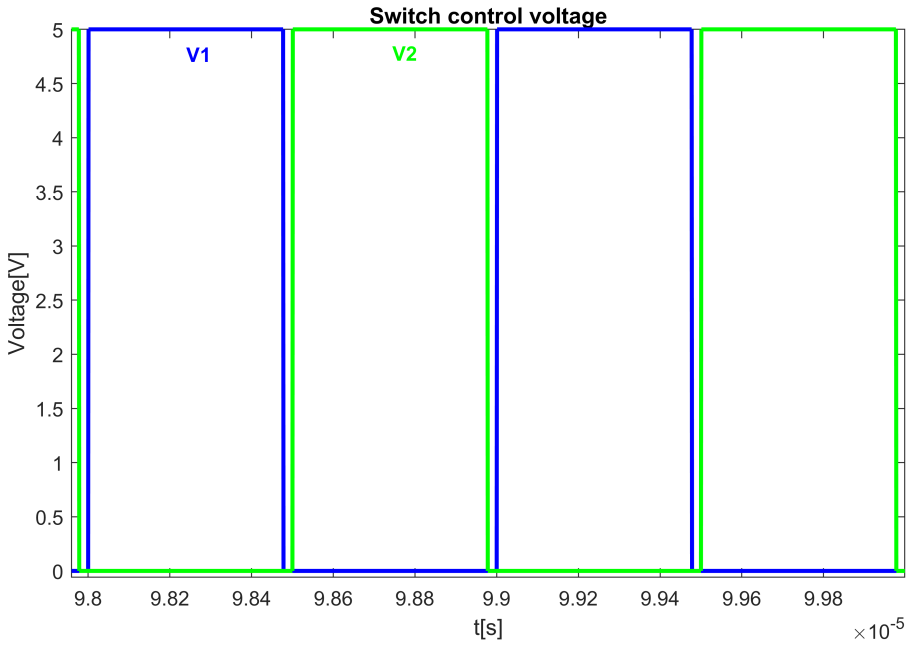

FIGURE 5.2: Control voltage of ideal switches, Square wave modulation

The output rectifier in the schematic is made up of diodes D1, D2, D3 and D4.
The capacitive interface that make possible to obtain a galvanic isolation is composed by C_{int1} and C_{int2}.

All the simulations are performed neglecting the rectification stage of the main voltage, when the $220V_{AC}$ is "converted" into $310V_{DC}$. This first stage will be designed for the implementation of the board but it has no relevance

in the simulations.
Below are reported and commented the simulation results, the normalized values of the components are those presented in the table 4.2.

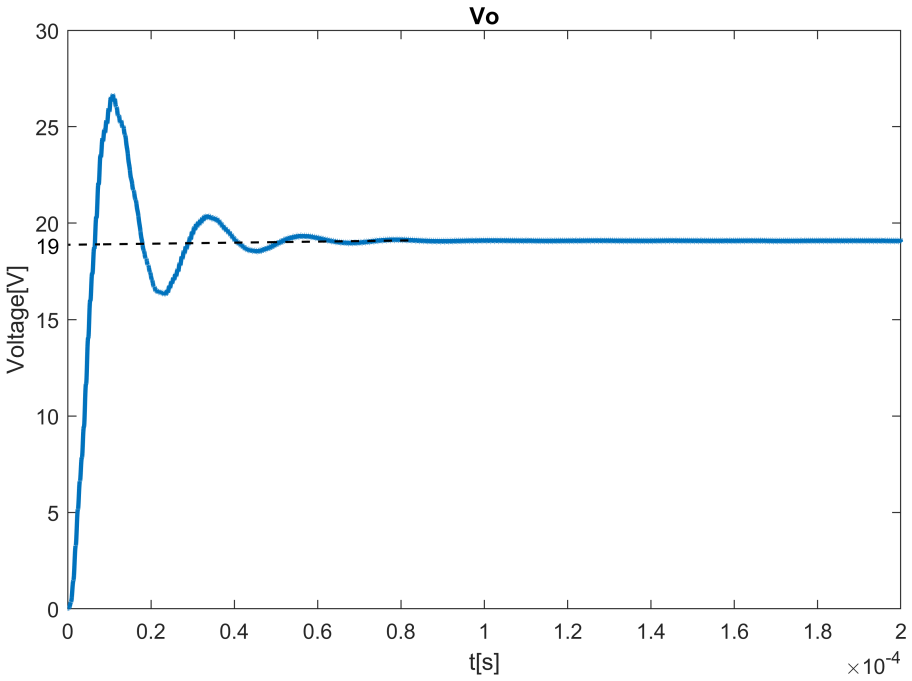

FIGURE 5.3: Output Voltage

In fig.5.3 and 5.4 are presented the output voltage and output current of the circuit. The signal reaches the steady state condition with an average value of about $19V$ for V_o and $1.9A$ for I_o. The simulation results seem to be agree with the calculated values.
The output power can be derived by multiplying the steady state voltage and current:

$$\overline{P_{out}} = 19V \cdot 1.9A = 36.1W$$

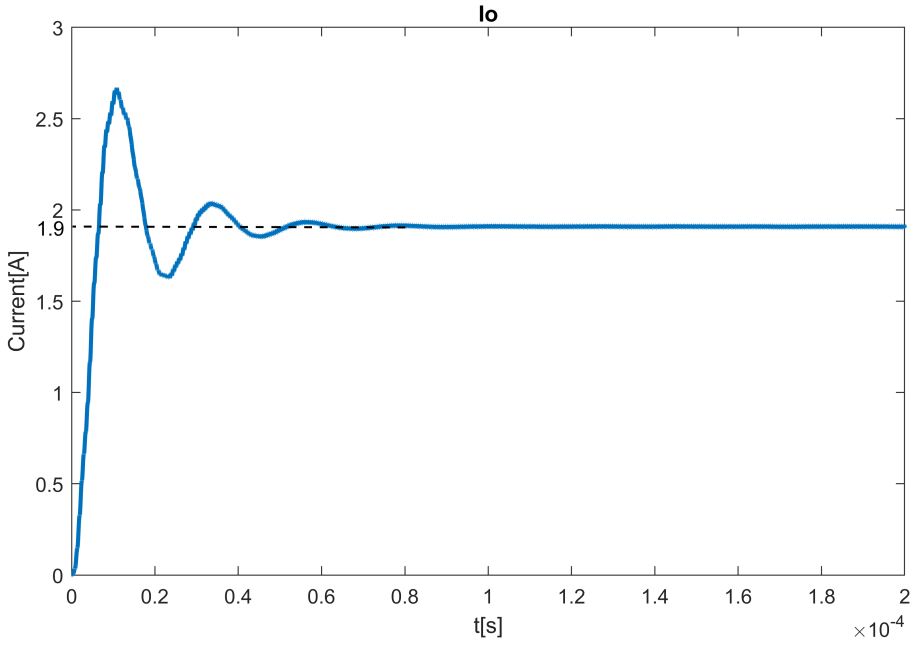

FIGURE 5.4: Output Current

There is a little difference compared to the input specifications. This is probably due to the conduction losses of diodes and to the normalization of the compensation network components, in fact a small deviation of the compensation network means a deviations from the resonance condition. In fig.5.6 is reported a parametric analysis of the output power for different values of the input inductor L_2. A small variations around $56\mu H$ has a considerable impact on the output power.

In fig.5.5 and 5.7 are illustrated the currents and the voltages of Half Bridge switches. TA1 is the high-side switch and TA2 is the low-one. The V_{sw} voltage is a square wave with a peak values of $V_d = 310$V.

As it can be seen the voltage and current change without meeting the Zero Voltage switching(ZVS) or Zero Current Switching(ZCS) conditions, for this reason a certain amount of power will be dissipated by the switches.

The capacitive interface voltage simulation result is shown in fig.5.8. For both C_{int1} and C_{int2} the quasi-sinusoidal signal has a peak to peak amplitude of about 180V (compared with 196V predicted in the "Power adapter design" chapter).

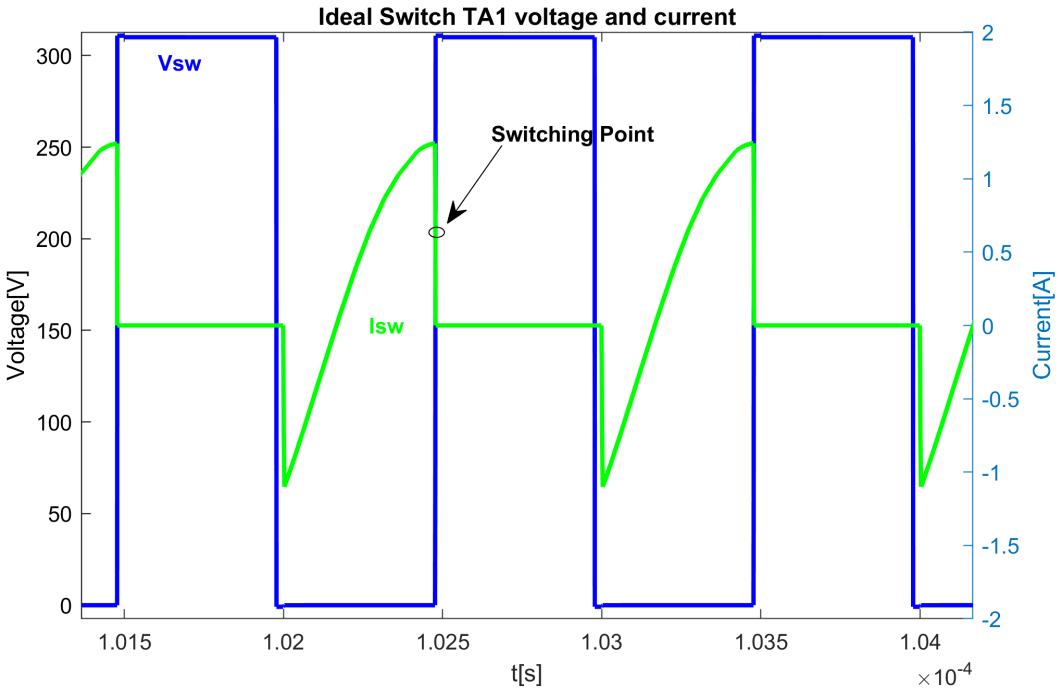

FIGURE 5.5: TA1 switch voltage and current in steady state

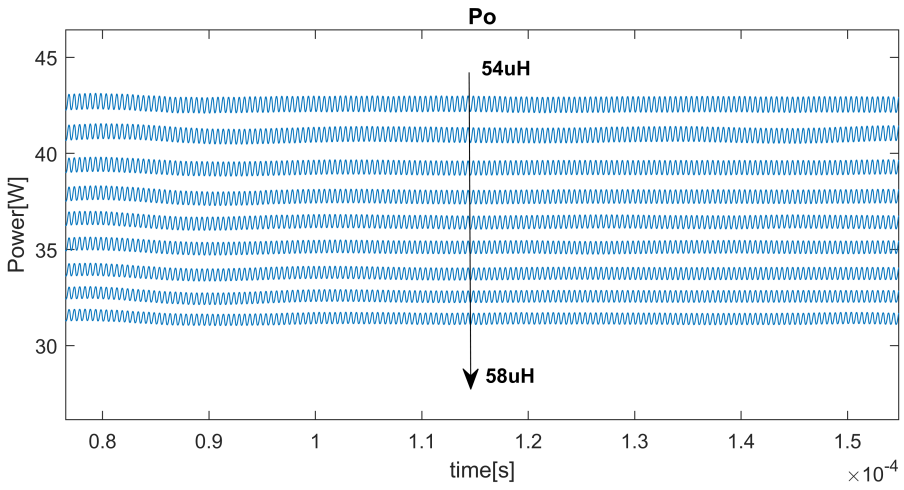

FIGURE 5.6: Output power P_o for different values of L2

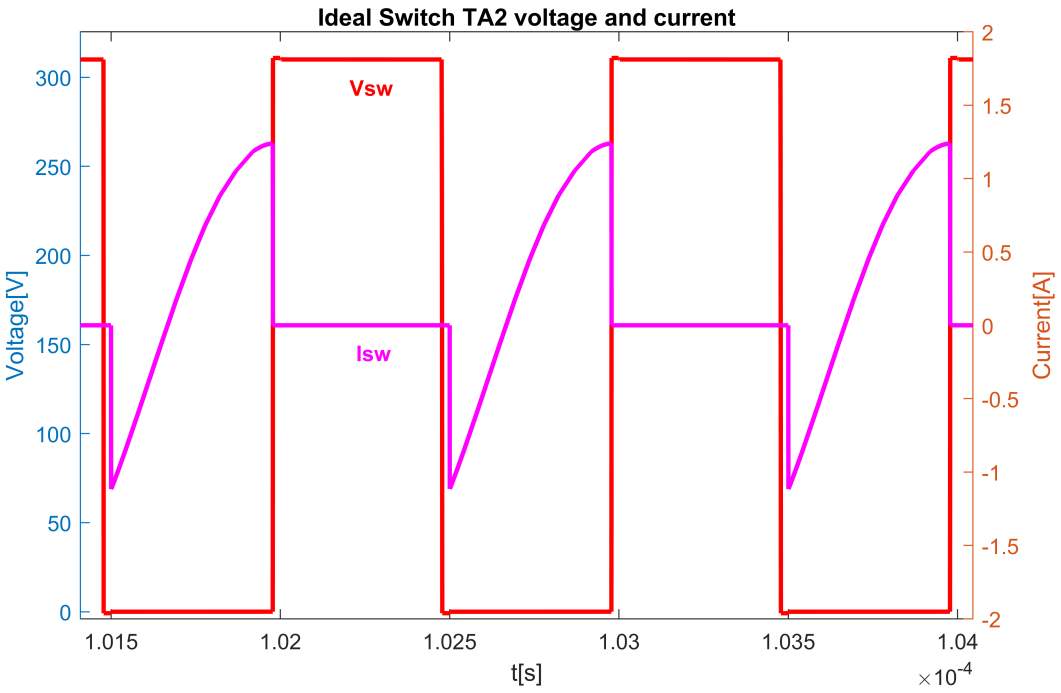

FIGURE 5.7: TA2 switch voltage and current in steady state

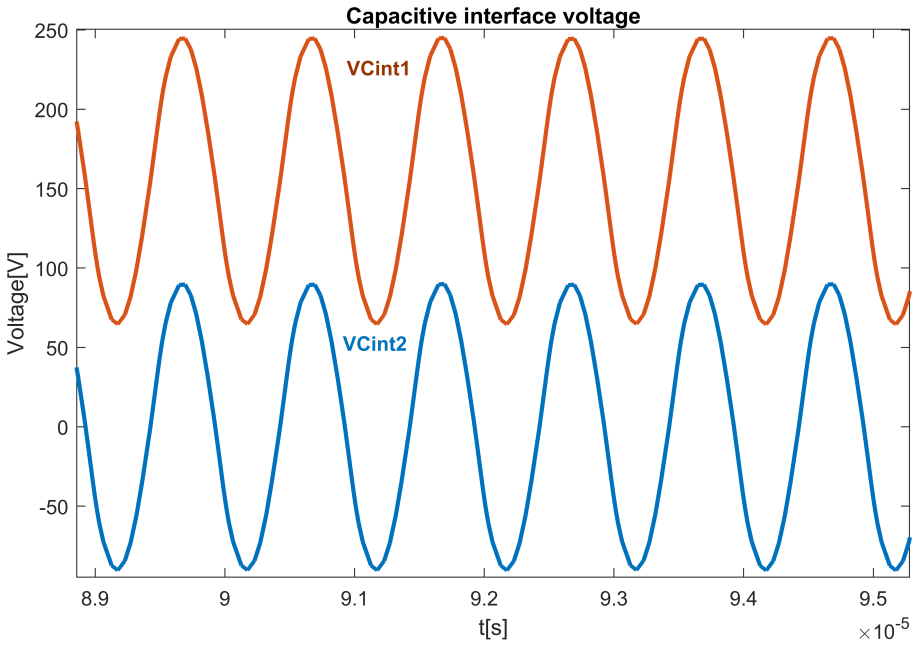

FIGURE 5.8: Capacitive Interface voltages

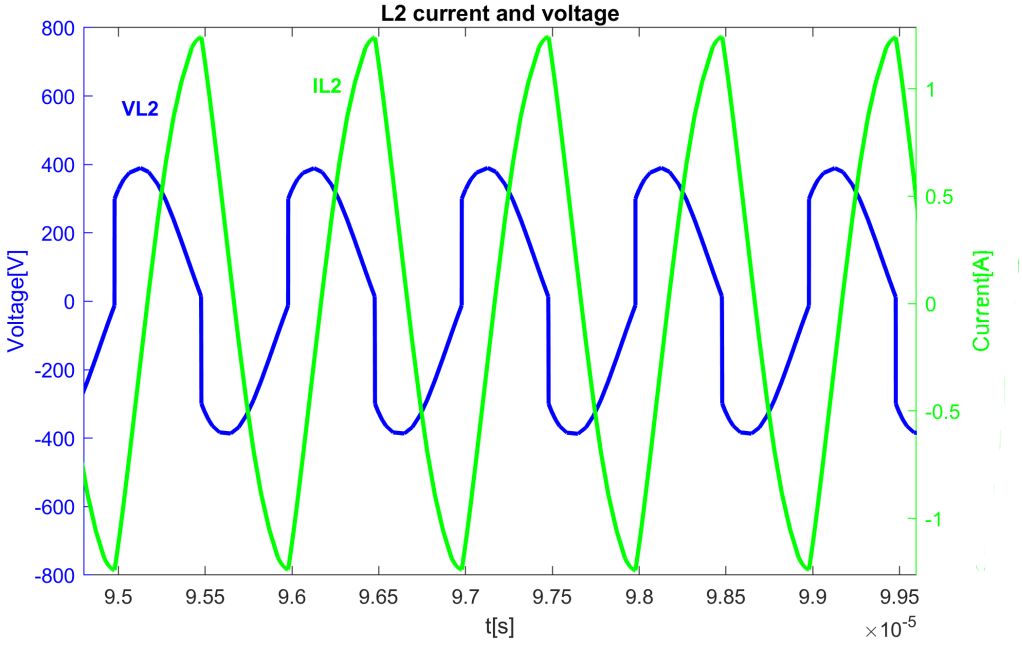

FIGURE 5.9: Input inductor L2 voltage and current

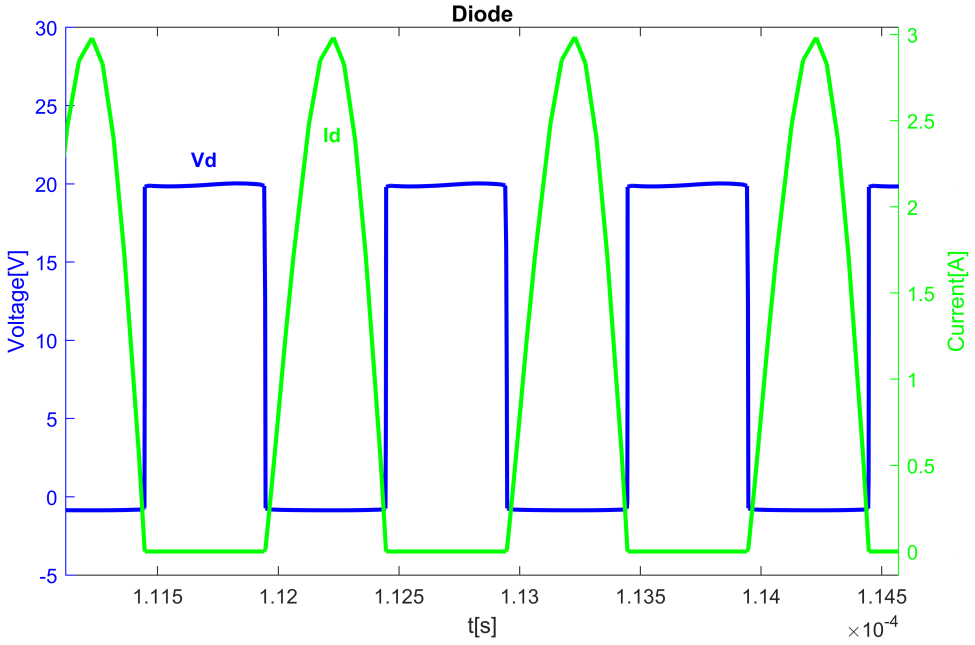

FIGURE 5.10: Diode voltage and current

The most stressed passive component of the circuit is the input inductor L2. In fig.5.9 it is possible to see that the V_{L2} reaches a peak value around 400V (compared with 415V predicted by equation(3.15), $|V_{L2}| = |Z_{L2} \cdot I_{C2}|$).

Using the graph in fig.5.11, the average value of the input power can be derived numerically with MATLAB or LTSpice. At this point, knowing the average values of input and output power, it is possibile to obtain an eximation of the system efficency(the conduction losses of diodes and switches are modelled, for this reason the efficiency in ideal simulation is not 100%).

$$\overline{P_{in}} \approx 39W \implies \eta = \frac{P_{out}}{P_{in}} = \frac{36.1W}{39W} = 92\%$$

This value cannot be considered relevant because it does not take into account of all the losses in the passive components. It can be used as an upperbound to indicate that with this circuit topology(without ZVS) is not possibile to achieve an efficency higher than 92%.

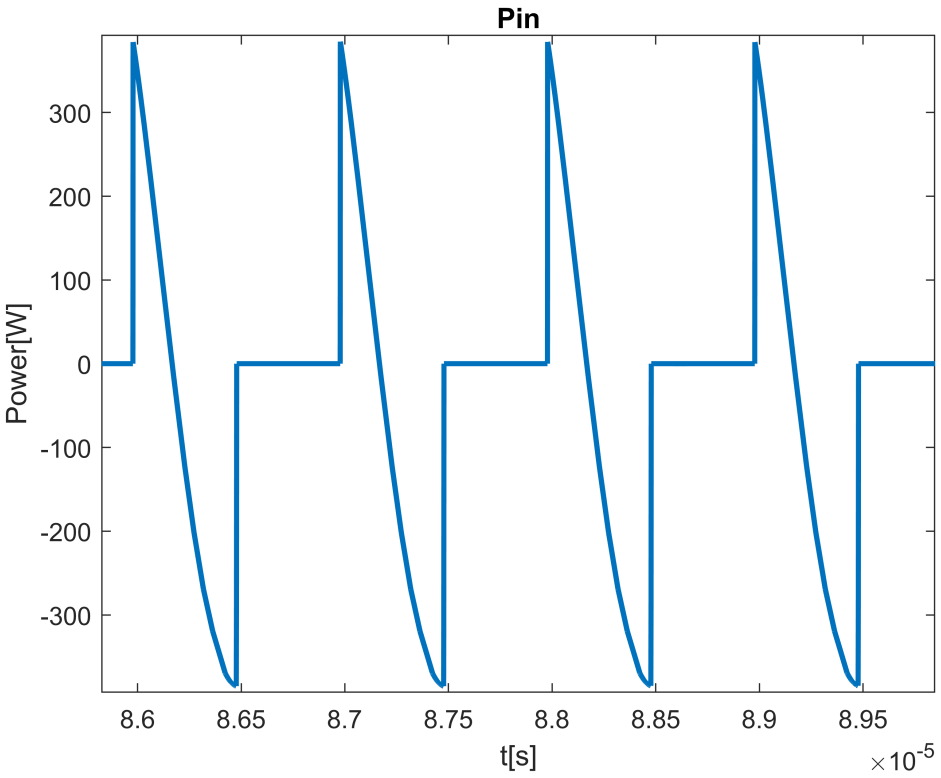

FIGURE 5.11: Input Power

Performing the ideal circuit simulations it was possibile to confirm the correctness of equations and to have a second estimation of the voltage and current behavior. It turns out to be interesting in the evaluation of real components.

Quantity	Specification	Ideal Simulation
V_o	20 V	19 V
I_o	2 A	1.9 A
P_o	40W	36.1 W

TABLE 5.1: Specification vs Ideal simulation

5.2 Real components selection

After analyzing the ideal simulations it is now possible to choose the real components for the board and to perform simulation in the real operation conditions.

5.2.1 Half-Bridge MOS

For the choice of the Half-bridge MOS transistor, as already reported in the "Design" chapter, three important parameters should be taken into consideration:

- Drain-source voltage $V_{DS} > 310V$
- Drain current $I_D > 1.2A$
- Speed $Q_g \implies$ Technology and dimension

The R_{dsON} was also considered by choosing the transistor with a low value of ON resistance in order to reduce the power dissipation.

As the switching frequencies are quite high, it was decided to use a Silicon Carbide device(SiC MOS). SiC MOSFETs offer better overall performance, higher efficiency, higher switching frequencies and lower ON resistance.

It was then chosen the STMicroelectronics **SCT10N120H** device:

- $V_{DS} = 1200V$
- $I_D = 13A$
- $Q_g = 22\text{nC}$
- $R_{dsON} = 520\text{m}\Omega$

This MOS is oversized for this application, large transitor implies large input capacitance and volume, but as the purpose is to make a demo board there are no size and weight requirements.

5.2.2 Inductors

Inductors are the most problematic components of the circuit because they are very stressed.

After doing some simulation with components from different munufacturers, the Coilcraft inductors were chosen. In particular the **Coilcraft MSS1048** Series, they are shielded surface-mount power inductors.
In fig.5.12 are reported the Datasheet graphs of Inductance versus current and frequency.
Analyzing the datasheet the self-resonant frequency(SFR) is greater than 1MHz considering our values of inductors ($L_2 = 56$ uH and $L_3 = 3.9$uH). Also the maximum achievable current is greater than $I_{L2max} \approx 1.2$A and $I_{L3max} \approx 3$A.

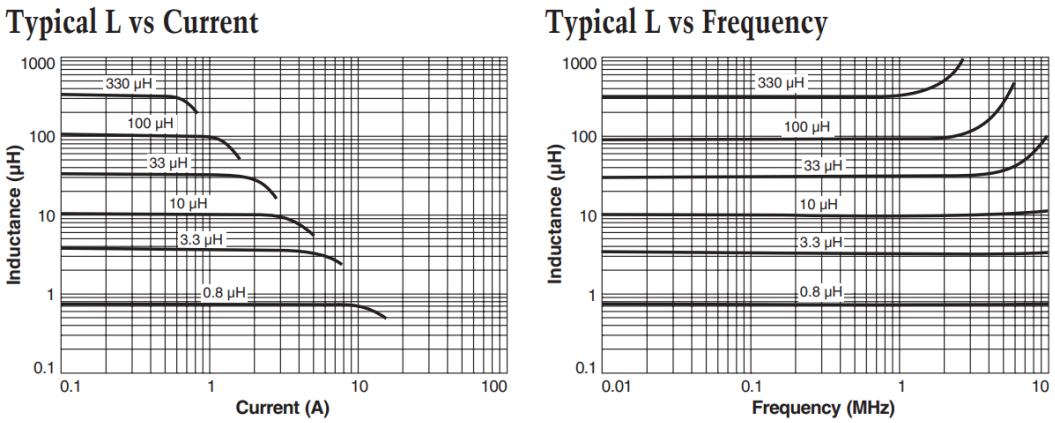

FIGURE 5.12: MSS1048 L curves

The manufacturer gives also some informations about Spice models. The equivalent lumped element model schematic is shown below in fig.5.13. It is useful to evaluate the losses and to make a real components simulation.

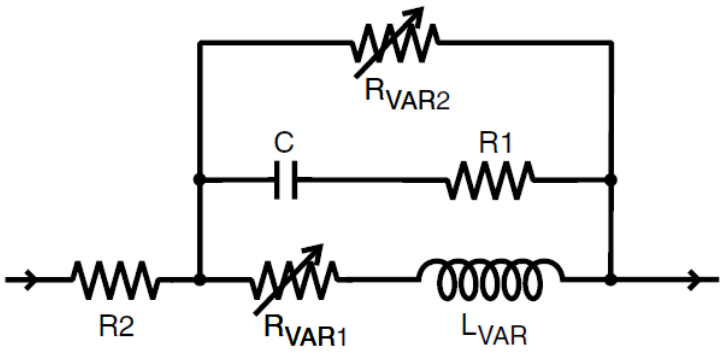

FIGURE 5.13: MSS1048 Spice model

5.2.3 Diodes

The choice of the diodes is based on the parameters described in the "Design" chapter and confirmed through the ideal simulations fig.5.10.

- $V_{RRM} > 20V$
- $I_F > 1A$
- Schottky

For the rectifier bridge were therefore chosen the STMicroelectronics **STPS5L60**, with a maximum average forward current of 5A and a maximum reverse voltage of 60V.

5.2.4 Driver

The drivers for the Half-bridge are necessary to turn ON/OFF the MOSFETs. SiC transistors needs a slightly negative voltage to be completely turned off, the driver should support negative gate driving.

The STMicroelectronics **STGAP2S** driver has been selected. It is a single gate driver which isolates the gate driving channel from the low voltage control. It is able to deliver 4A of driver current and it has a overall input/output propagation delay of 80ns.

5.3 Real components simulations

After selecting the components to be used for the construction of the board, the real components simulations should be performed.
The models of inductors, diodes and SiC MOSFETs have been loaded in LTSpice. In fig.5.14 is shown the schematic used for the simulations.

As can be seen from the schematic, the drivers for the Half-Bridge are not present in the simulation. The V_{gs} voltage is generated by an ideal voltage source, it is important to underline that the SiC MOSFETs need a slightly negative voltage to completely turn-off.

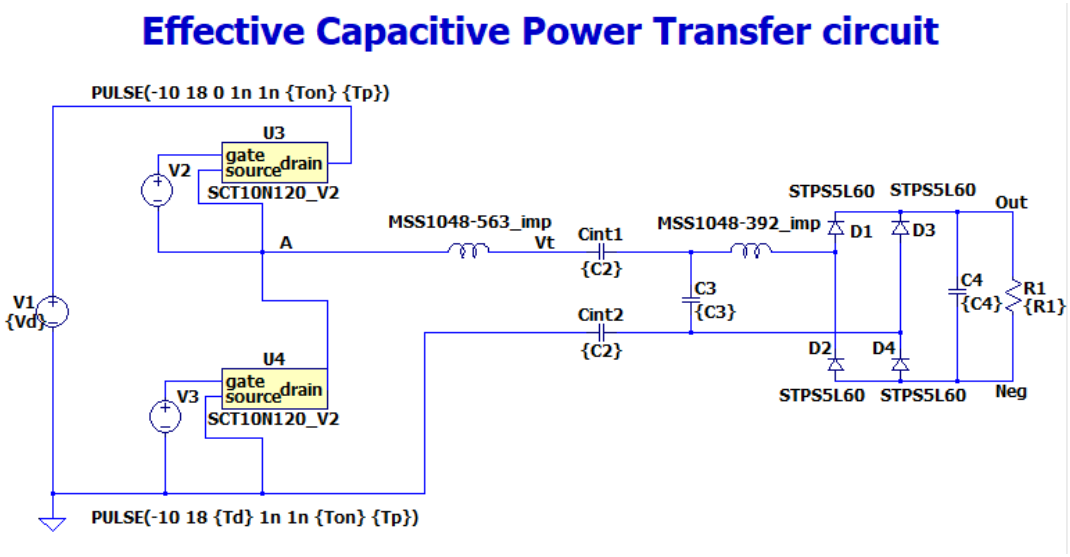

FIGURE 5.14: LTspice real simulation schematic

In fig.5.15 is shown the output voltage of the circuit, it has the same behavior of the ideal components simulation. There is only a small difference in the stady-state value that in this case is around $18.5V$, $0.5V$ less with respect to the ideal case 5.3.
The same happens in the current graph fig.5.16.

From the values of voltage and current is possibile to calculate the output power:

$$\overline{P_{out}} = 18.5V \cdot 1.85A = 34.2W$$

Between the ideal and real case there is a loss of about 2W in the output power, mainly due to the presence of parasitic components in the models.

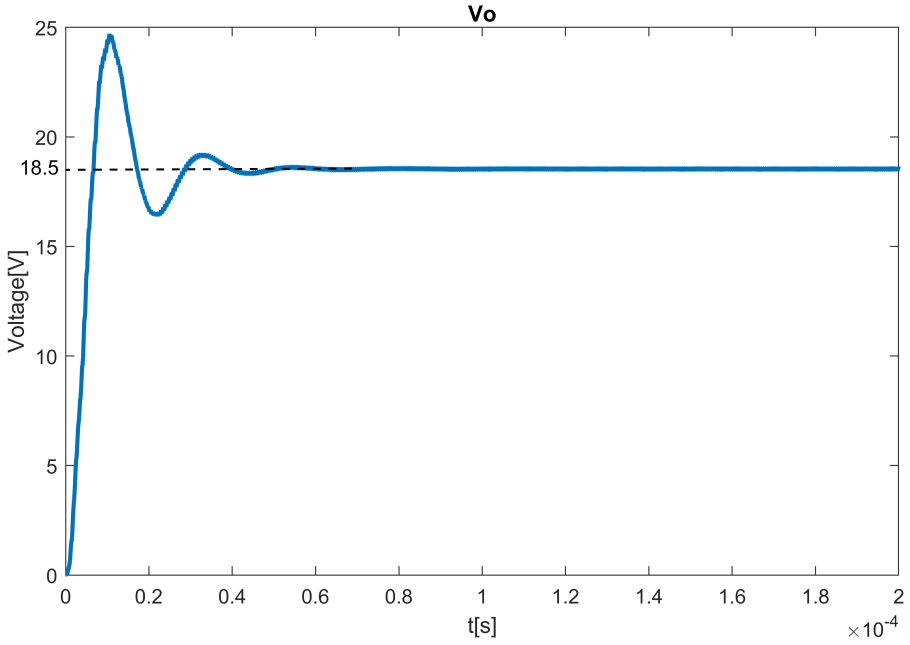

FIGURE 5.15: Output voltage Vo real components simulation

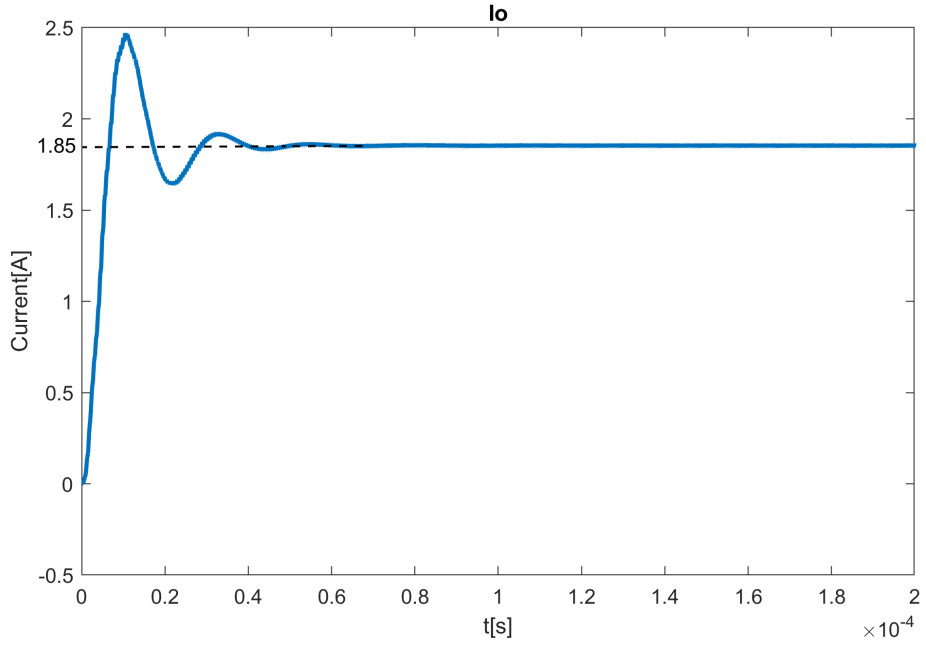

FIGURE 5.16: Output current Io, real components simulation

In fig.5.17 are shown the voltage and current waveforms of the high-side half bridge MOS. The graph is the same obtained in the ideal simualtions, it

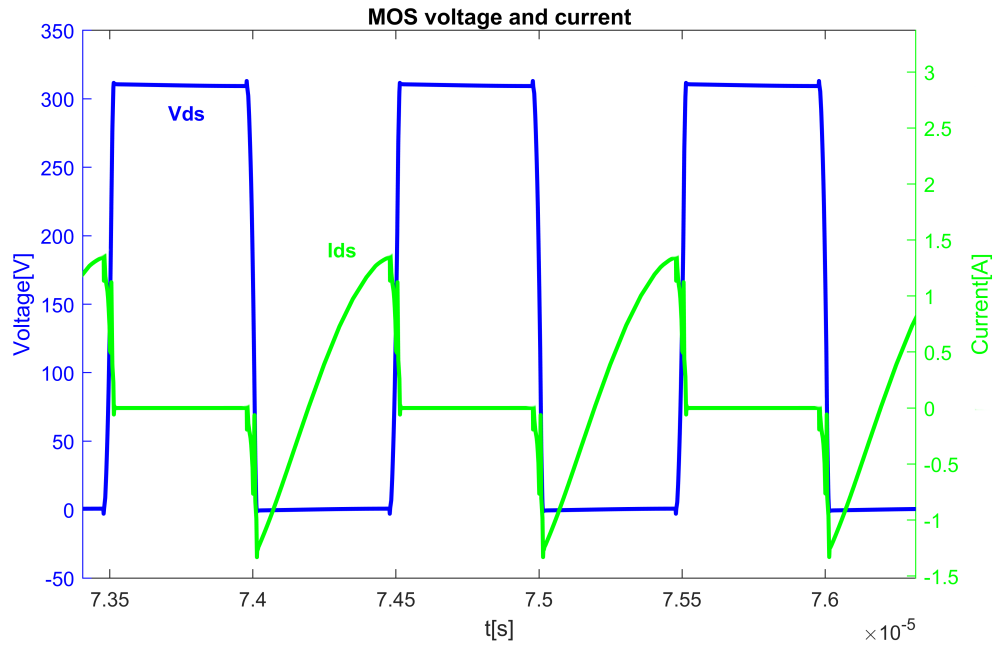

FIGURE 5.17: High-side MOS voltage and current, real components simulation

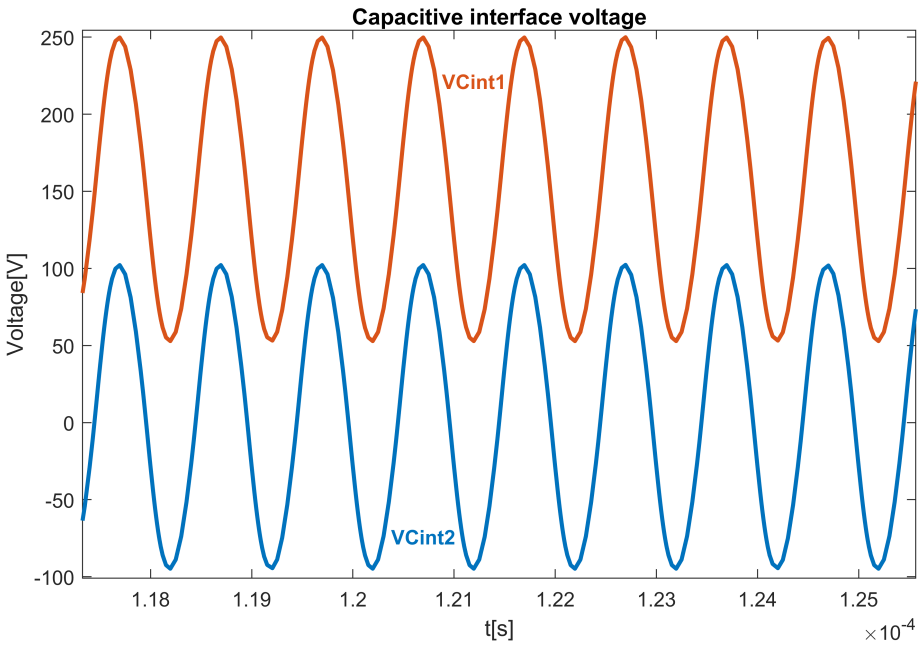

FIGURE 5.18: Capacitive interface voltage, real components simulation

is possible to derive numerically in LTSpice the average value of the drain current: $\overline{I_{ds}} = 130mA$ and the RMS current $I_{dsRMS} = 620mA$.
These values are very far from the absolute maximum rating of the SiC transistors.

The same happens for the capacitive interface voltage fig.5.18 and the L2 inductor fig.5.19.

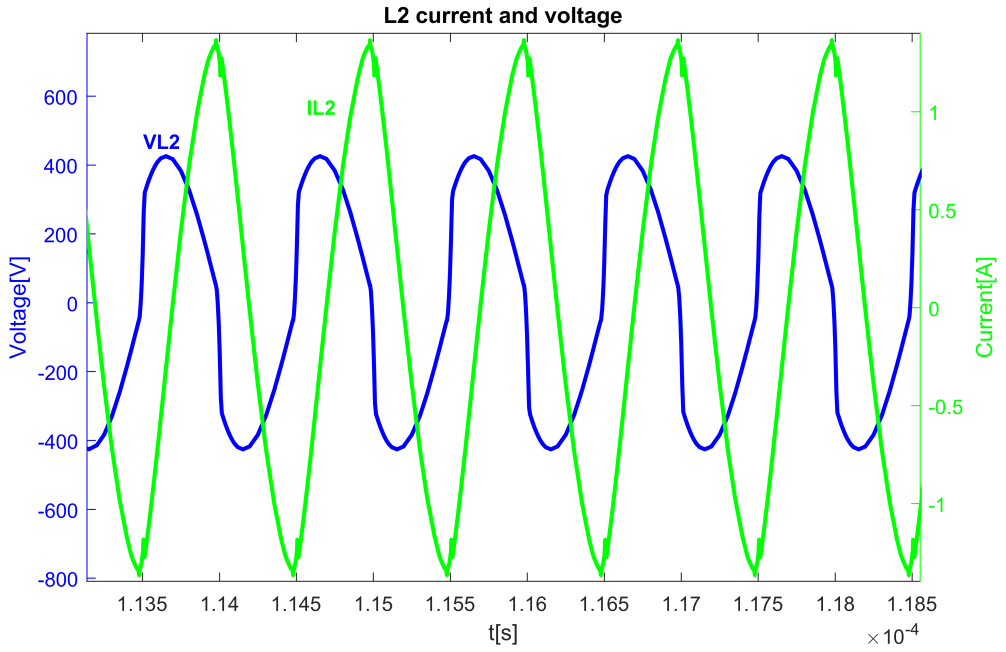

FIGURE 5.19: Input inductor L2 voltage and current, real components simulation

The average diode current can be derived with the graph in fig.5.20. It has the typical waveform of a diodes rectifier, with a voltage variation between 0V and 19V. After the full-wave rectifier is placed an output filter capacitor in order to reduce the diodes output voltage ripple.

With the graph of the input power fig.5.21 is possibile to derive numerically the average input power: $\overline{P_{in}} = 40.6W$.
The efficiency of the real components circuit can be obtained as:

$$\eta = \frac{\overline{P_{out}}}{\overline{P_{in}}} = \frac{34.2W}{40.6W} = 84\%$$

Compared to the ideal simulation the efficiency is reduced by 8%. Again it is important to point out that this value does not take into account the

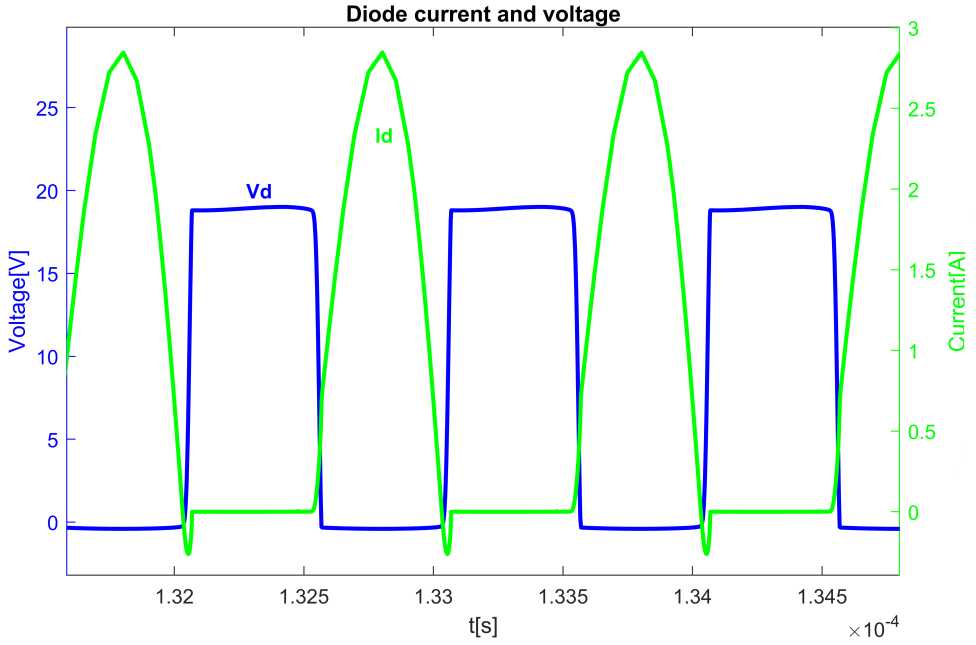

FIGURE 5.20: Diode voltage and current, real components simulation

power lost in the Half-bridge MOS drivers.

Quantity	Specification	Ideal Simulation	Real Simulation
V_o	20 V	19 V	18.5 V
I_o	2 A	1.9 A	1.85 A
P_o	40W	36.1 W	34.2 W

TABLE 5.2: Specification vs Ideal and Real simulations

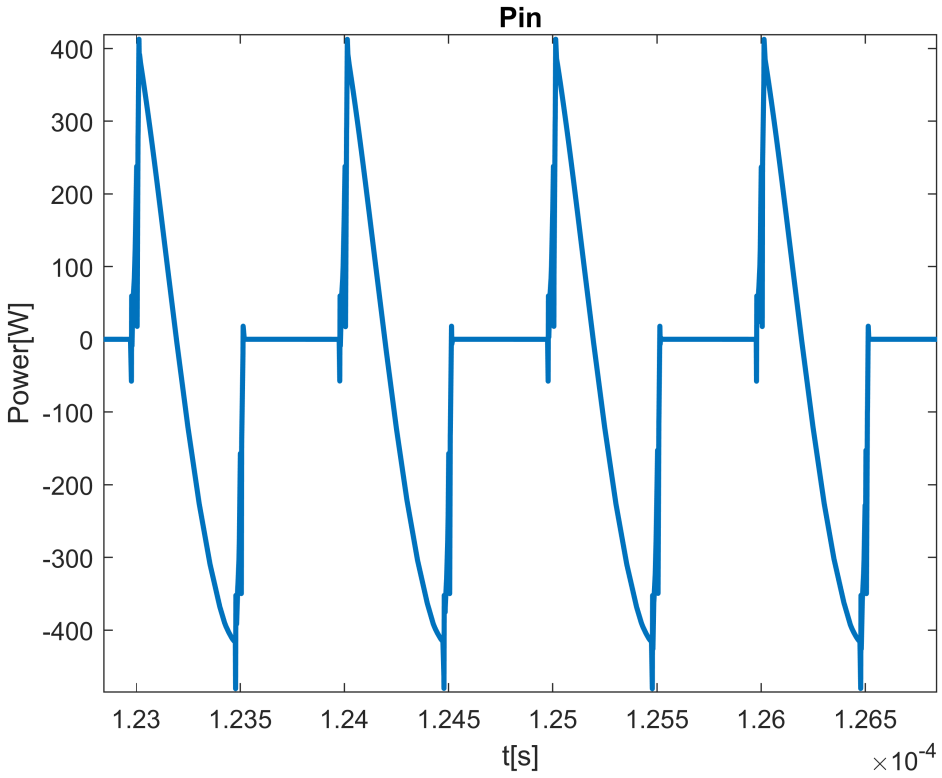

FIGURE 5.21: Input power, real components simulation

Chapter 6

PCB Design

After having designed the circuit and having verified the operation with the simulations, the next step is the layout design.
This chapter deals with the design of the PCB prototype board and the explanation of its operation and features. The board has been designed to be adaptable to different situations, especially for the Half-bridge stage and the output rectifier stage. The layout of the board was realized with Altium Designer software.

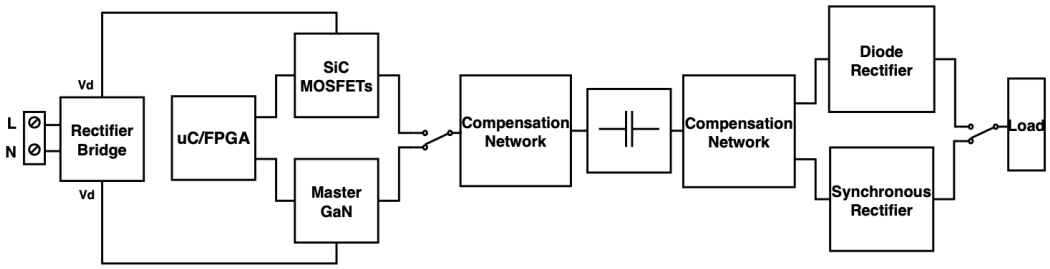

FIGURE 6.1: PCB building block scheme

In fig.6.1 is shown the building block of the PCB board. At the input there is a 50Hz main voltage bridge rectifier that converts the $220V_{AC}$ in $310V_{DC}$ for the half-bridge.
In the half-bridge inverter stage has been made a configuration for two different devices:

- **SiC MOSFETs**(SCT10N120H): directly mounted on the PCB board with the relative drivers(STGAP2S).
- **GaN HEMT**: an external board(STMicroelectronics EVALMASTERGAN) with integrated drivers, fig.6.2.

The idea is to compare the two technologies SiC and GaN in order to highlight the performance and efficiency.
In the PCB, for the MASTERGAN board, input pins(J3) have been left so that the output of the MASTERGAN board can be connected to the compensation network and to the rest of the circuit.

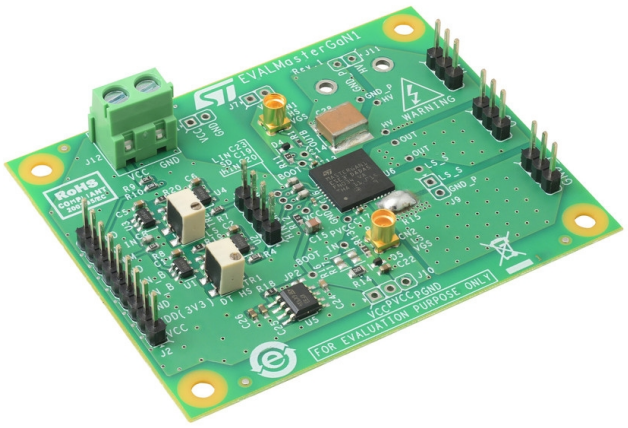

FIGURE 6.2: STMicroelectronics EVALMASTERGAN1 board

After the compensation network and the capacitive interface, the rectifier stage is present at the output. As for the input inverter stage, two different solutions are present for the output stage:

- **Diodes rectifier**
- **Active rectifier**(MOSFETs)

It was decided to add the synchronous rectification in order to increase the efficiency of the system and to implement a closed loop control system in the future.
The two blocks are in parallel, it is possibile decide to use one or the other by simply mounting the component on the board or not.

6.1 Schematics

In the images below are shown the schematics of the PCB board.
In fig.6.3 is reported the schematic of the circuit: the half-bridge MOSFETs(M1 and M2), the compensation network(L2, C3, L3), the capacitive interface(C2a and C2b), the output diode rectifier(D3, D4, D5, D6) with in parallel the synchronous rectifier(M3, M4, M5, M6), the output filter capacitor and the screw

connector for an external load.

In the schematic 2 fig.6.4 is represented the input power section: the bridge rectifier(BR1), the SiC drivers and connectors.

In fig.6.5 is reported the output power section: the active rectifier drivers, the comparator and connectors.

6.1.1 Input power section

The input power section is shown in the schematic 2 fig.6.4. It is essentially composed by:

- **SiC MOSFETs Drivers**: U1 and U2.
- **Driver power supply**: there are two ways to power the driver. It is possibile to use an external power supply(J5 and J8) or to use the two internal DCDC(PS1 and PS2).
- **Input bridge rectifier**: BR1

The input full-wave rectification is performed by STMicroelectronics STBR406, a single-phase 4A bridge.

The STGAP2S driver manufacturer suggests to add filtering capacitor close to logic inputs of the device for fast switching applications.

6.1.2 Output power section

The output power section is represented in the schematic 3 fig.6.5. It is composed by:

- **Synchronous rectifier drivers**: Maxim MAX15019 IC2 and IC3, are non isolated half-bridge drivers.
- **Drivers power supply**: As for the SiC MOSFETs drivers, there are two solution to power the devices. With an external voltage(J6) or with an internal DCDC(PS3).
- **Synchronous rectifier comparator**: Maxim MAX999(IC1).

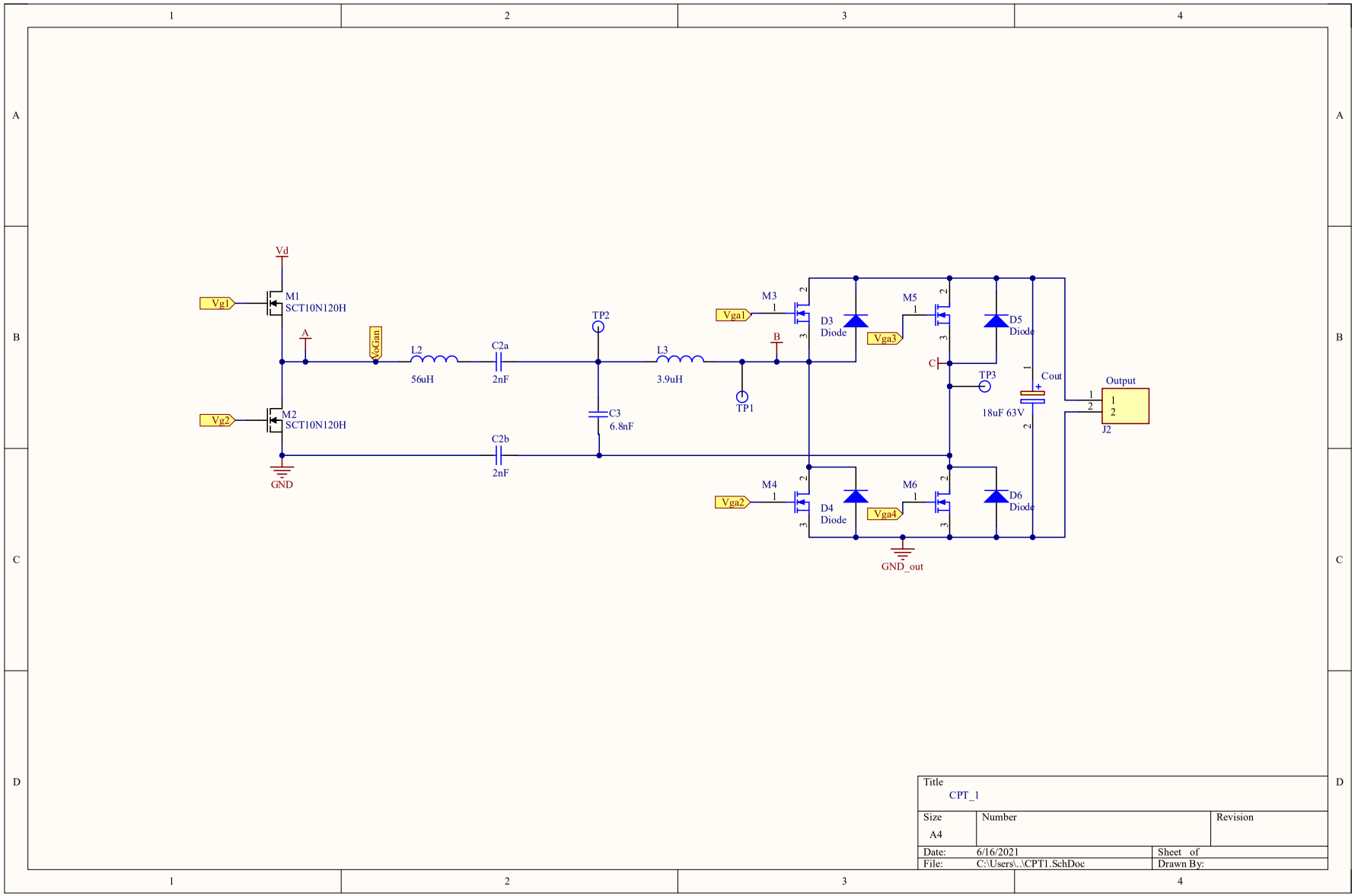

FIGURE 6.3: PCB Schematic 1, complete circuit

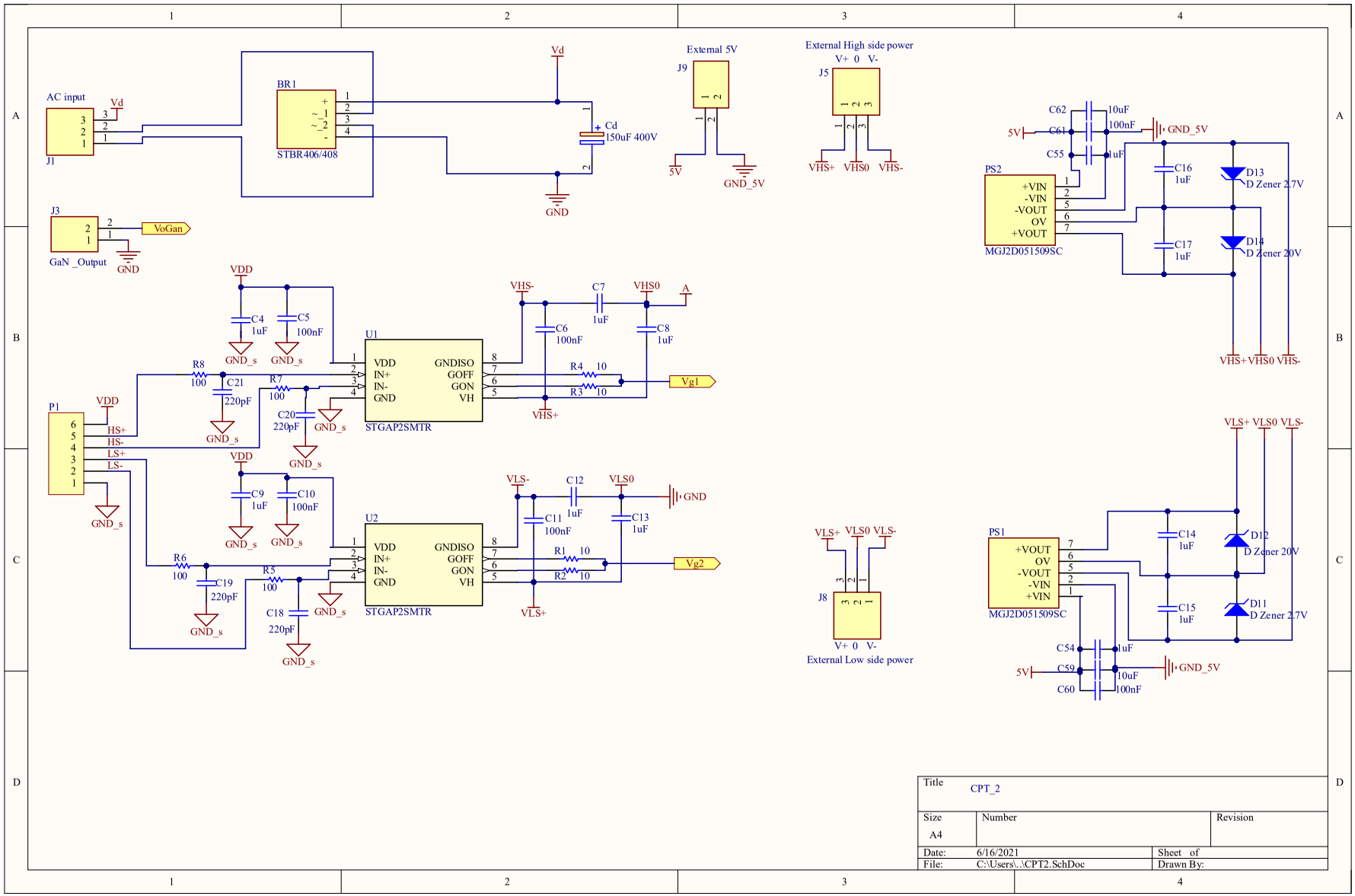

FIGURE 6.4: PCB Schematic 2, connectors, input rectifier and half-bridge drivers

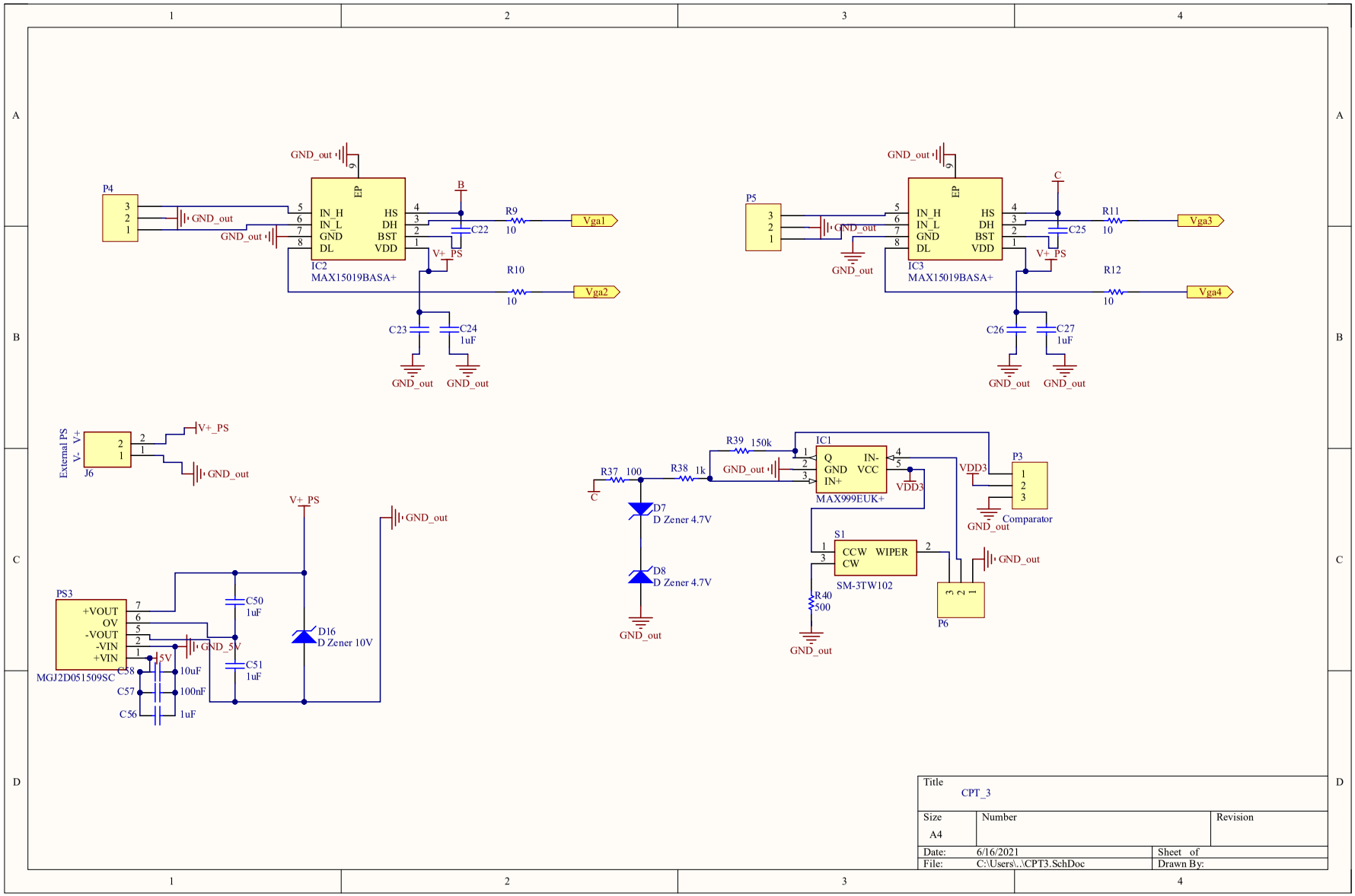

FIGURE 6.5: PCB Schematic 3, output rectifier drivers and comparator

6.2 Board Layout

When implementing circuits operating in the megahertz range, it is important to consider how the components are spaced, because of parasitic elements.
All the components are placed as close as possible to each other on the top layer. Long traces cause parasitic inductance which causes ringing in the circuit. This especially needs to be limited in the connection between drivers and transistors since the gates are particulary sensitive and ringing can compromise the operation of the circuit.

The layout is presented in fig.6.6. The dimensions of the board are (135x75)mm and it was decided to use a 4-layer structure: Top layer, Ground, Power and Bottom layer. A first prototype of the board was made using a two-layer structure but due to complexity and disturbances tracking of PCB this solution was discarded.

Three different trace widths are used in the layout:

- 0.5mm→ signal: low power signals of drivers and comparator.
- 0.9mm→ middle power: output power signals of drivers.
- (1.5-2)mm→ power: MOSFETs, compensation network and rectifier traces.

In the circuit there are many elements with different supply voltages and different ground references, for this reasons on the ground plane and power plane multiple nets regions can be identified.
Internal layers are better highlighted in fig.6.7. Four different ground regions can be identified:

- GND_5V: ground signal of the 5V input power supply of DCDC converters.
- GND_s: signal ground of the isolated SiC drivers.
- GND_IN: input ground of the circuit, before the decoupling capacitances.
- GND_OUT: output ground of the circuit, after the decoupling capacitances.

The footprints of surface and through-hole components are dimensioned in according to what is reported in the datasheet. A general overview and an additional confirmation is given by the 3D prototype of the board in fig.6.8.

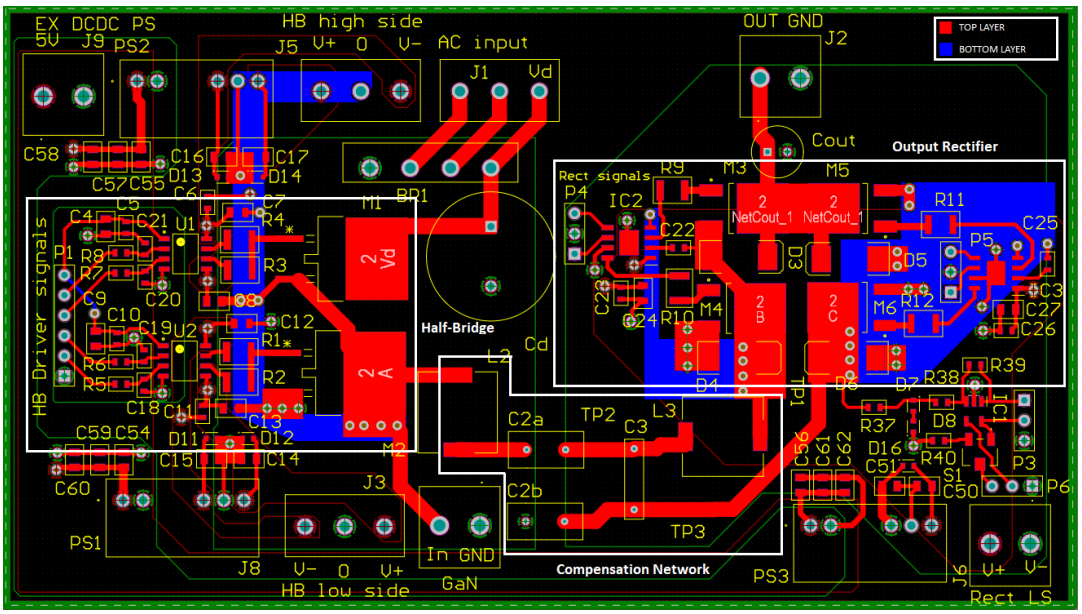

FIGURE 6.6: PCB layout

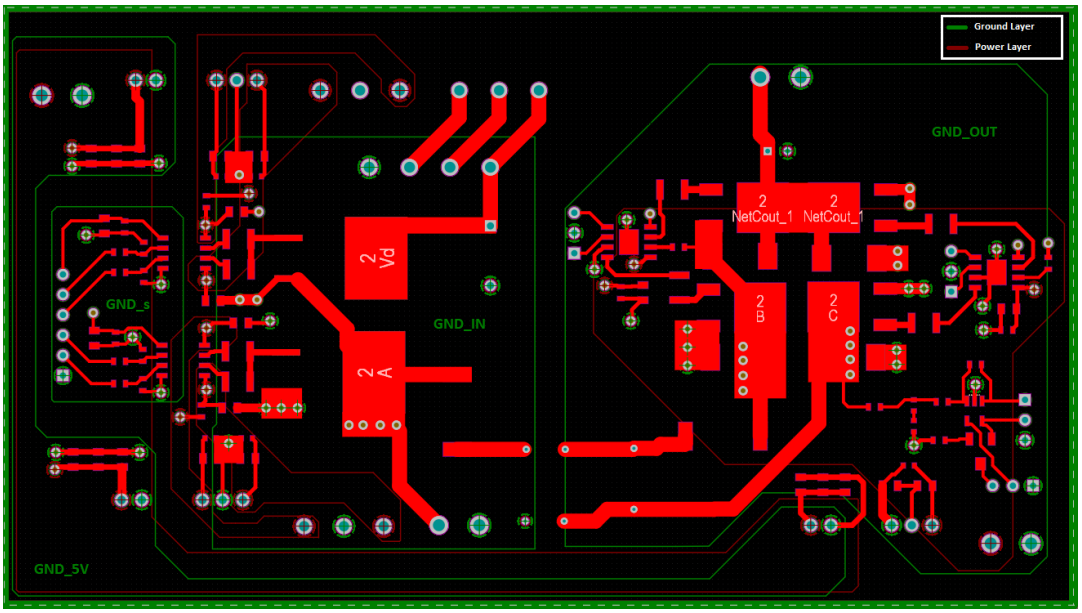

FIGURE 6.7: PCB layout, internal layers

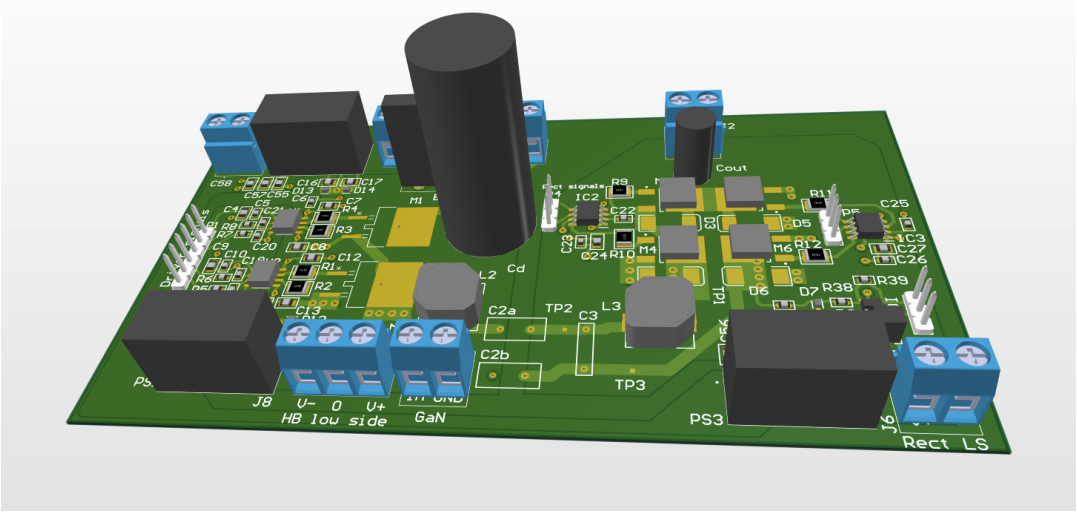

FIGURE 6.8: 3D PCB layout

Chapter 7

Experimental results

The last chapter of the thesis is dedicated to the experimental part of the project which was entirely carried out in the laboratories of Politecnico di Torino.
Due to problems of delays in the availability of some components, the assembly and measurement of the board was partially performed just in order to verify the correct operation of it.
In fig.7.1 is presented the board. Some components still need to be mounted, in particular the MOSFETs of the half-bridge inverter(M1 and M2). Instead the compensation network and the output diodes rectifier are mounted and can therefore be tested.

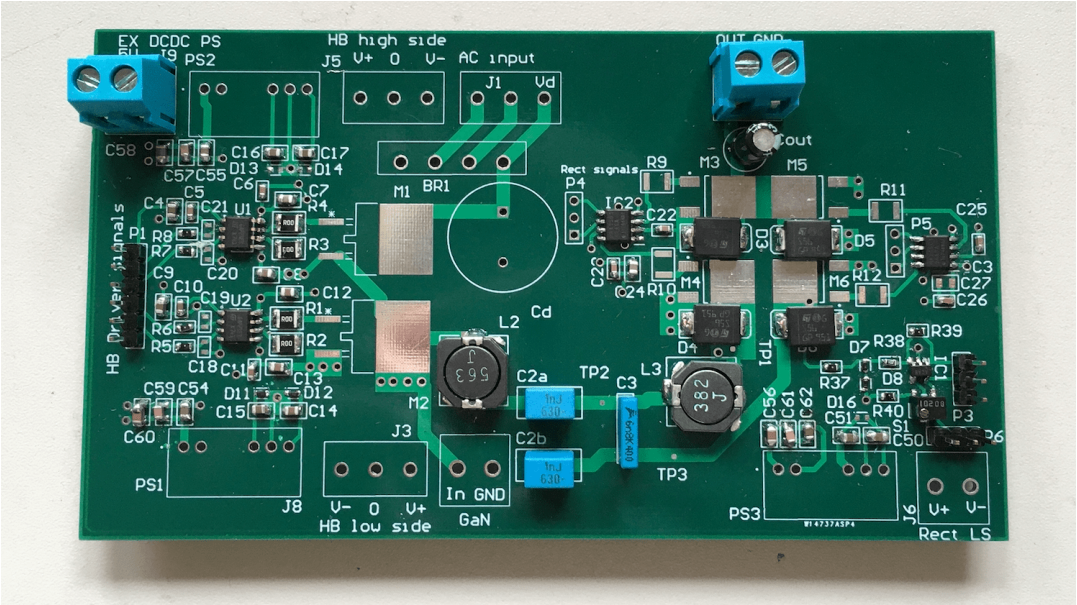

FIGURE 7.1: Adapter board prototype, partially mounted

The external STMicroelectronics EVALMASTERGAN1(GaN) is used as external inverter in order to test the circuit fig.7.4.
The laboratory setup involves the use of:

- Signal generator Rigol DG1022
- DC power supply Rigol DP832
- Digital oscillosope Rigol DS1054
- Multimeter HP 34401A

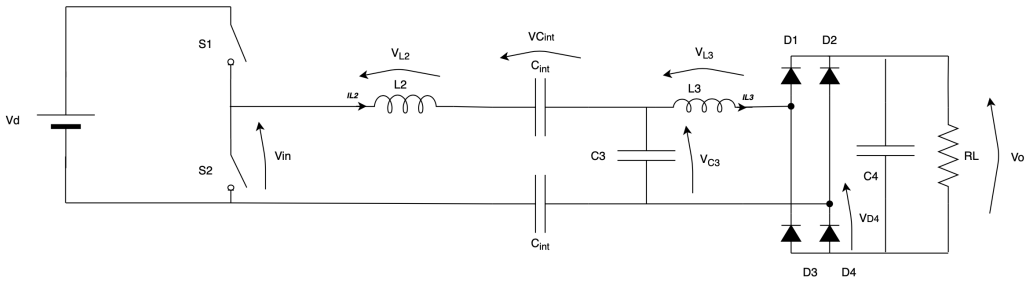

FIGURE 7.2: CPT scheme

The output of signal generator, properly configured(1MHz 0-5V square-wave), was connected to the PWM input pin of the EVALMASTERGAN1. Since the in-board 220V 50Hz rectifier stage was not mounted the DC voltage Vd that should be provided to the inverter fig.7.2, was generated by Rigol DP832. The maximum voltage that the DC power supply can provide is $60V_{DC}$, value sufficient to verify the operation of the circuit but lower than the 310 V with which the circuit was designed.
The output of the GaN inverter was measured with the oscilloscope fig.7.3 and then was connected to the CPT board, fig.7.4. The signal is a 0-60V "square wave" with a frequency of 1MHz.

In figure 7.5 is reported the input inductor L_2 voltage, except for the magnitude, the waveform is the same obtained in the simulations fig.5.19.

The capactive interface sinusoidal waveform is reported in fig.7.6.
The output voltage is represented in fig.7.7, it is a constant voltage with a ripple due to the output rectifier stage.

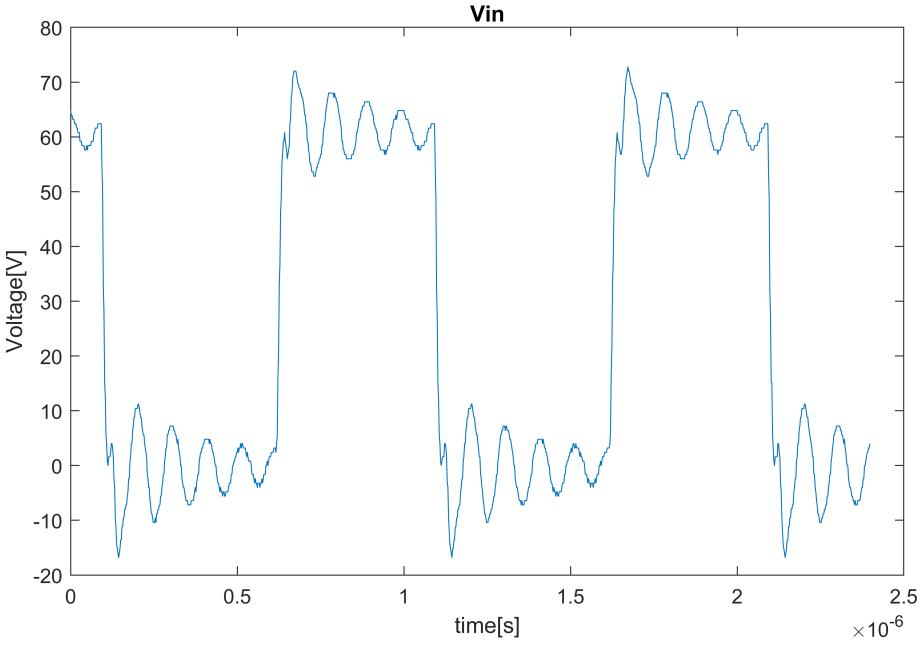

FIGURE 7.3: Inverter output voltage, in the scheme V_{in}

The results obtained in this final part of experimental measurements (reported in tab.7.1) confirm that the compensation network and output diode rectifier works correctly. The efficiency turn out to be very low, but the circuit is working with very different input parameters from those for which it was designed.

V_d	60V
I_d	16mA
V_o	1.5V
I_o	0.3A
P_o	0.45W
η	45%

TABLE 7.1: Measurement results

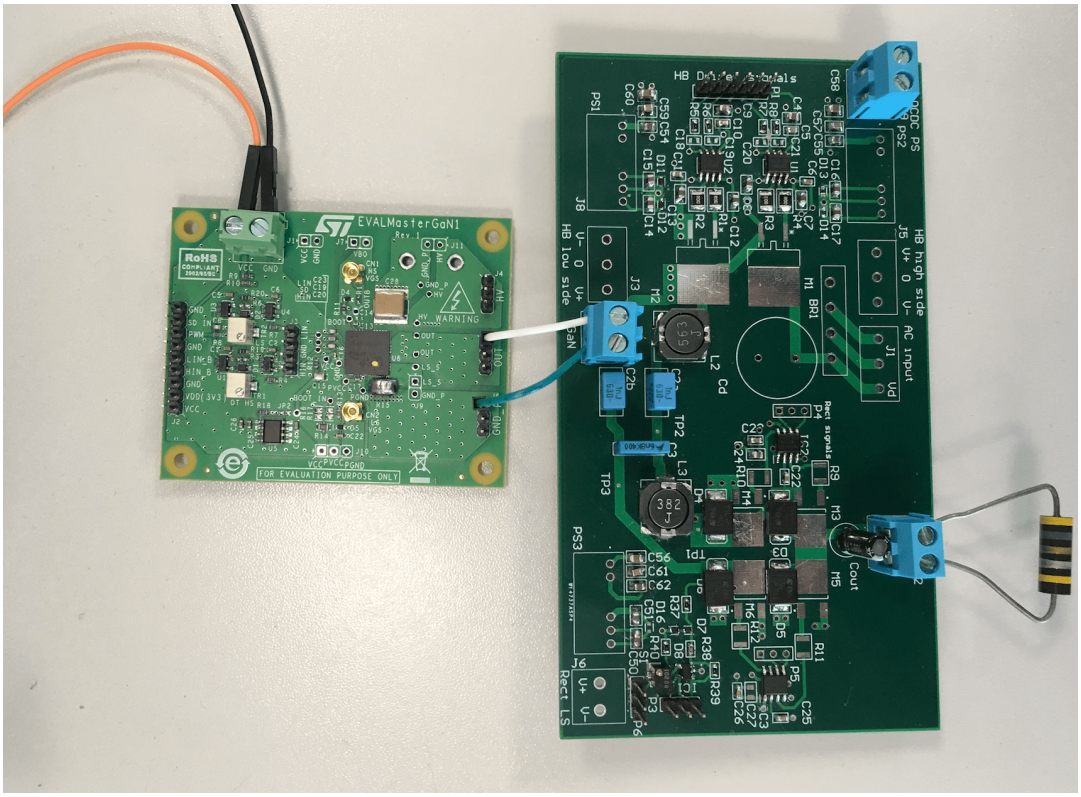

FIGURE 7.4: EVALMASTERGAN1 connected to the CPT board

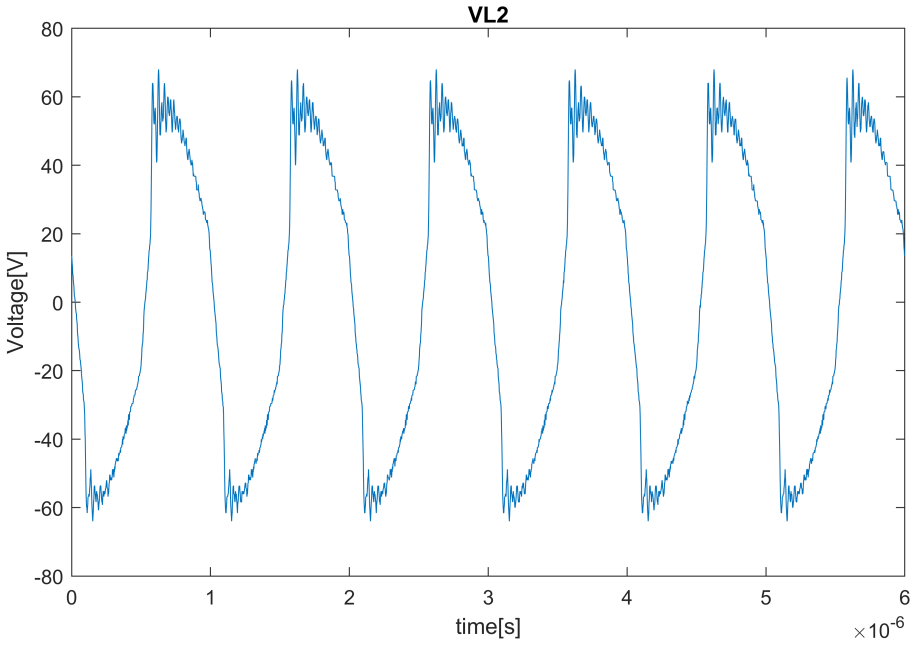

FIGURE 7.5: Input inductor L_2 voltage

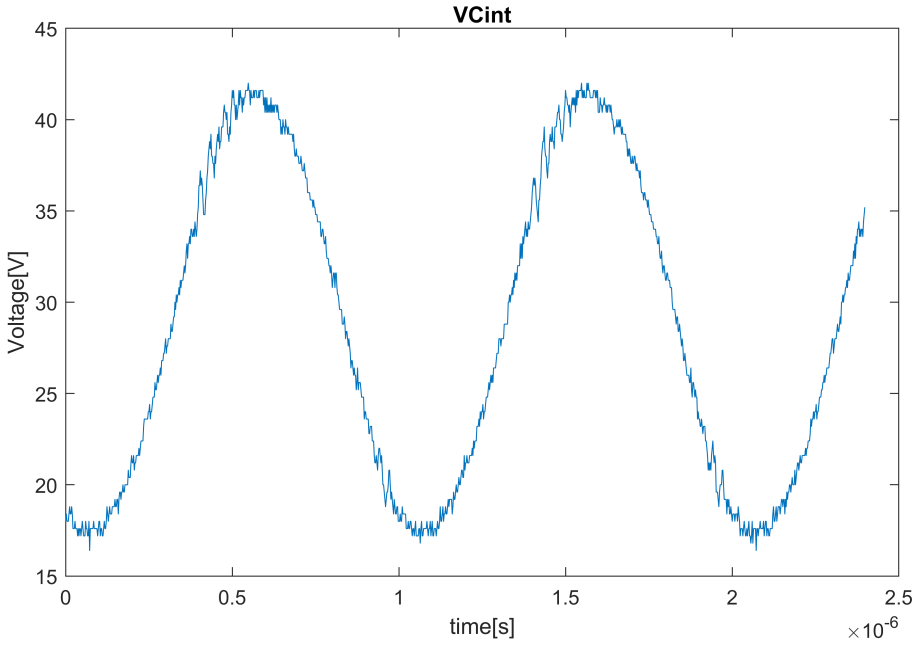

FIGURE 7.6: Capacitive interface voltage V_{Cint}

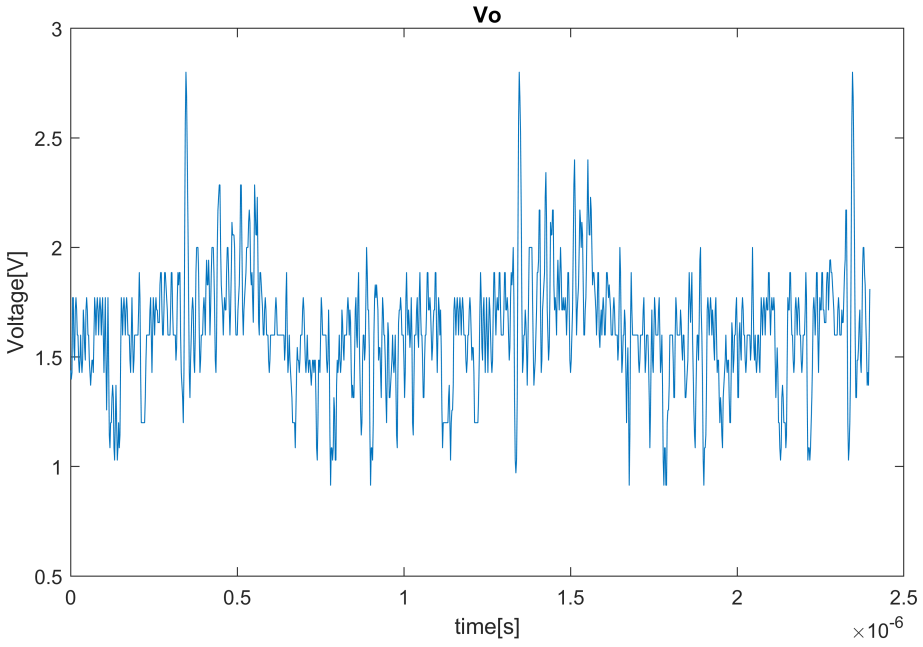

FIGURE 7.7: Output voltage V_o

Chapter 8

Conclusion

The thesis focused on the capacitive power transfer and its application on isolated converters. The application of CPT technology to power adapter is a very interesting topic in low/medium power adapter field. The possibility to implement the galvanic isolation without the use of heavy and bulky transformers it is a great advantage that could be an interesting topic to explore.

From the analysis of the presented topology, it was possibile to identify the input inductor L_2 as the most critical and stressed components of the circuit. Due to the high inductance values and to the stresses both of voltage and current.

From the real simulation results it is possible to confirm what has been obtained in the circuit analysis, the reduction from the 40W (specifications) to 34.2W (real components simulation) of the output power is only due to the losses of the compensation network, diodes and MOSFETs. The efficiency of 84% achieved it is a validation of the output power reduction.
Considering the using of CPT technology and the high input voltage conversion, from the rectified $310V_{DC}$ of the electric grid to the $20V_{DC}$ of the output voltage, the overall efficiency of the system turns out to be high compared to other solutions found in literature.

The last part of the thesis work was devoted to the layout implementation, components selection and board assembly.

8.1 Future works

Future works can be divided into three parts.
A first part will be devoted to a complete efficiency analysis of the circuit, highlighting the overall system efficiency as a function of load resistance R_L, input voltage V_{in} and working frequency.

A second part could be dedicated on the analysis of the circuit for a different load condition. In particular a constant voltage (such as a battery or a big capacitor) could be considered as a load.

A third part will be focused on the experimental measurement of the board first making a comparison between internal SiC MOSFETs and the external GaN board inverter.
The next step will be the experimental analysis using the output synchronous rectifier. A closed loop control system will be implemented in order to improve the system efficiency and to better stabilize the output voltage.

Chapter 9

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