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MASTER THESIS

Design and Characterization of a Power Supply Board for RF Avionics Application

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To my family...

Abstract

This thesis is focusing on the design of the Power Supply Board (PSB) of a Software Defined Radio (SDR) for a micro-satellites system intended to be compatible with NASA Deep Space Network (DSN). The thesis work has been carried out with the Italian aerospace company Argotec in Turin. The aim of the thesis is in accordance with the objective of Argotec company of designing an SDR to be used for their own satellites and to compete with current SDR in the aerospace market. The focal point is the definition of the architecture of the PSB and so the definition of the converters that will be implemented during the fabrication and the design of the primary isolated converter. After an initial survey and study of the different topologies which can be implemented for space application, several analyses are carried out in order to find which is the best architecture for our purpose using the LTspice software. After designed a custom isolated converter which is the core of the architecture, a Printed Circuit Board (PCB) is designed to better visualize the end goal and for tests.

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Acronyms

CCM Continuous Conduction Mode. 4

COTS Commercial Of The Shelf. 37

DCM Discontinuous Conduction Mode. 61

DPM Digital Processor Module. 90

DSN Deep Space Network. 1

ECSS European Cooperation for Space Standardization. 6

ESA European Space Agency. 13

FPGA Field Programmable Gate Array. 90

IC Integrated Circuit. 53

ICD Interface Control Document. 95

LDO Low Dropout Regulator. 33

LNA Low Noise Amplifier. 8

PCB Printed Circuit Board. 93

PSB Power Supply Board. 2

PSM Power Supply Module. 5

PWM Pulse Width Modulator. 60

RHPZ Right Half Plane Zero. 86

SDR Software Defined Radio. 1

SSPA Solid State Power Amplifier. 8

Chapter 1

Introduction

1.1 Background and Motivation

Small satellite systems are one of the most revolutionizing technologies of the last ten years and among the whole space industry. Lowering size and weight, reducing cost and time required to be developed, these systems have created an inverse trend that gave everyone access to space, both for scientific and economical purposes, supporting critical space missions.
Even if these systems are very attractive, they are also very difficult to be designed. One of the biggest challenges of these systems is communication: this is why satellites that are devoted to deep-space exploration are designed to work with NASA's greatest communication infrastructure, the Deep Space Network (DSN).
In small satellites, communication is often addressed by Software Defined Radio (SDR), being such kind of systems a compact, low power and flexible way to connect the platform or spacecraft with the ground station.
Communication is the key element to exchange information, commands, control data and more. However, the radios capability in connecting with Earth from millions of km away, with low signal power, exchanging data and tracking the orbit, required an extremely well-designed project. In fact, despite the large number of small satellites that are planned to be launched in the next years and the increasing number of companies that are starting to build small satellites, the market for SDR compatible with DSN includes very few

models.
One of the main aspects of an SDR is power management, the key element to optimize the RF signal power given the amount of energy that the satellite is able to reserve for the transceiver.
The work presented in this thesis is focused on the design and implementation of the power management of an SDR, following the requirements that space applications sets as lightness, smallness, radiation tolerance, reliability, cost, etc. Moreover, the kind of hardware which is under analysis comes with challenging requirements which make the design much more complex: high efficiency, noise immunity, output stability, low noise level at output, several heterogeneous loads to be managed, low ripple, etc.

1.2 Objectives

The goal of this master's thesis work is to provide an overview about the state of the art and perform the architectural definition of the Power Supply Board (PSB) of a new SDR given relevant performance and interface requirements. This in order to provide all the voltages and power to the different units of the radio (including the exciter, the receiver, the digital processing board, etc.) and then proceed with the circuit design of the main DC-DC converter included in the architecture.
An extremely relevant aspect of this thesis, that makes it an even deeper learning experience, is the collaboration with Argotec. Argotec is an aerospace engineering company based in Turin and with a US subsidiary in Maryland which will take part in two NASA missions with their micro-satellites ArgoMoon and LICIACube in 2021.
The focus of Argotec in building small satellites for deep-space applications and to support telecommunications around Moon and Mars, and its philosophy in having an all in-house implementation led this thesis work to become more than an experimental thesis. With the aim of producing its own SDR for its satellites and putting it on the market, this thesis is the reflection of how such so complicated systems are studied, simulated and produced in the next generation of aerospace products. The objectives of the thesis work can be summarized in the following list:

- Literature study of power management in Space borne systems and of Software Defined Radio;

- Definition of the specification and of the possible architectures that can be implemented in the PSM;
- Studying and analysis of the different converters;
- Selection of the best architecture for our purposes through comparison;
- Design of the main converter of the board and filters;
- Design of the PCB;

1.3 Thesis outline

The following lines provides a description on how this thesis is organized:

- **Chapter 2, Software Defined Radio in Space Borne Systems**, define some information of the SDR and its sub-units, as well as some introduction about electronics in space application, is reported;
- **Chapter 3, Definition of the Specification and Preliminary Study of the Possible Architectures**, clarification of specification of Radio and of the Power Supply Module and definition of the architectures that can be implemented
- **Chapter 4, Comparative analysis between converters and selection of them**, comparison between converters that can be adopted for the architectures
- **Chapter 5, Comparison process between architectures based on physical parameters**, the architectures are compared based on the main important parameters, like physical parameters, complexity, cost, etc
- **Chapter 6, Comparison Process Based on Output Voltage Stability, Out-put Ripple and Noise Level**, the remained architecture are compared based on the noise and output stability that provides
- **Chapter 7, Primary Converter Selection**, the main converter for the PSM is selected

- **Chapter 8, Fly-back CCM design**, the main converter is designed, reporting all the problems and the relative solutions. Also feedback loop design is described as well as load balancing feature.
- **Chapter 9, Rest of the PSM Design**, the PSM designed ends with some minor develop of the EMI filter, Connectors, Telemetries and the design of the PCB
- **Chapter 10, Conclusion and Future Work**, the thesis work ends by highlighting the results and the main future objectives of Argotec's SDR project.

Chapter 2

Software Defined Radio in Space Borne Systems

2.1 Power Electronics in the Space Environment

Every kind of system, from an electronic one to a mechanical one, that is designed to work in a space-borne environment, is subjected to several conditions that complicate the project from a physical point of view to a budget one.
Power electronics, during the last 20 years has emerged, especially in the space borne field, becoming in this way part of the most studied and applied for satellites and spacecraft.
In such kind of system, power electronics play an important role. Power board has the significant task of converting the power stored in the batteries or coming from the solar panels to all the modules and subsystems. Nonetheless, it is in charge of avoiding the propagation of electronic failures generated in other subsystems or in the power module itself. Moreover, part of the electronics hardware is reserved for monitoring the status of the subsystems which are feed by the PSM thanks to telemetries.

Power electronic boards implemented for space applications are subjected to extreme specifications and requirements. Besides the physical requirements which in general are very restrictive, since spacecraft and satellites are

always designed to be as smaller and lighter as possible, in addition to being designed to withstand the drastic environmental condition present in space, including radiation, absence of air which complicates the power dissipation process, high temperature differences, the power board has to be extremely reliable since if one the subsystems fail, it can compromise the success of the mission. Reliability is ensured in different ways:

- using derating standards
- using high reliable components
- implementing redundancy

Derating standards are part of the European Cooperation for Space Standardization (ECSS) standards previously discussed, which ensure the correct functionality of the systems and subsystems for all the European space activities. ECSS-Q-ST-30-11C - Derating document provides to customers a guaranteed performance and reliability to all the equipment implemented in these activities up to the end-of-life cycle [1]. For each kind of electric component, the ECSS-Q-ST-30-11c specify, in percentage, the margin on the maximum rating of each component that shall be considered to ensure good performances up to the end-of-life-cycle of that component.

High reliable components are those kinds of components that are built with material which well operate in harsh environments and under high stress operating condition. In space environment, it is suggested to use:

- high vibration resistance components
- out-gassing material, which avoids to release of fluids
- high temperature variations resistance material
- radiation resistance material

Redundancy, instead, is a feature that is good to have, but not imposed from any standards. It is part of a well established design, which has the aim of parallelizing each device and component, avoiding, in this way, the one point of failure structure.

2.2 Definition and characteristic of SDR

Software Defined Radios (SDR) are the next generation radios that have rapidly change the communications industry in the space field [2] [3]. They are implemented in spacecraft or satellites of small dimensions and communicate through them with an interface for sending and receiving data. Advantages of the SDRs are the reusability of the firmware and software, with the possibility of replacing it without any hardware changes, low power operation mode, low cost and compact design.
These benefits allow this type of radios a large impact and usability in space applications and there are involved in various network topology available for communication in the space:

- Near Earth Network; [4]
- Space Network; [5]
- Deep Space Network. [6]

The frequency operation of such kinds of radios is quite large: it spans from the UHF up to Ka Band. Key requirements of this type of system are higher data-rates, multi-channel and multi-band operation and advanced coding scheme, which allow the radios to be used in different kinds of missions and purposes.
The applications of an SDR are mainly focused on the communication between the spacecraft/satellites and earth, using the type of network in which the mission is operating. SDR are often used also for tracking of the orbit, especially in Deep Space missions, in which SDR give support to the spacecraft/satellite for the adjusting maneuver according to the orbit line due to the high distance from earth, complicating in this way the spatial control of the spacecraft/satellite.
Another interesting features of the SDRs are the modularity of their architectures. In fact, in order to allow flexibility in operation, building and integration phase, SDR units are always implemented in different layers. Each radio is usually composed of 4/5 different functional units.

The main ones usually include:

- **Digital processor module**, that carries the re-programmable processing components, like FPGA (and microprocessors). Devoted for the main task of the radio, this module performs the signal processing for modulation and demodulation functions, as well as tracking of the orbit and managing of the radio status, handling all the other slices of the radio. It also contains all the Rad-Hard memory elements;

- **Power Supply Module** has the purpose of providing several regulated voltage references from the unregulated bus coming from the spacecraft/satellite. Using different DC-DC converters, it carries the voltage and current which provides the necessary power to the different units and components of the radio. Other features of the PSM are the control of relative output voltage noise and stability which becomes important when these voltage references are used for RF modules;

- **Transmitter**, that using an exciter modulates the output carrier in the in-phase and quadrature (IQ) digital waveforms. With the help of a Local Oscillator, the signal is up-converted to the desired band;

- **Receiver**, devoted to the down-conversion from the desired band to the base-band or onto an intermediate frequency and then filtering and low noise amplification is performed.

The radio performances are enhanced with the help of other two (external) units, the Solid State Power Amplifiers (SSPA) and Low Noise Amplifier (LNA).
SSPA is a power amplifier that has the role of amplifying the signal power before sending it. It is part of the transmitter chain. LNA is an amplifier suitable for increasing the useful signal power with respect to the noise. It has a lower gain in contrast to SSPA, but its capability of recognizing the signal against the noise and increasing it allows this unit to be implemented in the receiver chain, in which, usually, the noise is important. These units can be integrated into the radio or separated according to the amount of power that they can dissipate, to avoid reaching higher temperatures.

Table 2.1 shows a possible configuration of SDR architectures. In this picture, a modem in base-band is introduced. In some cases, it is preferred

Receiver (Rx)
Transmitter (Tx)
Modem Baseband
FPGA
Power supply

Table 2.1: SDR architectures

to introduce an additional layer in the radio architectures to set up extra features for the radio. For instance, other layers could be used for creating multi-channel operations.
In the design phase of the architectures of the radio, a few considerations on the position of the layer about temperature dissipation could be done. Since the radio has a case which is shielded for the protection against radiation, therefore is extremely thicker, it is also especially complex to deal with temperature dissipation when it rises to 100°-120°C. A naïve solution is to design the radio by placing the hottest layer at the top or at the bottom, directly in contact with the shielded case, sharing one of the faces of the board, therefore increasing the power dissipation capability. Usually, PSM and DPM are the hottest.

Chapter 3

Definition of the Specification and Preliminary Study of the Possible Architectures

In this section are declared the specification and the requirements of the SDR and of the PSM. Moreover, are specified those architectures that can be implemented for the PSM with a short briefing of each of them.

3.1 Reference specification of the radio

The design of such kinds of systems is one of the most challenging projects that private aerospace industries are facing in the last decades. Having to work with such a large number of components, building different interconnected layers, resistant to radiation and huge temperature changes, in minimal space and weight, with the lowest cost as possible, has released in the aerospace world economy quite a few models, raising the bar of the capabilities and features that these radios have to afford for competing in this market.
The specifications that are discussed and listed in the following lines are not confirmed design specifications. Since Argotec‘s SDR is still under development, all the specifications and requirements imposed in this thesis work can be changed or modified, in terms of output voltage levels, power delivered at each line, physical constraints, RF operation band and so on.
In fact, these requirements are still being analyzed, taking as reference the

other radios models. Indeed, some of the requirements, which are used for this thesis work, are comparable with these models.

EXPECTED REQUIREMENTS	
Operation band	S-K band
Mass	1Kg
Form Factor	PC-104
Max power consumption	50W
Power interface	20-40V

Table 3.1: SDR requirements

Table 3.1 reports the main specification of Argotec SDR. In the max power consumption specifications may be included also the power required by the SSPA and LNA, taking into account that the power amplifiers of the SSPA will deliver at least 4-8W to RF power. The radio is not always working at 50W continuously since the radio is capable of performing different tasks which require different level of power.
As described in chapter 3.2, the PSM is directly connected to the unregulated bus of a spacecraft. One of the main goals of Argotec is to develop an SDR which is compatible with as many spacecraft as possible; in this way, the unregulated bus voltage range that PSM shall accept from the spacecraft must be wide and to prevent damages from over-voltages.
Thereby, in order to design an SDR which can be employed in plenty of circumstances, with several unregulated bus of different spacecraft, and so, by different aerospace companies, the voltage level at which the PSM is designed is 20-40V. This input voltage range allows the PSM and to Argotec‘s SDR to be implemented in several missions since it covers the largest amount of spacecraft unregulated bus voltage.

3.2 Reference specification of the Power Supply Module

Since this thesis work is focused on the design of the Power Supply Module of the SDR, the specifications listed in table 3.1 give us the first requirements that should be met in the project of the PSM.

The PSM characteristics depend on different factors:

- Interface requirements, based on the input and output quantity that it shall provide;
- Power requirements, useful as interface one, describe the amount of power that this board shall provide at max operation;
- Noise quality at input and output;
- Physical requirements, justified by the SDR dimensions and mass;
- Protection requirements, like inrush current, damaging by interruption of power and by short-circuit, etc.

As explained in the previous section, some of these specifications are not confirmed: the output voltage reference and power that the PSM shall provide, are not defined, but based on a preliminary design and according to the required amount of power for the units of the radio, the regulated output voltage with the relative output power are more or less:

- +8V at 20W for the SSPA
- +6V at 30W for the DPM
- +5V at 1W for the SSPA
- -5V at 50mW for the SSPA
- +4V at 0.7W for the LNA
- +3V at 0.2W for the SSPA

Recall that the power interface of the SDR which is presented in table 2.1, is also valid for the PSM, since the unregulated bus voltage interface coming from the spacecraft/satellite into the radio, is directly connected to the PSM.

Some other requirements like output voltage stability and output noise level, are not clear now: these specifications will be analyzed in the future study of SDR that Argotec is doing. Probably they will be imposed on the output reference used by the units of the radio that have deal with the RF signal for telecommunications.

For the physical requirements of the area and weight of the PSB, they can be extracted from the ones listed in table 2.1, by taking into consideration that the radio is composed of 4 layers:

- Weight < 250g
- Volume: 96mm x 100mm x 18mm

The specification of the volume is extracted from the standard PC-104 form factor.

In the end, the last requirements that PSM shall respect are the ones related to the protection and noise immunity. The PSM, as a subsystem of a bigger system that is the radio, is subjected to the same standard control that any system and subsystem in the aerospace engineer world is subjected to. Taking as reference the ECSS standard on electromagnetic compatibility (ECSS-E-ST-20-07C Rev.1 – Electromagnetic compatibility [7]), which are the one that the European Space Agency (ESA) has listed for their mission subsystem, a list of all the parameter scanning from the inrush current to the mask of the Conducted Emission and Conducted Susceptibility noise can be found. The information presents in this document will be discussed better in chapter 4, when they will become part of the comparative analysis of the architecture, that gives rise to the circuit model of the PSM.

Figure 2.1 shows how the PSM plays a crucial role in the SDR system. It is in charge of delivering the requested amount of power to all the modules and subsystems. Usually, it also provides power to the SSPA and LNA,

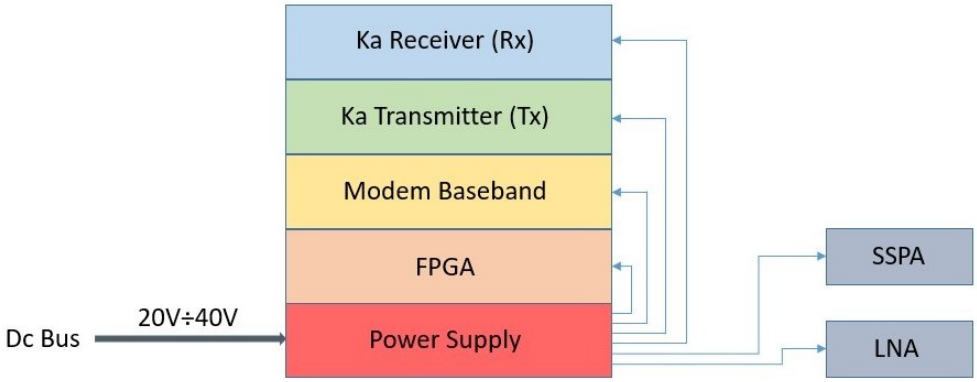

Figure 3.1: SDR, SSPA and LNA subsystem power connection

which are not integrated into the radio system. In the Argotec design of the SDR, the SSPA and the LNA maybe not feed by the PSM, which is inside the radio, but from the SSPA and LNA subsystem itself. This design feature will be analyzed and implanted just in case the PSM is not able to provide all the power to these subsystems if they will require a higher amount of power. SSPA, in fact, is the module that will absorb the largest amount of power in the radio and according to Argotec objectives, the SSPA will be powerful than the SDR models available in the market.

3.3 Definition of the architectures

. The architecture design is focused by a variety of parameter: not only physical specifications like area, volume and weight becomes meaningful for the PSM project, but also flexibility, efficiency, scalability, redundancy and cost are examined with the aim of developing a well-designed architecture of the PSM, able also to be easily adjustable if further changes will come up.

Several types of configuration can be used in the power electronic management, but in this case, since several output voltages levels must be converted from one unregulated bus, the architectures are very similar and they look like a crown of a tree: multiple output lines from a single input one.
Before going on with the definition and description of each of them, a clar-

ification for better understanding the architecture structure and converters name is necessary: all the converters that are directly connected to the unregulated input bus are called “primary converters”. All the converters that, instead, are connected to the primary converter and provides the output voltage references are called “secondary converters”.

Figure 3.2, 3.3 and 3.4 shows the different architectures that can be implemented for PSM of the Argotec‘s SDR.

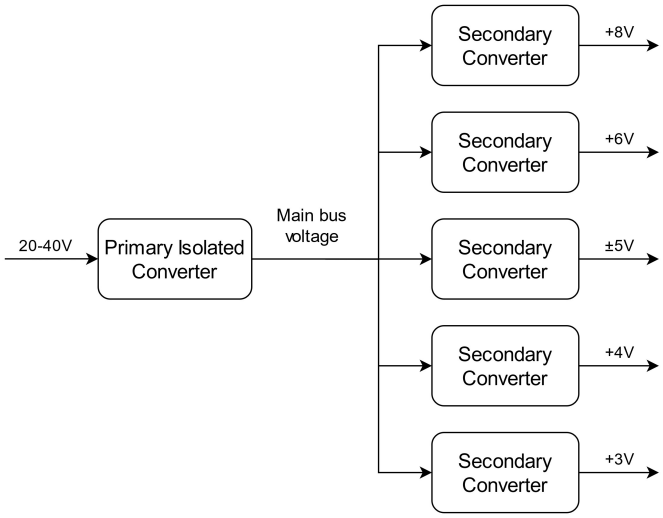

Figure 3.2: One isolated architecture or Family 1

Figure 3.2 displays a solution in which the unregulated input bus is directly connected to an isolated converter. This last one translates the unregulated input voltage to a fixed one, called main bus voltage, at which all the other secondary converters are connected. The output voltage of the isolated converter is not designed yet, since it is not necessary to define it at the moment.
Secondary converters, in this case, are not isolated since isolation has been introduced on the primary side.

Figure 3.3 shows the solution where no primary converter is used. Instead, a series of isolated converters are implemented, in which each of them

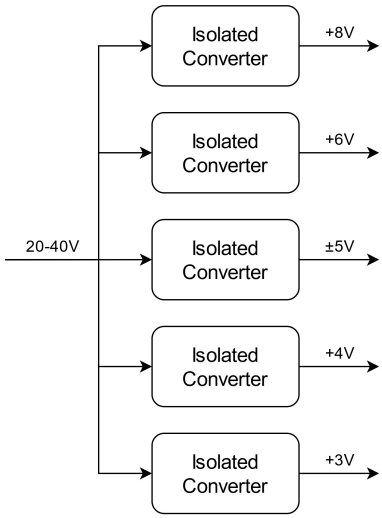

Figure 3.3: Multiple isolated architecture or Family 2

provides the different reference output voltages and the power for the other SDR modules. Is clearly visible that the isolation is introduced by each converter.

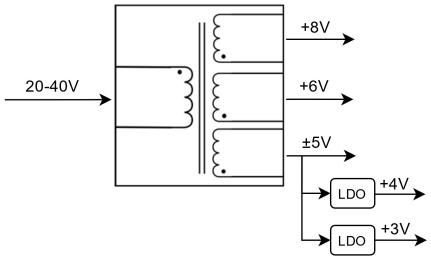

Figure 3.4: Fly-back multiple output architecture or Family 3

Figure 3.4 shows the solution with the Fly-back multiple output topology. In this way, the primary converter and secondary one are integrated into a

single converter. With this solution, the isolation and the conversion for the multiple outputs levels are merged in a key component. LDO linear regulators are appended for generating the remaining reference voltages without increasing the number of outputs of the Fly-back. LDO for +4V and +3V are attached to the +5V reference voltage since the dropout voltage is minimized and also because the power levels are low at these outputs.

Before going on, a clarification is needed: the listed architectures represent just a general topology; they can be better classified as a "family of architectures" since each architecture has different combinations according to which type of converter can be used. For example, taking as reference the Family 1 of figure3.2, by substituting one of the secondary non isolated converters with an isolated one, a different architecture is obtained, but the principle behind that architecture is based on the Family 1. Same works with Family 2 of figure 3.3 interchanging the isolated converters with a non-isolated one.

3.4 Preliminary study of the architectures

The goal of this section is to provide a general overview and description of the 3 main different architectures. The crucial aspect of each of them is illustrated, standing out the pros and cons between them which, unfortunately, are not enough for pointing out the most suitable architecture for PSM. This process is better discussed in the next paragraph, through which all the analyses are carried on and the best architecture for our purposes is obtained.
The architectures are analyzed according to several parameters. In the list below are reported just the main ones:

- Efficiency
- Isolation
- Area
- Weight
- Cost

- Complexity
- Number of components

Starting from architecture 1 is possible to notice that is the one which occupies the largest amount of area and weight. The primary converter support isolation which is an interesting feature in this application. Since the power is coming from the unregulated bus of the spacecraft/satellite, having isolation between the satellite and the PSM ensures that noise, instantaneous peak voltage and current do not interfere or damage the PSM unit and its components. Having just one primary converter between main bus and secondary converters, in case of failures, can compromise the functionality of the PSM and of the whole radio. Adding another primary converter, can increase the lifetime of the radio.

Going on with architecture 2, it can be observed that the total number of converters has decreased. The most interesting feature of this architecture is the redundancy: even if one of the secondary converters fails, the other ones can continue to operate with their own isolation. In contrary, if any noise or peak voltage arrives from the unregulated bus, these irregularities are reflected at the output reference voltage, and if it provides power to an RF component the quality of the telecommunications decreased.

In the end, architecture 3 is the simplest one: a single Fly-back converter, with 3 multiple outputs, is able to provide part of the necessary output reference voltages. With the help of a smaller switching regulator or with LDO, other reference voltages are provided. In this all-in-one component, thanks to the bulky 3 output coupled inductor, isolation is obtained between input and the 3 main outputs. The physical gains of these components in terms of occupied area and weight are in contrast with the output stability of the reference voltage: in fact, since they share the same coupled inductor, the 3 main output voltages are influenced by each other due to cross regulation. This means that each output reference voltage value can shift, sometimes even significantly, according to the amount of power that the other output reference voltage is carrying.

Chapter 4

Comparative Analysis Between Converters and Selection of them

this chapter has described the process through which the best architecture is obtained starting from the 3 different ones. The process is subdivided into different phases. Each phase is analyzed and executed in the most objective way as possible, figuring out the best architecture at each step.
Being this process complex and extended, a flow chart is reported at each step to better explain how this study is carried on.

4.1 Preliminary Consideration

When a generic electronic board has to be design, the architecture selection is usually carried on based on a high-level approach. The whole topology of the board is subdivided into several macro models which makes the design of the board less complex to be defined.
At this point, each macro model is obtained by averaging each feature of the components inside that macro model, from the physical point of view to an electrical one.
In this way, each macro model can be as a black box, which contains a defined number of components and can be studied and analyzed according to each averaged characteristic. Then the selection process can start: comparing the physical and electrical averaged characteristic of each architecture, taking in

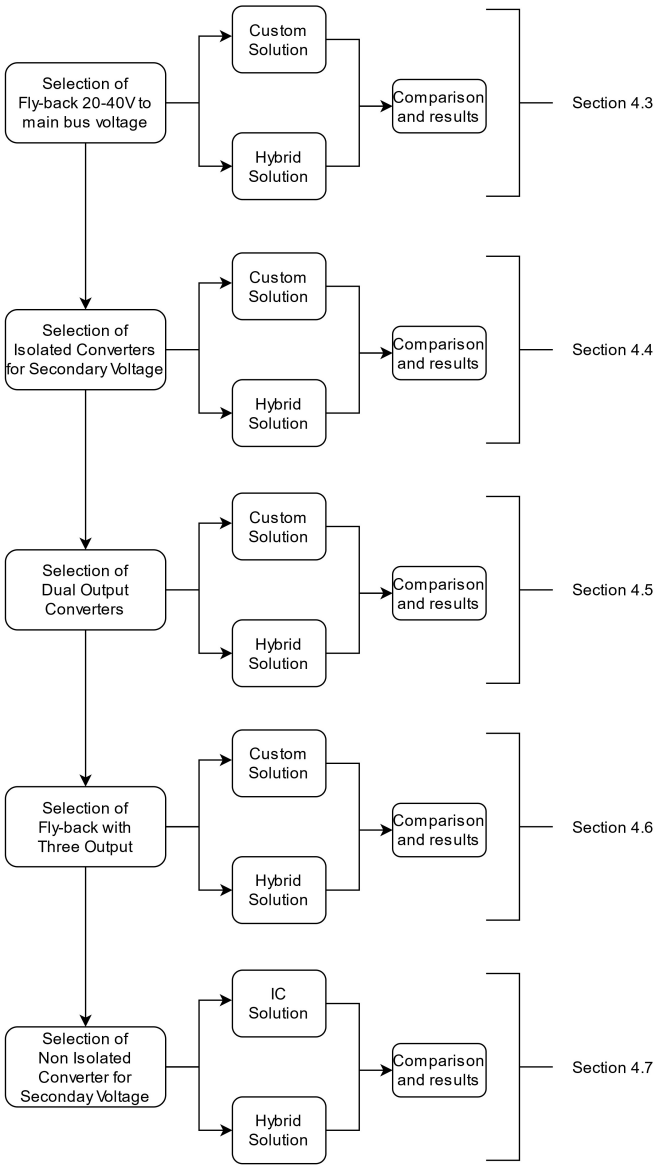

Figure 4.1: Flow chart of selection process for the converters.

care that some of these characteristics are more relevant than others, the final architecture is found.
In contrary to what is generally done when an architecture must be select, in this thesis work the approach was different: from low level to high level. In fact, instead of averaging each component (converter in this case) of each architecture, a DC-DC converter is directly compared among all the few possibilities, and the best one is chosen.

This approach can be used for two simple reasons: first, looking at each of the 3 families of architecture, and taking in consideration all the combinations of each of them, the plausible DC-DC converters are just these ones:

- One output converter: from 20-40V to main bus voltage (regulated voltage) (family 1)
- One output converter: several outputs (families 2 and 1)
- Two output converter: dual output ±5V (families 2 and 3)
- Three output Fly-back: from 20-40V to +8V, +6V, ±5V (family 3)
- One output non-isolated buck: several outputs (families 1 and 2)

The other important reason based on the low-to-high level approach is that the SDR, as its subsystems, including the PSM, should have space flight tested components. In fact, as was discussed in chapter 2, space flight tested components are radiation tolerant, low out-gassing, high temperature resistance, long life cycle, etc., all characteristics that reduce the failures rate of the component and give a higher probability of the success of the mission.
All these features make these components to be tested for thousand of hours, making them expensive and mostly scarce. Very few electronic companies are producing space flight tested components, which means very few components models are present in the market, which are still lower when the production is concentrated on DC-DC converters.

Nonetheless, in different well accomplished space mission, from low-orbit to moon and mars ones, have been used non space flight components. In fact, in some cases, the trade-off between cost, volume, weight and performances become relevant and commercial components can be preferable instead of space flight ones. However, those commercial components are subjected to

several tests, from temperature to vibration ones before being implemented in a space board.

If the design was made for ground application, the low-to-high level approach was meaningless: given the large number of COTS DC-DC converter models, it would difficult to compare them and find the best one for each situation.

4.2 Comparative analysis between converters based on the main characteristics

This section is dedicated to the comparison for each converter listed in section 5.1 based on the main characteristics for the converters and for the whole PSM.
The characteristics are listed in order of importance:

- **Input and output quantities:** the part number are chosen based on the input voltage range, the output voltage range and the maximum delivered power;
- **Physical quantities:** area and weight play a crucial role in this selection. The heaviest and largest components are discard;
- **Efficiency and cost:** the part number are compared according to the efficiency in the expected operating point and cost.

Efficiency and cost are not so important in this phase since area and weight of the whole PSM are the most restrictive requirements to be respect. This is mainly due to the low volume and weight that the SDR must occupy in a satellite or spacecraft. Moreover, must be taken in consideration that space flight tested component are heavier and larger than commercial components which makes these requirements even more restrictive.

This selection process take in consideration also different type of converters like:

- **Hybrid converter:** these converters are built on a very small PCB or on a die above a ceramic substrate, surrounded by a thick metal box with the aim of protecting the PCB from radiation. Inside this black

box are mounted all the components needed for implementing whatever kind of electronic unit. They are bulky and heavy but the efficiency is reasonably good. They are the simplest solution in the market: they have just be soldered on the PCB, sometimes with an EMI filter, but they are the most expensive, around 15k/20k€. Figure 4.2 shows some of this.

- **Integrate circuit (IC) converters:** these ones are, instead, just a part of the whole converter. In the IC there are the controllers for the feedback loop, the driver of the mosfet and the mosfet itself. Other parts of the converters instead must be added separately, like the transformers or coupled inductors. These are the lighter solution and occupy less area with respect to hybrid. Even if they required other components for building the whole converter, they are the cheaper ones. In general, they are not so complex, but they require a bit of design.

- **Custom converters:** this is the most complex solution. They are heavier than IC but lighter than Hybrid. The cost is much lower with respect to Hybrid ones, around 4k/5k€. This solution is a good trade-off between the previous ones. Complexity for this type of converters has to be considered, since it requires a challenging design.

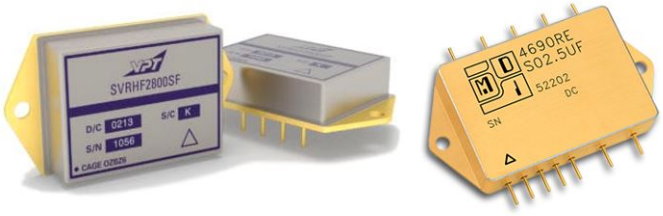

Figure 4.2: Hybrid converters.

4.3 Selection of Fly-back 20-40V to main bus voltage

This Fly-back corresponds to primary converter implemented in the architecture 1. (Figure 3.2). The main bus voltage is not fixed at the moment since it can be tuned easily later.
For this type of Fly-back there is only the Hybrid and custom solutions since IC isolated converters space grade components are not available in the market.

4.3.1 Hybrid Solution for Fly-back 20-40V to main bus voltage

Selection of Hybrid Converters Based on Electrical Quantities

In table 4.1 are reported the best hybrid rad-hard converters available in the market which satisfy the electrical requirements. The first five of this list are coming from VPT [8], the others ones from MDI company [9].
Recall that this type of converters are the simplest one: they just need to be soldered on the PCB and no design is required.

The output ripple voltage is not reported since there were not important differences.
In red are highlighted the power values which are too low for the PSM.

Selection of Hybrid Converters Based on Physical Quantities

Proceeding with the selection, the next step is dedicated to physical characteristics. Looking at the area parameters, on table 4.1, no important differences are noticeable between the remaining converters. Instead for what concerns weight, the last two converters of MDI weight almost double with respect to the VPT converters, due to the presence of the EMI input filter. They are highlighted in orange. At the end of the physical parameters selections phase, just 3 converters are still in the game.

HYBRID CONVERTER CHARACTERISTICS					
Part number	Vin	W	Area	Weight	EMI
SVLTR2800S	15-50V	40W	20,9cm^2	55g	no
SVRTR2800S	18-40V	40W	20,9cm^2	55g	no
SVRFL2800S	18-40V	100W	29, 1cm^2	88g	no
SVFL2800S	16-40V	110W	29, 1cm^2	86g	no
SVLFL2800S	16-40V	110W	29, 1cm^2	86g	no
5193	18-50V	40W	24, 6cm^2	90g	yes
5031	18-50V	75W	34cm^2	160g	yes
5031A	18-50V	100W	34cm^2	160g	yes

Table 4.1: Hybrid converter for architecture 1.

Selection of Hybrid Converters Based on Efficiency and Cost

Lastly, the efficiency and cost parameter are analyzed. These last 3 components are made by the same company and they have almost the same characteristics. In fact, also the cost is similar between them.
Taking a closer look at these components through the datasheet and focusing on the efficiency graphs, is possible to notice that the SVFL2800S have the best efficiency behaviour for the 50W load condition. Figure 4.3 report the efficiency curves for SVRFL and SVFL hybrid converter [10] [11] .

4.3.2 Custom solution for Fly-back 20-40V to main bus voltage

The alternative for the SVFL2800S Hybrid converter is the custom solution. The parameters considered for the custom Fly-back were related mainly to physical and cost since the electrical ones are tuned according to requirements. Weight, area and cost can be easily calculated by summing each parameter of the component that built a Fly-back.
While the complexity of designing a custom converter is well known to be

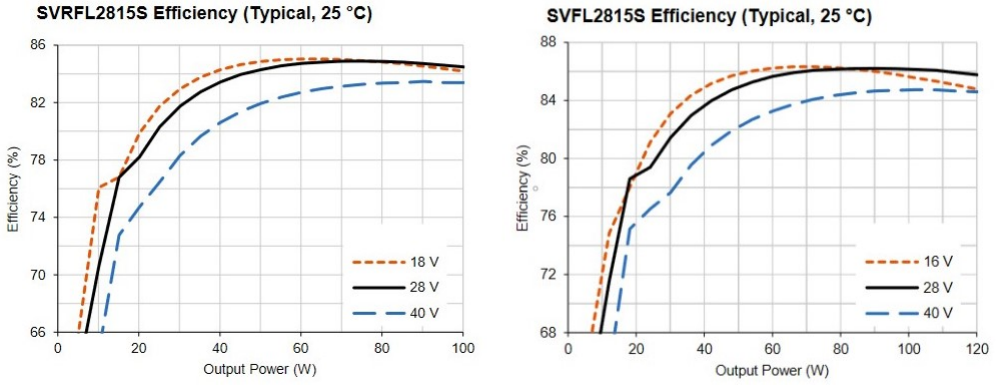

Figure 4.3: Efficiency over Power curves for SVRFL and SVFL [10] [11].

challenging, the efficiency is complicated to be extracted a priori. Making a reasonable approximation based on the average efficiency for a Fly-back converter, 70% to 75% can be reached without difficulty.
Table 4.2 report a list of the components, with their own physical and cost parameters, necessaries to build a Fly-back converter. In the table is considered also the feedback path, composed by a PWM controller and an isolation transformer, in order to introduce isolation also in the feedback loop. The designed of the Fly-back for this phase is based on a general topology where the estimates are rough, but still good for the comparative analysis goal. The parameters are coming from real component part number that can be actually used for this design.

4.3.3 Results of Fly-back 20-40V to main bus

Comparing the results of table 4.2 of the custom Fly-back with respect to SVFL2800S Hybrid converter from table 4.1, it can be notice that the custom Fly-back converter has a lot of advantages in terms of physical parameters and cost. In contrary, custom Fly-back has a higher complexity compared to the hybrid converter. In fact, if the hybrid converter has just to be soldered on the PCB, for the custom Fly-back there are an extremely long and tough procedures before it can be mounted on the PCB of PSM: starting from the choice of the topology, which depends on power, input and output voltage, an iterative process is often necessary to tune the components values. Once

Custom Fly-back			
Component	Area [cm^2]	Weight [g]	Cost [€]
Coupled inductor	$2cm^2$	4g	40€
Mosfet	$1cm^2$	1g	1500€
Schottky diode	$0.2cm^2$	0.5g	10€
RCD snubber	$0.3cm^2$	1g	15€
RC clamp 1	$0.5cm^2$	2g	10€
RC clamp 2	$0.5cm^2$	2g	10€
Out capacitor	$0.7cm^2$	1g	10€
In capacitor	$0.7cm^2$	1g	10€
PWM controller	$0.3cm^2$	1g	900€
RF transformer	$0.9cm^2$	4g	20€
EMI filter	$2cm^2$	4g	40€
Output filter	$2cm^2$	4g	40€
Result	$\mathbf{15cm^2}$	**25.5g**	**2605€**

Table 4.2: Custom Fly-back components and parameters.

chosen the right part number, a simulation via software is recommended for controlling how the converters works and make changes if needed, before designing the layout of the board.
Last, but no least, the testing procedure is necessary and require plenty of time: tests must be performed not only on output characteristics like output voltage, output ripple voltage and maximum available power, but also on primary and secondary current, incoming and out coming noise (better known as Conducted Emission and Conducted Susceptibility, better described in next paragraphs), power losses of each device (Diode, Mosfet, passive snubber circuit, Couple inductor, etc) and also tuning of components, that is usually mandatory.
Moreover, these tests should be repeated for different values of temperature, and if the board is designed to work in space environment, also a thermo-vacuum tests are compulsory.
However, also these tests must be performed on the hybrid converter, to verify the correct operation. Since it was already tested by the home company, it is reasonable to expect much less complications than a custom Fly-back,

taking in care that at each fail test of the custom Fly-back, a re-organization or even a redesign is needed, with new tests phases.

Another consideration which is relevant in order to choose one of the two converters is based on Argotec plans for the SDR project: since the objective is to built several of them, the low cost of custom Fly-back can play an important role, even if it require a longer process of development and tests. In fact, even being optimistic with the cost of the hybrid and being pessimistic with the cost of custom Fly-back, hybrid converter cost more than three times the custom one. Taking as an example of 50 PSM, the estimated cost for hybrid converters are 300.000 €extra than the custom one.

Hybrid and custom solutions have its own pros and cons which are completely different. Though these differences are relevant, it is to yet to prefer one solution instead of the other one since Argotec's SDR is still under development: number of SDR units, budget, project time and other information are not defined yet and may influence the design development.
The custom solution is the preferred one, for the low area and weight and most importantly the cost, but the Hybrid solution is not discarded for the reason explained above.

4.4 Selection of Isolated Converters for Secondary Output Voltages

These converters can be used in architecture 2 (Figure 3.3) and for a possible combinations of architecture 1. In this case must be choose a converter for each output reference voltages. Given the low power and the low input-output voltage range, the best converter for this specs is again the Fly-back. As specified for converter 20-40V to main bus voltage, also in this case no IC solution were available.

4.4.1 Hybrid Solution for Isolated Converters for Secondary Output Voltages

Selection of Hybrid Converters Based on Electrical quantities

In table 4.3 are reported all the hybrid converters available in the market that satisfy the electrical requirements. Just the +8V, +5V and +3V output values were available. For -5V, +6V and +4V no converters were found.
All of them are compatible with the unregulated input bus voltage 20-40V from the spacecraft.

No further selection could be done at this point, since the physical and efficiency/cost comparison have no meaning due to low number of components and almost no differences.

HYBRID CONVERTER CHARACTERISTICS						
Part number	Vin	Vout	W	Area	Weight	EMI
SVTR2800S	15-50V	+8V	35W	$20,9cm^2$	55g	no
SVRHF2800S	18-40V	+5V	15W	$14.5cm^2$	27g	no
SVHF2800S	15-50V	+5V	15W	$14.5cm^2$	28g	no
SVRCH2800S	16-40V	+3.3V	1.2W	$7.5cm^2$	16g	no
3809	16-50V	+3.3V	2W	$5cm^2$	18g	yes

Table 4.3: Hybrid converter for architecture 2.

4.4.2 Custom Solution for Isolated Converter for Secondary Output Voltages

For this custom converter the solution previously defined in subsection 5.3.4 is take as reference. The characteristic reported in table 4.2 are a good estimation also for this solution, even though area, weight and cost are a bit smaller since these Fly-backs carries lower amount of power.

4.4.3 Results of Isolated Converter for Secondary Output Voltages

Also in this case the same consideration done in subsection 5.3.4 about the lower area and cost of the custom solution with respect to hybrid converter are valid for more or less all the hybrid converters reported in table 4.3, in contrast to the less complexity required by the hybrid. Both solution are still considered, even if a custom one, as saw previously, has more advantages.

A note must be made for -5V, +6V and +4V reference output voltage: no hybrid converter was found for providing this reference voltages and no custom converter is designed for -5V and +4V since it has no meaning to design such a complex Fly-back for carrying very low power.
For these two output reference voltages an alternative solution is required: in addition to non-isolated converters, which will be discussed in the next paragraphs, a plausible solution could be a Point of Load or an LDO. These two devices could be directly attached to a reference output voltage like the +5V or +8V and are very good for low power application. Space grade Point of Load and LDO are popular in the market but they are expensive. This solution is taken in consideration but it will be better analysed in further section.

4.5 Selection of Dual Output Converters

This converter can be implemented for architecture 1 and 2 (Figure 3.2 and Figure 3.3) discussed in section 4.2, for generating the ± 5V dual output voltage.
Again, no dual output rad-hard IC solution were available.

4.5.1 Hybrid Solution for Dual Output Converters

Selection of Hybrid Converters Based on Electrical Quantities

Table 4.4 report all the hybrid dual output converters for ±5V output voltage. Once again, in this list are display just those converters that respect the input voltage range of the main bus or of the unregulated bus (in case of

architecture 2) and capable of providing the required amount of power. In this way the input-output quantities selection is already accomplished.

DUAL HYBRID CONVERTER CHARACTERISTICS						
Part number	Vin	Vripple	W	Area	Weight	EMI
SVRHF2800D	18-40V	180mV	15W	$10.6cm^2$	28g	no
SVSA2800D	15-50V	50mV	5W	$7.5cm^2$	15g	no
3809	18-50V	125mV	18W	$10.5cm^2$	35g	yes
3809A	16-50V	50mV	2W	$5cm^2$	18g	yes

Table 4.4: Dual output Hybrid converter.

Before proceeding with the analysis of dual converter, is crucial to point out that the dual converter can be used for two main different situations:

- **Generate ±5V:** +5V - 1W for SSPA and -5V - 50mW for SSPA
- **Generate ±5V, +4V and +3V:** +5V - 1.9W for SSPA and LNA and -5V - 50mW for SSPA

In fact, since +4V and +3V output voltages carries low power, they can be derived from +5V with LDO. In this way, the number of hybrids and/or custom converters is reduced, lowering area and cost.

In the process of analyzing datasheet of each converter, a specification about the dual output power of the dual output converter was noticed: for each converter present in Table 4.4, the power provided at the two different lines shall not exceed the 10% of difference between them. For better clarification, if one line provides 10W, the other line cannot provide a power lower than 1W. If this condition is not controlled and verified during the operation mode, the center tap of the dual output converter move and is not able to provide the correct dual output voltage [14].
This condition is not verified in either case. In fact, for the situation with the lowest difference in power, which is +5V - 1W and -5V - 50mW, the difference between them is lower than 10% leading to a heavily unbalanced dual output converter and with a variation of the output voltage which is too large for this applications. With this information, the hybrid dual output converter is discarded.

4.5.2 Custom Solution for Dual Output Converters

For what concern the custom dual output converter the design becomes much more complex than a single output converter. Several characteristics start to play an important role in dual output. The main one is the cross regulation between the two different output lines. Cross regulation is the influence of one of the power lines on the other line. For example, the voltage of an output line affects the other line voltage causing high noise, high output instability and difficult design. Moreover, if one component of one output circuit fails, the other output circuit is compromised.

4.5.3 Results of Dual Output Converters

Nonetheless, dual output custom converter is not a reasonable solution: it requires a lot of effort in the design and even more in the test phase due to cross regulation which is difficult to predict and control. Despite the challenge in design a dual output Fly-back, the reason why the custom solution is not considered is because of the low power that such converter has to provide: it has no meaning of using a custom dual output isolated converter for generating just 1W or 2W overall. Not only the power that shall be provided is extremely low and the efficiency will easily degrade, but also the cost is too high for this application.
A better solution could be represented by Point of Load and LDO again. These components are perfect for carrying low amount of power keeping a highly output voltage stability. They do not require complex design and the cost is lower with respect to a custom dual output Fly-back. With these considerations, no dual output converter is used neither for architecture 1 nor for architecture 2.

4.6 Selection of Fly-back with Three Output Voltages

This converter represents the entire architecture 3. This architecture is not just composed by the three output Fly-back converter, but there are at least two LDO or Point of Load. These are necessary since it is required to have 6 output voltages, and in the process of SDR development some other output

voltages could be added. The ideal topology represents a three output Fly-back with +8V, +6V and +5V and three Point of Load or LDO that generates the +4V, +3V and -5V.

4.6.1 Hybrid Solution for Fly-back with Three Output Voltages

Selection of Hybrid Converters Based on Electrical Quantities

The search for a three output rah-hard hybrid converter which respects the requirements on output power and output voltages was extremely difficult. No components were found for three main reasons:

- **Low maximum power:** hybrid converters that were found had a maximum power much less than 50W, like for example DVTR2800T which is capable of providing 30W. Putting two parallel converters, for providing 60W of power has no meaning since they will occupy a lot of areas and they are too expensive;
- **Output reference voltage:** no converter in the market is designed to provide the output reference voltage defined previously. In fact, most of them provide a voltage that is too high, like +15V or +12V. This means that LDO and/or Point Of Load are necessary also for +6V and +8V. Since power carried by these two voltages is high and that the dropout voltage of the LDO will be higher, the power dissipation of such devices will increase a lot, leading to a low efficiency PSM;
- **Dual output voltage:** even for those converters which seem to be interesting for the max power available, like the 40W 5031 from MDI company, they implemented the dual output conversion for ±5V. As saw in section 5.5, dual output conversion cannot be implemented for this application due to a high mismatch between +5V and -5V.

4.6.2 Custom Solution for Three Output Fly-back Converters

Three output custom Fly-back required an even more complex design. As point out in the dual output converter, cross regulation becomes challenging to control and outputs will influence each other.

4.6.3 Results of Three Output Fly-back Converters

A possible solution could be to add small switching regulators, Point of Load and/or LDO at each output of the three output Fly-back, to better stabilize the output voltage and reducing the noise. In this way, this upgrade of architecture 3 looks like architecture 1. However, the three output Fly-back has no advantages with respect to the single output Fly-back of architecture 1, in fact it is bigger, and so heavier and occupies larger a area, it has a higher cost and it does not provide redundancy.
No reasonable solutions were found, neither with hybrid components nor with the custom design. These results lead to excluding architecture 3 for the possible implementation of the PSM.

4.7 Selection of Non Isolated Converters for Secondary Output Voltages

These converters can be implemented for architecture 1. They are non isolated, since in this topology isolation is introduce in the primary converter, and IC rad-hard solutions are also available.

4.7.1 Hybrid Solution for Non Isolated Converters for Secondary Output Voltages

Selection of Hybrid Converters based on electrical quantities

Table 4.5 report the main hybrid converter available in the market.

Hybrid converters have a wide output range voltage, but they occupied a lot in terms of weight and area. Without any further selection, the SVPL1200S part number is the best among these.

4.7.2 IC Solution for Non Isolated Converters for Secondary Output Voltages

In tables 4.6 and 4.7 are list the IC buck converter. In the first table, there are the rad-hard components, which were tested and proved for working in a high radiation emission environment. The second table reports space

HYBRID BUCK CONVERTER CHARACTERISTICS					
Part number	Vin	Vout	W	Area	Weight
SVPL1200S	13V	5 to 3.3V	15W	$7.5cm^2$	18g
3793	12V	5 to 3.3V	15W	$15.4cm^2$	50g
M3H2800S	28V	15 to 3.3V	40W	$35cm^2$	125g
LS2800S	16-50V	15 to 1.5V	30W	$28cm^2$	80g

Table 4.5: Buck Hybrid converters.

resistant component which are those components that have a flight heritage in other space missions. The difference between space grade and space resistant is that the firsts are built for being implemented for space missions, instead, the second ones are general COTS components which through radiation and temperature tests have been discovered to be resistant to space conditions and have already been implemented for other mission [2].

IC BUCK RAD-HARD CONVERTER CHARACTERISTICS				
Part number	Vin	Iout	W	Area
RHRPMPOL01	12 to 3V	5 to 3.3V	7A	$2cm^2$
RHFL4900XX	12 to 3V	9 to 1.2V	3A	$1cm^2$
RHFL6000A	12 to 1.5V	12 to 0.5V	2A	$0.7cm^2$
TPS7A4501	20 to 2.5V	20 to 1.2V	1.5A	$0.9cm^2$

Table 4.6: Buck IC Rad-Hard converter.

In the market there are several non-isolated IC space grade components and the RHFL4900 seems to be ideal: it has a higher output current and a variable output range from 9V to 1.2V that can cover all the desired output voltage and it is also very small.

IC COTS BUCK RAD-TOL CONVERTER CHARACTERISTICS				
Part number	Vin	Vout	Iout	Area
LT8610	42 to 3.4V	40 to 3.3V	2.5A	$0.23cm^2$
LT8613	42 to 3.4V	40 to 3.3V	6A	$0.21cm^2$
LT3082	40 to 1.2V	40 to 0.5V	200mA	$0.11cm^2$

Table 4.7: Buck IC COTS Rad-tolerant converter.

4.7.3 Results of Non Isolated Converter for Secondary Output Voltages

Taking a look at the last 3 converters of table 4.7 which corresponds to the COTS components, it can be noticed that they are better than the IC and hybrid space grade. Not only they can work with higher input voltage, ensuring damage from spike voltages, but can also provide whatever value of output voltage. Moreover, the 3 different components of Linear Technology cover different applications with a wide output current range. These are very interesting features for the future development of the SDR: if any additional voltage is required, with one of the LT components, the desired output reference and power can be easily generated.

From the physical parameter point of view, LT family requires additional components like inductors, capacitors and resistors to build up a well functioning converter which increases a lot the area. Instead, since it does not require any additional components, the RHFL4900A which is the IC space grade, is the smaller one and lighter. However, COTS components cost less than 10€each with respect to the hundreds of euros of the IC space grade RHFL4900A.
Custom solution for a buck converter is not analyzed since a general space grade power Mosfet, necessary for the switching action of a buck, is larger, heavier and expensive with respect the COTS components of LT, or IC RHFL which integrate all the devices necessary for the switching action and also for the control feedback loop, as well as some other features like burst mode, enable, output tracking, soft start, etc.
Wide electrical characteristics, modularity and low cost make the LT family the best choice for all output voltages for the secondary converters of

architecture 1.

4.8 Conclusions of the Converters Comparisons

In this chapter was described the first phase of the selection process. For each of the 5 different converters, a solution was found.
Figure 4.4 and Figure 4.5 reports the currents combinations of the different possible converters that can be implemented for architecture 1 and architecture 2 respectively, were indicated as custom, it means a custom isolated solution, and, instead, with IC COTS or with IC Space grade a non isolated solution.
Recall that architecture 3 is not reported since it was discarded during the selection process. (section 4.6). Moreover, no dual converter is taken into consideration (section 4.5).

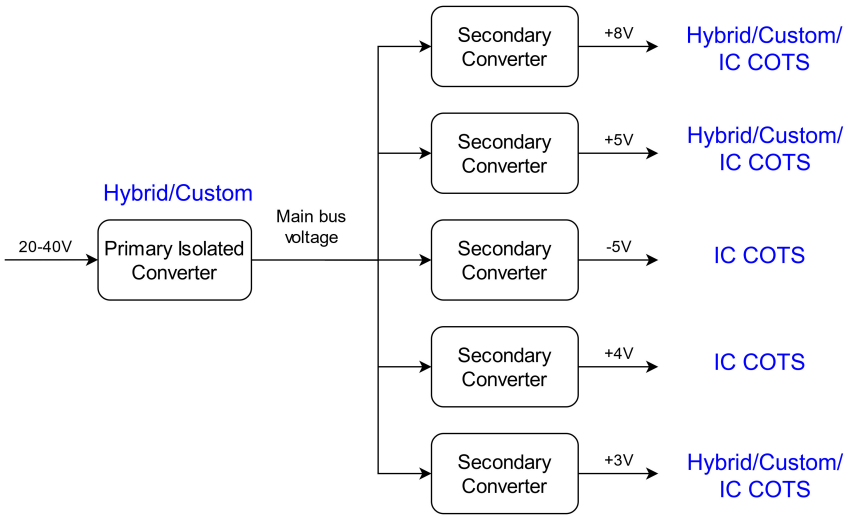

Figure 4.4: Combinations of converters for architecture 1.

In Figure 4.5 the question mark symbol indicates that for that converter the Hybrid and custom solution is not the best as point out in section 5.4.3.

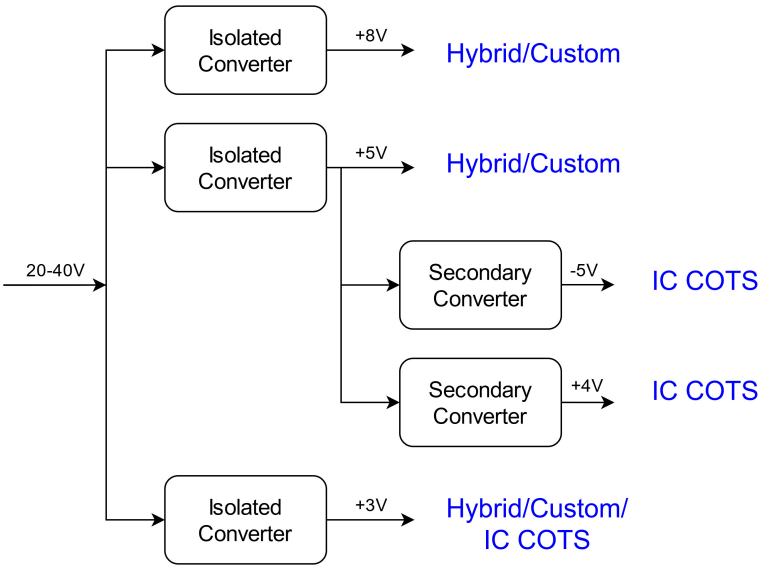

Figure 4.5: Combinations of converters for architecture 2.

In fact, an LDO can be introduced, which possibly, will be attached to +5V or +8V.

Chapter 5

Comparison process between architecture based on physical parameters

As described in the previous chapter, the selection process was based on choosing the architecture of the PSM starting from a low-level point of view, looking directly to the converters that can build up each architecture.
In the first phase, the comparison was based on selecting the plausible converter for the available architectures.
The second phase of the selection process, described in this chapter, will analyze which of the different combinations of each architecture is exceeding the physical limits of the board of the PSM that must be respected.
The goal of this chapter is to pass from the 54 combinations of architecture 1 and from the 27 of architecture 2 to few architectures that can be physically implemented above the board.

5.1 Selection based on physical parameters

The next phase of the selection process is focused on discerning some of these combinations subjecting them to the physical requirements.
According to the expected dimensions of the SDR, the PSM must be lighter than 250g and smaller than $96cm^2$. This selection process must be the first to be done since a lot of architectures that are the best in terms of efficiency, cost, noise and output stability are present, but if one of them is larger or

heavier than expected, it can not be used.

5.2 Selection Through Algorithm

First, the procedure starts using an algorithm that while is generating all the combinations of the architecture, changing the different types of converters, counts the values of area and weight of each converter per each combination. In the algorithm, all types of combinations are reported, from architecture 1 to architecture 2, since the combinations of architecture 2 have already been generated by the combinations of architecture 1, with the exception of the primary converter.

Figure 5.1 report the first results of the algorithm, the ones which are larger and heavier.
The ones indicated with H stands for Hybrid, C for custom and I for IC COTS.

The second combination is the one with the largest value, and even if it includes three hybrid converters, it respects the physical limits. This means that all the 54 combinations generated by the two architectures are physically good.

These two explanations give a reasonable idea of why all the combinations were physically good:

- at each selection of the converter done in chapter 4, a step was entirely devoted to eliminating those converters that were too heavier or larger;
- in these analysis some important characteristics are not considered, like the weight of the PCB, the voltage and current telemetry, the protection circuits, connectors, traces, etc., which will increase both the area and the weight of the PSM.

At this point, it becomes necessary to understand which of these combinations of architectures are in reality physically feasible.
During the layout phase of the PCB, some space must be left free for traces

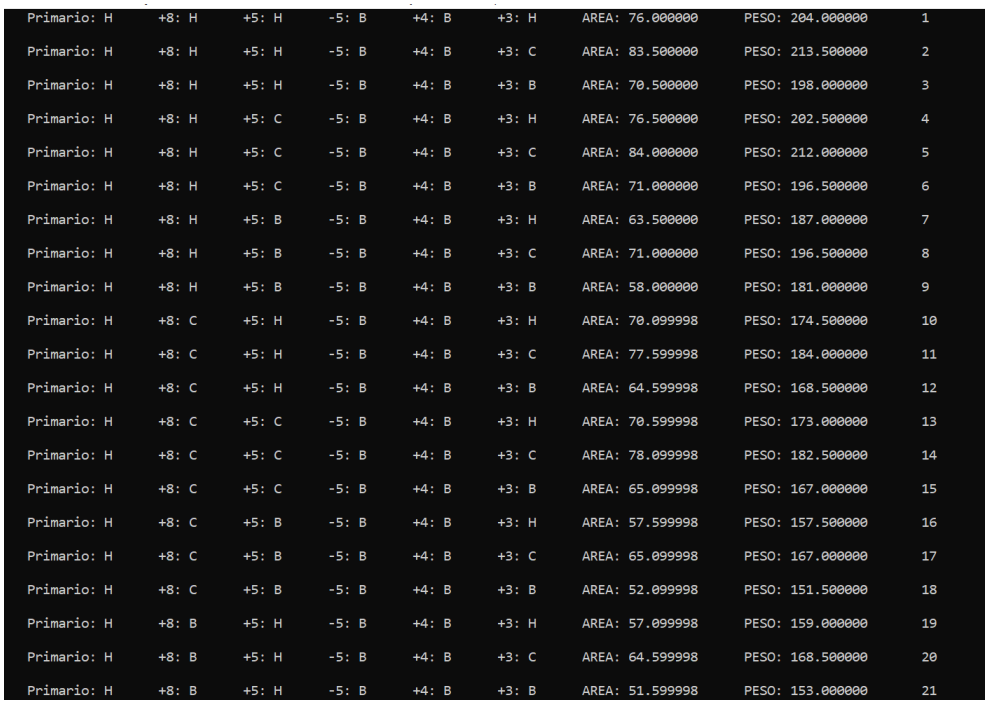

Figure 5.1: Combinations of architectures with area and weight.

and for introducing enough clearance between components. A good estimation for a correct routing is to not exceed 60% of the area of the components with respect to the area of both sides of the board.
Taking into account that, in Figure 5.1 the area values reported are not considering the connectors, the protection circuits and the V/I telemetry is better to not exceed the 40%. All the combinations of architectures that pass through the $70cm^2$ limits are not considered as plausible architectures for the PSM.

In this way two sub-groups of architectures are obtained: the ones that have more than 2 Hybrid converters in their structure, which make them less complex to be designed but expensive and too large to be implemented on a PC-104 form factor, and the ones with 2 or less Hybrid converters, which instead, includes Custom or IC design, but they are cheaper and physically implementable on the board.

5.3 Elimination of Combinations with New Data

With the new information obtained from the previous step, the number of architectures can be decreased: not only the ones which have a number of hybrid larger than 2 are discarded, but also those ones which exceed the $70cm^2$ of the occupied area.
Filtering the combinations according to these new data few combinations were left. +3V Hybrid converter as well as +3V custom solution is discarded for higher occupancy and also for the cost.

Therefore, just 3 converters could be a hybrid one: Primary converter, Secondary converter +8V and Secondary converter +5V and these are the combinations with no hybrid converter, one or a maximum two of them:

- No Hybrid converter
- Primary converter
- Secondary +8V converter
- Secondary +5V converter
- Primary and Secondary +8V converter
- Primary and Secondary +5V converter
- Secondary +8V and Secondary +5V converter

For architecture 2 the plausible combinations are more or less the same:

- No Hybrid converter
- Secondary +8V converter
- Secondary +5V converter
- Secondary +8V and Secondary +5V converter

5.4 Conclusion of the second phase

With these results, the second phase of the selection process ends. A lot of combinations are discarded and just the electrical and physical good ones are applicable. 7 different typologies are remained for architecture 1, with their own combinations, and 4 ones for architecture 2, with their own combinations.

Chapter 6

Comparison Process Based on Output Voltage Stability, Output Ripple and Noise Level

After these selection phases, the plausible combinations that can be implemented for the PSM are reduced and the remained ones are the electrically and physically good ones.
At this point, two main objectives must be accomplished in order to derive a single architecture that works for the PSM:

- Select the converter for +8V and +5V output reference voltage
- Select the architecture topology (with or without Primary converter)

The goal of this chapter is to find the solution to the previous objectives. This is accomplished by studying and analyzing the architectures from another point of view. With the help of the LT-spice software, the remained architectures are compared on:

- Noise level
- Output voltage stability
- Output ripple voltage

These specifications play an important role in the well-functioning of the SDR. Not only they allow the correct operation of the different modules and

of the different components, but it becomes important for suppressing noise for RF power amplifier‘s power supply lines. In fact, the switching noise generated by the Mosfet affects RF signal quality, and in such applications, where the lock at the carrier frequency happens at considerable low power, a small fraction of noise influences the quality of the data that are sent and received.

6.1 Definition of the Converter Models for Noise Analysis

The aim for this last selection phase is to find which architectures gives at the output the lowest amount of ripple and the higher output stability.
For what concern noise suppression, since no requirements has yet been enforced on noise level, in this paragraph, a short discussion about the different possibilities for implementing noise suppression is reported.

Comparative noise analysis needs models of the converters to be tested and compared through LT-spice simulation software. Since hybrid converters do not have their own model on LT-spice, a custom design of a Fly-back is considered for modeling both a hybrid converter and a custom itself. A single custom converter is designed both for Primary, Secondary +8V and Secondary +5V converter. IC COTS models were already present in the LT-spice software libraries.
For what concern secondary converters, higher performance IC COTS components were chosen due to two reasons:

- Power capabilities must be lower 65% than the nominal power rating of the components, according to ECSS derating standards [1].
- Efficiency, in general, decreased when the operating point is close to the max delivered power.

For example, +8V output voltage can be generated by LT8610, which has a maximum output current of 2.5A since 16W are required. Instead, LT8613 is chosen which can provide up to 6A at the output. In this way, by selecting a device with higher power capabilities the converter will work at lower power with respect to the max available, improving, in most cases, the efficiency.

The IC COTS converters for the relative output voltages are:

- +8V - LT8613 - 6A @500kHz
- +5V - LT8613 - 6A @500kHz
- -5V - LT3082 - 200mA
- +4V - LT8610 - 2.5A @700kHz
- +3V - LT3082 - 200mA

At the moment, the operating frequency of each of them is set in order to have the highest value of efficiency. It can be easily increased or decreased later by modifying resistors.
LT3082 is a low dropout linear voltage regulator, therefore no switching frequency is defined for this component.

6.2 Noise definition

To tests the converters as a function of noise is mandatory to introduce which kind of noise is present in an electronic board and how to represent it in the LT-spice environment.

In a generic system there are two kind of noise:

- noise generated by the system: in this case could be the noise generated by the switching action of the converter
- noise introduced into the system under test

In the first case, the noise generated by the system must be controlled and dumped otherwise any system or subsystem that is attached to it can run into interference and/or malfunctioning. At the same time, the noise cannot be completely removed from the device and so any system which is connected to it must be able to work properly.
In order to set a common standards, the ECSS developed a set of user-friendly standards based on Electromagnetic compatibility. The ECSS-E-ST-20-07C standard report the mask for the Conducted Emission and Conducted

Susceptibility that any system and subsystem shall respect [7].
Conducted Emission mask, in Figure 6.1 represents the amount of noise, classified in terms of max rms voltage at a different frequency, that a generic system and sub-system shall not exceed evaluated at its outputs. During a Conducted Emission test, if the amount of noise overcomes the mask limit means that this system provides an amount of noise which is too high and can compromise the nominal operation of the systems which are attached to it.

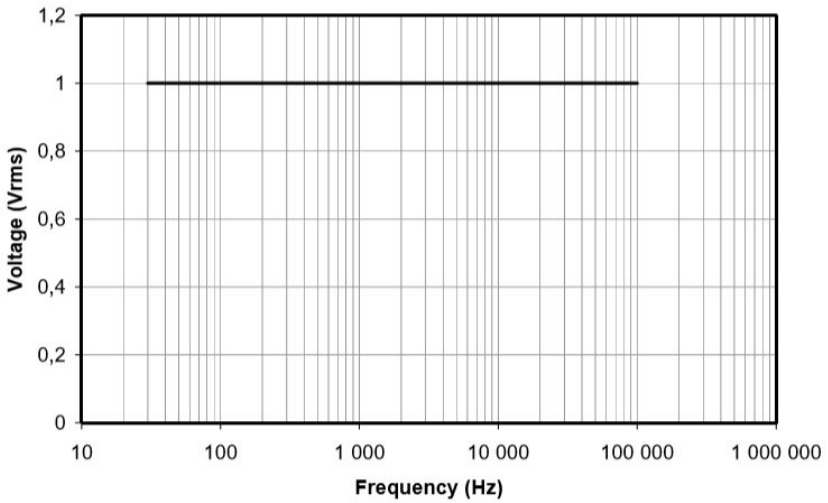

Figure 6.1: Conductive Emission mask.

Conducted Susceptibility are those noises that are generated by an external device introduced into the system by I/O or power cables. As well as Conducted Emission, it can be modeled via voltage and/or current source and it is used to test how a system reacts to these interferences. Figure 4.24 shows the Conductive Susceptibility mask.

For both the Conductive noises, there are two different types of them: Common mode and Differential mode. As the name suggests, the differences are based on how the tests are run: in common mode if just one power lead is tested, differential mode if both power leads are tested.

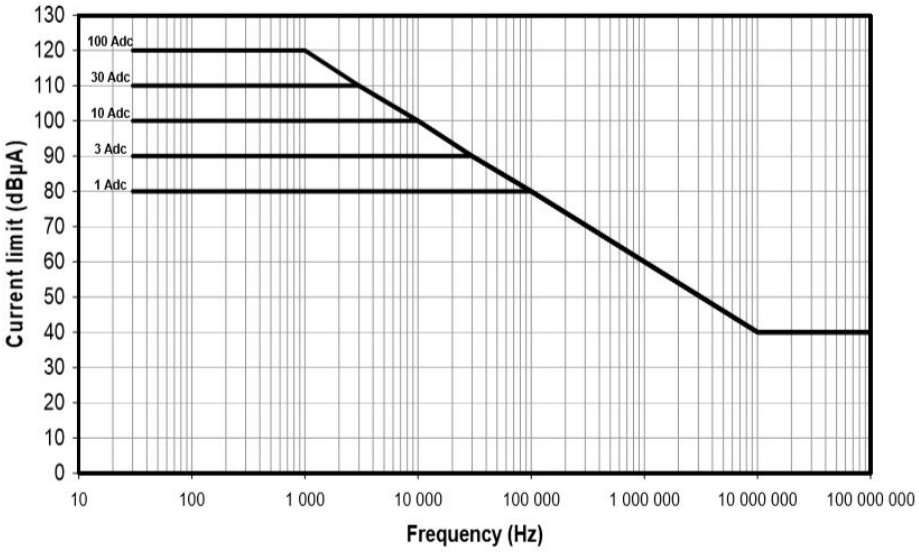

Figure 6.2: Conductive Susceptibility mask.

6.3 EMI and Output Filters

EMI filters and Output filters are passive filters, generally of the second order, usually made by passive components like inductors and capacitors, which become very commons in the electronic world.

6.3.1 EMI filters and noise coming from the input

EMI filters are placed at the power entry point of a device. They are necessary for reducing and protecting the device from EMI noise generated by the device itself as well as external EMI [15].
This type of filter is mandatory in a power board, otherwise, the noise generated by the DC-DC converters may return back from the input port and if it is higher than the mask, it may interfere with other subsystems.
This filter is necessary in order to reduce the Conductive Emission of the PSM at the input port.

6.3.2 Output Filters and sanity check for noise coming from the output

Output filters instead are placed at the output ports. These filters are useful to reduce the switching noise of a DC-DC converter, providing a clean spectrum and reduced output ripple. These features are crucial when the power line is feeding an RF device, which is extremely sensitive to noise and can affect the quality of the transmission of a signal.

6.3.3 Different Configuration of the Filters

Different configurations based on the number of filters and where they are placed could be analyzed for figuring out which is the best configuration that minimizes the noise received and emitted. These arrangements work both for architecture 1 and 2:

- One input filter and no Output filter
- Multiple input filter and no Output filter
- One input filter and Output filter for each outputs
- Multiple input filter and Output filter for each outputs

Figure 6.3 reports the last two structure, where in red are highlighted the input filter and light blue the output ones.

These configurations have differences only for the noise coming from the output. In fact, if the noise is coming from the input it will always encounter one input filter, independently of the configuration.
In order to test how the converters react when the noise is coming from the output, the devices under test will be of two kinds: at the output of the first noise is injected, modeled as series of voltage sources based on the Conductive Susceptibility mask of Figure 6.2; instead at the other one, the output voltage value is controlled to test how the system responds.

The analyses are carried on not only for Fly-back but also for IC COTS LT8613 and LT3082.

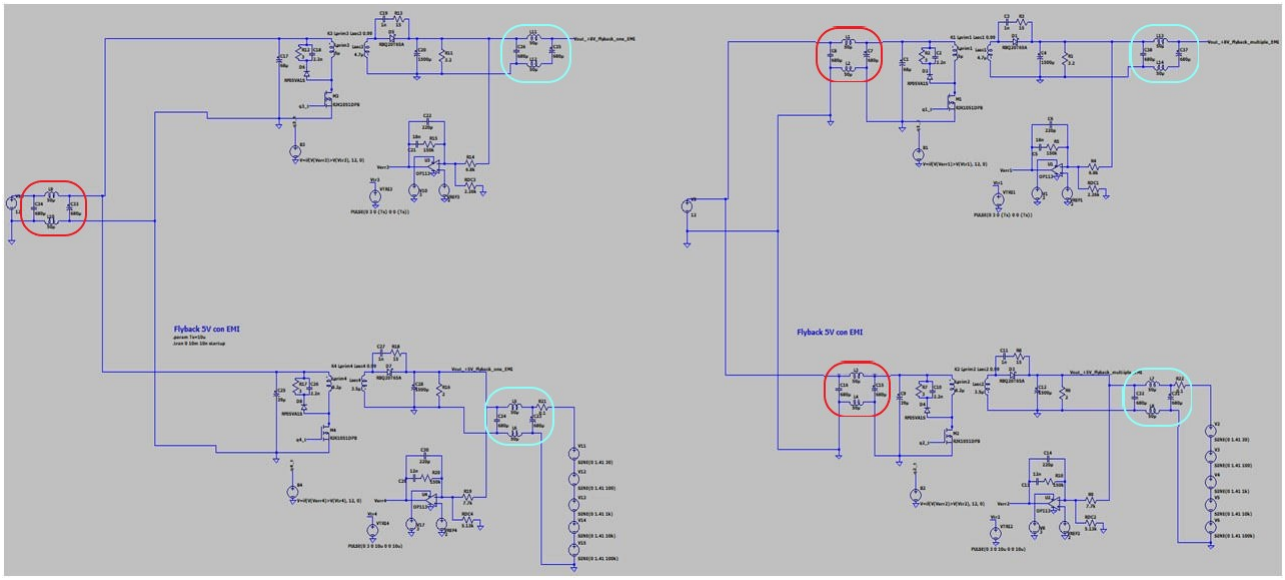

Figure 6.3: configurations of the filters.

Figure 6.4, Figure 6.5 and Figure 6.6 shows the results for Fly-back, LT8613 and LT3082 respectively at steady state.

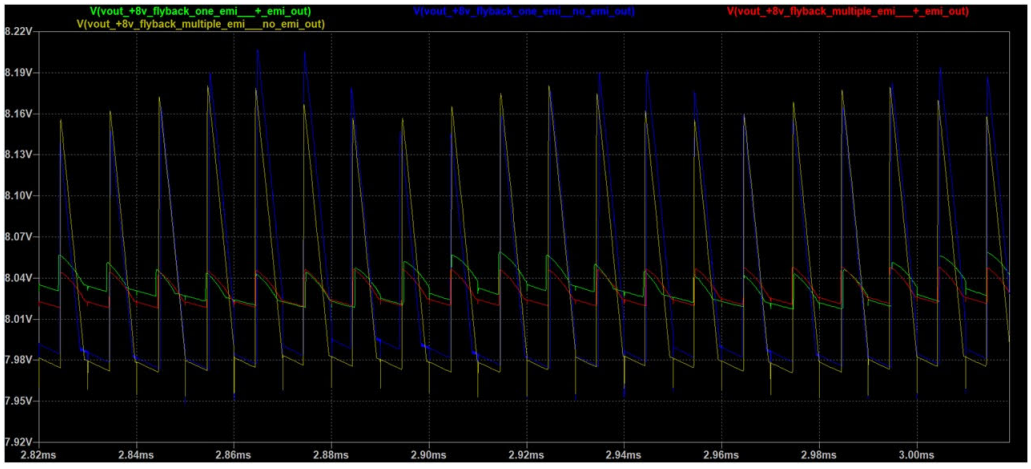

Figure 6.4: Output of Fly-back converter for different Filter topology.

Starting from the Fly-back simulation, it can be noticed that the topology

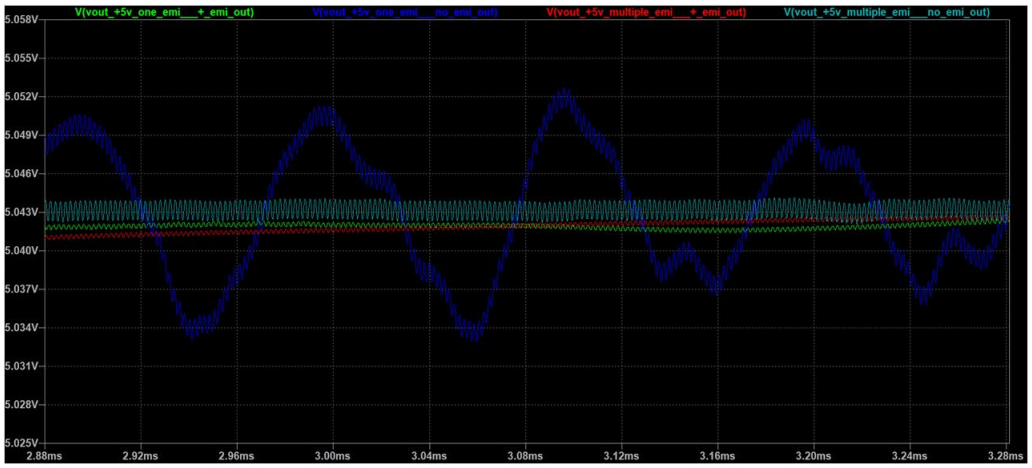

Figure 6.5: Output of LT8613 converter for different Filter topology.

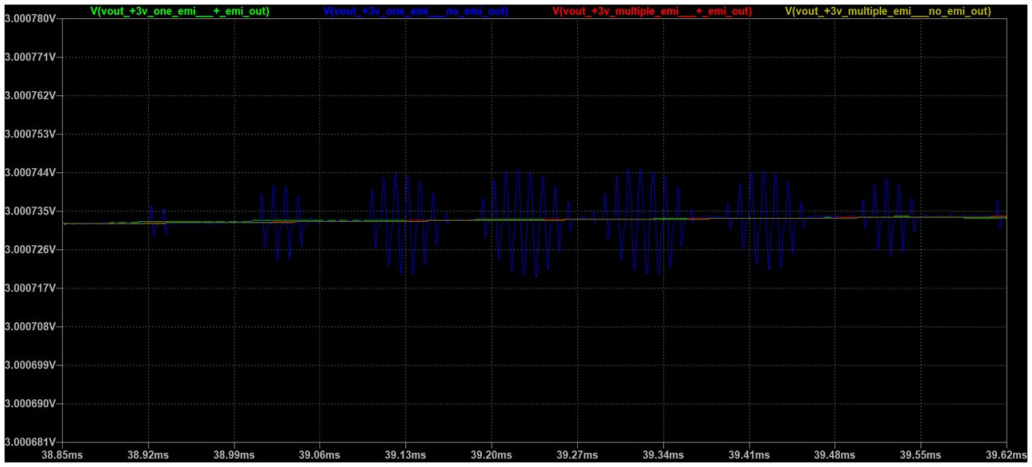

Figure 6.6: Output of LT3082 converter for different Filter topology.

with the lower ripple and higher stability are the ones with the Output filters, independently of the EMI input filter type. Same conclusions are valid for the Buck LT8613/10 converter where however the MULTIPLE EMI IN and NO EMI OUT filter topology give a practical result. No countable differences, instead, are observable for the LT3082 linear regulator.
What really matters is the presence of the Output Filter.
Through these conclusions, the final topology of the filters is the ONE EMI Input Filter and Output filters due to lower area, weight and cost that it

requires.

These informations are important both for architecture 1 and 2:

- for architecture 1 this means that no other filters are necessary in addition to the single EMI input filter placed before the Primary converter and the Output filters for each reference voltages. These analyses show indeed that an intermediate filter situated between primary converter and secondary ones is not improving the well functioning of the system.
- for architecture 2, instead, this means that is sufficient to build just one EMI filter since more input filter does not improve the overall system.

Figure 6.7 and Figure 6.8 displays the actual topology with architecture 1 and 2 respectively.

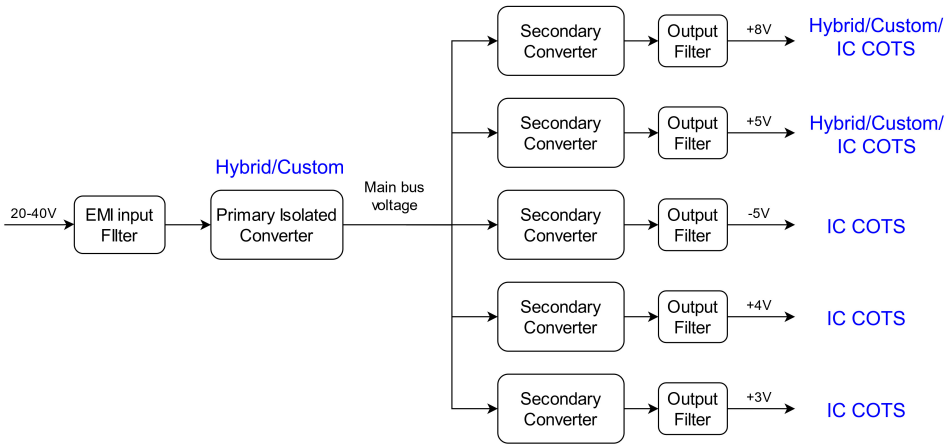

Figure 6.7: First architecture with Filter topology.

6.4 Selection of +8V and +5V Converter

Once that the Filter topology is defined, the comparative noise analysis between the remained combinations of architectures can continue.
The goal of this section is focused on selecting the convenient secondary

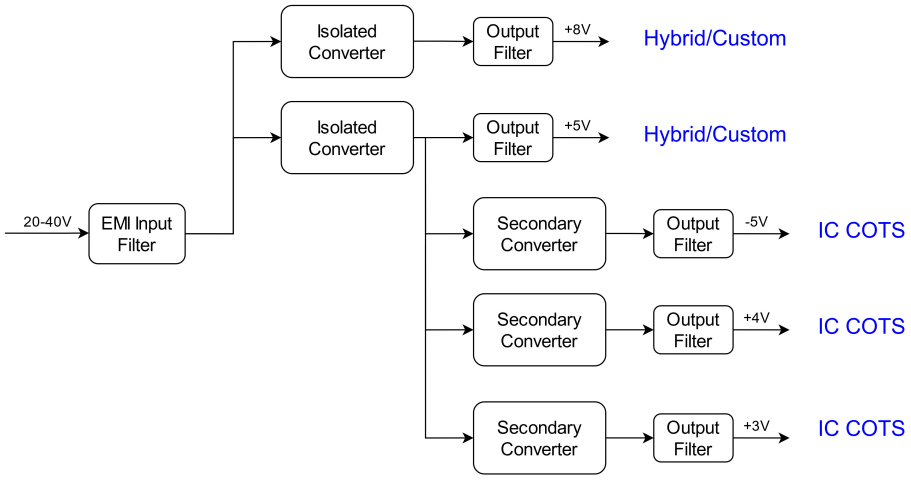

Figure 6.8: Second architecture with Filter topology.

converters for +8V and +5V. In chapter 4 a comparison between Hybrid, Custom and IC converters was done, highlighting the differences on area, weight, efficiency, cost and complexity. The comparison is carrying on emphasizing the noise spectrum purity, voltage stability and output ripple.

The Fly-back custom converter and the LT8613/LT3082 are compared by simulating them in two different methods:

- Insert noise at the input from main bus and sensing of +8V output
- Insert noise at +5V output and sensing of +8V output

The simulation could be done also by reversing the two converters.
Recall that the Hybrid converter is simulated in LT-spice with the Custom one.

Figure 6.9 shows both the model circuit of Fly-back and Buck LT8613 for the first mode simulation.

Through Figure 6.10 and Figure 6.11 it can be notice that IC COTS LT8613 converter generate an output voltage which is more stable, constant

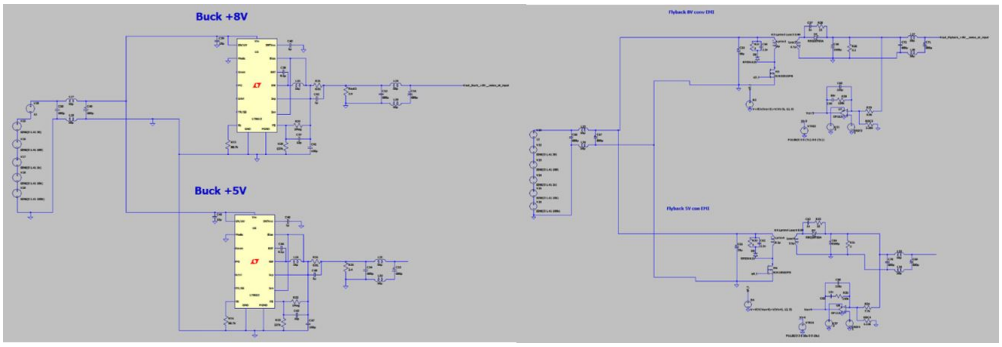

Figure 6.9: LT8613 and Custom Fly-back converter comparison with noise at the input.

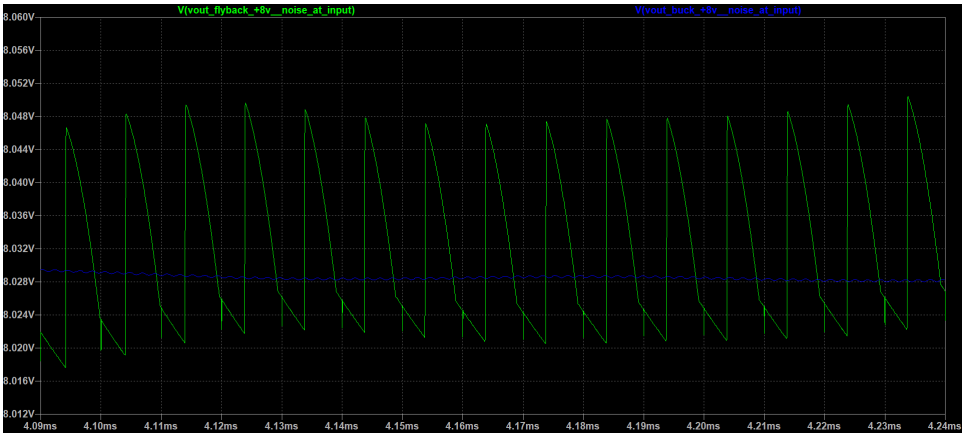

Figure 6.10: LT8613 and Custom Fly-back +8V output comparison with noise at the input at steady state.

and with lower ripple than the custom one. Even if the hybrid converter output stability and ripple can not be test through simulation, from datasheet can be seen that it is still worse than the LT8613.

Table 6.1 provide a recap of the comparison between +8V and +5V converter.

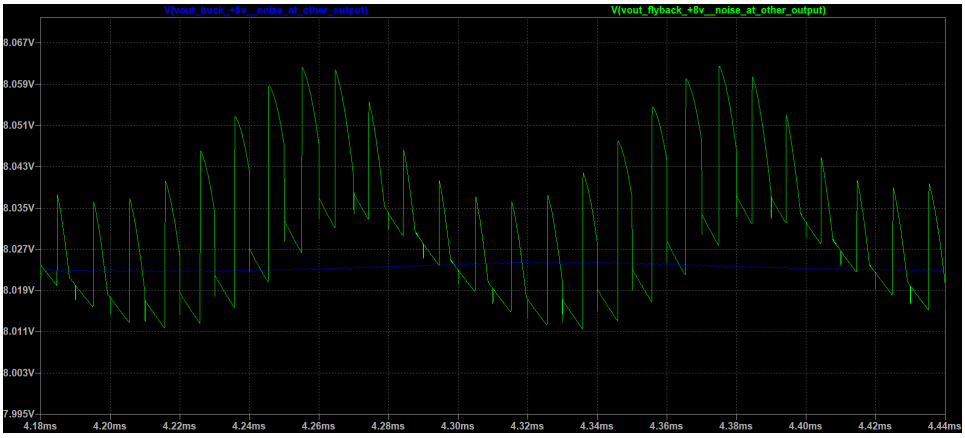

Figure 6.11: LT8613 and Custom Fly-back +8V output comparison with noise at the output +5V converter at steady state.

Parameter	**Custom Fly-back**	**Hybrid SVRFL**	**Buck LT8613**
Area	$15cm^2$	$20.9cm^2$	$2.5cm^2$
Weight	25.5g	55g	10g
Ripple	200mV	50mV	<10mV
Cost	2.6k€	8k€	50€
Efficiency	$\sim 75\%$	$\sim 85\%$	$\sim 90\%$
Complexity	High	Low	Medium
Out stability	Medium	Medium	High

Table 6.1: Comparison between Hybrid, Custom and Buck converter for +8V and +5V output voltages.

6.5 Conclusion of the Noise Analysis and Definition of the Final Architecture

With the information obtained by the comparative noise analysis of the previous section, it was proved that also for output stability and ripple neither the Custom Fly-back nor the Hybrid one are suitable for fulfilling the role of the secondary converters that generate the output references voltages of

+8V and +5V. LT8613 is the solution which is most advantageous for these output voltages.

For architecture 1 this implies that all the output voltages are generated by IC COTS converters of the LT family. The secondary converters, in this way, will be lighter, cheaper, more efficient and provides a better output voltage of any other topology discussed in this thesis work. The primary converter instead can be a Custom solution, since no important requirements are forced on the output ripple of the primary converter. Hybrid solution is considered only if a fast implementation is needed.

For architecture 2, since +8V and +5V converter must be isolated, one from Custom and Hybrid alternatives must be select. Looking again on Table 6.1 can be noticed that Custom solution is better, even if it may provide a higher output ripple and it require a lot of effort for designing it.

At this point, all the necessary analyses are available for choosing one of the two architecture. At the beginning of the comparative analysis, architecture 2 was the one that presented the lowest number of converters, one for each output voltage. During the selection process, the types of converter have changed, and 3 over 5 have become a non isolated one, with the need of being attached at the output of an isolated one.
Even if the number of converters of architecture 2 remained the same, architecture 1 lower a lot the area and weight of the secondary converters with the IC COTS solution.
At the end the architecture 2 has 2 Custom converter (Hybrid if necessary), where instead, architecture 1 presents just one Custom, lowering in this way the area, weight and cost dedicated for implement it.
Moreover, architecture 1 has a better behavior in terms of noise and voltage stability of the output references: in fact, due to the presence of the primary converter, the noise which is coming from the unregulated input bus, is filtered by the EMI filter and by the primary converter itself, providing, in this way, a stable main bus voltage to the secondary converters.
In architecture 2, the noise, once has passed the EMI filter, is going immediately to the isolated converter, which directly feeds the external subsystem.
Lastly, if redundancy want to be added as a feature of the PSM, is much easier to duplicate the converters of architecture 1, which occupy less area, than the ones of architecture 2.

Figure 6.12 shows the final architecture of the PSM, with the type of converters and filter topology.

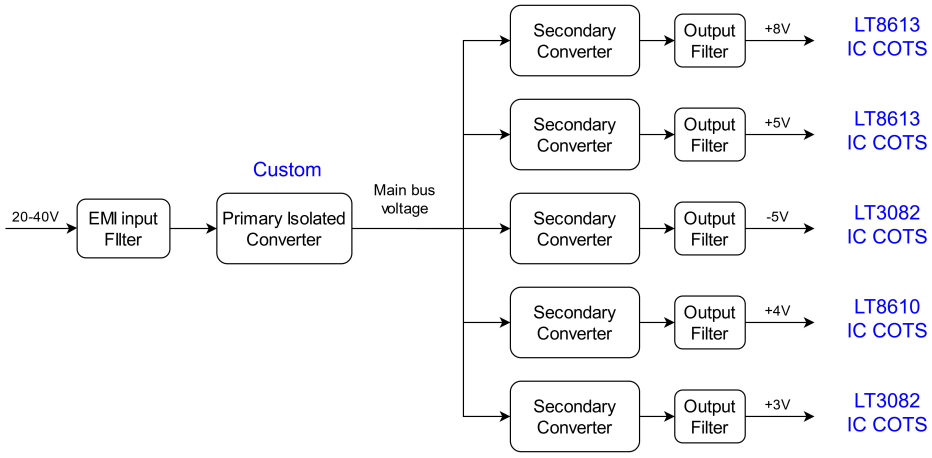

Figure 6.12: Final architecture of the PSM.

Chapter 7

Primary Converter Selection

Once that the architecture is selected, after the comparison process previously described, the only converter that has yet to be defined is the primary one. A custom converter solution was found to be the most interesting for this role. Hybrid one is still considered just in case other features are requested, like fast development, mounting and testing.

7.1 Definition of the Plausible Converters Topology

Fly-back A list of the parameters, derived from the electrical and physical requirements, that are necessary for choosing the best topology are reported:

- 50W max power
- 20-40V Input voltage range
- 10-40V Output voltage
- Isolation
- Low number of components
- Low area

Isolation is the most important parameter that must be ensured on the type of topology, otherwise noise, instantaneous peak voltage and current can interfere or damage the PSM unit and its components.
The most common isolated converter are:

- Fly-back
- Forward
- Push-Pull
- Half-Bridge
- Full-Bridge

Each of them has different features and are suited for particular cases for limiting the current or the voltage stresses. Most importantly they differ for what concerns the power range in which they can be implemented. Only the Fly-back converter is the most suitable for power lower than 100W. Moreover, Fly-back converter is also the one which need less number of components for being implemented, using just one magnetic core or better a coupled inductor and one switch. Fly-back can be seen as the isolated converter of the Buck-Boost, and it is capable of both reducing and increasing the output voltage with respect to the input. This is a good feature since this gives the possibility of tuning the output voltage according to requirements and/or problems.
Recall that the main bus voltage, which is the one generated by the primary converter can not exceed the 40V since IC COTS of LT can withstand maximum this voltage at the input.
Fly-back converter was chosen among the previous ones.

DC Transformer Another topology is actually available and it is called "DC Transformer" [16]. The configuration is equivalent to a Push-Pull converter. The difference between them relay on the fact that the DC Transformer has not a variable duty cycle for the two switches, but instead it is fixed on 50% and the two waveforms which drives the switches are shifted by 180°. In a real implementation the duty cycle is less than 50%, in order to

avoid that both switches are on or off at the same time; 45% is, in general, a good margin for guarantee a correct operation.
The conversion factor introduced by a DC transformer, in order to reduce or increase the output voltage, is based on the turn ratio of the transformer according to the following formula which is fixed.

$$\frac{V_{out}}{V_{in}} = \frac{N_s}{N_p} \tag{7.1}$$

Figure 7.1 shows a schematic of a DC transformer.

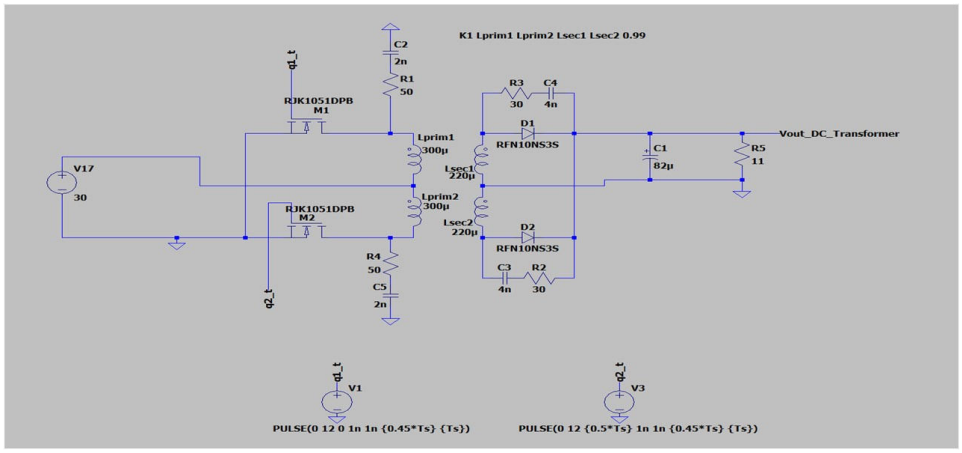

Figure 7.1: DC Transformer.

This means that the output voltage will not be constant since it is not tuned by a feedback loop and a PWM controller, but it will change according to the input one. Another consequence of this is that whatever noise, instantaneous peak current or voltage, voltage drops, etc, are not "filtered" by the DC transformer, but they passed through it being only converted according to the turns ratio.

7.2 Comparison Between Primary Converter Topology

Fly-back and DC Transformer can both be implemented in the architecture of the PSM. Moreover, the Fly-back converter can be implemented in two

different modes: CCM and DCM.

First, the Fly-back modes are compared, then the best between them is cross-checked with the DC Transformer.

7.2.1 Fly-back CCM and DCM Modes Comparison

In Continuous Conduction Mode (CCM) the current flowing through the coupled inductor is always higher than zero. In Discontinuous Conduction Mode (DCM), instead, the current can reach and stay at zero for a certain amount of time. In Table 7.2 are reported the main differences between the two Conduction Mode:

Parameter	**CCM**	**DCM**
Lp	Higher	Lower
Transformer size	Higher	Lower
Primary current	Lower	Higher
Secondary current	Lower	Higher
Losses	Lower	Higher
Control TF	Complex	Simpler
Closed loop Band	Lower	Higher
Stress on switch	Lower	Higher
Stress on diode	Lower	Higher

Table 7.1: Comparison between CCM and DCM Fly-back.

The DCM mode presents a higher peak and rms currents through the coupled inductor. Even if it has a lower primary inductance, and therefore a lower transformer, the stresses on the diode and on the switch are much higher, as well as the losses introduced by the magnetic core are significant than CCM. However, in CCM the control loop of the transfer function can become difficult to control if the voltage mode is used since a Right Half Plane Zero (RHPZ) is present at much lower frequencies which may lead to instability due to lower phase margin.

Fly-backs in CCM and DCM are compared in LT-spice. These converters were implemented with a rough design, which, however, was good enough for comparison purposes. The converters were designed for 50W, with an output voltage of 28V and the turn ratio equal to 1.
Figure 7.2 and Figure reports the output ripple and secondary current compared between DCM and CCM.

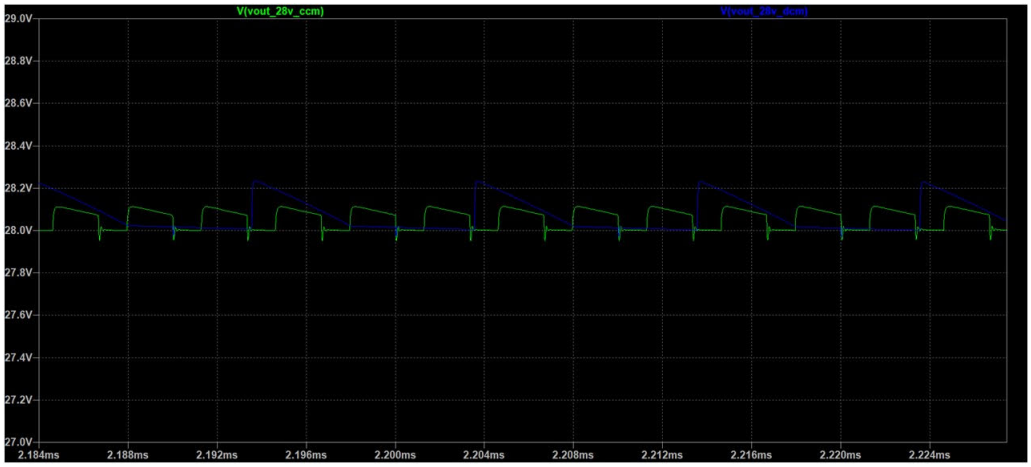

Figure 7.2: Output voltage for Fly-back in CCM and DCM.

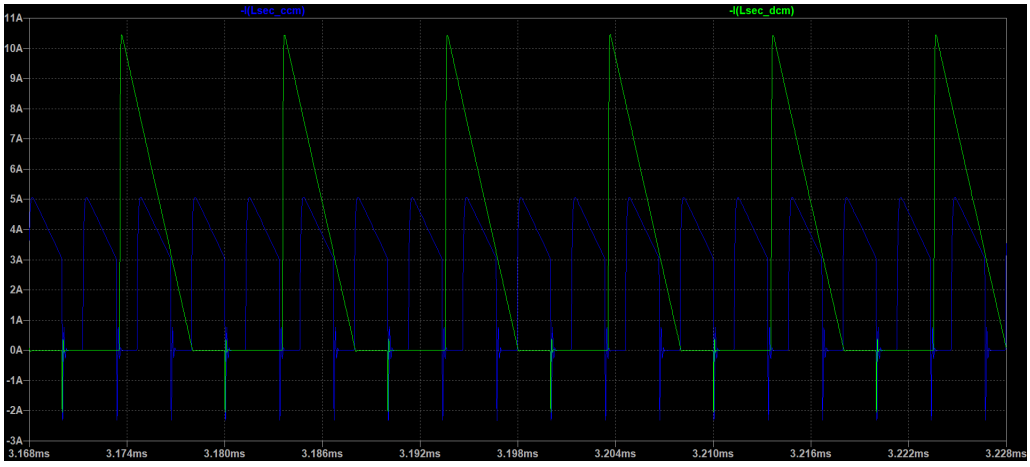

Figure 7.3: Secondary current for Fly-back in CCM and DCM.

The CCM mode is preferred for this application, since it reduces the

output ripple, giving a more stable main bus voltage to secondary converters. Moreover, the low current through the wingdings of the transformer will reduce the losses and avoid reaching higher temperature of the whole system.

7.2.2 Fly-back CCM Vs DC Transformer Comparison

The selection of the primary converter continues with the comparison between the CCM mode of the Fly-back and the DC Transformer. The two topologies are compared based on the previous parameters described in the CCM and DCM analysis. Table 7.2 report the main parameter compared between them.

Parameter	**Fly-back CCM**	**DC Transformer**
Lp	Lower	Higher
Transformer size	Lighter	Bigger
Primary current	Higher	Lower
Secondary current	Higher	Lower
Losses	Lower	Higher
Control TF	Complex	Simpler if none
Stress on switch	Higher	Lower
Stress on diode	Higher	Lower
Number of components	Higher	Lower
Output noise	Lower	Higher
Output ripple	Lower	Higher

Table 7.2: Comparison between CCM Fly-back and DC transformer.

The DC Transformer will have a bulkier magnetic core with respect to Fly-back. This depends on the fact that the DC Transformer implements a Transformer instead of a coupled inductor, which in general has a higher primary inductance. However, the DC Transformer will have lower currents through the windings, reducing the stresses on switches and diodes. Even if it uses two switches and two diodes the number of components are lower

than the Fly-back converter, since in the Fly-back must be considered also the feedback components.
No investigation has been done about the cost of the DC Transformer, but it is reasonable to expect that it will have a higher cost with respect to Fly-back since switches are expensive than a Feedback loop control.
Another aspect has to be analyzed about cost and lead time of the components: since DC Transformer requires a proper turns ratio based on the input-output conversion factor of the application, it is clear that the Transformer must be designed ad hoc. In fact, is very complex to find a rad-hard or rad-tolerant transformer that has a specific turn ratio which is also able to handle a specific current through its windings.
In general, this kind of ad hoc devices requires a lot of time in order to be designed, built and tested. Moreover, the cost of these solutions is important especially if the number of devices that can be built is not known yet. In fact, these types of custom solutions are recommended if the number of components needed is defined and only if this number is really high, in order to compensate the cost of the design, assembly and test phase.

In the end, Fly-back CCM and DC transformer are tested based on the noise level at the output. Both configurations are tested injecting the maximum Conductive Susceptibility noise, modeled with voltage sources, at the input, considering also the EMI input filter.
Figure 7.4 displays the steady state output voltage of the Fly-back CCM and DC Transformer, with the noise at the input. It is clearly visible that Fly-back has a more stable behaviour, lower ripple since it is capable also of filtering part of the incoming interference.

The DC Transformer solution is not the best at the moment:it is expensive since it is not known how many PSM will be developed yet and it will require a higher time in order to get the custom transformer and to test it. Moreover, the output main bus voltage that it is generated is not free of noise and peak currents/voltages, which may be a create trouble for what concerns the feeding of RF lines.

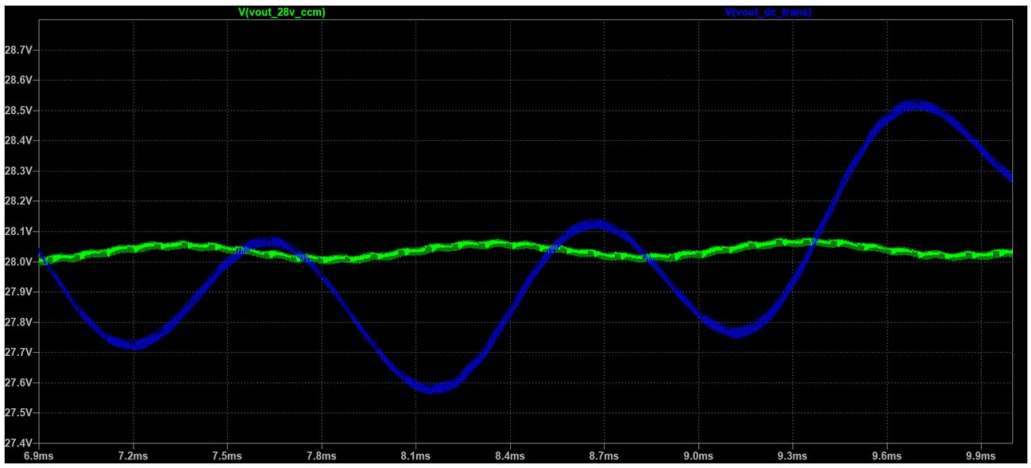

Figure 7.4: Fly-back CCM and DC Transformer .

7.3 Selection Process Conclusions

Fly-back in CCM is the last converter of the architecture that is selected, ending the last phase of the selection process started in chapter 4.
It is important to highlight that the PSM will be designed based on the structure of this final architecture, taking into account that some minor modifications can be introduced on converter typology, filters placement, increase or decrease of the amount of power, etc. Argotec's SDR is still under development: whatever new information concerning the project can change the structure of the PSM designed so far.
In fact, also the DC Transformer could be actually implemented in the next future if any problems arise with the Fly-back converter. Indeed, during the selection process, the focus has been moved on different alternatives and possibilities, studying and analyzing the contribution of any kind of architecture, filter placement, converters features and problems which will be helpful for the future evolution of the PSM.

Chapter 8

Fly-back CCM Design

This chapter is devoted to the design of the Fly-back, exploiting the requirements which allow the operation in CCM mode, the problems related to dimension the components and finding the proper part number, and all the solutions introduced to resolve those problems.

8.1 Dimension of the main characteristics of the Fly-back in CCM

Output Voltage

The output voltage of the primary converter provides the input voltage to the IC COTS LT family. Since the maximum input voltage of the secondary converters is 40V and since they are just able to down converter, the range of the output voltage of the Fly-back is 10-40V.
Higher is the output voltage of the Fly-back lower is the current that is flowing into the coupled inductor. However, higher is the voltage that IC COTS converters are receiving, lower is their efficiency due to conversion losses.
A commonly used voltage in the electronic world of the space application is the 28V which could be a reasonable value for the output voltage of the Fly-back.

Conversion Factor and CCM Constraints

Once that the output voltage is defined, the design of the CCM Fly-back can continue. Equation 8.1 report the DC conversion factor between input-output voltage, where D is the duty cycle and N is the turn ratio.

$$\frac{V_{out}}{V_{in}} = \frac{D}{N * (1 - D)} \tag{8.1}$$

From it, it is possible to derive the maximum and minimum duty cycle according to the minimum and maximum input voltage respectively, which are useful in the next phase of the design.

$$D = \frac{N * (V_{out} + V_{diode})}{N * (V_{out} + V_{diode}) + V_{in}} \tag{8.2}$$

The equation which ensure to work in CCM is the 8.3:

$$L_{prim} > \frac{V_{out}^2 * (1 - D_{max})^2 * N^2}{2 * P_{out,min} * F_{swt}} \tag{8.3}$$

The only parameter which is not still defined is the minimum output power that Fly-back has to deliver. As described in chapter 3, the SDR has different mode of operation which depends if it is transmitting, receiving, or it is doing both of them.
Table 8.1 is reporting the output current Vs output voltage for the expected power modes of the radio.

Power	**Vout**	**Iout**
50W	28V	1.8A
25W	28V	0.9A
9W	28V	0.33A

Table 8.1: Output current Vs Power modes

Equation 8.3 shows that for low power operation of the SDR, Fly-back converter goes into DCM mode which must be avoided for decreasing the currents and losses.

Impose CCM Mode Operation

Three different solutions are available:

- Lp smaller at high frequency in CCM at 9W
- Bigger Lp at low frequency in CCM at 9W
- Lp smaller and variable fsw

Recall that ensuring CCM in the lower power mode operation, implies CCM mode also at higher power modes.
The problems regardless of these solutions are respectively:

- High fsw implies high dissipation of power, for switch and magnetic core
- Bigger Lp implies higher cost, area and weight
- Additional circuit is required for checking power mode which implies complexity

Tuning of the Main Parameters

The parameter that can be tuned in order to start the design and understand which from the previous listed solutions gives better performances than the others are the turns ratio N, the switching frequency Fsw and the primary inductance Lp.
Figure 8.1, 8.2, 8.3 and 8.4 reports the main characteristic of the Fly-back versus the turns ratio. These figures are useful in order to shows which are the pros and cons of working with lower or higher N. Even if the signals reported in those figures are evaluated according to the defined values of Vout, Dmax and Pout, the trend of these signals with respect to N is always the one shown in this figures.

The figures reported above clearly show that in order to minimize the stresses and reduce the power dissipation, the best value for the turn ratio is N=1, and the value of Lp is reduced.

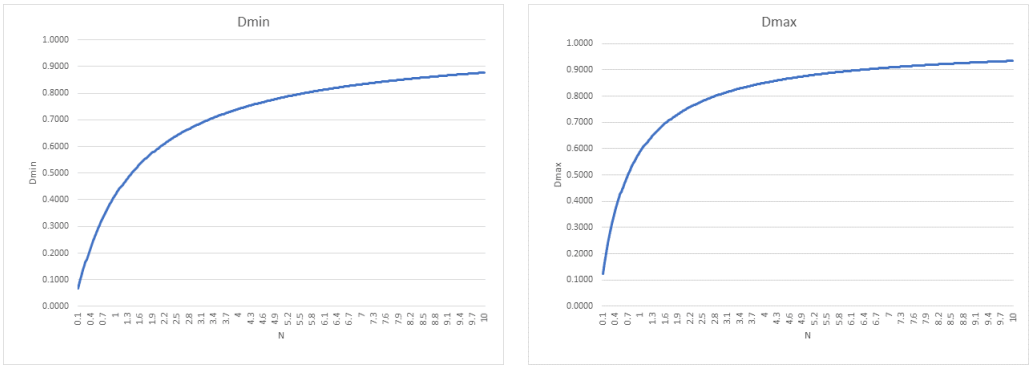

Figure 8.1: Minimum and Maximum Duty Cycle Vs Turn Ratio.

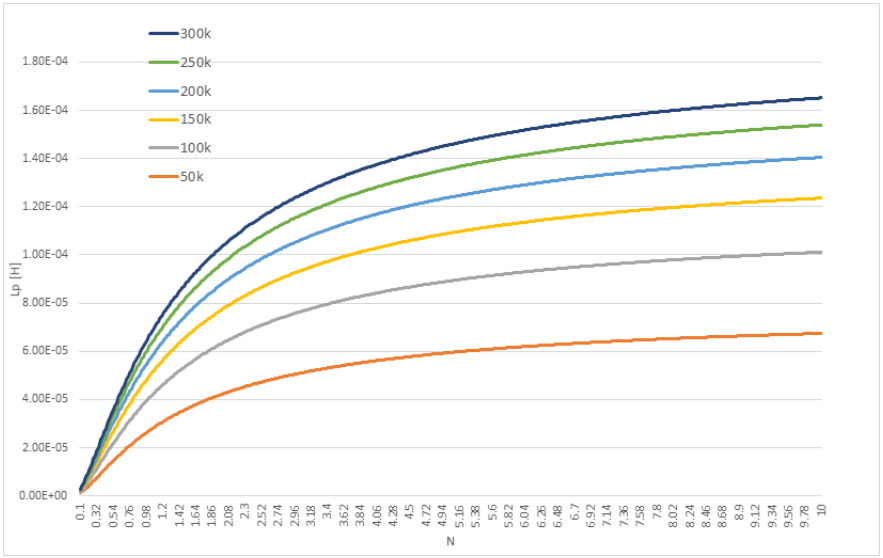

Figure 8.2: Primary Inductance value Vs Turn Ratio.

But still Lp and Fsw have to be defined. With the help of equation 8.3 it is possible to define which are the parameter for Lp and Fsw according to the two different solutions: smaller Lp at high Fsw, bigger Lp at low Fsw:

- Lp>25uH at 300KHz
- Lp>150uH at 50kHz

From the previous alternatives, the solution with lower Fsw seems to be the

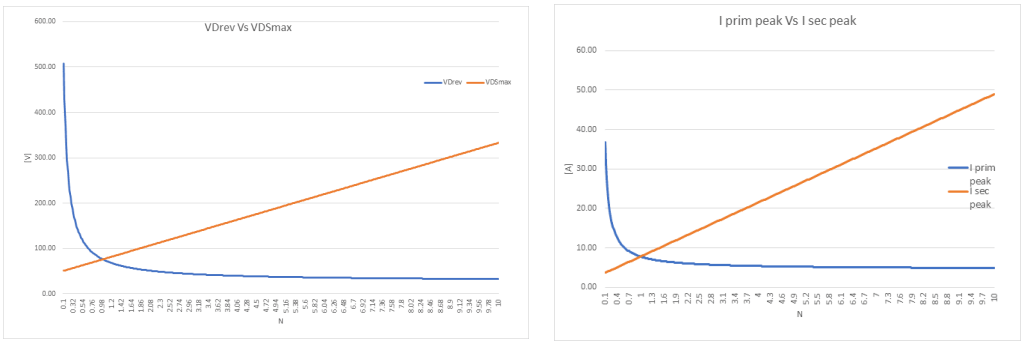

Figure 8.3: Diode and Drain-Source voltage, Primary and Secondary current Vs Turn Ratio.

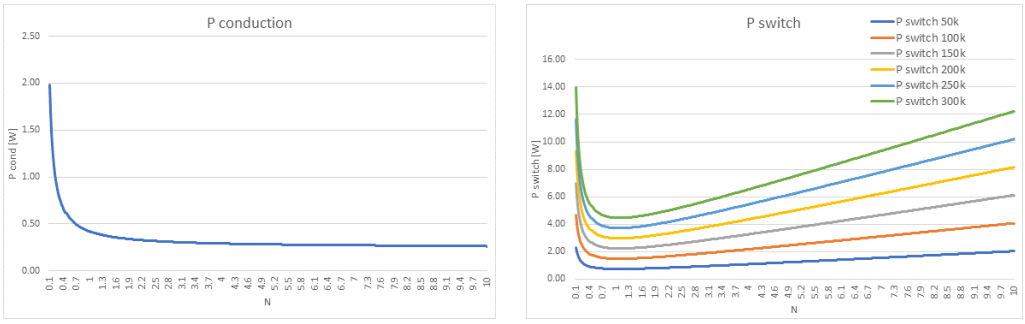

Figure 8.4: Conduction and Switching Losses Vs Turn Ratio.

best, since it reduces the power losses of the magnetic core and of the switch. However, Lp will be larger and the coupled inductor will be bigger.

Rad-Hard Coupled Inductor

In order to have a practical result and compared how bulky and heavy could be a 150uH coupled inductor with respect to a 25uH, a research of an rah-hard or rad-tolerant one is necessary.

The best coupled inductor found in the market is the 612PND of coilcraft [12]. Figure 8.5 displays the parameters of this component.

Has to be highlighted that the market for rad-hard coupled inductor to do note provides a lot of choices. In fact, is very common in these cases to

Part number[1]	Inductance[2] (µH)		DCR max[3] (Ohms)	SRF (MHz)[4] min	SRF (MHz)[4] typ	Coupling coefficient typ	Leakage L typ (µH)	Isat (A)[5] 10% drop	Isat (A)[5] 20% drop	Isat (A)[5] 30% drop	Irms (A) both windings[6]	Irms (A) one winding[7]
AE612PND472MSZ	4.7	±20%	0.040	26.0	33.0	0.98	0.22	13.90	15.20	16.36	3.16	4.47
AE612PND562MSZ	5.6	±20%	0.046	24.0	30.0	0.98	0.23	13.38	14.86	15.74	2.87	4.06
AE612PND682MSZ	6.8	±20%	0.048	18.0	23.0	0.98	0.22	12.10	13.56	14.20	2.81	3.98
AE612PND822MSZ	8.2	±20%	0.055	16.0	20.0	0.98	0.34	10.30	11.52	12.20	2.76	3.90
AE612PND103MSZ	10	±20%	0.058	14.0	17.0	0.98	0.34	8.80	10.00	10.66	2.56	3.62
AE612PND123MSZ	12	±20%	0.062	12.0	15.0	0.98	0.36	8.20	9.18	9.74	2.48	3.50
AE612PND153MSZ	15	±20%	0.072	10.0	13.0	0.99	0.41	7.40	8.36	9.03	2.30	3.25
AE612PND183MSZ	18	±20%	0.080	9.6	12.0	0.99	0.37	6.50	7.38	7.86	2.18	3.08
AE612PND223MSZ	22	±20%	0.096	8.8	11.0	0.99	0.41	6.00	6.80	7.26	1.99	2.81
AE612PND273MSZ	27	±20%	0.120	8.0	10.0	0.99	0.43	5.80	6.56	7.02	1.78	2.52
AE612PND333MSZ	33	±20%	0.150	7.6	9.5	0.99	0.56	5.50	6.10	6.52	1.59	2.25
AE612PND393MSZ	39	±20%	0.161	6.8	8.5	0.99	0.64	4.70	5.26	5.60	1.54	2.18
AE612PND473MSZ	47	±20%	0.180	6.0	7.5	0.99	0.70	3.70	4.34	4.60	1.45	2.05
AE612PND563MSZ	56	±20%	0.190	5.6	7.0	0.99	0.76	3.60	4.18	4.50	1.41	2.00
AE612PND683MSZ	68	±20%	0.210	5.2	6.5	0.99	0.88	3.50	4.04	4.32	1.35	1.90
AE612PND823MSZ	82	±20%	0.280	4.0	5.0	0.99	0.85	3.30	3.72	4.02	1.16	1.65
AE612PND104MSZ	100	±20%	0.300	3.6	4.5	>0.99	0.90	2.80	3.24	3.46	1.13	1.59
AE612PND124KSZ	120	±10%	0.410	3.4	4.3	0.99	1.31	2.60	2.94	3.16	0.96	1.36
AE612PND154KSZ	150	±10%	0.460	3.3	4.1	>0.99	1.46	2.20	2.54	2.70	0.91	1.29
AE612PND184KSZ	180	±10%	0.510	3.2	4.0	>0.99	0.93	2.10	2.42	2.58	0.86	1.22
AE612PND224KSZ	220	±10%	0.690	2.7	3.4	>0.99	1.54	1.90	2.16	2.28	0.74	1.05
AE612PND274KSZ	270	±10%	0.900	2.5	3.1	>0.99	1.17	1.70	1.94	2.10	0.65	0.92
AE612PND334KSZ	330	±10%	1.02	2.3	2.9	0.99	4.14	1.50	1.70	1.84	0.61	0.86
AE612PND394KSZ	390	±10%	1.12	2.2	2.7	>0.99	1.64	1.40	1.60	1.70	0.58	0.82
AE612PND474KSZ	470	±10%	1.53	1.8	2.2	>0.99	0.25	1.30	1.50	1.60	0.50	0.70
AE612PND564KSZ	560	±10%	1.69	1.6	2.0	>0.99	2.68	1.20	1.34	1.46	0.47	0.67
AE612PND684KSZ	680	±10%	2.29	1.4	1.7	>0.99	2.11	1.00	1.08	1.22	0.41	0.58
AE612PND824KSZ	820	±10%	2.55	1.1	1.4	>0.99	2.39	0.900	1.04	1.18	0.39	0.55
AE612PND105KSZ	1000	±10%	2.87	1.0	1.3	>0.99	4.28	0.850	0.948	1.05	0.37	0.52

Figure 8.5: Coupled inductor characteristics.

build a custom magnetic core ad hoc for the applications, but as well as the transformer of "DC Transformer" it will be expensive and a higher lead time is required.

First thing that can be noticed is that it is a 12.3mm x 12.3mm of area, independently on the value of the primary inductance. However, the current that the device can handle decreases as the value of Lp increases.

This may highlight a problem: in fact it is expected that the solution with lower Fsw and so with higher Lp is not electrically feasible due to the lower amount of current that a 150uH coupled inductor could sustain without reaching higher temperature and possibly damage the device.

Electrical Limits of AE612PND

In order to understand which are the electrical limit of the AE612PND component, the equations 8.3 and 8.4 must be used.

$$I_{prim,peak} = \frac{P_{out}}{V_{out} * (1 - D_{max}) * N} + \frac{V_{in} * D_{max}}{2 * L_p * F_{swt}} \tag{8.4}$$

In order to force CCM at the lower power mode, in equation 8.3 must be used the minimum power of 9W, instead in equation 8.4 must be used the maximum power of 50W, since the same coupled inductor shall be able to allow the maximum flow of current, which obviously corresponds to max power mode.

Table 8.2 shows the results for Fly-back in CCM mode:

Fswt	**Lpri**	**Iprim,rms**	**Imax,rms**
50kHz	180uH	3.32A	1.22A
300kHz	33uH	3.32A	2.25A

Table 8.2: Lprim Vs Fswt and current limit of the component

As Lprim decreased the maximum current which can flow through the component increase. However, even with the maximum switching frequency, the current is too high for the component which implies higher temperature rising during the nominal operation. The Fswt has not increased anymore otherwise losses will become important.
It can be noticed that with the same Vout and Pout,min the Iprim,rms current is constant since switching frequency and Lprim are inversely proportional.

8.1.1 Conclusion about Fly-back CCM

In table 8.2 has been shown that even with the maximum allowable Fswt the coupled inductor is not able to withstand the current necessary to provide 50W at the Fly-back output.

8.2 From CCM mode to DCM mode at low power operation

In the previous section was proved that even the AE612PND coupled inductor is not able to tolerate the current at 50W, when Lprim is designed at 9W in CCM, without losing performances on the power dissipation.
Clearly, the limiting factor is based on the 9W requirement at CCM, which increases the Lprim and lower the maximum acceptable current through the device.

A solution could be to pass from CCM to DCM mode in case of 9W power mode operation and, if necessary, DCM at 25W and 9W. This can be accomplished since power is lower and in turn, also the current will be lower even if it is in DCM mode. Moreover, the power dissipation will be higher in DCM than CCM.

Table 8.3 report the behaviour of the Fswt Vs Lprim behaviour with the Iprim current.

Mode	**Fswt**	**Lpri**	**Iprim,rms**	**Imax,rms**
CCM/DCM 9W	300kHz	12uH	3.39A	3.5A
CCM/DCM 25W	210kHz	8.2uH	3.6A	3.90A

Table 8.3: Lprim Vs Fswt for CCM/DCM

In the CCM/DCM 9W case, the only solution is at 300kHz, in which the coupled inductor current can reach a maximum of 3.5A, therefore capable of sustaining a Primary current of 3.39A.
For the CCM/DCM 25W case, which implies DCM at 9W, there are two possibilities: one at 210kHz and another one at 300kHz. This last option is not considered since the margin introduce in terms of maximum rms current is not worth for the increase of power dissipation.

Core Losses and Temperature Rise

Coilcraft provides an online tool to estimate the power dissipation of the magnetic core and the temperature rising during nominal operation [13].

For what concern the power dissipation of the core, there are not limits imposed by the application and by the environment.
Instead, about temperature rising there are limitations imposed by the scenario: in space environment the temperature can rise up to 60°C. In general, it is imposed to a spacecraft/satellite to not overcome the 100/120°C temperature. This implies that the maximum temperature at which the PSM can rise is 40°C, as well as the temperature for coupled inductor since temperature rise is defined at 20°C ambient temperature.
Table 8.4 and Table 8.5 report the calculation made with the online tool of coilcraft about core dissipation and temperature rising for CCM/DCM 9W and CCM/DCM 25W.

Power mode	**Core Loss**	**Temp rise**
50W	0.949W	56°C
25W	0.488W	29°C
9W	0.423W	25°C

Table 8.4: Fly-back CCM/DCM 9W

Power mode	**Core Loss**	**Temp rise**
50W	1.157W	68°C
25W	0.972W	57°C
9W	0.972W	57°C

Table 8.5: Fly-back CCM/DCM 25W

From previous tables can be noticed that, even if DCM at 9W and 25W allow us to use lower primary inductance, the losses and temperature rising reached in these configurations is not negligible and actually physically not feasible for this application.

8.2.1 Alternatives solutions

In the previous section it was shown that neither imposing DCM at 9W nor DCM at 25W the Fly-backs were not suitable for this application due to higher temperature rising.
Two solutions are proposed in order to overcome this problem:

- Custom magnetic
- Parallel Fly-back

Custom magnetic, as saw in section 7.1, has a lot of disadvantages. However, this is a simple solution since it requires just one coupled inductor.
Instead, with two parallel Fly-back solutions the power delivered by each Fly-back is reduced by half, reducing in this way also the current delivered and temperature of the system.
Another important feature of the Two Parallel Fly-back is the redundancy: in fact, even if one Fly-back fails, the other one can continue to operate.
Probably it will not be able to ensure the maximum power mode operation, or it can be afforded just in low temperature ambient cases but it can still provide power for most of the operation of the SDR.

However, during the development of the SDR, Argotec aim of increasing the power of the SSPA and on feeding the external units of LNA and SSPA directly from the PSM have been consolidated.
This features introduces in the SDR have changed the maximum power requirement for the PSM which pass from 50W to 80W maximum. One single Fly-back is not able to provide such an amount of power, even with a custom magnetic. This requirement is not fixed yet: it can be subjected to other modifications.

8.3 80W Two Parallel Fly-back

With the new maximum power level, new calculations are necessary in order to understand which are the power density capability of each Fly-back. Recall that all the power levels are divided by half in the two parallel configurations.

8.3.1 Force CCM mode at 4.5W

The most restricting configuration is first analyzed, which gives us low core losses due to lower current values. However, the rms current required by each Fly-back in order to provide 40W is too high and the coupled inductor able to withstand that current needs a Fswt of 850kHz.
This value of the switching frequency is unfeasible for the power dissipation of the switch: all the advantages of CCM at 4.5W are wasted.

8.3.2 CCM/DCM 4.5W and CCM/DCM 12.5W

The other two alternatives previously discussed for 50W Fly-back are proposed again for the new power level. The online tool of coilcraft is used for checking the core losses and temperature rise.
Table 8.6 and table 8.7. reports the information of the two alternatives. The tables show the results for a one Fly-back of the two; moreover, the old 25W value is listed in order to have a comparison between the previous implementation at 50W with respect to actual 80W.

Power mode	**Core Loss**	**Temp rise**
40W	0.777W	46°C
25W	0.406	24°C
12.5W	0.228W	13°C
4.5W	0.207W	12°C

Table 8.6: Fly-back CCM/DCM 4.5W for one Fly-back of the two parallel configuration.

Two consideration have to be done:

- The 25W value of a single Fly-back is clearly dissipating less power and temperature rise is lower than the Fly-back for 50W solution
- the DCM mode is giving poor performances than CCM, which becomes relevant in the CCM/DCM at 12.5W case.

Power mode	Core Loss	Temp rise
40W	0.837W	49°C
25W	0.527W	31°C
12.5W	0.455W	27°C
4.5W	0.455W	27°C

Table 8.7: Fly-back CCM/DCM 12.5W for one Fly-back of the two parallel configuration.

Another parameter that could be useful to highlight is the dissipation power of the switch report in Table 8.8. In fact, there is a factor of 2/3 between the switching frequency of the CCM/DCM 4.5W case and CCM/DCM 12.5W.

	CCM/DCM 4.5W	CCM/DCM 12.5W
Pswitch 40W	2.56W	1.9W
Pswitch 25W	1.79W	1.41W
Pswitch 12.5W	1.15W	1.25W
Pswitch 4.5W	1.02W	1.25W

Table 8.8: Fly-back CCM/DCM 12.5W for one Fly-back of the two parallel configuration.

8.3.3 Conclusion about Two Parallel Fly-back Mode

Table 8.8 shows again how DCM mode performs worse, especially in lower power condition.
The higher switching frequency of the CCM/DCM 4.5W becomes relevant when power mode operation increases.

However, given the results in tables 8.6, 8.7 and 8.8 can be notice that the performances of the Two Parallel Fly-back CCM/DCM at 4.5W are better

than CCM/DCM 12.5W, due to low temperature. For power losses instead, considering both magnetic core and switching ones, in overall they are very close, but surely the efficiency is worst during low power mode operation for the CCM/DCM 12.5W.
Two Parallel Fly-back CCM/DCM at 4.5W is choose.

An important aspect has to be point out: if the maximum power level of the SDR will be decreased, for any possible reason, and even if it is decided to return back to 50W, the implementation with Two Parallel Fly-back which share the power delivered to the load is preferred. The main reason of this is the redundancy. Besides temperature rise, which clearly is lower, both core losses and power switching are higher for the two parallel cases. Moreover, cost and area will double.
However, the redundancy feature which allows to the SDR different functionality even if one of the two Fly-back fails as higher benefits with respect to area and cost increment.

8.4 Output capacitor

In this section, it is described the selection of the output capacitor. Rad-hard and Rad-tolerant capacitors implement typical material which can be used in space application. Due to high vibration and huge temperature variation, the capacitors are subjected to extreme condition and they can be easily being damage. For this reason, no out-gassing material are mandatory, avoiding in this way the realizing of fluid into the board, which can run to failure a subsystem or even worse, can comprise the success of the mission.
The main drawback of this kind of capacitor is the low capacity at high voltage.

According to the value of Lp and Fsw defined before in the previous phases it can be derived that the output capacitor should be at least large than 500uF.
The voltage of the capacitor is the same of the output voltage of the Fly-back. However, derating must be considered, in order to increase the lifetime of the capacitor. Looking at the ECSS-Q-ST-30-11C [1], which reports the derating standards used by Europe space mission, can be seen that the output capacitor should have a voltage rating value which is 65% is larger than

28V. In other words, the output capacitor should be at least higher than 50V.

The highest value of rad-hard ceramic surface mount capacitor at 50V is a 4.7uF, so ceramic capacitor is excluded since it will require to many of them.
Polymer and tantalum capacitors are the suggested ones. The best two capacitors available in the market were of two kinds:

- Wet Tantalum trough hole 1000μF, 50V, ESR=0.3Ω
- Solid Tantalum surface mount 47μF, 50V, ESR=0.24Ω

Solid Tantalum capacitor will occupy a large area, since at least 11 of them are necessary in order to reach the 500μF requested, by putting in parallel.
However wet Tantalum one is a through hole capacitor: it will occupy 2 times the area since enough space must be left, both on the top and bottom layer. Moreover, it is bigger and it will reduce the mechanical properties of the board due to the holes.

Before considering one of the two previously listed solutions, it must be recalled that the Fly-back are two, and all the considerations about area should be doubled.
Clearly, at the moment, none of the two solutions is interesting enough.

8.4.1 Three parallel Fly-back 15V

In order to avoid through holes capacitors and to reduce a large cascade of parallel capacitors it is necessary to increase the capacity of each of them.
This can be accomplished by reducing the voltage rating of the capacitors.
With the aim of finding the best capacitors in terms of area and number of them necessary to reach 500μF limit, this approach was done backward.
First of all the best capacitors in terms of voltage- capacity rating was found.
It is a Solid Tantalum with a capacity range from 10μF to 2200μF and voltage rating of 4 VDC to 75 VDC.
The lower voltage rating capacitor is 35V with 100μF. At least 6 of them are necessary which in total occupy them $3cm^2$ more or less. The maximum voltage that can be put to a 35V considering derating is 20V. Another possibility is to choose a lower voltage rated capacitor. The first lower voltage rated

capacitor is a 25V with 220μF. In this case, just 3 capacitors are necessary to reach 500μF limit. However, the voltage that they can withstand with the derating is 15V.

Both the alternatives involve the use of lower voltage rated capacitor which means to lower the output voltage of the Fly-back.
The main drawback of lowering the output voltage is that the current shall be increased for providing the same amount of power. In turn this means that each Fly-back has to supply higher currents than before and new checks are mandatory for controlling if the coupled inductor can support the additional current values. Unfortunately, a single custom Fly-back in CCM can not have a higher power density than the one designed at 40W for 28V. Even decreasing to 20V the drawback in terms of core losses and temperature rise is too high to be considered for a plausible solution.

The suggested solution is to insert add another Fly-back in parallel. In this way the power requested is divided by the three converters and the current for each Fly-back will be lower and the power density of each Fly-back is reduced, decreasing the core losses and the temperature rise.

8.4.2 Defined the new Output Voltage for Fly-backs

As discussed in the previous section, the are two possibilities for the output voltage of the Fly-back:

- 20V with 35V 100μF
- 15V with 25V 220μF

They are compared and analyzed in table 8.9. It is reported also the Two Parallel Fly-back 28V, in order to demonstrate the limit of the old solution.

Can be notice that there are not such important differences among the Three parallel solutions. Instead for Two Parallel Fly-back there are too poor performances: despite having one less converter, the area and cost are not so much different. This totally depends on the output Wet Tantalum capacitors area and cost. Moreover, as discussed above, the peak current for the Two Fly-backs starts to be challenging to be handle by the coupled

	Fly-back 28V	**Fly-back 20V**	**Fly-back 15V**
Power	2 x 40W	3 x 27W	3 x 27W
Peak current	4.4A	3.6A	4A
RMS current	2.8A	2.2A	2.35A
Area	$19cm^2$	$25.5cm^2$	$22cm^2$
Cost	3500€	4670€	4700€
Capac. type	Wet - TH	Solid - SMD	Solid - SMD
Capac. value	1000μF	6 x 100μF 35V	3 x 220μF 25V

Table 8.9: Fly-back solutions and their parameter.

inductors.
Solution with 15V output voltage is the suggested one. However, if during test phases it will give temperature or core losses problems regardless the coupled inductor, the output voltage can be easily tuned by changing the resistors in the feedback loop and adding capacitors on top of the already soldered one on the PCB.
For this reason, output voltage can be perfectly adjusted in consequence to the first experimental results, which gives an important feedback and understanding about the power density capability of the Fly-back.

8.5 Load balancing

Load balancing, in the electronic world, refers to the process of equally subdividing the power provided by two or more converters to the load. This process has the aim of equalizing as possible the values of the currents that each regulator is supplying, balancing the stresses, temperature and power dissipation increasing the lifetime of each of them.
This technique is implemented both in linear and switching regulator.

In this application, the load balancing shall be implemented for Three Parallel Fly-back. In fact, since each converter is built with several discrete components, the tolerances, parasitic elements and differences in the layout will make them working in different operating conditions, changing the

amount of current and power that provides.

The main adopted methods for load balancing are:

- Drop method
- Hall sensors
- Master-slave [17]

Drop method is the simplest one: the balancing between converters are imposed by the voltage drop on a small resistors values, connected after the output capacitors of the Fly-backs. Usually, mΩ resistors are used.

Instead, hall sensors and Master-slave methods are realized with operational amplifiers by sensing the output current or inductor current. The differences between those currents are get at the op-amp's output at it used to control the feedback loop. However, Hall sensors required too many components and higher power dissipation for poor load balancing performances.

Master-slave method is the best one on current sharing. Unfortunately, it is based on a central converter, the master, which provides the reference output current for the others converter, the slaves, which are tuned according to the op-amp's output. MDI company provides an active parallel circuit based on the Master-slave. However, this method is not suitable for this application. In fact, if the master Fly-back fail, the other two are forced to not provide any power to the secondary converters.

Drop solution is used at the moment since it is a really simple implementation and no other circuit is required. Table 8.10 report the simulations results done for figuring out which is the best resistor value in terms of power sharing and power loss. The discrepancies among Fly-backs are introduced by putting the highest and lowest tolerances value at the main components which cause the current differences among Fly-backs, like output capacitors and coupled inductors. This configuration represents the worst case scenario for tolerances differences.

Drop method with R=10mΩ gives poor performances on current sharing. With R=50mΩ the current difference is 14% between minimum and

Res value	Iout 1, ave	Iout 2, ave	Iout 3, ave	Pdiss, tot
10mΩ	2.05A	1.76A	1.56A	0.1W
50mΩ	1.87A	1.81A	1.61A	0.47W
100mΩ	1.78A	1.78A	1.70A	0.92W

Table 8.10: Drop method current sharing performances and power dissipation at 80W.

maximum. Instead for R=100mΩ there is just 5% difference. The best compromise between performances and power losses is the 50mΩ resistor value. If higher current sharing efficiency is required, the resistor values can be easily increased.
Current sharing method using operational amplifier with no Master-Slave condition is working in progress.

8.6 Switch and Diode Design

As well as the Coupled Inductor, Switch and Diode are the main components of a Fly-back which required an accurate design, not only from a voltage and current derating but also on power dissipation and so on stresses.

Switch

The main parameter useful to allow a correct operation of the switch is the maximum voltage that it can withstand when it closes. Equation 8.5 shows how to evaluate the maximum voltage of the switch. The 20% of the maximum input voltage corresponds to an estimation of the ripple generated by the switching action due to leakage inductances.

$$VDS_{max} = Vin_{max} + N * (Vout + Vdiode) + 20\% * Vin_{max} \tag{8.5}$$

Instead, Figure 8.6 report the behaviour of the voltage at the high side part of the switch.

With equation 8.5 and 8.4 the voltage and current rating for the switch are respectively 76.5V and 4.4A. Assuming a Ton=Toff=50ns, which is a

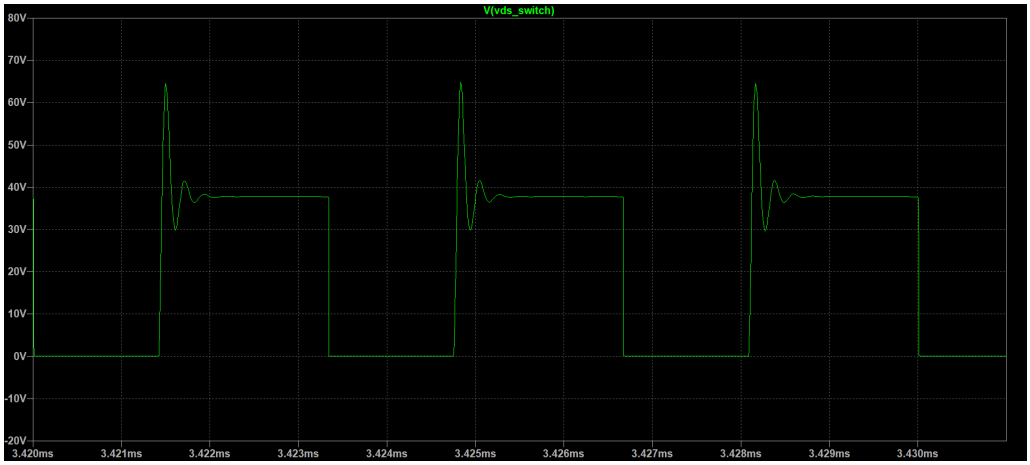

Figure 8.6: Voltage at the drain-source of the switch.

reasonable value for the turn on and off of the switch a power dissipation of 4W is get.
According to the derating percentage listed in the ECSS-Q-ST-30-11C document, the minimum values of voltage, current and power dissipation are:

- VDSmax $\geq$ 100V
- IDSmax $\geq$ 6A
- Pdiss $\geq$ 4W

The are several types of switches available in the market. Si Mosfet are the most common ones. However, GaN Fet are becoming popular in the power field. They provide higher critical electric field strength than silicon. Its higher electron mobility enables a GaN device to have a smaller area for a given rds,on hot resistance and breakdown voltage than a silicon semiconductor. Compared to silicon devices, this also allows devices to be physically smaller and their electrical terminals closer together for a given breakdown voltage requirement.
Moreover, they provide a faster turn on/off switching due to lower gate charges which are important when power losses have to be reduced.
However, the solution which is select for this board is a Silicon Mosfet, with considerably low rds, on hot and a low gate charges. This switch is preferred since it has a lower cost than the Gan Fet and it not require a driver. This

solution is chosen since it is the most convenient for a test board, preferring something which is easy to deal with and with lower cost.
A snubber circuit is necessary in order to damp the oscillation phenomena generated with the switching action and of leakage inductance and parasitic capacitance of coupled inductor and switch respectively. Without a snubber circuit, the output voltage behaviour will be affected. The simplest snubber circuit is made with a series of a resistor and a capacitor which are in parallel to the switch. The values of the snubber are tuned accordingly to leakage inductance and parasitic capacitance. For these components a tuning job is mandatory during the test phase: in fact, the current values which are considered are coming from formulas and from the simulations via LTspice, which will not corresponds to the real case.

Diode

The main parameters for design a diode are the reverse voltage and the average current through it. Equation 8.6 report how the minimum voltage of the Schottky diode is found. As well as the switch, the 20% of the maximum input voltage take in care the ringing phenomena.

$$VD_{rev} = Vout + \frac{Vin_{max}}{N} + 20\%\frac{Vin_{max}}{N} \tag{8.6}$$

Since the turn ratio N were designed to be equal to 1, as previously discussed in chapter 8, the diode reverse voltage is 76.5V equal to the maximum voltage across the Mosfet. Instead, the average current at the output in the maximum power condition is 1.8A.

According to derating, the minimum values of voltage, current and power dissipation are that has to be meet are:

- VDSmax $\geq$ 100V
- IDSmax $\geq$ 6A
- Pdiss $\geq$ 4W

Both Mosfet e Diode are chosen to be radiation resistant. A COTS models with similar characteristics were chosen and implemented in this first board, in order to reduce the cost, since the main goal of this board is to test the design of the whole architecture and components.

8.7 Feedback Loop Design

The custom Fly-back designed with discrete components needs a feedback loop circuit in order to control the output voltage value.
This means that the circuit must be a type 1 system. Usually an operation amplifier with capacitors and resistors introduce poles and zero in order to counter act the frequency response of the Fly-back.
The frequency behaviour of a Fly-back driven in voltage mode has a double pole which depends on the output capacitors value and on the inductances of the coupled inductor and a zero which instead totally depends on the output capacitors characteristics like capacitance and equivalent series resistance (ESR).
Voltage mode is chosen since the power mode of the Fly-back can vary as well as the current through the Mosfet. In this way, the current mode cannot provide a well controlled output voltage value. However, voltage mode has a drawback: right half plane zero (RHPZ) which decreases the total phase margin is present at very low frequency with respect to the current mode. In order to counteract the presence of the RHPZ, the cut-off frequency of the whole system should be at 20%-30% of the RHPZ frequency [18].

8.7.1 Isolated Feedback loop

The Fly-back DC-DC converter topology has the advantage of playing with an additional degree of freedom which is the turn ratio N thanks to coupled inductor. Moreover, this topology as an important feature which is the isolation. In fact, as discussed in chapter 8, isolation is fundamental for avoiding that peak current and interference can be transferred from the input to the output. Isolation, in this way, must be enforced also in the feedback loop.

Isolation can be introduced in three different ways:

- Analogically
- Opto-coupling
- Digitally

In the analog case, transformers can be the simplest way to isolate the output-input path. However, since error signal coming from the output of the

op-amp contains a DC component an additional device, which is in general known as feedback generator, endowed of two switches, is able to transfer the info of the error signal through the transformer thanks to the switching action of the switches.
The opto-coupler, instead, use a LED and a BJT, one for transmitting the information and the other for receiving it. It is an extremely simple solution and cheap solution which requires less design complexity. The digital case, like the most common ADUM from analog devices, introduces isolation converting into a digital form the error signal.

Even if opto-coupler seems to be the most convenient topology, its performance degrades with time and, moreover, it is extremely sensitive to radiation which may affect its nominal operation. Digital solution, instead, requires additional circuitry in order to perform the conversion of the signal into digital domain. This supplementary devices may complicate even more the design of the Fly-back.
The analog solution, with the help of a gate drive transformer and a feedback generator does not require more than these components, providing at the same time an integrated op-amp which, with the help of properly tuned capacitors and resistors, introduce poles and zeros, necessary to compensate the Fly-back response behaviour. Gate drive transformers are quite large but they are not so expensive and they introduce an high isolation between the two coils.

8.7.2 PWM controller

After the gate drive transformer, the information on the output voltage level must be used in order to turn on the Mosfet. For this purpose, a PWM controller is used.
Most of the rad-hard PWM controllers available in the market were designed to be implemented for a current mode controlled DC-DC converter. This because current mode control is the most used in the power design, since it has a simple transfer function of the converter to be compensated, the presence of the RHPZ is at high frequency and it avoids reaching a higher value of the peak current through the coupled inductor.
At this point, the selection of a current PWM controller was forced and an additional circuity design is necessary in order to adapt it to a voltage configuration. Thanks to the internal oscillator of the PWM and of a 5V reference

voltage, with the help of a BJT and resistors, the triangular waveform can be generated, which is necessary for the comparison between the error signal. Among the different rad-hard PWM controllers there are no important differences, except for the output current and area occupation. 1A as output current is sufficient to turn on the Mosfet in less than 50ns, since the total gate charge of the Mosfet is less than 35nC.

Chapter 9

Rest of the PSM Design

In this chapter are briefly reported the design and annotation of the other remained part of the PSM.

9.1 Secondary converters IC COTS Re-design

In chapter 4, was proved that IC COTS LT8613, LT8610 and LT3082 are the best solutions for providing the proper reference voltage and power to the internal and external units of the radio. During the design of the board, however, two considerations modify a minor structure of the secondary converters.
Instead of generating the +5V and -5V from two different converters, another DC-DC regulator of LT family was found to be radiation tolerant since it has a flight heritage on a lunar mission [19]. The LT8471 is a buck and a buck-boost converters, which is able to generate a positive and negative output voltage reference with just one single device. In this, way cost and area are reduced.
Another important consideration made during the design of the secondary converters is that for every IC COTS component that is implemented on the board, a long process of tests must be performed on the lot of each of them, in order to ensure that it is resistant to the extreme condition of the space environment. In fact, high temperature variation test and vibration one are mandatory for a COTS component to be considered reliable during the mission profile. However, in order to test an entire lot of a component, it is extremely expensive in time and cost. In fact, a lot is usually made by

thousands of components which required to buy all or a big part of them for obtaining a reliable result. Moreover, the inspection phases must be performed in different conditions for several characteristics like temperature range, vibration, etc.
With the purpose of minimizing cost and time for these tests phases, the LT8610 component was substitute with the LT8613. This was possible since both cost and area occupation are quite similar as well as the efficiency. Additionally, the LT8613 is capable of providing 3 times the output current of the LT8610 giving in this way a lot of flexibility for future development of the board.

9.2 Connectors and Telemetries

9.2.1 Connectors

As discussed in chapter 2, the SDR has different layers and each layer is entirely devoted to an unit. The nominal operation of the SDR is addressed with the help of two external units: SSPA and LNA. Since Argotec's objective is to provide power to the internal and external units of the radio from the PSM, several connectors must be implemented for interconnecting the PSM with the other units. For what concern the external connection outside the SDR like for SSPA, LNA and the input bus from spacecraft/satellite, micro-D connectors of 25 and 9 pins are chosen since these types of connections are used just for sharing power.
For what concern the connection between the internal units of the radio a stack-able connector is implemented. This type of connector allows to interface the different boards of the SDR, which are stacked vertically, with a single socket which contains 120 pins. This pins are used to provide power to the DPM, for enable signals coming from the FPGA and for telemetries which are generated inside the PSM.

9.2.2 Telemetries

With the aim of monitoring the status of the PSM and of all its output voltages, telemetries are generated inside the PSM. All DC-DC converters and the output voltage of the three parallel Fly-back are monitored both in voltage and current. Thanks to a current sense resistor and a voltage divider,

the informations are send to two ADCs, where one monitor the voltages and the other one the currents.
The outputs of the ADCs goes into the DPM module through the stack-able connector where the FPGA process these signals and provides a feedback about the operative of each output voltage and current generated by PSM. Thanks to these feedbacks, FPGA is able to control the operation of the DC-DC converters with the enable signals.

9.3 PCB Design

In order to test the design of the whole PSM, from the Isolated three parallel Fly-backs, to the secondary DC-DC converters, the telemetries and the connectors, a PCB must be designed. This is extremely useful since it will test how the circuit performs in the real case, apart from software simulations. Moreover, it will give important information about the occupancy density cover by the components over the PCB and understand if the PC-104 form factor is large enough to contain all these components. It is important to highlight that in general a PCB which is occupied by a value larger than 60% starts to be become extremely difficult to be designed since enough space must be left between components for soldering and desoldering phases and for traces and vias, necessary to connects the components.
The main concept behind the design of this PSB is to have a simple board to be managed several times. In fact, since it is a test board, a lot of adjustments must be performed in different part of the board. For example, snubber circuit for clamping the oscillation phenomena of the Fly-backs must be tuned based on the leakage inductance and parasitic capacitance present in the real circuit, as well as load balancing circuit, that can be modified with a different value of the ballast resistor or with a different type of balance method.
Another important aspect of PCB development is the electrical separation between macro models. This is extremely useful when tests have to be performed on a specific side of the PSM without compromising others parts of it if short circuits and/or peak voltages/currents, etc are generated.
Each sub-circuit like Fly-backs, EMI filter, secondary DC-DC converters and telemetries have been electrically separated with DNP zero ohms resistance, which can be mounted or unmounted depending if tests are performed for just a sub-circuit or more of them.

9.3.1 Components Placement

Before starting to routing traces and placing vias, a general study of the placement of components is necessary for two reasons:

- understating of available area
- minimize traces path

Component placement starts with connectors. The 3 micro-d female plug connectors are placed on the longest side of the board, leaving, in this way, enough spaces between them necessary when male connector has to be attached. Stack-able connector must be placed along an edge of the board in order to reduce the space that it occupies, but at the same time, it must be placed in a proper position that allows it to be easily reachable from any point of the board. Along the short side of the board, in the middle of it, can be an interesting point.
Once connectors are placed, the next step is to lay down the protection tvs diodes, which must be placed next to connectors in order to avoid that electrostatic charge generated by human interaction can damage the components. In the next step, the components of the remained sub-circuit were properly subdivided on top and bottom layer of the board: on the top one were laid down the EMI filter, the Fly-backs and the DC-DC converter which feed the PWM controller. On the bottom one instead are present the secondary DC-DC converters, output filters, current and voltage sense and ADCs. In this way the board is easily split in the two main part: primary side and secondary side, which makes easier the electrical tests phase.
On the top layer, the EMI filter is placed near the micro-d connector reserved to the input connections, in order to minimize trace lengths. The three parallel Fly-back, instead, are laid down horizontally, parallel to the stack-able connector.
For the bottom layer, the ADCs were placed close to the stack-able connector, since the telemetries were collected by the FPGA which manages them. Close to output connectors are spot the current and voltage telemetries since after them the output power goes to the connectors. The remained DC-DC converters are laid down in the remained part of the bottom layer.

Figure 9.1 and 9.2 reports the top and bottom layer of the PSM designed in Altium designer software.

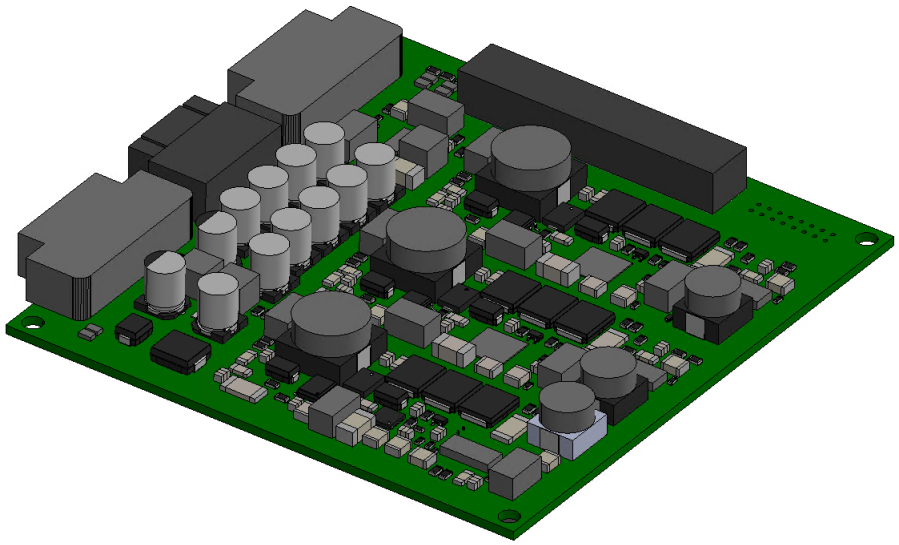

Figure 9.1: Top layer view of the PSM.

9.3.2 Routing of traces

In this type of electronic board the traces of connections between components must be larger enough to support the current which flows trough them. Being this board a power management one, no high frequency signals are present so no matching of traces is necessaries.
According to ECSS-Q-ST-70-12C which collects all the rules that have to be followed for improving the design of the PCB, it is reported a specification about the width of the traces Vs temperature: higher is the temperature, higher is the current that can flow in trace with the same width. A golden rule which can be extracted from these graphs is the 1:1 rule: for each mm of trace width, a 1A of current is assured. For what concerns vias, calculations are necessary with the aim of understanding which is the highest amount of current that can flow into it. With the help of Saturn toolkit, by inserting the height and the diameter of the via, the maximum allowable current that can flow through them is obtained.

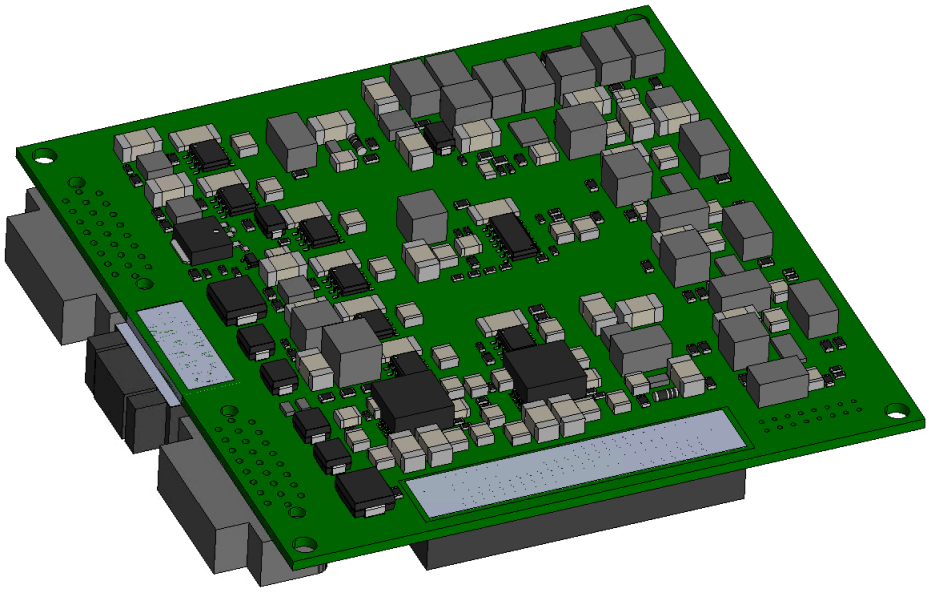

Figure 9.2: Bottom layer view of the PSM.

9.3.3 Power dissipation managing

Power dissipation on a power management board is extremely relevant since performances and failures highly depend on how it is managed. This becomes even more important when air not present like in a space environment. In fact, a lot of techniques which help temperature dissipation like heat sinks, cannot be implemented in this kind of application.
The main way to dissipates power is by contact: on the PSB board, a 4mm width connection has been implemented at the edge of the board for being connected to the case of the SDR. In this way, temperature is well dissipating with the connection between board and SDR's case. Moreover, in order to improve temperature diffusion, all the components which generate a high temperature rise like PWM controllers and DC-DC converters have been equipped with thermal pads, which, thanks to different vias, are connected to board edge contact.

Chapter 10

Conclusion and Future Work

10.1 Conclusion

In this thesis work the implementation of a power management supply board for a Software Defined Radio has been presented. The main purpose is to obtain a prototype of the board which is able to converter the main bus input voltage to several different output voltages providing power to the different units of the radio.

With the aim of reaching this goal, a preliminary design is tested via software with LTspice simulation software. In order to get a prototype and to test the board, a PCB of the PSM must be obtained. Thanks to Altium designer software, components have been placed and traces were route. Finally, a prototype was implemented, ready to be tested and to be upgraded according to future development.

10.2 Future Work

In the next phases of the PSM development, a series of tests must be performed on the board, in order to analyze the design and power capabilities. However, before proceeding with tests, several documents must be written down, like Interface Control Document (ICD), test plan, test procedure, etc. which provides a record of all interface information, from an electrical to a mechanical point of view (such as drawings, diagrams, tables, and textual information) generated for the project.

These tests are:

- Electrical tests, where Fly-backs capabilities and secondary DC-DC converters output voltages and power are tests;
- Conductive Emission and Conductive Susceptibility noise tests;
- Thermal tests;
- Mechanical tests, where the board is subjected to vibration tests and
- Thermo-vaccum test, where the board is test to high temperature variation in the absence of air

All these tests will give results and information on how the board behaves and which are the stressed point that has to be improved in the future phases. This test board is designed with the objective of learning which are the most complicated points of such a difficult design and to upgrade it developing better solutions.

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