POLITECNICO DI TORINO

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Master Thesis

Modeling and analysis of a three-phase ZVS full bridge DC-DC converter

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Abstract

The main goal of this thesis is to derive mathematical models which describe the static and dynamic behavior of three-phase zero-voltage-switching (ZVS) full bridge (FB) converters, which are commonly used in high power applications.
The analyzed circuit uses star-connected transformers and a hybdrige rectifier, which enhances efficiency by reducing the number of conducting diodes with respect to traditional full bridge rectifiers.
Switching flow graph (SFG) nonlinear modeling technique combines average and linearization operations with signal flow graphs theory; such technique is basically graphical, which makes the analysis intuitive and relatively easy.
The operating modes of the circuit and the steps to derive any switching flow graph are presented.
The switching flow graph of the circuit under study in then built and the static and dynamic models are derived from it.
Lastly, time-domain current and voltage waveforms are analyzed to get design equations of components; the design of a prototype for future measurements is done and simulations are provided to verify the validity of the mathematical models.

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Contents

Chapter 1

Introduction

1.1 Switch mode power converters

Switch-mode power converters (SMPC) are circuits able to regulate the output voltage through a control signal, the so-called duty cycle, independently of the input voltage fluctuations and of the load changes. The main reason why SMPC are so popular is that they have high efficiency, which is the key parameter when dealing with power electronics.
The control signal is periodic, therefore all the waveforms across the circuit are periodic. When the transients are expired, the circuit is at steady state, a condition in which each cycle (or period) is equal to the next one.
The operation of the circuit and the methods to derive mathematical models of them are presented.

1.1.1 Basic components and operating principle

The components present in basic SMPC topologies are switches and storage elements. Additional components like transformers and coupled inductors are present in more complex topologies.

Switches They are components able to behave either as a short circuit (ON-status) or as an open circuit (OFF-status). Typically, both active switches (transistors) and passive switches (diodes) are present in SMPC;

the status of active switches depends on their control signal, whereas the status of passive switches depends on the circuit. The role of switches in SMPC is to control the power flow from input to output, according to the control signal.

Storage elements They are components able to store energy: capacitors store electric energy, while inductors store magnetic energy.

Operating principle During each cycle, energy is transferred from the input source to the storage elements, from the input source directly to the load (the output port) and from the storage elements to the load.
Direct converters transfer energy in all the three ways just mentioned, whereas in indirect converters there is no direct energy flow from the input source to the load.
Both in direct and indirect converters each cycle may be divided in two parts according to the switches' status: during one part, storage elements are charged by the input source; during the other one, storage elements discharge transferring energy to the load.

1.1.2 Mathematical models

Mathematical models of the circuits are employed to study and design them. In SMPC, the static model describes the relation between DC quantities and it is used to determine the boundaries of the control signal.
The dynamic model describes instead the frequency response of the circuit and it is used to design a feedback network, which controls dynamically the output quantities.
The frequency response of a linear time-invariant (LTI) circuit is obtained applying Laplace transform to the circuit itself. Unfortunately, SMPC are nonlinear time-variant circuits, therefore some additional operations must be done.

Average Average operation is applied to obtain an equivalent time-invariant circuit from the original time-variant one.
According to the status of switches, SMPC work in different topologies; each of them is an LTI circuit, so they can be described by a linear mathematical model, like a matrix in the state-space averaging. Since the topology of the

converter changes with respect to time and those changes are periodic, it is possible to derive an equivalent representation as the weighted average of all the topologies with respect to their time duration. The aforementioned operation is not valid for any mathematical system, but it is valid for SMPC in general with a good approximation.
Even though average operation keeps the relations between DC quantities unchanged, it results in some information loss; in fact, time evolution of signals is not present anymore.

Linearization The circuit resulting from the average operation (or its equivalent representation, like the matrices in state-space averaging) is still nonlinear; linearization is then necessary. Linearization consists of considering the Taylor expansion of the analyzed signal around an operating point truncated at the first order.
In practice it is assumed that the circuit is working in small condition, which means that any signal is represented by the sum of its DC value and a variation, whose amplitude is much smaller than the one of the DC value. If two or more signals are combined with nonlinear functions, like the multiplication, such functions are expanded and the terms whose order is higher than one are neglected. The order of a term is given by the number of signal variations present in that term.

1.2 Full bridge DC-DC converters

The circuit that will be analyzed and modeled in the next chapters is a more complex version of the single phase full bridge converter, which will be first described. Each element that adds complexity can be analyzed separately, so they will be presented one by one.

1.2.1 Single-phase full bridge

The most used topology for high power level DC-DC converters is the full bridge converter, whose topology is reported in Fig. 1.1. It is a buck-derived isolated converter, which means that its behavior is similar to that of a buck converter, and it is also galvanically isolated thanks to a transformer.
The output node is connected to the filter inductor as in a buck converter and the conversion factor, which is defined as the ratio between output voltage

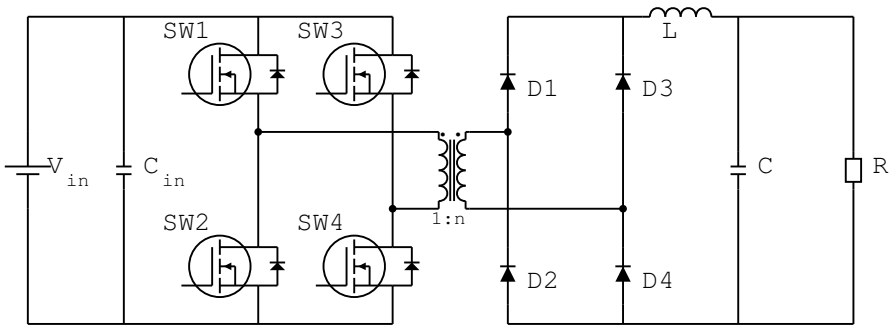


Figure 1.1: Single phase full bridge converter

and input voltage, depends linearly on the duty cycle.
Transformers are magnetic components able to rescale voltage and currents according to the turns ratio, which is the ratio between the number of turns of the windings on the secondary side and on the primary side. Since transformers can work only with AC signals, an inverter circuit is needed between the input source and the transformer itself.
The output voltage is a pure DC voltage, so the AC signal on the secondary side of the transformer must be rectified and filtered. The rectifier is needed because the DC component of an AC signal is zero, whereas the DC value of a rectified AC signal is non-zero; the output filter is needed because the AC component present in the rectified signal may be still too large or comparable with the DC component.

The reason why this circuit is suitable for high power application is that the stress is better distributed among semiconductor components than for other buck-derived topologies like push-pull converter or half bridge converter.

Block representation In general, full bridge converters can be represented as a cascade of functional blocks.

- Input source
- Input filter
- Inverter

- Transformer
- Rectifier
- Output filter
- Load

Figure 1.2: functional blocks description

In the case of the single phase FB shown in Fig. 1.1, the input filter is a single capacitor, the inverter is implemented as a MOSFET H-bridge, the transformer is a single phase one, the rectifier is implemented by a Graetz bridge rectifier and the output filter is a LC filter.

1.2.2 Three-phase operation

Single phase full bridge topology can be modified to make the converter handle more power.
As mentioned previously, an inverter block converts the DC input voltage into an AC quantity, which is later rectified. It is possible to use three-phase inverters and, as a consequence, three-phase rectifiers. Three phase transformers can be used as well as three single-phase transformers; it is convenient to connect them in star or in delta configuration, so the number of semiconductor components in inverter and rectifier blocks can be reduced.
The circuit in Fig. 1.3 shows a three-phase full bridge converter; as it can be seen, three star-connected single-phase transformers are used and, as a result, only a pair of transistor is added in the inverter and a pair of diodes is added on the Graetz brdige recitfier.
Control circuits for three-phase converters are more complicated, but nowadays digital control overcomes this issue. On the other hand, three phase operation reduces stresses on components, because it distributed among more elements. Moreover, input and output currents are at higher frequency, so the filters can be smaller.

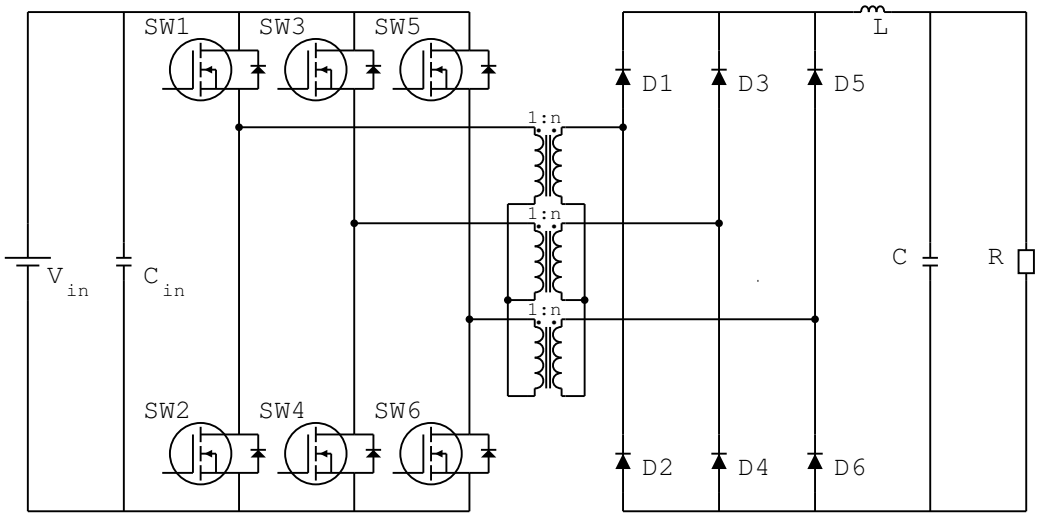


Figure 1.3: Three-phase full bridge converter with Graetz bridge rectifier

1.2.3 Hybridge rectifier

In any buck-derived converter, the rectifier unit is connected to the inductor of the output filter. Efficiency can be enhanced reducing the number of conducting diodes of the rectifier, since the losses due to diodes are basically conducting losses. The hybridge rectifier, whose name is given by mixing the words hybrid and bridge, combines rectifier and output filter blocks substituting the high-side diodes of the Graetz bridge with three inductors.
Inductors are magnetic components and they may be quite big in high-power applications. However, even though the number of inductors and their dimension are increased, which leads to a significant increase of the converter's volume, losses reduction results in a significant reduction of the dimension of the heat sink, and the overall volume of the converter is decreased.
The three-phase full bridge converter with Hybridge rectifier is reported in Fig. 1.4.

1.2.4 Zero-Voltage-Switching

Zero-voltage-switching is an important feature in pulse-width-modulated (PWM) converters, because it reduces switching losses, which are the main contribution in transistor losses.

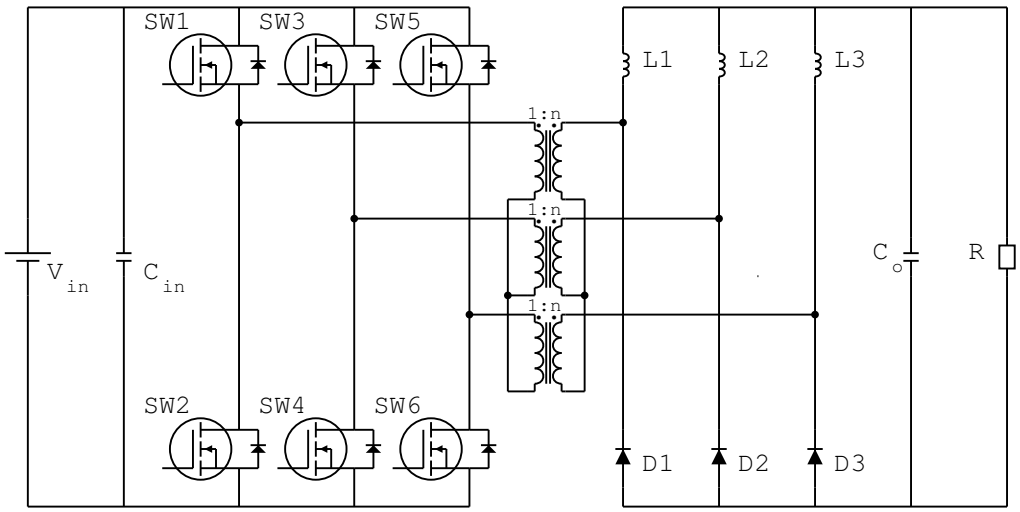


Figure 1.4: Three-phase full bridge converter with Hybridge rectifier

This effect is due to the resonance between the parasitic capacitances of the transistors and the equivalent inductance that such capacitance sees at its terminals. According to the operating modes and to the diodes conducting on the secondary side, the equivalent inductance seen by the parasitic capacitance can be either the leakage inductance at primary side of the transformer or the output filter inductor. ZVS is obtained if the energy stored in the equivalent inductance is large enough to charge the parasitic capacitances.
If the equivalent inductance is the filter inductance, the energy stored in it is large and ZVS is always reached; if the equivalent inductance is instead the leakage inductance, the minimum load condition to achieve ZVS should be verified, as it will be discussed later on.
The ZVS Three-phase full bridge converter with Hybridge rectifier is reported in Fig. 1.5.

Asymmetrical driving Driving signals of each pair are complementary. This kind of technique allows for a better exploitation of semiconductors and makes ZVS effective for a wide load range.

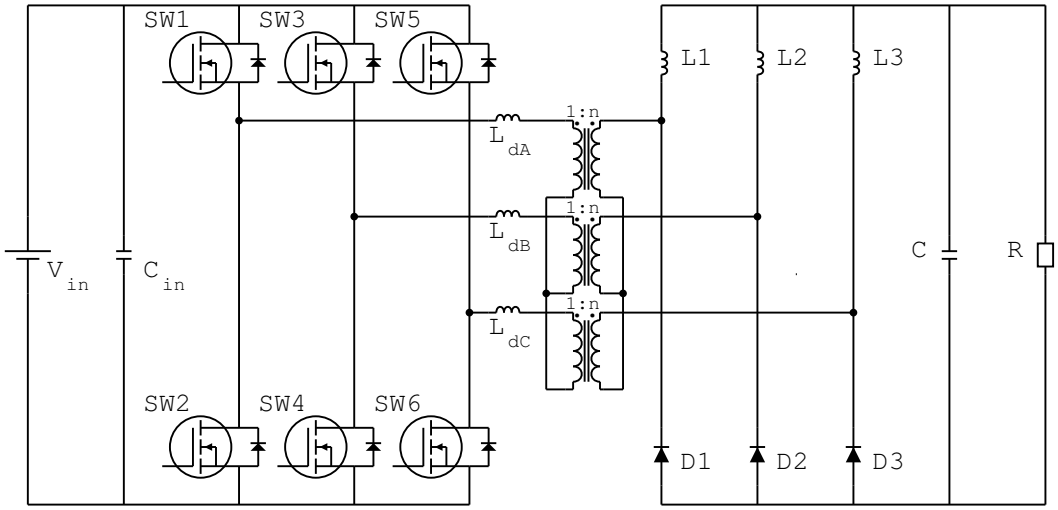


Figure 1.5: ZVS Three-phase full bridge converter with Hybridge rectifier

1.3 Switching flow graph technique

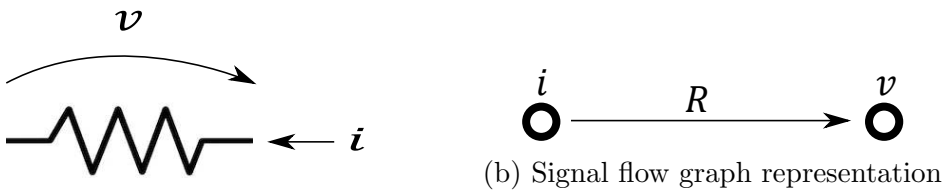
As mentioned previously, switch-mode power converters are nonlinear time-variant circuits, so a method to derive an equivalent linear time-invariant circuit is needed. The proposed method is basically graphical and makes the analysis intuitive and simple.
Switching flow graph method is presented and an example on a simple converter is given to better understand it.

1.3.1 General overview

Switching flow graph nonlinear modeling technique is a generalized method to obtain large signal model, static model and dynamic model of PWM switching converters.
It basically consists of building a signal flow graph for each stage of the converter under analysis, then of performing the average to get a large signal model of the converter; once the large signal model in obtained, the static and dynamic models can be obtained from it through linearization.

Signal flow graphs Signal flow graphs are graphical mathematical objects similar to block diagrams. Like block diagrams, they can be used do describe

LTI systems only and some mathematical rules, like Mason's gain formula and superposition of effects, can be used to derive relations between quantities.
The way to build a signal flow graph is quite easy: nodes represent signals; oriented branches, which connect nodes, represent the cause-effect relation between signals. Each branch has its own transmittance, which quantifies such cause-effect relation. In electric circuits, nodes are currents and voltages, whereas transmittances are impedances, admittances and constants.
There are two kind of nodes:
Input nodes are connected to other nodes with exiting branches only;
Output nodes are all the other nodes.
Fig. 1.6 reports current and voltage across a resistance and the signal flow graph related to it.



(a) Schematic representation

(b) Signal flow graph representation

Figure 1.6: Signals on a resistance

1.3.2 Building large signal model

The steps to derive a switching flow graph and the large signal model associated to it are here presented.

State space average-like procedure Similarly to the State-Space Average method, a SFG of each state needs to be built; all the graphs will be then merged together, as it is done for matrixes in State Space Average. All the graphs must have the same nodes (signals). Branches, instead, may exist in some graphs only, or they can have different transmittance in different stages.
Each stage is associated with a switching function, which is related to the time duration of the stage normalized to the switching period.
In the final switching flow graph, the branches which are not the same in

every graph are substituted by switching branches, which are characterized by the transmittance and a switching function. The switching function associated to the switching branch is the one corresponding to the stage where the branch exists. It is worth noting that branches can exist in several stages.

(a) ON stage (b) OFF stage

Figure 1.7: Signalflow graphs

Large signal model The large signal model can be derived directly from the switching flow graph. Each switching branch is substituted by a multiplier (the symbol used is an AND gate), whose input signals are the input node of the switching branch and the large signal value of the switching function and whose output signal is the output node of the switching branch. Such a model can be implemented on simulators like Simulink, for instance to test the large signal stability; moreover, it can be linearized to derive static and dynamic models.

(a) Switching flow graph (b) Large signal model

Figure 1.8: Switching flow graph and large signal model

1.3.3 Static and dynamic models

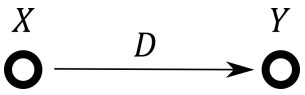
The most useful models that are obtained from the switching flow graph method are the static model, which is describes the behavior of the DC component of the signals and the dynamic model, which describes the behavior of the variation of the signals. Since they are linear, they are actual signal flow graphs; therefore, they benefit from the mathematical rules associated to them; for example Mason's gain formula can be employed to calculate closed loop transfer functions.

To obtain these models, it is necessary to translate linearization into graphical representation. Currents, voltages and control signals can be represented as the sum of their DC component value and first order variation; assuming small signal conditions, the variations whose order is higher than one are neglected.

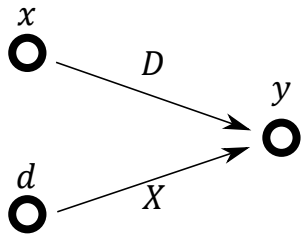
Static model Switching branches are replaced by continuous branches whose transmittance is the steady state value of the switching function. The circuit itself is at steady state, therefore impedances are replaced by their resistance only and admittances by their conductance. It may be useful to consider parasitic elements for pure reactive components in order to avoid having branches with infinite or zero transmittance. After the desired transfer function is obtained, it can be simplified setting to zero (or infinite) the parasitic elements.
Another possibility is to keep impedances and admittances in the static model and then calculate the limit for s approaching zero on the final expression of the desired relation.
Typically, the most important relation is the ratio between the output DC voltage and the input DC voltage, called static gain, which is indicated with the letter M.

Dynamic model The nodes of the dynamic model represent the first order variation of the signals. One additional node should be added for every independent control signal. Like the static model, the dynamic model is linear and Mason's gain formula and superposition of effects can be used.
Typically, the most important relation is the ratio between the variation of the output voltage and the variation of the control signal, which is indicated with the letter H.

Mason's gain formula This formula is used to get relations in systems that have feedback loops. Let first define what are loops and forward paths and then derive the formula itself.
A *Loop* is a path, i.e. a succession of nodes that starts from a node and ends in the same node. The loop gain is the product of the transmittances of the branches of the loops. Loops can be independent or touching. Two touching loops share one or more nodes, whereas independent loops do not share any node.



(a) Steady state signal flow graph



(b) Small signal signal flow graph

Figure 1.9: Signal flow graphs

A *Forward path* is a succession of nodes that starts from a node and ends to another node without touching any node more than once. There may be more than one forward path between two nodes. The gain of the forward path is given by the product of the transmittances of the branches present in the forward path.
Considering a generic output signal Y_2, a generic input signal Y_1, their ratio M is given by the following formula:

$$M = \frac{Y_2}{Y_1} = \sum_{i=1}^{N} \frac{M_i \Delta_i}{\Delta} \tag{1.1}$$

Where:

- N is the total number of forward paths present between the nodes Y_1 and Y_2
- M_i is the gain of i-th forward path, which is the product of the gain of the branches that connect directly Y_1 to Y_2
- Δ_i is the Delta obtained excluding the loops that touch the nodes present on the i-th forward path
- Δ is a quantity related to the loop gains and is given by the following expression: Δ = *1-(sum of all loop gains)+(sum of products of two independent loop gains)+(sum of products of three independent loop gains)+ ...*

1.3.4 Example: buck converter

To better understand switching flow graph technique, a simple converter is analyzed.

The topology of the circuit is introduced and the signal flow graphs associated to each stage of the converter are derived. Then the switching flow graph is derived from them and finally large signal model, static model and dynamic model are derived.

Circuit topology The topology of buck converter topology is presented in Fig 1.10.
Two switches are present: a diode D and a transistor SW. There are two storage elements: the filter inductor L and the output capacitor C_o. The capacitor C_{in} is the input filter. The load is here represented by the resistance R.

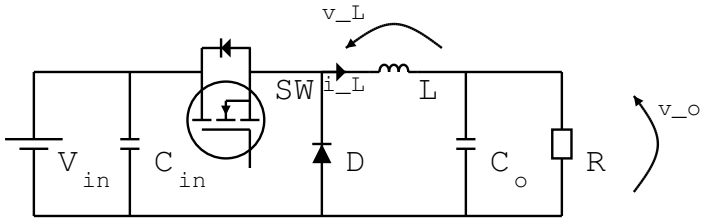


Figure 1.10: buck converter

ON stage When the transistor is conducting, the diode is open and the input voltage is connected to one end of the inductor, while the other end is connected to the output voltage. Therefore, the voltage across the inductor is given by the difference between the input voltage and the output voltage. Inductors current is equal to the inductors voltage divided by the inductors impedance and the output voltage is the inductors current multiplied by the RC parallel impedance.

OFF stage When the transistor is open, the diode conducts; the input voltage is not connected to inductor, whose voltage is equal to the output

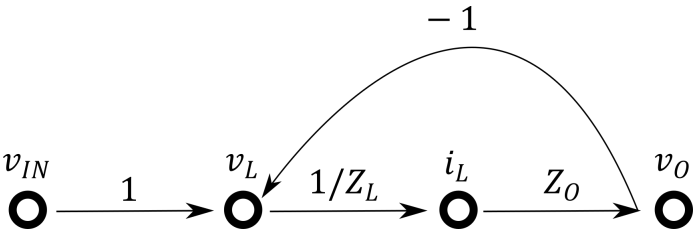


Figure 1.11: Signal flow graph - ON stage

voltage with negative sign.

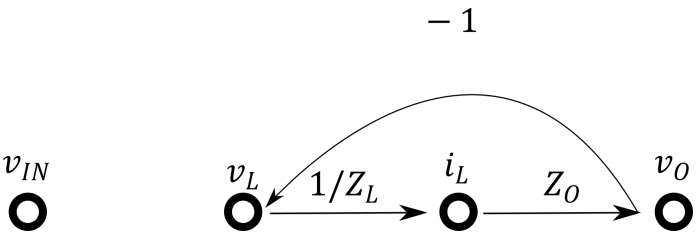


Figure 1.12: Signal flow graph - OFF stage

Switching flow graph As presented previously, the ON stage and OFF stage signal flow graphs can be merged to obtain a switching flow graph; the switching function k associated to is defined as:

$$k = \begin{cases} 1, & 0 < t < T_{ON} \\ 0, & T_{ON} < t < T_S \end{cases}$$

Where T_{ON} is the time interval in which the transistor is conducting. The switching flow graph reported in Fig. 1.13 is obtained substituting the branch that connects the input voltage to the output voltage with a switching branch.

Large signal model The large signal model is obtained substituting the switching branch with a multiplier. The multiplier is represented by an AND gate; the input signals of such multiplier are the large signal value of the input voltage v_{in} and the duty cycle d, large signal value associated to the

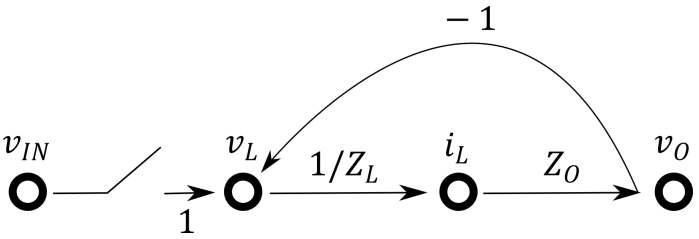


Figure 1.13: Switching flow graph

switching function k.

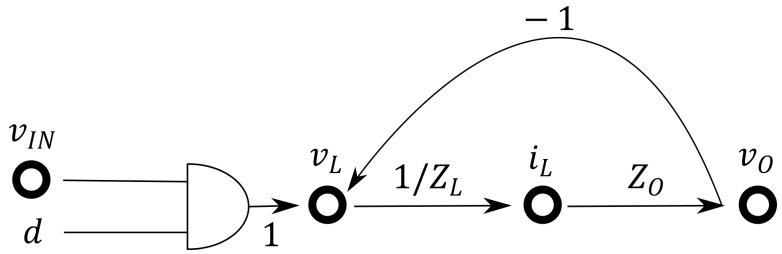


Figure 1.14: Large signal model

As mentioned previously, assuming small signal condition, each signal can be represented as the sum of its DC value and its variation. The product between signals can be therefore developed and linearized, as shown in equation 1.3.
In the case of the buck converter, the only product is the one between input voltage and duty cycle, equation 1.2.

$$v_L = v_{in}\, d \tag{1.2}$$

$$V_L + \hat{v_L} = (V_{in} + \hat{v}_{in}) \left(D + \hat{d}\right) = V_{in}\, D + D\hat{v}_{in} + V_{in}\hat{d} + \hat{v}_{in}\hat{d} \tag{1.3}$$

DC values can be grouped together in equation 1.4. Moreover, neglecting the second order term $\hat{v}_{in}\hat{d}$, the variation of the voltage across the inductor is linear, as shown in equation 1.5.

$$V_L = V_{in}\, D \tag{1.4}$$

$$\hat{v_L} = D\hat{v}_{in} + V_{in}\hat{d} \tag{1.5}$$

Static model The static model is obtained considering DC relations only. The nodes represent the DC component of the signals. Impedances are substituted by resistances and the switching branch is substituted by the steady state value of the duty cycle. The signal flow graph is reported in Fig. 1.15.

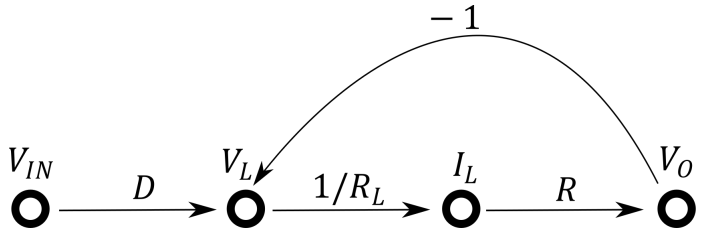


Figure 1.15: Signal flow graph - static model

As introduced previously, Mason's gain formula, can be exploited to get the steady state relation V_o/Vin.
In the case of the buck converter, there is one loop only, whose gain is reported in equation 1.7. The forward path between V_{in} and V_o is reported in equation 1.8 and the delta associated to it is reported in figure 1.9. The delta of the graph is reported in equation 1.10.
R_L is the equivalent series resistance of the inductor.

$$M = \sum_{i=1}^{N} \frac{M_i\, \Delta_i}{\Delta} \tag{1.6}$$

$$T = -\frac{R}{R_L} \tag{1.7}$$

$$M_1 = D\frac{R}{R_L} \tag{1.8}$$

$$\Delta_1 = 1 \tag{1.9}$$

$$\Delta = 1 - T = 1 + \frac{R}{R_L} \tag{1.10}$$

The ratio $M = V_o/Vin$ can now be calculated in equation 1.11. If the equivalent series resistance of the inductor is much smaller than the load resistance, it can be neglected as shown in equation 1.12

$$M = \frac{D\,(R/R_L)}{1 + (R/R_L)} = D\,\frac{1}{1 + (R_L/R)} \tag{1.11}$$

$$M = D\,\frac{1}{1 + (R_L/R)}\bigg|_{R_L \to 0} = D \tag{1.12}$$

Dynamic model The dynamic model is obtained considering signals' variations, which are represented by nodes. Since such a model is linear, superposition of effects can be applied; therefore, when the ratio between the variation of the output voltage and the duty cycle $H = \hat{v}_o/\hat{d}$ is calculated, the variation of the input voltage is set to zero.
As for the static model, Mason's formula is used to get the relation H.

$$H = \sum_{i=1}^{N} \frac{H_i\,\Delta_i}{\Delta} \tag{1.13}$$

$$T = -\frac{Z_o}{Z_L} \tag{1.14}$$

$$H_1 = V_{in}\frac{Z_o}{Z_L} \tag{1.15}$$

$$\Delta_1 = 1 \tag{1.16}$$

$$\Delta = 1 - T = 1 + \frac{Z_o}{Z_L} \tag{1.17}$$

The transfer function reported in equation 1.18 is obtained inserting equations 1.14, 1.15, 1.16 and 1.17 in equation 1.6.

$$H = \frac{V_{in}\,(Z_o/Z_L)}{1 + (Z_o/Z_L)} = V_{in}\,\frac{1}{1 + (Z_L/Z_o)} \tag{1.18}$$

The ratio $\frac{Z_L}{Z_o}$ is calculated in equation 1.19. It is then substituted in equation 1.18 to obtain the final expression in 1.20.

$$Z_L \frac{1}{Z_o} = sL\left(sC + \frac{1}{R}\right) = s\,\frac{L}{R} + s^2\,LC \tag{1.19}$$

$$H = V_{in} \frac{1}{1 + s\,\frac{L}{R} + s^2\,LC} \tag{1.20}$$

The most relevant figures of merit are derived from equation 1.20.

- dynamic gain

$$H_0 = \frac{\partial v_o}{\partial d} = V_{in}$$

- Complex conjugate poles frequency

$$f_P = \frac{1}{2\pi\sqrt{LC}}$$

- Quality factor

$$Q = \frac{R}{\sqrt{L/C}}$$

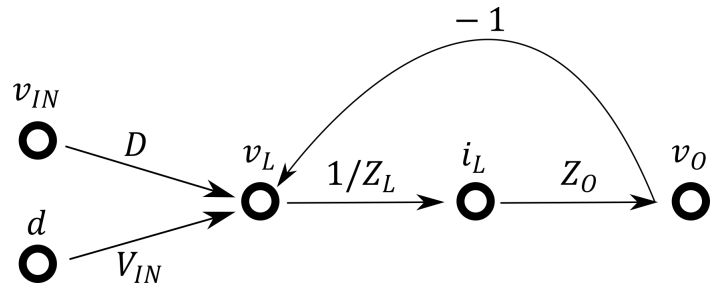


Figure 1.16: Signal flow graph - dynamic model

Chapter 2

Derivation of the mathematical model

2.1 Deep analysis of DMAX operating mode

The topology of the converter is presented and its operating modes are described. The operating mode DMAX is deeply analyzed by describing its stages. The load condition for zero-voltage-switching are then derived and finally, simulations on the software PSIM are briefly presented.

2.1.1 Circuit description and operating modes

The circuit under study, which was introduced in the first chapter and is reported in Fig. 2.1, is a three-phase converter, and three sections can be identified in the circuit. Each section is made by the cascade of a transistor pair, a transformer and a hybridge rectifier, which is a diode-inductor pair. The three sections are identical, so the values associated to the components are the same; for instance, the inductance of all three filter inductors has the value L. Three-phase operation is obtained by shifting the driving signals of the transistors by 120°. Letters A,B,C are associated to each section.
In high power application, the load can be modeled with a current source. In this analysis, instead, a load resistance is used. Since the output voltage is constant, there is no difference in the static behavior, but the quality factor of the frequency response is different.
The behavior of the circuit depends on the duty cycle value, which is related to the driving signal of the transistors. In PWM converters, the duty cycle

is defined as the ratio between the time in which the transistor is conducting and the switching period. Since asymmetrical duty cycle technique is employed, calling D the duty cycle associated to the high-side transistor, the duty cycle associated to low-side transistors is $1 - D$.
According to the duty cycle value, the converter may operate in different modes: if the duty cycle is smaller than 1/3, the converter works in minimum duty cycle operating mode (DMIN); if the duty cycle is bigger than 1/3 and smaller than 2/3, the converter works in medium duty cycle operating mode (DMED), whereas if the duty cycle is bigger than 2/3, the converter works in maximum duty cycle operating mode (DMAX). In DMIN mode, there are time intervals in which the low-side transistors conduct simultaneously, whereas in DMAX mode there are time intervals in which the high-side transistors conduct simultaneously.
The presence of a parasitic inductances on the primary side introduces load effect, which is expressed through a dimensionless quantity called normalized current I'_o. The load effect affects the boundaries of the operating modes and introduces an intermediate mode called DINT between modes DMIN and DMED. The most relevant parameters associated to each mode are the gains: the so-called static gain is defined as the ratio between the output DC voltage and the input DC voltage; the so-called dynamic gain is defined as the derivative of the output voltage with respect to the duty cycle, and it is the gain at the origin of the frequency response transfer function.
The following table reports the boundaries of the operating modes and the gain related to each one of them.

Operating mode	**DMIN**	**DMED**	**DMAX**
Duty cycle range	$I'_o < D < \frac{1}{3}$	$\frac{1}{3} + 2I'_o < D < \frac{2}{3}$	$\frac{2}{3} < D < 1 - 2I'_o$
Static gain $M = V_o/V_{in}$	$n\,(D - I'_o)$	$n\,(D - 3I'_o)$	$n\,(2 - 2D - 3I'_o)$
Dynamic gain $H_0 = \partial V_o/\partial D$	nV_{in}	nV_{in}	$-2nV_{in}$

Fig 2.2 shows the static gain vs duty cycle characteristics varying the normalized current I'_o and assuming turns ratio $n = 1$.
The dynamic gain is positive in operating modes DMIN and DMED and negative in DMAX mode, so a 180° phase difference is present. Since a feedback loop is used to control the output voltage, the converter should be designed to operate either in DMAX or in the DMED/DMIN for stability reasons.

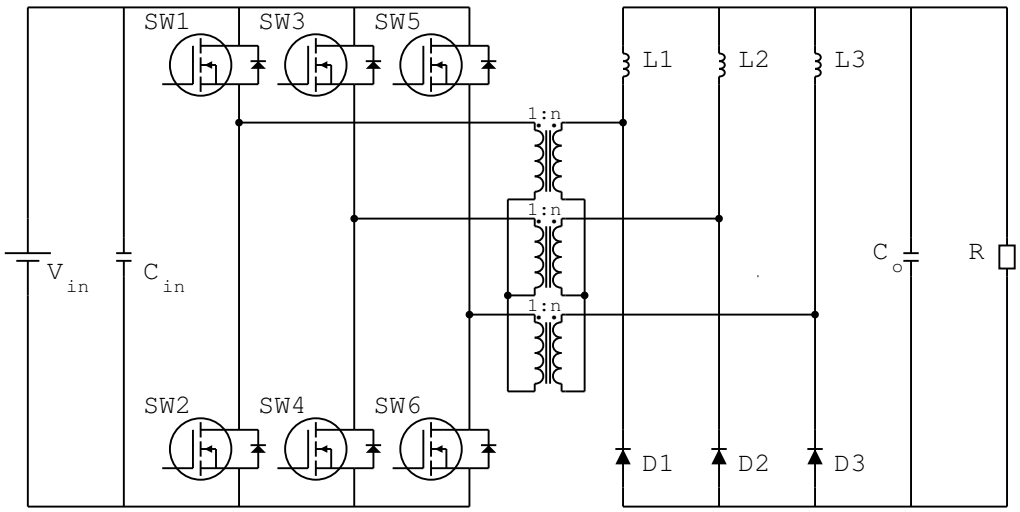


Figure 2.1: Three phase full bridge with Hybridge rectifier

As already mentioned, to have three phase symmetry, the components of each section should be equal. In particular, the inductance of all the filter inductors has the same value L and the turns ratio of each transformer is defined ad the ratio between the number of turns of the windings on the secondary side and the number of turns of the windings on the primary side $N_s/N_p = n$.

2.1.2 DMAX mode

As it was explained earlier, the converter should be designed to operate either in DMAX mode or in DMED and DMIN modes for stability reasons. Since the dynamic gain of DMAX mode is higher, it is chosen to analyze this mode.
In steady state conditions, all the signals of the circuit are periodic; due to three-phase operation, each signal of the three section is delayed of one third of the period with respect to the other stage, for instance the voltage across diode D_2 is delayed by one third of its period with respect to the voltage across diode D_1. Consequently, the frequency of input and output currents is three times the switching frequency.
Moreover, the switching cycle can be divided into three sub-cycles, which are composed by three stages; each section of the circuit experiences the three

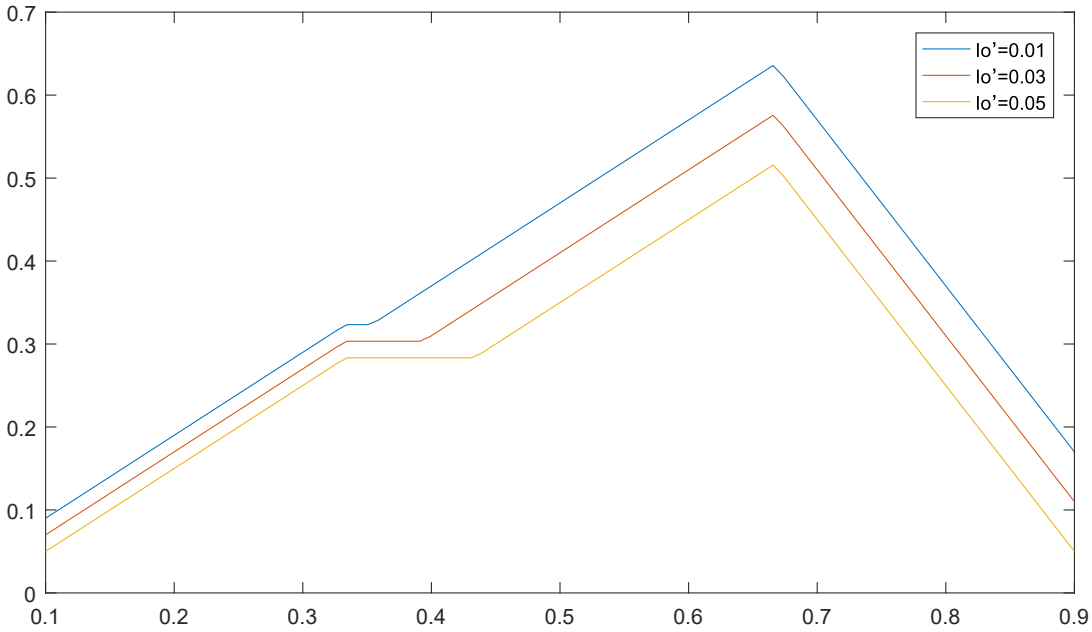


Figure 2.2: Static gain vs duty cycle

stages in a different sub-cycle. A sub-cycle begins when all high-side are turned on and ends when they are switched all on again. At a cycle-level analysis, it is assumed that transistor switching is instantaneous.
The stages are defined by the time instants in which the transistors are switched on and off t_0, t_1, t_3 and an additional time instant t_2 which will be introduced shortly. Fig. 2.3 shows the time intervals in which the transistors conduct and the time instants just mentioned.
The stages that compose the sub-cycle associated to section A is analyzed.

Stage 1 At time instant t_0, when transistor SW_6 turns off, transistor SW_5 turns on instantaneously and stage 1 begins.
Since transistors SW_1 and SW_3 were already conducting, all high-side transistors conduct and the input voltage is not connected to the transformers. Consequently, no energy is transferred from the input source to the load.
Due to the presence of leakage inductances, the voltage and current at the primary side of the transformers are not zero. The direction of the currents depends on the cycle, so basically they have the same direction that they

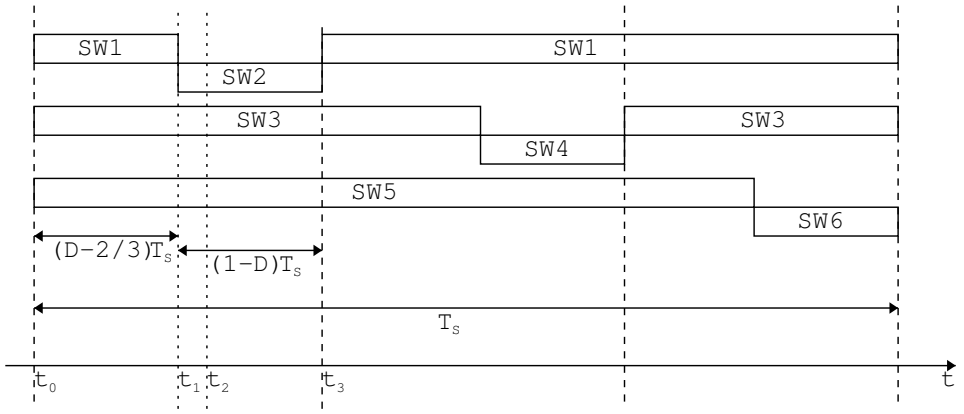


Figure 2.3: Transistors' driving signals and time intervals

had in the previous stage.
Similarly, the diode that is conducting is the one that was conducting in the previous stage; in this case, diode D_3.
The time duration of the stage is the time in which all the high-side transistors are off. Each high-side transistor conducts for a time equal to $(1 - D)\, T_S$ and each sub-cycle lasts $T_S/3$. The duration of stage is the difference between the two time intervals just mentioned, so $(D - 2/3)\, T_S$.

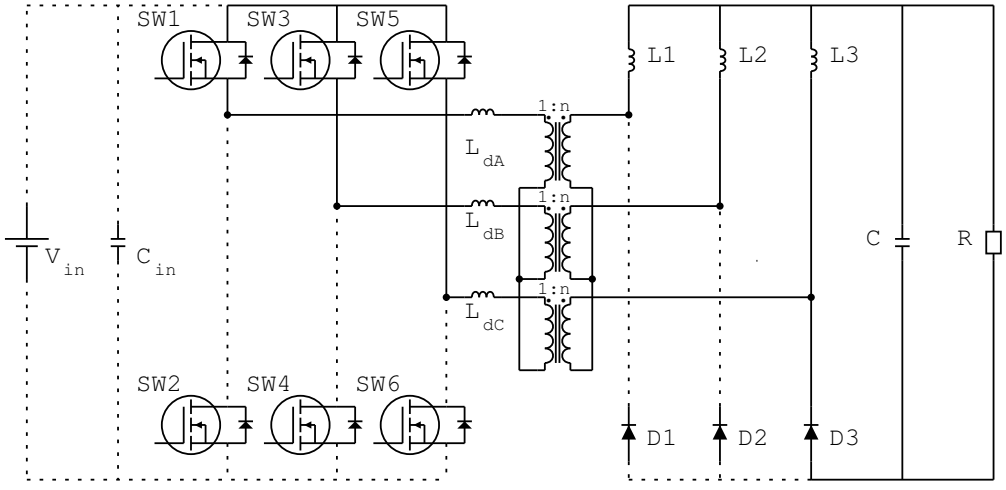


Figure 2.4: Stage 1 - schematic

Stage 2 At time instant t_1 , when transistor SW_1 turns off, transistor SW_2 turns on instantaneously and stage 2 begins.
The direction of currents in sections A and C must be inverted, so diode D_1 starts conducting and its current increases from zero to the output current, whereas the current through diode D_3 decreases from the output current to zero. When this transition ends, stage 3 begins.
During stage 2, filter inductors behave as current sources because their time constant is much bigger than the duration of the stage. The input voltage instead is a voltage source, so basically voltage is forced at the primary side and current is forced at the secondary side. However, since diodes D_1 and D_3 conduct, the voltage across the secondary side of sections A and C is clamped at the same value. The values of voltages and currents are now analyzed to calculate the time duration of the stage, which depends on the value of the parasitic inductance and on the output current.
As already introduced, the input source forces voltage at the primary side and the star-center, which is the common point of the transformers, is fixed at $(2/3)V_{in}$; therefore, the voltage across the parasitic inductance and the primary side of section A is $-\frac{2}{3}V_{in}$ as reported in equation 2.1, whereas the voltage across the parasitic inductance and the primary side of section C is $\frac{1}{3}V_{in}$ as reported in equation 2.2.
At the beginning of the stage, the current flowing through diode $D3$ is the output current I_o and it decreases linearly until it reaches zero. The current through diode $D1$ instead increases from zero to the output current I_o. Since the currents through filters inductors are assumed constant during the stage, the current variation in the diodes is the current variation in the secondary side currents $\Delta i_{sA} = I_o$.
Since the current at the primary side is equal to the current at the secondary side multiplied by the turns ratio, the current variation of the primary side is $\Delta i_{pA} = \Delta i_{pC} = nI_o$ both for sections A and C. As a consequence, the voltage across parasitic inductances v_{LdA} and v_{LdC} is the same, as reported in equation 2.3.

$$-\frac{2}{3}V_{in} = v_{pA} + v_{LdA} \tag{2.1}$$

$$\frac{1}{3}V_{in} = v_{pC} - v_{LdC} \tag{2.2}$$

$$v_{LdA} = v_{LdC} \tag{2.3}$$

$$v_{pA} = v_{pC} \tag{2.4}$$

Equation 2.2 is reorganized to get 2.5.

$$v_{pC} = \frac{1}{3}V_{in} + v_{LdC} \tag{2.5}$$

Substituting equations 2.3 and 2.4 into equation 2.5, equation 2.6 is obtained.

$$v_{pA} = \frac{1}{3}V_{in} + v_{LdA} \tag{2.6}$$

Finally, the expression of v_{LdA} reported in equation 2.7 is obtained substituting equation 2.6 in equation 2.1.

$$-\frac{2}{3}V_{in} = \frac{1}{3}V_{in} + v_{LdA} + v_{LdA} \rightarrow -\frac{2}{3}V_{in} - \frac{1}{3}V_{in} = 2v_{LdA}$$

$$v_{LdA} = -\frac{1}{2}V_{in} \tag{2.7}$$

When a constant voltage is applied to an inductor, its current decreases (or increases) linearly according to the following equation.

$$v_L = \frac{\Delta i_L\, L}{\Delta t} \tag{2.8}$$

Where v_L is the voltage across the inductance, Δi_L is the current variation during time Δt and L is the value of the inductance.
Since the voltage across v_{LdA} is constant, equation 2.8 valid and 2.9 is derived.

$$v_{LdA} = \frac{\Delta i_p L_d}{\Delta t_2} \tag{2.9}$$

Where Δi_p is the current variation at the primary side, which is equal to the output current times the turns ratio $\Delta i_p = -nI_o$, Δt_2 is the time duration of the stage and L_d is the value of parasitic inductance L_{dA}. Since the voltage across L_{dA} is half the input voltage as it was derived in equation 2.7, the time duration of stage t_2 is finally derived.

$$-\frac{1}{2}V_{in} = L_d\frac{-nI_o}{\Delta t_2} \rightarrow \Delta t_2 = 2\frac{nI_oLd}{V_{in}}$$

$$\Delta t_2 = 2\frac{nI_oLd}{V_{in}}\left(f_S\,T_S\right) \rightarrow \Delta t_2 = 2\frac{nI_oLd\,f_S}{V_{in}}T_S$$

The quantity $\left(nI_oLd\,f_S\right)/V_{in}$ is the so-called normalized current I'_o. The expression of time Δt_2 that will be used in the next sections is reported in equation 2.10.

$$\Delta t_2 = 2I'_oT_S \tag{2.10}$$

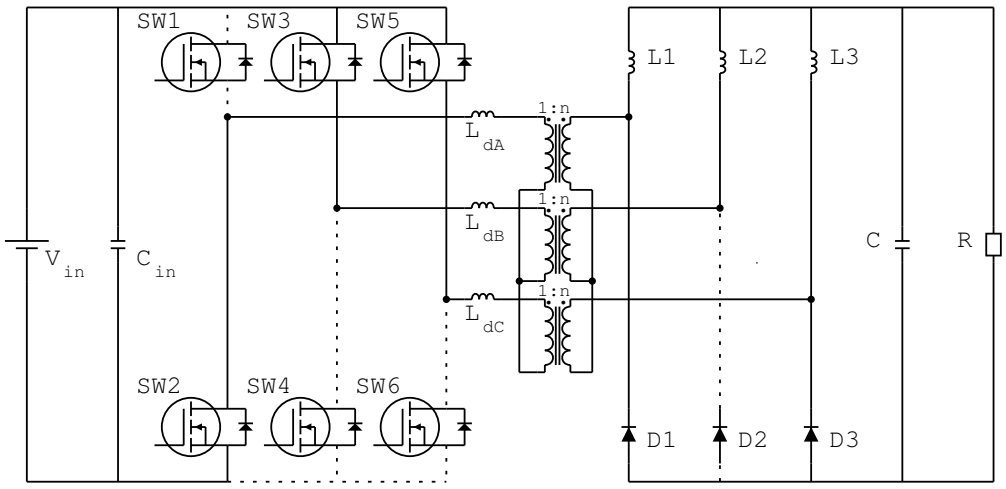


Figure 2.5: Stage 2 - schematic

Stage 3 When the currents in diode D_3 reaches zero, stage 3 begins.
Diode D_1 conducts and the input voltage is applied to inductors L_2 and L_3. The duration of the stage is calculated as the difference between the ON-time of low-side transistors, $(1-D)\,T_S$, and the duration of the second stage, $(2I'_o)\,T_S$, which is then $(1-D-2I'_o)\,T_S$.
To understand better the voltage division on the primary side, the impedances seen by the voltage source V_{in} are analyzed.
The equivalent impedance of the primary side of the transformers Z_p is the series of the parasitic inductance L_d and the parallel of the impedance seen from the intrinsic primary side Z'_p and magnetizing inductance L_m, which is not reported in the schematics of the converter, but is reported in the equivalent model of the transformer in figure 2.6.

Like in stage 2, the inductors behave as constant current sources, which are open circuits from a dynamic stand point. Therefore, the impedance seen at the primary side of the transformers is the series of the parasitic inductance and the magnetizing inductance. Such impedance is the same for all the sections of the circuit. Therefore, since the primary side of sections B and C are in parallel, their equivalent impedance is half the impedance of the primary side of section A. This is the reason why the voltage at the star-center of the primary is fixed at $\frac{2}{3}V_{in}$; these conditions are valid also for stage 2. However, only one diode conducts in stage 3 and the star-center of the secondary side is equal to the star-center of the primary side times the turns ratio, whereas in stage 2 diode D_3 conducts and the star-center is fixed at $\frac{1}{6}n\,V_{in}$.

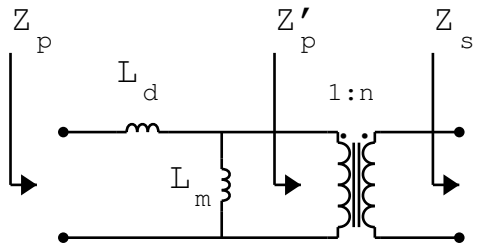


Figure 2.6: Transformer equivalent model

The three stages just described compose the sub-cycle associated to section A only. The two sub-cycles associated to sections B and C are not analyzed because the results is the same as the one just obtained.

2.1.3 Load condition for ZVS

Zero-voltage-switching (ZVS) is an important goal in PWM converters, because they are characterized by low conducting losses but high switching losses. ZVS is basically due to the resonance between the parasitic capacitance of the transistors and the equivalent inductance seen at their terminals. The energy stored in the equivalent inductance charges the parasitic capacitance of one transistor of a pair and discharges the capacitance of the other transistor of thar pair. If the energy stored in the inductance is large enough to fully charge/discharge the capacitances, ZVS is achieved.
In the case of the converter under study the behavior of low-side transistors and of the high-side transistors should be evaluated differently.

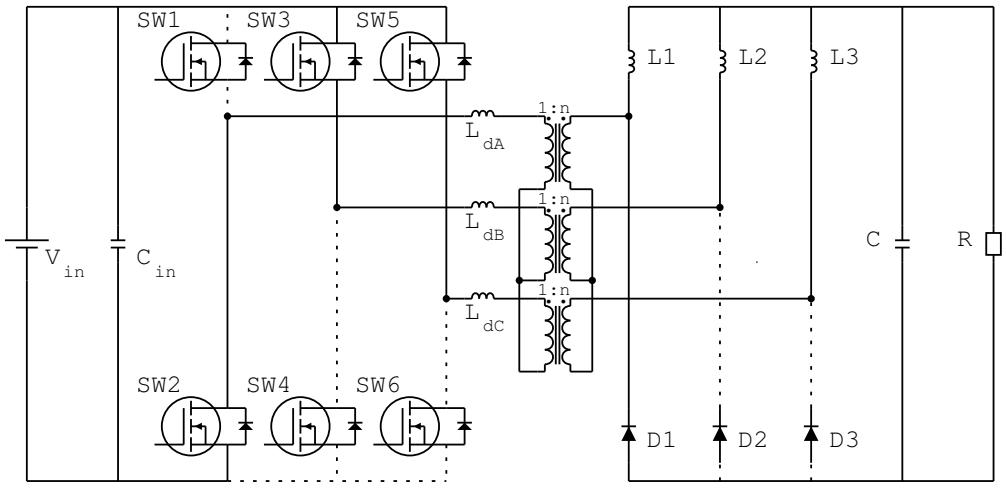


Figure 2.7: Stage 3 - schematic

Considering some dead time between the turn-off of a transistor and the turn-on of the other one, the high-side transistors always switch losslessly because they are not connected to the input voltage when they switch.
In the case of the low-side transistors there are two possible situations: when the low-side transistors are turned on, the equivalent inductance is the series of the leakage inductance and the filter inductance seen by the primary side, whereas when they are turned off the equivalent inductance is the leakage inductance only, because the diode is conducting at the secondary side.
Since the filter inductance is typically large, the energy stored in it is large too and ZVS is always achieved.
On the other hand, if the parasitic capacitance sees the leakage inductance only, the energy stored in it should be large enough to discharge the parasitic capacitance of the low-side transistor and discharge the parasitic capacitance of the high-side transistor. Since the energy stored in an inductor depends on the current flowing in it, ZVS depends on the output current.
The minimum load condition is now evaluated.
At the end of stage 3, when the low-side transistor is turned off, the current flowing through is is about $n\,(2/3)\,I_o$, and the energy stored in it is reported in equation 2.11.

$$E_{Ld} = \frac{1}{2} L_d I_p k^2 \approx \frac{1}{2} L_d \left(n \frac{2}{3} I_o \right)^2 = \frac{2}{9} n^2 L_d I_o^2 \tag{2.11}$$

The energy E_{Ce} of the low side parasitic capacitance is zero and at the end of the charge depends on the square iof the inbout voltage as shown in equation 2.12. The high-side capacitor instead is charged at the input voltage and must be discharged of the same amount E_{Ce}.

$$E_{Ce} = \frac{1}{2} C_e V^2 = \frac{1}{2} C_e V_{in}^2 \tag{2.12}$$

Since the energy stored in the leakage inductance must charge one capacitance and discharge the other one, it should be equal to twice the energy of the capacitance. Equation 2.13 reports the minimum load condition, i.e. the minimum output current I_o, to achieve ZVS for all transistors.

$$\begin{aligned} \frac{2}{9} n^2 L_d I_o^2 = 2 \left(\frac{1}{2} C_e V_{in}^2 \right) \rightarrow I_o^2 = \frac{9}{2} \frac{C_e V_{in}^2}{n^2 L_d} \\ I_o = \frac{3}{\sqrt{2}} \frac{V_{in}/n}{\sqrt{L_d/C_e}} \end{aligned} \tag{2.13}$$

2.1.4 PSIM simulations

The software PSIM was used to perform circuit simulations and compare their results with the mathematical models. All simulations are time-based, which means that signal are integrated in time domain.
Two kind of simulations were performed to get different results.

Steady state simulations It is possible to sweep the parameter of a component and compare the DC voltage on a desired measurement point. The value of the duty cycle, which was implemented as a voltage generator, was swept throughout its range and the DC output voltage was measured. The measurement is performed after a settable steady-state time is ended.

Small signal simulations It is possible to simulate the small signal behavior of the circuit exciting the circuit with a sinewave with settable amplitude and measuring the amplitude and phase of the sinewave of the desired measurement point on the circuit. The frequency of the excitation is swept in a range which should be defined in the simulation control panel.

2.2 Simplified converter model

Before analyzing the complete converter and deriving the models associated to it, a simplified version of the converter is studied. The simplification introduced basically consists of setting to zero the parasitic inductance on the primary side of the transformers. As a consequence, stage 2 does not exist and the duration of stage 3 is the maximum $(1-D)\,T_S$, because the normalized current I'_o, which depends on the parasitic inductance L_d is zero. This simplified analysis makes it possible to get more familiar with three-phase PWM converters and with switching flow graph method. Moreover, the effect of the parasitic inductances on the mathematical models can be evaluated comparing the most relevant figures of merit of the converter.

2.2.1 Building the switching flow graph

To build an effective flow graph, it is useful to follow some rules, like placing the sequence of nodes as they appear on the circuit, putting voltage nodes before current nodes for inductive elements and vice versa for capacitive elements. As in the buck converter example, the signals used to build the graphs are the ones related to the input side of the converter and the output side of the converter, so the input voltage v_{in}, the voltages across the inductors v_{L1}, v_{L2} and v_{L3}, the output current i_o and the output voltage v_o.
Fig. 2.8 reports the and the nodes present in the switching flow graph that will be derived. The polarity of the voltages and the direction of the currents will be always indicated on the schematics.

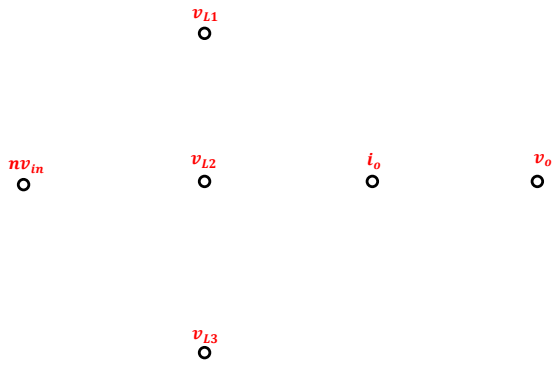


Figure 2.8: Signals - signal flow graph

Stage 1 - signal flow graph During stage 1, all high-side transistors conduct, therefore the voltage across the primary side of the transformers is zero. Diode D_3 is forward biased (because it was conducting in the previous stage) and the voltage drop across the other two diodes is zero, even if they do not conduct. As a consequence, the voltage drop across the inductors equals the output voltage (with negative sign) and all their currents decrease linearly.

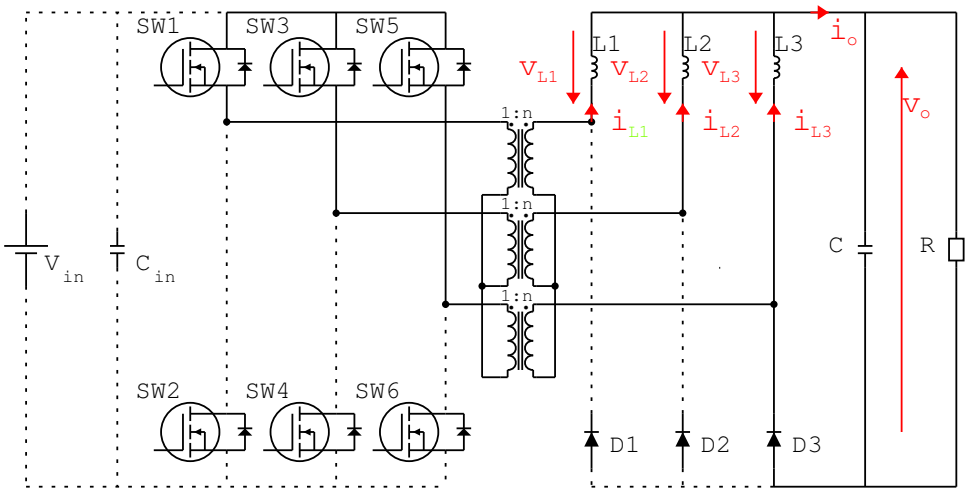


Figure 2.9: Stage 1 - schematic

The following equations are derived from the previous considerations:

- inductors voltages
$$v_{L1} = v_{L2} = v_{L3} = -v_o$$
- inductor's current
$$i_L = v_L \frac{1}{Z_L}$$
- output current
$$i_o = i_{L1} + i_{L2} + i_{L3} = (v_{L1} + v_{L2} + v_{L3}) \frac{1}{Z_L}$$

Where $Z_L = sL + R_L$ is the impedance of each inductor and $1/Z_o = (sC + 1/R)$ is the admittance of the output RC parallel. As it was mentioned

already, the components are assumed ideal in the analysis. A parasitic resistance is placed in series to the filter inductors because it is useful for deriving the static model, as it wll be explained shortly.
It is worth reminding that if two or more signals enter a node, it means that they are summed. The currents in the filter inductors are not present explicitly on the graph, but they are implicitly present as the voltage across the inductors divided by the impedance of the inductors and summed in the output current node i_o.
The signal flow graph associated to this stage is derived from the equations reported above and it shown in Fig.2.10. It is possible to notice just looking at the graph that input power is not transferred to the load, in fact the node v_{in} is not connected to any other node.
As mentioned in the previous chapter, the switching function is a variable related to the time duration of the stage. It is associated to the branches of the stage under study. The switching function is 1 during the stage and is zero elsewhere.

The switching function k_1 associated to stage 1 is reported in equation 2.14 and it large signal value is $d - 2/3$.

$$k_1 = \begin{cases} 1, & t_0 < t < t_1 \\ 0, & t_1 < t < t_3 \end{cases} \tag{2.14}$$

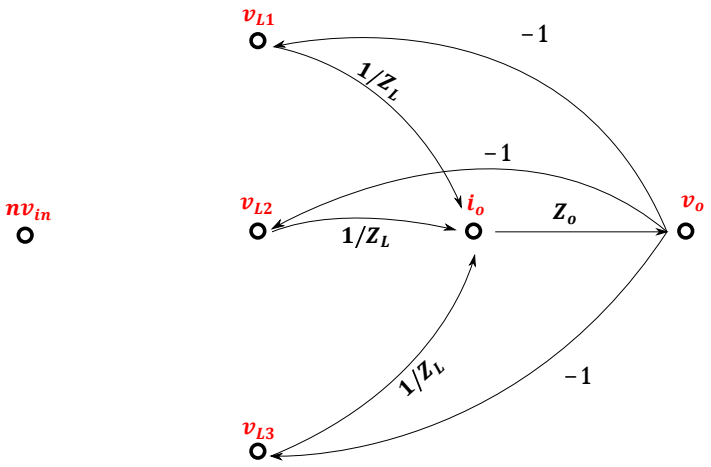


Figure 2.10: Stage 1 - signal flow graph

Stage 3 - signal flow graph As it was introduced previously, since the leakage inductance is zero, the normalized current I'_o is zero and stage 2 does not exist because its duration is proportional to the normalized current.
When transistor SW_2 is switched on stage 3 begins.
As it was explained when analyzing DMAX mode, the input source forces voltage on the primary side of the transistors. the impedance seen at the primary side of each transformer is the same. Therefore, since the primary side of the transformers of sections B and C are in parallel, their equivalent impedance is halved and the star-center is fixed at $(2/3)\,V_{in}$ Derive voltage on inductors
During stage 3, input power is transferred to the load, in fact the voltage node v_{in} is connected to the filter inductors' voltages.

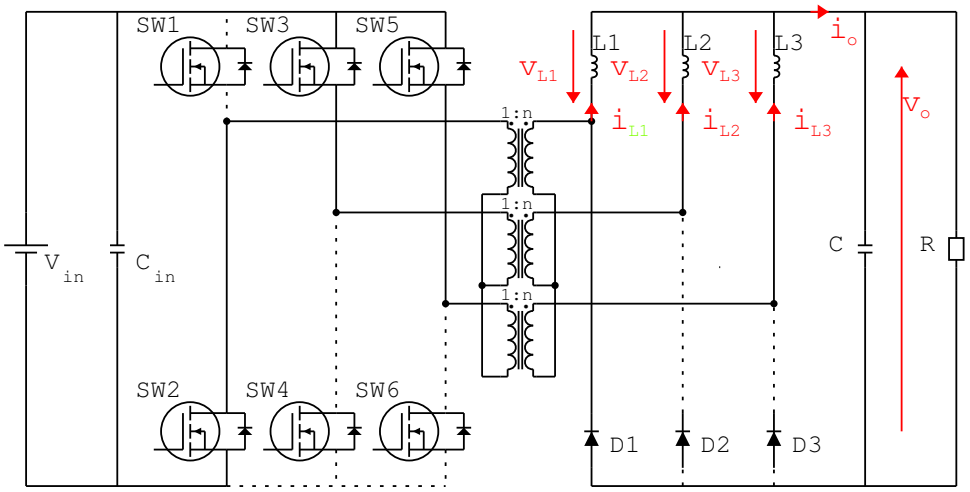


Figure 2.11: Stage 3 - schematic

The following equations are derived from the schematic in Fig. 2.11 and are reported on the signal flow graph associated with stage 3 in Fig. 2.12.

- Primary side voltages

$$v_{pA} = -\frac{2}{3}v_{in}$$

$$v_{pB} = \frac{1}{3}v_{in}$$

$$v_{pC} = \frac{1}{3} v_{in}$$

- Secondary side voltages

$$v_{sA} = -\frac{2}{3} n v_{in}$$

$$v_{sB} = \frac{1}{3} n v_{in}$$

$$v_{sC} = \frac{1}{3} n v_{in}$$

- Inductor voltages

$$v_{L1} = -v_o$$

$$v_{L2} = -v_o + v_{sB} - v_{sA} = -v_o + \frac{1}{3} n v_{in} - \left(-\frac{2}{3} n v_{in} \right) = -v_o + n v_{in}$$

$$v_{L3} = -v_o + v_{sC} - v_{sA} = -v_o + \frac{1}{3} n v_{in} - \left(-\frac{2}{3} n v_{in} \right) = -v_o + n v_{in}$$

- Output current

$$i_o = i_{L1} + i_{L2} + i_{L3} = \frac{v_{L1}}{Z_L} + \frac{v_{L2}}{Z_L} + \frac{v_{L3}}{Z_L}$$

- Output voltage

$$v_o = Z_o i_o$$

As is can be seen directly from the signal flow graph, there is a direct path from the input source to the load.
The switching function k_3 associated to stage 3 is reported in equation 2.15 and its large signal value is $1 - d$.

$$k_3 = \begin{cases} 1, & t_1 < t < t_3 \\ 0, & t_0 < t < t_3 \end{cases} \tag{2.15}$$

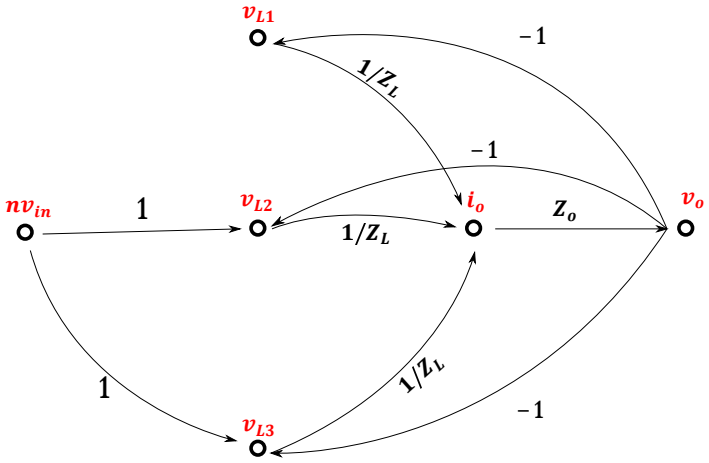


Figure 2.12: Stage 3 - signal flow graph

Switching flow graph As it was explained in the first chapter, average operation is performed on the signal flow graphs associated to the stages of the converter described above and a switching flow graph is obtained. The branches that exist in some stages only are replaced by switching branches, which are associated to the sum of the switching function of the stages in which hat branches existed.
The switching flow graph associated to section A is reported in Fig. 2.13. The branches that connect the input voltage to inductors voltages v_{L2} and v_{L3} exist in stage 3 only, so in the switching flow graph they are replaced by a switching branch with switching function k_3 and transmittance 1.

The switching flow graph just described is related to section A only; thanks to three-phase operation, it is not necessary to analyze the three stages of the other two sections, because the result is the same, apart from the switching branches. In the sub-cycle associated to section B, there are two switching branches connecting the node v_{in} with the nodes v_{L1} and v_{L3}; In the sub-cycle associated to section C, there are two switching branches connecting the node v_{in} with the nodes v_{L2} and v_{L3}.
The final switching flow graph, which is the combination of the three just mentioned, is reported in Fig. 2.14. The switching functions present in the final graph are the sum of the switching functions present in the graphs associated to the three sections.

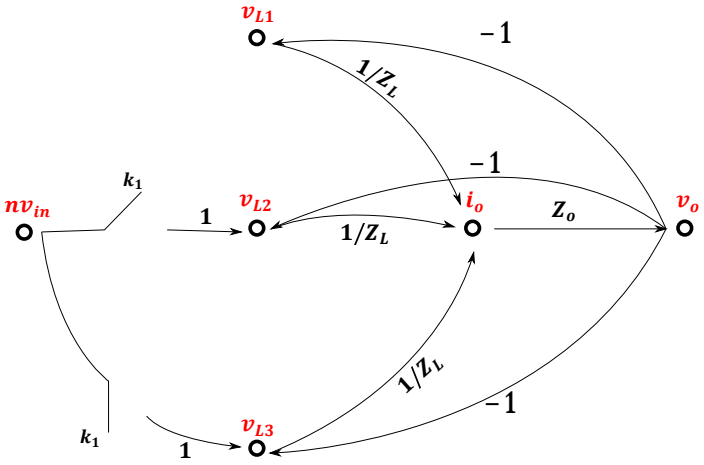


Figure 2.13: Switching flow graph - section A

2.2.2 Large signal model and linearization

As it was introduced in the first chapter, a large signal model, reported in Fig. 2.15, can be derived directly from the switching flow graph associated to the three sections.
To do that, switching branches should be replaced by a multiplier whose input signals are the input signal itself and the large signal value of the switching function.
In the case of the simplified converter model, the large signal value of the switching function is $2\,(1-d)$, in fact the switching function k_3 is associated to stage 3, whose duration is $(1-D)$.

It is useful to write the expression of the signals that contain a product of two or more signals to derive easily the steady state and small signal models. In the case of the simplified converter, the signals given by a product of two signals are voltages across inductors.
The expression of the voltage across each inductor is given by equation 2.16.

$$v_L = n\,v_{in}\,(2-2d) - v_o \tag{2.16}$$

Assuming small signal condition, each signal can be expressed as the sum of its DC value, indicated in capital letters, and its variation, indicated with the hat operator.

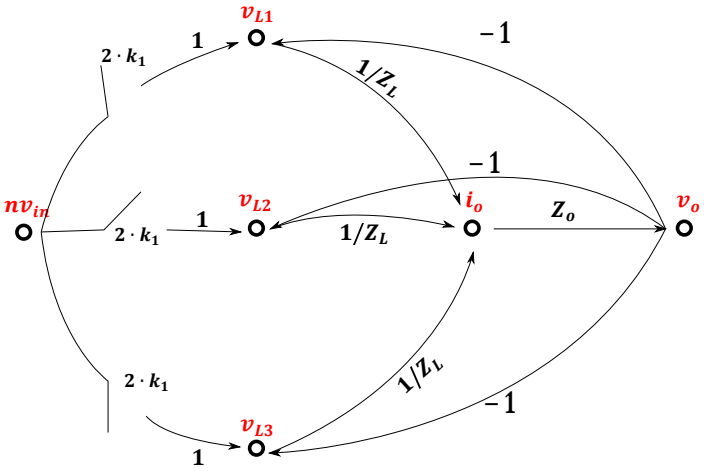


Figure 2.14: Switching flow graph - three sections

$$V_L + \hat{v_L} = n\ (V_{in} + \hat{v_{in}}) \left(2 - 2D - \hat{d}\right) - (V_o + \hat{v_o}) \tag{2.17}$$

Equation 2.17 can be developed.

$$V_L + \hat{v_L} = n\,V_{in}\,(2 - 2D) + n\,V_{in} \left(-2\hat{d}\right) + n\,(2 - 2D)\,\hat{v_{in}} - 2n\hat{v_{in}}\hat{d} - (V_o + \hat{v_o}) \tag{2.18}$$

Equation 2.18 can be regrouped to separate DC values and small signal variations.

$$V_L = n\,V_{in}\,(2 - 2D) - V_o \tag{2.19}$$

The first order variation is instead:

$$\hat{v_L} = n\,V_{in} \left(-2\hat{d}\right) + n\,(2 - 2D)\,\hat{v_{in}} - \hat{v_o} \tag{2.20}$$

The second order term $-2n\,\hat{v_{in}}\,\hat{d}$ is non linear. Assuming small signal conditions, it can be neglected.

2.2.3 Static model

To get the steady state signal flow graph, DC signals are present on the graph and switching branches must be replaced by regular branches, whose

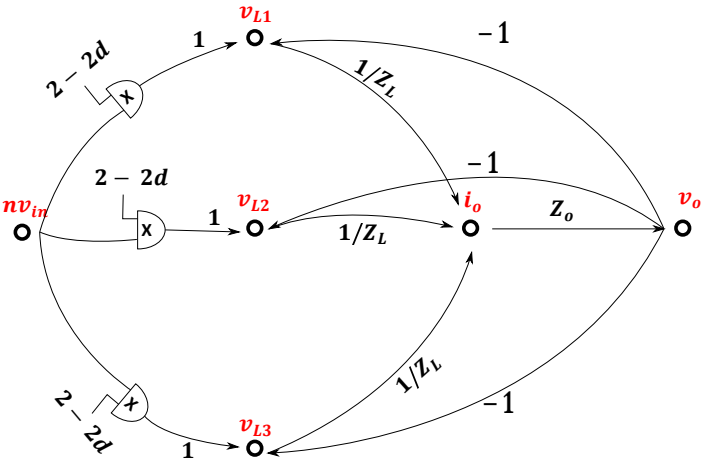


Figure 2.15: Large signal - signal flow graph

transmittance is equal to the steady state value of the switching function.
As mentioned in the previously chapter, there are two possibilities to deal with transmittances.
The first solution is to set the Laplace variable to zero $s \to 0$ when building the steady state signal flow graph; therefore, impedances are substituted by their resistances and admittances are replaced by their conductances. In the case of purely reactive components, i.e. ideal capacitors and inductors, it is possible to consider a parasitic resistance in series to inductor or in parallel to the capacitor in the graph; after the desired relation is obtain, the limits for inductor's series resistances approaching zero and the limits for capacitors' parallel resistances approaching infinite are calculated.
The second solution is to keep impedances on the graph, derive relations using Mason's gain formula and calculate the limit $s \to 0$ in the final formula. This solution is useful when there are loops that contain the ratio between impedances or admittances.
In the case of the simplified converter model, the first solution proposed is used, so the impedance of the filter inductor is replaced by the equivalent series resistance R_L.
The signal flow graph associated to the steady state DC quantities is reported in figure 2.16.

The steady state signal flow graph is a linear model, so relations between signals can be derived using the mathematical rules associated to sig-

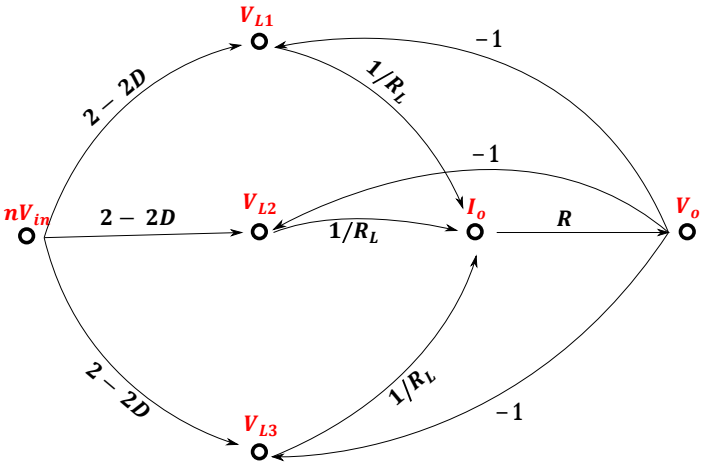


Figure 2.16: Steady state - signal flow graph

nal flow graphs. As it was introduced in the previous chapter, the relation $M = V_o/V_{in}$ is derived using Mason's gain formula, which is reported in 2.21. The node associated to the input voltage contains the turns ratio, so the ratio V_o/nV_{in} should be multiplied by the turns ratio to get the static gain M.

$$M = n\frac{V_o}{nV_{in}} = n\frac{\Sigma M_i \Delta_i}{\Delta} \tag{2.21}$$

There are three identical loops, which are touching. Their gains are reported in equation 2.22.

$$T_1 = T_2 = T_3 = -\frac{R}{R_L} \tag{2.22}$$

The Delta of the graph is calculated from the loop gains and is reported in equation 2.23.

$$\Delta = 1 - (T_1 + T_2 + T_3) = 1 + \frac{3R}{R_L} \tag{2.23}$$

The gain of the three forward paths between input and output node and the delta of each path are reported respectively in equations 2.24 and 2.25.

$$M_i = (2 - 2D)\,\frac{R}{R_L} \tag{2.24}$$

$$\Delta_i = 1 \tag{2.25}$$

The quantities just obtained are then substituted in Mason's gain formula to get the stati gain M.

$$\begin{aligned} M = n\frac{V_o}{nV_{in}} = n\frac{\Sigma M_i \Delta_i}{\Delta} = n\frac{3\,(2-2D)\,\frac{R}{R_L}}{1+\frac{3R}{R_L}} \\ = n\frac{2-2D}{\frac{R_L}{3R}+1}\bigg|_{R_L \to 0} = n\,(2-2D) \end{aligned} \tag{2.26}$$

As it was explained at the beginning of the paragraph, the equivalent series resistance was taken into account in the signal flow graph. The limit for R_L approaching zero is calculated in equation 2.26.

Comparison with simulations The validity of the mathematical model just obtained can be verified comparing it with circuit simulations.
Fig. 2.17 shows that the simulation results and the model perfectly overlap.

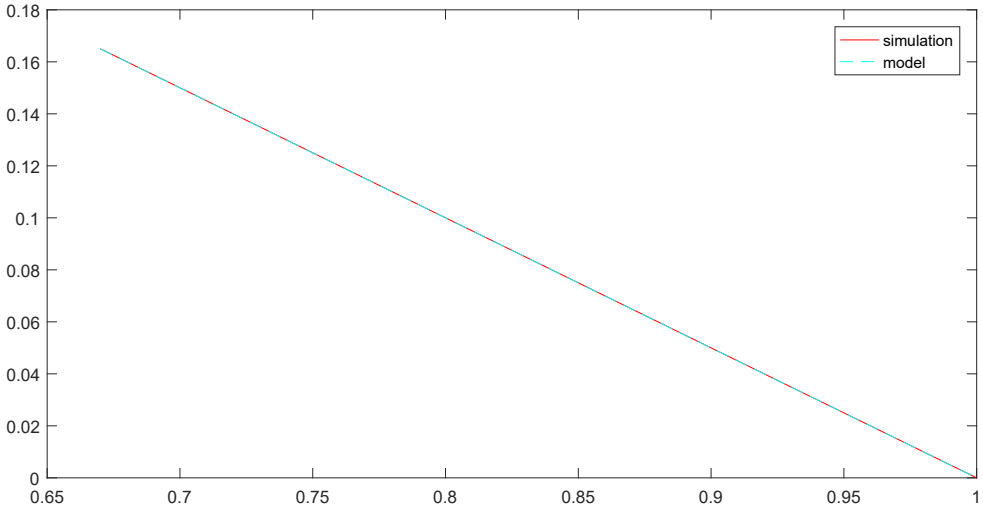


Figure 2.17: Static gain curves: model vs simulation

2.2.4 Dynamic model

The dynamic model is obtained assuming small signal conditions and neglecting the second order terms of the expression derived from the large signal model. In the signal flow graph in Fig. 2.18, the nodes represent the variation of the signals. As it can be seen, an additional node, the variation of the duty cycle $\hat{d}$, is present with respect to the other signal flow graphs. The transmittance of the branch exiting from it was calculated previously.
Like the static model, the small signal model is linear and Mason's gain formula can be applied. Superposition of effects can also be applied, so the variation of the input voltage $\hat{v}_{in}$ is set to zero and the ratio $\hat{v}_o/\hat{d}$ can be calculated. The node associated to the variation of the duty cycle $\hat{d}$ contains the factor -2. Consequently, to get the relation $\hat{v}_o/\hat{d}$, the ratio $\hat{v}_o/(-2\hat{d})$ obtained with Mason's gain formula should be multiplied by -2.

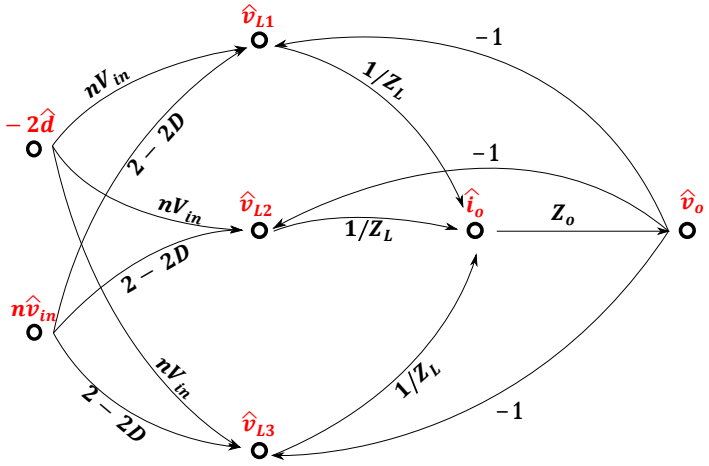


Figure 2.18: Small signal - signal flow graph

There are three identical loops, which are touching. Their gains are reported in equation 2.27.

$$T_1 = T_2 = T_3 = -\frac{Z_o}{Z_L} \tag{2.27}$$

The Delta of the graph is calculated from the loop gains and is reported in equation 2.28.

$$\Delta = 1 - (T_1 + T_2 + T_3) = 1 + \frac{3Z_o}{Z_L} \tag{2.28}$$

The gain of the three forward paths between input and output node and the delta of each path are reported respectively in equations 2.29 and 2.30.

$$H_i = (nV_{in})\,\frac{Z_o}{Z_L} \tag{2.29}$$

$$\Delta_i = 1 \tag{2.30}$$

The quantities just obtained before are used to get the control transfer function H.

$$H = -2\frac{\hat{v_o}}{-2\hat{d}} = -2\frac{\Sigma H_i \Delta_i}{\Delta} = -2\frac{3\,nV_{in}\frac{Z_o}{Z_L}}{1+\frac{3Z_o}{Z_L}} \tag{2.31}$$

Numerator and denominator of equation 2.31 are multiplied times the term $Z_L/\left(3Z_o\right)$ to obtain equation 2.32.

$$H = -2nV_{in}\frac{1}{1+3\frac{Z_L}{Z_o}} \tag{2.32}$$

The term $Z_L/\left(3Z_o\right)$ is developed in equation 2.33 and then substituted in equation 2.32 to obtain equation 2.34.

$$3\frac{Z_L}{Z_o} = 3\left(s\,L\right)\left(s\,C + \frac{1}{R}\right) = s\,\frac{3L}{C} + s^2\frac{LC}{3} \tag{2.33}$$

$$H = -2nV_{in}\frac{1}{1+s\,\frac{3L}{C}+s^2\frac{LC}{3}} \tag{2.34}$$

Figures of merit The most important figures of merit associated to the transfer functions are derived; they will be compared to the real converter model to evaluate the effect of non-idealities on the transfer function.

- **Dynamic gain**

$$H_o = -2n\,V_{in} \tag{2.35}$$

- **Poles frequency**

$$f_p = \frac{1}{2\pi\sqrt{\frac{LC}{3}}} \tag{2.36}$$

- **Quality factor**

$$Q = \frac{R}{\sqrt{\frac{L}{3C}}} \tag{2.37}$$

Comparison with simulations As for the static model case, simulations results have been compared to the model. Again, the model and the simulation curves perfectly overlap.

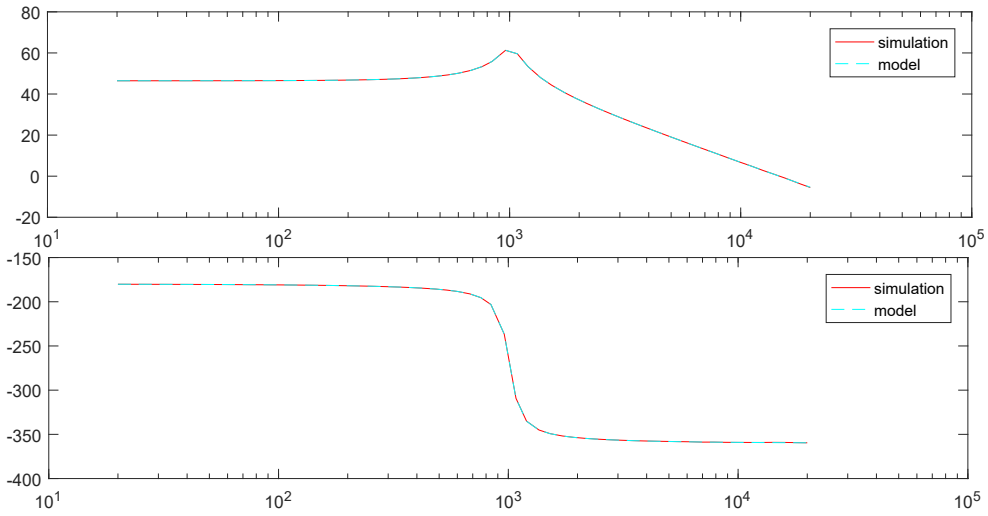


Figure 2.19: Dynamic behavior: model vs simulation

2.3 Complete converter model

The complete converter model is here finally analyzed. The circuit under analysis takes into consideration the leakage inductances of the transformers.

The mathematical models of this converter will be derived as for the simplified converter and the most relevant figures of merit of the models will be compared with the ones of the simplified converter to evaluate the impact of the leakage inductances on the behavior of the circuit.

2.3.1 Building the switching flow graph

As for the simplified converter, the switching flow graph is obtained combining the signal flow graph associated to each stage.
Besides the signals present in the simplified converter graphs, the currents flowing through the inductors are added (in the simplified converter model, they were implicitly summed in in the output current node). There are no nodes associated to the leakage inductance itself; its effect is considered in the branches that enter inductors' voltages nodes, allowing for a more compact SFG.
The signals present in the graphs are reported in Fig. 2.20.

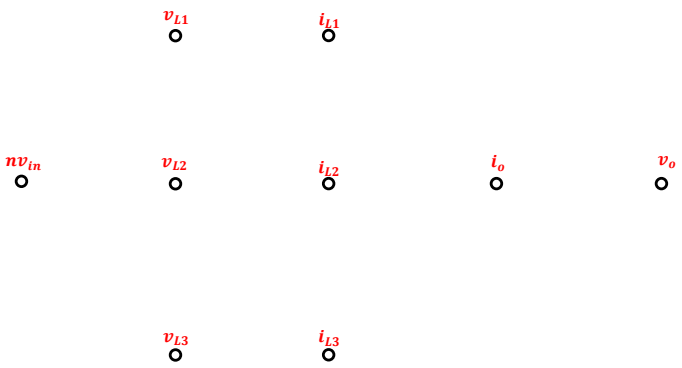


Figure 2.20: Signals - signal flow graph

Stage 1 Like in the simplified converter, during stage 1 the high-side transistors conduct and the input voltage is not transferring energy to the output. The presence of the leakage inductances however makes the voltage at the primary side of the transformers non-zero. The voltage across the leakage inductance is equal to the primary side voltage with negative sign, as reported in equations 2.38 AND 2.39.
The voltage across the secondary side of section A is equal to the secondary

side of section B; the voltage across the secondary side of section C is twice the voltage across the secondary side of section A with negative sign, as shown in equation 2.40.

$$v_{pA} = -v_{LdA} = -sL_d i_{pA} = -sL_d n i_{sA} \tag{2.38}$$

$$v_{pB} = -v_{LdB} = -sL_d i_{pB} = -sL_d n i_{sB} \tag{2.39}$$

$$v_{sC} = -2v_{sA} = -2v_{sB} \tag{2.40}$$

The voltage across the secondary side of the transformers is equal to the voltage on the primary side times the turns ratio.

$$v_s = nv_p \tag{2.41}$$

The voltage across inductors L_1 and L_2 are derived from the previous equations.

$$v_{L1} = -v_o - v_{sC} + v_{sA} = -v_o + 3v_{sA} = -v_o + 3nv_{pA} = -v_o - 3n^2\, sL_d i_{L1} \tag{2.42}$$

$$v_L = -v_o - v_{sC} + v_{sB} = -v_o + 3v_{sB} = -v_o + 3nv_{pB} = -v_o - 3n^2\, sL_d i_{L2} \tag{2.43}$$

The term $-3n^2\, sL_d$, present in equations 2.42 and 2.43, will be referred to as the leakage impedance A_{Ld}, as shown in equation 2.44.

$$Z_{Ld} = -3n^2\, sL_d \tag{2.44}$$

The following equations are derived from the previous considerations:

- inductors voltages

$$v_{L1} = -v_o + Z_{Ld}\, i_{L1}$$

$$v_{L2} = -v_o + Z_{Ld}\, i_{L2}$$

$$v_{L3} = -v_o$$

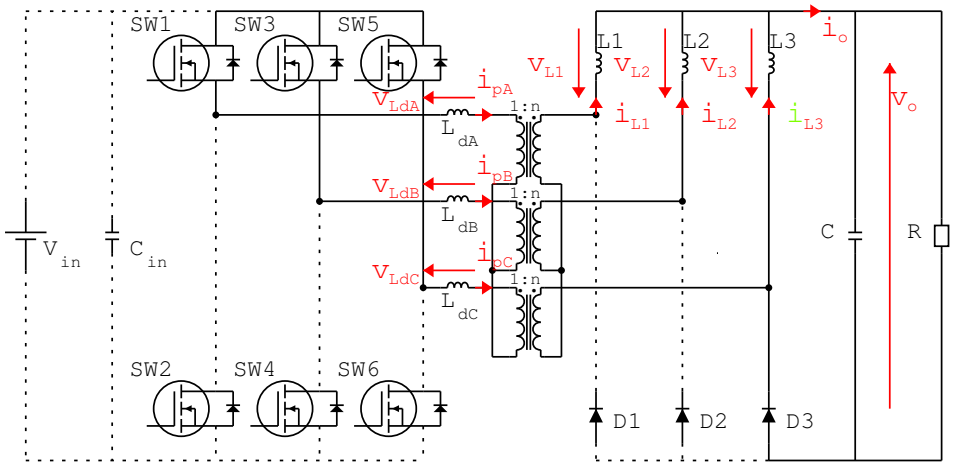


Figure 2.21: Stage 1 - schematic

- inductors currents

$$i_{L1} = v_{L1}\frac{1}{Z_L}$$
$$i_{L2} = v_{L2}\frac{1}{Z_L}$$
$$i_{L3} = v_{L3}\frac{1}{Z_L}$$

- output current

$$i_o = i_{L1} + i_{L2} + i_{L3} = (v_{L1} + v_{L2} + v_{L3})\frac{1}{Z_L}$$

- output voltage

$$i_o = Z_o v_o$$

The switching function k_1 associated to stage 1 is reported in equation 2.45 and its large signal value is $d - 2/3$.

$$k_1 = \begin{cases} 1, & t_0 < t < t_1 \\ 0, & t_1 < t < t_3 \end{cases} \tag{2.45}$$

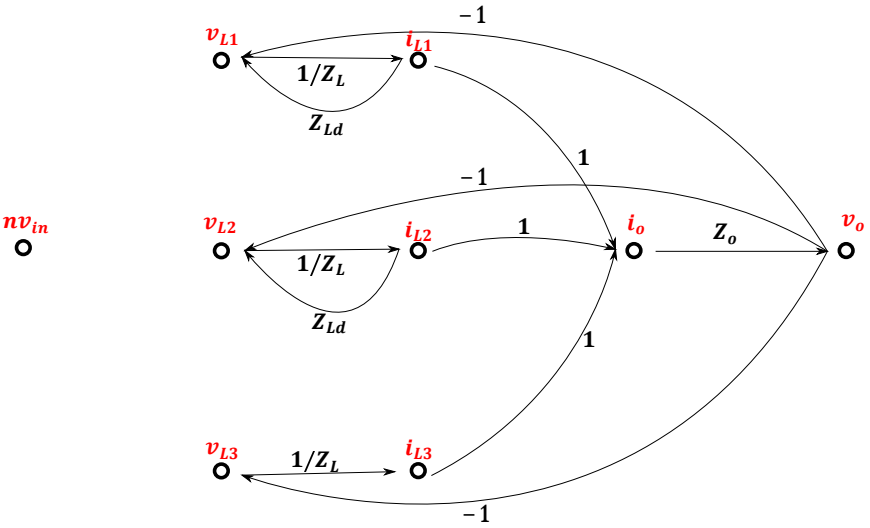


Figure 2.22: Stage 1 - signal flow graph

Stage 2 When transistor SW_2 is turned on, stage 2 begins. Diode D_1 starts conducting and the current in it increases, while current in diode D_3 decreases.
As it was introduced previously, the voltage at the star-center is $(2/3)\,V_{in}$, so the voltage across the leakage inductance L_{dB} and the primary side of section VB v_{sB} is $(1/3)\,V_{in}$, as shown in equation 2.46.
The voltage across the secondary side of section A is equal to the secondary side of section C; the voltage across the secondary side of section B is twice the voltage across the secondary side of section B with negative sign, as shown in equation 2.47.

$$v_{pB} = \frac{1}{3}v_{in} - v_{LdB} = \frac{1}{3}v_{in} - sL_d i_{LdB} = \frac{1}{3}v_{in} - sL_d n i_{sB} \tag{2.46}$$

$$v_{sA} = v_{sC} = -\frac{1}{2}v_{sB} \tag{2.47}$$

The voltage across the secondary side of the transformers is equal to the voltage on the primary side times the turns ratio.

$$v_s = nv_p \tag{2.48}$$

The voltage across inductor L_2 is derived from the previous equations.

$$v_{L2} = -v_o - v_{sC} + v_{sB} = -v_o + \frac{3}{2}v_{sB} = -v_o + \frac{3}{2}nv_{pB} =$$

$$= -v_o + \frac{3}{2}n\left(\frac{1}{3}v_{in} - sL_d n i_{sB}\right) = -v_o + \frac{1}{2}nv_{in} - \frac{1}{2}3n^2 sL_d i_{sB} \qquad (2.49)$$

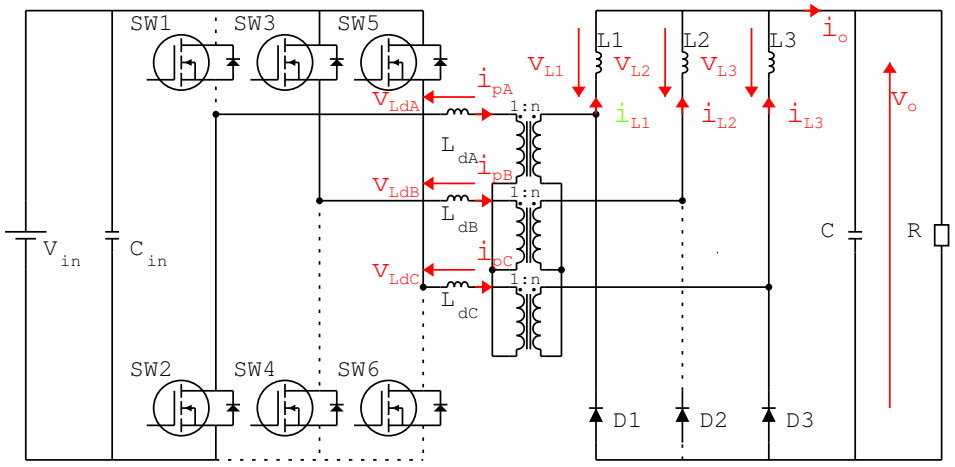


Figure 2.23: Stage 2 - schematic

The following equations are derived from the previous considerations:

- inductors voltages

$$v_{L1} = -v_o$$

$$v_{L2} = -v_o + \frac{1}{2}v_{in} + \frac{1}{2}Z_{Ld}\, i_{L2}$$

$$v_{L3} = -v_o$$

- inductors currents

$$i_{L1} = v_{L1}\frac{1}{Z_L}$$

$$i_{L2} = v_{L2}\frac{1}{Z_L}$$

$$i_{L3} = v_{L3}\frac{1}{Z_L}$$

- output current

$$i_o = i_{L1} + i_{L2} + i_{L3} = (v_{L1} + v_{L2} + v_{L3}) \frac{1}{Z_L}$$

- output voltage

$$i_o = Z_o v_o$$

The switching function k_2 associated to stage 2 is reported in equation 2.50 and its large signal value is $2\, i_o'$.

$$k_2 = \begin{cases} 1, & t_1 < t < t_2 \\ 0, & t_0 < t < t_1 \mathrm{V} t_2 < t < t_3 \end{cases} \tag{2.50}$$

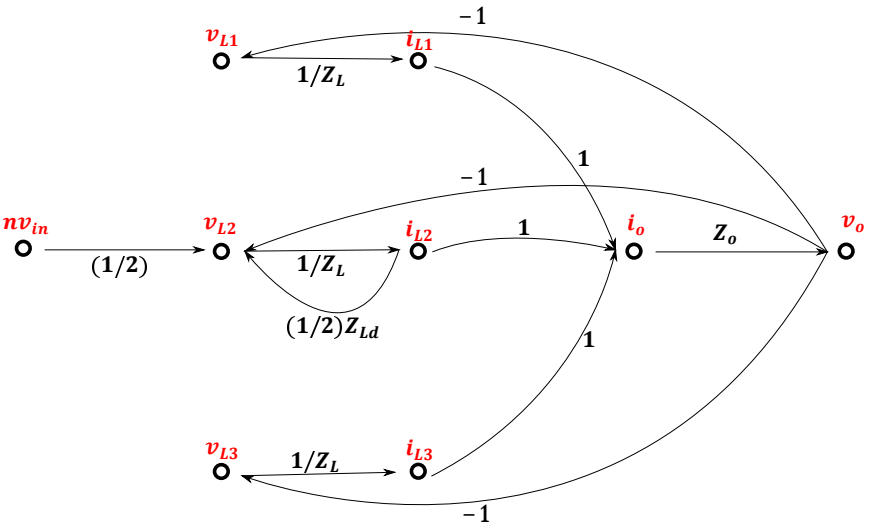


Figure 2.24: Stage 2 - signal flow graph

Stage 3 When stage 2 ends, stage 3 begins Diode D_3 does not conduct antmore, so diode D_1 is the only diode conducting.

$$v_{pB} = \frac{1}{3} v_{in} - v_{LdB} = \frac{1}{3} v_{in} - sL_d i_{LdB} = \frac{1}{3} v_{in} - sL_d n i_{sB} \tag{2.51}$$

$$v_{pC} = \frac{1}{3}v_{in} - v_{LdC} = \frac{1}{3}v_{in} - sL_d i_{LdC} = \frac{1}{3}v_{in} - sL_d n i_{sC} \tag{2.52}$$

$$v_{sB} = v_{sC} = -\frac{1}{2}v_{sA} \tag{2.53}$$

The voltage across the secondary side of the transformers is equal to the voltage on the primary side times the turns ratio.

$$v_s = nv_p \tag{2.54}$$

The voltage across inductor L_2 is derived from the previous equations.

$$\begin{aligned} v_{L2} &= -v_o - v_{sA} + v_{sB} = -v_o + 3v_{sB} = -v_o + 3nv_{pB} = \\ &= -v_o + 3n\left(\frac{1}{3}v_{in} - sL_d n i_{sB}\right) = -v_o n v_{in} - 3n^2 sL_d i_{sB} \end{aligned} \tag{2.55}$$

$$\begin{aligned} v_{L3} &= -v_o - v_{sA} + v_{sC} = -v_o + 3v_{sC} = -v_o + 3nv_{pC} = \\ &= -v_o + 3n\left(\frac{1}{3}v_{in} - sL_d n i_{sC}\right) = -v_o n v_{in} - 3n^2 sL_d i_{sC} \end{aligned} \tag{2.56}$$

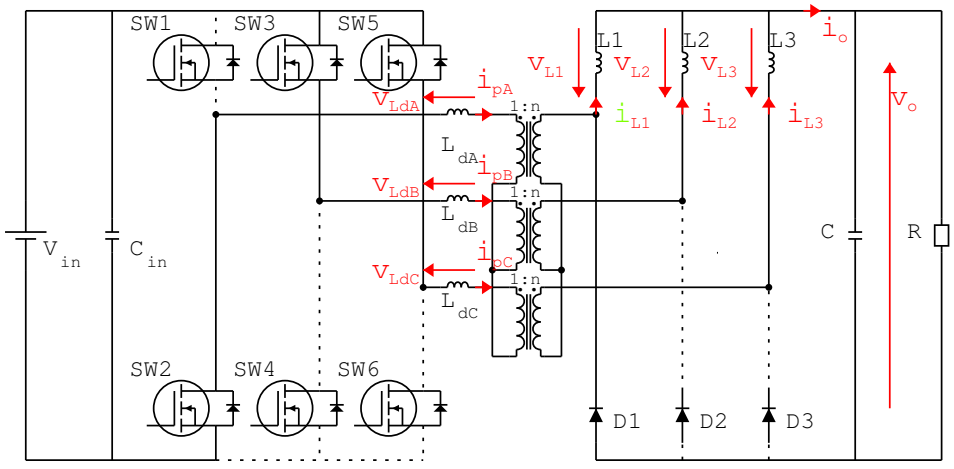


Figure 2.25: Stage 3 - schematic

The following equations are derived from the previous considerations:

- inductors voltages

$$v_{L1} = -v_o$$
$$v_{L2} = -v_o + nv_{in} + Z_{Ld}\, i_{L2}$$
$$v_{L3} = -v_o + nv_{in} + Z_{Ld}\, i_{L3}$$

- inductors currents

$$i_{L1} = v_{L1}\frac{1}{Z_L}$$
$$i_{L2} = v_{L2}\frac{1}{Z_L}$$
$$i_{L3} = v_{L3}\frac{1}{Z_L}$$

- output current

$$i_o = i_{L1} + i_{L2} + i_{L3} = (v_{L1} + v_{L2} + v_{L3})\,\frac{1}{Z_L}$$

- output voltage

$$i_o = Z_o v_o$$

The switching function k_3 associated to stage 3 is reported in equation 2.57 and its large signal value is $1 - d - 2\, i'_o$.

$$k_3 = \begin{cases} 1, & t_2 < t < t_3 \\ 0, & t_0 < t < t_2 \end{cases} \tag{2.57}$$

Switching flow graph Like in the simplified converter model, the switching flow graph of the sub-cycle associated to section A only was built, and the switching flow graphs associated to sections B and C can be derived directly from it.
There are five switching branches. Two branches connect the input voltage to inductors' voltages. In section A, the branch $nV_{in} \rightarrow v_{L2}$ is associated to the switching function $(1/2)k_2 + k_3$ and the branch $nV_{in} \rightarrow v_{L3}$ is associated to the switching function k_3. As a consequence, in section B the branch $nV_{in} \rightarrow v_{L3}$ is associated to the switching function $(1/2)k_2 + k_3$ and the branch $nV_{in} \rightarrow v_{L1}$ is associated to the switching function k_3. Finally,

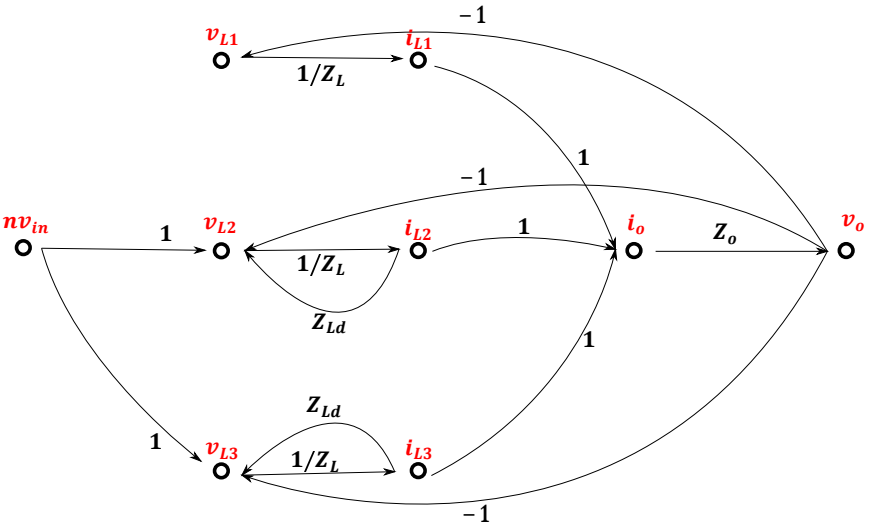


Figure 2.26: Stage 3 - signal flow graph

in section C the branch $nV_{in} \rightarrow v_{L1}$ is associated to the switching function $(1/2)k_2 + k_3$ and the branch $nV_{in} \rightarrow v_{L2}$ is associated to the switching function k_3.
A similar operation can be done for the switching branches that connect inductors' currents to inductors' voltages.
Fig. 2.27 reports the switching flow graph associated to section A; the large signal value of the switching functions k_1, k_2 and k_3 are reported in equations 2.58, 2.59 and 2.59.

$$k_1 = d - \frac{2}{3} \tag{2.58}$$

$$k_2 = 2i'_o \tag{2.59}$$

$$k_3 = 1 - d - 2i'_o \tag{2.60}$$

As it can be seen in the final graph reported in Fig. 2.28, the switching function of the branch $nv_{in} \rightarrow v_L$ is $(1/2)k_2 + 2k_3$, whereas the switching function of the branch $i_L \rightarrow v_L$ is $2k_1 + (1/2)k_2 + 2k_3$.
Their large signal values are reported in equations 2.61 and 2.62.

$$\frac{1}{2}k_2 + 2k_3 = \frac{1}{2}(2i'_o) + 2(1 - d - 2i'_o) = 2 - 2d - 3i'_o \tag{2.61}$$

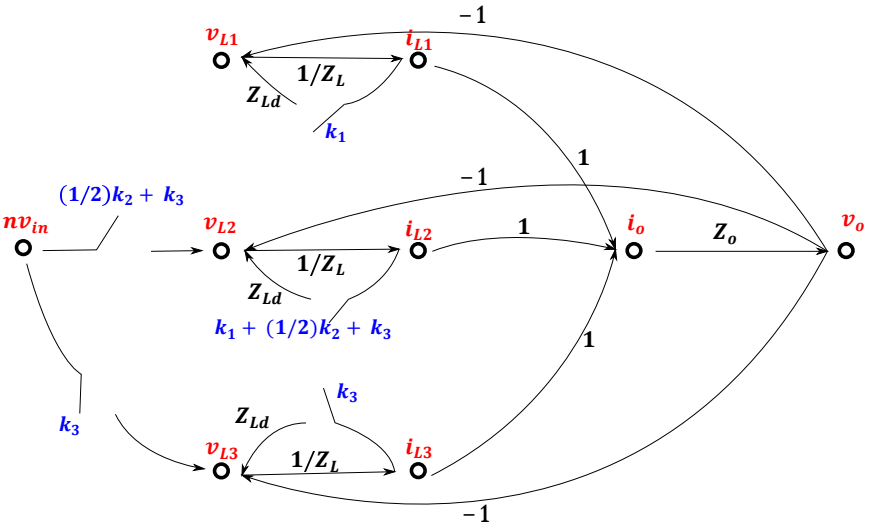


Figure 2.27: Switching flow graph - one section

$$2k_1 + \frac{1}{2}k_2 + 2k_3 = 2\left(d - \frac{2}{3}\right) + \frac{1}{2}\left(2i'_o\right) + 2\left(1 - d - 2i'_o\right) = \frac{2}{3} - 3i'_o \quad (2.62)$$

2.3.2 Large signal model and linearization

Starting from the complete switching flow graph just presented, the large signal model can be derived.
Like in the simplified converter case, the most tricky node is inductor's voltage. The large signal values of the switching functions just obtained are used to write down the large signal value of inductors' voltages and derive steady state and small signal models from it.
Since the equations and the graphs are already complicated, the input voltage is assumed constant, so its variation $\hat{v}_{in}$ is set to zero.

Starting from the large signal value of the switching functions derived in equations 2.61 and 2.62, the large signal value of inductor's voltage is derived in equation 2.63.

$$v_L = -v_o + i_L Z_{Ld}\left(\frac{2}{3} - 3i'_o\right) + \left(2 - 2d - 3i'_o\right) nV_{in} \quad (2.63)$$

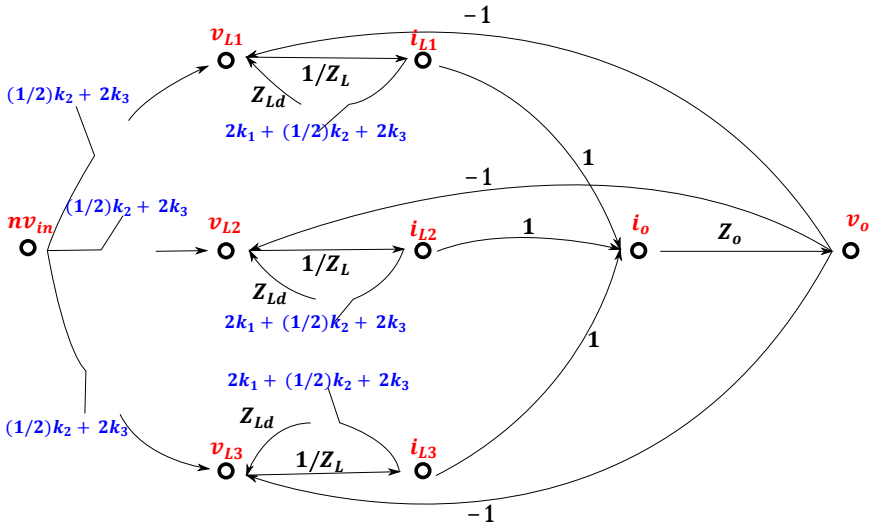


Figure 2.28: Switching flow graph - three sections

Assuming small signal conditions, each signal can be represented by the sum of its DC component and its variation:

- Output voltage
$$v_o = V_o + \hat{v}_o$$
- Normalized current
$$i'_o = I'_o + \hat{i}'_o$$
- Inductor current
$$i_L = I_L + \hat{i}_L$$
- Inductor voltage
$$v_L = V_L + \hat{v}_L$$
- Duty cycle
$$d = D + \hat{d}$$

The expression of v_L is then rewritten in equation 2.64.

$$V_L + \hat{v}_L = -V_o - \hat{v}_o + \left(I_L + \hat{i}_L\right) Z_{Ld} \left(\frac{2}{3} - 3I'_o - 3\hat{i}'_o\right) + \left(2 - 2D - 2\hat{d} - 3I'_o - 3\hat{i}'_o\right) nV_{in} \tag{2.64}$$

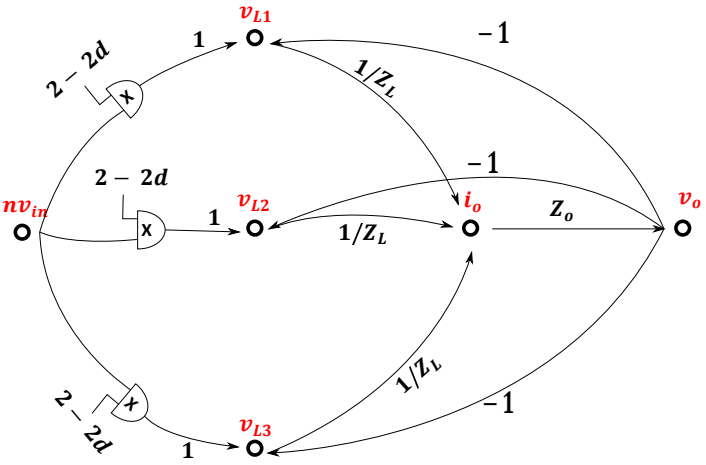


Figure 2.29: Large signal - signal flow graph

All the products in equation 2.64 are developed in equation 2.65

$$V_L + \hat{v}_L = -V_o - \hat{v}_o + I_L Z_{Ld}\left(\frac{2}{3} - 3I'_o\right) + \hat{i}_L Z_{Ld}\left(\frac{2}{3} - 3I'_o\right) - 3\hat{i}'_o Z_{Ld} I_L$$
$$-3Z_{Ld}\hat{i}'_o\hat{i}_L + \left(2 - 2D - 2\hat{d} - 3I'_o\right) nV_{in} - 3nV_{in}\hat{i}'_o - 2\hat{d}nV_{in} \quad (2.65)$$

The DC component and the first order variations are separated. The second order term $-3Z_{Ld}\hat{i}'_o\hat{i}_L$ is neglected.

$$V_L = -V_o + I_L Z_{Ld}\left(\frac{2}{3} - 3I'_o\right) + (2 - 2D - 3I'_o)\, nV_{in} \quad (2.66)$$

$$\hat{v}_L = -\hat{v}_o + \hat{i}_L Z_{Ld}\left(\frac{2}{3} - 3I'_o\right) - 3\hat{i}'_o\left(Z_{Ld} I_L + nV_{in}\right) - 2\hat{d}nV_{in} \quad (2.67)$$

The variation of the normalized current can be rewritten as a function of the variation of the output current, as shown in equation 2.68.

$$\hat{i}'_o = \hat{i}_o \frac{nf_S L_d}{V_{in}} \quad (2.68)$$

The final expression of the variation of inductor's voltage is finally reported in equation

$$\hat{v}_L = -\hat{v}_o + \hat{i}_L Z_{Ld}\left(\frac{2}{3} - 3I'_o\right) - 3\hat{i}_o \frac{nf_S L_d}{V_{in}}\left(Z_{Ld} I_L + nV_{in}\right) - 2\hat{d}nV_{in} \quad (2.69)$$

2.3.3 Static model

As it was explained in the first chapter, impedances can be replaced by the resistances in the static model ot the limit for s approaching zero can be calculated on the final expression.
In the case of the complete converter, the second solution is used and the signal flow graph associated to it is reported in Fig. 2.30.

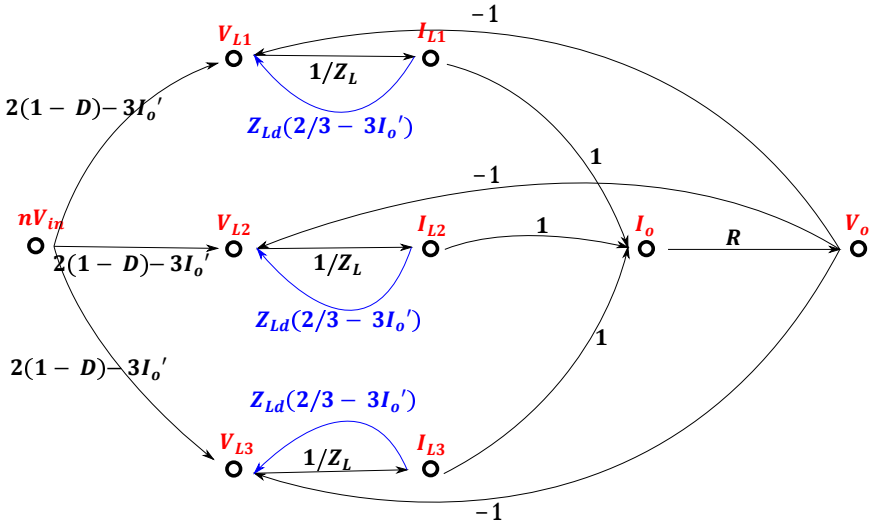


Figure 2.30: Steady state - signal flow graph

There are three touching loops in the path of the nodes $V_o \rightarrow V_{Li} \rightarrow I_{Li} \rightarrow I_o \rightarrow V_o$; the subscript i is associated to the sections A, B and C. They have the same loop gain T_1, which is indicated in equation 2.70.

$$T_1 = -\frac{R}{Z_L} \tag{2.70}$$

There are also three loops which are non-touching with each other, but are touching with the loops T_1; their path is $V_{Li} \rightarrow I_{Li} \rightarrow V_{Li}$. They all have the same gain T_2, which is reported in equation 2.71. As it can be seen from the graph, the transmittance of these branches still contain impedances, but their ratio is a finite number, as reported in equation 2.71.

$$T_2 = \frac{(2/3 - 3I_o')\, Z_{Ld}}{Z_L} = \frac{(2/3 - 3I_o')\,(-3n^2 s L_d)}{sL} = (2/3 - 3I_o')\left(-3n^2 \frac{L_d}{L}\right) \tag{2.71}$$

The Delta of the graph is calculated from them:

$$\Delta = 1 - 3T_1 - 3T_2 + 3T_2^2 \tag{2.72}$$

The gain of the three forward paths between input and output node and the delta associated to each path are calculated in equations. For a amore compact form, the ratio R/Z_L is expressed as $-T_1$, from equation 2.70.

$$M_i = (2 - 2D - 3I_o') \frac{R}{Z_L} = (2 - 2D - 3I_o')(-T_1) \tag{2.73}$$

$$\Delta_i = 1 - 2T_2 + T_2^2 = (1 - T_2)^2 \tag{2.74}$$

The quantities obtained before are then used to get the final formula of the static gain:

$$M = n\frac{V_o}{nV_{in}} = n\frac{\Sigma M_i \Delta_i}{\Delta} = n\frac{3\,(2 - 2D - 3I_o')(-T_1)(1 - T_2)^2}{1 - 3T_1 - 3T_2 - 3T_2^2} \tag{2.75}$$

Multiplying by $1/T_1$ both numerator and denominator of equation 2.75, equation 2.76 is obtained.

$$\begin{aligned} M &= n\frac{3\,(2 - 2D - 3I_o')(-T_1)(1 - T_2)^2 (1/T_1)}{(1 - 3T_1 - 3T_2 - 3T_2^2)(1/T_1)} = \\ &= n\frac{3\,(2 - 2D - 3I_o')(1 - T_2)^2}{(-1/T_1 + 3 + 3T_2/T_1 - 3T_2^2/T_1)(1/T_1)} \end{aligned} \tag{2.76}$$

Since the loop gain T_2 does not depend on 's' and the quantity $1/T_1 \to 0$ when $s \to 0$, it is possible to calculate the limit of equation 2.76.

$$M = n\frac{3\,(2 - 2D - 3I_o')(1 - T_2)^2}{(-1/T_1 + 3 + 3T_2/T_1 - 3T_2^2/T_1)(1/T_1)}\bigg|_{s\to 0}$$

$$M = n\frac{3\,(2 - 2D - 3I_o')(1 - T_2)^2}{3} = n\,(2 - 2D - 3I_o')(1 - T_2)^2 \tag{2.77}$$

Since the loop gain T_2 is typically small with respect to 1, the term $(1 - T_2)^2$can be neglected and the formula of the static gain M is finally reported in 2.78.

$$M = n\,(2 - 2D - 3I_o') \tag{2.78}$$

Comparison with simulations The circuit was simulated on the software PSIM. The static behavior was simulated with constant output current, in order to have constant parameterized current. To do that, the load resistance was then substituted with a current generator. The frequency response of the new circuit is different, but the steady state is not.
It can be easily seen that the curves do not overlap perfectly as in the leakage-less converter, even if the model of the components used in the simulation is ideal (e.g. zero voltage drop across a conducting diode). Such error is due to the intrinsic non-linearity of the mathematical model. However, such error is relatively low.
The leakage-less converter curve has been drawn too; it represents the upper limit of all the characteristics, in fact it is the curve that corresponds to $I'_o = 0$.

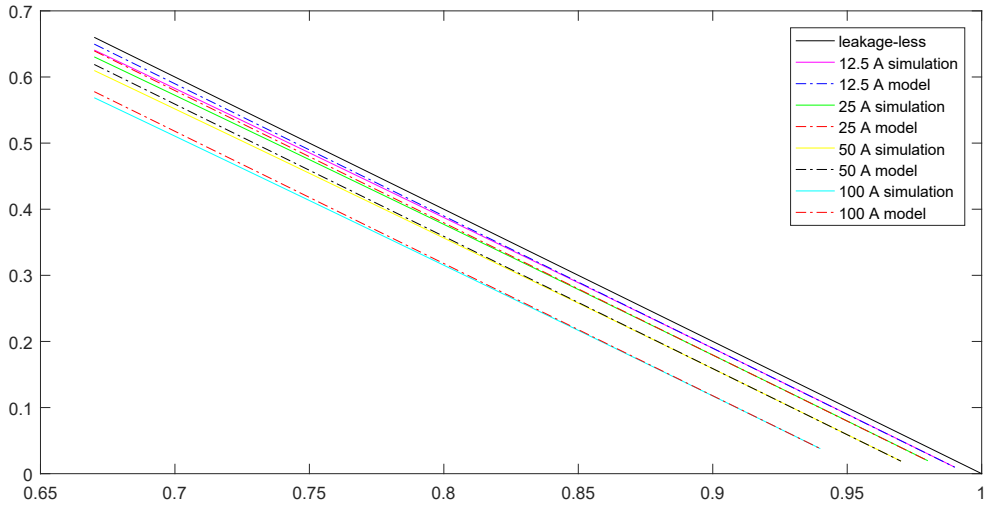


Figure 2.31: Static gain curves: model vs simulation

2.3.4 Dynamic model

As it was mentioned in the simplified converter, the small signal model is linear and superposition of effects can be applied. The variation of the input voltage is therefore set to zero and the transfer function $\hat{v}_o/\hat{d}$ is calculated.
To make the signal flow graph easier to read, the variation of the input

voltage $\hat{v}_{in}$ is not represented. Fig. 2.32 reports the small signal model of the complete converter.

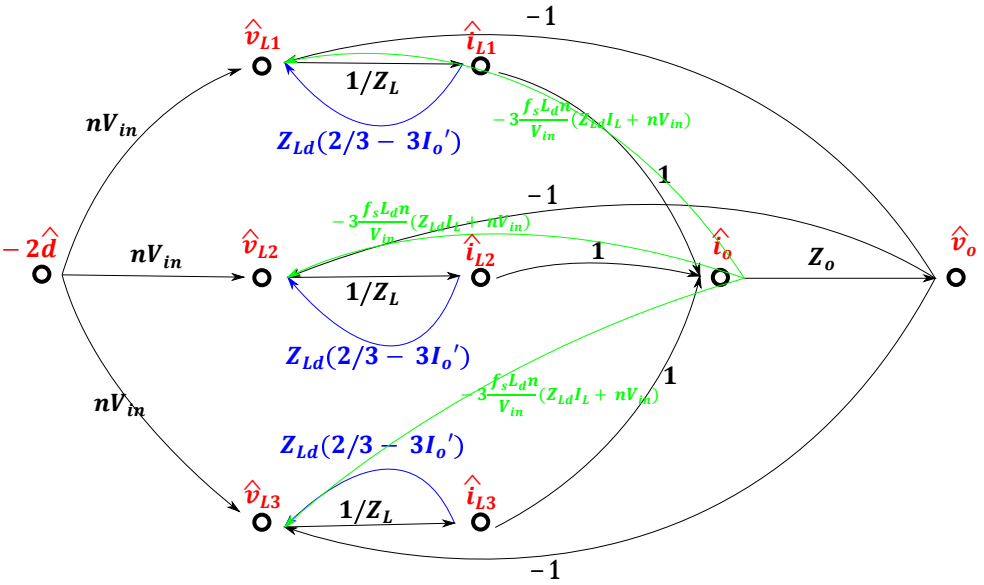


Figure 2.32: Small signal - signal flow graph

Mason's formula can be again exploited to derive the transfer function $\hat{v}_o/\hat{d}$.
There are three kind of loops and the feedback branches of each of them has a different color.
T_1's feedback branch is black and its path is $\hat{v}_o \to \hat{v}_{Li} \to \hat{i}_{Li} \to \hat{i}_o \to \hat{v}_o$; its gain is reported in equation 2.79.
T_2's feedback branch is blue and its path is $\hat{v}_{Li} \to \hat{i}_{Li} \to \hat{v}_{Li}$; its gain is reported in equation 2.80.
T_3's feedback branch is green and its path is $\hat{i}_o \to \hat{v}_{Li} \to \hat{i}_{Li} \to \hat{i}_o$; its gain is reported in equation 2.81.

$$T_1 = -\frac{Z_o}{Z_L} \tag{2.79}$$

$$T_2 = \frac{(2/3 - 3I_o')\, Z_{Ld}}{Z_L} = \frac{(2/3 - 3I_o')\,(-3n^2 s L_d)}{sL} = (2/3 - 3I_o')\left(-3n^2 \frac{L_d}{L}\right) \tag{2.80}$$

$$T_3 = -\frac{3\frac{n\,f_S L_d}{V_{in}}\left(Z_{Ld}\,I_L + nV_{in}\right)}{Z_L} = -\frac{3\frac{n\,f_S L_d}{V_{in}}\left(Z_{Ld}\,\frac{V_o}{3R} + nV_{in}\right)}{Z_L} \tag{2.81}$$

Where I_L is the DC value of inductor's current. Equation 2.82 gives a good estimation of it.

$$I_L \approx \frac{I_o}{3} = \frac{V_o}{3R} \tag{2.82}$$

The delta of the graph is reported in equation 2.83, whereas the forward path and the delta associated to it are reported in equations 2.84 and 2.85 respectively.

$$\Delta = 1 - (3T_1 + 3T_2 + 3T_3) + (6T_1T_2 + 6T_2T_3 + 3T_2^2) - T_2^3 \tag{2.83}$$

$$M_i = -2nV_{in}\frac{Z_o}{Z_L} \tag{2.84}$$

$$\Delta_i = 1 - 2T_2 + T_2^2 \tag{2.85}$$

Subsituting equations 2.83, 2.84 and 2.85 in Mason's gain formula, the transfer function is derived.

$$H = \frac{\hat{v}_o}{\hat{d}} = \frac{3\left(-2nV_{in}\frac{Z_o}{Z_L}\right)(1 - 2T_2 + T_2^2)}{1 - (3T_1 + 3T_2 + 3T_3) + (6T_1T_2 + 6T_2T_3 + 3T_2^2) - T_2^3} \tag{2.86}$$

Multiplying by Z_L/Z_o both numerator and denominator of equation 2.86, the expression of the transfer function can be simplified.

$$H = \frac{\hat{v}_o}{\hat{d}} = \frac{3\left(-2nV_{in}\frac{Z_o}{Z_L}\right)(1 - T_2)^2}{1 - (3T_1 + 3T_2 + 3T_3) + (6T_1T_2 + 6T_2T_3 + 3T_2^2) - T_2^3}\,\frac{\frac{Z_L}{Z_o}}{\frac{Z_L}{Z_o}} =$$

$$= \frac{3\left(-2nV_{in}\right)(1 - T_2)^2}{\frac{Z_L}{Z_o} - \left(3T_1\frac{Z_L}{Z_o} + 3T_2\frac{Z_L}{Z_o} + 3T_3\frac{Z_L}{Z_o}\right) + \left(6T_1T_2\frac{Z_L}{Z_o} + 6T_2T_3\frac{Z_L}{Z_o} + 3T_2^2\frac{Z_L}{Z_o}\right) - T_2^3\frac{Z_L}{Z_o}} \tag{2.87}$$

Since T_1 depends on s^2, T_3 depends on s and T_2 is a number, the denominator is reorganized to make simplifications.

$$H = \frac{3\left(-2nV_{in}\right)\left(1-T_2\right)^2}{\frac{Z_L}{Z_o}\left(-3T_1+6T_1T_2\right)+\frac{Z_L}{Z_o}\left(-3T_3+6T_2T_3\right)+\frac{Z_L}{Z_o}\left(1-3T_2+3T_2^2-T_2^3\right)} =$$

$$= \frac{3\left(-2nV_{in}\right)\left(1-T_2\right)^2}{-3\frac{Z_L}{Z_o}T_1\left(1-2T_2\right)-3\frac{Z_L}{Z_o}T_3\left(1-2T_2\right)+\frac{Z_L}{Z_o}\left(1-T_2\right)^3} \tag{2.88}$$

Recalling that the loop gain $T_1 = -Z_o/Z_L$ and the loop gain $T_3 = -3\frac{n\,f_S L_d}{V_{in}}\left(Z_{Ld}\,\frac{V_o}{3R}+nV_{in}\right)/Z_L$, equations 2.89 and 2.90 are derived. In the last expression, the ratio V_o/V_{in} is substituted by the static gain M.

$$-3\frac{Z_L}{Z_o}T_1 = -3\frac{Z_L}{Z_o}\left(-\frac{Z_o}{Z_L}\right) = 3 \tag{2.89}$$

$$-3\frac{Z_L}{Z_o}T_3 = -3\frac{Z_L}{Z_o}\left(-\frac{3\frac{n\,f_S L_d}{V_{in}}\left(Z_{Ld}\,\frac{V_o}{3R}+nV_{in}\right)}{Z_L}\right) =$$

$$= 3\frac{1}{Z_o}\left(3\frac{n\,f_S L_d}{V_{in}}\left(Z_{Ld}\,\frac{V_o}{3R}+nV_{in}\right)\right) = 3\frac{1}{Z_o}\left(\frac{n\,f_S L_d M Z_{Ld}}{R}+3n^2 f_S L_d\right) \tag{2.90}$$

Equations 2.89 and 2.90 can be now substituted in 2.88.

$$H = \frac{3\left(-2nV_{in}\right)\left(1-T_2\right)^2}{3\left(1-2T_2\right)+3\frac{1}{Z_o}\left(\frac{n\,f_S L_d M Z_{Ld}}{R}+3n^2 f_S L_d\right)\left(1-2T_2\right)+\frac{Z_L}{Z_o}\left(1-T_2\right)^3} \tag{2.91}$$

Both numerator and denominator of equation 2.91 are now divided by $(1-T_2)^2$.

$$H = \frac{3\left(-2nV_{in}\right)\left(1-T_2\right)^2}{3\left(1-2T_2\right)+3\frac{1}{Z_o}\left(\frac{n\,f_S L_d M Z_{Ld}}{R}+3n^2 f_S L_d\right)\left(1-2T_2\right)+\frac{Z_L}{Z_o}\left(1-T_2\right)^3}\,\frac{\frac{1}{(1-T_2)^2}}{\frac{1}{(1-T_2)^2}}$$

$$H = \frac{3\left(-2nV_{in}\right)}{3\frac{(1-2T_2)}{(1-T_2)^2}+3\frac{1}{Z_o}\left(\frac{n\,f_S L_d M Z_{Ld}}{R}+3n^2 f_S L_d\right)\frac{(1-2T_2)}{(1-T_2)^2}+\frac{Z_L}{Z_o}\left(1-T_2\right)} \tag{2.92}$$

Up to this point no approximation has been made. Moreover, impedances are general, so possible parasitic elements can be included in their expressions. The static gain M is present in the formula. For sake of simplicity, it is approximated with the static gain of the simplified converter $M = 2 - 2D$. The value of the loop gain T_2 depends on the steady state value of normalized current I'_o, which can be rewritten as reported in equation 2.93.

$$I'_o = \frac{nf_S L_d I_o}{V_{in}} = \frac{nf_S L_d V_o}{V_{in} R} = \frac{nf_S L_d M}{R} \tag{2.93}$$

An additional approximation is made. Typically, the loop gain T_2 is much smaller than 1, so equations 2.94 and 2.95 acceptable.

$$1 - T_2 \approx 1 \tag{2.94}$$

$$1 - 2T_2 \approx 1 \tag{2.95}$$

Such approximation can be verified:

$$|T_2| << 1$$

$$\left| \frac{Z_{Ld}}{Z_L} \left(\frac{2}{3} - 3I'_o \right) \right| << 1$$

Since the quantity between parenthesis cannot be grater than 2/3, the following condition is derived:

$$\left| \frac{Z_{Ld}}{Z_L} \right| << 1$$

Applying finally the approximations introduced in 2.94 and 2.95 into equation 2.92, substituting equation 2.93 and dividing numerator and denominator by 3:

$$H = \frac{(-2nV_{in})}{1 + \frac{1}{Z_o}\left(3Z_{Ld}I'_o + 3n^2 f_S L_d\right) + \frac{Z_L}{3Z_o}} \tag{2.96}$$

The impedances of the inductors and of the RC parallel are then substituted.

$$H = \frac{-2nV_{in}}{1 + \left(sC + \frac{1}{R}\right)\left(-9n^2 sL_d I'_o M + 3n^2 f_S L_d\right) + s^2 \frac{LC}{3} + s\frac{L}{3R}} \tag{2.97}$$

$$H = n\frac{-2nV_{in}}{1 + 3\frac{n^2 f_S L_d}{R} + s\left(\frac{L}{3R} + 3n^2 f_S L_d C - 9\frac{n^2 L_d I'_o}{R}\right) + s^2\left(\frac{LC}{3} - 9n^2 L_d C I'_o M\right)} \tag{2.98}$$

Dividing both numerator and denominator by $1+3n^2\frac{f_S L_d}{R}$, the final equation is obtained.

$$H = \frac{-2nV_{in}/\left(1 + 3n^2\frac{f_S L_d}{R}\right)}{1 + s\frac{\left(\frac{L}{3R}+3n^2 f_S L_d C - 9\frac{n^2 L_d I'_o}{R}\right)}{1+3n^2\frac{f_S L_d}{R}} + s^2\frac{\left(\frac{LC}{3} - 9n^2 L_d C I'_o M\right)}{1+3n^2\frac{f_S L_d}{R}}} \tag{2.99}$$

Figures of merit The most important figures of merit associated to the transfer functions are derived; they will be compared to the real converter model to evaluate the effect of non idealities on the transfer function.

- **Dynamic gain**

$$H_o = \frac{-2n\,V_{in}}{1 + 3n^2\frac{f_S L_d}{R}} \tag{2.100}$$

- **Poles frequency**

$$f_p = \frac{1}{2\pi\sqrt{\frac{\left(\frac{LC}{3} - 9n^2 L_d C I'_o M\right)}{1+3n^2\frac{f_S L_d}{R}}}} \tag{2.101}$$

- **Quality factor**

$$Q = \sqrt{\frac{\left(\frac{\left(\frac{L}{3R}+3n^2 f_S L_d C - 9\frac{n^2 L_d I'_o}{R}\right)}{1+3n^2\frac{f_S L_d}{R}}\right)\left(1 + 3n^2\frac{f_S L_d}{R}\right)}{\left(\frac{LC}{3} - 9n^2 L_d C I'_o M\right)}} \tag{2.102}$$

Comparison with simulations Small signal simulations have been performed. The curves are a litle bit shifted, due to the small error in the static gain, but this difference remains the same throughout all the frequency range, meaning that the poles frequency is modeled correctly.

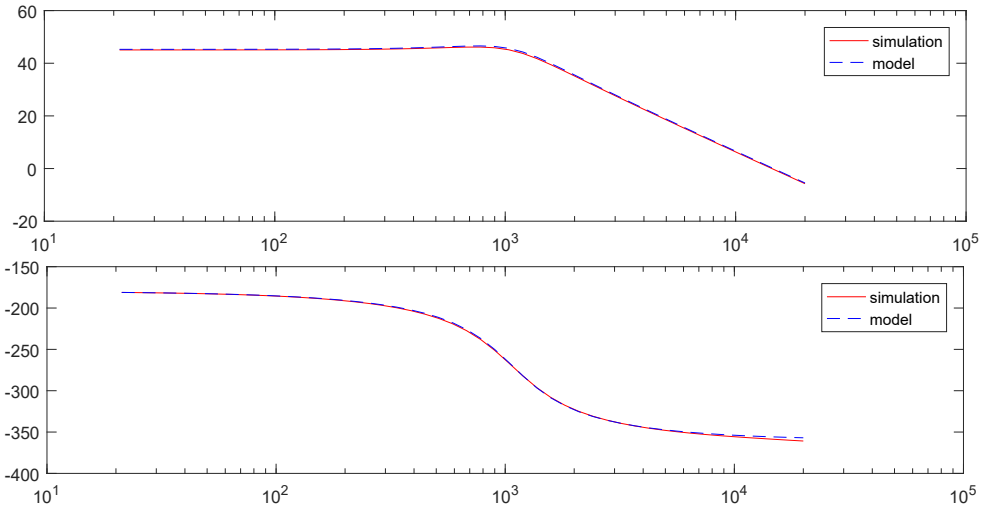


Figure 2.33: Dynamic behavior: model vs simulation

Chapter 3

Circuit design

3.1 Introduction

The mathematical models derived in the previous chapter can be verified building and testing a physical prototype; to design a physical circuit, current and voltage waveforms related to the components of the circuit mut be studied to derive parameters and stresses associated to each component.

3.1.1 Components' design parameters

The most relevant electrical parameters associated to each component are briefly listed.

Inductors

- maximum RMS current
- maximum peak current
- maximum ripple current
- inductance
- operating frequency

Output capacitor

- working voltage
- RMS current
- equivalent series resistance in case of an electrolytic capacitor
- capacitance in case of a ceramic capacitor
- Capacitance estimation for electrolytic

Input capacitor

- working voltage
- RMS current

MOSFET switch

- maximum blocking voltage
- ON resistance
- RMS current

Diode

- maximum reverse voltage
- peak current
- average current

Transformer

- RMS current
- turns ratio
- physical dimensions

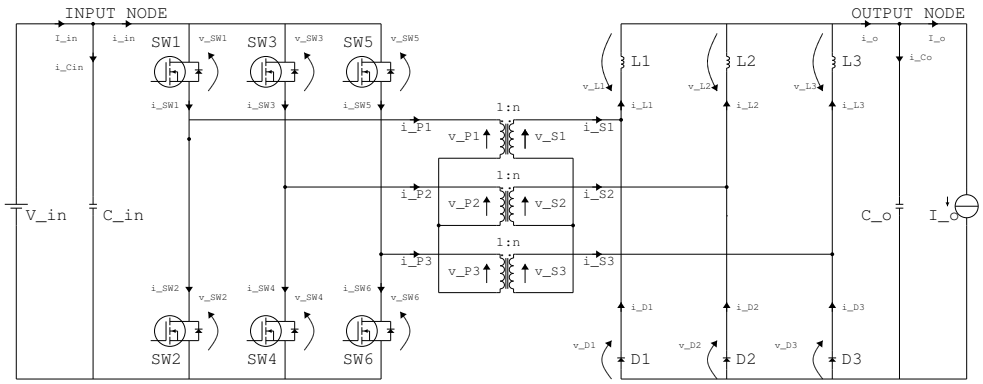


Figure 3.1: Schematic IDEAL

3.1.2 Reference schematics

The components present in the circuit may be grouped in to sets: the ones that provide DC-DC conversion, so basically switches, transformers, diodes, filter inductors and capacitors; and the ones needed to provide ZVS, so transformer's leakage inductances and transistors' parasitic capacitances, and the capacitors that are placed in series to the primary side of the transformers, which avoid core saturation of the transformers.
Two different schematics will be therefore used to study the behavior of the circuit:

Simplified converter It only contains components from the first set, so the ones responsible for DC-DC conversion; the analysis of the waveforms associated to the components of the first set will be referred to as this schematic.

Complete converter It contains all components and it will be used to design the remaining components; the results obtained from the analysis of schematic IDEAL will still be valid. As an example, the current at the primary side of the transformers is calculated from schematic IDEAL; the current flowing through the leakage inductance L_d is the primary side current, and the result obtained from schematic IDEAL will be used.

Components' values To make calculations easier, it is useful to consider each section of the circuit equal to the other ones; each section is composed

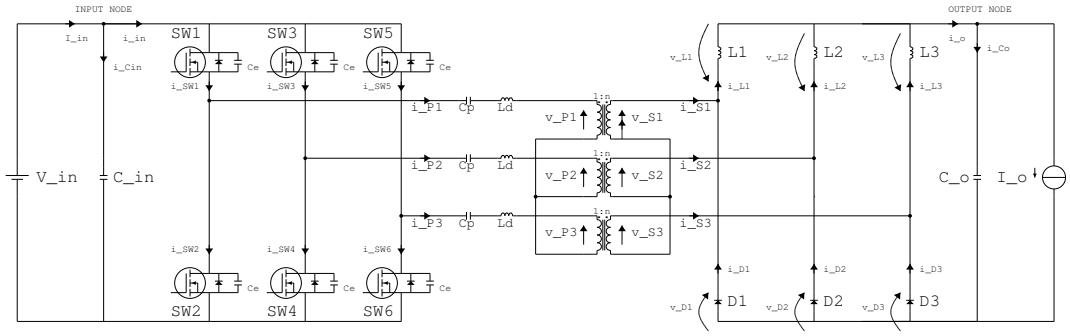


Figure 3.2: Schematic COMPLETE

by a cascade of a switch pair, a transformer and a diode-inductor rectifier. Each transformer is a $1 : n$ transformer, where:

- $n = \frac{N_S}{N_P}$ is the turns ratio
- N_S is the number of turns on the secondary side windings
- N_P is the number of turns on the primary side windings

The most relevant values are then:

- $\frac{N_{S1}}{N_{P1}} = \frac{N_{S2}}{N_{P2}} = \frac{N_{S3}}{N_{P3}} = n$
- $L1 = L2 = L3 = L$
- C_{in} is the capacitance of input's capacitor
- C_o is the capacitance of output's capacitor
- L_d is the value of transformers' leakage inductances
- C_e is the parasitic capacitance of transistors
- C_p is the capacitance of the primary-side capacitors

3.1.3 Test conditions

The mathematical models that have to be verified are the steady state voltage regulation factor (also called static gain) and the frequency response. Therefore, both static and dynamic measurements will be performed using an electronic load, which can behave as a constant current absorber or a resistance. The electronic load will be set to constant current when performing static measurements, whereas it will be set to resistance when performing dynamic measurements.

3.2 Converter's general design

As introduced previously, the waveforms of each component (currents and voltages vs time) must be studied.

Assumptions Before starting the analysis, it is important to define some assumptions which make the derivation of waveforms and equations easier:

1. Ideal components: components are ideal (e.g. diode forward voltage is zero); possible parasitic elements are considered only after the analysis is completed.

2. Time constant of the circuits are much bigger than the switching period: thanks to this assumption, reactive components do not resonate during the switching period.

3. Cyclostationary conditions: the circuit operates in regime condition, therefore waveforms are periodic.

4. Constant output voltage: typically, DC-DC converters must provide constant output voltage; therefore, the output voltage is considered constant with respect to the duty cycle and the ripple voltage is neglected.

Starting point All currents' waveforms in the circuits are derived from inductors' currents; to get those currents, the waveforms of the voltages across inductors must be found in the first place. One side of each inductor is connected to the output voltage. The other sides are connected to the secondary side of the transformers.

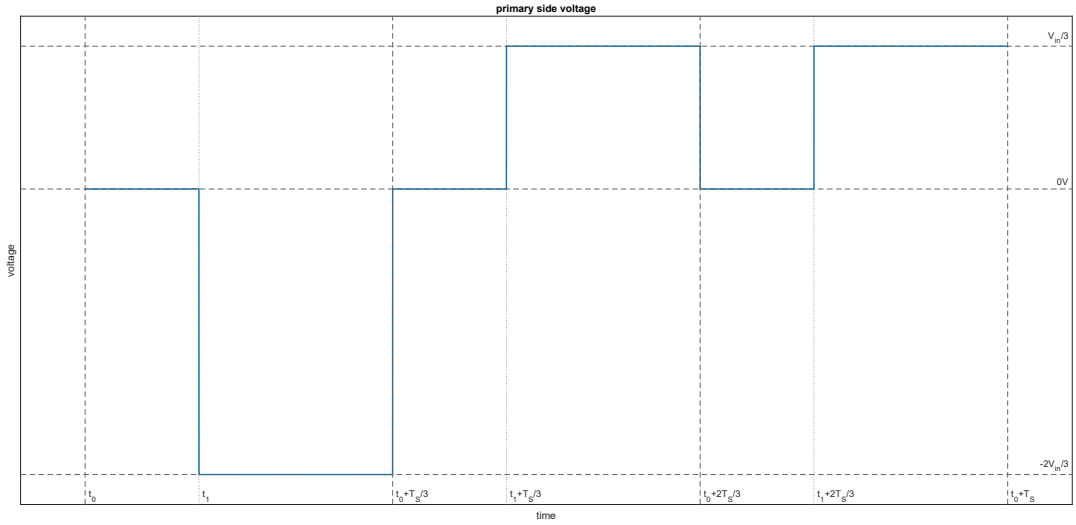


Figure 3.3: voltage on primary side

Considering the MOSFETs as ideal switches, voltages across the primary side of the transformers are easily derived: when all high-side switches are on, the voltage at the primary side is zero; when two high side switches are on and one low-side switch is on, the input voltage is divided on the primary sides.

The voltage applied to the primary side of transformer 1 is reported in figure (Fig.3.3).

3.2.1 Inductors

When the voltage applied to an ideal inductor is a rectangular periodic waveform, the current flowing through it is a periodic linear waveform, as it is shown in figures Fig. 3.4 and Fig.3.5; the slope of the current waveform is given by the ratio of the applied voltage and the inductance. Fig.3.6 reports the currents flowing through inductor L1 only; from now on, this is the reference waveform from which equations are derived.
The average of a linear periodic waveform is the arithmetic mean of the peak value and the bottom value, whereas the difference between those two values is the ripple.
Since the conditions just mentioned are true in this analysis, the following

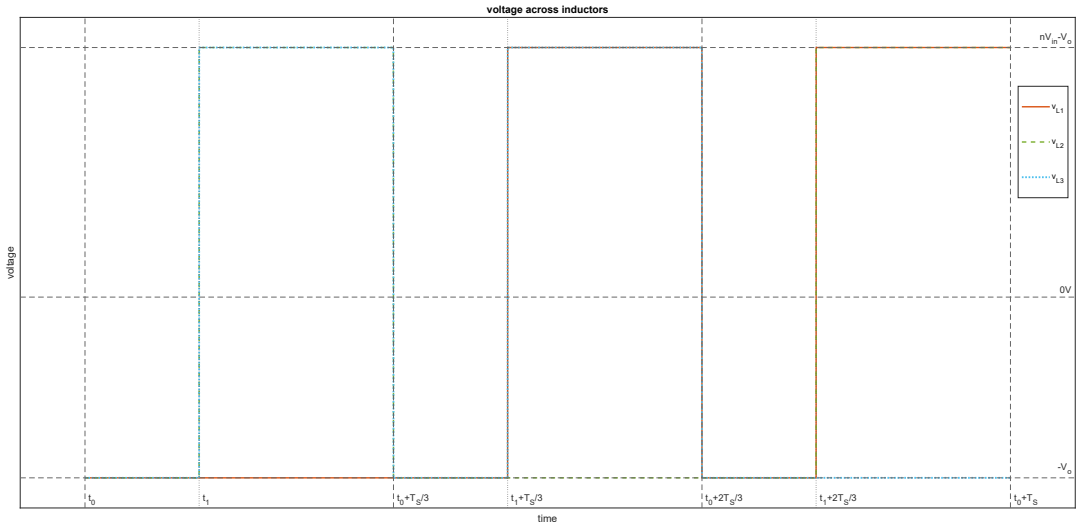


Figure 3.4: voltages across inductors

relations are valid:

$$\bar{I_L} = \frac{i_{L,pk} + i_{L,btm}}{2} \tag{3.1}$$

$$\Delta i_L = i_{L,pk} - i_{L,btm} \tag{3.2}$$

Combining equations (3.1) and (3.2) the following ones are derived:

$$i_{L,pk} = \bar{I_L} + \Delta i_L \tag{3.3}$$

$$i_{L,btm} = \bar{I_L} - \Delta i_L \tag{3.4}$$

Four additional current values will be useful for the analysis of the waveforms of the other components; those additional values are the values of the currents at the time instants corresponding tho a switch transition (both $ON \rightarrow OFF$ and $OFF \rightarrow ON$).
The plot of one current only is necessary to get all the six values. The ripple current is calculated from the slope and the time duration of the first descending part of the curve:

$$\Delta i_L = i_L(t_o) - i_L\left(t_0 + \frac{T_S}{3} + (D - 2/3)T_S\right) = \left|-\frac{V_o}{L}\right|\left(\frac{1}{3} + D - \frac{2}{3}\right)T_S = \frac{V_o}{f_S L}\left(D - \frac{1}{3}\right) \tag{3.5}$$

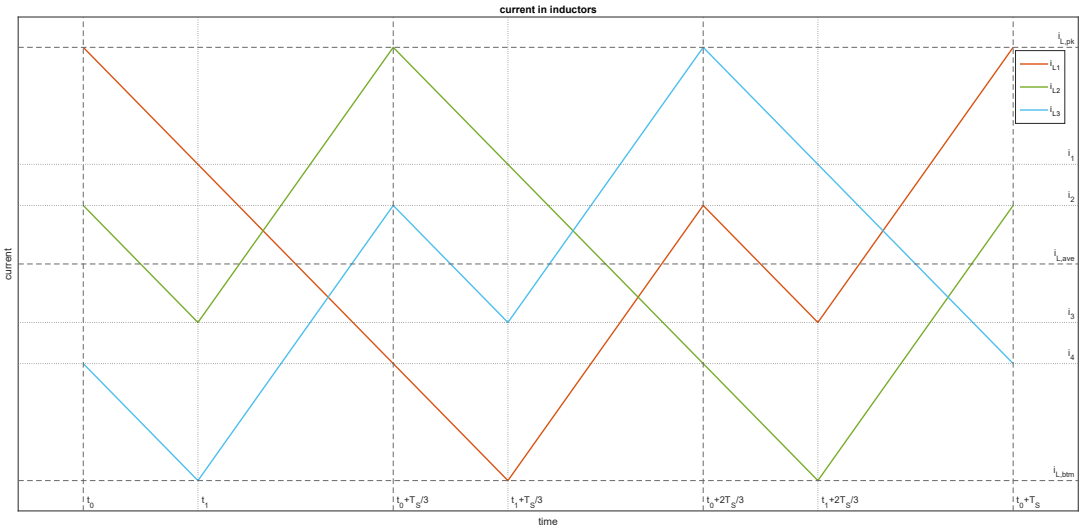


Figure 3.5: currents in inductors

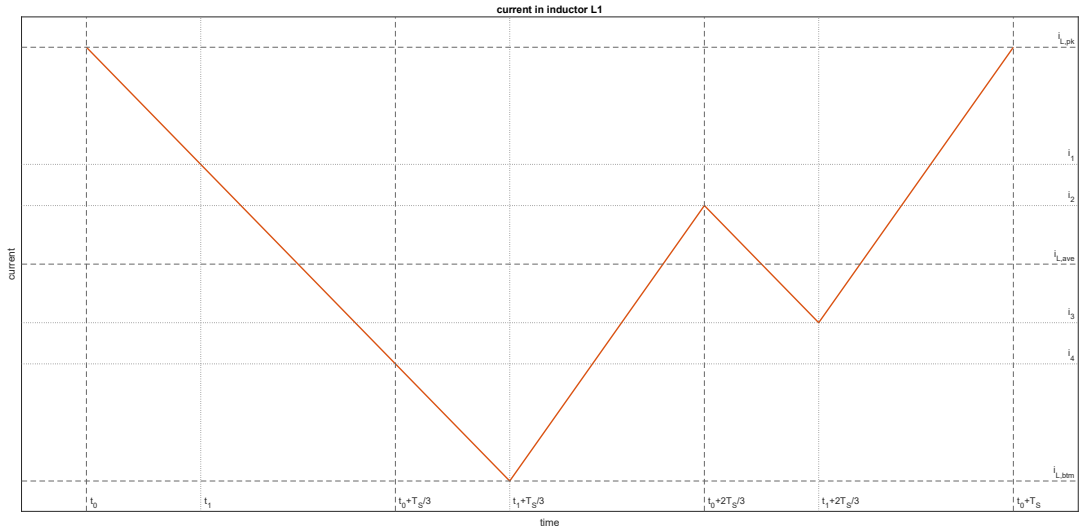


Figure 3.6: current in inductor L1

Substituting equation (3.5) in (3.3) and (3.4)

$$i_{L,pk} = \bar{I_L} + \frac{1}{2}\frac{V_o}{f_S L}\left(D - \frac{1}{3}\right) = \bar{I_L} + \frac{V_o}{f_S L}\left(\frac{D}{2} - \frac{1}{6}\right) \tag{3.6}$$

$$i_{L,btm} = \bar{I_L} - \frac{1}{2}\frac{V_o}{f_S L}\left(D - \frac{1}{3}\right) = \bar{I_L} - \frac{V_o}{f_S L}\left(\frac{D}{2} - \frac{1}{6}\right) \tag{3.7}$$

Similarly, the remaining four values are calculated: starting from a known value ($i_{L,pk}$ or $i_{L,btm}$) a current difference is added or subtracted, recalling that $V_o = nV_{in}2\,(1-D) \rightarrow nV_{in} = \frac{V_o}{2(1-D)}$

$$i_1 = i_{L,pk} - \frac{V_o}{f_S L}\left(D - \frac{2}{3}\right) = \bar{I_L} + \frac{V_o}{f_S L}\left(\frac{D}{2} - \frac{1}{6} - D + \frac{2}{3}\right) = \bar{I_L} + \frac{V_o}{f_S L}\left(-\frac{D}{2} + \frac{1}{2}\right) \tag{3.8}$$

$$\begin{aligned} i_2 &= i_{L,btm} + \left(\frac{nV_{in} - V_o}{f_S L}\right)(1-D) = \bar{I_L} - \frac{V_o}{f_S L}\left(\frac{D}{2} - \frac{1}{6}\right) + \left(\frac{\frac{V_o}{2(1-D)} - V_o}{f_S L}\right)(1-D) \\ &= \bar{I_L} + \frac{V_o}{f_S L}\left(-\frac{D}{2} + \frac{1}{6} + \frac{1}{2} - (1-D)\right) = \bar{I_L} + \frac{V_o}{f_S L}\left(\frac{D}{2} - \frac{1}{3}\right) \end{aligned} \tag{3.9}$$

$$\begin{aligned} i_3 &= i_{L,pk} - \left(\frac{nV_{in} - V_o}{f_S L}\right)(1-D) = \bar{I_L} + \frac{V_o}{f_S L}\left(\frac{D}{2} - \frac{1}{6}\right) - \left(\frac{\frac{V_o}{2(1-D)} - V_o}{f_S L}\right)(1-D) \\ &= \bar{I_L} + \frac{V_o}{f_S L}\left(\frac{D}{2} - \frac{1}{6} - \frac{1}{2} + (1-D)\right) = \bar{I_L} + \frac{V_o}{f_S L}\left(-\frac{D}{2} + \frac{1}{3}\right) \end{aligned} \tag{3.10}$$

$$i_4 = i_{L,btm} + \frac{V_o}{f_S L}\left(D - \frac{2}{3}\right) = \bar{I_L} + \frac{V_o}{f_S L}\left(-\frac{D}{2} + \frac{1}{6} + D - \frac{2}{3}\right) = \bar{I_L} + \frac{V_o}{f_S L}\left(\frac{D}{2} - \frac{1}{2}\right) \tag{3.11}$$

The design parameters listed in 3.1.1 can now be evaluated.

Maximum RMS current The current RMS value is approximately equal to the average value if the current ripple is small with respect to the average value:

$$i_{L,rms} \approx i_L, ave$$

The average value instead depends on the load. For constant load current

$$i_{L,rms,max} \approx \frac{I_{o,max}}{3} \tag{3.12}$$

whereas for constant load resistance

$$i_{L,rms,max} \approx \frac{V_o}{3R_{min}} \tag{3.13}$$

Maximum peak current It can be calculated studying the sign of its derivative with respect to the duty cycle. Since from the assumptions listed in 3.2, the output voltage is constant, the average value of the current $i_{L,ave}$ is independent of the duty cycle

$$\frac{\partial i_{L,pk}}{\partial D} = \frac{\partial}{\partial D}\left(\bar{I}_L + \frac{V_o}{f_S L}\left(\frac{D}{2} - \frac{1}{6}\right)\right) = \frac{V_o}{f_S L}\frac{1}{2}$$

The derivative is positive for any value of D, so the function is increasing in all the range of duty cycle values. Therefore, inductor's peak current value is maximum at maximum duty cycle:

$$i_{L,pk,max} = \bar{I}_{L,max} + \frac{V_o}{f_S L}\left(\frac{D_{max}}{2} - \frac{1}{6}\right) \tag{3.14}$$

Maximum ripple current Resorting to equation (3.5), the maximum ripple is calculated studying the sign of its derivative with respect to the duty cycle.

$$\frac{\partial \Delta i_L}{\partial D} = \frac{\partial}{\partial D}\left(\frac{V_o}{f_S L}\left(D - \frac{1}{3}\right)\right) = \frac{V_o}{f_S L}$$

The derivative is positive for any value of D, so like the peak value, also the ripple current is maximum for maximum duty cycle:

$$\Delta i_L = \frac{V_o}{f_S L}\left(D_{max} - \frac{1}{3}\right) \tag{3.15}$$

Inductance The value of the inductance can be derived imposing the minimumn bottom value to be larger than zero. The minimum bottom value is found studying the sign of the derivative:

$$\frac{\partial i_{L,btm}}{\partial D} = \frac{\partial}{\partial D}\left(\bar{I}_L - \frac{V_o}{f_S L}\left(\frac{D}{2} - \frac{1}{6}\right)\right) = -\frac{V_o}{f_S L}\frac{1}{2}$$

The derivative is negative for any D, so the function is decreasing. Therefore, the minimum bottom value occurs for maximum duty cycle:

$$i_{L,btm,min} = \bar{I}_{L,min} - \frac{V_o}{f_S L}\left(\frac{D_{max}}{2} - \frac{1}{6}\right) \tag{3.16}$$

Imposing equation (3.16) to be greater than zero the minimum inductance is found:

$$\begin{aligned} \bar{I}_{L,min} - \frac{V_o}{f_S L}\left(\frac{D_{max}}{2} - \frac{1}{6}\right) &> 0 \\ \frac{V_o}{f_S L}\left(\frac{D_{max}}{2} - \frac{1}{6}\right) &< \bar{I}_{L,min} \\ L &> \frac{V_o}{f_S \bar{I}_{L,min}}\left(\frac{D_{max}}{2} - \frac{1}{6}\right) \end{aligned} \tag{3.17}$$

Frequency The operating frequency of the inductor is the switching frequency of the transistors.

ESR When inductor's ESR is considered, the static gain is divided by a factor $1 + \frac{ESR_L}{3R}$ where R is the load resistance or the equivalent load resistance, given by $R = V_o/I_{o,max}$. The make the effect of inductor's ESR negligible, next condition should be verified.

$$1 + \frac{ESR_L}{3R} \approx 1 \rightarrow \frac{ESR_L}{3R} << 1 \rightarrow ESR_L << 3R \tag{3.18}$$

Output capacitor The sum of all inductors' currents, which is referred to as output current from now on, results in two contributions: the DC component I_O which fully flows in the load and the AC component i_{C_o} which

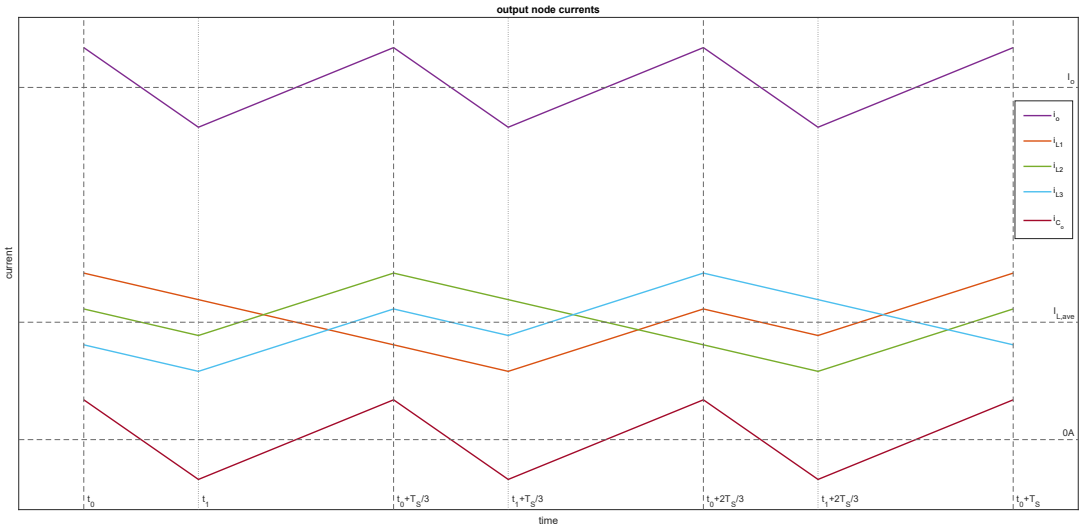


Figure 3.7: currents in output node

flows in the output capacitor C_o. The currents flowing in the output node are reported in Fig. 3.7.

$$i_o = i_{L1} + i_{L2} + i_{L3} = i_{o,DC} + i_{o,AC} = I_O + i_{C_o} \tag{3.19}$$

The characterstics of this current are the following:

- its frequency is three times the switching frequency
- it's a triangular waveform
- the slopes are equal to the sum of the slopes of each inductor's current

The peak value of the output current occurs at the end of each rising part, or at the beginning of the falling part, so at time instants $t_0, t_0 + \frac{T_S}{3}, t_0 + \frac{2T_S}{3}$:

$$\begin{aligned} i_{o,pk} = i_4 + i_2 + i_{L,pk} &= 3\bar{I}_L + \frac{V_o}{f_S L}\left(\frac{D}{2} - \frac{1}{2} + \frac{D}{2} - \frac{1}{3} + \frac{D}{2} - \frac{1}{6}\right) \\ &= I_o + \frac{V_o}{f_S L}\left(\frac{3D}{2} - 1\right) \end{aligned} \tag{3.20}$$

Similarly, the bottom current can be calculated:

$$i_{o,btm} = i_{L,btm} + i_3 + i_1 = 3\bar{I}_L + \frac{V_o}{f_S L}\left(-\frac{D}{2} + \frac{1}{6} - \frac{D}{2} + \frac{1}{3} - \frac{D}{2} + \frac{1}{2}\right)$$

$$= I_o + \frac{V_o}{f_S L}\left(-\frac{3D}{2} + 1\right) \tag{3.21}$$

The current flowing the the output capacitor can be now calculated as the difference between the output current i_o and the load current I_o.

$$i_{C_o} = i_o - I_o \tag{3.22}$$

The average current value is of course zero, whereas the peak-to-peak ripple is exactly equal to the output current's ripple.

$$\Delta i_{C_o} = i_{C_o,pk} - i_{C_o,btm} = \Delta i_o = \frac{V_o}{f_S L}(3D - 2) \tag{3.23}$$

The peak value of current i_{C_o} is half the peak-to-peak ripple:

$$i_{C_o,pk} = \frac{\Delta i_{C_o}}{2} = \frac{V_o}{f_S L}\left(\frac{3D}{2} - 1\right) \tag{3.24}$$

The sign of the derivative of $i_{C_o,pk}$ is studied to find its maximum value

$$\frac{\partial i_{C_o,pk}}{\partial D} = \frac{\partial}{\partial D}\left(\frac{V_o}{f_S L}\left(\frac{3D}{2} - 1\right)\right) = \frac{V_o}{f_S L}\frac{3}{2} \tag{3.25}$$

The derivative is positive for any D, so the maximum current $i_{C_o,pk,max}$ occurs for maximum duty cycle:

$$i_{C_o,pk,max} = \frac{V_o}{f_S L}\left(\frac{3D_{max}}{2} - 1\right) \tag{3.26}$$

and of course, the maximum peak-to-peak voltage ripple is:

$$\Delta i_{C_o,max} = \frac{V_o}{f_S L}(3D_{max} - 2) \tag{3.27}$$

Working voltage The working voltage is the output voltage.

$$V_{C_o} = V_o \tag{3.28}$$

RMS current The RMS current is found resorting to the formula of the parabolic triangle:

$$i_{C_o,rms} = \frac{i_{C_o,pk}}{\sqrt{3}} \tag{3.29}$$

Its maximum value is obtained substituting (3.24) in (3.29):

$$i_{C_o,rms,max} = \frac{i_{C_o,pk,max}}{\sqrt{3}} = \frac{V_o}{f_S L}\left(\frac{3D_{max}}{2} - 1\right)\frac{1}{\sqrt{3}} \tag{3.30}$$

Equivalent series resistance Maximum ESR can be calculated from the maximum output voltage ripple, which is given by specifications, and the maximum peak-to-peak output capacitor's current ripple (3.27).

$$ESR_{C_o} < \frac{\Delta v_{o,pp}}{\Delta i_{C_o,max}} = \frac{\Delta v_{o,pp}}{\frac{V_o}{f_S L}(3D_{max} - 2)} \tag{3.31}$$

Estimation of the capacitance The equivalent series resistance introduces a zero f_P; the capacitance of the output capacitor is typically chosen to have the zero beyond the poles frequency, so some kilohertz

$$C_o \approx \frac{1}{2\pi ESR f_P} \tag{3.32}$$

3.2.2 Diode

An ideal diode is a short circuit when it is conducting and is an open circuit when it is not conducting. Each diode conducts for one third of the switchig period, which corresponds to one period of the output current. When the diodes do not conduct, the reverse voltage applied to them is equal to the input voltage multiplied by the turns ratio.
As an example, voltage and current waveforms of diode $D1$ are reported in Fig. 3.8 and Fig.3.9.

Peak current The peak current is equal to the output peak current derived in (3.20); its derivative is the same of the output capacitor's current (3.25) of since the output DC current is constant with respect to the duty cycle,

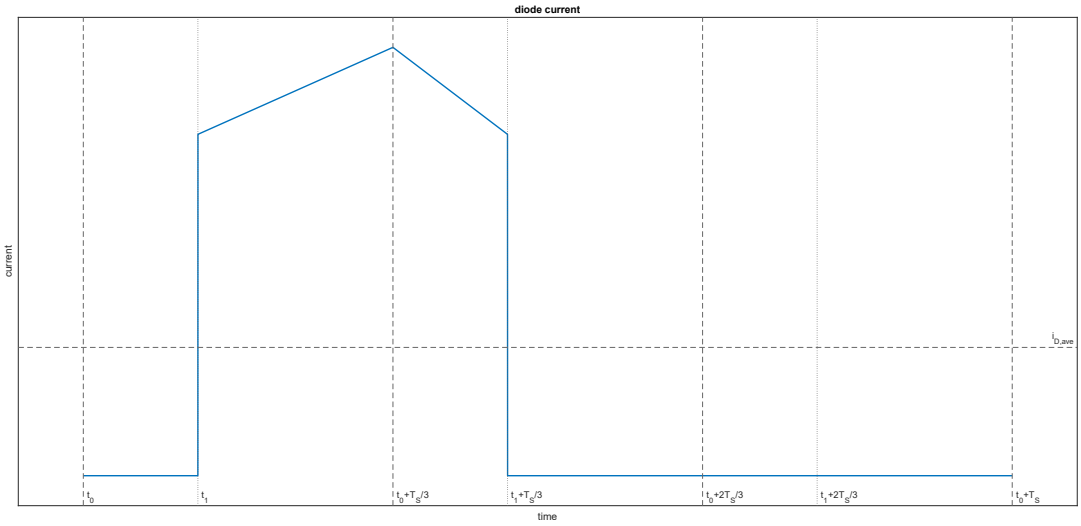


Figure 3.8: diode current

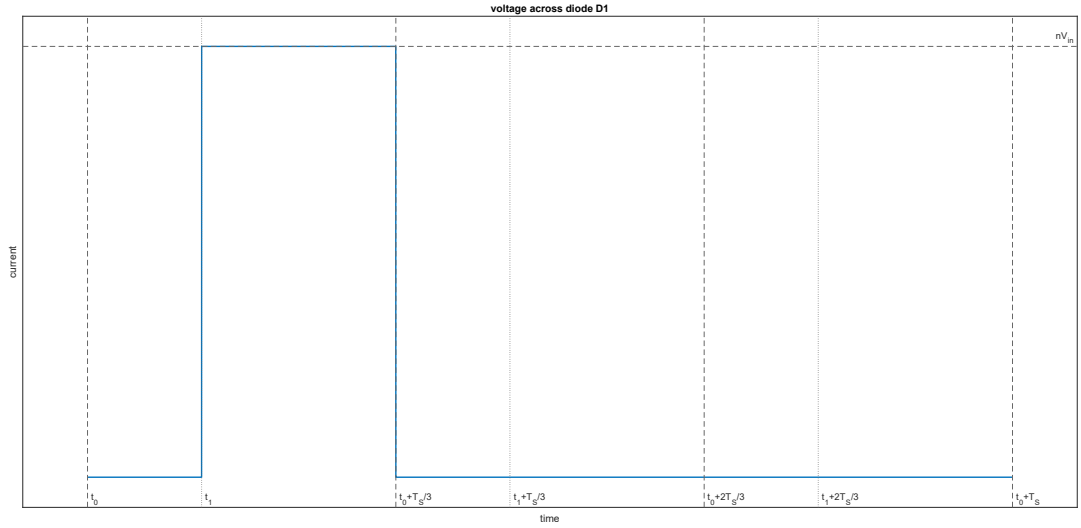


Figure 3.9: diode voltage

therefore the maximum diode peak current $i_{D,pk,max}$ is:

$$i_{D,pk,max} = i_{o,pk,max} = I_{o,max} + \frac{V_o}{f_S L}\left(\frac{3D_{max}}{2} - 1\right) \tag{3.33}$$

Average current The average diode current is equal to the load current when the diode is conducting; since the diode conducts for one third of the switching period, the average current is:

$$\bar{i}_D = \frac{1}{3} I_o$$

and of course its maximum value occurs for maximum load current

$$\bar{i}_{D,max} = \frac{I_{o,max}}{3} \tag{3.34}$$

Maximum reversse voltage the maximum reverse voltage is simply the maximum input voltage multiplied by the turns ratio:

$$v_{D,rev,max} = nV_{in,max} \tag{3.35}$$

3.2.3 Transformer

The voltage applied to the primary-side of the transformer was presented already in Fig. 3.3. The current flowing in the secondary side of each transformer is equal to the difference between inductor's and diode's currents. The current at the primary is equal to the current at the secondary multiplied by the turns ratio.

$$i_{S1} = i_{L1} - i_{D1} \tag{3.36}$$

$$i_P 1 = n i_{S1} \tag{3.37}$$

RMS current The RMS current can be evaluated roughly using flat-top approximation and considering all the positive parts to be $n\frac{I_o}{3}$ and the negative parts $-n\frac{2I_o}{3}$

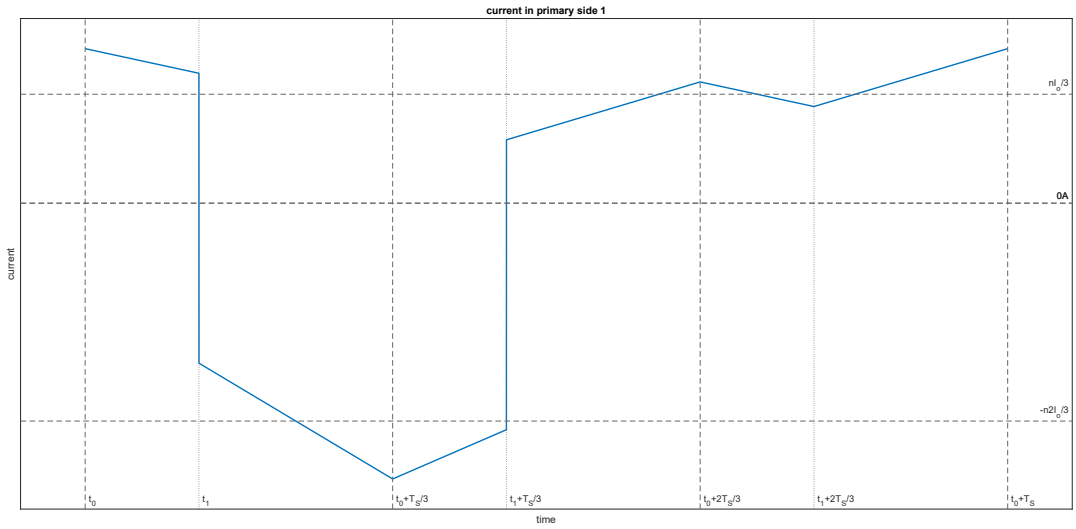


Figure 3.10: current at primary side

$$i_{P,rms} = \sqrt{\frac{1}{T_S}\left(\left(n\frac{I_o}{3}\right)^2\left(D-\frac{2}{3}\right)T_S + \left(n\frac{2I_o}{3}\right)^2\left(\frac{1}{3}\right)T_S + \left(n\frac{I_o}{3}\right)^2\left(1-D+\frac{1}{3}\right)T_S\right)}$$

$$= \sqrt{\left(n\frac{I_o}{3}\right)^2\left(D-\frac{2}{3}+4\frac{1}{3}1-D+\frac{1}{3}\right)} = \left(n\frac{I_o}{3}\right)\sqrt{2} \tag{3.38}$$

Since the RMS primary side voltage does not depend on the duty cycle, its maximum value depends on the output current only. The maximum RMS current at the secondary side is obtained dividing the maximum RMS current at the primary by the turns ratio.

$$i_{P,rms,max} = \left(n\frac{I_{o,max}}{3}\right)\sqrt{2} \tag{3.39}$$

$$i_{S,rms,max} = \frac{i_{P,rms,max}}{n} = \left(\frac{I_{o,max}}{3}\right)\sqrt{2} \tag{3.40}$$

Turns ratio The turns ratio n is a parameter which should be designed taking into account the required output voltage, the input voltage and the

maximunm static gain.
The maximum output voltage is given by the maximum ideal static gain:

$$V_o = V_{in} n \left(2 - 2D\right) \tag{3.41}$$

Since the duty cycle is limited in the range $\left(\frac{2}{3}, 1\right)$, the maximum static gain, which occurs at minimum input voltage, is:

$$M_{max} = n \left(2 - 2\frac{2}{3}\right) = n\frac{2}{3} \tag{3.42}$$

$$M_{max} V_{in,min} = n \left(2 - 2\frac{2}{3}\right) V_{in,min} = n\frac{2}{3} V_{in,min} \tag{3.43}$$

From this relations it is possible to choose a suitable turns ratio. Considering that the maximum theroretical gain is not actually achievable, it is better to keep some margin.

3.2.4 High-side switch

The most relevant parameters to be defined when designing a MOSFET are the ones related to stress and conduction losses.

Maximum blocking voltage The voltage across each transistor is ideally zero when it is conducting and is the input voltage when it is not conducting; therefore, the maximum blocking voltage is the maximum input voltage.

$$v_{SW,block,max} = V_{in,max} \tag{3.44}$$

ON resistance When high-side transistors are conducting, the current flowing through them is equal to the primary side current. The voltage drop across a conducting transistor is given in practice by the drain current times the drain-source resistance.
The peak drain current corresponds to the negative peak (Fig. 3.12). In that part, the diode is conducting, so its current is given by the sum of all inductors' currents and the secondary side current is equal to the sum of two inductors current. Therefore, the primary current is for sure smaller than twice inductor's peak current. Let use then this value as the secondary side

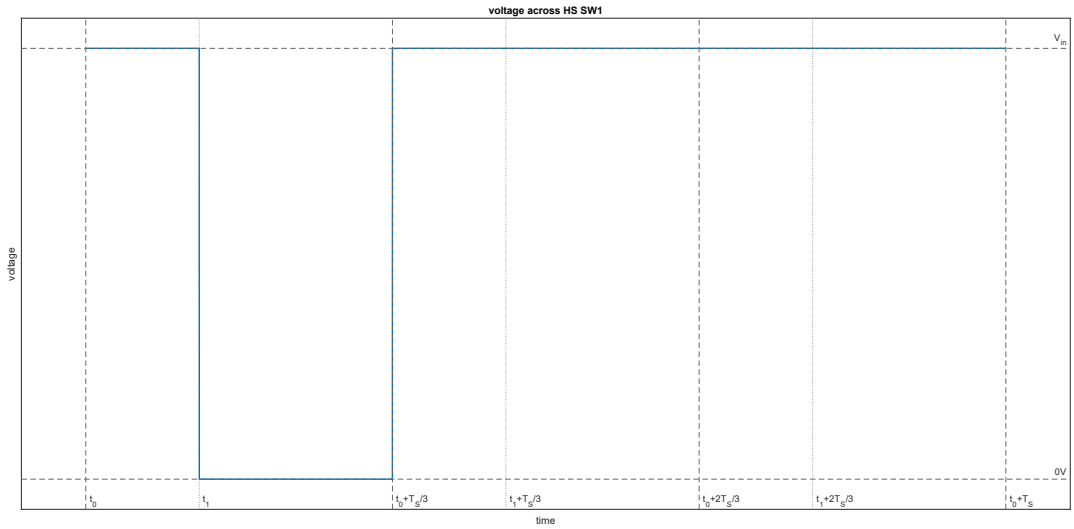


Figure 3.11: voltage on high-side switch

maximum peak current; the primary side peak current is derived multiplying by the turns ratio.

$$i_{SW,pk,max} = i_{P,pk,max} = n i_{S,pk,max} < n\left(2 i_{L,pk,max}\right) \tag{3.45}$$

Given the maximum voltage drop across the conducting transistors, for instance few percent of minimum input voltage, the maximum ON resistance is calculated.

$$r_{DS,on} < \frac{v_{SW,drop}}{i_{SW,pk,max}} \tag{3.46}$$

RMS current The RMS current is calculated to evaluate power dissipation due to conduction losses.
The current in transistor SW1 is analyzed again to derive the RMS current. Using flat-top approximation, the first part and the last one (the positive ones) are approximated with $n\frac{I_o}{3}$ whereas the negative part is approximated with $n\frac{-2I_o}{3}$.

$$i_{SW,HS,rms} = \sqrt{\frac{1}{T_S}\left(\left(n\frac{I_o}{3}\right)^2\left(D-\frac{2}{3}\right)T_S + \left(n\frac{2I_o}{3}\right)^2\left(D-\frac{2}{3}\right)T_S + \left(n\frac{I_o}{3}\right)^2\left(1-D+\frac{1}{3}\right)T_S\right.}$$

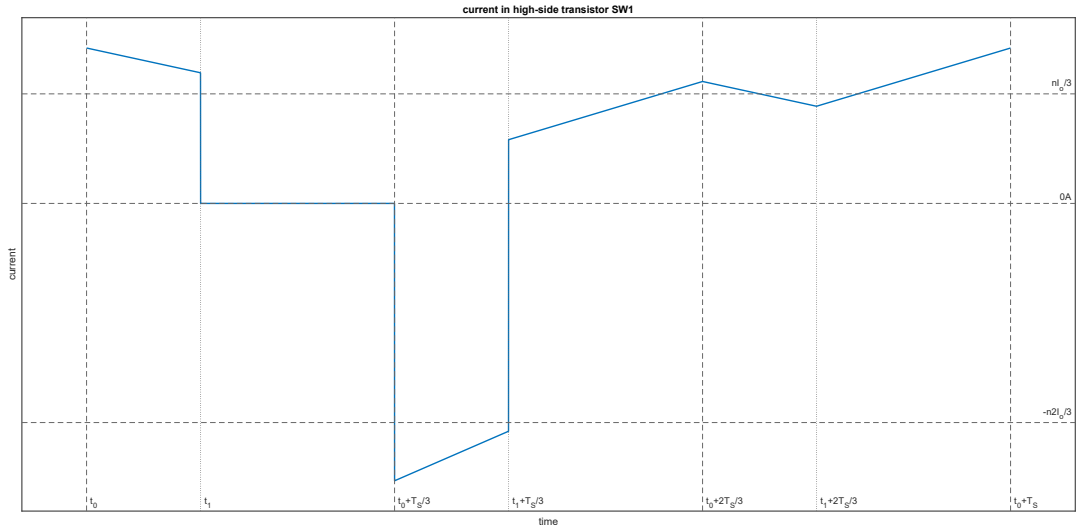


Figure 3.12: current in high-side switch

$$= \sqrt{\left(n\frac{I_o}{3}\right)^2 ((4D-2))} = \left(n\frac{I_o}{3}\right)\sqrt{4D-2} \tag{3.47}$$

$$\frac{\partial i_{SW,HS,rms}}{\partial D} = \frac{\partial}{\partial D}\left(\left(n\frac{I_o}{3}\right)\sqrt{4D-2}\right) = \frac{1}{2}\left(n\frac{I_o}{3}\right)\frac{1}{\sqrt{4D-2}}4$$

$$i_{SW,HS,rms,max} = \left(n\frac{I_{o,max}}{3}\right)\sqrt{4D_{max}-2} \tag{3.48}$$

The maximum dissipated power due to conduction losses is then derived.

$$P_{SW,cond} = r_{DS,on} i^2_{SW,HS,rms,max} \tag{3.49}$$

3.2.5 Low-side switch

The same parameters derived for the high-side switches are derived for the low-side ones.

Maximum blocking voltage The voltage applied to low-side switches is different from the high-side ones, but the maximum voltage is the same.

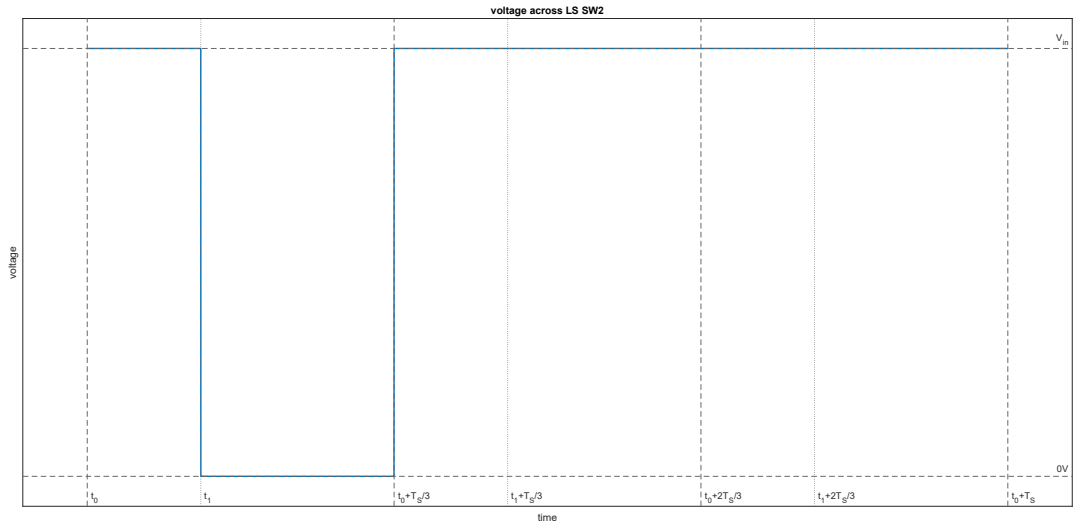


Figure 3.13: voltage across low-side switch

$$v_{SW,block,max} = V_{in,max} \tag{3.50}$$

ON resistance The drain source conducting resistance should be evaluated in the same way as it is done for the high-side switch. Since the peak current is the same, the same result obtained previously is valid.

RMS current The RMS current is calculate. Flat-top approximation is used again to make calculations easier.

$$i_{SW,LS,rms} = \sqrt{\frac{1}{T_S}\left(n\frac{2I_o}{3}\right)^2 (1-D)\,T_S} = \left(n\frac{2I_o}{3}\right)\sqrt{1-D} \tag{3.51}$$

$$\frac{\partial i_{SW,LS,rms}}{\partial D} = \frac{\partial}{\partial D}\left(\left(n\frac{2I_o}{3}\right)\sqrt{1-D}\right) = \frac{1}{2}\left(n\frac{2I_o}{3}\right)\frac{1}{\sqrt{1-D}}\,(-1)$$

$$i_{SW,LS,rms,max} = \left(n\frac{2I_{o,max}}{3}\right)\sqrt{1-D_{min}} \tag{3.52}$$

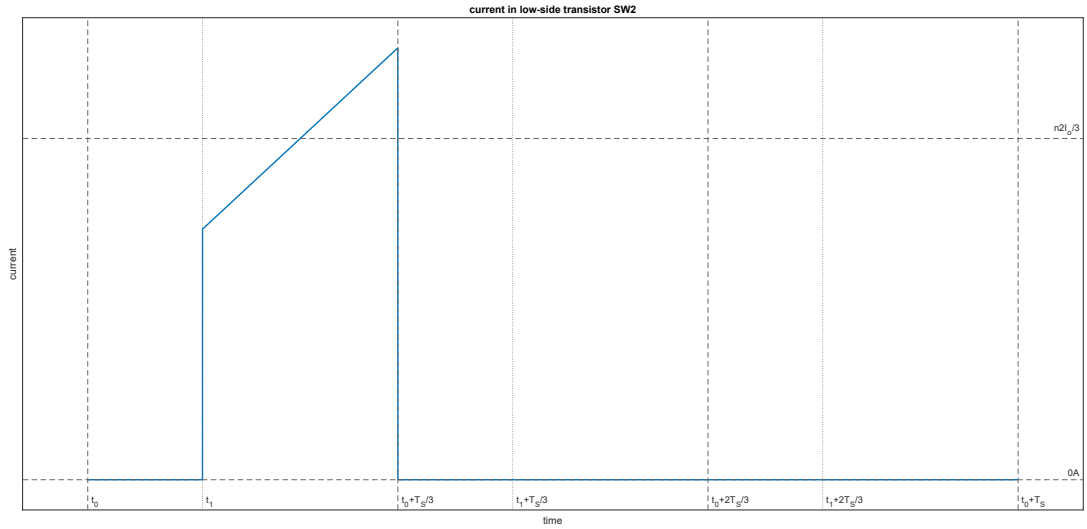


Figure 3.14: current in low-side switch

The maximum dissipated power due to conduction losses is then derived.

$$P_{SW,cond} = r_{DS,on} i^2_{SW,HS,rms,max} \tag{3.53}$$

3.2.6 Input Capacitor

The input current i_{in}, which is given by the sum of the DC current from the input voltage source and the current flowing in the input capacitor, can be calculated either as the sum of the currents flowing in the high-side transistors or as the sum of the currents flowing in the low-side transistors.

$$i_{in} = i_{SW1} + i_{SW3} + i_{SW5} = i_{SW2} + i_{SW4} + i_{SW6} = I_{in} + i_{C_{in}} \tag{3.54}$$

RMS current Since the low-side transistors are never conducting simultaneously, their currents are separated in time, so quadratic KCL law (section 3.5) can be exploited. Moreover, since the currents coming from the input voltage is a a pure DC current and the input capacitor's current is purely AC, they are separated in frequency, so quadratic KCL law is valid again.

$$i^2_{in,rms} = i^2_{SW2,rms} + i^2_{SW4,rms} + i^2_{SW6,rms} = I^2_{in} + i^2_{C_{in},rms} \tag{3.55}$$

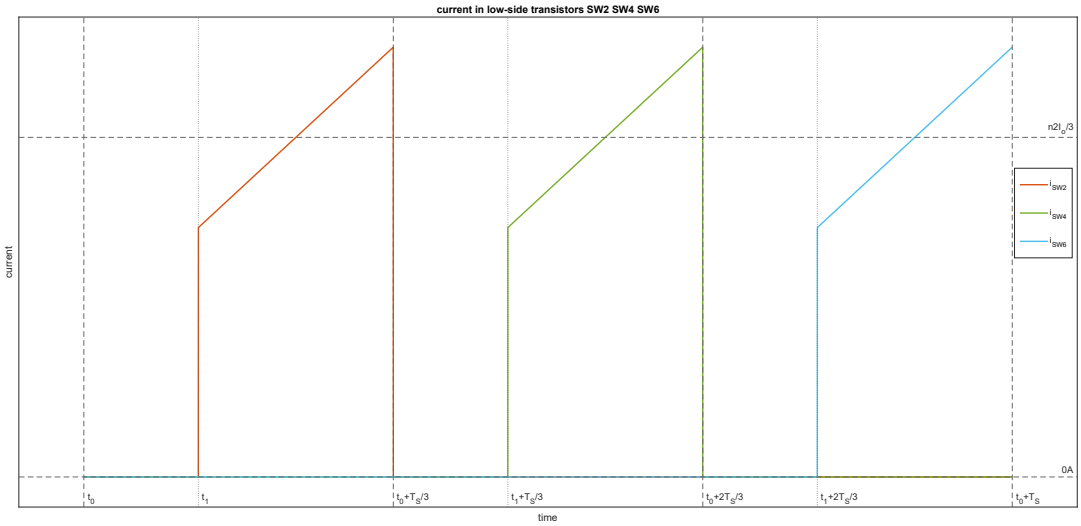


Figure 3.15: low-side transistors currents

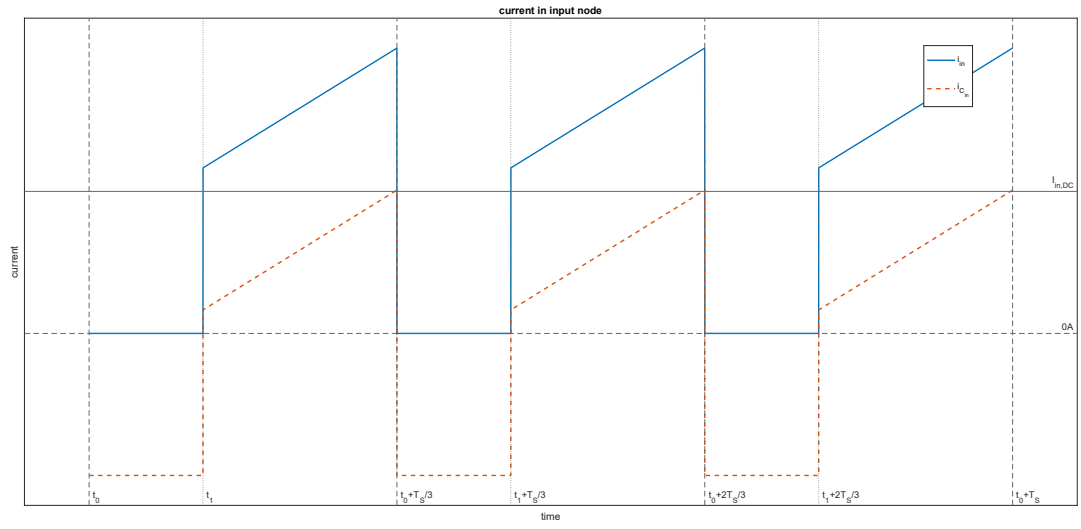


Figure 3.16: currents at input node

The RMS currents of low-side transistors are equal and their value is derived in equation 3.51.

$$i^2_{SW,LS,rms} = \left(\left(n\frac{2I_o}{3}\right)\sqrt{1-D}\right)^2 = n^2 I_o^2\left(\frac{4}{9} - \frac{4D}{9}\right) \tag{3.56}$$

The square value of the input DC current is derived from the static gain.

$$I^2_{in} = (GI_o)^2 = \left(n\left(2-2D\right)I_o\right)^2 = n^2 I_o^2\left(4 - 8D + D^2\right) \tag{3.57}$$

Combining equations (3.55), (3.56) and (3.57), the expression of input capacitor's RMS current is derived:

$$i^2_{C_{in},rms} = I^2_{in} - 3i^2_{SW,LS,rms}$$

$$\begin{aligned} i_{C_{in},rms} = \sqrt{I^2_{in} - 3i^2_{SW,LS,rms}} &= \sqrt{3n^2 I_o^2\left(\frac{4}{9} - \frac{4D}{9}\right) - n^2 I_o^2\left(4 - 8D + D^2\right)} \\ &= nI_o\sqrt{-D^2 + D\frac{20}{3} - \frac{8}{3}} \end{aligned} \tag{3.58}$$

Its derivative is studied to find the maximum value

$$\frac{\partial i_{C_{in},rms}}{\partial D} = \frac{\partial}{\partial D}\left(nI_o\sqrt{-D^2 + D\frac{20}{3} - \frac{8}{3}}\right) = \frac{1}{2}nI_o\frac{1}{\sqrt{-D^2 + D\frac{20}{3} - \frac{8}{3}}}\left(-2D + \frac{20}{3}\right)$$

The square root is always positive when it exists, so the sign of the last term is the only one that has to be studied.

$$\left(-2D + \frac{20}{3}\right) > 0$$

$$D < \frac{10}{3}$$

Since the duty cycle is defined only in the range $\left(\frac{2}{3}, 1\right)$, the function is always increasing and the maximum RMS current occurs at maximum duty cycle.

$$i_{C_{in},rms} = nI_o\sqrt{-D_{max}^2 + D_{max}\frac{20}{3} - \frac{8}{3}} \tag{3.59}$$

Working voltage The input capacitor is placed in parallel to the input voltage, so its working voltage is the input voltage.

3.2.7 Leakage inductance

The leakage inductance is intrinsically present in the transformers. However, physical inductors can be added in series to the primary side to control the ZVS more effectively.
The leakage inductance, however, introduces a load effect on the static gain and reduces the quality factor of the frequency response.

Inductance The value of the leakage inductance can be calculated so that the load effect does not affect the static gain dramatically. The ideal static gain is $M_{ideal} = n\,(2 - 2D)$. The static gain considering the effect of the leakage inductance is instead:

$$M_{real} = n\,(2 - 2D - 3I_o') \tag{3.60}$$

Where I_o' is the so-called normalized output current, which is given by:

$$I_o' = \frac{nf_S L_d I_o}{V_{in}} \tag{3.61}$$

To make the effect of $3I_o'$ negligible, the following condition is imposed

$$\begin{aligned} 3I_o' &<< (2 - 2D) \\ I_o' &<< \frac{(2 - 2D)}{3} \\ \frac{nf_S L_d I_o}{V_{in}} &<< \frac{(2 - 2D)}{3} \end{aligned}$$

$$L_d << \frac{V_{in}\,(2 - 2D)}{3f_S I_o} \tag{3.62}$$

RMS The current flowing through the leakage inductance is equal to the primary side current, whose maximum RMS value is calculated in (3.39)

$$i_{L_d,rms,max} = \left(n \frac{I_{o,max}}{3} \right) \sqrt{2} \tag{3.63}$$

peak current The peak current is equal to the peak current flowing on the primary side, which corresponds to the peak current estimated for the transistors in (3.45)

$$i_{L_d,pk,max} = i_{P,pk,max} = n i_{S,pk,max} < n \left(2 i_{L,pk,max} \right) \tag{3.64}$$

Operating frequency The operating frequency is the switching frequency.

3.2.8 Parasitic capacitance

Like the leakage inductance is intrinsically present in the transformers, parasitic capacitances are intrinsically present in MOSFETs. To achieve zero-voltage-switching, the value of the parasitic capacitance should be lower than a maximum value, derived from the load condition for ZVS

Capacitance The capacitance value can be derived from the minimum load conidtion to achieve zero-voltage-switching:

$$I_o > \frac{3}{\sqrt{2}} \frac{V_{in}}{\sqrt{L_d / C_e}} \tag{3.65}$$

Reversing (3.65), the maximum value for C_e is derived:

$$C_e < \frac{2 I_o^2 L_d}{9 V_{in}^2} \tag{3.66}$$

3.2.9 Primary capacitor

A capacitors in series to the primary side of the transformers is needed to avoid core saturation; in fact any DC voltage component applied to the primary side is blocked by the capacitor.
The value of the capacitance should not be too large, otherwise the capacitor would never block anything.

The value of the capacitance should not be too small, otherwise the ripple voltage across it would be too large.
As a rule of thumb, the capacitance value is estimated imposing the ripple voltage to be smaller than a percentage of the input voltage.

Capacitance Let calculate the maximum ripple voltage.

$$C_p = \frac{\Delta Q}{\Delta v_{C_p}} = \frac{\Delta Q}{10\% V_{in}} \tag{3.67}$$

The maximum charge ΔQ occurs at maximum current and minimum duty cycle, since it's given by the integral of the primary-side current in Fig. 3.10 according to the formula

$$\Delta Q = n \frac{2 I_{o,max}}{3} \frac{T_S}{3} \tag{3.68}$$

Combining equations (3.67) and (3.68) the value of the primary capacitor is obtained.

$$C_p = \frac{\Delta Q}{\Delta v_{C_p}} = \frac{n \frac{2 I_{o,max}}{3} \frac{T_S}{3}}{10\% V_{in}} \tag{3.69}$$

Working voltage When leakage inductances are present on the primary side of the transformers, overvoltages occur during switching transitions; therefore, it is a safe solution to use capacitors whose working voltage is at least twice the maximum input voltage.

RMS current The RMS current is equal to the primary-side RMS current calculated in (3.39).

$$i_{C_p,rms,max} = \left(n \frac{I_{o,max}}{3} \right) \sqrt{2} \tag{3.70}$$

3.3 Low-power prototype

There are no real specifications, so they will be derived from the limitations of the lab equipment.

3.3.1 Laboratory equipment

The RIGOL DP832 power supply is present in the labs; it has three channels, the maximum output values for each channel are reported in the following table.

channel	channel 1	channel 2	channel 3
max output current	3 A	3 A	3 A
max output voltage	30 V	30 V	5 V

Channels 1 and 2 can be connected either in series or in parallel to increase input power.
It is chosen to connect the channel in series, hence doubling the maximum input voltage.

3.3.2 Measurements

As mentioned in section (3.1.3), both static and dynamic measurements should be performed.
To test the static gain, the input voltage is from 40V to 60V and the duty cycle is adjusted so as to keep the output voltage equal to 25 V. It is convenient to use a 1:1 transformer turns ratio. Maximum ad minimum duty cycle values are derived.

$$V_o = nV_{in}\,(2-2D) \rightarrow D = 1 - \frac{V_o}{2nV_{in}}$$

$$D_{min} = 1 - \frac{V_o}{2nV_{in,min}} = 1 - \frac{25V}{2 \times 1 \times 40V} = 0.68 \tag{3.71}$$

$$D_{max} = 1 - \frac{V_o}{2nV_{in,max}} = 1 - \frac{25V}{2 \times 1 \times 60V} = 0.79 \tag{3.72}$$

The dynamic measurements are instead performed with maximum gain and maximum output voltage, so for $V_{in} = 60V$ and $D = \frac{2}{3}$; therefore, the

output voltage will be $40V$.
This condition is the one that gives maximum volt-second applied to the primary side of the transformer; it is necessary to take it into account when designing transformer.
From Fig. 3.3 presented in the previous section, the flux linkage λ is given by

$$\lambda = \| - \frac{2V_{in}}{3} \times (1 - D)T_S \| = \frac{2V_{in,max}}{3} \times (1 - \frac{2}{3})T_S \tag{3.73}$$

3.3.3 Load

The maximum load current is set to $I_{o,max} = 2.5A$, so the maximum output power, which is given at maximum output voltage, maximum load current, is $100W$.
The minimum load current is set to half the maximum current, therefore $I_{o,min} = 1.25A$

3.3.4 Others

Switching frequency In order to make the effect of parasitic components negligible, it is useful to pick a relatively low switching frequency, i.e. some tens of kilohertz.

$$f_S = 50kHz$$

$$T_S = \frac{1}{T_S} = 20\mu s$$

Output ripple The output ripple is 1% of the maximum output voltage, therefore:

$$v_{o,pp,max} = 1\% \, (40V) = 400mV \tag{3.74}$$

Voltage across transistors The voltage drop across transistors is subtracted from the primary side of the transformers; to have a low impact on the operation of the circuit, the maximum voltage drop allowed is 1% of the minimum input voltage.

$$v_{SW,drop} = 1\% V_{in,min} = 1\% \left(40V\right) = 400mV \tag{3.75}$$

The values of the components can now be designed.

3.3.5 Inductors

Inductance From equation (3.17)

$$L > \frac{V_o}{f_S \bar{I}_{L,min}} \left(\frac{D_{max}}{2} - \frac{1}{6} \right) = \frac{25V}{50kHz \times 0.417A} \left(\frac{0.79}{2} - \frac{1}{6} \right) = 274\mu H$$

The next value on the E12 series is taken, then $L = 330\mu H$

RMS current From equation (3.12)

$$i_{L,rms,max} \approx \frac{I_{o,max}}{3} = \frac{2.5A}{3} = 0.833A$$

Peak current From equation (3.14)

$$i_{L,pk,max} = \bar{I}_{L,max} + \frac{V_o}{f_S L} \left(\frac{D_{max}}{2} - \frac{1}{6} \right) = \frac{2.5A}{3} + \frac{25V}{50kHz \times 330\mu H} \left(\frac{0.79}{2} - \frac{1}{6} \right) = 1.18A$$

Ripple current From equation(3.15)

$$\Delta i_L = \frac{V_o}{f_S L} \left(D_{max} - \frac{1}{3} \right) = 0.69A$$

Operating frequency The operating frequency is $50kHz$.

ESR From equation (3.18)

$$ESR_L << 3R \rightarrow ESR_L < 5\% \frac{V_o}{I_{o,max}} = 5\% \frac{25V}{2.5A} = 500m\Omega$$

3.3.6 Output capacitor

Working voltage The working voltage is the maximum output voltage, so $40V$.

RMS current From equation (3.30)

$$i_{C_o,rms,max} = \frac{V_o}{f_S L}\left(\frac{3D_{max}}{2} - 1\right)\frac{1}{\sqrt{3}} = 161mA$$

ESR From equation (3.31)

$$ESR_{C_o} < \frac{\Delta v_{o,pp}}{\frac{V_o}{f_S L}(3D_{max} - 2)} = 717m\Omega$$

Capacitance From equation (3.32)

$$C_o \approx \frac{1}{2\pi ESR \times 5kHz} = 44\mu F$$

3.3.7 Diode

Maximum reverse voltage From equation (3.35)

$$v_{D,rev,max} = nV_{in,max} = 60V$$

Peak current From equation (3.33)

$$i_{D,pk,max} = i_{o,pk,max} = I_{o,max} + \frac{V_o}{f_S L}\left(\frac{3D_{max}}{2} - 1\right) = 2.78A$$

Average current From equation (3.34)

$$\bar{i}_{D,max} = \frac{I_{o,max}}{3} = 0.83A$$

3.3.8 Transformer core

Power transfomers, as well as magnetic components in general, are not usually present on catalogues, but have to be designed ad hoc. The design is no trivial task, because electrical specifications must fit in thermal, magnetic and dimension constraints. The proposed design criteria and the relative design flow are presented.

Design criteria A power transformer is a device which has to transfer energy from the primary-side to the secondary-side; therefore, energy should not be stored in the core, and this constraint can not be used as a design criterion. The design criteria are instead related to the losses; in fact, transformers should be able to withstand electrical stress and operate correctly.
From a circuit-level standpoint, power dissipation in the core should be kept low to maintain a high efficiency.
From a thermal standpoint, power dissipation in the core should be kept low, because power is dissipated in heat, and heat makes temperature increase. It is preferable to have magnetic cores working below a certain temperature (typically 100° C); moreover, if temperature arises beyond a critical value, called "Curie Temperature", magnetic properties are lost.
Temperature rise depends on thermal resistance, which depends on core material, shape, dimension and is difficult to determine. Therefore, approximate calculations will be used to derive core dimensions.
At high frequency (like 50 kHz) losses are given both by core and wire losses. Core losses are determined by the flux density swing and wire losses are due to the parasitic resistance of the windings.
It can be shown that minimum total losses occur when core losses are roughly equal to wire losses.

Design flow The design steps are here presented.

1. Choose core material and shape
2. Determine allowed power losses, derive core dimensions
3. Derive the number of turns
4. Derive dimension of wires

1 - Core material and shape The choice of core material and shape depends on the application. Ferrite cores are typically used for high frequency power transformers (i.e. switching frequency larger than tens of kilohertz); E-shape cores are a good compromise between dimension and power dissipation capability.
The material chosen is the following one from EPCOS/TDK: SIFERRIT material N87.

2 - Allowed power losses and core dimenions The maximum allowed power losses is set by efficiency constraints.
From core shape and material it is possible to derive an estimation of the thermal resistance as a function of core's dimensions; imposing a maximum temperature rise, core dimensions are derived.
μ F

The maximum power dissipate is set to be about 1% of maximum output power, so $P_{D,allowed} = 1W$. Since three transformers are present, efficiency is lowered by 3%.
As a rule of thumb, for ferrite materials, thermal resistance as a function of the external surface A_{ext} expressed in square centimeters is:

$$R_{TH} = \frac{800 \frac{^\circ \mathrm{C\,cm^2}}{\mathrm{W}}}{A_{ext}} \tag{3.76}$$

For E-shape cores, the ratio between surface area and window area (which is the area through which wires are wound) is constant regardless of the volume. Such ratio is about 22, so the thermal resistance as a function of the window area expressed in square centimeters is:

$$R_{TH} = \frac{36 \frac{^\circ C cm^2}{W}}{A_w} \tag{3.77}$$

The temperature rise is then

$$\Delta T = R_{TH} P_{D,allowed} = \frac{36 \frac{^\circ C cm^2}{W}}{A_w} \times 1W = \frac{36^\circ C cm^2}{A_w} \tag{3.78}$$

For a window area of 1 centimeter squared, the temperature rise is 36°, which is acceptable.

The core E36/18/11 is chosen . Its most important dimensions are reported.

- $A_W = 1.22 cm^2$ window area
- $A_c = 1.12 cm^2$ minimum core area
- $V_e = 9.72 cm^3$ core volume
- $MLT = 7.64 cm$ average length turn

3 - Number of turns Knowing core dimensions, a rough estimation of the maximum flux density swing can be derived from power constraints. In fact, datasheet provide relative core losses P_V (power dissipated vs core volume) varying switching frequency and flux density swing.
Relative core losses, expressed in kilowatts per cubic meter, are derived dividing the maximum allowed core losses by the core volume. Core losses are half the maximum allowed losses, hence $0.5W$.

$$P_V = \frac{0.5W}{9.72cm^2} = 51.4\frac{kW}{m^3} \tag{3.79}$$

From graphs present on the datasheet, a maximum peak flux density of $100mT$ is derived.
Ampere law relates flux density and volt-second according to the formula:

$$\Delta B = \frac{\lambda}{2NA_c} \tag{3.80}$$

Where ΔB is the peak flux density, λ is the volt-second applied to the primary side and N is the number of turns at the primary side.

The maximum volt-second occurs for maximum input voltage and minimum duty cycle.

$$\lambda = \frac{2}{3}V_{in,max}\left(1 - D_{min}\right)T_S = \frac{2}{3}60V\left(1 - \frac{2}{3}\right)20\mu s = 267V\mu s \tag{3.81}$$

Imposing the peak flux density smaller than $100mT$, a the condition on the number of turns is obtained.

$$\frac{\lambda}{2NA_c} < 100mT \tag{3.82}$$

$$N > \frac{\lambda}{2\left(100mT\right)A_c} = \frac{267V\mu s}{2\left(100mT\right)120cm^2} = 11.1 \tag{3.83}$$

The number of turns can be therefore for example 15.

4 - Dimension of wires Losses in the wires are determined by the wire turn resistance $R_{turn} = \frac{\rho \times MLT}{A_{wire}}$ and by the RMS current according to the following formula.

$$P_{wires} = \frac{\rho\,(MLT)\,N_P}{A_{wire}} i_{P,rms}^2 + \frac{\rho\,(MLT)\,N_S}{A_{wire}} i_{S,rms}^2$$
$$= \frac{\rho\,(MLT)}{A_{wire}} N_P \left(i_{P,rms}^2 + \frac{N_S}{N_P} i_{S,rms}^2 \right)$$

Where ρ is the resistivity of the copper, A_{wire} is the cross section of the wire and the ratio $N_S/N_P = n = 1$

The total currents are calculated.

$$\left(i_{P,rms}^2 + \frac{N_S}{N_P} i_{S,rms}^2 \right) = \left(n \frac{I_{o,max}}{3} \sqrt{2} \right)^2 + n \left(\frac{I_{o,max}}{3} \sqrt{2} \right)^2 = 2.77A^2 \quad (3.84)$$

Substituting the current value just calculated and imposing the power dissipated smaller than half the allowed power dissipated, the following expressions are obtained.

$$P_{wires} = \frac{(1.724\mu\Omega cm)\,(7.64cm)\,15}{A_{wire}} \left(2.77A^2 \right) \quad (3.85)$$

$$P_{wires} < 0.5W \quad (3.86)$$

Combining the two equations

$$\frac{(1.724\Omega cm)\,(7.64cm)\,15}{A_{wire}} \left(2.77A^2 \right) < 0.5W \quad (3.87)$$

$$A_{wire} > \frac{(1.724\mu\Omega cm)\,(7.64cm)\,15}{0.5W} \left(2.77A^2 \right) = 1.1mm^2 \quad (3.88)$$

Wires AWG #16 or AWG #17 are suitable
EPCOS/TDK EE36/18/11

3.3.9 High-side transistor

Maximum blocking voltage From equation (3.44)

$$v_{SW,block,max} = V_{in,max} = 60V$$

ON resistance From equation (3.46)

$$r_{DS,on} < \frac{v_{SW,drop}}{i_{SW,pk,max}} = \frac{400mV}{2 \times i_{L,pk,max}} = \frac{400mV}{2.36A} = 169m\Omega$$

The cold resistance reported on datasheet is typically half the hot resistance calculated here.

$$r_{DS,ON,cold} = \frac{169m\Omega}{2} = 85m\Omega$$

RMS current From equation (3.48)

$$i_{SW,HS,rms,max} = \left(n\frac{I_{o,max}}{3}\right)\sqrt{4D_{max} - 2} = 0.9A$$

The maximum dissipated power can be calculated

$$P_{D,SW} = r_{DS,ON} \times i^2_{SW,rms} = 169m\Omega \times (0.9A)^2 = 136mW$$

3.3.10 Low-side transistor

Maximum blocking voltage Like high-side transistor.

$$v_{SW,block,max} = V_{in,max} = 60V$$

ON resistance Like high-side transistor.

$$r_{DS,ON,cold} = \frac{169m\Omega}{2} = 85m\Omega$$

RMS current From equation (3.52)

$$i_{SW,LS,rms,max} = \left(n\frac{2I_{o,max}}{3}\right)\sqrt{1 - D_{min}} = 0.96A$$

The maximum dissipated power can be calculated

$$P_{D,SW} = r_{DS,ON} \times i^2_{SW,rms} = 169m\Omega \times (0.96A)^2 = 156mW$$

3.3.11 Input Capacitor

Working voltage The working voltage is the input voltage $60V$.

RMS current From equation (3.59)

$$i_{C_{in},rms} = nI_o\sqrt{-D_{max}^2 + D_{max}\frac{20}{3} - \frac{8}{3}} = 3.5A$$

3.3.12 Leakage inductance

Inductance From equation (3.62)

$$L_d << \frac{V_{in}\,(2-2D)}{3f_S I_o}$$

$$\frac{V_{in}\,(2-2D)}{3f_S I_o} = 213\mu H$$

Taking the 5% of the calculated value, the inductance is obtained

$$L_d = 10\mu H$$

RMS current From equation (3.63)

$$i_{L_d,rms,max} = \left(n\frac{I_{o,max}}{3}\right)\sqrt{2} = 1.17A$$

Peak current From equation (3.64)

$$i_{L_d,pk,max} = i_{P,pk,max} = ni_{S,pk,max} < n\,(2i_{L,pk,max}) = 2.36A$$

3.3.13 Parasitic capacitance

Working voltage It's equal to the input voltage $60V$

Capactiance From equation (3.66)

$$C_e < \frac{2I_o^2 L_d}{9V_{in}^2} = 965pF$$

3.3.14 Primary capacitor

Capacitance From equation (3.69)

$$C_p = \frac{n\frac{2I_{o,max}}{3}\frac{T_S}{3}}{10\%V_{in}} = \frac{\frac{n\times 2.5A}{3}\frac{20\mu s}{3}}{10\%60V} = 1.85\mu F$$

Working voltage Due to overvoltage on primary-side parasitic inductors, it may be safer to set the working voltage to twice the input voltage: $120V$

RMS current It is equal to the primary-side RMS current.

$$i_{C_p,rms,max} = \left(n\frac{I_{o,max}}{3}\right)\sqrt{2} = 1.18A$$

3.4 Future perspectives

In future, a prototype of the designed converter may be built and tested, possibly with a control feedback network.

3.5 Quadratic KCL

For signals separated in time or in frequency, quadratic KCL is true. It states that the square RMS of the sum of the signals is equal to the sum of the square RMS value of each signal. Both the example of time-separated signals and frequency-separated signals are provided.

Frequency-separated signals Let consider an output signal i_{sum} given by the sum of a purely DC signal i_{DC} and of a purely AC signal i_{AC} of period T_S.

$$i_{sum} = i_{DC} + i_{AC} \tag{3.89}$$

$$i^2_{sum,rms} = \frac{1}{T_S}\int_0^{T_S} \left(i_{DC} + i_{AC}\right)^2 \, dt \tag{3.90}$$

$$= \frac{1}{T_S}\int_0^{T_S} \left(i^2_{DC} + 2i_{DC}i_{AC} + i^2_{AC}\right) \, dt \tag{3.91}$$

$$= \frac{1}{T_S}\int_0^{T_S} \left(i^2_{DC}\right) \, dt + \frac{1}{T_S}\int_0^{T_S} \left(2i_{DC}i_{AC}\right) \, dt + \frac{1}{T_S}\int_0^{T_S} \left(i^2_{AC}\right) \, dt \tag{3.92}$$

The second term of equation (3.92) can be rewritten; the DC value is constant with respect to time, so it can be placed before the integral operator; the mean integral of a purely AC signal over a period is always zero.

$$\frac{1}{T_S}\int_0^{T_S} \left(2i_{DC}i_{AC}\right) \, dt = \frac{2i_{DC}}{T_S}\int_0^{T_S} \left(i_{AC}\right) \, dt = \frac{2i_{DC}}{T_S}\left(0\right) = 0 \tag{3.93}$$

The first and second terms of equation (3.92) are instead

- $\left(\frac{1}{T_S}\int_0^{T_S} \left(i^2_{DC}\right) \, dt\right) = i_{DC,rms^2}$: square RMS value of i_{DC}
- $\left(\frac{1}{T_S}\int_0^{T_S} \left(i^2_{AC}\right) \, dt\right) = i^2_{AC,rms}$: square RMS value of i_{AC}

The square RMS value of the sum is then

$$i^2_{sum,rms} = i^2_{DC,rms} + i^2_{AC,rms} \tag{3.94}$$

Time-separated signals Let consider an output signal i_{sum} given by the sum of two signals i_1 and i_2 separated in time, i.e. for any time instant if a signals is non-zero, the other one is zero.

$$i_{sum} = i_1 + i_2 \tag{3.95}$$

$$i^2_{sum,rms} = \frac{1}{T_S}\int_0^{T_S} (i_1 + i_2)^2 \; dt \tag{3.96}$$

$$= \frac{1}{T_S}\int_0^{T_S} \left(i_1^2 + 2i_1 i_2 + i_2^2\right) \; dt \tag{3.97}$$

$$= \frac{1}{T_S}\int_0^{T_S} \left(i_1^2\right) \; dt + \frac{1}{T_S}\int_0^{T_S} (2i_1 i_2) \; dt + \frac{1}{T_S}\int_0^{T_S} \left(i_2^2\right) \; dt \tag{3.98}$$

The praoduct of signals i_1 and i_2 is always zero, because they are never non-zero concurrently; since the integral of zero is zero, the second term of equation (3.98) is always zero

$$\frac{1}{T_S}\int_0^{T_S} (2i_1 i_2) \; dt = 0 \tag{3.99}$$

The first and second terms of equation (3.98) are instead

- $\left(\frac{1}{T_S}\int_0^{T_S} (i_1^2) \; dt\right) = i_{1,rms^2}$: square RMS value of i_1
- $\left(\frac{1}{T_S}\int_0^{T_S} (i_2^2) \; dt\right) = i^2_{2,rms}$: square RMS value of i_2

The square RMS value of the sum is then

$$i^2_{sum,rms} = i^2_{1,rms} + i^2_{2,rms} \tag{3.100}$$

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