Politecnico di Torino

Nanotechnologies for the ICTs

Investigation of low temperature SiGe epitaxy with high order precursors

Author:
Manuel Mencarelli

Supervisors:
Matteo Cocuzza
Andriy Hikavyy

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Abstract

Since the strain technology was introduced at the 90nm node, Silicon-Germanium (SiGe) is the most widely used p-MOS Source/Drain (S/D) material. With the continuous down-scaling of transistors, the contact resistance (R_c) at the S/D-metal interface is becoming a major part of the parasitic resistance in the device. Rc depends on two factors: it is directly proportional to the contact resistivity (ρ_c) and inversely proportional to the contact area between electrodes and S/D. In order to decrease the Rc impact, different approaches have been studied in the last years. Complex doping engineering allows achieving ultra-low ρ_c, while a higher contact area can be guaranteed by implementing a wrap around contact (WAC).

An increase of germanium concentration of SiGe S/D layers driven by increasing strain in the Si channel requires a decrease of epitaxial deposition thermal budget. To decrease the growth temperature, new silicon and germanium gas precursors are being intensively investigated to maintain a sustainable SiGe growth rate.

In this work, different aspects of low temperature epitaxy of SiGe through high order precursors have been studied in order to improve p-MOS S/D layers. Initially, morphological and electrical properties of in situ Boron and Gallium co-doped SiGe layers grown on Si (100) substrate have been analyzed. In particular, after a first characterization the grown samples have been submitted to different Laser annealing temperatures to investigate dopants activation/deactivation and diffusion. The work aims to reach a better understanding of the Gallium doping behaviour in order to reduce S/D material resistivity which is currently limited by B solubility.

Furthermore, low temperature SiGe growth on different Si surfaces has been studied with the use of a specially designed mask. The deposition on the patterned structure was initially tested with classic precursors to evaluate the different growth rates. Successively, it has been compared with low temperature processes based on high order precursors. This study helps to understand facets development in 3-dimensional future devices and consequently to avoid merging of S/D of adjacent fins, allowing WAC formation.

Preface

The project presented in the master thesis was performed at IMEC research center (Leuven) during a six-months internship within the group-4 materials epitaxy research team. The work was focused on low temperature epitaxy through high order precursors of SiGe in view of future p-MOS S/D application. The entire project was carried out under the guidance of the supervisor Andiy Hikavyy.

List of abbreviations

AFM	Atomic force microscopy
SiGe	Silicon-Germanium
S/D	Source/Drain
R_c	Contact resistance
ρ_c	Contact resistivity
A_c	Contact area
WAC	Wrap around contact
MOSFET	Metal-oxide-semiconductor field effect transistor
IC	Integrated circuit
GR	Growth rate
POR	Process of record
SEG	Selective epitaxial growth
CDE	Cyclic deposition etching
DCS	Dichlorosilane
CVD	Chemical vapor deposition
MBE	Molecular beam epitaxy
PAMBE	Plasma-assisted molecular beam epitaxy
PECVD	Plasma-enhanced chemical vapor deposition
UHVCVD	Ultrahigh vacuum chemical vapor deposition
SEM	Scanning electron microscopy
TEM	Transmission electron microscopy
BSE	back-scattered electrons
SE	Secondary electrons
ABF-STEM	Annular bright field scanning transmission electron microscopy
XRD	X-Ray Diffraction
HRXRD	High resolution X-Ray Diffraction
XRR	X-Ray Reflectivity
SIMS	Secondary ion mass spectroscopy
$\mu 4PP$	Micro four-point probe
R_s	Sheet resistance
MHE	Micro Hall Effect
STI	Shallow trench insulation

Contents

Chapter 1

Introduction

1.1 Project motivation

The metal-oxide-semiconductor field effect transistor (MOSFET) is the main building block of nowadays logic devices. Since the first integrated circuit (IC) has been created, the number of transistors present in the ICs has followed the Moore's law, that in 1965 predicted a MOSFET density integration doubling every two years [1]. This trend in the evolution of the electronics industry translates into the continuous reduction of the transistors dimensions. In early 2000^{th} the extreme geometrical scaling dimensions of the MOSFET started to be accompanied by the fundamental architectural changes to overtake several difficulties grown by the continuous shrinking. The most revolutionary improvements are the strained channel and the multi-gate devices: strain is used since 90 nm node [2] and finFET became the dominant device design from 22nm node [3]. Nowadays, to achieve strain in the Si channel, SiGe:B and Si:P Source/Drain (S/D) (respectively for p-type and n-type MOSFET) are grown epitaxially. SiGe must to be fully-strained in order to enhance channel mobility, and steadily increasing Germanium concentration allows to obtain higher levels of strain [4, 5]. Furthermore, the S/D material must demonstrate a low contact resistance (R_C) [6]. Indeed, in an ideal case, we would like the behaviour of a device to be determined only by the device itself. However, the presence of contacts resistance results in non-ideal electrical characteristics, with an undesired voltage drop in the metal/SiGe interface region. R_C is directly proportional to the contact resistivity (ρ_C) and inversely proportional to the contact area (A_C) [7]. Hence, the contact area decrease due to miniaturization of device's dimensions should be compensated by a doping increase in the SiGe layer, to avoid an uncontrolled increase of R_C. However, boron solubility has a lower solubility limit in germanium than in silicon [8, 9]. Hence, in high Ge content SiGe, B doping has reached its maximum and other effective dopants are studied to overcome this difficulty. Parallel to the doping increase, wrap-around contact (WAC) implementation would help to decrease R_C maximizing the contact area at scaled fin-pitch [10, 11]. Nevertheless, WAC formation presents others difficulties. Indeed, the SiGe epitaxial growth on a 3-Dimensional structure is generally not uniform due to faceting: depending on the Si plane the epitaxial material is growing, it can have different growth rates, and in the end

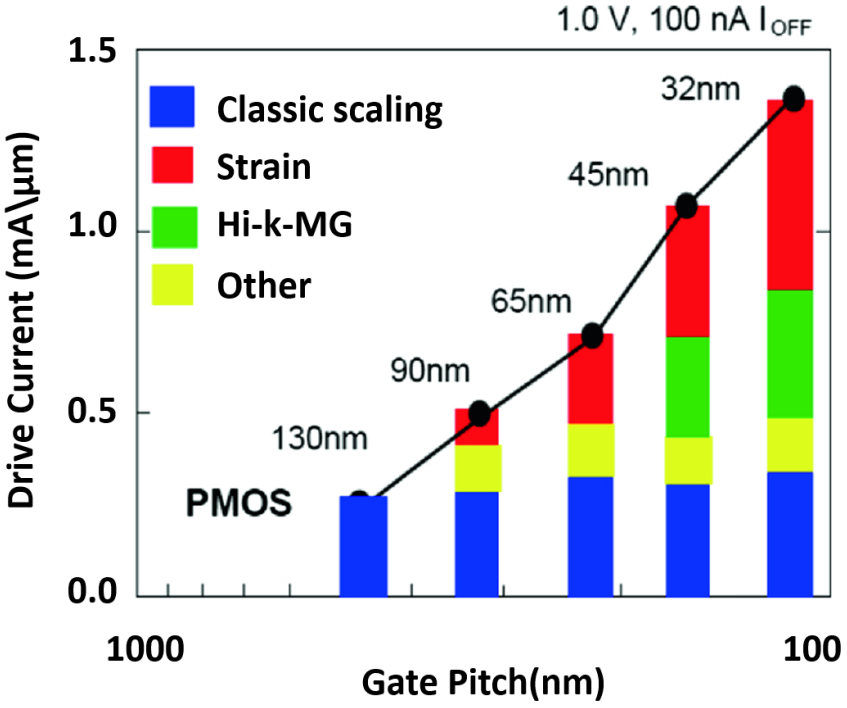


Figure 1.1: Impact of CMOS improvements beyond classic scaling on the drive current [12].

the slow growing planes will be dominant. This results in the so-called "diamond shape" of finfFET S/D [13]. Although this is not a problem until now, the latest technological nodes pose a very difficult challenge to avoid merging of epitaxial S/D of adjacent fins leading to a decrease of the contact area, making the WAC implementation impossible.

1.2 Project objectives

The work presented in this dissertation is divided into two different studies. Common objective of the two parts, is the reduction of contact resistance. We have seen in the previous section that R_C depends on both material resistivity and contact area. The first part is focused on the study of gallium as a SiGe co-dopant alongside boron, to overcome the B solubility limit in S/D. The second part is devoted to SiGe growth anisotropy study on different Si surfaces leading to faceting phenomenon.

1.2.1 SiGe:B:Ga Laser Annealing

The contact resistivity is usually lowered in a metal-semiconductor by enhancing the active carrier concentration in the interface region. Examples of very high B doping concentration due to its high solubility in SiGe can be found in literature [14]. Furthermore, thanks to its small atomic radius, when B is present in substitutional positions in the crystal lattice it relieves compressive strain in SiGe. This

strain compensation effect leads to an energetically favored incorporation of B, allowing (to some extent) above-equilibrium dopant activation [15]. Unfortunately, the solubility limit of B in germanium is much lower than in silicon. Hence, the increasing germanium concentration required in SiGe S/D brings a lowering of the active carriers. In figure 1.2 it is possible to observe that there is a maximum of active doping in the range of $40 < Ge\% < 70$, and it exponentially decreases at higher germanium concentration. To overcome this limit, other p-type dopants have been studied in the recent years. In this work, epitaxially grown SiGe layers in-situ co-doped with boron and gallium are studied. The gallium choice is based on its high solubility in Ge, which is higher than the boron one. Moreover, its atomic radius is larger than both boron's and germanium's radius, hence enhancing the strain and not reducing it like B incorporation. For these reasons, Ga has already demonstrated experimental evidences of contact resistivity improvement [16]. Aim of this work is to submit the B and Ga co-doped samples to Laser Annealing at different temperatures, studying the Ga dopants behaviour under these treatments. In particular, activation/deactivation and diffusion of gallium should be inspected. Typically, in situ B doped SiGe doesn't show significant improvements in active carrier concentration, probably due to already high concentration given by the strain compensation effect explained above. Since the gallium radius higher than the Ge one, there is no reason to observe such effect. For this reason, thermal treatments could in principle contribute to the carrier activation, helping to achieve lower resistivity.

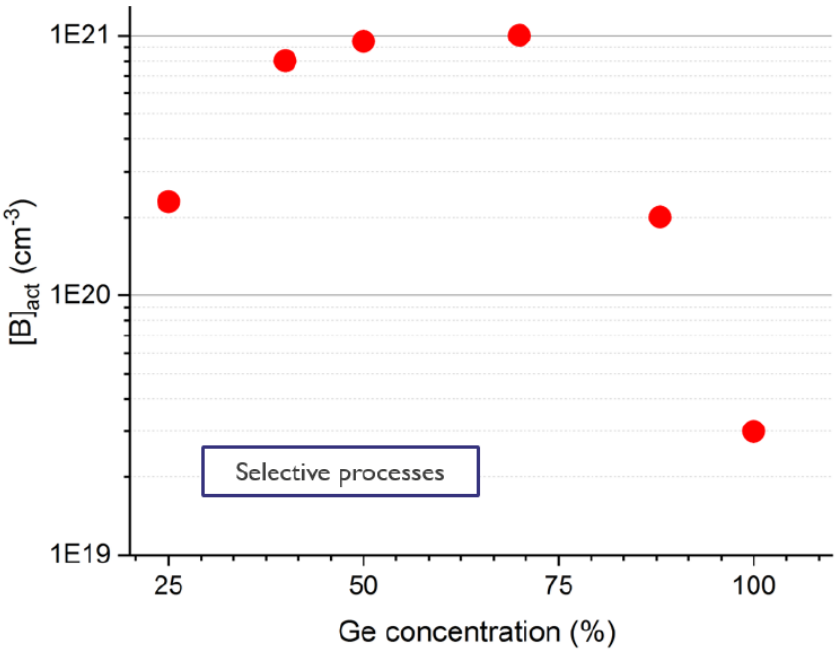


Figure 1.2: Maximum achievable Boron active concentration in function of germanium concentration. At Ge% higher than 70%, it drops due to smaller B solid solubility in germanium than in silicon [courtesy to Andriy Hikavyy]

1.2.2 SiGe growth on different Si surfaces

As discussed above, parallel to doping improvements R_C can be improved by Wrap-Around contact implementation. This type of contact refers to a metal/semiconductor interface extended through the entire S/D area, and not limited to the top surface as classically done. Nevertheless, practical implementation of WAC is not easy. In order to create WAC S/D epitaxial SiGe grown on adjacent fins must not merged. Thus, SiGe growth should be uniform through the entire fin to limit merging. Unfortunately, classical SiGe deposition shows a strong faceting effect due to growth anisotropy and merging is typical in advanced scaled devices (below 14 nm node). This defines the second part of the project where we will study the growth rate (GR) of SiGe on different Si surfaces. This will be done using a special structure with Si fins oriented along different directions, in order to obtain different crystal planes on the fins sidewalls. The deposition is initially performed using the process of record (POR) for SiGe epitaxial deposition, that usually shows a strong faceting limited by (111) slowly growing planes [13]. An evaluation of the planes growth rate will help to better understand the growth dynamics of finFET S/D. Next, a new low temperature deposition process based on high order precursors will be applied to these structures. It is known that growth rate of SiGe deposition on different Si planes changes with several parameters: temperature, precursors used and presence of oxide and nitride. The growth rates on the different surfaces will be calculated in order to understand if SiGe faceting can be limited by the new process. Several adjustments will be necessary during the work to optimize the deposition and allowing epitaxial growth on each surface.

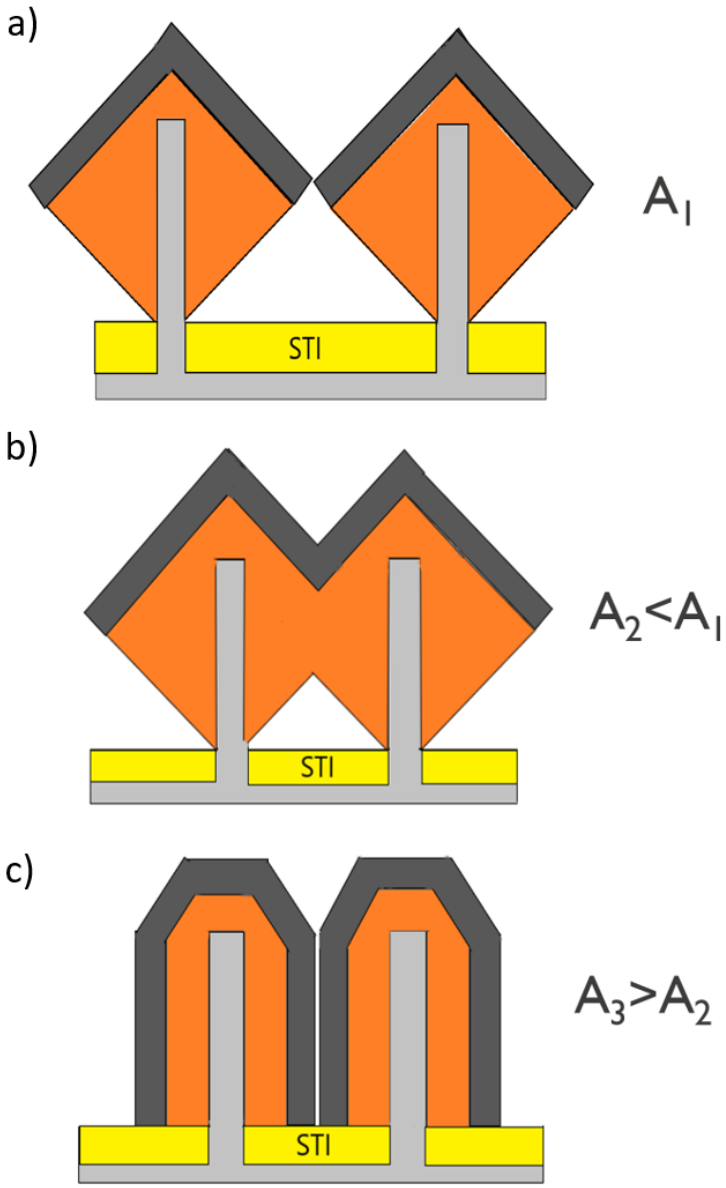


Figure 1.3: Representation of different contact area achievable after SiGe growth: a) faceted S/D deposition without merging; b) faceted S/D depositio with merging; contact area is reduced; c) uniform SiGe deposition, merging is avoided resulting in WAC formation.

Chapter 2

Theory of source and drain epitaxy

Given the importance of epitaxial growth in standard CMOS process, in this chapter a detailed explanation of epitaxy will be given. Afterwards, the current development of source/drain growth will be presented.

2.1 Epitaxy

Epitaxy refers to a specific type of crystal growth in which new crystalline layer is grown with the structure and orientation of the substrate. The term epitaxy comes from the Greek roots epi ($\epsilon\pi\iota$), meaning "above", and taxis ($\tau\alpha\xi\iota\zeta$), meaning "ordered manner". Numerous factors (e.g. process parameters and surface purity) should be well controlled to obtain the atoms perfectly arranged upon the substrate. Two different types of epitaxy are possible:

- Homoepitaxy: when the substrate and the epitaxial layer are of the same material.
- Heteroepitaxy: the epitaxial layer and the substrate are different materials.

In the case of heteroepitaxy, the substrate and the layer materials usually have different lattice parameters. If the lattice mismatch is small, and the thickness of the deposited layer is sufficiently low, the layer will conserve the substrate lattice parameter and the growth is called *pseudomorphic*. The layer structure forced in the substrate structure will thus accumulate elastic energy. In pseudomorphic growth there are two possibilities: if the lattice parameter of the layer is higher than the substrate one, the layer will be compressively strained, while if the substrate lattice parameter is higher than the layer one, the deposited layer will be tensily strained. As can be seen in figure 2.1, due to the Poisson effect (the atomic cell volume remains the same), if the in-plane lattice parameter ($a^{\parallel}$) is forced to match with the substrate, the out-of-plane lattice parameter ($a^{\perp}$) will change consequently, becoming higher with compressive strain and lower in case of tensile strain.

Nevertheless, after a certain thickness, the pseudomorphically strained layer will be no more the energetically favorite system and to minimize the energy misfit dislocations will be created in the layer to regain its natural lattice parameter.

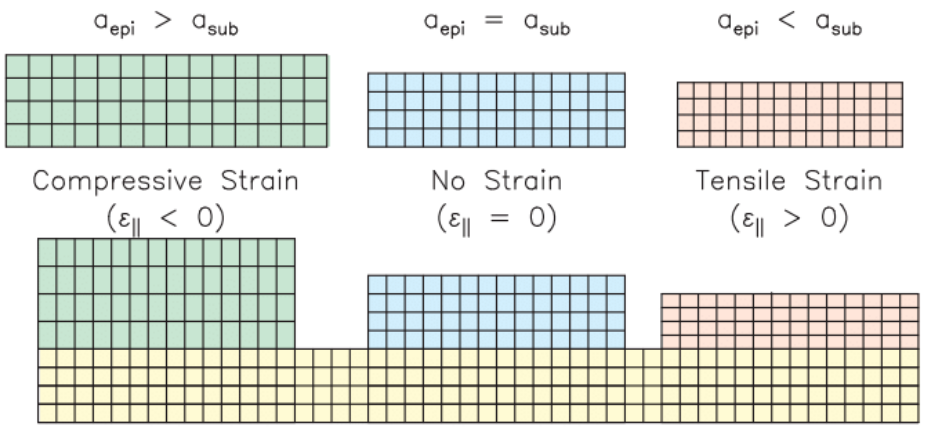


Figure 2.1: Schematic representation of pseudomorphically strained layer for different cases of lattice mismatch

This phenomenon is called plastic relaxation, and the thickness at which it occurs is called *critical thickness for plastic relaxation*. The critical thickness strongly depends on lattice mismatch and temperature.

Three different modes of growth are generally observed:

- Layer-by-layer (or Frank-Van der Merve): This growth is the optimal one because is fully 2D, each atomic layer is completely formed before the successive layer starts to grow. This happens when the chemical bond between the substrate and the adatoms is stronger than the one between adatoms.

- Islands (or Volmer-Weber): In this case the deposited material nucleates in 3D islands; it's the case of bond between adatoms stronger than the bond between substrate and adatoms.

- Layer-plus-islands (or Stransky-Krastanov): It's the intermediate case of the first two growth modes. Firstly, the growth will occur monolayer by monolayer, but after a certain thickness the islands growth will be energetically favorite and the growth will switch on the 3D one.

Another important aspect to consider to achieve epitaxial growth is the surface preparation. Indeed, as explained above, epitaxy refers to the deposition of a material maintaining the substrate crystalline structure. To allow this type of growth, it is necessary that the substrate surface is pure and free from contaminants. Unfortunately, silicon has a strong tendency to oxidize, and when exposed to air a thin layer of SiO_2 is created, called native oxide. For this reason, substrate surface is submitted to a cleaning preparation prior to epitaxy. Usually, such a preparation is composed by two steps:

- an ex-situ (outside the epitaxy tool) wet cleaning

- an in-situ (inside the epitaxy tool) hydrogen bake

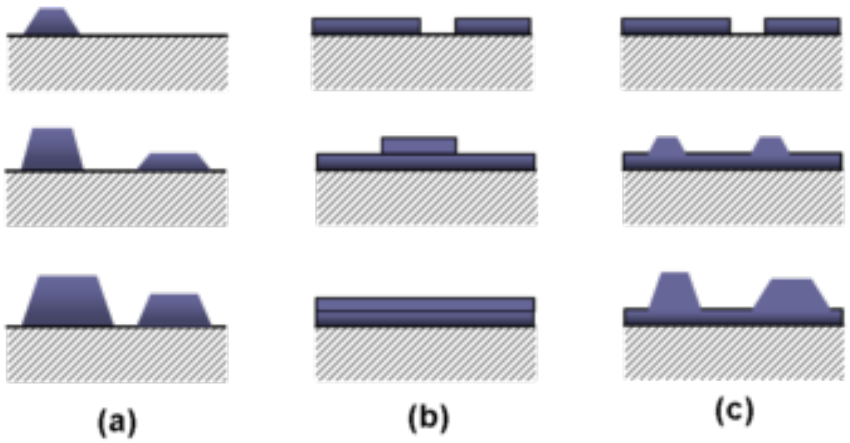


Figure 2.2: schematic diagram showing the three different modes of growth: (a) Islands, (b) Layer-by-layer, (c) Layer-plus-islands

The wet cleaning is typically done through immersion of the wafer in a diluted HF bath. After this type of cleaning, the majority of the oxide and impurities are removed, and the surface is "H-passivated". This means that the silicon dangling bonds adsorb hydrogen atoms. Nevertheless, this etch is not perfect and other contaminations can be created through air contact, before the wafer is inserted in the epitaxy chamber. An in-situ cleaning is thus needed, and the wafers are typically baked in H_2 in the temperature range of 700°-1100°for few minutes. Given the high thermal budget of the H_2 bake, different in-situ cleaning strategies are studied to be integrated in a low temperature process [17]. In this work, Previum clean developed by ASM [18] is performed to limit thermal budget during the low temperature deposition, while hydrogen bake is used for conventional process without stringent thermal budget request.

2.2 Low temperature epitaxy

As mentioned above, a fundamental aspect of every process integrated in the fabrication of advanced CMOS structures is the thermal budget. Indeed, also in the source/drain epitaxial growth thermal budget minimization is a must to avoid variability and reliability issues. High temperature processes risk, besides the possible unwanted dopants diffusion, stronger relaxation, losing its elastic force and failing to enhance channel mobility through strain. For SiGe growth gas precursors such as silane or dichlorosilane and germane are typically used, with addition of diborane for in-situ boron doping [19]. The growth rate depends on many factors: temperature, precursors flows, pressure, etc. Decreasing the epitaxy temperature usually results in a lowering of the growth rate, until no deposition occurs at all. For this reason the epitaxy of SiGe with the precursors mentioned above shows decent growth rates only in a temperature range down to ∼500°C. To reach lower deposition temperature the precursor gases should be changed. In

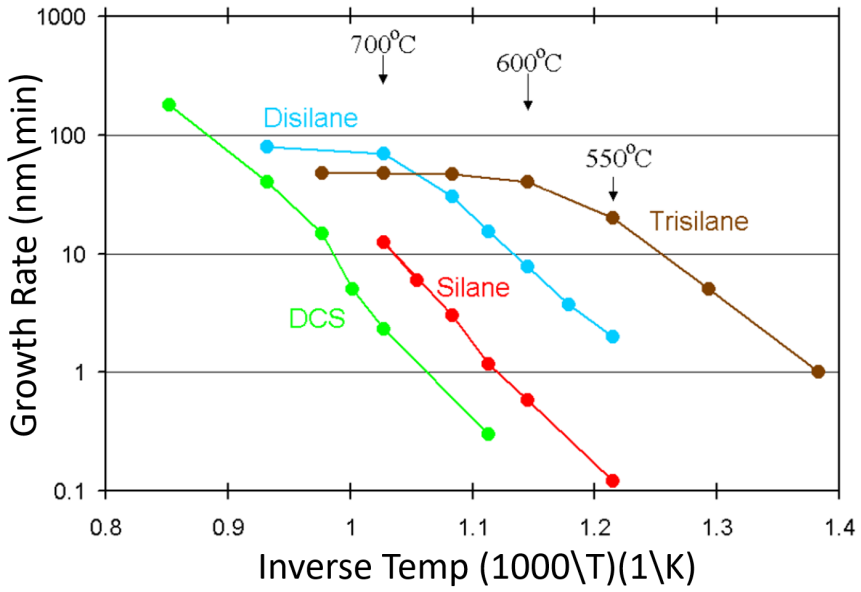


Figure 2.3: Arrhenius plots of silicon deposition using different silane order. It is possible to notice that the growth rate increase with the silane order [20].

the last years higher order silanes and germanes have been intensively studied as an alternative to conventional precursors [21]. In figure 2.3 the Arrhenius plots of classical precursors (DCS, silane) is compared with the ones of higher order silanes. One can notice that increasing the precursors order improves the growth rate at the equal temperature with respect to the deposition with silane; this consequently allows to obtain the same growth rate at lower temperature. Growth rate improvement can be explained by the different kinetics of the precursor gases when the substrate is covered by H atoms. Indeed, at low temperature the deposition rate is governed by hydrogen atoms desorption from the surface, which rate strongly depends on thermal energy. Next the reaction paths of the classical and high order precursors will be explained, in order to understand their different properties.

2.2.1 Silane kinetics

It is known that at low temperature the Si adsorption is controlled by hydrogen desorption from the surface [22]. In fact, a silane molecule needs two free site to be adsorbed producing two adsorbed hydrogen atoms whose desorption is not immediate and strongly depends on temperature. The reaction between the silane molecule and the Si surface can be expressed as follows:

$$SiH_4 + 2\_ \rightarrow \underline{Si}H + \underline{H} + H_2 \tag{2.1}$$

$$\underline{H*} + \underline{H} \rightarrow H_2 + 2\_ \tag{2.2}$$

$$H_2 + 2\_ \rightarrow 2\underline{H} \tag{2.3}$$

Where _ denotes a free site available for adsorption, $\underline{X}$ an adsorbed specie and $H*$ an excited hydrogen atom. The adsorption reaction is shown in figure

2.4 and the balance between the silane adsorption and the Hydrogen desorption defines the growth kinetic.

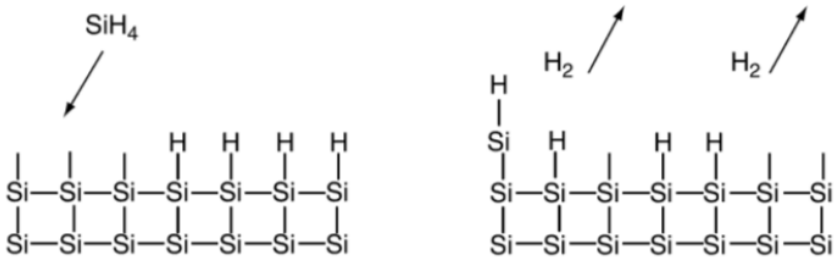


Figure 2.4: Schematic of epitaxy based on silane [23]

2.2.2 Disilane kinetics

As can be seen from the Arrhenius plot, disilane has a higher growth rate than silane at low temperatures. This can be explained by two different factors: the weaker Si-Si bond with respect to the Si-H bond (lower activation energy) [24] and the possibility to react with an H-passivated surface. In fact, high order precursors do not need free sites to deposit since they can directly react with hydrogen present on the surface. This type of reaction allows to obtain a deposition much less controlled by H desorption. After the disilane molecule brakes to a SiH_3 ligand on the surface, a SiH_4 molecule is created as a byproduct and in turn it reacts with the surface, but this time, with a reaction controlled by hydrogen desorption. The reaction pathway can be expressed as follows [25]:

$$Si_2H_6 + \underline{H} \rightarrow \underline{Si}H_3 + SiH_4 \tag{2.4}$$

$$\underline{Si}H_3 \rightarrow \underline{Si}H_2 + \underline{H} \tag{2.5}$$

$$2\underline{Si}H_2 \rightarrow 2\underline{Si}H + H_2 \tag{2.6}$$

$$2\underline{Si}H \rightarrow 2\underline{Si}_2 + H_2 \tag{2.7}$$

2.2.3 Germanium incorporation

The germane and digermane can be considered very similar to the silane and disilane respectively, with germane that undergoes a correspondent reaction of silane:

$$GeH_4 + 2\_ \rightarrow \underline{Ge} + 2\underline{H} + H_2 \tag{2.8}$$

As in the silane case the adsorption needs two neighboring sites and consequently it is limited by the hydrogen desorption; nevertheless the germane molecules are much more reactive and its activation energy is lower, due to weaker Ge-H bond with respect to the Si-H one. Thus, addition of germane precursor brings an increase of the growth rate with respect to the pure silicon deposition

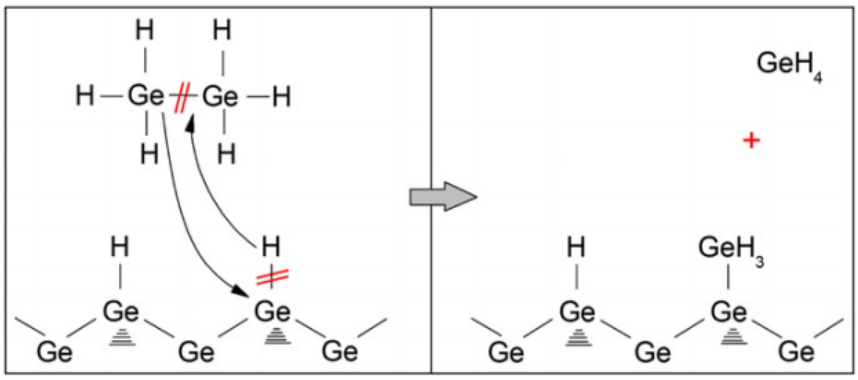


Figure 2.5: Schematic representation of the digermane adsorption mechanism on a fully H-covered surface [26]

[23]. The improvement on the kinetics due to the use of digermane instead of germane, as in the case of disilane, is given by its ability to create its own adsorption site (without a free site available) by using an H atoms to form a GeH_4 molecule as byproduct and leaving a GeH_3 ligand on the surface. This reaction is shown in figure 2.5, and it follows a type of reaction similar to the one seen with Si_2H_4. The germane byproduct will then react with a lower rate through the reaction explained above. The reaction path on the surface through digermane injection can be written as [26]:

$$Ge_2H_6 + \underline{H} \rightarrow \underline{Ge}H_3 + GeH_4 \tag{2.9}$$

$$\underline{Ge}H_3 \rightarrow \underline{Ge}H_2 + \underline{H} \tag{2.10}$$

$$2\underline{Ge}H_2 \rightarrow 2\underline{Ge}H + H_2 \tag{2.11}$$

$$2\underline{Ge}H \rightarrow 2\underline{Ge}_2 + H_2 \tag{2.12}$$

2.3 Selective epitaxial growth

The SiGe S/D epitaxy step is integrated in the CMOS process when structures comprising silicon dioxide and silicon nitride layers. Hence, the deposition should be selective, meaning that SiGe layer must deposit only on exposed silicon regions. To obtain Selective Epitaxial Growth (SEG), an etchant should be added to the vapour chemistry along with the silicon and germanium precursors. Usually, the most used etchant to accompany a DCS/silane + germane chemistry is Hydrocloric acid [27]. The selectivity is possible due to the different growth mechanisms on a monocrystalline substrate with respect to amorphous surfaces such as SiO_2 and Si_3N_4. Whereas on Si and SiGe the adatoms are incorporated in surface steps, on amorphous materials the Si and Ge adatoms need free atoms that act as nucleation centers. The adatoms on these surfaces form small clusters, whose dimensions change with loss or addition of new adatoms. When the cluster dimension reach a critical value, further growth becomes energetically

favorable. Clusters that are smaller than this critical size can be easily etched [28, 29]. Adding the right amount of HCl in the chemistry helps to avoid formation of clusters above critical dimensions and to remove the small ones through the reaction [30]:

$$Si + 2HCl \rightarrow SiCl_2 + H_2 \tag{2.13}$$

A similar reaction is obtained for germanium. The etch rate on Si substrate is lower due to the more stable adatoms. By tuning the HCl low a perfect selectivity can be achieved. The process selectivity is governed by the interaction between the reactive species and the surfaces, for this reason is different in the case of oxide and nitride. Nitride selectivity is usually harder to obtain, probably due to a more stable H passivation on oxide [31]. A important challenge that HCl addition helps to overcome is the pattern dependency. Indeed, two different type of loading effect exist in SiGe deposition: global loading effect (i.e. strong increase in growth rate and slight increase in Ge content switching from a blanket wafer to a dielectric masked wafer) and local loading (i.e. slight increase in growth rate and Ge content going over from a large area to a smaller area in masked substrate). It has been proved that adding HCl to the deposition chemistry minimizes the growth rate pattern dependency [32]. Although typically the selective process are achieved with a co-flow of precursors and HCl etchant, for the low temperature processes a cyclic deposition/etching (CDE) has been developed (i.e. deposition and etch steps are separated) with Cl_2 as etchant. Indeed, HCl etch rate is insufficient for SiGe at temperature below $\simeq$ 450°C (depending on Ge content). Using Cl_2 gives the possibility to greatly reduce the etching process temperature. Use of a cyclic approach is preferred due to the very high etch rate on pure germanium (that is present in numerous future applications), because with this process can be sufficiently capped by SiGe avoiding direct contact with Cl_2 [33].

2.4 Faceting

"Faceting" is referred to the appearance of different crystallographic planes during the growth of a crystal caused by growth kinetic anisotropy. Indeed, the growth rate strongly depends on the crystalline surface considered, resulting in a not uniform deposition but with different facets exposed. Typically, the facets presented are slowly growing planes that limits the growth of the material. Faceting is a prime concern during crystallline films growth. Despite the Si technology development would require a better understanding of the crystal deposition, nowadays this phenomenon is still a controversy basis. It has been postulated previously, that the growth rate variation between different planes is strictly related to different Si dangling bonds surface densities [34].

Experimentally, it results that the ratio between different Si planes' growth rates is in fact nearly constant with respect to temperature variation in the low temperature regime, and rather close to the ratio of their dangling bonds densities. The parameters of the three main crystal planes are reported in Table 2.1. This simplistic view helps to understand the origin of the faceting phenomenon. Un-

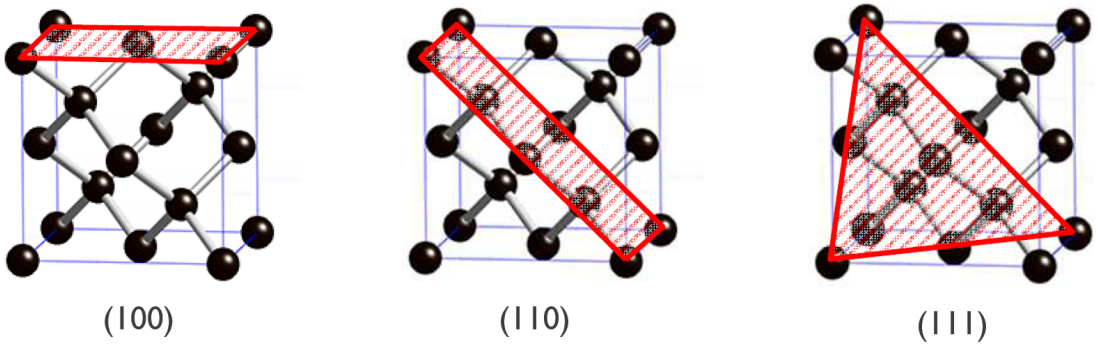


Figure 2.6: Schematic representation of the Si lattice cell with the three major planes highlighted. It is postulated that growth anisotropy comes from different dangling bonds densities. [35]

Plane	Lattice area	Dangling bonds	Dangling bonds density (cm^{-2})
(100)	a^2	4	1.36
(110)	$\sqrt{2}a^2$	4	0.96
(111)	$\sqrt{3}/2a^2$	2	0.78

Table 2.1: Parameters of the three main Si planes. Dangling bonds density is calculated by dangling bonds number present in a single cell plane and the plane area.

fortunately, this is the case only for pure Si deposition, where the growth relies on Arrhenius plot with a determined activation energies, similar for all the faces. In SiGe SEG, the growth kinetics is much more complex. The vapour mixture in the chamber is composed by different gases, material precursors and etchant, each one with its own activation energy and reaction ratios between surfaces. For this reason, a real Arrhenius plot does not exist for this type of depositions. Therefore, the ratios between different surface GR depend on several process conditions (temperature, pressure, chemistry, etc.). For example, (311) facets were known to limit the growth of SiGe deposition in a temperature range down to 750 °C, while at lower temperature they are not appearing [44]. The temperature range in which (311) facets appear obviously can change with variation of process condition. Nevertheless, this effect testify that the final crystal shape depends on a large number of different variables.

Chapter 3

Methodology

In this chapter, the methodology of this thesis work will be explained. The epitaxial process used for the growth of the investigated samples and characterization techniques utilized are presented. Since many characterization techniques have been used during the work, they will be listed in different groups: microscopy techniques, structural and compositional characterization and electrical characterization.

3.1 Reduced Pressure CVD Epitaxial growth

As explained previously, epitaxy refers to a specific type of deposition where the deposited layer follows the substrate crystalline structure and orientation. This particular growth is usually obtained using Molecular Beam Epitaxy (MBE) or Chemical Vapor Deposition (CVD). These two techniques in turn subdivide in numerous sub-techniques depending on the growth parameters, like Plasma-Assisted MBE (PAMBE), Plasma-Enhanced CVD (PECVD), Ultrahigh Vacuum CVD (UHVCVD). In this work, the studied layers have been grown using Reduced Pressure CVD in an ASM Intrepid XP cluster designed for 300 mm production. CVD is a technique that allows the growth of high quality thin films through

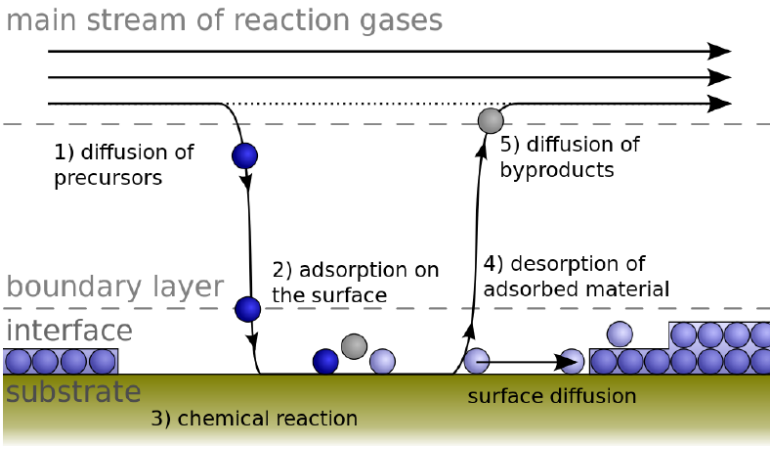


Figure 3.1: Steps of a chemical vapor deposition process

Figure 3.2: ASM Intrepid XP, RPCVD tool used to grow the samples

volatile precursors that react chemically and/or decompose on the substrate surface. The volatile by-products created during the reactions are removed by the carrier gas flow through the chamber. The carrier gas used in the processes is H_2, that has demonstrated to be the most promising in terms of selectivity [33]. Reduced pressure is used to limit any unwanted gas phase reactions and increases the uniformity across the substrate. This growth technique also allow in situ doping. This is achieved by injection of a dopant-containing gas in the chamber. For example, inserting B_2H_6 alongside Si_2H_6 and Ge_2H_6, results in Boron doped Silicon-Germanium. Thus, with respect to implantation technique, two steps (implantation and activation annealing) are substituted by a single Deposition/Doping process. Furthermore, since the impurity atoms tend to occupy substitutional positions, usually no post-epitaxy thermal treatment is required.

3.2 Microscopy techniques

The resolution of microscopy techniques is limited by the diffraction effect, and in the case of optical microscopy it is of the same order of the radiation wavelenght. For this reason, in order to see a feature at nanoscale level, imaging techniques utilize electrons for increasing the resolution. In the case of electron microscope, the resolution is limited by the De Broglie length, which is much lower than the visible light wavelength. In this work Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM) have been used and will be discussed further.

3.2.1 Scanning Electron Microscopy

The scanning electron microscopy is a technique that produces images by scanning the sample with a high-energy beam of electrons. The interaction between the electrons beam and the sample generates back-scattered electrons (BSE),

secondary electrons (SE), and characteristic X-rays. The BSE are electrons reflected back after an elastic interaction with the surface while SE are electrons originated from inelastic interactions. Different detectors are installed to collect different signals and produce the images. Each signal has a different role in the images acquisition: SE are responsible for showing morphology and topography of the sample while BSE are most valuable for illustrating contrast in composition. In the present work SEM has been used to analyze morphology of the grown layer in order to check relaxation or surface defects, as well as to observe selectivity of the processes.

3.2.2 Transmission Electron Microscopy

The Transmission Electron Microscopy (TEM) is an electrons-based microscopy technique which utilizes transmitted through the sample electrons. To allow the transmission of an electron beam the sample should be previously prepared. Thanks to a Focused Ion Beam a very thin lamella ($\sim$ 50 nm thick [37]) is produced from a specimen. This implies that TEM is a destructive and very expensive technique, due to the complex sample preparation. The main components

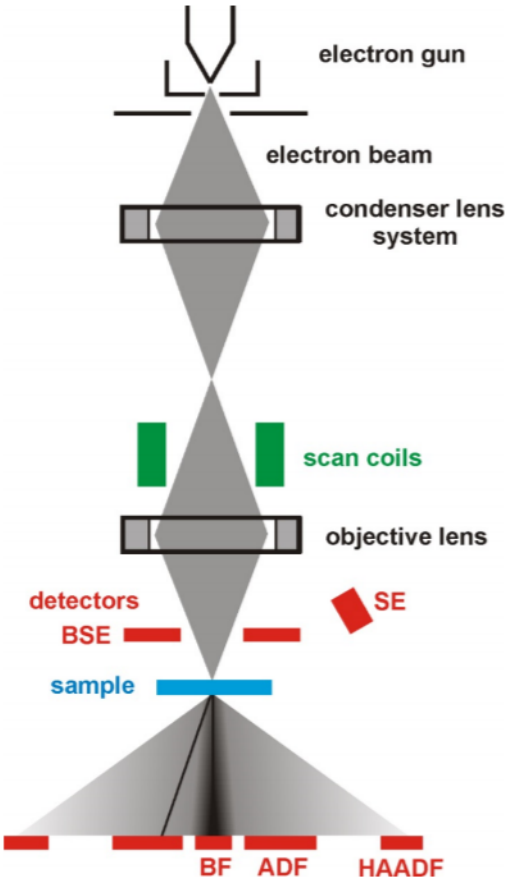


Figure 3.3: Scheme of a scanning transmission electron microscope that shows the main components and the electrons path. The detectors are positioned after the thin sample. Here are present the bright field detector (BF), the annular dark field detector (ADF) and high angle annular dark field detector (HAADF) [38]

of a TEM are an electrons gun, electromagnetic lenses, and a camera, assembled in a vertical column in vacuum. There are two different types of TEM: Conventional TEM (CTEM) and Scanning TEM (STEM). CTEM is a wide-beam technique, where the electrons impinge the entire area of interest and the image, formed by an objective lens, is collected in parallel. STEM utilizes a focused beam, formed by an apposite lens before the specimen, that scans the surface collecting information of each pixel in series. The STEM point by point analysis allows to obtain a higher sensitivity and this configuration is used in the present work. Furthermore, STEM configuration allows to use different types of detectors obtaining images with contrast depending on different sample's characteristics. In particular, in this thesis Annular Bright field STEM (ABF-STEM) has been intensively ysed. In this configuration an annular detector is used, that collects electrons in an angular range between α and $\alpha/2$, where α is the probe-forming aperture semiangle [39]. The ABF-STEM contrast is determined by the degree of crystallinity of the scanned sample. The STEM tool used also allows to obtain elemental mapping of the sample through energy-dispersive X-rays analysis (EDS).

3.3 Structural properties and compositional analysis

Now the techniques used to characterize structure and composition of the layers are described.

3.3.1 X-Ray Diffraction

X-Ray Diffraction (XRD) is a technique that allows to determine the crystalline structure of the grown material. Crystals are made of atoms arranged in an ordered manner. The crystalline structure is composed by repeated atomic planes defined by Miller indices. X-Ray impinging the substrate are elastically scattered by the atomic planes, producing constructing interference when the Bragg's Law (3.1) is satisfied (3.4)

$$2dsin\theta = n\lambda \tag{3.1}$$

Where d is the interatomic distance, θ is the incident angle, n is an integer and λ is the X-Ray wavelength. In an XRD setup, a detector is placed into a goniometer in order to take the intensity of the radiation in function of the angle, as shown in Figure 3.5. Knowing the radiation wavelength and measuring the angles that generate the Bragg's peaks, the distance between planes can be calculated. In fact, since a crystal is formed by many planes with different orientation and interatomic distance, numerous peaks will be present, each related to a specific family of lattice planes. In our work two special setups are used: the Bragg-Brentano configuration ($\omega - 2\theta$ scan) and the X-ray Reflectivity (XRR). The tool used for our measurements is "JVX 7300LM" by Jordan Valley.

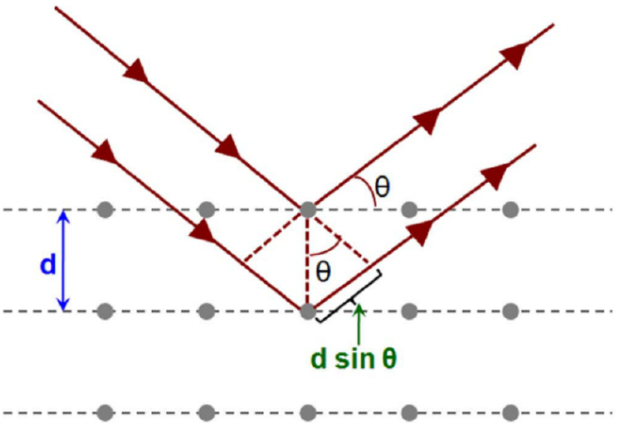


Figure 3.4: Incident and reflected X-Rays on lattice planes

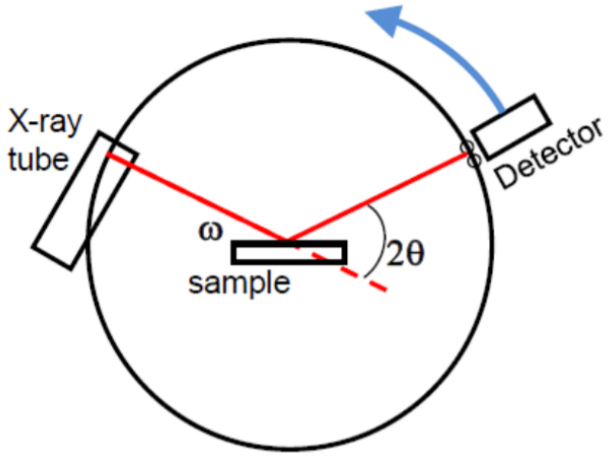


Figure 3.5: Typical XRD setup with a detector moved on a goniometer

$\omega - 2\theta$ scan

In the $\omega - 2\theta$ scan the X-ray source and the detector are rotated in a coupled way in order to analyze only a specific direction (Bragg's peak), called diffraction vector. In our case the direction scanned is (400), by tilting the sample is possible to measure another direction. Analyzing SiGe layers on Si substrate, two main peaks will be present in this type of data: the Si peak and the SiGe one. Indeed, as already mentioned in chapter 2, the SiGe layer is grown pseudomorphically, hence maintaining the in-plane lattice constant of the silicon. Contrary to this, the out-of-plane lattice constant should change in order to keep the same cell volume of bulk SiGe, allowing detection by this type of scan. The relative position between the two peaks will provide information about anything that can change the lattice parameter of the SiGe layer, Ge concentration and degree of relaxation. Moreover, a layer thickness can be extracted from the peak width and interference fringe that are formed next to it. A plot of this type of measurement is reported in Figure 3.6. Thickness and germanium composition are found by fitting the raw data using the software furnished by the tool producer.

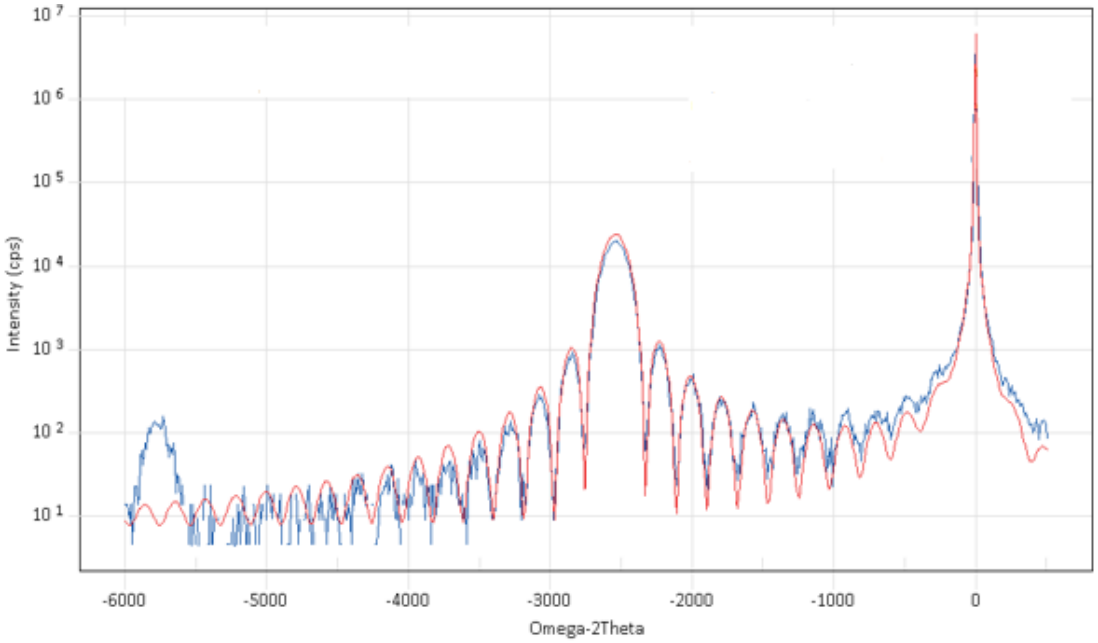


Figure 3.6: An example of $\omega - 2\theta$ scan, where the silicon substrate peak at $\omega - 2\theta$=0 and the SiGe peak is at $\omega - 2\theta \approx$-2600(arcsec). Numerous interference fringes are visible, allowing thickness extraction.

XRR

XRR technique is always based on X-rays interference, but between rays reflected at interfaces of different materials. For this reason, it is not needed that the sample is crystalline and XRR works for every type of layer. Indeed, in the case of a SiGe layer on Si, the interference fringes are not caused by scattering with atomic planes but by interference of the rays reflected at vacuum-SiGe and SiGe-Si interfaces. When X-rays impinge a substrate, the reflectivity plot in function of the angle is exponentially decaying as soon as the incidence angle becomes smaller than the total reflection angle. When a thin layer of another material is deposited on top of the substrate, the interference pattern is superimposed to the exponential behaviour, thus generating fringes on the reflectivity plot. The fringes periodicity in this type of data is strongly sensitive to the layer thickness, and with the fitting software it can be precisely determined. Although the data acquisition is similar to XRD, moving the X-rays source and the detector at different angles, the length scale are different. In XRD, interference is generated by plane distance in the range of few Armstrong, and according to the Bragg's law, the Bragg's angle is typically in the order of tens degrees. In XRR the layer thickness is typically much higher, and the interference pattern periodicity is in a much smaller angular scale, usually few 0.1 degrees. This difference in the scanned angular range is the main variation between XRD and XRR experimental setup. In Figure 3.7 an example of XRR plot is reported, it is possible to see the interference fringes superimposed on top of the typical exponential decay.

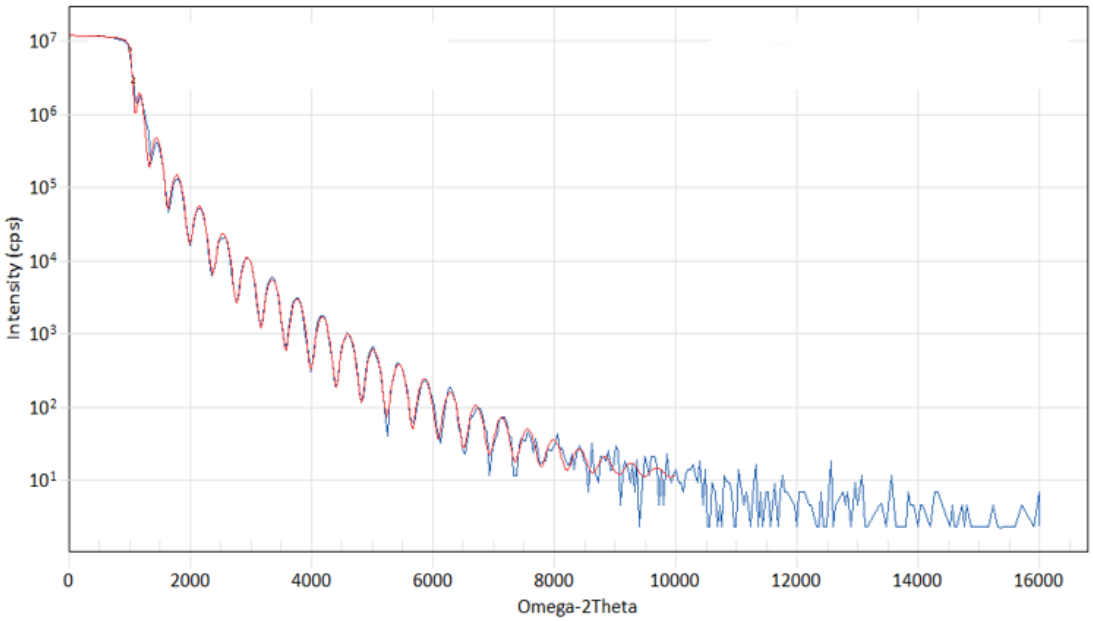


Figure 3.7: A typical XRR profile. The reflectivity is measured next to the total reflection angle, where it decreases exponentially.

3.3.2 Secondary Ion Mass Spectroscopy

Secondary Ion Mass Spectroscopy (SIMS) is a technique that allows to obtain the elemental composition of a thin film. An ion beam is impinged at the sample, causing an emission of secondary ions through scattering on the surface. The emitted ions are then collected by an electric field and their mass is analyzed with a mass spectrometer. To avoid any contamination or scattering with the

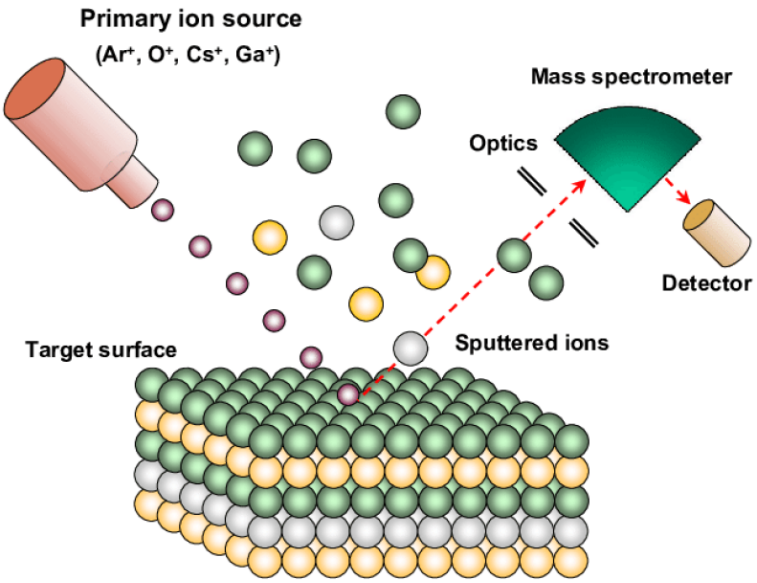


Figure 3.8: Schematic of SIMS way of working

gas, the chamber should be in vacuum. SIMS is a destructive technique due to substrate sputtering necessary for ions emission. Although only 1% of the atoms that leave the surface are charged, their spectrum gives a precise quantification of the various elements abundance in the sample. Furthermore, analyzing the variation of the signal for each element and controlling the sputtering rate, an elemental depth profile is also obtainable. Elemental detection precision is in a range from one per million to one per billion, while a depth resolution of 1 nm can be achieved.

3.4 Electrical characterization

Finally, the techniques used to obtain electrical properties of the layers are described. Such techniques allow to measure sheet resistance, active carrier concentration and mobility.

3.4.1 Micro-four-point probe measurement

Micro-four-point probe ($\mu 4PP$) is a measurement that allows to obtain sheet resistance (R_s) of a thin film layer. Sheet resistance is a measure of resistance used to characterize layers of homogeneous thickness, and it is expressed as:

$$R_s = \frac{\rho}{t} \tag{3.2}$$

Where ρ is the resistivity and t the thickness. R_s is defined as the resistance of a square of the thin film, with the current implied to flow along the plane of the sheet. Indeed, the equation 3.2 is obtained by the classical resistance equation with equal length and width, hence simplified. The importance of this parameter in the thin films characterization is due to its invariability under scaling of the contact, being the same regardless of the square size. This allows to characterize and compare samples of different size. The $\mu 4PP$ technique allows to measure

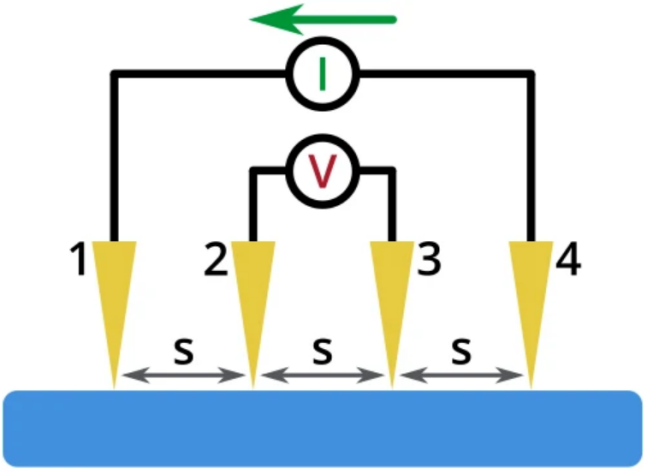


Figure 3.9: Schematics of in-line Micro-four-point probe

R_s excluding the contact resistance of the probes. It is formed by four probes: a constant current flows on two probes and the voltage is measured with the other two. A geometry factor needs to be applied, depending on the geometry of the probes, to extract the sheet resistance. The most common geometries are square and in-line. In our measurements an in-line array has been used, a simple scheme is reported in figure 3.9.

3.4.2 Micro Hall effect

In heavily doped samples, not all the dopants are active. While M4PP gives the resistance it is not able to yield individual contribution of mobility (μ) and active carrier concentration (N_S), Micro Hall Effect (MHE) measurement allows to separate the two quantities. MHE is alsp measured using a collinear 4-point probe but in proximity of a boundary. In our instrument the probe is formed by 7 points (Figure 3.10), but each single measurement utilizes only 4 points: measurements are performed separately using probes 1-2-3-4, 4-5-6-7 and 1,3,5,7, being de-facto three M4PP. Performing several measurements with "sub-probes" of different pitch, allows to quantify the distance from the layer edge, needed for physical quantities extraction. Together with the boundary requirement, MHE measurements also needs a magnetic field applied perpendicularly to the layer. In fact, the Hall effect consists in the production of a voltage difference in a conductor, transverse to an electric current and to an applied magnetic field perpendicular to the current. As a result, the sheet current density and the electric field are no longer parallel, and they are related by a sheet resistance tensor rather than a scalar sheet resistance. The tensor contains the sheet resistance (R_S) and the Hall sheet resistance (R_H), that can be individually measured. N_S and μ can be calculated from these two equations [40]:

$$N_S = \frac{B_Z}{ZeR_H} \tag{3.3}$$

$$\mu = \frac{ZR_H}{R_S B_Z} \tag{3.4}$$

Where B_Z is the applied magnetic field and $Z = \pm 1$ is the charge carrier type. Measurements in this work have been done by using a CAPRES CIPTech-M300.

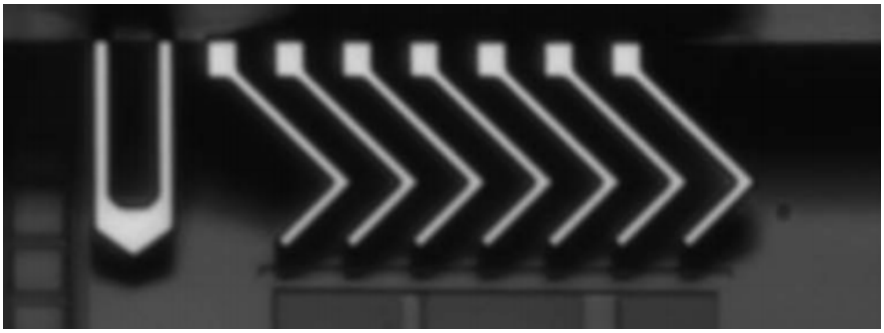


Figure 3.10: A head with 7 probes used to measure mobility and active carriers concentration by the Micro Hall Effect

Chapter 4

SiGe:B:Ga experimental results

In this chapter the results obtained during study of SiGe in situ co-doping with Gallium and Boron will be presented. After a brief introduction of the samples and their basic properties, influence of laser annealing at different temperatures on SiGe:B:Ga.

4.1 Samples description

In the course of this experimental work many samples with very different process conditions were used. For this reason, we face a difficulty of more than one parameter changed, which make analysis rather difficult. Only the most interesting results will be described in detail here.
The lot used counts of 23 samples prepared on 300 mm Si(100) wafers. The SiGe layers are grown through a low temperature deposition, using Si_2H_6/Ge_2H_6 as precursors mixture at 400°C and H_2 as carrier gas. In-situ doping is obtained by co-flowing gas precursors containing Ga and B together with Si and Ge precursors. B_2H_6 has been used for Boron while Tri-tert-butylgallium TTBGa (figure 4.1) was the choice for Gallium precursor. Some layers have been grown using cyclic deposition/etching approach, applying Cl_2 as an etchant. Furthermore, all the wafers had stripes of oxide distributed on the surface, helping to study selectivity of the process and allowing electrical characterization by micro-hall technique.

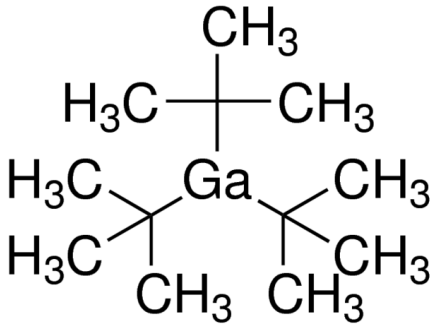


Figure 4.1: Schematic representation of the Tri-tert-butylgallium molecule

The samples are divided in three main groups: only B doped samples, samples grown by CDE recipe with Ga and B co-doping and finally samples submitted to a post deposition in-situ hydrogen annealing presenting a set of 3 wafers doped only with Ga. Next the main characteristics of the different sets of samples will be presented.

4.1.1 SiGe:B samples

As mentioned above the first set of samples is SiGe:B. These sample will serve as reference for the successive samples, where Gallium precursor is added, for comparison of morphological and electrical properties. The main recipe features are presented in Table 4.1 : in particular, there are two series of samples with different digermane flows and three different level of doping.

Name	Ge_2H_6 flow rate	B_2H_6 flow rate
Sample A1	5 a.u.	0 a.u.
Sample B1	5 a.u.	0.5 a.u.
Sample C1	5 a.u.	60 a.u.
Sample D1	9 a.u.	0 a.u
Sample E1	9 a.u.	0.5 a.u.
Sample F1	9 a.u.	30 a.u.

Table 4.1: Process conditions used to grow SiGe layers of the first group

In-line top-view SEM inspections were performed both on Si (where SiGe is deposited) and on SiO_2 (to study selectivity). In Figure 4.2 two samples with no doping and different amount of Ge are shown. One can notice a good morphology of the SiGe deposited on the Si substrate, while on SiO_2 some SiGe particles are observed. The number of SiGe particles on SiO_2 dramatically changes for the B-doped samples, as shown in Figure 4.3. It's clear that with a higher diborane flow a total loss of selectivity appears, resulting in a full oxide coverage by SiGe. This could be brought from an exceeding GR, that could prevent the etchant gas to remove successfully the deposited material. Nevertheless, we know that this effect is also consequence of an autocatalytic dissociative chemisorption of B_2H_6 on silicon oxide, letting the surface be more reactive towards gas precursors [41]. Regarding the morphology of the grown layer there are not clear differences with the addition of doping, apart from the samples with the highest concentration. In that case, the surface becomes rough probably due to B concentration exciding, causing clustering of the atoms that can not be incorporate in the crystal structure.

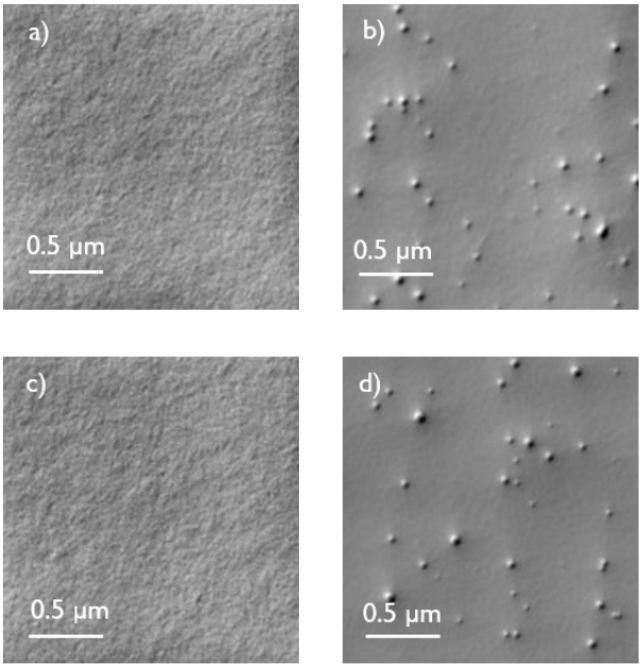


Figure 4.2: SEM inspections of the not-doped samples: a) Sample A1 deposition on Si, b) Sample A1 deposition on SiO2, c) Sample D1 deposition on Si, d) Sample D1 deposition on SiO2

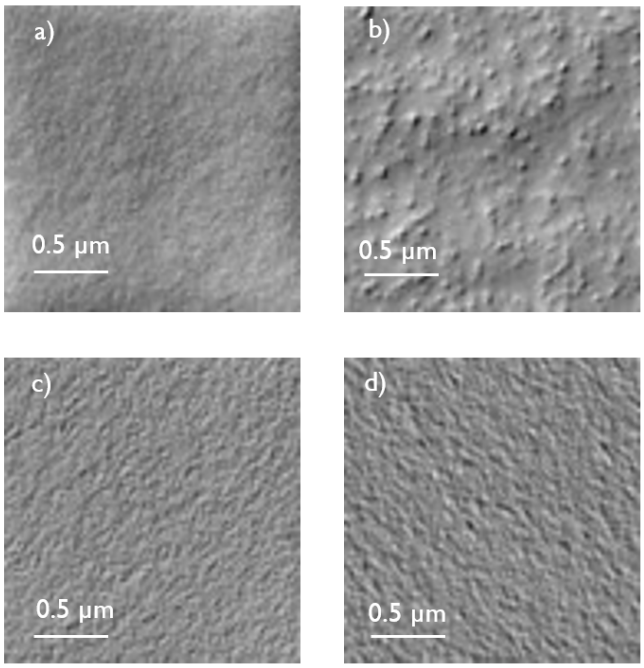


Figure 4.3: SEM inspections of the B-doped samples: a) Sample F1 deposition on Si, b) Sample F1 deposition on SiO2, c) Sample C1 deposition on Si, d) Sample C1 deposition on SiO2.

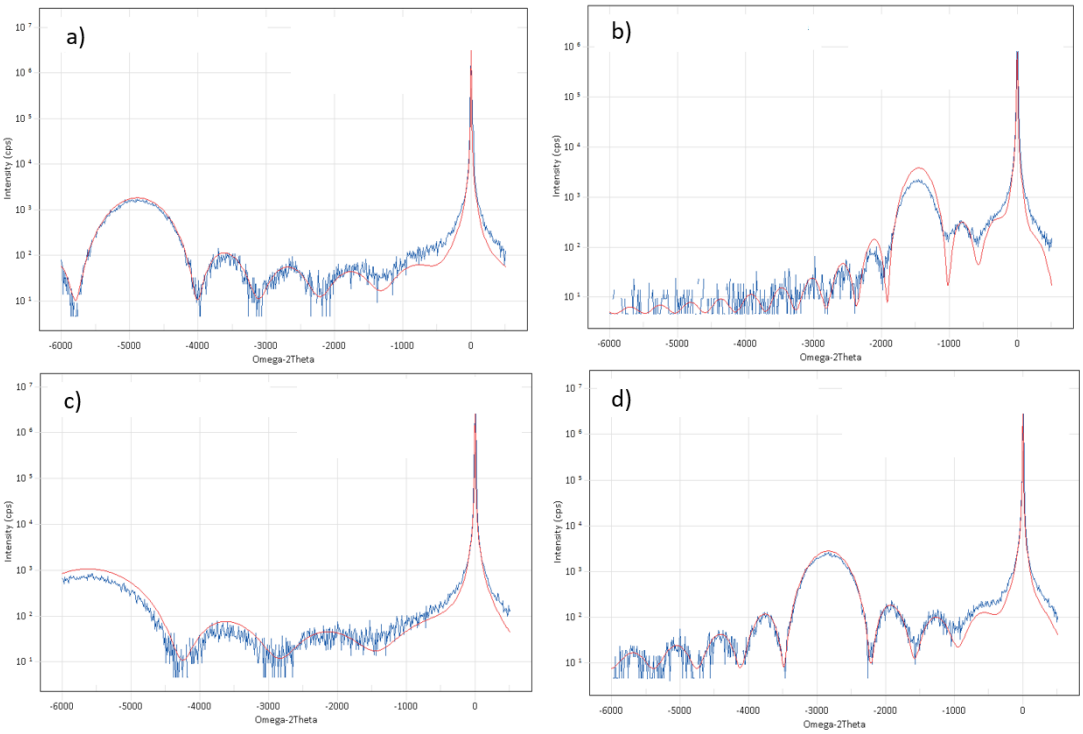


Figure 4.4: XRD profiles of the SiGe doped layers: a) Sample B1, b) Sample C1, c) Sample E1, d) Sample F1.

The layers thickness and the germanium percentage were measured by HRXRD. As will be seen, the layer thickness generally is not uniform throughout the entire wafer, showing a centrosymmetric profile. For this reason each wafer was measured at different points of the radius, to obtain the actual thickness for a particular zone. Typical measurements performed at the centre of the wafers are shown in Figure 4.4. Together with the raw data the fit of the curve done with an appropriate software is shown. Values of thickness and germanium percentage are found from the fit. The differences in the thicknesses are due to different growth rates and the deposition time chosen to avoid relaxation.

The germanium concentration behaviour is not straightforward. At a first glance the Ge concentration in the SiGe layer depends only on the digermane flow, in particular in its ratio with respect to the disilane one. Nevertheless, from the XRD results one can see that at constant disilane and digermane flows the Ge concentration varies with diborane flow; more precisely, the Ge concentration decreases with increasing dopant flow. The Ge percentage found from HRXRD is called "apparent", because it depends on the out-of-plane lattice constant of the layer which can be influenced by other elements (for example B is smaller than Si or Ge causing compensation effect). A strong Ge concentration change can not be explained only by compensation effect and it's likely that the Ge_2H_6 and B_2H_6 are competing with each other during deposition. The growth rate and the germanium percentage as function of the diborane flow are shown in the graph 4.5. To characterize our sample electrically two different measurements have been done: a sheet resistance scan through the entire diameter with the micro four point

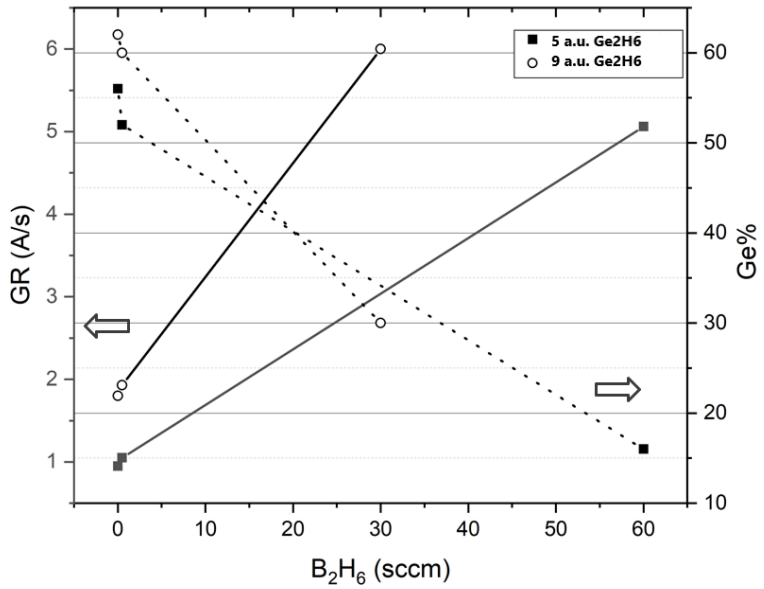


Figure 4.5: Growth rate (right axis) and germanium percentage (left axis) in function of different diborane flows at fixed digermane flow.

probe and a Micro-Hall effect measurement at the edge of an oxide stripe presents on the wafers. A typical profile of the sheet resistance across a diameter is shown in Figure 4.6, where symmetric variation are due to the thickness changes caused by the wafer rotation during SiGe deposition. Resistivity can be found using the sheet resistance and the thickness profile applying a simple equation:

$$\rho = R_s \cdot t \tag{4.1}$$

The measured points that not follow the profile but are much higher than the neighbors are due to measurements done on the stripes of oxide.

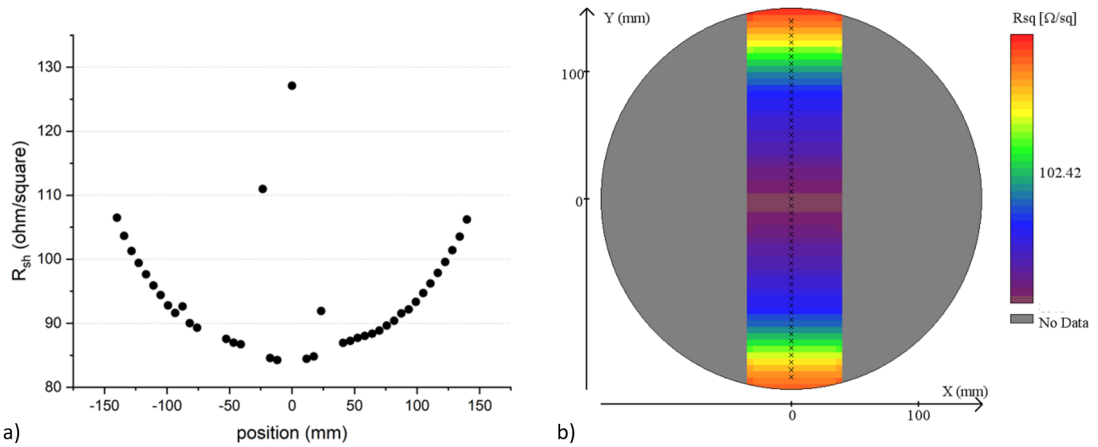


Figure 4.6: a) Example of sheet resistance measurement (Sample F1) along a diameter through Micro 4-point probe. b) The measured points on the wafer are displayed with a color scale for data visualization.

4.1.2 SiGe:B,Ga CDE samples

The second group is composed of six samples, grown by cyclic deposition/etching process. The first one, without Ga doping, is used as reference. Besides Ga doping during the deposition step of SiGe together with diborane, some samples had TTBGa spike before each cycle in an attempt to increase gallium doping. The Ga spike deposition time was varied for the different wafers. On top of that small changes have been done compared to the reference (e.g. different ratio between deposition and etch timee). SEM pictures and the XRD spectrum of the reference sample are presented in figure 4.7(a),(b),(c). A good morphology of the layer can be observed with some clustering appearing on the SiO_2 despite the addition of the etching step, showing a not perfect selectivity. With addition of Ga precursors it has been raised the deposition and etch steps duration. This was necessary due to delay in Ga incorporation shown in previous experiment. For this reason, a considerable Ga concentration is achieved after some nanometers of deposition and the deposition step can not be too short. SEM inspections (4.7 (d),(e)) clearly show that the roughness of the surface is increased and this time the oxide is fully covered, meaning that the etching step is too short to remove the layer grown on SiO_2 during long deposition step. The XRD spectrum also testifies a bad morphology of this layer, because the Bragg's peaks are not resolved. To obtain the thickness of the layer XRR has been performed. To get a higher gallium concentration without layers morphology deterioration a different strategy has been used: the deposition/etch time similar to the reference, with addition of Ga spikes of different durations before each cycle. The growth details of the presented samples of this group are described in table (4.2):

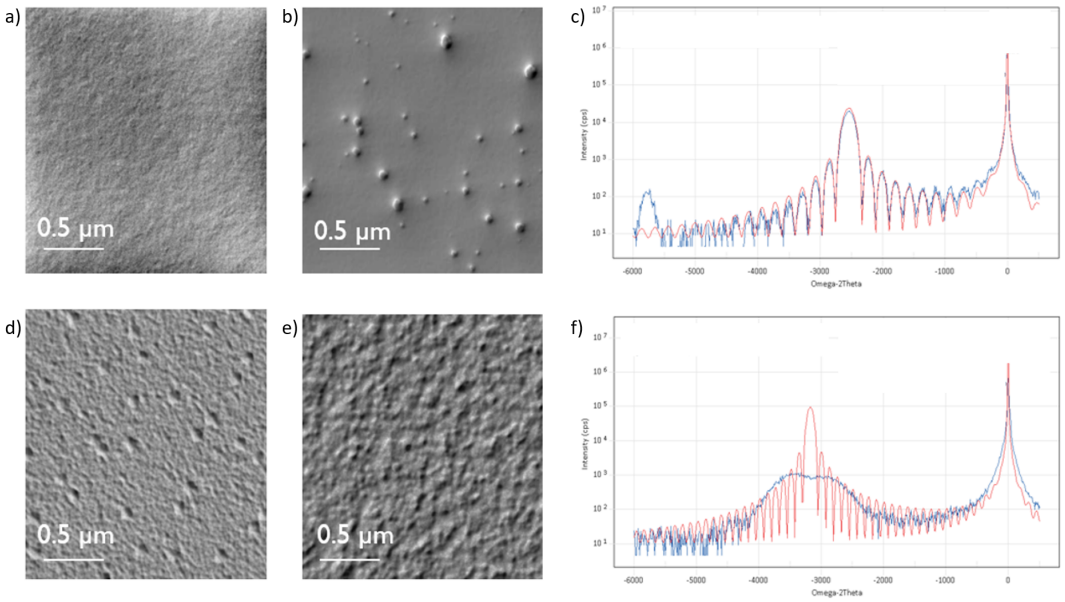


Figure 4.7: a),b) SEM images of sample reference 2 respectively on silicon and silicon oxide. c) XRD profile of samples reference 2. d) e) SEM images of sample A2 respectively on silicon and silicon oxide. f) XRD profile of samples A2.

Name	TTBGa flow rate	Ga spike time	Dep/etch time (s)
reference 2	0	-	15/3
Sample A2	9.5 a.u.	-	60/15
Sample B2	9.5 a.u.	30 s	15/3
Sample C2	9.5 a.u.	60 s	15/3
Sample D2	9.5 a.u.	600 s	15/3

Table 4.2: Process conditions used to grow SiGe layers of the second group

As can be seen from the SEM pictures (4.8), the SiGe layers show good morphology for low Ga deposition times, while the third one, with the longest spike deposition time, shows rough surface with completely covered oxide. The increased roughness can be due to possible exceeding of the Ga solubility limit, while the total loss of selectivity can be due to the formation of a very thick Ga layer on the oxide that could not be removed by the etching step. The XRD results bring very interesting outcome: the addition of the Ga spike lowers the growth rate of the SiGe layers. An increase of Ga spike duration brings a SiGe GR decrease. Considering that the the etching rate and the growth rate could not be separately calculated, this effect could be attributed to both an increase of the etching rate of the layer with higher Ga concentration, or an effective deterioration of SiGe growth on Ga layer deposited after spike.

The carrier concentration has been calculated using micro-Hall measurements and is reported in Figure 4.9. We can see that total active concentration does not show a clear improvement, with all the samples in the same range apart for the one with longest Ga deposition time where a decrease is noticeable. Also if

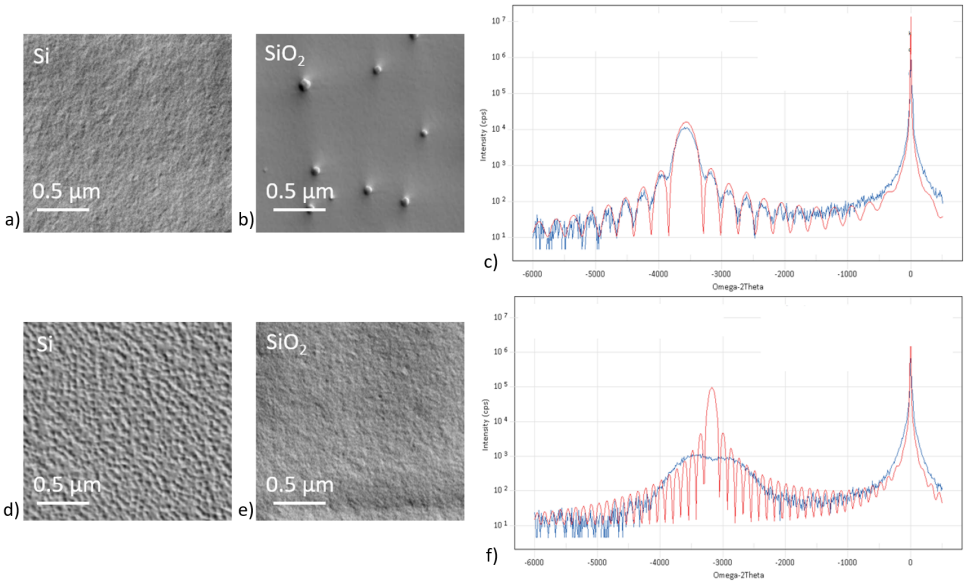


Figure 4.8: : a),b) SEM images of sample C2 respectively on silicon and siliconoxide. c) XRD profile of samples C2. d) e) SEM images of sample D2 respectivelyon silicon and silicon oxide. f) XRD profile of samples D2.

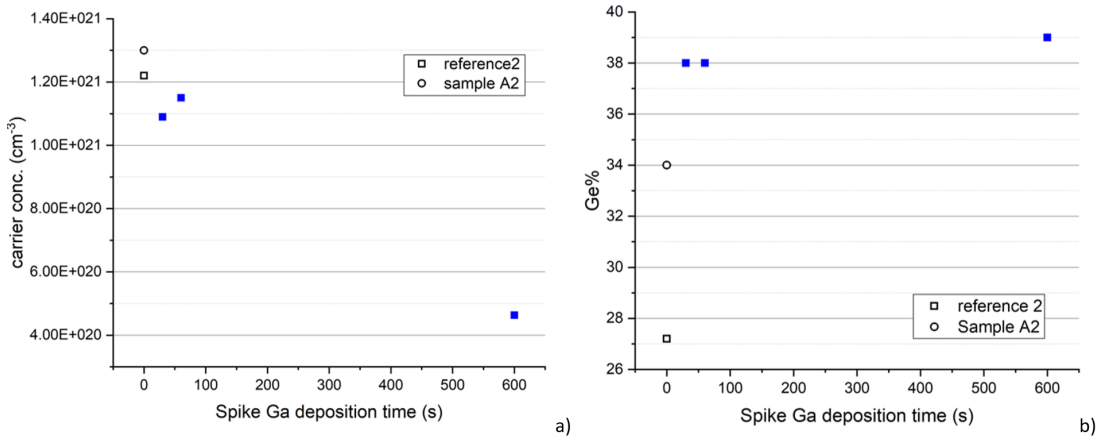


Figure 4.9: a) Active carrier concentration through MHE in function of spike Ga deposition time, b) Germanium percentage found by XRD profile in the SiGe layers in function of spike Ga deposition time

an increase in doping concentration through Gallium is not visible, these layers demonstrate an important result: with B and Ga co-doping its possible to achieve the same active doping concentration but with higher Ge content in the layers. We already know that a strong competition between Ge_2H_6 and B_2H_6 exists, but this competition is not so strong between Ge_2H_6 and TTBGa: the trend is clear in the figure 4.9(b), where the Ge percentages from XRD fitting are reported.

4.1.3 SiGe:B,Ga samples / in-situ H2 annealed

The last group of the samples consists of two series of wafers submitted to an in-situ H_2 annealing with the aim of reduce the roughness of the layer. These samples have been grown with single step deposition. Three SiGe samples which are only Gallium doped and three wafers B and Ga co-doped. For each serie one sample has been kept without hydrogen annealing for a reference, while the other two received a 450°C and 500°C annealing respectively. A summary of the samples is reported in the following Table (4.3):

Name	TTBGa flow rate	B_2H_6 flow rate	H_2 anneal T (°C)
Ga ref 3	2 a.u.	7 a.u.	-
Sample A3	2 a.u.	7 a.u.	450
Sample B3	2 a.u.	7 a.u.	500
B-Ga ref 3	4 a.u.	7 a.u.	-
Sample C3	4 a.u.	7 a.u.	450
Sample D3	4 a.u.	7 a.u.	500

Table 4.3: Process conditions used to grow SiGe layers of the third group

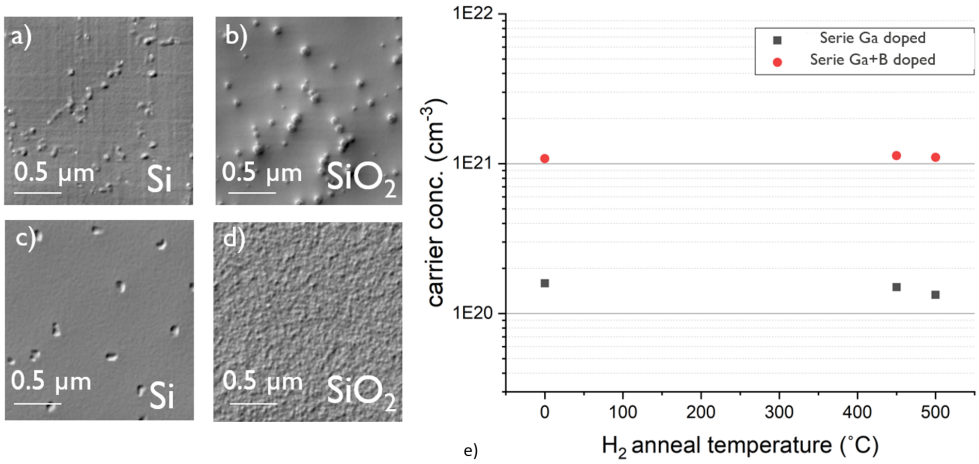


Figure 4.10: a),b),c),d) SEM images, on Si and SiO_2, of samples Ga Ref 3 (a),(b) and B-Ga Ref 3 (c),(d). e) Carrier concentration through MHE of the samples in function of annealing temperature

The duration of the hydrogen annealing was 10 minutes. How can be seen from the SEM pictures of the two reference samples (4.10), these two recipes resulted in layers with clustering on the surface and some relaxation can be observed in the Ga-doped sample. As expected, the sample doped with B shows full oxide coverage by SiGe due to absence of intrinsic selectivity in these process. The samples submitted to the annealing did not show any improvement in the morphology of the samples, but also no extra relaxation occurred due to thermal budget. Electrical characterization testified that annealing was not effective for dopant activation neither, since the carrier concentration of the annealed samples is equal to the reference one (Figure 4.10(e)). Finally, wet HCl clean typically used for Ga removal from the surface was applied without success, suggesting that the particles seen on the surface are not formed by pure Gallium but SiGe.

4.2 Laser annealing results

After the analysis done in the previous section, the samples have been submitted to a laser annealing at different temperatures. Purpose of this experiment is to observe the behaviour of the Ga doping under this treatment, in particular to analyse activation/deactivation of dopants and their diffusion in the layer or in the substrate. We already know from previous experiments that Ga tends to concentrate at the surface of the layer, effect that can help to lower the contact resistivity; we are also interested to see if a further pile-up of dopants on the surface can take place under laser annealing. To obtain the results of the annealing at different temperatures, each wafer has been divided in five zones, each one submitted to a laser annealing at a specific temperature, in a range from 800°C to 1100°C. In Figure 4.11 the different zones characterized by their own temperature are shown. The annealing duration is 1 μs and the central stripe is left without annealing for reference.

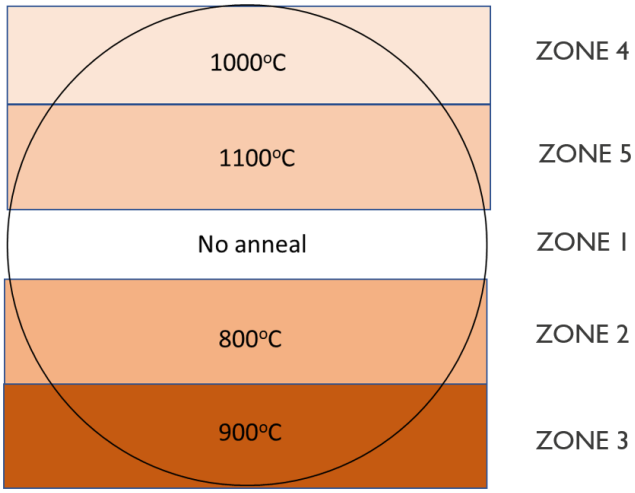


Figure 4.11: Schematic of the zones into which each wafer has been subdivided and the relative LA temperature.

4.2.1 Electrical characterization

To obtain the influence of the different temperature laser annealing on carrier activation/deactivation, the carrier concentration should be found in each different zone of the wafer. To do so, micro-4PP scanning sheet resistance measurement has been done along the diameter crossing perpendicularly all the zones, while thickness was extracted from HRXRD at different points along the radius of the wafer. Due to the centrosymmetrical thickness profile every radius could be measured. Through sheet resistance and thickness, in each point the resistivity has been calculated, and from the latter the carrier concentration can be obtained by the characteristic resistivity in function of active carrier concentration. Being the characteristics of Germanium and Silicon slightly different due to differences in mobility, the calculus will take care of the Ge percentage in the SiGe layer doing a weighted average of the two results. After a first evaluation of the most meaningful samples, micro-Hall measurements are separately performed in each chosen zone of the samples to obtain the separated contribution of mobility and carrier concentration. The majority of the samples did not show significant differences in results after the annealing treatment: the carrier concentration rely on the same range for all the zones and the sheet resistance is characterized by the usual symmetric profile. Some wafers exhibit a start of relaxation at the highest temperature annealed zone, and in that point the resistance profile has a distortion from the usual profile. In correspondence of relaxation and a change of resistance, also the calculated carrier concentration will change, but this is only an apparent artifact because at this stage we are not taking into account possible mobility changes. Examples of such results are listed in Figure 4.12, where the reference of the second group and a lightly doped samples of the first one are reported.

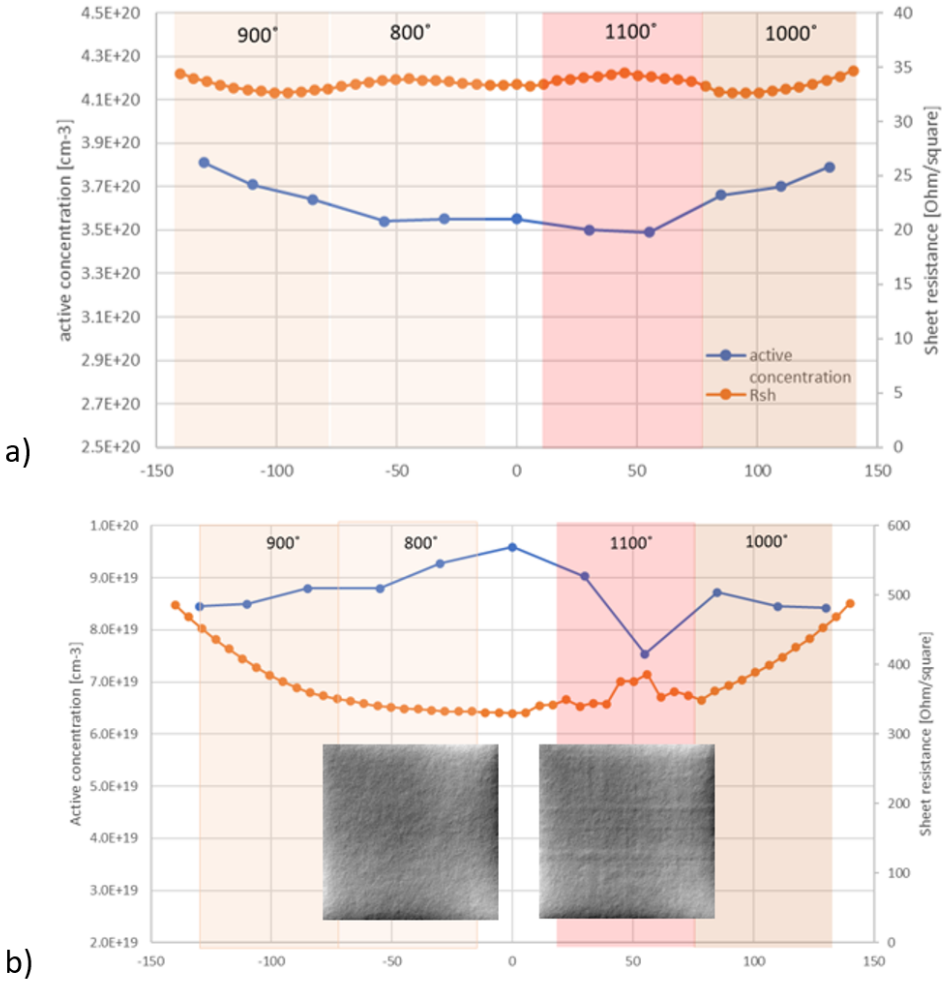


Figure 4.12: Examples of sheet resistance measurement through the diameter of the wafers. In this cases there is no clear evidence of LA effect on carrier concentration. a) Sample Reference 2. b) Sample B1.

Only two wafers showed an abrupt step between the zones in the resistance profile. Both samples exhibit a visible "jump" in the sheet resistance in the zone 5 (highest temperature), and less marked differences or no differences at all between the others. This two wafers C1 and E1 belong to the first group, so they contain only B as a dopant. Nevertheless, these two samples showed an opposite behaviour in the zone 5, with E1 increasing consistently while C1 reducing resistance in that zone. At this point, we can suppose this effect is brought by different morphology between the two samples: indeed, as shown in the inserts of Figure 4.13, we know that C1 is characterized by a very high doping and we supposed from the surface roughness that the B concentration was beyond the solubility limit, while D1 is lightly doped and shows good surface morphology. While the lightly doped sample shows relaxation in zone 5, that can cause the higher resistance observed, the morphology of the very highly doped sample can be considerably improved by the high temperature annealing. In fact, B atoms in interstitial sites can be helped to move to a substitutional site. This brings dopant

activation and an improvement of the layer's cristallinity, leading to the notable decrease in the resistance observed. Finally, the difference that exists between samples B1 and E1, both lightly doped, can be caused by the higher Ge content of the latter, that leads to a higher degree of relaxation.

Regarding the Ga doped samples, as already mentioned, none of them showed abrupt steps between different zones. The majority of them only exhibit a little step between zone 5 and the other zones. Examples of typical resistance profile for such samples, are reported in Figure 4.14, samples A2 and B2 of the second group. The small improvement given by the high temperature laser annealing is visible in almost every sample of this group.

The samples presented above, being the most interesting, have then been measured by MHE, to further understand laser annealing effect and if there are any mobility improvements. This type of measurement is ideally conceived for conductor samples. For this reason not all our wafers gave acceptable data, in particular

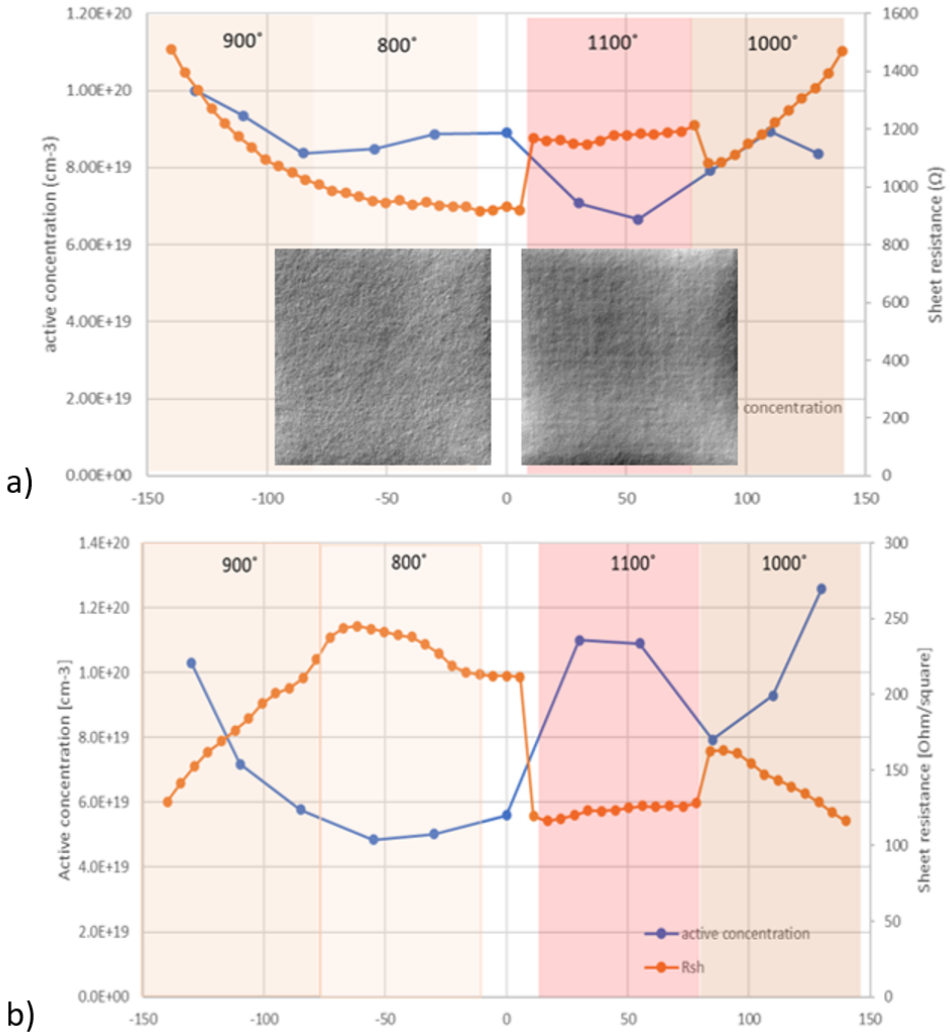


Figure 4.13: Sheet resistance profile examples where abrupt jumps due to laser annealing are visible. a) Sample E1. b) Sample C1.

for the lowly doped layers this technique was not available. The results obtained are shown in the graphs in figure 4.15. It is interesting to observe how in the C1 sample both the active carrier concentration and the mobility increase with the annealing temperature increase, giving rise to the net improvement visible in the resistance profile. Contrariwise, the Ga-doped samples exhibit inverse behaviour between active carrier and mobility: when the concentration decreases a mobility increase is present, and in the case of decreasing mobility is noticeable a remarkable rise in active concentration. The net result of these two parameters change is the slight decrease of resistance peculiar of our Ga-doped samples.

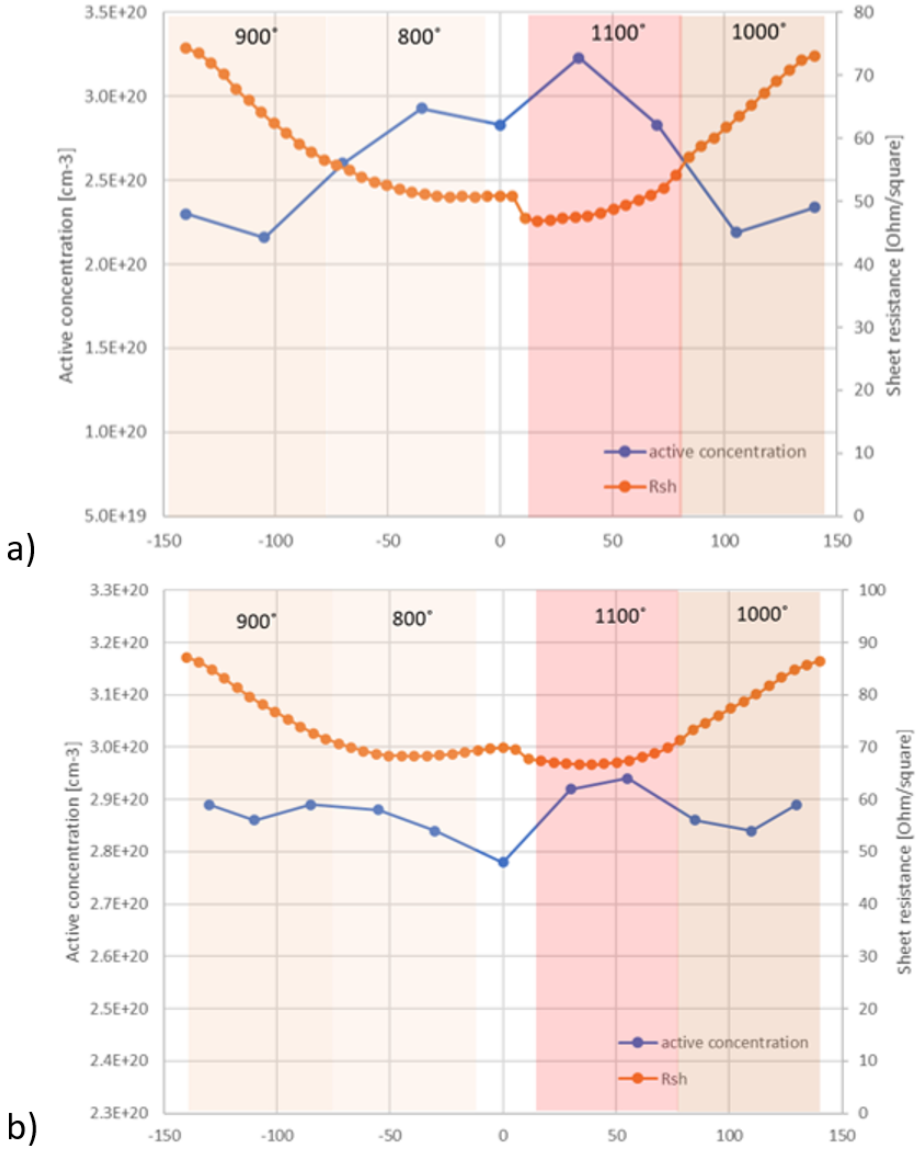


Figure 4.14: Typical sheet resistance profiles of Ga doped samples, a small variation is visible in correspondence of zone 5. a) Sample A2. b) Sample B2.

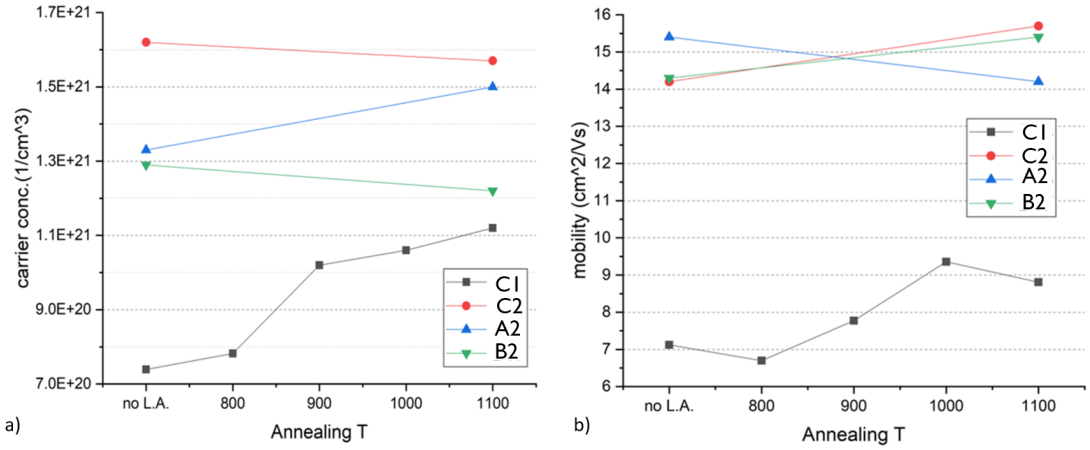


Figure 4.15: Active carrier concentration (a) and mobility (b) of several SiGe layers as function of laser annealing temperature. Data obtained by MHE.

4.2.2 SIMS results

To observe the effect of the laser annealing on the dopants diffusion the most interesting samples were characterized by SIMS. Aside dopants diffusion, the total chemical concentration of the various elements present in the layers can be inspected and this gives an idea on the portion of active doping with respect to the total doping amount. To study the diffusion the Ga and B profiles of different zones have been compared; to account for layer's thickness nonuniformity SIMS profiles have been normalized. However, the diffusion in the silicon substrate does not depend on the junction depth and normalization can create artifacts between the profiles. For this reason the normalization was done in two parts:

$$x_n = \begin{cases} x/x_j & 0 > x > x_j \\ 1 + (x - x_j)/x_{jm} & x > x_j \end{cases} \tag{4.2}$$

Where x_n is the normalized depth, x_j is the junction depth and x_{jm} is the average junction depth of the entire wafer. It is important to notice that every zone is quite large, also inside the same one the thickness can vary. For this reason, as junction depth was not used the XRD data of the zone, but it was directly measured from SIMS profile using the germanium concentration. From profiles comparison, SIMS data show negligible diffusion of dopants both in the SiGe layer and in the Si substrate. The result was the same in all the wafers inspected; two examples are reported in Figure 4.16. In particular, the samples E1 (a) and B2 (b) are shown. C1 is B-doped and the boron concentration is displayed for each 5 different zones, while B2 is Ga-B co-doped and the two elements concentration is reported for the zone 1 and zone 5. It is interesting to notice how the B2 profile are not constant but oscillating, due to the cyclic nature of the deposition. Having noticed that no important diffusion happens, we can look at chemical concentrations in our samples. In the following table the samples with the highest chemical or active dopants concentrations are reported.

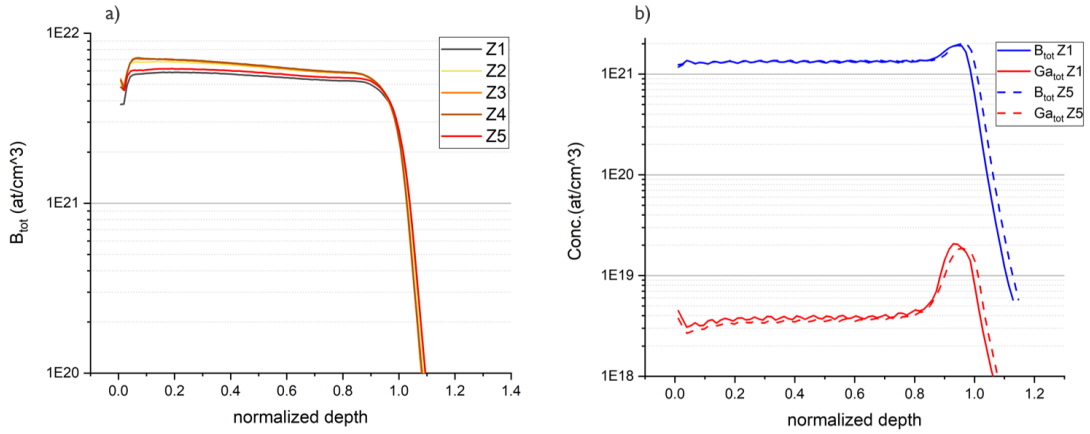


Figure 4.16: a) Boron concentration profiles of sample E1 in each zone. b) Boron and gallium profiles of Zone 1 and Zone 5 of sample B2.

Name	SIMS B $[at/cm^3]$	SIMS Ga $[at/cm^3]$	μHall (active c.) $[1/cm^3]$
Sample C1	5.9E21	-	7.4E20
Reference 2	2.6E21	-	1.3E21
Sample C2	2.5E21	1.8E19	1.6E21
Sample D3	1.25E21	1.2E19	1.45E21

Table 4.4: Chemical and active concentrations measured by SIMS and MHE of the samples with highest doping concentration.

The C1 sample, as expected, is the one with the highest B chemical concentration due to the highest B_2H_6 flow applied. Nevertheless, this shows the lowest active doping level reported in table. This can be explained by a bad morphology, which means that B amount is above the solubility limit, resulting in a considerable amount of non active dopants. The reference of the second group, the CDE B-doped samples, shows much higher active doping with less than half of chemical concentration thanks to good morphology and a very high percentage of activation. The active doping is slightly increased with the addition of Ga in the sample C2, but with the drawback of a lower carrier mobility. Since the conductivity, in the case of high p-type doping, is approximated by:

$$\sigma = e \cdot p \cdot \mu_p \tag{4.3}$$

with e the holes charge, p the holes concentration and μ_p the holes mobility, no significant electrical improvement is noticed. Recalling the Ga incorporation delay, can be interesting to analyze the different Ga concentration in our samples. In figure 4.17 (a) are reported the concentrations of the group 2 as function of the spike doping deposition time. As expected, the Ga concentration increase with increasing of the spike time, but that's not true passing from 0 to 30 seconds. To understand this lowering on Ga concentration, we should recall the change on the SiGe deposition step time: being the step time lower, the thickness of the

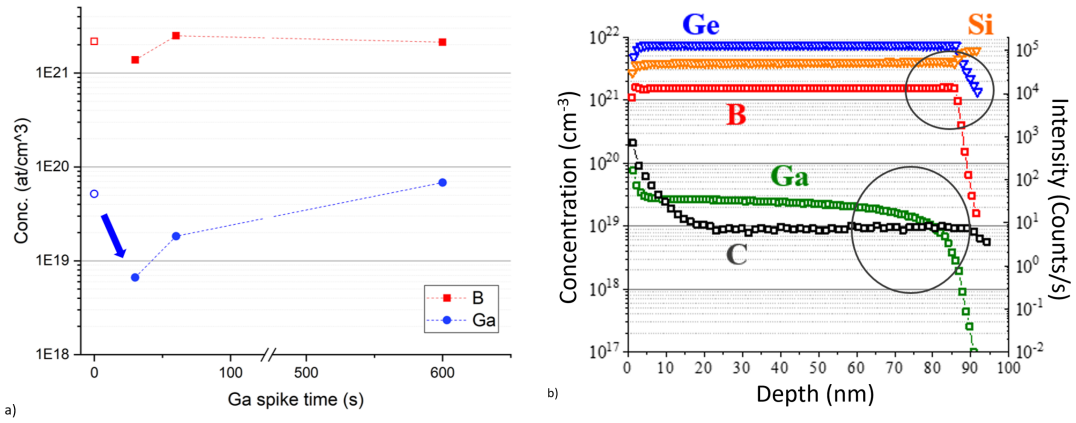


Figure 4.17: a) Boron and Gallium concentration in function of Ga spike time. SiGe Dep/etch times are different for the sample without spike doping and this results in a higher incorporation. b) Elemental depth profile of a B-Ga co-doped layer, the incorporation delay of gallium is clear [Clement Porret courtesy].

SiGe layer deposited during each step will be lower as well, and Ga will not reach the highest concentration that is obtained after a thicker deposition due to Ga incorporation retardation. The delay on Ga incorporation with respect to B can be observed on figure 4.17 (b), where the results of a previous study are shown.

The last outcome that can be analyzed from SIMS inspections regards the presence of carbon in the layer. Due to its small atomic radius, carbon is an element used on n-type MOSFET source and drain regions to achieve tensile strain in the channel [42]. The presence of this element in the SiGe layers should be avoided because its effect is opposite to the one of Ge, and it would reduce the compressive strain that we need in p-type MOSFET. The Ga precursor that we have used is a metal-organic precursor, and so it contains C (as can be seen from TTBGa formula 4.1). Nevertheless, from SIMS data it's clear that carbon

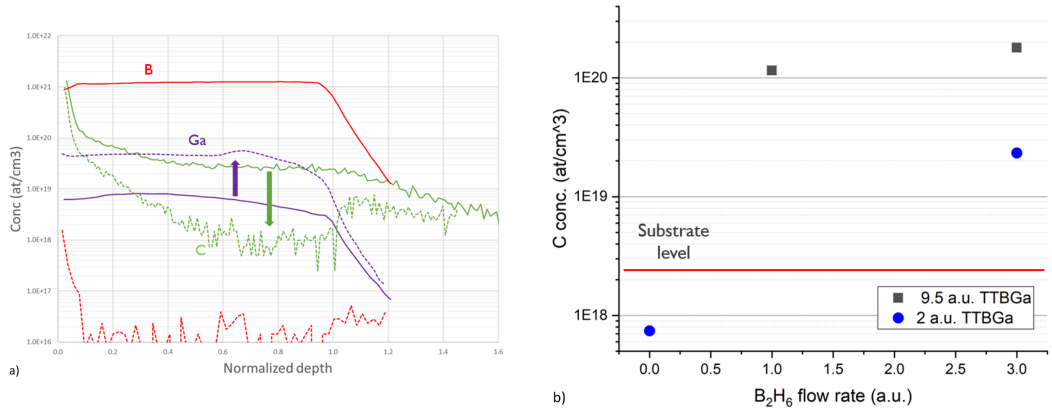


Figure 4.18: a) Boron, gallium and carbon depth profiles reported for samples Ga ref 3 and B-Ga ref 3. b) Carbon concentration from SIMS measurement in function of diborane flow and for different TTBGa flows.

incorporaton depends not only on TTBGa flow. It's in fact clear the dependence from the B_2H_6 flow, that demonstrates catalytic effect on the reactions for carbon incorporation. The level of C in the layers as a function of the diborane flow is reported in figure 4.18 (a). It can be noticed that at the same amount of TTBGa flow, the carbon level on the layer remains under the substrate level in the sample without B_2H_6 and it increases remarkably when boron precursor is added; the other couple of samples demonstrate that the trend exists also passing from 1 a.u. to 3 a.u. of diborane flow. SIMS profiles are shown in figure 4.18 (b) whence the first couple of points are taken.

Chapter 5

SiGe growth on different Si planes

In this chapter the results of the experiments conducted on the growth of SiGe on different surfaces of Si will be analyzed. Aim of the study is to confirm the different growth rates found in the literature of the SiGe grown with standard precursors at 500°C and subsequentally to find the respective growth rates of depositions with high order precursors at 400°C. The study will be performed with different conditions and on different substrates.

5.1 (100) substrate

In this section the results obtained on the patterned structure on Si (100) substrate are analyzed. The importance of the substrate used comes from the fact that, if the crystalline orientation is different, the lateral surfaces of the "wagon wheel" fins are different. The alignment of the structure is possible thanks to the fast fourier trasform technique: through FFT the orientation of a single fin can be determined, thanks to the known pattern of the reciprocal lattice, and from that all the other surfaces are found with the use of stereographic projection. In figure 5.1 can be observed the stereographic projection superimposed to the fins structure: for our purposes, considering only the surfaces perpendicular to the substrate, we should refer to the planes present on the external circumference. The planes referring to each direction are the one growing perpendicular to the line that links the center to the circumference point. Hence, to identify the planes growing on the fins lateral edges we should search for points at 90°from the considered fin direction. Nevertheless, on (100) substrate a 90°symmetry is present and the planes perpendicular to the fin direction coincide to the one along it. Another feature of this substrate is that the different planes are comprised in an angular span of 45°: in the wagon wheel structure 5 fins cover such a span, and as a consequence, only five fins should be studied. To measure the thickness of the SiGe layers grown on the fins, TEM inspections are performed. The fins are tilted and not parallel one to another, thus only one sample is not enough to clearly measure each fin, an error of misalignment would be present. At the same time the lamella preparation is a time requiring and expensive technique, and it's not convenient to create five different lamellae perpendicular to each different fin. For this reason two lamellae are prepared for each wafer, perpendicular to fin 1 and

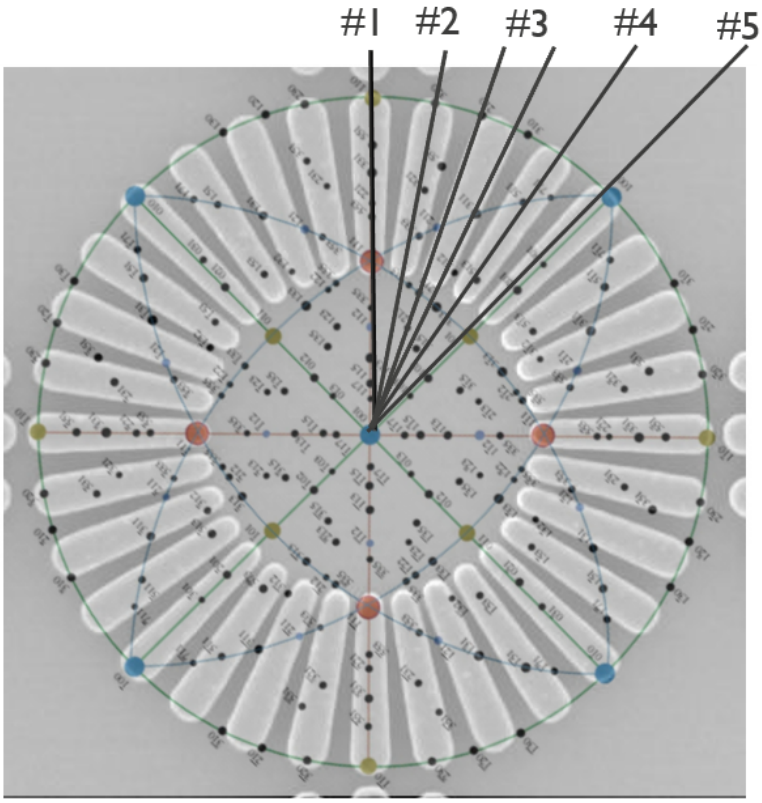


Figure 5.1: Wagon wheel structure with stereographic projection overlapped. The five spikes inspected are evidenced.

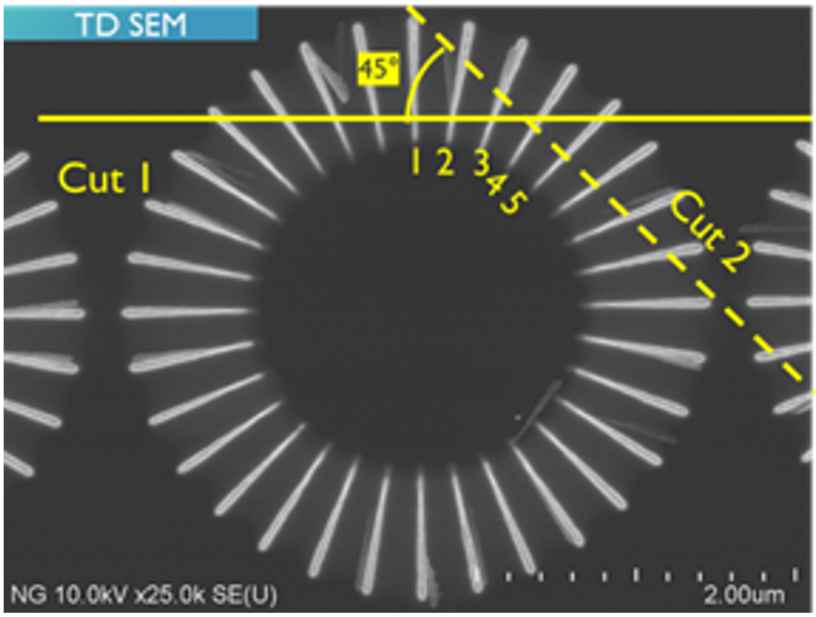


Figure 5.2: Schematic of the two different cuts used to study the results through TEM inspection.

fin 5, as shown by the two "cut" in Figure 5.2. The following table lists the fin number and the correspondent sidewall surface:

Fin number	Surface
1	(110)
2	(320)
3 (1)	(210)
3 (2)	(310)
4	(510)
5	(100)

Table 5.1: Crystalline planes exposed on (100) wagon wheels structure

5.1.1 Classical deposition on (100) substrate

Firstly, a deposition has been done with a known recipe, using DCS and germane as precursors at temperature of 500°. The germane mass flow was nearly four times higher than the diclorosilane one to obtain a high germanium percentage, while diborane and hydrocloridic acid were added to obtain a doped layer and a selective deposition. A diluted HF clean and a 5 minutes pre-epi bake at 775°was done in order to remove native SiO_2. The result of this deposition is shown in Figure 5.3, where all the five fins from the respective cuts are displayed. First of all, it can be noticed that the SiGe layer is present only on the sidewalls and not on the top of the Si_3N_4, proving the perfect selectivity of the recipe. Then, the difference on the layer shape between each fin is clear. The thickness of the layer changes radically from fin 1 to fin 5, demonstrating a different growth rates that cause faceting on patterned structure. Moreover, at the interface between the lateral surface and the nitride on top of the fin, new facets develop with the new surface being dependent on the fin orientation. In the first fin, with lateral growing plane being (110) surfaces, the facets are formed by (111) planes being very slowly growing and having a 35°angle with (110). In the fin 5, the faceting kinetic is completely different: the exposed plane at the top interface being (100) as the lateral one, the growth continues upwards exposing others (100) planes that develop perpendicular to the existent ones. The fins in the middle are comprised between these two limiting cases and the angles of their facets move from 35°of fin 1 to 90°of fin 5. The layer thickness on each sidewall are reported in Figure 5.4, where they are displayed in function of the spike sidewall number. It is interesting to notice that (110) plane is the slowest between the ones present, while (510) is the fastest one. The ratio between (110) and (100) growth rates is $R_{110} = 0.69$.

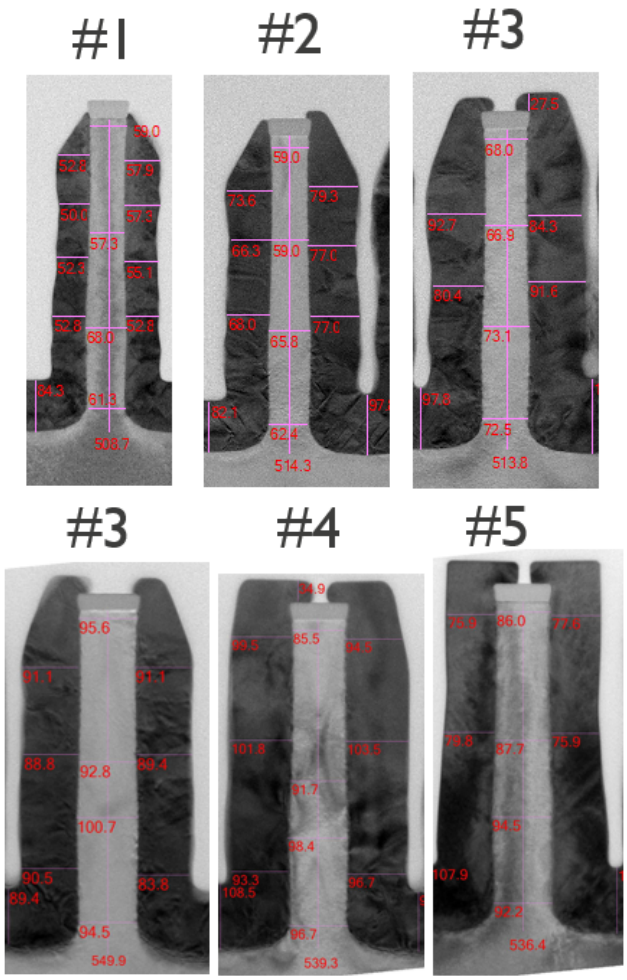


Figure 5.3: TEM images of the five fins with different exposed planes. The thickness differences are clear, result of a strongly anisotropic growth rate.

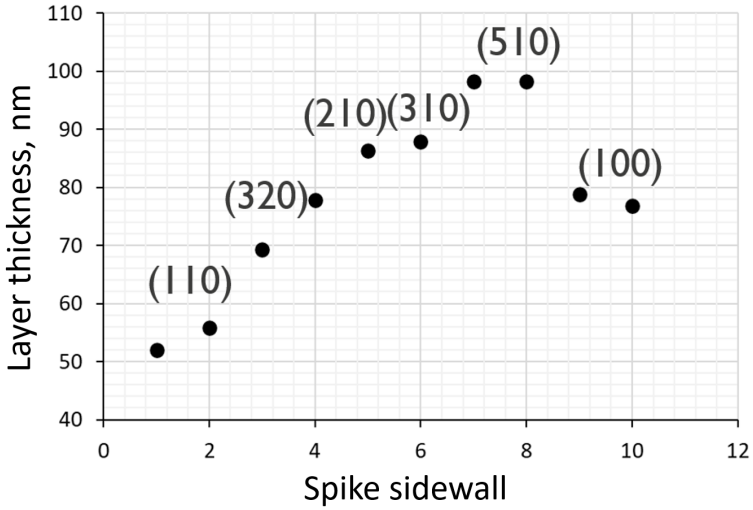


Figure 5.4: Thicknesses of the deposited SiGe layers on each Si fins. The planes present on the sidewalls are reported.

5.1.2 Low temperature deposition on (100) substrate

The SiGe CDE deposition on this structure has been repeated at 400°C and with high order precursors (disilane and digermane). To the best of our knowledge, the growth rates on different Si surfaces at this temperature and with this precursors set have not been investigated. In particular, this type of deposition is currently used only for the growth of SiGe layers on (100) silicon substrates but it is unknown how it works on differently oriented substrates. Unfortunately, the first growth attempt has been done with parameters tuned as in actual devices, and did not show any SiGe growth. This is probably due to a very large open silicon area, much larger than in the case of device wafers, where only small Si area is exposed and main part of the substrate is covered by oxides forming Shallow Trench Insulation (STI) and nitrides used for spacers formation. Two wafers are thus grown and studied: one with the open silicon area as before and one with oxide deposited between the spikes. To deposit in the structure with very large Si open area, the etching step was removed, and the process will likely result in non selective deposition. The results of the sample without oxide are shown in Figure 5.5.

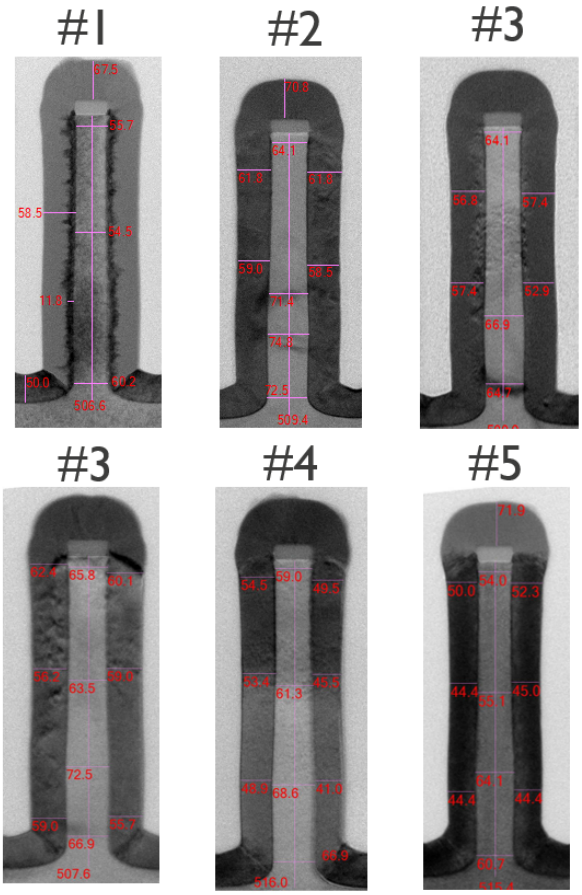


Figure 5.5: TEM images of the fins with layers grown with low temperature process. In spikes 1 and 5 the contrast allows to understand the layers crystallinity.

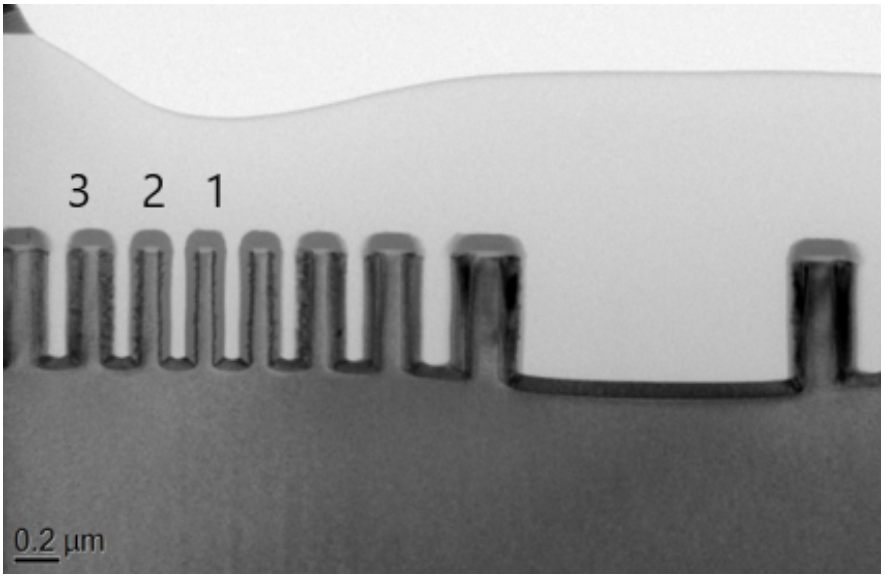


Figure 5.6: Unroated TEM inspection of the cut 1. It is visible that also spikes 2 and 3 are characterized by a first layer of epitaxial growth followed by amorphous deposition.

As can be observed, this time the SiGe layers are uniform through the entire fin and the deposition looks similar in all 5 fins. The reported images are from bright field STEM, which contrast depends on the density and crystallinity of the layers. It is therefore clear, from the spike 1, that the SiGe deposition is not crystalline but amorphous. In particular, there is a high contrast between the first 10 nm SiGe deposited and the rest, meaning that the deposition has started crystalline and after few grown nanometers it turned to amorphous deposition. The fifth fin instead shows a different behaviour: it is possible to see that the material is crystalline along the entire sidewalls and shows a net contrast with the material deposited on the top nitride, that is instead amorphous. Unfortunately, this type of contrast is not possible for the fins comprised between the two extremes: due to their tilting, the sample should be rotated and the thickness of material that should be pierced by the electrons is higher. Nevertheless, from the unrotated specimen (5.6) (not high resolution) can be noticed the evolution of crystallinity also for the middle fins. Going from fin 1 (surface (110)) to fin 5 (surface (100)) the crystalline portion of the layer increases, becoming completely crystalline for a sidewall of fin 4 and, as seen before, both the sidewalls of fin 5. The crystalline region prior to the epitaxy breakdown is defective and is characterized by the presence of (111) twinning defects, the breakdown is therefore likely due to surface roughening caused by the lower adatoms mobility at this temperature [43]. The critical thickness of epitaxial breakdown is clearly dependent on the surface plane, and the recipe should be adjusted to obtain a crystalline deposition on every fin (surface). As expected due to the above argument, the amorphous material deposited on the silicon nitride shows that the deposition was not selective. The etching step with Cl_2 should be added to achieve selectivity. As already mentioned, the second deposition was performed on a wafer with silicon oxide present between the spikes. This is done to simulate the STI present on the device wafers

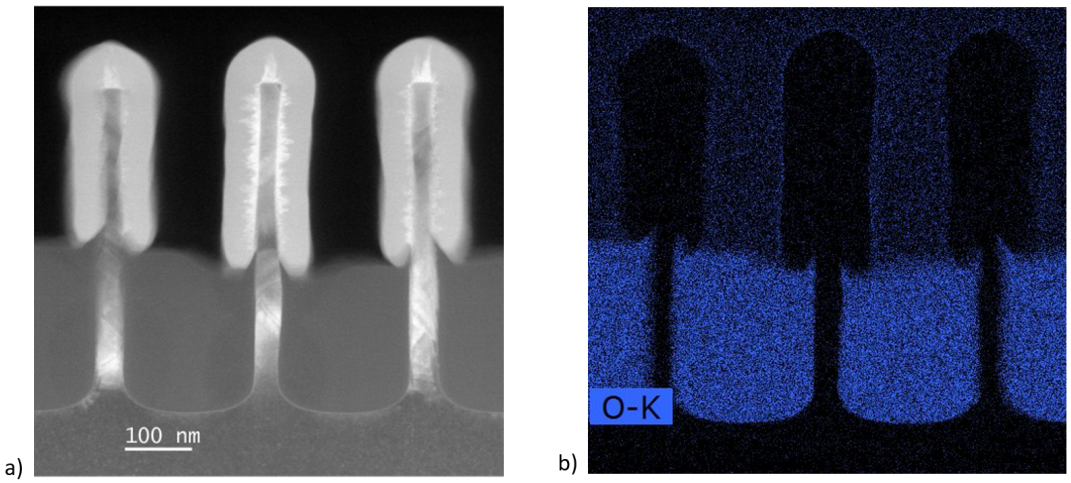


Figure 5.7: a) TEM image of the wagon wheel structure with oxide deposited to cover the substrate. The central fin has (100) sidewalls but the deposited material is amorphous. b) Oxygen elemental mapping of the same cut. No oxygen is visible on the silicon sidewalls.

and significantly reduce the Si open area. The deposition was then repeated with the same amount of precursor gases, but this time CDE deposition was possible. Unfortunately, due to a different etching process to prepare the substrate (due to the process flow used to deposit SiO_2), the Si_3N_4 has been completely removed and the silicon is exposed on top. This causes the impossibility to observe the selectivity of this process towards nitride, although it is clearly selective towards oxide. From TEM inspections (figure 5.7(a)) results that the deposition is similar to the previous one, but this time the SiGe layer is always amorphous, also on the (100) surface. Also if the recipe should be optimized to deposit on different planes, it is typically used to grow on (100) surfaces, therefore this was an unexpected result. Moreover, on the exposed fin top the Si surface is (100) and there an epitaxial grow is clearly visible. It can be thought that the epitaxy breakdown, at least on (100) surface, is caused by the presence of native oxide on the sidewalls. Howewer, an EDS mapping didn't give any sign of oxygen on the fin sidewalls (figure 5.7(b)); the effect of the SiO_2 presence on the epitaxial growth should be further investigated.

5.2 (110) substrate

In this section we will see the results of the SiGe epitaxial growth on the structure patterned on (110)-oriented wafers. On this substrate the sidewalls' surfaces are not repeated after 45°but after 90°, hence 9 spikes should be studied. To do so, 2 cuts are not enough and for each wafer 3 lamellae are created and inspected. Moreover, on the new substrate there is not a 90°as in the previous one. Hence, to know which planes are exposed on the fin sidewalls should be looked the direction perpendicular to the one along the fin. For this reason in figure 5.8 the directions of the fin and the perpendicular ones are denoted by lines of the same color. In the new structure together with (100) and (110) planes will be present also the (111) surface, that is of great relevance for our purposes due to its important contribution on the SiGe faceting [44]. The surfaces on each sidewall, as suggested by the stereographic projection, are reported in Table 5.2.

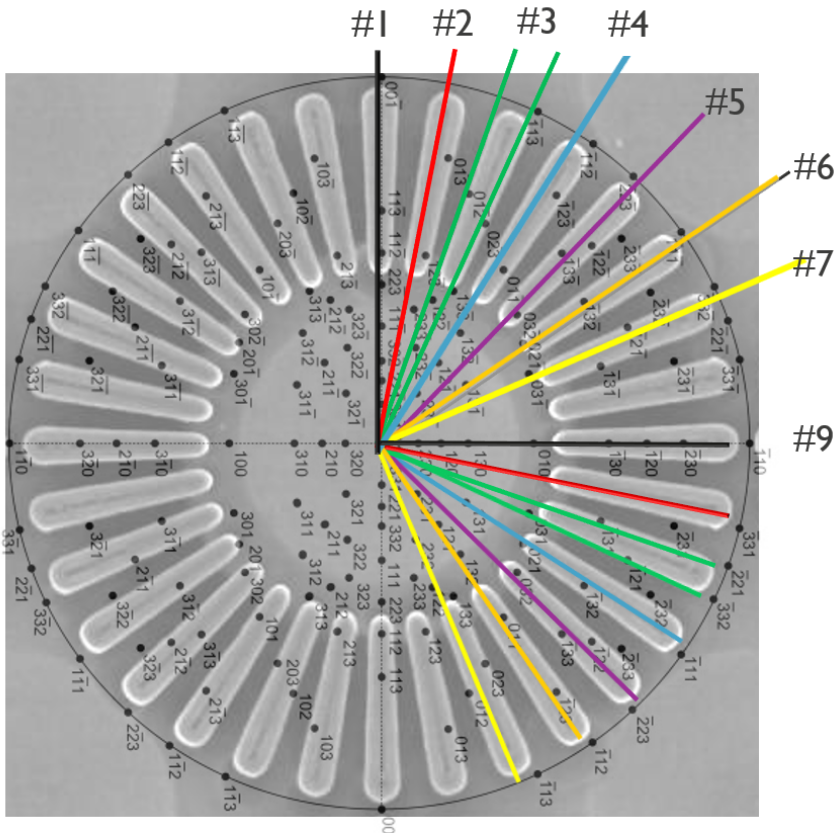


Figure 5.8: Stereographic projection centred on (110) substrate overlapped to the wagon wheels substrate. The surface sidewalls are perpendicular to the direction of the fin, to know in which surface are the SiGe growing should be seen the direction at 90°. The fin direction and its normal one are linked by the same line color.

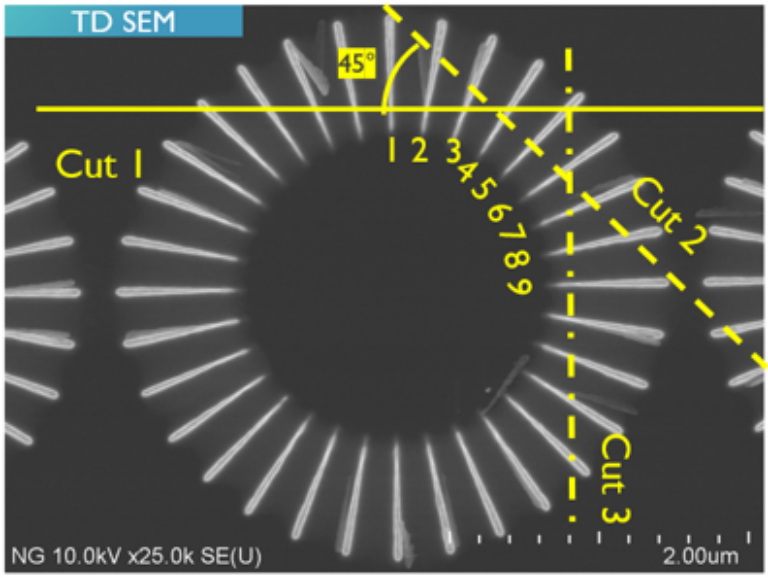


Figure 5.9: The 3 cuts needed to obtain the cross-section of all 9 different fins are shown.

Fin number	Surface
1	(110)
2	(331)
3 (1)	(221)
3 (2)	(332)
4	(111)
5	(223)
6	(112)
7	(113)
8	(115)
9	(100)

Table 5.2: Crystalline planes exposed on (110) wagon wheels structure

5.2.1 Classical deposition on (110) substrate

Also on this new substrate we have started analysing the SiGe epitaxial growth through a deposition at 500°C with DCS and germane as precursors. The deposition with conventional precursors has been done on a wafer with silicon oxide between the spikes to observe if it has an effect on the growth. The deposition, also in this case, results in a crystalline SiGe layer with very different thickness on each spikes. Due to the wide range of growth rates also strong faceting occurred as soon as a new facet was created at the Si-Si_3N_4 interface. Differently than the first case, the faceting showed very different characteristic with respect to the fin considered: in some spikes, e.g. spike 1, the exposed facet at the top has an higher growth rate than the sidewall surface and faceting results in an overgrowth; contrarily, in other spikes, e.g. spike 9, the facet is a limiting factor for the SiGe growth due to a lower GR than the spike sidewall surface. Also if

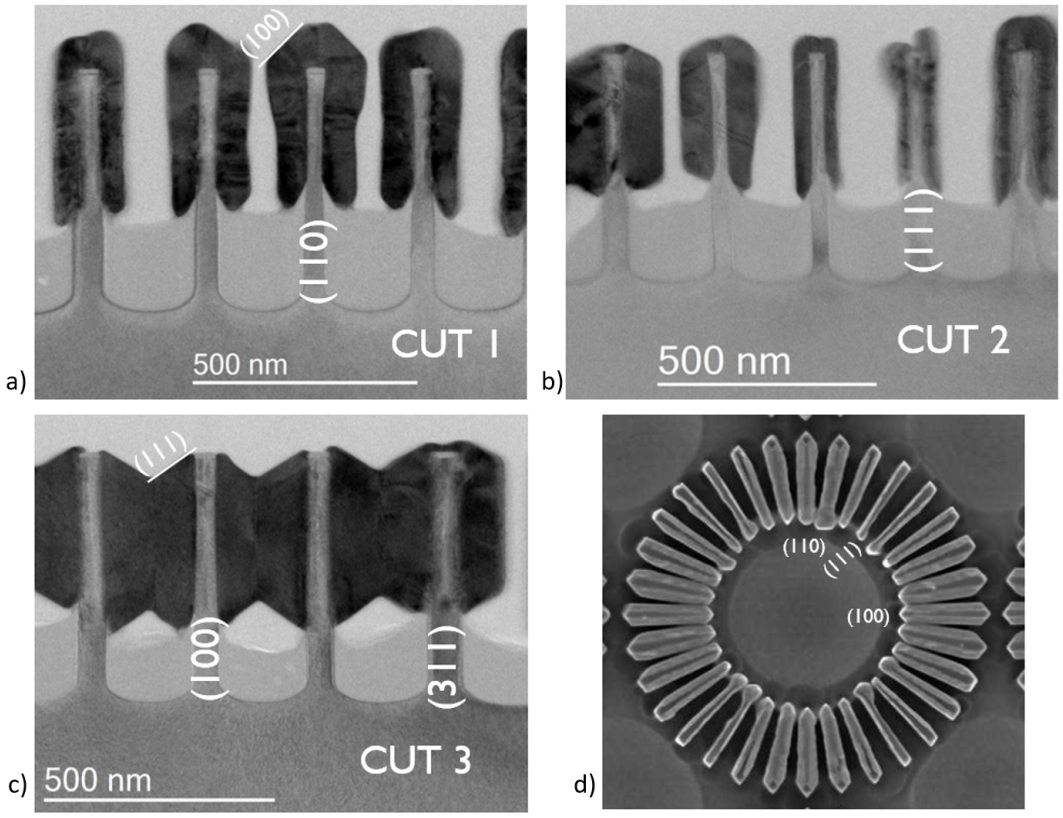


Figure 5.10: In figures (a),(b) and (c) three different cuts inspected with TEM are reported. It is possible to see the thickness difference between the spikes and the appearance of the new facet. In figure (d) a top-view SEM image of the structure is reported.

the overgrowth just discussed brings a completely covered nitride, the deposition is still selective, being the top of the spikes with limiting facets completely clean. As done on the previous substrate, the thickness and growth rate were calculated using the TEM cross-section images. In this case it can be noticed that on the third cut are present the surfaces with the highest growth rate, and the SiGe layers on the different spikes are merged. To use this thicknesses limited by merging can convert in an error, but from the top-view SEM picture it's visible that the growth was not limited since the layers have just touched in a small zone. Hence, we can assume the growth rates found by that thicknesses as true. In the case of overgrown layers instead, the thickness profile is clearly not uniform, with the width of the higher part depending not only from the growth rate of the sidewall surface. To avoid influence of other planes, the thickness on the lower part of the fin has been considered, where the thickness can be considered uniform. The final growth rates are reported in figure 5.11. As expected, the (111) plane is the slowest growing with a very small growth rate, reason why it is a limiting plane during the crystal growth. The ratio between (110) and (100) rates is $R_{110} = 0.77$, close to the one found previously. The temperature and the precursors used were the same, hence the same ratio was expected. Nevertheless, this small difference can be addressed either to the difficulties present to find the right thickness of

each plane (due to the facets overgrowth) or on SiO_2 presence effects (e.g. loading effects).

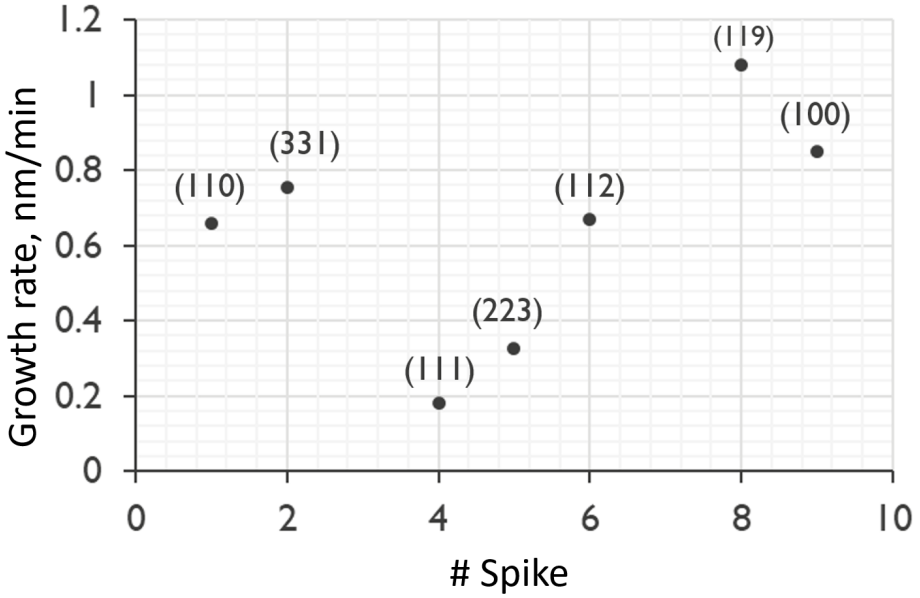


Figure 5.11: In the graph are reported the growth rates on the different exposed surface. The rates are based on the thicknesses seen from TEM cross sections.

5.2.2 Low temperature deposition on (110) substrate

The low temperature deposition has been repeated on the same (110) substrate, also in this case with silicon oxide present between the spikes to limit Si open area. The recipe used for this deposition was the same used for the low temperature deposition on the (100) substrate, with the deposition/etch ratio set at 7.5 to obtain a selective epitaxial growth. The etching process to create the structure has been optimized and the nitride is present on the fins top to observe selectivity towards nitride of the recipe. Unfortunately, also this low temperature deposition resulted in an amorphous growth of SiGe on every surface, (100) comprised. On the latter, as reported in figure 5.12, are visible the (111) faceted crystalline cusps observed also in the first experiments, that as seen above are typical of the epitaxy breakdown. The only notable feature is the better selectivity of the deposition: also if amorphous material is present on the Si_3N_4, its shape clearly denotes that the material was not deposited immediately on it but it is consequence of the lateral layers overgrowth. The SiGe epitaxial growth on this structure was not obtained with the low temperature process used, some changes must be done to overcome these results. First of all, a pre-epi bake at 775°C was done to ensure a very clean Si surface. Then, the gas precursors mixture was changed as schematized in Figure 5.13. Furthermore, the deposition/etching ratio was reduced and it was set at 5. Both digermane and diborane were remarkably augmented, but should remembered that the two gases adsorptions are in contrast with each other. Hence, if the diborane is increased also the digermane should

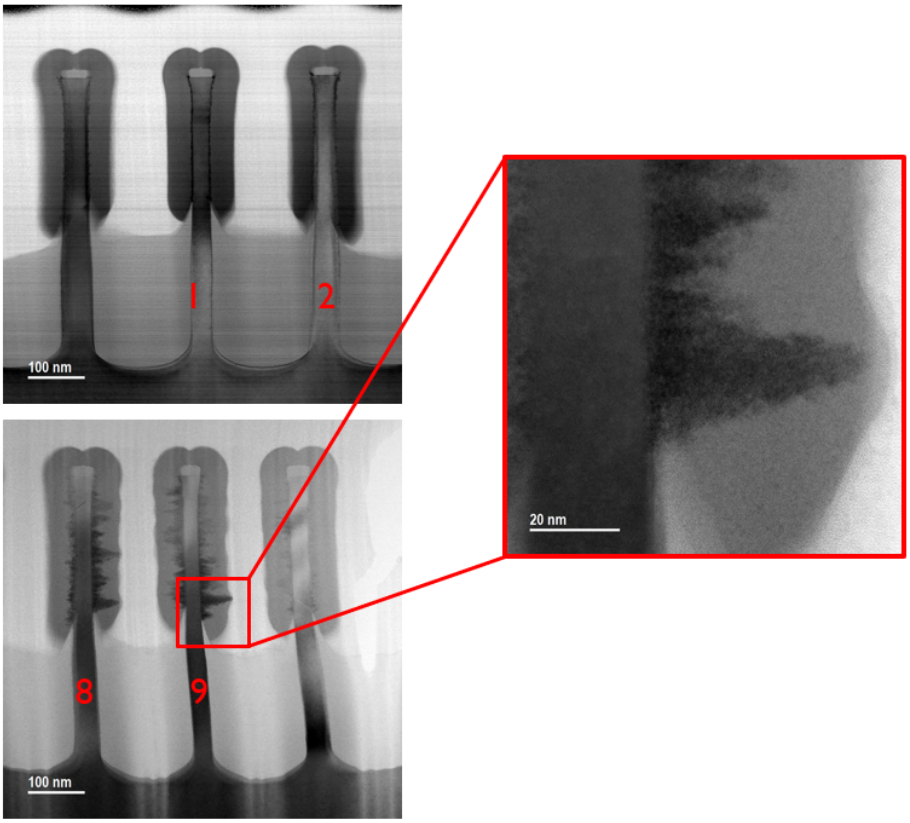
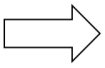


Figure 5.12: TEM images of the cut 1 and cut 3. The deposited layers were amorphous on every spikes. A zoom of the crystalline cusps on (100) surface is shown.

be increased to avoid a lowering of Ge concentration in the layer. Should be also mentioned that the arbitrary unit reported are different between silicon and germanium precursors and the dopant gas, being the B_2H_6 flow much lower. The recipe modification gave the desired results, allowing a crystalline epitaxial deposition on every Si surface present in the structure. The differences between the SiGe layers of this deposition and the ones seen above with classical precursors are surprising. The thicknesses of the deposited materials, in this case, are very close on every different surface, demonstrating that the growth rate is no more strongly dependent on them. In particular, the (111) GR, that is usually very

	Old recipe
Si_2H_6	0.5 a.u.
Ge_2H_6	1.5 a.u.
B_2H_6	3 a.u.
Dep/etch	7.5



	New recipe
Si_2H_6	0.5 a.u.
Ge_2H_6	9 a.u.
B_2H_6	15 a.u.
Dep/etch	5

Figure 5.13: Parameters used for the low temperature depositions

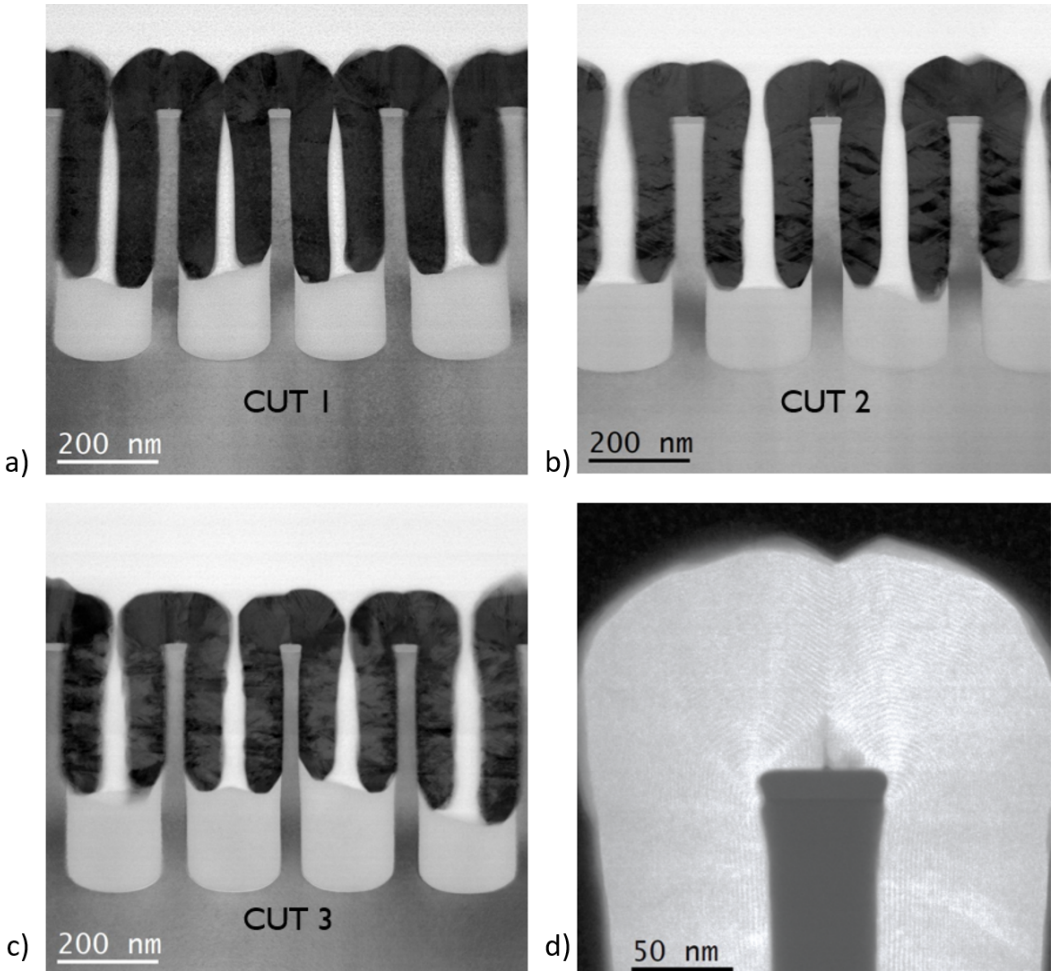


Figure 5.14: a),b),c) TEM inspections of the 3 different cuts. d) High resolution Zoom of the central fin of cut 1.

small, is now in the same range than all the others. This property is reflected in the absence of facets in these spikes: also if the top is covered with nitride and the facets do not develop as in device's Si fins, with the previous deposition facets were present at Si-Si_3N_4 interface. The layers in this experiment are instead uniform and do not show any form of faceting. The only remarkably dis-homogeneity is the thickness on the top that is higher than the lateral one. Nevertheless, this difference is not to be attributed to the growth orientation. Indeed, it is likely due to a mass-limitation mechanism, with the lateral growth reduced by the small amount of reactive gas available in the tight space between the spikes after a certain thickness of SiGe deposited. Instead, on the top the concentration of reactive gas remains high throughout the entire deposition, allowing an higher GR. The concept can be better understand looking at figure 5.15, where it is clearly visible the proximity of SiGe adjacent layers. Regarding the selectivity of the deposition, the top nitride is completely covered from SiGe and usually this is the prove for a lack of selectivity. Instead, it is possible to notice that this is not the case.

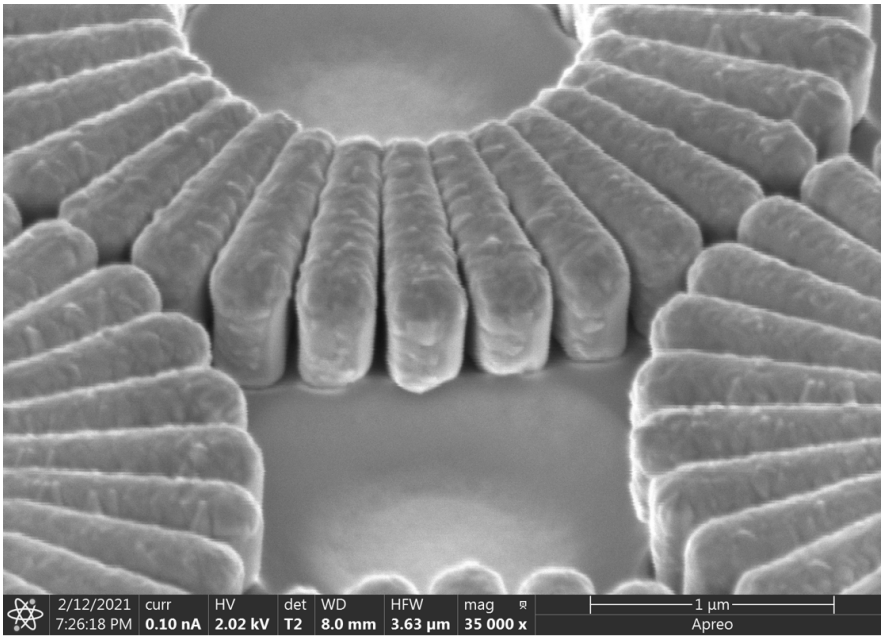


Figure 5.15: SEM tilted image of the wagon wheel structure with crystalline SiGe deposited.

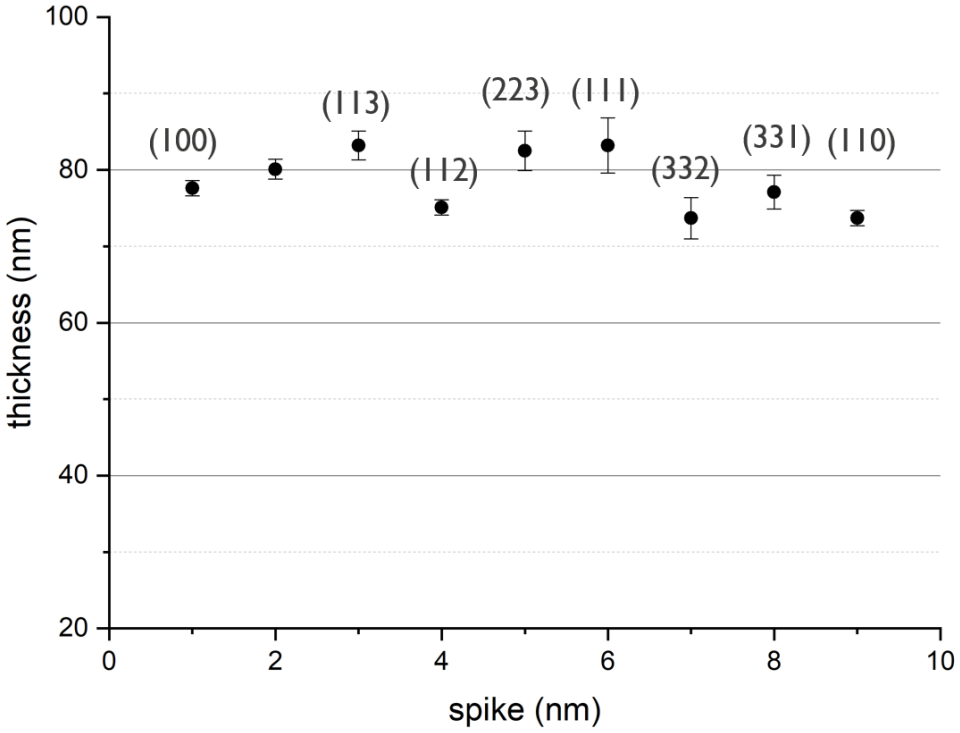


Figure 5.16: Thicknesses of the SiGe layers obtained with low temperature process. With this deposition the growth rates are very close, independently from the growing surface.

From the zoom of the N°1 fin reported in figure 5.14(d), the single layers deposited at each cycle are distinguishable. From that, we can notice that the first layers are present only on the Si sidewalls and they do not extend on the Si_3N_4 cap. Each successive deposition covered the already present SiGe layer, continuously increasing the area and pushing upwards the layer boundaries. After several cycles, the layers covered the entire fins and the growth continued also on the top nitride. The thicknesses of the grown layers are reported in Figure 5.16, where the miller indexes of the different surfaces are also specified. It should be mentioned that the surfaces doesn't correspond at the same fin numbers of before (Table 5.2) due to a different circumference portion inspected, but the present surfaces are always the same. From the mentioned Figure, is further clear how the growth rate are similar and the dependence from the surface orientation is nearly lost. Without slow growing planes present in this deposition, there is no reason to think that the S/D SiGe epitaxial growth with with this process would develop facets and would have non-uniform profile.

Chapter 6

Conclusions

In this chapter a brief summary of the results and an outlook for future research are presented.

6.1 Summary

The experimental work done on B-Ga in-situ co-doping SiGe confirms its interesting properties and sustains it as a material for future p-MOS S/D layers. Morphology characterization confirms that within the right parameters the Ga doped layers have low defectivity and there are no evidences of relaxation. Compositional analysis shows that the growth process allows to incorporate Ga quantities depending from TTBGa flow rate, while high B concentration ($1{\cdot}10^{21}$) is incorporated. Nevertheless, the chemical Ga concentration observed is of two order of magnitude lower then the B one, hence electrical properties are not yet enhanced by gallium addition. Despite this, compositional analysis has demonstrated that the strong competition observed between germanium and boron incorporation is not present between germanium and gallium. Thus, higher germanium concentration is observed in B-Ga co-doped samples, allowing to achieve high doping concentration and a germanium concentration close to the targeted one, $Ge_{\%} \approx 50$. Nevertheless, the laser annealing treatment did not show relevant improvements on the SiGe layers electrical properties. Indeed, M4PP measurement showed that B-Ga co-doped layer presented a small sheet resistance decrease only under the highest tried laser annealing temperature. The main problem of the process is the incorporation of unwanted C atoms. This element, besides to lower the channel strain given by germanium concentration, seems to bring a degradation of the SiGe layer's electrical properties (to be confirmed by further studies). Despite the metal-organic Ga precursor is the C source, we have observed that boron presence helps to incorporate it. Thus, new process conditions should be found to limit C presence in B-Ga co-doped layers.

The studies done on SiGe growth on different Si surfaces showed exciting results. The SiGe grown through process of record is characterized, as expected, by strong growth anisotropy. The growth rate ratios between the main crystalline planes have been calculated, finding value similar to literature. A very poor (111)

GR is observed, that is the limiting plane in S/D standard facets. Although the difficulties to achieve crystalline deposition through low temperature process, deposition parameters have been adjusted until epitaxial deposition on every exposed surface was achieved. The low temperature process gave rise to uniform layers, with thicknesses (hence GR) comparable on every spikes, independently from the growing surface. Therefore, being (111) not a limiting plane with this process, there is no reason to think that the S/D layers will be characterized by faceted growth.

6.2 Future works and outlook

SiGe:B:Ga is a promising material for future p-MOS S/D applications. Yet there are many questions open about the physics of this material and the process to obtain the best characteristics. Although gallium has been introduced to enhance B doping limit, in the sample processed the Ga concentration present is too small to have a real impact on the material resistivity. Hence, in future works the process should be optimized to obtain gallium incorporation at least of the boron concentration level. A possible way, is to follow the gallium spike doping approach used on the CDE grown layers, finding an optimal precursor flow and deposition time to obtain the highest Ga concentration that allows an acceptable layer's morphology.
It has been observed that an high C concentration is present in the SiGe:B:Ga layers, where a lower concentration is present for SiGe:Ga. The correlation between boron presence and carbon incorporation should be studied. A cyclical doping approach could be used in future works: SiGe:Ga and SiGe:B could be deposited in different step, avoiding to have diborane in the chamber in the Ga doping step. Carbon incorporation through this process could be analysed to better understand this phenomenon.

Regarding the study on wagon wheels structure, an uniform deposition has been obtained. A deep theoretical understanding of faceting in crystal growth is still missing. For this reason, the root causes of the obtained result are not clear. The three main factors that distinguish the new process from the standard one and can influence this deposition are: the lower temperature, the precursors used, the cyclic deposition/etching. In future works this factors could be separated to understand what limits the most the facets formation.

Furthermore, a pre-epi hydrogen bake is present in the low temperture process resulting in crystalline deposition. Although the thermal budget prior to deposition does not involve relaxation issues, in future applications as 3D stacked devices a low thermal budget throughout the entire process could be required. The influence of the pre-epi bake should be better investigated, to understand if its role is limited to impurities removal from the surface or its thermal energy brings surface reconstruction that actively effects the SiGe growth rates. Ideally, the same result should be obtained without the use of the bake, to maintain a low total thermal budget.

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I want to dedicate this work to all who I love: to my family, that has always believed in me also during the most difficult times; to my love Giulia, that with her energy illuminates every day of our life; to my friends, that also at great distance I always feel close.

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Bibliography

[1] Intel Website: `https://www.intel.com/content/www/us/en/silicon-innovations/moores-law-technology.html`

[2] Scott E. Thompson et al., *A 90-nm Logic Technology Featuring Strained-Silicon*, IEEE Transactions on Electron Devices 51(11):1790 - 1797, (2004).

[3] Mark Bohr (2011), `https://download.intel.com/newsroom/kits/22nm/pdfs/22nm-Details_Presentation.pdf`

[4] Els Parton, Peter Verheyen, *Strained silicon — the key to sub-45 nm CMOS*, III-Vs Review, 19 (3): 28-31, (2006).

[5] C. Auth et al., *A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors*, VLSI Technology Digest of Technical Papers, p.131, (2012).

[6] Hsiang-Jen Huang, Kun-Ming Chen, Chun-Yen Chang, Liang-Po Chen, Guo-Wei Huang, Tiao-Yuan Huang, *Reduction of Source/Drain Series Resistance and Its Impact on Device Performance for PMOS Transistors with Raised $Si_{1-x}Ge_x$ Source/Drain*, IEEE electron device letters, 21 (9), p. 448, (2000).

[7] Rinus T.P. Lee, W.-Y. Loh, R. Tieckelmann, T. Orzali, C. Huffman, A. Vert G. Huang, M. Kelman, Z. Karim, C. Hobbs, RJ.W. Hill, S.S. Papa Rao, *Technology Options to Reduce Contact Resistance in Nanoscale III-V MOSFETs*, ECS Transactions, 66 (4), p.125-134 (2015).

[8] C. Claeys and E. Simoen, *Germanium-Based Technologies—From Materials to Devices*, (Elsevier, Amsterdam, (2007).

[9] S. Solmi, E. Landi, and F. Baruffaldi, *High concentration boron diffusion in silicon: Simulation of the precipitation phenomena*, Journal of Applied Physics 68, 3250 (1990).

[10] S.C. Song et al., *Holistic Technology Optimization and Key Enablers for 7nm Mobile SOC*, VLSI technology Symposium , pp 198-199, (2015).

[11] M. Garcia Bardon et al., *Dimensioning for power and performance under 10nm: The limits of FinFETs scaling*, ICICDT, pp 1-4, (2015).

[12] *International Technology Roadmap for Semiconductors, 2015 edition*

[13] Jianwei Peng et al., *Source/drain eSiGe engineering for FinFET technology*, Semiconductor Science and Technology (2017).

[14] Z. Zhang et al., *Ultra Low Contact Resistivities for CMOS Beyond 10-nm Node*, IEEE Electron Device Letters (2013).

[15] Shyam Gannavaram, Nemanja Pesovic, Mehmet C. Ozturk, *Low Temperature Recessed Junction Selective Silicon-Germanium Source/Drain Technology for sub-70 nm CMOS*, IEDM (2000).

[16] Jean-Luc Everaert, Marc Schaekers, Hongyu Yu, Lin Lin Wang, *Sub*-$10^{(-9)}$ $\Omega{\cdot}cm$ *2 contact resistivity on p-SiGe achieved by Ga doping and nanosecond laser activation*, Symposium on VLSI Technology Digest of Technical Papers (2017).

[17] P.E. Raynal, V. Loup, L. Vallier, M. Martin, J. Moeyaert, B. Pelissier, Ph. Rodriguez, J.M. Hartmann, P. Besson *Wet and Siconi® cleaning sequences for SiGe p-type metal oxide semiconductor channels*, Microelectronic Engineering, 187-188 (2018).

[18] ASM international web site: https://www.asm.com/Pages/Press-releases/ASM-INTERNATIONAL-EXPANDS-TECHNOLOGY-OFFERINGS-WITH-INTEGRATED-SURFACE-CLEAN-PROCESS-MODULE.aspx

[19] Syun-Ming Jang, Kenneth Liao and Rafael Reif, *Chemical Vapor Deposition of Epitaxial Silicon-Germanium from Silane and Germane: II . In Situ Boron, Arsenic, and Phosphorus Doping*, journal of the electrochemical society (1995).

[20] Keith H. Chung, *Silicon-based epitaxy by Chemical Vapor Deposition using novel precursor neopentasilane*, PhD (2010).

[21] A. Hikavyy, I. Zyulkov, H. Mertens, L. Witters, R. Loo, N. Horiguchi, *Use of high order precursors for manufacturing gate all around devices*, Materials Science in Semiconductor Processing (2016).

[22] M. Liehr, C. M. Greenlief, S. R. Kasi, M. Offenberg, *Kinetics of silicon epitaxy using SiH4 in a rapid thermal chemical vapor deposition reactor*, Applied Physics Letters (1990).

[23] J. Cressler, *Silicon Heterostructure Handbook*, CRC taylor and Francis group, LLC (2006).

[24] J.F. Damlencourt, *Low temperature epitaxy of Si and SiGe usind disilane-based chemistry for electronic purposes*, ECS Transactions (2010).

[25] B.A. Ferguson, C.T. Reeves, D.J. Safarik, and C.B. Mullins, *Silicon deposition from disilane on Si(100)-2×1: Microscopic model including adsorption*, Journal of Applied Physics (2001).

[26] F.Gencarelli, B.Vincent, L.Souriau, O.Richard, W.Vandervorst, R.Loo, M.Caymax, M.Heyns, *Low-temperature Ge and GeSn Chemical Vapor Deposition using Ge2H6*, Thin Solid Films (2012).

[27] J.M. Hartmann, F. Bertin, G. Rolland, F. Laugier, M.N. Séméria *Selective epitaxial growth of Si and SiGe for metal oxide semiconductor transistors*, Journal of crystal growth 259, 419-427 (2003).

[28] W. A. P. Claassen and J. Bloem, *The Nucleation of CVD Silicon on SiO_2 and Si_3N_4 Substrates*, J. Electrochem. Soc., vol. 127, 194 (1980).

[29] W. A. P. Claassen and J. Bloem, *The Nucleation of CVD Silicon on SiO_2 and Si_3N_4 Substrates*,J. Electrochem. Soc., vol.127, 1836 (1980).

[30] M. R. Goulding, *The selective epitaxial growth of silicon*, Materials Science and Engineering, BI7 (1993) 47-67.

[31] W. A. P. Claassen and J. Bloem, *The Nucleation of CVD Silicon on SiO_2 and Si_3N_4 Substrates*, J. Electrochem. Soc., vol. 128, 1353 (1981).

[32] S. Bodnar, E. de Berranger, P. Bouillon, M. Mouis, T. Skotnicki, and J. L. Regolini, *Selective Si and SiGe epitaxial heterostructures grown using an industrial low-pressure chemical vapor deposition module*, Journal of Vacuum Science Technology B 15, 712 (1997).

[33] Andriy Hikavyy, Clement Porret, Erik Rosseel, Alexey Milenin, Roger Loo *Application of Cl2 for low temperature etch and epitaxy*, Semiconductor Science and Technology (2019).

[34] J.M. Hartmann, M. Burdin, G. Rolland, T. Billon *Growth kinetics of Si and SiGe on Si(1 0 0), Si(1 1 0) and Si(1 1 1) surfaces*, Journal of crystal growth, 288-295 (2006).

[35] Vincent Destefanis *Reduced pressure chemical vapor deposition and etch of Si/SiGe heterostructured on (100), (110) and (111) substrates*, PhD (2010).

[36] D. Dutartre, A. Talbot and N. Loubet *Facet Propagation in Si and SiGe Epitaxy or Etching*, ECS Transactions, 473-487 (2006).

[37] P. J. Goodhew *General Introduction to Transmission Electron Microscopy (TEM)*, John Wiley Sons (2011).

[38] Frank Krumeich *https://www.microscopy.ethz.ch/downloads/TEM.pdf.*

[39] Scott D. Findlay, Naoya Shibata, Yuichi Ikuhara, Rong Huang, Eiji Okunishi, Hidetaka Sawada, Yuji Kohno and Yukihito Kondo *Annular Bright-Field Scanning Transmission Electron Microscopy: Direct and Robust Atomic-Resolution Imaging of Light Elements in Crystalline Materials*, Microscopy today (2017).

[40] Maria-Louise Witthøft, Frederik W. Østerberg, Janusz Bogdanowicz, Rong Lin, Henrik H. Henrichsen, Ole Hansen, Dirch H. Petersen *A variable probe pitch micro-Hall effect method*, Beilstein Journal of Nanotechnology (2018).

[41] D. Lapiano-Smith, F.R. Mcfeely, *A mechanism for diborane induced selectivity loss in the chemical vapor deposition of silicon from SiH2Cl2*, Journal of Applied Physics (1992).

[42] Kah Wee Ang et al., *Enhanced performance in 50 nm N-MOSFETs with silicon-carbon source/drain regions* IEDM Technical Digest. IEEE International Electron Devices Meeting (2004).

[43] K. A. Bratland, Y. L. Foo, J. A. N. T. Soares, T. Spila, P. Desjardins, J. E. Greene *Mechanism for epitaxial breakdown during low-temperature Ge (100) molecular beam epitaxy* Physical review B (2003).

[44] Didier Dutartre, Alexandre Talbot, N. Loubet *Facet Propagation in Si and SiGe Epitaxy or Etching*, ECS Transactions (2006).