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Analysis and Design of Compound Semiconductor Stacked Power Amplifiers

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Abstract

The thesis concerns the stacked amplifier topology for high frequency applications, and in particular, the goal of the following analysis is the design of a 3-stages stacked amplifier, working at 26 GHz.
The possibility to overcome the problem linked to the breakdown voltage limitation on V_{DS} and modularity makes the stacked topology particularly interesting at RF. In particular the output power and gain are directly proportional to the number of stacked stages.
From a schematic point of view, a stacked amplifier is made up of two basic stages: a Common Source (CS) and a Pseudo-Common Gate (CG), which corresponds to a Common Gate with a capacitance connected on the its Gate terminal.

What is important, in order to get the maximum output power from each stage, is to provide them the proper load. The latter can be computed by a load-pull simulation.
It can be shown that for low frequencies ($\omega << \omega_T$), inter-stage matching can be exploited by simply tuning the Gate capacitance of the pseudo-common Gate stage. The previous result turn out to be false when the working frequency rises and a CG stage's input impedance will probably be different from the optimum load, even tuning the Gate capacitor.
An inter-stage matching network (InMN) is thus necessary between stages. Three basic InMN topologies are analyzed in this thesis: the shunt inductor, the feedback capacitor and the series inductor. In the present design, only the first one provides acceptable results.

Two technologies of pHEMT are taken into account and compared in the following discussion: commercial GaN and InGaAs pHEMT processes.
Device intrinsic parasitics have been extracted for both technologies and compared. The GaAs transistor was characterized by a very low output impedance, with respect to the GaN. The low impedance will increase the complexity of the output matching network.

Through a load-pull simulation, the optimum load impedance for the GaN is obtained, enhancing a maximum output power of ~ 32 dBm and a gain of ~ 12 dB. What comes out from simulation is however a strongly elliptical dynamic load line for both the first and the second stages (CS and pseudo-CG, respectively). Starting from a 2 stages device, the three InMN are tested out: as an example, in the case of the shunt inductance, C_g and

L_{shunt} are swept over a given range; when the obtained Drain-Source impedances are close to the optimum value, the InMN reached its goal.
The same can be said for the other topologies of InMNs, but the best results are achieved through a shunt inductance of 175 pH, together with a $C_g = 0.22$ pF.

On the other hand for the 3-stages case, the previously cited InMN is kept unchanged, while a new one is added between the two pseudo-common Gate stages. All the three possibilities are again analyzed; the best solution seems to be use of a shunt inductor (296 pH, which leads to a $C_g = 105$ fF).

Unfortunately the GaN device results to be unstable out-of-the-band, requiring the insertion of a dissipative network containing a resistance and some other bypass reactive elements. A negative consequence is the decrease in Gain.
Whilst the network is effective for the CS stage, both the 2-stages and the 3-stages amplifiers can not be stabilized, due to the presence of an instability tank between 20 GHz and 43 GHz.

The previously described procedure is repeated for the GaAs device, starting from the load-pull analysis and following with the InMN choice. The maximum obtainable output power is 25 dBm while the corresponding gain is 12.3 dB.
Also in this case, the best solution for the middle inter-stage matching, resulted to be a 332.3 pH shunt inductance, together with a $C_g = 0.175$ pF.
The third stage required a $C_g = 80$ fF and a 580 pH shunt inductance.
The ideal amplifier is characterized by a gain of 18 dB and an output power close to 29 dBm.

Even if the GaAs device results to be unstable, it can be successfully stabilized.

The proper biasing voltage can be provided to the three transistors, in two ways: an independent biasing network for each Gate terminal or through voltage division from the Drain voltage of the stack (self-bias). The first option is straightforward but requires a large number of sources and reactive element, so the self-bias was chosen.
When biasing, the voltage Source, an ideal voltage generator, is usually followed by wires, transitions, etc.. introducing disturbances in the circuit. A proper network behaves like a short circuit, at the working frequency, while it should be "transparent" at $f \neq f_0$. So a buffer capacitor has to be inserted, making the amplifier less subject to the cited problem. Biasing networks feed the Gate of the CS and the overall Drain voltage.

Input and output matching networks have been designed to adapt the external 50 ohm terminations to the optimum Source and load complex impedances of the stacked cells.

Finally the last design step involves the definition of the layout. It was chosen an asymmetrical solution in order to enhance compactness and cross-talk immunity. Two layouts, one based on lines and one with lumped inductors were proposed; the use of inductors does not strongly change performance with respect to the previous case, but a more compact layout can be obtained.

The use of real components leads to a narrow-band amplifier, as conformed by frequency simulations in the $(24 - 29)$ GHz. Only around 26 GHz can be profitably used, without a performance worsening. In particular for a 3-stages GaAs amplifier the obtained gain is ~ 17.29 dB, while the corresponding P_{OUT} is close to 29 dBm.
If compared to a single stage's performance the output power is about 4 dB larger; ideally it should have been 4.8 dB.

Achieving wide-band behaviour with a stacked cell is a major issue, and it is object of possible future work

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Chapter 1

Introduction

1.1 Thesis Motivation

Radio Frequency communication systems are based on transceivers.
Both the transmission and receiver stages require an amplification of the original signal. In particular a transmitted signal, which propagates through air and matter, is attenuated, so it has to be boosted by an high power amplifier before transmission and by a low-noise amplifier in reception.
The design frequency is chosen to be 26 GHz. It is in the millimeter wave range and in particular it is included into the 5G band, which ranges from 24.25 GHz to 52.6 GHz.
26 GHz and 28 GHz are two of the most important bands for mobile networks, due to the amount of spectrum available.

The possibility to overcame the problem linked to the breakdown voltage limitation and modularity makes the stacked topology particularly interesting at RF. In particular the output power and gain are proportional to the number of stacked stages.
Moreover in a stacked power amplifier the use of Gate capacitance allows, at least at low frequency, to an inter-stage matching and so maximum output power generation, without the need for additional networks.

1.2 Thesis Goal and Organization

The goal is to design a stacked amplifier for high frequency applications, namely working at 26 GHz. A full design procedure involves an initial theoretical part, with the corresponding numerical simulation, followed by a real technology-based analysis. The latter includes the physical layout design, too.

In Chapter 2 the basic concepts of power amplifiers are recalled, with a application

context example; moreover the most relevant figures of merit are defined and analyzed.
In Chapter 3 simulation results are reported: detailing the common Source and common Gate stages and comparing a 2-FET stacked topology with the cascode amplifier.
Chapter 4 is dedicated to the analysis of a real device: the GaN, with all of its parasitic components. In particular technology's performance are evaluated when applied to a CS, 2-stages and 3-stages amplifier. Since at the working frequency the devices results to be unstable, a stabilization network is proposed.
Firstly the de-embedding procedure is applied, in order to define its intrinsic and extrinsic model.
In chapter 5 a new technology, namely the GaAs, is taken into account. The same analysis which was performed in chapter 4 is now applied, in order to compare the obtained results.
The chapter 6 is devoted to the physical structure of the amplifier, the layout. A first look at the single components and networks is followed by their actual application to the overall amplifier.
In particular input and output matching networks are added to the previous design, in order to make it as complete as possible.
Finally the 'real' amplifier's performance are evaluated and compared with the ideal ones.

Chapter 2

Basic Concepts

2.1 Power Amplifier

All the theory about Power amplifiers (PA) can be found in [7].
In order to explain the role of power amplifier in electronics, it is necessary to consider a general transceiver, as reported in fig: 2.1. Both receiver (RX) and transmission (TX) steps require signal amplification, even if the goal of the used amplifiers is different in the two cases.
In particular as for the receiver, once the signal is captured by the antenna and filtered in order to choose the proper channel, it needs to be amplified by a low noise amplifier (LNA), in order to be correctly used. The LNA is a linear amplifier, whose main goal is to amplify the signal introducing the lowest possible additional noise.
What is more interesting in this context is the transmitter: the base-band signal is encoded and through a mixer moved at an higher frequency (around f_{LO}) depending on the local oscillator . After a further filtering step, the signal has to be amplified by a Power amplifier, so to bring the signal to a suitable power level to be transmitted.
Such an amplifier is not linear and trades efficiency, linearity and output power.

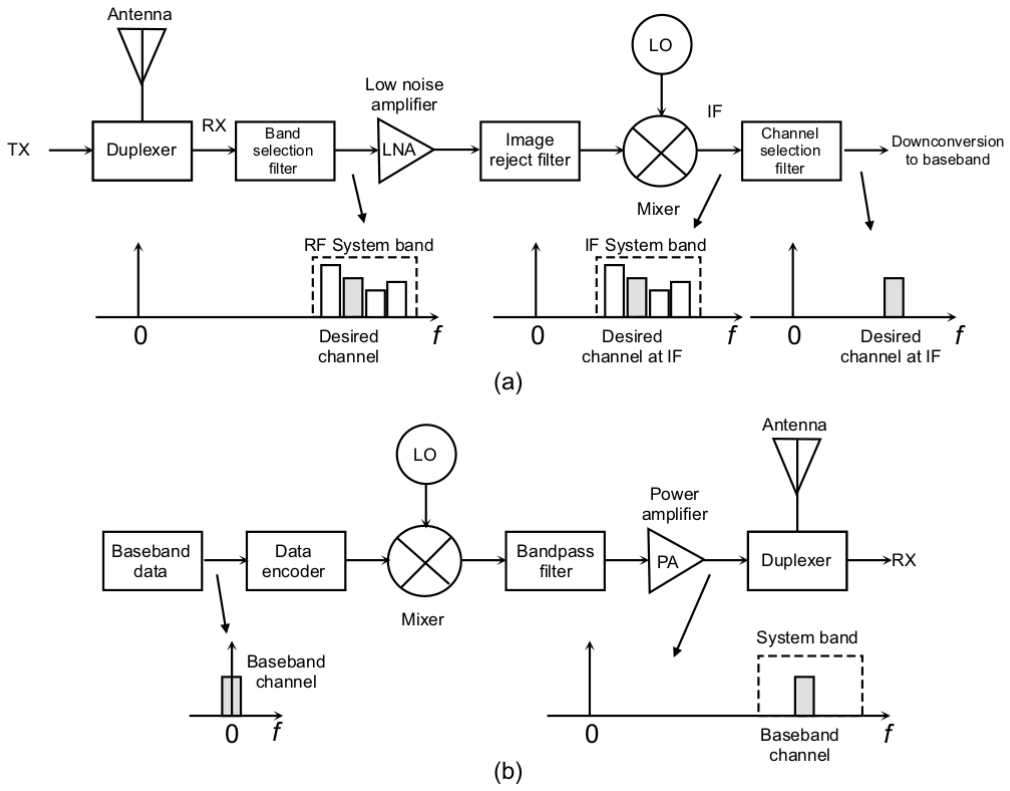


Figure 2.1: Heterodyne TX - RX circuit

A power amplifier can be seen as a device which receives two inputs: a DC feed and the RF signal (at the fundamental frequency f_0) to be amplified; since it is basically non linear, its output will contain a DC component, the fundamental and some harmonic contributions at $n \times f_0$. The device should ideally use part of the DC input power to only amplify the RF component; however unwanted effects such as high-order-harmonics (HOH) and inter-modulation products (IMPs) cause a partial power transfer to the harmonics and so a degradation of the efficiency.

The region in which the amplifier can operate is limited, as for what concerns the voltage, by the breakdown voltage on one side and by the knee voltage on the opposite one.

As for the current, it can sweep between 0 and I_{DSS}. A conservative choice limits the maximum Gate-Source voltage to 0 V, in order not to exceed Shockley potential and thus allowing current to flow through the Gate terminal. When applying a null V_{GS}, I_{DSS} corresponds to I_{max}.

Despite this a positive, but low, V_{GS} can be applied, without direct conduction effects. In the thesis the conservative approach was preferred.

Once the device is biased, the quiescent point can be uniquely defined on the output

characteristics and defining the allowed current and voltage swings. Differently from a linear amplifier, the swing will not only be a small signal variation, but parameters will be able to move over the whole characteristics.
A class A amplifier is characterized by the maximum swing in voltage and current, due to a quiescent point in the centre of the characteristics. This leads to the maximum output power, defined as

$$P_{OUT,max} = \frac{V_{BD} I_{DSS}}{8} = \frac{V_{DS,\,pk}}{\sqrt{2}} \frac{I_{D,\,pk}}{\sqrt{2}}$$

However the efficiency, namely

$$\eta = \frac{P_{OUT}(f_0)}{P_{DC}}$$

is 50% since also for a null RF input, some DC power is dissipated, heating the device.
Despite the ideal maximum power, the achievable one depends on the actual load, which defines the Dynamic Load Line (DLL); in order to obtain the best performance, the DDL should be a straight line, meaning that reactive components are fully compensated, ranging from the maximum voltage V_{DD}, when current is null, to the maximum current, when V_{DS} is equal to the knee voltage. When the amplifier is loaded by a non-optimum impedance, clipping phenomena will cause an output power reduction. Currents and voltages exceeding the limits get clipped, causing non-linear effects such as distortion.

On the other hand the quiescent point of a class B amplifier lays on the horizontal axis, thus allowing for a positive current swings only. When the input signal is null, also the current is 0, causing the power consumption to be null, too.
The harmonic content results to be much stronger due to voltage clipping and so linearity decreases. Therefore a tuned load must be adopted.

An important parameter used to describe an amplifier is the Gain: actually three types are defined, depending on whether the amplifier is input matched or not. However in practice only the operative gain provides interesting results.

$$G_{OP} = \frac{P_{OUT}(f_0)}{P_{in}(f_0)}$$

The input power P_{in} will be lower with respect to the available one, since the unmatched input does not grant maximum power transfer.

Another figure of merit is the Power Added Efficiency (PAE), which follows the efficiency trend when the input power is low, but then decreases with the Gain.

$$PAE = \frac{P_{OUT}(f_0) - P_{in}(f_0)}{P_{DC}} = \eta \left(1 - \frac{1}{G_{OP}}\right)$$

One of the most significant plots describing a power amplifier is the $P_{in} - P_{out}$ characteristic (fig: 2.2), in which it is possible to identify the 1 dB compression point, in which the amplifier is usually employed, in order to maximize the output power (1.6 times the

maximum value in linear region), keeping the harmonics to low values.
Before the compression point the behavior is linear, while after it the output power saturates for any input value; this causes a gain decrease in saturation (fig: 2.3).

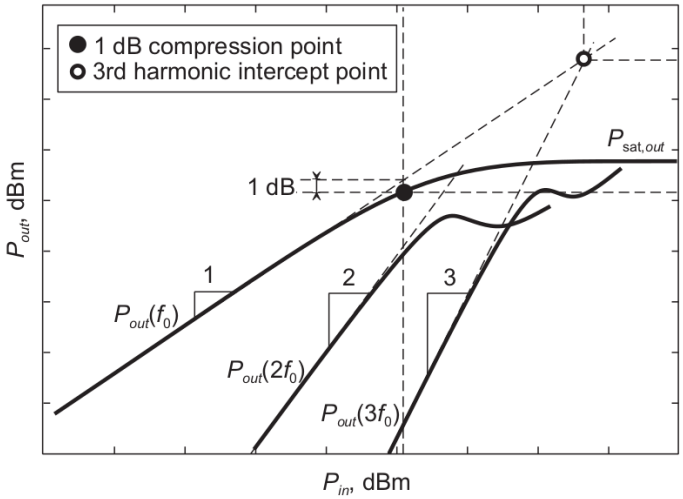


Figure 2.2: $P_{in} - P_{out}$

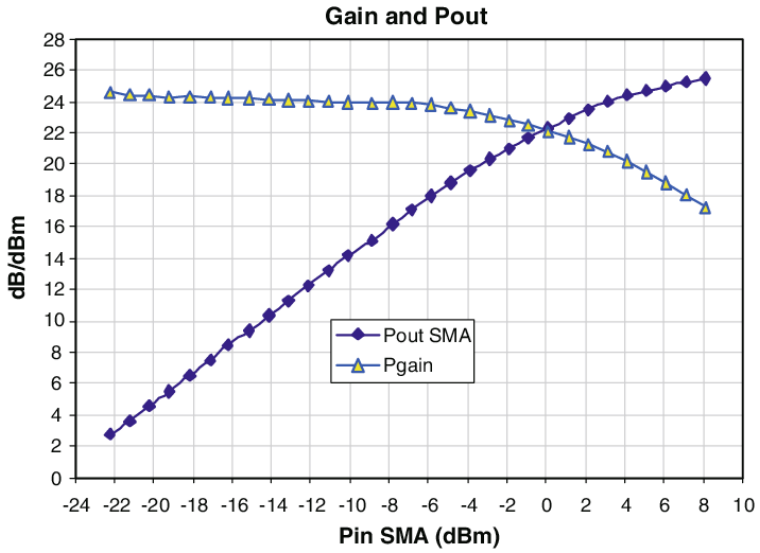


Figure 2.3: $P_{in} - Gain$

Chapter 3

Cascode and Stacked PA

3.1 The Cascode PA

3.1.1 Introduction - Cascode Amplifier

The cascode amplifier, whose schematic is reported in fig: 3.1, is made up of two stages: a CS and a CG. The former drives the Source of the CG; latter's Gate is grounded. It was firstly proposed by Roger Wayne Hickman and Frederick Vinton Hunt in 1939 for voltage stabilization applications [13].

The cascode shows the same transconductance of a single CS stage, but this configuration introduces some positive characteristics too, such as improvement in the input and output impedance and higher input-output isolation.
Since the CS is loaded by a low input impedance stage (the CG), its gain $A = gm \times V_{gs}$ dramatically falls; this result is however positive since the feedback capacitance C_{GD}, which causes a bandwidth reduction proportional to the 1^{st} stage gain (Miller effect), results to be much less significant. Rephrasing, Miller capacitance seen from the input results to be much lower than a single stage's one. So the main advantage of the cascode is the improvement in frequency behavior.
The reduction in gain can be compensated by a proper choice of the load (active loads); overall the cascode configuration does not lead to a significant increase in gain with respect to a CS stage.

Disadvantages are linked to the presence of a further component with respect to the single FET amplifier. As a consequence an higher supply voltage will be required; both the transistors have to operate in saturation, imposing limitations on the lower acceptable value of V_{DD}.

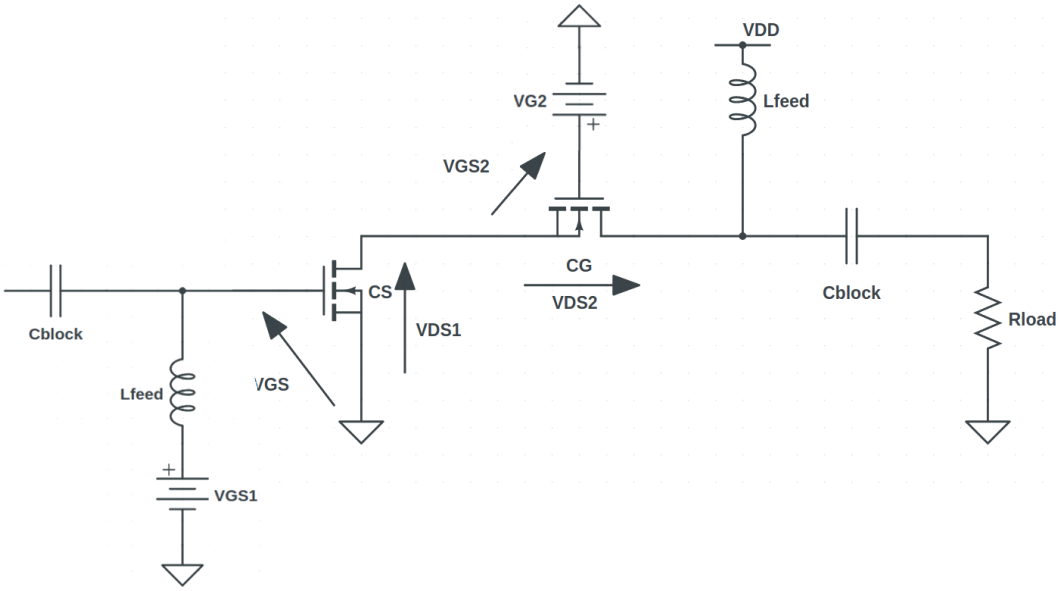


Figure 3.1: Cascode circuit

3.1.2 Analysis and Simulation with Ideal Components

FET Parameters

A FET can be modeled in different ways, depending on how $I_{ds}(V_{gs})$ is described: Curtice's quadratic and its natural evolution is the cubic model, which takes into account for a large range of phenomena, neglected by its predecessor; it results to be more realistic but is complicated to be employed.

In the following simulations it will be used a linearized model of Curtice's quadratic model, whose circuit is represented in fig: 3.2.

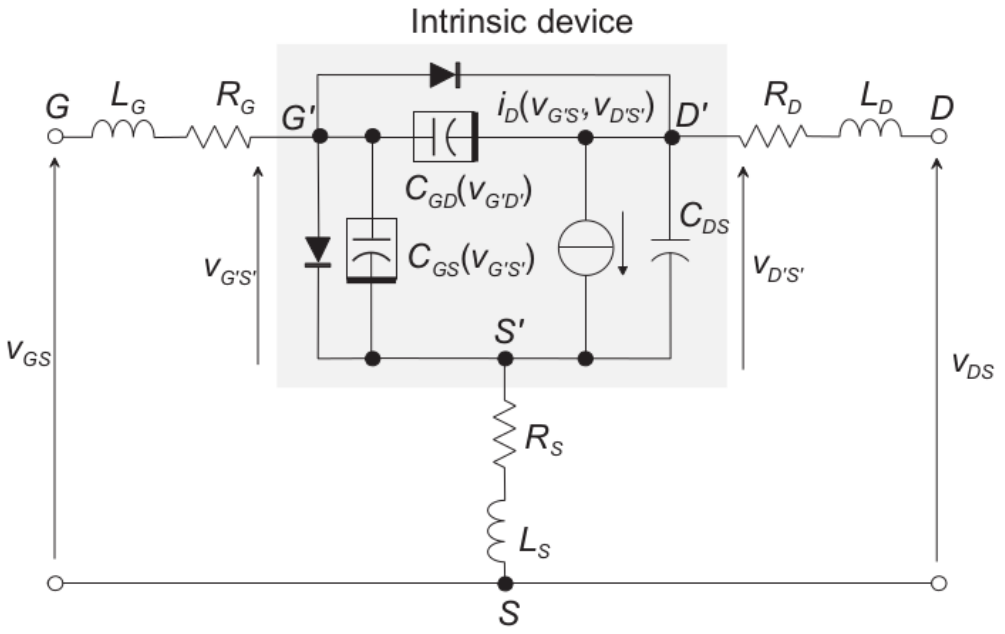


Figure 3.2: Curtice FET model

It is possible to identify Extrinsic and Intrinsic parameters. The former are linked to the inductive behavior of traces and can be represented as a L-R series impedance on each terminal. Besides, the latter ones include capacitances, resistances and the driven current Source.
Taking a closer look at the intrinsic components, the difference in capacitors is noteworthy as the Drain-Source capacitance is mainly geometrical and therefore turns out to be weakly dependent on V_{GS} and V_{DS}; thus it is approximately constant. On the other hand C_{GD} and C_{GS} are strongly dependent on driving voltages.
Other components are the two diodes simulating direct Gate conduction, which takes place when the Shockley junction potential is overcome, and breakdown, respectively.
The active element, namely the controlled current Source results to be dependent on V_{GS} and V_{DS} and can be described by the following equation:

$$i_{DS} = [A0 + A1 \times v_1 + A2 \times v_1^2 + A3 \times v_1^3] \times [1 + \lambda v_{DS,i}] \times \tanh(\alpha v_{DS,i})$$

where

$$v_1 = v_{GS,i}[1 + \beta(v_{DS0} - v_{DS,i})]$$

By fitting all the parameters in the previous equation, a proper characteristics can be obtained; in particular chosen model parameters and technological parameters are shown

in tab: 3.1 and tab: 3.2, respectively.
These will be used in section 3.1.2: to design the cascode amplifier.

A0	A1	A2	A3	C_{GS}	C_{GD}	C_{DS}
0.5 A	0.5 A/V	0 A/V^2	0 A/V^3	0.7 pF/mm	0 F/mm	0 F/mm

Table 3.1: Ideal FET model parameters

g_m	I_{DSS}	V_{th}	f_T	C_{GS}
500 mS/mm	700 mA/mm	−1 V	110 GHz	0.7 pF/mm

Table 3.2: Ideal FET technological parameters

For simplicity all the parasitic capacitors are set to 0, a part from C_{GS}, which will be necessary in the following when introducing the Pseudo-common Gate stage. Also λ and α are null. Since the terms A2 and A3 were chosen to be null, the model is simplified to a linear one, which can be described as

$$I_{DS} = [A0 + A1 \times V_{gs} + A2 \times V_{gs}^2 + A3 \times V_{gs}^3] \;=\; [0.5\,\text{A} + 0.5\,\text{A/V} \times V_{gs}]$$

However

$$I_{DS} = g_m(V_{gs} - V_{th})$$

so that $g_m = 0.5\,\text{A/V}$ and $V_{th} = -1V$.

Also breakdown voltage is neglected in this first model, by setting it at a very high value.

Common Source stage

The Common Source stage is one of the principal amplification stages: the input signal to be amplified is applied to the Gate of the FET and the corresponding output is taken on the Drain terminal. The schematic is reported in the following figure:

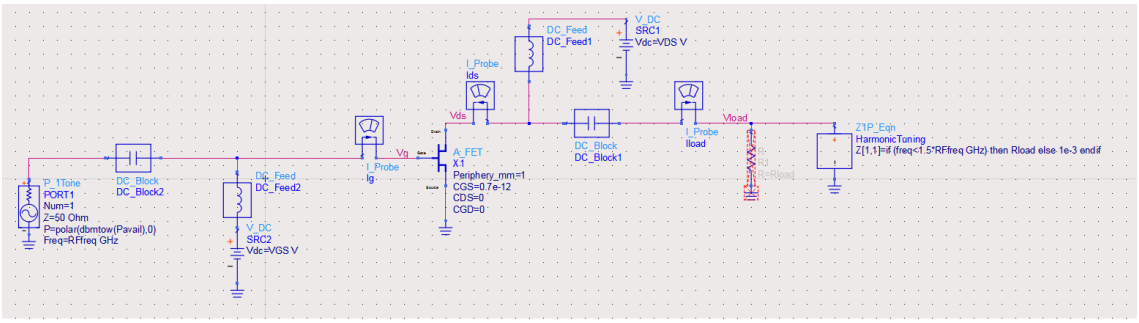


Figure 3.3: Common Source circuit

The first step is selecting the quiescent bias point, which in turn defines the class of operation of the amplifier. The FET trans-characteristic and output characteristics are shown in Fig: 3.4, for a class A amplifier, for which the quiescent point has to fall in the middle of the output characteristics, so that $I_{DS} = \frac{I_{DSS}}{2} = 0.35\,\text{A}$. The corresponding input voltage is $-0.3\,\text{V}$.
Moreover the Drain-Source voltage is arbitrarily chosen to be $6\,\text{V}$, to be representative of MMIC GaAs technologies, since the breakdown occurs at $12\,\text{V}$.
Another important feature that can be inferred from the output characteristics, is the optimum load: since the model does not take into account parasitic components, a part from C_{GS}, the load is purely resistive, $Z_{opt} = R_{opt}$, which in turn, is equal to $\frac{v_{DS}}{i_{DS}}$. The optimum value of the ratio leads the characteristic to be fully covered, allowing the maximum possible swing for both current and voltage. A larger resistance would decrease the slope of the dynamic load line, causing current clipping; besides a smaller load leads to voltage clipping due to a larger slope.

For a class A amplifier $R_{opt} = 2 \times \frac{V_{DS} - V_{knee}}{I_{DSS}}$, which is about 15Ω, as shown in the plot. A different value would lead to clipping effects and so to distortion.

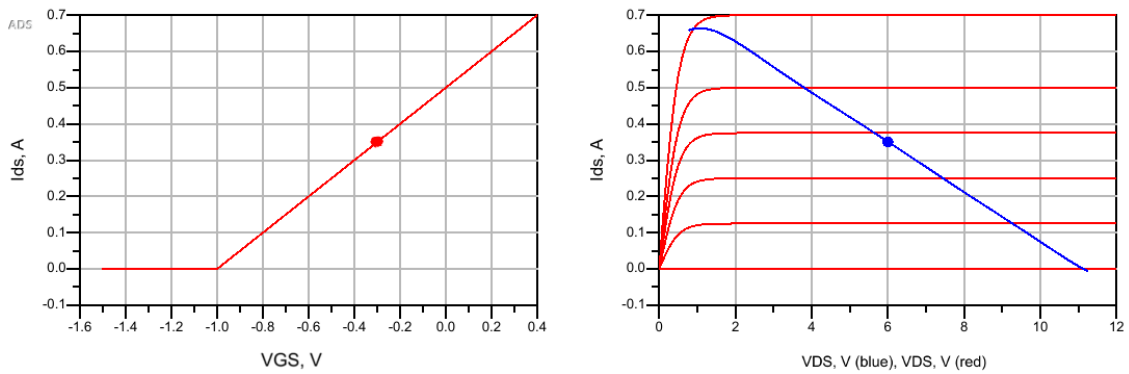


Figure 3.4: Common Source trans-characteristic(left) and output characteristics with dynamic load line (right)

Finally Drain efficiency's behavior is shown in fig: 3.5 : for a class A amplifier, it should be about 50%, in correspondence of the 1 dB compression point, where the amplifier is supposed to be used in order to obtain the best performance. The maximum efficiency does not consider the effect of the knee voltage, otherwise it would be a bit lowered.

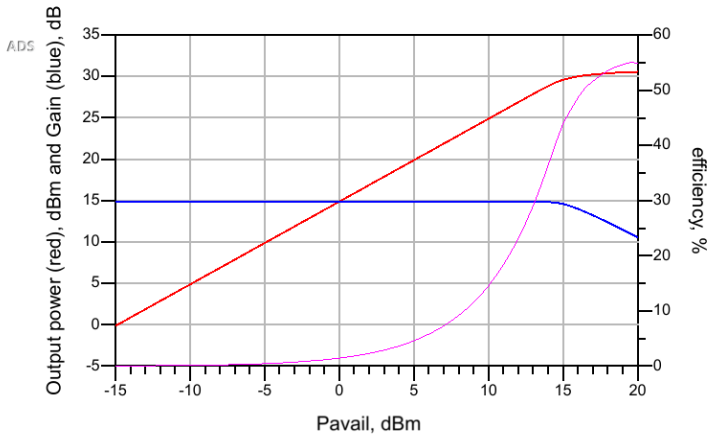


Figure 3.5: Common Source Parameters: P_{OUT}, Gain and DE

As for the maximum output RF power, namely

$$P_{max} = \frac{1}{8} \times 2(V_{DS} - V_{knee}) \times I_{DSS} = 0.96\,\text{W or } \ 30\,\text{dBm}.$$

This result is also reported in fig: 3.5.
The operating gain, defined as $\frac{P_{out}}{P_{in}}$, is about 15 dB, with the selected model parameters.

Taking now into account a class B amplifier and so choosing a $V_{GS} = -1\,\text{V}$, namely the threshold voltage, the quiescent point will be on the horizontal axis, i.e. at zero Drain

current, as shown in fig: 3.6. The optimum load is the same as in the previous case, while the gain is 6 dB lower, as expected and efficiency goes up to roughly 78%, as shown in fig: 3.7 and as expected from theory [7].
In the following simulations, a tuned load is applied.

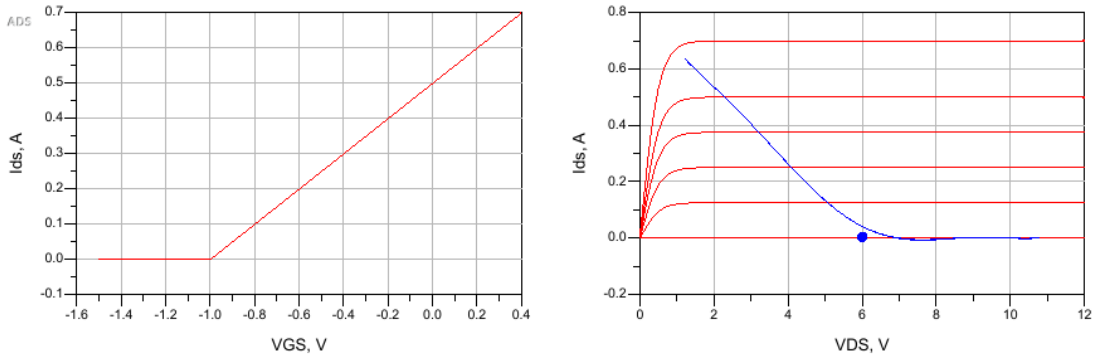


Figure 3.6: Common Source trans-characteristic (left) and output characteristics with dynamic load line (right)

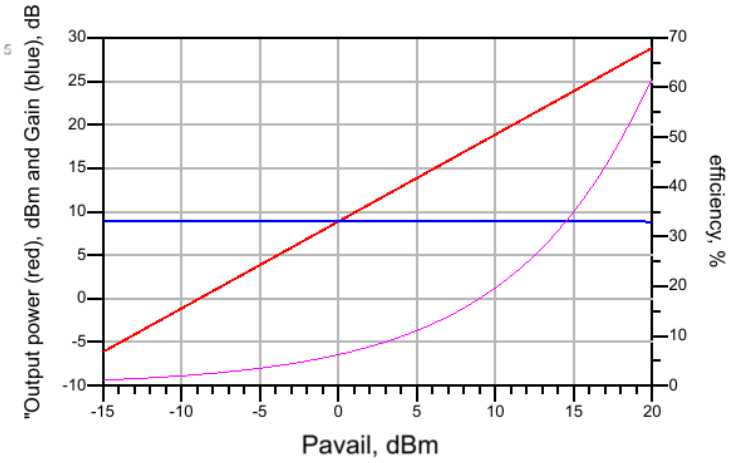


Figure 3.7: Common Source parameters: P_{OUT}, Gain and DE

For V_{GS} between $-1\,\mathrm{V}$ and $-0.3\,\mathrm{V}$ the amplifier works as a class AB.
Fig: 3.8 shows the efficiency and gain when sweeping the Gate-Source voltage, from values associated to a class A up to a class AB.
As shown in fig: 3.8, the maximum efficiency ranges between 50% and 78%, while gain undergoes soft compression before saturation as a function of the input power. To take into account this phenomenon the optimum load should be set slightly higher than that of class A.

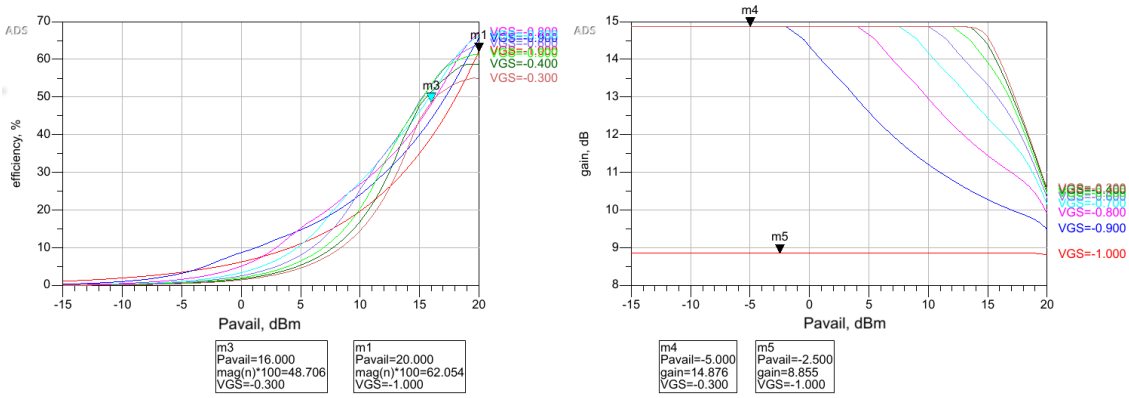


Figure 3.8: Common Source parameters behavior when sweeping V_{GS}

Common Gate stage

The second stage of a cascode is the common Gate, for which the input signal is injected in the Source terminal and the output is taken from the Drain one.
Since it will be used as the second stage for the cascode, it is necessary to consider the voltage on the Drain of the previous stage (i.e. at the Source of this stage), namely 6 V; moreover it is necessary to make it work in the same condition as the other stage and so on the Drain the applied voltage will be 12 V. So that the overall V_{DS} is 6 V.

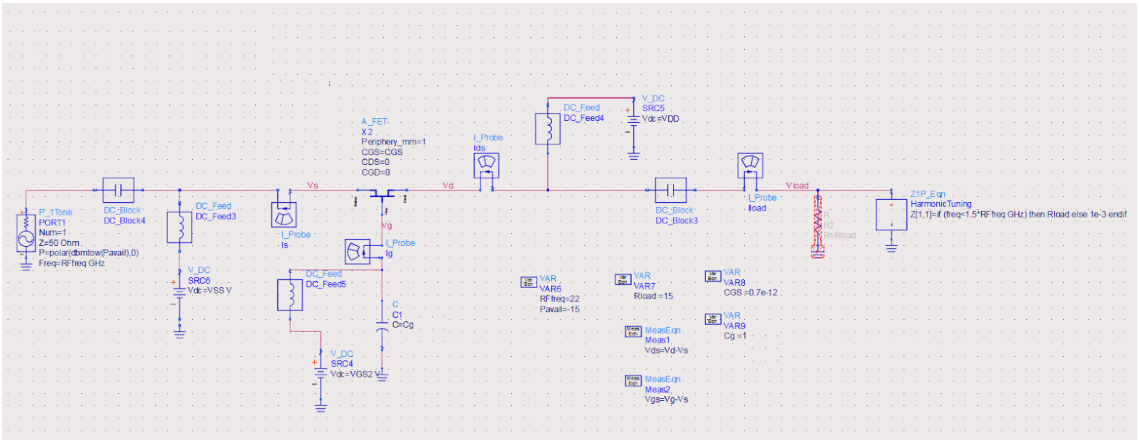


Figure 3.9: Common Gate circuit

Since it is biased in the same point of the common Source stage, it will be characterized by the same R_{opt}, given in section: 3.1.2.
The CG stage is a non-inverting stage, so both load and Drain-Source currents and voltages are in phase. Fig: 3.11 shows CG's performance in terms of P_{out}, Gain and efficiency.
The output power follows the classical behaviour: it linear for low input power, while

saturates after compression. It is $\sim 31\,\text{dBm}$ at $1\,\text{dB}$ compression, as expected for a Class A amplifier and reported in the previous section for a CS.
According to simulations, Gain is $7.8\,\text{dB}$ at $1\,\text{dB}$ compression.
Finally the efficiency results to be $\sim 80\%$.

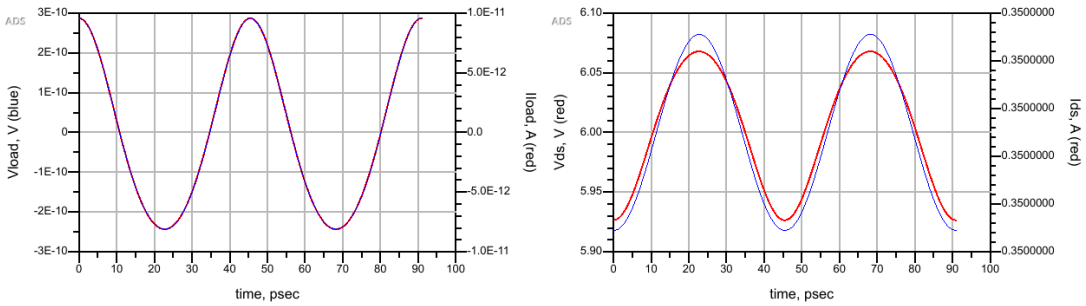


Figure 3.10: Common Gate stage waveforms in phase: V_{load} and I_{load} (left); V_{ds} and I_{ds} (right)

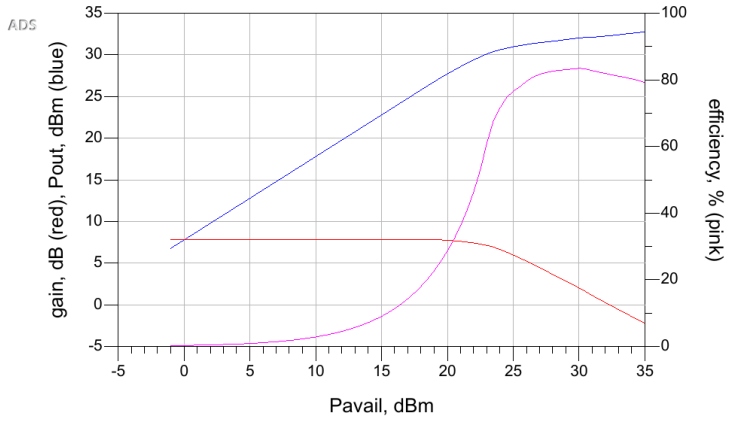


Figure 3.11: Common Gate stage performance: P_{OUT}, Gain and DE

Complete Cascode

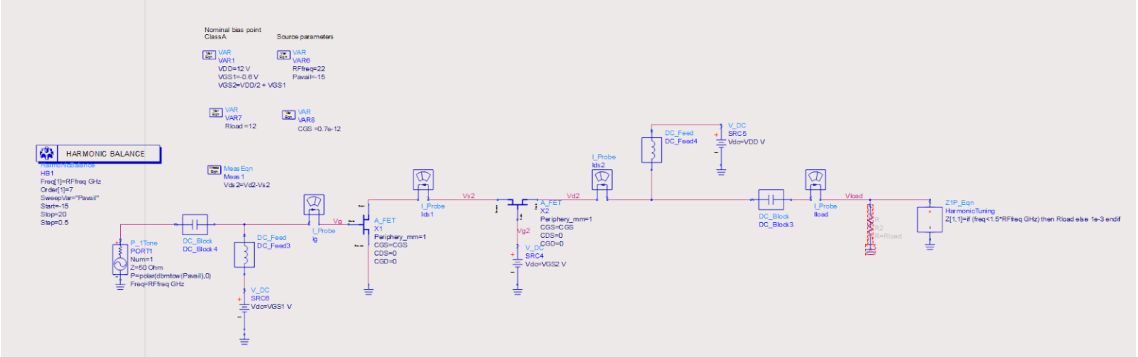


Figure 3.12: Cascode circuit

The supply voltage V_{DD} will be defined as $V_{DS,CG} - V_{TH}$, given the maximum Drain-Source voltage of the CS stage to be V_{TH}. Since $V_{DS,CG} = 6\,\text{V}$, and the threshold voltage is $-1\,\text{V}$, $V_{DD} = 7\,\text{V}$.
In order to keep both the transistors in saturation, the voltage supply is divided as follows between the two devices: $V_{DS,CG} = 5\,\text{V}$ and $V_{DS,CS} = 2\,\text{V}$. As a consequence, CG Gate voltage has to be $V_{DS,CS} + V_{GS} = 2\,\text{V} - 0.3\,\text{V} = 1.7\,\text{V}$.

As for the the dynamic load line, reported in fig: 3.13 (upper plot), it is clear that the optimum load for the CG stage is purely resistive, and the dynamic load line is a straight line; it is linked to the fact that the chosen load is a resistor. On the other hand CS stage's dynamic load line is turned into an ellipse, indicating that the optimum impedance will have complex component, too. It is due to the presence of a capacitive component, namely C_{GS}, in the following stage.

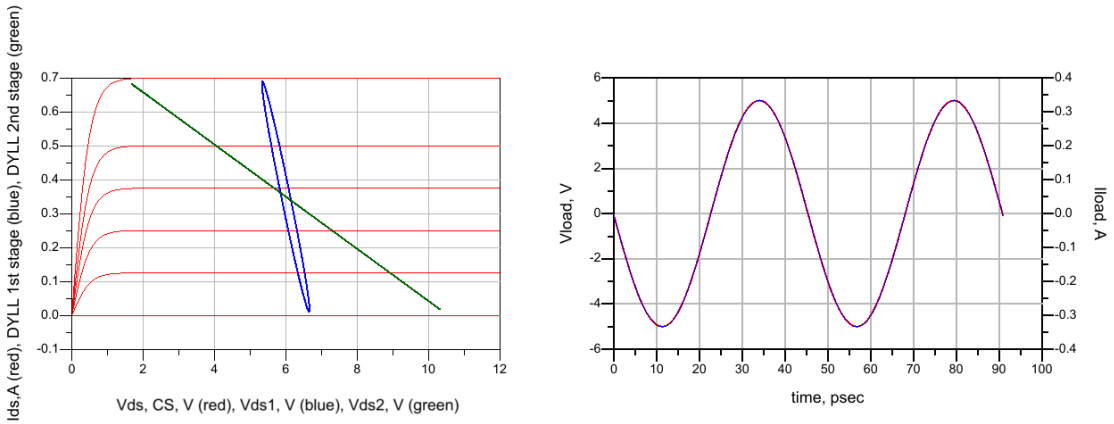


Figure 3.13: Cascode dynamic load lines by CS and CG stages (left); in-phase V_{load} and I_{load} (right)

As for the waveforms on the load (fig: 3.13 left plot), they're both sinusoidal and in phase.

Let's now take a look at Cascode performance in fig: 3.14. Its efficiency, gain and output power are basically the same as a single CS stage (fig: 3.5), as expected.

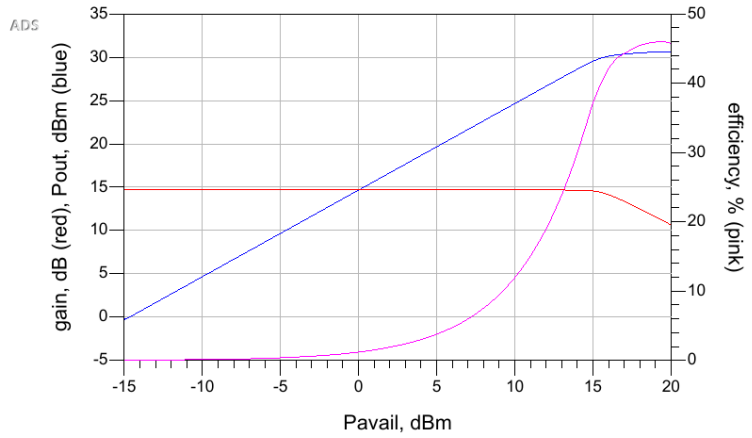


Figure 3.14: Cascode performance: P_{OUT}, Gain and DE

Taking now a closer look at the CG stage, given that the only parasitic component taken into account up to this point is the Gate-Source capacitance, the input admittance of a CG stage, seen from its Source terminal, will be the sum of two contributions: the real component is given by g_m, while the imaginary part, it is due to C_{GS}, only.

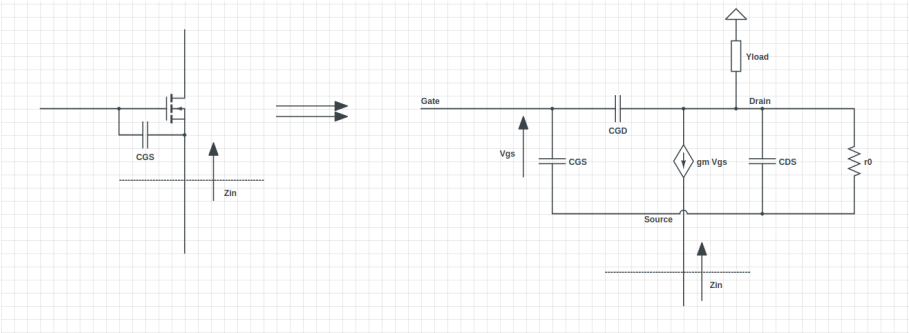


Figure 3.15: CG input admittance's computation simplified circuit

The overall admittance will be $Y_{in} = g_m + j\omega C_{GS}$. Given the technological parameters $g_m = 0.5\,\mathrm{S/mm}$ and $C_{GS} = 0.7\,\mathrm{pF/mm}$, harmonic components' simulations results, are shown in fig: 3.16.

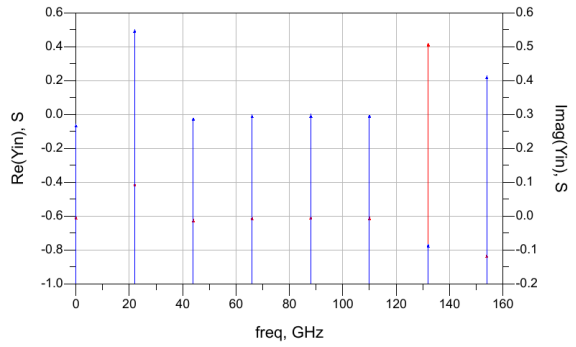


Figure 3.16: CG input admittance - harmonic components

3.2 Stacked Amplifier

3.2.1 Introduction - Stacked Amplifier

When designing a single transistor amplifier, a main issue is the limited allowed Drain voltage swing, due to the low breakdown voltage and the high knee voltage[10].
An increase in device's size is deprecated because of the increased device parasitics, and of the more complicated matching networks required due to the lowering of input and output impedances.
Combining many devices is thus mandatory to achieve high output powers.
The use of parallel transistors does this by summing up the current contributions, at fixed V_{DS}, but it shows some disadvantages such as the reduction in the output impedance

and the increase in DC Drain current. Moreover, being in parallel, the effect of parasitic capacitances will be stronger and stronger depending on the number of devices. Finally this solution requires increasing the input power, in order to feed all the FETs.
An alternative solution is represented by the stacked-FET amplifier [3]: the schematic is reported in fig: 3.17.

An n-stage Stacked amplifier is made up of two basic stages: a Common Source and $(n-1)$ Pseudo-Common Gate, which corresponds to a Common Gate with a Gate capacitance connected on its Gate terminal. The presence of C_{GS} causes a voltage division between the Gate-Source capacitance itself and the Gate capacitance.
If necessary other Pseudo-CG stages can be added in series to the first one, making the stacked structure, modular. Each stage of making the stacked amplifier will be characterized by the same electrical quantities, such as V_{DS}, V_{GS} and so current, etc.. All the stages are so designed to work in the same quiescent point.
The use of series devices cause an increase in the Drain voltage while keeping the total Drain current equal to that of a single FET; moreover the gain will result higher with respect to the parallel FET architecture, since the input power splitting is not required.
Even if single device's Drain-Source voltage is basically unchanged, in order to avoid breakdown, the achievable total Drain-Source voltage can be much higher, namely $n \times V_{DS}$, where n is the number of stacked transistors, and the output power will be consequently n times higher.

In tab: 3.3, some characteristics of parallel and series amplifier topologies are compared.

	Single FET	Parallel FETs	Stacked amplifier
I_{DS}^{pk}	I_m	$n \times I_m$	I_m
V_{DS}^{pk}	V_m	V_m	$n \times V_m$
Z_{OUT}	R_{OPT}	R_{OPT}/n	$n \times R_{OPT}$
P_{OUT}^{RF}	$\frac{1}{8}V_m I_m$	$n \times \frac{1}{8}V_m I_m$	$n \times \frac{1}{8}V_m I_m$
P_{IN}^{RF}	P_i	$n \times P_i$	P_i
P_{DC}	$\frac{1}{2}V_m I_m$	$\frac{1}{2}V_m I_m \times n$	$\frac{1}{2}V_m \times nI_m$
Voltage Gain	$g_m R_{OPT}$	$g_m R_{OPT}$	$n \times g_m R_{OPT}$
C_{in}	C_{gs}	$n \times C_{_{gs}}$	$C_{_{gs}}$

Table 3.3: FET amplifier Topology comparison

The parallel FETs topology can not be said to be modular since by adding new devices, the input impedance decreases causing the input matching network to be redesigned; on the other hand it does not happen for the stacked amplifier for which new stages can be added without altering the previous ones given that every transistor works in the same quiescent point. In addition it can be shown that the DC characteristic of an ideal stacked amplifier is the same as a single FET stage, simply with the Drain voltage scaled by a factor n.

The maximum number of stages which can be stacked is limited by the cutoff frequency of the technology as:

$$n_{max} = \left\lfloor \frac{1}{ln(1 + f_0/f_T)} \right\rfloor$$

Biasing

In the stacked amplifier, all the cells must be biased at the same quiescent point, so as to generate in-phase V_{DS} voltages
Since the stages share the same DC current, each transistor should have the same V_{GS}.
In order to satisfy this requirement, the corresponding Gate voltage for the CS stage is $V_G = V_{GS0}$, then, in order to obtain the same voltage drop, the Gate voltage of the i^{th} CG stage must be set to:

$$V_{G,i} = V_{DD}^{(i-1)} + V_{GS}^{i} = \frac{V_{DD}}{n}(i-1) + V_{GS0}$$

where n is the overall number of stages, while i is the actual stage.
The biasing Gate voltage can be directly provided from the outside at the correct level, even if it requires a proper feed network for each of the devices. Another method, much more efficient in terms of additional elements to be inserted is named self-bias and will be analyzed in section: 5.5.3.
In spite of this, in the following simplified simulations, the bias will be provided through external sources on each Gate terminal.

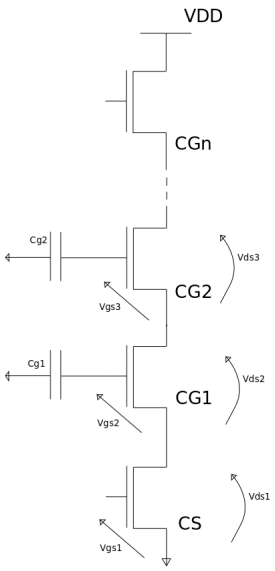


Figure 3.17: Stacked amplifier circuit topology

3.2.2 2-stages Stacked amplifier

A 2-stage Stacked amplifier is made up of the same two stages of a Cascode: a Common Source and a Common Gate; the only circuital difference is the presence of the Gate capacitance on the latter, making it a Pseudo-CG stage (hereafter indicated just as CG).

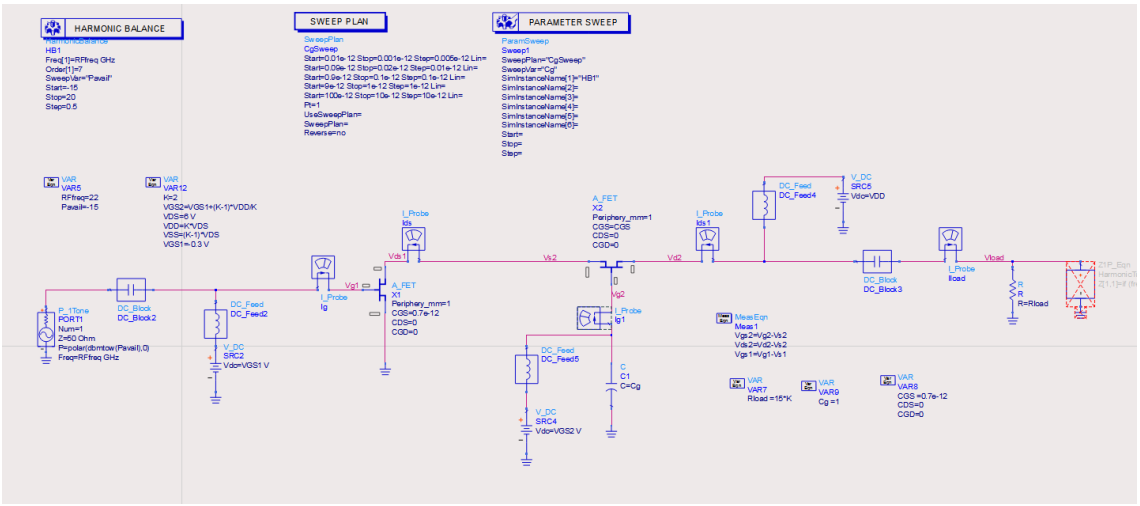


Figure 3.18: Stacked amplifier circuit

Despite the improved reliability, the partition causes a worsening in gain with respect to the ideal 3 dB, due to the fraction of P_{OUT} reaching the Gate of the following stage, with respect to the ideal case; the real gain is so defined as $n \times Gain_{CS} - (n-1)$. A similar reasoning can be applied to the power.

Pseudo-CG input impedance

Taking into account the small signal circuit of the Common Gate stage and neglecting C_{GD} and C_{DS}, the resulting schematic is the following:

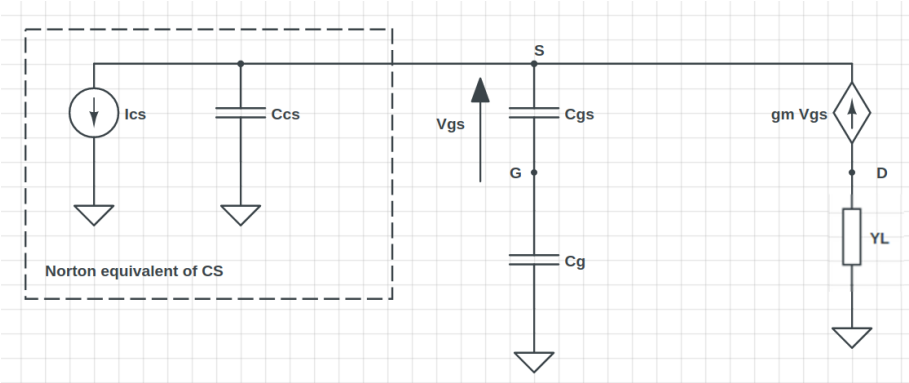


Figure 3.19: 2-stages Stacked amplifier small signal simplified circuit for Y_in and Z_{DS} computation

From the small signal circuit in fig: 3.19, the following equations can be defined, through KCL and KVL:

$$v_{in} = -v_{gs} - \frac{i_g}{j\omega C_g}$$
$$i_{in} = -(i_g + g_m v_{gs})$$

Moreover i_g can be computed by applying ohm's law for impedances as:

$$i_g = v_{gs} \times j\omega C_{gs}$$

So

$$Y_{in} = \frac{i_{in}}{v_{in}} = \frac{-(i_g + g_m v_{gs})}{-v_{gs} - ig/j\omega C_g} = \frac{v_{gs} j\omega C_{gs} + g_m v_{gs}}{v_{gs} j\omega C_g + v_{gs} j\omega C_{gs}} \times j\omega C_g =$$

$$= \frac{j\omega C_{gs} + g_m}{1 + C_{gs}/C_g}$$

Now, setting

$$A = 1 + C_{gs}/C_g \tag{3.1}$$

the previous results can be written as:

$$Y_{in} = \frac{g_m}{A} + j\omega \frac{C_{gs}}{A} \tag{3.2}$$

The input impedance of the Stacked amplifier is not so different from the a cascode's one, as reported in section: 3.1.2, a part from the introduction of the A term.

Under the hypothesis that C_{gd} and C_{ds} are both null, the optimum impedance has to be purely real, namely $Z_{opt} = R_{opt}$; as a consequence, in order to obtain matching with the previous stage, $Re\{Z_{in}\} = R_{opt}$ so

$$\frac{A}{g_m} = R_{opt} \quad \Rightarrow \quad A = g_m R_{opt}$$

As a consequence, the input admittance can be rewritten as:

$$Y_{in} = \frac{1}{R_{opt}} + j\omega \frac{C_{gs}}{g_m R_{opt}} \tag{3.3}$$

Focusing on the imaginary term of eq. 3.3, it is possible to observe that it is *capacitive* and dependent on the ratio $\frac{C_{gs}}{g_m}$, which correspond to the cutoff frequency of the device ω_T.
The final result will consequently be

$$Y_{in} = G_{opt}\left(1 + j\frac{\omega}{\omega_T}\right)$$

From a theoretical point of view, when the working frequency is much lower than f_T, ($f_0 << f_T$), the second term results to be negligible and so the overall admittance can be approximated with its real part only. In this condition each device shows a purely resistive impedance and matching can be performed by simply tuning the Gate capacitance of the following stage[3].
On the contrary at higher frequencies, the input impedance eq: 3.3 shows an increase in its reactive term, linked to the Gate-Source capacitance. As the capacitive component is introduced, a shift in voltages' phase occurs; the so called waveform de-phasing, causing V_{DS} of the different stages not to be in phase.
Reactive inter-stage elements will be necessary to guarantee the single V_{DS} to be in phase. In particular since the parasitic contribution is capacitive, the compensating element will have to be inductive; since in this section only ideal components are analyzed, inter-stage matching networks will be explained in section 4.8.1, applied to real devices.
Furthermore at $f_0 \sim f_T$, the device can not be considered unilateral any more leading to a more and more relevant role of C_{GD}.
Because of the cited phenomena, when working at high frequency, the optimum load is a complex number, making it quite impossible to manually compute the correct Gate capacitance to be inserted at each stage. As a consequence a real design involves the use of simulation, so to optimize C_g, taking into account all the parasitic effects, as shown in the section dedicated to the real device.

Pseudo-CG output impedance

The output impedance is defined as $Z_{DS} = \frac{v_{ds}}{ids}$, at operative conditions.
The input of the Common Gate is represented by a Norton equivalent current generator and the corresponding capacitance that model the Common Source stage; as a consequence $I_{cs} = g_m v_{gs1}$.
The transconductance, g_m, is the same for the CS and CG stage, since they adopt the same device; the same is true for the parasitic capacitances.

According to KCL :

$$g_m v_{gs} = g_m v_{gs} - v_{gs} j\omega C_{gs}$$

$$v_{gs}(g_m + j\omega C_{gs}) = g_m v_{gs} \quad \Rightarrow \quad v_{gs} = \frac{g_m v_{gs}}{g_m + j\omega C_{gs}}$$

The ratio $\frac{g_m}{C_{gs}}$ is defined as cutoff frequency of a FET device ω_T, so

$$v_{gs} = \frac{1}{1 + j\omega/\omega_T}$$

The Drain-Source voltage can also be written as a function of v_{gs}:

$$v_{ds} = -Z_L g_m v_{gs} + v_{gs} - \frac{i_g}{j\omega C_g}$$

By adopting the parameter A (eq: 3.1) defined in section: 3.2.2, $-v_{gs}A = -v_{gs} + \frac{i_g}{j\omega C_g}$, v_{ds} can be defined as

$$v_{ds} = v_{gs}(-Z_L g_m + A)$$

Finally the Drain-Source impedance is

$$Z_{DS} = \frac{v_{ds}}{ids} = \frac{-Z_L g_m + A}{-g_m} = Z_L - \frac{A}{g_m} \tag{3.4}$$

By choosing a proper value of A, namely $g_m R_{opt}$, $Z_{ds} = Z_L - R_{opt}$.
Since the objective is to achieve $Z_{ds} = R_{opt}$, needed to achieve the maximum swing , the load impedance will have to be equal to $2R_{opt}$ so that $Z_{ds} = 2R_{opt} - R_{opt} = R_{opt}$.
From eq. 3.4 the Drain-Source impedance is independent on the actual output impedance of the previous stage; it is still true if $C_{ds} \neq 0$. The only element that influences it is the Gate capacitance C_g.

Ideal 2-stages Stacked amplifier performance

Given the previous equations, it is possible to choose a proper Gate capacitance for the CG stage, which is able to guarantee inter-stage matching, providing the CS with its optimum resistance.
In order to make some numerical computations, some data is required: as defined in section: 3.1.2, the optimum impedance of a CS stage is 15 Ω; moreover the Gate-Source capacitance is set to 0.7 pF/mm (see section: 3.1.2). Finally, the transconductance, previously obtained from the input characteristic (section: 3.1.2) of the CS stage, was 0.5 A/V. Under the hypothesis that

$$A \;=\; g_m \times R_{opt} \;=\; 0.5\,\text{A/V} \times 15\,\Omega \;=\; 7.5$$

Under the hypothesis of a $1mm$ periphery and by inverting eq: 3.1, it is now possible to find C_g :

$$C_g = \frac{A-1}{C_{GS}} = \frac{7.5-1}{0.7\,\text{pF}} = 0.107\,\text{pF}$$

The input admittance, defined in eq: 3.3, working at 26 GHz, can be estimated to be

$$Y_{in} = \frac{1}{15\,\Omega} + j \times 2\pi \times 26\,\text{GHz}\frac{0.7\,\text{pF}}{0.5\,\text{A/V} \times 15\,\Omega} = (0.067 + j0.013)\,\text{S}$$

Let's now apply theoretical results.

The obtained dynamic load lines are reported in the first plot in fig: 3.20; the green one, namely CG' one is a straight line, meaning that the used load is real.

The blue curve, associated to the CS, differently, has a more elliptical shape because of parasitic capacitances.

The other plots show voltage and currents in time: only V_{load} and I_{load} are in-phase, due to the resistive load. The other twos are shifted, meaning a complex load is required for both the stages.

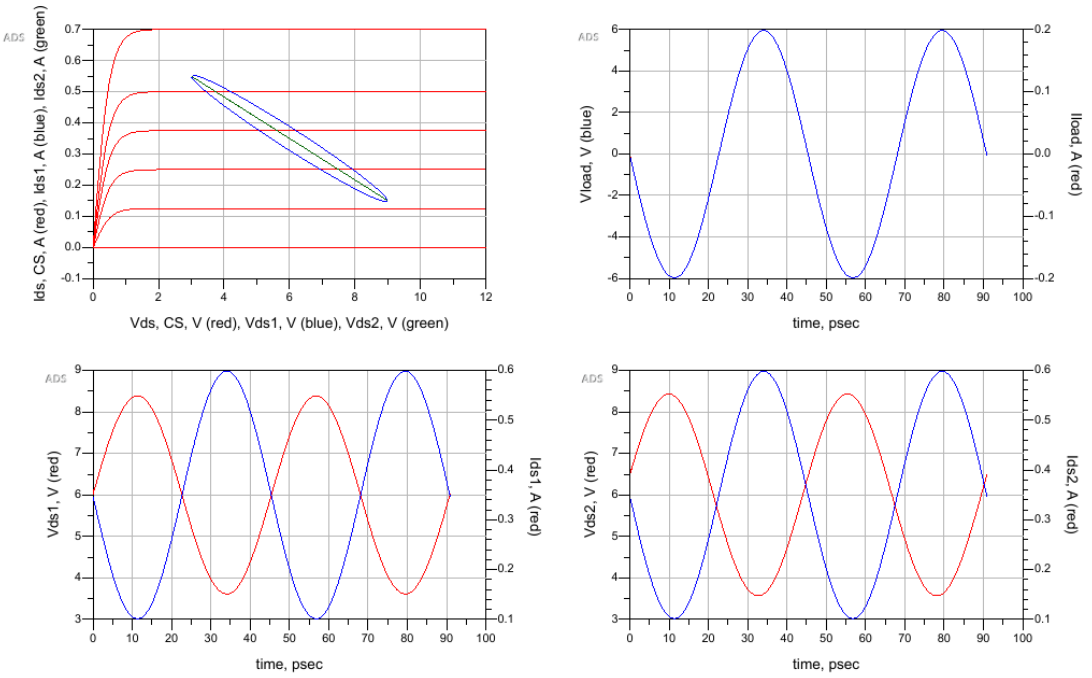


Figure 3.20: Stacked amplifier DLLs for CS and CG stages (top left); in-phase I_{load} and V_{load} (top right); de-phased I_{ds1} and V_{ds1} (bottom left); de-phased I_{ds2} and V_{ds2} (bottom right)

Fig: 3.21 shows a 2-stages Stacked amplifier performance. A comparison with the CS stage will be performed in the following sections.

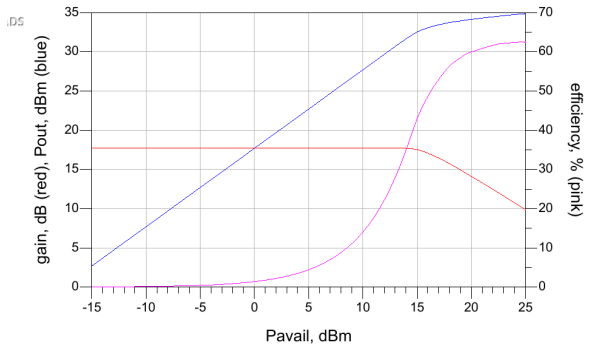


Figure 3.21: Stacked amplifier performance: P_{OUT}, Gain and DE

Simulated input impedance and output impedance are reported in fig: 3.22 and fig: 3.23, respectively. Also the actual A is computed.
In particular Y_{in} and Z_{DS} are computed both trough the definition (Y_{th} and Z_{th}) and through circuital quantities (Y_{in} and Z_{DS}), such as voltages and currents.
Theoretical values are confirmed by simulations.

Eqn YinCG=-Ids.i/Vds2

Eqn Zin=1/YinCG

YinCG[indCg,indP,1]	Zin[indCg,indP,1]
0.067 + j0.013	14.468 - j2.800

Eqn A=1+CGS[0,0]/Cg[indCg]

Eqn Yth= 0.5/A+j*2*pi*26e9*CGS[0,0]/A

Eqn Zth=1/Yth

A	Yth	Zth
7.495	0.067 + j0.013	14.449 - j2.796

Figure 3.22: Stacked amplifier Y_{in}: computed and measured comparison

Eqn Zds=-Vds2/Ids1.i

Eqn Zdsth=Rload[0,0]-A/0.5

Zds[indCg,indP,1]	Zdsth
15.010 + j1.066E-10	15.010

Figure 3.23: Stacked amplifier Z_{DS}: computed and measured comparison

3.2.3 3-stages Stacked amplifier

In order to determine which is the impedance Z_{ds2} and Z_{ds3}, it is necessary to consider the following small signal circuit, where the CS stage has again been represented through its Norton equivalent circuit, while for the two CG stages, the same simplified model of fig. 3.19, which considers C_{GS} as the only parasitic element, was used.

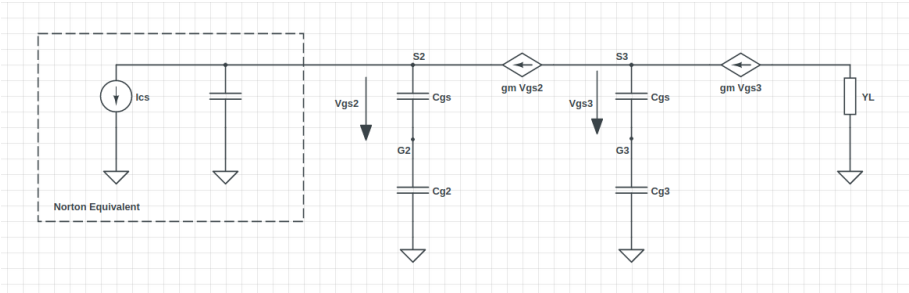


Figure 3.24: 3-stages Stacked Small signal signal simplified circuit for Y_in and Z_{DS} computation

Starting from the third stage:

$$v_{ds3} = -Z_L g_m v_{gs3} + v_{gs3} - \frac{i_{g3}}{j\omega C_{g3}}$$

and choosing to set, as before for A_2,

$$-v_{gs3}A_3 = -v_{gs3} + \frac{i_{g3}}{j\omega C_{g3}} \tag{3.5}$$

$$v_{ds3} = (A_3 - Z_L g_m) v_{gs3}$$

So the impedance will be:

$$Z_{DS3} = -\frac{A_3}{g_m} + Z_L \tag{3.6}$$

Now analysing the outer loop,

$$v_{gs2} - \frac{i_{g2}}{j\omega C_{g2}} - Z_L g_m v_{gs3} - v_{ds3} - v_{ds2} = 0$$

and with $-v_{gs2}A_2 = -v_{gs2} + \frac{i_{g2}}{j\omega C_{g2}}$ the previous equation becomes:

$$\begin{aligned} & A_2 v_{gs2} - Z_L g_m v_{gs3} - v_{ds3} - v_{ds2} = 0 \\ \Rightarrow \quad & v_{ds2} = A_2 v_{gs2} - Z_L g_m v_{gs3} - v_{gs3}(A_3 - Z_L g_m) \\ & = A_2 v_{gs2} - A_3 v_{gs3} \end{aligned}$$

By applying KCL to the S_3 node,

$$\begin{aligned} g_m v_{gs2} &= g_m v_{gs3} + v_{gs3} \times j\omega C_{gs} \\ v_{gs3} &= \frac{g_m v_{gs2}}{g_m + j\omega C_{gs}} \end{aligned}$$

So

$$v_{ds2} = A_2 v_{gs2} - A_3 \frac{g_m v_{gs2}}{g_m + j\omega C_{gs}}$$

And finally

$$\begin{aligned} Z_{DS2} &= -\frac{A_2}{g_m} + A_3 \frac{1}{g_m + j\omega C_{gs}} = \\ &= -\frac{A_2}{g_m} + A_3 \frac{g_m - j\omega C_{gs}}{g_m^2 + \omega^2 C_{gs}^2} \end{aligned} \tag{3.7}$$

From the input impedance equation, namely eq. 3.2 it is clear that the real part has to be the optimum resistance of the previous stage, so $A_2/g_m = R_{opt}$

$$A_2 = g_m R_{opt} \tag{3.8}$$

This choice imposes the load of this stage to be $2 \times R_{opt}$, so that the Z_{DS2} is equal to R_{opt}. Now the input impedance of the third stage, which is the load of CG2, is again eq. 3.2, leading to

$$A_3 = g_m R_{opt} \times 2 \tag{3.9}$$

in order to respect the previous request. The objective is to obtain $Z_{DS3} = R_{opt}$, so, from eq: 3.6, the load has to be $3 \times R_{opt}$.

A general rule can so be derived: the output impedance of the n_{th} stage (i.e. the input impedance of the $(n+1)_{th}$ stage) has to be $n \times R_{opt}^{CS}$. So each stage will have to show to its previous one a different impedance, depending on the actual position is the schematic. As an example the CS stage will have to "see" R_{opt}, while the first CG stage needs $2 \times R_{opt}$ and so on [10].

Ideal 3-stages Stacked amplifier performance

In order to set some simulations, the correct C_{g2} and C_{g3} have to be computed.
Again the optimum load is $15\,\Omega$, as well as $g_m = 0.5\,\mathrm{A/V}$ so

$$A_2 \;=\; 0.5\,\mathrm{A/V} \times 15\,\Omega \;=\; 7.5$$

while

$$A_3 \;=\; 0.5\,\mathrm{A/V} \times 15\,\Omega \times 2 \;=\; 15$$

Moreover $Z_{ds3} = R_{opt} = 15\,\Omega$ and $Z_{load} = 3 \times R_{opt} = 45\,\Omega$. From eq: 3.7,

$$Z_{DS2} \;=\; -\frac{7.5}{0.5\,\mathrm{A/V}} + 15\frac{0.5\,\mathrm{A/V} - j \times 2\pi \times 26\,\mathrm{GHz} \times 0.7\,\mathrm{pF}}{(0.5\,\mathrm{A/V})^2 + (2\pi \times 26\,\mathrm{GHz} \times 0.7\,\mathrm{pF})^2} \;=\; (13.9 + j5.8)\,\Omega$$

Since no variation affect the second stage (A is now named A_2, but has the same value), the second CG Gate capacitance remains 0.107 pF; the input impedance is unchanged as well ($(0.067 + j0.013)\,\mathrm{S}$). The impedance $Z_{in2} \sim 15\,\Omega$, is the optimum load, required by the CS stage; this is due to a proper choice of C_{g2}.

Z_{DS3} is computed by applying eq: 3.4:

$$Z_{DS3} \;=\; R_{load} + \frac{A_3}{g_m} \;=\; 45\,\Omega + \frac{15}{0.5\,\mathrm{A/V}} \;\sim\; 15\,\Omega$$

The input impedance of the third stage is computed through eq: 3.2:

$$Y_{in3} \;=\; \frac{g_m}{A_3} + j\omega\frac{C_{gs}}{A_3} \;=\; \frac{0.5\,\mathrm{A/V}}{15} + j \times 2\pi \times 26\,\mathrm{GHz}\frac{0.7\,\mathrm{pF}}{15} \;=\; (0.033 + j0.006)\,\mathrm{S}$$

In terms of impedance $Z_{in3} \sim 29\,\Omega$, showing that a proper choice of C_{g3} allows for a variation in the real part of the input impedance. This value is close to the ideal $30\,\Omega$ optimum load, required at the Drain of the first CG stage.

For the computation of C_{g3}, the eq: 3.5 is inverted as done in the previous section for the second stage:

$$C_{g3} \;=\; \frac{C_{GS}}{g_m R_{opt} \times 2 - 1} \;=\; 51.3\,\mathrm{fF}$$

The following table summarizes a 3-stage stacked amplifier main quantities:

A_2	Z_{DS2}	Y_{in2}	A_3	Z_{DS3}	Y_{in3}
7.5	$(13.9 + j5.8)\,\Omega$	$(0.067 + 0.013j)\,\mathrm{S}$	15	$15\,\Omega$	$(0.033 + j0.006)\,\mathrm{S}$

Table 3.4: 3-stage stacked amplifier input admittance and output impedance

Both the output impedances show a real part close to $15\,\Omega$, which is the optimum resistance, computed in the previous section.

As for simulations, the obtained dynamic load lines are reported in the first plot in fig: 3.25; the green one, associated to the last stage, results to be a straight line, due to the used real load. Instead the other DLLs are elliptical because of the uncompensated reactive nature of the following stages' parasitics.
The other plots show voltage and currents in time: as before only V_{load} and I_{load} are in-phase, due to the resistive load. The other three are shifted, meaning a complex load is required for the stages to be properly matched.

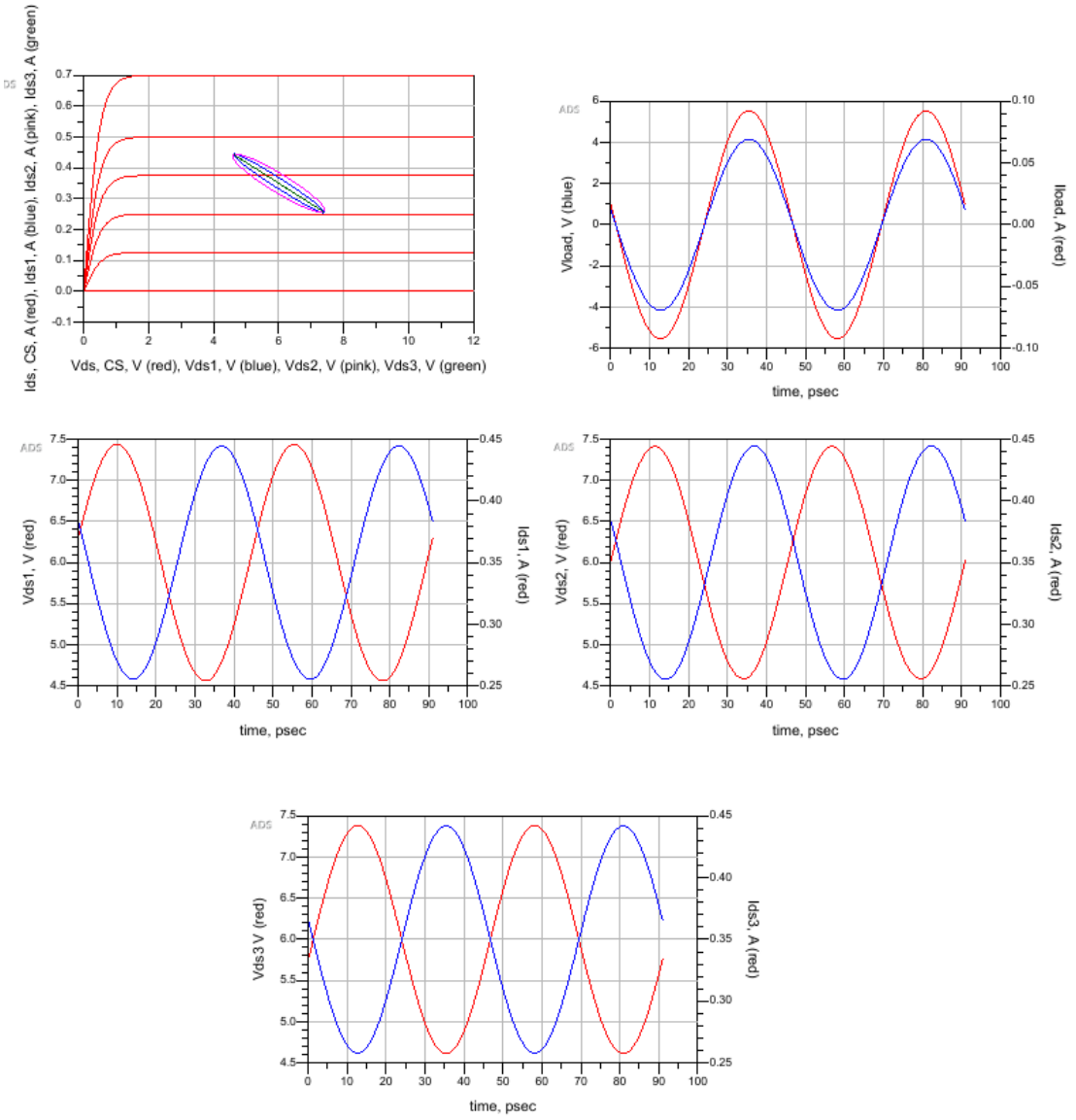


Figure 3.25: Stacked amplifier DLLs for CS, CG1 and CG2 stages (top left); in-phase I_{load} and V_{load} (top right); de-phased I_{ds1} and V_{ds1} (bottom left); de-phased I_{ds2} and V_{ds2} (bottom right); de-phased I_{ds3} and V_{ds3} (bottom)

Fig: 3.26 shows a 3-stages Stacked amplifier performance. A comparison with the CS stage will be performed in the following sections.

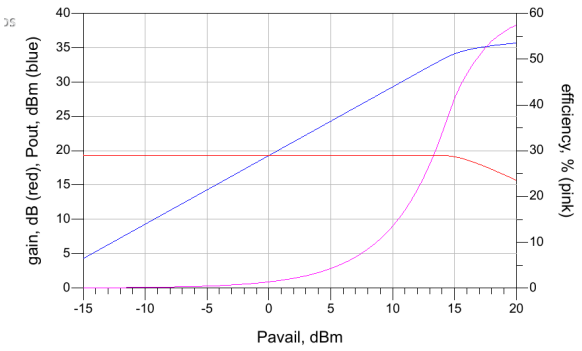


Figure 3.26: Stacked amplifier performance: P_{OUT}, Gain and DE

The input admittances and output impedances are calculated through simulations as before in fig: 3.27 and fig: 3.28:

Eqn YinCG2=-Ids.i/Vs2

Eqn Zin2=1/YinCG2

YinCG2[indCg,indP,1]	Zin2[indCg,indP,1]
0.067 + j0.013	14.449 - j2.796

Eqn A2=1+CGS[0,0]/Cg2[indCg]

Eqn Yth2= 0.5/A2+j*2*pi*26e9*CGS[0,0]/A2

Eqn Zth2=1/Yth2

A2	Yth2	Zth2
7.495	0.067 + j0.013	14.449 - j2.796

Eqn Zds2=-Vds2/Ids2.i

Eqn Zdsth2=Rload[0,0]-A2/0.5*2

Zds2[indCg,indP,1]	Zdsth2	Rload[0,0]
13.243 - j5.464	15.021	45.000

Figure 3.27: Stacked amplifier impedance (2^{nd} stage)

Eqn YinCG3=-Ids2.i/Vs3

Eqn Zin3=1/YinCG3

YinCG3[indCg,indP,1]	Zin3[indCg,indP,1]
0.033 + j0.006	28.977 - j5.608

Eqn A3=(1+CGS[0,0]/Cg3[indCg])

Eqn Yth3=0.5/A3+j*2*pi*26e9*CGS[0,0]/A3

Eqn Zth3=1/Yth3

A3	Yth3	Zth3
15.031	0.033 + j0.006	28.977 - j5.608

Eqn Zds3=-Vds3/Ids3.i

Eqn Zdsth3=Rload[0,0]-A3/0.5*3

Zds3[indCg,indP,1]	Zdsth3	Rload[0,0]
14.938 - j8.581E-15	-45.187	45.000

Figure 3.28: Stacked amplifier impedance (3^{rd} stage)

Theoretical results are confirmed by simulations.

As mentioned before, in fig: 3.29 gain and output power of a 3-stage, a 2-stage stacked and a CS stage are compared:

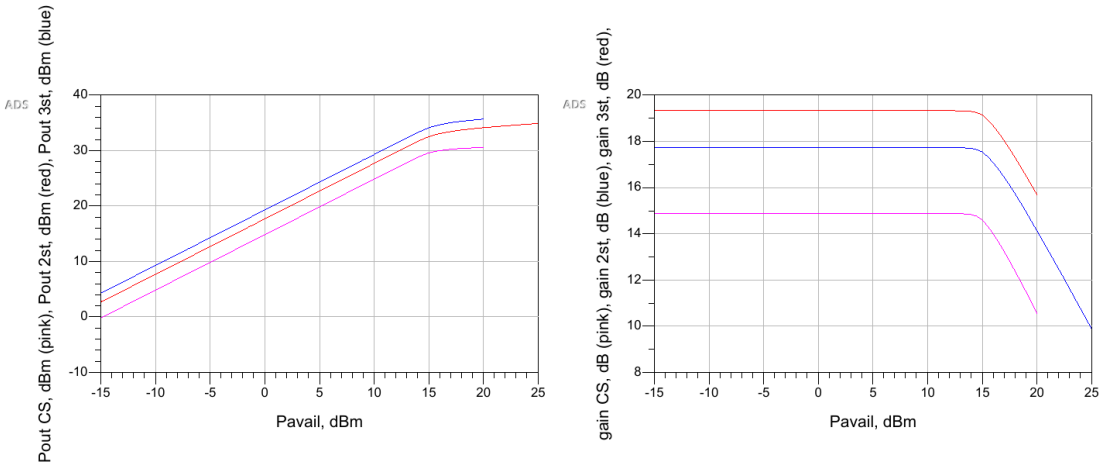


Figure 3.29: 2-stages and 3-stages Stacked amplifier performance comparison: P_{OUT}(left) and Gain (right)

The plot on the right shows that a CS amplifier gain is about 15 dB. From theory it

is known that a 2-stage stacked amplifier's gain is twice a single stage, meaning an ideal increase of 3 dB, which is confirmed by the cited plot; the blue curve, in fact, is just below 18 dB. The third stage causes a further increase of 1.8 dB, confirmed by red curve at ~ 19.5 dB.
A similar reasoning can be applied to output power, represented in the first graph.

3.3 Cascode and Stacked comparison

In this section simulations of a cascode and a 2-stages stacked topologies will be compared. As mentioned when introducing the stacked amplifier, the main difference from a circuital point of view is the insertion of the Gate capacitance in CG stages. The common Gate is so turned into a pseudo-CG stage with some variations on the input impedance, as noticed in section: 3.2.2:

$$\begin{aligned} Y_{in,cascode} &= g_m + j\omega C_{GS} \\ Y_{in,stacked} &= \frac{g_m}{A} + j\omega \frac{C_{gs}}{A} \end{aligned} \tag{3.10}$$

Fig: 3.30 compares two of the main figures of merit, namely gain and output power. The former is 14.7 dB, equal to a CS in the case of a cascode configuration; as for the stacked, it is theoretically twice the gain of a CS, in natural units (or 3 dB larger). From the graph it is about 17.7 dB.
From table: 3.3 the same reasoning can be applied to the output power of the stacked amplifier and resulting in ~ 34 dBm (when reaching saturation $P_{in} \sim 15$ dBm).

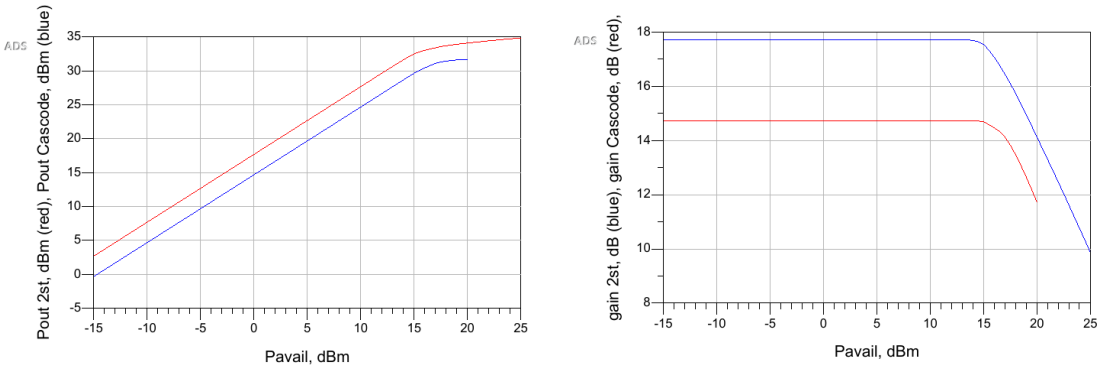


Figure 3.30: Stacked amplifier and Cascode performance comparison: P_{OUT}(left) and Gain (right)

Chapter 4

Real Device - GaN

In this chapter and in the following one, FETs based on two different commercial MMIC technologies are compared in terms of performance, stability, matching network and internal parameters. In this chapter a GaN HEMT technology will be considered, while the next chapters will deal with a GaAs HEMT one.

4.1 Device evaluation

It is now taken into account a real device:commercial Depletion Mode GaN HEMT Technology. In particular a $6 \times 100\,\mu$m device is used The chosen design frequency is 26 GHz. According to the foundry non-linear model, the device is characterized by a -2 V threshold voltage, while the breakdown voltage is 120 V; the suggested Drain voltage is 20V and the corresponding I_{DSS} is 0.423 A. Moreover the declared output power the device will be able to provide is 1.8 W(32 dBm).

The following figure shows the DC input and output characteristics of the device, in which it is clear that $V_{TH} = -2$ V and $I_{DSS} = 0.391$ A, as expected.

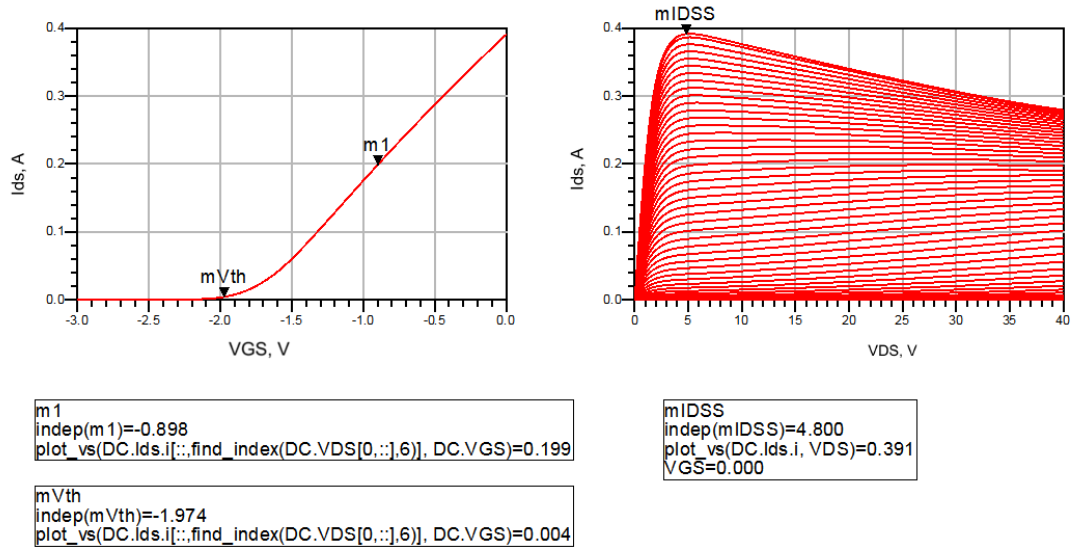


Figure 4.1: CS stage DC characteristics: trans-characteristics (left) and output characteristics (right)

Moreover the knee voltage is about 3 V. As a consequence the optimum intrinsic load will be

$$R_{OPT} = 2\frac{V_{DD} - V_{knee}}{I_{DSS}} = 64.8\,\Omega$$

In order to use the FET as a class A amplifier, it is necessary to properly choose the Gate voltage, so that the corresponding current is $1/2I_{DSS}$. In this case, from fig: 4.1, $V_{GS} = -0.9\,\mathrm{V}$.
As for the transconductance, it can be computed as $\frac{dI_{DSS}}{dV_{GS}}$ and, as reported in the following plot (blue curve), it is abut 0.22 A/V for the class A:

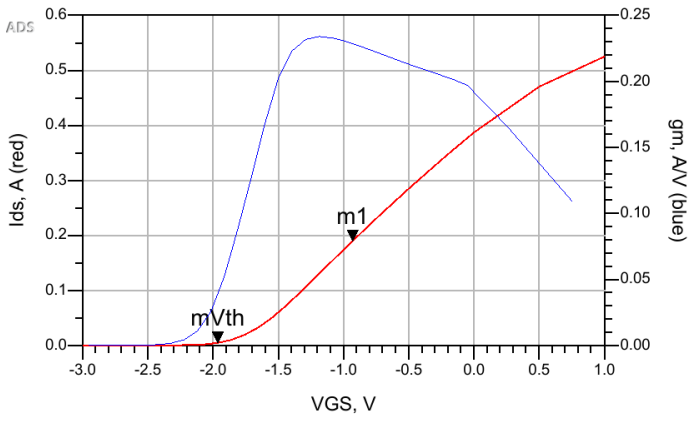


Figure 4.2: Trans-characteristics and transconductance for a CS stage

An S-parameter simulation is performed; taking a look at S12 it is possible to see that it is quite 0 for the whole frequency range and so the device can be said to be unilateral.

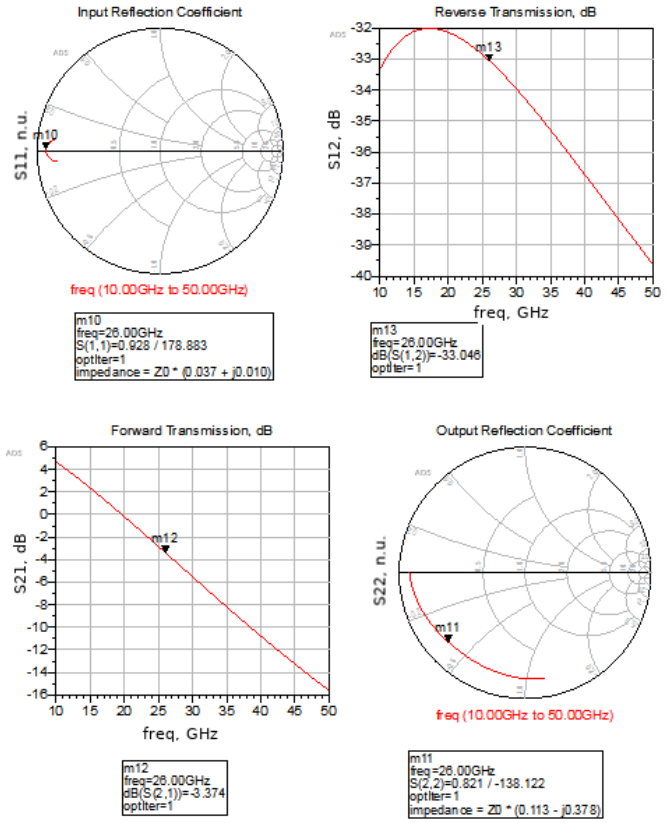


Figure 4.3: S-parameter simulation CS stage

Moreover it is verified which is the stability range for both the input and output impedances; it will be necessary later on, when performing the load-pull simulation.

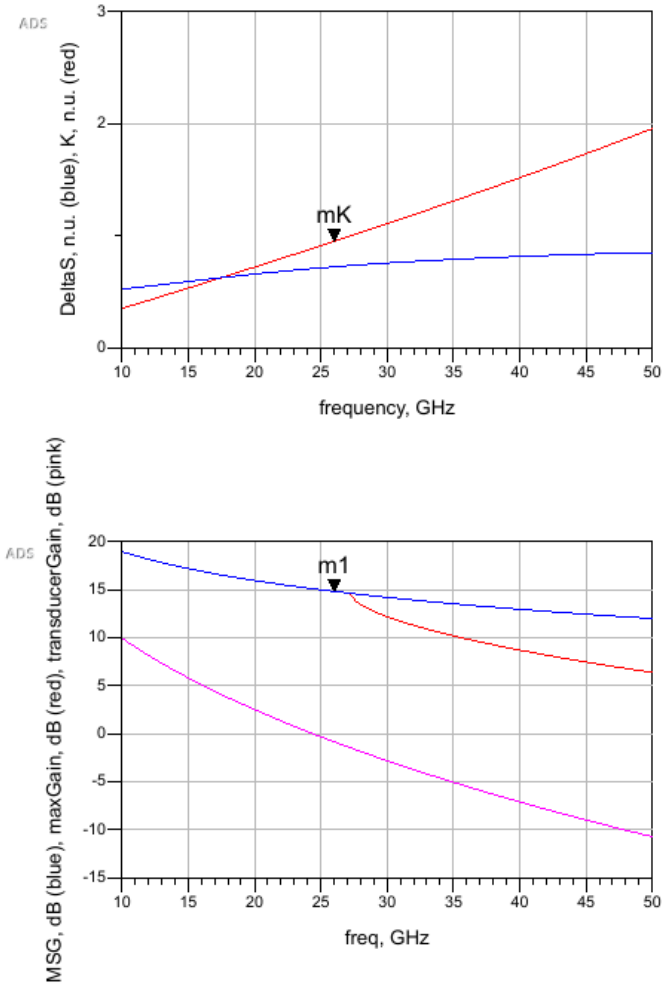


Figure 4.4: Stability parameters: K and ΔS (top) and Gain (bottom)

From the first plot of fig: 4.4, it is clear that the device is potentially unstable at the working frequency, since the double-parameter stability criterion[7], involving Rollet coefficient, is not respected, given $K \leqslant 1$ @ 26 GHz.
As a consequence the Maximum Available Gain (MAG) is still not defined.
As for what concerns stability circles, from fig: 4.5, only a small portion of the Smith Chart is unavailable. Given the potential instability, it will be necessary to avoid to choose a load and an input impedance inside that region.

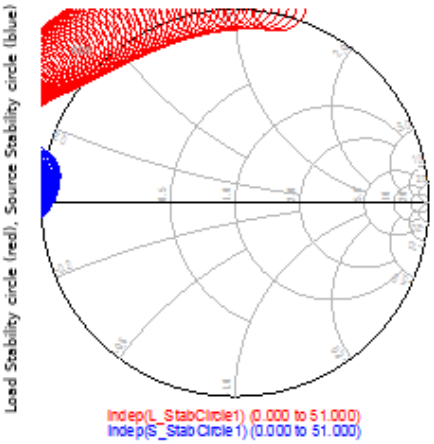


Figure 4.5: Stability circles

4.2 CS Stabilization

Stabilization is not only important at the working frequency but also out of the band. In general the device has to be stabilized at low frequency too, namely from DC to the design bandwidth, in order to prevent out-of-band oscillations, since there is no control on the loads; in this condition, the FET has an high gain and is potentially more unstable.
In order to stabilize the CS, it is necessary to insert a dissipative network containing a resistance. Some other reactive elements allow for series resistor bypass so that gain is only reduced below the band of interest. On the other hand, at the working frequency, MAG should be as close as possible to the original one, in the stable range, since a loss in gain is undesirable.
Overall the stabilization circuit is reported in fig: 4.6, where the resistive element is decoupled by an L-C resonator; moreover the DC bias at the Gate is provided through an L-R network.

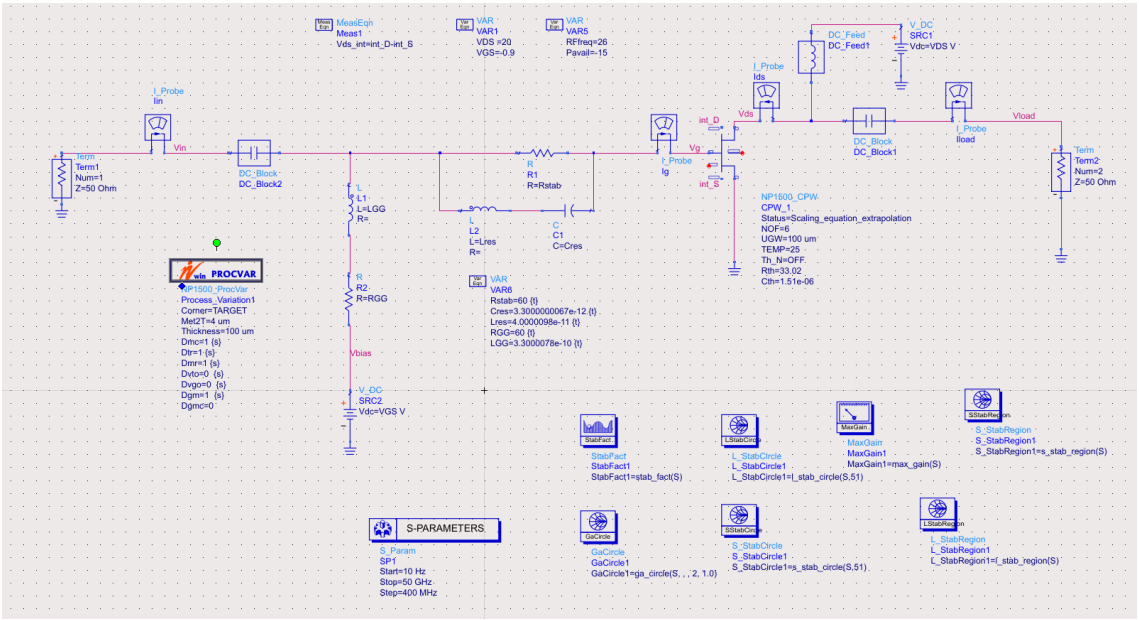


Figure 4.6: Stabilization circuit for a CS stage

All of these parameters are manually swept in order to move stability circles out from the Smith Chart and to maximize the MAG.
In general a complete stabilization (from DC to 26 GHz) leads to an high degradation of the gain, especially for rising frequencies; the possibility to accept potential instability in band allows for an increase in gain.
A good compromise can be obtained with the parameters reported in the following table:

R_{stab}	C_{res}	L_{res}	R_{GG}	L_{GG}
35 Ω	650 fF	45 pH	100 Ω	13 nH

Table 4.1: GaN Stabilization network components

With these numerical values, Rollet factor is always larger than 1 as well as $\Delta S \leq 1$; looking at the Smith Chart, the stability region is outside from the circles and the whole chart can be used.
As for gain, the penalty is about 0.6 dB @ 26 GHz, as shown in fig: 4.7. Then it is even lower for higher frequencies; however gain reduction is stronger at lower frequencies, enhancing stability.

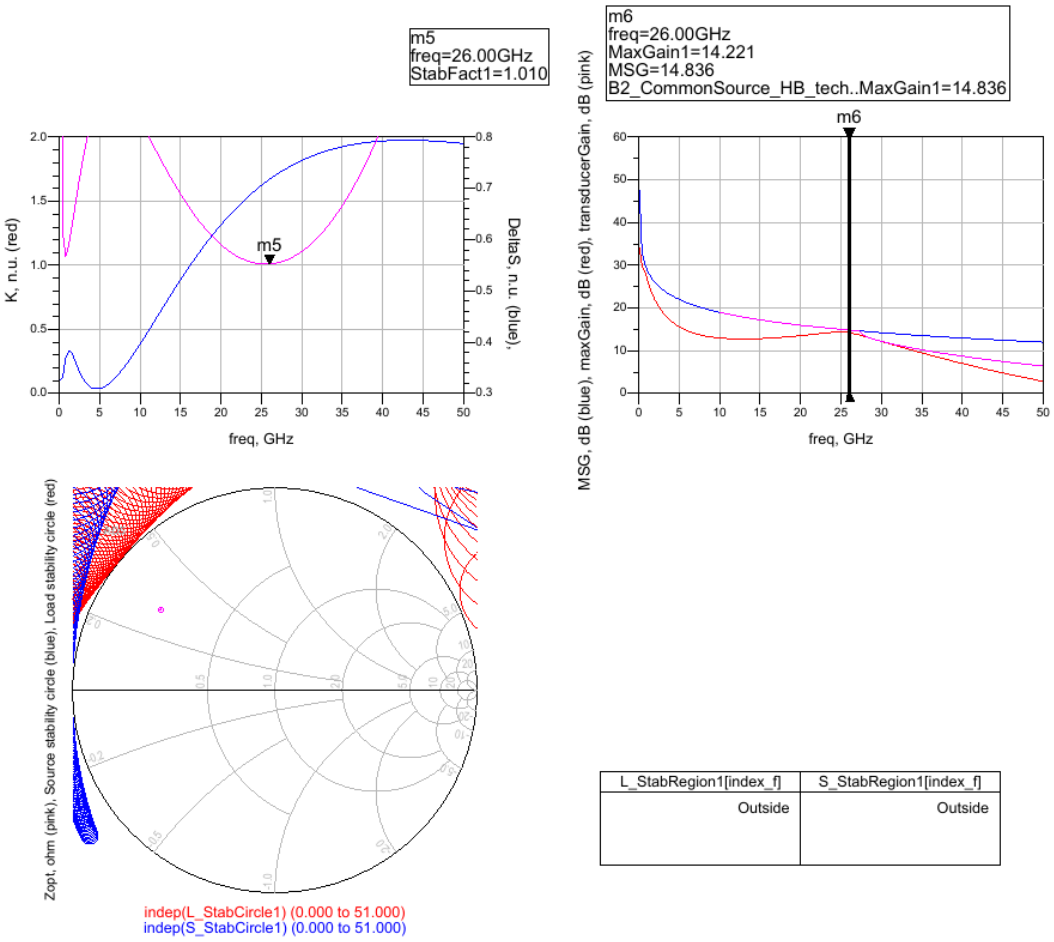


Figure 4.7: Stabilized CS stability performance: K and ΔS (top left) and Gain (top right); stability circles (bottom)

4.3 Class A

In the following a load-pull analysis is performed.
In order to do that all the possible loads (in a given range) are tested by sweeping the real and imaginary part and the 1 dB compression point for the gain is identified. In that point, the variable (P_{OUT}, $Gain$, DE and PAE) is computed and the contour is evaluated.
In particular:

- $P_{OUT}^{max} = 31.66\,\text{dBm}$
- $PAE^{max} = 32.33\%$
- $Gain^{max} = 13.15\,\text{dB}$
- $\eta^{max} = 35.15\%$

As shown in fig: 4.8, the PAE and the DE are maximized by the same load, while it is quite different in the output power case.
In particular, $Z_{OPT}^{PAE} = Z_{OPT}^{DE} = 7.5 + j12.5\,\Omega$, while $Z_{OPT}^{Gain} = 2.15 + j16.9\,\Omega$

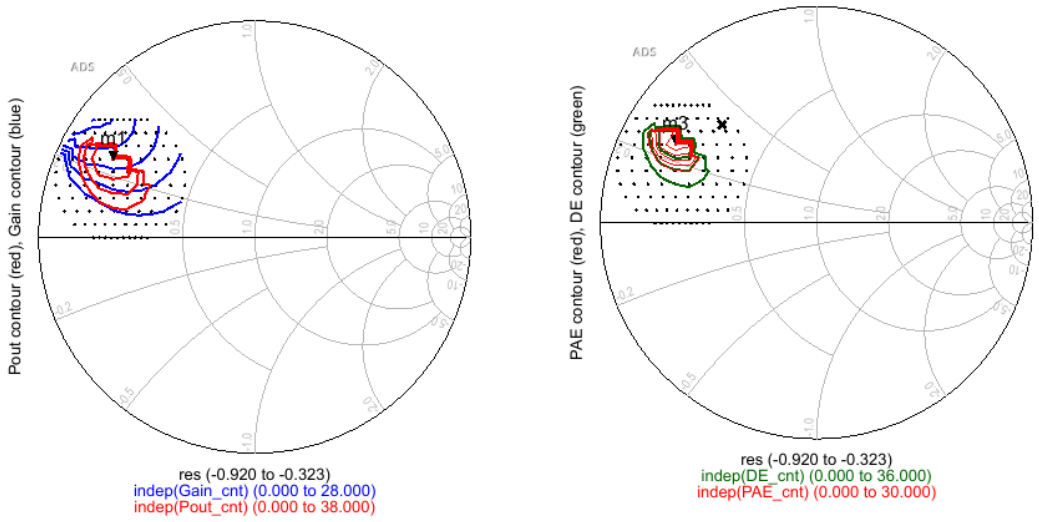


Figure 4.8: Load Pull simulation results for Gain, P_{OUT}, DE and PAE

As for P_{OUT} maximization, after a manual tuning of the load, it turns out that $Z_{OPT}^{intrinsic} = 64.175\,\Omega$ and $Z_{OPT}^{extrinsic} = (10 + j15)\,\Omega$ ($Y_{OPT,B}^{extrinsic} = (0.027 - j0.046)\,\mathrm{S}$). The previously computed values are referred to a 1 dB compression condition.

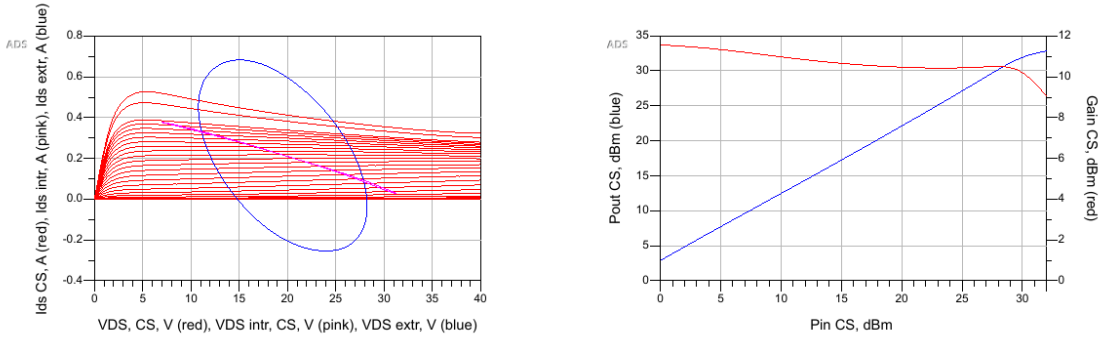


Figure 4.9: Common Source Class A output characteristics with extrinsic and intrinsic DLLs after CW optimization (left); P_{OUT} and Gain (right)

In this case the intrinsic dynamic load line (pink curve in fig: 4.9) is turned into a single line, allowing the maximum power transport, which reaches 32 dB, as expected. On the contrary, the extrinsic load line is expanded into an ellipse, due to reactive effects of the load.

The following results are obtained from the harmonic balance analysis, by using the previously computed load (maximized P_{OUT}):

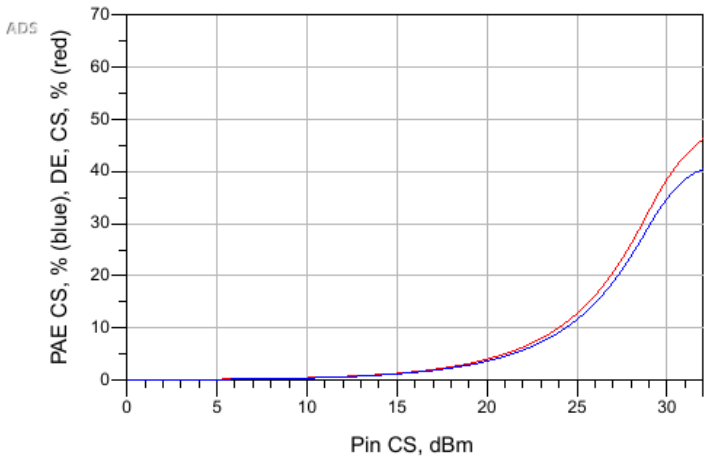


Figure 4.10: Common Source Class A performance after CW optimization: PAE and DE

The main parameters to be observed at 30 dBm, which is the 1 dB compression point, are:

- $P_{OUT} = 31.9\,\text{dBm}$
- $G_{AV} \sim 10\,\text{dB}$
- DE = 38%
- PAE $\sim$ 34 %

Which are coherent with the previously computed ones.
It is also necessary to verify that conduction does not take place when negative voltages are applied to the Gate terminal. Fig: 4.11 shows that forward Gate conduction is only experienced at $V_{GS} \geq 1.4\,\text{V}$, which is much larger than the used ones.

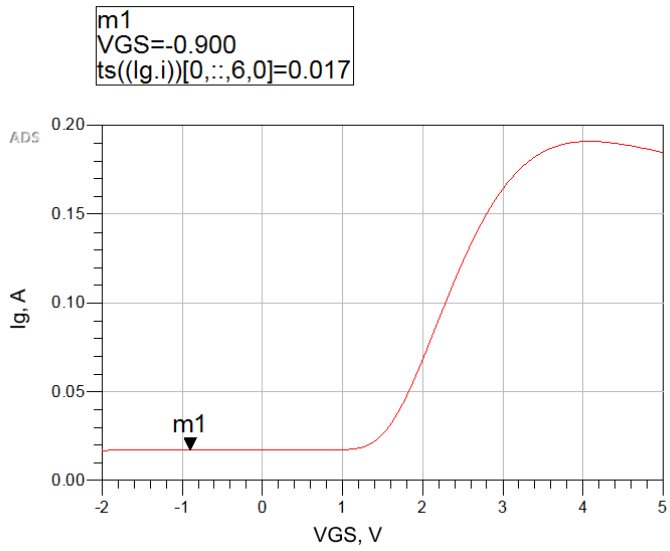


Figure 4.11: Gate current

Finally it is possible to analyze voltages and currents in time:

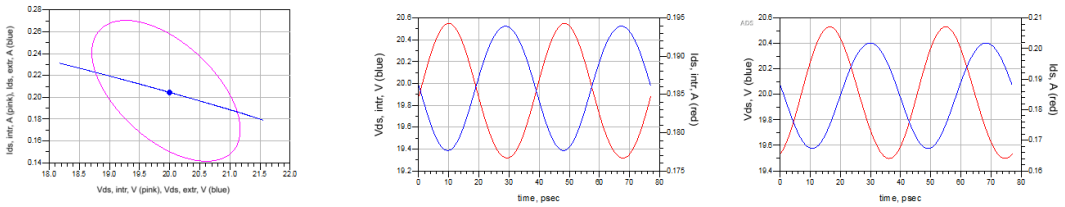


Figure 4.12: Intrinsic and extrinsic dynamic load lines for a CS (left); Intrinsic (center) and extrinsic (right) V_{DS} and I_{DS}

As expected the intrinsic waveforms are in phase each other, implying an ohmic load. As for the extrinsic ones and so as for the load, voltage and current are shifted. The same information is represented by the dynamic load-line.
Fig: 4.12 takes into account an input power of 10 dBm, so no distortion takes place.

4.4 Class AB

As for a class AB amplifier, the Gate voltage will have to be in the $-0.9\,\text{V}, -2\,\text{V}$ range; in particular it was chosen $V_{GS} = -1.1\,\text{V}$.

Once tuned for P_{OUT} maximization, the following characteristic holds:

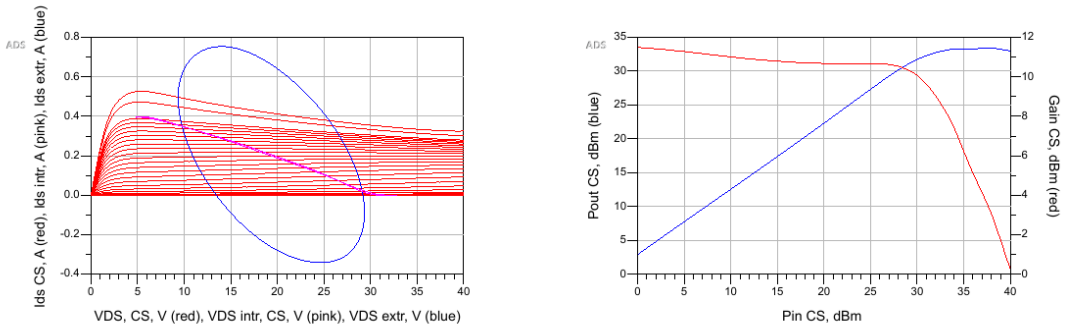


Figure 4.13: Common Source Class AB output characteristics with extrinsic and intrinsic DLLs after CW optimization (left); P_{OUT} and Gain (right)

In this case the optimum conductance (G_0) should be a bit larger than a class A's one [7]; in particular $Z_{OPT}^{intrinsic} = (64.3 + j0.02)\,\Omega$ and $Z_{OPT}^{extrinsic} = (10 + j15.3)\,\Omega$ ($Y_{OPT,B}^{extrinsic} = (0.03 - j0.046)\,\mathrm{S}$).
According to theory, by reducing the circulation angle and so moving from a Class A to a Class B, Gain should decrease when $P_{in} \sim 0$, meaning small signal condition; in particular in fig: 4.13 it is about 13 dB. Since the variation in the circulation angle is not marked with respect to 2π, also gain degradation will not be so significant. Finally as for the harmonic balance simulation, both PAE and DE increase with respect to the previously computed values (at 1 dB compression).

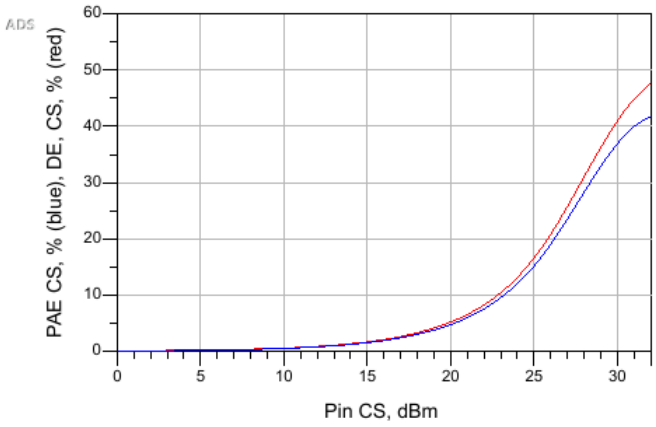


Figure 4.14: Common Source Class AB performance after CW optimization: PAE and DE

4.5 Class B

As for a class B amplifier, the Gate voltage will have to be $-2\,\mathrm{V}$
Once tuned for P_{OUT} maximization, the following characteristic holds:

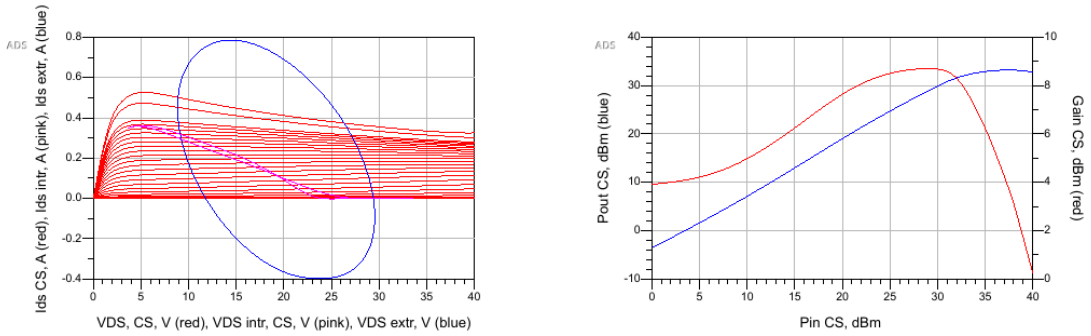


Figure 4.15: Common Source Class B output characteristics with extrinsic and intrinsic DLLs after CW optimization (left); P_{OUT} and Gain (right)

In this case $Z_{OPT}^{intrinsic} = (74.3 + j3.2)\,\Omega$ and $Z_{OPT}^{extrinsic} = (8.2 + j15.1)\,\Omega$; what is worth to be noticed is that G_0 is the same as a class A amplifier ($Y_{OPT,B}^{extrinsic} = (0.027 - j0.051)\,\mathrm{S}$), as known from theory [7].
Moreover Gain for a class B amplifier is expected to be 6 dB lower than a class A, in small signal condition; the plot on the right (fig: 4.15) shows a Gain of 4 dB with respect to the 10 dB of a Class A. On the other hand at 1 dB compression, gain is 9 dB.
Finally as for the harmonic balance simulation show an increase in both PAE and DE with respect to Class A and AB.

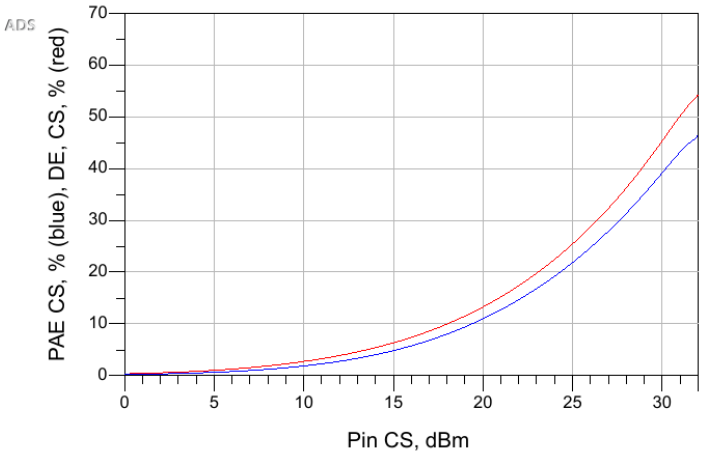


Figure 4.16: Common Source Class B performance after CW optimization: PAE and DE

4.6 Intrinsic and Extrinsic parameters evaluation

In order to compute Intrinsic and Extrinsic parameters, it is necessary to perform a de-embedding technique: first of all FET's S-parameters are evaluated in Hot and Cold conditions. As for the latter $V_{DS} = 0$ and $V_{GS} = 3\,\mathrm{V}$.
On the other hand the Hot FET situation corresponds to the standard working condition. When taking into account the Cold FET, it is possible to directly extract the extrinsic parameters, such as:

L_G	L_D	L_S	R_G	R_D	R_S
322.9 nH	500.8 nH	~ 0	1.98 Ω	0.619 Ω	0.524 Ω

Table 4.2: GaN Extrinsic parameters

By applying some equations[7] it is then possible to derive the intrinsic parameters, too:

C_{GD}	C_{DS}	C_{GS}	R_I	R_{DS}
0.389 fF	17.45 pF	1.34 pF	0.584 Ω	$\sim 20k\,\Omega$

Table 4.3: GaN Intrinsic parameters

As it is possible to see from fig: 4.17 the previously computed parameters are quite stable in frequency.

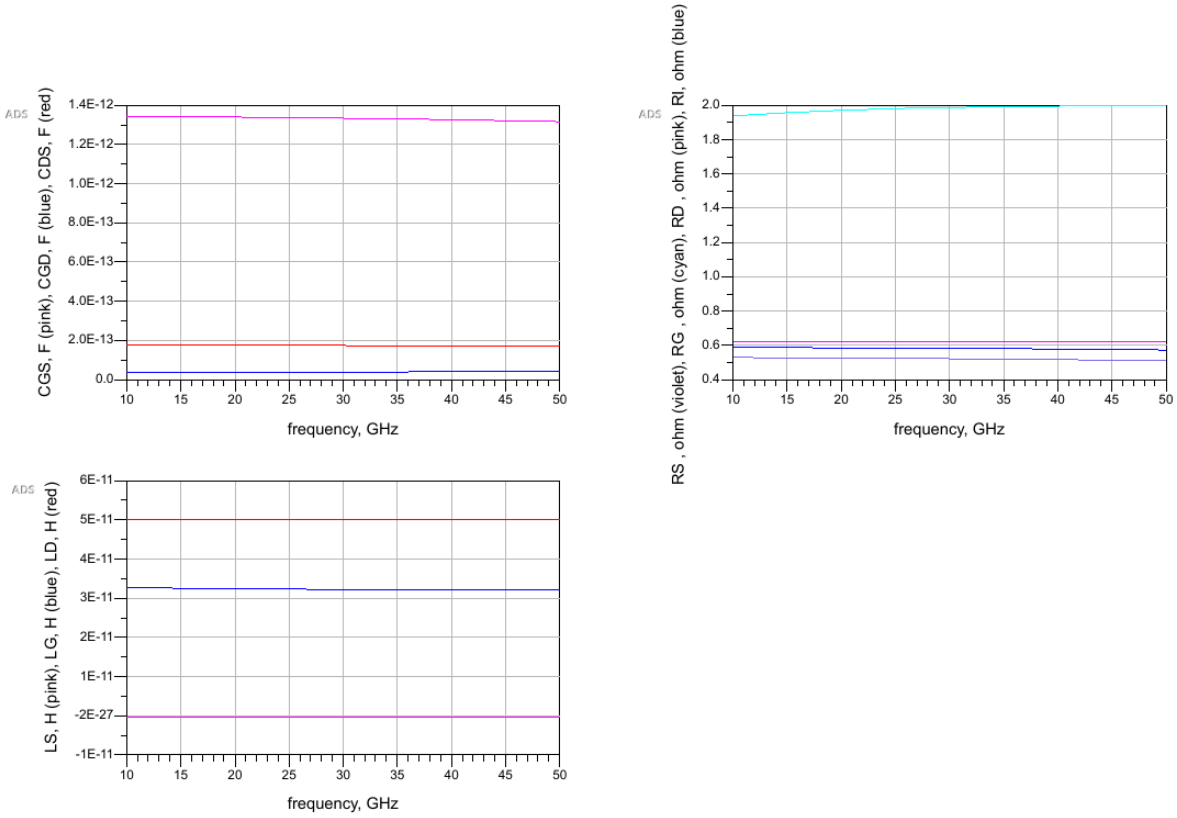


Figure 4.17: Intrinsic and extrinsic parameters in frequency

The corresponding equivalent circuit is represented in fig: 4.18, which is the model proposed by Curtice. In this case two parameters are still missing: the transconductance and the time delay for the current controlled generator.
These can be derived from de-embedding equations resulting into: $g_m = 0.214\,\mathrm{A/V}$ and $\tau = 1.745\,\mathrm{ps}$.

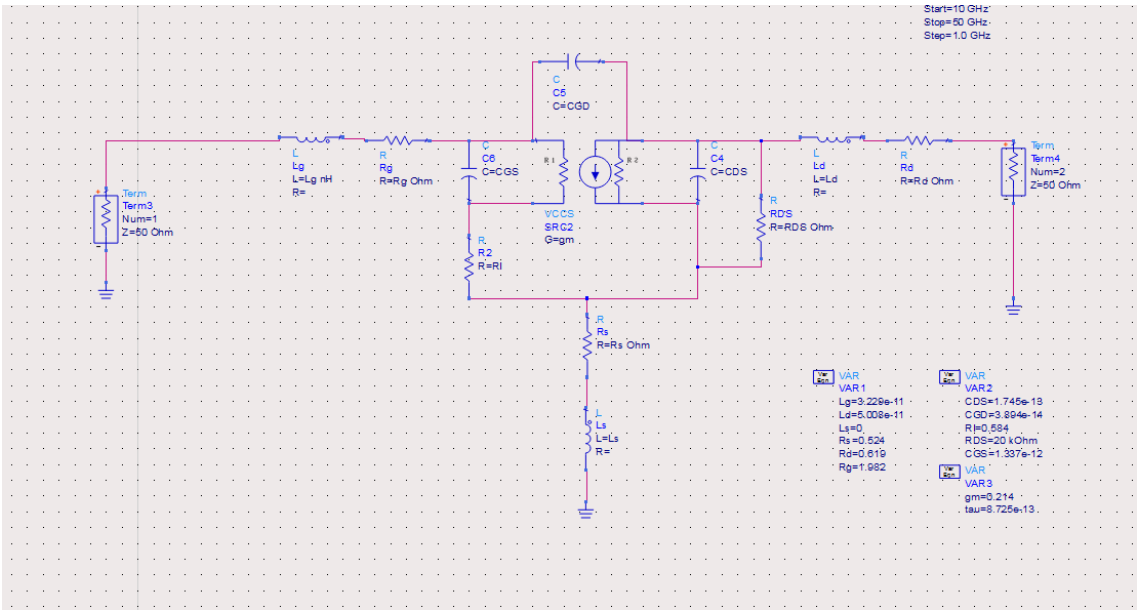


Figure 4.18: Curtice model exploiting the extracted parameters

In order to verify if the extracted parameters are correct, a negative impedance contribution is added in series and in parallel, in order to remove extrinsic and intrinsic contributions, respectively. The actual value corresponds to the previously computed ones, as reported in tab: 4.2 and tab: 4.3, but with a negative sign.
In this way the voltage which is measured before the negative impedance will be the intrinsic one: in fig: 4.19 the highlighted nodes correspond to the intrinsic ones.
However it is necessary to introduce an equal and positive contribution too, so that the overall device from outside, is the same as the real FET.

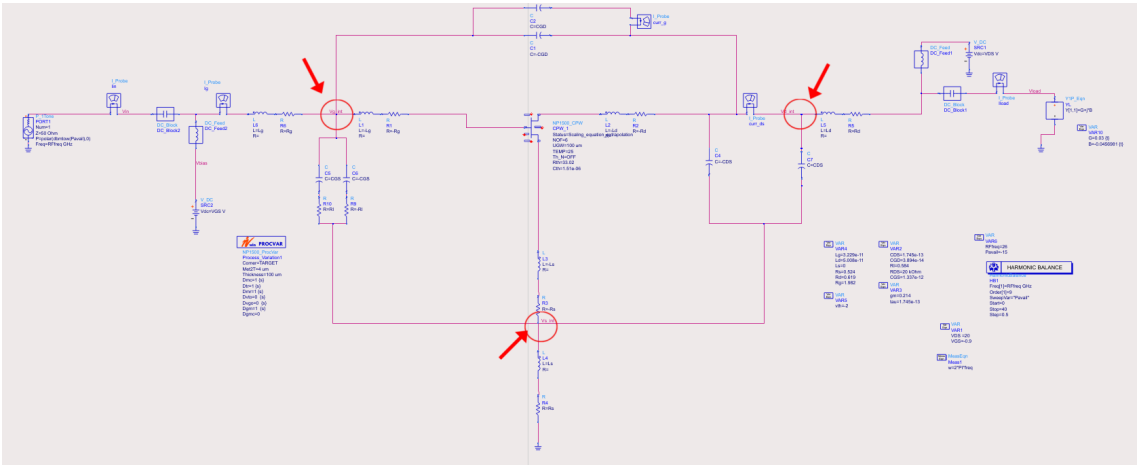


Figure 4.19: Parameter removal circuit with intrinsic nodes, highlighted

The intrinsic current I_{DS}^{intr} can be computed by summing two contributions: the first one is the current measured after C_{DG} cancellation (curr_g in the schematic), while the second one is measured after C_{DS} (curr_ds in the schematic). The resulting current is only due to the controlled generator, and so it corresponds to the intrinsic one.

The Drain-Source resistance can not be removed since is intrinsically connected to I_{DS}, defining how it changes depending on v_{ds}, being the current a function of both V_{ds} and V_{gs}. R_{DS} is so the only element which will not be removed.
The intrinsic I_{DS} can be represented by its Norton's equivalent generator (controlled current generator) and the parallel R_{DS}.

The idea is to define the dynamic load line at the intrinsic, so that it should be as close as possible to a straight line, as reported in fig: 4.9, given the optimum load and the correct input power level.
In fig: 4.20, the load line defined at the induced intrinsic terminals is compared to CS' one, measured at the real intrinsic terminals, available in the foundry model.
The result is quite similar even if a more elliptical behavior is shown by the "artificial" load line. Such a shape is a consequence of a stronger reactive effect.
Taking a look at the single currents and voltages (fig: 4.21), the shape is basically the same at the real and fictional intrinsic nodes as for what concerns voltages. On the other hand a more significant variation can be observed in the current: while the real current shows a pinch-off, not allowing negative currents, the artificial one has a small negative peak.
These small variations could be due to a not perfect, even if acceptable, parameter extraction.

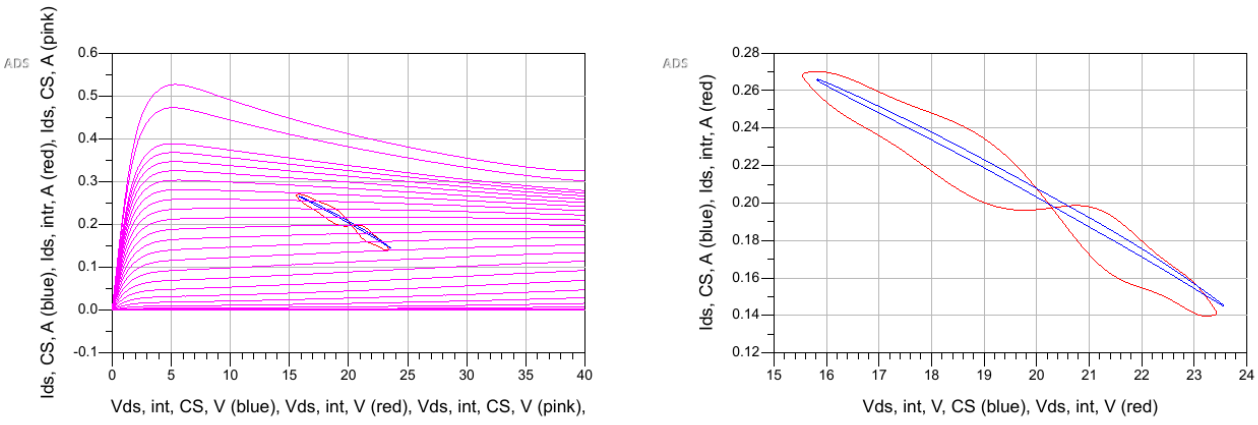


Figure 4.20: DLL comparison: real intrinsic (blue curve) and the one resulting from parameters removal (red curve)

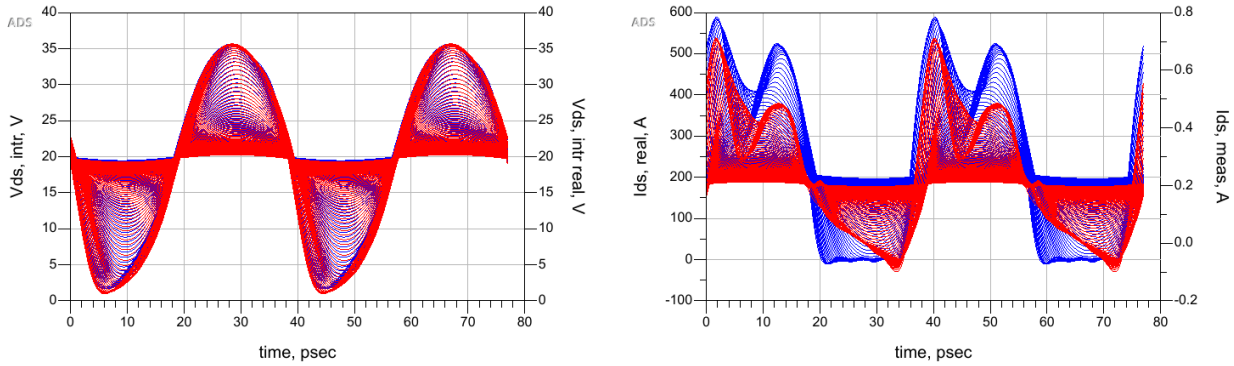


Figure 4.21: Real intrinsic currents and voltages compared to the extracted from parameters removal

4.7 Equivalent model

Given the relationship between the optimal intrinsic impedance (resistance) and the optimal extrinsic impedance computed in section: 4.3, it is possible to derive an equivalent LC circuit which performs the same impedance conversion, that is indirectly done by the FET.

In order to derive such a model, S-parameter simulations are performed: firstly the correct intrinsic load is inserted at the input and the output reflection coefficient Γ_{OUT} is measured (fig: 4.22). By sweeping L and C values, the coefficient is changed and when it is equal to the one associated to the wanted extrinsic impedance, then the goal is reached. In particular $\Gamma_{OUT} = conj(\Gamma_{Z_{OPT}})$, so since $Z_{OPT} = (10 + j15.3)\,\Omega$, $\Gamma_{Z_{OPT}} = \frac{Z_{OPT}-Z_0}{Z_{OPT}+Z_0} = 0.69\angle 144.76°$.

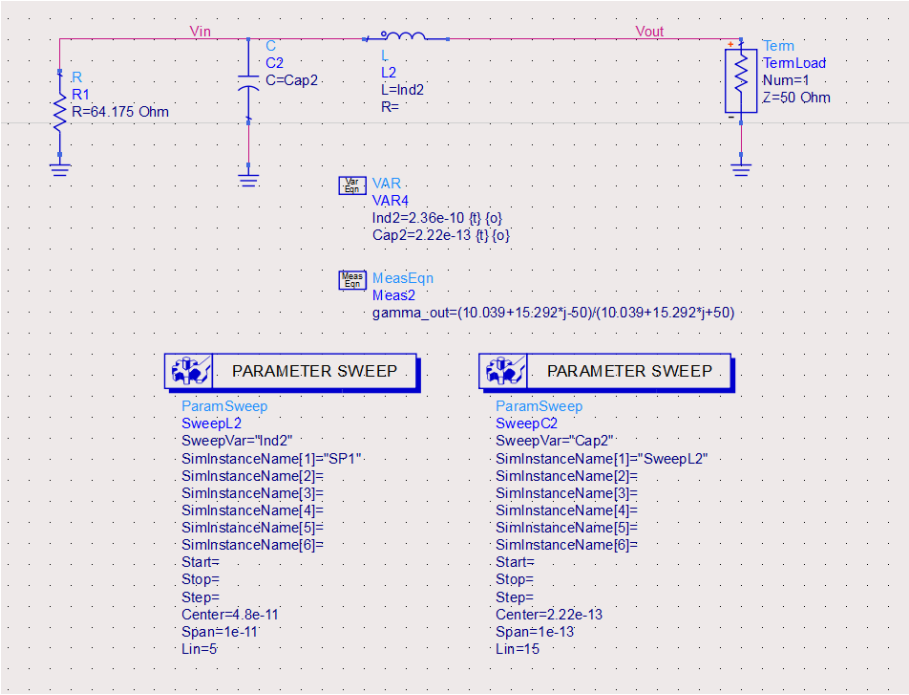


Figure 4.22: Equivalent model side 1 - intrinsic resistance is transformed into the corresponding extrinsic complex impedance

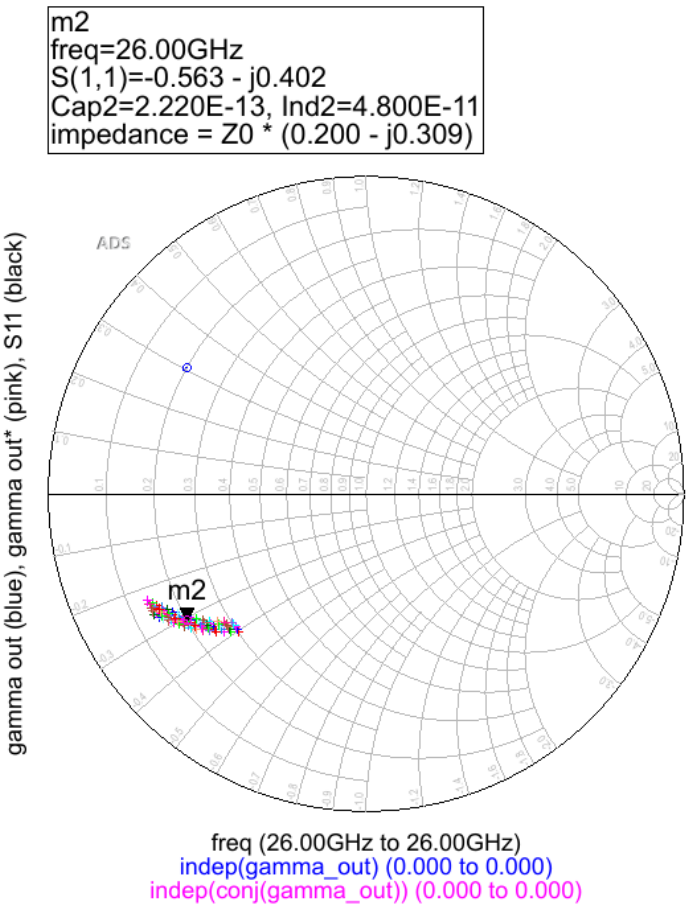


Figure 4.23: Smith Chart side 1 - intrinsic resistance is transformed into the corresponding extrinsic complex impedance

The opposite procedure is performed for the derivation of the input reflection coefficient: the extrinsic complex load, is inserted and Γ_{IN} is measured (fig: 4.24). In this case, defined as $\Gamma_{IN} = \frac{R_{OPT}-Z_0}{R_{OPT}+Z_0} = 0.12$ is the objective to be achieved through a tuning of the LC 2-port. Being Γ_{IN} a real number, its conjugated value is Γ_{IN} itself.
By changing L and C values, the measured Γ_{IN} is moved in the Smith Chart, until it reaches the wanted value, namely 0.12.

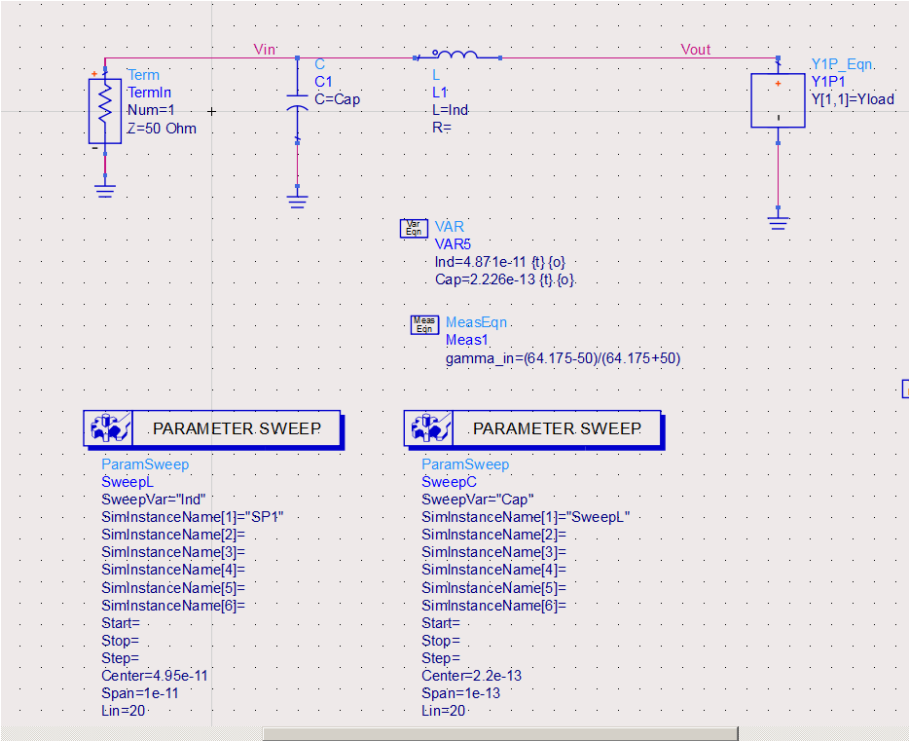


Figure 4.24: Equivalent model side 2 - extrinsic impedance is transformed into the corresponding intrinsic resistance

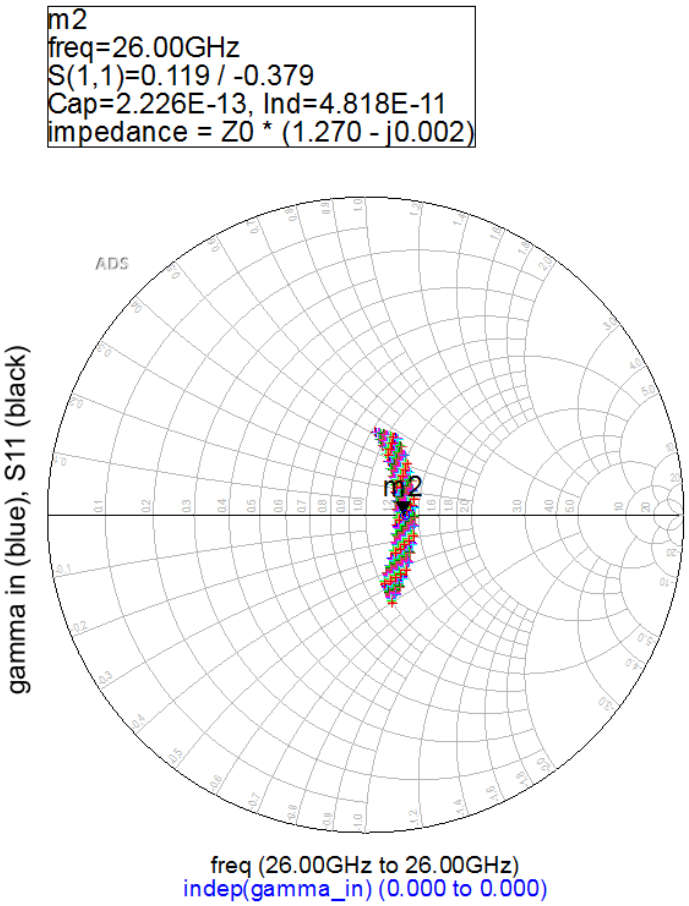


Figure 4.25: Smith Chart side 2- extrinsic impedance is transformed into the corresponding intrinsic resistance

At the end of the analysis, L and C values computed in the two cases are coherent each other.

L	C
48 pH	22.2 pF

Table 4.4: GaN Equivalent model parameters

Thanks to the model, it is possible to replace a FET in simulations, such as the common Source stage in the Stacked case.

4.8 Stacked amplifier, 2-stages

As explained in previous sections, the Stacked amplifier has to be polarized so that both the two stages operate in the same working point; so a $V_{DD} = 40\,\text{V}$ is applied in order to guarantee $V_{DSi} = 20\,\text{V}$.
Moreover the load admittance is chosen to be half of the optimum one.

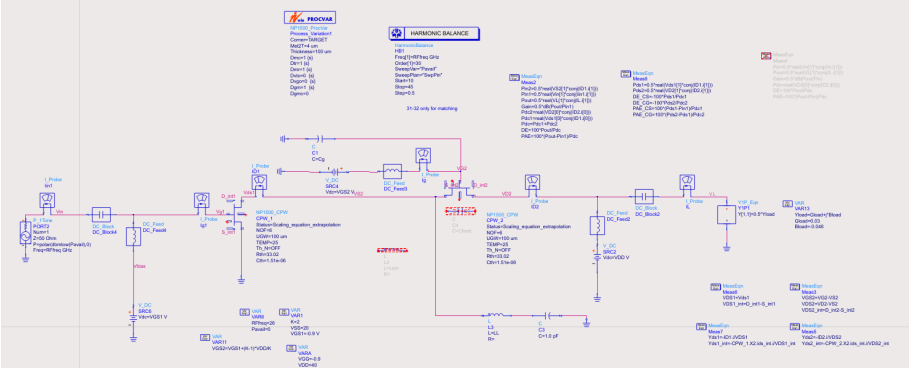
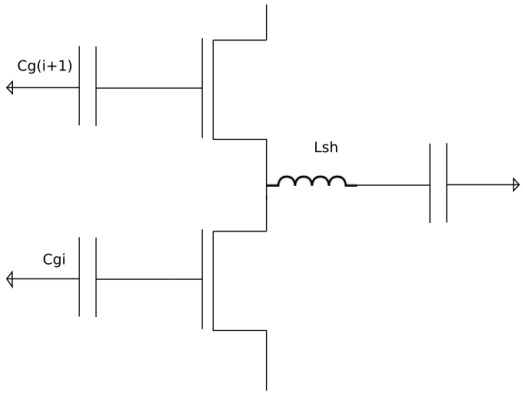


Figure 4.26: 2-stages Stacked amplifier circuit

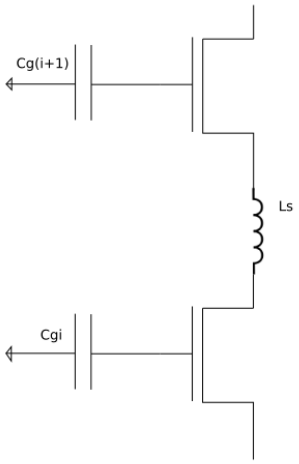
4.8.1 Cg evaluation

As explained in previous sections the inter-stage matching is necessary to guarantee each stage to be loaded by its optimum impedance, defined through the load-pull simulation and so allowing the maximum output power to be delivered.
The Gate capacitance can only match the real part of the impedance, however its evaluation is not as simple as in the ideal case, due to the unknown exact model of the FET. So a mathematical analysis can not be performed in order to evaluate the capacitance to be inserted.
In order to compute the correct value is so necessary to go through a series of simulations. The objective is to match Common Source stage's output impedance and the following one's input impedance; since C_g can only adjust the real part, the imaginary one is tuned through the use of additional elements, such as:

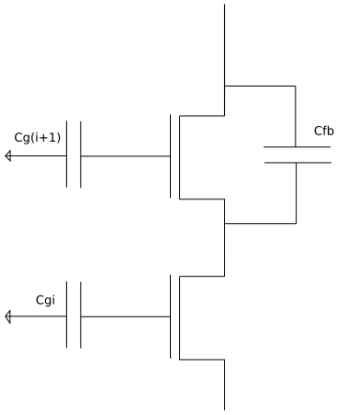
- Shunt inductance
- Series inductance
- Feedback capacitance



(a) Shunt inductance



(b) Series inductance



(c) Feedback capacitance

Figure 4.27: Interstage matching techniques

The insertion of a Shunt inductance, as explained in [1], causes overall load seen by a give stage to be defined as the parallel between the input impedance of the following stage and the shunt itself.
The circuit is reported in fig: 4.27a, in which a decoupling capacitor is added; it has to be large enough to act as an ideal open for the DC component.

As for the series inductor, proposed by [2], the impedance shown by the inductor has to be summed up with the following stage's one.
The schematic is shown in fig: 4.27b.

Finally the feedback capacitor exploits Miller's effect, for which the feedback element can be modeled as two grounded impedances placed where the previous element (the feedback

capacitor) was removed; this allows the rest of the circuit to be unaltered.

$$Y^S_{Miller} = j\omega C_{feed}(1 - A_V) \quad \text{and} \quad Y^D_{Miller} = j\omega C_{feed}(1 - 1/A_V)$$

In the case of a capacitive feedback element, Miller's impedances will still be capacitances, but since it is applied to a non inverting stage, namely the pseudo-CG stage, whose gain is larger than 1, the capacitance to the Source will be negative. This leads to a reduction in the capacitive impedance due to parasitic components, since it placed in parallel to the input impedance.
However this method has a drawback due to the increase in capacitive impedance on the Drain, which makes the output matching more complicated.
Fig: 4.27c reports the latter technique.

In fig: 4.28 (left plot) the extrinsic impedance Y_{DS} is computed for both the two stages. By sweeping C_g (from 100 fF to $10nF$), the real part of Y_{DS} is changed, up to the moment in which it reaches the brown circle, meaning that $Re\{Y_{DSi}\}$, has been converted into the optimal conductance, computed in section: 4.3 and granting the maximum power transfer. The red dot is the final objective: Y_{OPT}, while its constant conductance circle is represented in brown. Y_{DS1} is represented by blue traces whilst pink ones represent Y_{DS2}; also the latter admittance has to be as close as possible to the red dot.
So a good inter-stage-matching solution will allow both the admittances to be close to the optimum one.
In fig: 4.28 (right plot) is referred to the intrinsic parameters, but reports the same information.

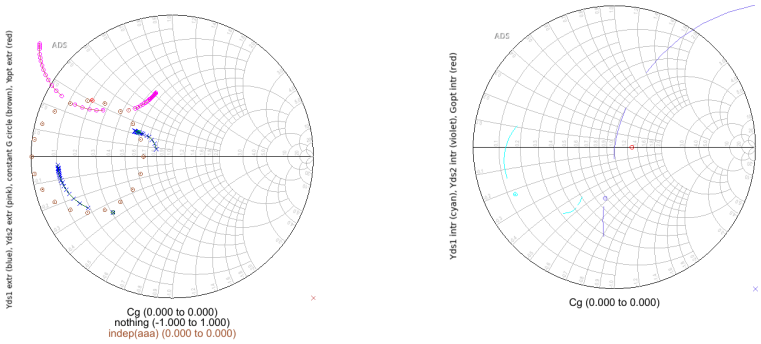


Figure 4.28: Extrinsic (left) and intrinsic (right) Y_{DSi} matching, by C_g sweep

There are clearly two points in which the blue curve intersects the brown one. The first one leads to $C_g = 61.3\,\text{fF}$, while the other one to $C_g = 0.875\,\text{pF}$.

Shunt inductor

The shunt inductance, it is swept between 202.8 pH and 227 pH, taking into account the intersection in the upper part of the chart ($C_g = 0.875$ pF), as shown in the following fig: 4.29. It is decoupled by a 1 nF capacitor.
The major advantage, linked to the use of a shunt network, is the possibility to separately tune the real and imaginary part. Moreover L_{shunt} only affects the input impedance, while the output one is not changed.
When the wanted extrinsic impedance is obtained, also the intrinsic one should coherently be matched to the wanted value (right plot).
In this case $L_{shunt} = 216$ pH. Y_{DS1} results to be quite close to the optimum one, but Y_{DS2}, falling outside the Smith Chart, indicates a general impossibility of the solution.

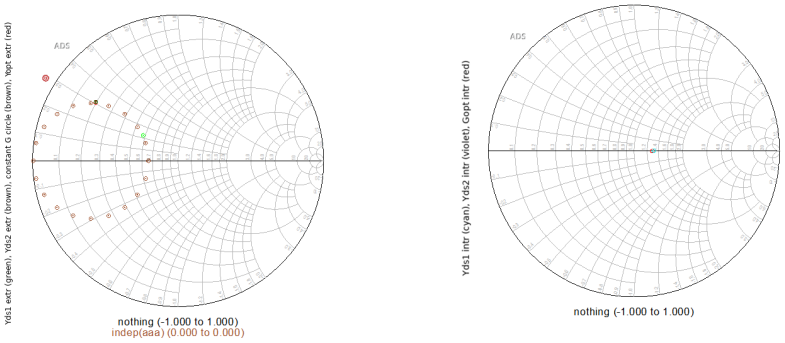


Figure 4.29: Extrinsic (left) and intrinsic (right) Y_{DSi} matching in the Upper point intersection

As for the other intersection (lower one with $C_g = 61.3$ fF), by sweeping between 92 pH and 93 pH, the following result is obtained:

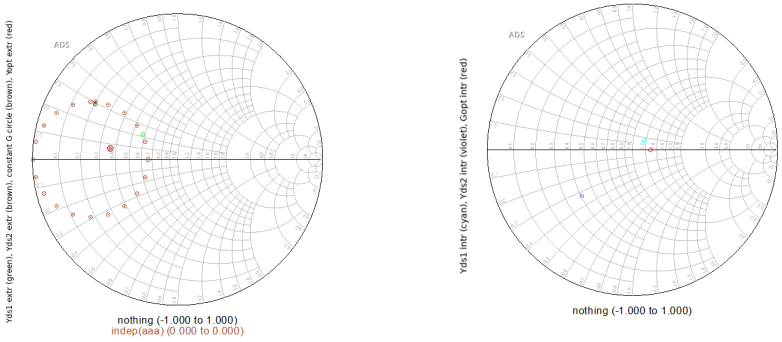


Figure 4.30: Extrinsic (left) and intrinsic (right) Y_{DSi} matching in the lower point intersection

In this case $L_{shunt} = 92.5\,\text{pH}$. Even if both the admittances are inside the chart, Y_{DS2} is not very well matched, differently from Y_{DS1}.

Series inductor

As for the use of a series inductor, it is not able to perform the stage matching, as reported in fig: 4.31, the optimum impedance cannot be obtained.

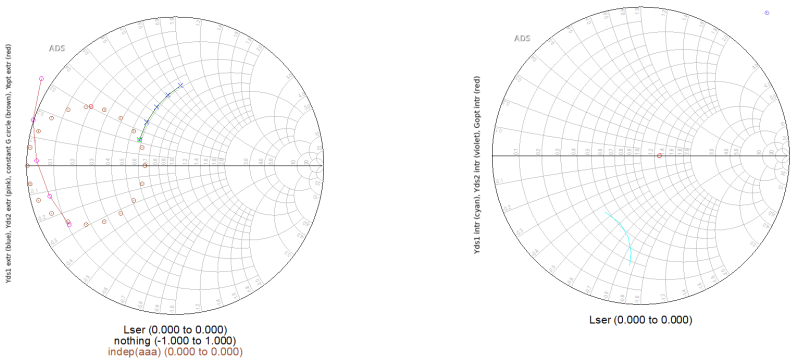


Figure 4.31: Extrinsic (left) and intrinsic (right) Y_{DSi} matching by L_{series} sweep

Feedback capacitor

A similar result can be derived when taking into account the use of a feedback capacitor.

Conclusion

In general the analyzed solutions are not the best ones since even if Z_{DS1} is matched, the second one is not. By analyzing the obtained results, it is possible to claim that a solution which does not guarantee a perfect Z_{DS1} matching, on the other hand allows Z_{DS2} to be. A compromise granting better performance, but not perfect matching for both Z_{DS1} and Z_{DS2}, could be found, by further changing C_g.

In the end the shunt inductor solution is chosen but with a different Gate capacitance; by using $C_g = 0.22\,\text{pF}$ (previously not considered), Y_{DS2} mismatch is much reduced with respect to the other cases:

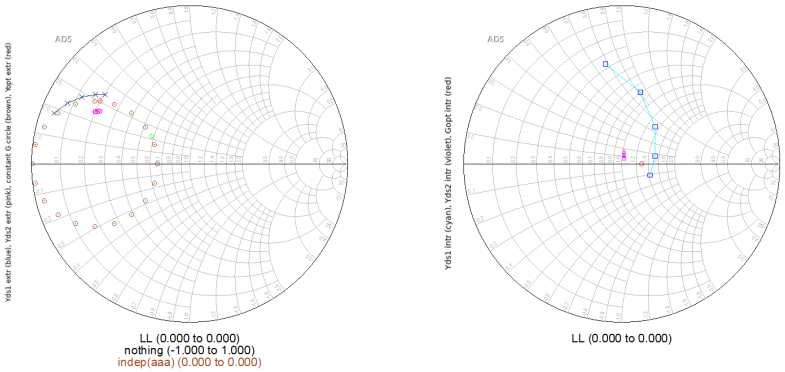


Figure 4.32: Extrinsic (left) and intrinsic (right) Y_{DSi} matching through L_{shunt} sweep, given $C_g = 0.22\,\text{pF}$

The chosen shunt inductance will be 175 pH.

By choosing a correct Drain-Source impedance, the intrinsic dynamic load line is expected to be as close as possible to a straight line, in order to maximize the output power. From fig: 4.33, both CS and CG load lines behave in the correct way, giving a further evidence of proper inter-stage matching.

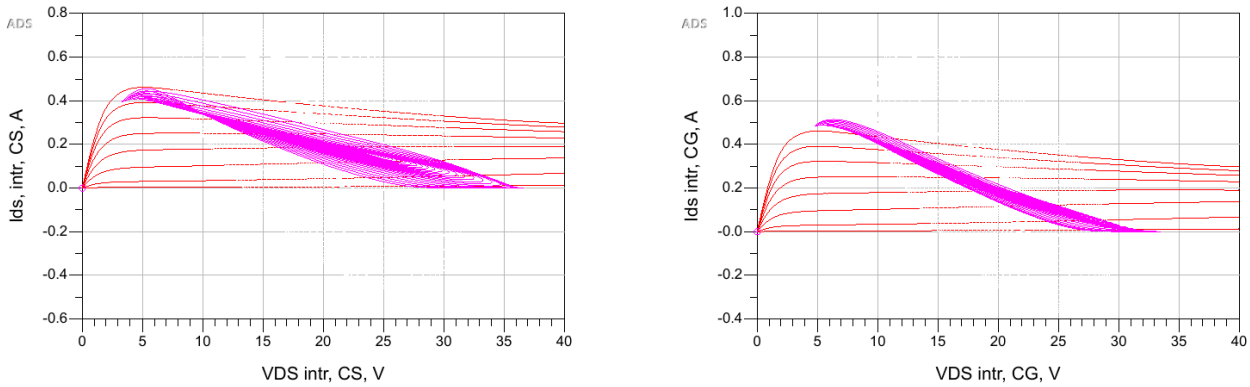


Figure 4.33: $C_g = 0.22\,\text{pF}$ and $L_{shunt} = 175\,\text{pH}$ extrinsic (left) and intrinsic (right) dynamic load lines

4.8.2 performance

Taking now into account the achieved performance, fig: 4.34, which can be obtained with such a configuration, it is clear that gain is as expected 3 dB higher than a single stage amplifier can provide. As a consequence the output power is 3 dB larger than the CS case. Taking a look at the gain graph, it is about 12 dB for the CS stage and $\sim$ 15 dB for the Stacked amplifier.

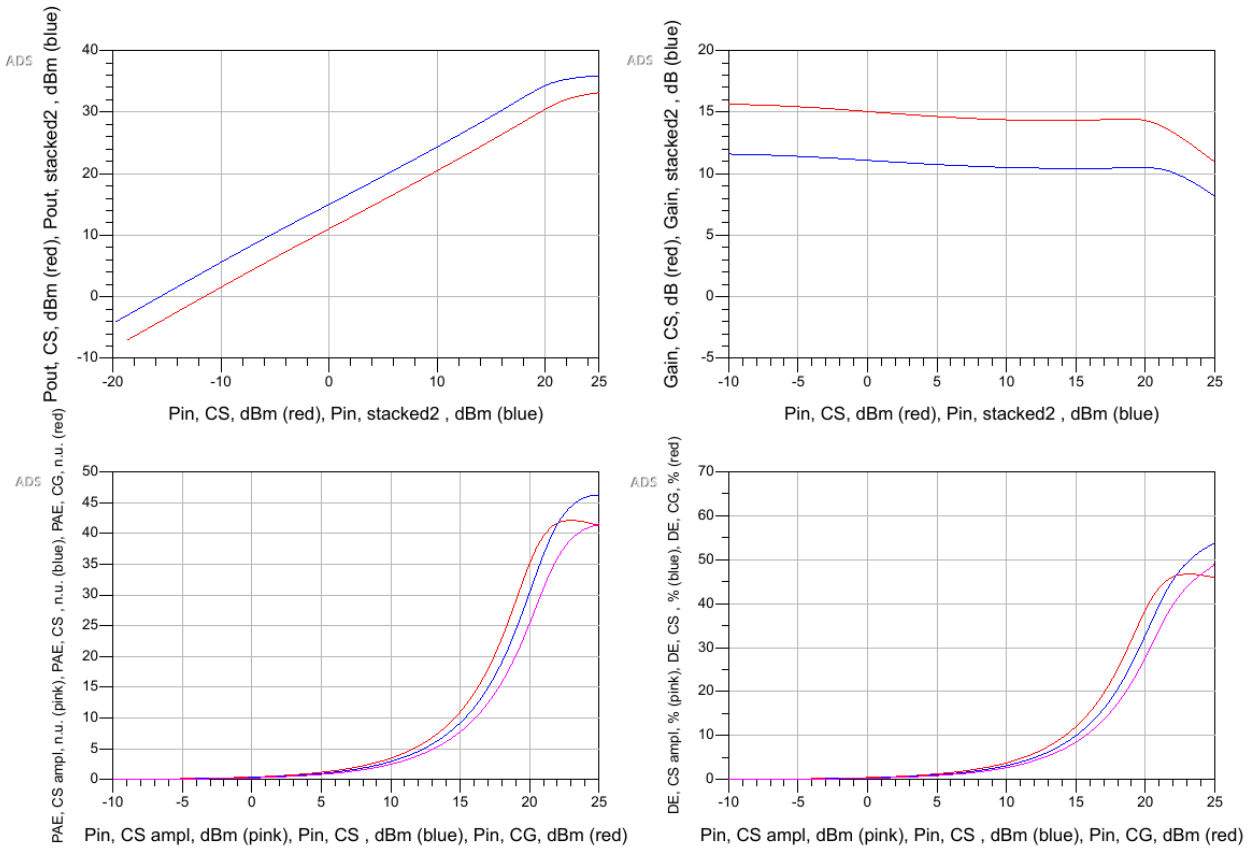


Figure 4.34: $C_g = 0.22\,\text{pF}$ and $L_{shunt} = 175\,\text{pH}$ performance: P_{OUT} (top left), Gain (top right), PAE (bottom left) and DE (bottom right)

The efficiency of the CG stage is quite the same as the previously computed for the single CS stage, due to the proper matching between the two stages.
As for PAE, all the stages show a similar behavior with respect to the single CS.

4.9 Stacked amplifier, 3-stages

The 3-stages Stacked amplifier requires a $V_{DD} = 60\,\text{V}$, since three 20 V voltage drops have to be guaranteed on each FET between Drain and Source. All the transistors are biased in Class A, so a $VGS = -0.9\,\text{V}$ is necessary.
The load is required to be $1/3 \times Y_{OPT}$.

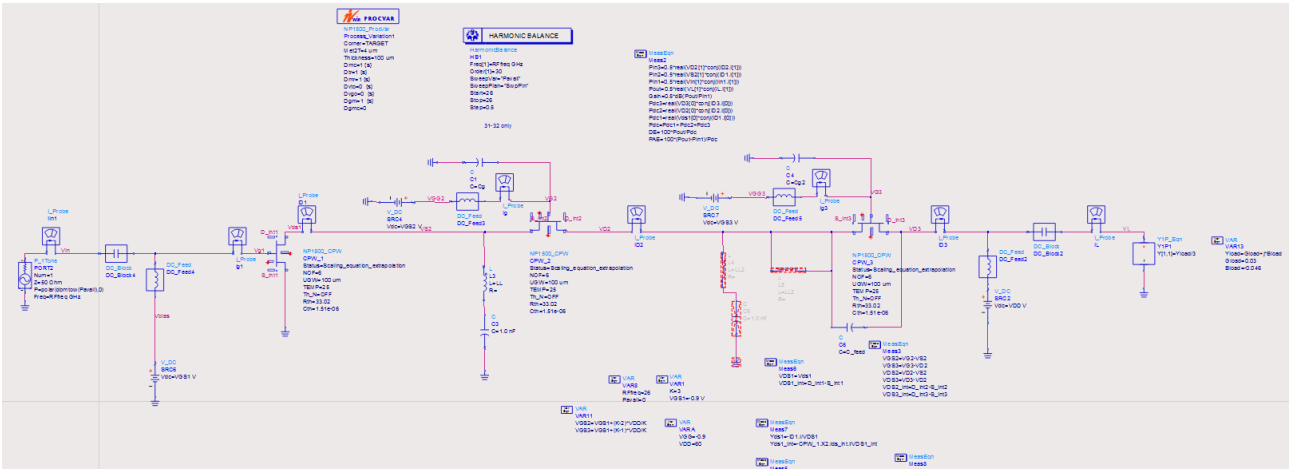


Figure 4.35: 3-stages Stacked amplifier circuit

4.9.1 Cg evaluation

The actual computation of the Gate capacitance for the second pseudo-common Gate stage, is performed by sweeping the C_{g2} itself and by adding a further matching network.
In particular a shunt inductance with a 1 nF decoupling capacitance is used.
Fig: 4.36 shows a 10 fF to 150 fF capacitance sweep, while L_{SHUNT} is varied from 100 pH to 1 nH:

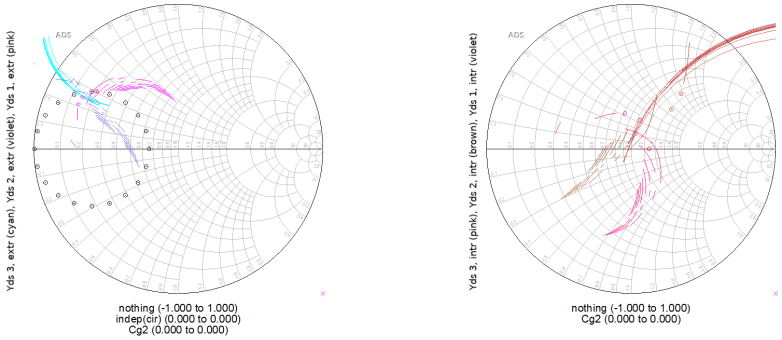


Figure 4.36: Extrinsic (left) and intrinsic (right) Y_{DSi} matching, by C_{g2} and L_{SHUNT} sweep

The insertion of a further pseudo-common Gate stage causes both Y_{DS1} and Y_{DS2} to change.

From fig: 4.36 it is possible to define that the optimal C_{g2}, which is able to minimize each Z_{DS} deviation with respect to the optimal one, is 105 fF. As for the shunt inductance, it is 296 pH. The resulting impedances are reported in fig: 4.37

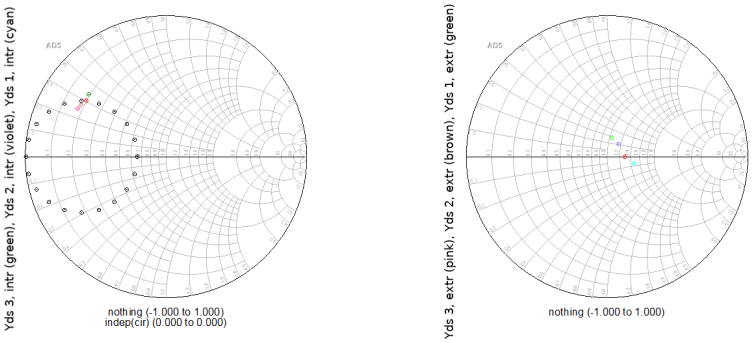


Figure 4.37: Extrinsic (left) and intrinsic (right) Y_{DSi} matching, through L_{SHUNT} = 296 pH and C_{g2} =105 fF

The intrinsic dynamic load lines are quite straight, as expected; first stage's line is somehow more elliptical with respect to the other ones, since as shown in fig: 4.37, Z_{DS1} is the most distant from the ideal load among the three.

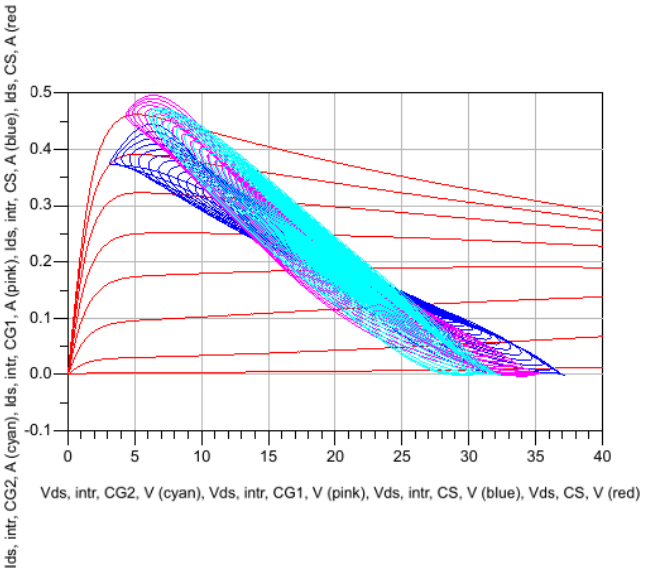


Figure 4.38: Intrinsic load lines for a 3-stages stacked amplifier, through two shunt inductors InMNs; the first InMN is based on C_g = 0.22 pF and L_{SHUNT} = 175 pH, while the second one C_{g2} = 105 fF and L_{SHUNT} = 296 pH

A second matching solution is tried out: the series inductance, but unfortunately, the simultaneous matching of the three Drain-Source impedances is not possible, as shown in fig: 4.39.

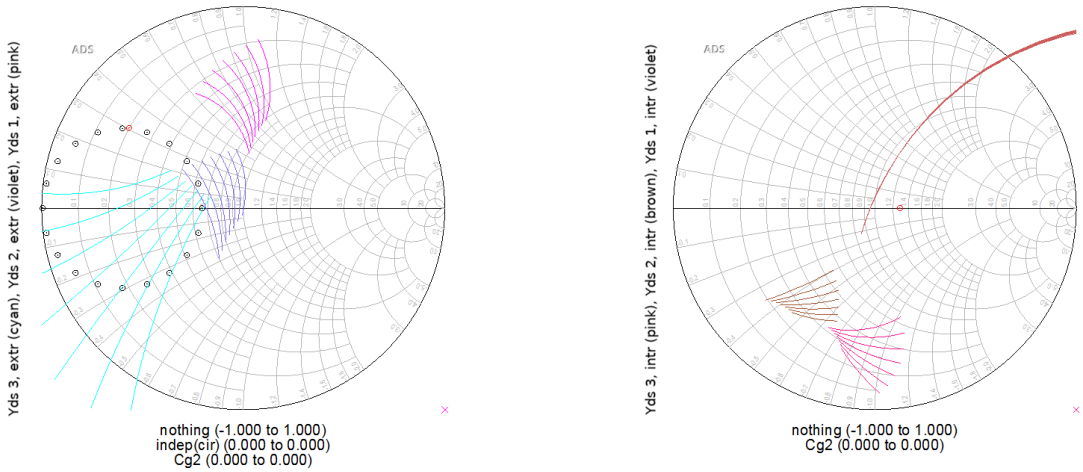


Figure 4.39: Extrinsic (left) and intrinsic (right) Y_{DSi} optimization, by C_{g2} sweep and series inductor

4.9.2 Performance

In fig: 4.40 the achievable performance are reported; as reported in the first two plots the difference in gain (and so in P_{OUT}) between the single stage and the 2-stages is 3 dB, as explained before.
On the other hand the third stage allows for a theoretical increase in gain of 1.8 dB. Due to the the imperfect matching, the obtained gain growth is only 1.2 dB, namely ranging from 14.3 dB to 15.5 dB.
The same information can be obtained by looking at the output power plot.

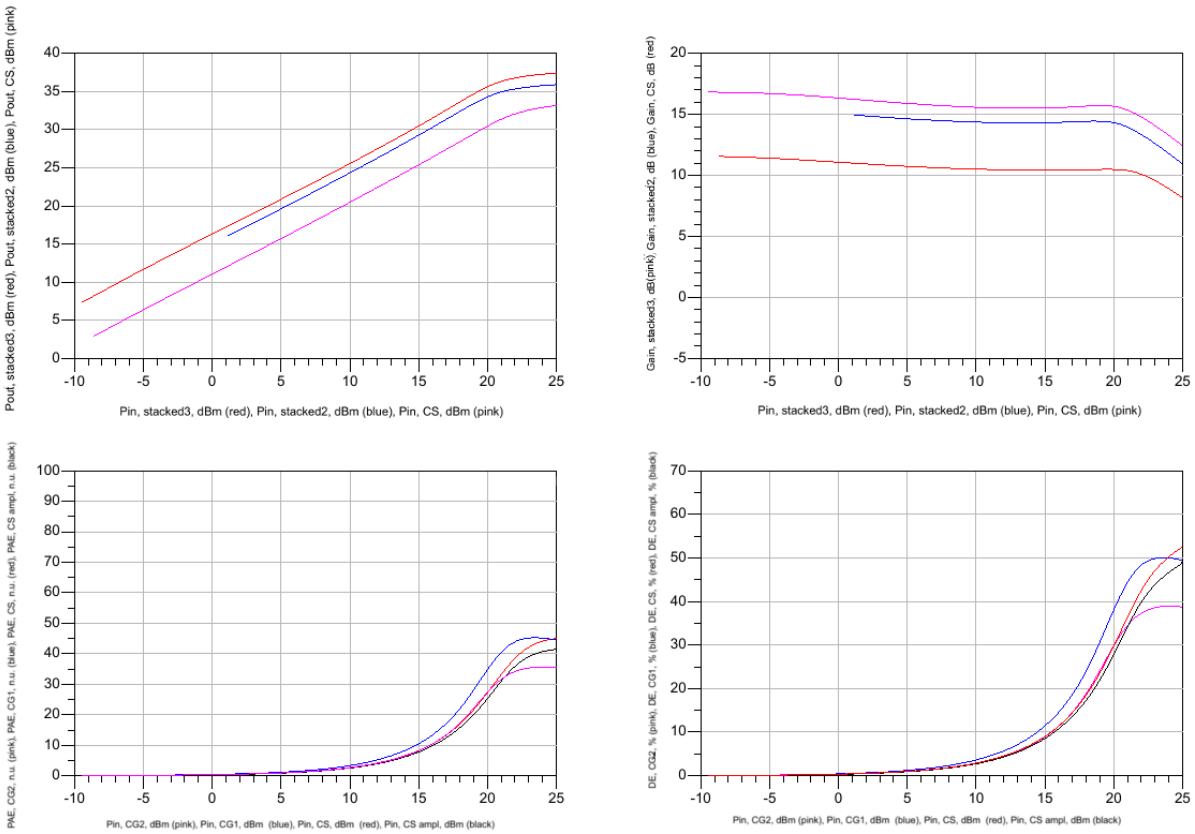


Figure 4.40: $C_g = 0.22\,\text{pF}$, $C_{g2} = 105\,\text{fF}$ performance: P_{OUT} (top left), Gain (top right), PAE (bottom left) and DE (bottom right)

On the other hand the efficiency of CS and CG1 stages are quite the same as the previously computed for the single CS stage, due to the proper matching between the two stages; third stage's efficiency is a bit lower since its Z_{DS} is not perfectly matched, as shown in fig: 4.37.
As for PAE, again, it is lower in the case of the third stage for the same reason.

4.9.3 Stabilization

As reported in section: 4.2, the single CS stage is not stable; the same can be said for the two stage Stacked amplifier: in fig: 4.41,

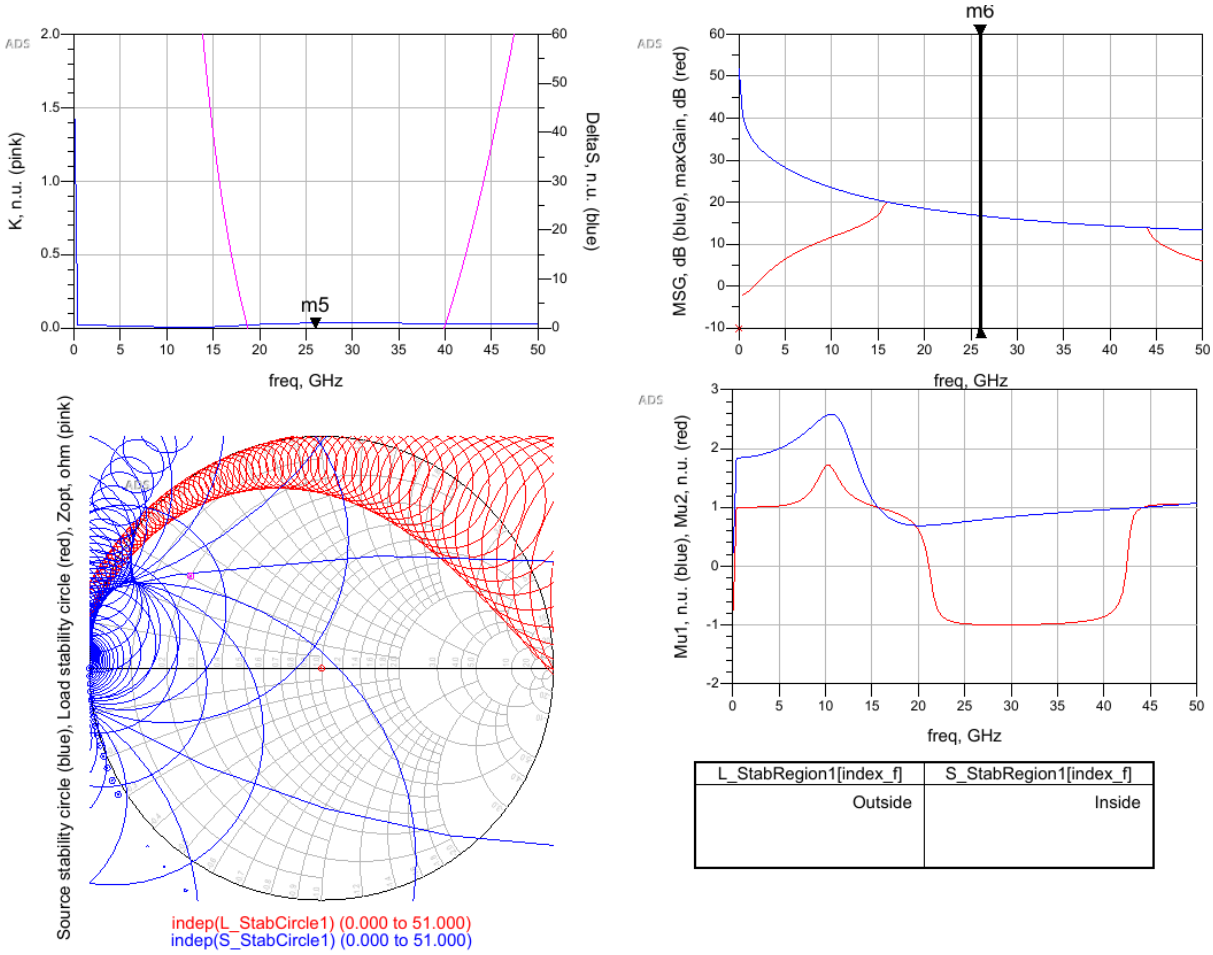


Figure 4.41: Unstabilized 2-stages Stacked amplifier stability performance: K and ΔS (top left) and Gain (top right); stability circles (bottom left); Mu1 and Mu2 (bottom right)

It is clearly unstable in the working frequency range; moreover the use of the same stabilization network as in the case of a CS is not suitable and can not improve the situation. The instability tank can not be altered in this way.

Differently from the CS, Stacked amplifier's stability is also influenced by the proper matching between two stages, a part form the input stabilization network; the choice of C_g and shunt components is so crucial for a proper stabilization.

Unfortunately also for the 3-stages stacked amplifier's stabilization through the standard network is made impossible.

The instability problem makes the stacked amplifier's design unfeasible, at the chosen working frequency, so a new technology is taken into account: the GaAs, which will be analyzed in the next chapter and in the following one.

Chapter 5

Real Device - GaAs

5.1 Device evaluation

It is now taken into account the second real device: commercial Depletion Mode InGaAs pHEMT Technology. In particular a $4 \times 100\,\mu$m device is used. Again, the chosen design frequency is 26 GHz.
According to the foundry non-linear model the optimal Drain-Source voltage is 4 V, while the breakdown voltage is 9.5 V; the device is characterized by a -0.95 V pinch-off voltage. Given the previously cited periphery, namely $400\,\mu$m, the device will be able to provide 0.208 A.
The following figure shows the DC input and output characteristics of the device, in which $V_{TH} = -1.25$ V and $I_{DSS} = 0.2$ A.

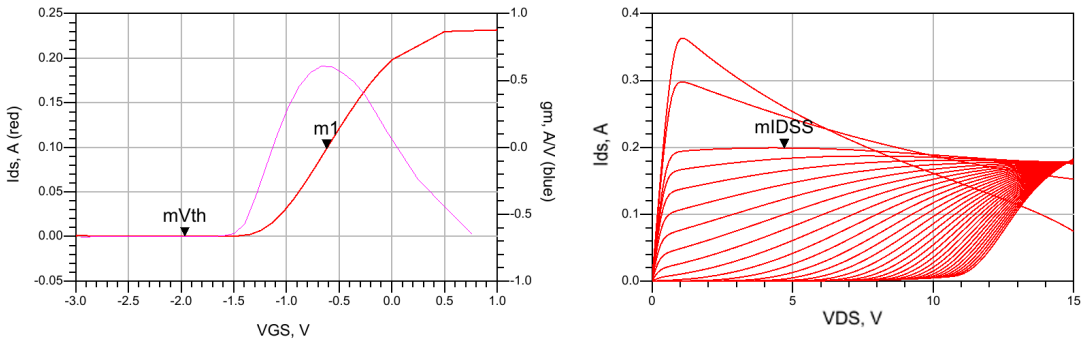


Figure 5.1: Common Source trans-characteristic and transconductance (left) and output characteristics (right)

In order to use the FET as a class A amplifier, it is necessary to choose $V_{GS} = -0.6$ V, so to obtain a quiescent current of 0.1 A.
However it is chosen to work with a class AB amplifier with a -0.5 V Gate polarization,

so that the transconductance is about 0.18 A/V.

From the S-parameter simulation, taking a look at S12, which is quite 0 for the whole frequency range, the device can be said to be unilateral.

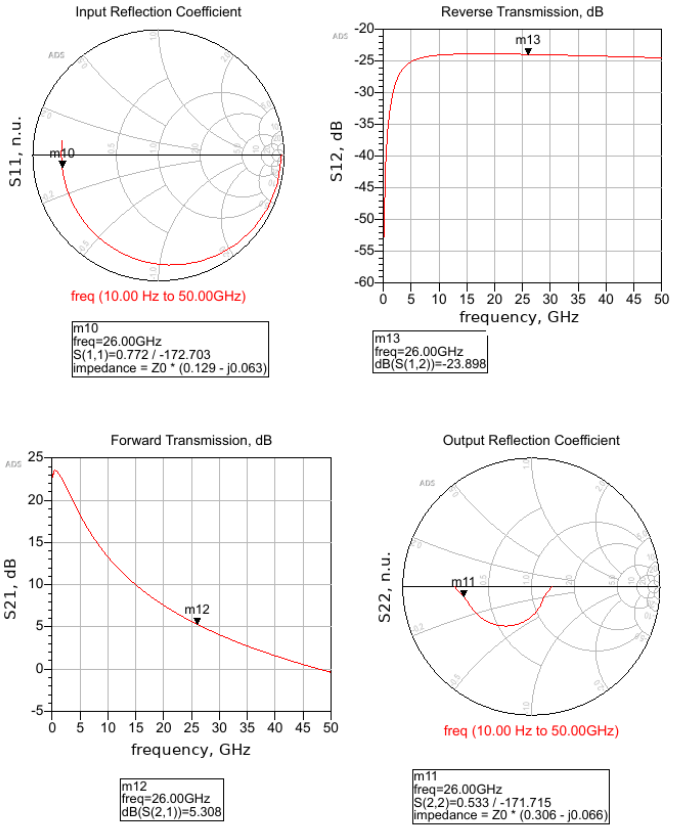


Figure 5.2: S-parameter simulation CS stage

As for the load pull analysis, results concerning contours are reported in fig: 5.4, while maximum parameters are shown in tab: 5.3. No stabilization networks are used in this first analysis.

P_{OUT}^{max}	$Gain^{max}$	PAE^{max}	DE^{max}
25 dBm	10.85 dB	37.76%	42.29%

Table 5.1: GaAs load-pull performance

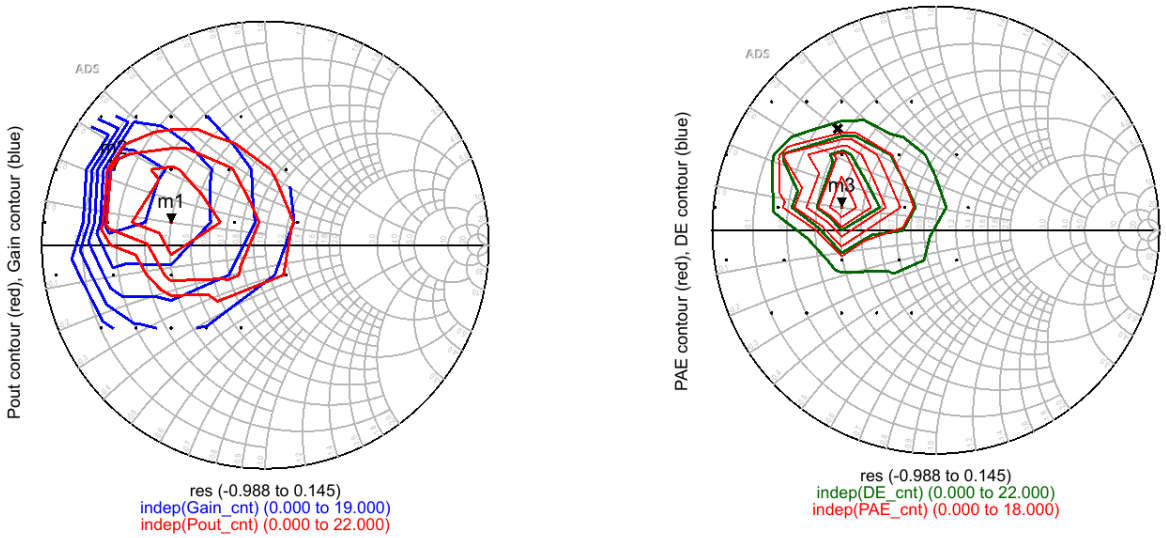


Figure 5.3: Load pull simulation results for Gain, P_{OUT}, DE and PAE

from which:

- $Z_{OPT}^{Pout} = (15 + j7.5)\,\Omega$
- $Z_{OPT}^{Gain} = (6 + j10)\,\Omega$
- $Z_{OPT}^{PAE} = (16.95 + j9.3)\,\Omega$
- $Z_{OPT}^{DE} = (16.95 + j9.3)\,\Omega$

Also in this case thee optimum impedance for DE and PAE's maximization is the same one.
In the following the first impedance will be used, so to maximize the output power; the associated admittance is $Y_{OPT} = (0.053 - j0.026667)\,\mathrm{S}$.
Since for this technology no intrinsic pins are available, only the extrinsic dynamic load line can be defined, taking into account a CS configuration:

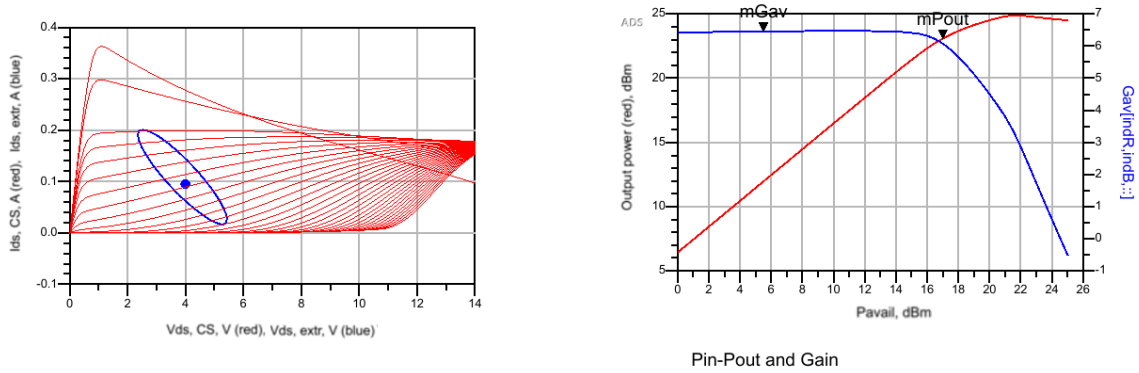


Figure 5.4: Common Source output characteristics with extrinsic DLL (left); P_{OUT} and Gain (right)

As expected it is elliptic; furthermore the maximum output power for a 1 dB compression gain ($\sim 17\,\text{dBm}$) is the expected one. In this condition the other parameters are shown in fig: 5.5:

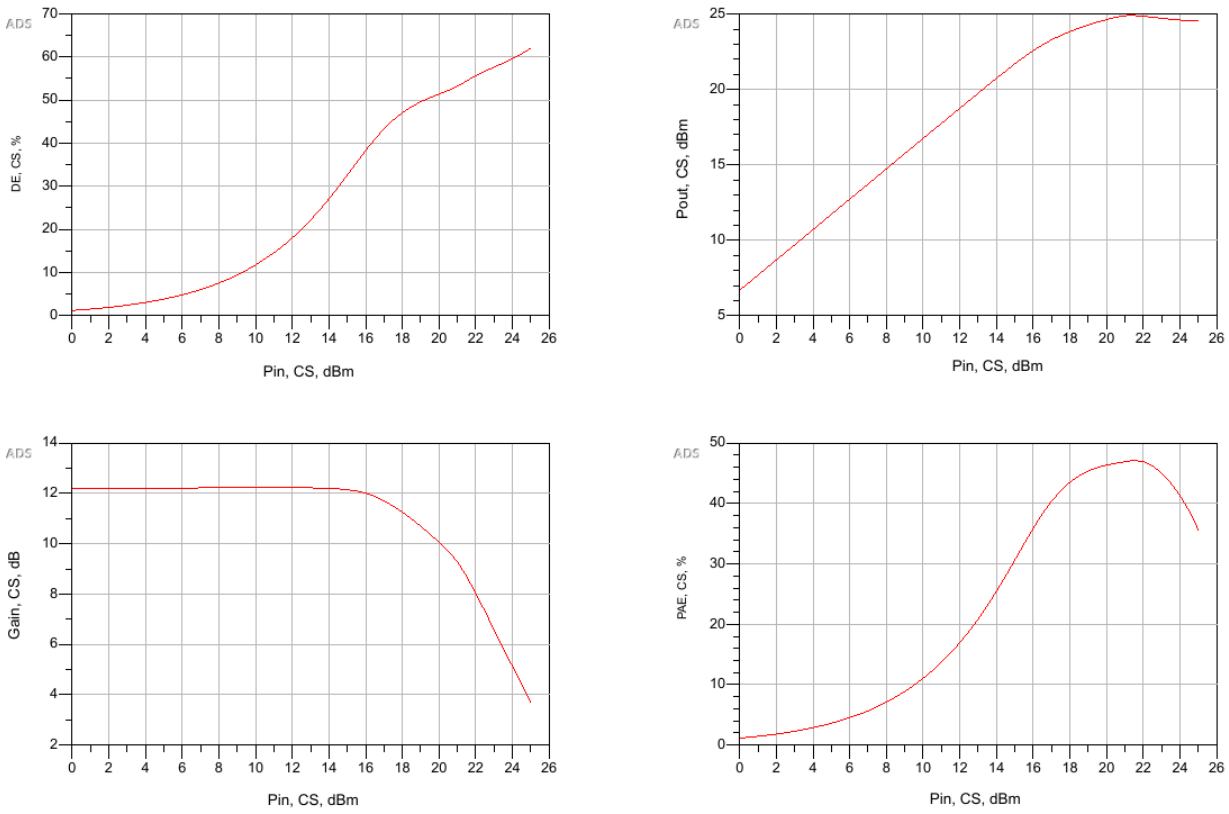


Figure 5.5: CS parameters: DE (top left), P_{OUT} (top right), Gain (bottom left) and PAE (bottom right)

5.2 CS stabilization

Let's now analyze a single CS stage: its stability parameter K is lower than 1 for a large frequency range, namely low frequencies, whose impedance can not be controlled. The potentially unstable region is also shown by stability circles which cover most of the Smith Chart, making it quite impossible to use the correct optimum load, which would fall inside the unstable region, without adding a stabilization network.

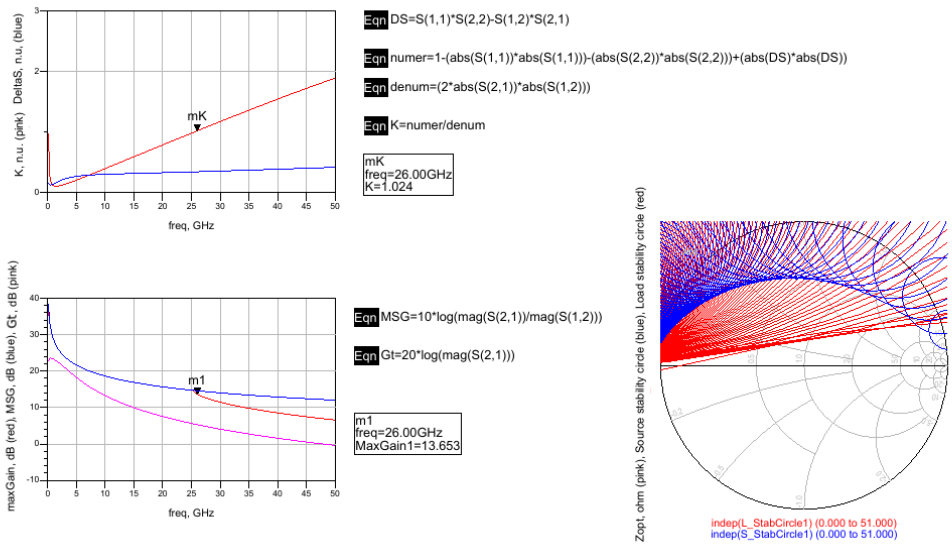


Figure 5.6: CS stability performance: K and ΔS (top) and Gain (bottom left); stability circles (bottom right)

In order to achieve stabilization, it is employed the same network which was used for the GaN HEMT (the schematic is plotted in fig: 4.6). In fig: 5.7 it is reported the final result showing a Rollet factor ≥ 1 and a $\Delta S \leq 1$ for all the frequency range.
Taking a look at the graph on the right, gain loss with respect to the MAG, at the working frequency is about 1 dB while it increases, at lower frequencies.

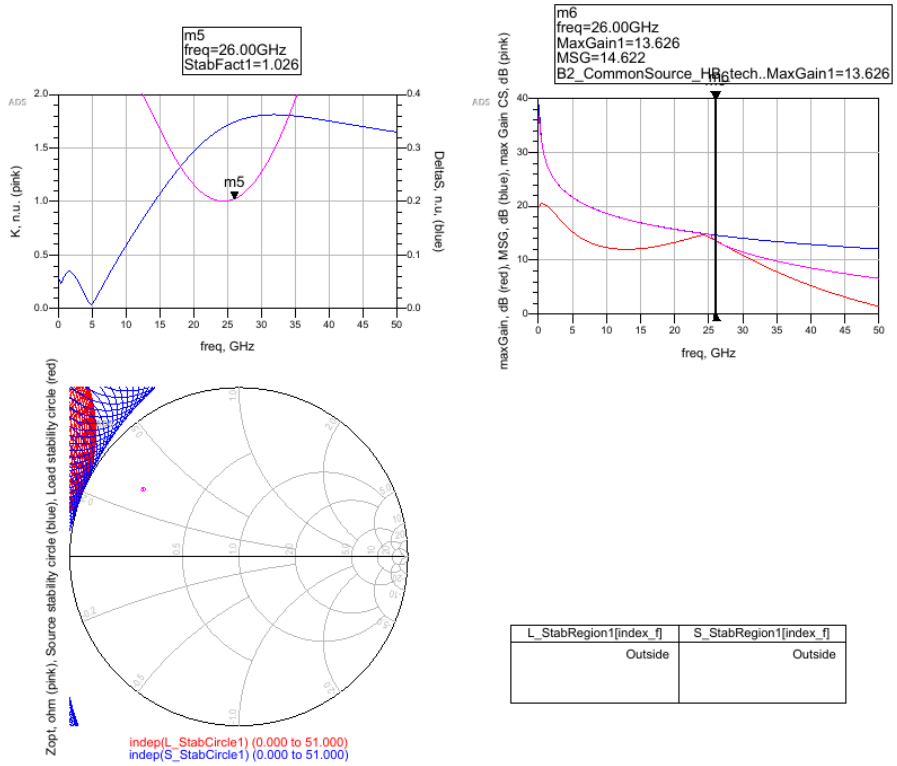


Figure 5.7: Stabilized CS stability performance: K and ΔS (top left) and Gain (top right); stability circles (bottom)

The following table reports network's parameters:

R_{stab}	C_{res}	L_{res}	R_{GG}	L_{GG}
54.28 Ω	0.30 pF	120 pH	100 Ω	6.9 nH

Table 5.2: GaAs stabilization network parameters

5.3 Intrinsic and Extrinsic parameters evaluation

Repeating the de-embedding procedure for the GaAs HEMT[1], as described before in section: 4.6, the following parameters are obtained:

[1]In the case of GaAs, hot FET's S-parameters are evaluated at $V_{DS} = 4\,\text{V}$ and $V_{GS} = -0.5\,\text{V}$, while as for the Cold FET $V_{DS} = 0\,\text{V}$ and $V_{GS} = -3\,\text{V}$. Finally pinch off is obtained for $V_{DS} = 0\,\text{V}$ and $V_{GS} = 3\,\text{V}$

L_G	L_D	L_S	R_G	R_D	R_S
19.8 pH	17.7 pH	1.67 pH	3.43 Ω	2.37 Ω	0.62 Ω

Table 5.3: GaAs Extrinsic parameters

As for the intrinsic parameters

C_{GD}	C_{DS}	C_{GS}	R_I	R_{DS}
57.9 fF	118.4 fF	385.6 fF	0.765 Ω	58.39 Ω

Table 5.4: GaAs Intrinsic parameters

Moreover $\tau = 0.123$ ps and $g_m = 0.339$ A/V. The obtained value is different with respect to the previously evaluated one; this could be due to the low R_{DS}, which makes the de-embedding derived not correct.
These parameters are quite stable in frequency as shown in fig: 5.8

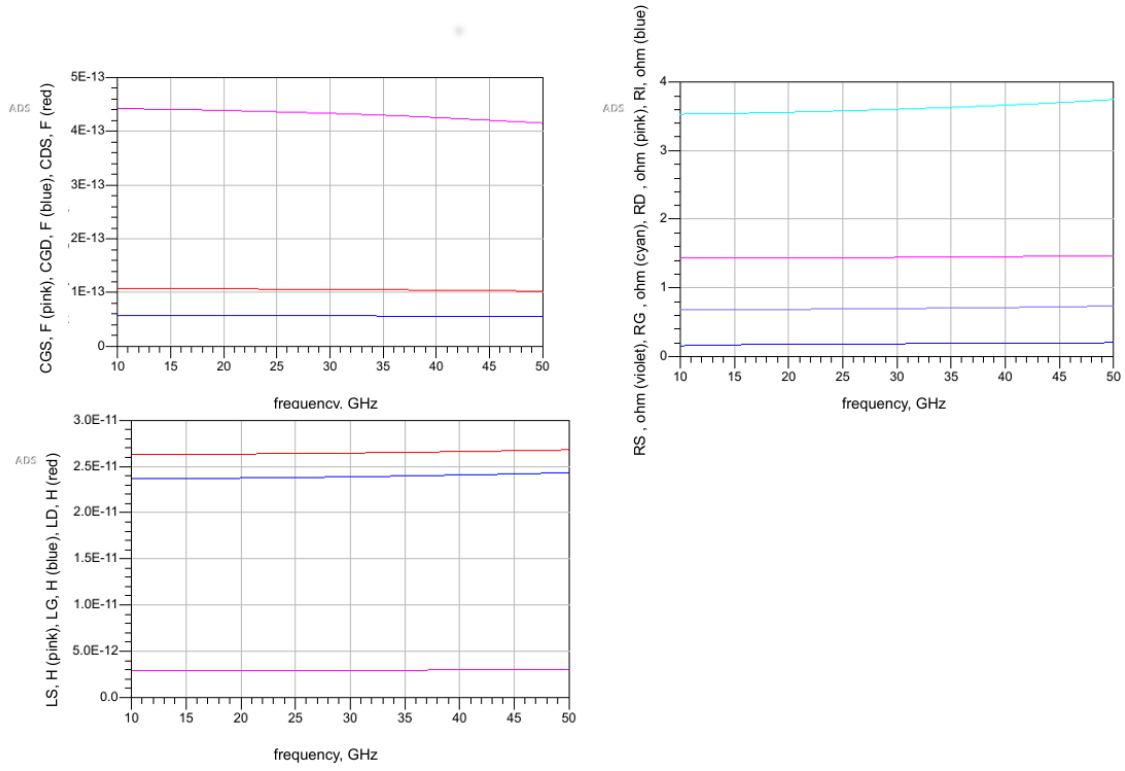


Figure 5.8: Intrinsic and Extrinsic parameters in frequency

Let's now proceed as in section: 4.6, removing the intrinsic and extrinsic contributions in order to verify the extracted parameters. Fig: 5.9 reports the same circuit as for the GaN; the only difference is to be found in the used FET. The intrinsic current is computed

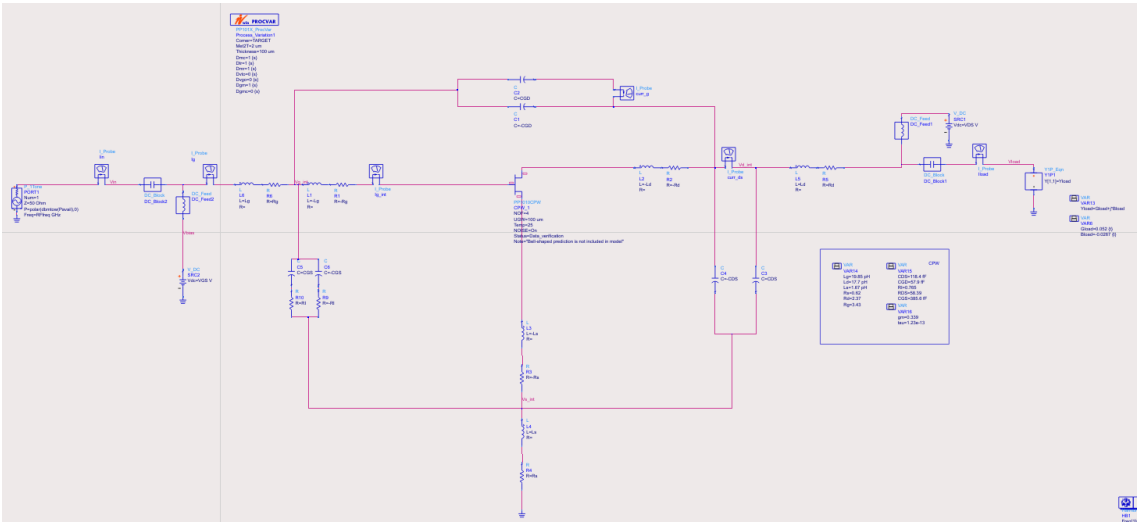


Figure 5.9: Parameter removal circuit with intrinsic nodes

by summing up the two contributions: curr_g and curr_ds in the schematic.
As before the Drain-Source resistance can not be removed.
The resulting DLL, reported in fig: 5.10, shows an elliptical behavior, meaning that parameter extraction is not perfect. With respect to the GaN, no comparison can be performed with the intrinsic load line, due to the absence of intrinsic pins in the used model.

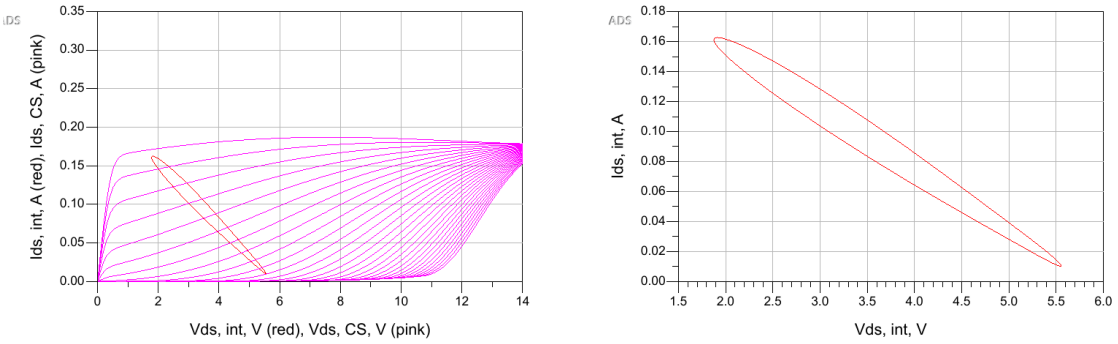


Figure 5.10: Intrinsic DLL resulting from parameters removal

5.4 Stacked amplifier, 2-stages

In order to properly bias the Stacked amplifier a $V_{DD} = 8\,\mathrm{V}$ is applied at pseudo-CG's Drain, so that each $V_{DS} = 4\,\mathrm{V}$, as expected; load's admittance is chosen to be half of the optimum one.

5.4.1 Cg evaluation

Differently from the other case, the GaAs HEMT can also be properly matched through the use of the series inductance, as well as through the feedback capacitance.
Another possible matching technique is base on the use of the C_g only and on a fine tuning of the load, so that through the former, Y_{DS1} is properly matched. Then a variation of the load admittance, allows for a variation in Y_{DS2}.
Starting from the shunt inductance, without changing the load and so Y_{DS2}, a good compromise, namely $C_g = 0.175\,\text{pF}$ and $L_{shunt} = 332.3\,\text{pH}$, could be the one reported in fig: 5.11, in which Y_{DS1} is quite close to the optimum admittance, while the other one could be improved by changing a bit the load.

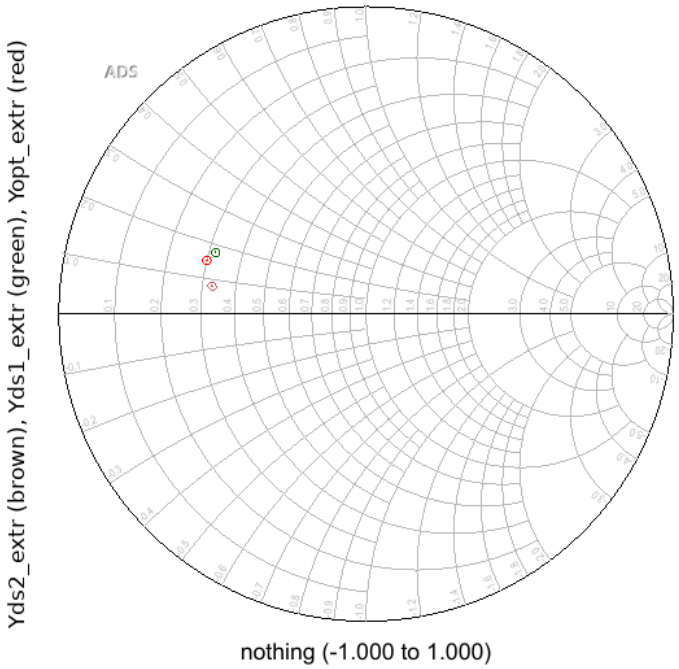


Figure 5.11: Extrinsic Y_{DSi} matching with $C_g = 0.175\,\text{pF}$ and $L_{shunt} = 332.3\,\text{pH}$

In these condition, the achievable performance are reported in fig: 5.12: being a two stages Stacked amplifier, the increase in gain and so in the output power with respect to a single CS is ideally 3 dB; the assumption is confirmed by simulations.

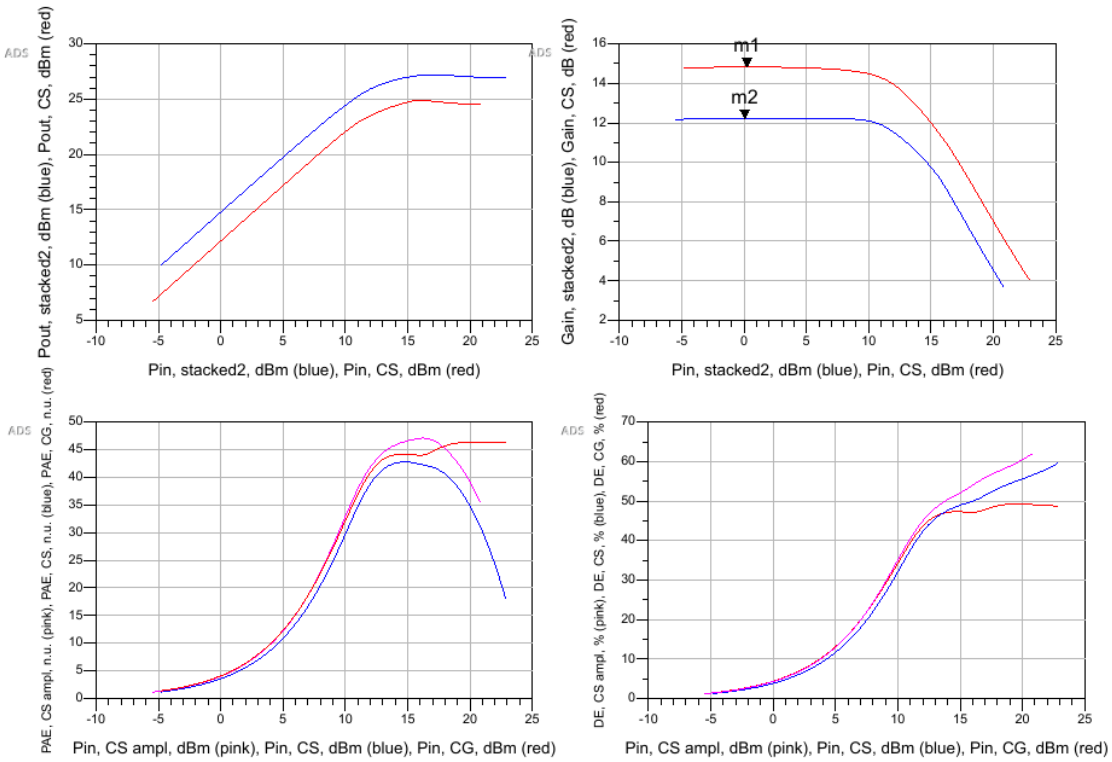


Figure 5.12: performance with $C_g = 0.175\,\text{pF}$, $L_{shunt} = 332.3\,\text{pH}$: P_{OUT} (top left), Gain (top right), PAE (bottom left) and DE (bottom right)

Moreover PAE and DE of the single stages are similar to those of a CS.

Taking now into account the use of C_g only, as shown in fig: 5.13, it is possible to obtain a similar result with respect to the shunt case in terms of matching; in general it could be said that it is even improved.

The best configuration requires $C_g = 0.398\,\text{pF}$ and $G_{LOAD} = 0.0533\,\Omega$, $B_{LOAD} = -0.0449\,\text{S}$.

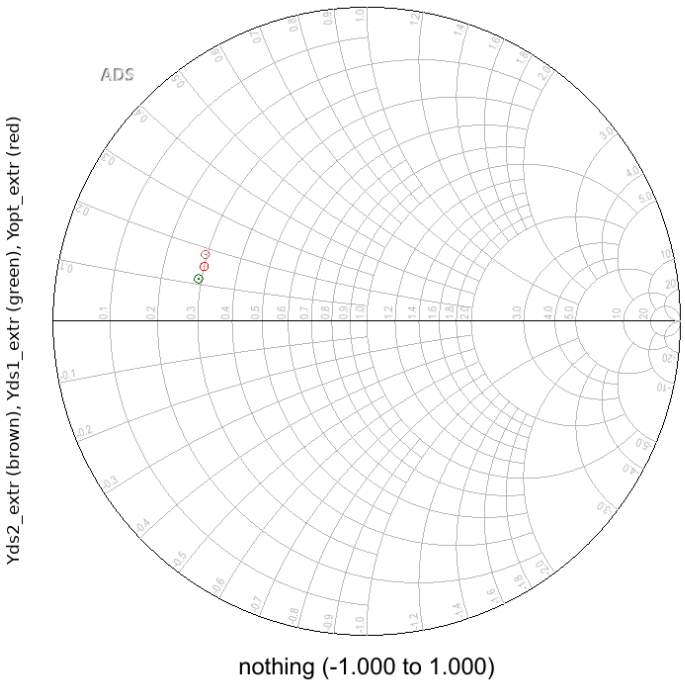


Figure 5.13: Extrinsic Y_{DSi} matching with $C_g = 0.398\,\text{pF}$ and load variation

The use of a single reactive element makes this configuration preferable with respect to the other one which also requires an inductor. On the other hand it is necessary to consider the fact that the optimum load is changed

As for the use of a series resistance, the achievable matching for both the two FETs is a bit worse with respect to the previous case, as reported in the following image. The compromise was reached through the use of $C_g = 0.26\,\text{pF}$ and $L_{series} = 5\,\text{pH}$.

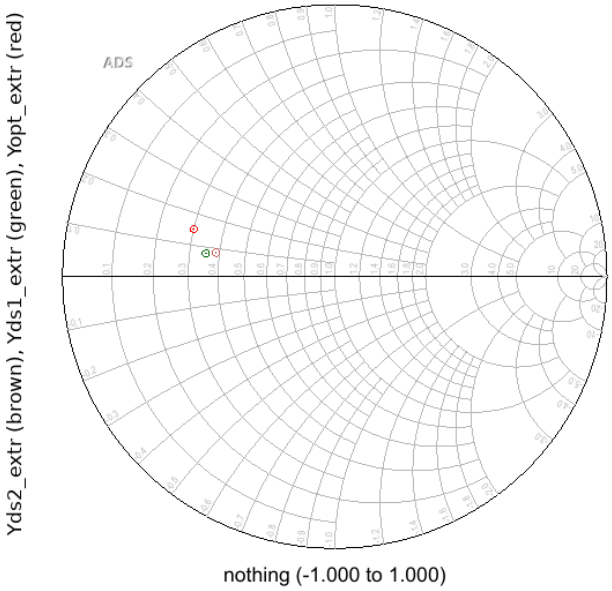


Figure 5.14: Extrinsic Y_{DSi} matching with $C_g = 0.26\,\text{pF}$ and $L_{series} = 5\,\text{pH}$

Finally the use of a feedback capacitor leads to unsatisfactory results, since taking into account the best point, both Y_{DS1} and Y_{DS2} can not fall close to the optimum value. By sweeping feedback capacitor's value, it is clear that the best performance can be obtained when $C_{feed} = 7\,\text{fF}$.

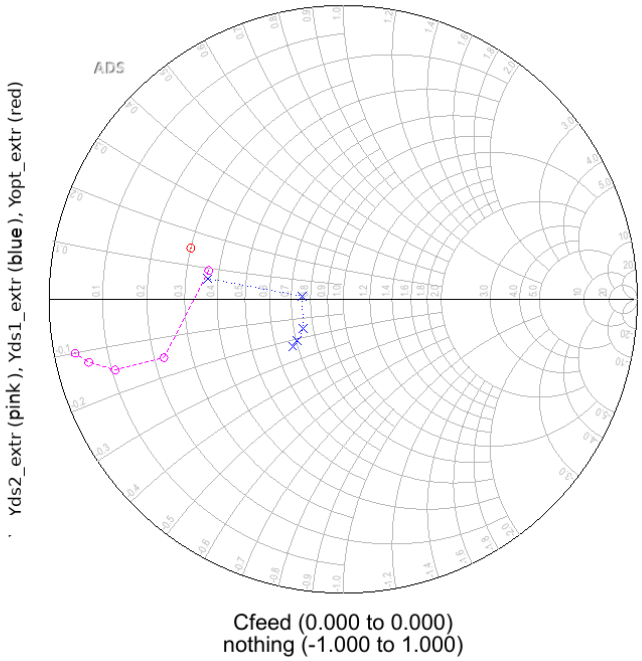


Figure 5.15: Extrinsic Y_{DSi} matching with $C_g = 0.24\,\text{pF}$ and C_{feed} sweep

Overall the best solution is the one involving a variation in the load or the use of a shunt inductance. The latter solution will be used in the 3-stages Stacked amplifier, since accounting for load variation in the design of the third stage would be more complicated.

5.4.2 Stabilization

In order to stabilize the Stacked amplifier, the previously designed network was a bit changed so to obtain better performance and so a lower gain loss with respect to the MAG.

R_{stab}	C_{res}	L_{res}	R_{GG}	L_{GG}
$23.88\,\Omega$	$0.49\,\text{pF}$	$76\,\text{pH}$	$100\,\Omega$	$7.65\,\text{nH}$

Table 5.5: GaAs 2-stages Stabilization network parameters

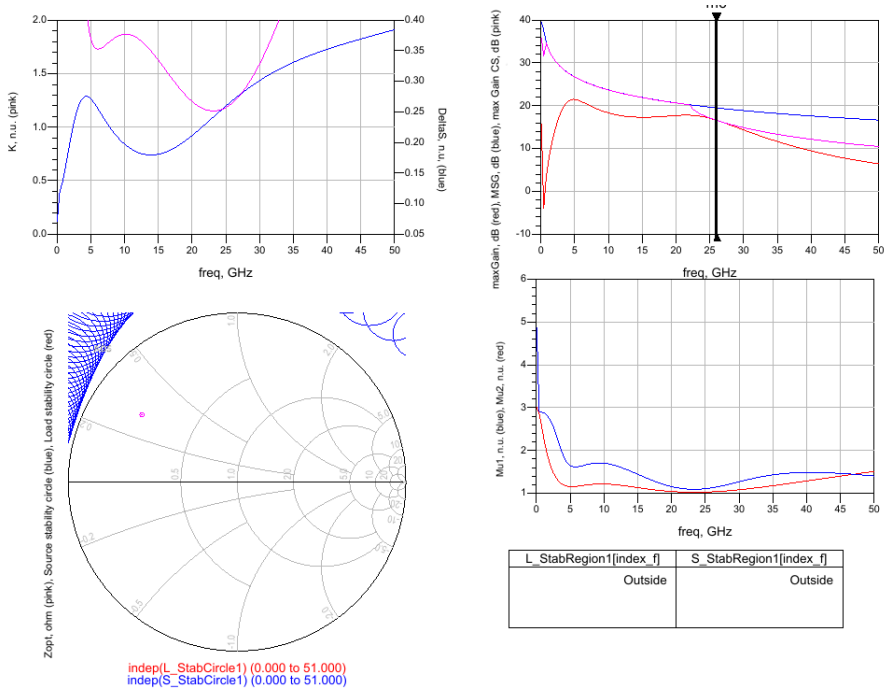


Figure 5.16: Stabilized Stacked amplifier stability performance: K and ΔS (top left) and Gain (top right); stability circles (bottom left); Mu and Mu1 (bottom right)

In this case the gain loss is lower with respect to the case of a single stage CS for the higher frequencies.

5.5 Stacked amplifier, 3-stages

In order to properly bias the Stacked amplifier a $V_{DD} = 12\,\mathrm{V}$ is applied so that each $V_{DS} = 4\,\mathrm{V}$, as expected and the load admittance is chosen to be 1/3 of the optimum one.

5.5.1 Cg evaluation

Taking into account an inner inductive shunt matching as described in section: 5.4.1, all the four matching solutions are tested for the added stage.
The best solution involves the use a further shunt inductance (schematic in fig: 5.17): as reported in the picture 5.18, by sweeping L_{shunt}, the third admittance is not changed (the light blue curves are almost parallel and superimposed each other) and so a variation in the load is still necessary to achieve a fine matching.

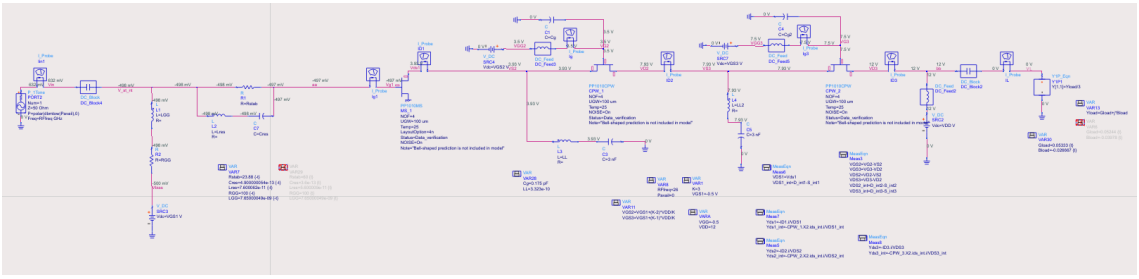


Figure 5.17: 3-stages Stacked amplifier with Shunt - Shunt InMN schematic

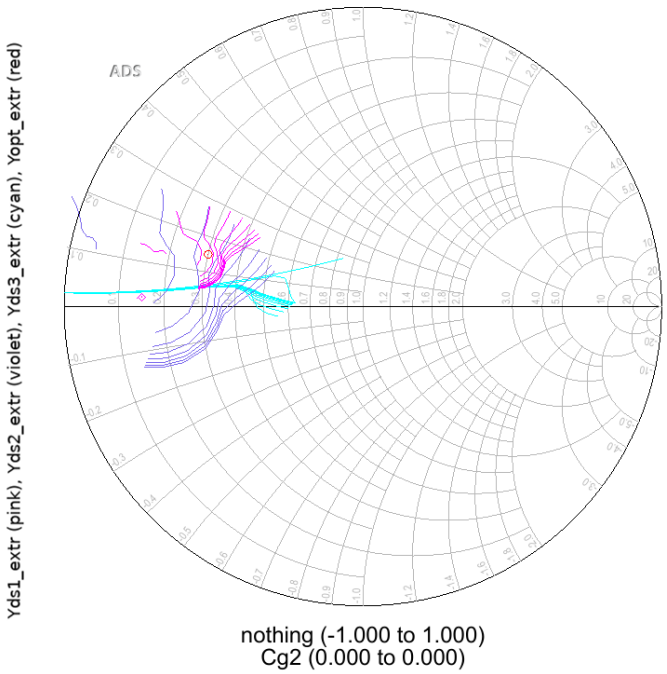


Figure 5.18: Extrinsic Y_{DSi} matching by L_{shunt} and C_{g2} sweeping

In particular by using values reported in table: 5.6 a good matching is achieved

L_{Shunt2}	C_{g2}	G_{load}	B_{load}
580 pF	80 fF	0.05224 S	−0.0397 S

Table 5.6: GaAs 3-stages parameters: shunt-shunt InMN

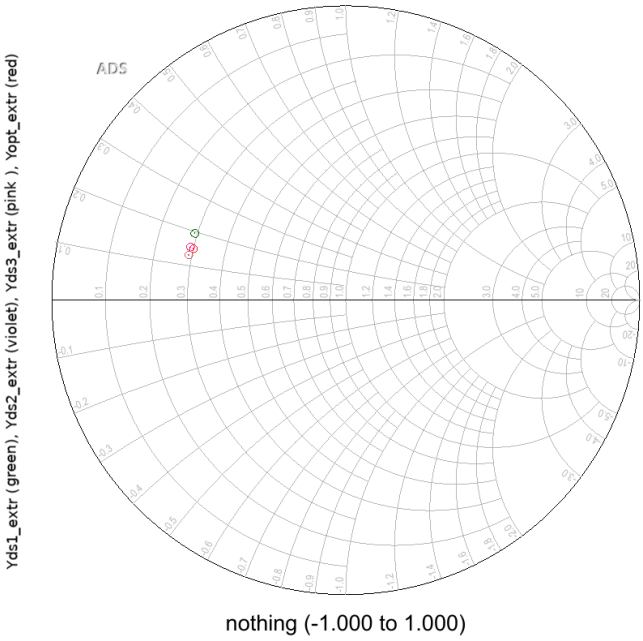


Figure 5.19: Extrinsic Y_{DSi} optimization through $L_{Shunt2} = 580pF$ and $C_{g2} = 80\,\text{fF}$

As for performance, differently from the GaN HEMT, the increase in gain and so in the output power between the second and the third stages, is not 1.8 dB as expected, but about 3 dB. With respect to a usual stacked amplifier, the variation of the load can be responsible for the cited P_{OUT} rise.

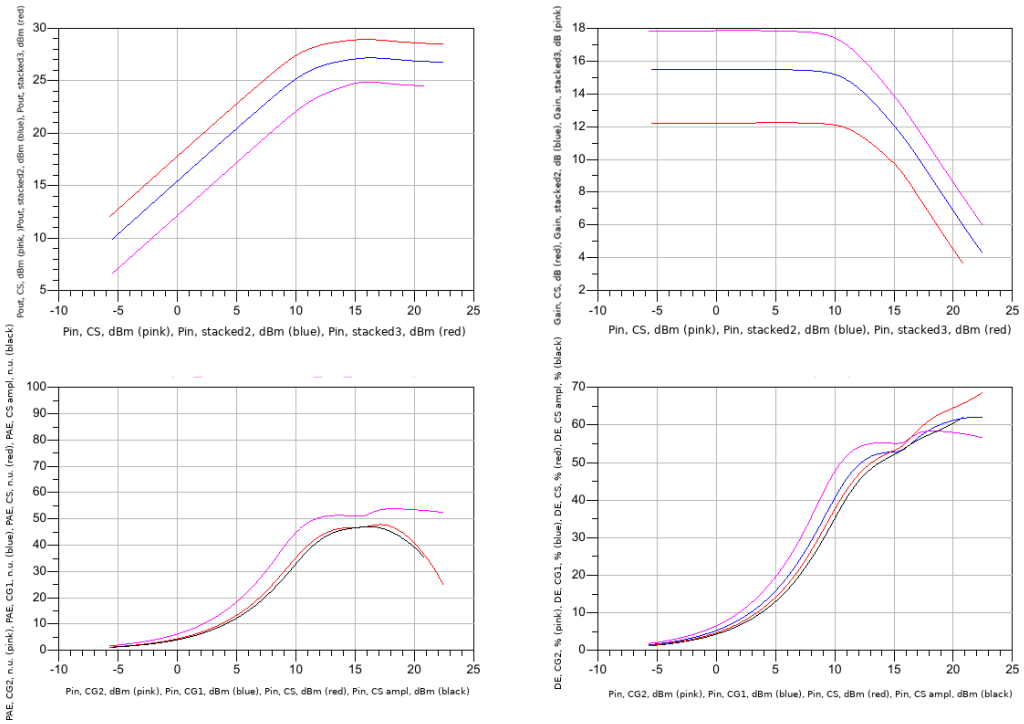


Figure 5.20: 3-stages Stacked amplifier performance with $L_{Shunt2} = 580\,\text{pF}$ and $C_{g2} = 80\,\text{fF}$: P_{OUT} (top left), Gain (top right), PAE (bottom left) and DE (bottom right)

PAE and DE are basically the same as a single CS stage.

As for the use of a series inductor and the feedback capacitance, the contemporary matching for all the three FETs is not possible even with a variation in the load. In the case of series inductor, the increase in L_{series} causes Y_{DS1} and Y_{DS2} to move closer to the wanted value, but the opposite happens for Y_{DS3}.
A similar effect can be observed in the case of the feedback capacitor.

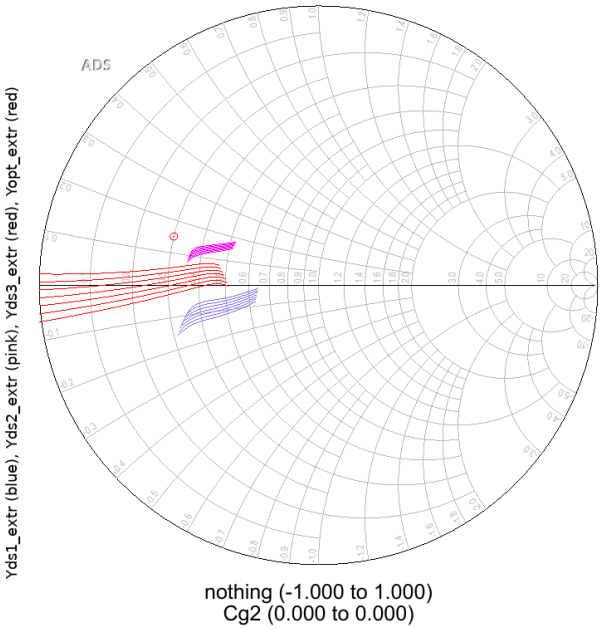


Figure 5.21: Extrinsic Y_{DSi} matching by series inductor sweep

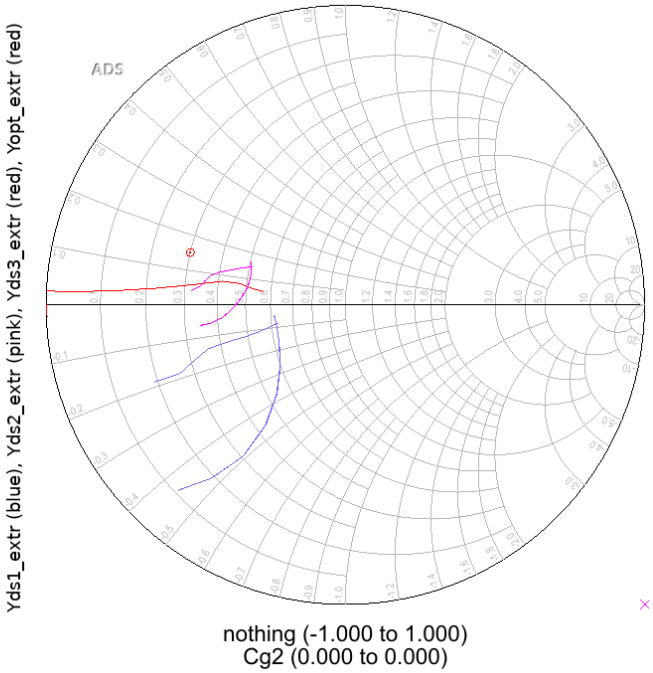
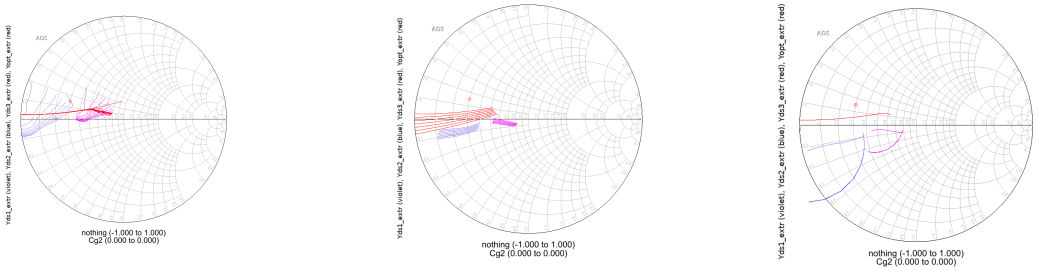


Figure 5.22: Extrinsic Y_{DSi} matching by feedback capacitor sweep

The use of a series inductance as a second stage matching does not lead to any significant

result, since, whatever is the other matching element (shunt inductance, series inductance or feedback capacitor), the obtained admittance is not simultaneously the wanted one for all the three FETs.
In the following figures simulation results are reported; when Y_{DS1} is matched, then Y_{DS2} will not be so. The variation of the load is not suitable for matching.



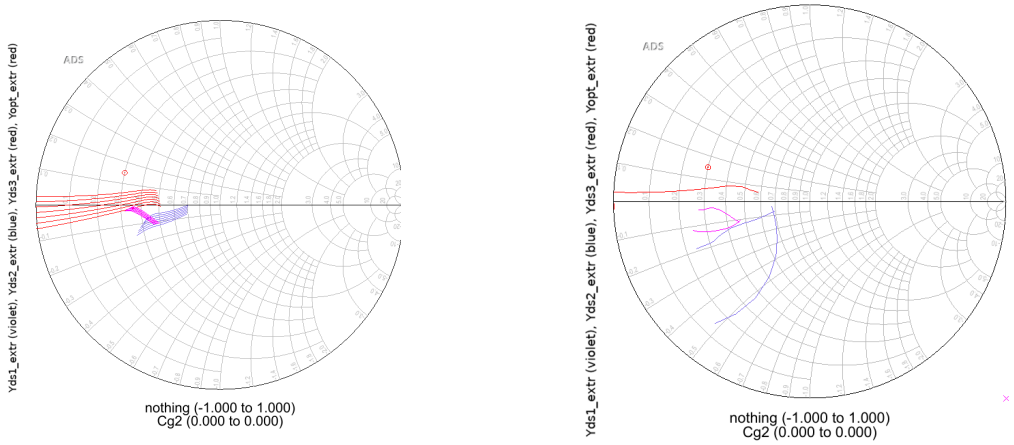
(a) series-shunt (b) series-series (c) series-feed

Figure 5.23: Extrinsic Y_{DSi} matching techniques

Finally, better matching results can be obtained trough the use of the feedback capacitor as a second stage matching solution.
Even if the feedback capacitor - series inductor and feedback capacitor - feedback capacitor configurations are again unsuccessful for matching, as shown in fig: 5.24, the use of a shunt inductor in the third stage seems to be a correct solution (fig: 5.25 and fig: 5.28). In the latter a variation in the load is still necessary:

L_{Shunt2}	C_{g2}	G_{load}	B_{load}
460 pF	146 fF	0.05350 S	−0.0449 S

Table 5.7: GaAs 3-stages parameters: feedback-shunt InMN



(a) feed-series (b) feed-feed

Figure 5.24: Extrinsic Y_{DSi} matching

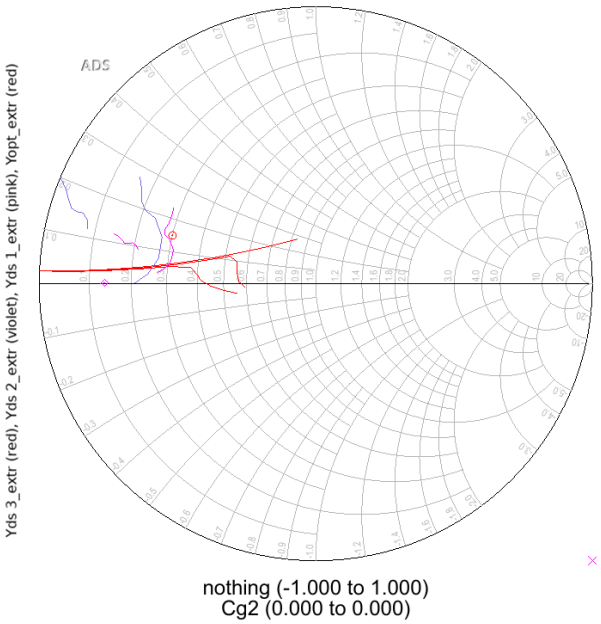


Figure 5.25: Extrinsic Y_{DSi} matching with feedback capacitor (1^{st} InMN) and shunt inductor (2^{nd} InMN); shunt inductor sweep

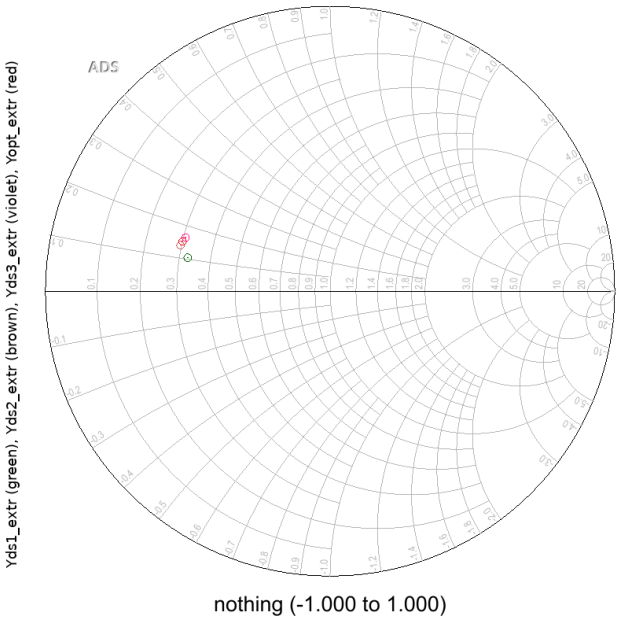


Figure 5.26: Extrinsic Y_{DSi} matching with feedback capacitor (1^{st} InMN) and shunt inductor (2^{nd} InNM); $L_{shunt} = 460\,\text{pF}$, $C_{g2} = 146\,\text{fF}$

As for performance, a 5 dB raise in gain between the second and the third stages is observed. This result is a bit larger with respect to the previous case, namely the shunt-shunt configuration and is again linked to a load variation, which improves inter-stage matching.

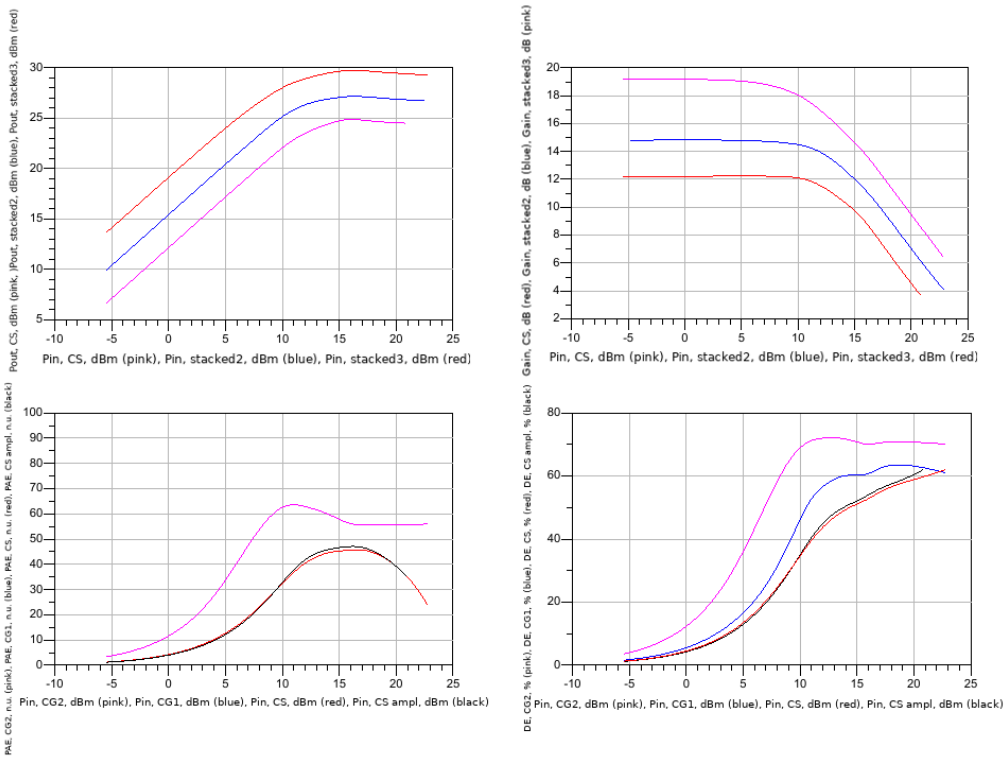


Figure 5.27: Feedback capacitor (1^{st} InMN) and shunt inductor (2^{nd} InMN) performance: P_{OUT} (top left), Gain (top right), PAE (bottom left) and DE (bottom right)

5.5.2 Stabilization

No variations are required when applying to the 3-stacked amplifier the stabilization network as reported in the following figure:

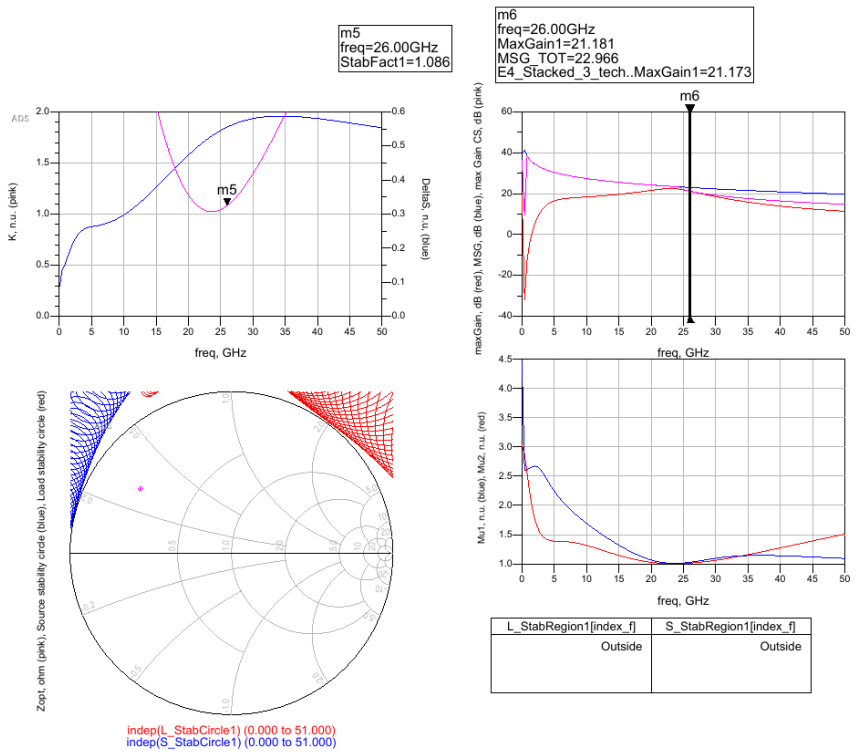


Figure 5.28: 3-stages Stacked amplifier stability performance: K and ΔS (top left) and Gain (top right); stability circles (bottom left); Mu and Mu1 (bottom right)

5.5.3 Bias network

In order to provide the proper biasing voltage to the three transistors, there are two main possibilities [**5**]:

- an independent biasing network for each Gate terminal, resulting into three different voltages to be provided from the outside;
- a single voltage, namely $V_{DD} = 12\,\text{V}$, which is reduced through voltage divisions to the wanted values.

The first approach will not be analyzed since requires a large number of sources.
A more interesting approach is reported in fig: 5.29:

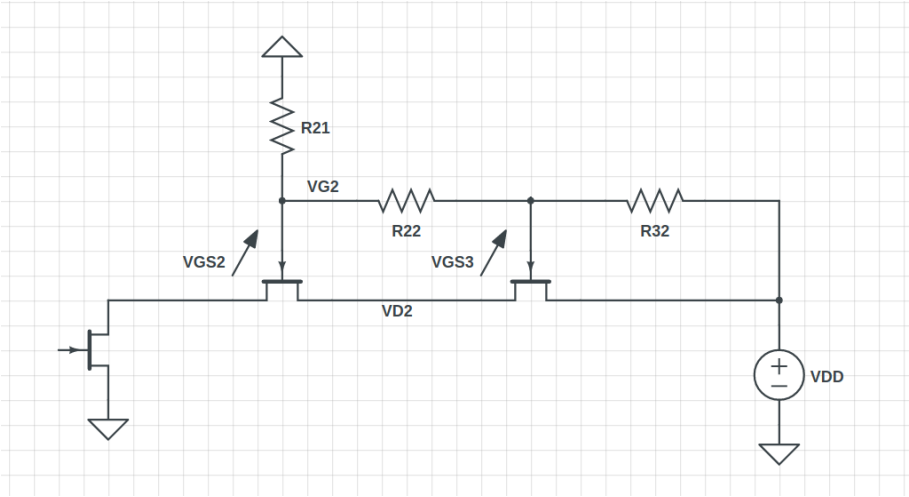


Figure 5.29: Self bias schematic (DC only)

In this case only resistive elements have to be added: thanks to the two voltage partitions, it is possible to impose that $V_{GS2} = V_{GS3} = -0.5\,\text{V}$, given $V_{D1} = 4\,\text{V}$ and $V_{D2} = 8\,\text{V}$. In particular the following equations can be derived, by considering ideal Gate terminal:

$$V_{GS2} = V_{G3}\frac{R_{21}}{R_{21} + R_{22}} - V_{D1}$$

$$V_{GS3} = V_{DD}\frac{R_T}{R_T + R_{32}} - V_{D2}$$

where $R_T = (R_{21} + R_{22})$.
The two equations result in

$$R_{22} = R_{32} \times 0.8889$$

$$R_{21} = R_{32} \times 0.777$$

The initial hypothesis is $R_{32} = 2400\,\Omega$ ($2393.68\,\Omega$ achieved with real technology resistors), so that the current flowing in the bias network is negligible with respect to the Drain one. As a result $R_{22} = 2130\,\Omega$ ($2134.43\,\Omega$ with real technology resistors) and $R_{21} = 1875\,\Omega$ ($1875.18\,\Omega$ with real technology resistors).
Taking a look at the simulations with this configuration, the effective current flowing in the network results to be 1.83 mA in correspondence of R_{32}. The obtained current seems acceptable since as said is much smaller than the Drain one, namely 93.6 mA.

Chapter 6

Layout - GaAs

In order to approach the layout of the Stacked amplifier, it is firstly necessary to replace ideal components with the ones provided by the foundry, which are physically achievable in such a technological process. Obviously since the devices are now real, they will not show an ideal behavior, so that for example capacitors' measured impedance will have a real part too; moreover it will show inductive effects.
In the following sections different components are described.

6.1 Real elements

6.1.1 Resistors

Thin film resistors are available in the library, showing a resistance of $50\Omega/\square$. An increase in the maximum current which can flow through the line is obtained by connecting and using the two metal layers.
In the stabilization network a Thin film resistor (TFR) is used, since the wanted value is about $23\,\Omega$ and these kind of resistors are limited to low resistance ranges. On the other hand MESA resistors are exploited for higher values and will be used for the self bias network.

6.1.2 Capacitors

Foundry' library includes two types of capacitors: even if both exploit two metal layers (MET1 and MET2), CAPA shows a two floating terminals, while COV has a termination connected to a back-via.
By properly tuning the physical dimensions of the capacitor, its actual capacitance is changed and compared with the wanted one. When designing the shape it should be kept

into account that a squared layout is preferable with respect to a rectangular one, so to reduce inductive parasitic effects.

6.1.3 Shunt networks

As for lumped inductors the foundry proposes two layouts: the rounded and the squared ones. Moreover a microstrip can be used for the same purpose.
However, taking a look at the wanted inductance values, the line results to be too long and so space consuming. Besides the squared inductor is preferable since can be made more compact than the rounded one.

6.1.4 Stabilization network

The Stabilization network (right section only) is physically made as shown in fig: 6.1. With respect to the ideal case

- the inductive component is obtained through lines;
- Tees and corners are accounted for the real layout result.

Even if the structure is more complicated than before, all these elements' parameters can be designed to obtain a proper stabilization of the device.
As shown in the following sections the use of such a network causes a gain loss of $\sim 1.5\,\mathrm{dB}$ with respect to the ideal case.

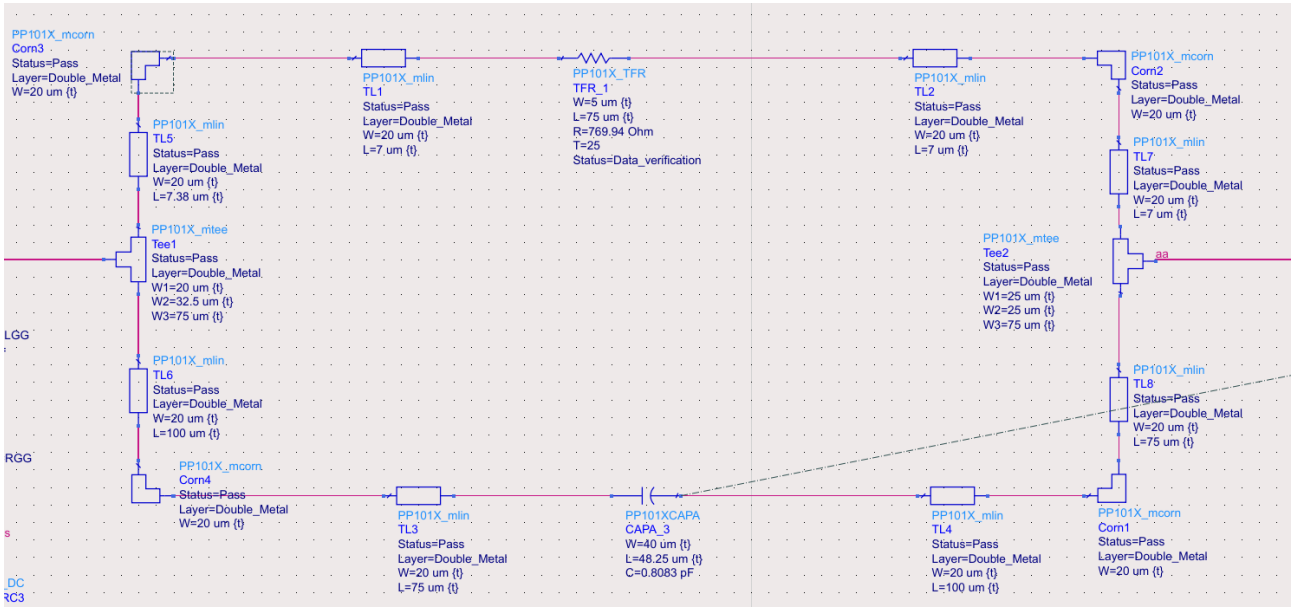


Figure 6.1: Real stabilization network schematic

Taking now into account the whole 3-stages Stacked amplifier, the stability network is tuned so to fulfill its role: the presence of lines and corners causes unwanted reactive effects which have to be considered. In particular the stability factor results not to be larger than 1 for a small frequency range ($\sim 20\,\text{GHz}$).
An increase in the resistance could improve the stability factor but it would also lead to an unwanted increase in gain losses. A good compromise is reported in fig: 6.2 in which it is clear that $K > 1$ for the whole frequency range; moreover stability circles show that both the load and the Source impedances can fall in each point of the Smith Chart.

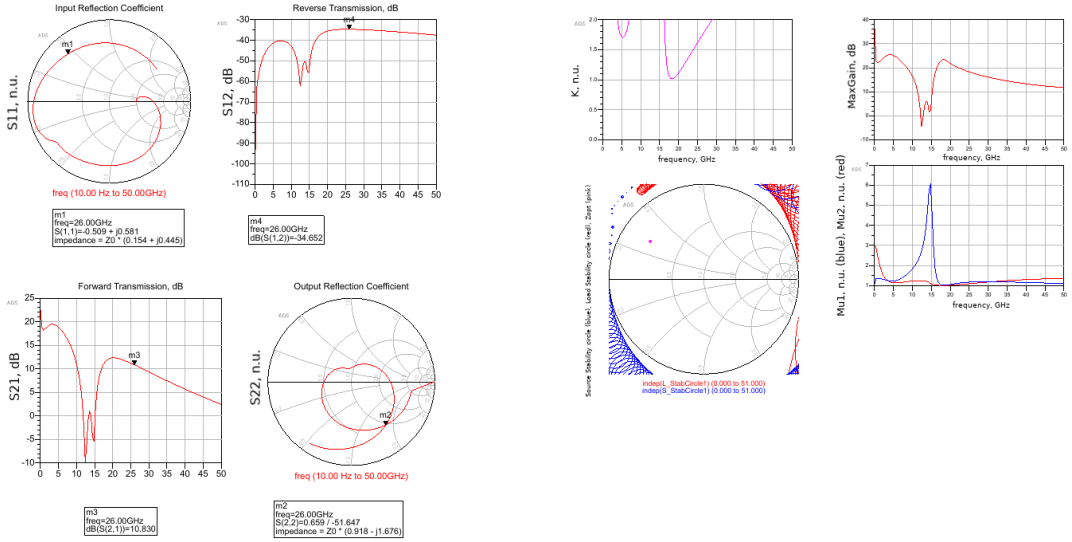


Figure 6.2: Real 3-stages Stacked amplifier performance: S-parameters (left plots) and stability parameters (right plots)

As for performance, fig: 6.3 shows a gain reduction of $\sim 1.5\,\text{dB}$ with respect to the ideal case, for low input power values.

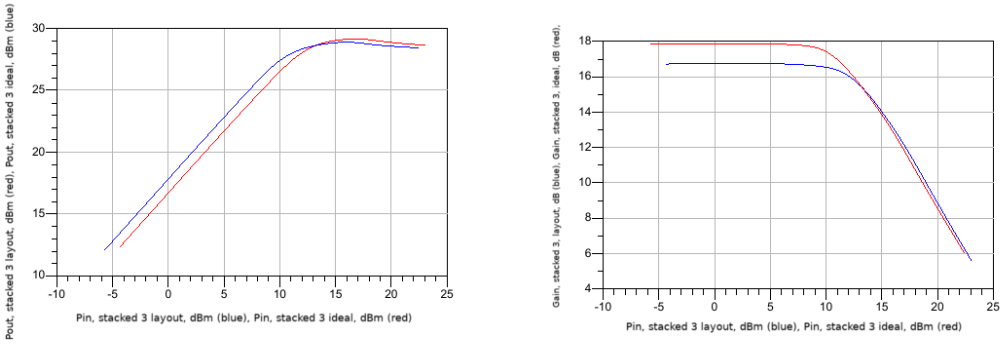


Figure 6.3: Real 3-stages Stacked amplifier performance: P_{OUT} (left), Gain (right)

The previously studied stabilization network will not used, due to high losses linked to its insertion, but a new one is designed, so to satisfy two requirements: unconditional stability over the whole frequency domain and low gain (and so output power) losses. The schematic representation is below reported; fig: 6.5 is the resulting layout structure.

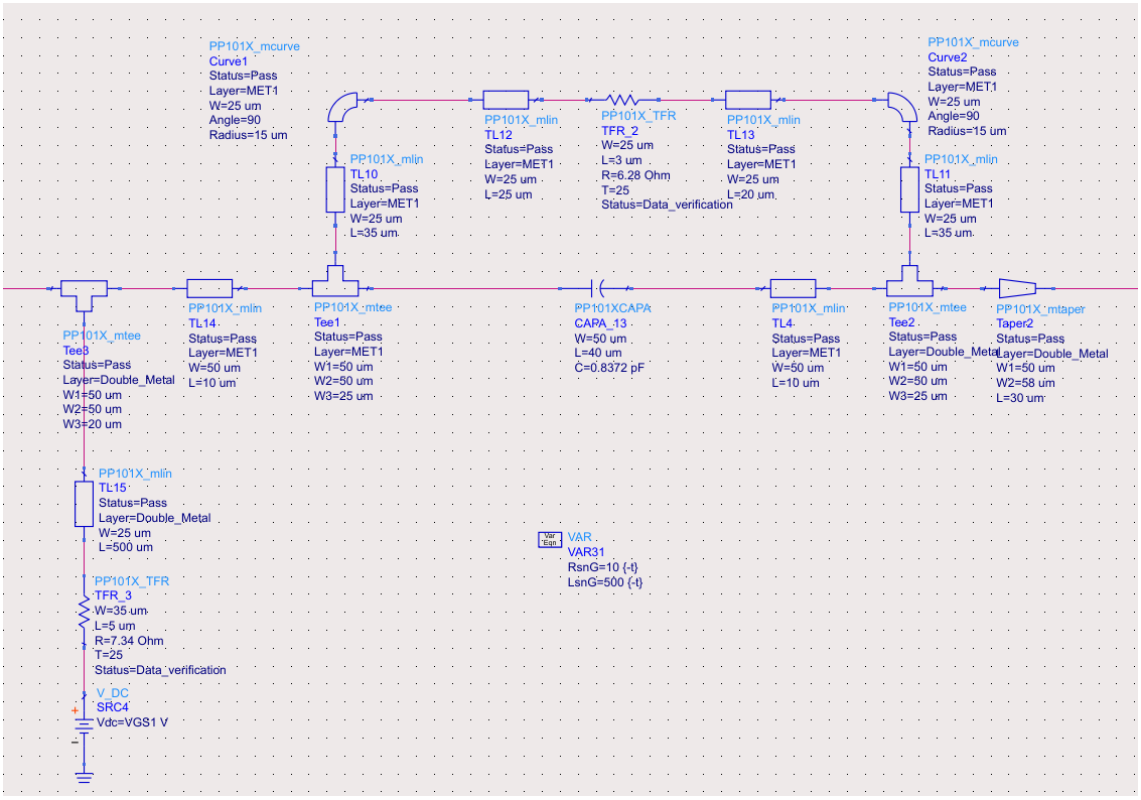


Figure 6.4: New stabilization network schematic

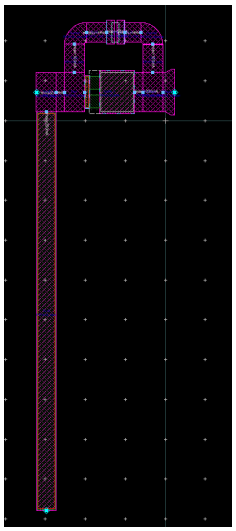


Figure 6.5: New stabilization network layout

A significant improvement in performance can be observed with respect to the previous network: the new one allows for a reduction of gain to 17.6 dB (fig: 6.6); consequently losses are about 0.25 dB. The upper plot shows a quite good inter-stage matching for all the three stages, even if it will be improved in the following sections.
Furthermore the device results to be unconditionally stable as shown in fig: 6.7.

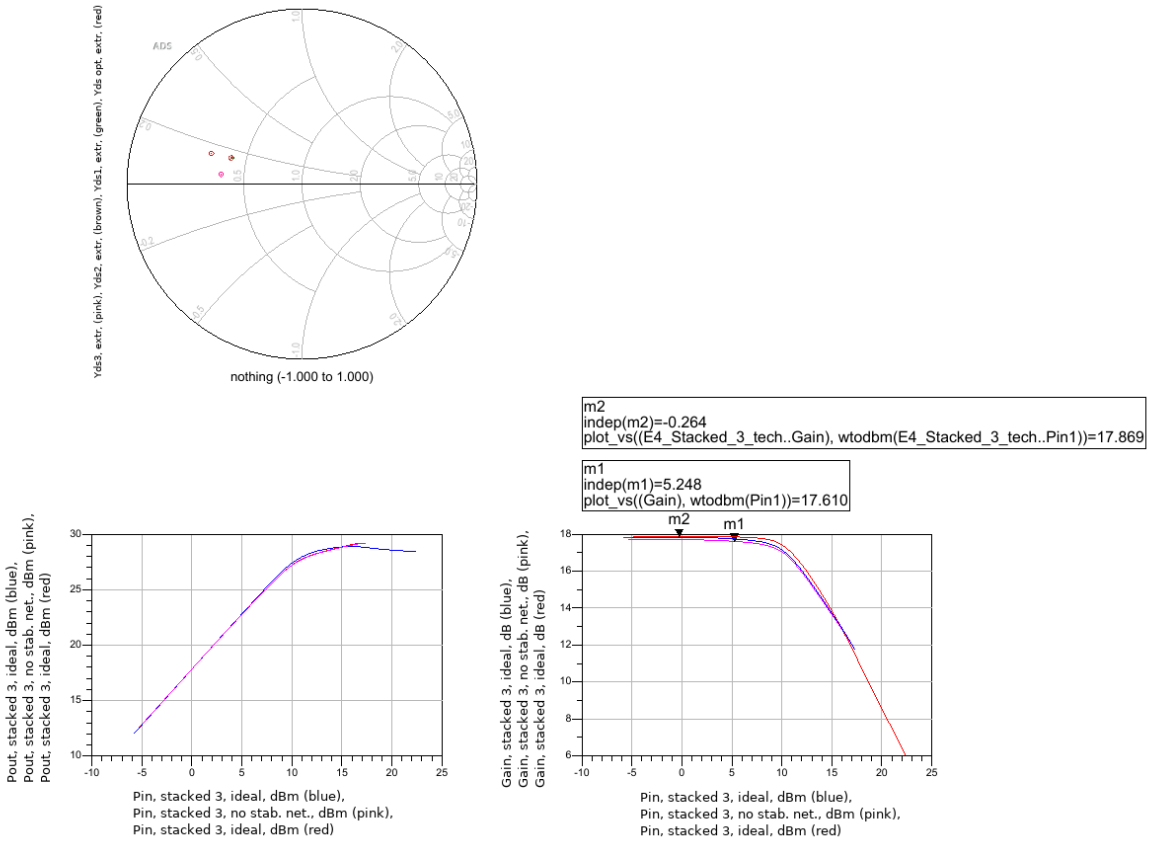


Figure 6.6: Stabilized Stacked performance comparison: Y_{DSi} matching (top);P_{OUT} (bottom left); Gain (bottom right)

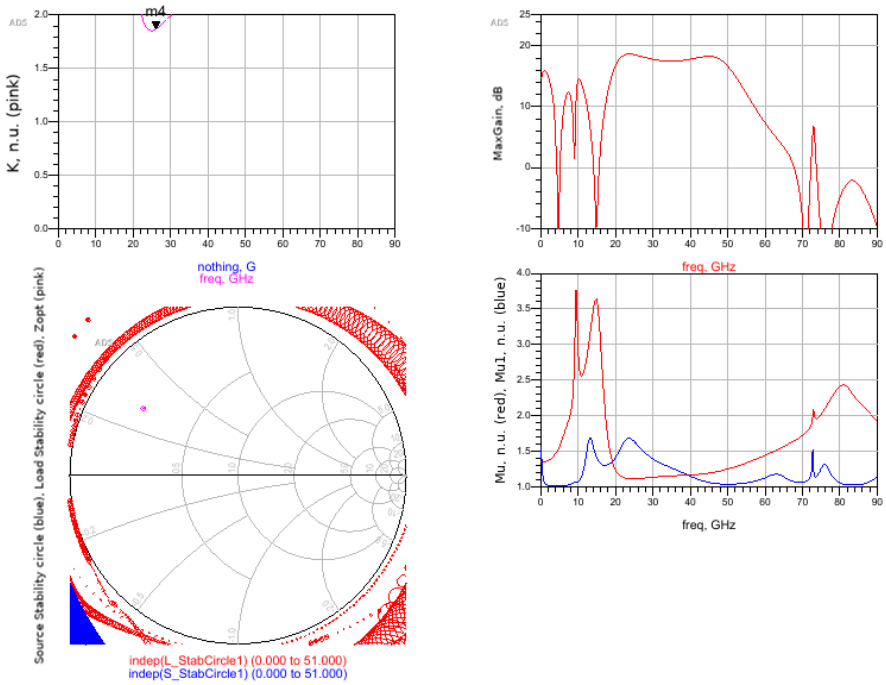


Figure 6.7: Stabilized Stacked performance: K and ΔS (top left) and Gain (top right); stability circles (bottom left), Mu and Mu1 (bottom right)

6.1.5 Output matching network

The optimum load, computed in the previous section, made up of a real and an imaginary part, is definitely not the actual termination which will be connected to the amplifier in a real case use. What is more probable is to have a $50\,\Omega$ termination; this impedance has so to be converted into the optimum one, namely $\frac{1}{3}(52 - j27)\,\mathrm{mS}$, being placed after the third stage, through the use of a matching network.

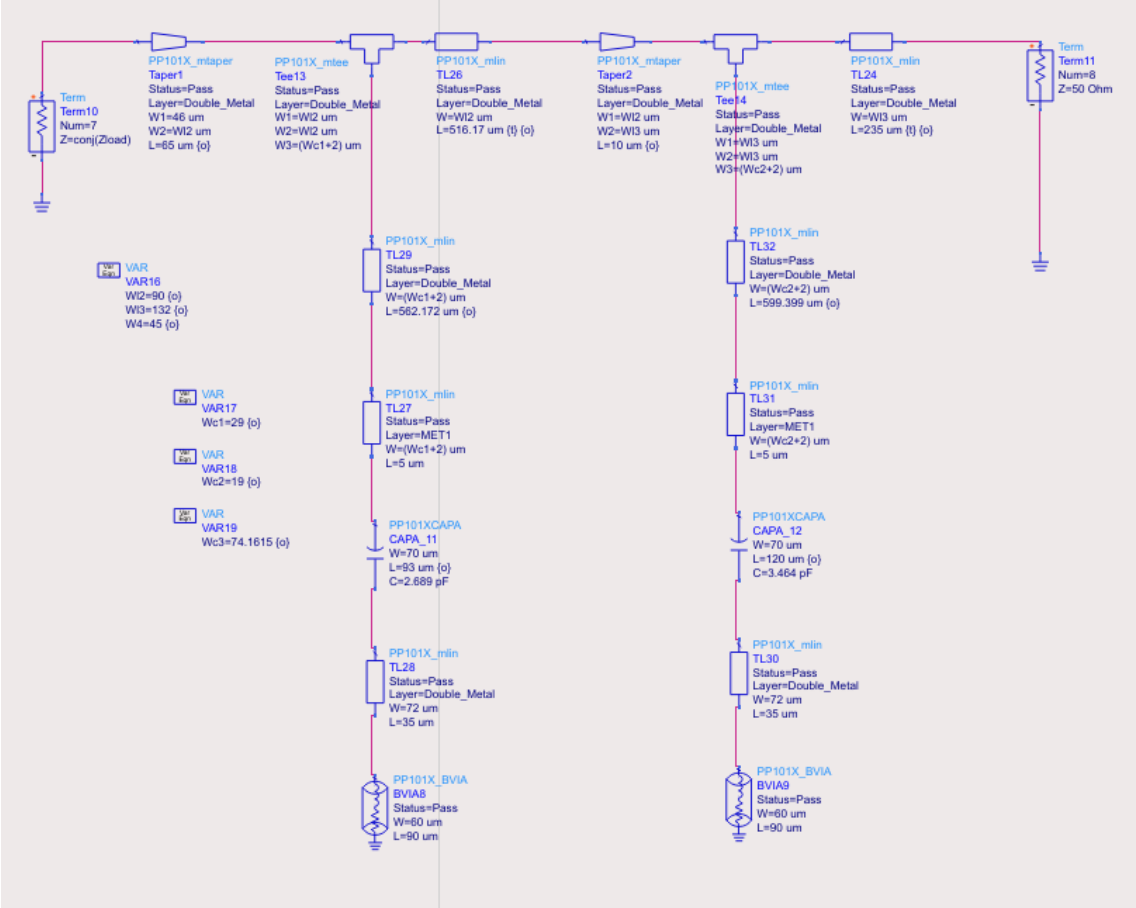


Figure 6.8: Real Output matching network schematic

In fig: 6.8 PORT1 is set to the complex conjugate of the wanted load, so that when the impedance shown by the network is exactly Z_{LOAD}, $S11$ results to be null (in linear units). On the other hand PORT2 is a standard $50\,\Omega$ load.

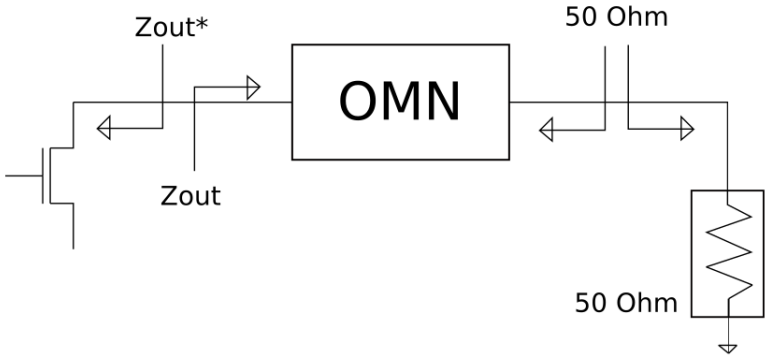


Figure 6.9: Output matching network principle schematic

The simple matching network based on a two line-stub (L network) is not sufficient alone, since an increase in bandwidth causes lines' length to increase too much, resulting to be totally unsuited with respect to the amplifier. The solution is to add other L networks in cascade with the first one; in particular properly optimized simulations show quite no differences between the use of two and three shunts, so the minimal element solution is chosen.
From fig: 6.10, bottom plot, the $S11|_{\mathrm{dB}}$ parameter, representing the input reflection coefficient, should be as close as possible to 0 in linear units; in the useful frequency range 24 GHz−29 GHz, $S11$ reaches very low values, namely < -20 dB at the borders and -40 dB at the working frequency.

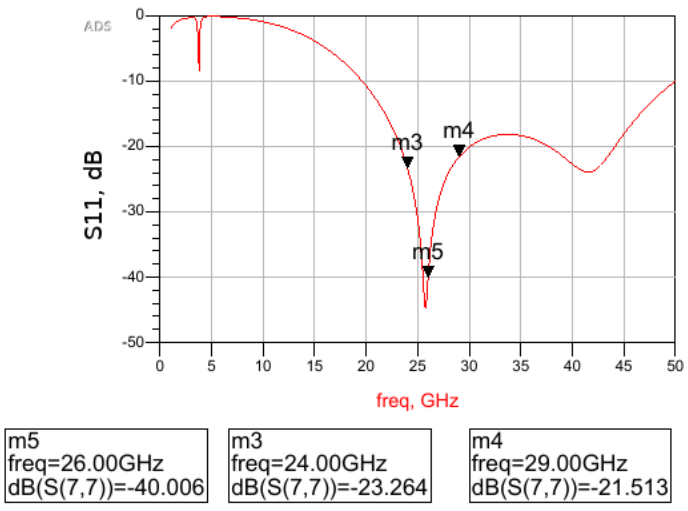


Figure 6.10: Matching Bandwidth

The presence of a capacitor CAPA replacing one of the two stubs (fig: 6.8) is due to the fact that the same result, employing the line, would have required it to be too long. Moreover the taper at the beginning of the matching network is linked to the physical structure in the layout: taper's input size which is equal to FET's Source terminal is converted into following lines' actual size.

Finally in fig: 6.11 it is reported the layout:

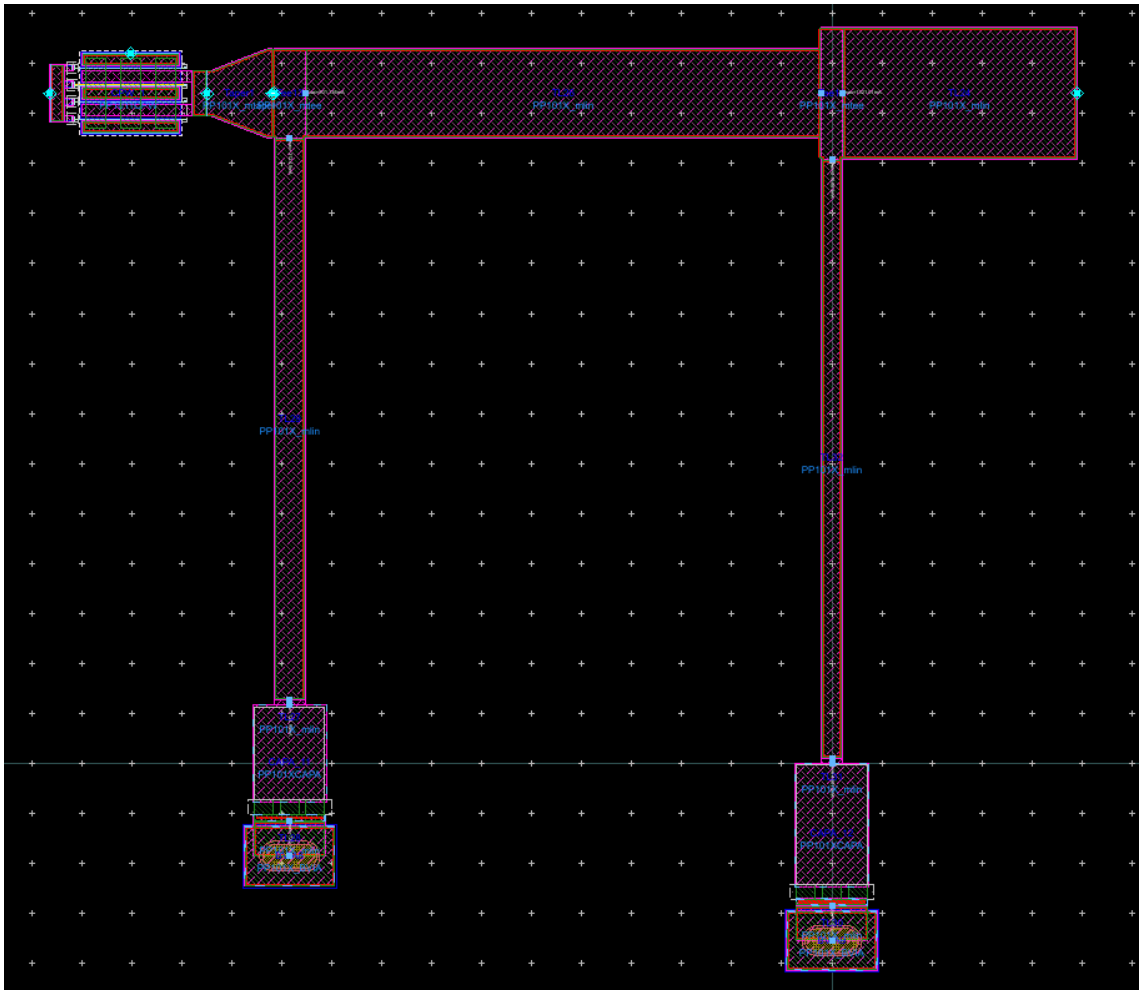


Figure 6.11: Output matching network layout

Another important thing to do is to replace the ideal DC_BLOCK with a real one: it will be a series capacitor, large enough to behave like an ideal one. In particular it is chosen a 4.12 pF, namely 100 um $\times$ 100 um.

6.1.6 3-stages Stacked amplifier

An effect of the introduction of real lines is an inter-stage matching worsening; it can be corrected by manually tuning the actual value of the two shunt lines. The result is reported in fig: 6.12:

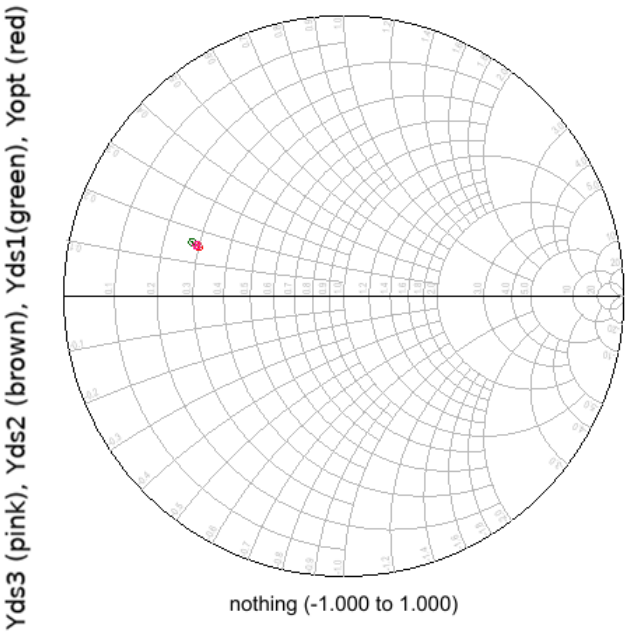


Figure 6.12: Real 3-stages Stacked amplifier extrinsic matching performance with OMM

Let's now concentrate on a more realistic structure by inserting lines among each FET couple, replacing the ideal wire; in order to properly analyze the layout structure also bends are inserted. The actual size (width and length) is measured by placing components and drawing connections between them which could guarantee compactness in the structure but also physical achievability.
Moreover lines are used to connect resistors, inductors and capacitors.

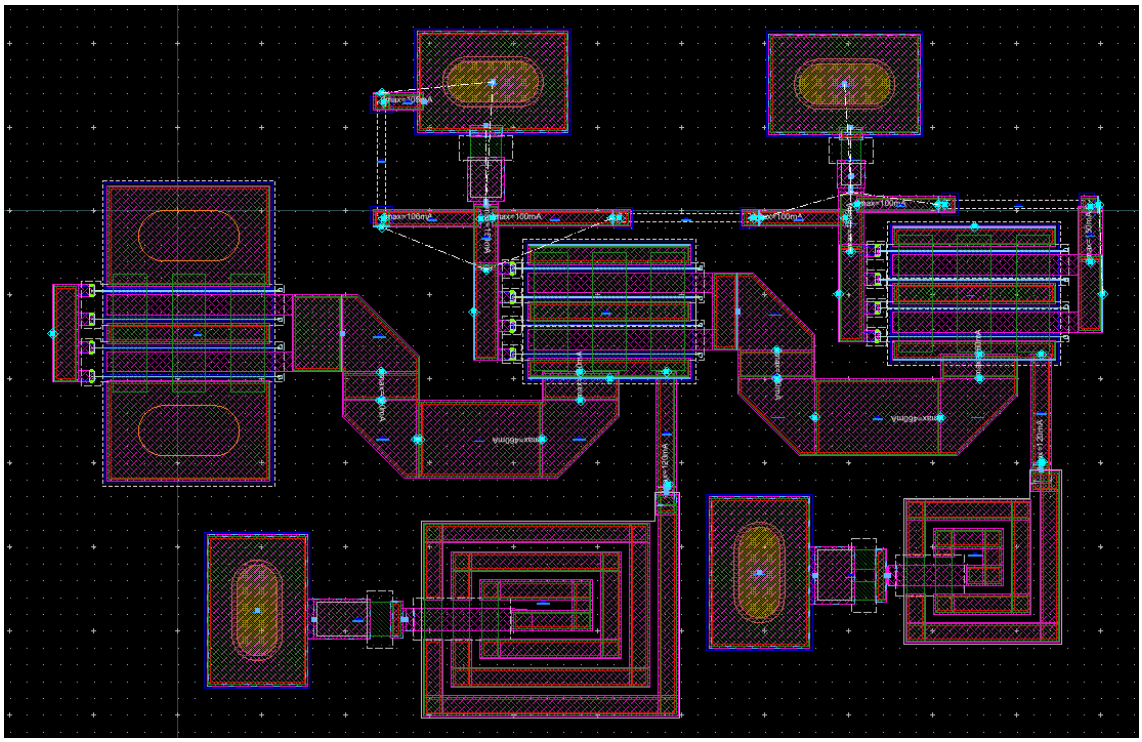


Figure 6.13: Real 3-stages Stacked amplifier layout

As shown in fig: 6.13 it was chosen to use just a single Source terminal, instead of using a symmetrical solution; this way symmetry is traded with compactness and cross-talk immunity [5]. In the first case each component should have been duplicated, taking into account that each of them would have been placed in parallel to the other one, causing an halving of every component. Another thing to be noted is the use of squared inductors and capacitors with two floating terminals.
The use of real lines causes, as previously explained a reactive effect and so shunt inductors and Gate capacitors have to be tuned so to better fit the new structure in terms of inter-stage matching and performance.
The whole schematic is reported in the figure below:

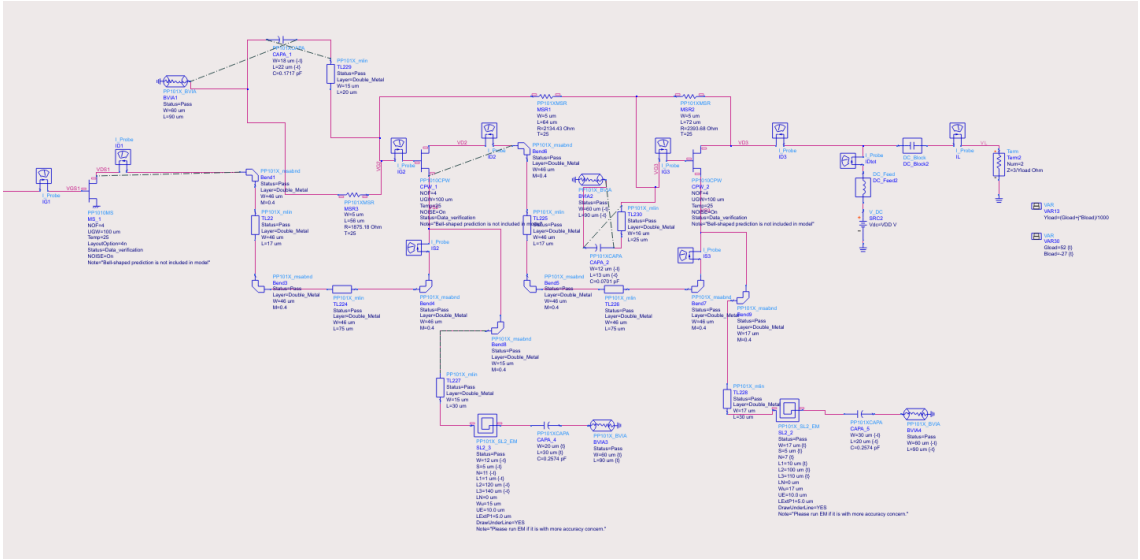


Figure 6.14: Real 3-stages Stacked amplifier schematic

Even if this new configuration does not allow for a perfect inter-stage matching (fig: 6.15 on the Smith Chart all the Drain-Source impedances are quite far away from the optimum one), the obtained performance are satisfactory, leading to a 0.07 dB loss in gain and output power.
On the other hand PAE and DE are a bit lower for the CS and CG2 stages.

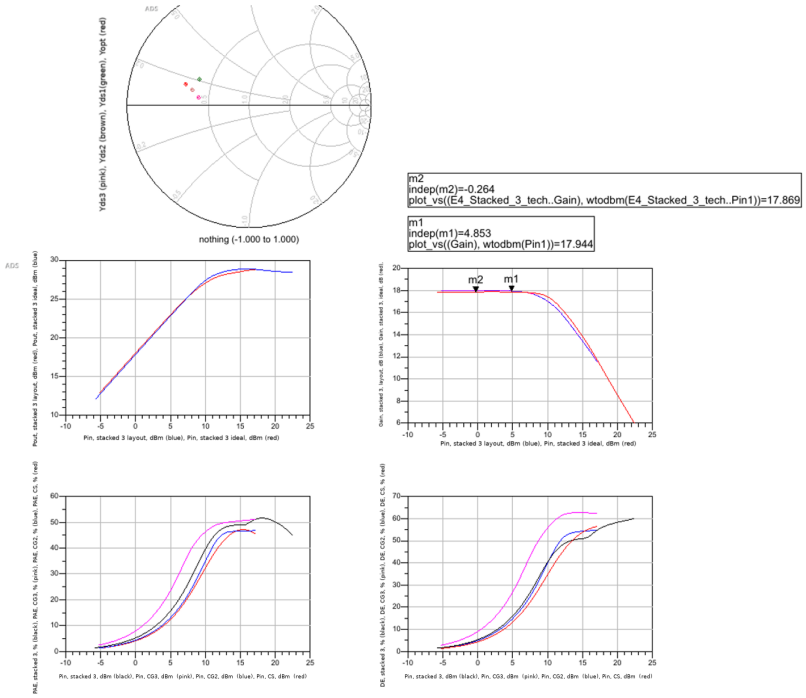


Figure 6.15: Real 3-stages Stacked amplifier performance: Y_{DSi} matching (top); P_{OUT} (top left), Gain (top right), PAE (bottom left) and DE (bottom right)

The insertion of the output matching network does not cause a significant variation in performance; fig: 6.16 compares output power and gain with and without the network (blue and pink curves). It is clear that the two curves are superimposed each other.

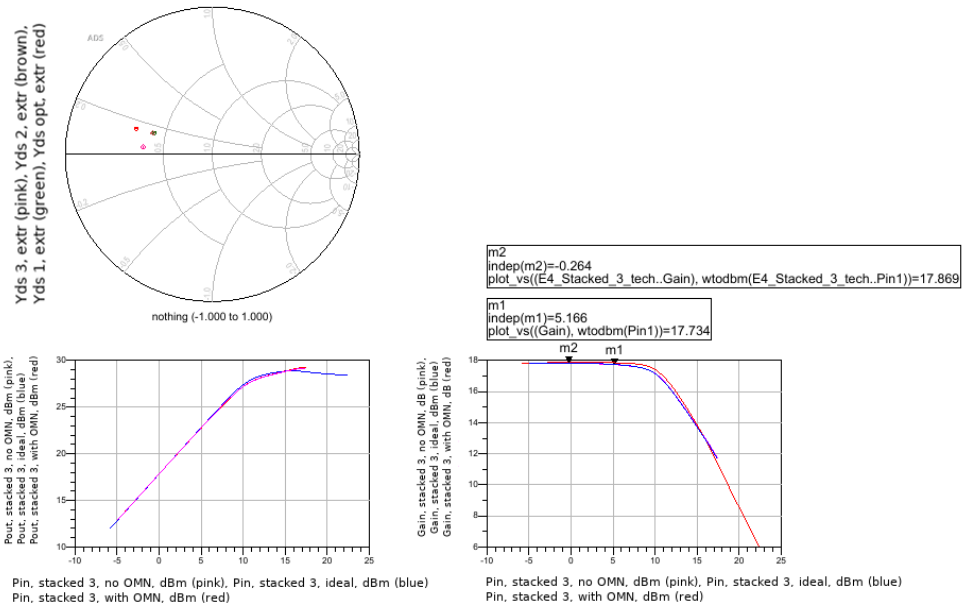


Figure 6.16: Real 3-stages Stacked amplifier performance with OMN:Y_{DSi} matching (top); P_{OUT} (bottom left), Gain (bottom right)

6.1.7 Input matching Network

Once all the other networks are designed, it will be possible to create the input one, too. The overall input impedance is measured as:

$$Z_{in} = \frac{V_{in}(f_0)}{I_{in}(f_0)}$$

This value slightly changes as the input power sweeps, so it will be necessary to choose the value associated to the working input power, namely in correspondence of the compression; it happens at $\sim 13\,\text{dBm}$ leading to an input impedance of $(4.73 - j0.82)\,\Omega$.
The use of small signal parameters (S to Z conversion) would not have been fully comprehensive of amplifier's input power behavior.
The optimized circuit used for matching is reported in the following image:

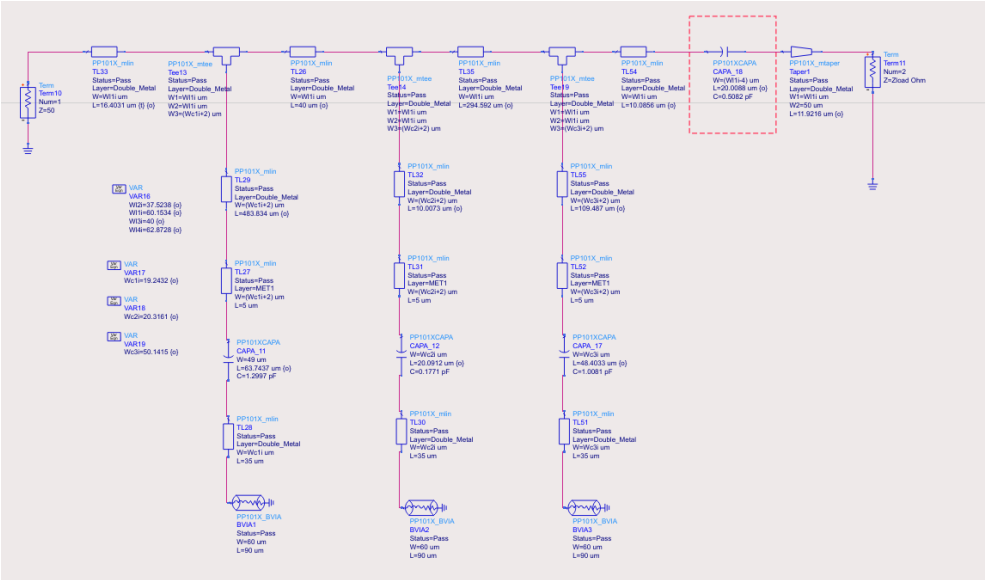


Figure 6.17: Input matching Network

In fig: 6.17 it was highlighted the series capacitor: it is the real component which replaces the DC_BLOCK in the ideal schematic. It should be large enough to act as an ideal component, but since every capacitor acts like an open circuit for the DC, it is designed as a matching network element.
The real DC_BLOCK could be placed both at the end and at the beginning of the input matching network, but by simulating its behavior, it was seen that in the first case, the following line would have been much longer than in the second one.
As comes out from the simulation, in the $(24-29)$ GHz band, the input reflection coefficient is lower than -20 dB, leading to a proper matching.

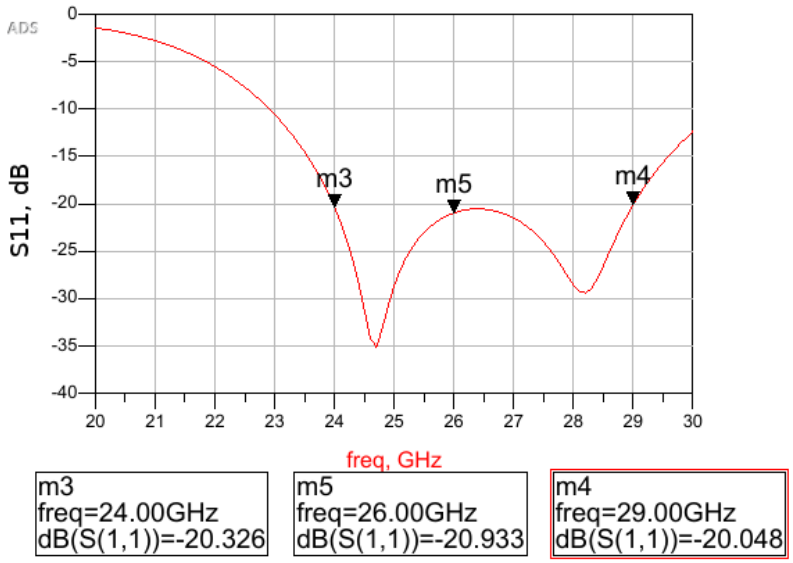


Figure 6.18: Input matching Network performance in terms of bandwidth

Finally fig: 6.19 represents the final layout of the matching network:

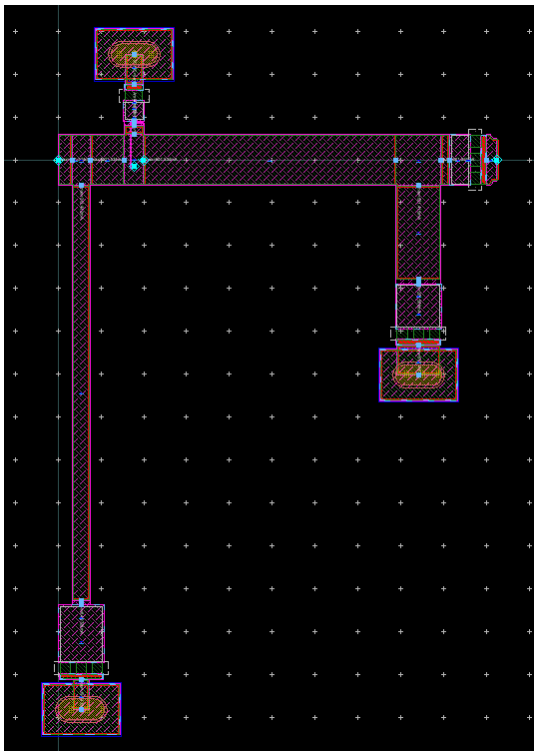


Figure 6.19: Input matching Network layout

Let's now take a look at what happens to the whole amplifier when the new network is applied, as reported in fig: 6.20.
The output power seems to be unchanged as the curves are superimposed, while gain shows a reduction of about 0.5 dB (red curve), which could be due to the insertion of new non-ideal components.

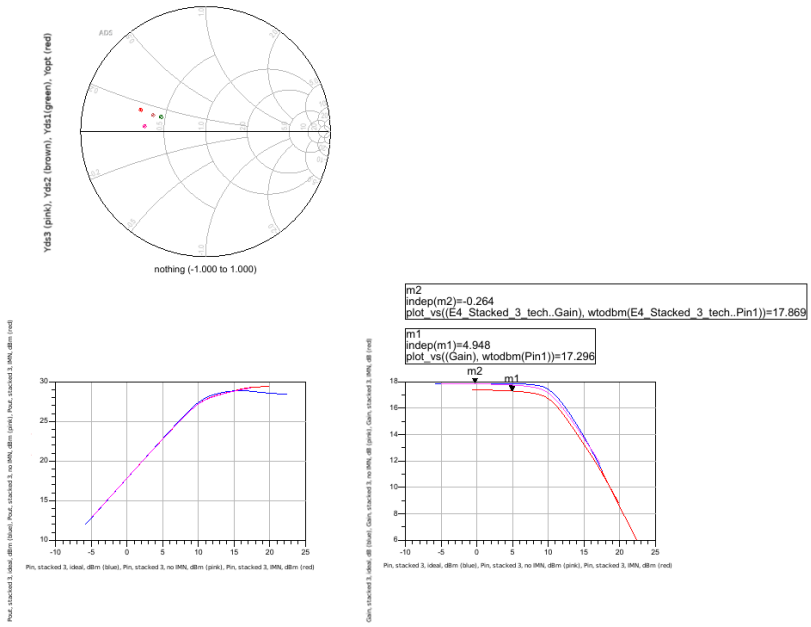


Figure 6.20: Real stacked amplifier performance with OMN and IMN: Y_{DSi} matching (top); P_{OUT} (bottom left), Gain (bottom right)

6.2 Biasing Circuit

As for the Common Source stage, it has to be fed by an external Source, which was represented, for simplicity, with an ideal voltage generator in the previous sections. However, it was a too simplified hypothesis since the ideal generator is followed by non-ideal components, such as wires, transitions, etc.. In order to face this problem, a buffer capacitor, which keeps all the possible disturbances away from the amplifier, can be inserted. The capacitor is DC charged from the outside, by connecting the probe to a specific PAD.

The buffer capacitor will be the core of the biasing circuit (in the following "Cooling Circuit") which guarantees that whatever is connected after it, behaves like a short circuit ($\Gamma_{TARGET} = -1$), in band. Instead, for the other frequencies, it should be basically "transparent", meaning that it will not interfere, with the rest of the circuit.
The circuit reported in fig: 6.21 will be connected to stabilization network's resistor by PORT1. On the other hand PORT2 is used to represent the actual feeding PAD.
The basic circuit only involves the first TEE and its capacitive shunt toward GND, while the rest makes the structure wide-band and implies the insertion of other large capacitors. The first capacitor is used to guarantee a short circuit in-band, since it is much smaller than the other ones; the latter, on the other hand, impose a unitary reflection coefficient for lower frequencies.

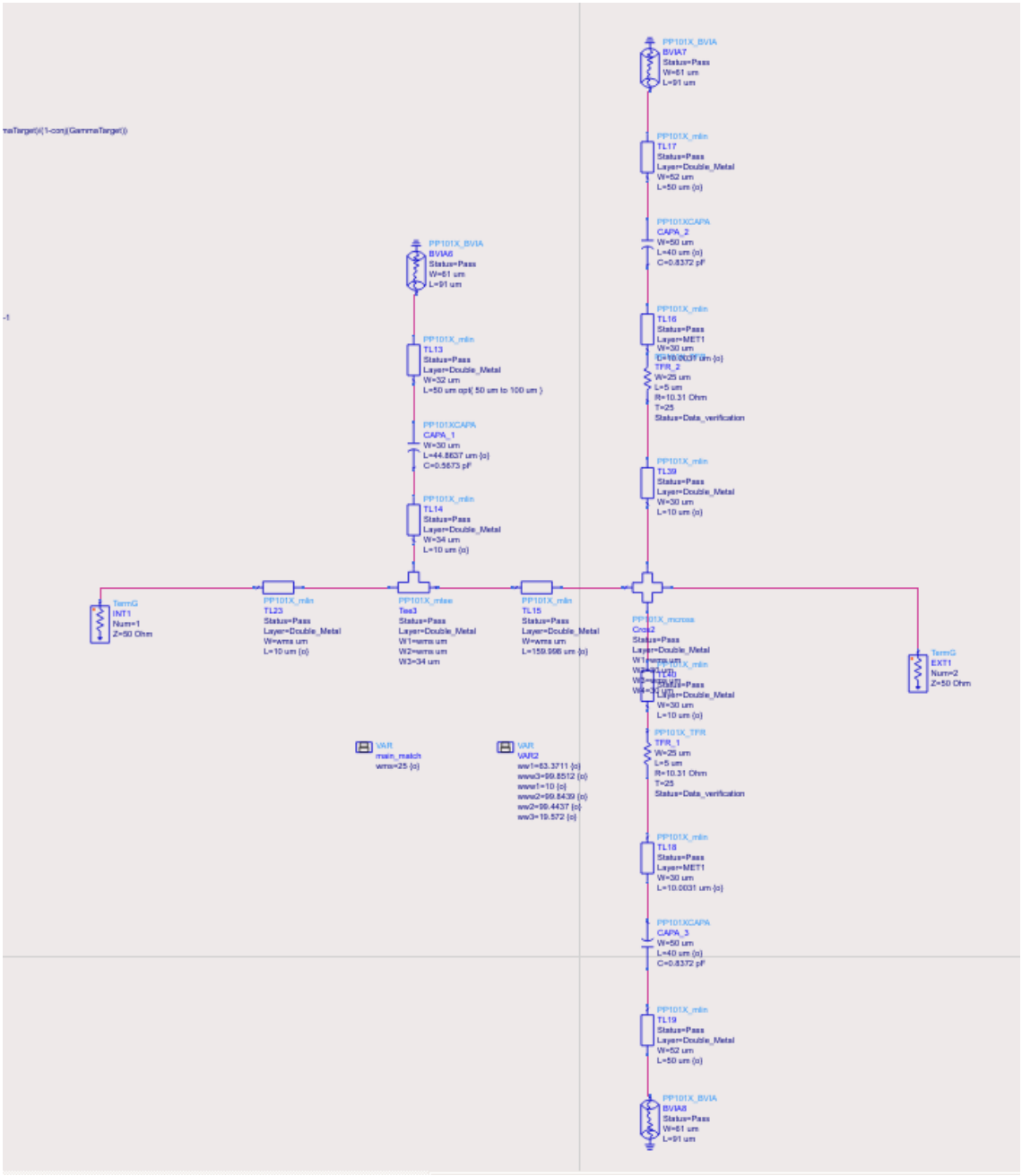


Figure 6.21: Biasing Circuit schematic

The idea behind the performed analysis is to map PORT2's reflection coefficient (Γ_L) on the Smith Chart; such a coefficient will be represented as a circumference as known from theory.

The cooling circuit, which is placed between the two PORTs causes a transformation of

the actual Γ_L, when observed from the input PORT, according to its S-parameters.

$$\Gamma_{in}(\Gamma_L) = \frac{S11 - \Delta \times \Gamma_L}{1 - S22 \times \Gamma_L}$$

As usual $\Delta = S11 \times S22 - S12 \times S21$.
The previously cited transformation is a conformal mapping between two complex planes, which, given a circumference with radius R and center C, generates the conformal circumference (R', C') and vice-versa.
In particular in the following, starting from a circumference (R', C') it is computed the corresponding one, seen from the input PORT (R, C).By imposing $R' = 1$ and $C' = 0$, the new center is defined as

$$C = \frac{S11 - \Delta \times conj(S22)}{1 - |S22|^2}$$

Moreover, given the radius associated to Γ_{in} plane,

$$R = \left| \frac{S12 \times S21}{1 - |S22|^2} \right|$$

(C, R) can be shown to be a circle plus its internal or external region.

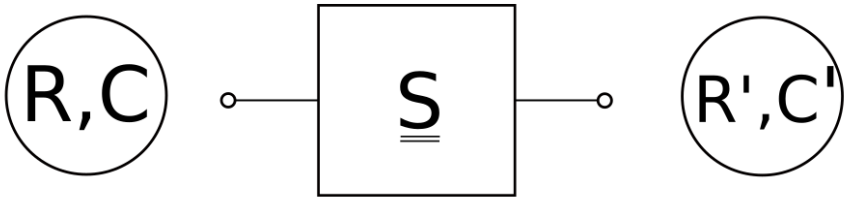


Figure 6.22

As previously said the target reflection coefficient is set to -1 and the error with respect to it is computed and quantified in terms of $C - \Gamma_{TARGET}$.
The maximum error in the reflection coefficient is linked to the distance between the target coefficient and the center of the actual one; being it a circumference, it is also necessary to take into account for the radius.

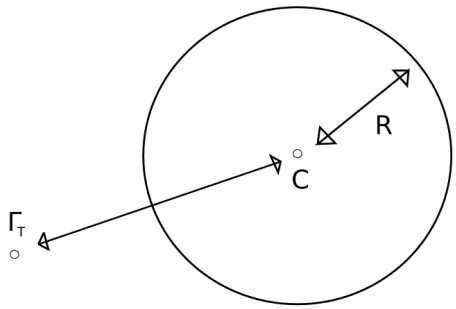


Figure 6.23

The error, in terms of absolute values, is so defined as:

$$\Gamma_{err}^{max} = R + |C - \Gamma_{TARGET}|$$

On the other hand the minimum error is

$$\Gamma_{err}^{min} = | - R + |C - \Gamma_{TARGET}||$$

Taking now into account complex quantities, it is possible to define both the best and worst obtainable reflection coefficients as follows:

$$\Gamma_{BEST} = C - R \times e^{j\angle(C-\Gamma_{TARGET})}$$

$$\Gamma_{WORST} = C + R \times e^{j\angle(C-\Gamma_{TARGET})}$$

Another reflection coefficient which can be computed is Γ_{WORST}^{L}, that is basically previous one but reported on PORT2, through the S-matrix. It could be useful to verify which loads are associated to the worst reflection coefficients.
Starting from the reflection coefficient transport formulae:

$$\Gamma_{in} = S11 + \frac{S12 \times S21 \times \Gamma_L}{1 - S22 \times \Gamma_L} \quad where \quad \Gamma_L = \Gamma_{WORST} \quad and \quad \Gamma_{in} = \Gamma_{WORST}^{L}$$

$$\Gamma_{WORST}^{L}(\Delta - \Gamma_{WORST} \times S22) = S11 - \Gamma_{WORST}^{L}$$

$$\Gamma_{WORST}^{L} = \frac{\Gamma_{WORST} - S11}{\Gamma_{WORST} \times S22 - \Delta}$$

Finally it is possible to compute the mismatch between the impedance associated to the worst case load and the target impedance:

$$Mismatch = \frac{Z_W - Z_T^*}{Z_W + Z_T} \quad where \quad Z_W = Z_0 \times \frac{1 + \Gamma_W}{1 - \Gamma_W} \quad and \quad Z_T = Z_0 \times \frac{1 + \Gamma_T}{1 - \Gamma_T}$$

$$Mismatch = \frac{\Gamma_{WORST} - conj(\Gamma_{TARGET})}{1 - \Gamma_{WORST} \times \Gamma_{TARGET}} \times \frac{1 - \Gamma_{TARGET}}{1 - conj(\Gamma_{TARGET})}$$

As for what concerns performance, fig: 6.24, shows a maximum error of 0.011 at the working frequency (top left plot); while it reaches worse results for lower frequencies.
The result plot on the first Smith Chart is $C + R \times e^{j\angle(C-\Gamma_{TARGET})}$ and it mostly falls close to the point representing the short circuit ($Z \sim 0$), confirming that the circuit works properly. Possible phases are swept from 0 to 350.
The second Smith Chart shows the previous result at 26 GHz.

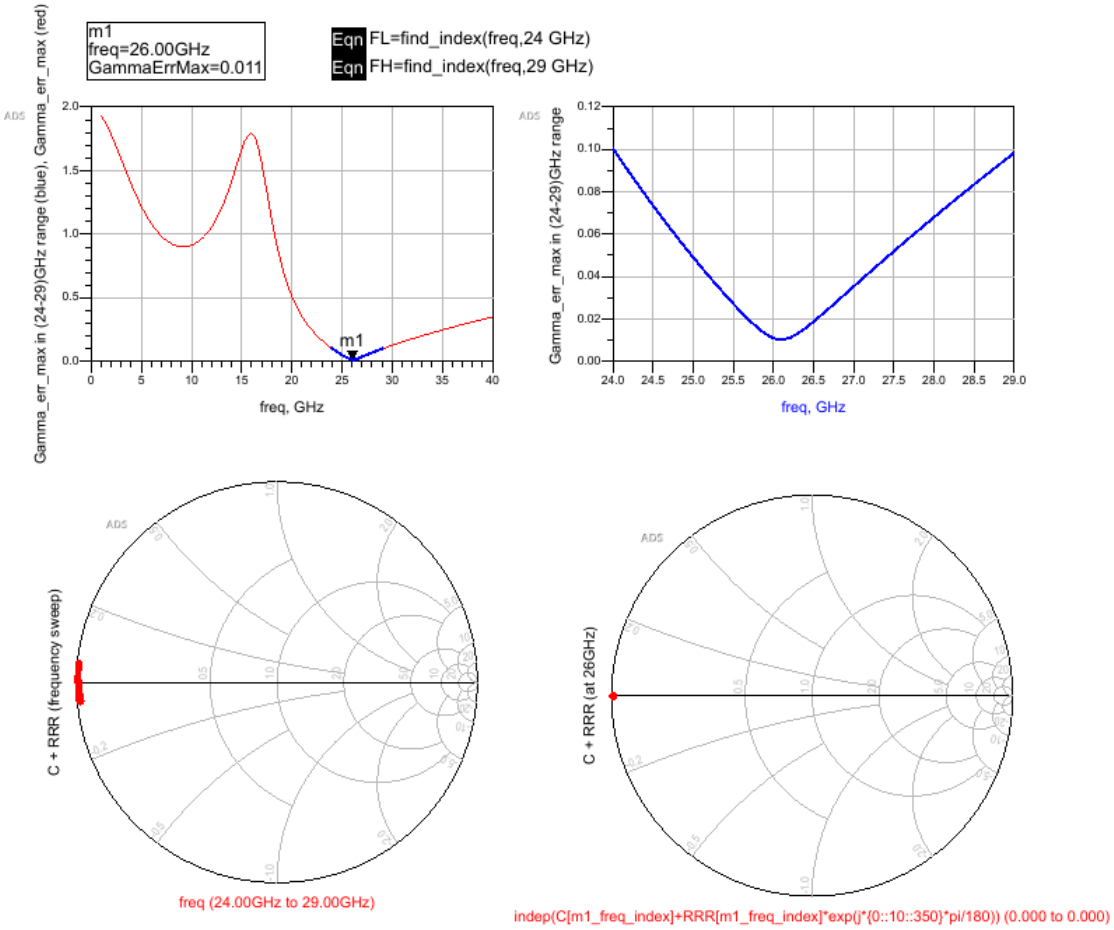


Figure 6.24: Cooling Circuit performance

The resulting layout is reported in fig: 6.25:

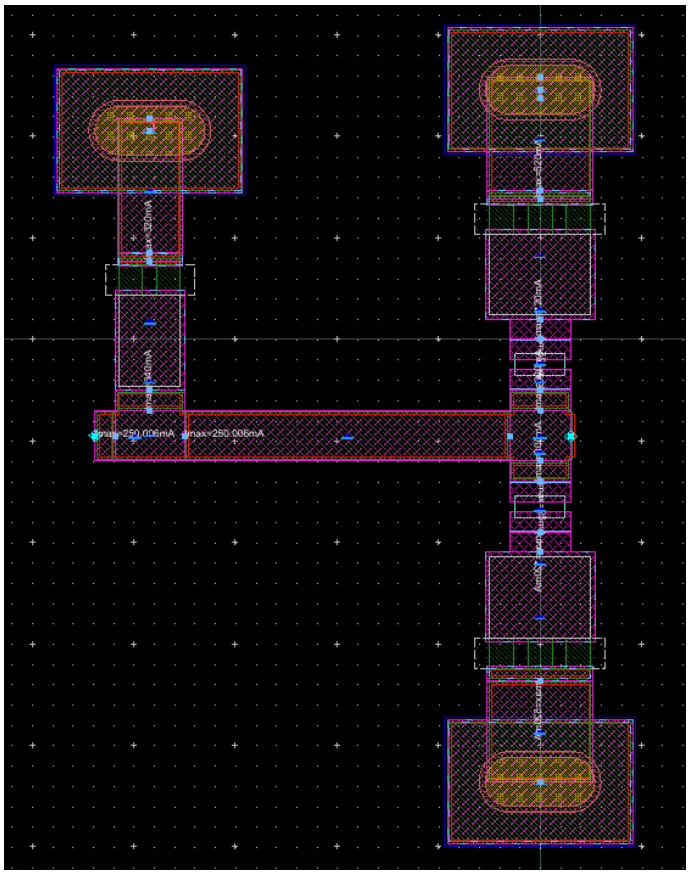


Figure 6.25: Cooling Circuit layout

When the network is replaced in the amplifier schematic, performance are not significantly changed, as shown in fig: 6.26, meaning that the cooling system behaves in a proper way.
Moreover the measured input impedance at 13 dBm, is basically the same as before ($(4.73 - j0.824)\,\Omega$), leading to the use of the same input matching network.

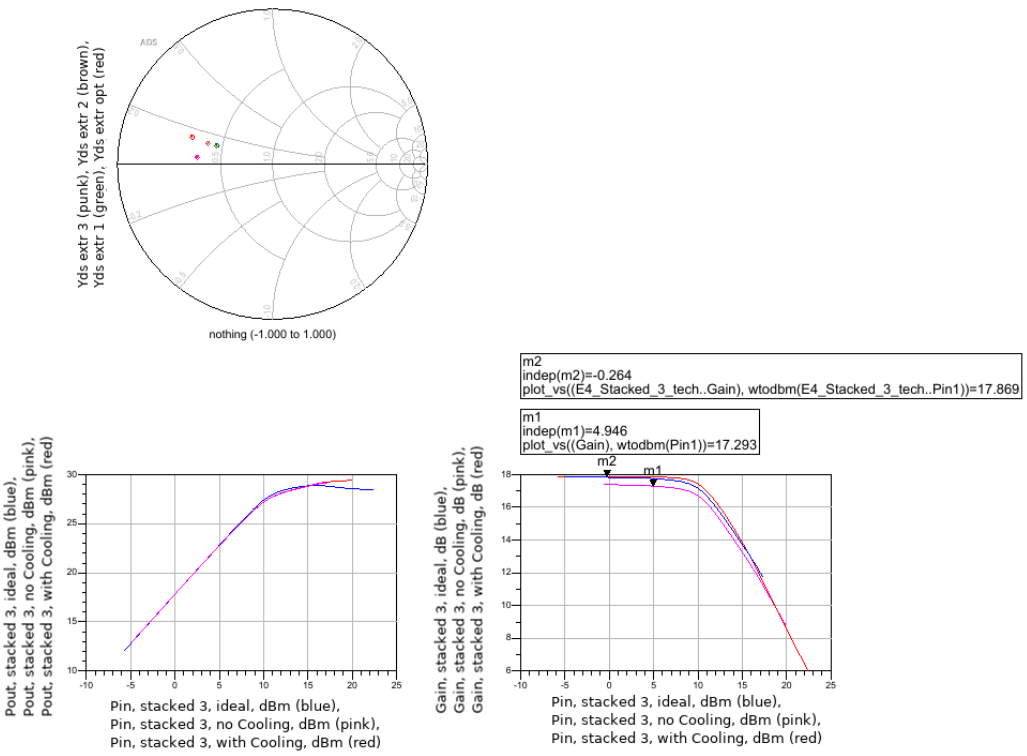


Figure 6.26: Stacked amplifier performance with IMN, OMN and Biasing network: Y_{DSi} matching (top); P_{OUT} (bottom left), Gain (bottom right)

The DC feed is not due to the ideal generator any more, but provided by the PAD. It replaces the second termination in fig: 6.21.
Since the polarization has to be delivered to the Gate terminal, in the schematic an ideal Source was still connected to the PAD, representing the external voltage Source, which could also be not ideal.

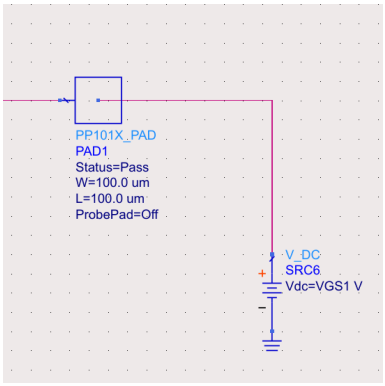


Figure 6.27: PAD connection

The cooling system is also applied to the output voltage Source V_{DD} with the same goal and the same restrictions. The only difference is that the impedance seen by the rest of the circuit should be as large as possible, ideally, meaning an open circuit.
This is due to the fact that, as in the ideal case a BIASTEE prevents the DC to interfere with the RF component, also in the real case it has to be guaranteed; so since at f_0 (in band) the feeding branch looks like an open, no RF component will flow there, but in the load. The same can be said for the DC which is free to flow in the branch but not through the DC-blocking capacitor.

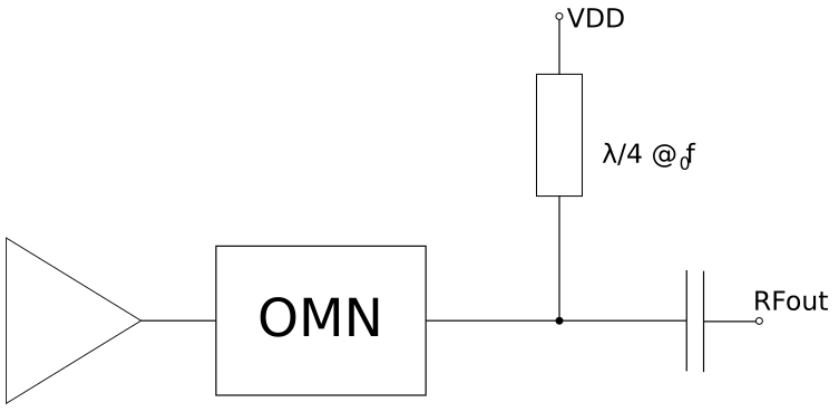


Figure 6.28: Output biasing principle schematic

Since the cooling system guarantees a short circuit, it will be sufficient to use a quarter wave transformer so to move the impedance from a null value to the open circuit point on the opposite point of the Smith Chart.
However a simple line, which is the simplest $\lambda/4$ transformer, would result to be too long; in fact 1038 um would be required. An alternative is to use a Π network:

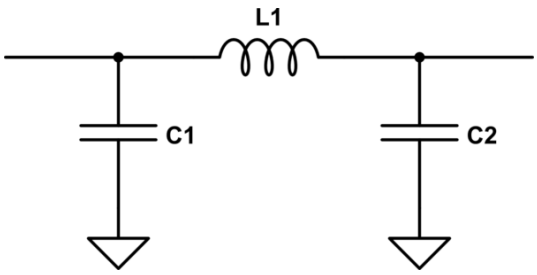


Figure 6.29: Transmission line equivalent Π model

From a theoretical point of view, a transmission line can be fully described by the use of a PI model with lumped elements, as shown in fig: 6.29; $L1$ is the self-inductance per unit length, while $C1$ and $C2$ are capacitances per unit length.
The characteristic impedance Z_0 can be computed as

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

As a first hypothesis, resistive elements are set to 0; moreover, since the transmission lines works in both the directions, the capacitors should be equal.
It results that

$$X_L = Z_0 \quad and \quad X_C = Z_0$$

so overall

$$L = \frac{Z_0}{2\pi f} \quad and \quad C = \frac{1}{2\pi f Z_0}$$

Finally given a central frequency of 26 GHz and a characteristic impedance of 50 Ω, $L = 0.3\,\text{nH}$ and $C = 0.12\,\text{pF}$.
In this case the impedance transformation is perfectly performed and the input impedance results to be close to infinity (fig: 6.30). Cooling system's impedance is computed through an equivalent RC parallel circuit, resulting in $R = 0.24\,\Omega$ and $C = 6.9\,\text{pF}$ as a further confirmation of system's performance.

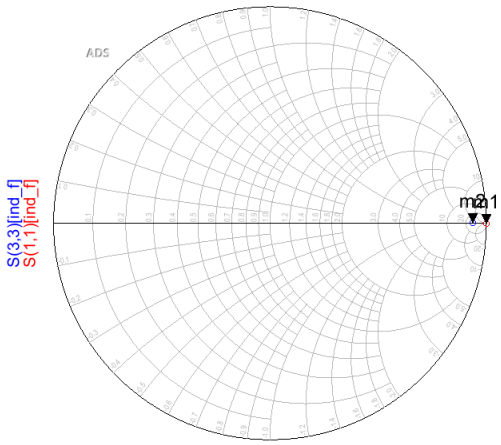


Figure 6.30: PI network performance

In the real case the resulting circuit is represented in fig: 6.31, while the corresponding layout is in fig: 6.32. Since the real design involves a more complicated model, simple calculations can not be carried on and the actual matching is obtained through simulations.

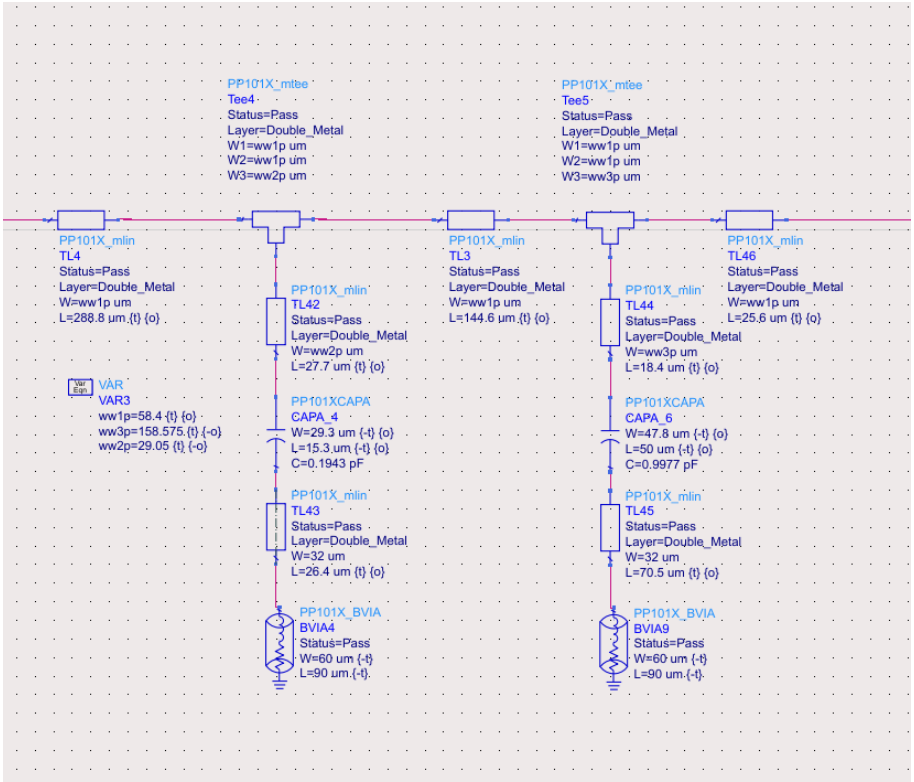


Figure 6.31: PI network schematic with real components

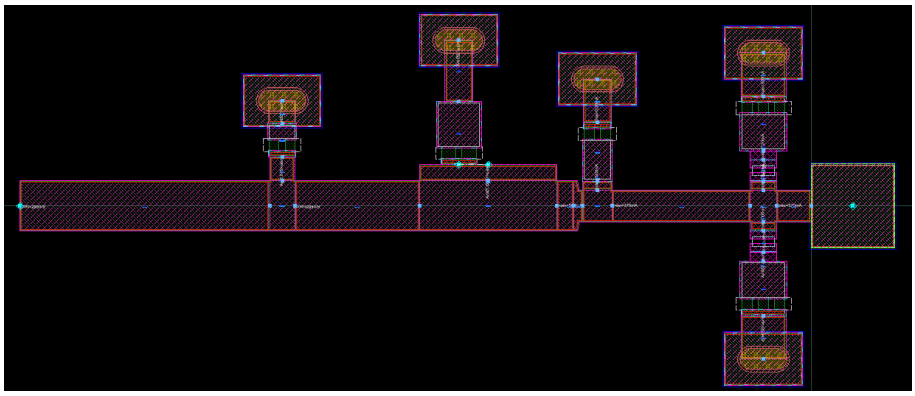


Figure 6.32: PI network & Cooling system layout

An important criteria to be taken into account when designing the microstrips, is the maximum allowed current, which is linked to the actual width and thickness of the line The previously cited limit only concerns the DC component of the flowing current, so, the latter is measured through an harmonic balance simulation (red curve):

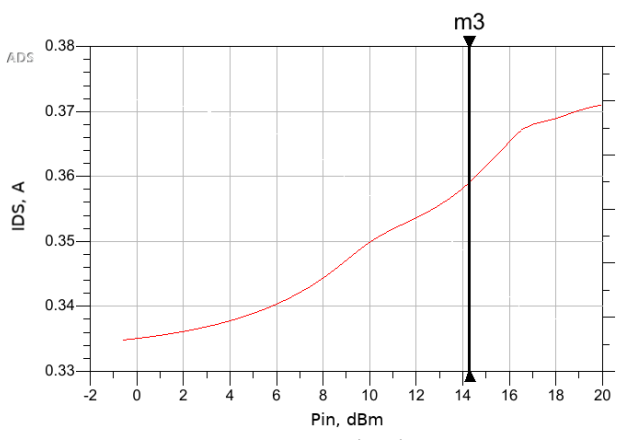


Figure 6.33: PI network max DC current

The actual value depends on the input power, so it is necessary to consider the saturation case, which will be the operating situation. In correspondence of $P_{IN} \sim 13\,\text{dBm}$ the measured current is 0.36 A. The minimum required width will be 36 um.
The previous width was largely guaranteed in the PI network; the same can not be said for the cooling system, which has to be modified with respect to the input one:

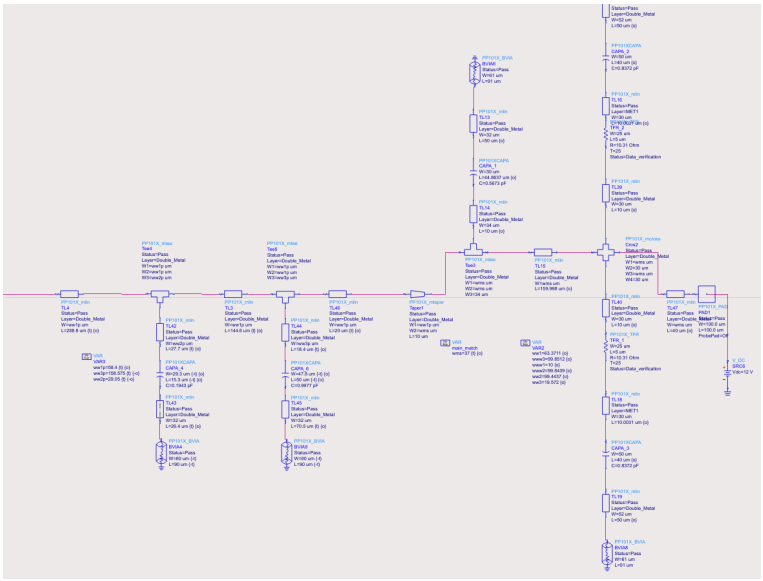


Figure 6.34: Output biasing network: a Π network is followed by the usual "Cooling circuit"

As for the input cooling circuit, the maximum allowed current is not a problem since it involves a Gate current, which can be said to be approximately null, differently from the Drain one.

The real PI network is not as performing as the ideal one, which transforms a short circuit into a perfect open; in fact the measured impedance at its input is estimated to be only $\sim 1500\,\Omega$ (fig: 6.35). Despite this, as shown in the following section, when adding this section to the amplifier, the overall performance will not suffer severe penalties.

Pavail	(Vin[1]/Iin.i[1])
0.000	1.498E3 + j19.894
0.500	1.498E3 + j19.894
1.000	1.498E3 + j19.894
1.500	1.498E3 + j19.894
2.000	1.498E3 + j19.894
2.500	1.498E3 + j19.894
3.000	1.498E3 + j19.894
3.500	1.498E3 + j19.894
4.000	1.498E3 + j19.894
4.500	1.498E3 + j19.894
5.000	1.498E3 + j19.894
5.500	1.498E3 + j19.894
6.000	1.498E3 + j19.894
6.500	1.498E3 + j19.894
7.000	1.498E3 + j19.894
7.500	1.498E3 + j19.894
8.000	1.498E3 + j19.894
8.500	1.498E3 + j19.894
9.000	1.498E3 + j19.894
9.500	1.498E3 + j19.894
10.000	1.498E3 + j19.894
10.500	1.498E3 + j19.894
11.000	1.498E3 + j19.894
11.500	1.498E3 + j19.894
12.000	1.498E3 + j19.894
12.500	1.498E3 + j19.894
13.000	1.498E3 + j19.894
13.500	1.498E3 + j19.894
14.000	1.498E3 + j19.894
14.500	1.498E3 + j19.894

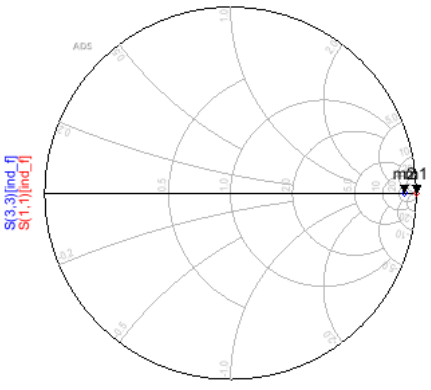


Figure 6.35: PI network performance

In order to connect the cited network to the remaining circuit, it is necessary to choose a proper position: the best results are obtained when inserting it after output matching network's taper.

6.3 Overall amplifier

The final step in the amplifier design is to add all the cited circuits to the single Stacked stage.
With respect to the previous section results, the insertion of the output feeding network causes a further decrease in gain: as shown in fig: 6.36 in saturation, the maximum value is 17.29 dB, while the ideal one is close to 17.9 dB. The previous result was obtained through an additional tuning of networks, in order to improve inter-stage matching and the gain itself.

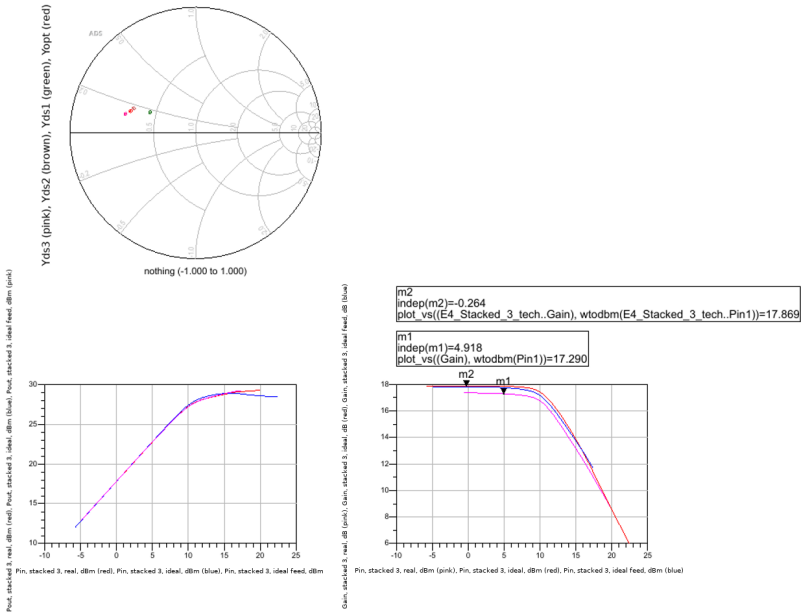


Figure 6.36: Stacked amplifier performance with IMN, OMN, Input and Output bias networks: Y_{DSi} matching (top); P_{OUT} (bottom left), Gain (bottom right)

Let's now compare the 3-stages amplifier with single CS stage, in terms of Gain and output power:

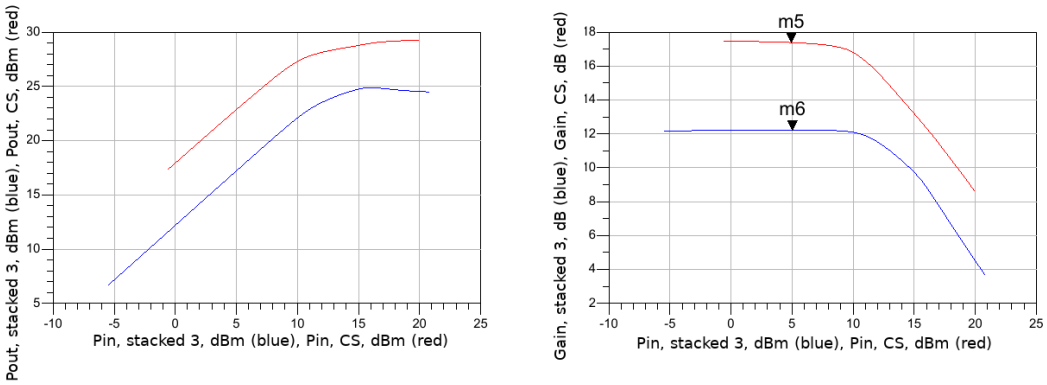


Figure 6.37: Comparison between a CS and a real 3-stages Stacked amplifier

From fig: 6.37 (right plot), the blue curve shows the gain of a CS, which is 12.23 dB; on the other hand the red curve reaches 17.38 dB, meaning that the improvement is $\sim 4.8dB$. However the overall stacked PA goes into compression before the CS stage alone, due to the variation applied to the output load with respect to the theoretical one. The output power at 3 dB compression (28 dBm) is 3 dB higher than the saturated output power of the CS alone, and can be further increased up to more than 29 dBm by allowing more compression.

As for stability, the overall amplifier results to be unconditionally stable, as shown by stability circles in fig: 6.38:

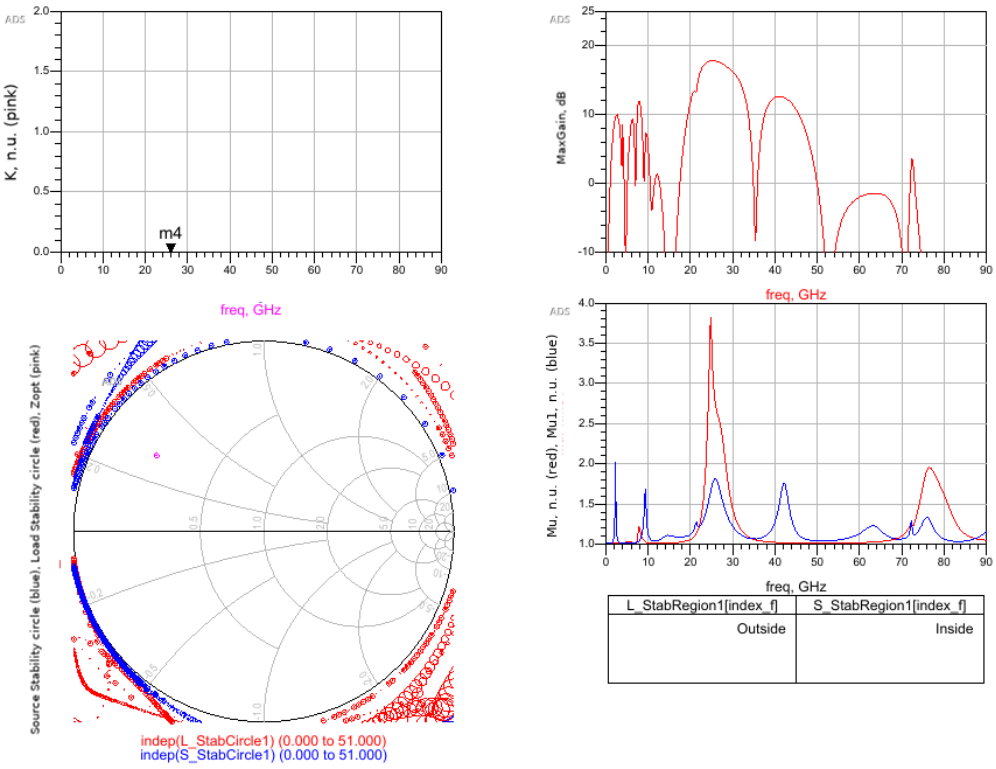


Figure 6.38: Stacked amplifier stability performance: K and ΔS (top left) and Gain (top right); stability circles (bottom left); Mu and Mu1 (bottom right)

Finally the resulting layout is reported in fig: 6.39; this configuration is a bit too space consuming due to long lines. A possible solution is to replace them with inductors (rectangular shaped) if the associated inductance value results to be physically achievable; this option will be investigated in section 6.3

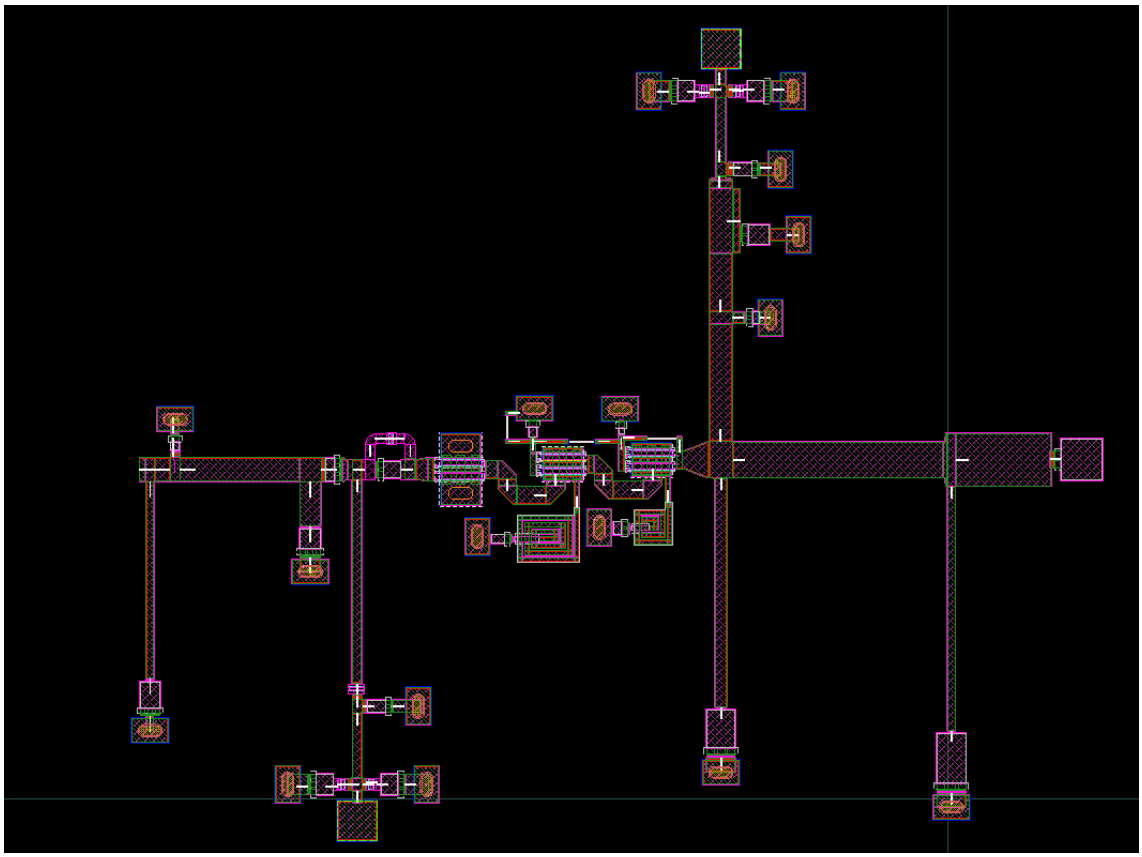


Figure 6.39: 3-stages Stacked amplifier Layout with OMN, IMN, biasing networks

It could be now interesting to investigate the frequency behavior of the designed networks: the analyzed frequency range is 24 GHz − 29 GHz. performance resulting from an harmonic balance with frequency sweep are reported in fig: 6.40, fig: 6.41 and fig: 6.42. It is clear that the device is not wide-band and only frequencies around 26 GHz can be profitably used: inter-stage matching is not achieved any more leading to gain of about 15 dB (@29 GHz) and an output power of 27 dBm, at the same frequency. These values are strongly below the designed one at 26 GHz.
Also PAE and the efficiency result to be degraded, especially for the second CG stage at $f \neq f_0$.

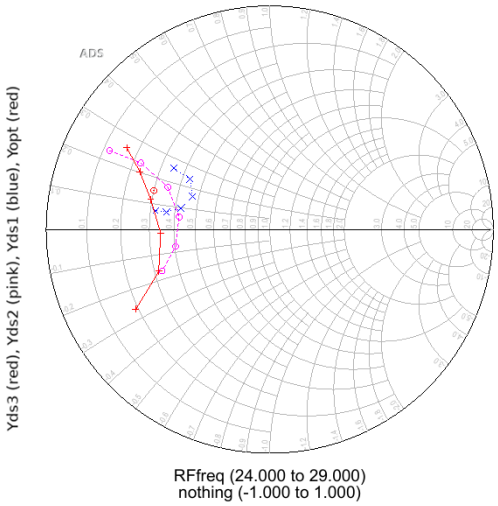


Figure 6.40: Extrinsic Y_{DSi} frequency behavior in the 24 GHz – 29 GHz range

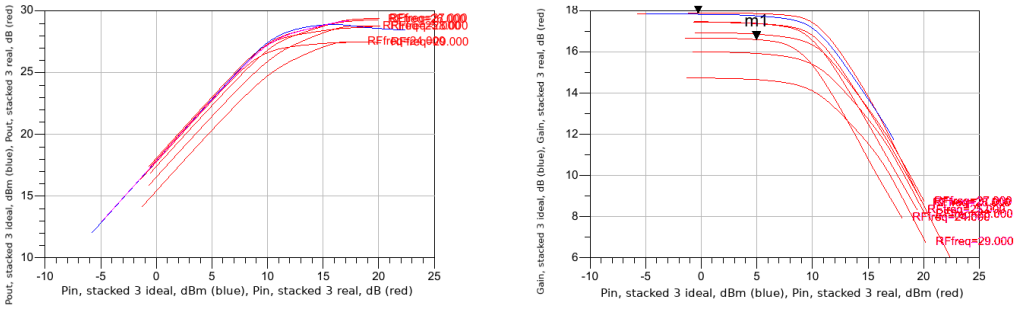


Figure 6.41: Frequency behavior performance in the 24 GHz – 29 GHz range: P_{OUT} (left), Gain (right)

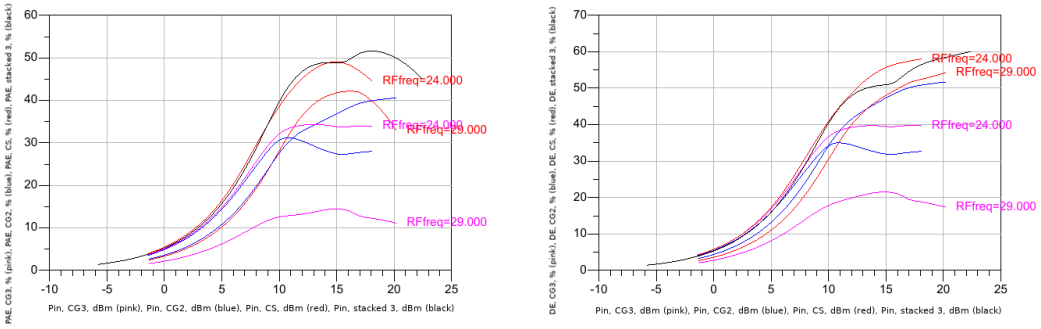


Figure 6.42: Frequency behavior performance in the 24 GHz – 29 GHz range: PAE (left) and DE (right)

Inductor variant

As previously claimed in this section will be analyzed the introduction of inductors, replacing too long lines.
In order to obtain the same performance as before, the frequency behavior of the line was compared with the replacing element's one, in terms of impedance; as a general assumption the solution exploiting inductors shows a lower resistance than the other one.
In particular the first schematic which is presented in fig: 6.43 is the input matching network; only the first branch was characterized by the presence of a long line; in fig: 6.44, new network's performance are compared with the previous ones. Finally fig: 6.45 shows the new layout.

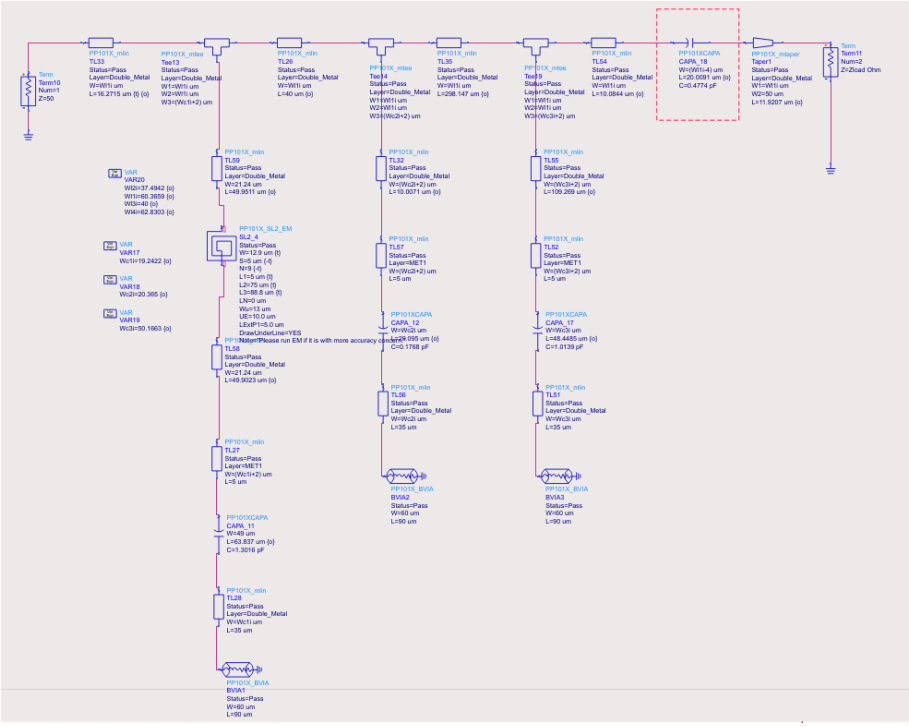


Figure 6.43: Input matching network schematic with inductors

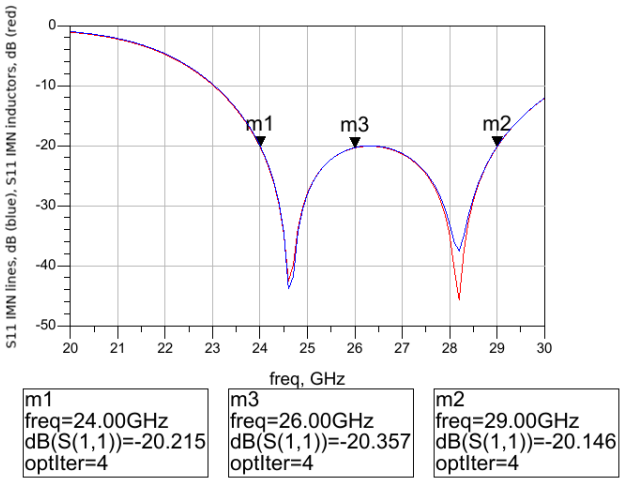


Figure 6.44: Input matching network performance

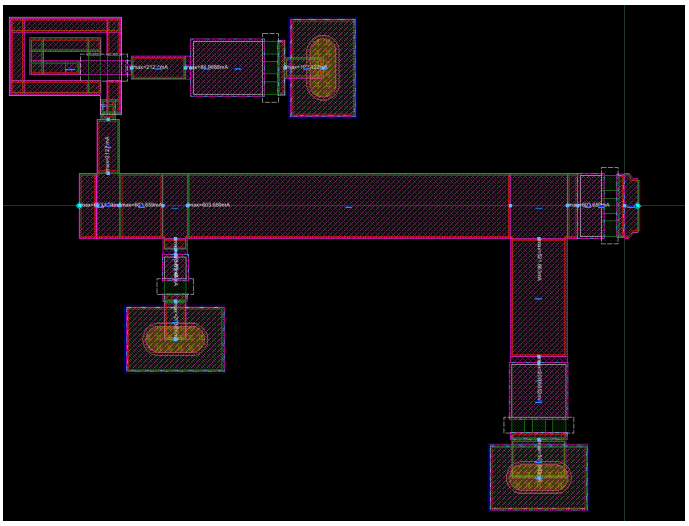


Figure 6.45: Input matching network layout with inductors

Also the Output matching network had to be modified with the introduction of two inductors, as follows from the schematic in fig: 6.46.
Taking a look at fig: 6.47, it is possible to note an increase in performance for a quite large frequency range, when using inductors.

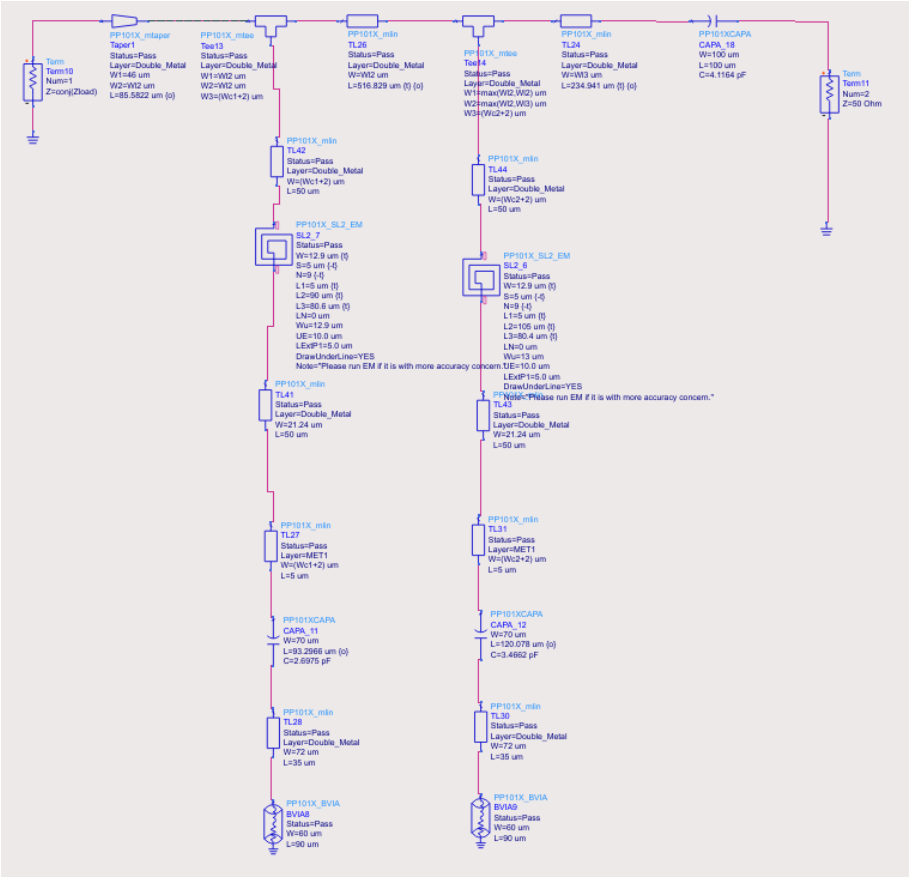


Figure 6.46: Output matching network with inductors

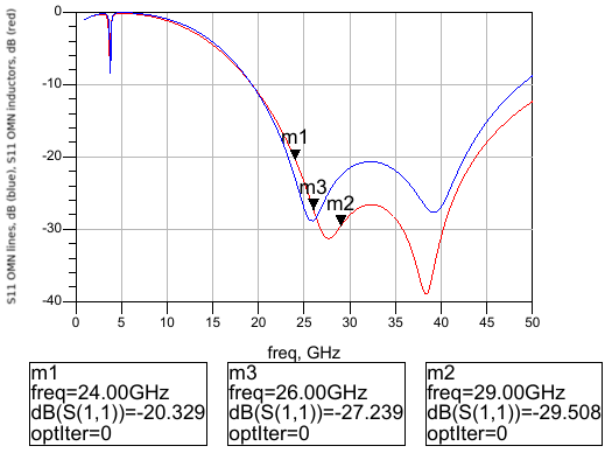


Figure 6.47: Output matching network performance

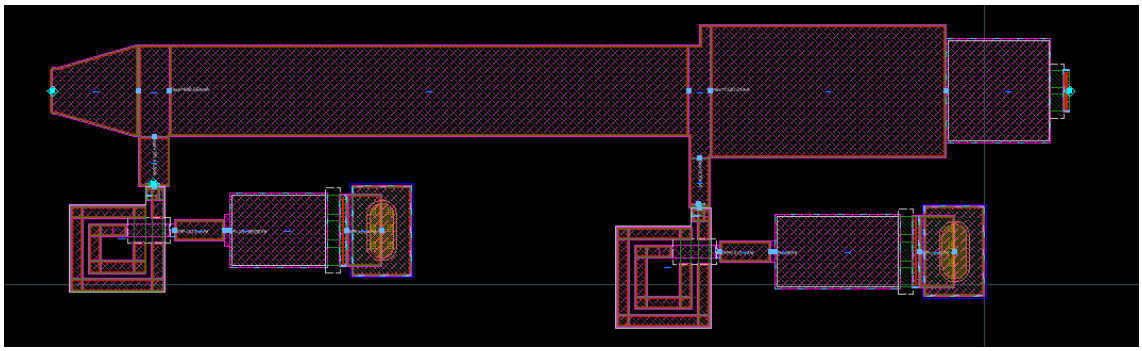


Figure 6.48: Output matching network layout with inductors

Finally the stabilization network was modified as reported in fig: 6.49 and fig: 6.50.

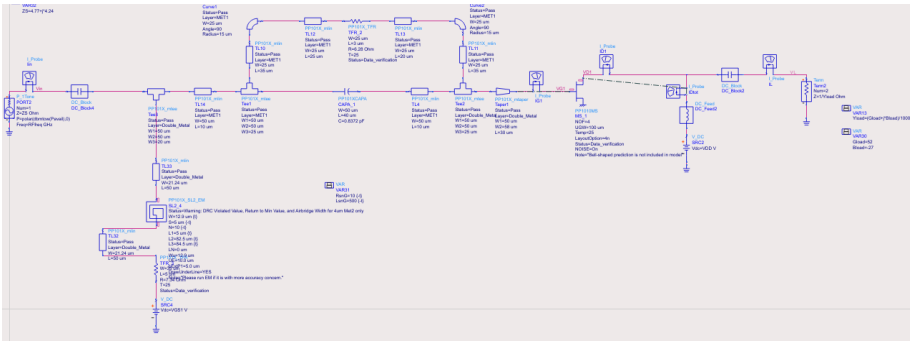


Figure 6.49: Stabilization network with inductors

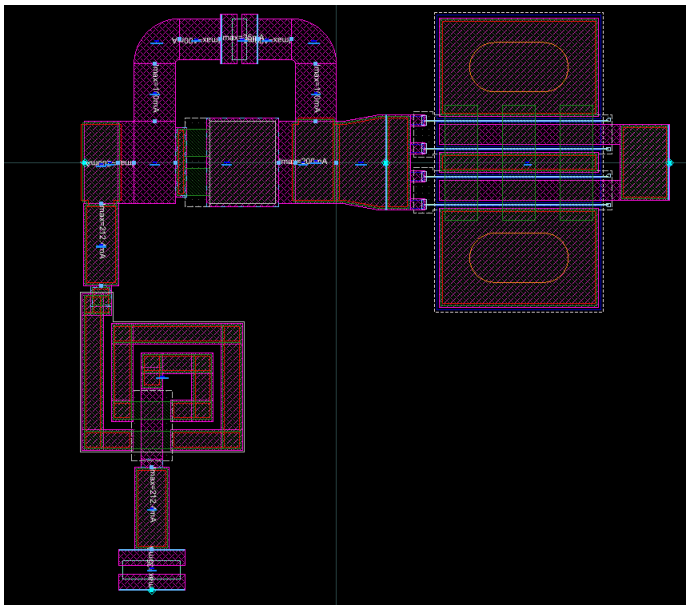


Figure 6.50: Stabilization network layout with inductors

The final layout is reported in the image below: if compared with the previous one, it results to be much more compact.

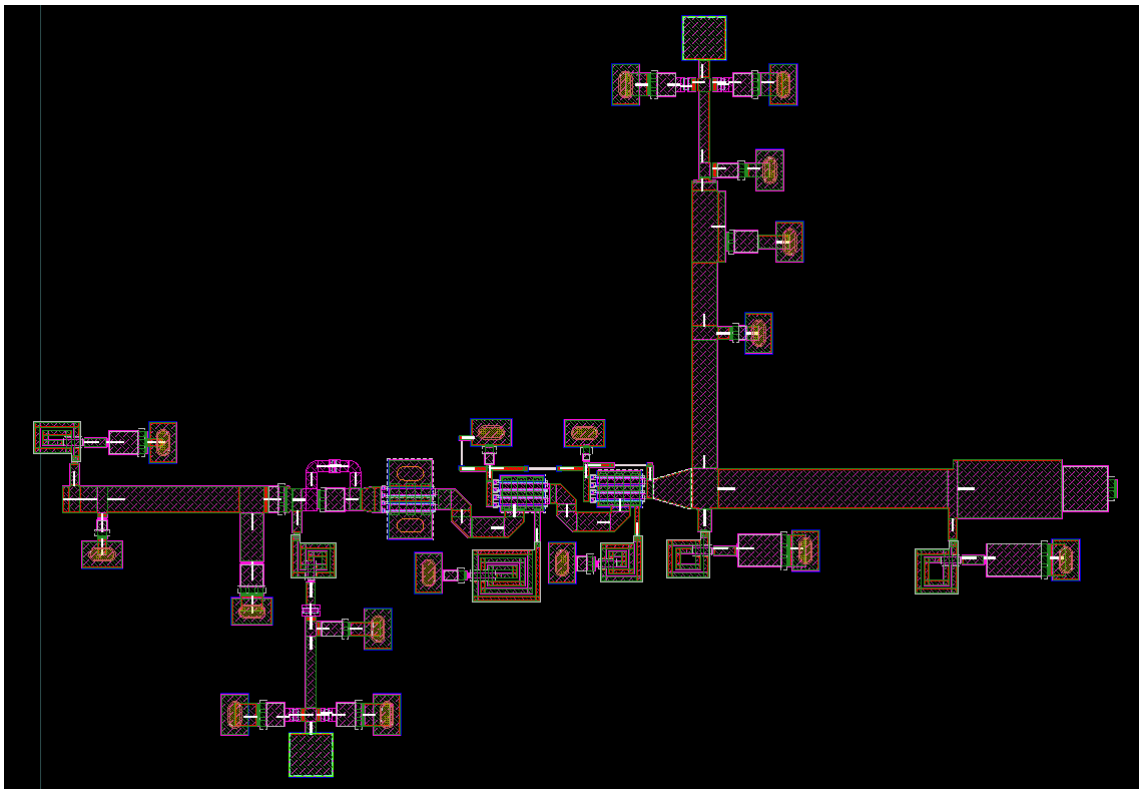


Figure 6.51: 3-stages stacked amplifier layout with inductors

Taking now a look at performance, it is possible to see a low increase, in gain up to 17.404 dB, while the output power seems to be unchanged.
However it is not a problem since the cited frequencies are higher than the working one.

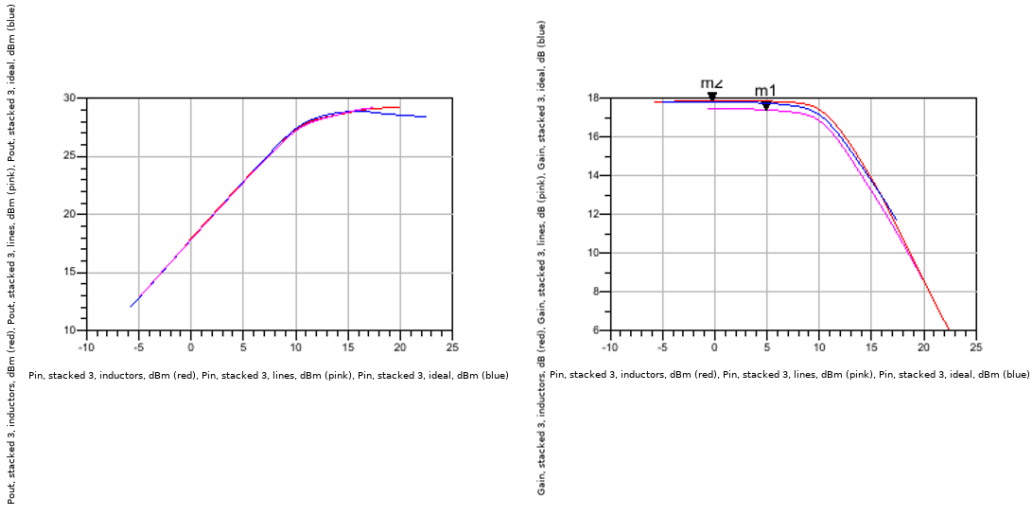


Figure 6.52: 3-stages stacked amplifier performance with inductors: P_{OUT} (left), Gain (right)

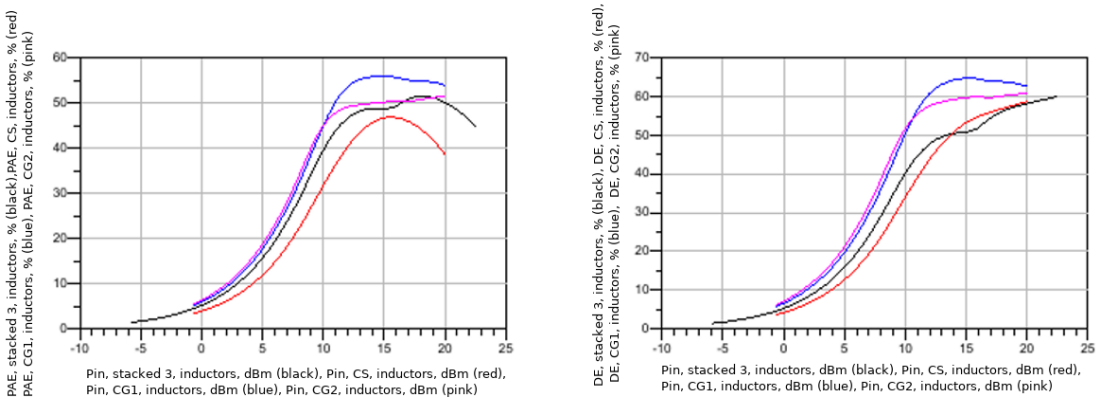


Figure 6.53: 3-stages stacked amplifier performance with inductors: PAE (left), DE (right)

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