Politecnico di Torino

DIPARTIMENTO DI ELETTRONICA E TELECOMUNICAZIONI
Corso di Laurea Magistrale in Ingegneria Elettronica

Tesi di Laurea Magistrale

Analysis and Design of Multi-Stage Doherty Power Amplifiers for Wireless Communications

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Anno Accademico 2020-2021

Contents

Glossary

AM	Amplitude Modulation
BJT	Bipolar Junction Transistor
CAD	Computer-Aided Design
CCA	Current Conduction Angle
DPA	Doherty Power Amplifier
EER	Envelope Elimination and Restoration
EM	Electromagnetic
ET	Envelope Tracking
FET	Field Effect Transistor
IIN	Impedance Inversion Network
IMN	Input Matching Network
IoT	Internet of Things
LF	Linearity Factor
LINC	LInear amplification using Nonlinear Components
LSSP	Large-Signal S-Parameter
LTE	Long-Term Evolution
OBO	Output BackOff
OFDM	Orthogonal Frequency-Division Multiplexing
OMN	Output Matching Network
PA	Power Amplifier
PAE	Power-Added Efficiency
PAPR	Peak-to-Average Power Ratio
PM	Phase Modulation
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
SCS	Signal Component Separator
SFDR	Spurious Free Dynamic Range
SSB	Single SideBand
VCCS	Voltage Controlled Current Source
WCDMA	Wideband Code Division Multiple Access

Chapter 1

Introduction

Wireless connectivity has surely become an important part of our lives in the current society. The rise of smartphones and Internet of Things (IoT) devices, a revolution that took the world by storm in the last decade, translates to a ever-growing need for new technological solutions in the Radio Frequency (RF) field in order to satisfy the need for faster, more secure, more efficient communication channels.

The key-word is *efficiency*: be it a pocket device powered by a battery or a huge baseband station connected to the mains, the efficient use of energy is of paramount importance for every RF transceiver. Analyzing the power budget of such a system shows the most power-hungry part is the Power Amplifier (PA) and that's indeed where most of the engineering effort is spent.

Most of the modern modulation schemes, such as Orthogonal Frequency-Division Multiplexing (OFDM), Wideband Code Division Multiple Access (WCDMA) or Long-Term Evolution (LTE), share a common trait: all of them produce signals whose envelope is not constant or, in equivalent terms, characterised by a high Peak-to-Average Power Ratio (PAPR). Making an amplifier work well with such a wide dynamic input range is incredibly tricky: the best efficiency figures are usually obtained when the device works at maximum drive while the non-constant envelope input forces it to work in the back-off region for most of the time, making the average efficiency drop.

To overcome this limitation many efficiency enhancement schemes have been proposed, the most renowned being the Envelope Elimination and Restoration (EER) [1] and the Envelope Tracking (ET), with the aim to dynamically modulate the amplifier drain bias according to the input levels: this technically ensures the amplifier works in the high efficiency region no matter what the input level is since, thanks to the modulated bias, the

amount of wasted DC power in back-off is reduced.

A similar yet different solution is the architecture proposed by W.H. Doherty [2] in the years preceding the second world war. The paper describes this novel architecture employing only two amplifiers, vacuum tubes, and some creative use of the load-modulation effect. The simplicity of the DPA is what made it very popular among the RF designers: when compared to the aforementioned techniques that modulate the bias there's no need for extra circuitry to track the input envelope, the system itself is built to self-enhance its efficiency.

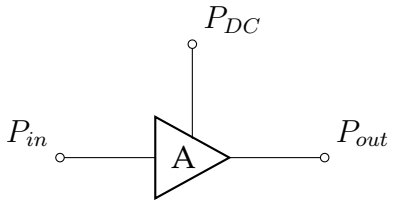
While the original work covered only the basic scheme with two devices, the idea behind the DPA can be generalized to an arbitrary large number of devices. This work aims to explore the design process for a three-stage DPA, starting from pencil-and-paper calculations up to Electromagnetic (EM) simulations carried out in Agilent ADS.

Chapter 2

Power Amplifiers

2.1 A whirlwind tour

A power amplifier is an electronic device whose task is to boost the power level of a given input signal to a desired value. To better understand how this is achieved the amplifier can also be thought as a three terminal device, with an input terminal, and output terminal and a terminal for the DC feed: the amplifier behaves as a DC-to-AC converter that modulates the DC voltage according to the RF signal at the input.



The signal amplification is done by a nonlinear component able to withstand large amounts of power. The typical choice for an active device is a Field Effect Transistor (FET) or Bipolar Junction Transistor (BJT), vacuum tubes were also widely used before the advent of the transistor and their use is now limited to niches where extremely high powers are handled. For the purpose of this work the use of of a FET device is assumed.

The main difference between a PA and a common voltage amplifier is related to the input signal swing: the latter is usually analyzed under the *small-signal* assumption, meaning that the input voltage swing v_{gs} is a small fraction of the DC bias voltage V_{DD}. This assumption makes sure that, once the device is correctly biased in the linear region, the device output current will follow the input value.

When working with large amounts of power the input signal may be large enough to drive the device outside the region where the linearized results are valid, thus requiring a new model for a proper analysis, the *large-signal* model. The presence of nonlinear effects greatly complicates the modeling as many device parameters become dependent on the input drive level to some extent.

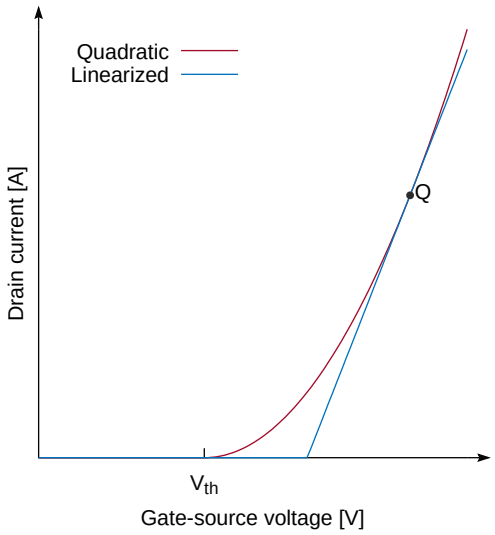


Figure 2.1: FET transconductance models

2.2 Operation classes

The choice of the bias point is fundamental in the design process of a PA as every characteristic depends on it; every PA can be categorized in several *classes* of operation depending on the chosen bias point.

The bias point (indicated with the letter Q) for a FET device is defined by the gate voltage V_{GG} and the drain voltage V_{DD} or, in an equivalent way, by the quiescent drain current I_{DC} and the drain voltage. The choice for the placement of Q is limited by the physical behaviour of the device: the drain current cannot go below zero nor above a maximum value I_{max} where the gate junction becomes forward-biased, and the drain voltage is clamped between the knee voltage V_k, where the device enters the saturation region, and the maximum voltage V_{br} the device can physically endure before breaking down.

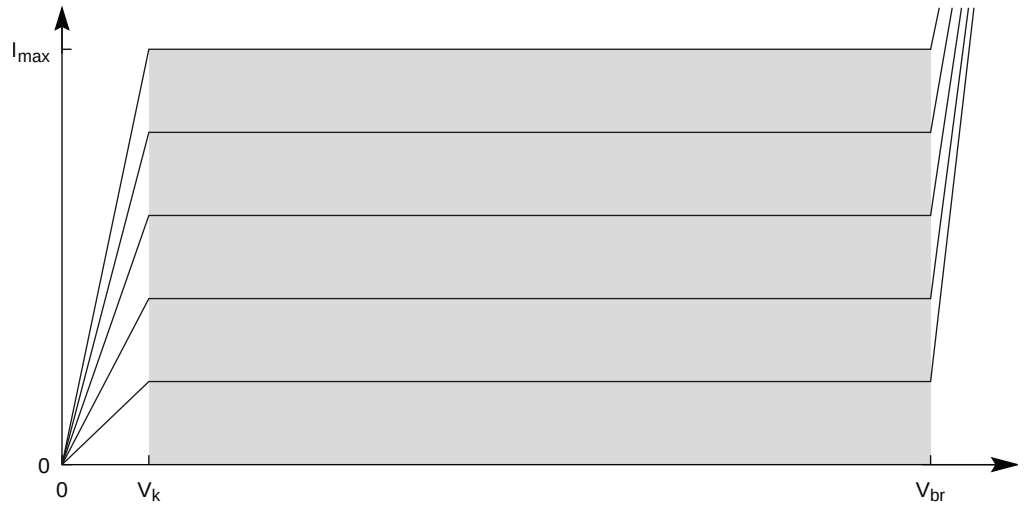


Figure 2.2: Usable current and voltage characteristic

The imposed limits describe the relatively large usable area as depicted in Figure 2.2. Being the ultimate goal for a PA the emission of power, the idea is to maximize both the drain voltage and current amplitude in order to maximize the P_{out}.

For the time being the bias voltage is considered to be equal to the mean value between the knee voltage and the breakdown one, right in the middle of the usable V_{ds} range. This is not the only possible choice but is the common one that won't influence the validity of the explanation.

The choice of a suitable quiescent current, on the other hand, is more nuanced. A general formulation of the bias point in mathematical terms is:

$$\xi = \frac{I_{DC}}{I_{Max}} \tag{2.1}$$

This variable can take a maximum value of 1 and can even become negative, the value reflects the vertical position of the bias point with respect to the maximum amount of current the device is able to deliver. A negative quiescent current has no physical meaning in itself but allows for seamlessly dealing with negative gate voltage biases using the same theoretical framework.

Assuming a sinusoidal input signal and a constant transconductance, the PA drain current is a sinusoidal waveform whose time-dependant behaviour, where $\theta = \omega t$, is described as:

$$i_D(\theta) = \begin{cases} \frac{I_{max}}{1-cos(\Phi/2)}[cos(\theta) - cos(\Phi/2)] & -\Phi/2 \leq \theta \leq \Phi/2 \\ 0 & \text{otherwise} \end{cases} \tag{2.2}$$

The parameter Φ is the Current Conduction Angle (CCA), representing the fraction of the input sinusoid for which the amplifier is active. The CCA can be related to the parameter ξ by means of:

$$\Phi = 2 \arccos\left(\frac{\xi}{\xi - 1}\right) \tag{2.3}$$

The bias point affects the shape of the drain current waveform. As pictured in Fig. 2.3 the waveforms are chopped for $\xi < 0.5$: moving the current value below the midpoint increases the possibility of hitting the current floor while, on the other hand, decreases the amount of static power consumed by the amplifier.

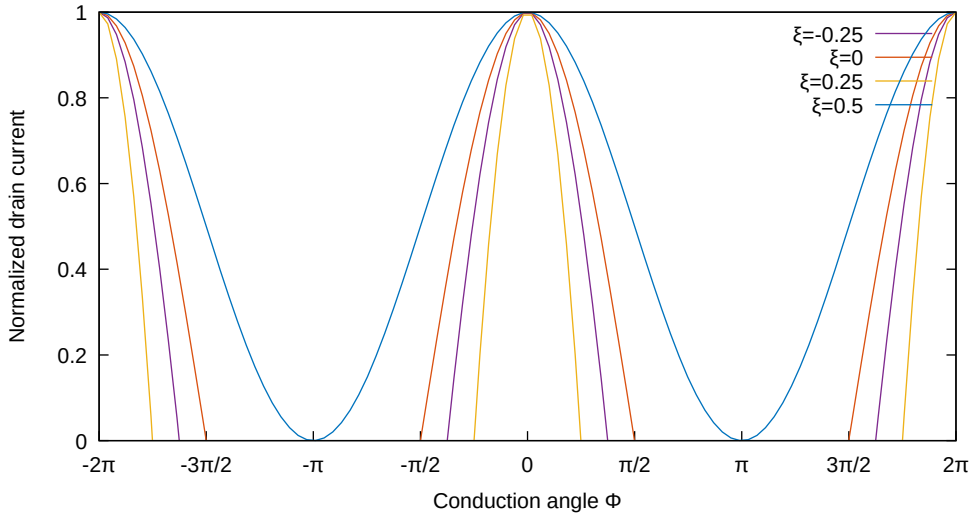


Figure 2.3: Drain current waveform for different values of ξ

The chopped waveform described analytically in Eq. 2.2 can be also expressed in a more generic form, introducing the dependance on a normalized scale factor x:

$$i_d(x, \theta) = \begin{cases} \frac{I_{max}}{1-\cos\left(\frac{\Phi}{2}\right)} \left[x \cdot \cos(\theta) - \cos\left(\frac{\Phi}{2}\right)\right] & -\frac{\Phi_x}{2} \leq \theta \leq \frac{\Phi_x}{2} \\ 0 & \text{otherwise} \end{cases} \tag{2.4}$$

where Φ_x is the one-sided angular width of the bell-shaped figure. In Figure 2.3 the curve obtained for $\xi = 0$, corresponding to class B operation for $x = 1$, has $\Phi_x = \pi/2$, half of the conduction angle. A general formulation for Φ_x is found by imposing the drain current to be zero at the extremity of the bell:

$$i_d\left(x, \frac{\Phi_x}{2}\right) = 0 \rightarrow \Phi_x = 2\cos^{-1}\left[\frac{1}{x}\cos\left(\frac{\Phi}{2}\right)\right] \tag{2.5}$$

A PA can still be considered as a linear device, but only for low values of P_{in}. When the input drive becomes significant the overall performance of the device are limited by the device's nonlinearities.

The power gain G, one of the main figures of merit for a PA, experiences a compression effect instead of being constant as the input level increases. An estimate of the extra driving power needed to complement the decreasing gain is given by the *added power* term, defined as:

$$P_{add} = P_{out} - P_{in} = P_{out}\left(1 - \frac{1}{G}\right) \tag{2.6}$$

As stated before, one of the main figures of merit for a PA is its *drain efficiency* η, defined as:

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.7}$$

The efficiency parameter gives a rough idea of how effective the DC-to-RF power conversion is and, ideally, it should reach the maximum value of 100%. As defined the efficiency has a major flaw in that the gain compression phenomena is not taken into account at all, making that a poor parameter for benchmarks and comparisons.

To overcome this problem a better figure of merit, the Power-Added Efficiency (PAE), is defined:

$$PAE = \frac{P_{add}}{P_{DC}} = \frac{P_{out}}{P_{DC}}\left(1 - \frac{1}{G}\right) = \eta\left(1 - \frac{1}{G}\right) \tag{2.8}$$

The two efficiency figures reach the same value when the gain is high, but the second term decreases as the gain rolls-off thus making the PAE more effective in describing the actual PA performance.

The whole family of PAs can be divided in *classes* depending on their conduction angle Φ or their working mode (conventional vs. switching). A small excerpt of this classification is reported in the table below.

Class	ξ	Φ	η_{max}
A	0.5	2π	50%
AB	$0 < \xi < 1$	$2\pi < \Phi < \pi$	$50\% < \eta < 78.5\%$
B	0	π	78.5%
C	< 0	$< \pi$	$\approx 100\%$

The reported efficiency are only theoretical. The laws of thermodynamics are pretty clear on the matter, no physical RF amplifier can ever reach conversion efficiencies as high as $100\,\%$. Several improvements can be made by employing switching amplifiers working in class E or, using the conventional amplification methods, applying some tricks to minimize the power lost on higher-order harmonics and keeping the current and voltage waveforms in-quadrature as much as possible.

2.3 Load Line matching

Another big difference between small-signal amplifiers and power amplifiers is the kind of output matching. Jacobi's theorem of maximum power transfer states that, given a source with internal resistance Z_S connected to a load Z_L, the transferred power is maximum when the following equality holds:

$$Z_L = Z_S^* \tag{2.9}$$

This matching condition, called *conjugate matching*, ensures all the available output power from the PA is transferred to the load. This reasoning overlooks an important detail, the impedance seen by the drain is what sets the voltage and current swings or, in other terms, the maximum power the active device can push. Maximising the transfer of a small amount of power is definitely not one of the present design goals therefore a different loading condition is required.

The loadline matching [3] allows to study the problem the problem in a simple and intuitive way: the optimal load condition is the one that maximises the device output power.

With reference to a class A amplifier the optimum load is:

$$R_{opt} = \frac{V_{br} - V_k}{I_{max}} \tag{2.10}$$

In the I-V plane this equality defines a straight line with slope $1/R$ as pictured in Fig. 2.4. The load is optimal as it allows the device dynamic to span the whole available range, using smaller or larger values is bound

to increase the chances of having the current or voltage clip with adverse effects on the PA performance.

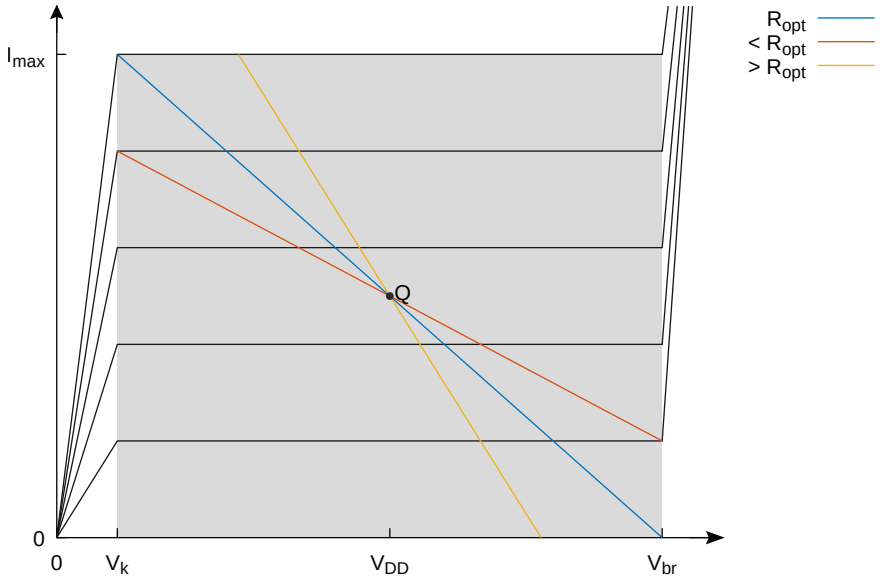


Figure 2.4: Load line behaviour

2.4 A look at nonlinearities

The root cause of many problems can be traced back to the active device drain behaviour. When the current waveform begins to deviate from its canonical trend, becoming a truncated sinusoid, the output spectral purity goes downhill. The side effect of the truncation is the introduction of spurious harmonic components at frequencies different than the fundamental one f_0. Beside requiring some kind of filtering, this means the amplifier is wasting part of the DC power on unwanted components, limiting its usefulness at working conditions.

This behaviour can be described analytically by evaluating the magnitude of the spectral components of I_D. The Fourier series expansion of the drain current waveform (Eq. 2.2), taking into account the cosine symmetry, is:

$$I_D = \sum_{n=0}^{+\infty} I_n cos(n\omega t) \tag{2.11}$$

Where the Fourier coefficients for the n-th harmonic component are:

$$I_n = \begin{cases} \frac{I_{max}}{2\pi}\frac{2sin(\Phi/2)-\Phi cos(\Phi/2)}{1-cos(\Phi/2)} & n=0 \\ \frac{I_{max}}{2\pi}\frac{\Phi-sin(\Phi)}{1-cos(\Phi/2)} & n=1 \\ \frac{2I_{max}}{\pi}\frac{sin(n\cdot\Phi/2)cos(\Phi/2)-n\cdot sin(\Phi/2)cos(n\cdot\Phi/2)}{n(n^2-1)(1-cos(\Phi/2))} & n\geq 2 \end{cases} \tag{2.12}$$

Figure 2.5 shows the peak values for each harmonic component up to the fifth order, normalized to I_{max} for different values of Φ.
The DC component rapidly decreases with the CCA as the amplifier draws less and less power in static conditions, leading to an increase of the efficiency term. The fundamental component, on the other hand, shows a slight increase for Φ between 2π and π only to return to the starting value and then decrease towards zero. The fluctuations in the fundamental component amplitude are strictly linked to the behaviour of the high-order components: positive values translate to DC power being "stolen" from the fundamental while negative values have the opposite effect. The $\Phi = \pi$ point is an interesting example of *destructive interference*: odd harmonics have a zero in that point and the odd ones give an alternating positive/negative contribution that, when summed together, decrease the fundamental current just enough to make its value equal to the one for $\Phi = 2\pi$

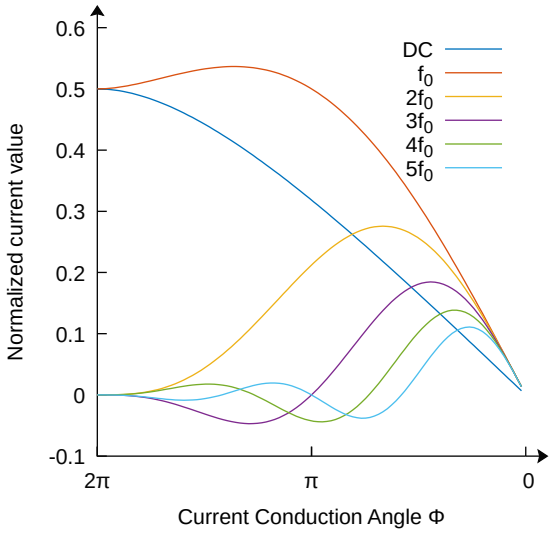


Figure 2.5: Harmonic components

2.5 Tuned load

The design process for a PA must take into account three main points:

- The output power must match the prescribed level;
- The amplifier must ensure the correct operation within a specified bandwidth;
- The amplification must be as efficient as possible, in order not to waste power and meet the power budget requirements;
- The amplifier must be as linear as possible, to ensure the output signal is not heavily distorted.

As it often happens it is not possible to satisfy all the requirements at the same time, the designer is forced to choose the best compromise that balances the three parameters.

The goal of highly linear amplifiers clashes with the demand for highly efficient solutions. As seen in the previous section the η is maximized by reducing the CCA and, at the same time, introducing progressively more nonlinearities. The linearity of a PA is quantified by the Spurious Free Dynamic Range (SFDR), defined as the range of input power for which the power of the intermodulation products remains below the noise floor. With reference to Eq. 2.12 and Fig. 2.5 the SFDR decreases with Φ, the unwanted harmonic content must be eliminated in order to restore its value to an acceptable level.

The *tuned load* condition is perhaps the simplest solution for this problem. In order to clean the current spectrum a tuned network, like the one pictured in Fig. 2.6, is interposed between the drain and the load.

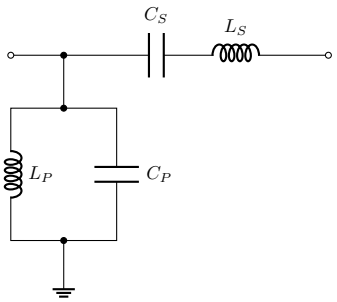


Figure 2.6: Tuned network

The network is composed of two resonating LC tanks put in parallel and in series to the drain with the twofold aim of suppressing every component at integer multiples of the frequency f_0, and to prevent the leakage of power thus keeping the drain efficiency high.

The $L_P \parallel C_P$ tank, assuming an infinite Q-factor, is an open circuit at f_0 and an open circuit elsewhere; similarly the $L_S + C_S$ tank is a short circuit at f_0 and an open circuit elsewhere. This condition ensures the current and voltage across the load are zero for the n-th harmonic and, as a consequence, the output power is also null.

A tuned network able to filter out every other harmonic beside f_0 is not physically realizable as the Q is limited by the finite parasitic resistance of the components. Moreover, when the working frequency is in the GHz range, resonators with such a thin bandwidth becomes exceptionally hard. Practical designs often limit themselves to the first two harmonic components with the highest amplitude, the 2nd and 3rd, while considering the higher order ones as small enough to be neglected.

Again, this is not the only possible solution. The harmonic components can be harnessed to improve the fundamental output power instead of being suppressed, as done for class F amplifiers.

Chapter 3

High-efficiency Power Amplifiers

3.1 Introduction

Systems where a PA is employed have strict requirements in terms of power efficiency. Be it part of a transceiver working in a base station, handling tens if not hundreds of kilowatts, or part of a portable device, where the power budget is limited, the power amplifier should be able to convert DC power to RF power in the most efficient way. Inefficient amplifiers have adverse effects on the system durability as they produce more heat, requiring complex solutions to cool the system down, and on the operating costs, as they draw more power. Moreover portable devices face several limitations to their battery life due to PAs making bad use of the available power.

The two figures of merit introduced before, the efficiency η and the PAE, are evaluated when the amplifier is working with full input drive, in saturation. In real world applications the PA is often required to work with modulated input signals showing a time-varying envelope and power. Designing an amplifier with only the signal peak power in mind is therefore not enough, every time the input power drops the amplifier is forced to work backed off from saturation and therefore with poor efficiency.

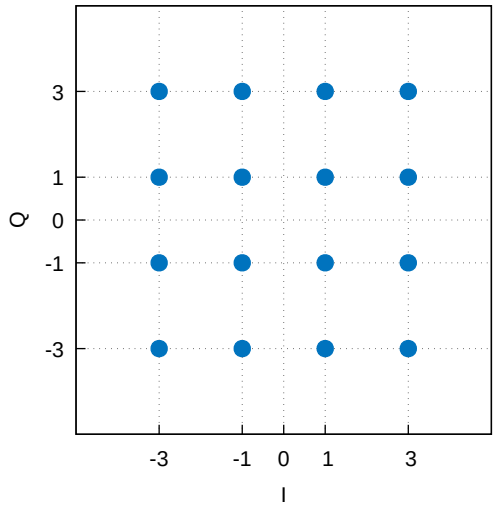


Figure 3.1: 16QAM constellation

For a generic signal modulation scheme it is possible to infer some statistical properties such as the peak and the average power levels. For example in a 16 Quadrature Amplitude Modulation (QAM), such as the one pictured in Fig. 3.1, the power of each symbol is related to their distance from the constellation center: if all the symbols are equiprobable it is therefore possible to see how a higher power level is associated to the symbols in the corners, while the average value is lower than that.

For a generic modulation it is possible to quantify how often its amplitude x is below the maximum value by means of the Peak to Average Power Ratio (PAPR), defined as:

$$PAPR|_{dB} = 10 \log_{10} \left(\frac{P_{peak}}{P_{avg}} \right) \tag{3.1}$$

The starting point to understand the root cause of the efficiency drop in backoff and how to overcome it is an ideal tuned amplifier biased in class B and connected to its optimum load, shown in Fig. 3.2.

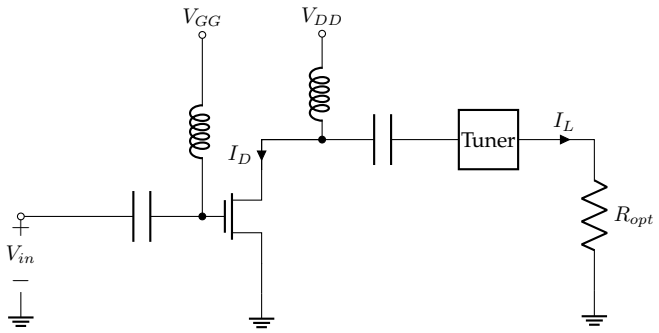


Figure 3.2: Tuned power amplifier

If the input signal is at its maximum level the drain current swings between zero and I_{max} and the voltage between V_k and V_{br}. The device dynamic is fully utilized and the output power is maximum. Evaluating the Fourier series coefficients (Eq. 2.12) for the case where $\Phi = \pi$ gives:

$$I_0 = I_{DC} = \frac{I_{max}}{\pi} \qquad I_1 = \frac{I_{max}}{2} \tag{3.2}$$

The voltage swing is simply $\Delta V = V_{br} - V_k$. All the parameters needed to evaluate the magnitude of the power component at DC and f_0:

$$P_0 = P_{DC} = \frac{V_{DD} I_{max}}{\pi} \qquad P_1 = \frac{1}{2}\frac{\Delta V I_{max}}{4} \tag{3.3}$$

The efficiency at saturation, if V_k is negligible, is thus $\eta = \pi/4 \approx 0.785$.

If the device is assumed to be linear, reducing the drive power of a generic quantity k^2 impacts both the maximum voltage and current swings by the same amount:

$$I_{max,BO} = I_{max}/k \qquad \Delta V_{max,BO} = \Delta V/k \tag{3.4}$$

Figure 3.3 shows the difference between the amplifier working at saturation and the case where the input is backed off by 6dB ($k^2 = 4$).

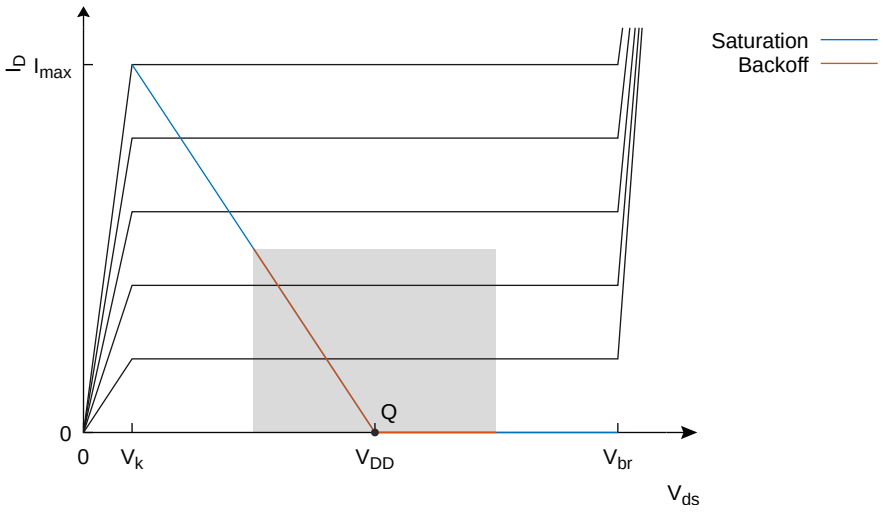


Figure 3.3: Dynamic behaviour at backoff

The shaded rectangle indicates the reduced working zone. The active device is limited and the output power is only a fraction of its maximum value.

For a generic value of k the output power is:

$$P_0 = P_{DC} = \frac{V_{DD} I_{max}}{\pi k} \qquad P_1 = \frac{1}{2} \frac{\Delta V I_{max}}{4k^2} \tag{3.5}$$

This result highlights a significant difference between the DC component amplitude and the fundamental one: the former has a weaker dependence on the factor k than the latter, when the input power level decreases the DC component fades more slowly than the signal power. Recalling the definition of efficiency it is possible to generalize it for an arbitrary input back off level:

$$\eta_{backoff}(k) = \frac{P_1}{P_{DC}} = \frac{\pi}{4k} \frac{\Delta V}{V_{DD}} \tag{3.6}$$

With reference to the previous example, a 6dB decrease of the input power translates to a drain efficiency of $\eta_{backoff}\big|_{k=2} = \pi/8 \approx 0.393$, nearly half of the peak efficiency of a class B amplifier.

3.2 Efficiency Enhancement Techniques

The need for efficient and linear power amplifiers prompted the academic and industrial world to focus on this goal. Several techniques have been

devised starting from the first decades of the 20th century and, as it often happens, many of those have been since forgotten and re-discovered.

This section aims to give a few examples of how the problem was tackled from different angles.

3.2.1 Outphasing

The outphasing technique was first introduced by Chireix [4] in 1935 as an efficient alternative to conventional PAs in Amplitude Modulation (AM) radio transmitters. The very same technique was re-discovered by Cox [5] nearly 40 years later and dubbed as "LInear amplification using Nonlinear Components (LINC)" after its working principle.

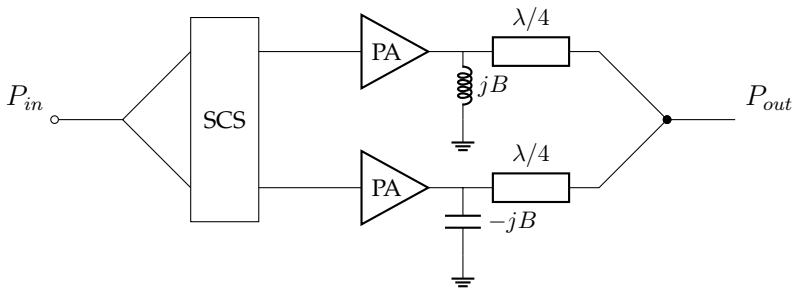


Figure 3.4: Block scheme

As shown in Figure 3.4, the Signal Component Separator (SCS) separates the amplitude-modulated signal [1] S_{in} into two phase-modulated components with opposite phase variations, S_1 and S_2.

$$\begin{aligned} S_{in} = A(t)cos(\omega t) &= \frac{1}{2}\Big(cos(\omega t + \arccos(A(t))) + cos(\omega t + \arccos(A(t)))\Big) \\ &= \frac{1}{2}\left(S_1 + S_2\right) \end{aligned} \tag{3.7}$$

The AM to PM conversion yields two signals with constant envelope as the information is encoded in the differential phase shift. The signals are then feed into two power amplifiers, built upon nonlinear devices, working at saturation and thus really efficient. The original signal waveform is restored by means of summing the two amplified signals on the load resistor R_L.

[1] The technique can also be applied to signals employing both AM and Phase Modulation (PM), the phase content remains intact.

$$S_{out} = G(S_1 + S_2) = G \cdot A(t)cos(\omega t) \tag{3.8}$$

The LINC name is thus justified, the output signal is linearly amplified by nonlinear devices.

The peculiar connection between the amplifier output is the key feature in the outphasing amplifier: the joint action of the two amplifier on the load triggers the load-modulation for the two amplifiers. The load seen from the first device is [3]:

$$Z_1 = \frac{R_L}{2}(1 - j \cot \arcsin A(t)) \tag{3.9}$$

and can be seen as a constant resistive component and a reactive one depending on the outphasing angle and, in turn, on the input envelope. The latter is responsible for the decrease of η in backoff and, if properly compensated by the parallel inductor, allows the amplifier to work with higher efficiency. The same analysis can be carried out for the second amplifier with similar results, this time the reactive part is inductive and is compensate by the parallel inductor.

3.2.2 Envelope Elimination and Restoration

A simpler but similar technique is the Envelope Elimination and Restoration (EER) proposed by Kahn [1] in 1952. The original objective was to amplify signals employing Single SideBand (SSB) modulation, thus encoding information in both the amplitude and the phase.

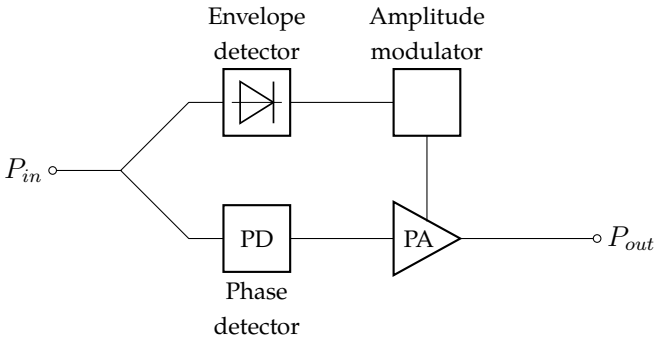


Figure 3.5: Block scheme

In a EER amplifier the input signal is split into a constant-amplitude signal, containing only the phase information, and a variable-amplitude one, the signal envelope. The phase-derived signal is amplified by a PA

that, given the constant input amplitude, is tailored to work in saturation all the time. The envelope, on the other hand, is fed into an amplitude modulator setting the amplifier drain bias voltage. The output signal shape is restored by modulating the amplifier supply voltage and, at the same time, keeps the efficiency constant by making the DC power consumption track the input signal level.

3.3 The Doherty Power Amplifier

The Doherty PA takes its name from its inventor, the American electrical engineer William H. Doherty, who in 1936, only a year after Chireix's paper, came up with the idea for a novel efficiency enhancement technique while working for Bell Labs. The author itself describes its invention in its seminal paper [2] as:

> A new form of linear power amplifier has been developed which removes the limitation of low efficiency inherent in the conventional circuit, permitting efficiencies of 60 to 65 per cent to be realized, while retaining the principal advantages associated with low-level modulation systems and linear amplifiers [...]

Despite being born with vacuum tubes in mind, the idea behind the Doherty PA was quickly adapted to modern solid-state amplifiers, and thanks to its simplicity and elegance it quickly diffused everywhere.

The DPA, pictured in Figure 3.6, consists of two equal power amplifiers, named *Main* and *Auxiliary* respectively, whose output nodes are connected together and to the load by a power combiner.

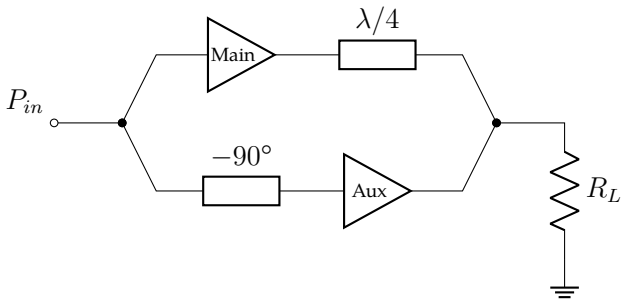


Figure 3.6: Block diagram of a Doherty amplifier

The cornerstone is the smart use of the active load modulation, already exploited in the outphasing PAs, to extend the backoff range for which the efficiency remains high.

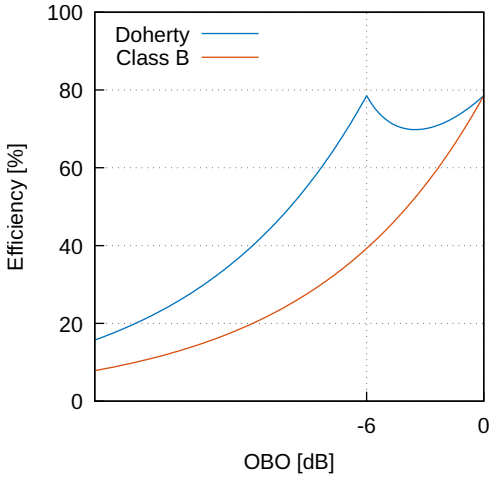


Figure 3.7: DPA drain efficiency

Two regions are defined according to the input drive level or, equivalently, in terms of the backoff level with respect to the maximum output power level.

For low driving powers the Auxiliary device is turned off, leaving only the main responsible for the signal amplification. The load resistance R_L in this region is higher than R_{opt} in order to accomodate the reduced v_{gs} while keeping the voltage swing at its maximum value $\Delta V = \frac{V_{br}-V_k}{2}$. Since the amplifier is driven into early saturation the efficiency ramps up to the maximum value η_{max} as pictured in Figure. 3.7. If the input power is evenly split among the two branches the maximum achievable output power is $3\mathrm{dB}$ less than the saturation value.

As the input drive grows the Auxiliary amplifier starts being operative contributing to the total power transferred by the DPA to the load. The increase of current on the load, the in-phase sum of the output current of each transistor, starts modulating the load seen by the two amplifiers and, in order to keep the Main in saturation, the load seen from its end must be progressively reduced as the input drive decreases.

The junction between the two amplifiers, pushing currents I_1 and I_2 respectively, can be modeled with an equivalent circuit shown in Figure 3.8.

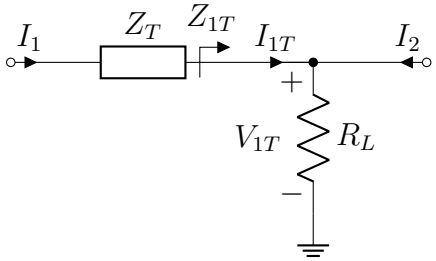


Figure 3.8: Active Load principle

The impedances seen from the two amplifiers are:

$$\begin{aligned} Z_1 &= \frac{Z_T^2}{Z_{1T}} = Z_T^2 \left(\frac{V_{1T}}{I_{1T}}\right)^{-1} = Z_T^2 \left[Z\left(\frac{I_{1T}+I_2}{I_{1T}}\right)\right]^{-1} \\ Z_2 &= \frac{V_{1T}}{I_2} = Z\left(\frac{I_{1T}+I_2}{I_2}\right) \end{aligned} \tag{3.10}$$

The load modulation, thanks to the presence of the $\lambda/4$ inverter, reduces the Main load as the input level grows, keeping its voltage swing at its maximum value and the drain efficiency high. The voltage saturation, combined with the presence of the quarter-lambda transformer, has another interesting side-effect. Given the transmission line impedance matrix:

$$\begin{bmatrix} V_{1T} \\ I_{1T} \end{bmatrix} = \begin{bmatrix} 0 & jZ_T \\ jY_T & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} \tag{3.11}$$

It follows that $I_{1T} = jY_T V_1$: beside the 90 degree phase shift, the "transformed" current depends only on the drain voltage of the Main PA, meaning that in the high-power region its value remains constant.

The gradual load reduction for the Main amplifier forces it to work in saturation when the input drive is high but, on the other hand, the Auxiliary amplifier works with lower efficiency until it reaches the saturation. Figure 3.7 well describes this effect, the inflection in the efficiency curve can be traced back to the non-saturated Auxiliary PA.

In order to keep the Auxiliary turned off when not needed no external circuitry is needed, greatly contributing to the elegance of the DPA design. The Auxiliary amplifier is simply biased in class C, with a biasing "depth" proportional to the selected v_{gs} turn-on voltage: when the gate voltage is below that threshold the active device is off and draws no power, its output is ideally an open circuit so all the power output by the Main goes directly to the load.

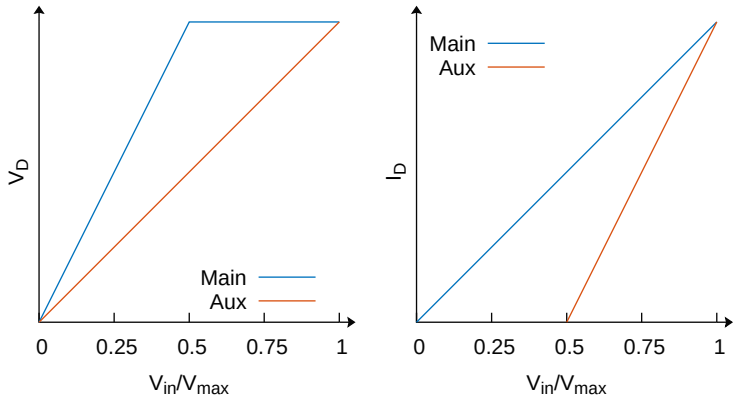


Figure 3.9: Dynamic behaviour

Considering a B-C DPA the two devices exhibit a drain voltage and drain current profile shown in Figure 3.9. This DPA configuration shown is designed assuming the same maximum current level for both the Main and the Auxiliary PA, maximizing the combined output power.

From a physical standpoint the maximum amount of power a FET device can output is connected to its physical size trough the drain current. Modeling the transistor as a constant transconductance device allows to write:

$$i_d \propto G_m \cdot V_{gs} \propto W/L \tag{3.12}$$

The transistor periphery is an important design parameter as it sets the maximum current level for an active device and therefore defines the PA capabilities.

In a symmetrical DPA, where both devices have the same size, it would be physically impossible to have both the Main and the Auxiliary amplifiers reach the same power level in saturation. Identical devices share the same G_m but, as seen in Figure 3.9, the Auxiliary amplifier, accounting for the reduced voltage dynamic, needs a much higher value to catch-up with the Main. Symmetrical configurations are consequently forced to under-use the power capabilities of the Main amplifier and are often called "Doherty-Lite".

Breaking the symmetry and using differently-sized devices solves the problem of having different transconductance values while bringing new ones. This configuration has some practical problems beside requiring the

separate design of two amplifier stages: the range of current ratios that's synthetisable is limited by the available device sizes, thus effectively limiting the designer freedom.

A middle ground between the two solutions mentioned above is the use of a symmetric configuration with unequal input split. Relaxing the restriction on the splitting factor allows the designer to divert more power to the Auxiliary device to make up for the smaller transistor transconductance. Being this a zero-sum game, the increase of power to the Auxiliary branch is followed by a decrease in the Main one, meaning that the DPA gain will surely be lower than expected.

3.4 A practical look at the DPA

It is possible to formulate a compact set of design equations for a generic DPA starting from a description of its behaviour.

The Main and Auxiliary amplifiers are assumed to have different peak current values, whose ratio is indicated as:

$$\gamma \triangleq \frac{I_A^{max}}{I_M^{max}} \tag{3.13}$$

The input drive level is represented by the parameter x ranging from 0, when no signal is applied at the DPA input, to 1, when the input reaches its maximum level. The value x_{break} separates the low-power region from the high-power one.

The Main amplifier output current ramps-up linearly with x and, when $x = x_{break}$ the current amplitude is reduced by a factor $1/\beta$ with respect to the maximum value. This allows to write:

$$I_M = x \cdot I_{max}^M = \begin{cases} \frac{I_M^{max}}{\beta} & \text{for } x = x_{break} \\ I_M^{max} & \text{for } x = 1 \end{cases} \tag{3.14}$$

It follows that the input level threshold is connected to the current backoff level:

$$x_{break} = \frac{1}{\beta} \tag{3.15}$$

The Auxiliary amplifier, as stated before, is powered off in the low-power region and its current starts growing in a linearly with x right after the breaking point:

$$I_A = \begin{cases} 0 & \text{for } x \leq x_{break} \\ I_A^{max}\frac{(x-x_{break})}{(1-x_{break})} = \gamma I_M^{max}\frac{(x-x_{break})}{(1-x_{break})} & \text{for } x > x_{break} \end{cases} \tag{3.16}$$

This framework describes the drain current profile of the two amplifiers in terms of their current ratio or in terms of current backoff: the two parameters, as it will be shown later, are not independent.

$$\frac{I_A}{I_M} = \frac{\gamma}{x}\frac{(x - x_{break})}{(1 - x_{break})} \tag{3.17}$$

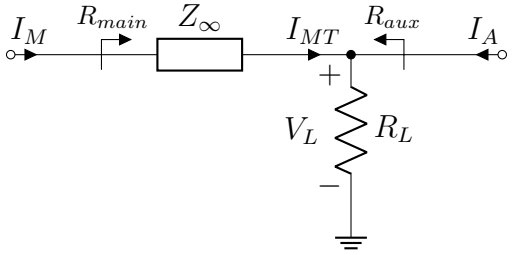


Figure 3.10: Circuital equivalent of the output node

The presence of the quarter-wavelength inverter in the output node makes the evaluation of the currents flowing into R_L tricky as it introduces a $90°$ phase shift. Without loss of generality this detail can be neglected by requiring the presence of a proper phase-compensation network on the input side of the Auxiliary amplifier, as shown in Fig. 3.6.

With reference to Fig. 3.10, the currents flowing into the load are:

$$I_M = \frac{V_L}{Z_\infty} = \frac{R_L(I_{MT} + I_A)}{Z_\infty} = \frac{R_L}{Z_\infty}\left(I_{MT} + \frac{I_A}{I_M}I_M\right) \tag{3.18}$$

and:

$$I_M\left(1 - \frac{R_L}{Z_\infty}\frac{I_A}{I_M}\right) = \frac{R_L}{Z_\infty}I_{MT} \rightarrow I_{MT} = I_M\left(Z_\infty - R_L\frac{I_A}{I_M}\right) \tag{3.19}$$

The loading conditions are thus easily evaluated by applying Eq. 3.11 to the results obtained above:

$$R_{main} = \frac{I_{MT}}{I_M}Z_\infty = \frac{Z_\infty}{R_L}\left(Z_\infty - R_L\frac{I_A}{I_M}\right) \tag{3.20}$$

$$R_{main} = \begin{cases} \frac{Z_\infty^2}{R_L} & \text{for } x \leq x_{break} \\ \frac{Z_\infty^2}{R_L} - Z_\infty \frac{\gamma}{x} \frac{x\beta - 1}{\beta - 1} & \text{for } x > x_{break} \end{cases} \tag{3.21}$$

$$R_{peak} = \frac{V_L}{I_A} = Z_\infty \frac{I_M}{I_A} \tag{3.22}$$

$$R_{peak} = \begin{cases} \infty & \text{for } x \leq x_{break} \\ Z_\infty \frac{x}{\gamma} \frac{\beta - 1}{x\beta - 1} & \text{for } x > x_{break} \end{cases} \tag{3.23}$$

As expected, Eq. 3.21 and Eq. 3.23 show the dependence of the load resistance to the input drive x. Given the general equations that determine those values, some boundary conditions are needed to ensure the DPA is working as expected:

Maximum efficiency at backoff Since the Main amplifier is the only one working at the brink of the low-power region it should work with optimal loading conditions. Considering that the current amplitude for $x = x_{break}$ is scaled by a factor of $1/\beta$, from Eq. 3.21 it follows that:

$$R_{main}|_{x=x_{break}} = \frac{Z_\infty^2}{R_L} = \beta R_{opt,M} \tag{3.24}$$

Maximum efficiency at saturation When $x = 1$ the two devices are working in saturation and their current amplitudes reach the maximum values. Eq. 3.21 and Eq. 3.23, evaluated in this point, give:

$$\begin{cases} R_{main}|_{x=1} = \frac{Z_\infty^2}{R_L} - Z_\infty \gamma = R_{opt,M} \\ R_{peak}|_{x=1} = \frac{Z_\infty}{\gamma} = R_{opt,P} = \frac{R_{opt,M}}{\gamma} \end{cases} \tag{3.25}$$

Combining the conditions imposed to the two amplifier allow to get the following relationships:

$$\gamma = \beta - 1 \qquad Z_\infty = R_{opt,M} \qquad R_L = \frac{R_{opt,M}}{\beta} \tag{3.26}$$

The first relationship is particularly interesting as it ties the maximum current ratio with the backoff level.

While useful in the analysis process, the β parameter is not really useful during the design process as the backoff level is usually specified in terms

of power. It is possible to show that, given the equations of the output power levels:

$$P_{out} = \begin{cases} \frac{1}{2}(V_{br} - V_k) I_M^{max} \beta = P_{sat} & \text{@ saturation} \\ \frac{1}{2}(V_{br} - V_k) I_M^{max} \frac{1}{\beta} = P_B & \text{@ backoff} \end{cases} \tag{3.27}$$

the Output BackOff (OBO) is related to β trough:

$$OBO = 10 \log \left(\frac{P_{sat}}{P_B} \right) = 10 \log \beta^2 = 20 \log \beta \tag{3.28}$$

In order to validate the equations regulating the Doherty PA behaviour, a small design example is in order. Considering two ideal half-watt transistors characterised by:

$$I_{max} = 1A \qquad V_{br} = 1V \qquad V_k = 0V \qquad R_{opt} = 1\Omega$$

and requiring a OBO of $-6\mathrm{dB}$, the design parameters are:

$$\beta = 2 \qquad Z_\infty = 1\Omega = Z_\infty \qquad R_L = \frac{1}{2}\Omega$$

Figure 3.11 shows the results obtained by simulating the designed amplifier using ADS, where the active devices are replaced with equivalent current generators.

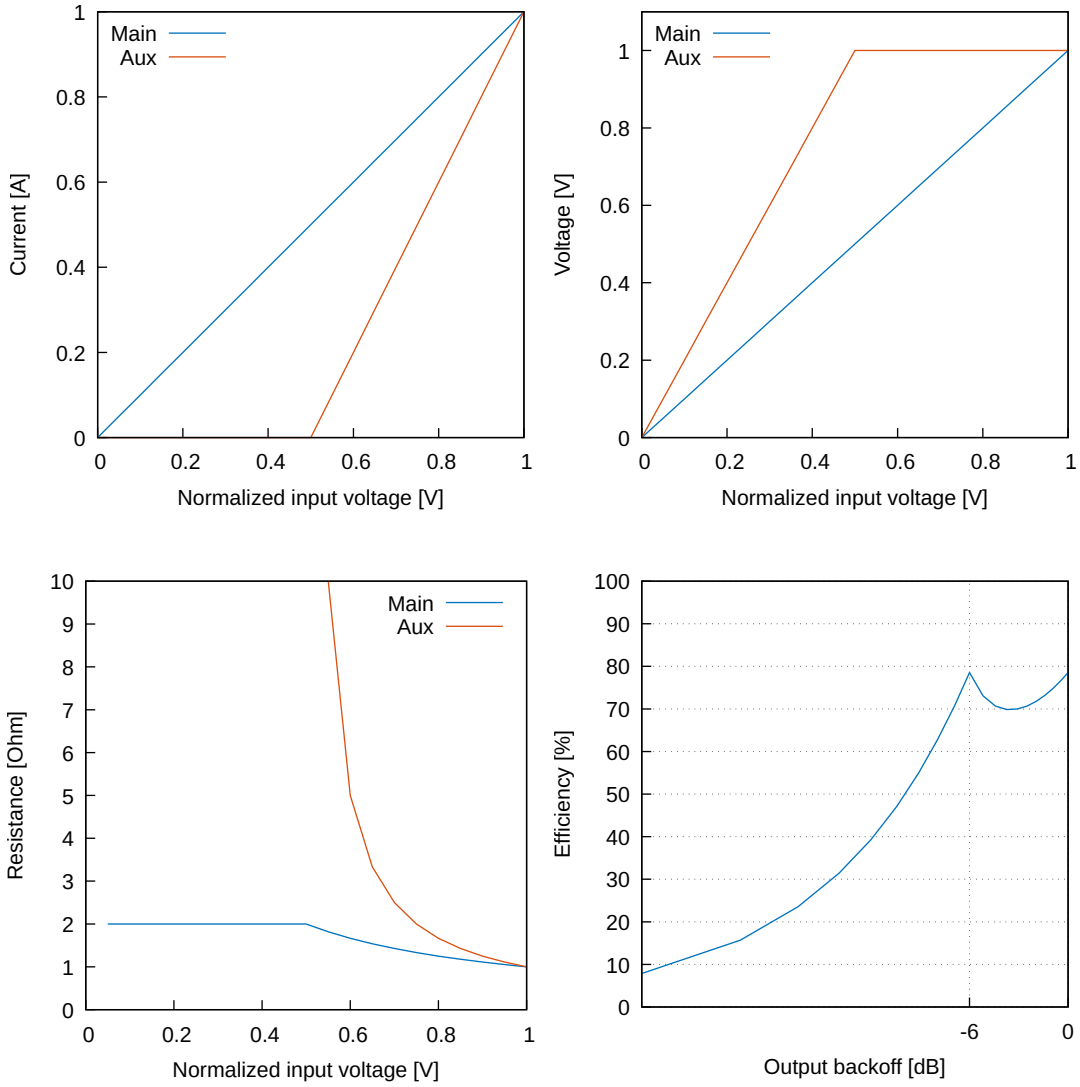


Figure 3.11: Device behaviour

3.5 Beyond the conventional DPA

Following a divide-et-impera approach the idea behind the Doherty PA can be generalized to an arbitrarily large number of devices. The naïve idea is to apply the load modulation trick in a recursive fashion as shown in Figure 3.12. The Main device is brought into saturation by the first Auxiliary device, and this pair of device is in turn brought into saturation by the second Auxiliary device and so on. From a practical standpoint the design of such a system becomes unmanageable once the device count is greater

than three or four as the mutual interaction between the devices increases and the layout becomes complex.

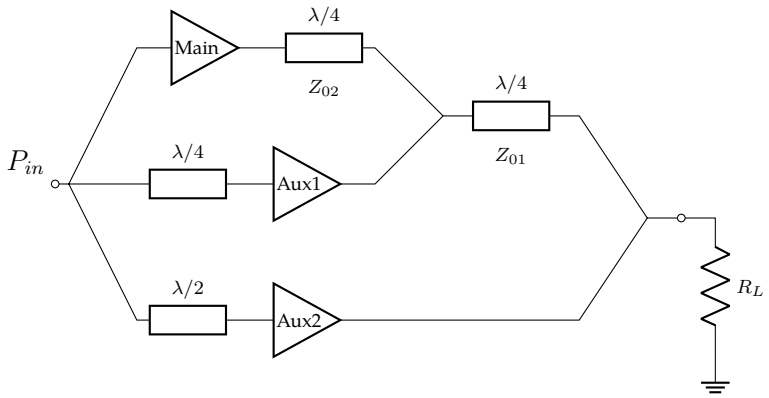


Figure 3.12: 3-stage Doherty PA

Figure 3.13 shows the efficiency levels achievable by 2 and 3 stage DPAs, compared with the well-known efficiency curve of a class B amplifier and an asymmetrical implementation. The overall high-efficiency region is maintained over a wide range of OBO power, employing more devices enlarges the region by adding more efficiency peaks to the chain-shaped efficiency curve.

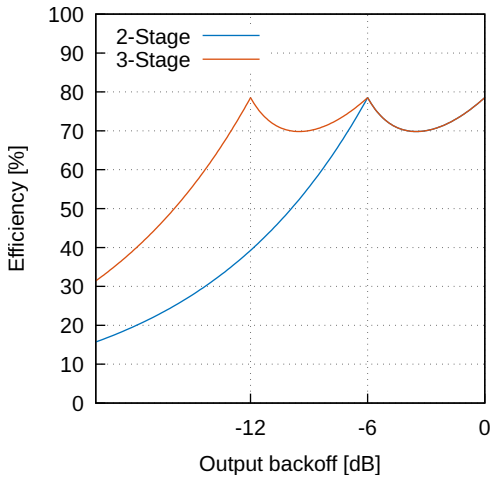
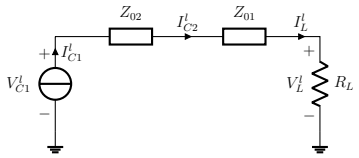


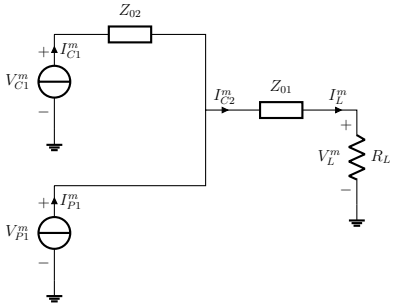
Figure 3.13: Efficiency of multi-stage DPAs

A set of design equations limited to the $N = 3$ case was devised by Srirattana [6] et al. starting from the circuit shown in Figure 3.14. The circuit

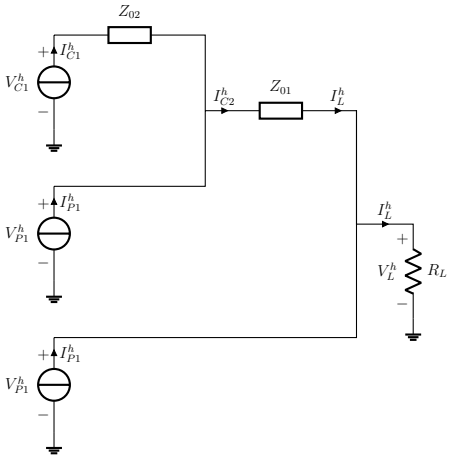
represents the DPA at low-input conditions, medium-input and high-input conditions. For the sake of simplicity the transmission lines are assumed to be lossless, the powered-off amplifiers to be ideal open circuits and the drain bias for the three devices to be the same. These assumptions may not reflect the reality but greatly simplify the calculations.



(a) Low-power region



(b) Medium-power region



(c) High-power region

Figure 3.14: Equivalent circuits for a three-stage DPA

Low-power region In this region the analysis is straightforward. There only active amplifier is the Main one and there is no load modulation happening, the load seen by the active device is:

$$R_{C1} = \left(\frac{Z_{02}}{Z_{01}}\right)^2 R_L \tag{3.29}$$

Medium-power region This region is very similar to a classical two-stage Doherty, the main difference is the presence of an extra Impedance Inversion Network (IIN) before the load. Given the presence of lossless elements the power output by the two devices is completely transferred to the load. After some algebra the equations describing the load value for the Main and the first Auxiliary devices are found to be:

$$\begin{aligned} R_{C1} &= Z_{02} \\ R_{P1} &= \frac{Z_{01}^2 Z_{02}}{R_L Z_{02} - Z_{01}^2} \end{aligned} \tag{3.30}$$

High-power region In this region finding the closed-form representation of the loads require a fair bit of trivial algebra, the resulting load values for the three devices are:

$$\begin{aligned} R_{C1} &= Z_{02} \\ R_{P1} &= \frac{Z_{01} Z_{02}}{Z_{02} - Z_{01}} \\ R_{P2} &= \frac{Z_{01} R_L}{Z_{01} - R_L} \end{aligned} \tag{3.31}$$

In order to choose the width of the high-efficiency region in terms of backed-off power with respect to the maximum value (OBO), the breaking points where the load modulation kicks in must be carefully defined. Given an OBO requirement of B_1 dB with an intermediate OBO level of B_2 dB, both expressed as negative values, the following coefficients can be defined:

$$\alpha_1^2 = 10^{B_1/10} \qquad \alpha_2^2 = 10^{B_2/10} \tag{3.32}$$

Finding the characteristic impedance for the quarter-lambda transformers is a matter of applying once again the law of energy conservation between the active amplifiers and the load.

Low-power region The low-power region ends as soon as the output power hits the first threshold P_{B1}. The only power contribution is given by the Main, the only device powered on.

$$P_L = \frac{V_{DD}^2}{2R_{C1}} = \frac{V_{DD}^2}{2R_L}\left(\frac{Z_{01}}{Z_{02}}\right)^2 = P_{B1} \tag{3.33}$$

$$Z_{01}^2 = 2R_L\frac{P_{B1}Z_{02}^2}{V_{DD}^2} \tag{3.34}$$

Medium-power region The medium-power region ends as soon as the output power hits the second threshold P_{B2}.

$$P_L = \frac{V_{DD}^2}{2R_{C1}} + \frac{V_{DD}^2}{2R_{P1}} = P_{B2} \tag{3.35}$$

$$Z_{02}^2 = \frac{V_{DD}^4}{4P_{B1}P_{B2}} \tag{3.36}$$

The equations can be further simplified and expressed in terms of the coefficients α_n and the DPA load R_L. Substituting 3.36 into 3.34 gives:

$$Z_{01}^2 = 2R_L\frac{P_{B1}}{V_{DD}^2}\frac{V_{DD}^4}{4P_{B1}P_{B2}} = R_L\frac{V_{DD}^2}{2P_{B2}} \tag{3.37}$$

And given the alternative formulation for the power terms:

$$P_{B1} = P_{max}\alpha_1^2 \qquad P_{B2} = P_{max}\alpha_2^2 \qquad P_{max} = \frac{V_{DD}^2}{2R_L} \tag{3.38}$$

The two characteristic impedances can be written as:

$$Z_{01} = \frac{1}{\alpha_2}R_L \qquad Z_{02} = \frac{1}{\alpha_1\alpha_2}R_L \tag{3.39}$$

The α_n coefficients are also useful for determining the maximum current value for each amplifier, or, in other words, the relative size of each active device. A relation on the relative maximum current levels for the different amplifiers can be extracted from 3.31, assuming the same drain voltage V_{DD} across the three devices:

$$\frac{I_{max,P1}}{I_{max,C}} = \frac{\alpha_2(1-\alpha_1)}{\alpha_1\alpha_2} \qquad \frac{I_{max,P2}}{I_{max,C}} = \frac{1-\alpha_2}{\alpha_1\alpha_2} \tag{3.40}$$

Once again the idea of using a symmetric configuration with even input splitting is proven to be incompatible with the enlargement of the covered

OBO region. The use of differently-sized devices, drain bias modulation or unequal power splitters at the input is thus needed in order to raise the gain level.

The choice of an optimum load value in this case, especially in light of the need to use differently-sized devices, is not straightforward. A smart solution to this problem [6] is to consider the DPA behaviour in saturation: the input splitting is heavily biased towards the last Auxiliary device, it makes sense to ensure the load it sees is the optimum one to increase the gain. From 3.31 the following can be obtained:

$$R_{P2} = R_L \frac{Z_{01}}{Z_{01} - R_L} = R_{opt} \rightarrow R_L = (1 - \alpha_2) R_{opt} \tag{3.41}$$

The conventional symmetric three-stage Doherty doesn't fully exploit the devices full potential due to its recursive nature. To better understand this problem it is useful to start from a small design example. The very first step is to define the two OBO levels, in this case $B_1 = -12\mathrm{dB}$ and $B_2 = -6\mathrm{dB}$, together with the relative coefficients $\alpha_1 \approxeq 0.251$ and $\alpha_2 \approxeq 0.5$.

Applying 3.40 yields:

$$\frac{I_{max,P1}}{I_{max,C}} = 3 \qquad \frac{I_{max,P2}}{I_{max,C}} = 4$$

It can be noted how the output current for the Main amplifier is extremely low with respect to the other two devices. As soon as the device enters the medium-power region the load modulation starts affecting the Main device and keeps it in saturation, but when the DPA enters the high-power region the modulation stops abruptly.

In hindsight this result is not surprising, Fig. 3.14 shows the quarter-lambda Z_{02} connected to an active device on both ends: in the high-power region the voltage on both ends is kept constant to the highest value V_{DD} and, according to 3.11, this means the current is constant too. The Main device is thus forced to work at reduced operation in the last part of the OBO, affecting the DPA gain.

Figure 3.15 shows the results obtained by simulating the designed amplifier using ADS, where the active devices are replaced with equivalent current generators.

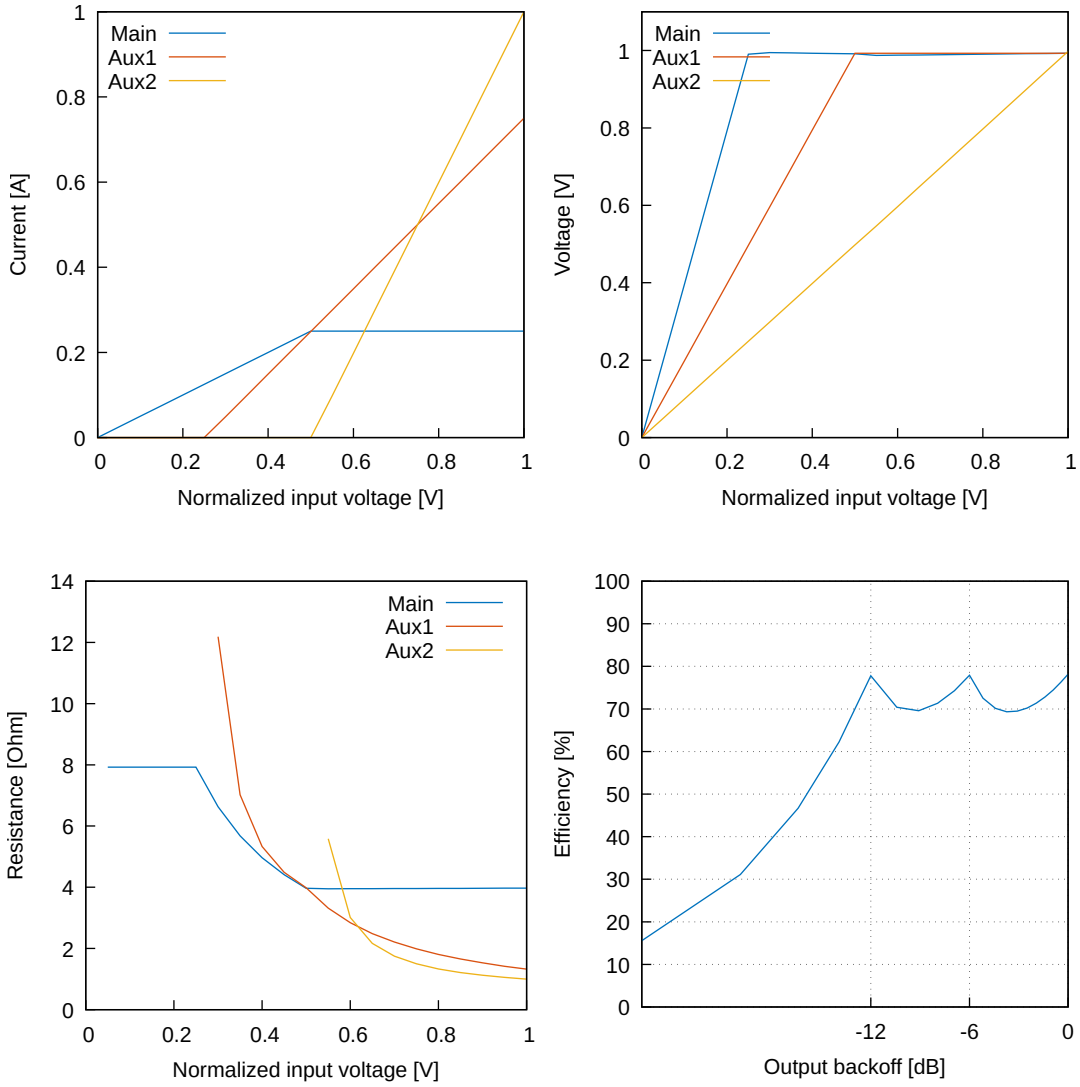


Figure 3.15: Device behaviour

But what happens when the drain current for the Main amplifier is not kept constant and is linearly ramped up instead?

Breaking out of the equilibrium condition disrupts the DPA behaviour in backoff conditions, as shown in Figure 3.16. For $v = 0.25$ the output power is basically halved from the expected value and so is the drain efficiency. When the amplifier enters the medium-power region the incorrect load modulation begins to reduce R_{main}, effectively choking the device drain: the output power keeps sinking until the second Auxiliary device kicks in. Once the three amplifiers are turned on the DPA is still not

working as intended, but on the right track. When the three devices finally reach their maximum current amplitudes the output power and efficiency return to their expected levels.

While extreme, this example highlights how fundamental it is for the Main current profile to be as close as possible to the theory. Ensuring the current saturation for the Main device is not easy and is typically achieved by means of a feedback loop that regulates the input splitting according to the input drive, greatly increasing the amplifier complexity.

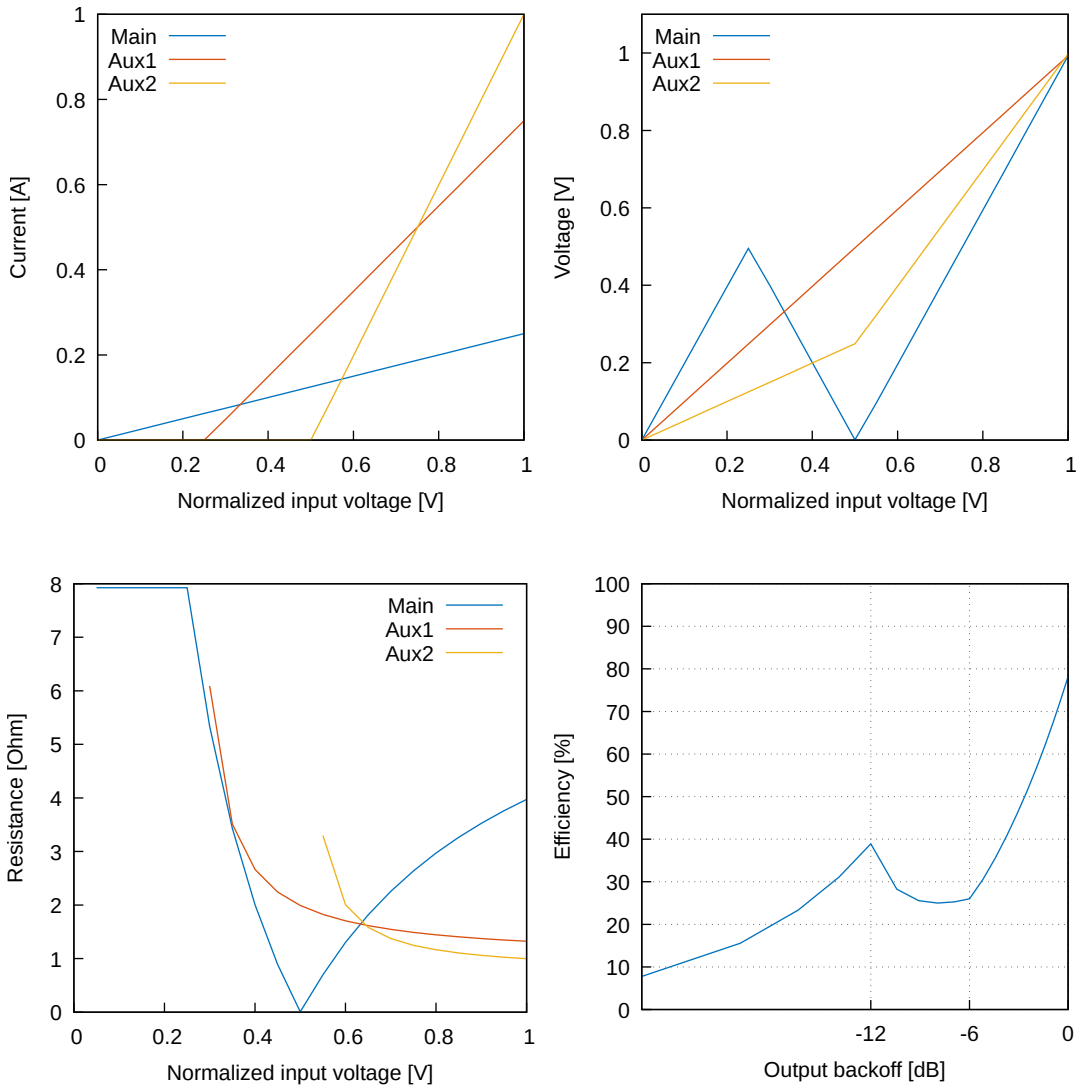


Figure 3.16: Device behaviour w/ linear Main current profile

3.6 3-Stage DPA – with a twist

The limitations of the conventional three-stage DPA have been analyzed in depth. The focus is mostly on the redesign of the output combiner and the accurate choice of the biasing arrangement for each device. Neo et. al proposed an interesting approach, shown for three-devices only but easily extensible to a generic number of devices, where the output combiner and the load R_L are modeled as a 3-port black-box. Ohm's law links the current and voltages seen at each of the three ports at the two backoff points $B_{2,1}$ and at full-drive condition F:

$$\begin{bmatrix} \underline{V}_F \\ \underline{V}_{B_1} \\ \underline{V}_{B_2} \end{bmatrix} = \begin{bmatrix} [Z] & [0] & [0] \\ [0] & [Z] & [0] \\ [0] & [0] & [Z] \end{bmatrix} \begin{bmatrix} \underline{I}_F \\ \underline{I}_{B_1} \\ \underline{I}_{B_2} \end{bmatrix} \tag{3.42}$$

The load modulation is ensured by forcing the voltage saturation condition and the proper current level to 0 when a device should be turned off. Solving the set of equations in the several $z_{i,j}$ unknowns, and then synthesizing the resulting scattering matrix are the following steps if this design methodology is adopted.

A significant result in this field was the discovery of a novel output combiner that avoids most of the issues that plague the conventional DPA. This solution was devised by Gajadharsing et al. [7] at NXP (now known as Ampleon), consisting of a small but effective modification to the way the load modulation is applied.

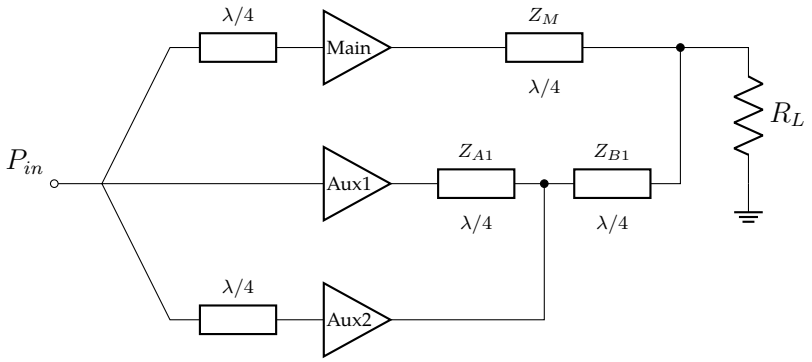


Figure 3.17: Block scheme of the NXP DPA

Comparing the new DPA, shown in Figure 3.17, with the classic implementation, shown in Figure 3.12, gives a glimpse of the underlying difference between the two: the "recursive" load modulation is abandoned in

favour of a better scheme where all the device loads are modulated at the same time.

The quarter-wavelength inverters ensure the inactive amplifiers have no effect on the active one:

- **Low-power region**: the Main is the only active device. Z_{A1} and Z_{B1} ensure the load effect on the output node is null.
- **Medium-power region**: the Main and the first Auxiliary devices are active, the former modulates the load of the latter by pushing current into the output node. The second Auxiliary device, with its infinite output impedance placed in parallel with the first Auxiliary finite one, doesn't affect the modulation.
- **High-power region**: the three devices are all active at the same time. The second Auxiliary device modulates the load for the Main *and* the first Auxiliary this time.

The phase delay introduced by the quarter-wavelength transformers in the signal path is taken into account when designing the input network: the input to the three branches is delayed to make sure the output signals are in phase.

The main advantage of this topology is the ability of driving the three amplifiers up to arbitrary values of maximum current, breaking free from the limitations described in Eq. 3.40. Symmetric configurations become possible, saving a great amount of time for the designer who has to focus on a single amplifier cell. Figure 3.18 shows the dynamic load lines of every amplifier for such a configuration.

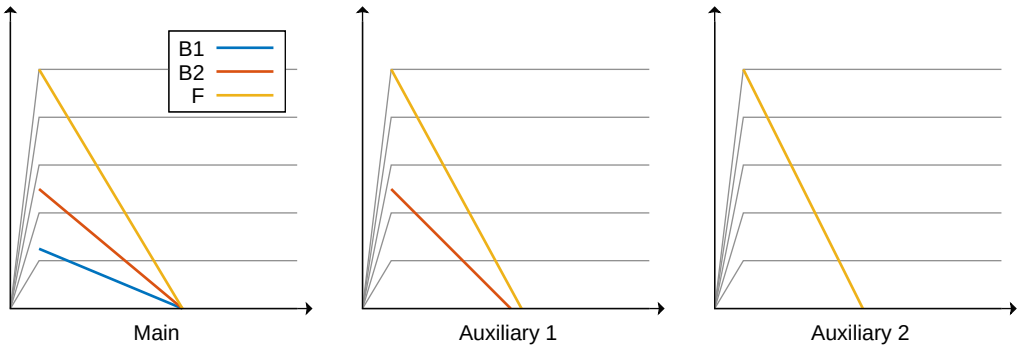


Figure 3.18: Load modulation for a three-stage DPA

The following design equations are derived from the extensive work done by Piazzon [8] on this topic. The starting point is again the determination of the two alpha coefficients relative to the selected backoff levels B_1 and B_2, as done in the previous section.

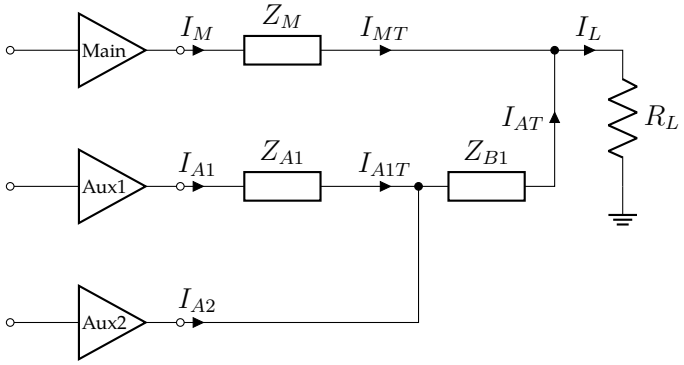


Figure 3.19: Annotated block scheme of the three-stage DPA

With reference to the current and voltages shown in Figure 3.19, the power balance at backoff and saturation can be written as:

$$\begin{cases} P_{B1} &= \frac{I_{MT,B1}^2 R_L}{2} = P_{max}\alpha_1^2 \\ P_{B2} &= \frac{(I_{MT,B2}^2 + I_{AT,B2}^2) R_L}{2} = P_{max}\alpha_2^2 \\ P_{max} &= \frac{(I_{MT,F}^2 + I_{AT,F}^2) R_L}{2} \end{cases} \tag{3.43}$$

The subscripts ending with *-t* represent the currents "transformed" by the quarter-wavelength adapters according to Eq. 3.11. It's worth noting that, after the first backoff point is reached, V_M remains constant thanks to the load modulation, making $I_{MT,B1} = I_{MT,B2} = I_{MT}$ constant in turn. This simplification turns Eq. 3.43 into an easily solvable set of three equations in three unknowns:

$$\begin{aligned} I_{MT} &= \alpha_1 \sqrt{\frac{2P_{max}}{R_L}} \\ I_{AT,B2} &= (\alpha_2 - \alpha_1) \sqrt{\frac{2P_{max}}{R_L}} \\ I_{AT,F} &= (1 - \alpha_1) \sqrt{\frac{2P_{max}}{R_L}} \end{aligned} \tag{3.44}$$

Armed with the knowledge of the currents flowing into the load, finding the characteristic impedances values is a matter of applying Eq. 3.11 (the phase shift introduced by $\pm j$ is taken into account by the input network) and some algebra:

$$\begin{aligned} Z_M &= \frac{V_{DD}}{I_{MT}} = \frac{V_{DD}}{\alpha_1} \sqrt{\frac{R_L}{2P_{max}}} \\ Z_{B1} &= \frac{V_{DD}}{I_{AT,F}} = \frac{V_{DD}}{1 - \alpha_1} \sqrt{\frac{R_L}{2P_{max}}} \\ Z_{A1} &= \frac{V_{DD}}{I_{A1T}} = \frac{V_{DD}}{V_L} Z_{B1} = \frac{V_{DD}^2}{1 - \alpha_1} \frac{1}{I_{MT} + I_{AT,B2}} \sqrt{\frac{R_L}{2P_{max}}} = \\ &= \frac{V_{DD}^2}{2\alpha_2(1 - \alpha_1) P_{max}} \end{aligned} \tag{3.45}$$

The set of design equations is complete. The design parameters are the target output power P_{max}, the peak voltage amplitude across the active devices V_{DD} and the external load R_L.

A significant difference with the previous implementation is that no device is directly connected to R_L: the voltage across it can be different than the one of the saturated active devices, turning this parameter into a free variable that, if set to the canonical value of 50Ω, avoids the need for an extra impedance matching network.

The different output combiner is also affecting the devices sizing ratios, as seen by evaluating the devices output current at full drive:

$$
\begin{aligned}
I_{M,F} &= \frac{(I_{MT} + I_{AT,F})R_L}{Z_M} = \alpha_1 \frac{2P_{max}}{V_{DD}} \\
I_{A1,F} &= \frac{V_{DD}}{Z_{A1}} = \alpha_2(1-\alpha_1)\frac{2P_{max}}{V_{DD}} \\
I_{A2,F} &= I_{L,F} - I_{M,F} - I_{A1,F} = (1-\alpha_1-\alpha_2(1-\alpha_1))\frac{2P_{max}}{V_{DD}}
\end{aligned}
\tag{3.46}
$$

Taking the current values for the two Auxiliary amplifiers and normalizing them to the value of the Main device gives:

$$
\frac{I_{A1,F}}{I_{M,F}} = \frac{\alpha_2(1-\alpha_1)}{\alpha_1} \qquad \frac{I_{A2,F}}{I_{M,F}} = \frac{1-\alpha_1-\alpha_2(1-\alpha_1)}{\alpha_1}
\tag{3.47}
$$

Once again the device sizes depend on how large the requested high-efficiency OBO is. The different topology allowing the full use of the Main device has a great impact on the device sizing requirements: a DPA design with $-12\mathrm{dB}$ of OBO and an intermediate level of $-6\mathrm{dB}$ yields the following ratios:

$$
\frac{I_{A1,F}}{I_{M,F}} = 1.5 \qquad \frac{I_{A2,F}}{I_{M,F}} = 1.5
$$

The two Auxiliary amplifiers have the same size and are only slightly bigger than the main. Symmetric configurations are also favorable in this case, the Main device would still be underutilized but not by a large amount.

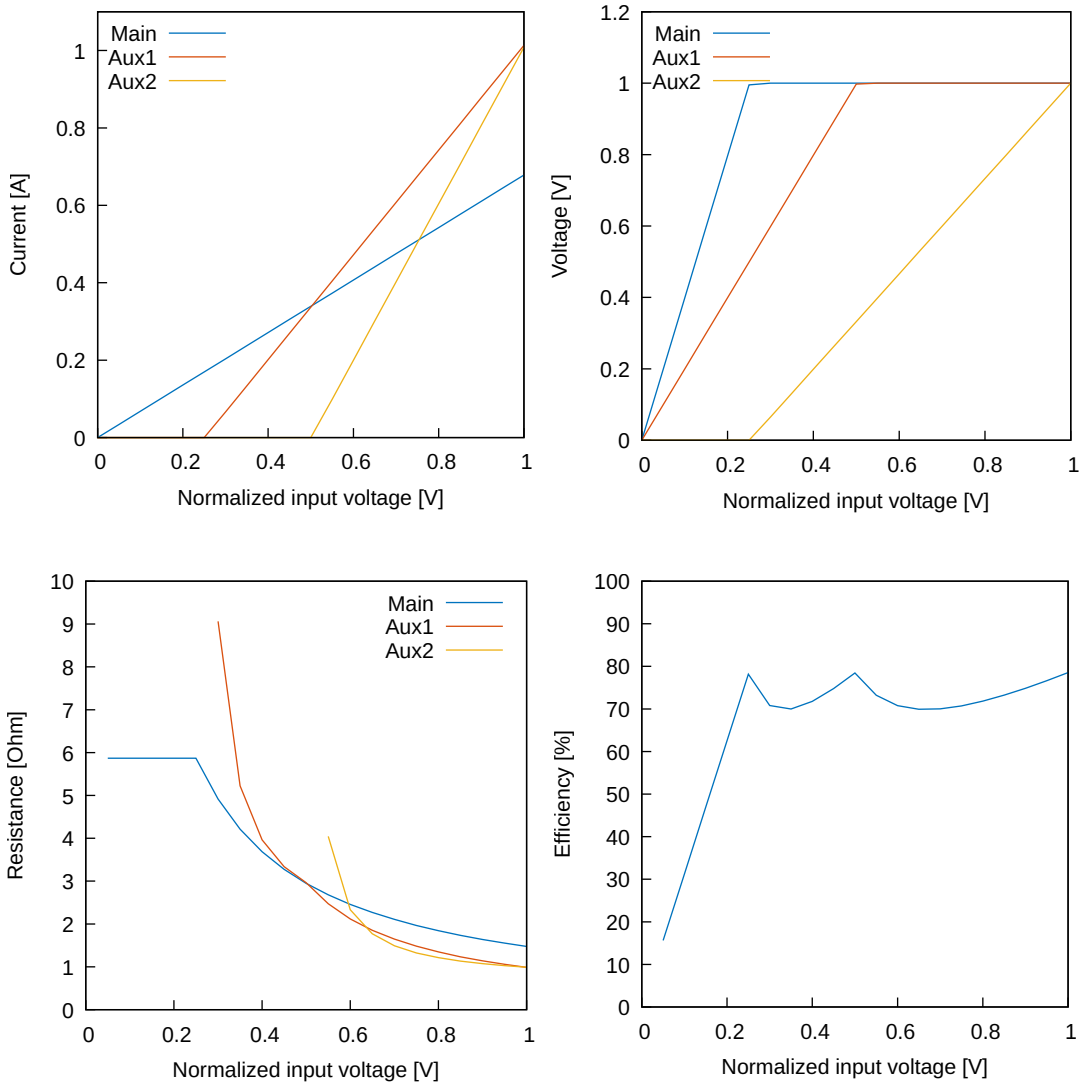


Figure 3.20: Device behaviour

Chapter 4

Design examples

4.1 Introduction

The previous chapters laid the theoretical groundwork for the practical design of two devices: a symmetric two-stage and a three-stage Doherty PAs. The main aim here is to first and foremost validate the models used throughout the analysis of the Doherty inner workings, together with the obtained closed-form design equations.

4.2 Device Modeling

The most important step in the design of a RF circuit is the selection of a suitable model for the active device. While calculations carried out with pencil and paper remain an helpful tool in the preliminary design process, a Computer-Aided Design (CAD)-based approach is essential in this field.

Power amplifiers, as already stated, deal with signals showing large current and voltage swings, dictating the need for a more complex large-signal model rather than a relatively simpler small-signal one. The extra complexity of a large-signal model stems from the need to model several physical behaviours that, unlike their small-signal counterparts, if ignored can render the model completely useless for the analysis purposes. The high operating frequencies are also a source of additional complexity as many effects are also frequency-dependent.

The different device models for a FET device can be roughly divided in two macro classes, depending on their approach to the problem.

S-parameter models This kind of model describes the FET device as a three-port black-box device, forgoing any link with the circuital elements.

The scattering parameters (often abbreviated as S-parameters) are derived from a sample specimen biased at a certain working point and with an input at a given frequency f. The S_{ij} parameters are enough to locally approximate the transistor behaviour, CAD programs are able to synthesize simulation-blocks out of the collected measurements.

The downside to this approach is the heavy dependance on the measurement conditions of the S-parameters, the model is unable to give meaningful results outside of the tested working conditions. While it is possible to sample the device behaviour under a wide range of bias arrangements and operating frequencies it is often not practical nor economically viable. This kind of modeling solution is employed where the device is operated in small-signal behaviour, the obtained model is unfit for large-signal simulations.

Equivalent-circuit models This kind of model describes the FET device in terms of an equivalent circuit approximating the behaviour of the transistor under a generic working point and frequency. This approach is much more general with respect to the aforementioned one based on S-parameters but requires a great deal of attention in the formulation of the model.

Being this a large-signal model, many the active and passive components used in it are nonlinear and generically described as functions of the driving quantity. Moreover the behaviour of the gate junction and the device breakdown must be somehow modeled too: when the input signal is small this two problems can be safely neglected, the operating input swing makes it hard to trigger them.

An ideal model would need a large number of elements, and parameters, to perfectly trace the transistor behaviour. Existing models strike a balance between accuracy and practicality by employing a limited number of tunable parameters. The set of parameters is evaluated after fitting the data obtained from a statistically-significant number of empirical observations.

Both the models are thus derived from measurements, but the circuital description offers a significant advantage over a S-parameter one: the results can be scaled upwards and downwards together with the device periphery. This advantage, together with the frequency and bias independence of the representation, make the equivalent circuit models a practical choice.

Among the different models employed for different FET devices, the Curtice-Ettenberg cubic nonlinear model [9] is conceived for the simulation of GaAs-based MESFETs.

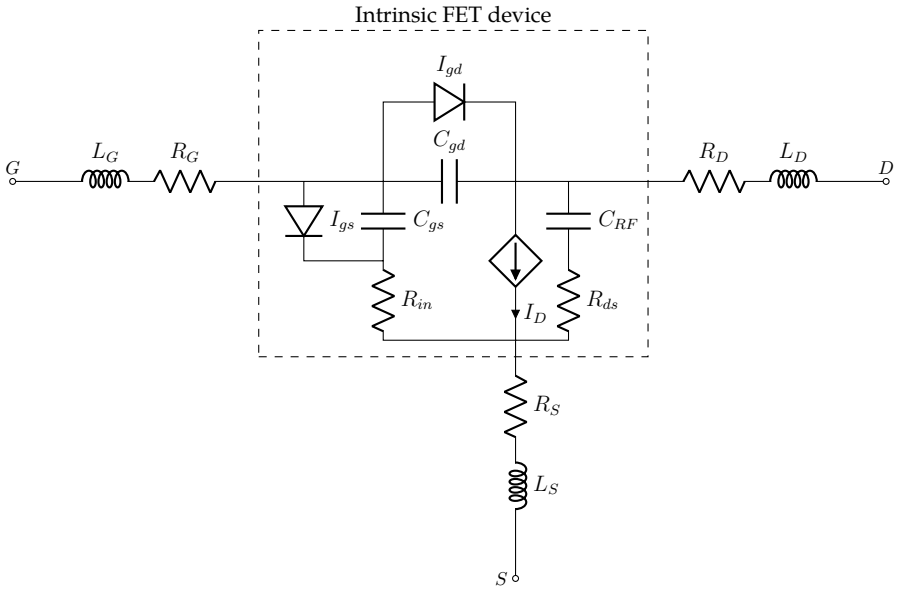


Figure 4.1: Large signal FET model

The equivalent circuit is pictured in Fig. 4.1; when compared to the usual small-signal quadratic model used in pencil and paper calculations the differences are few but significant.

At the heart of the transconductance device is the Voltage Controlled Current Source (VCCS) whose output current is described as:

$$I_D = (A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3) \tanh(\gamma V_{DS}) \tag{4.1}$$

The third-degree polynomial gives an extra degree of freedom with respect to the second-degree one employed by the quadratic Curtice model: the device transconductance, defined as $G_M = \frac{\partial I_D}{\partial V_{gs}}$, is not linearly dependent on the input and the extra terms allows to properly model this detail.

In 4.1 A_0 defines the amount of current flowing when no gate voltage is applied while A_1 serves the same purpose of g_m, the transconductance, in a small-signal quadratic model. The γ defines the impact of the channel length modulation on the saturation current.

The driving quantity is not the gate voltage itself but V_1, defined as:

$$V_1 = V_{gs}(t - \tau)[1 + \beta(V_{ds}^0 - V_{ds}(t))] \tag{4.2}$$

This quantity, where V_{ds}^0 is the drain voltage for which the A_n coefficients are evaluated, takes into account for several effects:

- The gate delay τ, the time needed for a ΔV on v_{gs} to be reflected on I_D.

- The channel modulation effect, via γ.
- The channel pinch-off effect, via β.

Two reverse-biased diodes are placed across the gate-drain and gate-source nodes, serving a two-fold purpose: their presence models the current flow when the v_{gs} becomes too high and the device breakdown condition and, at the same time, the nonlinear capacitances C_{gs} and C_{gs}. These two quantities are described in terms of the diode depletion capacitances as:

$$C_{gs} = \frac{C_{gs,0}}{\sqrt{1 - \frac{V_{gs}}{V_{bi}}}} \qquad C_{gd} = \frac{C_{gd,0}}{\sqrt{1 - \frac{V_{gd}}{V_{bi}}}} \tag{4.3}$$

Where $C_{gs,0}$ and $C_{gd,0}$ are the measured capacitance values at zero-bias and V_{bi} is the gate built-in potential. The equations are valid only when the gate to source and gate to drain voltage is below V_{bi} or, in other words, when the gate junction is not forward biased.

The series C_{RF}-R_{ds} dispersion network models the change of output conductance at high frequency: when C_{RF} becomes a short the whole R_{ds} is put in parallel with the output load, therefore increasing the output conductance.

4.3 Active device characterization

The active device employed for the following designs is modeled using the aforementioned cubic Curtice model. The device is supposed to behave as a power FET able to output around $0.85\,W$ when working in optimal conditions. The cubic polynomial is defined as:

$$P(x) = A_0 + A_1 \cdot x + A_2 \cdot x^2 + A_3 \cdot x^3$$

$$A_0 = 0.125 \qquad A_1 = 0.1097 \qquad A_2 = 0.003475 \qquad A_3 = -0.0023$$

and is plotted for several values of the driving quantity V_1 in in Fig. 4.2.

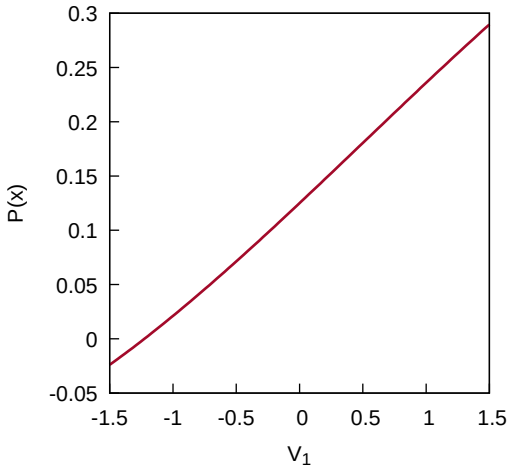


Figure 4.2: Cubic polynomial

The drain current is modeled by taking into account the maximum pinch-off voltage VTO as:

$$I_D(V_1, V_{DS}) = \begin{cases} P(V_1)\tanh(\gamma V_{DS}) & V_1 > VTO \\ P(VTO)\tanh(\gamma V_{DS}) & V_1 \leq VTO \end{cases} \tag{4.4}$$

For values below the pinch-off the drain current drops down to a constant small quantity.

Different RF CAD packages implement the Curtice-Ettenberg model in different (and often incompatible) ways and, speaking of differences, the implementation in Keysight Advanced Design System (shortened to ADS) has a peculiar way of evaluating the pinch-off voltage. While other implementations honour the VTO parameter specified by the user, this implementation performs several intermediate calculations to derive it from the polynomial representation of the drain current. A suitable value V must satisfy the following invariants:

$$\begin{cases} f(V) = A_0 + A_1 \cdot V + A_2 \cdot V^2 + A_3 \cdot V^3 \leq 0 \\ f'(V) = 0 \\ f''(V) > 0 \end{cases}$$

The advantages of this method are two-fold as it allows to avoid introducing meaningless parameters that may influence the numerical stability of the simulation and, at the same time, serve as a way to double-check

the correctness of the A_n values. With reference to Fig. 4.2, the voltage $V_i \approx -1.2$ satisfies the requirements for being the threshold value VTO.

Real transistors are characterized by a large number of spurious resistive and reactive components, called *parasitic* elements. This set of elements can be generally divided in *intrinsic* elements and *package* ones on the basis of whether they are introduced by the FET physical structure or by wires and bonding fixtures. In order to keep the model as close as possible to the reality, several main parasitic elements are embedded with the following values:

L_D	$12\,pH$	R_D	$0.8\,\Omega$	L_S	$0.2\,pH$	R_S	$0.2\,\Omega$
L_G	$12\,pH$	R_D	$0.4\,\Omega$	C_{gs}	$0.8\,pF$	C_{gd}	$0.5\,pF$
C_{ds}	$0.08\,pF$	R_{gd}	$0.e\,\Omega$	R_{ds}	$1\,M\Omega$	R_{in}	$5\,\Omega$

Figure 4.3 shows the results obtained by running the modeled device trough a small-signal simulation with the aim of obtaining the DC characteristics.

The device transconductance in small-signal regime is also pictured with its non-constant growth after the threshold gate voltage is crossed. While useful for a general assessment of the device characteristics, this quantity is not really useful in the design of a device operating in large-signal conditions as it will not keep a steady value when the input level is raised. Nevertheless, the assumption of a constant transconductance is often adopted for simplifying the calculations, some manual tweaking of the obtained values is in order to get satisfying results.

The breakdown phenomena occurs for a source-drain voltage of around $50\,V$ while the knee voltage is around $3\,V$, the best placement for the drain bias voltage is right in the middle of the usable V_{DS} region, leaving a generous safety margin to avoid the breakdown region:

$$V_{DSS} = 18\,V$$

Estimating the admitted voltage swing for the gate is slightly more involved. Firstly the definition of a maximum drain current value that should not be crossed is required, avoiding the possibility of forward-biasing of the gate junction. To avoid this the gate junction the maximum target drain current is chosen to be $I_{DSS} = 0.26A$, corresponding to $V_{gs} \approx 0.1\,V$, while making sure the gate junction does not become forward-biased. The FET channel is completely blocked for $V_{gs} \leq -1.2\,V$, meaning that the drain current is negligible and approximately zero below that point. The whole usable range of input voltages for the amplifiers considered here is between the two voltages estimated above.

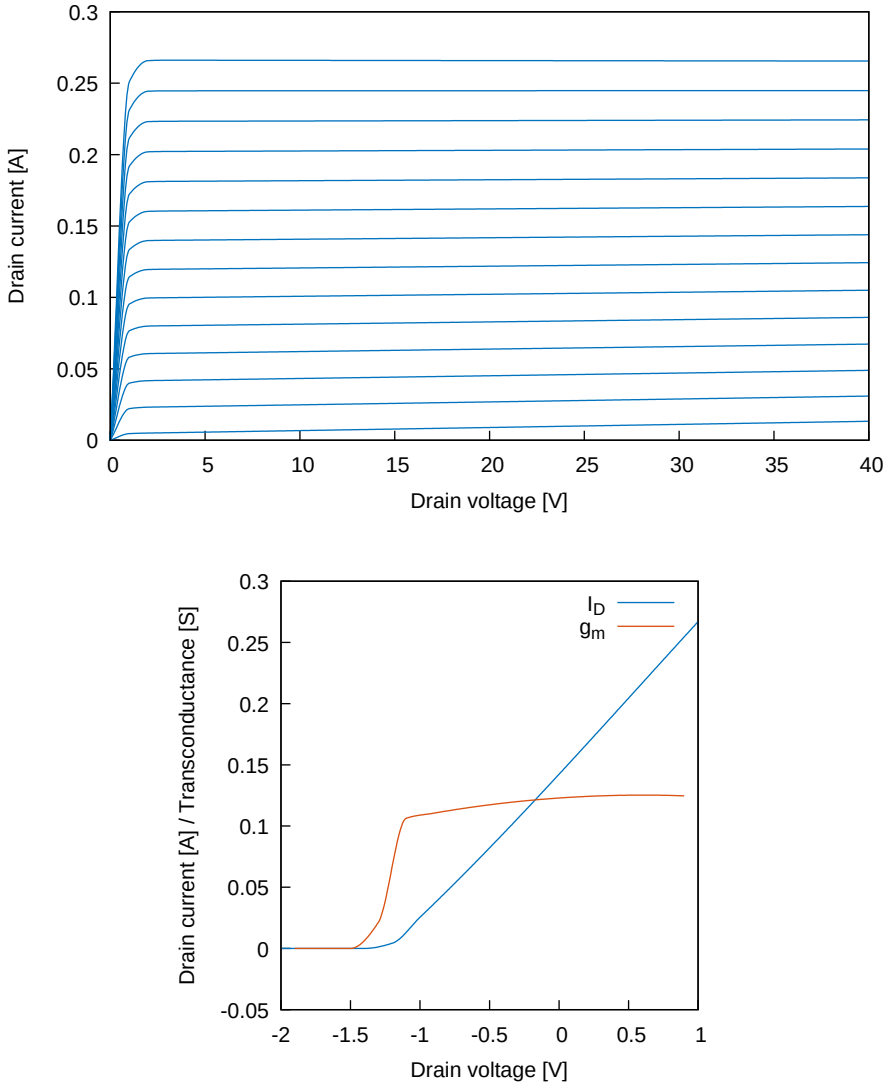


Figure 4.3: FET drain current behaviour

Figure 4.4 shows the results of a Large-Signal S-Parameter (LSSP) simulation run with the aforementioned transistor. This kind of simulation is much more useful than its small-signal counterpart as it allows the designer to have a rough idea of how the nonlinearities affect the input and output impedances.

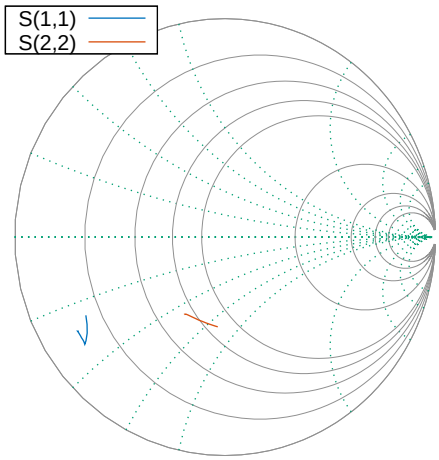


Figure 4.4: Small-signal S-parameters

For the purpose of analyzing the load lines right at the device's intrinsic plane, the effective value of the parasitic reactances on the drain side must be evaluated. This computation can be performed [1] by biasing the device gate below the threshold value, making the VCCS an open-circuit, and tuning the (negative) values of a series L and a parallel C until the reflection coefficient at the output port resembles the value of an open-circuit. While the negative component values have no practical meaning, their magnitude offers a glimpse of the true composition of the output reactance, including but not limited to the Miller effect.

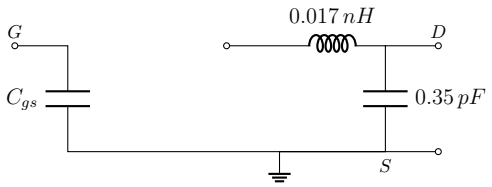


Figure 4.5: Simplified FET model for parasitics computation

The device is not unconditionally stable. The geometrically-derived stability factor for the load side μ allows to define a single necessary and sufficient condition for the device to be unconditionally stable. The μ factor is defined as:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \cdot \Delta| \cdot |S_{12}S_{21}|} \tag{4.5}$$

[1] This procedure was kindly suggested by Chiara Ramella

where Δ is the determinant of the S-parameter matrix and $\mu > 1$ is enough to ensure the unconditional stability at the working frequency. For the device at hand the value is approximately 0.31, Figure 4.6 shows a clearer picture of the potential input and output loads that may cause the device to be unstable, calculated over a frequency range of $2\,GHz$ to $4\,GHz$. Considering that in a Doherty amplifier the modulated loads are all expected to be near the real axis, the device conditional stability is not a problem on the load side. On the other hand some problems may arise on the input side, if a conjugate match is achieved the source load may be well into the unstable circle.

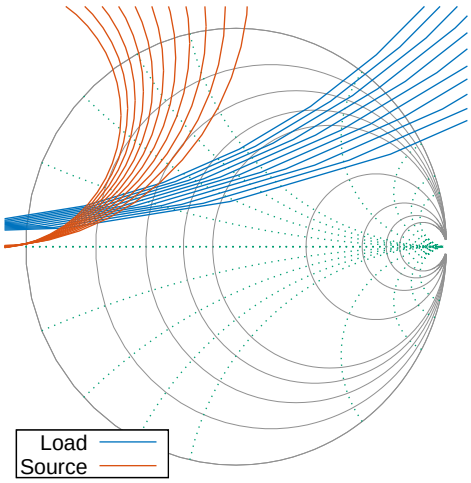


Figure 4.6: Load and source stability circles

A parallel RC compensation network can be introduced in series with the gate terminal in order to provide a better stability margin. A $R = 12\,\Omega$ in parallel with $C = 5\,pF$ is enough to move the unstable region towards the edge of the Smith chart while affecting the gain by only $1\,dB$.

4.4 Design – Two-stage

The previous chapter introduced a set of closed-form analytical equations for the design of a "conventional" two-stage Doherty PA, this section aims to validate the results by applying the design rules to a real design project: a symmetric DPA with $6\,dB$ of OBO, working at $f_0 = 3\,GHz$ and an output power of $P_{max,DPA} = 1.8W$.

Before attempting the design it is useful to make a short detour and spend a few words on the topic of linearity. This work is mostly focused on the world of high-efficiency power amplifiers but, in order for the device to be useful in real world scenarios, an eye should be also kept on the AM-AM distortion: the overall gain for a PA is definitely not constant and depends on the chosen bias points for the N devices.

Across the whole low-power region ($x < x_{break}$) the only contribution to the gain figure is given by the main device or, in other words, by an amplifier with class AB bias. This guarantees the gain is pretty high when the input level is small, approaching the levels of a class A amplifier, with a sharp roll-off when the input level becomes high enough to have the drain current waveform clip to zero. The decline of the Main amplifier's gain continues throughout the high-power region ($x > x_{break}$) but this time is opposed by the contribution coming from the Auxiliary amplifier being on. The two effects combine together and shape the total gain of the DPA and by harnessing the complementary behaviour shown by the two amplifiers one can try to offset the inevitable gain decrease and keep the gain almost constant in the high-power region.

A useful parameter that can help with the choice of the bias point ξ for the Main amplifier is the Linearity Factor (LF) [10]. This quantity is defined as the difference between the output power of the DPA at hand and the one of an ideal amplifier with the same maximum power and behaving linearly, evaluated above x_{break}:

$$LF = \frac{1}{1 - x_{break}} \int_{x_{break}}^{1} \left(P_{out,DPA}(x) - (P_{max,DPA} \cdot x^2)\, dx \right) \tag{4.6}$$

The ideal condition is to keep $LF = 0$ or at least as close to zero as possible. Figure 4.7 [8] provides a helpful graphical method for determining a suitable value of bias point by plotting the relationship between the OBO and the ξ when $LF = 0$.

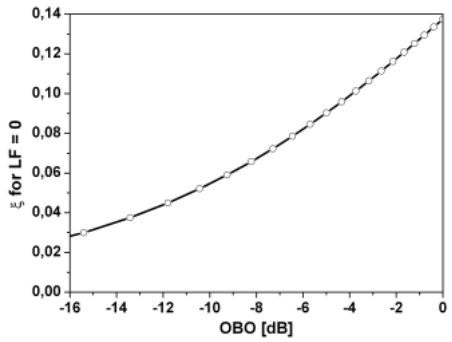


Figure 4.7: Conditions for zero linearity factor

For the purpose of this design the optimal bias level is found to be $\xi = 8\%$, a result that is coherent with the rule of thumb of taking the 10% of the I_{DSS}.

With reference to Eq. 3.14 the value of x_{break} can be estimated as $x_{break} = 0.501$. A slightly more precise evaluation can be carried out by rewriting the Fourier coefficients for the fundamental current component (Eq. 2.12) in terms of the input drive:

$$I_1(x) = x \cdot \frac{I_{max}}{2\pi} \frac{\Phi(x) - sin(\Phi(x))}{1 - \cos\left(\Phi(x=1)\right)} \tag{4.7}$$

The following equation is obtained and must be resolved by numerical means:

$$x_{break}\left[\Phi(x_{break}) - sin(\Phi(x_{break}))\right] = \frac{1}{\beta}(\Phi(1) - sin(\Phi(1))) \tag{4.8}$$

where $\Phi(x)$, the Main amplifier CCA for the chosen bias point and input drive, can be formulated analytically as:

$$\Phi(x) = 2\pi - 2\cos^{-1}\left(\frac{\xi}{x(1-\xi)}\right) \tag{4.9}$$

The obtained $x_{break} = 0.447$ is a slightly more accurate estimate that keeps into account the waveform shape and the effects of the current clipping. This value matches the theoretical expectations, the Auxiliary device starts working halfway trough the input dynamic, contributing to the DPA operation for the upper 6dB of OBO.

The value of the breaking point is also used for the computation of the Auxiliary device bias point, starting from its conduction angle. The Auxiliary device is still turned off for $x = x_{break}$ and in terms of Eq. 2.4 the peak value can be written as:

$$i_d(x_{break}, 0) = 0 \rightarrow \Phi_A = 2\cos^{-1}(x_{break}) \tag{4.10}$$

The current conduction angle for the two amplifiers are $\Phi_M \approx 190°$ and $\Phi_A \approx 127°$ respectively for the Main and the Auxiliary, corresponding to (deep) class AB and class C.

Evaluating the DC bias current is needed to find a suitable approximation of the gate bias point. The value is derived from the definition of ξ itself: while ξ for the Main device was chosen to minimize the LF, for the Auxiliary device the computation is slightly more involved and requires inverting Eq. 4.9. A general formulation of the bias point ratio in terms of the conduction angle is thus:

$$\xi = \frac{-\cos\left(\frac{\Phi}{2}\right)}{1 - \cos\left(\frac{\Phi}{2}\right)} \tag{4.11}$$

The computed values are:

$$\xi_M = 0.08 \qquad \xi_A = -0.8$$

The presence of a negative result is not an error and deserves an explanation: the gate voltage for the class C device is purposefully kept below the threshold to delay its activation and, as a consequence, while it remains in this condition it does not output any current at all. The I_{DC} term mentioned above and in the definition of ξ is to be considered as a *virtual* current, a mathematical extension that has no physical meaning beside allowing to use the same definition of ξ for sub-class C biases.

Once $I_{DC,M}$ and $I_{DC,A}$ are known, an approximation of the gate bias voltage can be finally evaluated as:

$$V_G = V_{pinchoff} + \frac{I_{DC}}{g_m} \tag{4.12}$$

The constant transconductance hypothesis is exploited once again in the design, the approximation introduced is not too heavy as the fluctuation of g_m with the input drive is quite small. A useful expression for the transconductance value is:

$$g_m = \frac{I_{max}}{V_{builtin} - V_{pinchoff}} \tag{4.13}$$

that for the present active device yields $g_m = 0.119\,S$. The DC current levels for the two amplifiers are:

$$I_{DC,M} = 0.02\,A \qquad I_{DC,A} = -0.202\,A$$

and the gate bias voltage for the two branches:

$$v_{g,M} = -1.03\,V \qquad v_{g,A} = -2.89\,A$$

As expected the DC current level for the Auxiliary amplifier is negative, the gate bias voltage well below the threshold turns off the device before the breaking point is reached.

The two amplifiers employed in this design are perfectly equal and are both pushed to the same maximum current level, guaranteeing the contributions to the DPA output power are equal among the two devices.

4.4.1 Input power splitter

The main advantage of a symmetric Doherty PA is being able to re-use the same amplifier cell in both the Main and the Auxiliary branches. To perform the load modulation as expected in the high-power region the amount of power fed into each device must be different: the Auxiliary device is biased below threshold and therefore needs extra power to catch-up with the Main device.

A reasonably good approximation for the normalized splitting factor Δ can be derived with some considerations on the input power for each amplifier:

$$P_{in} = \frac{V_{gs,max}^2}{2R_{in}} \tag{4.14}$$

where the maximum gate-source voltage excursion is:

$$V_{gs,max} = \frac{I_{max} - I_{DC}}{g_m} \tag{4.15}$$

The power flowing into the main device can be thus expressed in terms of device-dependent parameters, R_{in} and g_m, and design quantities, I_{max} and ξ:

$$\begin{aligned} P_{in,M} &= \frac{(I_{max,M} - I_{DC,M})^2}{2R_{in,M}g_{m,M}^2} = \frac{(I_{max,M}(1-\xi_M))^2}{2R_{in,M}g_{m,M}^2} \\ P_{in,A} &= \frac{(I_{max,A} - I_{DC,A})^2}{2R_{in,A}g_{m,A}^2} = \frac{(I_{max,A}(1-\xi_A))^2}{2R_{in,A}g_{m,A}^2} \end{aligned} \tag{4.16}$$

The fraction of total input power, the sum of the input power for the two devices, flowing into each branch of the DPA can be readily computed

as:

$$\begin{aligned}\Delta_M &= \frac{P_{in,M}}{P_{in,M}+P_{in,A}} = \left[1+\left(\frac{I_A(1-\xi_A)g_{m,M}}{I_M(1-\xi_M)g_{m,A}}\right)^2\frac{R_{in,M}}{R_{in,A}}\right]^{-1}\\ \Delta_A &= \frac{P_{in,A}}{P_{in,M}+P_{in,A}} = \left[1+\left(\frac{I_M(1-\xi_M)g_{m,A}}{I_A(1-\xi_A)g_{m,M}}\right)^2\frac{R_{in,A}}{R_{in,M}}\right]^{-1}\end{aligned} \tag{4.17}$$

The use of the same active device for both the amplifier allows to further simplify the two equations into a quantity that is only dependent on the chosen bias point ξ. Plugging the numbers obtained before yields:

$$\Delta_M \approx 21\,\% \qquad \Delta_A \approx 79\,\%$$

As expected the power distribution favours the Auxiliary amplifier. It is useful to re-state that this result is valid under the assumption of constant transconductance, during the simulation phase with a CAD package this value is fine-tuned to achieve the desired results.

The need to split the power and introduce a $90°$ phase shift between the two branches suggests the use of a unequal branch-line coupler, pictured in Fig. 4.8. The structure is composed of four quarter-wavelength transformers and each pair of transmission lines on the opposite sides have the same characteristic impedance, named Z_A and Z_B.

While the physical structure of the coupler gives the power splitting and phase shifting behaviour, the choice of the two impedances determines how the power is distributed among the two output ports. Given the impedance all the ports are matched to, named Z_∞, and the power splitting ratio:

$$K = \frac{P_2}{P_3} \tag{4.18}$$

it is possible to evaluate the two impedances as:

$$\begin{aligned}Z_A &= Z_\infty\sqrt{\frac{K}{1+K}}\\ Z_B &= Z_\infty\sqrt{K}\end{aligned} \tag{4.19}$$

From a practical point of view, when the coupler is implemented using microstrips, the characteristic impedance may not get too small or too big as that may hamper the feasibility of the circuit from a physical point of view.

For the design at hand the impedances for the two branches are:

$$Z_\infty = 75\,\Omega \qquad K = \frac{0.18}{0.82}$$

$$Z_A = 31.8\,\Omega \qquad Z_B = 35.1\,\Omega$$

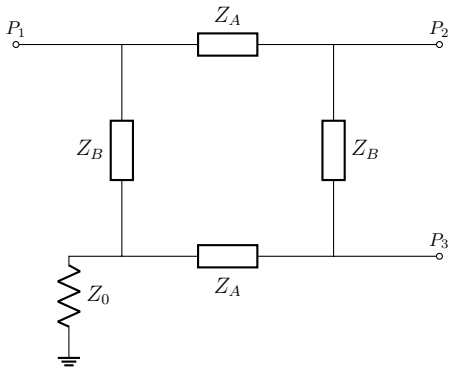
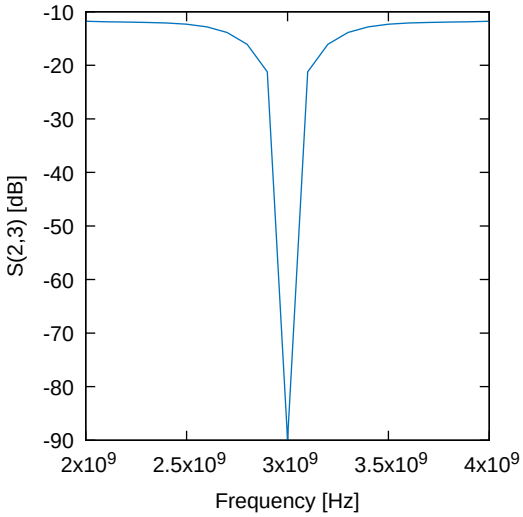
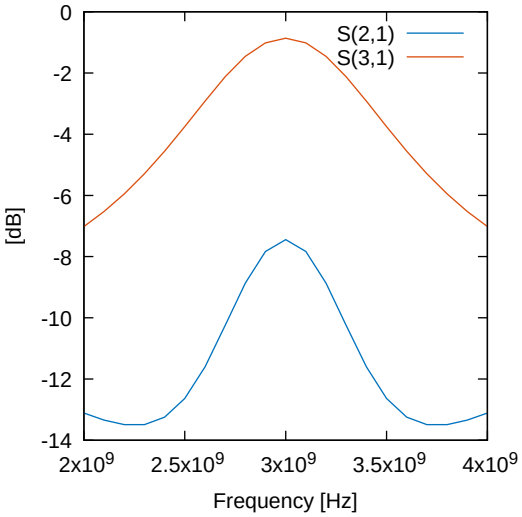


Figure 4.8: Branch line coupler

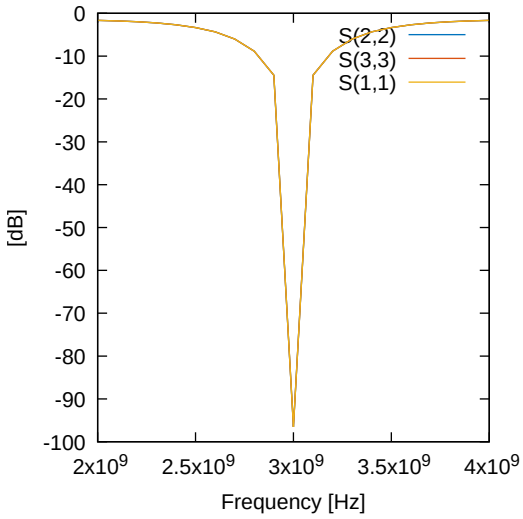
When implemented in ADS the splitter behaves as expected. The two output ports are well-insulated (Fig. 4.9a) and the power is correctly distributed among them: the Main device gets $18\,\% \approx -7.74\,dB$ of the input power, while the Auxiliary device gets the remaining $82\,\% \approx -0.86\,dB$ as shown in Fig. 4.9b. Each port is correctly matched to Z_0 as predicted by the theory and as confirmed by the simulation results, shown in Fig. 4.9c. Fig. 4.9d shows the phase difference between the two branches, introduced by the branchline coupler: it is interesting to highlight how the correct phase difference is kept only at center frequency, inherently limiting the splitter usefulness for broadband uses.



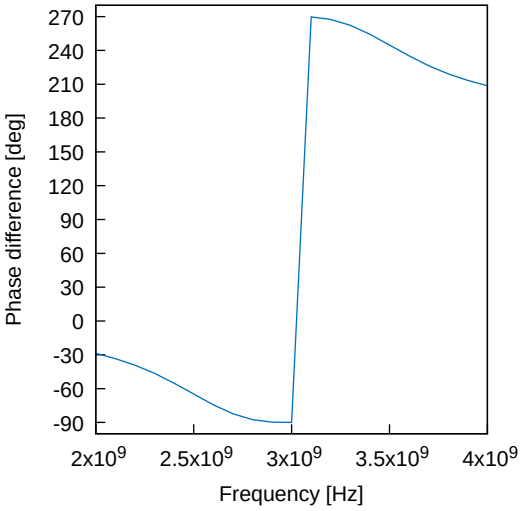
(a) Branchline coupler isolation



(b) Port-to-port transmission



(c) Port matching



(d) Phase difference

4.4.2 Output matching network

In order for the Doherty PA to be effective, the modulated load must be faithfully reproduced at the device's intrinsic plane. To achieve this the parasitic elements on the drain side must be taken care of; there are several ways to perform this, for this design the choice falls on resonating the parasitics away.

The Output Matching Network (OMN) is pictured in Fig. 4.10 and

shows how the package inductance L_d together with the series capacitance C_m resonate at f_0, while the drain-source capacitance C_{ds} forms with the parallel inductance L_m another resonating element at the central frequency. The introduction of a series capacitance is advantageous from the layout point of view as it doubles as a DC-blocking element for the drain bias-tee.

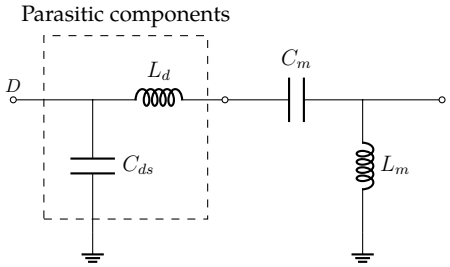


Figure 4.10: Lumped-element output matching network

The matching network is implemented in its distributed form, as shown in Fig. 4.11, where the shunt inductance is replaced by a short $(< \lambda/4)$ short-circuited stub $TL2$. The DC bias is brought to the drain thanks to a $\lambda/4$ stub, showing an infinite impedance at the junction node at the fundamental and at the same time shorting the second harmonic. A big (10pF) capacitor is added to improve the voltage stability with respect to some small amount of noise.

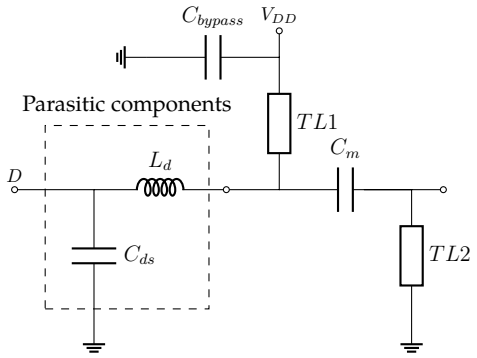


Figure 4.11: Distributed-element output matching network

The computed values for the two compensating elements are:

$$C_m = \frac{1}{(2\pi f)^2 0.017\,nH} \approx 166\,pF \qquad L_m = \frac{1}{(2\pi f)^2 C_{ds}} \approx 8\,nH$$

and a good enough approximation for the transmission-line equivalent of L_m is given by the telegrapher's equation for a short-circuited transmission

line:

$$X_{sc} = Z_0 \tan(\beta l) = 2\pi f L_m \tag{4.20}$$

The characteristic impedance and the electrical length are free parameters, although the latter must be less than $90\,^\circ$, and must be carefully chosen in order to make the stub synthesizable with microstrip lines. An acceptable balance between the two parameters is achieved for $\beta l = 56.45\,^\circ$ and $Z_\infty = 100\,\Omega$.

Since the design process for the OMN is entirely based on the device parameters, the same network can be shared among the two amplifiers.

4.4.3 Input matching network

The input matching network is interposed between the branch line coupler output port and the FET gate terminal, realizing a conjugate match to ensure the maximum power transfer to the amplifier. Having to deal with a heavily nonlinear device means the input impedance cannot be uniquely determined for every input drive level, a suitable approximation for the development of the Input Matching Network (IMN) can be extracted with a LSSP simulation.

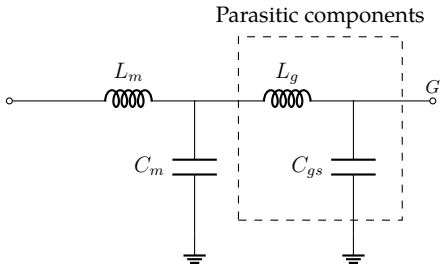


Figure 4.12: Lumped-element input matching network

Given the use of a branch line coupler, the input networks do not have to introduce any phase shift and, on the other hand, must preserve the existing phase relationship to ensure the correct load modulation.

The whole matching network is implemented using three transmission lines with $Z_0 = 50\,\Omega$ and length $90\,^\circ$, $22.1\,^\circ$ and $138\,^\circ$ respectively. As done for the OMN, the DC feeding is brought via a transmission-line connection, but a separate DC blocking capacitor of a few tens of pF is needed.

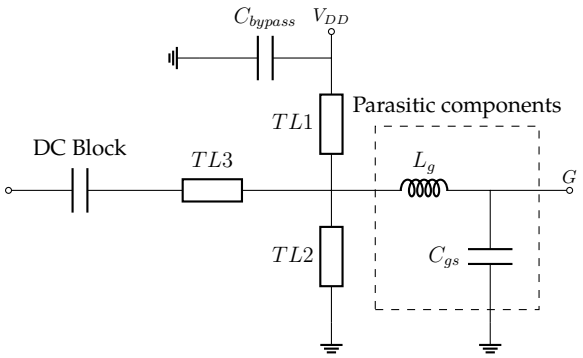


Figure 4.13: Distributed-element input matching network

4.4.4 Power combiner

The output power combiner network includes two quarter-wavelength transformers, one to ensure the inverse load modulation for the Main amplifier and another one to transform the $50\,\Omega$ load into the desired load. The design equations in Eq. 3.26 yield:

$$Z_{\infty}^{TL1} = R_{opt,M} \qquad R_L = \frac{R_{opt,M}}{2} \qquad Z_{\infty}^{TL2} = \sqrt{R_L \cdot 50\,\Omega}$$

The value of optimum load being used is an approximation made on the basis of the expected load line:

$$R_{opt} = \frac{2(V_{DD} - V_K)}{I_{DSS}}$$

A more precise value can be obtained by performing a Load-Pull analysis on the active device.

The implementation with ideal transmission line is pictured in Fig. 4.14.

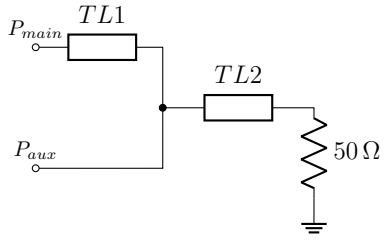
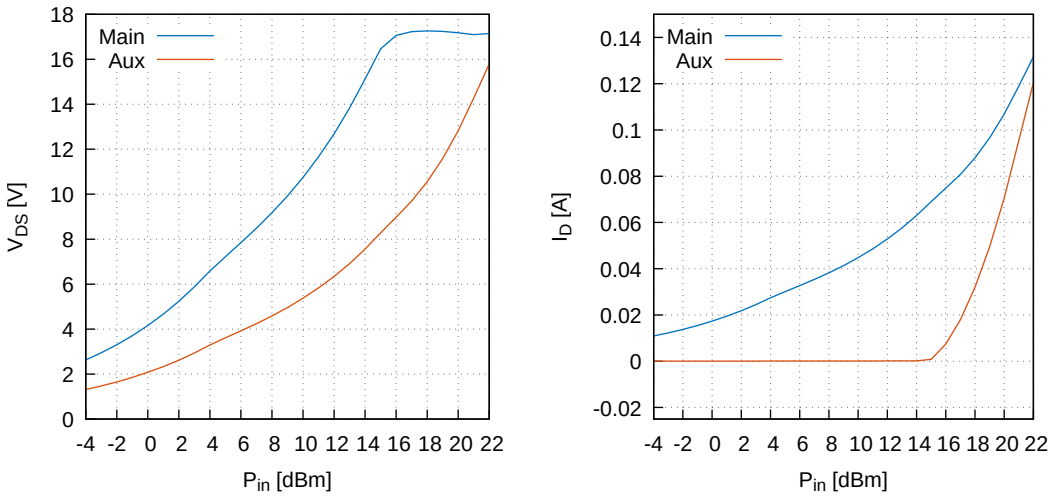


Figure 4.14: Distributed-element input matching network

4.4.5 Simulation results

This section collects a few interesting results extracted from the harmonic balance simulation of the designed DPA. Figure 4.15b shows the symmetric structure working as expected: thanks to the unequal power splitting both the devices reach the same current level when pushed to the maximum drive level of $22\,dBm$. A further confirmation of the Doherty effect working as expected is Fig. 4.15a: the Main amplifier drain current is being locked at around V_{DD} thanks to the load modulation induced by the Auxiliary device.



(a) Drain-source voltage

(b) Drain current

The device reaches the prescribed output power target, achieving a P_{max} of around $1.7\,W$ as shown in Fig. 4.16. The same figure also shows the overall power gain of the whole DPA: the decreasing trend in the left hand side of the graph can be attributed to the Main amplifier being biased in class AB. In fact when the input signal is small enough the AB amplifier behaves mostly as one biased in class A would do with little or no harmonic distortion. When the input signal level increases the amplifier "flips back" to class AB operation, bringing down the gain.

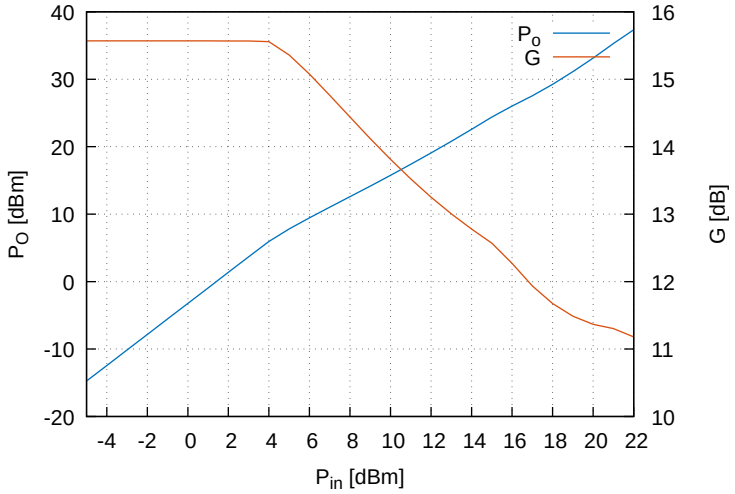


Figure 4.16: DPA output power and gain

The drain efficiency η, shown in Fig. 4.17, remains quite high throughout the whole OBO region of around $6\,dB$ with a slightly higher peak at its end.

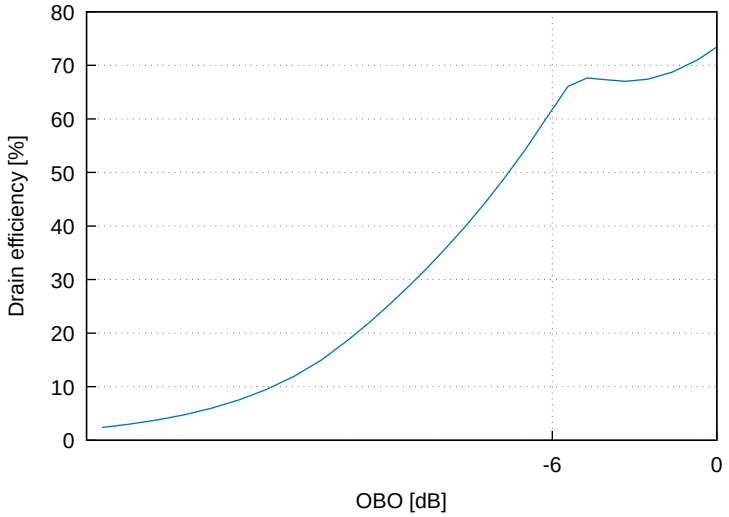


Figure 4.17: DPA drain efficiency

The previous results are obtained by supplying the circuit with an input signal at frequency of $f = 3\,GHz$, the DPA behaviour is expected to degrade as soon as the frequency shifts from the center value. Figure 4.18

and Figure 4.19 respectively show the output power, gain and the drain efficiency for different working frequencies ranging from $2.8\,GHz$ to $3.2\,GHz$.

While the gain and output power remain relatively unchanged, the efficiency drops down considerably, losing up to $20\,\%$. This behaviour is expected as the Doherty relies on the precise modulation of the load: the frequency shift causes problems of phase coherence between the input signals and, consequently, between the output signals that are expected to sum-up in phase. Moreover the use of a quarter-wavelength transformer, a known bandwidth-limited structure, in the output power combiner further contributes to the resulting DPA narrow frequency operation.

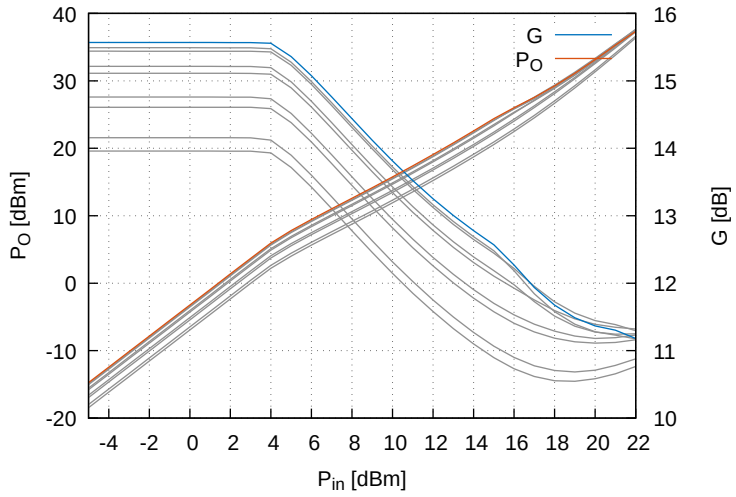


Figure 4.18: DPA output power and gain – with swept f

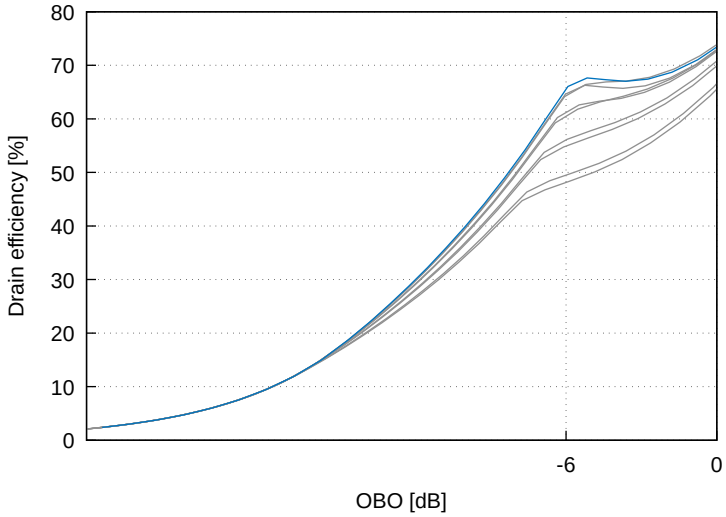


Figure 4.19: DPA drain efficiency – with swept f

4.5 Design – Three-stage

The design procedure for a three-stage symmetric Doherty PA follows closely the one already outlined for the two-stage case: the additional device introduces one more high-efficiency point and affects the load modulation for the whole set of devices. The goals for the design are a OBO of around $10dB$ with an intermediate efficiency peak for $6dB$ of backoff and a target output power of $2.8\,W$ at a working frequency of $3\,GHz$.

According to Eq. 4.9 the CCA for the Main amplifier, assuming $LF \approx 0.6$, is $\Phi_M = \Phi(1) \approx 187°$, corresponding to a bias arrangement in deep class AB.

With the same concept of normalized input drive x used in the previous design, the two "breaking points" that mark the separation between low, medium and high power regions can be expressed in terms of the α coefficients introduced in Chapter 3. With the help of Eq. 4.7 the following two equations can be obtained, relating the Main device's drain current to the backoff factors:

$$\begin{aligned} x_{break,1}\left[\Phi(x_{break,1}) - sin(\Phi(x_{break,1}))\right] &= \alpha_1(\Phi(1) - sin(\Phi(1))) \\ x_{break,2}\left[\Phi(x_{break,2}) - sin(\Phi(x_{break,2}))\right] &= \alpha_2(\Phi(1) - sin(\Phi(1))) \end{aligned} \tag{4.21}$$

When solved by numerical means the two values of x are:

$$x_{break,1} \approx 0.26 \qquad x_{break,2} \approx 0.46$$

From these values the two auxiliary amplifiers' CCA can be derived via Eq. 4.10, imposing the i-th device to be turned off for $x = x_{break,i}$:

$$\Phi_{A1} \approx 150\,° \qquad \Phi_{A2} \approx 125\,°$$

The next logical step after determining the class for the three active devices is the computation of the gate bias level. By combining Eq. 2.1 and Eq. 4.11 the DC current levels for the three amplifiers can be determined:

$$I_{DC,M} = 15.6\,mA \qquad I_{DC,A1} = -92\,mA \qquad I_{DC,A2} = -222\,mA$$

together with the proper required voltage, using Eq. 4.12:

$$V_{G,M} = -1.12\,V \qquad V_{G,A1} = -1.66\,V \qquad V_{G,A2} = -2.31\,V$$

4.5.1 Input power splitter

Being the designed Doherty PA symmetric, all the devices have the same periphery and the unequal input feeding makes up for the transconductances being ahe same. The fraction of total input power required by the i-th amplifier in a N-stage DPA can be expressed by generalizing Eq. 4.16:

$$\Delta_i = \frac{P_{in,i}}{\sum_{j=1}^{N} P_{in,j}} = \left\{ 1 + \sum_{j \neq i}^{N} \left[\left(\frac{I_j(1-\xi_j) g_{m,i}}{I_i(1-\xi_i) g_{m,j}} \right)^2 \frac{R_{in,i}}{R_{in,j}} \right] \right\}^{-1} \tag{4.22}$$

If the two devices are assumed to have the same transconductance and input resistance in order to simplify the calculations, the splitting factors for the three devices are:

$$\Delta_M \approx 14\,\% \qquad \Delta_{A1} \approx 30\,\% \qquad \Delta_{A2} \approx 56\,\%$$

The power distribution in unsurprisingly skewed towards the amplifier with a deeper bias.

The implementation of a three-stage power divider with unequal splitting ratios can be achieved by cascading two Wilkinson power splitters. By properly choosing the order of the output ports it is also possible to have the splitter impose the desired phase relationship between the three branches: in a 3-stage DPA the Main amplifier and the second Auxiliary one must be fed with a delay of $90\,^\circ$ to ensure the phase coherency between the three currents flowing on the load.

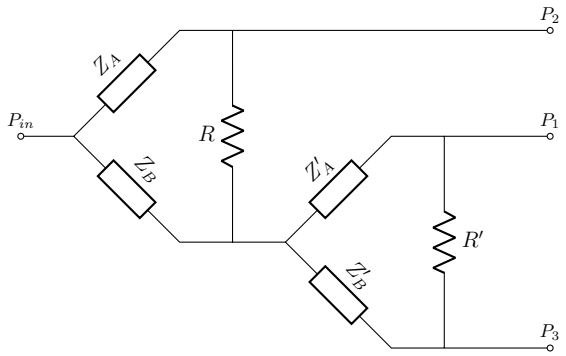


Figure 4.20: Cascaded unequal Wilkinson splitter

The splitter, pictured in Fig. 4.20, is designed according to the equations

derived by Parad & Moynihan [11]:

$$\begin{aligned} K &= \sqrt{\frac{P_3}{P_2}} \\ Z_A &= Z_{in}\sqrt{K(1+K^2)} \\ Z_B &= Z_{in}\sqrt{\frac{1+K^2}{K^3}} \\ R &= Z_{in}\left(K+\frac{1}{K}\right) \end{aligned} \tag{4.23}$$

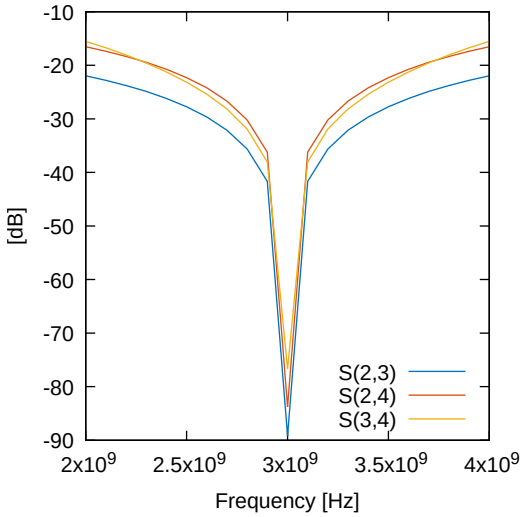
For this network to work as expected, the first splitter must deliver Δ_{A1} of the input power to the first branch, while the remaining power is split according to Δ_M and Δ_{A2}:

$$\begin{aligned} K &= \sqrt{\frac{1-\Delta_{A1}}{\Delta_{A1}}} \\ K' &= \sqrt{\frac{1-\Delta_{A1}-\Delta_M}{\Delta_M}} \end{aligned} \tag{4.24}$$

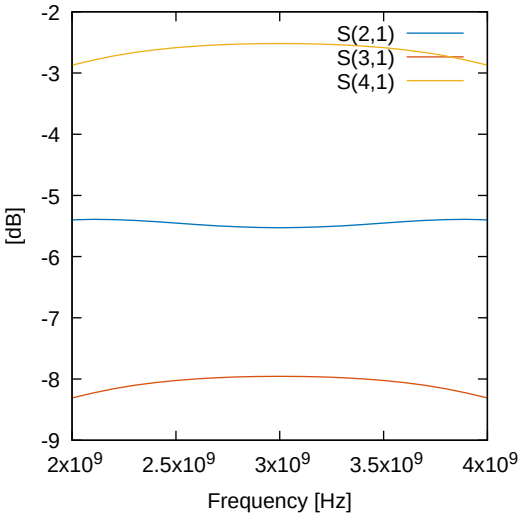
Given the input port resistance $Z_{in} = 50\,\Omega$ the following values are evaluated:

$$\begin{aligned} Z_A &= 112.8\,\Omega \qquad Z_B = 48\,\Omega \qquad R = 109\,\Omega \\ Z'_A &= 103.5\,\Omega \qquad Z'_B = 25.9\,\Omega \qquad R' = 81.8\,\Omega \end{aligned}$$

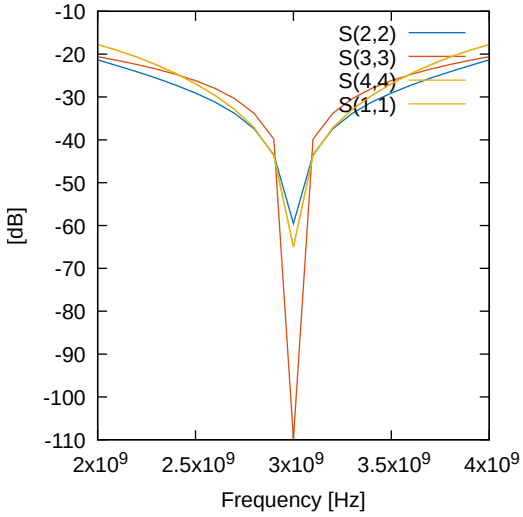
When implemented in ADS the splitter behaves much as expected, producing the correct phase difference and delivering the correct amount of power to each output port while maintaining a good isolation between them. Once again the narrowband nature of the splitter can be noticed, the extensive use of quarter-wavelength transmission lines makes this naïve design unsuited for broadband applications.



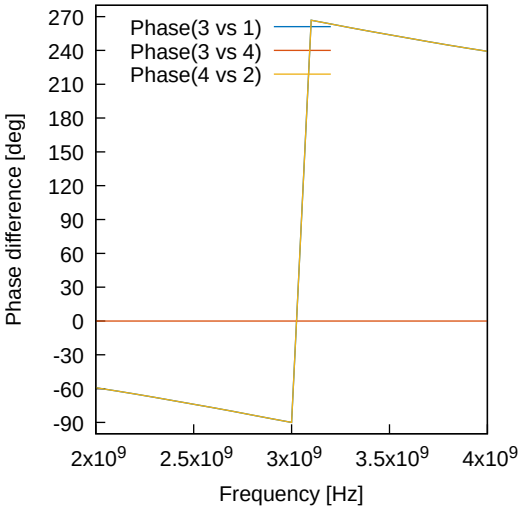
(a) Port isolation



(b) Input-to-output transmission



(c) Port matching



(d) Phase difference

4.5.2 Power combiner

The output power combiner is the most critical network for a DPA as is responsible for the correct modulation of the load seen by each of the three devices. The impedances of the three transmission lines, named Z_{0n}, can be evaluated using Eq. 3.45 on the basis of the target output power and the external load resistance R_L. This last parameter being independent from the Doherty operation is useful to tweak the characteristic impedances and

make them fall in the acceptable range; for the current design $R_L = 25\,\Omega$.

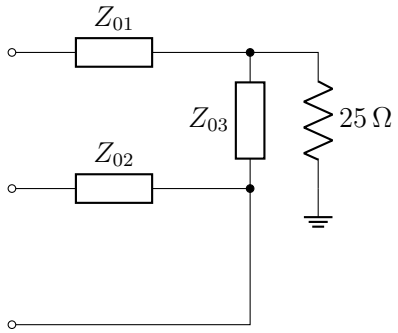


Figure 4.22: Output power combiner network

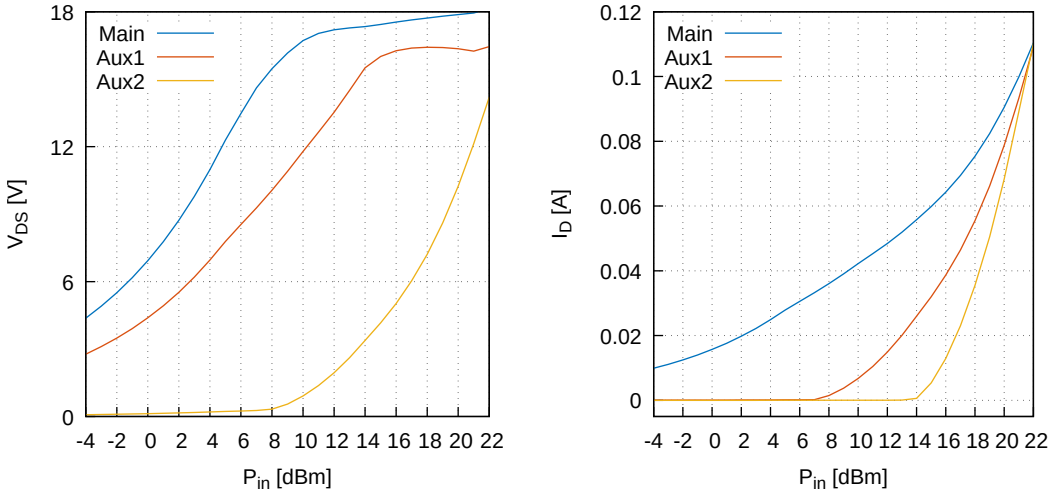
$$Z_{01} = 106\,\Omega \qquad Z_{02} = 131.6\,\Omega \qquad Z_{03} = 49\,\Omega$$

The phase difference introduced by the quarter-wavelength transformer is recovered by the delay introduced from the input splitter, ensuring the three currents sum coherently on the output load.

4.5.3 Simulation results

The complete DPA, made from all the pieces designed in the previous sections, is implemented in ADS and tested with an harmonic balance simulation.

The circuit requires a fair amount of hand-tuning to achieve the expected results, the non-constant transconductance and the gradual turn-on behaviour of the FET are to be attributed for most of the changes in the bias voltage and power splitting factors. Figure 4.23a and 4.23b show the drain current and the V_{ds} behave as predicted by the theory with some minor differences: the Main amplifier is not perfectly kept in voltage saturation by the other two devices, nor the second Auxiliary device manages to reach the maximum voltage.



(a) Drain-source voltage

(b) Drain current

The overall gain in the low-power region remains pretty much unchanged from the two-stage case as only the Main device is active and the bias points are quite close. Once again the gain starts rolling-off when the class AB amplifier's current starts clipping to zero. The descent is slightly attenuated by the gain contribution of the first and second Auxiliary amplifiers that, albeit biased in class C, give a significant contribution mostly in the high-power region. The output power for peak input power is slightly less than expected due to the drastic gain compression effect for the Main amplifier that, being the main contributor to the overall DPA gain, affects the whole figure of merit.

The drain efficiency curve, pictured in Fig. 4.25 does not show the typical three-peaked shape. The $-10\,dB$ OBO point takes a hit due to the presence of a small runaway DC current being drawn by the two Auxiliary amplifier, even though they are powered off. The $-6\,dB$ OBO is slightly misaligned with the efficiency peak due to the small corrections made to the bias voltages and power splitting factors.

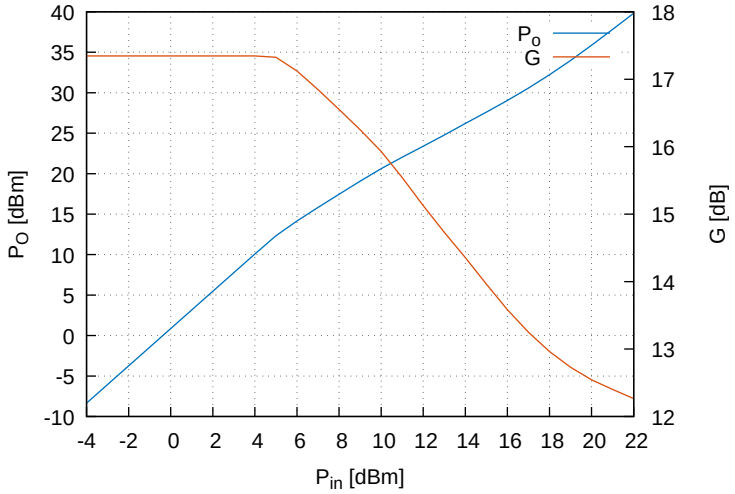


Figure 4.24: DPA output power and gain

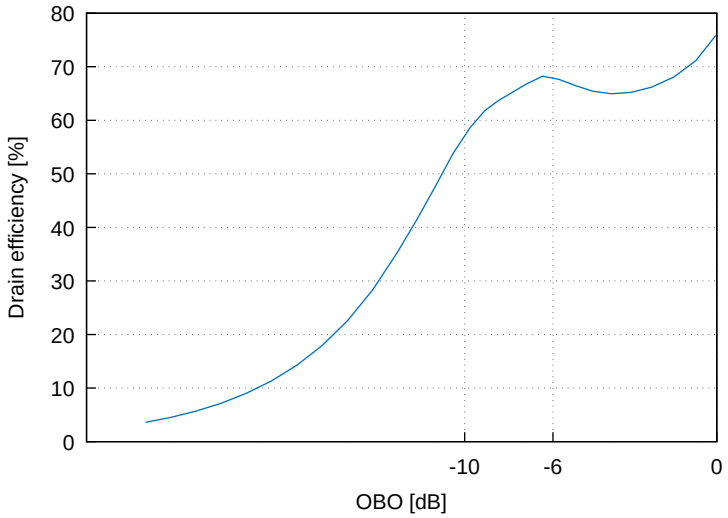


Figure 4.25: DPA drain efficiency

The evaluation of the main figures of merit for different working frequencies ,$f_0 \pm 0.2\,GHz$, gives some interesting and unexpected results. When working at frequencies higher than $3\,GHz$ the DPA performs slightly better, while for lower frequencies the performance drops as expected.

This effect can be traced back to an overall increase of the drain current for the three devices, possibly caused by an incorrect load modulation that does not move anymore only along the real axis. The compensation

technique employed for the drain parasitics, by resonating them away, is characterised by a pretty small Q factor and, when operating in broadband conditions, the perfect transfer of the load modulation to the device intrinsic plane is not guaranteed. Nonetheless within a range of $100\,MHz$ the DPA is still usable and shows good characteristics.

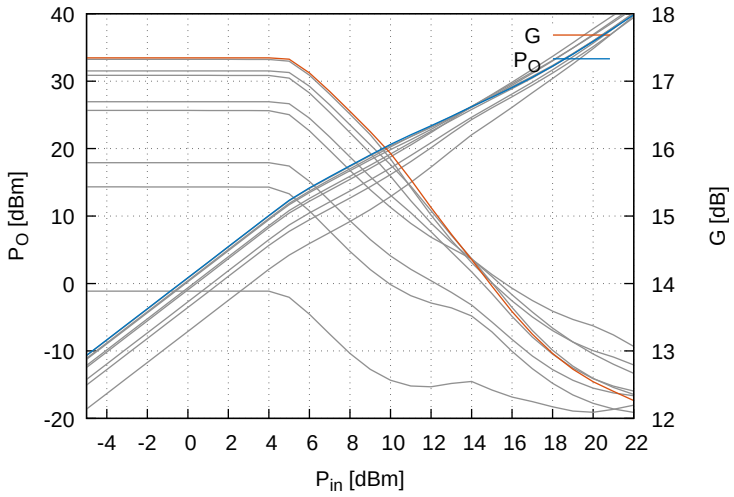


Figure 4.26: DPA output power and gain – with swept f

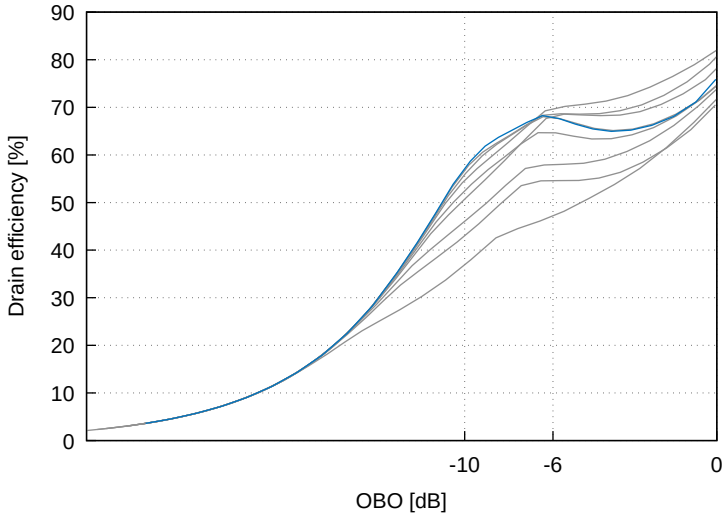


Figure 4.27: DPA drain efficiency – with swept f

Chapter 5

Conclusions and Future Work

5.1 Conclusions

This work explored some important details behind the efficiency enhancement brought by the Doherty architecture. The principle behind the loss of efficiency is explained in qualitative and analytical terms, accompanied by a brief introduction to some solutions such as the EER or Chireix's outphasing techniques. The idea of exploiting the dynamic load modulation effect, at the heart of the DPA, is first applied to a conventional two-device amplifier in order to extract a set of solid design equations.

The Doherty concept is also stretched to allow the use of three devices, ensuring a large high-efficiency region of amplification. The analysis covers the two main arrangements that are employed for this configuration: the "classic" three-stage Doherty and the NXP one. Both of them are developed from the ground-up, showing their respective strengths and weaknesses, in order to be able to compare the two. A set of design equations matching the ones already seen in the literature are derived, proving the analysis' soundness.

The design equations obtained for the two and three device DPA are validated by designing and simulating two amplifiers, starting from the specifications. The design process is made slightly more challenging by the use of a symmetric configuration with uneven input power splitting.

The design sections follow a step-by-step approach with extensive explanations and cover the design of the input and output matching networks, the bias network and the input and output power combiners and splitters. For each amplifier the most significant simulation results are collected and compared against the theoretical expectations: the two DPA behave similarly as expected in their optimal working conditions.

On the topic of input splitters, two different solutions are proposed: one exploiting branch-line couplers and the other exploiting two cascaded Wilkinson splitters.

5.2 Future work

The use of a cubic Curtice-Ettemberg model with enough parasitic elements certainly simplified the design process. A "real" device model with a richer set of parasitic elements and with its heavily non-constant transconductance makes the design process much harder: the mutual interaction between the transistors needs some care not to disrupt the load modulation. Applying the design steps to a more complex model is certainly one of the future steps.

One of the main problems with the set of analytical design equations is their effective feasibility: some values of characteristic impedance, for example, are bounded by the technological limits when implemented with microstrip lines. Some further work may be carried out in this direction, by evaluating the upper and lower boundaries to the achievable DPA performance depending on the range of possible Z_0. Similarly, the need for uneven input splitting can sometimes end up requiring impossibly small or large splitting factors, making them hard to implement.

The designed output matching networks can be much improved by employing a smarter compensation technique for the parasitic elements: for instance, the L and C on the drain side can be absorbed to form a quarter-wavelength transformer.

A few simulation results show the DPA frequency behaviour. No particular care is given to the operational bandwidth during the design, explaining the suboptimal results. The design can be certainly improved by replacing most of the narrow-band components employed with wide-band equivalents where possible.

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