Politecnico Di Torino

Master's Degree in Biomedical Engineering

Academic Year 2020/2021

Chip characterization and Database development for HD CMOS MEAs

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Abstract

Multi-electrode array chips are rapidly growing as one of the main ideal technologies to unveil complex electrophysiological dynamics of both cells and tissues. While this technology can rely on the special interaction of living cells with the peculiar structure of this kind of devices, it remains clear that the cell cultures' biological environments can still represent a harsh condition for electronics. Consequently, the original purpose of this Final Project was to use the high-throughput CMOS multi-electrode array developed by Imec to characterize the electrodes' impedance variation after different bio-chemical treatments and packaging. Those experiments would have consisted in the electrical and physical monitoring of such devices during the growing of multiple cultures of living cells on-chip, requiring a consistent on-site presence. However, due to the worsening of the global pandemic situation in the late fall of 2020, the Final Project changed from a laboratory research to a more smart-working project, thus dividing it in two. The first part is dedicated to the characterization and validation of the chips mentioned above, while the second one contains the design and development of a new database to store all the chips information. In this Master's Thesis, we exploited the chip testing to measure characteristics and yields of the different chip batches, with the September 2020 batch having a 34% output caused by a poorly wire-bonding, while the December 2020 batch is standing at a 80% output. Thus remarking how important the wire-bonding and the encapsulation processes are in the fabrication of a chip. Moreover, the chip testing also served as imaging asset, providing new insights for the correct programming of the chips every time the respective software is updated. During the design and development of the database, we were able to make a more user-friendly interface, therefore reducing the time for catalog devices, improving the storage space and its consultation. In conclusion, the work presented here should make an important contribution both for a better imaging asset development, essential for correct chip evaluations, and for a faster chip production and experimentation, smoothing the bureaucratic process by improving the overall team communication.

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List of Abbreviations

Al	Aluminum
AP	Action potential
BCFL	9,9-bis(4-hydroxy-3-methyl)fluorene
BEOL	Back-end-of-line
CLSM	Confocal Laser Scanning Microscope
CMOS	Complementary metal oxide semiconductor
DB	Database
ExC	Extracellular
GUI	Graphical user interface
HD	High density
IC	Integrated circuit
InC	Intracellular
MEA	Multi-electrode array
Ms	Microsoft
PBS	Phosphate-buffered saline
PCB	Printed circuit board
PHN	Primary hippocampal neurons
SEM	Scanning Electron Microscope
SNR	Signal-noise ratio
TiN	Titanium Nitride
UVO_3	Ultraviolet Ozone

1. Motivation of the final project

Multi-electrode array chips are rapidly growing as one of the main ideal technologies to unveil complex electrophysiological dynamics of both cells and tissues. As this technology present many interesting features for the drug development paradigm and the general study of cell cultures, there are still numerous issues hampering its potential. Most of these problems are strictly related to the harsh environments of the experiments performed on these devices. In the specific, these environments can influence the speed of the deterioration process of the chip's electrical components, strongly reducing their efficiency over the time. Hence, the initial motivation was to have a better understanding on this issue. In particular, the original purpose of this Final Project was to use the high-throughput CMOS multi-electrode array developed by Imec (Leuven, Belgium) to characterize the electrodes' impedance variation after different bio-chemical treatments and packaging. Those experiments would have consisted in the electrical and physical monitoring of such devices during the growing of multiple culture of living cells on-chip, requiring a consistent on site presence.

As the project started in September 2020, few improvements were made on the experimental level. Thus being mainly because of the general preparation I required to have a safe experience in this new environment, learning the general laboratory guidelines and how to perform the various experiments. However, due to the worsening of the global pandemic situation in the late fall of this year, we had to change to new stricter safety guidelines, which resulted in hampering a full in-lab project. For this reason the original aim of this Final Project had to be revisited. We decided to arrange a more remote-working compatible project, without removing what had been done in the first few months, resulting in a two sections project. In the first part, we exploit the different data and experiments arranged in the first few months, which were dedicated to the characterization and validation of the chips mentioned above, to study how critically the different stages of the fabrication process can influence the chip functionalities. However, for the second one we opted for the design and development of a new database to store all the chips information, with the aim of improving the overall chip management process.

2. Imec Sparrow chip

2.1 State of the art

2.1.1 Multi Electrode Arrays

In physiology, action potentials (APs) occur when the membrane potential of a specific cell rises and falls rapidly. This event occurs in several type of cells, called electrogenic cells, where it can play a central role in cell-to-cell communication, like in neurons, or is exploited to activate intracellular processes. A multi-electrode array (MEA) is a grid of tightly spaced microscopic electrodes employed to record and stimulate these electrogenic cells. The necessity for such devices has been known since the scientists understood that, to effectively understand the processes of a dynamic neural system, there is the need to simultaneously record different physiological events happening at single-cell scale level. While one of the main applications is to improve the understanding of how neural systems works, MEAs are also widely used as effective and rapid screening platforms in pharmacology and toxicology, for drug testing and tissue-based biosensors [1].

Unfortunately, since the technology was not advanced enough, it was not possible to develop and fabricate devices with this high resolution till the second half of the 20th century. At the end of that century, thanks to the advance of microelectronics science and the ability to manage big quantity of data, a first introduction to such technology was possible, resulting in a large quantity of designs, applications and new neurophysiological information [1].

Charles A. Thomas published the first paper describing a planar multi-electrode array in 1972. The device (Figure 2.1) was fabricated on glass substrates and using photolithography two rows of 15 gold electrodes of 7 μm^2 and 100 µm pitch were patterned. The electrodes were also plated with platinum black to reduce the impedance of their connection to the culture medium. These MEAs were initially employed to record cultured dorsal root ganglion neurons. Unfortunately, because of the growing neurons creating an insulation layer, these first recording experiments were unsuccessful. However, recordings were successfully performed when using cardiac myocytes [2].

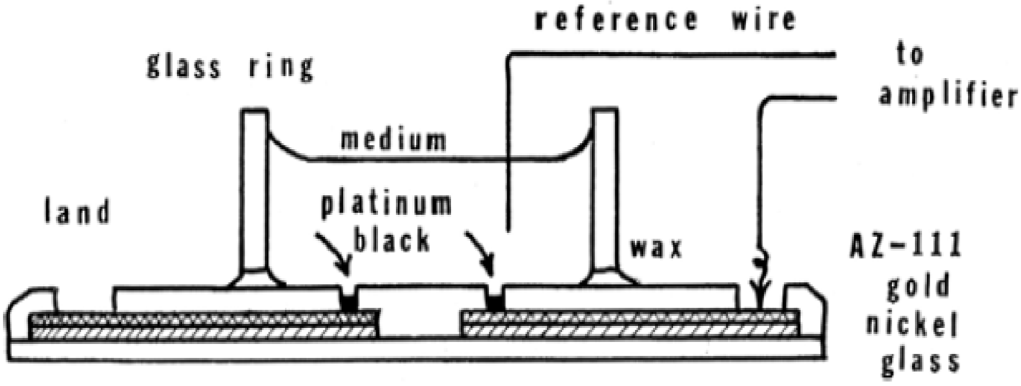


FIGURE 2.1: Schematic diagram of the first multi-electrode array structure developed by Charles A.Thomas. [2]

Five years later, in 1977, Guenter Gross and his collaborators proposed the idea of a similar multi-electrode array, succeeding for the first time in recording of action potentials from single neurons derived by Helix pomatia (snail) ganglia [3]. New developments followed in the upcoming years: in 1980 Jerome Pine reported the first successful recording from single dissociated neurons, derived from mammalian central nervous system cultures, using a multielectrode array of 4x4 (16) gold electrodes, platinized and insulated with silicon dioxide [4].

Following up on his earlier work, Gross used his arrays to record from dissociated spinal cord cultures in 1982. Thus obtaining good signals from spontaneous activity, highlighting specific properties like the periodic and aperiodic bursts and the influence of temperature on this activity. In the subsequent years, many improvements were achieved by different research groups. These upgrades proved how MEAs could provide a means for long-term non-invasive communication for cultures of single neurons or simple networks in both stimulation and recording. Therefore this technology proved to be much more superior to conventional electrodes [1].

In 1991, Chibin Chien and Jerome Pine investigated the use of MEAs combined with voltage-sensitive dye recording on small networks of cultured neurons. They demonstrated that even when the dye signal was low, only 1% of the initial fluorescence, the stimulus-locked synaptic potentials and the action potentials were still cleanly measurable by this type of device, thus showing a very high sensibility for these signals [5]. Over the time, advances of passive planar arrays technology, simplicity of photolithography and the interest from big commercial companies further increased. This allowed multiple research groups to develop many custom arrays suited for very different research projects, increasing accordingly the neurophysiological knowledge, and bringing improvements in all the fields [1]. The advances in lithographic techniques, fueled by the semiconductor industry, allowed a gradual increase in performance and reliability of MEAs, while the first passive array devices, for either in vitro and in vivo applications, became commercially available in the late 90s and early years of this century.

Starting from the early 2000s, active MEAs using complementary metal-oxide-semiconductor (CMOS) technology were fabricated in academic facilities and industrial foundries. The possibility of active MEAs to integrate electronic components, with the parallel improvement of additional processing steps for better biocompatibility, further widened the variety of explorations and possibilities provided by the multi-electrode array technology.

2.1.2 High Density CMOS MEAs

High Density (HD) CMOS MEAs lean on high resolution, reduced crosstalk and higher functionality. For these reasons, the main application of these chips is to acquire information from a large number of bio-signals, derived by single cells, within both short/long periods of time. However, the implementation of these electronic systems is constrained by many factors. These issues can include space limitation, heat emission, sensor-to-signal-source proximity, and invasiveness to the biological specimen. Consequently, for the monitoring of electrophysiological properties multiplexing is fundamental to avoid such problems, obtaining better sensing and actuation capabilities. Therefore, the complementary metal-oxide-semiconductor technology is essential to obtain such integrated circuits, allowing the replacement of large analog components with digital signal processing blocks [6].

To date, numerous HD CMOS MEAs have been published, each of them varying in technical specifications such as noise compliance, number of electrodes and functionalities. For instance, Park et al. (2018) [7] presented a fully integrated CMOS MEA chip composed of 32x32 (1024) multimodality pixels divided in four 16x16 groups. Each group was equipped with its own signal-conditioning block which could be used in parallel. Each of these pixels consisted in four 12 μm x 12 μm photodiodes and one 28 μm^2 square gold-plated electrode (Figure 2.2), reaching a total of 4096 optical detection sites and 1024 electrodes with an electrode pitch of 58 μm. The total cellular interfacing field of view was a square of 1.85 mm^2, which could be used either as a stimulator and as a sensor array. Major examples of application fields were drug screening and cellular characterization. Those were supported by the real-time extracellular potential recording, optical detection, charge-balanced biphasic current stimulation, and cellular impedance modality available in each single pixel.

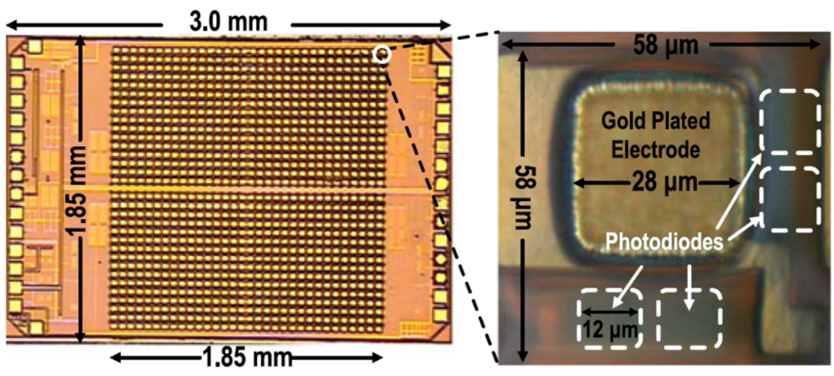


FIGURE 2.2: Microphotograph of Park's chip centered on the array with a magnification of a single pixel on the right. [7]

Another notorious example of HD CMOS MEAs was developed by Dragas and her collaborators in 2017 (Figure 2.3) [8]. This chip, built exploiting a different CMOS technology (0.18 µm) respect the previous one (0.13 µm), consisted of one array of 59760 electrodes distributed over 332x180 pixels with an electrode pitch of 13.5 µm. The total number of the measurement and stimulation modalities was 6, two more than Park et al. (2018) [7]. Furthermore, the cellular interfacing field of view was even larger, having an active area of 4.48x2.43 mm^2. Thus whilst all the other characteristics, including noise, power consumption and spatial resolution, were still comparable with the other state-of-the-art devices. Like the previous device, the presence of a switch matrix means that any measurement/stimulation unit can be connected to any electrode of the array, allowing different functions to run in parallel, making the chip ideal for *in vitro* applications [8].

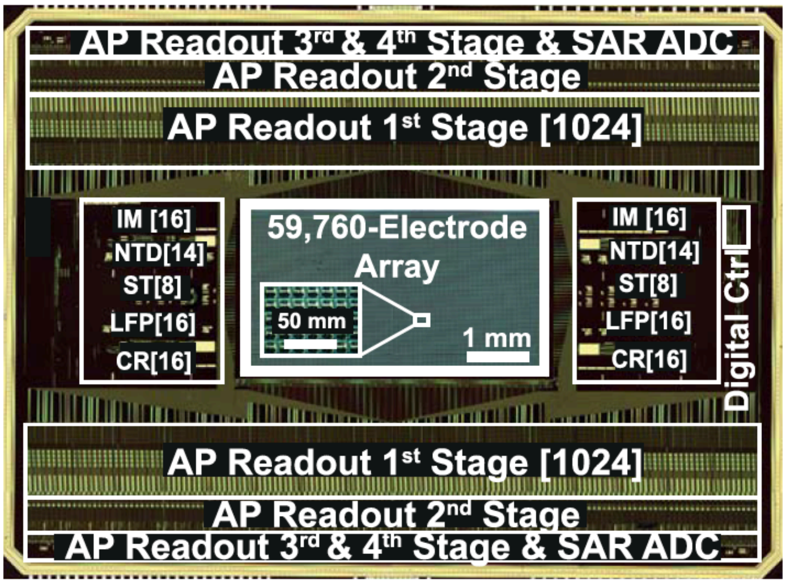


FIGURE 2.3: Microphotograph of Dragas's chip with superimposition of the different stages illustration. [8]

In the same year, Abbot et al. (2017) [9] published a similar device. While the structure was similar to the chip described in Park et al. (2018), consisting of a 32x32 array with 1024 recording/stimulation pixels spaced by an electrode pitch of 126 µm, it differed for the electrode type. The presence of nanoscale vertical intracellular electrodes (Figure 2.4) gave the possibility to finally use intracellular recording for *in* *vitro* cells. Thus improved the drug development paradigm, allowing to examine the effects of different medicines on the delicate dynamics of a cardiomyocytes/neurons network, erasing the gap between multi-electrode and patch-clamp[1] arrays.

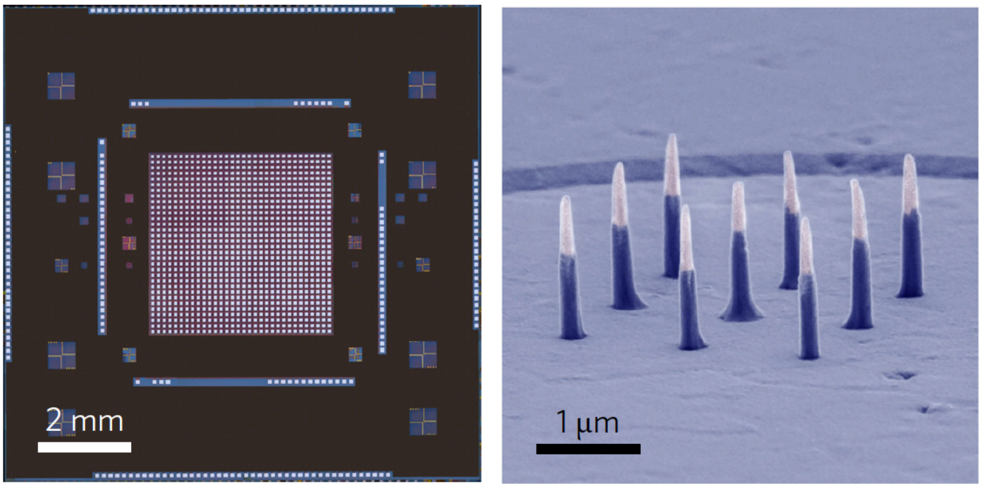


FIGURE 2.4: Microphotograph of the 32x32 pixels array and false-colored scanning electrode microscope (SEM) image of 9 vertical intracellular electrodes. [9]

All these chips exploit similar CMOS process technology to integrate active electronic components on the same substrate, leveraging the possibility of including a much higher electrode number and density. Due to the possibility of using active switches to time multiplex signals, integrated circuits make it doable to transfer data from chips with a high number of channels and to overcome the connectivity limitation of passive devices. Furthermore, such co-integration allows for a better amplification of the signals, improving the overall quality due to the minimal resistances and parasitic capacitances. Both passive and active multi-electrode arrays (MEAs) can be considered ideal technologies to discover new characteristics and dynamics of cells and tissues. Nonetheless, when studying complex neuronal cultures, active MEAs are more interesting compared to passive devices. This preference derives from their potential in achieving many key features such as superior sensing, smaller electrode size, reduced crosstalk, and higher functionality [10]. On the downside, the problem that many active

[1] Patch-clamp: electrophysiological technique used to measure small currents passing through cell's ionic channels by exploiting the use of micropipettes.

MEA devices share is the characteristic of being mainly dependent on a single operational modality. This restricted selection can be viewed as a great limit, especially considering that the field of application in the biological and electrophysiological dynamics requires the assessment of synergies between multiple mechanisms.

In order tackle functionality limitations of the devices presented above, Mora-Lopez and coworkers at Imec designed a multimodal chip [10]. This device combines a unique set of functionalities: recording biosignals with high SNR, voltage/current stimulation, fixed frequency impedance monitoring and impedance spectroscopy measurements. Since this was the study device employed throughput this thesis, its specifications are elaborated in detail in the section below.

2.1.3 **The Imec HD CMOS MEA chip**

The Sparrow CMOS multi-electrode array chip features 16384 Titanium Nitride (TiN) electrodes, 1024 parallel readout channels, 64 multiplexers, 64 stimulation units and 64 ADCs. The array is divided in 16 active areas (Figure 2.5) as a 4x4 matrix, with the possibility to access each single area simultaneously or independently, each one composed of 1024 electrodes arranged as a 32x32 matrix with an electrode pitch of 15 μm. The electrodes of each active area are grouped in 256 pixels, meaning four electrodes per pixel which can be selected via a 4-to-1 multiplexer, and are surrounded by eight 50x235 μm^2 TiN reference electrodes. For research reasons, the electrodes inside each active area are also divided in 4 groups depending on the different size (which are 2.5x3.5 μm^2, 4.5x4.5 μm^2, 7x7 μm^2 and 11x11 μm^2) to investigate the correlation between signal strength/noise behavior and electrode size [10].

Chip fabrication can be summarized as follows: the wafers were processed using a standard 0.13 μm CMOS technology, using a 6-metal-layer aluminum back-end-of-line (BEOL) stack. After the CMOS fabrication, the wafers were post processed in-house following four main steps: passivation, via opening, electrode deposition and band pad opening, obtaining the design previously discussed.

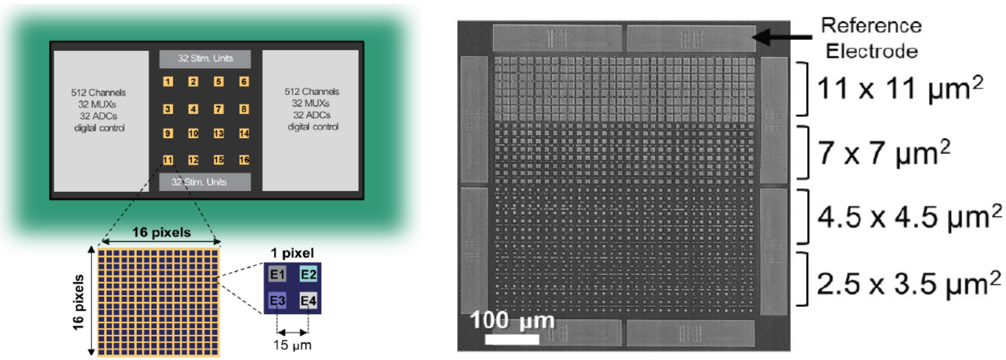


FIGURE 2.5: Illustration of the Sparrow chip structure plus a magnification of one single active area surrounded by eight reference electrodes, obtained through SEM imaging, featuring the four different electrodes sizes. [10]

The Sparrow chip features one of the highest number of modalities (six) available for an active MEA device, each one that can be independently performed. These modalities can be used for:

1. *Current Stimulation modality*: used for better controlling the charge delivered to cells/tissue;

2. *Voltage Stimulation modality*: used for influence cell behavior (the stimulation current applied will be determined by the electrode impedance);

3. *Extracellular Recording modality*: used to measure action potentials in any kind of electrogenic-cell which, thanks to the electrode pitch of only 15 μm, makes possible to achieve single-cell resolution, tracking all the electrical activities of the active cells placed on top of the device;

4. *Intracellular Recording modality*: used in pharmacological screening to search the properties of cell ion channels and, since it's a reversible and non-invasive process, it allows multiple switches between the Intracellular and Extracellular modalities, without the risk of any harm to the cell culture;

5. *Fast Impedance Monitoring modality*: used to measure the impedance of the electrodes (approximate value), it can also be used to study cell contractility by

applying small (0.5-5 nA) alternate currents to the electrodes, while measuring the electrode voltage in the channel (since the currents used are low, this functionality will not modify the cellular physiology);

6. *Impedance Spectroscopy modality*: used for non-invasive monitoring of cellular processes (can be applied also to non-electrogenic cells).

From all the modalities present on the chip, in our experiments we focused only on voltage recording, voltage stimulation and fast impedance monitoring, since these are the most relevant measurements for chip characterization.

2.1.4 **Device characterization**

Table 2.1 provides a comprehensive comparison of Imec's device and the other state-of the art devices introduced in '2.1.2 High Density CMOS MEAs'. Imec's chips stands out in different evaluation criteria. First, from the functionality point of view, our chip has the largest number (6) of interfacing modalities, with the possibility of doing Intracellular (InC) Recording which is only available for this chip and the one from Abbot et al. (2017) [9]. Other advantages in the functionality field are the small electrode pitch, second only to the Dragas et al. (2017) [8] work, which allows us to reach single-cell resolution, the possibility to enable multi-well assays and the ability of charge balancing, all while having the other characteristics very competitive compared to the other devices. Second, from the performance point of view, our chip achieves the highest temporal resolution and low noises when compared to these state-of-the-art devices.

In the performance section, after the total maximum power consumption comparison, the main characteristics we want to measure and evaluate are noise, impedance and stimulation (the last two will be considered in '2.1.6 Applications of the device'), since they can have the biggest impact on the functionality of our device.

	Park et al. (2018)	Dragas et al. (2017)	Abbot et al. (2017)	This work
Technology	0.13 μm	0.18 μm	0.35 μm	**0.13 μm**
Functionality				
No. Electrodes	1024	59760	1024	**16384**
Electrode pitch	58 μm	13.5 μm	126 μm	**15 μm**
No. Interfacing modalities	4 (ExC,CCS,IS,Opti.)	5 (ExC,CVS,CCS,IS,Chem.)	3 (ExC,InC,CVS)	**6 (ExC,InC,CVS,CCS,IM,IS)**
Enables multi-well assays	No	No	No	**Yes (16)**
No. Recording channels	4 (LFP,FB)	2048 (AP) 32 (LFP)	1024 (FB)	**1024 (AP,FB)**
No. Stimulation units	4 (I)	16 (V or I)	(Ext.)	**64 (V) + 64 (I)**
No. Indipendent stim. waveforms	4	6 (V or I)	3 (V)	**64 (V) + 64 (I)**
No. Sites for CVS*	--	N/A	1024	**4096**
No. Sites for CCS*	4	6	--	**64**
No sites for IS*	4 (V Source)	32 (V Source)	--	**64 (I Source)**
No. Sites for IM*	--	--	--	**1024**
Charge balancing	No	No	No	**Yes**
Intracellular recording	No	No	Yes	**Yes**
Performance				
Channel gain	22-412	30-7000	150-375	**2-3000**
Channel band width	0.1 Hz - 600 Hz 0.1Hz - 26 kHz	1 Hz - 300 Hz 300 Hz - 10 kHz	1 Hz - 5 Hz	**0.5 Hz - 10 kHz 300 Hz - 10 kHz**
Input-referred noise	12.6 μV_{rms} (FB) 7 μV_{rms} (AP)	5.4 μV_{rms} (FB) 2.4 μV_{rms} (AP)	250 μV_{rms} (FB)	**12 μV_{rms} (FB) 7.5 μV_{rms} (AP)**
CVS/CCS range	-- / ± 32 μA	± 1.5 V / ± 300 μA	4 V / --	± 1.65 V / ± 382.5 μA
CVS/CCS resolution (LSB)	250 nA	2.9 mV / 29 nA	--	**103 mV / 2 pA**
IS freq. range	100 kHz - 2 MHz	1 Hz - 1 MHz	--	**10 Hz - 1 MHz**
Temporal resolution of IM	N/A	10 ms	--	**0.1 ms**
ADC resolution	(Ext.)	10b @ 20 kS/s	(Ext.)	**10b @ 30 kS/s**
Total power	N/A	86 mW	12** mW	**95 mW**

*Simultaneously;**Stimulators not included; IM: impedance monitoring; IS: impedance spectroscopy; ExC: extracellular; InC: intracellular

TABLE 2.1: Functionality and performance comparison between Imec Sparrow chip (This Work) and state-of-the-art devices from '2.1.2 High Density CMOS MEAs'. [11]

Since the electrodes on the CMOS MEA chip are divided in four different size groups, it is possible to evaluate how the noise is changing depending on the different dimensions of the electrodes. Understanding this feature it's the key of knowing which size fits the best for our experiments in term of signal strength. These evaluations were previously performed in Miccoli et al. (2019) [10] during neuronal recording experiments. In this study, the total noise was summarized as the combination of two components: the readout electronics noise and the thermal noise. Thus considering both the chip characteristics and the electrodes-electrolyte/cells interactions. As a result, different signal-noise ratio (SNR) were obtained for each type of electrode (Figure 2.6).

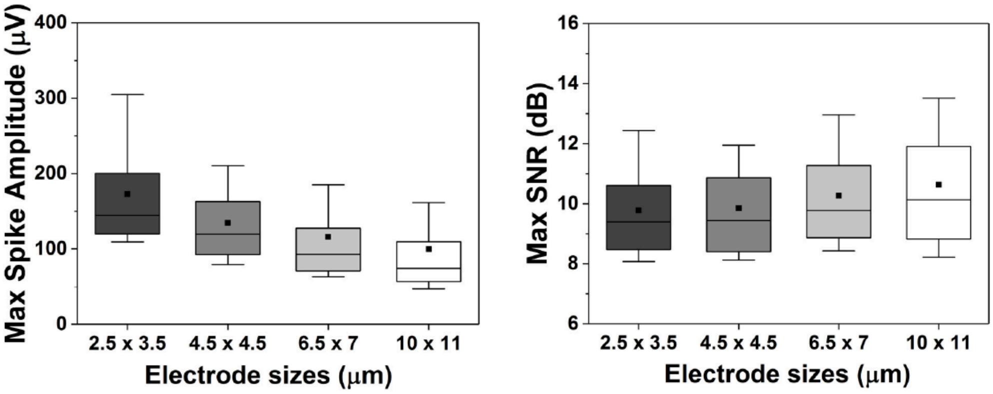
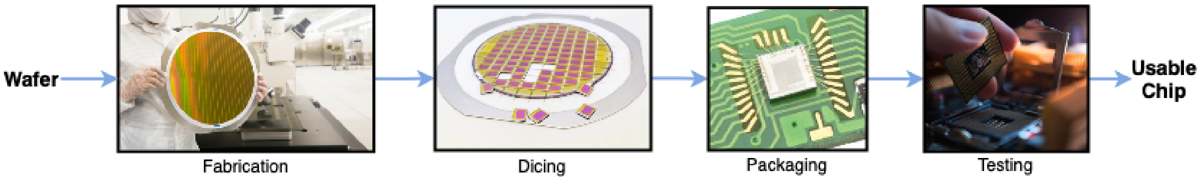


FIGURE 2.6: Boxplots of the different electrodes sizes for: maximum spike amplitude [left] and maximum signal-noise ratio (SNR) [right]. [10]

The comparison of these results remarked two different trends: while the max spike amplitude was higher in smaller electrodes (172.9±71.6 μV for the 2.5x3.5 μm^2 electrode) and lower in larger electrodes (99.9±70.1 μV for the 11x11 μm^2 electrode); the total maximum noise in the smaller electrodes (7.3±0.6 μV_{rms} for the 2.5x3.5 μm^2 electrode) was higher but still comparable with the total maximum noise recorded in the larger electrodes (6.4±1.3 μV_{rms} for the 11x11 μm^2 electrode). For this reason, a device with higher spatial resolution can be developed by exploiting only small (2.5x3.5 μm^2) electrodes. However, the presence of four different electrodes sizes allows the studying of different phenomena happening at very different scales.

2.1.5 **Packaging and encapsulation**

From the silicon wafer to the usable chip there are many different steps, which can be summarized in four stages. The wafer processing is the first stage, which is the core of the chip's fabrication as described in '2.1.3 The Imec HD CMOS MEA chip'. Second, after the chip's main structure is complete, the wafers are divided into individual dices. This dicing process prepares the chips for assembly, consisting in two major steps: wafer mounting and wafer saw. The final stage of our device fabrication is the packaging of the Integrated Circuit (IC). During this process, the chip is interfaced with a printed-circuit board on which it is mounted and connected; the main steps consist in die attachment, IC wire-bonding and IC encapsulation. Once assembled, our device is ready to use. However, because during the fabrication many things can go wrong causing malfunctions of the device, before using them for our experiments, they must be electrically tested. Our last stage, the IC testing, is used to assess the functionality of these devices. It is performed for every single chip and it has to be repeated for the same chip when manually encapsulated.



The integrated-circuit wire-bonding is the process of providing electrical connection between the silicon chip and the external leads of the semiconductor device using very fine bonding wires. The wires used for the wire-bonding of our chip are made of aluminum (Al) and connected to the bond pads through the process of Al wedge bonding. During this process, the aluminum wires are clamped and brought one by one in contact with the different pads, then an ultrasonic energy is applied, for a limited amount of time, to each wire while being pressed to the corresponding pad, forming the wedge bond between the two [13]. The wires are then run to the corresponding lead fingers, against which are then again pressed with the same modality. The wire is then broken off by clamping and moving away the wire (Figure 2.7).

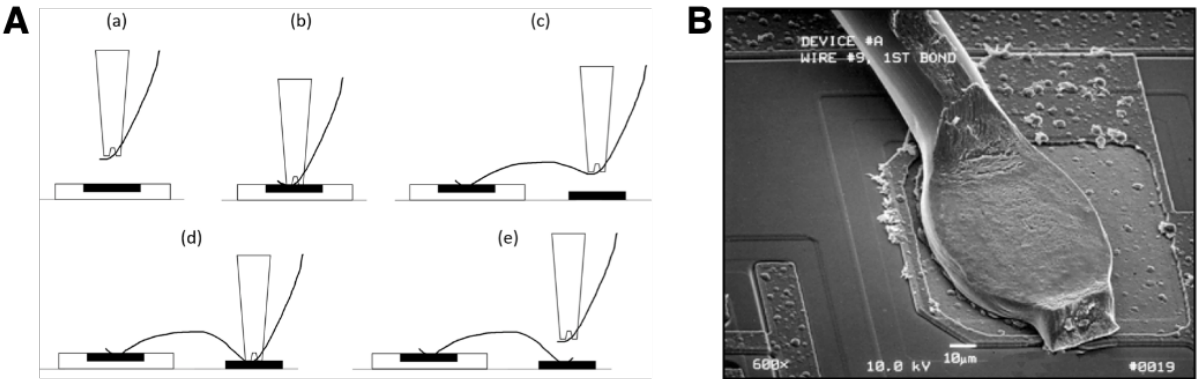


FIGURE 2.7: [A] Schematic outlining the wedge wire-bonding as a 5 (a-e) step process plus **[B]** SEM image of a typical bonding on an IC bond pad. [14]

For the encapsulation process, generally each research group develops its own packaging strategy which usually is not shared on the papers, like the three state-of-the-art chips considered before. If the specific epoxy used for a chip is always different, it is also true that it is something that almost every chip working with cell cultures has to do in order to avoid issues. One explanation of why the encapsulation process is fundamental for this type of devices can be found in Hierlemann et al. (2011) [15]. As written in the paper, and as shown in '2.3 Results', the chip and its components can be very sensible to corrosion, especially when considering active devices and long-term cultures.

2.1.6 **Applications of the device**

The key to success of these multi-electrode array devices in these neuroscientific fields is obvious when we consider their main advantages. First, they have long-term (weeks/months) multisite action potential readout, allowing constant evaluations of cell networks from the moment of seeding till the mature conditions. Furthermore, they have a very high control over the biochemical environment, since they require very small volumes of solution; for the same reason, they have a high tissue efficiency, needing a very small quantity of tissue for the seeding. Nonetheless, it is also possible to easily determinate functional changes, especially because of the close correlation between electrophysiological and morphological changes, which can also be detected by the combination of both electrophysiological and fluorescence readout.

For these reasons and as stated before in '2.1.1 Multi Electrode Arrays', this type of devices have a wide application both in the pharmaceutical industry, as biosensors or for drug-development, and in the academic environment, useful for a better comprehension of complex behaviors of neuronal cell networks.

To better picture the potential of MEAs, we can also analyze the different application fields of the state-of-the-art devices considered in '2.1.2 High Density

CMOS MEAs'. Regarding the device presented by Park et al. (2018), the first application was to study a cell-culture of rat cardiomyocytes for drug development in pharmaceutical industry [7]. The experiments consisted in the application of a biphasic current stimulation used to pace the cells, all while measuring the pacing threshold and capture rate, in both normal conditions and with the culture under the effects of a isoproterenol drug, demonstrating how the successful real-time optical measurement of cardiomyocyte beating can be exploited for massive, fully automated parallel drug-screening.

The MEA by Dragas et al. (2017) was used to analyze the average activity of a slice of dissociated rat cortical neurons, by recording its spike amplitudes triggered by a biphasic voltage pulse [8]. Thus proving to be one of the first chip to allow different measurement/stimulation functions to perform simultaneously while targeting multiple cells at once, paving the way to the possibility of making complex neurophysiological experiments.

The application by Abbot et al. (2017) was similar to the one of Park et al. (2018), it used a culture of neonatal rat ventricular cardiomyocytes to perform the first-of-its-kind high-precision network electrophysiology [9], which was possible by exploiting its intracellular nanoelectrodes, opening up to the possibility for a more precise tissue-based pharmacological screening for both cardiac and neuronal cultures.

For Imec's CMOS MEA device, Miccoli et al. (2019) employed a cell culture of primary rat hippocampal neurons (PHN) to assess the functionality of the chip through the evaluation of the culture's electrophysiological activity exploiting the Impedance monitoring and Voltage recording modalities (Figure 2.8) [10]. The chip was successfully evaluated, proving to be not only comparable to those of the best state-of-the-art systems but also having the potential to further improve the knowledge on the neuroscientific and drug-development topics. Most of our chip's success comes from the ability to perform three specific modalities: Impedance monitoring, Voltage recording and Cell electroporation.

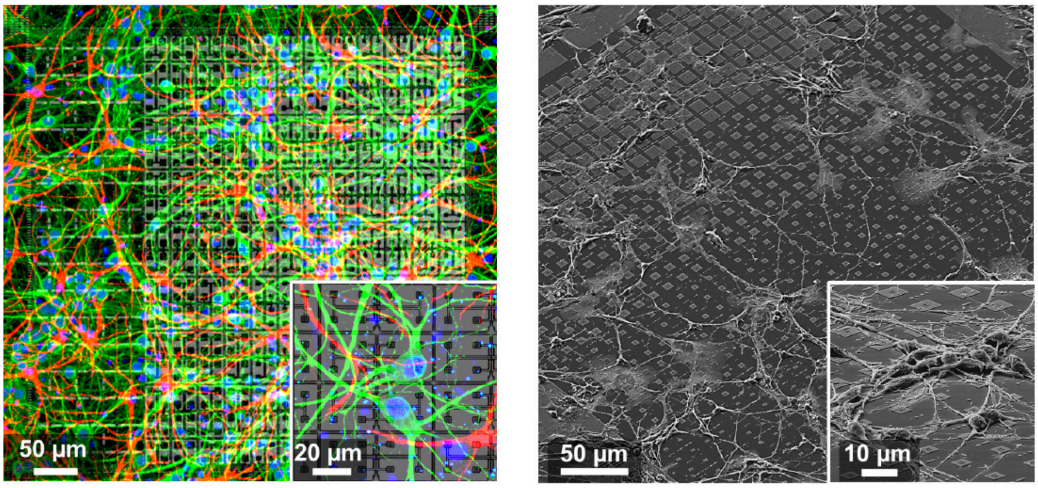


FIGURE 2.8: Confocal image of a 14 days-in-vitro immunostained[2] PHN culture, and SEM image of a 3 days-in-vitro PHN culture, all performed on a single area. [10]

To understand the reason why these modalities are so important, we have to give a brief introduction. The Impedance monitoring modality is used to measure the variations of the distance between the cultured cells and the different electrodes, exploiting the ability of the cell to act as a barrier for the current path, which is strongly correlated to the cell number and adherence. Thus, permitting to distinguish between a freshly seeded culture and a developed one just by applying a square-wave current excitation signal generated on the chip and then measuring the resulting AC voltage by the corresponding channel. The Voltage recording modality, which measures the different electrical potentials of the culture, is used to study the neuronal communication, permitting the simultaneous monitoring of both the culture electrophysiological activity and its growth over time, obtaining a potential fast microscope-free non-invasive electrical imaging technique. For the Cell electroporation, thanks to the single-cell resolution obtained through the small sizes and distances of the electrodes on this MEA, tiny transient holes can be made in single cells just by sending small currents through the electrodes, increasing the permeability of the cell membrane, allowing the introduction of chemicals, drugs or DNA inside the cell [16].

[2] Immunostained: chicken polyclonal anti-MAP2 antibody (ab92434, abcam) and goat anti-chicken IgY Alexa Fluor 488 (A11039, Invitrogen) were used to stain neurons, while polyclonal rabbit anti-GFAP (Z0334, Dako) and goat anti-rabbit IgG Alexa Fluor 568 (A11036, Invitrogen) was used for glia cells. [10]

This feature can be exploited to let transcription factors enter via these holes, reprogramming the cells into what the user wants (Figure 2.9).

By being able to perform all these modalities plus the other four, the potential applications of the device largely increases, allowing us to perform multiple evaluations in very diverse conditions on different cell cultures.

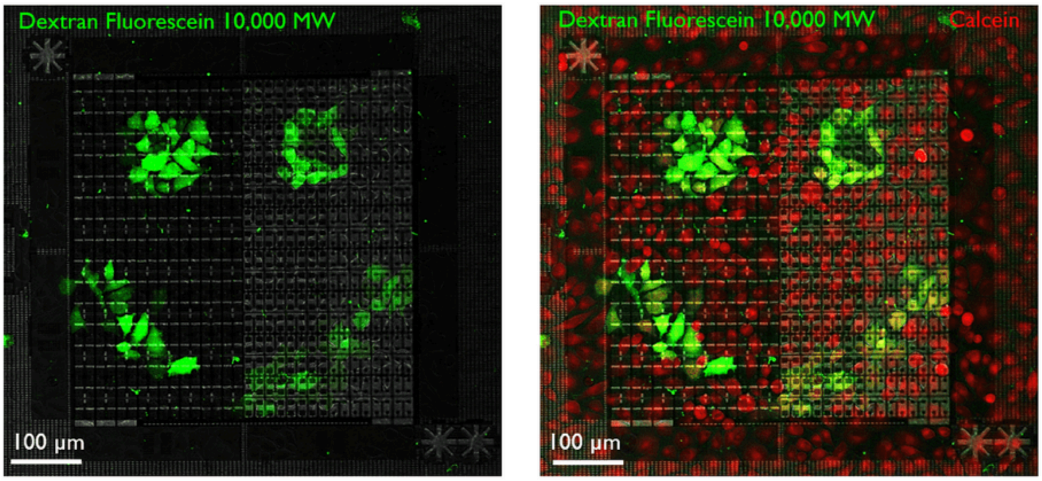


FIGURE 2.9: Example of confocal imaging of single-cell electroporation in combination with Dextran Fluorescein to recreate a desired pattern using neural progenitor cells. [17]

2.2 Materials and methods

2.2.1 Chip packaging and conditioning

Chip wire-bonding and packaging was performed by an external company (Taipro Engineering, Belgium). The resulting chip batches that were tested are summarized in Table 2.2.

	Taipro September 2020	Taipro December 2020
No epoxy*	30	20
External epoxy wires**	10	--
External epoxy full***	10	--
No. total chips	50	20

*No epoxy: naked chip wire-bonded to the PCB
**External epoxy wires: wire-bondings and their close surroundings are covered in epoxy
***External epoxy full: all electrical parts are covered in epoxy, plus a glass ring is glued on top of the PCB to contain cells and cell medium

TABLE 2.2: Summary of tested batches considered during our characterizations.

Prior to chip testing, the devices were prepared with UVO_3 treatment for 15 minutes to hydrophilize the surface. Next, an 8.4x8.4x5 mm (w-l-h) silicone insert (Ibidi GmbH, Germany) was carefully applied on the chip around the multi-electrode array between the active areas and the bonding wires using a stereomicroscope (Figure 2.10).

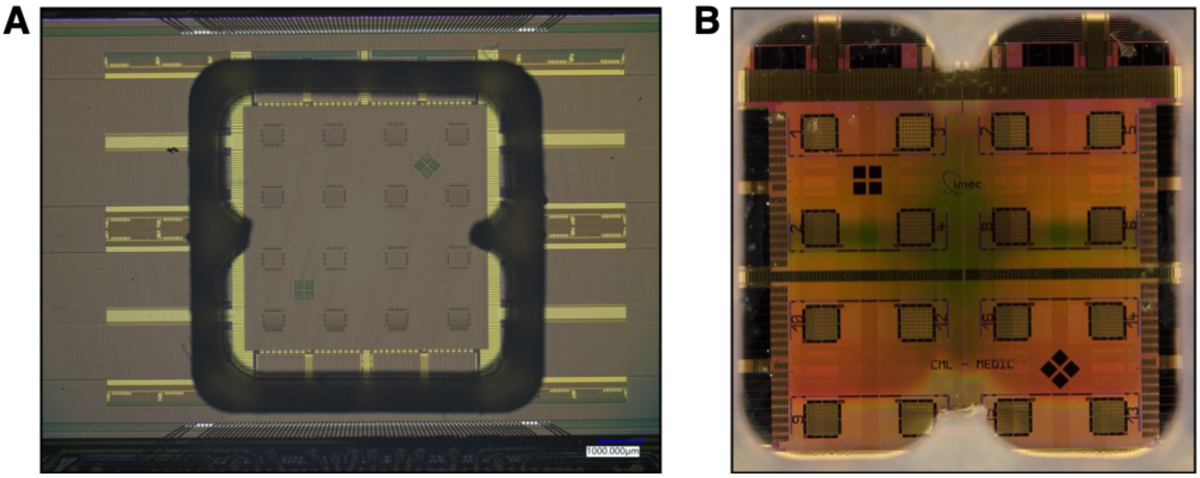


FIGURE 2.10: [A] Microscope picture of the applied silicone insert around the chip active areas plus **[B]** magnification of the active areas disposition, numbered from 1 to 16.

The chips that were not encapsulated by the packaging company ('no epoxy' chips) (Figure 2.11), were encapsulated in-house with a biocompatible epoxy after a first testing process, shown in '2.2.3 Chip testing'. More specifically, the two components EPO TEK 353ND-T epoxy was employed. It has interesting characteristics: it is highly thixotropic, with non-flowing properties and has high temperature resistance. To perform the encapsulation, the silicone insert was removed from the chip, which was then processed through UVO_3 treatment for 17 minutes. Next, the chip was placed on a hot plate at 60° Celsius inside an inorganic chemical hood, while the epoxy was prepared mixing the two components (named Part A and Part B) with a 10:1 ratio. After the preparation, the encapsulation was carried on with the help of a syringe and, after completing the packaging, the chip was placed inside a vacuum oven for 5 hours to cure the applied epoxy.

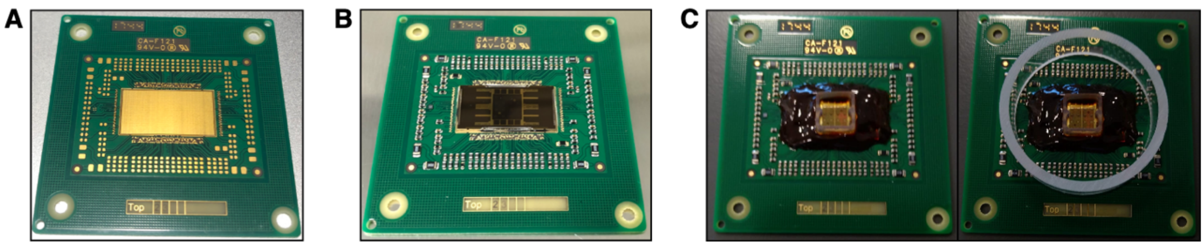


FIGURE 2.11: Photographs of **[A]** printed circuit board (PCB) used for chip packaging, **[B]** 'no epoxy' Taipro chip and **[C]** manually encapsulated chip with insert plus glass ring used in 'external epoxy full' Taipro chips for comparison.

2.2.2 Calibration and testing hardware/software

As shown in the diagram in Figure 2.12, the experimental chip testing setup consisted of few components. As the chip is wire-bonded to the printed circuit board (PCB), this one is screwed inside a grey frame used to steadily connect the carrier PCB with the battery-powered mother PCB. Then, these two boards are connected to the lab computer through an I/O custom setup hardware, allowing both the recording and the programming (Inf4med software) of the wire-bonded chip.

Additionally, to compensate the input errors from the chips channels, we performed ADC calibration by connecting a function generator to the main battery-powered custom setup board (mother PCB). The connection was made through a BNC connector with 2 jumpers, while the generator's output was set as a sinusoidal voltage generator signal with frequency 1kHz, amplitude 600 mV_{pp} and offset 600 mV.

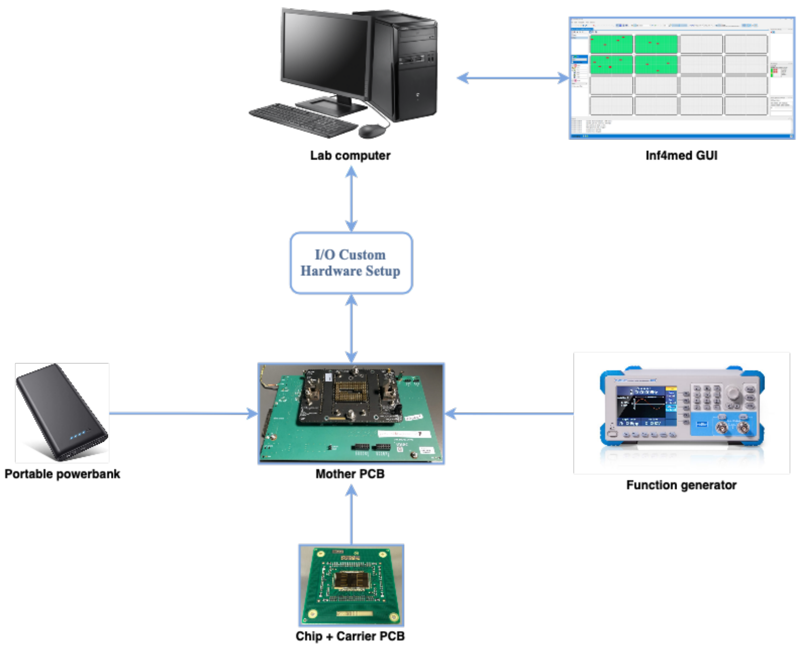


FIGURE 2.12: Experimental setup for chip testing.

On the lab computers, a in-house custom made GUI is available to connect the system with Imec's CMOS MEA chips. This Inf4med application has a user friendly multi-document interface that allows the user to create and upload Sparrow configuration maps/settings, acquire, record, visualize and postprocess data. However, for the testing process we used two premade configuration maps (Figure 2.13), set to evaluate only 4 of the 16 active areas.

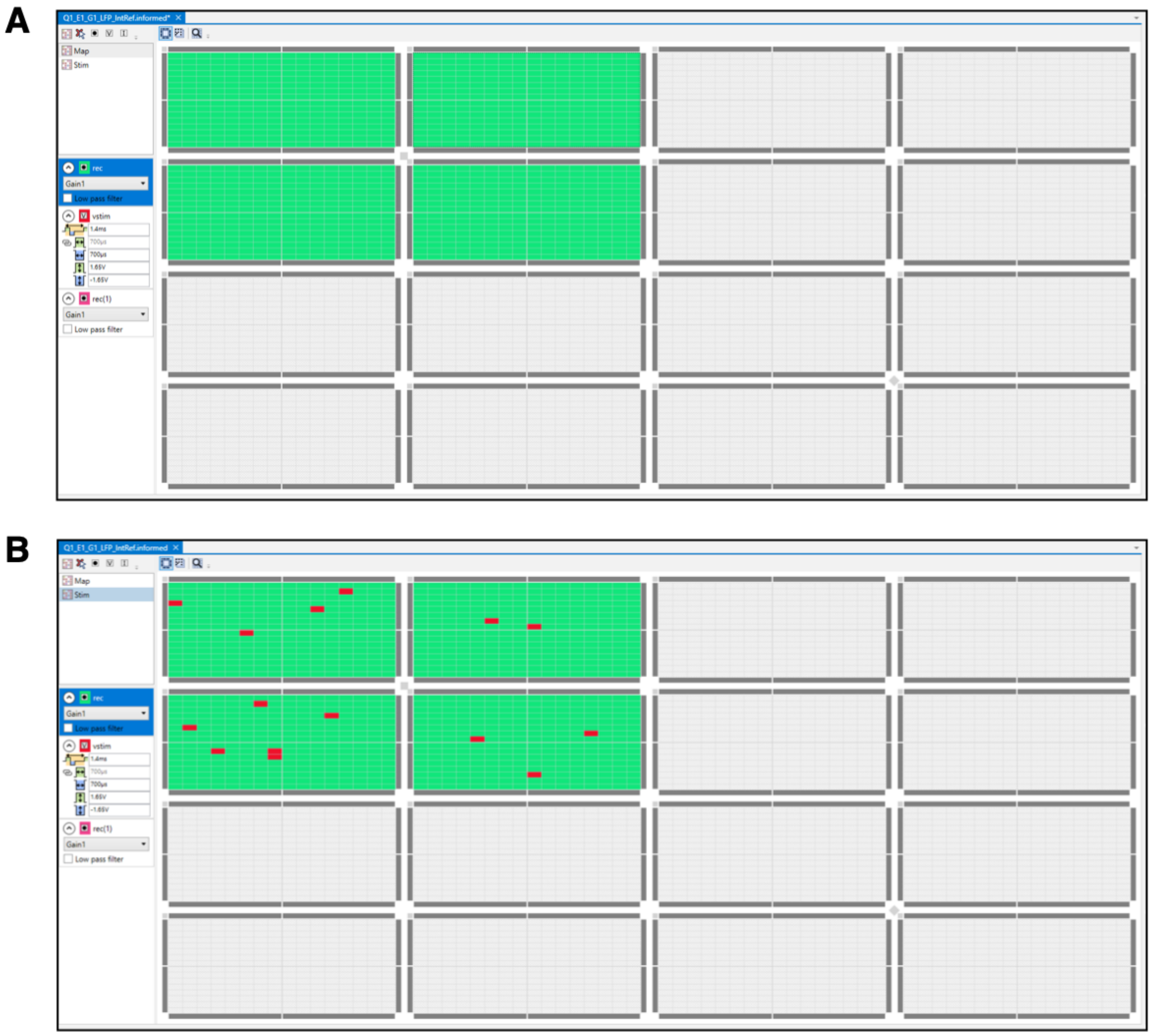


FIGURE 2.13: Inf4med premade configuration maps used for **[A]** voltage recording test and **[B]** voltage stimulation test of the first 4 wells.

2.2.3 Chip testing

The chip testing process was divided into two stages, as shown in Figure 2.14. After the preparation of the setup, the first testing process, named Dry testing, was used to quickly discern between working and broken chips. In this case, only the correct connection between the chips and the setup was evaluated, performed without the need to use saline solution (PBS) during the measurements.

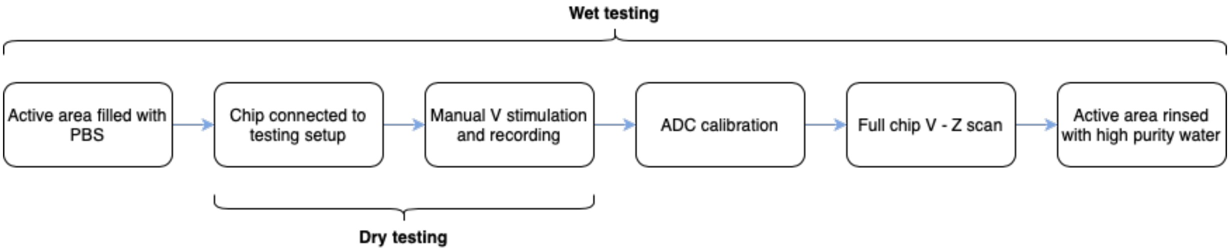


FIGURE 2.14: Comparison between Wet and Dry testing stages.

As a result, after this first stage, the working chips needed to be re-tested. In this second case, named Wet testing, the chip area surrounded by the insert was filled with 200 µl of PBS. The chip was then carefully connected to the chip holder of the battery-powered custom setup board (mother PCB), which was previously connected to the function generator. After securing the connection between the chip and the custom setup board, the chip was covered by a carton box to avoid light interference. Once all parts of the system were successfully connected and working, the calibration and evaluation of the chip started by running the Inf4med application on the computer lab. After controlling that the right sampling frequency of the chip for the communication was 30kHz, a first manual voltage recording was conducted using premade configuration maps to verify the noise performance. A second test was then carried on to control the correct functioning of the voltage stimulation and the uniformity of the applied signal. In the end, the ADC calibration and the full chip scans (Voltage recording and Impedance measurement) were automatically carried on for all the active areas of the chips. The results of this testing and the calibration pack were then saved in the bio-lab cloud storage.

This procedure was performed one single time for the working ‘external epoxy wires’ and ‘external epoxy full’ chips. For the ‘naked’ ones instead, the procedure was repeated after their in-house encapsulation, to ensure the correct working of such packaged chips and to record any alterations in performance.

After the execution of the tests, the custom bench setup was disassembled. The chips were freed from the grey frames and the region of the multi-electrode array (surrounded by the insert) was rinsed three times with high purity/deionized water to remove any trace of PBS.

2.2.4 **Electrode mapping**

In order to confirm that the electrodes in the CMOS MEA chip were correctly addressed by the software, an assay based on pH imaging was developed. BCFL (AAT Bioquest, USA), a pH sensitive dye indicator, was used to visualize pH changes at the electrodes which were triggered by applied stimulation voltages. The pH of the solution surrounding the electrodes varied because of the stimulation induced Faradaic reactions occurring at TiN electrode surfaces. The BCFL indicator was diluted in high purity water with respective 1:99 ratio. Next, the solution was mixed and put on the multi-electrode array of the Sparrow chip. To perform these evaluations, we prepared the same chip testing setup discussed in '2.2.3 Chip testing', with the CMOS MEA chip under the focus of the confocal microscope. The imaging was then performed by a Zeiss 780 Confocal Laser Scanning Microscope (CLSM) with a 20x water immersion objective. To correctly perform this imaging, we had to manually insert the different active areas positions inside the microscope GUI (Zen software). Then, using a Inf4med custom configuration map (Figure 2.15), we timed for each active area the stimulation of the four different electrodes of the pixels with the acquiring protocol of the microscope. During this procedure, the indicator was excited with both a 440 nm and 505 nm laser to measure the pH variations. After singularly studying each single well, all the acquisitions were saved and processed using ImageJ to increase the quality of the images.

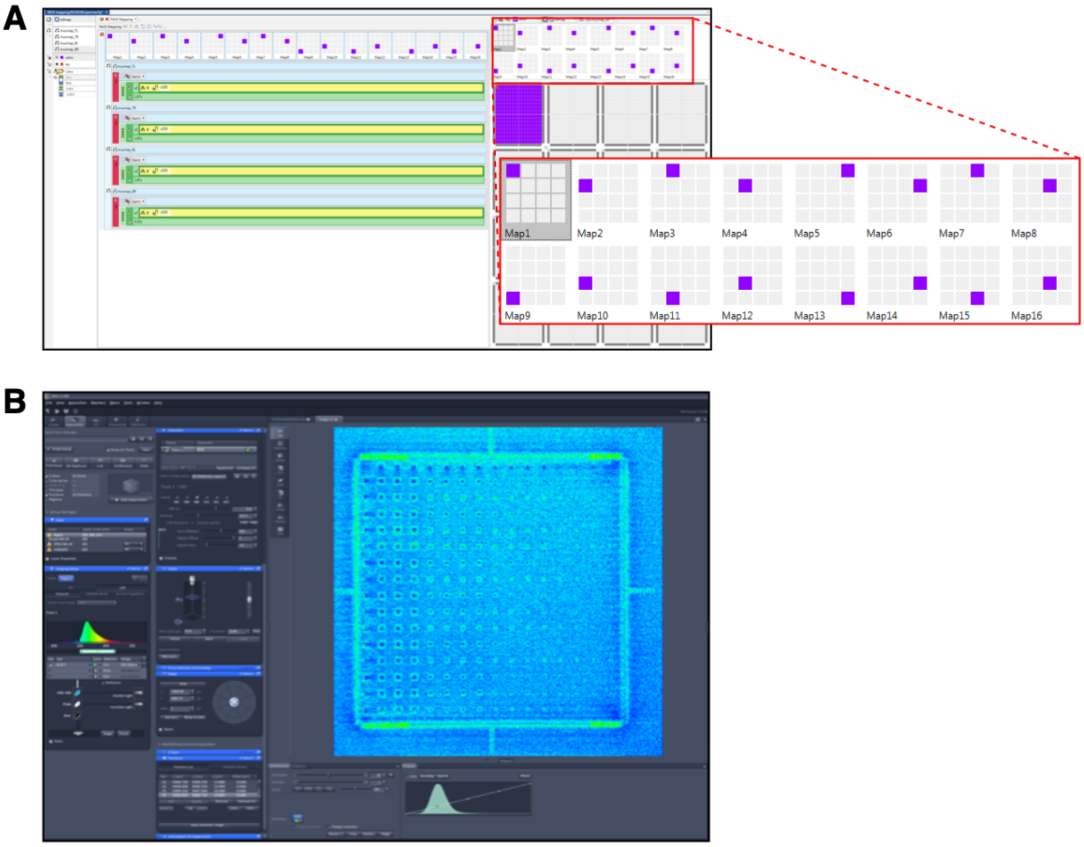


FIGURE 2.15: [A] Inf4med custom stimulation map used to trigger the different electrodes at specific intervals, with a focus on the active areas sequence, and **[B]** Zen software used to record the stimulation.

2.3 Results and discussion

2.3.1 Chip characterization

As previously discussed in '2.1.5 Packaging and encapsulation', a good wire-bonding of the chip is essential for the obtaining of a good working device. During our testing experiments we had the opportunity to study and evaluate both a bad wire-bonded chip batch (Taipro September 2020) as well as a good wire-bonded batch (Taipro December 2020). Thus, giving us the opportunity to have a practical experience on how this stage can influence the output of the whole fabrication process, Table 2.3.

Testing output	**Taipro September 2020**	**Taipro December 2020**
Fully functional* or Partially functional**	17 (6* + 11**)	16 (11* + 5**)
Cannot be powered/acquire	33	4
*Fully functional: all channels working and good noise levels. **Partially functional: noise too high and/or some channels are broken.		

TABLE 2.3: Results comparison between the two tested chip batches.

As a result of the bad wire-bonding performed by the external company (Taipro Engineering, Belgium), the yield of the first batch (50 chips, September 2020) is 34%. For comparison, the second tested batch (20 chips, December 2020) has a yield of 80%, while a greater previously tested third batch (50 chips, March 2020), had also a yield of 80%. To calculate this output, both fully functional and partially functional chips were considered over the total number of chips, since both can be exploited to perform different experiments.

From the physical point of view, the difference between good and bad wire-bonding is easily recognizable by using a standard microscope (Figure 2.16). A bad wire-bonding is usually characterized either by the superimposition of the nanowires on different bond pads, or their complete rupture. Unfortunately, because of the presence of a thick epoxy layer performed during the encapsulation process, this feature was clearly visible only on the 'naked' chips.

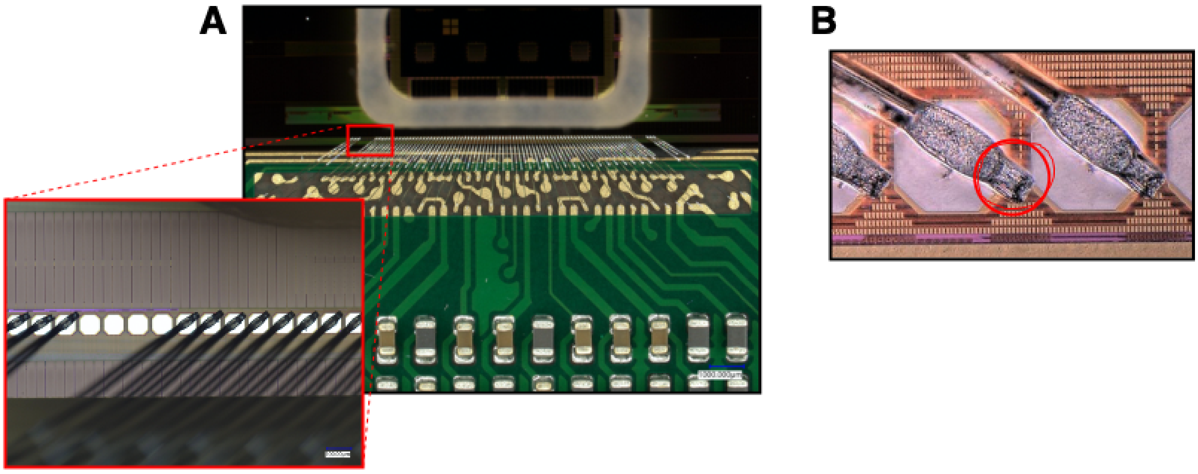


FIGURE 2.16: Microscope pictures of **[A]** correct wire-bonded 'naked' chip, with a focus on the wire-bondpad connections, and **[B]** bad wire-bonding example with the red-circle remarking the connection of a single wire with multiple bondpads.

During the dry testing of the chips, not-working chips were easily recognizable because of their initial problems. These issues mainly concerned the powering up of the chip or the connection with the setup. However, for the differentiation between 'fully working' and 'partially working' chips we needed a more precise evaluation. For this purpose, we exploited the Inf4med software to check that every important feature of the chip, like the acquisition and stimulation processes (Figure 2.17), was working correctly. If the device was working flawlessly, the chip was labeled as 'fully working'. In the other case, we had to remark which problems presented and decide whether it could be suitable for experiments. Unfortunately, this process was based on a qualitative evaluation mainly relying on personal experiences, meaning that no rigorous methodology based on quantitative results could be applied.

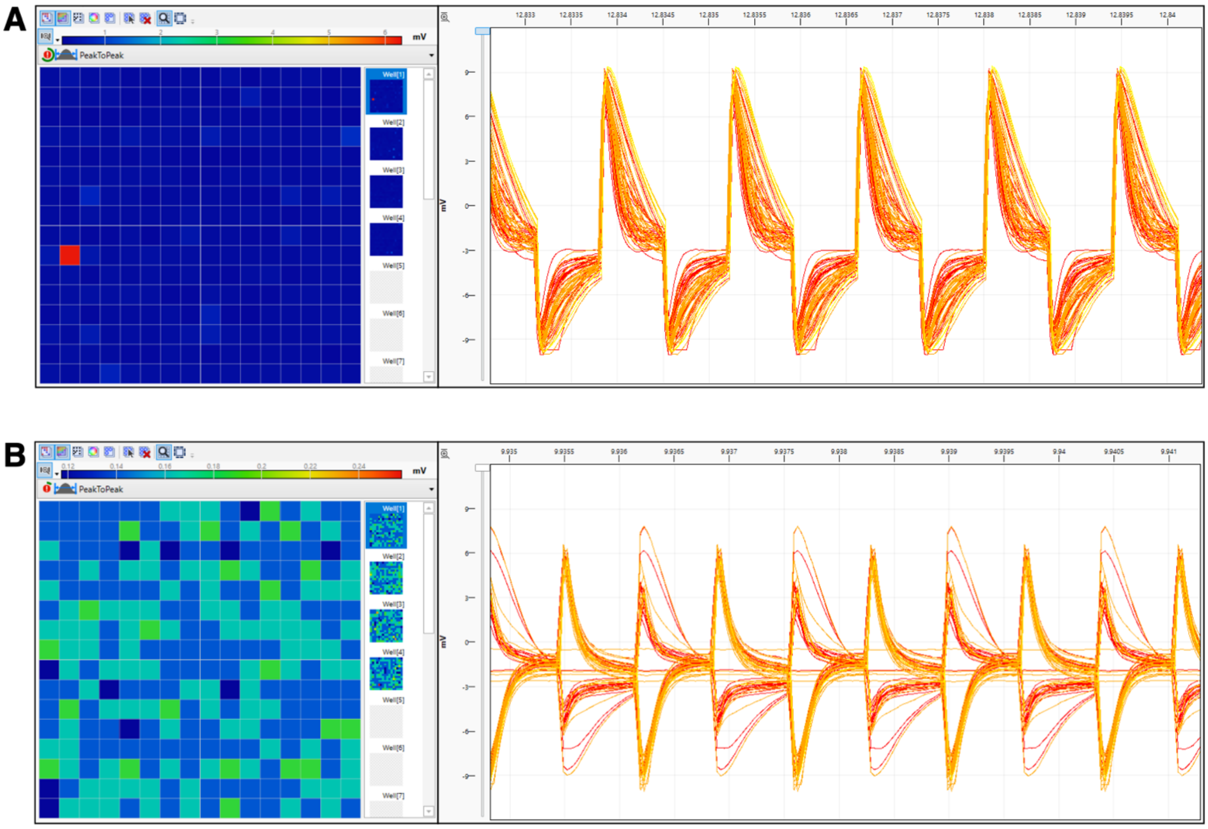


FIGURE 2.17: Pictures of In4med voltage recording electrode map and voltage stimulation acquisitions of **[A]** full working chip and **[B]** partially working chip.

2.3.2 Chip packaging and chip corrosion

The problem of short-circuit, caused by the presence of a conductive liquid between the nanowires and/or the different chip's components, is very common during electrophysiological experiments. However, the corrosion of the chip's electrical components is even more significant for chips fabricated with CMOS technology, since they are not designed to being immersed in PBS solution for very extended periods of time (weeks/months). Furthermore, this situation worsen when considering the possibility of using the modalities featured by these devices such as voltage/current stimulation. These features can create different redox potentials while delivering voltage/current pulses, causing severe electrochemistry issues and the corrosions of the materials composing the chip, aluminum in the first place [15]. For these reasons, a good encapsulation is mandatory when working with cell cultures since it both protects the chip against these chemical reactions, caused by either the featured modalities and the cell culture itself, and prevent the exposition of such cells from toxic materials released by the chip, avoiding their premature death.

In our case, after each processed chip was mounted and wire-bonded onto small PCBs, we used the EPO TEK 353ND-T. This epoxy is two component, highly thixotropic with non-flowing properties and high temperature resistance, perfect to encapsulate the bond wires and pads. Considering how this encapsulation was performed by the external company and its characteristics, we divided our batches of chips in three different categories as previously described in '2.2 Materials and methods'.

One practical example of the importance of this encapsulation process is shown in Figure 2.18. In this microscope pictures, the corrosion effect is remarkable all around the different electrical components right outside the surface covered with the epoxy layer.

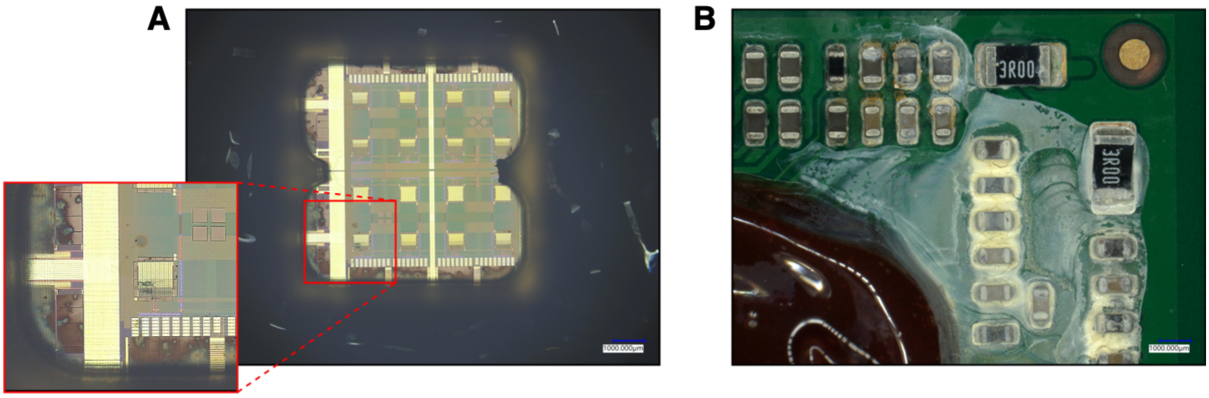


FIGURE 2.18: Microscope pictures of **[A]** corrosion on the chip active area, with magnification on corrosion effects, and **[B]** corrosion on the PCB electrical components.

There are no visible performance differences between 'external epoxy wires' and 'external epoxy full' chips. Considering these results, to avoid corrosion problems the ideal epoxy layer should cover all electrical parts in the surroundings like the 'external epoxy full' chips.

However, more issues arose after the packaging process was entrusted on an external company. Unfortunately, a problem concerning the internal distance between the encapsulation layer and the MEA's active areas occurred during the testing of Taipro September 2020 chips (Figure 2.19). To reduce and secure the cell medium volume during the experiments, we needed to plug small (8.4x8.4x5 mm) silicone inserts around the MEAs active areas. Because of the limited amount of space between the wires and the electrodes, the presence of unnecessary epoxy can interfere with the attachment of such inserts, causing leaking. As a result, the few last packaged working chips of this batch resulted completely unusable, forcing us to return all the chips of this batch.

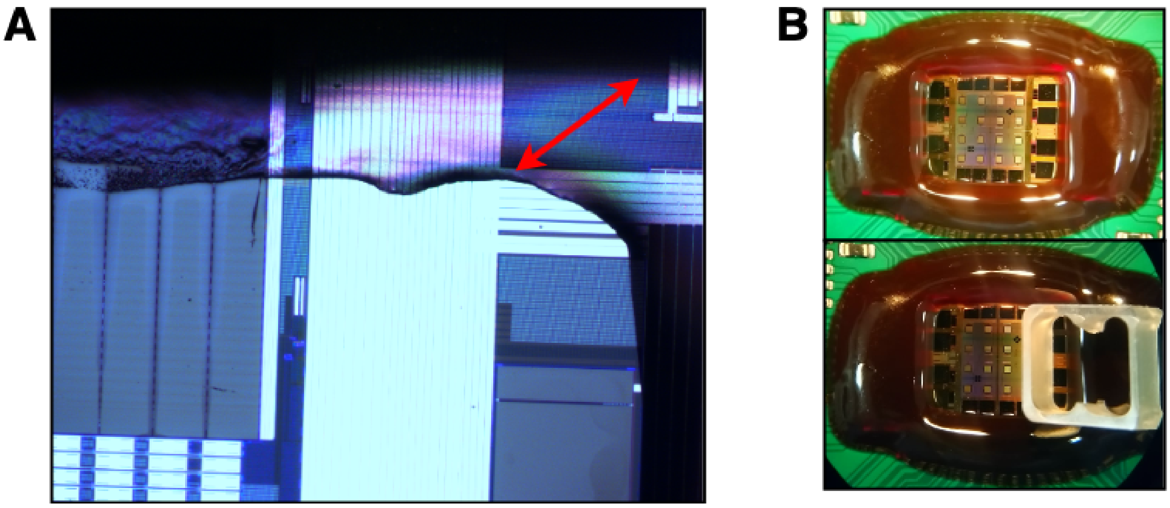


FIGURE 2.19: Microscope pictures of **[A]** chip internal area covered by an excess of epoxy and **[B]** practical example of epoxy excess consequence on 'external epoxy wires' Taipro September 2020 chip.

2.3.3 Electrode mapping

As previously discussed in '2.2 Materials and methods', we recorded the electrode activation map of all the active areas of numerous chips, using the Zeiss 780 Confocal Laser Scanning Microscope (CLSM). With this mapping, we wanted to confirm that the chip evaluations performed during the chip testing could be correctly achieved by the solely exploitation of the premade configuration maps used with inf4med software. Secondly, we wanted to control the correct association between the interface programmed electrodes and the stimulation on the chips, thus proving the correct coincidence between what the user program and what it is obtained on the practical level. For this reason, we decided to perform the electrode mapping on multiple chips coming from both working and non-working batches, to confirm the differences. A practical example of the obtained results is shown in Figure 2.20.

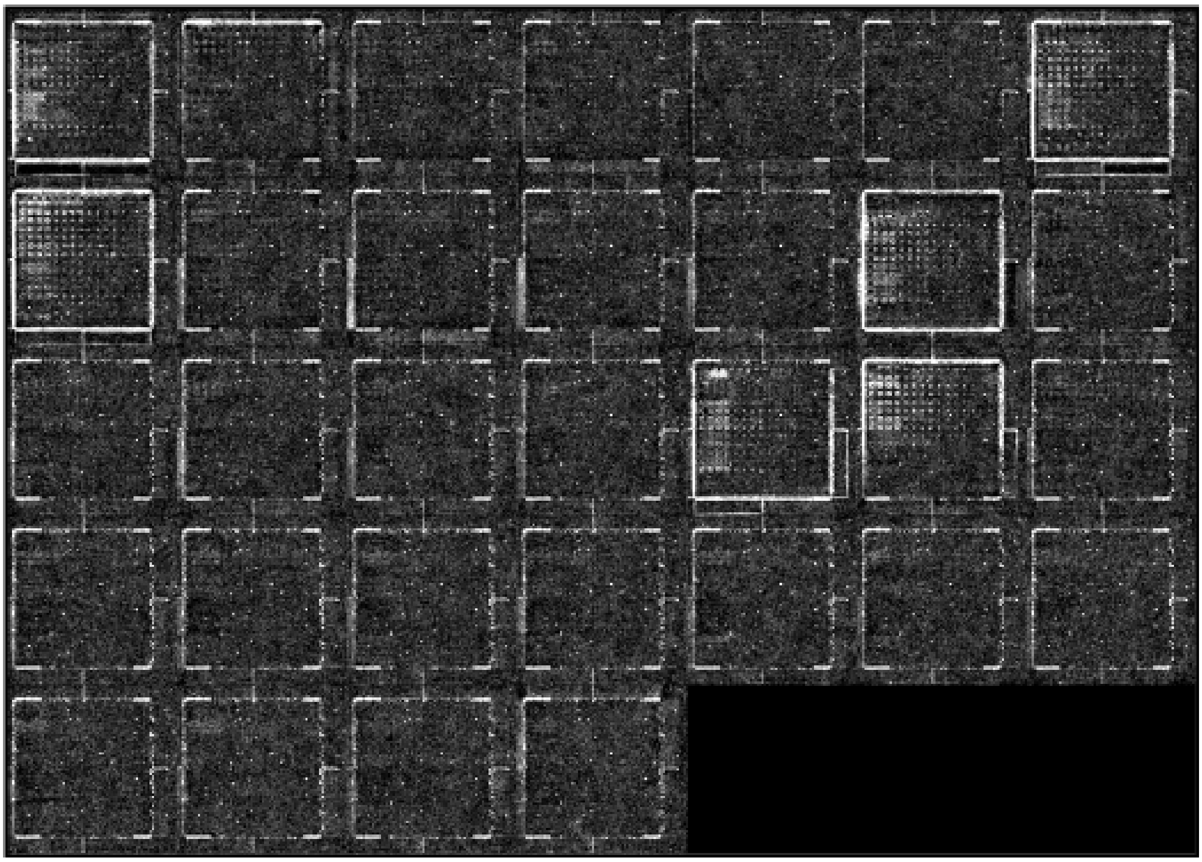


FIGURE 2.20: Sequence of 32 frames obtained using the confocal microscope during the imaging of one chip single active area.

To better comprehend the results over the time sequence, we decided to modify the images using ImageJ application. In this case, we post-processed the image sequences by adjusting their brightness and using a temporal-color code to mark the activation of each electrode, obtaining Figure 2.21.

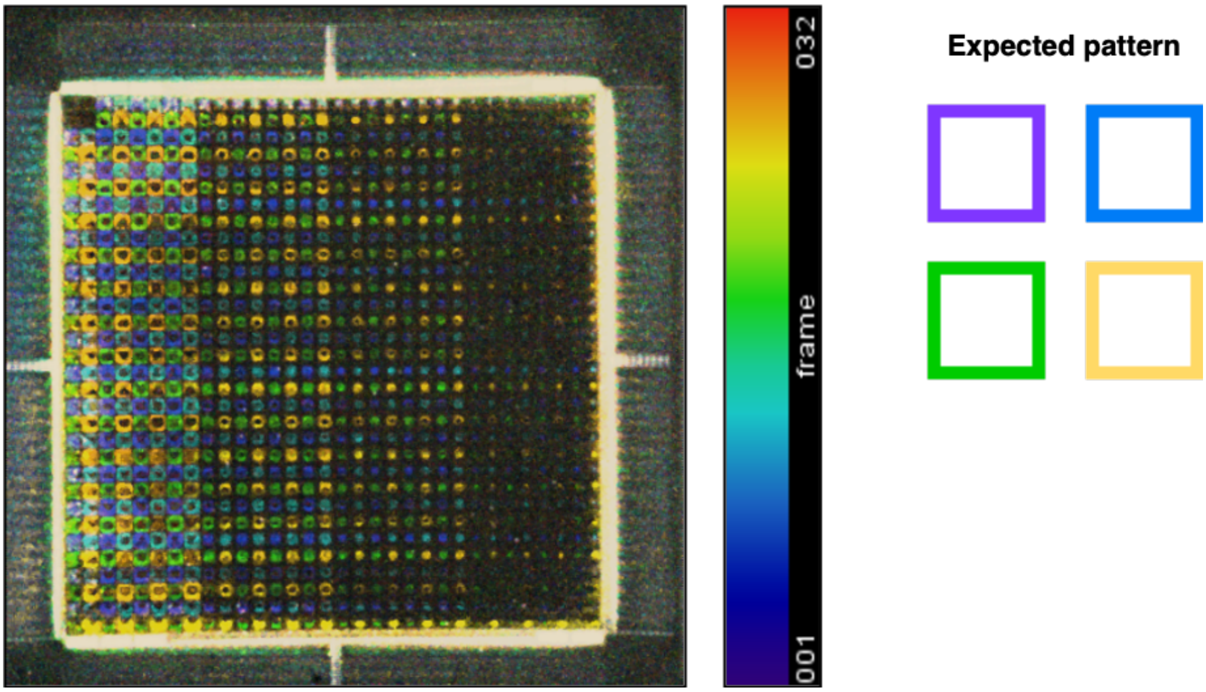


FIGURE 2.21: Temporal-color codification of the 32 frames image acquisition for a single active area plus expected correct pattern.

Thanks to this procedure, we were able to distinguish whether the 'fully working' chips were really working correctly. As a result, we noticed that some of the tested chips, from Taipro December 2020 batch, remarked some operational problems that were not visible during the previous '2.2.3 Chip testing' (Figure 2.22). These discrepancies were caused by the limited tested area set for the stimulation test map used during Dry and Wet testing, proving how qualitative these first assessments were. Nonetheless, some other chips showed minor stimulation discrepancies probably due to some small wire-bonding problems (Figure 2.23).

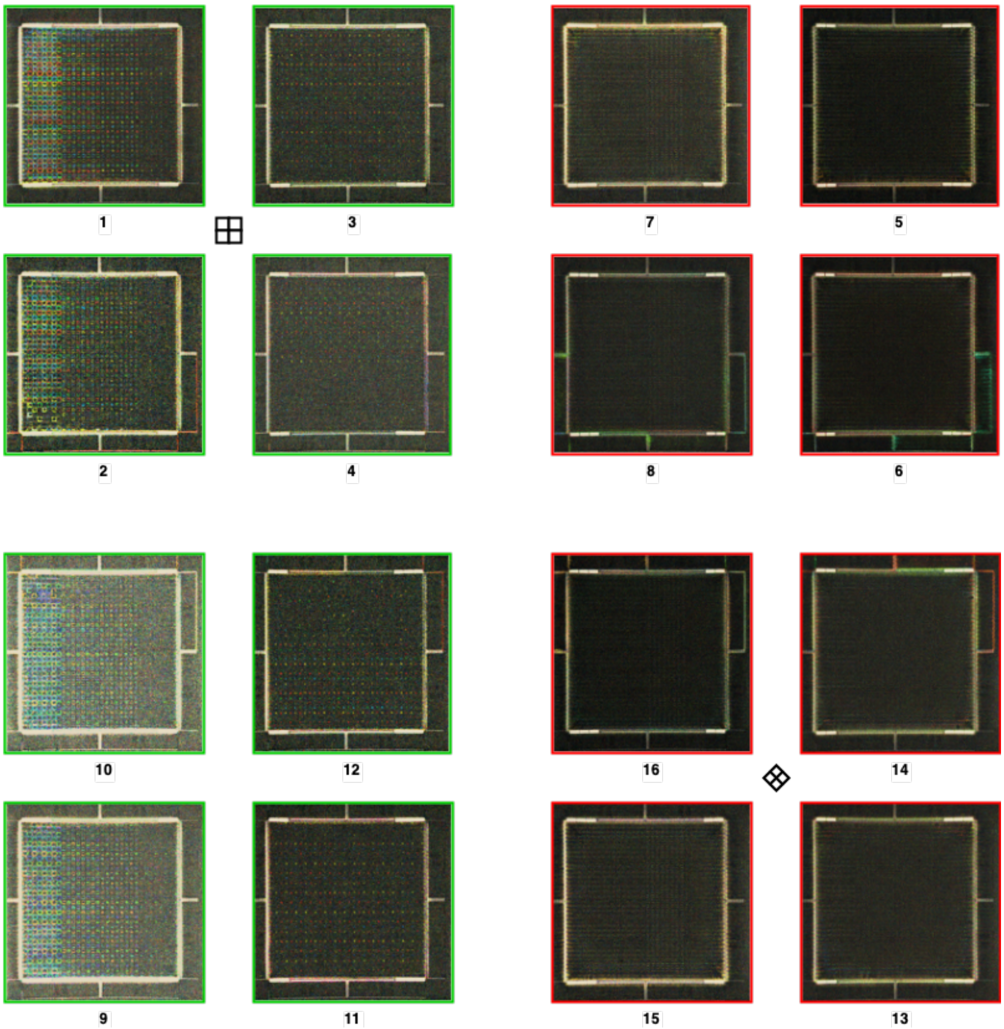


FIGURE 2.22: Picture of all the temporal-color coded active areas of a previously Wet tested 'working chip' from Taipro December 2020 (chip E7G). The green wells are working while the red ones are not responding.

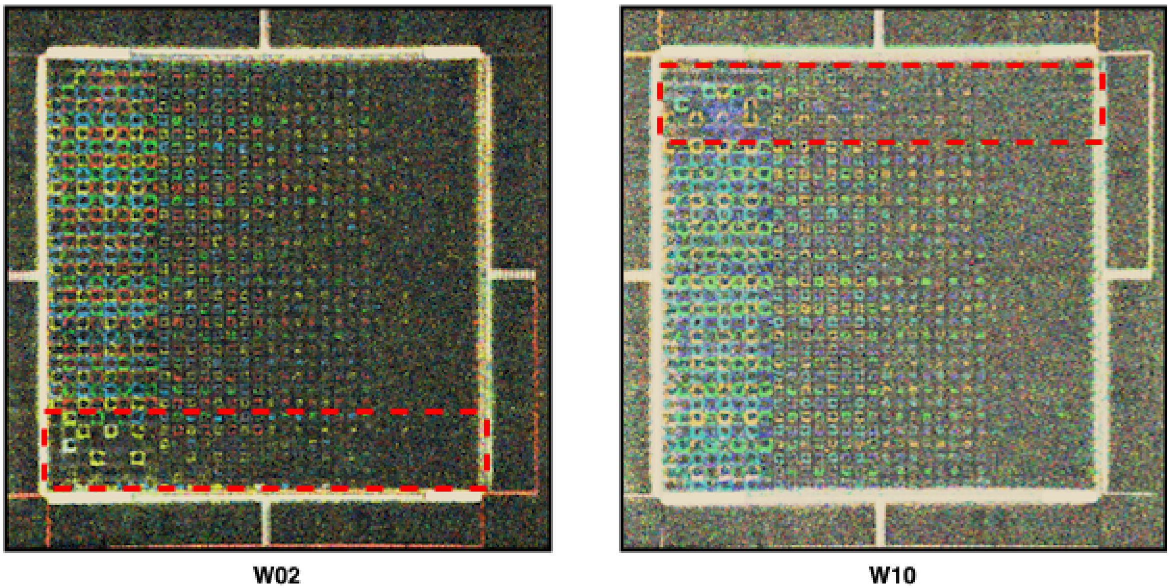


FIGURE 2.23: Pictures of two temporal-color coded wells from a 'working chip' with the focus on some minor stimulation related issues.

3. Imec Sparrow Database

3.1 State of the art

The HD CMOS MEA chips shown in ‘Chapter 2: Sparrow chip’ can be used for different experiments. As every experiment can include a multitude of devices working in parallel, a great quantity of chips (100+ per year) must be tested and prepared for such purpose. As a result, a database is required to efficiently manage all the chips data and their respective experimental information.

The original Sparrow chip Database consisted in one Microsoft Excel file containing all the chips data (Figure 3.1). It contained information about the general characteristics of the chips, from their wafer coordinates and packaging status to their testing data and experiments history. Different colors were used to differentiate between ‘Good’ (green), ‘Acceptable’ (yellow) and ‘Bad’ (red) chips. As this system can be a valid temporary database with few devices, it clearly showed a lot of long-term issues, having problems with both information filtering and data clustering. This Excel database was freely accessible for all the Imec’s lab users. Since different users had different ways to evaluate, the lack of a rigorous method to fill in the various fields of this database strongly hampered its efficiency, creating evaluation discrepancies between similar chips. As this method proved to be very easy to use, its great flexibility in the overall evaluation system and the absence of the chips’ availability information caused it to be insufficient to correctly track every single chip.

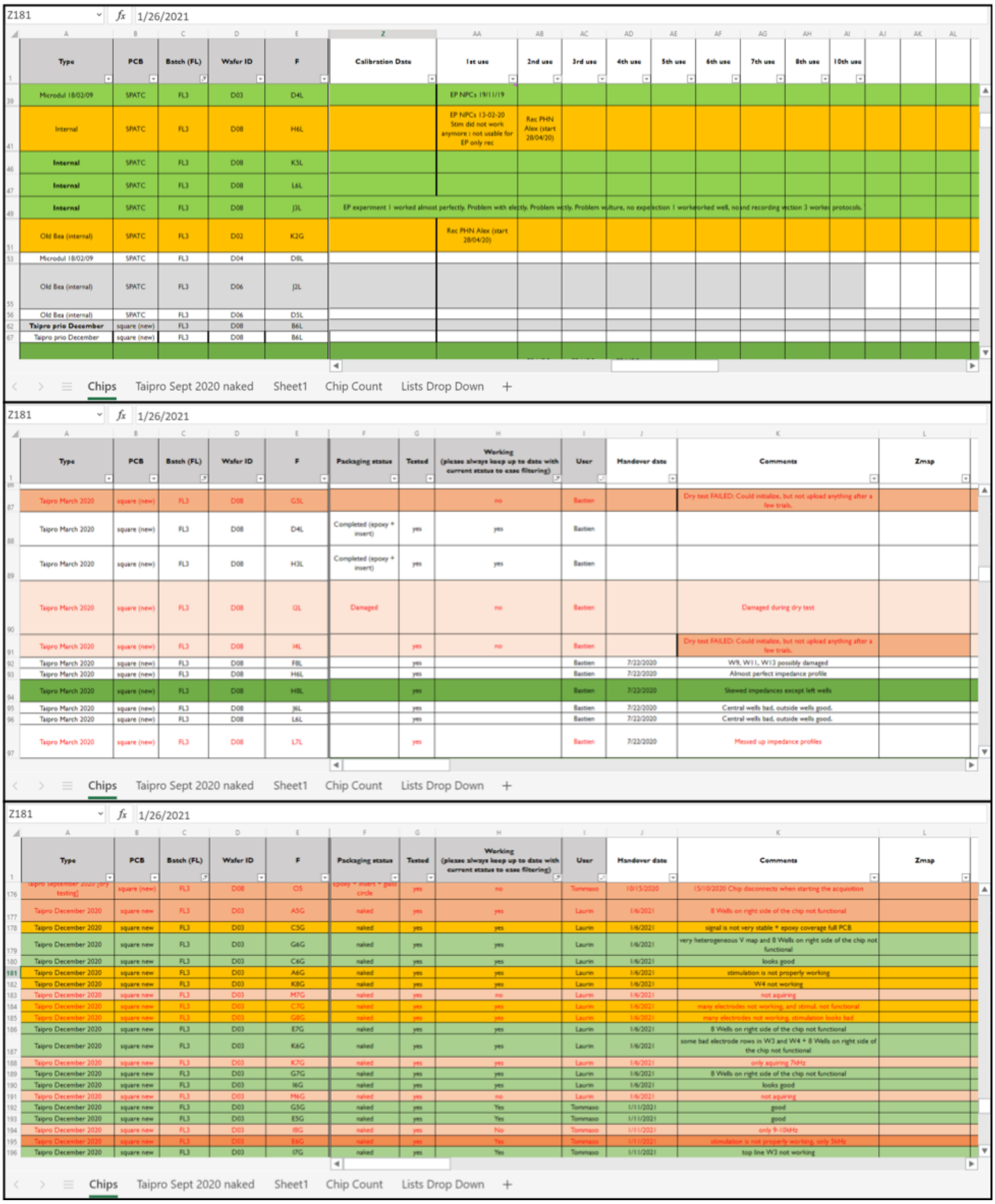


FIGURE 3.1: Pictures of the old Microsoft Excel database.

For these reasons, a first prototype of a new database was developed during 2018 using Microsoft Access (Figure 3.2). It consisted in two different tables (Chip_Tracker and Usage) filled using a form with a great multitude of fields. This new structure managed to solve most of the previous issues, however its poorly ergonomic user-interface caused many users to return back to the old Microsoft Excel database, discouraging the use of the new one.

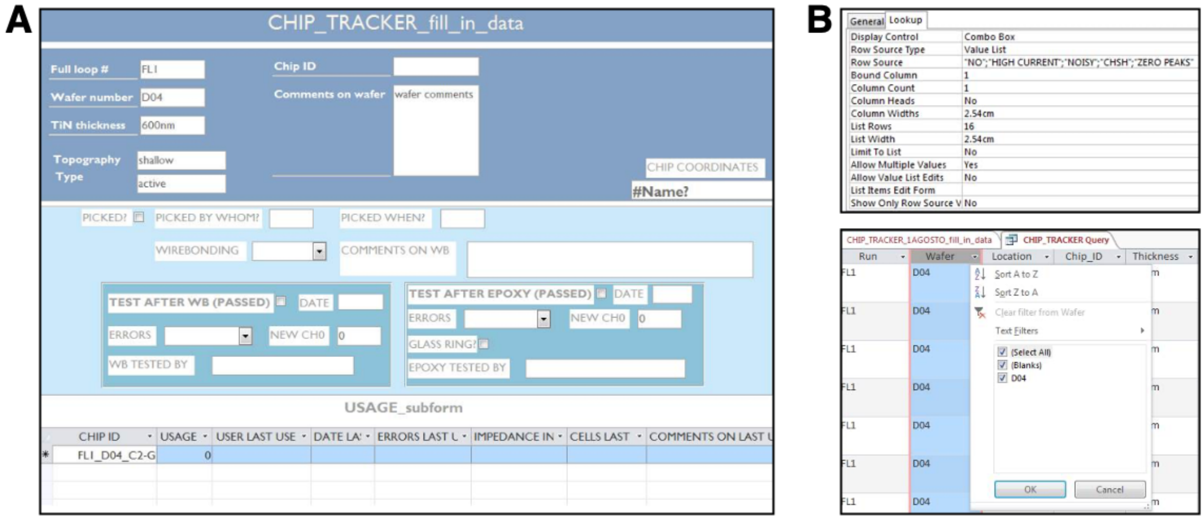


FIGURE 3.2: Pictures of old Microsoft Access database (2018), with focus on **[A]** form to fill to insert new data and on **[B]** database tables.

Because of the situation described in 'Chapter 1: Motivation of the final project' and these previous considerations, we decided to design and develop a new valid database to store all the chips information. Since every user of the lab had to use the personal Imec's laptop as the workstation, we opted for a selection of the pre-installed softwares. For our purpose, a multitude of different options were available in Imec's application catalog. However, because of time reasons and ergonomic features we decided to go for three of them: Ms SharePoint, Ms Excel and Ms PowerBI.

3.2 Methods

After the selection of the most suitable programs for our Sparrow Database, we started designing the new database while trying to preserve the previous Ms Excel structure. In this case, we assigned different objectives to each program:

- Ms Excel: as a very intuitive program for lists, it is the first step into the Database, exploited to facilitate the insertion of large amounts of new data.

- Ms SharePoint: is the Sparrow Database itself, it is used to contain all the chips information, while making it shareable with all the authorized users, and the user chip-requests.

- Ms Outlook / Teams: are the communication channels, they are automatically programmed to connect the Sparrow Database with the Users / Supervisors in order to simplify the request procedure, they can also be used for general automated communication from the Database.

- Ms Power BI: is the easiest way to have a general look on the whole Database, allowing to perform quick measurements automatically (eg. Number of chips available, Average max chip-impedance,...).

Once the structure of the Database was programmed as shown in Figure 3.3, the whole system was evaluated by lab users to have feedback. During this process the Database has been continuously tested and modified in order to fulfill all the different requests, obtaining the final result shown in '3.3 Results and discussion'.

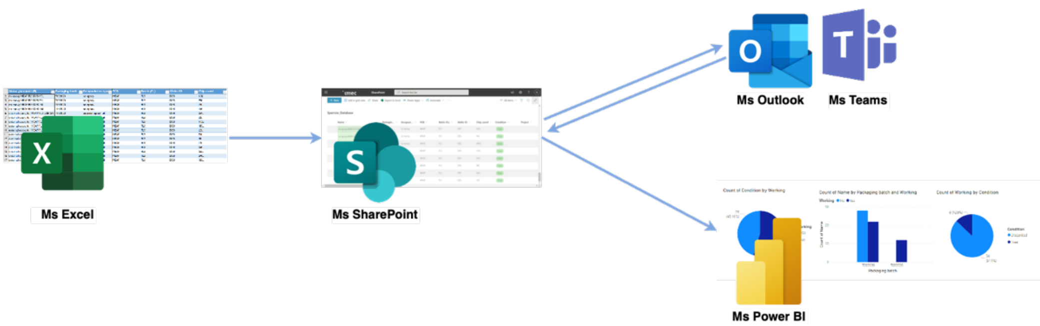


FIGURE 3.3: Communication process between the different Microsoft applications.

3.3 Results and discussion

3.3.1 Database structure

As previously introduced, this second part of the thesis represents the creation and development of a new Sparrow Database starting from already existing models.

For tracking the status ('free', 'in use', 'discarded') of all the chips, a simple Excel-SharePoint Database structure is used. It consists in: one Excel file, used to insert the generic information of the new chip batches into the main database, and two SharePoint lists which are the Sparrow_Database, containing all the information about the stored chips, and the User_Request, used to reserve specific chips for the different experiments. The workflow of the new developed Sparrow Database can be described in four main stages as shown in Figure 3.4.

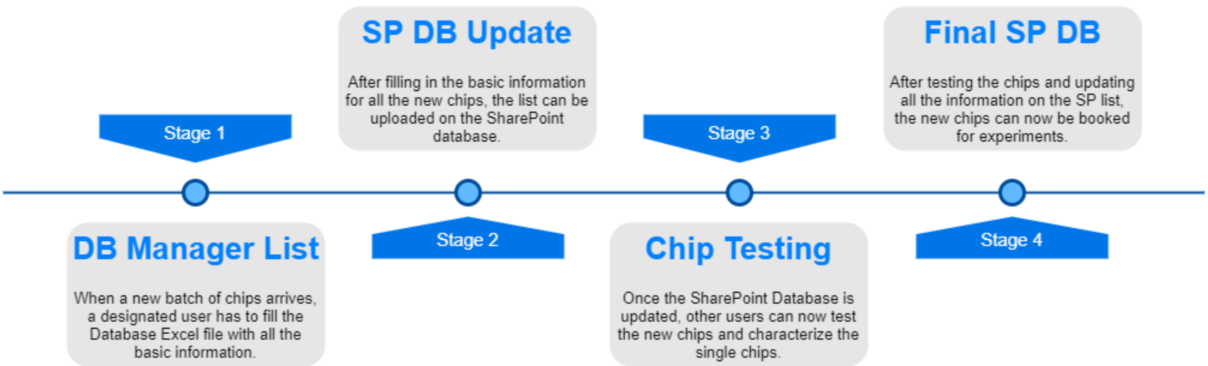


FIGURE 3.4: Sparrow Database workflow.

First Stage: To increase the speed of the whole database-filling process, when a new batch of chips arrives, before testing the chips one or more users are assigned to the role of 'Database Manager'. These designated users have to fill the DB Manager List Excel file (Figure 3.5) with all the generic information (*Packaging batch*, *Encapsulation type*, *PCB*, *Batch (FL)*, *Wafer ID* and *Chip coordinates* fields) for each new chip. While these first six fields are mandatory, the *Name*, *Condition* and *Project name* fields are not. The *Name* field is automatically generated after filling the six fields before, representing a unique code used to identify each single chip; at the same time, the *Condition* (which is automatically set as 'Free') and *Project name* fields are to be used only at DB Manager's discretion to reserve beforehand chips that have to be used in specific projects, and can't be booked by anyone else.

1	Name *(automatic fill)*	Packaging batch	Encapsulation type	PCB	Batch (FL)	Wafer ID	Chip coord
2	no epoxy MEAP FL3 D08 K3L	T032020	no epoxy	MEAP	FL3	D08	K3L
3	no epoxy MEAP FL3 D08 F5L	T032020	no epoxy	MEAP	FL3	D08	F5L
4	no epoxy MEAP FL3 D08 L5L	T032020	no epoxy	MEAP	FL3	D08	L5L
5	no epoxy MEAP FL3 D08 D6L	T032020	no epoxy	MEAP	FL3	D08	D6L
6	external epoxy full MEAP FL3 D08 G2L	T032020	external epoxy full	MEAP	FL3	D08	G2L
7	external epoxy full MEAP FL3 D08 J2L	T032020	external epoxy full	MEAP	FL3	D08	J2L
8	external epoxy full MEAP FL3 D08 M3L	T032020	external epoxy full	MEAP	FL3	D08	M3L
9	external epoxy full MEAP FL3 D08 H5L	T032020	external epoxy full	MEAP	FL3	D08	H5L
10	external epoxy full MEAP FL3 D08 L2L	T032020	external epoxy full	MEAP	FL3	D08	L2L
11	external epoxy full MEAP FL3 D08 E4L	T032020	external epoxy full	MEAP	FL3	D08	E4L
12	external epoxy full MEAP FL3 D08 I5L	T032020	external epoxy full	MEAP	FL3	D08	I5L
13	external epoxy full MEAP FL3 D08 L3L	T032020	external epoxy full	MEAP	FL3	D08	L3L
14	external epoxy full MEAP FL3 D08 G6L	T032020	external epoxy full	MEAP	FL3	D08	G6L
15	external epoxy full MEAP FL3 D08 G5L	T032020	external epoxy full	MEAP	FL3	D08	G5L
16	external epoxy full MEAP FL3 D08 D4L	T032020	external epoxy full	MEAP	FL3	D08	D4L
17	external epoxy full MEAP FL3 D08 H3L	T032020	external epoxy full	MEAP	FL3	D08	H3L

FIGURE 3.5: Picture of Dabatase Manager list used during our database development.

Second Stage: After filling the DB Manager List Excel file, the Database Manager uploads all the information contained inside this file into the SharePoint Sparrow_Database list, making it available to all the users (Figure 3.6). In case of mistakes, it is still possible to intervene and modify each single information, even the one set by the Database Manager.

imec SharePoint Search this list

+ New | Edit in grid view | Share | Export to Excel | Power Apps | Automate | ··· | All Items*

Sparrow_Database

Name	Packagin...	Encapsul...	PCB	Batch (FL)	Wafer ID	Chip coord	USER
no epoxy MEAP FL3 D08 E1	T092020	no epoxy	MEAP	FL3	D08	E1	Tommaso
no epoxy MEAP FL3 D04 L9L	T092020	no epoxy	MEAP	FL3	D04	L9L	Tommaso
no epoxy MEAP FL3 D03 L8L	T092020	no epoxy	MEAP	FL3	D03	L8L	Tommaso
no epoxy MEAP FL3 D03 J8L	T092020	no epoxy	MEAP	FL3	D03	J8L	Tommaso
no epoxy MEAP FL3 D04 F2L	T092020	no epoxy	MEAP	FL3	D04	F2L	Tommaso
no epoxy MEAP FL3 D08 I8L	T092020	no epoxy	MEAP	FL3	D08	I8L	Laurin
no epoxy MEAP FL3 D08 G7L	T092020	no epoxy	MEAP	FL3	D08	G7L	Laurin
no epoxy MEAP FL3 D08 C3L	T092020	no epoxy	MEAP	FL3	D08	C3L	Laurin
no epoxy MEAP FL3 D08 A6L	T092020	no epoxy	MEAP	FL3	D08	A6L	Laurin
no epoxy MEAP FL3 D08 A3L	T092020	no epoxy	MEAP	FL3	D08	A3L	Laurin

FIGURE 3.6: Picture of the SharePoint Sparrow_Database list.

Third Stage: Once the upload of all the information is done successfully, all the users can now test the chips of the new batch and fill the SharePoint Sparrow_Database list with the results. This information, apart from the nine fields added by the Database Manager, consists in: *Status*, which is automatically set as 'New' for each new chip and can be modified as 'Used', after the first experiment, or as 'Thrashed', if it is no longer working; *USER*, which is manually set by the person testing the chip; *Handover time*, which refers to the testing date, and is manually added by the user; *Packaging status*, which is automatically set as 'No' but can be switched to 'Yes' if the chip is manually packaged by the user; *Tested*, which is automatically set as 'No' but can be switched to 'Yes' after the chip is successfully tested by the user; *Working*, *Power up*, *Detected*, *Acquiring*, *Noise test*, *Z MOhm* (which measures the biggest impedance recorded) and *Stimulation working*, are all information manually added by the user during the testing of the chip.

In case of a missing chip, it is also possible for the normal users to insert the single chip information in the SharePoint Sparrow_Database list. However, in this case it is also necessary to fill all the fields that are normally filled by the Database Manager, with close attention to the *Name* field, which is no longer automatically generated but needs to be correctly put by the user.

Fourth Stage: After filling the Sparrow Database, all external users can now go to the Imec SharePoint site and reserve chips for specific experiments by sending a request through the SharePoint User_Request list (Figure 3.7). To send a booking request, the process is similar to adding a new single chip in the main Sparrow_Database list. In this case the user have to create a new item filling all the different lists: *Requester*, used to specify the name of the user that is going to use the chip; *Chip name*, used to select the chip, which is done with a lookup column referring to the *Name* field of the SharePoint Sparrow_Database list; *Experiment name*; *Starting* and *Ending date*, which is important that are valid; and *Approval*, which is automatically set as

‘Pending’ and should not be modified by the user. After the new item in User_Request is saved, a request is automatically sent by the database to the supervisors through Microsoft Outlook, who will decide whether approve or reject it, thus modifying respectively the Approval status as ‘Approved’ or ‘Rejected’ in the SharePoint User_Request list. If approved, this procedure will mark the chip as not available for the other users, without removing it from the chip booking list, while automatically changing the *Condition* field as ‘In use’ in the main SharePoint Sparrow_Database list for the period assigned in the *Starting-Ending date* fields.

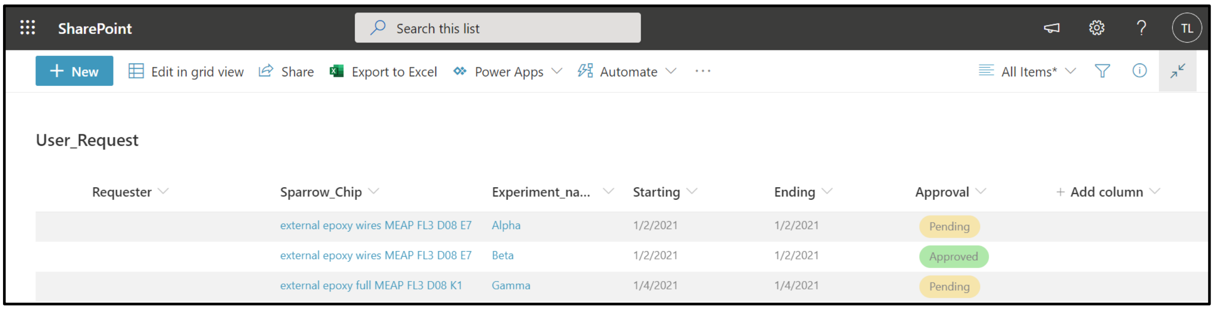


FIGURE 3.7: Picture of the SharePoint User_Request list.

3.3.2 Main workflows

To automate most of the procedure previously described and to keep the database always updated, we used Power Automate to develop and exploit two main SharePoint flows. Since most of the work and communication between different SharePoint lists can be easily made directly on the lists themselves, the two main flows are made specifically only for the approval of valid new requests and for the control of the expired ones.

Start approval when new valid request is created

This first SharePoint flow connects the user's request with the main Sparrow Database. After the correct automatic evaluation from the system, the request passes through the approval of a supervisor. This process consists of 4 stages (Figure 3.8):

- The flow is automatically triggered when a new item (valid or not) is created in the User_Request list.

- All the information filled by the user inside the User_Request new item are loaded into the flow, which is then analyzed.

- For each item of the User_Request list, first the *Chip name* is compared to the one from the new request (control chip name). If they match, then a second control takes place to evaluate if the comparison is taking place between the new request and itself, by controlling the *Chip name Id*. If they are not, a final check is performed to evaluate if the *Starting date* of the new request is after the *Ending date* of the already existing valid requests for the same chip, controlling if the two periods are overlapping. This last step allows the user to book a specific chip even if it is temporarily used in another experiment when the request is made (allowing the user to book it without the need of waiting it to be marked as 'Free'). If the two periods are instead overlapping, a mail is automatically sent to the requester explaining the problem and the request is automatically marked as 'Rejected'.

- If the request is not rejected in the step before, it is considered valid and a mail is sent to the supervisors for the approval. The supervisor can now reject or approve the request, in both cases a mail is sent back to the requester with the outcome (plus an optional comment from the supervisor) and the request is automatically marked as either ‘Rejected’ or ‘Approved’; in the second case, the status of the requested chip is also changed as ‘In use’ in the main Sparrow_Database list when the reserve period starts.

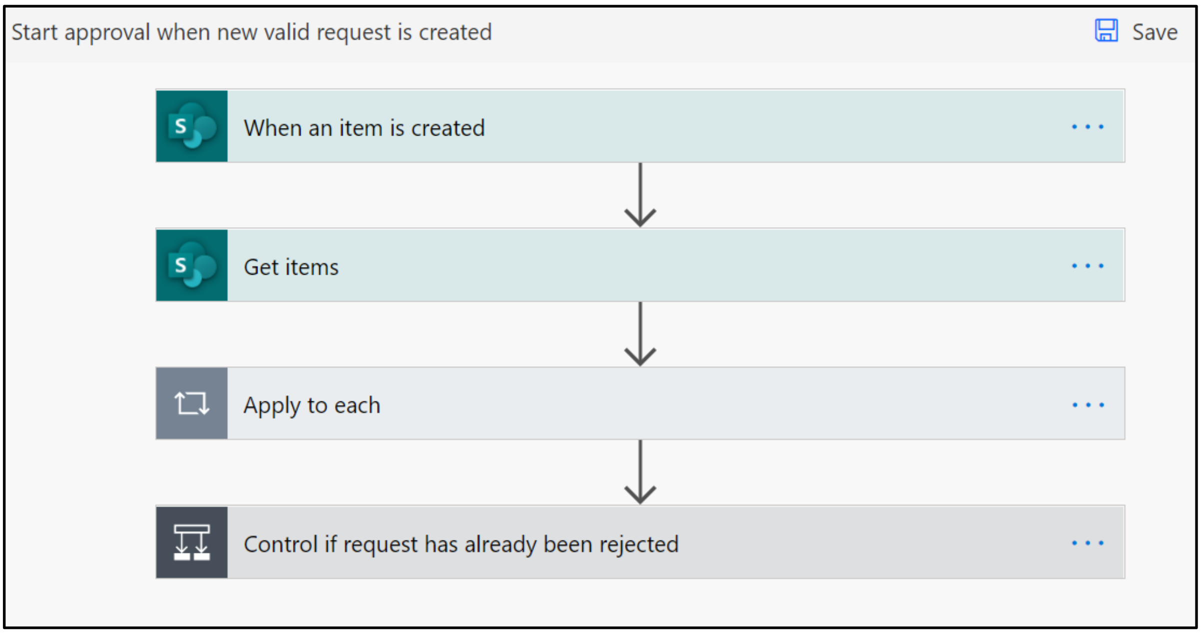


FIGURE 3.8: 4-stages Start-approval process.

The step-by-step of the full Start-approval workflow is shown in Figure 3.9.

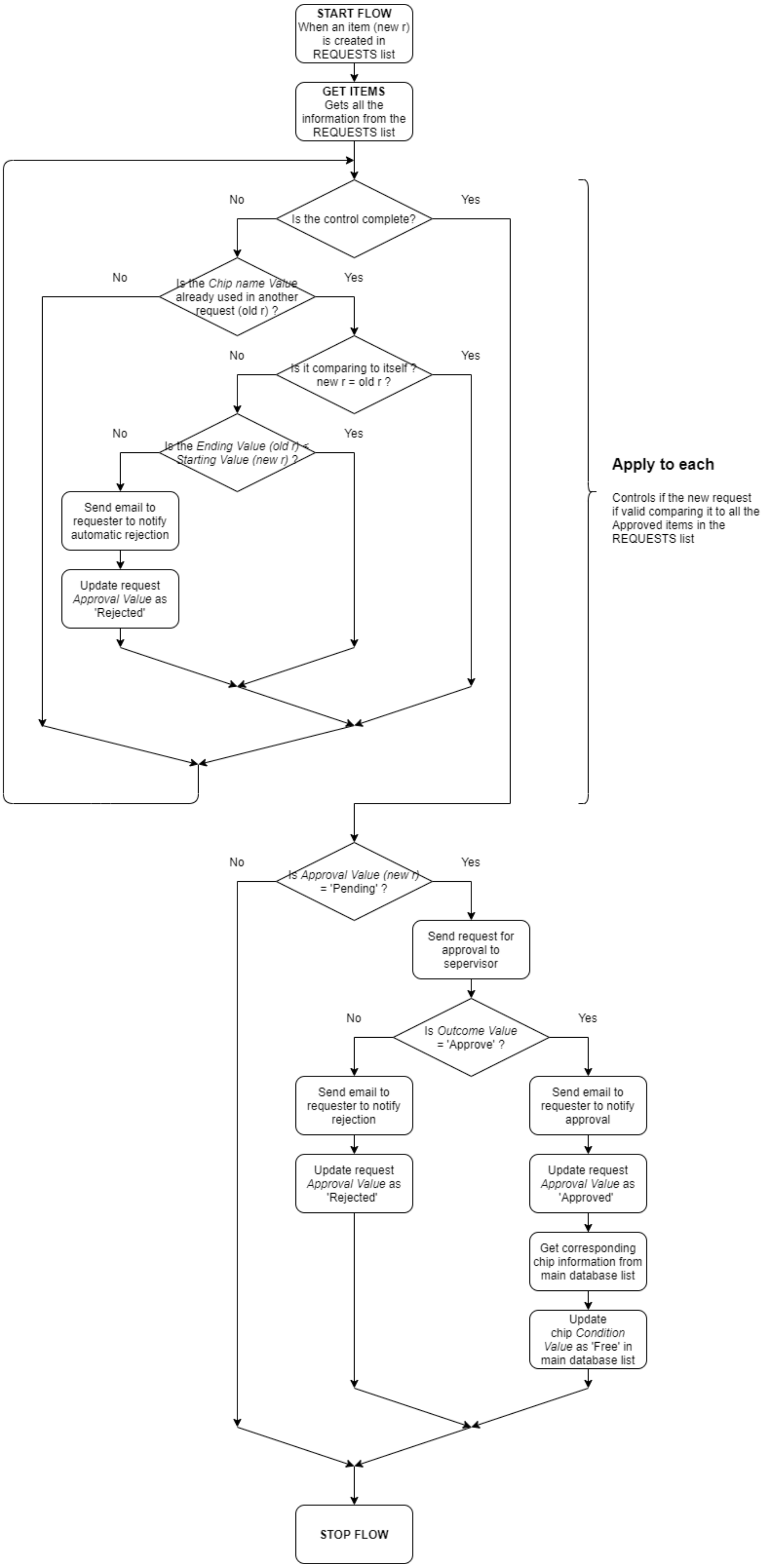


FIGURE 3.9: Complete workflow of the Start-approval process.

Timed control of expired requests

This second SharePoint flow periodically controls that old and non-valid requests are not considered, making sure that no longer booked chips are marked back as 'Free'. This process consists in 5 stages (Figure 3.10):

- The flow is set to be automatically triggered at a specific time every day, in this case 06:00 AM Central European Time (CET), which is set in the Recurrence block of the flow.

- After the flow starting, the current date/time is loaded into the flow.

- The SharePoint User_Request list is fully loaded into the flow.

- For each item of the request list, it compares the *Status* value considering only the previously 'Approved' requests. For each one of them, the *Ending date* of the request is compared with the current date/time obtained in the second step, if the *Ending date* is less than the current one it updates the *Status* value of the specific request to 'Expired', marking the corresponding chip in the main Sparrow_Database list as 'Free'.

- Each item of the User_Request list is controlled a second time, considering again only the 'Approved' requests. It then compares the current date with the *Starting date* and *Ending date* of every 'Approved' request, if the current date is in between those two, it marks the chip in the main Sparrow_Database list as 'In use'.

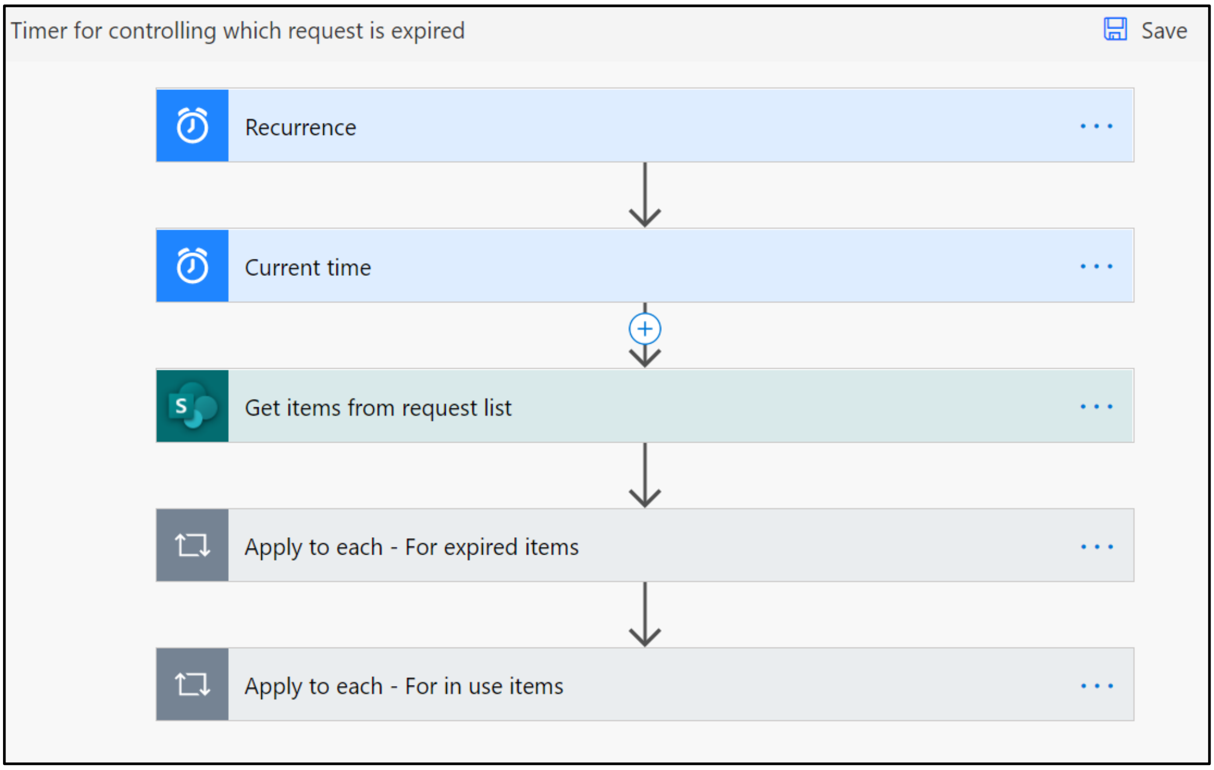


FIGURE 3.10: 5-stages Request timed-control process.

The step-by-step of the full Request timed-control workflow is shown in Figure 3.11.

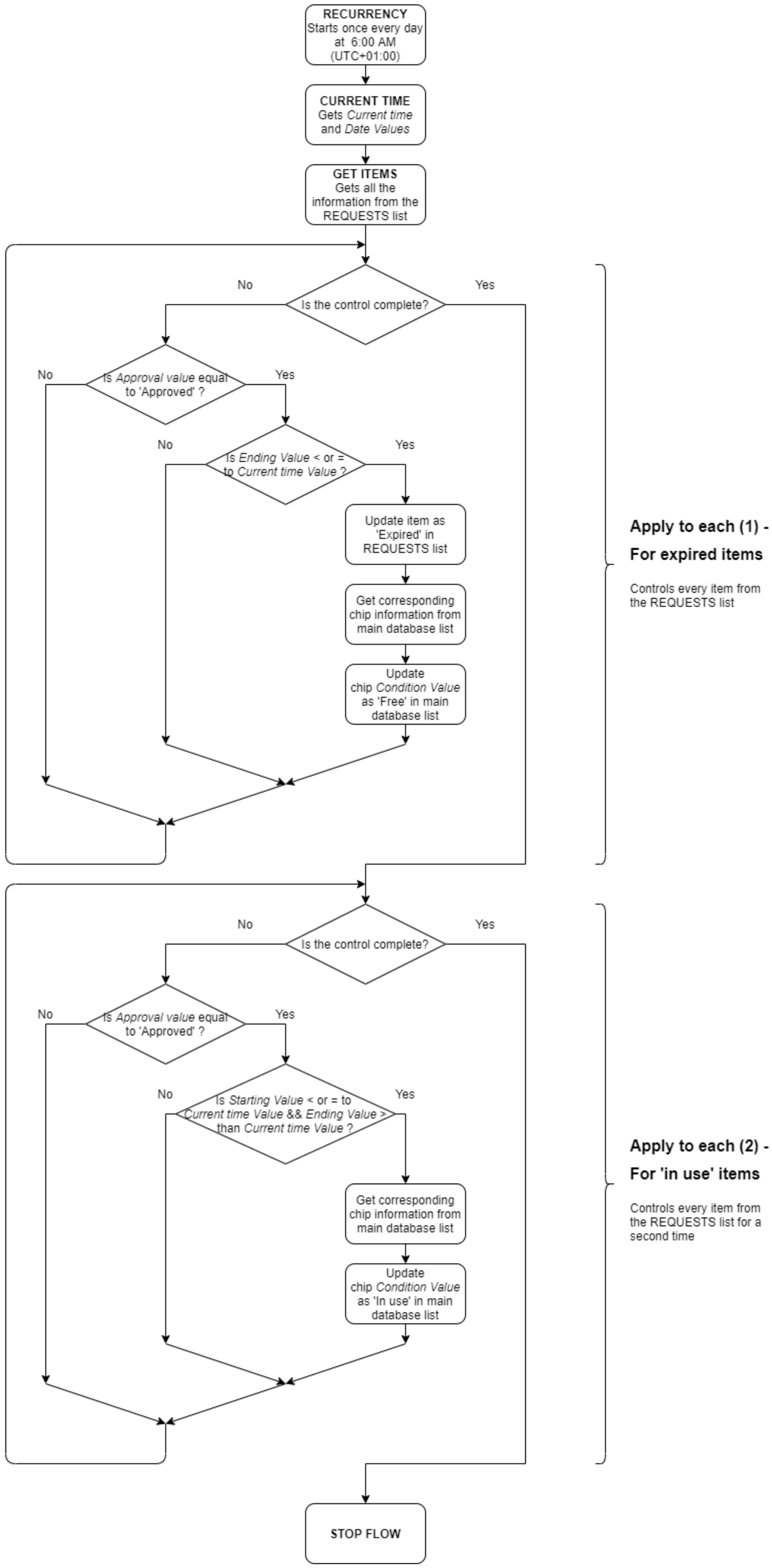


FIGURE 3.11: Complete workflow of the Request timed-control process.

Database graphic summary: Power BI

As the final step, once the main database is filled, all the information can be represented connecting the SharePoint list to a Microsoft Power BI (Figure 3.12) custom infographic slide. This connection allows the users to design a personal infographic page containing all the key elements to a better and faster comprehension of the chips situation in real-time.

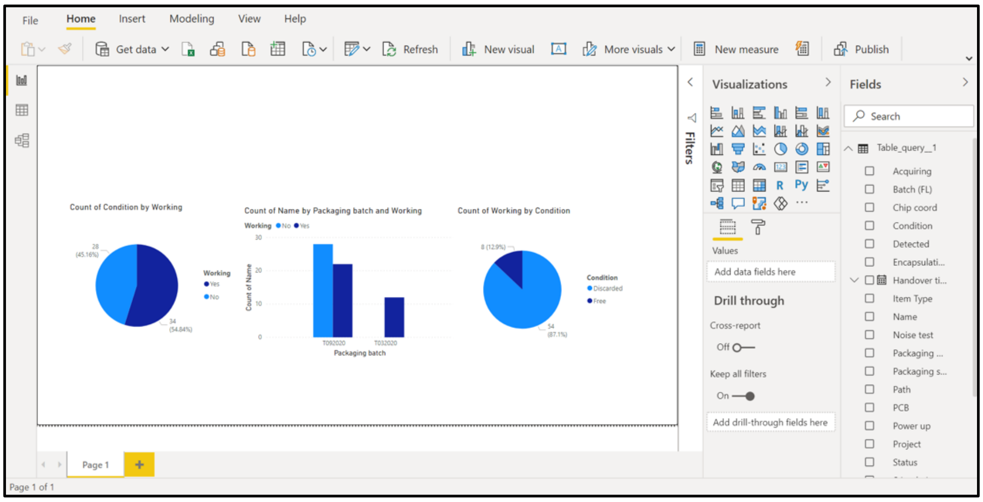


FIGURE 3.12: Picture of the Microsoft Power BI main developing page with 3 custom charts.

Although Ms SharePoint software hindered the database workflow programming due to its rigid structure, the obtained Sparrow Database was able to converge the pros of both the Ms Excel and Ms Access database versions. It resulted in a more rigid evaluation structure respect the Excel database solving all the long-term problems, allowing for a better classification similar to the Ms Access one. At the same time, it improved the user experience because of its simplicity, which is similar to the Excel file. Moreover, the division between the different exploited softwares and the split between their supervision helped reduce the work-load on the single users, improving the overall experience.

4. **Conclusions**

In this Master's Thesis, we exploited the chip testing to measure characteristics and yields of the different chip batches, with the September 2020 batch having a 34% output caused by a poorly wire-bonding, while the December 2020 batch is standing at a 80% output. Thus remarking how important the wire-bonding and the encapsulation processes are in the fabrication of a chip. Moreover, the chip testing also served as imaging asset, providing new insights for the correct programming of the chips every time the respective software is updated. Furthermore, it also helped to evaluate the effectiveness of the current normal chip testing process (Dry and Wet testing), showing how an automatic better imaging is possible with a confocal microscope, largely improving the quality of such evaluations.

In the second part, during the design and development of the database, we were able to achieve a middle-ground database between the Ms Access version, characterized by a strong professionalism component, and the Ms Excel version, which was instead more linear and intuitive. Thus improving the long-term stability and efficiency while making a more user-friendly interface, therefore reducing the time for catalog devices, improving the storage space and its consultation.

In conclusion, the work presented here should make an important contribution both for a better imaging asset development, essential for correct chip evaluations, and for a faster chip production and experimentation, smoothing the bureaucratic process by improving the overall team communication.

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