Trans-impedance Amplifier at cryogenic temperature for silicon quantum bits

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HOURIEZ Thomas
thomas.houriez@grenoble-inp.org

Supervisors:
Dr. Louis JANSEN Louis.jansen@cea.fr
M. Adrien Morel Adrien.morel@cea.fr

Master Nanotech Phelma, Grenoble Institute of Technology

CEA, IRIG, PHELIQS LaTEQs Team (Transport Electronique Quantique et Supraconductivité)

CEA, LETI, DACLE Group (Département Architecture Conception et Logiciels Embarqués)

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Abstract

This internship took place in the frame of a collaboration between the LATEQS (studying nano-systems at very low temperature) and the LETI (focused on the research in micro-nano electronics) dedicated to the development of a CMOS-based qubit technology for quantum computing.

This work was focused on the study of a Trans-impedance Amplifier (TIA) used to measure a current and to convert it into a voltage readable by standard electronics. Here, the TIA measures the output current of a silicon spin qubit in order to perform the read-out of the quantum state of the qubit. As the qubit operates at low cryogenic temperature ($\approx$ 100mK), the TIA was designed to operate at low temperature and low power consumption. Therefore, because the performances of the TIA reduces for decreasing temperatures, the possibility was investigated to compensate this reduction by applying a back-gate voltage to the transistors when the transistors are implemented in the Fully Depleted Silicon-On-Insulator (FDSOI).

Both simulations and experimental characterization of single MOS transistors identified the increase of the threshold voltage and the decrease of the Sub-threshold Slope to be the main effect of decreasing the temperature (from 300K to 77K) on the MOS characteristics. It was also shown that implementing the transistors on the FDSOI technology allows to compensate the increase of the threshold voltage by applying a positive back-gate voltage.

The characterization of the TIA focused on the bandwidth (limiting the maximum speed at which the current measurements can be performed), the power consumption, and the noise. According to simulations, increasing the back-gate voltage from 0 to +4V at low temperatures does not change the bandwidth but leads to a reduction of the minimal operating power of 69%. At 77K, experiments demonstrated a lower reduction of the minimal power consumption of 35% and a reduction of the noise of 30% when increasing the back-gate voltage from 0 to +4V.

The interest of using the back-gate voltage to improve the performance of the TIA at low temperature was confirmed concerning power consumption and noise. Further studies should be extended down to the temperature of 4.2K or even lower, which is closer to the operating temperature of the qubit core.

Résumé:

Ce Projet de Fin d'Etude a été effectué dans le cadre d'une colaboration entre le LATEQS (étudiant les nano-systèmes a très basses températures) et le LETI (dédié à la recherche en micro et nanoélectronique) dans le but de développer des qubit basés sur une technologie CMOS classique pour le calcul quantique.

Ce travail se concentre sur l'étude d'un Amplificateur Trans-Impédance (TIA) utilisé pour mesurer un courant et le convertir en une tension détectable par un circuit électronique classique. Ici, le TIA mesure le courant de sortie d'un qubit de spin, ce qui permet d'éffectuer la lecture de l'état quantique du qubit. Le qubit de spin ne fonctionnant qu'à très basse température ($\approx$ 100mK), il es établit que le TIA doit fonctionner aux basses températures et à basse consommation d'énergie. La diminution des performances du TIA en réduisant la température est donc étudiée. La possibilité de compenser cette diminution en appliquant une tension sur la back-gate lorsque la technologie FDSOI est utilisée est aussi étudiée.

Les simulations ainsi que la caractérisation expérimentale d'un transistor MOS seul ont identifié l'augmentation de la tension de seuil et la diminution de la sub-threshold slope comme étant les effets principaux d'une diminution de la température de 300K à 77K. Il est aussi montré que lorsque la technologie FDSOI est utilisée pour implémenter les transistors, l'application d'une tension positive sur la back-gate permet de compenser l'augmentation de la tension de seuil.

La caractérisation du TIA est concentré sur la bande passante (limitant la vitesse maximale à laquelle peuvent être effectué les mesures de courant), la puissance de fonctionnement minimale, et le bruit. D'après les simulations, augmenter la tension de back-gate de 0 à +4V à basse température ne créer aucune augmentation de la bande passante et se traduit par une réduction de la puissance de fonctionnement minimale de 69%. A 77K, les résultats expérimentaux démontrent une réduction plus faible de la puissance minimale de 35 % et une réduction du bruit d'environ 30% quand la tension de back-gate est augmentée de 0 à +4V.

L'intérêt d'utiliser la tension de back-gate pour améliorer les performances du TIA aux basses températures est confirmé pour la consommation d'énergie et le bruit. Dans de futures recherches, il serait intéressant d'étudier de l'influence de la tension de back-gate à la température de 4K, plus proche de la température d'opération des qubits.

Introduction

A quantum computer relies on the quantum mechanical phenomena of superposition and entanglement to perform calculations, allowing the implementation of quantum algorithms, which are in some cases much more powerful than any classical algorithm. This could be of great interest for efficient problem solving in cryptography, data searching, and also quantum mechanical simulations (Feynman(1981), [1]).

Currently, many challenges remain to meet the requirements defined by the physicist D. Di Vincenzo in 2000 [2] necessary to build a quantum computer. The fundamental challenges involve the initialization, manipulation and reading of the quantum bit within a long enough coherence time of the quantum state. In addition, the state of a qubit presents a low stability due to its quantum nature, and the implementation of error correction algorithms using multiple qubits is needed in order to achieve an acceptable error level. Therefore, up-scaling the number of qubits is also crucial and the development of classical electronics capable of controlling a large number of qubits is necessary in order to realize a quantum computer.

Among the different ways to physically implement qubits, the spin of an electron trapped inside a quantum dot (fabricated on a classical Si wafer) has been demonstrated to be a promising candidate [3], [4], [5]. These semiconductor qubits have an acceptable fidelity and speed. Moreover, this technology benefits from the long experience of the semiconductor industry to obtain reliable up-scaling in the number of qubits occupying a very small footprint (10^8 qubit/mm^2). Nonetheless, these qubit structures only present quantum behavior at very low cryogenic temperature (0.1 - 1K).

When controlling the cryogenic qubit with room temperature electronics, heat diffusion from room temperature towards the low temperature qubit chip must be avoided. This implies that wires connecting the control electronics to the qubits must be long enough, which limits the speed of the signal from control electronics to qubits. The maximum number of wires is also limited (especially if carrying an AC signal), limiting parallelism.

To allow a higher number of connections between control electronics and qubits without loss in data transfer speed, a viable approach is to place the control electronics close to the qubit architecture at low temperatures. It is therefore necessary to develop circuits able to operate at cryogenic temperatures (4.2K or below) consuming sufficiently low-power to avoid self-heating effect.

This work will study the performance of a trans-impedance amplifier (TIA) at cryogenic temperatures. A TIA is suitable to measure the current through a high impedance device and converts it to a voltage readable by standard electronics. In the context of qubit research, it can be used to read the state of a quantum dot of a CMOS spin qubit by measuring its output current. Previous work (mostly on digital circuits) has shown that the performance of circuits is modified when operating at cryogenic temperature. As an example, the maximum frequency of ring oscillators is reduced at low temperature [6]. This is mostly due to an increase of the threshold voltage of CMOS transistors with decreasing temperature. Therefore, this work will be focused on the interest of using the back-gate of the MOSFET to compensate the effect of cryogenic temperature on the front gate, in order to improve the performance of the TIA with respect to bandwidth, power consumption and noise.

First, the main characteristics of the Fully Depleted Silicon-On-Insulator (FDSOI) technology used for the TIA fabrication is introduced. Then, the influence of the back-gate on single MOS transistors characteristics is presented. Finally, the evolution of the performance of the TIA with the back-gate, is studied, both in simulations and in measurements.

Chapter 1

Interest and challenges of cryo-CMOS technology

1.1 Si spin qubit

1.1.1 Implementation of a qubit

A quantum bit is a two-state quantum system, where the basis states are noted $|0>$ and $|1>$. On the contrary to classical bit, a qubit can be in a coherent superposition of these two states, described by the linear combination $|\psi> = \alpha\ |0> + \beta\ |1>$. Here, $\alpha, \beta \in \mathbf{C}^2$ are related to the probabilities $|\alpha|^2$ and $|\beta|^2$ to find the qubit in the state 0 and 1, so that $|\alpha|^2 + |\beta|^2 = 1$. The probability to find the qubit in a given state can vary continuously between $|0>$ and $|1>$, giving the qubit state an analog aspect.

The state of a qubit can also be represented by the Bloch sphere presented in figure 1.1, where the surface of the sphere is a 2D representation of all the possible states of the quantum system given by the complex coefficients α and β. The Bloch sphere uses a polar coordinate system: the basis states are conventionally represented on opposite directions of the vertical axis, while θ represents the orientation towards $|0>$ from $|1>$ state and ϕ represents the phase difference between the two states.

A system of n classical bits has 2^N different states and can only be in one state at a time when it is measured, so that computations are performed successively on a classical computer. On the contrary, qubits can be in a coherent superposition of these 2^N states, meaning that calculations for different states can be performed at the same time. This allows parallelism to a scale not conceivable using a classical computer.

The implementation of a qubit can be achieved by different physical quantum systems:

- Trapped ions: qubits are stored in the electronic state of an ion. The ion is spatially confined in the potential trap of an electromagnetic field, which isolates it from external perturbations. The quantum information is represented by the quantized motion of ions sharing a trap. This technology presents a very high fidelity and is the most advanced in term of quantum gate implementation, making it promising for a universal quantum computer. The main concern is scalability, since trapped ions occupy a very large area (1 mm^2).

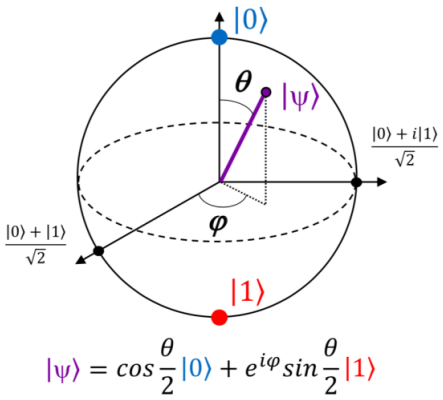

Figure 1.1: Bloch sphere representation of all the possible states occupied by a qubit

- Superconducting qubit: when placed at cryogenic temperatures, some metals (aluminium, niobium or rhenium) exhibit superconducting properties, where all free electrons condense into the same quantum energy level at a macroscopic lengthscale. The qubits can therefore be manipulated by tuning their classical parameters (capacitance, inductance) [7]. Google recently demonstrated the operation of a 53 qubits array to implement a quantum algorithm.
- Semiconductor qubits: this implementation can use the leverage of the progress made in the classical semiconductor industry in term of miniaturization and fabrication process in order to achieve the up-scaling of the number of qubits. The qubits are represented by the spin of an isolated electron, and the semiconductor spin qubit can be fabricated on quantum dot structures on materials like GaAs [8] or Si [5]. Recent works demonstrated high fidelity of the quantum state for a single qubit, and the operation of a CNOT quantum gate on two qubits [9].

In the following, the principle of the semiconductor spin qubit as developed at the CEA-LATEQS in close collaboration with the CEA-LETI will be presented.

For the semiconductor qubits, the spin of a single electron, which can be in two states noted $|\uparrow>$ and $|\downarrow>$, is used to represent the state of the qubit. The first plat-form used for semiconductor spin-qubit was GaAs. Nonetheless, the non-zero nuclear spin of this material interacts with the spin of electrons, thus greatly limiting the coherence time of quantum states. Now, isotopically purified Silicon-28, exhibiting zero nuclear spin, has been developed and achieves much longer coherence time, thereby increasing the time during which the qubit can be manipulated.

Using the spin of an electron to represent a qubit requires to isolate a single electron, this can be achieved in a single electron transistor (SET). A SET is similar to a classical transistor, except that tunneling barriers exist between the drain and source regions and the channel. In addition, the channel is small enough to exhibit quantization of states, creating a quantum dot in the channel (cf. fig 1.2). In this case, when the appropriate voltage is applied on the gate, an energy level E_n of the channel is aligned with the Fermi levels of source and drain, and an electron can tunnel across the channel. Due to the repulsive Coulomb interaction existing between electrons, the presence of one electron increases the electrostatic energy of that level, preventing other electrons from tunneling through the barrier, so that electrons can only be

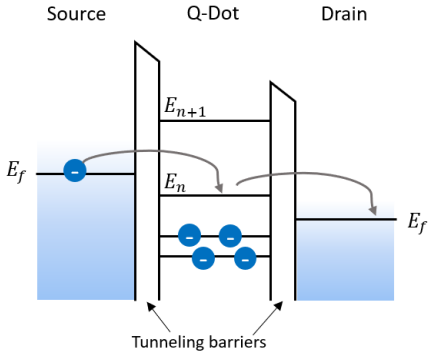

Figure 1.2: Band diagram of a Single Electron Transistor (SET), consisting of a quantum dot connected via tunneling barriers to source and drain contacts.

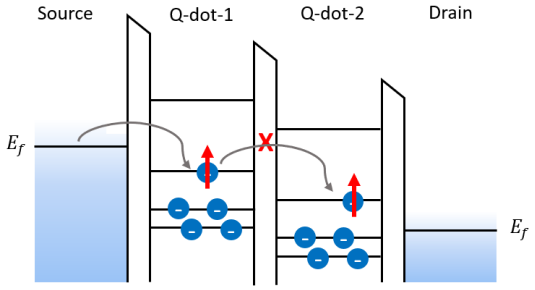

Figure 1.3: Band diagram of a double quantum dot structure implementing a spin qubit.

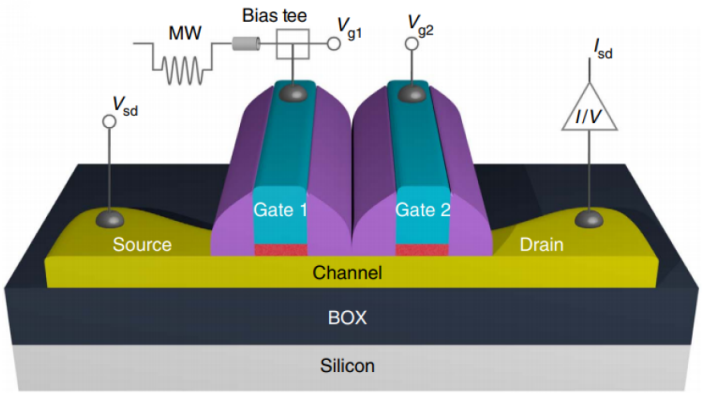

Figure 1.4: Simplified schematic of a double gate structure fabricated on CMOS technology. Adapted from Maurand(2016), [5].

transferred one by one across the channel. This is the so-called Coulomb blockade regime.

The spin of the electron containing the qubit state can be determined using a double gate architecture (cf. fig 1.3 and fig 1.4), where two quantum dots (each controlled by an individual gate) are placed next to each other in the channel. One electron is placed in each quantum dot, the first contains the qubit state while the second is kept in the down state and serves as a reference. Two spin states are then involved in the read-out process. In the anti-parallel state $|\uparrow\downarrow>$, the two electrons can be located in the same dot, forming a singlet. In the parallel state $|\downarrow\downarrow>$, the two electrons cannot occupy the same dot due to the Pauli exclusion principle, they form a triplet. The difference of energy between singlet and triplet permits to distinguish the two configuration. Performing a current measurement across the two quantum dots permits to determine the spin state of the qubits.

1.1.2 Control electronics of the qubit core

In order to operate a qubit, it is necessary to be able to initialize, manipulate and read its quantum state. The control electronics must be able to perform all these steps without disturbing the state of the qubit.
The usual method for controlling the qubit at cryogenic temperature is to place the control electronic at room temperature (cf fig 1.5.a). In this case, the diffusion of thermal energy from control electronics towards the quantum system must be limited in order to avoid heating up the qubits with destruction of the quantum coherent state. This means that long cables (of the order of 1 m) with relatively high resistance must be used to make the connection, imposing a large cable capacitance. This implies a long delay for a signal to travel along the cable, limiting the minimal time to complete a full cycle from initialization to read-out. In addition, the limit on heat diffusion also puts a boundary on the maximal number of wires carrying an AC signal, which will become a problem if a high number of qubit needs to be operated at the same time.

To avoid these limitations, the control electronics can be placed much closer to the temperature of the qubit core (cf fig 1.5.b). This allows shorter connections between control electronics and qubits (of the order of 1cm), reducing the wire capacitance and thus the delay through the wire. As the heat transfer is also reduced when the circuit is placed at 4.2K, the number of connections can also be increased, which allows more parallelism during the control of multiple qubits.

As the Si-spin qubits uses the same technology as the classical CMOS electronics, it is in principle possible to place the control electronics and the qubits on the same chip, pushing further the improvements just discussed (cf fig 1.5.c). Nonetheless, the technologies for qubits and control electronics require different constraints for the fabrication process, and this co-integration has not yet been demonstrated.

The advantage of placing the control electronic circuit at cryogenic temperature (4.2K and below) was discussed in terms of delay and number of connection between the control electronics and the quantum core. The power consumed by a circuit also results in self-heating. This implies that if the circuit consumes more than the cooling capacity of the cryostat, the temperature needed could not be achieved. Therefore, these circuits also need to operate at low power.

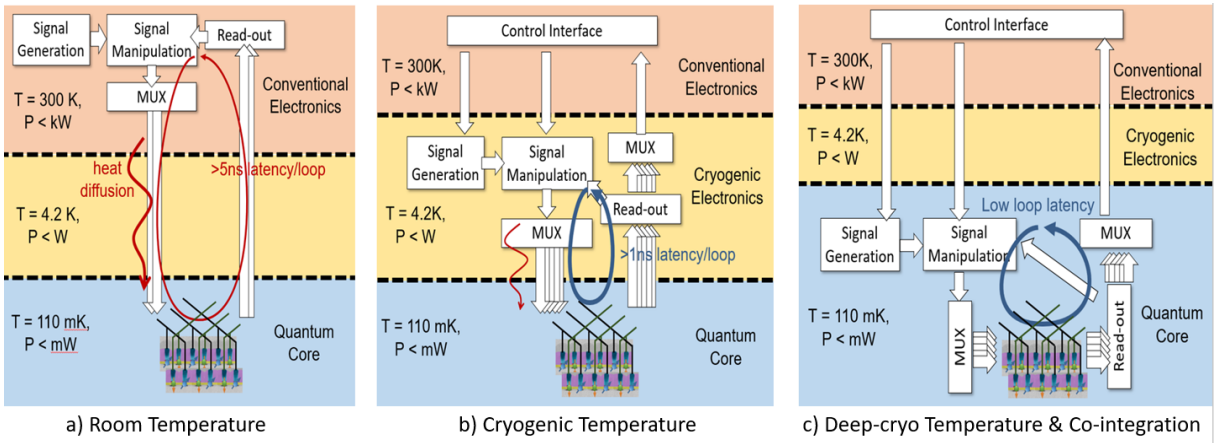

Figure 1.5: Summary of the solutions for the implementation of the control electronics at different temperature stage.

1.2 MOS characteristics at cryogenic temperature

In this section, the main consequences of cryogenic temperature on MOS transistor characteristics are presented. As will be shown in the following, the influence of cryogenic temperature on parameters like threshold voltage is problematic for the design of circuits when using a classical Bulk-CMOS technology.

1.2.1 Threshold voltage

One of the main effects of cryogenic temperature on MOSFETs is the increase of the threshold voltage.

Considering the case of a MOS junction made of p-doped Si, V_{gb} is defined as the voltage between the metal Gate and the p-Si Bulk. For this junction, the majority carriers are holes and are present in the channel close to the oxide interface. When no voltage is applied across the junction(V_{gb} = 0V), the hole concentration is higher than the doping density N_a, this is called the accumulation regime. When increasing V_{gb}, the hole concentration will decrease until it becomes lower than N_a, which is called the depletion regime. Continuing to increase V_{gb}, minority carriers will start to appear in the channel, and the inversion regime is reached when their concentration in higher than the concentration of majority carriers. In the inversion regime, the threshold voltage V_{th} is defined as the gate voltage V_{gb} necessary to obtain a minority carrier concentration $n(0) > N_a$, so that the conducting channel is occupied by enough electrons to obtain a significant current from source to drain when $V_{gb} > V_{th}$.

For the classical MOSFET technology, the threshold voltage can be calculated using the simple expression:

$$V_{th} = \phi_{MS} + 2\phi_F + \frac{Q_{dep}}{C_{ox}} \tag{1.1}$$

Where:

- $\phi_{MS} = \phi_M - \phi_S$ is the difference between the work function of the metal gate and the semiconductor.
- $\phi_F = k_B T/q \; ln(N_a/n_i)$ is the electro-chemical potential, where N_a is the doping density of the substrate and $n_i = 3,9.10^{16}.T^{3/2}.e^{-E_g/(2k_BT)}$ is the density of electrons in undoped silicon. ϕ_F therefore depends on the doping level and on the temperature.
- $Q_{dep} = \sqrt{4\epsilon_s q N_a \phi_F}$ is the charge in the depletion region and C_{ox} is the gate-oxide capacitance per unit area, such that Q_{dep}/C_{ox} is the voltage created by depletion charges.

The dominant parameter in the dependence of V_{th} on temperature is the intrinsic density of electrons n_i. From the equation 1.1, it can be calculated that V_{th} decreases when temperature increases. Therefore, when going from room temperature down to cryogenic temperature, V_{th} will increase. This is illustrated in figure 1.6, which shows the $I_d - V_g$ curve of a NMOS transistor at T = 300K and T = 4.2K

Previous experiments confirmed the increase of V_{th} when decreasing temperature. Fig 1.7 shows the evolution of the threshold voltage of a short-channel Low Voltage Threshold (LVT)

NMOS. An approximately linear relation between V_{th} and T is observed from T = 300K to T = 100K. At lower temperatures, the increase of V_{th} slows down and the maximum V_{th} shift obtained at T ≈ 0K is about 160mV.

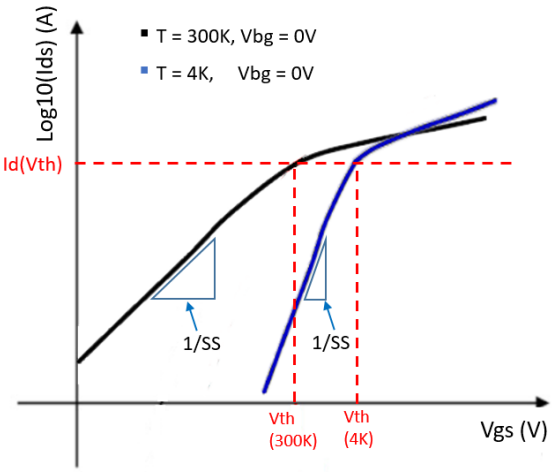

Figure 1.6: Comparison of the $I_d - V_{gs}$ characteristics of a MOSFET at room temperature (300K) and cryogenic temperature (4K). With decreasing temperature, the V_{th} increases and the Sub-threshold slope (SS) decreases.

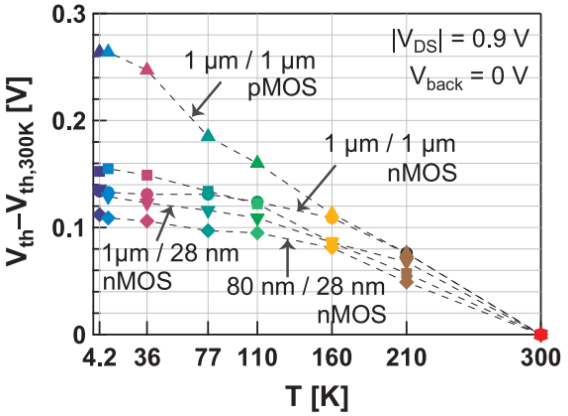

Figure 1.7: Evolution of the V_{th} shift with respect to room temperature $\Delta V_{th} = V_{th}(T) - V_{th}(300K)$ for different channel width and length in the saturation regime. Adapted from Beckers(2019), [10].

The equation 1.1 is only valid for Bulk MOS transistor, whereas in the case of Silicon-On-Insulator technology, the body effect, which is to say the shift of threshold voltage when changing the voltage V_{sb} between back-gate and Source is much larger and must be taken into account. This is detailed later in section 1.3.

1.2.2 Sub-threshold slope (SS)

A MOS transistor is said to operate in the Sub-threshold regime (also called Weak Inversion) when $V_{gs} < V_{th}$. As previously explained, V_{th} is the voltage at which the concentration of minority carriers becomes higher than the doping density N_a, meaning that the current I_d flowing through the conductive channel formed increases strongly. In the sub-threshold regime, a few electrons can still cross the channel, mostly thanks to a thermally activated diffusion process. The small drain current created by these electrons presents an exponential relationship with the gate voltage V_{gs}. The 'speed' at which the current I_d decreases when decreasing V_{gs} below V_{th} can be characterized by the Sub-threshold slope (SS), defined as $SS = \frac{\partial V_{gs}}{\partial log_{10}(I_d)}$. The $I_d - V_{gs}$ curve of a MOSFET and its corresponding SS is represented in fig 1.6. The value of SS can be expressed as:

$$SS = \underbrace{(1 + \frac{C_{dep}}{C_{ox}})}_{m} . \underbrace{ln(10)\frac{k_B.T}{q}}_{n} \tag{1.2}$$

In equation 1.2, the factor n is proportional to the temperature via the k_BT/q factor and is therefore responsible for the temperature dependence of SS. The pre-factor m is the electrostatic efficiency and depends on the electrostatic properties of the MOSFET. In the ideal case,

the capacitance C_{dep} created by the depletion region can be neglected. This gives a theoretical minimum of $m = 1$, which can be closely approached in modern MOSFET technology. Considering the ideal case (m=1), at room temperature (T = 300K), the minimal value of SS achievable is 60mV/dec. This value can be greatly reduced when reducing the temperature, reaching a theoretical value of SS below 1mV/dec at T = 4.2K.

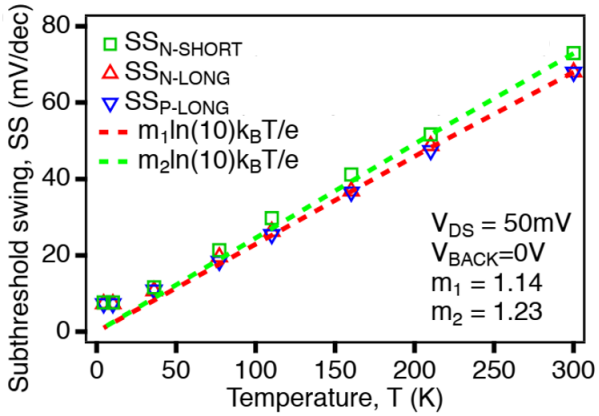

Figure 1.8: Value of SS measured at $I_d = 10^{-11}$A for n-type and p-type long-channel (N/P-LONG) and n-type short-channel (N-SHORT) transistors. Dashed lines stand for the linear temperature dependence from equation 1.2 with values of m equal to 1,14 and 1,23. Adapted from Bohuslavskyi (2017) [11]

The result of previous experiments carried at LATEQS is shown in figure 1.8. From the graph, it can be concluded that the SS is greatly improved at cryogenic temperature, as predicted by the theory. The linear dependence of SS with respect to T predicted by equation 1.2 is observed for T > 40K. Nonetheless, for T < 40K, the SS starts to saturate and reaches a value of around 7mV/dec at T = 10K. According to [11], this can be explained by the band tail broadening probed at low temperature and limiting the value of SS.

The benefit of the SS reduction seems clear for digital circuits as it means that the same I_{on}/I_{off} ratio can be obtained for a smaller variation of V_{gs}. The voltage supply VDD could therefore be down-scaled, reducing the power consumption of the circuit. The benefit is nonetheless not obvious for analog circuits, as most of them are designed to operate in the strong or moderate inversion regime.

1.2.3 Mobility

The mobility is one of the key parameters of a MOSFET characterising the transport of charge carriers in the channel. It is defined as the proportionality factor which relates the velocity of the carriers to the electric field applied between drain and source. The source-drain current I_d for an applied voltage V_{ds} can be expressed as:

$$I_d = \frac{W}{L}\mu_{eff}N_{inv}eV_{ds} \tag{1.3}$$

where μ_{eff} is the effective mobility, N_{inv} is the two dimensional inversion charge carrier density, and e is the charge of an electron. W and L are the channel width and length. At moderate transverse electric field (low V_{ds}), the mobility remains approximately constant, so that a linear

dependence of I_d as a function of V_{ds} can be assumed. At high electric field, the velocity tends to saturate, inducing a reduction of μ_{eff} at high V_{ds}. A dependence of μ_{eff} on N_{inv} can also be observed.

Physically, μ_{eff} depends on many different sources of scattering opposing the movement of carriers in the channel. Three main scattering mechanisms can be distinguished:

- Phonon Scattering (PS): at finite temperature, acoustic (low frequency) and optical (high frequency) phonons are present in the channel and interact with the charge carriers.
- Coulomb Scattering (CS): due to impurities, dopants and surface states at the Si/SiO2 interface, static charges can be found in the channel. These charges interact with the charge carriers through Coulomb interaction.
- Surface Roughness (SR): for a classical bulk Si technology, the conductive channel created under the gate is formed just under the Si/Oxide interface. This interface contains some defects, modifying the band structure of Si close to the oxide interface and in turn the mobility. Additionally, for the FDSOI technology, a second interface exists between the thin Si layer carrying the current and the buried oxide (BOX). The density of defects at the back-gate interface is generally lower than at the front-gate interface.

For FDSOI transistors, the additional mechanisms of Remote Coulomb Scattering (RCS) and Soft optical Phonon Scattering (SPS) , resulting from the presence of a thin layer of HfO2 in the gate stack, also have an influence on the mobility.

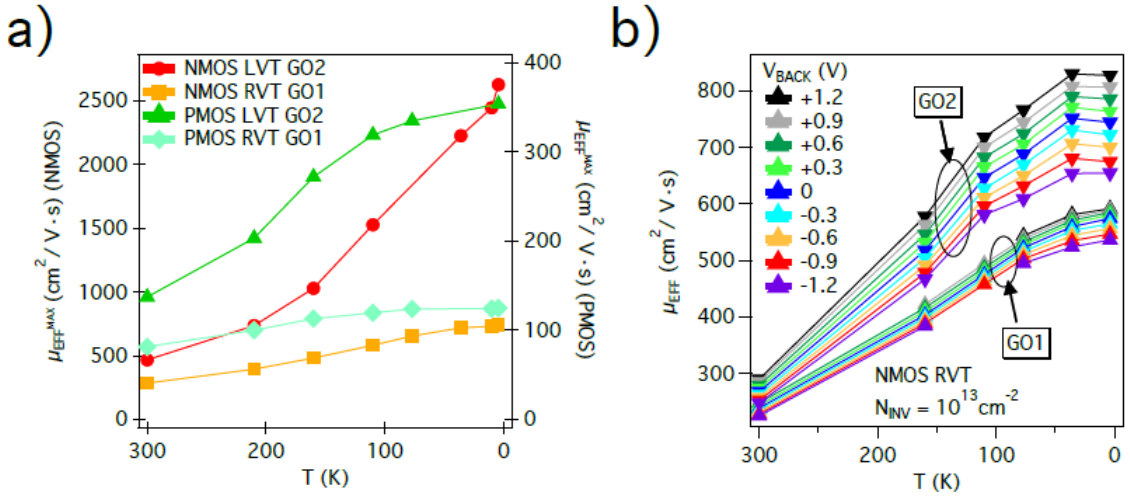

Figure 1.9: a) Evolution of the maximal mobility μ_{eff}^{max} with temperature from 300K to 4K for RVT (Regular Voltage Threshold) and LVT (Low Voltage Threshold) NMOS and PMOS devices (W=1μm, L=1μm). b) Evolution of μ_{eff} with back-gate voltage V_{bn} for NMOS RVT for thin (GO1) and thick (GO2) gate oxide thickness. From Bohuslavski(2019) [12]

The evolution of the mobility with temperature and back-gate voltage has been previously studied experimentally for 28nm FDSOI transistors [10]. Some of the results are presented in figure 1.9 a and b for large channel NMOS and PMOS (W=1μm, L=1μm) with thin (GO1) and thick (GO2) Equivalent Oxide Thickness.

Most of the temperature dependence of mobility originates from Phonon Scattering (PS).

The phonon density decreases with decreasing temperature, thereby increasing the mobility. Coulomb Scattering (CS) is predicted to become stronger at low temperature, while Surface Roughness (SR) doesn't depend on temperature. As can be seen in figure 1.9.a, the resulting effective mobility increases with decreasing temperature, for both NMOS and PMOS. For the thin gate oxide (GO1) devices used in the TIA layout, the influence of temperature on μ_{eff} is weaker.

The figure 1.9.b shows the dependence of the mobility with respect to the back-gate voltage V_{bn} for NMOS devices. μ_{eff} increases when an increasing V_{bn} is applied, as shown for all temperatures between T=300 and 4K. The positive voltage applied to V_{bn} attracts the electrons to the back-gate in turn moving the conductive channel from the front Si/oxide interface to the back interface. As the density of defects is lower at the back interface, SR is reduced, resulting in an increased mobility at positive V_{bg}. The effect of V_{bn} on μ_{eff} is weaker for the GO1 device.

1.2.4 Kink effect and sub-threshold fluctuations

Kink effect

The Kink effect designates an excess drain current visible in the saturation regime of a MOSFET . It arises from the threshold voltage shift due to the forward biasing of the source-substrate diode. This effect is usually observed in Partially Depleted SOI, due to the presence of a Si layer between the channel and the buried oxide, called the floating body. Impact ionization created by the current I_d flowing from the drain to the source generates charge carriers which are stored in this floating body. This creates a parasitic substrate potential V_b, which translates in an increase of I_d due to the body transconductance $g_b = \frac{C_{dep}}{C_{ox}} g_m$. The Kink effect in $I_d(V_{gs})$ is observed in Bulk MOS operating at low temperatures and in SOI MOS from room to low temperatures [13]. Thank to the absence of a floating body for the Fully Depleted SOI, no Kink effect is observed at room temperature [14]. In short-channel devices, the very efficient gate coupling as well as the proximity of the carriers to the source or drain also helps reducing the Kink effect.

Sub-threshold fluctuations

Sub-threshold oscillations characterize the anomalies in the $I_d(V_{gs})$ curve in the Sub-threshold regime at temperatures below 100K, and cause a large increase of the variability of the Sub-threshold current. They are attributed to the presence of dopants diffused from source and drain into the channel, and are less important for devices with less diffusion of dopants into the channel, although further research need to be done to confirm this hypothesis [10]. Resonant electron/hole tunneling occurs due to the defect electronic states created by the dopants in the channel. As shown in [15], sub-threshold fluctuations increase the sub-threshold current variability by several orders of magnitude.

1.3 Fully Depleted Silicon on Insulator technology

Several solutions exist to improve the performance of CMOS transistors at cryogenic temperature while keeping the standard bulk-Si structure. For example, increasing the channel doping can reduce the threshold voltage close to zero at room temperature, resulting in a threshold voltage around 0.4V at cryogenic temperatures. Alternatively, the voltage supply VDD can be increased to maintain the performance of the MOS from 300 down to 4.2K, this solution results nonetheless in a higher power consumption. The solution chosen to realize the Trans-impedance amplifier (TIA) is the Fully Depleted Silicon On Insulator (FDSOI) platform. In the FDSOI technology, the ability to tune the threshold voltage using the back-gate voltage V_{bg} allows to compensate for the temperature dependence of the threshold voltage and makes this technology a promising choice for the design of low power electronics at cryogenic temperature.

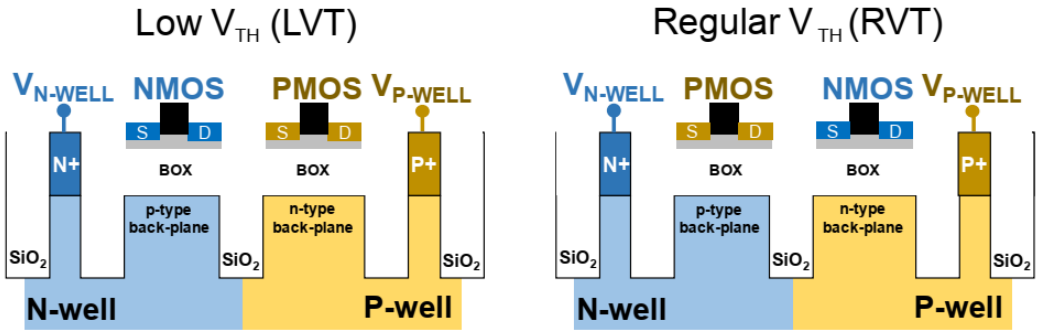

Figure 1.10: a) Low V_{th} (LVT) architecture designed for high-performance applications with a possibility to apply a forward back-gate biasing up to +3V/-3V for NMOS/PMOS at room temperature. b) Regular V_{th} (RVT) architecture used for low-power applications. In this configuration, NMOS (resp. PMOS) channel is placed on top of a p-doped (resp. n-doped) back-plane, resulting in a regular voltage MOSFET. NMOS and PMOS are separated by a deep SiO2 trenches. Adapted from Bohuslavski(2019), [12]

The Silicon On Insulator (SOI) technology consists in adding a buried Silicon-Oxide layer (BOX) under the Silicon junction which isolates the MOSFET channel from the bulk Silicon. This configuration presents several advantages compared to classical bulk MOS, like smaller parasitic capacitances, reduced junction leakage and a simpler isolation of adjacent transistors. Moreover, in the Fully Depleted (FDSOI) version, the Si layer carrying the channel is thin enough so that when a conductive channel is created, it occupies all the thickness of the Si layer. Thus, no floating body is present under the channel, and the Kink effect is totally suppressed in FDSOI. This geometry also improves the electrostatic control so that the electrostatic efficiency m can reach values around 1.1 to 1.05, close to the ideal value of 1.

More importantly, this configuration allows to use the bulk Silicon layer on the back-plane as a second gate (referred as back-gate) in addition to the front-gate (G terminal). A conductive channel can be formed by applying a voltage V_{bg} between the back-plane and the source. In practice, the back-gate is used to modulate the threshold voltage of the transistors while the formation of the channel is controlled by the front-gate. The modulation of the threshold voltage when applying a voltage V_{sb} from the gate to the bulk is called the body effect. While this effect does exist in bulk Si, the gate-like structure of FDSOI greatly improves this effect. The control of V_{th} using the body effect is essential to compensate the rise of V_{th} at cryogenic temperature, and allows to maintain a constant V_{th} when cooling the transistors from 300K to 4K, as shown

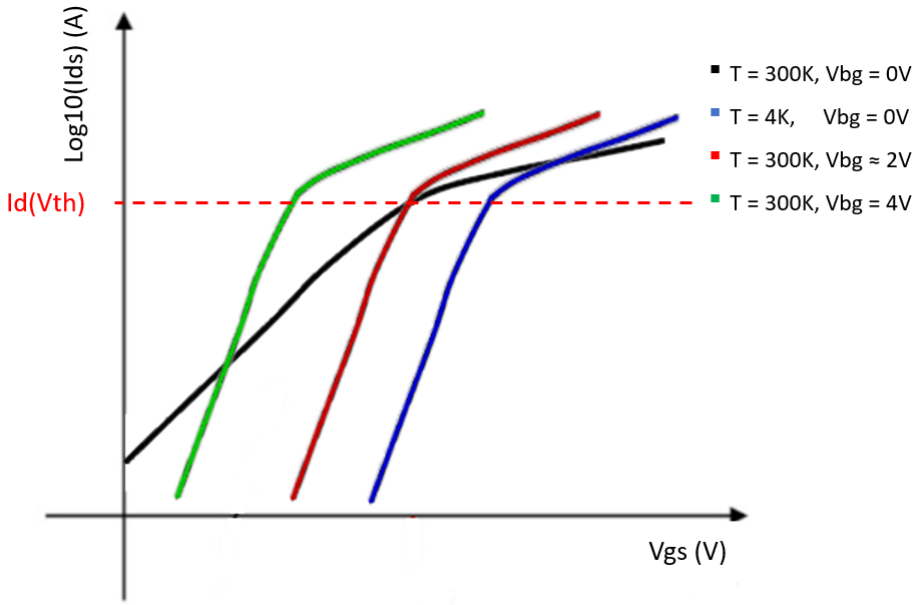

Figure 1.11: Illustration of the influence of the back-gate voltage V_{bg} on the $I_d(V_{gs})$ characteristics of a FDSOI transistor. The increase of V_{th} when decreasing the temperature from 300K to 4K can be compensated by applying an adequate voltage V_{bg}. V_{bg} can be further increased to obtain a value for $V_{th}(4K)$ below its room temperature value.

in fig 1.11. The temperature dependent threshold voltage shift of around 150mV for NMOS and 200mV for PMOS can be compensated by a back-gate voltage of 2V (resp. 3V) for NMOS (resp. PMOS).

In addition, the back-gate voltage can be further increased in order to obtain a V_{th}(T=4.2K) smaller than V_{th}(T=300K). Smaller V_{th} allows a smaller V_{gs} for the same drain current I_d, so that VDD can be reduced. In cryogenic circuits used for the control of an array of qubits, the minimal temperature that can be achieved in the cryostat can be limited by the power consumption of the control electronics due to the self-heating effect. A smaller VDD is therefore of interest to reduce the power consumption of the circuit.

Chapter 2

Study of single MOS transistors

Before starting the simulations and experiments on the Trans-impedance Amplifier circuit used for the read-out of a quantum dot, the influence of cryogenic temperature and back-gate voltage on individual NMOS/PMOS transistors will be discussed in this chapter.

2.1 Evolution of threshold voltage with temperature and back-gate voltage

The threshold voltage of a transistor depends on the temperature. Previous experiments as described in Chapter 1 had shown that V_{th} increases with decreasing temperature until around 100K and starts to stabilize for T < 100K. To check the validity of the model used for the simulation of more advanced circuits, experimental results on individual transistors are compared to the results obtained by simulation. The simulations presented in this work where performed on Cadence Virtuoso, and used a transistor model that has been developed by ST-Microelectronics specifically for the 28nm FDSOI technology. The transistor model has not been designed for low cryogenic temperatures. The model stops converging below T = 85K so the simulations presented will be carried at temperatures between 300 and 90K.

Like the transistors used in the TIA, the NMOS and PMOS models used for the simulations of individual transistors are designed for FDSOI thin film devices. The Regular Voltage Threshold (RVT), thin gate oxide thickness (GO1 with an equivalent oxide thickness of 1.6nm) version is used. Dimensions similar to the transistors used in the TIA are chosen, and the NMOS and PMOS devices considered have same channel length L = 300nm (long channel) and channel width W = 10 μm. Fig. 2.1 shows the schematic of the NMOS and PMOS transistor.

The threshold voltage is here defined as the gate voltage V_{gs} for which the normalized drain current $I_{d,norm}$ defined as $I_{d,norm} = I_d.L/W$ reaches $I_{d,norm,th} = 10^{-7}$A for NMOS and $I_{d,norm,th} = 2.10^{-8}$A for PMOS. The difference between the taken values of normalized current comes from the lower mobility of charge carriers in PMOS, so that the threshold voltage reflects primarily the carrier density in the channel. For the saturation regime, V_{th} is defined at V_{ds} = 0.9V. V_{th} is extracted from a sweep of the gate voltage V_{gs} where $I_{d,norm}(V_{gs} = V_{th}) = I_{d,norm,th}$. This is done at different temperatures between 300 and 90K with a step of 10K and for Back-gate voltages V_{bg} = 0V, 2V and 4V, as shown in figure 2.2.

In agreement to experimental observations, V_{th} shows a linear dependency with respect

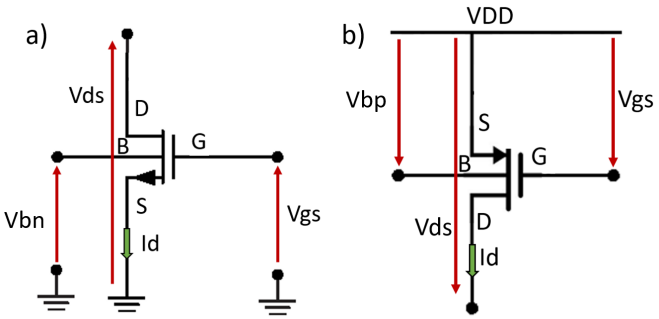

Figure 2.1: a) Schematic of a NMOS transistor and definition of V_{gs}, V_{ds}, V_{bn} and I_d. The voltage V_{bn} is the back-gate voltage of NMOS and is equal to $V_{bn} = V_{bulk} - V_s = V_{bulk}$. b) Same schematic for a PMOS transistor. V_{bp} is the back-gate voltage of PMOS and is equal to $V_{bp} = V_{bulk} - V_s = V_{bulk} - VDD$.

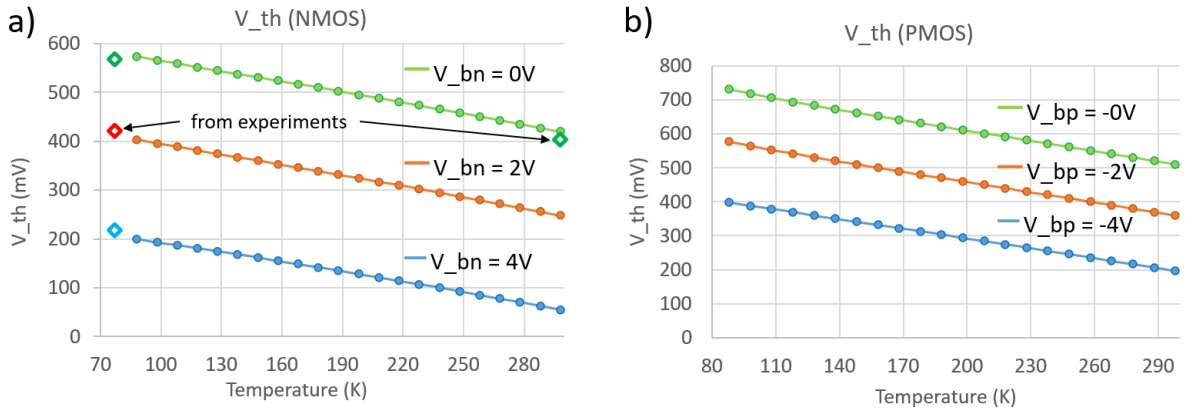

Figure 2.2: Evolution of V_{th} with temperature at different V_{bg}, for a) NMOS and b) PMOS. Lines represent the results obtained by simulations, dots are the experimental results for room temperature (300K) at $V_{bg} = 0$V and for liquid nitrogen temperature (77K) at $V_{bg} = 0, 2$ and 4V.

to the temperature down to T=90K. The temperature coefficient, defined as $\frac{\partial V_{th}(T)}{\partial T}$ is equal to 0.75mV/K for NMOS and 1.12mV/K for PMOS, and stays constant for back-gate voltages between 0V and 4V.

In addition to simulations, experimental measurements on one of the NMOS transistor being part of the TIA are done. No PMOS device was accessible for measurement in the TIA, so the comparison is possible only for NMOS. The transistor used for characterization has same L (300nm) and W (10 μm) as the one in simulations. More details on the experimental apparatus is given in Section 2.2.3. The V_{th} obtained at T = 300K (for $V_{bn} = 0$V) are similar in simulation and in experiment. Experimental values of V_{th} at T = 77K are close to the values obtained by simulations at T = 90K for all V_{bn} between 0 and +4V. This implies that the saturation of V_{th} (cf. [10]) starts around 90K for the NMOS considered, therefore V_{th} has little variations when decreasing the temperature from 90 to 77K. This allows to obtain realistic values of V_{th} using the simulation model limited to T=90K, and the simulation results are validated concerning the V_{th} of transistors.

The influence of the back-gate voltage V_{bg} on V_{th} is now investigated. The back-gate voltage V_{bg} is defined as the voltage between bulk and source: $V_{bn} = V_{bulk} - V_s$. For NMOS, the source is connected to GND so that $V_{bn} = V_{bulk}$, while for PMOS, the source is connected

to VDD so that $V_{bp} = V_{bulk} - VDD$. To study the evolution of V_{th} with V_{bg}, the $I_d - V_{gs}$ curve of the MOS is calculated for different values of V_{bg} between 0V and 5V with a step of 0.2 V. As can be seen in fig. 2.3, this is done at T = 300 and 90K to check the influence of the back-gate with temperature.

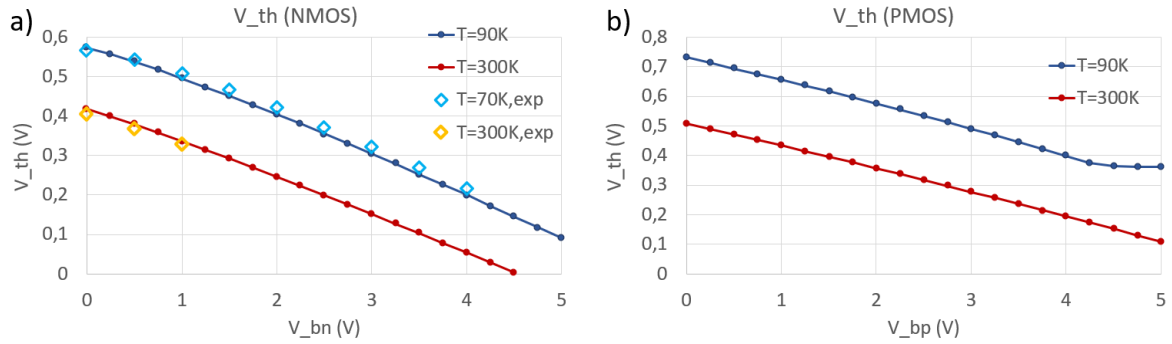

Figure 2.3: Evolution of V_{th} with Back-gate voltage at T=90K for a) NMOS and b) PMOS. Lines represent the results from simulations, dots are the experimental results for V_{bg} between 0 and 1V at T = 300K and for V_{bg} between 0 and 4V at T = 77K.

According to figure 2.3, V_{th} decreases linearly with increasing the back-gate voltage, and this for both NMOS and PMOS devices at 300K, 90K (from the simulations) and 77K (from the experiments). The linear relationship holds from $V_{bg} = 0$ to 5V, except for the PMOS device at T = 90K, exhibiting a saturation of V_{th} at 0.36V. This linear relationship can be characterized by the γ coefficient defined as $\gamma = -\frac{V_{th}(V_{bg}) - V_{th}(0)}{V_{bg}}$. At $V_{bg} = 4$V, we find $\gamma = 95$mV/V for NMOS and $\gamma = 82$mV/V, and γ stays approximately constant for temperatures between 300K and 77K. The results of simulations and experiments are in agreement, validating the simulation for the $V_{th}(V_{bg}$ dependence.

The study of the threshold voltage with the back-gate voltage yields the V_{bg} needed to compensate the increase of V_{th} with decreasing temperature. From fig. 2.3, this value is evaluated at $V_{bn} = 1.8$V for NMOS and $V_{bp} = 2.9$V for PMOS when cooling the transistors from 300K to 90K

In addition, it is also possible to balance the V_{th} of NMOS and PMOS by further increasing V_{bp} for PMOS. The difference between $V_{th}(NMOS)$ and $V_{th}(PMOS)$ is around 85mV at T=300K and 145mV at T=90K. The additional voltage to apply on V_{bp} compared to V_{bn} to obtain $V_{th,NMOS} = V_{th,PMOS}$ is therefore $V_{bp} = V_{bn} + 1.0$V at T=300K and $V_{bp} = V_{bn} + 1.7$V at T=90K.

In conclusion, the simulations demonstrate the possibility to tune the back gate in order to keep the threshold voltage constant for decreasing temperature. The maximum back-gate voltage applicable to the transistors without damaging the oxide is around +/-5V, this corresponds to a V_{th} shift of 480mV for NMOS and 420mV for PMOS. From previous results, it can be predicted that maintaining a constant V_{th} with temperature should be achievable down to T = 4.2K. Nonetheless, obtaining equal V_{th} for NMOS and PMOS while compensating the V_{th} shift at 4.2K would require a V_{bp} of at least 2.9 + 1.7 = 4.6V for PMOS, close to the maximal back-gate voltage applicable. Experimental characterization of PMOS at 4.2K would therefore be of interest to test this possibility.

2.2 Evolution of the transconductance g_m

The transconductance g_m of a transistor is an important parameter to characterize the performance of analog circuit stages, especially with respect to the gain of a transistor. g_m relates the variations of current I_d through the drain of a transistor to variations of its gate voltage V_{gs} by the expression $g_m = \frac{\partial I_d}{\partial V_{gs}}$. g_m therefore characterises the voltage to current gain of the transistor.

Before studying the influence of temperature and back-gate voltage on g_m, the different regimes of operation of a MOSFET transistor will be given. The TIA has been designed to operate at a biasing current $I_{bias} = 10\mu$A. In this case, the transistors composing the TIA operate at high I_d, imposing $V_{gs} > V_{th}$, which corresponds to the Strong Inversion regime. This regime can be divided in the triode and the saturation region. The triode region corresponds to $V_{ds} < V_{gs} - V_{th} = V_{overdrive}$, in this case I_d increases linearly with increasing V_{ds}. In the saturation region, where $V_{ds} > V_{overdrive}$, I_d is approximately constant with increasing V_{ds} due to velocity saturation at high transverse electric field. In addition, biasing the TIA at low I_{bias} would be of interest for low power operation where the self-heating effect is reduced. In this case, the transistor operates in the sub-threshold regime at $V_{gs} < V_{th}$, also called Weak Inversion regime. The current mirrors used in the TIA can only operate in the saturation regime or in the sub-threshold regime at high V_{ds}, for which I_d is independent of V_{ds}. The triode region will therefore not be studied.

The complete set of expressions of I_d, g_m and g_{ds} as a function of V_{gs} and V_{ds} in all regions of operation of transistors are given in the Table 3.2 in Appendix 1, where g_m is defined as $g_m = \frac{\partial I_d}{\partial V_{gs}}$ and g_{ds} as $g_{ds} = \frac{\partial I_d}{\partial V_{ds}}$.

In the Strong Inversion saturation regime g_m can be expressed as a function of V_{gs} as:

$$g_m = \beta.(V_{gs} - V_{th}) \tag{2.1}$$

Here β is a parameter dependent on the technology and is equal to $\beta = \frac{W}{L}.\mu.C_{ox}$, where μ is the effective mobility of electrons or holes inside the channel, and C_{ox} is the oxide capacitance between the metal gate and the channel. To study the evolution of g_m with V_{gs} in different conditions, a sweep on V_{gs} from 0 to 1V is simulated on Cadence Virtuoso, g_m is then extracted as the derivative of I_d with respect to V_{gs}. This is repeated at various back-gate voltages $V_{bg} =$ 0, 2 and 4V, and at T = 300 and 90K. The simulations presented in this section where carried out on both NMOS and PMOS. As similar results where obtained for PMOS, only the results for the NMOS devices are included in the figures and discussed, as shown in fig. 2.4. Here, V_{bg} refers to the back-gate voltage applied to the NMOS device, called V_{bn} in the previous sections where both NMOS and PMOS are studied.

In the left part of figure 2.4, it can be observed that, at a given temperature, the variation of the back-gate voltage is translated as a shift in the g_m-V_{gs} curves of NMOS towards lower V_{gs} when V_{bg} is increased. From the equation 2.1, this can be explained by the reduction of V_{th} when V_{bg} is increased. The shift towards lower V_{gs} was also observed for PMOS when applying a negative back-gate $V_{bp} = -V_{bg}$. To confirm this, the right figure represents the evolution of g_m as a function of the overdrive voltage, defined as $V_{over} = V_{gs} - V_{th}$. At T=300K, the g_m-V_{over} curves are all superimposed for both NMOS and PMOS, confirming that most of the influence of V_{bg} on g_m comes from the V_{th} shift. At T=90K, this is valid for all values of V_{bg} for PMOS,

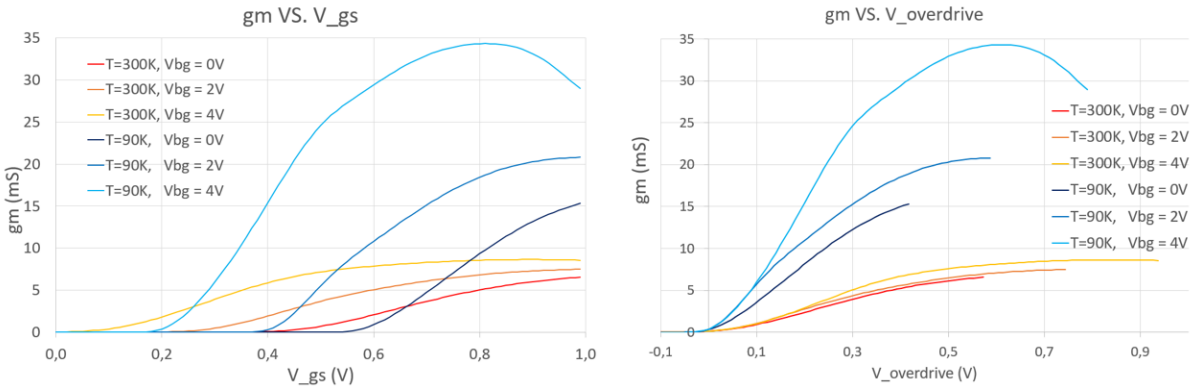

Figure 2.4: Evolution of the g_m as a function V_{gs} (left) and as a function of $V_{overdrive}$, at different Temperatures (300K and 90K) and different back-gate voltage $V_{bn} = V_{bg} = 0$, 2 and 4V, for a NMOS

but only for $V_{bg} < 2$V for NMOS, while g_m of NMOS is increased for $V_{bg} = 4$V at same V_{over}. The increase of g_m for $V_{bg} = 4$V implies a strong increase of I_d with V_{over}. This results in a saturation of I_d at high V_{over} which translates into a reduction of g_m, as observed in fig. 2.4.

Concerning the evolution of the g_m-V_{over} curve with respect to temperature, fig. 2.4(right) shows that g_m is increased by a factor 3 for NMOS and 2 for PMOS when going from 300K to 90K. This can explained by the variation of μ with temperature resulting in a variation of β with temperature (β proportional to μ). As discussed in Section 1.2.3, the mobility of long channel devices is increased with decreasing temperature due to Phonon Scattering becoming negligible at 90K. In fig 1.9, the mobility at 90K is multiplied by a factor 3 for NMOS and a factor 2 for PMOS compared to 300K, which is well correlated with the increase of g_m observed in the simulations.

While the evolution of g_m has been studied with respect to V_{gs}, the operating point of the TIA circuit studied later is defined by a biasing current. This current is defined by an external reference and copied in the TIA. Therefore, it is also of interest to study the dependence of g_m with respect to I_d. From the expression of I_d presented in Appendix 1 Table 3.2, an expression of g_m is found both in Strong Inversion and in Weak Inversion, respectively:

$$\text{Strong Inv.: } g_m = \sqrt{2.\beta.I_d} \quad | \quad \text{Weak Inv.: } g_m = \frac{I_d}{\epsilon.U_t} = \frac{I_d.q}{\epsilon.k_B.T} \tag{2.2}$$

where in Strong Inversion, the β coefficient is considered independent of I_d. In Weak Inversion, ϵ is a non ideality factor equal to 1 in the ideal case. The evolution of g_m with Temperature and Back-gate voltage in both Strong and Weak Inversion regime will also be investigated during the simulations. To obtain the $g_m - I_d$ curves, a sweep on V_{gs} is performed retaining the corresponding values of I_d and g_m. The results of these simulations are shown in figure 2.5 and figure 2.6.

In the Weak Inversion regime ($I_d < 3.10^{-6}$A), the logarithmic plot in fig 2.5 shows a relationship of the type $ln(g_m) = c + ln(I_d) = ln(k.I_d)$ where $k = e^c$ is constant with I_d. This implies a linear dependence between g_m and I_d, as predicted by the equation 2.2 for the Weak Inversion. This equation also shows that changing the temperature from 300K to 90K should translate into a multiplication of g_m by a factor 3.3, and this is verified in the simulation results along the entire range of the Weak Inversion regime. Concerning the influence of the Back-gate

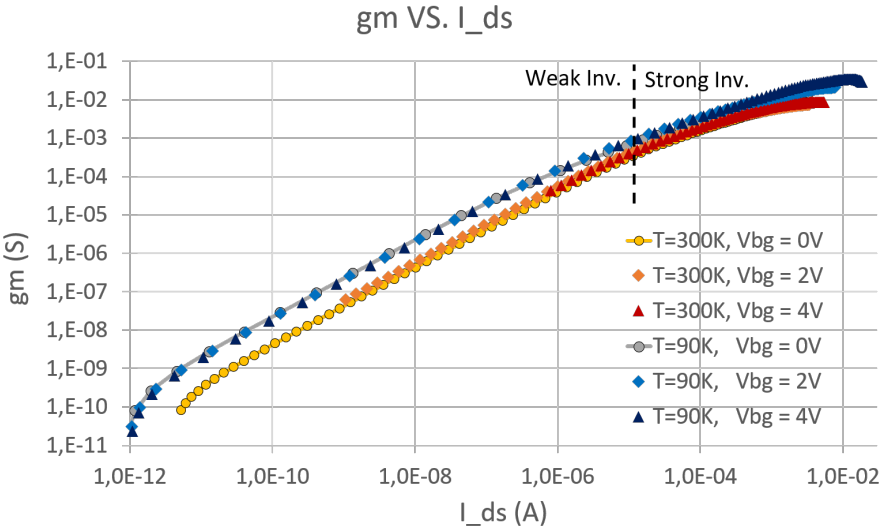

Figure 2.5: Evolution of g_m as a function of I_d in Weak and Strong Inversion regime in a logarithmic scale, at different temperatures and different back-gate voltage, for a NMOS

voltage, no change of g_m is observed when changing V_{bg} from 0V to +4V in Weak Inversion, as predicted by Equation 2.2 (Weak Inv.) where no factor depends on V_{bg}.

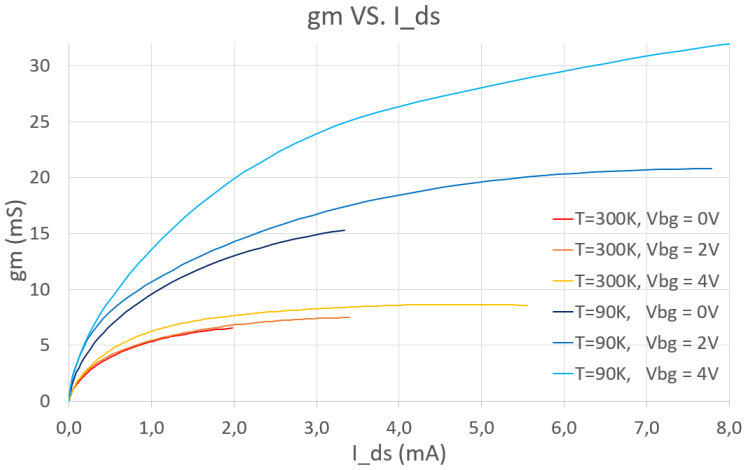

Figure 2.6: Evolution of g_m as a function of I_d, at different temperatures (300K and 90K) and different back-gate voltage (0V, 2V and 4V), for a NMOS. A square-root dependence of g_m with respect to I_d is seen in all conditions.

As can be seen in figure 2.6, in the Strong Inversion regime, g_m exhibits a square-root dependence with respect to I_d, as predicted by equation 2.2 (Strong Inv.). Again, the influence of temperature and back-gate voltage on g_m can be explained by their influence on β via the mobility μ. As for the evolution of g_m with V_{gs}, a small increase of g_m with increasing V_{bn} and a stronger increase of g_m with decreasing temperature is observed.

2.3 Experimental results

To check the validity of the model used by the simulations, experimental measurement as been carried. Since no isolated transistor was available for characterization, one of the NMOS integrated in the TIA (N3 in figure 3.2) as been used, this transistor as same characteristics as the one used in simulation: W= 10μm, L= 300nm and gate oxide thickness of 1.6nm (GO1). As can be seen in fig 3.2, the transistor N3 is diode connected, i.e. the gate and the source are connected together. A schematic of the diode connected NMOS with the instrument used for its characterization is shown in fig 2.7.

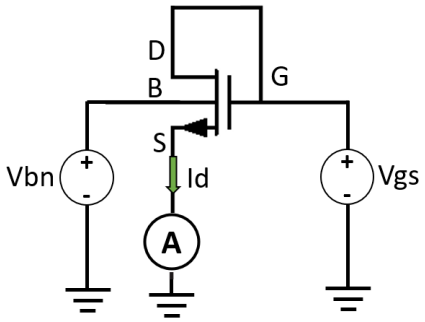

Figure 2.7: Schematic of the diode connected NMOS transistor used for experimental characterization, where the gate and drain terminal are connected. V_{gs} and V_{bn} are controlled by external DC sources, the current I_d is measured by a pico-amperemeter.

The $I_d - V_{gs}$ curve of the transistor is studied by applying a DC voltage on the gate V_{gs} using a multi-channel DC source (called DAC) while the drain current I_d is measured using an amperemeter able to measure DC currents in the range of 1 pA to 10mA. The back-gate voltage of the NMOS V_{bn} is also controlled by the DAC to see the influence of V_{bn} on the threshold voltage V_{th} and the Sub-threshold slope SS. The measurement is performed at room temperature (300K) and at cryogenic temperature by placing the chip in a container filled with liquid nitrogen at 77K (cf. fig 3.23 in Appendix 3).

As can be seen in fig 2.8, at T=300K, V_{th} = 0.40V at V_{bn} = 0V, and SS is evaluated at SS = 62.5mV/V, close to the theoretical minimum of 60mV/dec. At 300K, V_{bn} has been kept in the range of $\pm$1V in order to avoid damaging the p and n-wells in the bulk.

At T=90K, the back-gate voltage range can be increased to $\pm$4V without damaging the device. V_{th} is increased to 0.57V at V_{bn} = 0V and is reduced to 0.21 at V_{bn} = 4V. The experimental values of threshold voltage are also included in fig 2.3 for comparison with simulation, and very close results are observed for all temperatures and all V_{bn}. In addition, at T=90K, the SS is reduced. The mean value of SS along 3 decades of I_d from 10^{-10}A to 10^{-7}A is evaluated at SS = 18.7mV/V, and this values stays constant for all values of back-gate voltage tested between 0 and +4V.

These experimental results confirm the validity of the model used in simulation for long channel NMOS in term of threshold voltage, with very close results in term of threshold voltage and Sub-threshold slope and similar results were obtained concerning the influence of the back-gate voltage.

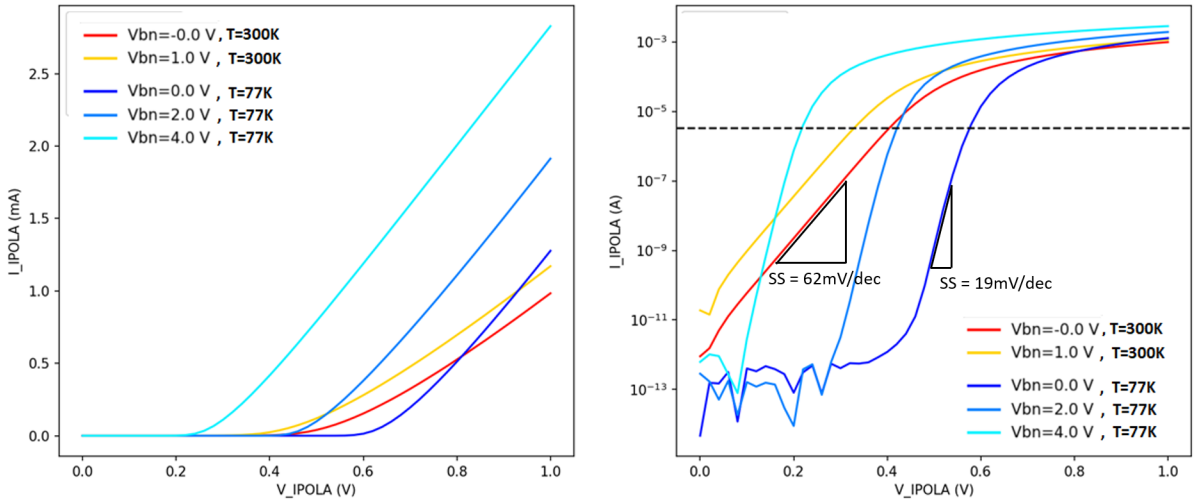

Figure 2.8: Experimental measure of the I_d-V_{gs} at room temperature 300K and at liquid nitrogen at 77K and for Back-gate voltage V_{bn} between 0V and +4V applied on the NMOS.

Chapter 3

Study of the TIA circuit

This chapter will present the general characteristics and performances of the Trans-Impedance Amplifier (TIA) circuit composed of the FDSOI transistors described in the previous chapter. In the context of spin qubit manipulation and read-out, the TIA measures the current of the high-impedance quantum dot device to perform the read-out of the quantum state. The principle of the read-out using the TIA is therefore to measure the output current of the qubit which is in the range of tens of nA, and to convert the current into a voltage readable by standard electronics. The TIA is composed of an operational amplifier and a feedback network, as shown in the basic schematic of fig. 3.1. A previous characterization of this TIA was conducted in the frame of the study of a larger circuit performing the excitation and current sensing of a co-integrated double quantum dot. This work is presented in [16].

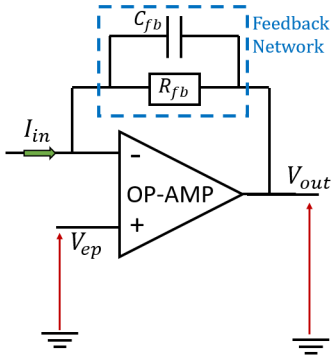

Figure 3.1: Basic schematic of a Trans-impedance Amplifier (TIA) composed of an operational amplifier (OP-AMP) and a Feedback network (blue square). Oscillations of input current I_{in} are amplified and converted and into oscillations of output voltage V_{out}.

3.1 Description of the TIA circuit

First, the circuit will be studied in the operational amplifier (OP-AMP) mode without the feedback network.

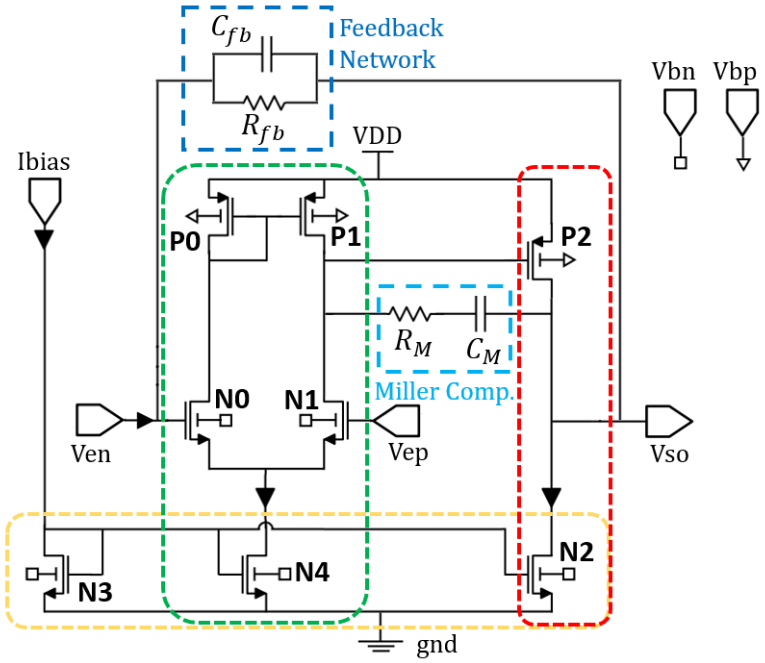

Figure 3.2: Topology of the TIA composed of the OP-AMP and of a Feedback network (dark blue). The OP-AMP composed of a differential amplification stage (green) and a common source stage (red) with Miller compensation (light blue).

3.1.1 OP-AMP mode

The OP-AMP used for the TIA is a custom circuit designed by LETI IC (integrated circuit) designers. As can be seen in figure 3.2, it is composed of a differential amplification stage (green box) providing an output voltage proportional to the voltage difference between the inputs $V_{ep} - V_{en}$. This signal is then sent to a common source amplifier (red box) which provides the gain necessary to obtain a high output voltage range. These two stages are biased by a current mirror (yellow box) copying the current provided by an external current source.

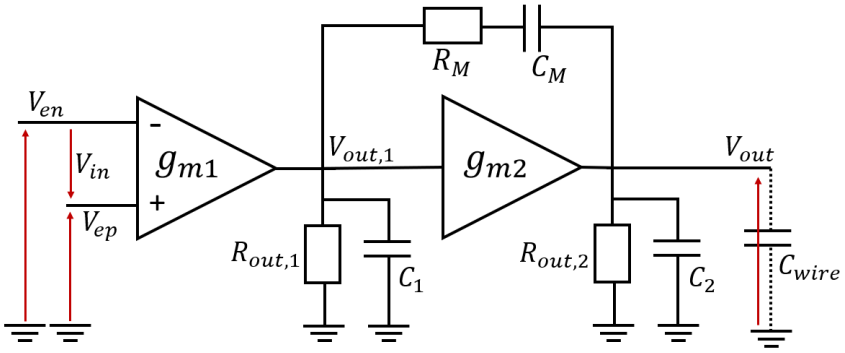

Figure 3.3: Equivalent block diagram of the OP-AMP. g_{m1} and g_{m2} are the gain of stages 1 and 2. Output resistance and capacitance of stages 1 and 2 are also represented. The common-mode V_{ep} is set to 0.6 V for all simulations. R_M and C_M forms the Miller compensation network.

The OP-AMP circuit is equivalent to the circuit shown in fig 3.3, where $g_{m1,2}$ is the transconductance gain of stages 1 and 2, and $R_{out1,2}$ and $C_{1,2}$ are the equivalent output resis-

tance and capacitance of stages 1 and 2.

The voltage applied at the input V_EP and V_EN can be written as: $V_{ep} = V_{cm}$ and $V_{en} = V_{cm} - V_{in}$. Here, the common mode voltage V_{cm} is the DC voltage of V_EP and V_EN, and is equal for both inputs. Applying an adequate common mode voltage V_{cm} is necessary to achieved a correct operation of the OP-AMP, the acceptable range of V_{cm} will be discussed in following sections.
A change of the quantum device state measured by the TIA is translated by oscillations of its output current around a continuous value. In the OP-AMP mode, this is represented by applying low amplitude voltage oscillations V_{in} around the DC component V_{cm} to the V_EN input. Therefore, the maximal input frequency for which the circuit achieves a correct amplification of the input signal will determine the maximum frequency at which the measurement of the quantum device can be achieved. This is characterized by the bandwidth of the circuit, which will be characterized in following sections.

The differential pair has a gain defined as : $A_{v1} = \partial V_{out,1}/\partial V_{in}$. This can be decomposed as : $A_{v1} = g_{m,N1} \cdot R_{out,1}$, where $g_{m,N1} = \partial I_{out,1}/\partial V_{in}$ is the transimpedance gain of the stage and $R_{out,1}$ is the equivalent output resistance of the stage. A transistor exhibits an output resistance equals to $1/g_{ds}$, thus the output resistance of stage 1, created by the output resistance of N1 and P1 in parallel, is equal to $R_{out,1} = 1/(g_{ds,N1} + g_{ds,P1})$. The gain of the differential pair is therefore $A_{v1} = \dfrac{g_{m,N1}}{g_{ds,N1} + g_{ds,P1}}$.
Some parasitic capacitances are present between the terminal of N1 and P1 transistor, like N1 and P1 drain-source capacitances and the capacitance created by the wires at the output of stage 1. These capacitances can be represented by the equivalent output capacitance C_1. This capacitance in parallel to $R_{out,1}$ results in a RC filter at the output of the stage, limiting the Bandwidth of the stage to frequencies lower than $F_{cutoff,1} = \dfrac{1}{2.\pi.R_{out,1}.C_1}$

Similarly, the gain of the second stage is defined as $A_{v2} = \partial V_{out}/\partial V_{out,1}$. In the same way as for stage 1, it can be expressed as $A_{v2} = \dfrac{g_{m,P2}}{g_{ds,N2} + g_{ds,P2}}$. This stage also has a finite Bandwidth due to its equivalent output resistance and capacitance, and the frequency cutoff is given by $F_{cutoff,2} = \dfrac{1}{2.\pi.R_{out,2}.C_2}$. The output of stage 2 is the output of the TIA. Therefore, the total output capacitance includes the capacitance of connection between the Vso pin and any external system. This can be of the order of 0.1-1pF if the TIA is connected to another circuit at cryogenic temperature, or between 100 and 300pF when it is connected through long cables to an electronic block placed at room temperature (300K).

A large capacitance at the input of the circuit (up to 100-300pF when it is used at T = 300K while measuring a device placed at 4.2K) results in a poor stability of the OP-AMP. In addition, the two dominant poles of the low-pass filters increases the instability of the circuit. To solve this, a Miller compensation (capacitance C_M) as shown in fig 3.2 (light blue box) is added. Due to the Miller effect, the capacitance C_M seen at the output of stage 1 becomes $A_{v2}.C_M$, which is much larger than C_1. The resulting equivalent output capacitance is finally $C_{eq,1} = C_1 + A_{v2}.C_M \approx A_{v2}.C_M$. This further reduces the bandwidth of the OP-AMP but also improves its stability. In addition, the resistance R_M creates a negative zero in the transfer function, improving the gain and phase margin.

The performances of the OP-AMP with Miller compensation are given by the equations:

$$\text{for the DC gain: } G_{dc} = A_{v1}.A_{v2} = \frac{g_{m,N1}}{g_{ds,N1} + g_{ds,P1}}.\frac{g_{m,P2}}{g_{ds,N2} + g_{ds,P2}} \tag{3.1}$$

$$\text{for the Bandwidth: } BW = \frac{1}{2.\pi.R_{out,1}.C_{eq,1}} = \frac{g_{ds,N1} + g_{ds,P1}}{2.\pi.C_M.A_{v2}} \tag{3.2}$$

$$\text{and for the gain-bandwidth product: } GBW = G_{dc}.BW = \frac{g_{m,N1}}{2.\pi.C_M} \tag{3.3}$$

The theoretical expression found for the GBW of the OP-AMP only depends on the transconductance of N1 and of a constant capacitance.

Using the expression of g_m as a function of $I_{ds,N1} = I_{bias}$ given by equation, we find, for a MOS in weak and strong inversion (in the saturation regime) respectively:

$$W.I: \quad GBW = \frac{q}{\epsilon.k_B.T} \cdot \frac{I_{bias}}{2.\pi.C_M} \quad | \quad S.I: \quad GBW = \frac{\sqrt{2.\beta_{N1}.I_{bias}}}{2.\pi.C_M} \tag{3.4}$$

Finally, equation 3.4 (W.I.) shows that, starting in the Weak Inversion regime, GBW increases proportionally to I_{bias}. When further increasing I_{bias}, the Strong Inversion regime is reached, and GBW increases more slowly with I_{bias} due to the square-root relationship. Concerning the temperature dependence, a significant increase of GBW should be observed in Weak Inversion due to the $1/T$ factor, whereas in Strong Inversion, the theoretical expression shows no strong dependence of GBW with temperature. The small increase of β at low temperature should results in a weak dependence of GBW on temperature. No dependence of GBW on back-gate voltage is expected in Weak Inversion since none of the factor present in equation 3.4 (W.I.) has a dependence on V_{bg}. In Strong Inversion, a small increase of GBW with positive V_{bg} should be explained by a small increase of β.

3.1.2 TIA mode

Now that the OP-AMP circuit has been studied, the feedback network (dark blue box in fig. 3.2) given by R_{fb} and C_{fb} in parallel is added to obtain a trans-impedance amplifier (TIA). In TIA mode, the input considered is now an AC current source i_{in} of amplitude of the order of 10nA.

For an ideal OP-AMP (infinite DC gain and Bandwidth), the feedback network gives the following transfer function:

$$\underline{H}(s) = \frac{R_{fb}}{1 + R_{fb}.C_{fb}.s}, \quad \text{with complex } s = i2\pi f \text{ for a frequency f} \tag{3.5}$$

When the DC gain and Bandwidth are not limited by the OP-AMP, the feedback network sets the gain of the TIA to $G_{dc} = R_{fb} = 10.6\ \text{V}/\mu\text{A}$ and the bandwidth to $BW = \frac{1}{2.\pi.R_{fb}.C_{fb}} = 4.29\text{kHz}$ for $R_{fb} = 10.6\text{k}\Omega$ and $C_{fb} = 291\text{pF}$.

3.2 Simulation of the TIA on Cadence Virtuoso

3.2.1 Frequency behavior of the OP-AMP and the TIA

Before characterizing the TIA, the OP-AMP alone will be studied without the feedback network. First, the gain and phase of the OP-AMP are evaluated as a function of frequency along a logarithmic sweep performed between 1Hz and 1GHz at a given operating point (defined by the biasing current I_{bias}, the voltage supply VDD, the back-gate voltages $V_{bn,p}$ and the temperature T). Fig. 3.4 shows the transfer function of the OP-AMP at $I_{bias} = 10\mu$A, $VDD = 1$V, $V_{bn,p} = 0$V and $T = 300K$ with the extraction of the DC gain G_{dB} and the Bandwidth BW.

The transfer function of the OP-AMP presents two negative poles $\omega_{p,1}$ and $\omega_{p,2}$ and a negative zero ω_z. At the nominal biasing current $I_{bias} = 10\mu$A, their values are $\omega_{p,1} = 10$Hz, $\omega_z = 1$MHz, $\omega_{p,2} = 50$MHz. The transfer function also shows large gain and phase margin at $I_{bias} = 10\mu$A. For all other values of I_{bias} between 1nA and 100μA, sufficient margins are found thanks to the Miller compensation.

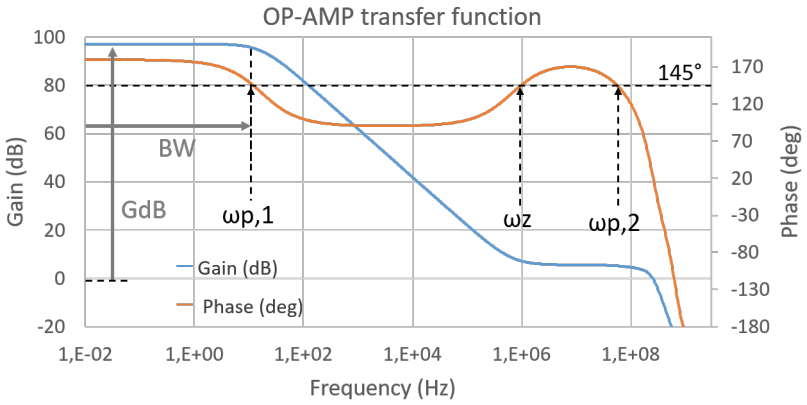

Figure 3.4: Gain and Phase of the transfer function of the OP-AMP at T=90K for $I_{bias} = 10\mu$A and VDD=1V. G_{dB} is defined as the gain (dB) at 0.01Hz. Bandwidth is defined as the frequency for which $Gain(f) = G_{dB} - 3$dB, which coincides with $\omega_{p,1}$. $\omega_{p,1}$, ω_z, $\omega_{p,2}$ are extracted using the phase.

The obtained evolution of G_{dB}, BW and GBW with the biasing current is shown on a logarithmic scale in fig 3.5. These quantities are also calculated using the equations 3.1, 3.2 and 3.3, where the values for transconductance g_m and channel conductance g_{ds} of transistors is extracted directly from the simulation for the different operating points.

For $I_{bias} > 10n$A the values of G_{dB} and BW calculated from transfer function and from the values g_m and g_{ds} gives the same result. G_{dB} presents a slow decrease with I_{bias} and the BW exhibits a linear relationship with I_{bias}. Below 10nA, a small deviation between the 2 methods is observed. The gain-bandwidth product GBW is proportional to I_{bias} in Weak Inversion, which is coherent with the theoretical expression in Eq. 3.4 (WI), and its increase slows down in Strong Inversion, which corresponds to the square-root relationship in I_{bias} in Eq. 3.4 (SI). Moreover, the small deviation of G_{dB} and BW cancel each other, so that both method of extraction of GBW gives same result on all the I_{bias} range. Therefore, the internal consistency of the models used in the simulations is confirmed.

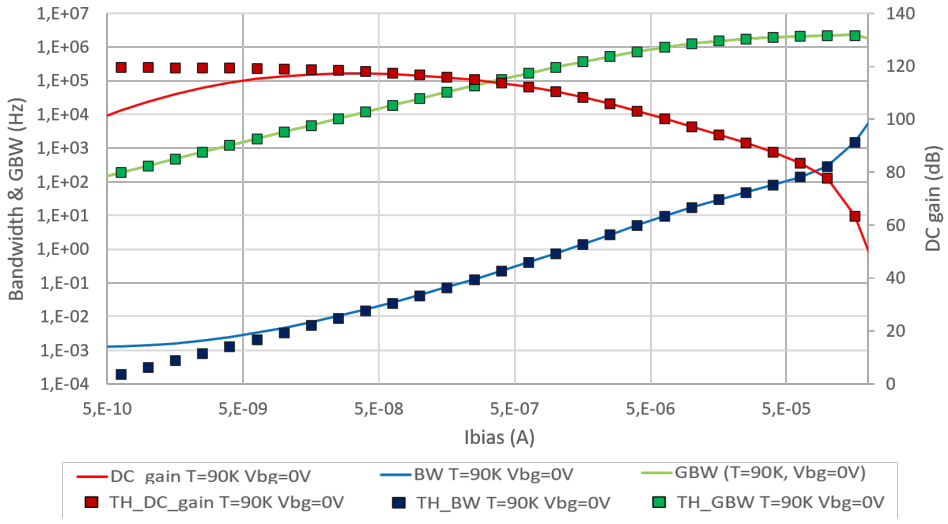

Figure 3.5: Simulations of G_{dB}, BW and GBW as a function of I_{bias}, at T=90K and for a back-gate voltage $V_{bg} = 0$V, a common mode $V_{cm} = 0.6$V and a voltage supply $VDD = 1$V. The values extracted from the frequency sweep are in full lines, the ones extracted from the values of g_m and g_{ds} given by simulations on Virtuoso and using equations 3.1, 3.2 and 3.3 are represented as squares

The evolution of GBW with respect to the power consumption of the OP-AMP is now studied. In the simulations, the power consumption is calculated as $P = VDD \times I_{vdd}$. I_{vdd} is the total current flowing into the OP-AMP and is the sum of the currents flowing in the differential amplification stage $I_{s1} = I_{bias}$ and in the common source stage $I_{s2} = 2 \times I_{bias}$, so that $P = 1 \times 3 \times I_{bias} = 3I_{bias}$. Therefore, the evolution of GBW with respect to $Power$ is similar to the evolution with respect to I_{bias} in equations 3.4 and only changes by a factor 3. The dependence of GBW on $Power$ is studied at T = 300 and 90K for different back-gate voltage (0V, 2V and 4V).

Here, an opposite back-gate voltage is applied to NMOS compared to PMOS, so that an applied back-gate voltage V_{gb} gives $V_{bn} = V_{bg}$ and $V_{bp} = -V_{bg}$ (where $V_{bn,p} = V_{bulk} - V_s$). The results are presented in figure 3.6.

In Weak Inversion (for $P < 10^{-5}$W), the expected linear dependence of GBW on $Power$ is observed for all values of temperature and V_{bg}. Reducing the temperature from 300K to 90K increases the GBW by a factor 3, attesting that GBW is proportional to 1/T (cf Eq. 3.3), whereas no influence of V_{bg} is shown in Weak Inversion. In Strong Inversion, at 90K, the maximal GBW achieved is reduced to 2.10^6 Hz at $P = 2.10^{-4}$W. This can be corrected by applying a back-gate of $V_{bg} = 2V$. In this case the square-root dependence of GBW in Strong Inversion ($P > 10^{-5}$W) is respected until the operating Power of 100μW, and the GBW can reaches 2.10^7Hz.
Applying a positive V_{bg} could finally be of interest for high performance at high power, especially when the TIA is operated at cryogenic temperature where applying $V_{bg} > 2$V multiplies the maximal GBW by 10.

By including the feedback network in the simulation, the frequency behavior of the TIA is now studied. When the OP-AMP is correctly biased, the DC gain G_{dB} and the Bandwidth BW are limited by the feedback network so that $G_{dB} = 10,6.10^6 = 140$ dB and $BW = 4,29$ kHz. As shown in fig 3.7, the maximal BW is of 4.64kHz at 300K and 4.72kHz at 90K. The

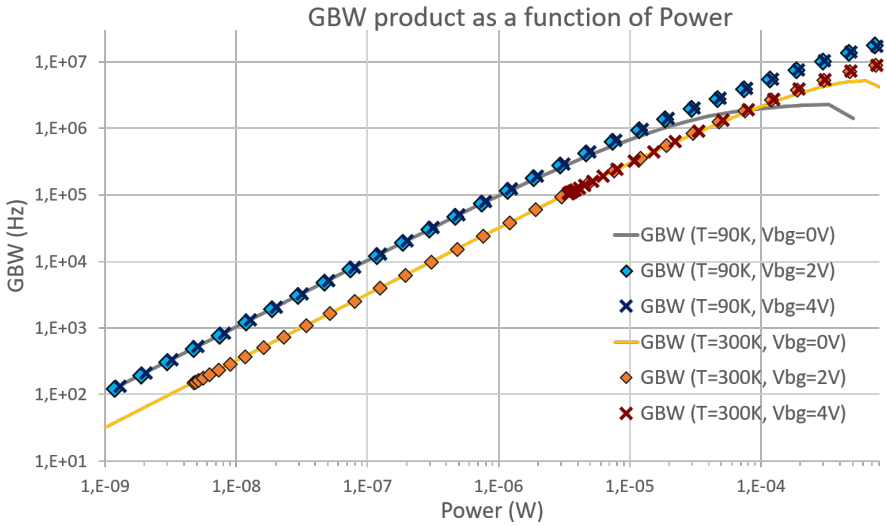

Figure 3.6: Evolution of GBW with Power consumption $P = 3.I_{bias}$, for T=300K and T=90K and for V_{bg} = 0V, 2V and 4V.

small difference can be explained by a variation of the resistance R_{fb} with temperature which changes the cut-off frequency of the feedback network.

The characterisation of the OP-AMP has shown that its DC gain is approximately constant when reducing $Power$ whereas the Bandwidth is reduced, such that the Bandwidth of the TIA can be limited by the OP-AMP at low operating Power. This behavior is confirmed in fig 3.7, where the -3dB bandwidth has been computed as a function of $Power$. The bandwidth starts decreasing when $P = 4.10^{-7}$W at 300K and when $P = 1.10^{-7}$W at 90K, which corresponds in both case to $GBW \approx 1,3.10^{4}$Hz for the OP-AMP. No improvement of this value is observed when a V_{bg} up to +4V is applied.

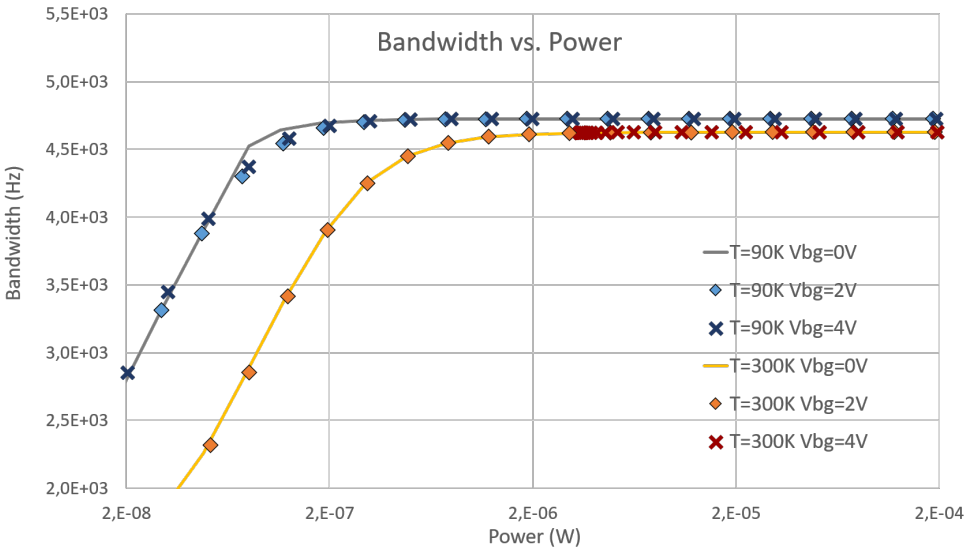

Figure 3.7: Evolution of the Bandwidth with Power consumption, for T=300K and T=90K and for V_{bg} = 0V, 2V and 4V.

3.2.2 Influence of back gate on power reduction

The minimal voltage supply VDD necessary to have a correct operation of the TIA and its evolution with the Back-gate voltage is now investigated. The transfer function of the TIA is plotted for different values of VDD between 0V and 1V, at high and low I_{bias} (10μA and 10nA) and for T=300K and T=90K. To ensure a correct biasing of transistors N0 and N1, the common mode V_{cm} is tuned according to VDD at $V_{cm} = 0.6 \times VDD$.

In all those cases, both G_{dB} and BW stay constant when reducing VDD until the DC gain is abruptly reduced when VDD becomes too low, as can be seen in fig 3.8. This comes from the fact that the biasing current I_{bias} imposed on stage 1 and 2 by the current mirrors in turn imposes a values on $V_{overdrive} = V_{gs} - V_{th}$ for the transistors in the TIA (where V_{th} depends on temperature and back-gate voltage). When VDD becomes too small, the required V_{gs} cannot be achieved for all transistors, which results in the abrupt decrease of G_{dB} observed. The minimal VDD for correct operation of the TIA can therefore be characterized by the value for which G_{dB} starts decreasing.

Using this condition, the evolution of the minimal VDD (VDD_{min}) as a function of V_{bg} is studied. Because higher values could damage the device, V_{bg} is limited to +4V. First, an opposite back-gate voltage is applied to NMOS and PMOS ($V_{bn} = -V_{bp} = V_{bg}$). According to fig. 3.9 (equal V_{bg}), at 300K, $VDD_{min} = 0.6$V for $V_{bg} = 0V$ and can be decreased to 0.25V for $V_{bg} = 4V$. At 90K, $VDD_{min} = 0.82$V at zero back-gate and decreases to 0.44V for $V_{bg} = 4V$.

The same procedure is followed for an equal threshold voltage between NMOS and PMOS. This is done by increasing further $|V_{bp}|$ in order to compensate for the higher V_{th} of PMOS, and V_{bp} is chosen depending on V_{bn} such that $V_{th,PMOS}(V_{bp}) = V_{th,NMOS}(V_{bn})$. The results (fig 3.9 (equal V_{th})), indicate a stronger reduction of VDD_{min} at T=300K down to $VDD_{min} = 0.12$V for $|V_{bp}| = 6.25$V, but applying this voltage would damage the device in a real case (for which $|V_{bp}|$ is kept below 4V). This nonetheless demonstrates that the minimum VDD achievable is limited by the higher V_{th} of PMOS.

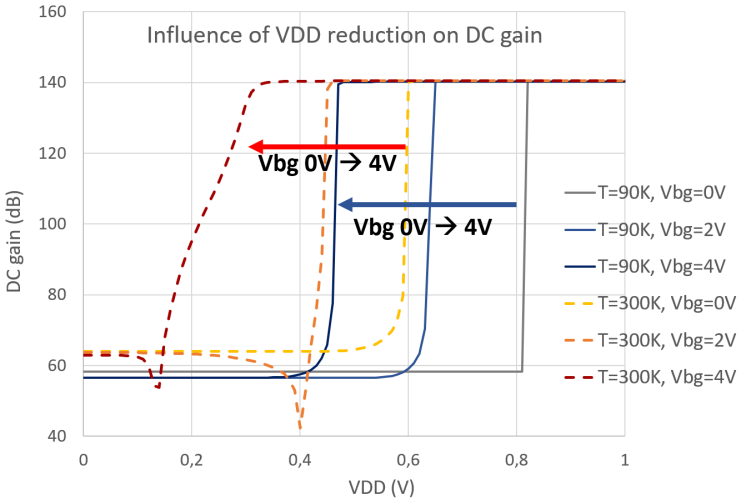

Figure 3.8: DC gain as a function VDD of the TIA for different V_{bg} at T=300K and T=90K, showing the minimum value of VDD for which the gain collapse.

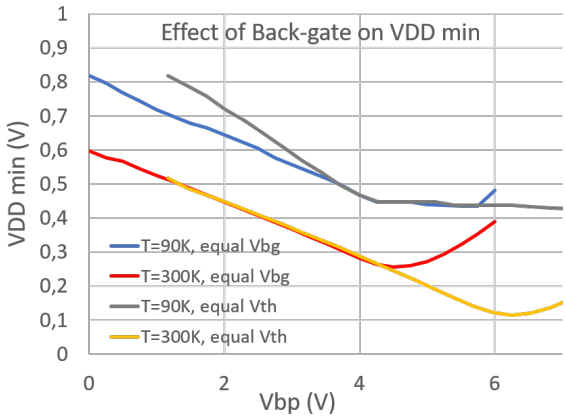

Figure 3.9: Evolution of the minimum VDD providing a correct DC gain of +20dB, at T=300K and T=77K for $I_{bias} = 10\mu$A. In the equal V_{bg} condition, an opposite voltage is applied on NMOS and PMOS ($V_{bn} = -V_{bp}$), whereas for the equal V_{th}, V_{bp} is tuned according to V_{bn} in order to obtain $V_{th}(NMOS) = V_{th}(PMOS)$

In order to find the operating point of minimal power consumption, the same work has been carried at low I_{bias}. The minimal I_{bias} providing a bandwidth of 4.3kHz limited by the feedback network is equal to 4.10^{-7}A at 300K and 1.10^{-7}A at 90K. Therefore, the evolution of the impact of V_{bg} on VDD_{min} when decreasing I_{bias} is studied from $I_{bias} = 10\mu$A to 10nA. The evolution of VDD_{min} with I_{bias} is shown in fig. 3.22 in Appendix 2.

At the lowest biasing current $I_{bias} = 10$nA, VDD_{min} is reduced for all back-gate voltage compared to the high I_{bias} case. At T=90K, the minimal value obtained at $V_{bg} = 4$V is $VDD_{min} = 0.33$V. The minimal power consumption $P_{min} = VDD_{min} \times I_{bias,min}$ can finally be estimated to be $P_{min} = 0.33\text{V} \times 10^{-7}\text{A} = 33$nW. Considering that, at zero back-gate voltage and T= 90 K, VDD_{min} is increased to 0.8V while I_{bias} is unchanged, the minimal power at $V_{bg} = 0$V is $P_{min} = 80$nW. Finally, the back-gate allows a reduction of 69% of the minimal power consumption of the TIA.

Moreover, it has been demonstrated that the entirety of the influence of the Back-gate voltage on power reduction comes from the reduction VDD_{min}, as no influence on $I_{bias,min}$ was observed.

3.3 Experimental results

For the experimental characterization of the TIA, the pins of the TIA was connected to the various instruments by using a matrix box, as shown in Appendix 3 fig. 3.23. A multi-channel DC voltage source (DAC) is used to apply the DC voltages necessary to perform the tests on the TIA. Current measurements are performed using a pico-amperemeter (measuring currents in the range of 1 pA to 10mA), and DC voltage measurements are performed using a voltmeter (cf fig. 3.10). As detailed later, a Lock-In amplifier is used for the AC measurement both to apply the AC signal to the TIA and to perform the measurement of the AC output voltage of the TIA (cf fig. 3.11). To characterize its performance at cryogenic temperature, the circuit was placed in a container filled with liquid nitrogen at T = 77K.

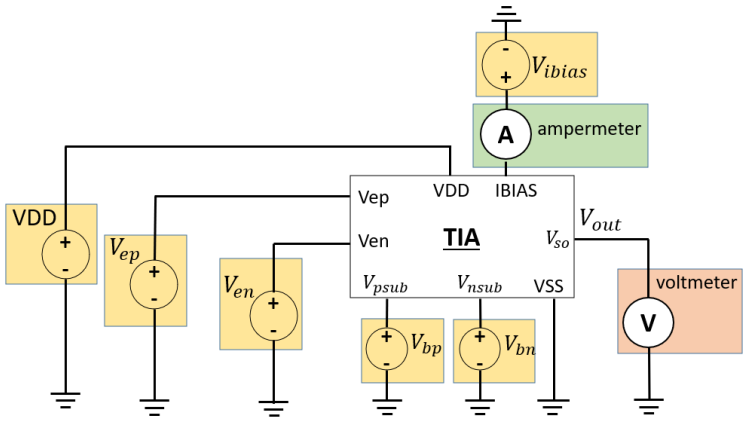

Figure 3.10: Schematic of the setup used for the DC characterization of the TIA. The VDD (supply voltage), IBIAS (biasing current), Vep, Ven (TIA inputs), Vbsub, Vnsub (NMOS and PMOS back-gate) pins are all controlled by a multi-channel DC voltage source (yellow). instead of controlling the biasing current I_{bias} directly by applying a current on the IBIAS pin, it is controlled by the voltage applied using the DC source. An amperemeter (green) is used to measure the corresponding value of I_{bias}. The output voltage V_{out} is measured with a voltmeter (red).

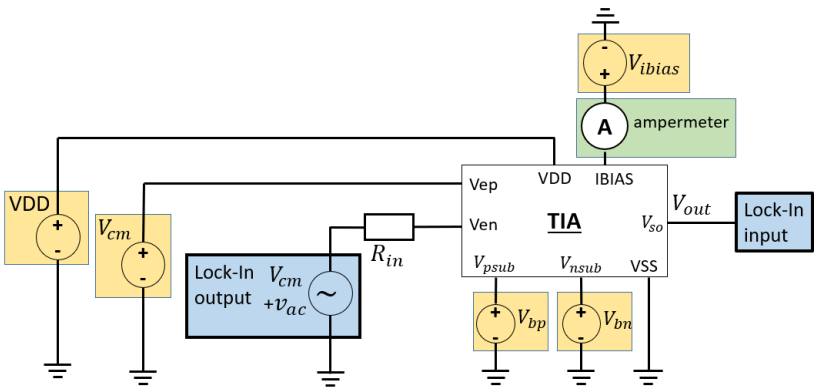

Figure 3.11: Schematic of the setup used for the AC characterization of the TIA. The VDD (supply voltage), IBIAS (biasing current), Vep (positive input), Vbsub, Vnsub (NMOS and PMOS back-gate) pins are all controlled by a multi-channel DC voltage source (yellow). The Ven pin is connected to the output of a Lock-In amplifier (blue), which is used to apply an AC voltage of amplitude 10mV on the Ven input. The signal is converted in a AC current of 10nA amplitude by the input resistance $R_{in} = 1\text{M}\Omega$. The output signal V_{out} is connected to the Lock-In amplifier input, which performs the demodulation of the V_{out} signal to allow precise measurement of low amplitude signals.

3.3.1 DC characterization of the TIA

Follower range

To obtain a correct amplification and Bandwidth, the transistors of the TIA must operate in Strong Inversion regime. Therefore, the common mode voltage V_{cm} at the inputs must be chosen so that $V_{gs} > V_{th}$ for the transistors composing the TIA. As V_{th} increases with temperature, the acceptable range of V_{cm} is reduced. In order to measure this range, the TIA is connected in Follower mode, meaning that the input VEN is disconnected. A DC voltage V_{cm} is applied on VEP and will be copied on the output VSO as long as the biasing point of the transistors defined by V_{cm} is correct.

According to fig. 3.12, the reduction of the range of V_{cm} allowing a correct polarization of the differential pair at the input from [0.22V ; 0.84V] at 300K to [0.5V ; 0.88V] at 90K is mostly due to a increase of V_{min} (where V_{min} is defined as the minimum value of V_{cm} allowing a correct operation of the TIA as a follower, corresponding also to a correct polarization of the differential pair). This comes from the condition $V_{gs,N1} > V_{th,NMOS}$ necessary for a correct operation of the differential pair and defining the value of V_{min}. Therefore, increasing the back-gate voltage $V_{bg} = V_{bn} = -V_{bp}$ should reduce the value of V_{min} and increase the working range of the follower. This is confirmed by the experiment, and V_{min} is reduced by around 0.1V per volt applied on V_{bn} which is close to the reduction of $V_{th,NMOS}$ with V_{bn}. The maximal range obtained for $V_{bn} = -V_{bp} = 4\text{V}$ is of $V_{cm} \in [0.10V; 0.92V]$, this is even better than the V_{cm} range at 300K. Finally, it has been demonstrated that the back-gate can be used to compensate the reduction of V_{cm} range with temperature.

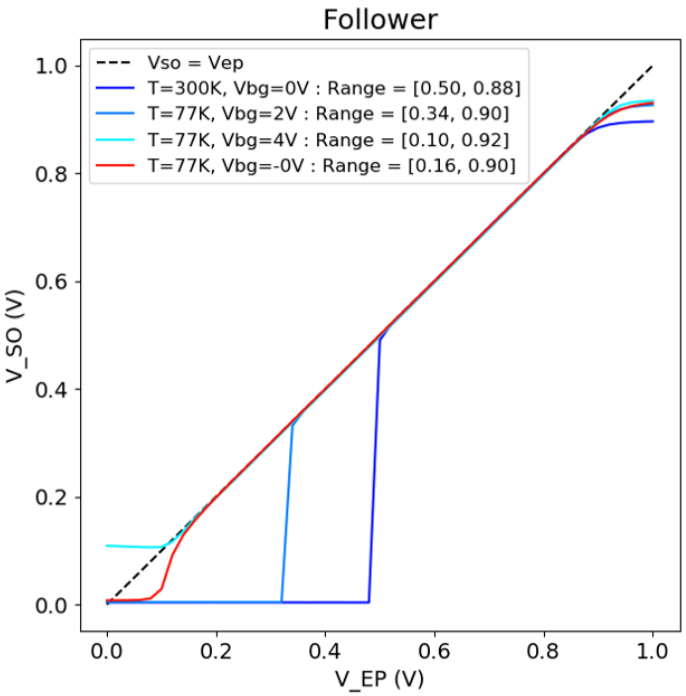

Figure 3.12: Output voltage V_SO as a function of input voltage V_EP for the TIA operating as a follower at T=300K and T=77K for V_{bg} = 0, 2 and 4V, and the corresponding acceptable range of V_{cm}. The black dashed line represent the value of VSO for a correct operation of the follower.

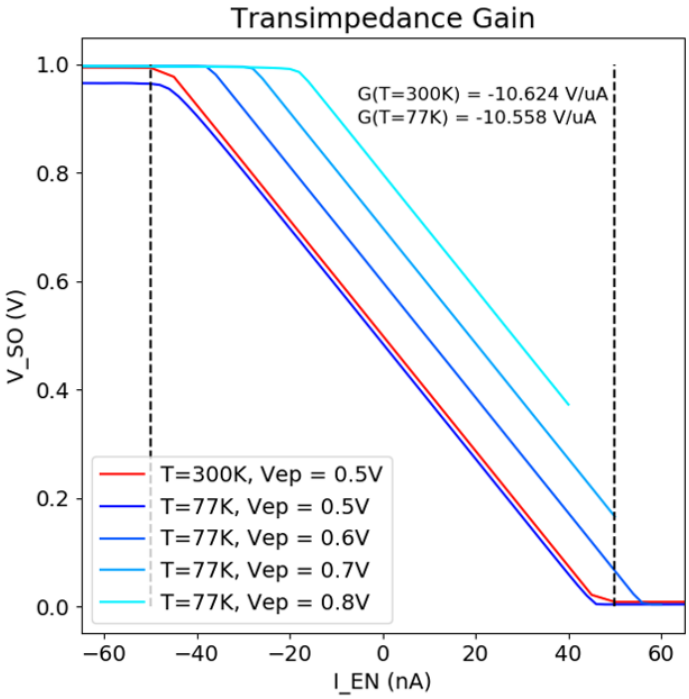

Figure 3.13: Output voltage V_SO at T=300K and T=77K, as a function of the input current I_EN at different common mode voltage V_{cm} applied on V_EP. The calculated trans-impedance gain G is shown for T = 300 and 90K. The black dashed lines are placed at symmetric values of I_EN = ± 50nA.

Impedance gain

In DC mode, the gain of the TIA, defined as $G = \frac{\partial V_{out}}{\partial I_{in}}$, depends only on the feedback resistance: $G = R_{fb}$. This is true as long as the output V_{out} is not saturated, which limits the current range. The gain and current input range of the TIA. The voltage VEN is swept between 0V and 1V, and the output VSO is measured by the multi-meter, while the common mode voltage on VEP is kept constant at VDD/2=0.5V. The result is shown in fig. 3.13 at 300K and 77K.

A small variation of G between 300K and 77K is observed and can be explained by a variation of the resistance R_{fb} with temperature of around 5% (as developed in [ref loick tia]). The center of the input range is defined by the common mode V_{cm}. At T=300K, it is set at $V_{cm} = VDD/2 = 0.5$V, inducing a symmetric input range for I_{in} between -45nA and +45nA. Nonetheless, at T=77K, $V_{cm} = 0.5$V is at the limit of the follower range, so that V_{cm} must be increased to 0.6V to achieve an output range from 0V to 1V. This in turn shifts the input range from -55nA t o+35nA. To obtain a symmetric input range at 77K, a correct operation at $V_{cm} = 0.5$V can be obtained by imposing a positive back-gate voltage.

3.3.2 AC characterization of the TIA

TIA Bandwidth

Now that the DC mode of the TIA has been studied, a correct DC operating point can be chosen to perform the AC characterization. To study the frequency behavior of the circuit, the Lock-In amplifier sends a signal of given frequency to the VEN input of the TIA, the output signal VSO is sent back to the Lock-In which performs the demodulation of the signal. This technique allows precise measurement of low amplitude signals in noisy environment.

In order to generate an AC current at the VEN input, a resistance $R_{in} = 1M\Omega$ is connected to VEN, and an AC voltage is applied on its terminal using the Lock-In amplifier (cf. fig. 3.11). As $V_{en} = V_{ep}$, the amplitude of the current applied at the input of the TIA is: $i_{in} = \frac{v_{in}}{R_{in}}$. Considering the resistance R_{in} at the VEN input, the circuit now behaves as an inverting amplifier. For R_{in} = 200kHz, the DC gain and Bandwidth, when not limited by the OP-AMP, are: $G = \frac{v_{out}}{v_{in}} = \frac{R_{fb}}{R_{in}} = 50 = 34\text{dB}$ and $BW = \frac{1}{2.\pi.R_{fb}.C_{fb}} = 4.29\text{kHz}$. Therefore, the transfer function should contain two cutoff frequencies, one stable defined by $R_{fb}//C_{fb}$, the other coming from the finite Bandwidth of the OP-AMP and depending on the biasing current. To obtain the transfer function of the circuit in this mode, the gain and phase are extracted along a frequency sweep done from 10Hz to 500kHz (highest frequency achieved by the Lock-In). An example is shown in fig. 3.14 at $VDD = 1\text{V}$, $V_{bg} = 0\text{V}$, $V_{cm} = 0.5\text{V}$ and T=300K at $I_{bias} = 10\mu\text{A}$.

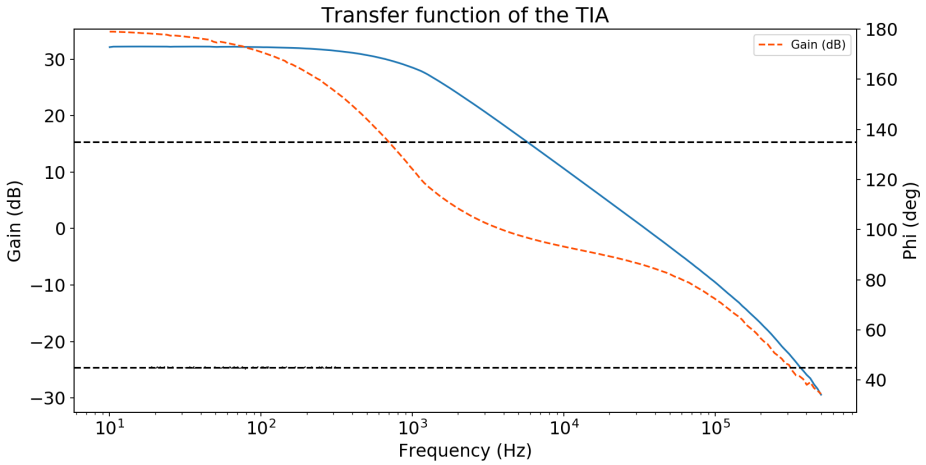

Figure 3.14: Transfer function of the TIA at T = 77K, $I_{bias} = 10\mu\text{A}$, VDD=1V and $V_{cm} = 0.6\text{V}$. The dashed lines shows the respective values for the phase at which the two cut-off frequencies are extracted.

From each frequency sweep, the DC gain is extracted at the frequency of 10Hz, and the two cutoff frequencies are defined as the frequencies for which the phase is equal to 180-45=135 degrees and 90-45=45 degrees. The DC gain and cutoff frequencies are finally extracted for different values of I_{bias} from 0.1nA to 100μA.

The plot of the cut-off frequencies shows two different regime. At high I_{bias}, the cut-off frequency of the OP-AMP is higher than the one of the Feedback network. Thus, the Bandwidth of the TIA (defined by the lowest cut-off frequency measured in the inverting amplifier mode) is limited by the Feedback network. This frequency is theoretically equal to 4.29kHz, nonetheless

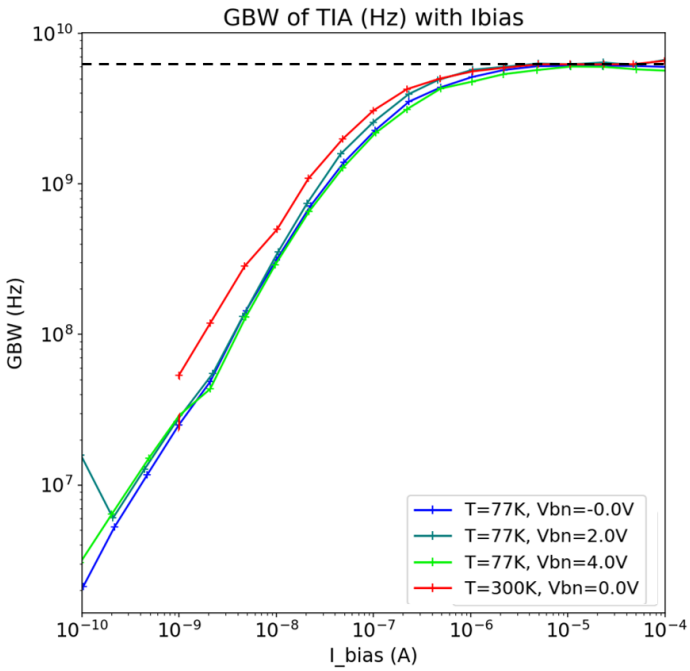

Figure 3.15: Evolution of the GBW of the TIA. The black dashed line indicates the maximal value of GBW defined by the feedback network. GBW is measured for $V_{bg} = 0, 2$**and**4V and T=77K and at T=300K.

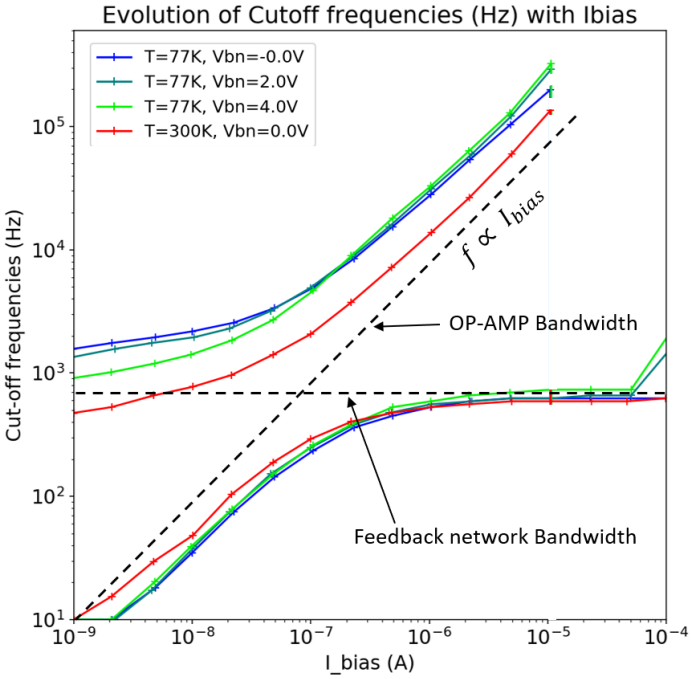

Figure 3.16: Evolution of the 2 cut-off frequencies extracted from the transfer function plot at Phi = 135 degrees and Phi = 45 degrees. The black dashed lines indicate the values of cut-off frequencies of the Feedback network (constant) and of the OP-AMP (proportional to I_{bias}, diagonal). The results are given for $V_{bg} = 0, 2$**and**4V and T=77K and at T=300K.

the experiment indicate a lower value around 0.8kHz, this can be attributed to variations in the value of the capacitance C_{fb}. The cut-off frequency of the OP-AMP decreases linearly with decreasing I_{bias}, and drops under the Feedback network cut-off frequency at $I_{bias} < 1\mu$A at T=77K. In this regime, the Bandwidth of the TIA is limited by the OP-AMP and decreases with I_{bias}. As can be seen in fig. 3.16, changing the back-gate voltage from $V_{bg} = 0$V to $V_{bg} = 4$V gives the same results in term of DC gain and cut-off frequencies, confirming the results obtained in the simulations.

VDD reduction

To find the minimal operating point of the TIA, the effect of back-gate voltage on VDD reduction is now studied and compared to the simulations. A frequency sweep is performed for different values of VDD between 0.75V down to 0.55V. In the simulations, the common mode voltage V_{cm} was kept to 0.6*VDD to ensure a correct biasing in all conditions. Nonetheless, this was not possible for the experiment, V_{cm} was therefore set to be just above the minimal value of follower range V_{min} (depending on V_{bg} and Temperature).

As in the simulations, DC gain and Bandwidth stay constant until an abrupt change of

the DC gain is visible when VDD becomes too low. The minimal VDD is characterized by the minimum value giving the correct DC gain, i.e. defined as $\frac{R_{fb}}{R_{in}} = 10 = 20\text{dB}$. To study the influence of the back-gate on VDD reduction at T=77K, the DC gain is measured along a 2 dimensional sweep is performed on VDD (step 0.5V) and V_{bg} (step 0.5V). The result at $I_{bias} = 10\mu\text{A}$ is shown on fig. 3.17. From this plot, VDD_{min} is extracted as a function of the back-gate voltage V_{bg} (where $V_{bg} = V_{bn} = -V_{bp}$). Fig. 3.18 shows the result at both high (10μA) and low (10nA) I_{bias}.

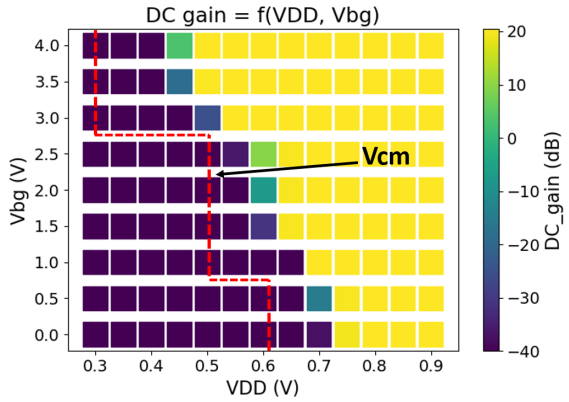

Figure 3.17: DC gain in the inverting amplifier mode (extracted as the gain (dB) at a frequency of 10Hz) for a 2D sweep along VDD (step 0.05V) and along V_{bg} (step 0.5V). Sweep made at $I_{bias} = 10\mu$A and T=77K. The red line represent the value of V_{cm} which was tuned with V_{bg}

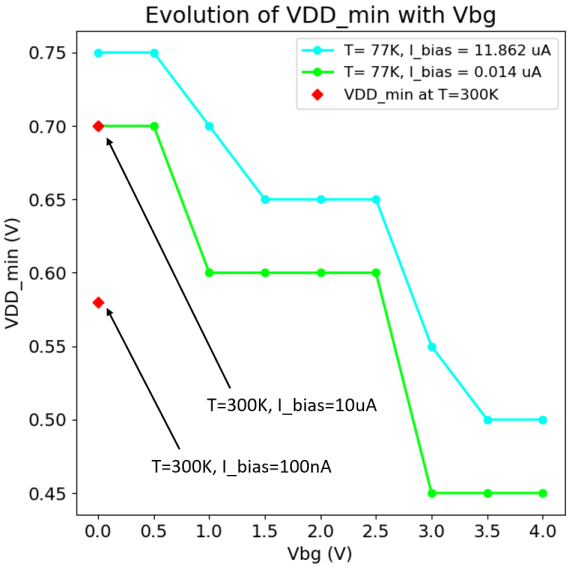

Figure 3.18: Effect of V_{bg} on VDD_{min} where VDD_{min} is extracted from fig. 3.17 as the minimum VDD for which DC gain = 20dB. V_{bg} sweep is performed at $I_{bias} = 10\mu$A and 10nA at 77K. Red squares indicate VDD_{min} at 300K for $V_{bg} = 0$V.

At high I_{bias}, the maximum applicable Back-gate voltage $V_{bg} = 4$V induces a reduction of VDD_{min} of 0.25V (from $VDD_{min} = 0.75$V at $V_{bg} = 0$V to $VDD_{min} = 0.5$V at $V_{bg} = 4$V). At low I_{bias}, VDD_{min} is reduced by around 0.25V for all values of V_{bg}, reaching 0.45V for $V_{bg} = 4$V.

A plateau can be observed in the region where $V_{cm} = 0.5$V, and VDD_{min} decreases abruptly when V_{cm} is changed to 0.3V. This could indicate that the minimum value of VDD is limited by $V_{cm} = 0.5$V applied at the input rather than the threshold voltage of transistors in the circuit in this region. Nonetheless, at $V_{bg} = 4$V, $V_{cm} = 0.3$V is low enough compared to the minimum VDD obtained (0.45V at low I_{bias}), so that the total reduction of VDD_{min} from $V_{bg} = 0$V to $V_{bg} = 4$V is not affected by V_{cm}.

In conclusion, at 77K, the Back-gate allows a significant reduction of VDD and results in a reduction of the power consumption of 35% when the maximum value $V_{bg} = 4$V is applied. This is nonetheless lower than the reduction of 69% predicted by the simulations.

Characterization of the Noise

The TIA is the first block of the measurement chain (as presented in Chapter 1) and is placed right after the qubit, and is therefore the block that will limit the Signal to Noise Ratio (SNR) of the whole measurement chain. The noise of a signal can be characterized by its Power Spectral Density (PSD)in W/Hz, representing the power distribution of the signal along the frequency spectrum. Physically, two main sources of noise can be identified in most of electronic components:

- Flicker Noise: also called '1/f noise', it exhibits a $1/f^{\alpha}$ power spectral density, where α is close to 1. It is the dominant source of noise at low to moderate frequencies, and becomes negligible against thermal noise at higher frequencies.
- Thermal Noise: comes from the random thermal motion of charge carriers in the channel. Its power spectral density is constant for all the frequency spectrum (i.e. it is a white noise).

To obtain a value easily comparable to a voltage, the noise is here characterized by the square root of the PSD, called the Voltage Spectral Density (VSD) in $V/\sqrt{Hz}$. In order to characterize the noise of the TIA, the output of the Lock-in is connected to the VEN input of the TIA without imposing any signal, and the output of the TIA VSO is sent back to the Lock-In. Before carrying out the measurement on the operating TIA, the noise coming from the instruments, wires and power supplies, referred as 'Base-band noise', is characterized by measuring the noise when the TIA is not powered. The noise VSD of the operating TIA is then measured. Results are presented at different temperatures in fig. 3.19 and for different Back-gate voltage at 77K in fig. 3.20.

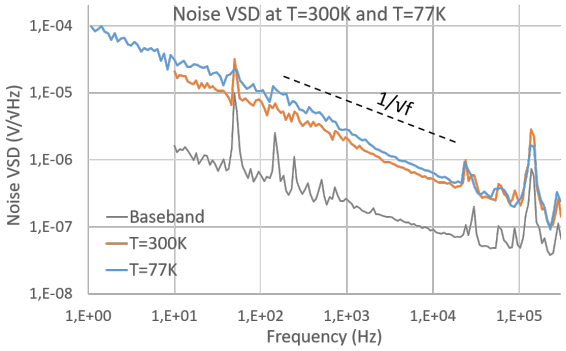

Figure 3.19: Noise expressed as Voltage Spectral Density (VSD) at the output V_SO of the TIA at T = 300K and T = 77K. The Base-band (i.e. the VSD coming from the setup without considering the TIA) is also shown (grey curve).

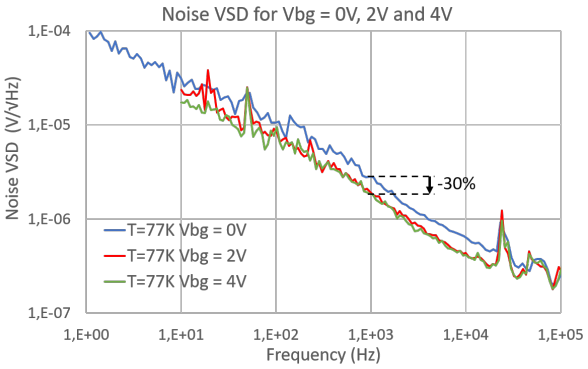

Figure 3.20: Voltage Spectral Density (VSD) at the output V_SO of the TIA for different values of the back-gate voltage V_{bg} = 0V, 2V and 4V at low temperature.

The noise VSD exhibits a $1/f^{\alpha}$ dependence with respect to frequency where α is close to 1/2, characteristic of a Flicker noise (for which VSD has a $1/f^{1/2}$ dependence). Due to the Lock-In frequency being limited to 500kHz, the region of dominance of Thermal noise over Flicker noise at high frequencies is not observed, and the evolution of Thermal noise with temperature could not be studied. When decreasing the temperature from 300K to 77K, a small increase of the noise VSD is observed. As the thermal noise is predicted to decrease at 77K, this comes from an increase of the Flicker noise.

According to fig. 3.20, when a positive back-gate $V_{bg} = 2$V is applied at 77K, the noise is reduced by approximately 30%. This can be explained by the fact that a positive voltage V_{bg} tends to attract the electrons towards the back-gate, moving the conductive channel away from the oxide/semiconductor interface. This in turn reduces surface scattering of the electrons, which contributes to the noise, and therefore reduces the total noise. No further improvement is observed for $V_{bg} = 4$V, implying that applying +2V on the back-gate is enough to completely move the channel away from the oxide interface.

To confirm this explanation, it is of interest to reduce the contribution of other sources of noise. For Thermal noise, this could be achieved by studying the noise at deep cryogenic temperature (4.2K). In this case, as the contribution of surface scattering to the total noise should increase, the effect of a positive V_{bg} should be enhanced.

Conclusion

The characterization of the Trans-impedance Amplifier (TIA) has been conducted at cryogenic temperatures in the conditions required in the context of the read-out of a spin quantum bit. First, the general principles of silicon spin qubits for quantum computing were presented. The advantages of implementing the qubit control electronics close to the qubit core operating at low cryogenic ($\approx$ 100mK) temperature was discussed . This pointed out the necessity to operate the TIA, measuring the current of a qubit device to perform the read-out of its quantum state, at low temperature and low power consumption rather than at room temperature. The interest of fabricating the circuit on the Fully-Depleted Silicon-on-Insulator (FDSOI) technology was also discussed.

The influence of cryogenic temperatures on single transistors was studied. The main effect of a decreasing temperature are the increase of the threshold voltage V_{th} and the reduction of the Sub-threshold Slope SS in the electrical characteristic of transistor. The ability to compensate the increase of the threshold voltage by tuning the back-gate voltage V_{bg} available when the transistors are implemented in the FDSOI technology was demonstrated experimentally for decreasing temperatures from 300K down to 77K. Moreover, the transistor characteristic were simulated using Cadence Virtuoso software. A good agreement between the experimental and simulation results was found concerning the dependence of V_{th} with respect to the temperature and V_{bg}.

Finally, the TIA was characterized both in simulations and experiments. The bandwidth of the TIA was studied given that it limits the maximum frequency at which the measurement of the qubit state can be performed. As the TIA is the first block of the measurement chain connected to the quantum device, this block sets the maximal Signal-to-Noise Ratio achievable, it is also the block with the highest power consumption. Therefore, the noise and the power consumption of the TIA were measured. The evolution of the bandwidth and power consumption of the TIA with respect to temperature and V_{gb} was studied.

The evolution of these parameters with temperature and back-gate voltage was first studied by simulations at 300K and 90K. This allowed to predict eventual improvements when a back-gate voltage is applied. At 90K, no improvement of the bandwidth is shown, whereas a reduction of the power consumption of 69% is predicted.

The experimental characterization of the TIA was then performed at 300K and 77K. A preliminary DC analysis allowed to find a correct operating point for the AC analysis, and also showed an increase of the common mode V_{cm} range at 77K when increasing the back-gate voltage from 0 to 4V. At the temperature of 77K, applying a back-gate voltage of +4V resulted in a reduction of 35 % of the power consumption thanks to a reduction of the minimal voltage supply VDD allowing a correct operation of the TIA. A reduction of approximately 30% of the noise (when expressed as a Voltage Spectral Density) was also observed. Further simulations would be necessary in order to understand the different results obtained in simulation compared to the experiments concerning the reduction of the supply voltage VDD.

For qubit operation, the TIA circuit would be placed at a temperature of 4.2K or even lower, closer to the temperature of the qubit core. Therefore, it would be of interest to study the influence of the back-gate on the performance of the TIA at such low temperatures. Experiments need to be performed in order to complement the transistor modelisation, which does not exist below 90K.

The Gantt chart illustrating the different tasks completed during the internship and their advancement in time is presented in Fig.3.21. A cost estimate of the internship is given in Table 3.1.

Table 3.1: Estimated cost of the internship

Type	**Item**	**Cost (EUR)**	Percentage
Instrument	Lock-in amplifier	5500	10%
	Multi channel DC power source	431	10%
	Pico amperemeter	2530	10%
TIA chip	CRYA project	48 000	2%
	packaging	1300	2%
	PCB chip	2500	2%
Consumables	Liquid nitrogen	200	100%
Software	Cadence virtuoso license	42 500	
Student	Retribution	7900	100%
	Total		9200

The design and characterization of the TIA circuit studied in this work is a part of the CRYA project including various quantum devices and control electronics. The manufacturing cost of the whole project is estimated around 48,000 euros. The price of the Cadence Virtuoso license is confidential, so an estimation is given and is not taken into account in the the total cost estimate of the internship.

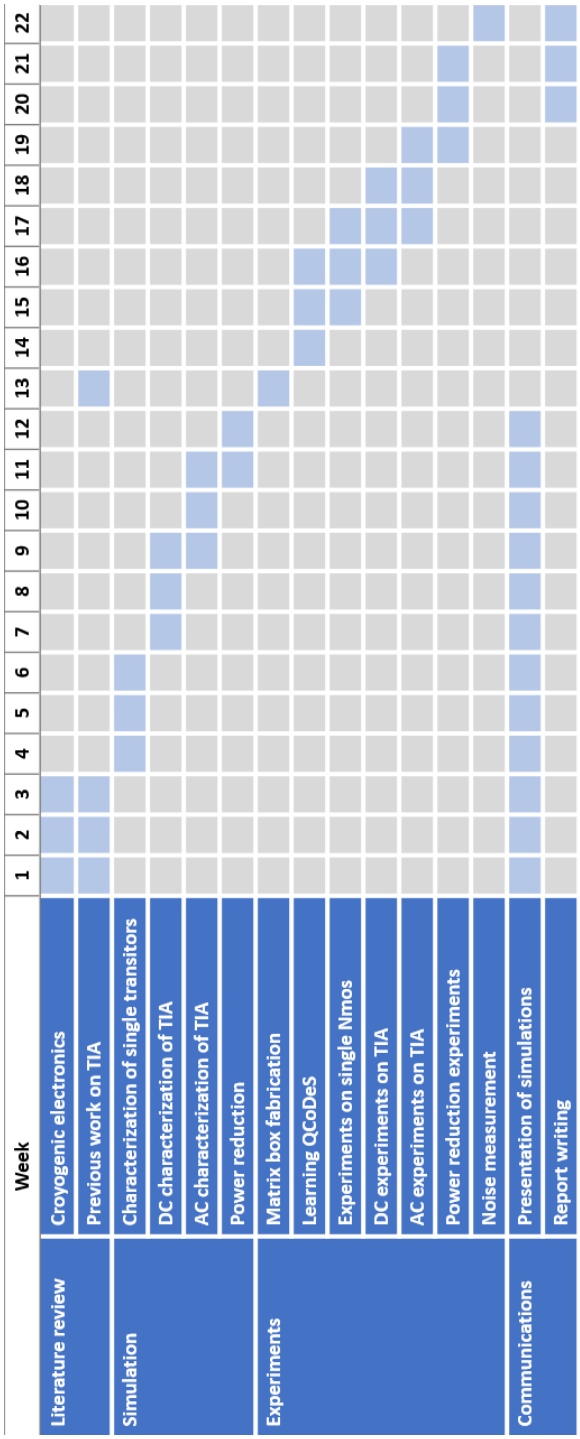

Figure 3.21: Gantt chart illustrating the different tasks completed during the internship and their advancement in time. The internship took place as remote work from week 1 to 12, and at the CEA/IRIG laboratory from week 13 to week 22.

Acknowledgment

I would first like to express my sincere gratitude to my supervisor Louis JANSEN (LATEQS) for giving me the opportunity to realise my Master Thesis project in the LATEQS group. He provided me a good guidance throughout this internship and and gave me an excellent support during the period when I was working at distance as well as during the time when I was carrying out the experiments at the LATEQS.

I also thank my supervisor Adrien MOREL (LETI), who also helped me to carry out the simulations during my work at distance and gave me some guidelines to conduct the experiments and useful advice for the writing of the report.

I also address a special thank to Loïck Leguevel, PhD student at the LETI, for helping me to carry out the experiments and for showing me how to use the QCoDeS library for the control of the instruments.

Although my time spent in the laboratory was short, I would like to thank as well all the LATEQS team for their involvement and their support. I especially thank Xavier JEHL for his support and his advice and François Lefloch, director of the LATEQS laboratory. My thanks also goes to the other students of the laboratory for their motivation and their kindness.

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Appendices

3.4 Appendix 1

Table 3.2: Expression of I_d, g_m and g_{ds} for the different regime of operation of a MOSFET transistor

Regime	Weak Inv.	Strong Inv. Triode	Strong Inv. Saturation
Condition	$V_{gs} < V_{th}$	$V_{gs} > V_{th}$ $V_{ds} < V_{gs} - V_{th}$	$V_{gs} > V_{th}$ $V_{ds} > V_{gs} - V_{th}$
I_d	$I_s.e^{\frac{V_{gs}}{\epsilon.U_t}}.(1 - e^{\frac{-V_{ds}}{U_t}})$	$\beta.[(V_{gs} - V_{th}).V_{ds} - \frac{V_{ds}^2}{2}]$	$\frac{\beta}{2}.(V_{gs} - V_{th})^2.(1 + \lambda.V_{ds})$
g_m	$g_m = \frac{I_s}{\epsilon.U_t}.e^{\frac{V_{gs}}{\epsilon.U_t}}$ $\approx \frac{I_d}{\epsilon.U_t}$ $(V_{ds} >> U_t)$	$g_m = \beta.V_{ds}$	$g_m = \beta.(V_{gs} - V_{th})$ $= \sqrt{2.\beta.I_d}$ $= \frac{2.I_d}{V_{gs} - V_{th}}$
g_{ds}	$g_{ds} = \frac{I_s}{U_t}.e^{\frac{V_{gs}}{\epsilon.U_t}}.e^{\frac{-V_{ds}}{U_t}}$ $\approx \frac{I_d}{U_t}.e^{\frac{-V_{ds}}{U_t}}$ $(V_{ds} >> U_t)$	$g_{ds} = \beta.[(V_{gs} - V_{th}) - V_{ds}]$	$g_{ds} = \frac{\beta}{2}.(V_{gs} - Vth)^2.\lambda$ $\approx I_d.\lambda$

In table 3.2, g_m is defined as $g_m = \frac{\partial I_d}{\partial V_{gs}}$ and g_{ds} as $g_{ds} = \frac{\partial I_d}{\partial V_{ds}}$.

In the Weak Inversion regime, I_s is defined as the drain-source current I_d at $V_{gs} = V_{ds} = 0$V. The expression of g_m is given considering $(1 - e^{\frac{-V_{ds}}{U_t}}) \approx 1$, which is true for $V_{ds} >> U_t$ where $U_t = \frac{k_B T}{q} = 25$mV at T = 300K and 83mV at T = 90K.

In the Strong Inversion regime, the parameter λ represents the small increases of I_d with increasing V_{ds} in the saturation region. This effect, called the channel length modulation, is known to be stronger in short-channel devices. The transistors used in this work are long channel transistors (L¿300nm), so this effect is neglected in the expression of I_d used in Chapter 2.

3.5 Appendix 2

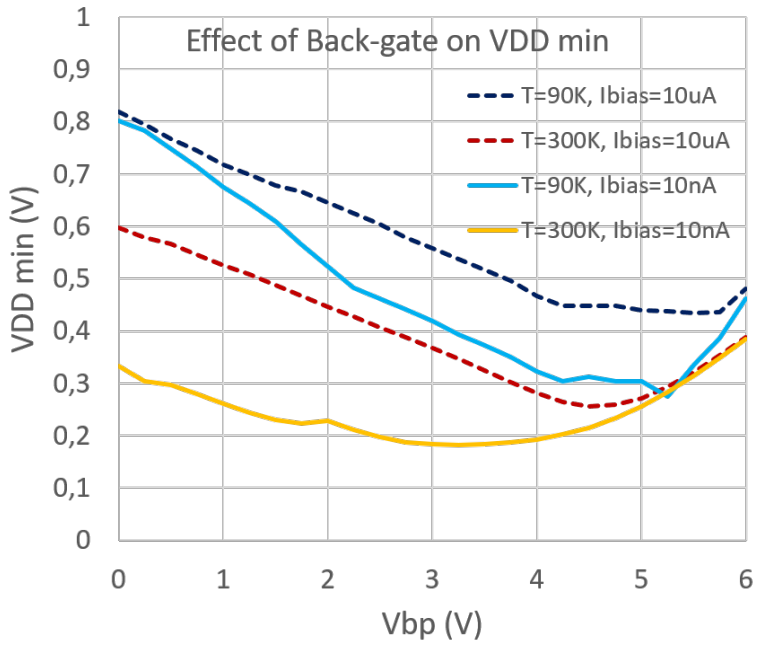

Figure 3.22: Comparison of the minimum supply voltage VDD_{min} providing a correct DC gain of +20dB as a function of the V_{bp} at high I_{bias} (10μA) and low I_{bias} (10nA). The simulations is performed at T = 300K and T = 90K. An opposite back-gate voltage is applied on NMOS and PMOS ($V_{bn} = -V_{bp}$).

Fig. 3.22 shows a comparison of VDD_{min} calculated by simulations at high I_{bias} (10μA) and low I_{bias} (10nA).
At T = 300K, the VDD_{min} found at V_{bg} = 0V is strongly reduced from 0.6V to 0.33V when I_{bias} is decreased from 10μA to 10nA. This result in a smaller influence of the back-gate voltage on the VDD_{min} reduction. At high I_{bias}, increasing V_{bg} from 0 to 4V results in a decrease of 0.31V on VDD_{min} from 0.6V to 0.29V. The same increase of V_{bg} at low I_{bias} results in a smaller decrease of 0.13V on VDD_{min}.
At T = 90K, VDD_{min} is around 0.81V for both high and low I_{bias}. The reduction of VDD_{min} with V_{bg} is stronger at I_{bias} = 10nA. At I_{bias} = 10μA, increasing V_{bg} from 0 to 4V decreases VDD_{min} from 0.82V to 0.46V. The same increase of V_{bg} at I_{bias} = 10nA results in a decrease of 0.47V on VDD_{min} from 0.8V to 0.33V. This strong reduction on VDD_{min} at low temperature and low I_{bias} allows a significant reduction of the power consumption of the TIA, as discussed in Chapter 3.

3.6 Appendix 3

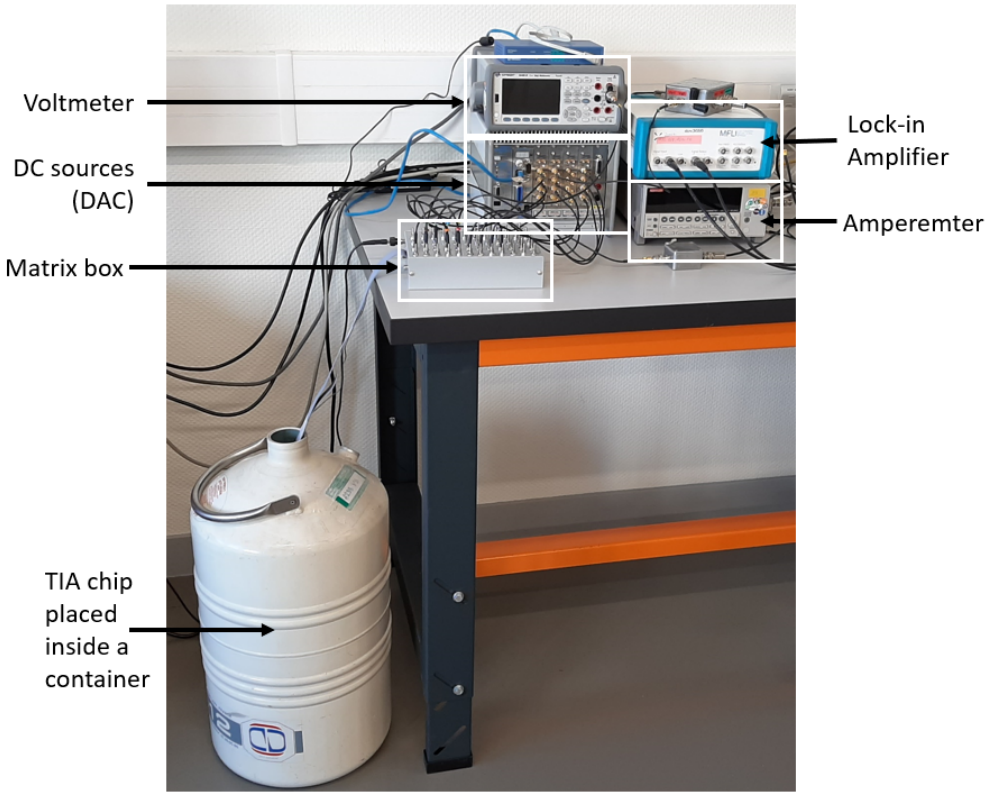

Figure 3.23: Photo of the experimental setup used for the characterization of the TIA circuit and the the diode connected NMOS. The amperemeter, voltmeter, multi-channel DC source (DAC) are connected to a matrix box (fabricated during the internship), itself connected to the TIA circuit by a 51D connector. The TIA chip mounted on a PCB is placed in a container filled with liquid nitrogen to perform the tests at the temperature of 77K.

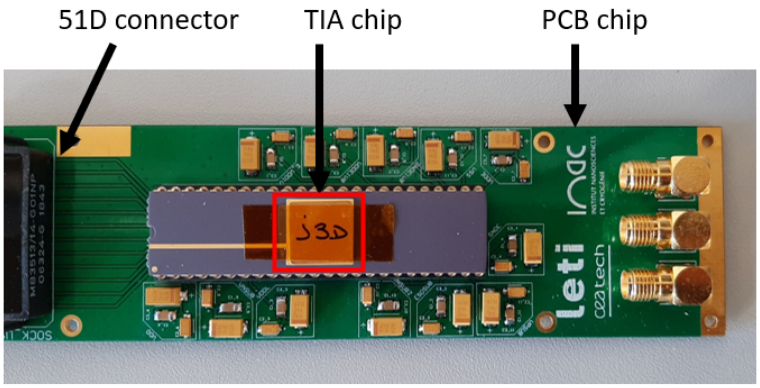

Figure 3.24: Detail of the TIA chip mounted on a PCB chip.