

MASTER THESIS REPORT

in partial fulfillment of
The Degree of Master of Science
in Micro and Nanotechnologies for IC
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Acquisition path for IoT applications: Design of an ADC

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Confidential

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Abstract

English version:

This master thesis is about designing an analog to digital convertor ADC based on TSMC 22 nm Ultra Low Leakage ULL technology, dedicated to IoT applications. The general context of this project is to replace the externally made ADC in the Dolphin's testbench to connect 16 different sensors to the newly launched IPs by the French company. SAR is the most adequate architecture that fits the required specifications, for instance it has 12 bit resolution, medium sampling rate between 1 and 2 MS/s and ultra low power consumption.

The main building blocks of this selected circuit are a DAC, a comparator and a logic block.
An efficient switching scheme controlled by the logic unit allows to use this same circuit to convert both single ended and differential sensors signals without using an extra preamplifier.
The common architecture is based on a dynamic latched comparator with high sensitivity and consuming only 117.64 nW.
The DAC is based on a differential capacitive circuit formed by the combination of 3-bit C-2C array for the LSB and 9-bit binary weighted capacitors for the MSB. It creates the successive threshold voltages $\frac{VDD}{2^i}$ with extremely reduced power consumption compared to available circuits.
The designed convertor fits the specifications required by IoT applications by providing 12 bit data at 1.4 MS/s. The prelayout design consumes less than 400 nW approaching the state of the art performances in terms of Figures of Merit (FoM) with its 0.2 fJ/c-s as FoMw and 194 dB as FoMs.

Abstract

French version:

L'objet de ce projet de fin d'étude est de réaliser le design d'un convertisseur analogique numérique CAN destiné aux applications ≪ Internet des Objets ≫ basé sur la technologie TSMC 22 nm ULL. Le contexte global du projet est de remplacer le convertisseur fourni par d'autres fournisseurs dans le banc de test des nouvelles IPs afin de convertir les données analogiques de 16 différents capteurs. SAR ADC est l'architecture la plus compatible avec les spécifications. En effet, le circuit a une résolution de 12 bits, un taux d'échantillonnage moyen compris entre 1 et 2 MS/s et consomme le minimum possible d'énergie.

Le convertisseur est essentiellement constitué d'un comparateur, un convertisseur numérique analogique CNA et une partie de contrôle logique.
Un réseau d'interrupteurs bien synchronisé et contrôlé par la partie logique permet au même circuit de convertir convenablement des signaux de capteurs de types différentiel et single-ended à la fois, sans avoir recours à un préamplificateur. Le comparateur est un circuit à verrouillage dynamique de haute sensibilité et ne consomme que 117.64 nW.
Quant 'au CNA, il est formé d'une combinaison d'un réseau C-2C de 3-bit pour le LSB et un réseau de 9 capacités dimensionnées en mode binaire pour les MSB. Son rôle et de générer les niveaux de voltage successives $\frac{VDD}{2^i}$ à partir du signal de référence avec une très faible consommation. Ensuite, la différence des signaux d'entrées est comparée à chaque étape de conversion, à ces niveaux dans le

cadre de l'algorithme SAR pour fournir le code numérique correspondant.
Le circuit réalisé répond aux spécifications en terme de résolution et rapidité avec un taux d'échantillonnage de 1.4 MS/s. Dans cette étape de pré-layout, les blocks assemblés consomment moins de 400 nW à l'état actif ce qui permet au circuit d'avoir une place considérable parmi les circuits de l'état de l'art suite à ses performances remarquables. En effet, il atteint des valeurs de 0.2 fJ/c-s pour la figure de Merit de Walden et 194 dB pour la figure de Merit de Schreier.

Abstract

Italian version:

Questa tesi di laurea riguarda la progettazione di un convertitore analogico-digitale ADC basato su tecnologia TSMC 22 nm ULL (Ultra Low Leakage), dedicata alle applicazioni IoT. Il contesto generale di questo progetto è sostituire l'ADC realizzato esternamente nel banco di prova di Dolphin per collegare 16 diversi sensori alla nuova IP, lanciata dalla società francese. SAR è l'architettura più adeguata alle specifiche richieste, ad esempio, ha una risoluzione a 12 bit, una frequenza di campionamento media tra 1 e 2 MS / s e un ultra basso consumo energetico - raggiungendo meno di 400 nW per conversione.

In oltre è considerata una delle architetture più avanzate in termini di figure di merito FoM con 0.2 FJ / C-S FoMw e 194 DB FoMs. I principali elementi costitutivi del circuito selezionato sono un DAC, un comparatore e un blocco logico. Un efficiente schema di commutazione controllato dall'unità logica consente di utilizzare questo circuito per convertire entrambi i segnali dei sensori single ended e differenziali senza l'utilizzo di un preamplificatore aggiuntivo.

L'architettura comune si basa su un comparatore dinamico a latch ad alta sensibilità che consuma solo 117.64 nW. Il DAC si basa su un circuito capacitivo differenziale formato dalla combinazione di array C- 2C a 3 bit per gli LSB e di condensatori binary wigthed a 9-bit per gli MSB. E ciò crea le tensioni di soglia successive $\frac{VDD}{2^i}$ con consumi estremamente ridotti rispetto ai circuiti attualmente disponibili. Il convertitore progettato si adatta alle specifiche richieste dalle applicazioni IoT fornendo dati a 12 bit a 1,4 MS / s. Il design prelayout consuma meno di 400 nW avvicinandosi alle prestazioni standard con il suo 0.2 fj / C-S FoMw e 194 dB FoMs.

Glossary

IoT	The Internet of Things
ADC	Analog to Digital Converters
ULP	Ultra Low Power
SoC	System on a Chip
WSN	Wireless Wensor Networks
TSMC	Taiwan Semiconductor Manufacturing Company
ULL	Ultra-low Leakage
SME	Small or medium-sized enterprise
SPEED	System Platform for Energy Efficient Design
ML	Machine Learning
AI	Artificial Intelligence
FDSOI	Fully Depleted Silicon On Insulator Transistor
FSR	The Full Scale (input) Range
LSB	The Least Significant Bit
MSB	The Most Significant Bit
QE	The Quantization Noise/ErrorQE
SNR	Signal-to-Noise ratio
$P_{signal,rms}$	The rms power of the input signal
SNDR	The Signal to Noise Distortion Ratio
ENOB	The Effective Number Of Bits
DNL	The Differential Non-Linearity
INL	Integral Non-Linearity
FoMw	Walden Figure-of-Merit
FoMs	Schreier Figure-of-Merit
BWin	The input bandwidth at which the SNDR drops by 3 dB
S&H	Sampling and Holding
Q&E	Quantizing and Encoding
SAR	Successive Approximation Register
DAC	Digital to Analog Converter
CLK	Clock signal

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1 Context and objectives of the Master Thesis

1.1 Introduction

The Internet of Things (IoT) is one of the relevant emerging technologies nowadays. Their applications are involved in different domains. It combines smart production processes with the impressive advance in embedded systems to launch a new era of inter-connectivity and digitization, where everything is connected, smart and information is everywhere. Thanks to the familiarization with new smart objects, home, cities and robots, many industrial experts are talking about a 4th industrial revolution "Industry 4.0" [1] combining real and virtual worlds.
Thus, analog to digital converters (ADC) are one of the vital elements in IoT. They are widely used to interface the surrounding analog world with the digital part of the devices. They are essential for modern sensors such as audio, biomedical and automotive sensors for which real collected information need to be digitized for filtering, monitoring, signal processing and analysis enhancement. Such converters play an important role in understanding the sensed data.
In order to satisfy the continuously growing demand on communication devices, Ultra low power applications (ULP) and IoT, state of the art System on a Chip (SoC) contain not only miniaturized and compact mixed signal circuits but also low power and portable ones. In fact, the low power consumption is one of the most relevant requirements for portable devices and wireless sensor networks (WSN) to create an efficient network of interconnected "Smart Things". For better performance, reduced area and long-term operation without battery replacement, many circuits and blocks should incorporate newer technologies and nodes. Besides, WSN do not have to lose critical information varying in the real world, therefore they need to incorporate Always On parts to continuously sense and collect data. An ADC, which is one of the main components integrated in such devices, need to be highly compact, ultra-low power, and should have wide and adaptable precision and sampling rate with different type of analog sensors.

In this context, Dolphin Design is launching a new branch of smart and power efficient platforms and IPs to gain chairs in the expanding IoT market. The pre-designed SoC used to connect with externally made ADCs when interfacing the sensors dedicated to the target application. However, the aim of the French company is to make the new SoCs compact and fully integrated with all necessary parts that are presented as a plug and play systems.
The main objective of this project is to design a low power ADC that connects the digital circuitry up to 16 different analog sensors using advanced core technology which is TSMC 22 nm ultra-low leakage (ULL).This will constitute one of the important blocks in the peripheral part of the systems.

The first part of this chapter presents the company then a second part is dedicated to report the general definitions and equations related to the ADC. A third part classifies the state of the art types of architectures and relate them to the project's specifications. Finally, the aims and objectives of the master thesis are described in the fourth part.

1.2 Presentation of the company

Dolphin Design is a French small or medium-sized enterprise (SME) situated in France, Israel and Canada working in the field of semiconductor industry and IC design. Following the market evolution and the need for developing new IPs that have the state of the art performances, its motivation is to develop ultra-low power and energy efficient devices destined to many fields of use in the IoT domain.

The newly named company in 2018, founded in 1985 under the name of Dolphin Integration, has a new organization facing the new challenges of the IC and semiconductor market. The strategy aims to provide IPs with faster response time and reliable operations with intermittent connectivity allowing the longest possible life time for the battery with efficient power management. To be competitive, the new solutions are set to be cost effective. The new brand of products has the label of a System Platform for Energy Efficient Design namely SPEED targeting the audio, wearable, vision and metering markets. For each application, Dolphin design is providing a single platform that allows building efficient SoC with extremely short time to market. For instance, SPIDER, CHAMELEON, BAT, RAPTOR and PANTHER are the last constituents of the product portfolio.
SPIDER is conceived as a turnkey platform destined to power management. It incorporates power efficient and low leakage regulators and oscillators combined with MAESTRO which is a CPU-less power controller compatible and scalable with any process and SoC design. Thanks to this platform, a reduction of time to market is guaranteed with achieving an ultimate power efficiency and embedding more functionalities.
CHAMELEON is a subsystem architecture based on CPU-less and event-driven data management system. It is a platform designed using 22 nm FDSOI technology and presented through a full plug and play approach allowing to designers to accelerate the design cycle. It is capable to store and process data while the CPU is in deep sleep mode and allows low-power consumption in active mode. With its low-latency and tiny Machine Learning (ML) accelerator it provides ultra-responsive operations. RAPTOR and PANTHER are advanced IPs that come in addition to CHAMELEON for acceleration and boosting.
When it comes to the energy efficient audio platform, BAT is proposed. It provides a standard voice interface adapted to almost any device. It regroups converters and filters having the state of the art performances and an AI unit offering voice activity detection and command with Ultra-low power consumption [2].

1.3 Analog-to-Digital Converter (ADC): General Definitions

In this section some general definitions related to ADCs and used throughout this report are briefly reviewed. The quality of such a converter is extremely related to some parameters which could be qualified as static and dynamic performance metrics.
An ADC converts an input voltage into a digital code which can be described by the so called "Actual Transfer Function". It is an Ideal Transfer Function when assuming a perfectly linear ADC for which, whatever the initial input level is, the code is linear with respect to the input voltage. Figure 1.1 shows the transfer characteristic of an ideal ADC without any errors.

The Full Scale (input) Range (FSR) is defined as the range of input signal that can be digitized. As shown in Figure 1.1, it is the difference between the maximum value and the minimum value of the input, Vin_H and Vin_L respectively. The Least Significant Bit (LSB), ideally is the smaller variation in analog input voltage that induces a change in the output code. For an ADC transfer characteristic with a N-bit resolution, the FSR includes $2^N - 1$ transitions so the LSB voltage can be written as $VLSB = \frac{FSR}{2^N - 1}$. However, for simplicity and for large N, $VLSB \equiv \Delta = \frac{FSR}{2^N}$ is more commonly used in literature [4].
The Quantization Noise/Error QE is defined as the difference between ideal infinite and finite resolution transfer characteristics (deviation in the output code). It is expressed as $\varepsilon(x) = x - Q(x)$ and has values within an LSB interval $\pm\frac{VLSB}{2}$ as shown in Figure 1.1.c

The rms quantization noise power is the rms value of QE and limits the maximum achievable Signal-to-Noise ratio (SNR) for an ADC in the absence of any other noise source expressed by 1.1.

$$\varepsilon_{rms} = \frac{\Delta}{\sqrt{12}} \tag{1.1}$$

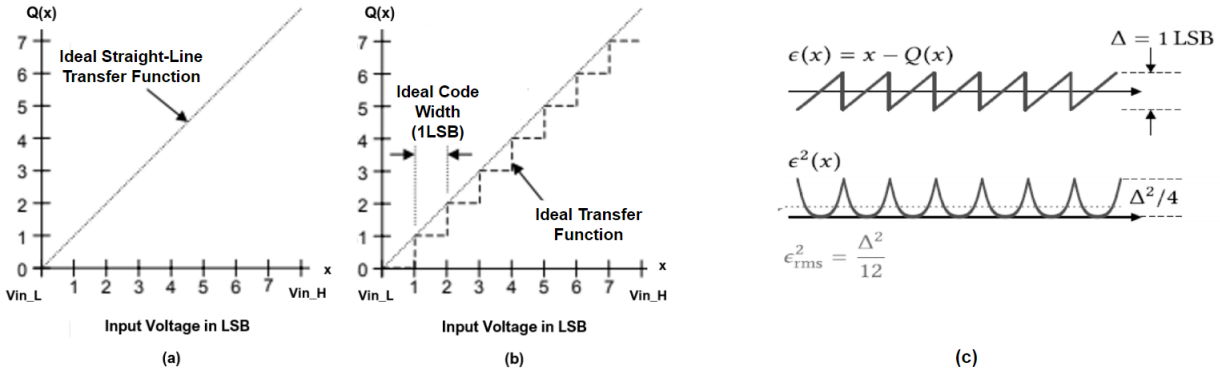

Figure 1.1: *Transfer characteristics of an ADC in comparison to the ideal transfer curve along with the quantization errors. (a) Ideal Straight-Line Transfer Function (infinite resolution) (b) Ideal Transfer Function (finite resolution) (c) Quantization noise/error [3]*

The Signal to Noise Ratio (SNR) can be defined as the ratio of the power of the signal and total noise power generated by quantization process, expressed in 1.2.

$$SNR = 10\log(\frac{P_{signal,rms}}{{\varepsilon_{rms}}^2})\ [dB] \tag{1.2}$$

For an input sinusoidal signal with a peak-to-peak value equal to the FSR the SNR expression could be simplified to include a direct relation with the resolution N. In fact, $P_{signal,rms}$ which is the rms power of the input signal, can be written as: $(\frac{FSR}{2\sqrt{2}})^2$. Then, by replacing the expression of Δ in 1.2, the SNR could be expressed by 1.3:

$$SNR = N * 6.02 + 1.76\ [dB] \tag{1.3}$$

The Signal to Noise Distortion Ratio ($SNDR$) is defined as the ratio of the rms Signal power $P_{signal,rms}$ to the sum of all the unwanted (non-linear and noise sources) components power: noise, distortion, clock jitter etc.
The Effective Number Of Bits ($ENOB$) is a parameter that shows the accuracy of the converter. It also relates the performance of the practical converter to the ideal ADC resolution with a unique noise source QE such as $SNR_{ideal,ADC} = SNDR_{real}$. Using 1.3 the ENOB can be expressed by 1.4:

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{1.4}$$

To achieve better performance, the ENOB should be as close as possible to the resolution of the ADC. There are two major parameters of non-linearity of the ADC response which may let the real code

curve deviate from the ideal one. The differential non-linearity (DNL) and the integral non-linearity (INL) are key metrics for an ADC performance evaluation [5].
Differential Non-Linearity (DNL) is defined as the maximum difference between the analog input voltage edges at each conversion step that induces a code transition at the ADC output and the ideal voltage difference of a step which is VLSB as visible in Figure 1.2. In other words, if the analog input voltage edge for a conversion number I is denoted as $V_{edge,i}$ the DNL can be expressed by 1.5:

$$DNL = \max_{i \in [0.2^N - 1]} \left(\frac{V_{edge,i+1} - V_{edge,i}}{VLSB} - 1 \right) \tag{1.5}$$

The result is normalized to VLSB [5].
Integral Non-Linearity (INL) is defined as the maximum vertical difference between the real input voltage corresponding to the transitions in the output code of the real ADC and the transitions corresponding to the best-fit line as shown in Figure 1.2. It indicates the deviation of the real curve with respect to the ideal one and can also be interpreted as the sum of DNL [5]. INL can be expressed by 1.6.

$$INL = \max_{i \in [0.2^N - 1]} \left(\sum_{j=1}^{i} \frac{V_{edge,j+1} - V_{edge,j}}{VLSB} - 1 \right) \tag{1.6}$$

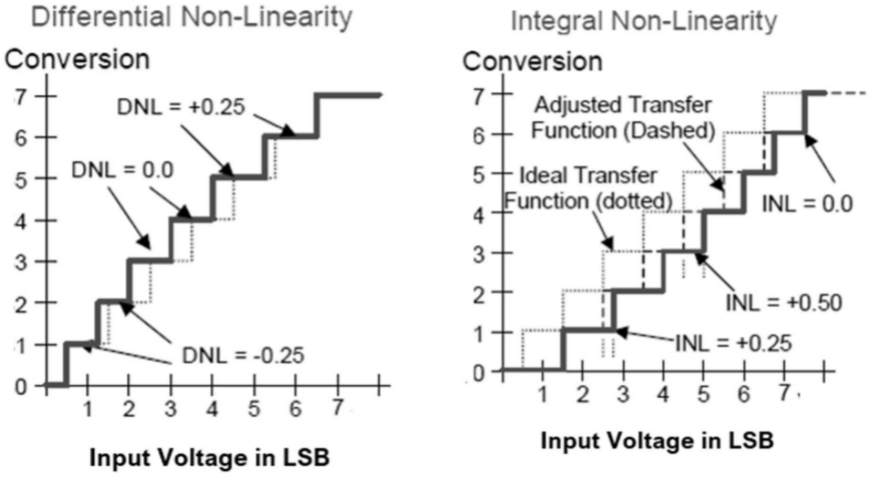

Figure 1.2: *Differential Non-linearity and Integral Non-linearity example*

For the same input analog voltage, the output code of the real ADC may deviate from the expected response behavior due to some errors. Offset and gain are among the major static errors that affect the ADC output. The offset error is defined as the deviation of the real output around the point of zero. It occurs when the output code transition **does not raise around an input value of** $\pm\frac{VLSB}{2}$. There are two kinds of offset error: positive offset and negative offset. For the former, the output value is larger than 0 when the input voltage is less than $\frac{VLSB}{2}$ from below. When it comes to the latter, the input value is larger than $\frac{VLSB}{2}$. At the last conversion step, the Gain error, is defined as the deviation of the real response from the ideal one at the center value of the input voltage for the corresponding step. Both types of static errors could co-exist as shown in Figure 1.3.

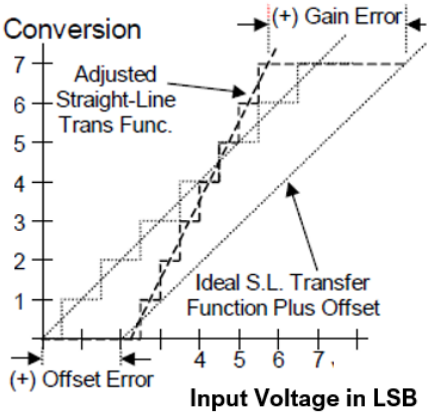

Figure 1.3: *Offset and Gain errors*

1.4 ADC Figures of Merit and classification

1.4.1 ADC Figures of Merit

There are many different types of ADCs proposed in litterature or available in the market, each architecture is identified by distinct characteristics depending on the target application. In fact, the context and the specifications of the system to design dictate the ranges of different parameters such as the resolution, the sampling rate, the power consumption, the accuracy, the noise figures and many others and then allow to select the most adequate ADC type. A simple way to make this decision is to define a figure of merit that regroups the relevant parameters in a compact formula according to which, one can benchmark the performance of the ADCs. There are two common figures of merits: the Walden Figure-of-Merit (FoMw) [6] and the Schreier Figure-of-Merit (FoMs) [7].
The FoMw [6] is expressed in Joule per conversion step (for low power applications in fJ/c-s) and defined by 1.7.

$$FoMw = \frac{Padc}{min(2BW_{in}, f_s).2^{ENOB}} \quad [Joule\ per\ conv - step] \tag{1.7}$$

Where Padc is the power consumed by the ADC from its power supply, BW_{in} is the input signal bandwidth for which ENOB drops only by $\frac{LSB}{2}$ from its value at DC input and f_s is the clock frequency at which the input data is acquired and converted. As shown in 1.7 it relates the energy consumption to the conversion level. It is more suitable for low-resolution and not thermal noise limited architectures. Besides, the effect of power and speed is similar for the same resolution. In fact, the effort of keeping the same FoMw with an extra bit of resolution is as hard as doubling the speed for the same power and conversely as hard as consuming the half power for the same bandwidth.
On the other hand, the FoMs [7] is expressed by 1.8.

$$FoMs = SNR + 10\log(\frac{BW_{in}}{Padc}) \ \ [dB] \tag{1.8}$$

In addition, there is a modified expression cited in [7] that takes into account not only the signal to noise ratio but also the distortion information, expressed in 1.9.

$$FoMs(modified) = SNDR + 10\log(\frac{BW_{in}}{Padc}) \ \ [dB] \tag{1.9}$$

Since it is expressed in dB, BW_{in} is defined as the input bandwidth at which the SNDR drops by 3 dB.
There are some differences noticed between both expression 1.7 and 1.9 that make each of them suitable for a specific criterium. Unlike FoMw, the power supply is indicated in the denominator in 1.9 so that high value of FoMs is preferred for energy efficiency. Furthermore, it is better for high resolution designs.

1.4.2 ADC classfication

The ADC process in two main steps. First, Sampling and holding (S&H), then, Quantizing and Encoding (Q&E). Each architecture operates differently in order to satisfy those two operations. The most used types, but not only, are Flash, folding and interpolating, sigma delta, pipelined and successive approximation register SAR ADC.
Flash ADC, also called direct ADC, is used mainly for applications related to Video digitization or fast signal in optical storage [8]. It is the fastest architecture. It can reach up to GHz sampling rates [9] thanks to its simultaneously clocked comparators that are running in parallel. Based on a simple working principle, the main building components are resistors and comparators which are the only source of speed limitation by the gates propagation delay. On the other hand, this structure makes it large and expensive. In fact, as shown in Figure 1.4, for N bit resolution converter, the flash circuit is composed of 2^N resistors and 2^{N-1} comparators that let the sampled voltage divided into 2^N equal intervals, then a decode logic part deliver the output code. Thus, Each additional bit require twice the number of comparators. As a result, they are more adapted for resolution lower than 8 bits. Conversely, for higher number of bits the implementation will be impractical especially for low-power design [8].

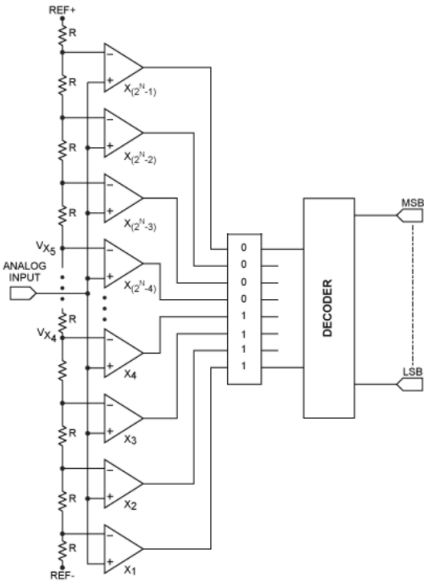

Figure 1.4: *Example of N-bit Flash ADC [9]*

To Reduce the hardware of Flash ADC, a **folding circuit** for analog pre-processing can be used. It

maintains the "one-step" nature of flash conversion. There is no need for inter-stage DAC, which makes it a compact an efficient architecture. As shown in Figure 1.5.a, the principle is based on information extraction from zero crossings. Thus, no need for linear processing as in Flash [10]. This architecture, reported in Figure 1.5.b, is more adapted for low resolution designs for instance from 6 to 8 bits. However, it suffers from linearity issues and mismatch between some components especially for the tail-current and the transconductance gain at the differential pairs [10].

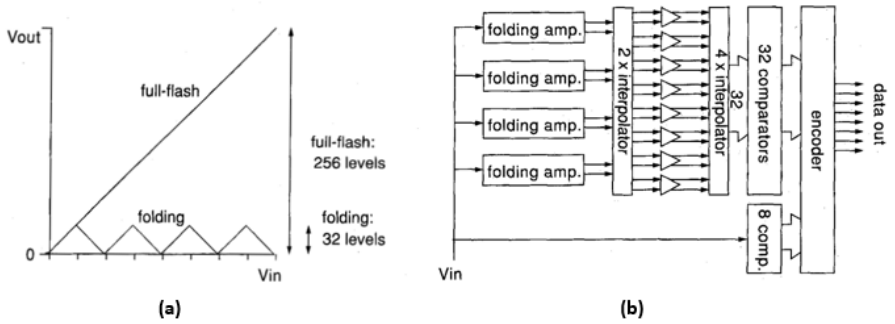

Figure 1.5: *(a)Transfer curve of folding circuit (zig zag) in comparison with the transfer curve that would belong to a full flash converter (straight line) (b)An example of a block diagram of a folding and interpolating ADC[10]*

For medium speed applications in the range of hundreds of MS/s, the resolution can be increased by cascading sub-ADCs. This consists in **the pipelined ADC** architecture. An example is shown in Figure 1.6. In fact, each sub-ADC quantizes and converts a few bits then the residue is amplified and quantized by the following sub-block. Depending on the number of stages, the circuit can be adapted to a wider range of applications in terms of resolution and sampling rate [11]. Nevertheless, this architecture is not adapted to low area applications because of the inter-stage amplifiers.

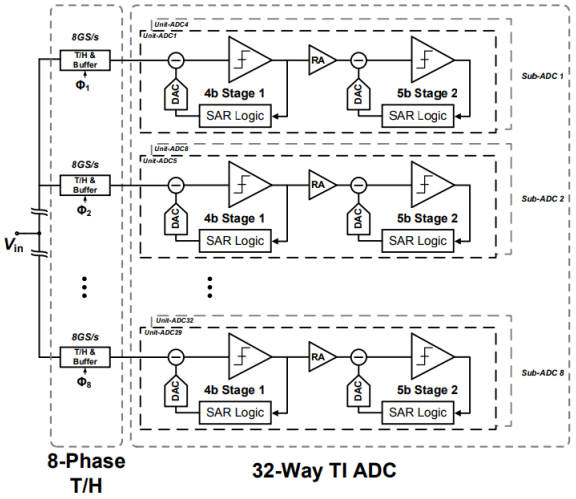

Figure 1.6: *The block diagram of a 64GS/s time-interleaved pipelined ADC[12]*

The sigma delta converter operates as a 1-bit sampling converter. The analog input signal should be relatively slow for the oversampling, that is to say, it can be sampled many times. Each sampling operation result is accumulated and averaged with the main input using a digital filter. The building blocks of the converter are reported in Figure 1.4. The oversampled input goes to the integrator. The integration is then compared to ground. After some iterations, it produces a serial bit stream. Finally the output is a serial bit stream with a number of 1's proportional to the value of the input voltage Vin. This operation induces latency limitations comparing to other solutions. In fact, the sigma delta converter is not suitable for event triggered IoT applications since during the multiple sampling phases critical information could be lost. In addition, it is difficult to adopt this circuit in control loop, where feedback loops require small delays. One field of application that could lose its performance and become harmful using this converter is healthcare monitoring. However, it is well adapted for small bandwidth application such as high-fidelity sounds applications, with relatively higher resolution and lower cost compared to other converter types [13].

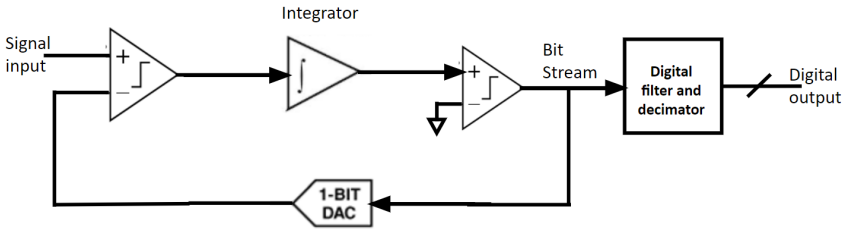

Figure 1.7: *Simplified circuit of Sigma delta ADC with basic building blocks*

The SAR ADC is a successive approximation register consisting mainly in a sample and hold block to sample the input signal, a digital to analog converter DAC and a comparator. The input signal is compared to the DAC voltage and depending on the result, successive fractions of the reference voltage are added or reduced to decide on the conversion bit until the resolution is reached. Two different input modes could be presented to a SAR ADC: single-ended input or a differential input. Generally, there are architectures with one DAC adapted to the first mode and others with a differential DAC to convert signals from the second mode[14]. Without loss of generality Figure1.8 shows a N-bit SAR ADC having single-ended input and a single DAC array.

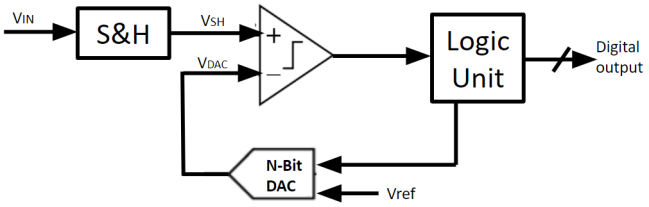

Figure 1.8: *Simplified circuit of SAR ADC with basic building blocks*

In Table 1.1 are reported the main characteristics of each converter in order to compare them and to decide on the most adequate architecture that matches this work specifications.

Architecture	Resolution	Sampling rate	Power consumption	Speed	Cost
Pipelined	6-14	Large Up to 1 GS/s	Medium	Medium-fast	Medium-low
SAR	6-13	Medium Up to 10s MS/s	Low	Medium-fast	Low
Flash	4-12	Large Up to 10s GS/s	High	Very fast	Expensive
Folding/ interpolating	4-12	Large Up to 10s GS/s	Medium	Medium-fast	Medium
Sigma-delta	10-24	Regulable Up to 1 MS/s	Medium-low	Very slow	Low

Table 1.1: Comparison of ADC architectures

1.5 Objectives and organization

This Master thesis project aims to design and characterize through simulations a complete ADC circuit that faces single-ended and differential inputs provided by 16 different sensors. Based on TSMC 22 nm ULL, the key parameter of the design is the low power consumption. This work is devoted to fulfill the following objectives:

- Select the most adequate ADC architecture that matches the specifications
- Choose different possible circuits for each block from the state of the art, optimize them if possible and select the most appropriate one.
- Test the coherence and compatibility of the selected blocks.
- Extract the ADC parameters not only in ideal case but also when introducing some non-linearities, offsets, mismatch and real aspects.

The first part of this report is dedicated to the description of the context of the project. It presents general definitions and the state of the art related to ADC architectures and their classification; the objectives and the motivation of the internship. The second part faces the ADC circuits to the project specifications to select the most appropriate one and details its main building blocks. The third part presents the comparator block and compares some selected circuits. The fourth part details the working principle of the DAC block and compares three circuits in terms of performances and power consumption. The fifth part presents the logic part and how control signals are generated generically or in a programmable manner to convert any signal having voltage amplitude in the range of sensitivity. Finally, the last section is dedicated to assembling all the selected blocks and testing their functionality in ideal case. It describes the impact of some injected non-idealities on the converted data such as comparator offset, capacitive parasitics, real switches and DAC mismatch.

7 Conclusion and perspectives

Through this Master thesis project, an ADC is designed at pre-layout level for Dolphin Design platforms to be used internally.The design uses the TSCMC 22 nm ULL technology and biased at 0.8 V as supply voltage.
First, among different types of converters, the SAR ADC is selected for its close performances to the target specifications dedicated for IoT applications. In fact, the choice is driven by the low power consumption, the medium to low sampling rate, the low cost and the rapidity of this type of ADC. The circuit is based on a differential digital to analog DAC, a comparator and a logic unit. The DAC is based on two capacitive switched arrays, which takes a hybrid structure personally modified for this project. In fact, the 8 larger bits are binary weighted are associated with a 3-bit C-2C array to reduce the total cpacitance and then, the power consumption. For instance, the selected DAC consumes less than 200 nW during a conversion. The comparator is based on a dynamic latched type. The design started by testing available circuit in the state of the art and modify them with respect to the specifications in terms of sensitivity and power. The selected circuit is also personally modified from available circuits in literature, since some sensitivity problems are met for small input amplitudes, a comparator based on a PMOS differential pair was proposed. It shows correct comparison result and consumes only 117.64 nW per conversion cycle.
One of the aims of this project is to make a circuit converting both single-ended and differential signals provided by the 16 sensors to be faced, without using a pre-amplifier for power and area reduction. In fact, the proposed solution is to use common building blocks and adapt the logic unit with implementing an efficient programmable FSM that generates controlling signals for both modes.
The analog circuits, the comparator and the switched capacitor based DAC are implemented and tested through Cadence Virtuoso. However the FSM is implemented using a VHDL and a Verilog code using an internal tool, namely SMASH simulator. Finally for assembling all the building blocks, a Verilog-AMS model is implemented for mixed signal simulations. Using this testbench, the correctness functionality of the converter is studied in an ideal case where analog components are modelized in Verilog. Simulation results show correct conversions that goes through all possible codes for both modes: differential and single-ended. Another point is that some non-linearities are introduced to check the performances of the design. For instance the mismatch between both DACs is tested. Simulations show that the adequate situation is when they are not interdigitized, so they need to be implemented separately during the Layout phase. Also the effect of the switch resistance, especially during the sampling phase, is highlighted. A suggestion for future related work, is to design a bootstrapped switch serving as sampling block separately from the DAC to improve the sampled signal quality. Besides, three possible models for parasitic capacitances are introduced to select which one impacts more the conversion result. In fact, for DAC III architecture, when the parasitics are implemented at the top plate of the capacitor, the conversion code is extremely altered. However, from the bottom plate, the node that is connected to the switch, show little impact on the conversion result. When it comes to the comparator, some corner simulations were operated to test its sensitivity. The Verilog-AMS model showed that the offset voltage has little dependency on the common mode voltage and when is between 5 mv, does not impact the conversion result. However, Monte Carlo simulations taking into account mismatch and process variations on all transistors reflects higher values of the offset over 200 simulated samples. In order to optimize this point, a strategy of resizing is started and to be continued for next steps of designing this ADC. It is based on depicting which transistor pair impacts more the offset, resize it in order to reduce that offset and without increasing the power consumption. The sizes that fits the most with this design trade off will be selected.

Finally, the main objectives of the internship are achieved. SAR ADC is the adequate architecture that fits well with the specifications. The proposed DAC and comparator circuits, that are expected to consume the dominant part of the converter, consume together less than 400 nW which is extremely low compared to the state of the art. At a sampling rate of 1.4 MS/s and an estimated ENOB of 11.5, the Walden figure of merit FOMW and the Schreier FOMS can be estimated to 0.2 fJ/c-s and 194 dB respectively.
The obtained performances, that can also be optimized in the future, are considered as encouraging results to convert the design into Layout and extract the post-layout performances which would be in the same ranges as the specifications and also representing an interesting design with state of the art characteristics, or even better.