Anderson BORDIN

Master Degree in Micro and Nano Technologies for Integrated Systems

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Feasibility study of a characterization setup for novel X-ray sensors

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Confidentiality: No

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I shall be telling this with a sigh
Somewhere ages and ages hence:
Two roads diverged in a wood, and I
I took the one less traveled by,
And that has made all the difference.

The Road Not Taken – Robert Frost, 1916

Acknowledgements

I am very grateful to Busca and Stergios for their patience and valuable advice. This thesis became notable, and the activities more pleasant with your encouragement ...

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My thanks to PoliTO, Phelma, and EPFL. These institutions formed me a great professional, and introduced me to a new world ...

I dedicate this thesis to Arnau, Joaquin, and Fátima, Nanotech colleagues without whom I would not have gone so far ...

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Ao Rodrigo e a Tana, pela companhia e por sempre me receberem de braços abertos ...

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Ao Papai e a Mamãe, as minhas sinceras desculpas por toda a ausência ...

Abstract

The European Synchrotron Radiation Facility (ESRF) is an international research center in which more than 5000 users per year are selected to conduct experiments in the most varied scientific fields, such as physics, biology, or chemistry. After 30 years of activity, the ESRF has embarked on an ambitious upgrade program and to date is the first fourth-generation high energy synchrotron operational worldwide, under the name of ESRF-EBS (Extremely Brilliant Source). The new source is capable of delivering X-rays with unprecedented brightness and coherence, in some cases exceeding the performance of the previous third-generation machine by a factor of larger than a hundred times. Such aspects set new requirements for new instrumentation wit better performance to cope with the capabilities of the new source.

The XIDER project, part of a challenging instrumentation program underway at the ESRF, addresses this quest for more suitable and efficient instrumentation. A central aspect of the project is the use of compound semiconductors such as Cadmium Telluride (CdTe) or Gallium Arsenide (GaAs) to be able to absorb high energy X-rays (30-100 keV). The performance of these sensors is constantly evolving and therefore an adequate optoelectronic characterization is required to optimize the design of the associated readout electronics.

The aim of the thesis is to develop an experimental setup for the characterization of CdTe sensors specially designed for the XIDER project. The goal of the system is the extraction of main physical parameters such as drift time and carrier mobility of the sensors. For this purpose, the thesis work is focused on the study, simulation, and characterization of the dedicated front-end readout electronics, based on a low-noise amplifier, through commercially available low-noise amplifiers. Finally, a feasibility study for the final setup is proposed, also presenting mechanical aspects and the characterization of the sensors for different temperatures.

keywords

Synchrotron Radiation; High-Z Sensor Characterization; Analog Front-End Electronics

Résumé L'installation européenne de rayonnement synchrotron (ESRF) est un centre de recherche international dans lequel plus de 5000 utilisateurs par an sont sélectionnés pour mener des expériences dans les domaines scientifiques les plus variés, tels que la physique, la biologie ou la chimie. Après 30 ans d'activité, l'ESRF s'est lancé dans un ambitieux programme de mise à niveau et est à ce jour le premier synchrotron haute énergie de quatrième génération opérationnel au monde, sous le nom d'ESRF-EBS (Extremely Brilliant Source). La nouvelle source est capable d'émettre des rayons X avec une luminosité et une cohérence sans précédent, dépassant dans certains cas les performances de la machine précédente de troisième génération d'un facteur supérieur à cent fois. Ces aspects imposent de nouvelles exigences pour une nouvelle instrumentation avec de meilleures performances pour s'adapter aux capacités de la nouvelle source.

Le projet XIDER, qui fait partie d'un ambitieux programme d'instrumentation en cours à l'ESRF, poursuit cette quête pour une instrumentation plus adaptée et plus efficace. Un aspect essentiel du projet est l'utilisation de semi-conducteurs composés tels que le tellurure de cadmium (CdTe) ou l'arséniure de gallium (GaAs) pour pouvoir absorber les rayons X à haute énergie (30-100 keV). Les performances de ces capteurs sont constamment en évolution et donc une caractérisation optoélectronique adéquate est nécessaire pour optimiser la conception de l'électronique de lecture associée.

Le but de la thèse est de développer un dispositif expérimental pour la caractérisation de capteurs CdTe spécialement conçus pour le projet XIDER. Le but du système est l'extraction des principaux paramètres physiques tels que le temps de dérive et la mobilité des porteurs des capteurs. A cet effet, le travail de thèse se concentre sur l'étude, la simulation et la caractérisation de l'électronique de lecture frontale dédiée, basée sur un amplificateur à faible bruit, à travers des amplificateurs à faible bruit disponibles dans le marché. Enfin, une étude de faisabilité du montage final est proposée, présentant également les aspects mécaniques et la caractérisation des capteurs pour différentes températures.

mot-clés

Rayonnement Synchrotron; Caractérisation de Capteur Haute-Z; Électronique Frontale Analogique

Astratto

L'European Synchrotron Radiation Facility (ESRF) è un centro di ricerca internazionale in cui vengono selezionati più di 5000 utenti all'anno per condurre esperimenti nei più svariati campi scientifici, come la fisica, la biologia o la chimica. Dopo 30 anni di attività, l'ESRF ha intrapreso un ambizioso programma di aggiornamento ed e' ad oggi il primo sincrotrone di quarta generazione ad alta energia in funzione nel mondo, sotto il nome di ESRF-EBS (Extremely Brilliant Source). La nuova sorgente è in grado di fornire raggi X con brillanza e coerenza senza eguali, superando in alcuni casi di oltre cento volte le prestazioni della precedente macchina di terza generazione. Per far fronte alle prestazioni della nuova sorgente, e' quindi richiesta strumentazione con performance più spinte.

Il progetto XIDER, parte di un ambizioso programma di strumentazione in corso all'ESRF, cerca di rispondere a questa domanda per strumentazione più adatta ed efficiente. Un aspetto centrale del progetto è l'uso di semiconduttori composti come tellurio di cadmio (CdTe) o arseniuro di gallio (GaAs) per riuscire ad assorbire fotoni X ad alta energia (30-100 keV). Le prestazioni di questi sensori sono in continua evoluzione ed è quindi necessaria un'adeguata caratterizzazione elettro-optica per ottimizzare il design dell'elettronica di lettura associata.

L'obiettivo della tesi è quindi quello di sviluppare un setup sperimentale per la qualificazione dei sensori CdTe appositamente realizzati per il progetto XIDER. L'obiettivo del sistema è l'estrazione dei principali parametri fisici di trasporto come il tempo di drift e la mobilità dei portatori. Con questo scopo, il lavoro di tesi si 'e focalizzato sullo studio, simulazione e caratterizzazione di un'elettronica di lettura, basata su un amplificatore di carica a basso rumore, scegliendo tra possibili opzioni disponibili sul mercato. Infine, uno di studio di fattibilità per il setup finale e proposto, presentando anche aspetti meccanici e termini per la caratterizzazione dei sensori in temperatura.

parole chiave

Radiazione di Sincrotrone; Caratterizzazione del Sensore ad Alta Densità; Elettronica Front-end Analogica

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Glossary

ASIC - Application-Specific Integrated Circuit

CSA - Charge Sensitive Amplifier

EBS - Extremely Brilliant Source

ESRF - European Synchrotron Radiation Facility

GBWP - Gain-Bandwidth Product

HPD - Hybrid Pixel Detector

NPD - Noise Power Density

OPA - Operational Amplifier

PCB - Printed Circuit Board

SNR - Signal-to-Noise Ratio

TIA - Transimpedance Amplifier

1 Introduction

"The essence of strategy is choosing what not to do"
Michael Porter

X-RAYS have played a crucial role in social development, since their discovery in 1895 by Wilhelm Röntgen, exhibiting rapid growth in their scientific use into many different fields of physics, chemistry and biology. The most commonly used X-ray sources are conventional X-ray tubes, easily accessible but limited in terms of the intensity they can provide. An alternative way to generate X-ray radiation with improved properties are synchrotron radiation sources, able to provide tunable X-ray photon beams with increased intensity and beam quality.

1.1 Synchrotron Radiation Sources

Synchrotron radiation was first indirectly observed in 1947 [1, 2], when the scientific use of X-rays was already well established. This radiation occurs when charged particles are forced to change direction in a path orbit. Modern facilities accelerate electrons at relativistic velocities, obtaining narrow emission and superior emitted power compared to conventional X-ray laboratory sources (see figure 1.1) [3].

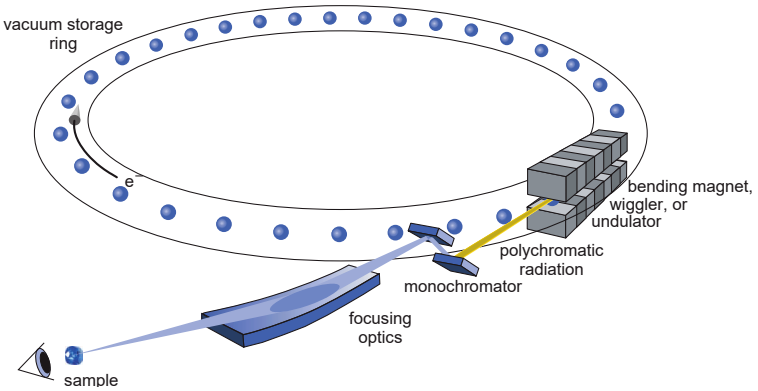


Figure 1.1: Schematic view of a synchrotron light source. Storage rings are powerful X-rays sources designed and dedicated to generate tunable photon beams from the far-infrared to the hard X-ray regime (1 meV - 150 keV). Adapted from [3].

The "quality" of an X-ray source can be described in terms of its *brilliance*, defined as the number of photons per second per unit bandwidth (normally 0.1%) passing through a defined area, or, in a more qualitative way, the amount of useful photons reaching the sample. Mathematically:

$$\text{Brilliance} = \frac{\text{photons/second}}{(\text{mrad})^2\ (\text{mm}^2\ \text{source area})\ (0.1\%\ \text{bandwidth})}$$

The brilliance, also called *brightness*, represents the metric used to follow the evolution of light sources throughout the years, as well as to compare them with X-ray tubes as shown in figure 1.2. The use of light sparks emitted by unshielded cyclotrons is usually referred as the *zeroth generation*.

After attesting its potentialities, the growing interest in synchrotron radiation pushed the emerging of the *first-generation*. These facilities were accelerators initially built for high-energy or nuclear physics, where synchrotron radiation was generated as a secondary parasitic event.The 1^{st} generation set the basis for all the modern multi-user facilities, showing a 10^5 superior brilliance performance compared to conventional sources.

The *second-generation* is marked by the construction of larger storage rings dedicated exclusively to the production of synchrotron radiation. This generation explores solely bending magnets, an electron deflector, to guide the beam on an orbit path. The increasing demand for brighter beams led to the design of *third-generation* synchrotrons [2]. This new category, operational since the early 1990s, provides 10^{13} higher brightness compared to X-ray tubes thanks to insertion devices, a periodic magnetic arrangement placed on the beam orbit [4, 5].

Collective efforts in the synchrotron community stimulated progress towards even brighter beams, thanks to upgrades in the insertion device technology [6, 7, 8], and with high-performance X-ray optics. They lead to the reduction of beam emittance, a qualitative measure related to how narrow the electron beam is. The interest for low-emittance storage rings guided the advent of the *fourth-generation*. In general, a light source is considered to be 4^{th} generation if it exceeds by one order or more an important parameter as brightness or coherence (either temporal and spatial) compared to previous sources. Improved magnet lattice combined with high-performance X-ray optics translate into brighter beams [3].

Today, there are about 40 operational light sources of all generations installed in 14 countries, 10 of which are third-generation sources [10]. In the last decade, 5 facilities have launched initiatives to built 4^{th} generation ultra-low emittance machines:

- New facilities
  - MAX-IV in Sweden (operational)
  - Sirius in Brazil (operational)
- Upgrade projects
  - Advanced Photon Source (APS-U) in USA
  - Super Photon Ring-8 GeV (SPring8-II) in Japan
  - European Synchrotron Radiation Facility (ESRF) - Extremely Brilliant Source (EBS) in France (operational)

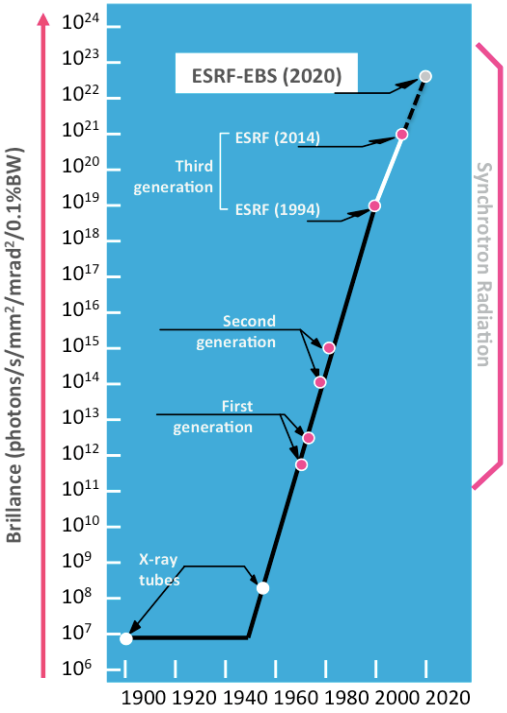


Figure 1.2: Since the 1950s, X-ray source brilliance has increased orders of magnitude over the years, dictating synchrotron family generations. Adapted from [9].

The ESRF in Grenoble is a joint research facility funded by 22 partner countries (13 members and 9 associate) and it was the world's first high-energy third-generation synchrotron light source. Inaugurated in September 1994, for the last 30 years the ESRF has shown remarkable achievements: beam uptime higher than 98%, 5000 users/year, over 32000 publications, and four Nobel prize laureates.

In 2018, the ESRF underwent a 20-month shutdown to replace the storage ring with an improved X-ray source known as ESRF-EBS (Extremelly Brilliance Source). The EBS is the first high-energy 4th generation machine providing X-ray in the 30 kev to 150 keV energy range. The new ESRF-EBS storage ring has a circumference of 844 meters, consisting of 32 magnetic cells as shown in figure 1.3. It stores a 200 mA multibunch electron beam at 6 GeV in its full performance [9], operational since March 2020.

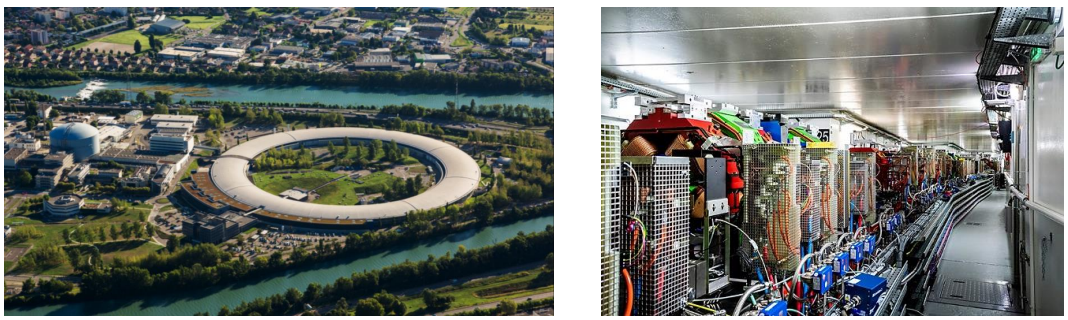


Figure 1.3: External picture of ESRF-EBS building [left], and magnetic section of the storage ring [right].

1.2 X-ray Detection

The construction of advanced storage rings and the realization of new experiments brings instrumentation challenges, especially regarding X-ray detection. New detectors need to be efficient, sufficiently fast and able to cope with the higher photon-flux provided by the ESRF-EBS source.

As already mentioned, the ESRF-EBS is a high energy synchrotron able to provide X-ray photons up to 150 keV. Silicon (Si) material is the most appropriate choice at a relatively low energy range (< 20 keV), showing high absorption efficiency for sensor thickness up to 500 μm. In addition, Si sensors offers low-noise performance, uniform response and robustness, making them the standard solution for X-ray detection [11].

However, as the energy of the photons increases to several tens of keV, Si-based sensors become transparent, i.e., the absorption efficiency drops to negligible levels (see figure 1.4). Therefore, a mandatory solution is the use of compound semiconductors, capable to provide adequate stopping power (thanks to their high-density), leading to acceptable absorption efficiency of hard X-ray photons (30 - 100 keV). Some commercial solutions are Cadmium Telluride (CdTe) or Gallium Arsenide (GaAs) sensors, and figure 1.4 shows their typical absorption efficiency curves compared to Si sensors. Intuitively, the absorption efficiency and its capability to stop radiation depends on the material density and the sensor thickness.

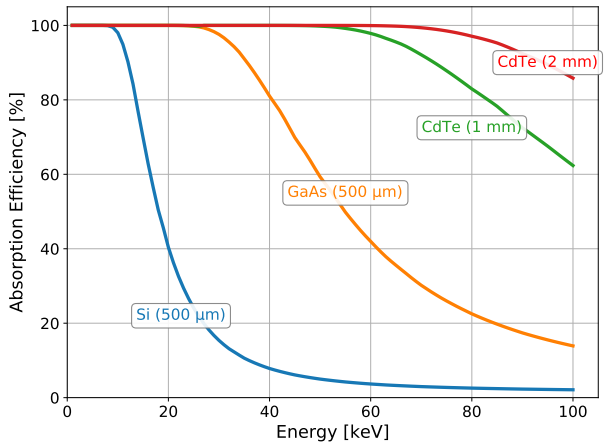


Figure 1.4: Comparative absorption efficiency curves for different sensors materials over a wide X-ray energy range [12, 13]. NIST XCOM database [14].

High-density materials, also known as *high-Z*[1], offer sufficient absorption efficiency for high energy photons. However, they possess several weaknesses due to their compound nature. Compared to elemental semiconductors, high-Z materials show high defects concentration leading, for example, to image non-uniformities as shown in figure 1.5 [15, 13].

Nowadays, Hybrid Pixel Detector (HPD) is the state-of-the-art technology for X-ray 2D detection. These detectors are composed of two main parts: the semiconductor sensor and the readout ASIC[2] chip. The semiconductor sensors is responsible for the absorbing of the

[1] These materials are called high-Z due to their atomic number (Z). CdTe has an average atomic number of 50; GaAs has an average atomic number of 32, both significantly higher than Si (Z = 14)
[2] Application Specific Integrated Circuit

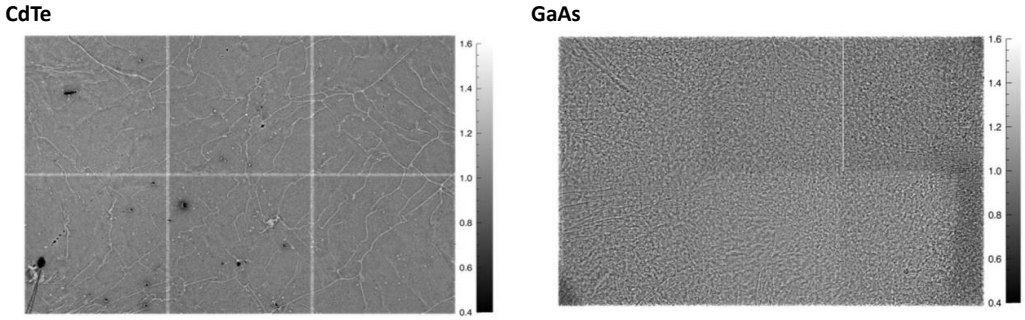


Figure 1.5: Flat-field images of high-Z sensors show imperfections, generally not stable over time. Adapted from [16].

incoming radiation, whereas the ASIC does the signal readout. The term *hybrid* stems from the fact that they are manufactured separately and later assembled together by a dedicated interconnection process, as schematically shown in figure 1.6. Since the first utilization at a synchrotron beamlines in 1999 [17], HPD technology became a succeeding technology used in diffraction, scattering, and imaging experiments.

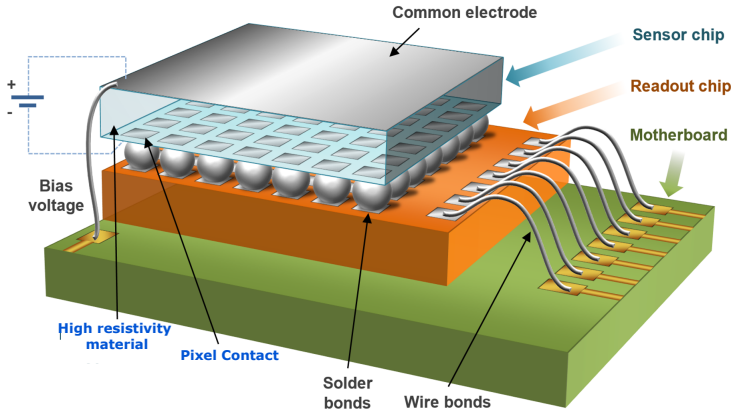


Figure 1.6: Generic architecture of a hybrid pixel detector. The pixelated semiconductor sensor is connected to the CMOS readout ASIC by means of bump bonding technology. Adapted from [18].

Nevertheless, ESRF-EBS providing high energetic beams with improved brilliance and coherence for some experiments cause the Si-based detector to be no more efficient to absorb high energy photons, whereas the ASIC readout is not sufficiently fast to cope with high photon fluxes. Therefore, the new source demands instruments with better sensor and advance readout electronics.

1.3 Thesis Scope

The ESRF facility (FR) and Heidelberg University (DE) are jointly developing a novel detector system named XIDER (**X**-ray **I**ntegrating **De**tecto**r**). The XIDER detector is specifically conceived to operate with high photon flux and hard X-ray regime (30 - 100 keV) afford by the ESRF-EBS. This detector is based on hybrid pixel technology combining a novel readout scheme with the use of high-Z semiconductor material.

The XIDER comprehends an R&D Phase, focused on the study of the new scheme, followed by the Engineering Phase, dedicated to the development of the final detector. The ASIC design is responsibility of Heidelberg University, while the system development and coordination of the project is a duty of the ESRF Detector Unit.

The XIDER project depends strongly on the quality of the semiconductor sensors. High-density materials for X-ray detectors represent on-going technology since sensor performance is continuously evolving. Therefore, it is of fundamental importance to characterize their electrical properties to improve and optimize the design of the readout electronics ahead to the production phase.

Typical sensor parameters to be tested are resistivity, charge carrier mobility, and carrier lifetime, those who have implications on charge collection properties. The sensor qualification also investigates the temperature dependence, major concern related to leakage current, which doubles at every $\Delta 8°C$. Such information serves as a system performance estimation, inspiring requirements to the ASIC circuit layout [15, 19].

> The goal of the thesis is to built a testing platform for the characterization of electrical properties of CdTe sensors specifically designed for the XIDER project. Major interested parameters to be extracted are the carrier lifetime and mobility, signal shape, sensor temperature-dependence and sensor stability in time [20, 21, 22].

The objectives of the thesis are carried out under the supervision of the Detector & Electronics group, member of the Instrumentation Service Development Division. The Detector Unit offers support, maintain and development of cameras in the field of X-ray detectors. For better organization of the thesis goals, the work is subdivided into three workpackages (WP).

WP1 **Study, Simulation & Validation of Readout Electronics**
This WP focuses on the functional definition, design, and validation of a complete readout chain for sensors. This duty involves a theoretical and simulation phase for the conception of low-noise preamplifier for fast, and accurate signal digitization. System simulations are done using TINA SPICE-model tool, while custom-designed Printed Circuit Boards (PCBs) are conceived and realized with Altium Designer software.

WP2 **Design of Experimental Setup**
This WP focuses on the design and implementation of an experimental setup for high-Z sensors based on the electronics realized in WP1. Mechanical and thermal considerations for sensor heating and cooling are addressed as well.

WP3 **Characterization measurements and Data Elaboration**
The experimental setup is thoroughly exploited for the extraction of main sensor parameters, for example carrier lifetime and mobility, stability in time, signal shape and sensor behavior at different operative temperatures. Dedicate data analysis tools are conceived to automatize and optimize data elaboration of the previous measurements.

1.4 Cost Estimation and Project Schedule

The project schedule in the form of a Gantt chart is presented in the following. The initial phase comprehends the study and qualification of the readout electronics, and the built of a validation platform. The second phase is the construction of the sensor housing and the characterization setup, followed by the sensors measurements. There are two rounds of PCB design, related to the validation and the final composition phase, as well as some time devoted to the analysis and reporting of the results.

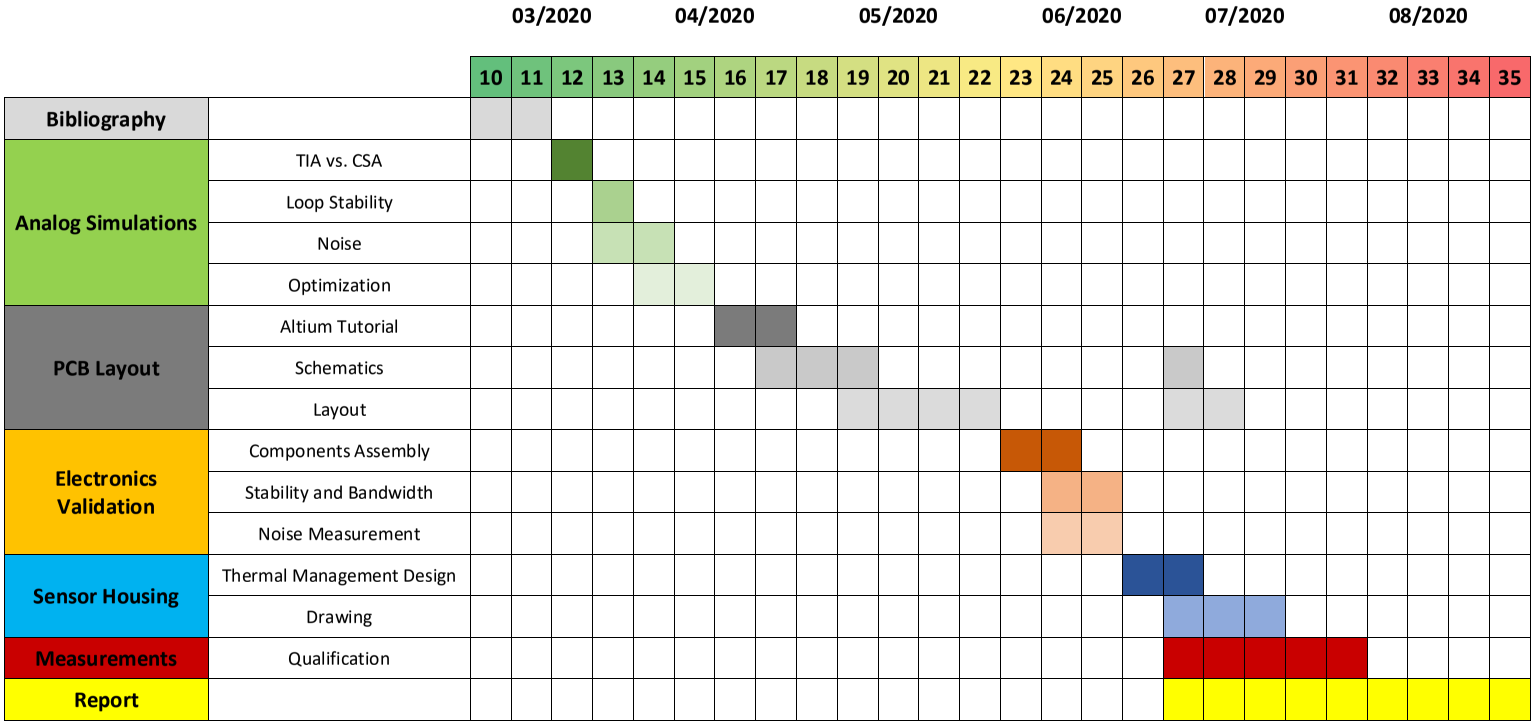
However, the above-mentioned workpackages and the project schedule had to be reformulated after the COVID-19 pandemic breakthrough, forcing the entire ESRF staff to work remotely. The experimental nature of this thesis was particularly impacted by not having access to laboratory facilities and equipment. In addition, suppliers have faced major delays, causing the sensors to be delivered in late July. This prevented them from being assembled and qualified. Thus, the thesis goal was adjusted, focusing on electronics development and the feasibility study of the setup implementation.

Table 1.1 summarizes the cost-estimation for the realization of the thesis. Different amplifiers were acquired and tested, as well as passive components (capacitors, resistors, ferrite beads) for the correct functioning of the circuit. Low noise power supply, high precision oscilloscope, and a pulsed laser source are some of the necessary equipment. Also, there is the cost of software licensing, incorporated into the costs with personal.

Table 1.1: Bill of Materials

Item / Activity	Characteristic	€
Active Components	OPAs	450.00
Passive Components	Cap, Res, etc.	710.00
PCBs	4-layer PCB, 5 units	550.00
Cables & Connectors	SMA, BNC, etc.	200.00
Tools	tweezers, screwdrivers	300.00
Infrared Laser	Alibava Systems, 830 nm	5 000.00
Oscilloscope	Teledyne Lecroy WavePro 2.5GHz HD	30 000.00
Waveform Generator	Agilent 33250A 80 MHz	3 700.00
DC Power Supply	Aim-TTi EL302RT	540.00
CdTe sensors	10 units	10 000.00
Personal	Student and Engineer Assistance	20 000.00
TOTAL		71 450.00

*Most expenses are related to the electronic validation phase.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Part I

Design of a Charge-Sensitive Amplifier

2 Analog Front-End Electronics Simulations

"Get your facts first, then you can distort them as you please"
Mark Twain

SEMICONDUCTOR detectors are complex systems designed to provide information about incoming radiation. The sensor element absorbs photons, whereas the front-end electronics processes the generated signal. This chapter presents analysis and simulations of the complete readout chain as well as concepts for network analysis. Significant parameters such as *ballistic deficit*, *rise time*, and *noise considerations* are presented for different chosen amplifiers.

2.1 Equivalent Model of the Sensor

In order to perform circuit analysis, the sensor is usually schematised as a current generator (i_D) in parallel to a capacitor (C_D) and a resistor (R_D), as shown in figure 2.1. This description is a simplified approximation to describe sensor electrical characteristics.

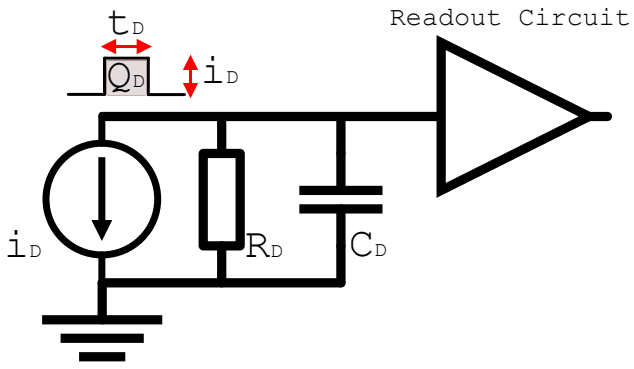

Figure 2.1: Equivalent electrical circuit of an X-ray sensor. The characteristics of the sensor influences the behavior of the readout circuit, directly connected to the sensor electrode [19].

The sensor capacitance can be estimated using simple geometrical considerations. Typical sensor thickness values are in the order of 500 μm to 2 mm. The pixel size ranges from 75×75

μm^2 to 200×200 μm^2 for typical applications on diffraction and scattering experiments [23, 24, 25]. The simplest possible approximation is a parallel-plate capacitor:

$$C_D = \epsilon_0 \epsilon_r \frac{A}{d}, \tag{2.1}$$

where d is the sensor thickness, A the pixel area, while ϵ_0 and ϵ_r are the vacuum and the relative permittivity of the sensor material, respectively. Table 2.1 shows typical material constants for Si, CdTe, and GaAs. The pixel capacitance, therefore, depends on both material choice and layout dimensions.

CdTe sensors 1 mm thick are the most likely candidates to be used in the XIDER project. In the worst-case scenario, the electronics is loaded with only 4 fF capacitance. Even doubling this value using a more sophisticated model, this contribution is basically negligible.

Table 2.1: Properties of typical sensor materials.

Material	Z	ϵ_r	ρ [g/cm^3]	E_i [eV/pair]
Si	14	11.7	2.32	3.67
GaAs	32	13.1*	5.32	4.21
CdTe	50	10-11*	5.85	4.43

*Depends on the manufacturing process [26]

With a similar approach, the resistor R_D can be estimated with an ohmic approximation:

$$R_D = \rho \frac{d}{A}, \tag{2.2}$$

where ρ is the resistivity of the material, leading to an equivalent resistance in the order of 50 GΩ ($\rho \geq 10^{11}$ Ωm). Thus, R_D can also be neglected due to its extremely high value.

Finally, for the equivalent current generator, some simplifications are required. The amount of charge generated within the sensor (Q_D) is proportional to the incoming X-ray photon energy ($E_{X\text{-ray}}$), and depends on a sensor constant called E_i. This parameter represents the average energy required from the incoming photon to generate an electron/hole pair. Mathematically,

$$Q_D = e \frac{E_{X\text{-ray}}}{E_i}, \tag{2.3}$$

where e is the elementary charge. Typical values of E_i are presented in Table 2.1.

Accurate computation of the signal coming from the detector can be performed using specific Monte Carlo tools based on the Shockley–Ramo theorem [27, 28]. These complex calculations are out of the scope of this thesis, and therefore, a simplified rectangular current pulse of amplitude i_D, duration t_D, and charge Q_D, is a satisfactory approximation.

In the case of X-ray laboratory sources, such as X-ray tubes and radiactive sources, currents of tens of nA are generated. In this case, a low-noise electronic circuit is necessary for their detection. On the other side, laser sources can provide much higher current due to the flux intensity, relaxing the electronics requirements.

For the sensors characterization, not only X-rays, but laser sourcescan be exploited. In both cases, using X-ray and fast pulsed laser sources, the carriers drift time t_D is determined by the transport properties within the sensor, being in the order of 50 ns.

Table 2.2: Signal output comparison for different light sources; drift time in the sensor t_D=50 ns.

Source	N_D	Q_D [fC]	i_D [nA]
X-ray	5000	0.8	16
Laser	210000	33.0	670

Two simple examples are proposed to give the reader an estimation of the quantities. In the case of silver anodes ($E_{X\text{-}ray} \sim 22.1$ keV), about 5000 carriers (N_D) are generated within the CdTe sensor per X-ray photon. The current associated with the drift of these charges is about 16 nA.

$$i_D = e\frac{E_{X\text{-}ray}}{E_i}\, t_D \; = e\frac{22.1 \text{ keV}}{4.43 \text{ eV}}\, 50 \text{ ns} = \; 16 \text{ nA} \tag{2.4}$$

In the case of a 100 μW laser source with pulse duration of 5 ns, about 210000 carriers are generated per pulse. With comparable drift time, the output current is about 670 nA. Detailed calculation shown in annex 6.1.

2.2 Charge Sensitive Amplifier

There are typically two options to readout the sensor element: the *Transimpedance Amplifier* (TIA) and the *Charge-Sensitive Amplifier* (CSA). The TIA configuration converts the current into a voltage, and preserves the signal shape at the output of the amplifier. The CSA, however, integrates the current providing an output amplitude proportional to the incoming charge. Figure 2.2 sketches the architectures, as well as the output signal shape.

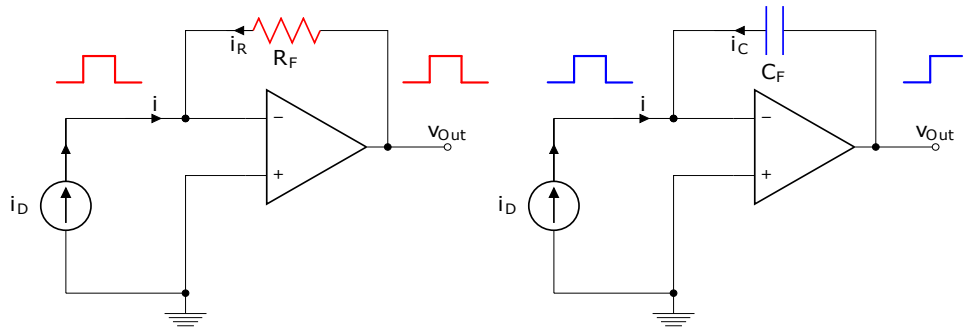

Figure 2.2: The TIA [left] is used as a current-to-voltage converter, whereas the CSA [right] is used for a charge-to-voltage conversion.

The CSA configuration is the most appropriate solution for the purpose of the thesis, since sensor parameters such as carrier life and mobility do not depend on the shape of the signal, but on the associated charge.

The current i_D coming from the detector is forced to flow exclusively into the the feedback capacitance C_F. Therefore, the overall electrical behavior is given by the capacitor fundamental equation

$$i_D = - i_c = C_F \frac{dv_{out}}{dt}. \tag{2.5}$$

By integrating both sides of equation 2.5, it is stressed that the output voltage is proportional to the charge coming from the detector Q_D, and inversely proportional to C_F, which sets the charge-to-voltage gain. v_0 is a DC component, which can be set to zero.

$$v_{out} = -\frac{1}{C_F} \int i_D dt = -\frac{Q_0}{C_F} + v_0. \tag{2.6}$$

It is clear that without a proper discharge component, the CSA output becomes quickly saturated as more and more charges are accumulated over time. The most straightforward element to respond to this requirement is a simple feedback resistor R_F.

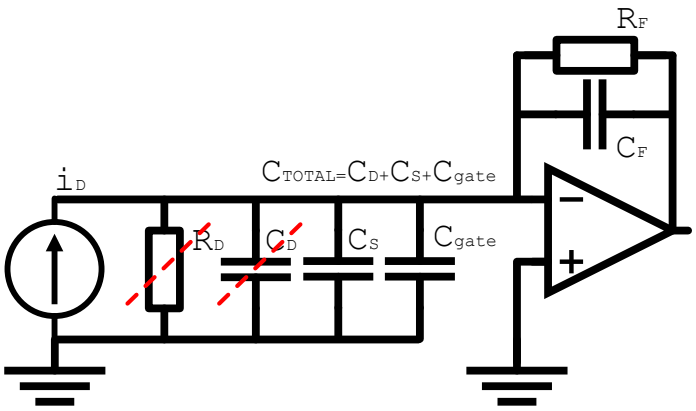

Figure 2.3: Front-end readout circuit of a charge-sensitive amplifier. Equivalent sensor circuit couples to the CSA configuration. C_D is in the order of a few fF compared to C_{gate} and C_S in the pF range; R_D is in the order of GΩ, much higher than the OPA impedance. Both elements can be disregard.

The complete CSA architecture is shown in figure 2.3. Three capacitive components loading the amplifier input are highlighted: C_D is the already mentioned detector capacitance, C_{gate} is the amplifier input capacitance, and C_S is the parasitic stray capacitance due to the layout. C_{total} is the sum of them three. The effect of C_{gate} and C_S to the CSA implementation are analysed separately later in this chapter.

One of the goals of workpackage 1 is to find a suitable commercial amplifier among pre-selected candidates to cope with parameters shown in table 2.2. Therefore, circuit simulation are used to study the amplifier response for parameters like bandwidth and noise. TINA (Toolkit for Interactive Network Analysis) from Texas Instruments, was chosen to perform this optimization study.

Table 2.3 compares commercial operational amplifiers (OPAs) that have been identified as potential candidates for the CSA implementation. The main parameters are extracted from their datasheets. The gain-bandwidth product (GBWP) determines the maximum frequency at

which the device can work, C_{gate} represents the lumped input capacitance, and v_n and current i_n are the voltage and the current noise sources.

Table 2.3: List of pre-selected commercial amplifier for CSA implementation.

OPA	GBWP [MHz]	C_{gate} [pF]	v_n [nV/$\sqrt{Hz}$]	i_n [fA/$\sqrt{Hz}$]
OPA858	5500	0.82	2.5	-
OPA818	2700	2.4	2.2	3.0
OPA657	1600	5.20	4.8	1.3
OPA859	900	0.80	3.3	-
ADA4817	$\geq$ 410	1.40	4.0	2.5

2.3 Amplifier Signal Response

The CSA signal response is presented starting from a simplified approach to a more sophisticated model. In the simplest scenario, both the sensor and the amplifier are consider ideal. The sensor delivers the total charge Q_D in a delta-like pulse $Q_D = i_D t_D$. The amplifier integrates the charge instantaneously, reaching the maximum amplitude with zero delay and no losses. Mathematically, the ideal output is described as follows:

$$v_{out}(t) = \frac{Q_D}{C_F}\left[e^{-\frac{t}{\tau_F}}\right], t \geq 0 \tag{2.7}$$

where τ_F is the discharge time constant related to $R_F C_F$. The charge-to-voltage gain is determined by the capacitor C_F, which determines the sensitivity of the circuit. Instead, R_F influences how quickly the capacitor C_F is discharged.

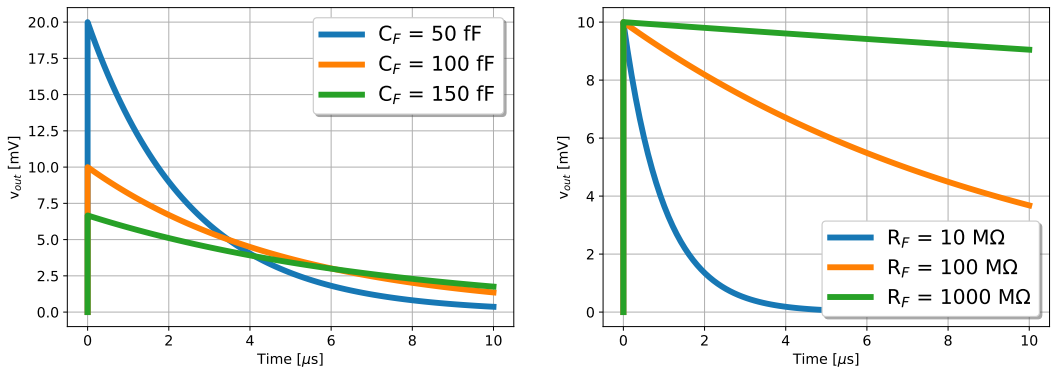

Figure 2.4: CSA dependencies for an ideal amplifier in response to a delta-pulse input.

Figure 2.4 evidences that smaller C_F leads to higher charge-to-voltage gains, while smaller R_F causes faster discharge. However, the OPA behavior is not ideal since it does not respond instantaneously. In reality, the circuit response is limited by the so-called circuit *cutoff*, the frequency above which the system does not operate as an integrating configuration anymore.

In order to determine the dependencies of the cutoff frequency with circuit parameters, a few basic notions about how an amplifier works are needed.

The basic function of an OPA is the amplification of the voltage difference across its input terminals (V^+ - V^-) by a factor gain A_{OL}. However, the capability of the OPA to amplify signals decreases in frequency. The f_{GBWP} represents the maximum frequency where the amplification happens, i.e., gain larger than 0 dB, as shown in figure 2.5. The gain-bandwidth product is defined as the product $f_{GBWP} = A_{OL} \cdot f_0$. The A_{OL} value is the zero-frequency open-loop gain, and f_0 is the -3dB bandwidth (cutoff frequency) of the amplifier. These parameters are qualitatively shown in figure 2.5.

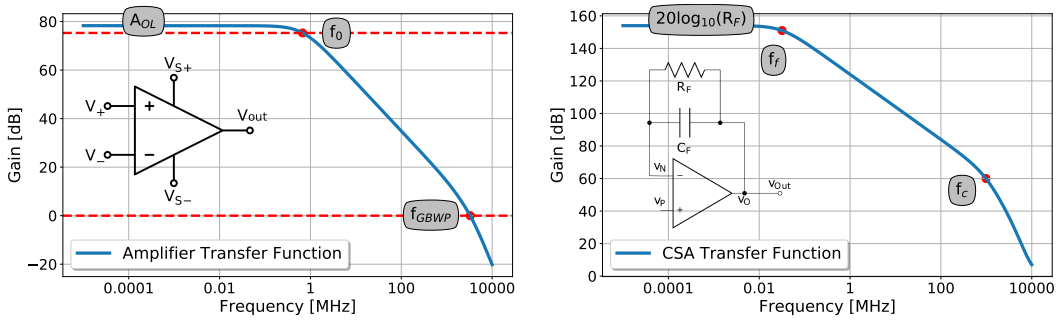

Figure 2.5: The amplifier frequency response shows essential information for the CSA design optimization. f_{GBWP} frequency is defined at unity-gain (0 dB), and relates to how fast the amplifier responds [left]. The integration behavior of the CSA topology [right] lasts from f_f to f_c frequency range.

The frequency response of CSA configuration is different than the one of an OPA. In fact, the topology shown in figure 2.3 affects the circuit performance. When the parasitic loads are taken into, it can be demonstrated that the CSA cutoff frequency (f_c) is the following:

$$f_c = \frac{f_{GBWP}}{\frac{C_{total}}{C_F} + 1}. \tag{2.8}$$

Equation 2.8 evidences that the maximum frequency for a CSA is proportional to f_{GBWP}, justifying the choice for faster amplifiers. The performance is worsen by a factor C_{gate}/C_F, where C_{gate} is the OPA input capacitance, and C_F is the feedback element. C_F is chosen to be smaller than C_{gate} because of the required sensitivity. C_F can not be excessively reduced by forcing the ratio C_{gate}/C_F to increase, thereby reducing the overall system response. Therefore, choosing C_F is a compromise between larger gain and faster response.

The CSA response of a realistic OPA for an ideal delta-like pulse of charge Q_D is described by

$$v_{out}(t) = Q_D \frac{R_F}{\tau_F - \tau_C} \left[e^{-\frac{t}{\tau_F}} - e^{-\frac{t}{\tau_C}} \right], t \geq 0 \tag{2.9}$$

where $\tau_c = 1 / 2\pi f_c$ is the associated time with the cutoff frequency. Thus, equation 2.8 can be rewrite as:

$$\tau_c = \frac{1}{2\pi} \frac{\frac{C_{gate}}{C_F} + 1}{f_{GBWP}}. \tag{2.10}$$

Equation 2.9 shows the CSA response has two contributions: one related to the circuit response (τ_C), and the second related to the discharge profile (τ_F). Figure 2.6 shows that the charge integration is no more instantaneous, but it requires a time $t=t_D$ to be processed.

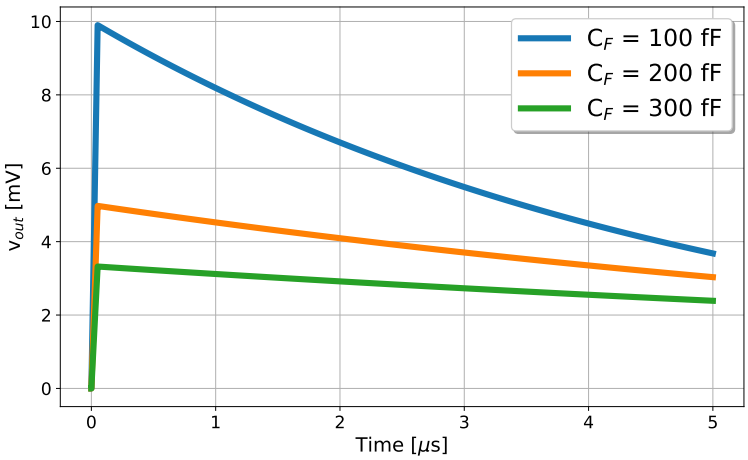

Figure 2.6: For a given resistor R_F, different C_F leads to different charge-to-voltage gain and discharge profiles, and need to be optimized. The response of the CSA topology to a delta-like pulse is composed of a fast rise-edge component related to the cutoff frequency, and a slow discharge dominated by τ_F.

As shown in section 2.1, the signal coming from the detector is assumed to be rectangular, instead of a delta. The output can be obtained by the convolution of the rectangular shape of duration t_D and charge Q_D with the OPA response, which was expressed in equation 2.9. The typical output of a realistic CSA topology is shown in figure 2.7. As highlighted in the inset, v_{out} reaches it maximum when the full charge has been delivered, i.e., $v_{peak}=v_{out}(t=t_D)$. In this condition, in order to guarantee the full charge accumulation, the ratio v_{peak}/v_{max} is calculated. Called *Ballistic Deficit*, it represents the ratio between the real *vs.* the theoretical voltage peak, and needs to be optimized.

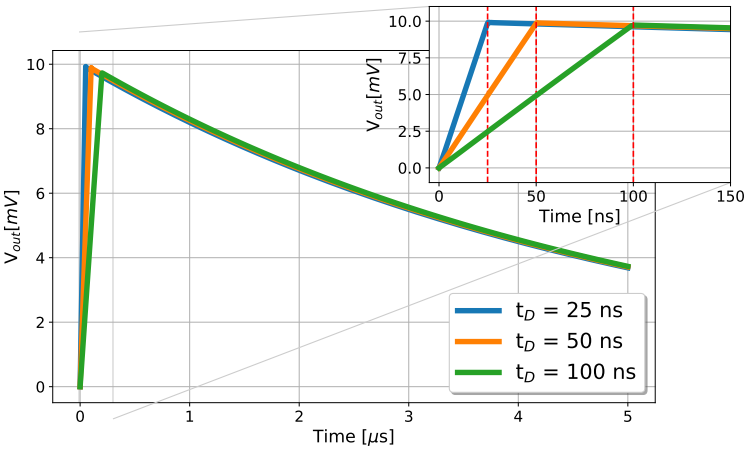

Figure 2.7: CSA response to a rectangular current pulse. For a given charge Q_D, the maximum voltage is reached when the full charge is collected, at the end of the carrier drift time t_D.

The voltage peak, proportional to the integrated charge, is the relevant parameter to be measured for the sensor characterization. This maximum value is equivalent to:

$$v_{peak}(t=t_D) = \frac{Q_D}{t_D} R_F \left[1 - e^{-\frac{t_D}{\tau_F}}\right]. \tag{2.11}$$

Ideally, the CSA implementation exploits only a C_F capacitor for the feedback. Therefore, the theoretical maximum voltage (v_{max}) occurs when $R_F \rightarrow \infty$.

$$v_{max} = \frac{Q_D}{C_F}. \tag{2.12}$$

Thus, the ratio (P) of the peak voltage to the maximum voltage is defined as:

$$P = \frac{v_{peak}}{v_{max}} = \frac{\tau_F}{t_D}\left(1 - e^{-\frac{t_D}{\tau_F}}\right). \tag{2.13}$$

This effect refers to the incomplete charge integration of a pulse in comparison to an infinitely accumulated charge. Equation 2.13 can be used to be optimized to guarantee the maximum charge collection by choosing proper $C_F R_F$. The capacitance C_F determines the gain of the CSA, set by the minimum charge sensitivity to be read (see figure 2.4, left). Therefore, R_F is the remaining parameter to be modified.

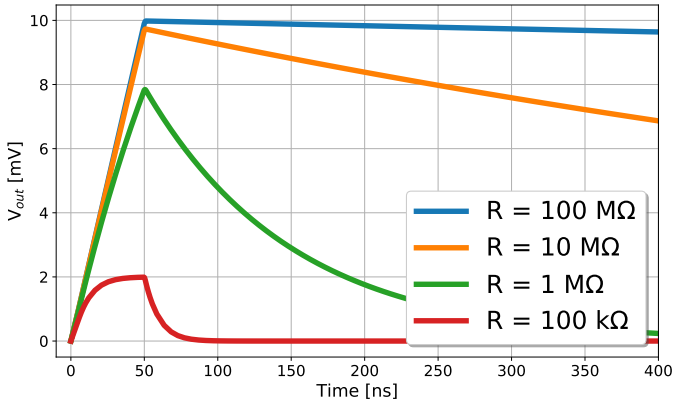

Figure 2.8: The ballistic deficit express the loss of output signal amplitude with respect ideal implementation. The maximum voltage is reached when the full charge is collected at the end of the drift time t_D=50 ns.

Higher resistor values match the ideal CSA implementation. However, an infinite time constant τ_F causes the amplifier to overflow. In this case, the amplifier cannot handle another event before it gets discharged. The appropriate choice of the R_F value is a trade-off between the ballistic deficit and the count rate capability. Figure 2.8 shows the influence of the R_F on real output signals for a chosen C_F value of 100 fF.

After several analysis, C_F is chosen as 100 fF and R_F equals to 50 MΩ. The sensitivity, therefore, is 10 mV/fC, with a time constant τ_F of 5 μs. Using this values in the feedback network, 22.1 keV X-ray photons generate an output of 8 mV, while a 100 μW infrared laser source (λ=830 nm) generate a 330 mV output.

2.4 Circuit Stability

A critical feature for the CSA circuit is the stability. Wrong feedback parameters leads to unstable CSA operation. Figure 2.9 shows qualitatively the response of an stable *vs.* unstable amplifier for the same input pulse.

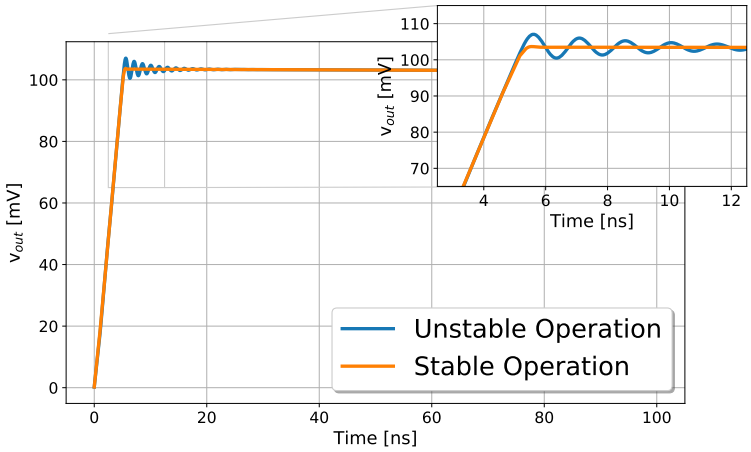

Figure 2.9: Circuit stability is a major concern for the CSA implementation. The feedback network can cause distortions and signal overshoots if not properly designed.

The typical technique to ensure system stability is the well-known *open-loop* analysis, performed in the Laplace domain. The feedback loop is interrupted as depicted in figure 2.10. The net is then excited with an small signal (v_{test}), and the circuit response (v_{loop}) is measured. The returns provide the open-loop gain (G_{loop}).

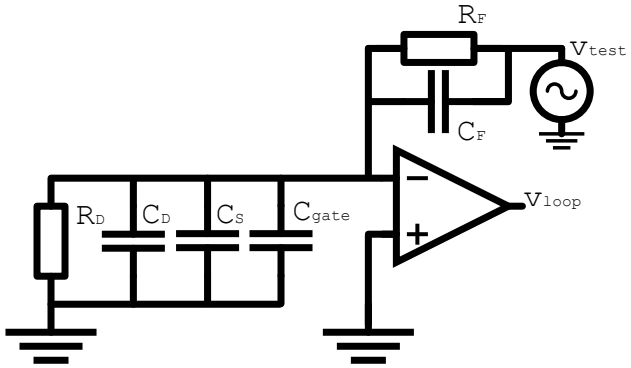

Figure 2.10: Open-Loop test circuit. This approach permits to measure the gain given by the feedback components, despite locating key frequencies for the CSA stability analysis.

The related transfer function, $H_{G_{loop}} = v_{loop}(s) \,/\, v_{test}(s)$ is given by:

$$H_{G_{loop}}(s) = \frac{v_{loop}(s)}{v_{test}(s)} = -\frac{A_{OL}}{1+s\tau_0}\left(\frac{1+s\tau_F}{1+sC_{total}R_F}\right), \tag{2.14}$$

The G_{loop} transfer function is qualitatively presented in figure 2.11 [top]. The plot shown in figure 2.11 [bottom] shows the phase delay of the output signal with respect to the test input pulse. It shows the influence of the pole and zero frequencies of the G_{loop} transfer function on

the phase plot[1]. A pole frequency causes a negative 90° phase shift while a zero frequency causes a positive 90° shift.

The sufficient condition for circuit instability relates to the *phase margin* (PM). It is calculated as the complementary value to a 180° phase shift at the frequency where the loop gain is equal to 1 (0 dB). For example, in figure 2.11 [bottom], the PM is 180 - 103.8 = 76.2°. According to the Bode stability criterion, a circuit is said stable when it shows a *phase margin* (PM) $\geq$ 45°.

Therefore, changing feedback parameters affect the phase shift curve, and consequently the phase margin. Finally, for the chosen amplifiers and feedback network C_F=100 fF and R_F=50 MΩ, a phase margin close to 80° ensure proper CSA operation.

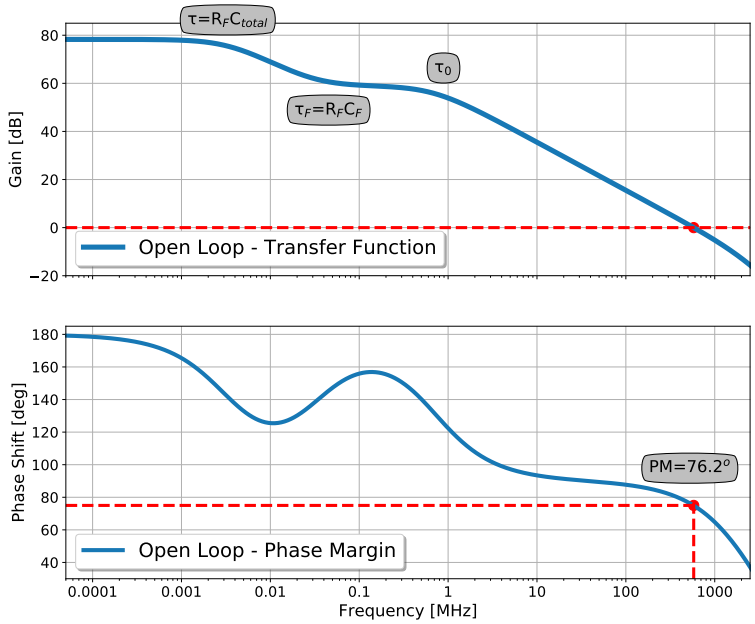

Figure 2.11: Open-loop transfer function. At loop gain equals to 1 [top], the phase margin is roughly 76° [bottom]. This is sufficient for a stable operation.

2.4.1 Noise Analysis

An important feature of the front-end electronics is the noise performance. The signal-to-noise ratio (SNR) characterizes the quality of the CSA, and relates to the sensitivity of the architecture. It determines the minimum charge signal that can be distinguished with respect to the background level.

In order to optimize the electronics noise response, the system noise sources must be identified. For the CSA implementation, the operational amplifier is the main noise source. However, the passive components also generate noise. Thus, the output noise is the sum of all noise sources at the input, amplified by the noise gain.

The real CSA implementation shown in figure 2.3 is modified by an equivalent electrical model. Figure 2.12 summarises the noise contribution of the amplifier. Its simplified noise

[1]A pole frequency corresponds to a corner frequency at which the slope of the magnitude bode plot *decreases* by 20 dB/decade; a zero corresponds to a corner frequency at which the slope *increases* by 20 dB/decade.

model has a constant voltage (v_n) and a current (i_n) noise sources in series with the inverting input terminal. This values of these sources are informed in the components datasheet, as indicated in Table 2.3.

Additionally, the CSA feedback resistor contributes to the total noise by adding thermal noise at temperature T. It is replaced by an equivalent current noise source ($i_{n_{RF}}$) given by $\sqrt{4k_BT/R_F}$, where k_B is the Boltzmann constant.

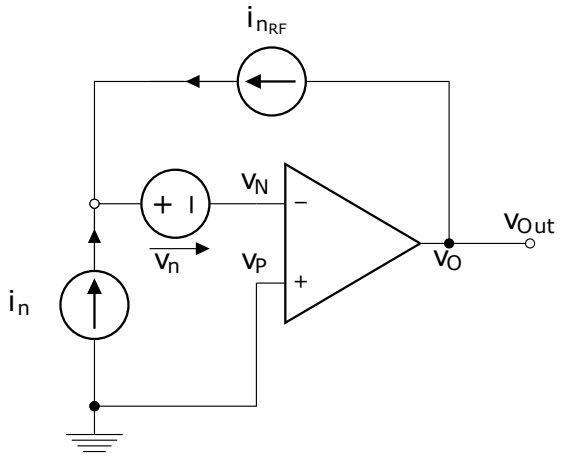

Figure 2.12: The charge-sensitive amplifier configuration with its equivalent noise sources. Adapted from [29].

The noise sources are assumed to have a flat frequency spectrum (white noise). Its format is shaped according to the noise transfer function (noise gain). It can be demonstrated that the noise sources are transferred to the output as given:

$$H_v(s) = \left[\frac{1 + sC_{total}R_F}{1+s\tau_F}\right]\left[\frac{1}{1+s\tau_c}\right] \tag{2.15}$$

$$H_i(s) = R_F\left[\frac{1}{1+s\tau_F}\right]\left[\frac{1}{1+s\tau_c}\right], \tag{2.16}$$

where voltage $H_v(s)$ and the current and $H_i(s)$ noise gains are computed in the Laplace domain. Expressing the noise sources in the frequency domain leads to the noise power spectral density (NPD). It is a convenient way to present the noise of the system, usually expressed in units of $\frac{nV}{\sqrt{Hz}}$. The NPD is given by a factor equal to the square of the noise sources, shaped by the square of the respective transfer function. Mathematically,

$$v_{NPD}(s) = \sqrt{{v_n}^2 * H_v(s)^2} \tag{2.17a}$$

$$i_{NPD}(s) = \sqrt{{i_n}^2 * H_i(s)^2}. \tag{2.17b}$$

Figure 2.13 shows the voltage ($v_{NPD}(s)$) and current ($i_{NPD}(s)$) noise power density for the charge-sensitive amplifier. The total noise is the resultant of both contributions.

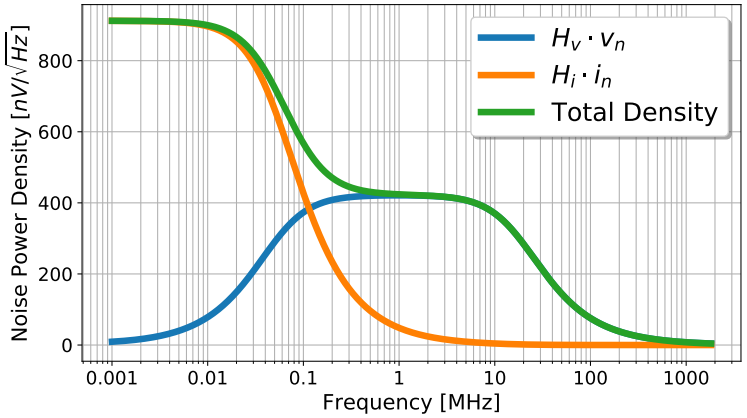

Figure 2.13: Noise spectral density plot for the charge-sensitive amplifier. The frequency response of the i_n has the shape of a low-pass filter; the component related to v_n has the response of a band-pass filter.

Finally, the total noise is converted from the noise power density into RMS noise (σ_{RMS}) voltage. This method sum the spectral contributions over the entire frequency range. Figure 2.14 shows qualitatively what is expressed in equation 2.18.

$$\sigma_{\mathrm{RMS}} = \sqrt{\int_0^{\infty} [v_{\mathrm{NPD}}(s) + i_{\mathrm{NPD}}(s)]\, df} \ . \tag{2.18}$$

Figure 2.14 shows that the total RMS noise saturates since the amplifier bandwidth limits the integration. Thus, instead integrating the noise power density until $f \to \infty$, equation 2.18 can be adjusted to integrate up to the system cutoff frequency f_c. Moreover, the system noise also depends on the amplifier input sources. Thus, the total noise represents a trade-off between larger integration windows and the value of the input noise sources.

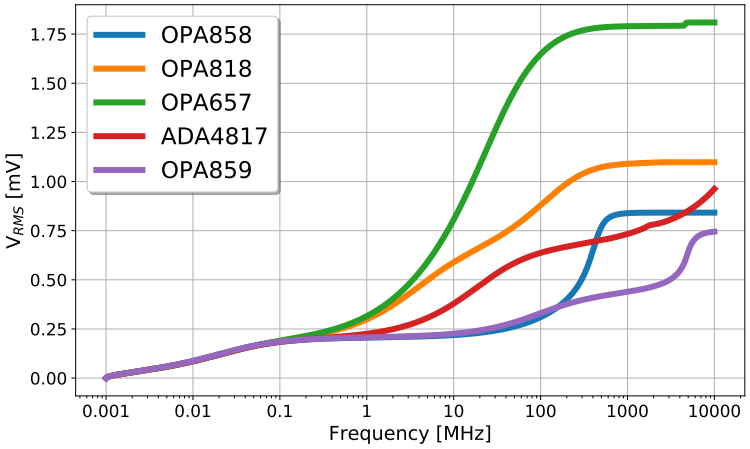

Figure 2.14: Converting noise spectral density into RMS noise voltage evidences that the total noise saturates at high frequencies since the CSA does not integrate the signal above the cutoff frequency.

2.4.2 Influence of Stray Capacitance

All the analysis carried until now considered the C_{gate} capacitance as the unique parasitic element loading the electronics. In reality, when implemented in Printed Circuit Boards

(PBCs), the components suffer from parasitics caused by the elements interconnection and metallic pads. Thus, the board contribution, called *stray capacitance* (C_S) adds to C_{gate}.

In order to understand how C_S influences the system's parameters, a round of simulations is performed. The influence of the stray capacitance were studied ranging from 0 to 10 pF. The C_S element, highlighted in figure 2.3, increases C_{total} since $C_{total}=C_{gate}+C_S$, and degrades the performance in terms of t_r, ballistic deficit, and noise.

The first studied contribution is the rising time (t_r) dependence. This parameter relates to CSA bandwidth, and express how fast a amplifier can respond. Mathematically $t_r = 0.35/f_c$.

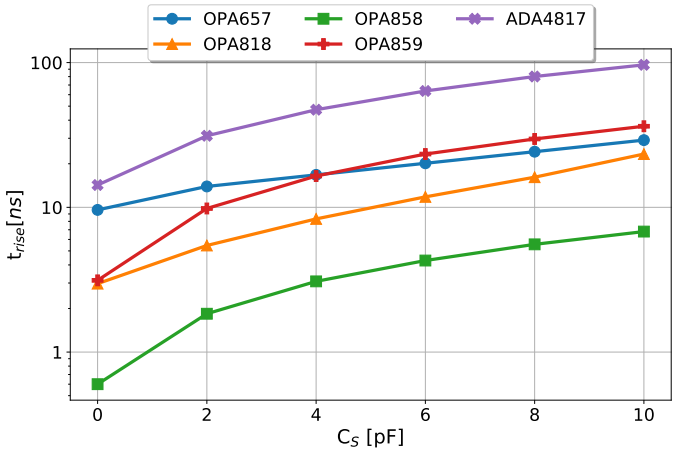

Figure 2.15: Influence of C_S represents a limiting factor in terms of system rise and bandwidth.

Figure 2.15 indicates the influence for the selected amplifiers presented in Table 2.3. The rising time is sufficiently fast for integrating a pulse with duration of t_D=50 ns for most of them. Both OPA858 and OPA818 are the amplifiers with the best response for C_S = 10 pF, showing a rise time of 6.8 and 24 ns, respectively. Expressed in terms of bandwidth, the circuit cutoff frequency is 51.5 and 14.6 MHz in the worse scenario.

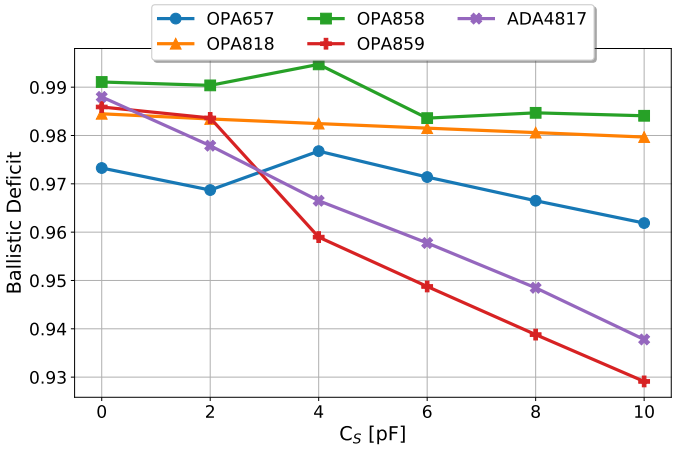

Figure 2.16: Influence of C_S on the ballistic deficit. C_{total} slows down the amplifier response, causing some OPAs to be discarded due to their insufficient response

The second studied parameter is the Ballistic Deficit. Again, the less impacted amplifiers are OPA858 and OPA818. C_S practically do not alter their capacity to integrate the charge, as

shown in figure 2.16. Differently, OPA818 and ADA4817 lose up to 7% of the incoming charge. This behavior is inadequate for the CSA implementation.

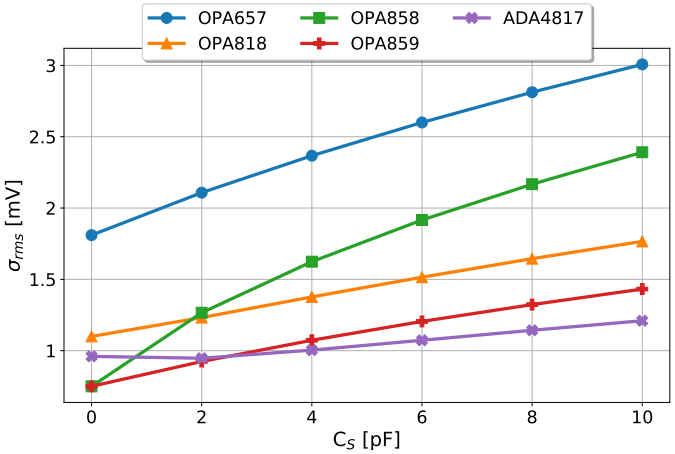

Figure 2.17: TINA simulation of the total CSA noise. Large bandwidth amplifiers are more severely impacted by C_S.

Finally, ADA4817 and OPA859 show the best performance in terms of noise RMS. It happens because C_{total} reduces their bandwidth, forcing the noise value to saturate. Therefore, the levels verified to OPA858 and OPA818 are tolerable compared to their performance concerning other parameters.

Table 2.4 summarizes the performance for pre-selected solutions for the CSA implementation for C_S=0 pF. Simulations with increasing input loads confirm OPA858 as the most suitable candidate for the CSA implementation. The considerations presented on this chapter are further validated on chapter 3.

Table 2.4: CSA performance for pre-selected amplifiers.

OPA	σ_{RMS} [mV]	f_c [MHz]	P [%]	PM [°]
OPA858	0.75	586.1	99.1	75.0
OPA818	1.10	118.0	98.4	88.6
OPA657	1.81	36.3	97.3	86.1
OPA859	0.75	111.7	98.6	86.7
ADA4817	0.96	24.5	98.8	88.2

3 Analog Front-End Electronics Validation

"However beautiful the strategy, you should occasionally look at the results"
Sir Winston Churchill

THE simulation and analysis held on the previous chapter indicates suitable amplifiers for the Charge-Sensitive Amplifiers (CSA) readout implementation. In this chapter, real system measurements are compared to the optimization study carried in Chapter 2. For this purpose, a dedicated Printed Circuit Board (PCB) is designed to validate the real behavior of several commercially available OPAs in comparison to the simulations in terms of bandwidth (BW), rise time (t_r), ballistic deficit (P), and voltage noise level (σ_{rms}). The PCB was realized using a dedicated CAD tool (Altium Designer), by designing the schematic and the associated layout. The result of this task is shown in figure 3.1, which also highlights the implemented structures.

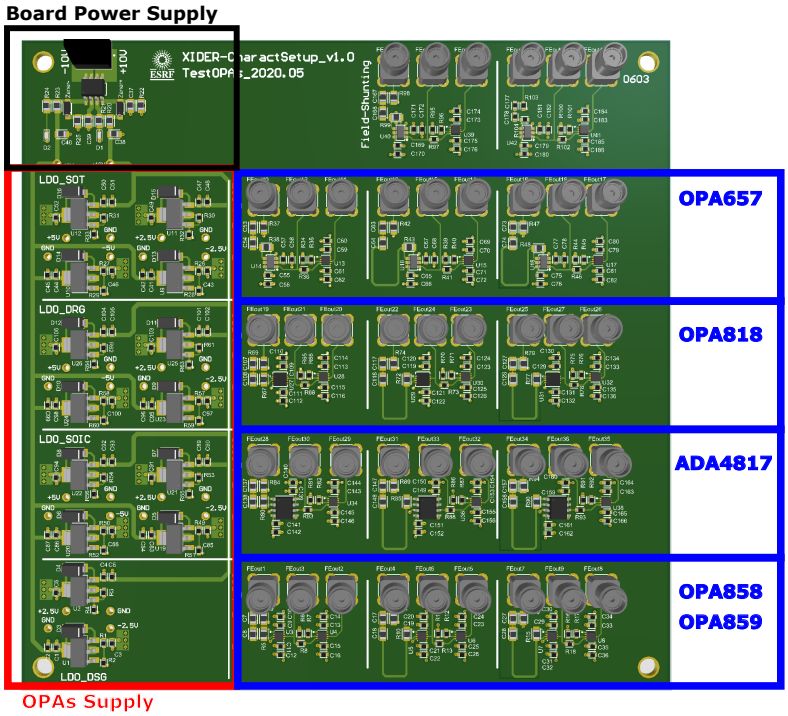

Figure 3.1: Characterization PCB used for front-end electronics validation. The testing platform is also used for debugging purposes to identify possible circuit optimizations. Implemented using Altium Designer software.

As can be seen in figure 3.1, the power supply circuit and noise filtering are isolated on the left side of the PCB. It consists of voltage regulators and passive elements to reduce noise interference from the DC power supply. The center-right of the PCB layout accommodates several distinct amplifiers (OPAs).

Moreover, figure 3.1 shows that many layout variations are necessary. In general, the OPAs are non-compatible in terms of pinout, and supply rail (± 2.5 V or ± 5 V) according to their functionalities. Each row allows testing OPAs with their distinct package, while each column tests particular layout techniques to reduce parasitic loads.

The proposed layout of figure 3.1 has another important feature. In order to test the amplifier without the additional difficulties of the sensor, the test platform uses a *pulser* structure to emulate the signal coming from the detector (see figure 3.2). Another important peculiarity is that the feedback capacitor C_F is not soldered on the board but is a parasitic contribution. This technique generates a capacitance of 120 fF, as explained in the appendix 6.2), and confirmed by Fodisch et al. [29].

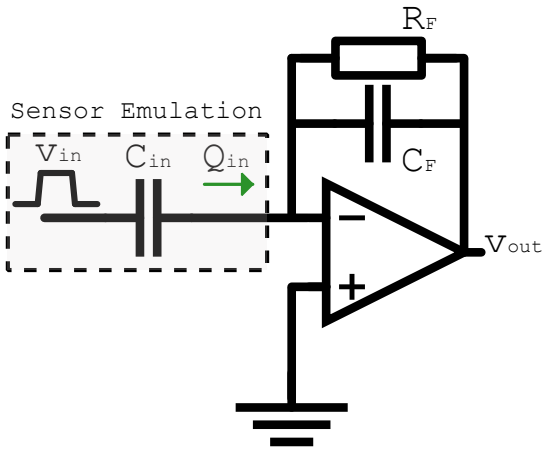

Figure 3.2: Pulser circuit. When driven by a voltage waveform source V_{in}, the capacitor C_{in} provides an equivalent charge Q_{in}.

The configuration shown in figure 3.2 is composed of a C_{in} capacitor connected in series to the amplifier. When pulsed with a voltage step waveform (V_{in}), it provides a charge (Q_{in}) given by:

$$Q_{in} = C_{in}\, V_{in} \tag{3.1}$$

In order to give the reader a sense of some values, the capacitor C_{in} is chosen to be 500 fF. When a 10 mV square wave is pulse through it, approximately 6 fC are delivered to the CSA. Another convenience of this circuit is that v_{in} and C_{in} can be easily modified, exploring the sensitivity of the circuit.

3.1 Validation Protocol Description

This section presents the methods used to characterize the analog front-end electronics. These protocols enable the comparison of measured and simulated data.

Bandwidth (BW)

The first parameter to be characterized is the system bandwidth (BW). As a reminder, it represents the maximum frequency range in which CSA operates as an integrator.

In order to determine the system cutoff frequency (f_c), the circuit transfer function is measured. Sine waves of amplitude A_0 and frequency f_0 are injected into the circuit thanks to a Marconi 2031 10 kHz-2.7 GHz signal generator, while the peak-to-peak output amplitude A is recorded. The same procedure is repeated by increasing the input frequency f_0, covering a wide frequency range. Finally, the system transfer function is determined simply dividing the output by input amplitude A/A_0 (see figure 3.3). Finally, the ratio is expressed in dB units.

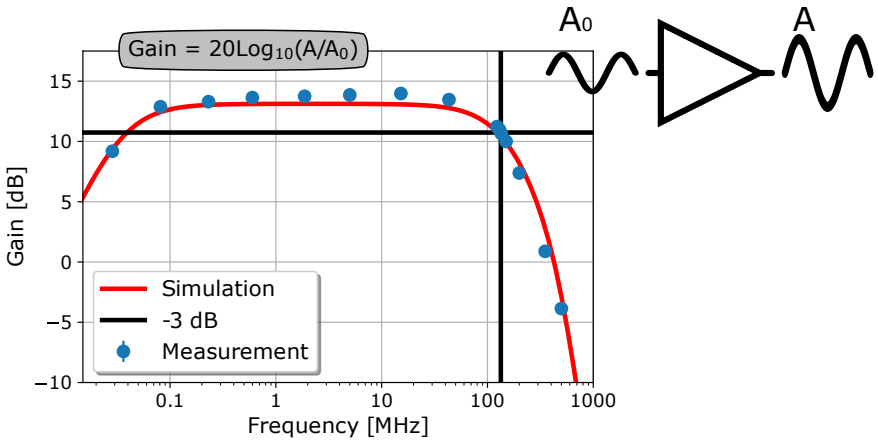

Figure 3.3: Bode diagram plot of the circuit frequency response.

It worth mentioning the topology of the pulser is different from the one shown in figure 2.5. However, the f_c corner frequency value still represents the edge of the integration window. The pulser circuit transfer function has the shape shown in figure 3.3, and the cutoff frequency of the system is determined at the -3 dB level with respect the plateau gain level. Such value express at which frequency the power of the signal is reduced to one-half. Figure 3.3 shows the transfer function measurement with a cutoff frequency slightly above 130 MHz. The same procedure is repeated for all investigated OPAs. Comparison with the simulations is carried out later in this chapter.

t_{rise}

The CSA bandwidth and the signal rise time (t_r) are closely-related parameters. This parameter computes the limit of a system to respond to abrupt input changes. Since the cutoff frequency (f_c) is equal to $1/(2\pi RC)$, t_r and BW correlates as follow:

$$t_r = 2.2RC = 2.2\tau_C = \frac{2.2}{2\pi f_c} = \frac{0.35}{f_c} \tag{3.2}$$

Thus, from the transfer curve, the rise time is also calculated. Despite an indirect measure, the tested amplifiers have a sufficiently fast response, faster than the waveform generators at disposal. Thus, this is the most reliable and accurate method to test t_r.

Signal Response

The next validation involves measuring the shape of the amplifier's output signal to check for

distortions. The Marconi generator used previously, despite operating up to GHz range, is limited to sine and triangular waveforms. In order to create square waveforms, an Agilent 33250A 80 MHz waveform generator is explored. However, the Agilent limits the signal rising time to approximately 5 ns, slower than the OPAs response. Therefore, this value will be adopted from now on as the input rise time without further penalties.

Finally, the output signal is recorded with a Teledyne LeCroy WavePro 254HD High Definition Oscilloscope. Considering a step-like input signal, the CSA topology response is given as follow:

$$v_{out}(t) = V_{in} C_{in} \frac{R_F}{\tau_F - \tau_C} \left[\exp\left(-\frac{t}{\tau_F}\right) - \exp\left(-\frac{t}{\tau_C}\right) \right], t \geq 0 \tag{3.3}$$

where V_{in} is the input signal amplitude, R_F is the feedback resistance, τ_F is related to the feedback network, and τ_C linked to the OPA cutoff frequency according to equation 3.2. Therefore, measuring the CSA output for a given input allows comparing the ideal response and extracting unknown parameters such as C_F (shown in figure 3.4).

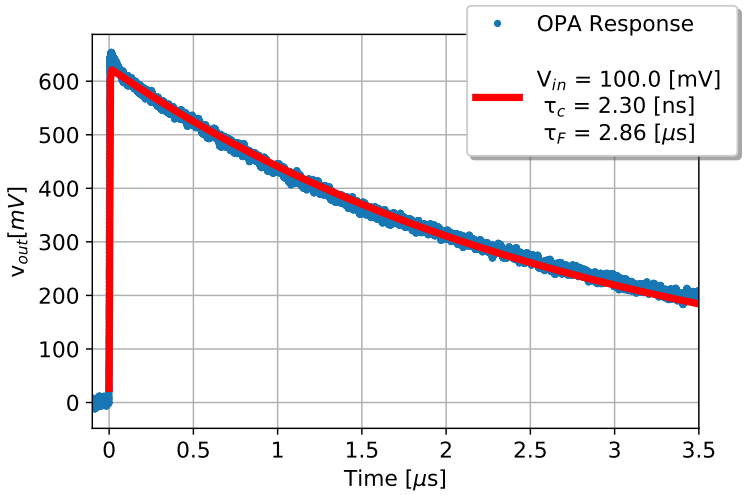

Figure 3.4: Charge Sensitive Amplifier signal response to a rectangular pulse; small overshoot occurs because the passive probe loads the output.

The example shown in figure 3.4 is confronted with equation 3.3, where parameters as τ_F and τ_F are estimated. The input amplitude V_{in} is known. τ_C is equal to 2.3 ns, corrupted by the waveform generator, which is not sufficiently fast. Thus, t_r is equal to 5.0 ns according to equation 3.2.

The discharge profile has a time constant value τ_F of 2.85 μs. The resistor R_F has a value of 47 MΩ, while C_F is estimated as 62.1 fF, smaller than the desired 120 fF. Further details are discussed along the chapter.

Moreover, other tests were made to validate the pulse shape at the output of the CSA. In particular, the height of the output signal is an important attribute to be studied. Using a simplified description, the signal height can be estimated. Assuming the charge generated by

the pulser has to flows necessarily onward the feedback network, the output voltage (V_{out}) is mathematically given by:

$$Q_{in} = Q_{out}$$
$$C_{in}\, V_{in} = C_F\, V_{out}.$$

Figure 3.5 shows the fit of the signal peak heights. The CSA has an excellent linearity with respect to the input amplitude V_{in}, with a maximum deviation ≤ 5.0 mV.

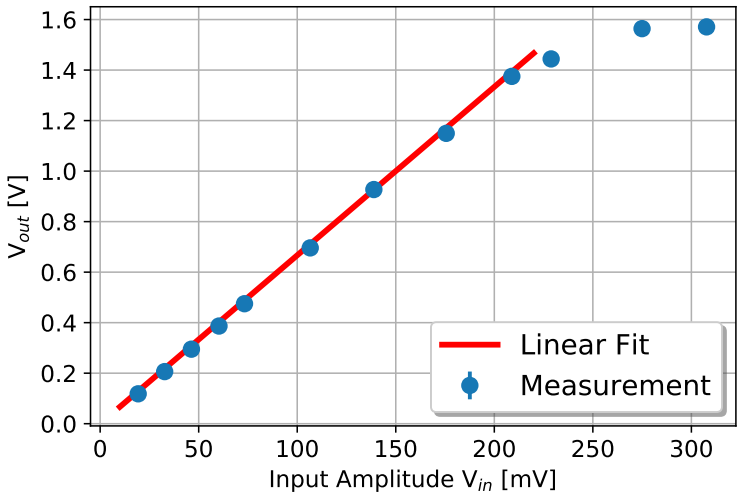

Figure 3.5: Variation of the output peak height for an given input amplitude V_{in}. Signal distortion is observed when the OPA is forced into saturation condition.

Finally, the curve slope has information about the gain. The linear fit results in a gain around 7, given by the ratio of test input capacitance over feedback capacitance (450 fF / 65 fF).

Ballistic Deficit (P)

The ballistic deficit is related to the incomplete charge collection by the amplifier, and needs to be characterized. The estimation of the ideal signal amplitude uses the previously defined parameters (V_{in}, C_{in}, C_F) to simulate the CSA output using the software TINA. Subsequently, the fitting of the measured signal (called *Signal Fitting*) is compared to the theoretical value (*Simulation*), as shown in figure 3.6.

The ballistic deficit estimation comes from the comparison to the simulation. However, the simulation takes into account parameters extracted from direct measurement, especially from the transfer function and the signal response. Therefore, the use of realistic parameters guarantees consistency. As shown in figure 3.6, the ballistic deficit is close to 100%, which means a minimal charge loss.

Noise (σ_{rms})

Another important feature of the front-end electronics is the noise performance. This parameter determines the minimum signal amplitude that can be distinguished from the background level. Here are presented two different methods to verify the system noise level.

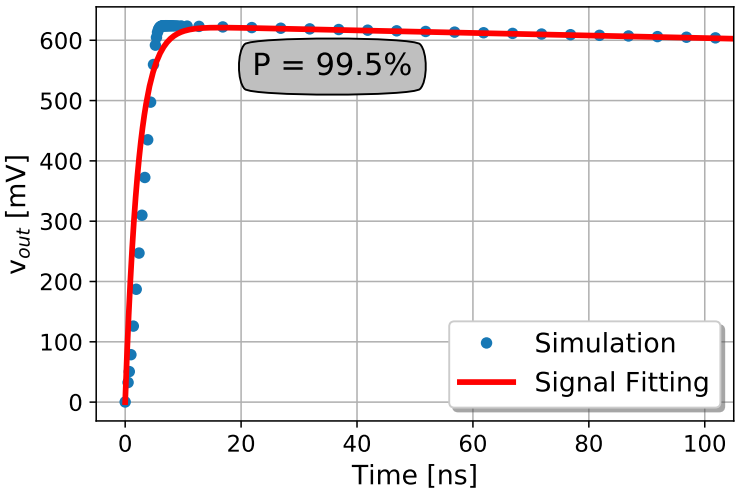

Figure 3.6: Effect of the ballistic deficit on the pulse height. A peak amplitude inferior to 2% compared to the theoretical signal is considered appropriate.

There are a number of noise sources within the OPA which contributes to increase the noise level, as discussed in chapter 2. Although they can be determined individually, measuring the total noise of the system represents a more important figure. The most simple method consists of shorting to ground (GND) the OPA inputs while recording samples at the output. After acquiring approximately 1000 samples of 10 μs time duration, the average voltage standard deviation of the set is calculated. This measure has a strong correlation with the system noise level.

The method described above represents an easy and quick verification measure. The precise estimation of the system noise level consists on applying the "*Sine-wave testing and fitting*" protocol, as described in the IEEE Standard 1241-2010 [30]. The IEEE Standard method probes the noise level in systems as the CSA [29]. The CSA response to a pure sine-wave is also a sine-wave with the same frequency, but with potentially different amplitude and phase. Applying a sine-wave with a proper frequency to the CSA causes the system noise to superimpose the output signal. The IEEE method implies fitting the the CSA output with a four-parameter sine wave function. Finally, the noise level is obtained from the standard-deviation of the fitting residuals (R) [30]. Mathematically, R is calculated as follow:

$$R = \sum_{n=0}^{N-1} [y(n) - A_0 \cos(2\pi f_0 t_n) - B_0 \sin(2\pi f_0 t_n) - C_0]^2 \tag{3.4}$$

with fitting parameter A_0, B_0, C_0 related to the sine wave amplitude, and f_0 the input frequency. Lastly, t_n is the nominal time associated with the *nth* data value.

Therefore, a sine wave of amplitude A_0, and frequency f_0 is injected into the systems. The posterior data evaluation utilizes an Matlab toolbox equipped with a graphical user interface. It is made available from Budapest University of Technology and Economics [31], as mentioned in the IEEE Standard. Exploiting this method, the noise contribution coming from the waveform generator and the one coming from the CSA circuit can be studied and treated separately.

Figure 3.7 shows qualitatively the sine-wave test method. The 10 μs frame duration is sliced into 5000 parts. The curve is fitted, and the standard deviation of the residuals reveals the noise level. Detailed calculation, and further information is shown in [30], Annex B.

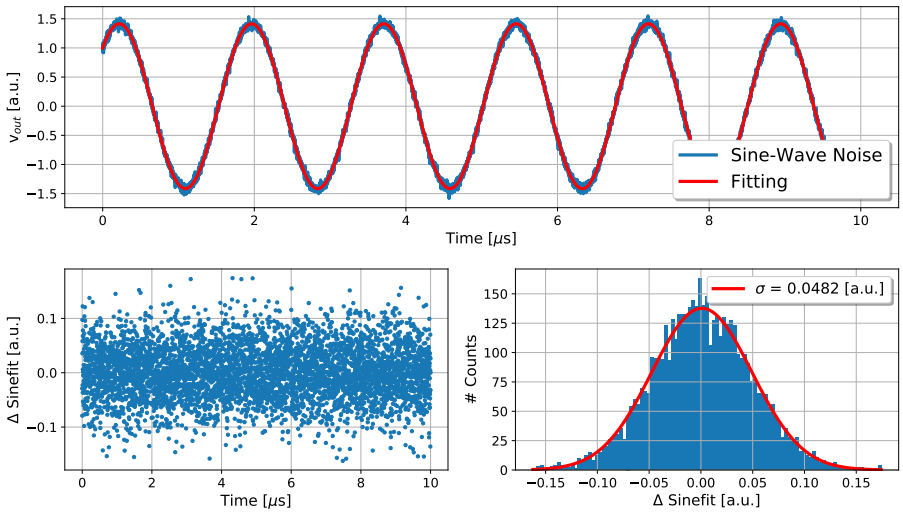

Figure 3.7: Example of noise measurement of the charge-sensitive amplifier using the sine-wave method. The noise is superimposed to the output signal [top]. The fitting residuals are presented in the time domain [lower left], while the standard deviation of the histogram plot [lower right] expresses the system noise.

3.2 Discussion and Results

This section focuses on applying the validation protocol described earlier. The objective is to define the best operational amplifier among the pre-selected ones highlighted in the Table 2.3.

The simulation and design phase indicates the candidates which are more reliable and offer better results, as summarized in Table 2.4. The main criterion is circuit stability, higher cutoff frequency, reduced ballistic deficit, and low noise level. Among the various possibilities, **OPA657** was preferred for the initial tests mainly because it has a large voltage supply rail ($\pm$5 V), i.e., a larger headroom until the output signal saturates. However, in addition to the higher input capacitance, the measured noise level is excessively high. The output signal is deformed with ripples superimposed to it.

The second tested component is the **OPA818**, a performance update for OPA657. With a similar voltage supply rail ($\pm$ 5 V), it shows a marginal gain in terms of product gain bandwidth (GBWP). However, due to a lower input capacitance, it has remarkable advantages compared to the previous version. Consequently, it has better noise behavior ($\times$2.3 smaller) and approximately $\times$7 faster response. The drawback of OPA818 is its package style (8-pins WSON DRG package). Despite the better insulation for electromagnetic interference (EMI), it is more susceptible to layout parasitic, besides being difficult to solder.

Although the **OPA859** has a GBWP in an intermediate regime (900 MHz), its performance is counterbalanced by its low input capacitance and voltage noise sources. It operates at $\pm$2.5 V supply, and made available exclusively in an 8-pins WSON DSG package. Similarly to the

OPA818, this package is difficult to sold and sensitive to layout parasitic. For these reasons, this circuit is easily induced to oscillations and is therefore discarded.

The next amplifier is the **ADA4817**. This component can be biased at ± 2.5 V or ± 5 V depending on the requirements. ADA4817 has the lowest GBWP value among all candidates (410 MHz), translated into the lowest noise level. However, ADA4817 shows a rising time close to 30 ns, inappropriate for the CSA architecture.

Finally, the CSA implementation with the **OPA858** shows the best performance concerning the studied parameters. Its internal design is optimized to meet specifically a wideband, low-noise amplifier for photodiodes. Despite the 8-pins WSON DSG package, and a supply rail of ± 2.5 V, the OPA858 has the largest GBWP, and ultra-low input capacitance, delivering the fastest response compared to any other candidate.

Therefore, the best results were achieved with OPA858 and OPA818 amplifiers. Table 3.1 summarizes the OPA performance in comparison to the simulations.

Table 3.1: Numerical estimation of the CSA electrical characteristics *vs* experimental comparison

	OPA858		OPA818	
	theory*	exp	theory*	exp
t_r [ns]	1.13	1.70 $\pm$0.025	2.02	2.63 $\pm$0.003
BW [MHz]	310.9	206.3 $\pm$3.04	173.3	133 $\pm$0.1
P [%]	99.5	99.4 $\pm$0.1	99.9	99.4 $\pm$0.1
σ_{rms} [mV]	1.07	4.80 $\pm$0.08	1.11	4.45 $\pm$0.21

*simulations held using parameters obtained from measurements

As can be seen from Table 3.1, the measured parameters diverge marginally from the TINA simulations. The observed mismatches can be understood assuming that C_{in} and C_F vary within some tolerance. In addition, the layout also influences the performance of the CSA and can be optimized. Nonetheless, the measurements confirm the proper functionality of the charge-sensitive configuration, besides confirming OPA858 having superior performance.

Although the approach using the parasitic capacitance is functional and integrates the charge [32, 29], its implementation revealed to be unreliable and difficult to reproduce. Therefore, a 100 fF capacitor can be soldered on top of the R_F resistor, reducing the parasitic capacitance, and ensuring the CSA functionality.

As noted in Table 3.1, the system parameters vary concerning simulations. The tested noise level, in particular, is higher than expected, and its contribution involves the capacitances C_{in} and C_F. Figure 3.8 evidence that a C_{in} value larger than 10 pF would generate a similar noise level as observed. This value is unrealistic even taking into account parasitic contributions.

The influence of the feedback capacitor is also investigated. The C_F contributes especially as a current noise source. Mathematically, the noise power density has a dependency described as:

$$i_{NPD} \sim \sqrt{\frac{1}{2\pi R_F C_F}}. \tag{3.5}$$

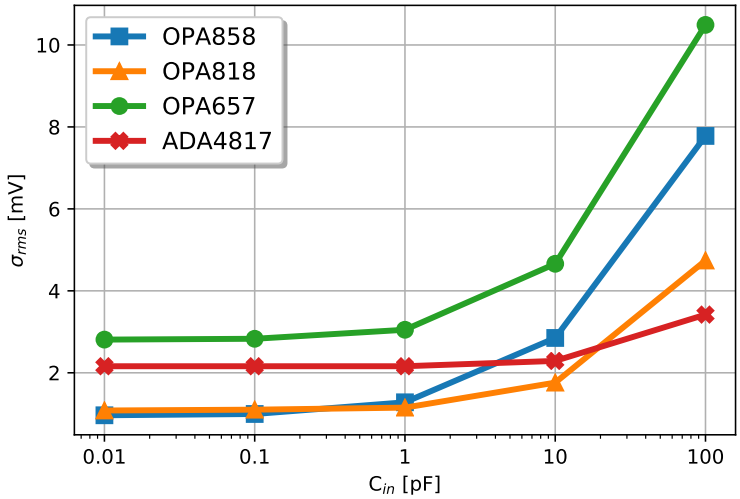

Figure 3.8: Dependence of the output noise level with respect to the input capacitance C_{in}. C_F assumed constant equal to 100 fF.

The complete dependency is expressed in equation 2.13. Figure 3.9 shows a measure evidencing the relation obtained in equation 3.5. As the C_F value is made larger, the noise level decreases. This behavior occurs since the system bandwidth is shortened. Thus, the measured noise level of about $\times 3$ higher than the simulation requires further studies to be optimized.

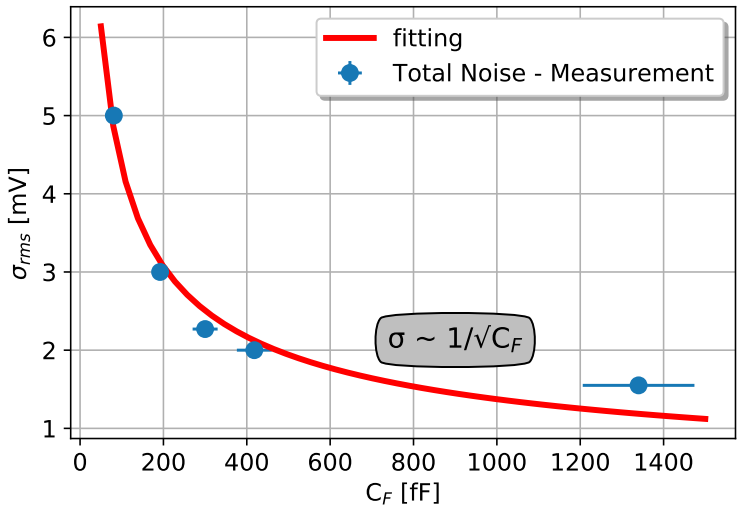

Figure 3.9: Simplified fitting model illustrates the noise level respecting the $1/\sqrt{C_F}$ trend. C_{in} assumed to be 400 fF.

During the characterization and validation phase, the role of C_F capacitor was proven. Its influence on the charge integration, in addition to its contribution to the noise level, was tested.

Concerning the amplifiers validation, the candidates highlighted on Table 3.1 show satisfactory performance. In particular, the OPA858 suggests being the ideal candidate for Charge-Sensitive configuration. In addition, the OPA818 is also a suitable candidate, especially because it has a wider output voltage swing. For this reason, both candidates guarantee the proper functioning of the front-end readout electronics.

Finally, the minimum signal that could be read at the output is equivalent to a charge of about 6.5 fC. This value is about $8\times$ larger than the signal generated by an X-ray source, but $5\times$ smaller than a pulse caused by a laser source. Thus, some extra precautions in the CSA design, and isolation of sensitive circuit parts, must lead to an even better signal-to-noise ratio.

Part II

Design of a Custom Sensor Housing

4 Feasibility Study of the Characterization Setup

"Simplicity is the ultimate sophistication"
Leonardo Da Vinci

THIS chapter presents the feasibility study of the characterization platform. After studying and validating the readout electronics, the thesis part II covers mechanical and thermal requirements for the high-Z sensor characterization setup. This investigation involves solutions for the heating and cooling of the sensor chip, a central element to characterize its electrical properties. It denotes a necessary implementation since the semiconductor transport parameters depend directly on temperature [33], as well as the stable response of the sensor.

4.1 Chips Prototypes & Interconnections

The CdTe sensors of the XIDER project need to be characterized, as previously emphasized. Instead of using a full reticule with thousands of pixels, the first test prototypes have a reduced area with a 4×4 pixel matrix. Specially designed for characterization purposes, these matrices permit to qualify three different pixel pitches (100, 200, and 300 μm). Figure 4.1 shows the prototype chip, which allows investigating the parameters variability for different pixel sizes.

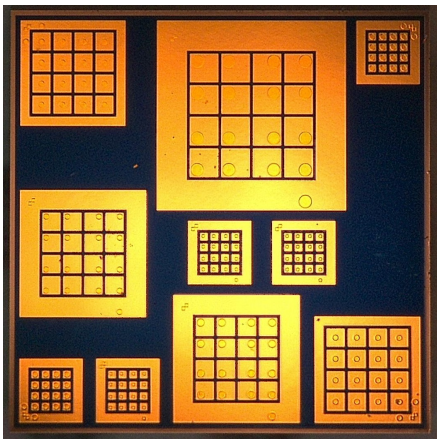

Figure 4.1: CdTe prototype chip has total area of 13×13 mm^2; the readout electronics is directly connected to each pixel. Adapted from [25].

The chip shown in figure 4.1 is bounded to the readout PCB via dedicated microelectronic interconnection methods, i.e., direct bump bonding. Since the stray capacitance loads the readout electronics and reduces its performance, the Charge-Sensitive circuit has to be placed as closed as possible to the pixels.

The PCB traces are elements that also increase the circuit load. Figure 4.2 shows the influence of the trace width with respect to the parasitics it introduces. The distance (H) between signal traces to voltage planes also plays a role to decrease parasitic contributions.

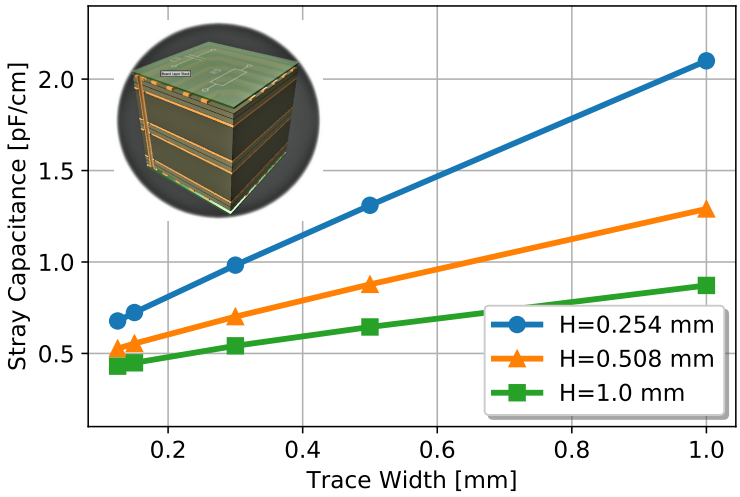

Figure 4.2: Separating GND/Power planes away from the signal traces reduce C_S drastically; trace width shows a minor impact for thin interconnections. Data gathered from Saturn PCB Toolkit [34].

4.2 Thermal Management

The sensor temperature influences the physical transport parameters of the semiconductor material. Heating and cooling the chip sensor for just a few degrees (ΔT=20°C) is sufficient to investigate its stability and robustness. As reported by Rivetti [19], the sensor leakage current doubles at every Δ8°C, causing significant shifts in the electronics DC operating point. Therefore, it justifies efforts to implement a temperature-controlled environment.

Peltier modules are a compact solution for alter the temperature of the sensor. The module comprises two ceramic plates separated by a semiconductor chip. When a current passes through it, a temperature gradient sets up according to the Peltier effect [35]. This causes one of the module's plates to become cooler, while the other side becomes hotter. In addition, these modules operate reversibly: in case the current polarity is inverted, the hot side starts cooling, and vice-versa.

The Peltier modules are rated according to the maximum current they handle. Consequently, this sets the maximum ΔT they produce. Compact solutions with comparable size to the sensor chip prototype (15$\times$15 mm^2 module), usually provide cooling capacity superior to 2 $\mathrm{W/cm}^2$, and a maximum temperature difference is ΔT=70 °C.

Despite controlling the sensor temperature, these modules cannot absorb heat. Hence, dissipating the heat at the hot surface is essential. A simple solution is the use of a heat sink element placed in contact to the hot surface by proper adhesion techniques. Figure 4.3 shows that the Peltier module transfers the heat to the sink. This sink has a large exposed area, and exchanges heat with the surrounding by convection.

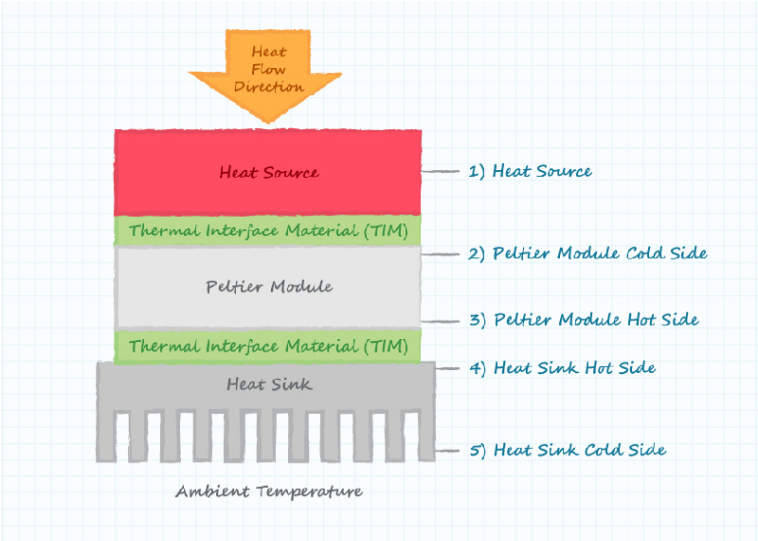

Figure 4.3: Peltier power dissipation system. Accurate thermal analysis requires dedicated simulation tools to understand the heat dynamics. Adapted from [36].

More sophisticated solutions can be explored. The use of water-cooled metallic blocks is recurrent. However, this thermal reservoirs are massive, and their fixing on the PCB is challenging. Therefore, Aluminum heat sinks are the simplistic option considering the total power they are able to dissipate.

In addition to the heat generated by the Peltier module, the readout electronics consumes electrical energy and dissipates heat. The heat disperses from the components through the circuit board or dissipates to the surrounding. Therefore, the characterization setup needs a forced-air cooling system since the natural heating exchange may not be sufficient.

The selection of the cooling fan implies understanding where and how much heat is generated. In the following, the airflow is calculated. Since the geometry of the system influences on how the air circulates to the surroundings, a rule of thumb is assumed. Considering a box with open periphery, the surface area (S) for heat exchange is given as follow:

$$S = 1.8 \times H \times (W+D) + 1.4 \times W \times D \ [m^2] \tag{4.1}$$

Equation 4.1 computes the side and top area of a rectangular box. The calculus depends on the frame width (W), height (H), and depth (D). Finally, the required air flow (V) can be empirically estimated as:

$$V = \frac{1}{20}\left[\frac{Q}{\Delta T} - U \times S^2\right] \times S_F \ [m^3/min]. \tag{4.2}$$

In order to give the reader some estimation concerning the characterization setup, a temperature variation ΔT=20°C is assumed. The total heat (Q) is the sum of the Peltier module (5 W) and the electronics dissipation (overestimated to 15 W). The heat transfer coefficient (U) represents the air capacity to exchange heat, equal to 25 $W/(m^2\ K)$. Finally, S_F is a safety factor, chosen to be equal to 2. Applying equation 4.2 to a rectangular box of geometry $100\times100\times100\ mm^3$, leads to a necessary air-flow of 0.1 m^3/min.

4.3 Mechanical Design of Custom PCB Holder

This section studies the mechanical assembly of the characterization setup. After validating the Charge-Sensitive readout, and formulate the thermal management, the sensor housing is the last element to be addressed. Qualitatively, the casing protects the sensor chip from impacts and scratches that may damage it. It also holds the electronics and necessary cabling for the electronics supply.

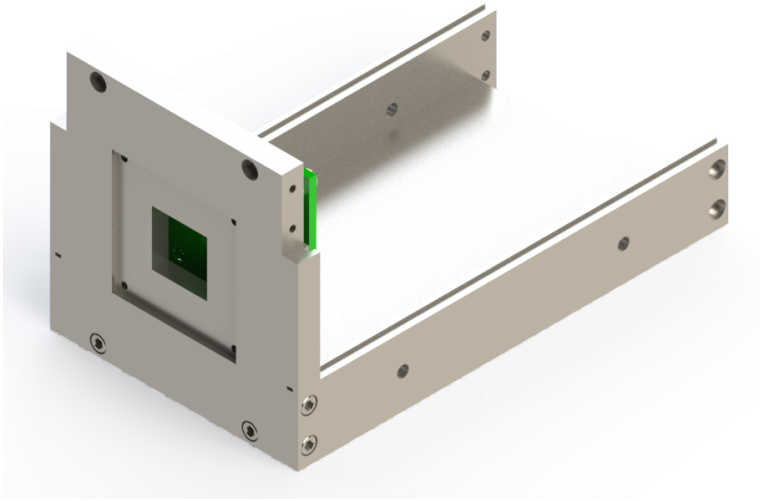

Figure 4.4: Assembly of the characterization platform. The sensor is exposed externally through a opening on the front-frame, while the readout electronics remains hidden inside the housing.

As is shown in figure 4.4, the frontal frame has an opening to expose the sensor to the beam. This frame has an undercut to accommodate a translucent material, possibly vitreous carbon or a Kapton foils. These materials are made of light elements (mainly carbon), which are essentially transparent to X-ray photons. This protection prevents the sensor from being damaged, and against undesirable external light that may arrive at the semiconductor and generate free carries.

Figure 4.5 [left] shows the aluminum heat sink glued directly on the Peltier module (hidden). Fully assembly stacking is schematically presented in figure 4.3. It also exhibits electronic components related to the circuits power supply and the sensor biasing, despite high-speed connectors placed on the periphery of the board. These elements conduct the signal from

different pixel pitch to the CSA readout electronics, placed on another PCB. Finally, figure 4.5 [right] shows the cooling fan placed at the rear of the casing.

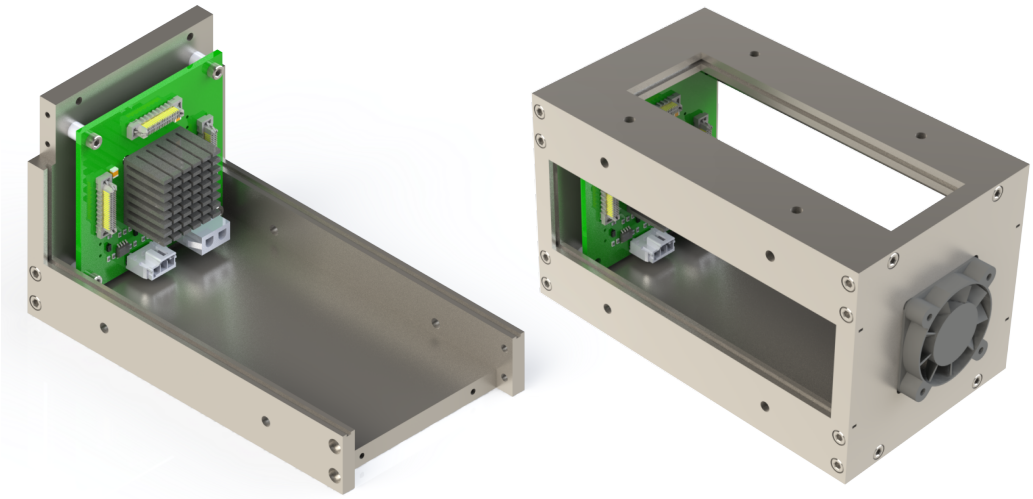

Figure 4.5: Power supply components are placed at the bottom of the sensor board; high-speed connectors on the periphery bring the sensor signal to the readout circuit, placed on a distinct PCB. The cooling fan makes turbulent the air inside the case, facilitating heat exchange.

The chosen high-speed connectors permit boards to be assembled in a 90° arrangement, as shown in the inset of figure 4.6. Therefore, the readout board with the Charge-Sensitive Amplifiers are mounted perpendicularly to the sensor board, saving space of the casing design. Figure 4.6 also shows the connectors used to plug the amplifiers to the oscilloscope from the side of the sensor housing. The housing box is then closed with thin metallic plates to shield the electronics against electromagnetic interference.

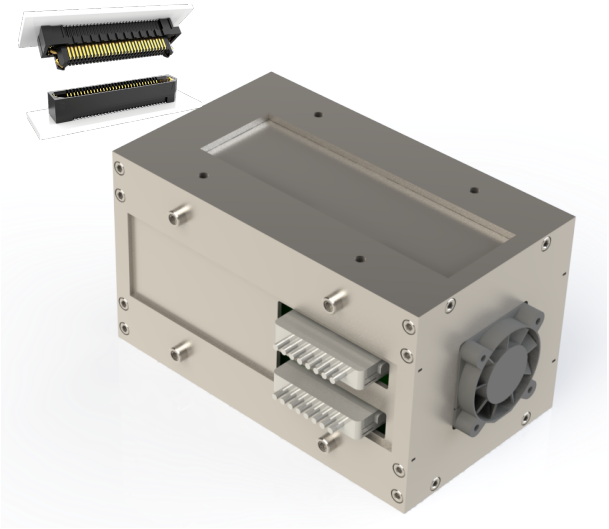

Figure 4.6: Final drawing of the sensor case. The chosen dimensions depend mainly on the fan and connectors, and can be easily adjusted according to their availability with suppliers.

The external rigid frame facilitates the handle of the characterization setup. It holds the readout electronics with an easy connection to the oscilloscope. Despite delays caused by the COVID-19 pandemic, the sketch shown in figure 4.6 should serve as a pilot design for the final characterization setup.

Conclusion

5

The European Synchrotron Radiation Facility (ESRF) has recently undergone an update program. This gave rise to the first fourth generation high energy source in the world, called ESRF-EBS (Extremely Brilliant Source). The improvement in the beam characteristics implied in the necessity for new instruments capable to cope with brighter and more coherent beams. In particular, the detectors' absorption efficiency for high energy photons needs to be enhanced compared to standard Silicon-based sensors used nowadays.

The goal of this thesis was to develop a characterization setup for compound semiconductor sensors. These materials show adequate detection efficiency to operate at the 30 - 100 keV energy range. However, their performance is evolving, so their electrical characterization is of core importance for the XIDER chip design.

The thesis is subdivided into two main parts. Chapter 2 is focused on the study and simulation of a dedicated readout chain based on a limited number of amplifiers. The results are optimized in terms of bandwidth, ballistic deficit, and noise performance. Chapter 3 shows the experimental validation of the Charge-Sensitive circuitry, and reveals the OPA858 as the best low-noise amplifier to be used in the sensor qualification readout.

The thesis Part II focus on the implementation not only the electronics functionality, but thermal aspects related to electronics stability, as well as the heating and cooling of the sensor. Moreover, mechanical elements are explored, while the proposed house-frame ensures the easy handling of the setup.

Because of the COVID-19 pandemic, the effort on Part I was emphasized, while the Part II became a feasibility study. Nevertheless, the readout system was extensively studied, while thermal and mechanical concepts addressed. Therefore, the qualification setup is validated, ready to be implemented in the coming months.

Annex

6

6.1 Annex A

Charge-Generation using a Laser Source

On chapter 2, the carrier generation using infrared light was discussed. This section describe briefly the current estimation.

Considering a 100 μW laser source, with pulse duration of 5 ns, the number of photon per pulse is given by:

$$N_{ph} = \frac{P \cdot T}{E_{ph}} = \frac{P \cdot T}{\frac{hc}{\lambda}} = \frac{100\,\mu W \cdot 5\text{ ns}}{\frac{hc}{830\text{ nm}}} \tag{6.1}$$

where h is the Plank's constant (6.62×10^{-34} m^2kg/s), and c is the speed of light (299792458 m/s). Substituting this values in equation 6.1 leads to 2.1 million of photons per pulse. However, supposing that only 10% of the photons contributes to generate carries within the sensor, the total charge is given as:

$$Q = N_{ph} \cdot \eta \cdot e = 2.1\times10^{6} \cdot 0.1 \cdot 1.602\times10^{-19} \tag{6.2}$$

Thus, 210000 carriers contribute to generate a charge of 33 fC. Considering a typical carrier drift time t_D = 50 ns, the current coming out from the sensor is 33 fC / 50 ns = 670 nA.

6.2 Annex B

Field-Shunting Layout

It worth noting that the two endcaps of the feedback resistor package (R_F) introduce a parasitics capacitance called *Miller capacitance*. Modeled as a parallel plate capacitor, this parasitic contribution derives from geometric aspects, and can easily overcome the targeted C_F $\sim$100 fF value.

Not only is the separation of the endcaps is responsible for unwanted capacitances, but also the area of the pads. Therefore, although the longer SMD packages decrease the parasitic capacitance (from 0603 to 0805 family), they also have a larger pad area. Such effect compensates for the gains in increasing the distance between the endcaps, making it difficult to get rid of parasitics.

However, the choice for longer packages is justified, considering that it facilitates the application of another technique to reduce the capacitance. Adding a ground trace under the feedback resistor shunts the lateral side **E** field, dumping it to ground, as shown in figure 6.1. Therefore, most of the capacitance is now in the PCB insulating layer ($\epsilon_r \sim 4$) and *not* through air. Such *field-shunting* technique is able to reduced the above mentioned 100 fF down to 12 fF [32].

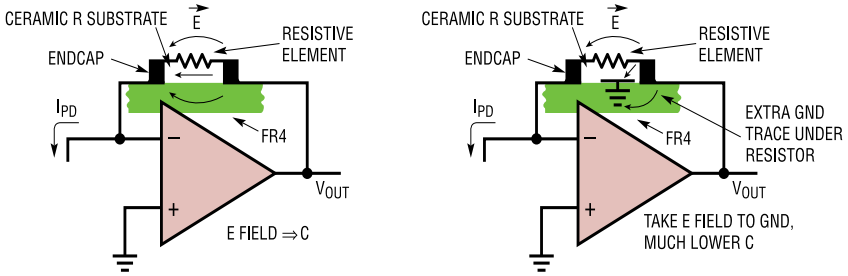

Figure 6.1: Normal layout (left) and Field-Shunting layout (right); minimal pad sizing and enhanced layout reduces *Miller capacitance*, extending bandwidth and improving noise performance. Adapted from [32]

7 Bibliography

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