POLITECNICO DI TORINO

Department of Energy

Master Thesis in Electrical Engineering

Hardware Design and Testing of a 50 kW T-Type Active Rectifier for Fast Charging Applications

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Summary

This thesis deals with the schematic and PCB design process of the active front-end (AFE) for a 50 kW ultrafast battery charger for electric vehicles. Ultrafast chargers are and will increasingly be a key technology, being at the heart of the transportation electrification.

The thesis work has been carried out in collaboration with the interdepartmental Power Electronics Innovation Center (PEIC) at the Politecnico di Torino and it consists of the detailed hardware design of the AFE, from its schematics to the final printed circuit boards (PCBs) and the testing of the converter.

The hardware development of this prototype is a work carried out in sequential stages and has required transversal engineering skills, both electrical, electronic and mechanical. In fact, the process started from the theoretical study phase of the active rectifiers, going through the design of the schematic and PCBs, until the assembly and testing of the boards.

Alla mia cara nonna Maria Teresa

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Chapter 1

Introduction

1.1 Goals and Structure of the Thesis

The goal of this work is the design, assembly and testing of an Active Front End prototype for an off-board battery fast charger. The thesis has been carried out in collaboration with the interdepartmental *Power Electronics Innovation Center* (PEIC) at the Politecnico di Torino.

This thesis deals with the detailed hardware design of a 50 kW AFE[1], from its schematics to the final Printed Circuit Boards (PCBs) and the testing of the converter. Therefore, the thesis has been divided into the following chapters:

1. Introduction
   - 1.1 Goal of the thesis.
   - 1.2 Theory review: summary of the main charger structures and main project specifications.
2. Hardware Design
   - 2.1 Description of the system and introduction to Altium Designer (adopted electrical CAD software).
   - 2.2 Design of the schematics and components choice.
   - 2.3 Design of the Printed Circuit Boards.
3. Preliminary Testing and Assembly of the Converter.
4. Conclusions: summary of the main results obtained and skills acquired.

[1] Active Front End (AFE)

The design of a converter requires time an resources. In fact, it is an iterative process of continuous development and improvement in its every aspects (hardware, control and testing). This activity needs coordination and interaction between the members of a research and development team. This was also the case for the converter in my thesis. I contributed to a part of the development of the project, with the task of hardware design. In particular, I took care about the realization of the schematics and PCBs, the definition of the BOM[2], the assembly of the components in the laboratory and the prototype experimental validation. During my thesis period I worked both with my supervisors and with other members of the team, with whom objectives, specifications and modifications of the various parts of the converter have been discussed.

The activities I carried out followed a defined time process, starting from an initial training phase in which I studied from a theoretical point of view the functioning of PFCs[3] and Active Rectifiers and then I learnt the basis of the electrical CAD software Altium Designer 20. Subsequently, I was involved in the realization of the schematic diagram of the converter boards, where I chose and designed the needed electronic components. Afterwards, once the electrical schematics were defined, I performed the design of the PCBs (later checked and finished by PEIC team members Stefano Borlo and Fabio Mandrile, who supervised me during my thesis work). Then I created the lists with all the components to be acquired, called Bill Of Materials, which has been used to complete the purchase orders. At the end of these activities, I had access to the laboratory at the Politecnico di Torino in order to proceed with the assembly of the converter and the preliminary experimental verification tests.

[2]Bill Of Materials (BOM)

[3]Power Factor Corrector (PFC)

1.2 Battery Chargers for Electric Vehicles

The second decade of this century was marked by a technological revolution, the development and evolution of electrification of vehicles, both with hybrid (PHEV) and fully electric (BEV) solutions. This is mainly due to the increasingly stringent regulations in terms of pollutant emissions, a topic that is becoming relevant and an important part of the public debate in recent years. In fact, electric vehicles are a viable solution to reduce the emissions of CO2, NOx and PMs. Moreover, the energy production and its consumption are not coupled anymore. In fact, the electrical energy for mobility can be generated by high efficiency thermal plants or renewable sources. Therefore, it is expected that the future will be increasingly marked by this type of traction. Hence, an essential element for the functioning of these technologies is the energy source, the battery.

Batteries require stringent specifications, in particular high durability and low recharging times. In case of electric and even hybrid vehicles, although with less weight, the issue of the batteries and their recharge has become the focus of companies, universities and consumers. In fact, the main problem is the time needed to recharge batteries with an increasingly high capacity, necessary to guarantee the autonomy. Therefore, it is precisely in this area that off-board chargers have been developed with the possibility of recharging with high power direct current, which make it possible to drastically reduce charging times. These devices are at the centre of a continuous innovation both in terms of structure and components and are one of the key elements in the technological evolution of electric propulsion.

1.2.1 Types of Charging of Electric Vehicles and PHEVs

The battery charger is an electronic power converter whose main purpose is the transfer of electrical energy, through a regulated conversion, from a source, which is usually represented by the electric grid (distribution, domestic or local micro grid), to a load, which is represented by the battery of an electric vehicle (BEV) or plug-in hybrid (PHEV).

Considering the state of the art, many structures with different features for the chargers have been proposed.
Hence, it will be listed a classification of the main features of such devices.

The charging of BEV and PHEV vehicles differs from the type of connection between the battery and the source, which can be of three types:

1. **AC conductive**: the connection is between the AC mains and the battery, with AC/DC and DC/DC conversion stages.

2. **DC conductive**: the connection is made in direct current. In this case an external battery charger is required because of the typical power ratings, in order to perform the AC/DC conversion and ensure the electrical isolation. Then the DC connection between the DC supply and the battery is possible, where voltage and current is a function of the energy required by the battery itself.

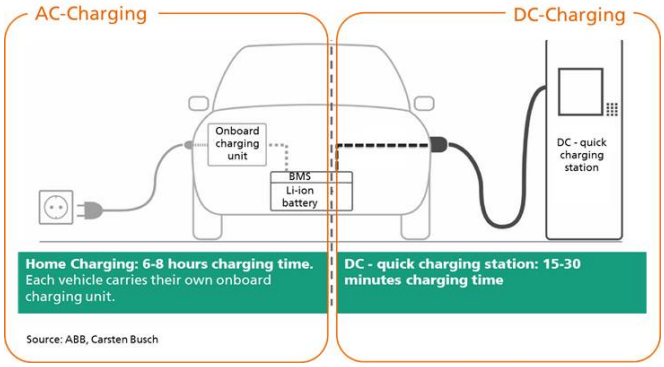

Figure 1.1: Conductive AC and DC charger example [1].

3. **Inductive (Wireless)**: it can be seen as a transformer with magnetic circuit in air and high frequency transmission, with primary and secondary represented respectively by windings in the ground and on board vehicle. The schematic principle of this charging mode is depicted in Fig.1.2.

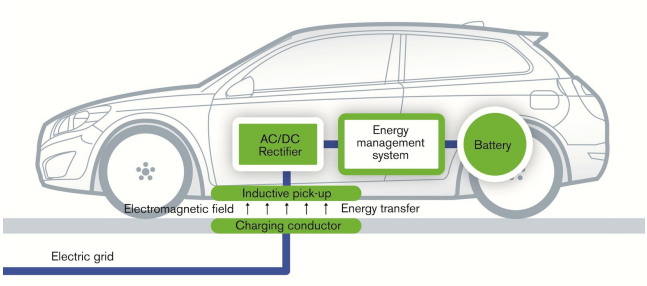

Figure 1.2: Wireless charger example [2].

Regarding conductive charging, the standard IEC 61851 [3] defines four charging modes, each one linked to physical connection (sockets and plugs), electrical features (voltage and power levels) and communication protocols.

- **Mode 1**: domestic AC charging or private charging of small vehicles, with typical powers from 1 to 4 kW (current less than 16A) and connection to the

grid via domestic or external socket and on board battery charger. Mandatory in every vehicle for emergency situations.

- **Mode 2**: AC charging via both domestic and public networks, where an on board battery charger is needed.
- **Mode 3**: AC charging, with typical power ratings of 3-6-7-11-22 kW and available in public charging stations, private wall-boxes or industrial charge.
- **Mode 4**: high power DC charging through off board charging stations, with power up to 400 kW.

	AC-charging Wall outlet	AC-charging Wall outlet IC-CPD	AC-charging Wallbox	AC- public charging-station	Inductive charging	DC-charging
Mode	1	**2**	**3**		-	**4**
Standard		IEC 62752/UL 2231	IEC 61851-1/-21/-22		IEC 61980-3	IEC 61851-23
Power class	max. 1ph 16A (3.7 kW) max. 3ph 16A (11 kW) max. 3ph 32A (22 kW)		max. 1ph 16A (3.7 kW) max. 3ph 63A (43 kW)		2...5 kW 11 kW	25 kW-400 kW
Connection	Schuko	Schuko	CCE		Schuko / CCE	
Communication	none	Control Pilot	Control Pilot / Power Line		Wireless	Power Line

Figure 1.3: Charging modes [4].

It can be observed that these ways of recharging differ mainly according to the available powers, leading to different charging times. In fact, the time needed is reduced as the power increases and the recharge with the highest power is called fast charge, i.e. belonging to Mode 4 and it is available in public charging stations with off-board battery charger. The DC fast charge allows a strong reduction of charging times, meeting the needs of consumers because it is designed thinking to applications where long distances are travelled and allows two main issues to be resolved:

- Battery with limited autonomy;
- Range anxiety due to long recharge time.

1.2.2 Battery Charger Structures

In general a battery charger is a converter made up of several stages in series, which regulate the charging process. It ensures high efficiency in order to reduce losses and therefore charging costs. Hence, as shown in the figure below it is composed by AC/DC conversion stage, connected to a capacitive DC-link that allows the connection to the battery mediated by a DC/DC converter.

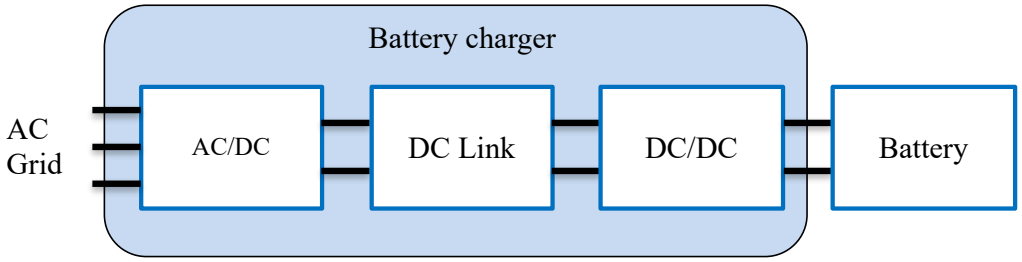

Figure 1.4: General charger scheme.

Each of these stages can perform tasks and have different characteristics, leading to the following classification:

- Conductive and inductive charging.
  A first classification can be based on the type of electrical energy transfer, which can take place through a physical connection with conductors between the mains and the battery, or through inductive charging. In both cases there is a physical separation between the two parts of the converter, in which energy is transferred by a high frequency resonant (HF) system. Usually for inductive recharge, it is not possible to achieve high efficiency due to the dispersed flux and this leads to higher costs. However, in this case the charge can be done either with the vehicle stationary or in motion, with a system of coils buried in the road.

- Unidirectional and bidirectional battery charger.
  A converter is defined unidirectional if it allows the transfer of energy in one direction only. This means for the battery charger that the power direction goes from the mains to the battery (G2V). However, if the layout of the converter is changed, accepting an increase in cost and complexity, it is possible to create a bidirectional structure Fig.1.5, which allows the transfer of energy in both directions, even from the battery to the mains (V2G). In this case it is necessary to avoid battery degradation generated by frequent charge and discharge cycles [5].
  However, the implementation of V2G can bring multiple benefits. In fact, improvements to the stability of the electric grid are expected. Electric

vehicles (whose batteries can provide energy immediately available) connected to the grid, contribute, together with the resources distributed throughout the territory, to form a storage network that can transfer energy in case of necessity for the national or local grid. Indeed, the V2G could have the following main advantages:

- Possibility of strongly reduce power consumption peaks from the mains and aim at the average value;
- Possibility of implementing frequency regulation with inertial support when the network frequency moves away from the set-point;
- Make voltage regulation through reactive power control.

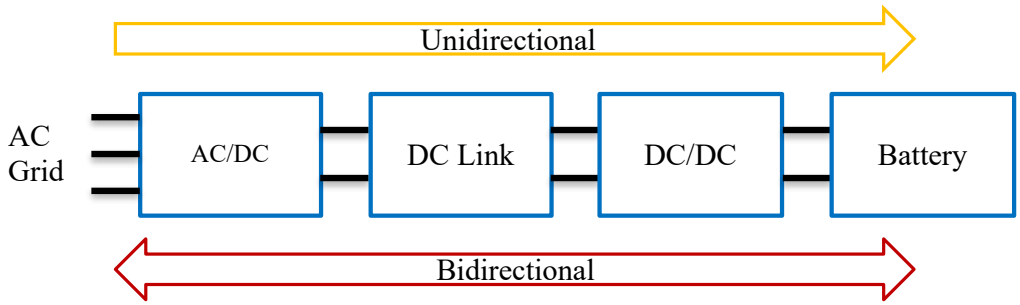

Figure 1.5: Unidirectional and bidirectional battery charger scheme.

- On-board and off-board charger.
  This characterization is related to the position of the charger in relation to the vehicle and it is based on the power of the converter. If the charging type is single-phase or three-phase, with low power, the battery charger tends to be on-board, due to its small size, so the possible charging modes are 1 and 2. On the other hand, if the exchanged power rises it is necessary to use an off-board, AC or DC battery charger (fast and ultra-fast charging). In this case, charging mode 3 is possible.

- Charging levels of battery chargers.
  - Level 1: low power 1-4 kW where slow single-phase on-board charger is used (mandatory).
  - Level 2: medium power 4-22 kW both single-phase and three-phase charger, with charging times shorter than the previous case but still of the order of hours, used in public or industrial environments where an on-board charger is required.

– Level 3: high power 22-450 kW both three-phase AC and DC charger, in the case of fast and ultra-fast charging, with reduced charging times, used in public and industrial environments where an off-board charger is required.

Table 1.1: Levels of charge.

Power Level Types	Charger Location	Typical Use	Expected Power Level	Charging Times	Vehicle Technology
Level 1	On-board	Homee	1.4kW (12A)	4-11 hours	PHEVs (5-15 kWh)
230 Vac (EU)	1-phase		1.9kW (20A)	11-36 hours	EVs (16-50kWh)
Level 2 (Primary)	On-board	Private	4kW (17A)	1-4 hours	PHEVs (5-15kWh)
400 Vac (EU)	1 or 3 phase	or public outlets	8kW (32A)	2-6 hours	EVs (16-30kWh)
			19.2k (80A)	2-3 hours	EVs (3-50kWh)
Level 3 (Fast)	Off-board	Filling station	50kW	0.4-1 hour	EVs (20-50kWh)
(up to 600 Vac or 800 Vdc)	3-phase		100kW	0.2-0.5 hour	

1.2.3 General Information on Battery Systems

The output of the system is the battery pack of an electric vehicle. It generally consists of cells of the same type, in order to ensure uniformity of voltage and energy consumption. The battery cells can be connected in series, to obtain the desired DC voltage level, and in parallel, for ensuring sufficient discharge current for the application. The specifications of a cell are related to the type of chemistry and usually for BEV, the lithium polymer cell is adopted. Its main characteristic is the energy density, compared to other cells, such as those used in PHEV, but lower power density. The nominal state of charge is measured by the capacity, which is usually expressed in Ah (charge necessary to provide a certain constant current in one hour) and represents the energy that can be extracted from the cell under specific conditions. The following figure shows the trend of the cell voltage as a function of the capacity. It is suggested not to go above a maximum value of Depth of Discharge (DoD), which is defined as the share of power supplied by the battery, in order to increase the number of cycles that the battery can perform and therefore the life of the battery (usually 80% DoD).

On the other hand, with regard to the behaviour when the battery cells are charged, Fig.1.7 shows the initial constant current (CC) area, where the battery voltage is at its minimum and the maximum current is supplied to the cells. Once the cell voltage approaches the maximum, the current supplied by the charger must drop down to its minimum, even to zero, and this is an approximate constant voltage zone (CV). This is the charging profile needed by the battery and must be guaranteed by the charger.

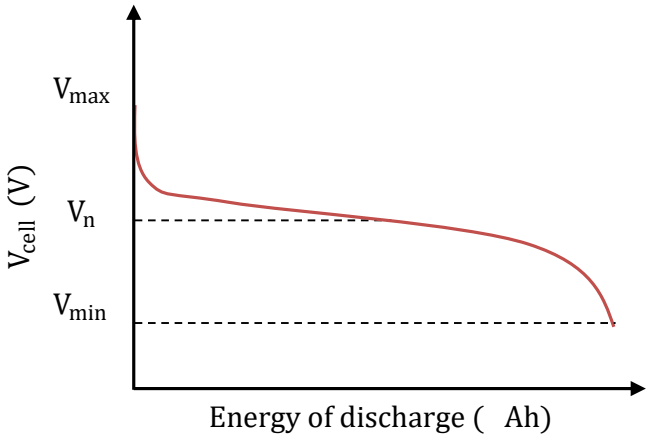

Figure 1.6: Cell discharge.

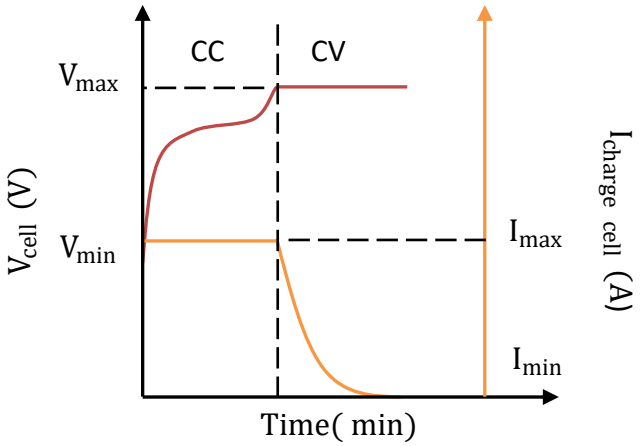

Figure 1.7: Battery cell charge.

1.2.4 Active Front End and Main Structures

The stage of the battery charger that interfaces to the power grid and allows the conversion from alternating current to direct current (AC/DC), is called Active Front End (AFE).

This terminology denotes the structure that performs the AC/DC conversion, which is composed by an active rectifier or Power Factor Corrector (PFC), which instead of being formed by diodes only, which cannot be controlled, is composed of controlled transistors (MOSFET, IGBT). Moreover, being an application that interfaces with the mains, it is subject to the power quality standards, with

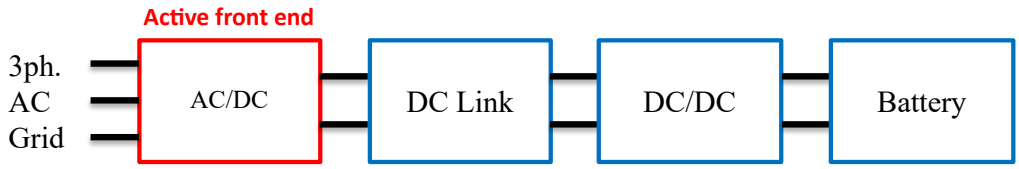

Figure 1.8: Charger block scheme with AFE.

particular reference to THD[4], which must not exceed 5% [6]. Moreover, in the application taken into account, which considers V2G, bi-directionality and the regulation technique with Pulse Width Modulation (PWM) techniques are adopted.

Starting from the classical two levels three phase inverter, three variants of the structure, developed by the buck converter and the three phase rectifier are presented [7], [8]. These have in common three identical bridge legs connected to a DC-link separated in two parts by a mid-point. Therefore the AC input can be switched so to be connected to the DC-link terminals or to the mid-point itself.

Three-Phase Inverter with Two Levels

It is a bidirectional structure with only two instantaneous modulation levels available and current independent phase voltage formation. It uses six controlled switches. The semiconductors are subjected to the full DC-link voltage.

This structure has the minimum number of components and has low conduction losses but does not allow the adoption of DC-link balancing techniques.

[4]THD or Total Harmonic Distortion is a power quality indicator that measures the total harmonic distortion of an electrical quantity. It is defined as the ratio between the Euclidean sum of the RMS values of the harmonics of the electrical quantity (voltage or current), excluding the fundamental and the RMS value of the fundamental.

$$THD = \sqrt{\frac{\sum_{n=2}^{\infty} X_n^2}{X_1^2}}$$

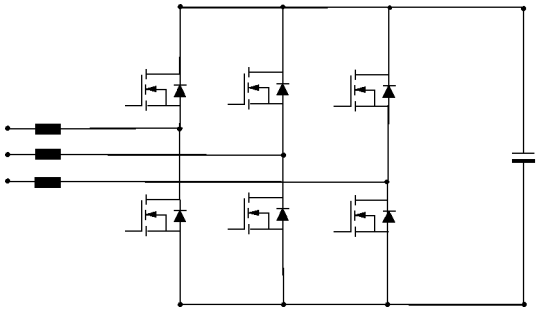

Figure 1.9: 2 Levels Three-Phase Inverter.

Three-Switch Inverter

It is a structure with three switches in which each transistor is combined with four diodes that switch to the fundamental frequency and it can be bidirectional. The connection with the real mid-point of the DC-link is made possible and this allows the regulation techniques with third harmonic current injection which balances the voltages with respect to the DC-link mid-point. In this layout the transistors are subjected to half the voltage of the DC-link, however there is the disadvantage of having a high number of components, that in conduction introduce voltage drops and losses and whose connections introduce additional parasitic inductances in the switching mesh.

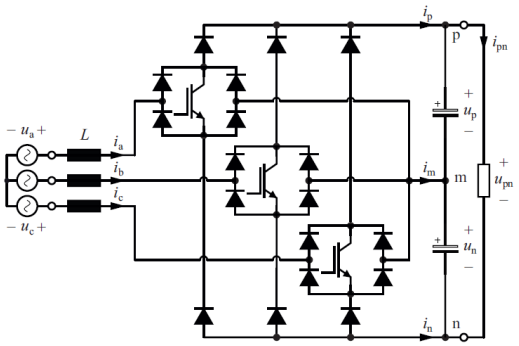

Figure 1.10: Vienna Three-Switch Inverter [8].

Three-Levels T-Type Inverter

It is a bidirectional structure with 12 active switches, which minimizes the number of components in ensuring both three-level modulation and DC-link voltage balancing by injecting current to the homopolar sequence (zero sequence current). In conduction, the current flowing in the DC-link only passes through a transistor

and together with the possibility of having three levels of modulation allows the lowest losses. The connection with the mid-point is made by two switches in series that make possible the bidirectionality of the connection. The components of the inverter legs must support the entire DC-link voltage.

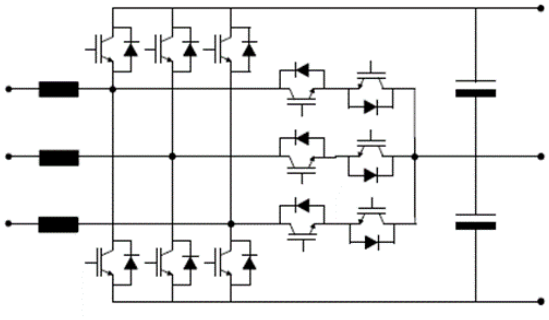

Figure 1.11: Vienna Three-Levels T-Type Inverter.

Three-Levels Neutral Point Clamped Inverter

It is a bidirectional structure with 12 active switches, similar to the Vienna T-Type in which are added 6 diodes that allow to halve the voltage rating of the transistors, which must support half of the DC-link voltage in interdiction. Also in this case low conduction losses are possible, thanks to the three-levels modulation.

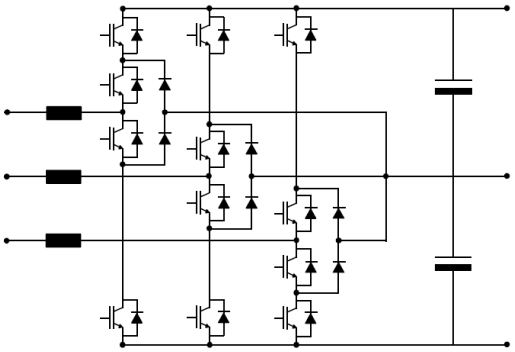

Figure 1.12: Vienna Three-Levels Neutral Point Clamped Inverter.

1.2.5 Active Front End Object of the Thesis

The converter, object of this thesis, is an Active Front End 3 Levels T-Type Inverter and represents the AC/DC stage of an ultra fast battery charger. The choice of this layout is mainly due to the better ratio between costs and benefits, made possible

by the T-Type structure for the desired application.
The main specifications of this converter are shown in the following table.

Table 1.2: Converter's main specifications.

Parameter	**Value**
Rated Power	50 kW
Phase Voltage	230 V
Maximum Phase Current	72.5 A_{rms}
DC-link Voltage	800 V
Switching Frequency	72 kHz
Maximum Estimated Efficiency	99.5 %
Maximum Power Losses	500 W

The rated power of the converter, which can be assumed to 50 kVA, is suitable for fast charge applications for electric vehicles. In addition, this converter can be combined with others to create a modular structure and increase the power available for DC conductive charging, reducing charging time for all types of vehicles, including those for public transport and logistics.

The connection is with the LV distribution grid, hence it is a 230 V phase voltage system.

This choice gives a a maximum input phase AC current that can be calculated as follows:

$$\hat{I}_{AC,in} = \frac{2}{3} \cdot \frac{S}{\hat{V}_{ph}} = \frac{2}{3} \cdot \frac{50.000}{\sqrt{2} \cdot 230} = 102.5 A_{pk} = 72.5 \ A_{rms} \tag{1.1}$$

Where:

- $\hat{I}_{AC,in}$: maximum peak input phase AC current.
- S: apparent power (VA).
- $\hat{V}_{ph}$: peak phase voltage (V_{pk}).

Due to the high current value, it is necessary to design an inverter structure with parallel legs. In fact, the inverter is made with an input stage containing the part of the filters, protections and pre-charge, while the power part is divided into two equal subconverters, operating in parallel and coupled through common and differential mode inductors.

Therefore, the phase current is halved and this affects both the choice of power components, the rating of the protections and the controllability itself. Furthermore,

the inductive coupling allows the interleaving of the legs.
Interleaving is the management of the modulation of the two legs in parallel with a phase shift angle that can be selected at will. This allows to obtain advantages both from the point of view of efficiency and the sizing of the reactive components. In fact, the choice of having a phase shift of 180°, i.e. a half period between the operation of the two legs in parallel, causes a ripple frequency twice the switching one, ensuring lower losses and reactors with reduced dimensions. The fact of having more legs allows to further exploit the interleaving as the current is divided by the number of legs, while the ripple frequency is multiplied.

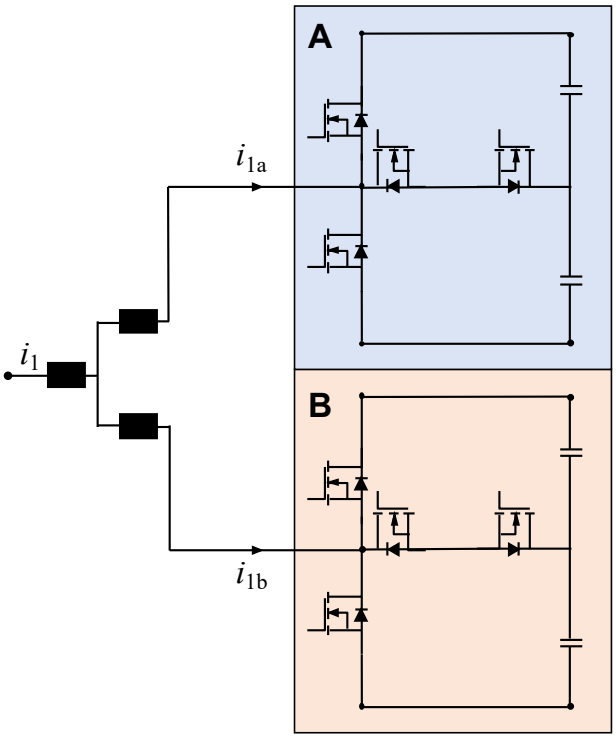

Figure 1.13: AFE Phase.

The DC-link has a voltage of 800V because the converter works with zero mid-point current modulation, which adjusts and balances the DC-link voltage between the two potentials with respect to the mid-point.

The desired switching frequency is 72 kHz and the main reason is related to EMI limits. With an interleaved leg control, odd harmonics are cancelled and only the even multiples of the switching frequency remain, bringing disturbances to frequencies above 144 kHz [9]. Furthermore, the choice of the switching frequency requires the use of SiC MOSFETs, which are suitable for high frequency switching

and in boost mode of the converter, obtains a strong reduction of reverse recovery charge, lowering the losses. In addition, these transistors are inherently bidirectional due to the body diode. This also reduces losses by working in a controlled and fully bidirectional way in both the first and third electric quadrant.

Ultimately, the decision to design a high power Active Front End (AFE) for ultra fast charging bidirectional applications is linked to the fact that the increasing spread of battery-powered vehicles will lead to a series of upgrades of the existing power grid, opening up to new scenarios of interchange between the power grid and vehicles and renewable resources or local storage. This solution provides greater flexibility in the creation of fast charging stations for electric vehicles, with the possibility of integrating the power required from the grid with energy located in storage systems that can help to reduce the peak loads of the grid. In addition, bi-directional structures can generate new scenarios for the management of the electric grid, being integrated in energy regulation in the same way as the converters of renewable sources. In this way, it becomes possible to use the energy stored in the batteries of the fleet of electric vehicles to regulate the grid voltage level, reducing the harmonic pollution of the voltage. Moreover, batteries and chargers can be used, through advanced control techniques, to regulate frequency and support short-circuit currents during faults in order to make the distribution grid more stable [10].

In the next chapters, the design of the converter will be discussed in more detail. The organization of the conversion structure will be first analysed, with an explanation of the project on Altium Designer software. Afterwards, the schematics of the boards, the design choices and the components will be deepened. Then there will be a chapter in which the guidelines and steps for the creation of the converter PCBs will be studied. Finally there will be two conclusive chapters, one containing the construction of the prototype and the experimental validation of the project, the last one containing the conclusions of the thesis.

Chapter 2

Hardware Design

2.1 System Description and Introduction to Altium Designer

The Active Front End project has been organized following a PCB (Printed Circuit Board) oriented structure. This means that the overall project is divided into sections representing the sub-modules, which are the PCBs composing the converter. Each of these sub-modules represents a part with specific role inside the functionality of AFE.

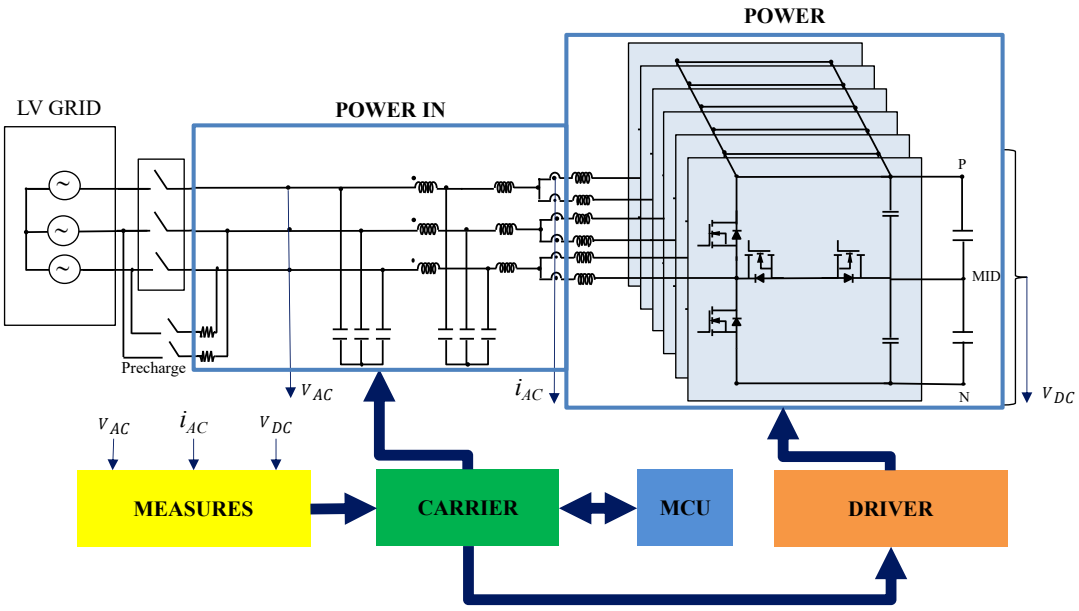

Figure 2.1: Active Front End boards and schematic.

The AFE is composed by the following boards, that can be seen also in the Fig.2.1:

1. Power input board: PCB containing the components of the AC side input filters and the precharge circuit;

2. Power board: PCB containing the power components of the three levels t-type inverter and the DC-link capacitors;

3. Driver board: PCB with the drivers circuitry of two parallel legs of one phase (repeated for the three phases);

4. Measures board: PCB where the main measures necessary for the control are, which are AC phase voltages, AC input currents and DC-link voltage;

5. Carrier board: PCB containing the converter power supply circuits with all the necessary supply voltage levels, the communication part (UART, USB, JTAG, CAN), all the connectors with all incoming or outgoing signals to the other boards, NTC measure, precharge relays and interface with MCU board;

6. MCU board: PBC with the microcontroller and the components that are necessary to its correct functionality and the connector for the coupling with the Carrier board.

It has been used the software Altium Designer, in order to realize the hardware design of the converter. In Altium Designer, a PCB project is the set of documents required to specify and manufacture a printed circuit board. The project file is an ASCII file that lists the documents inside the project, as well as other project-level settings, such as the required electrical rule checks, project preferences, and project outputs. The documents necessary to create a PCB project are the schematics and the PCB. A single PCB project is associated to one board, which is a sub-module of the converter. Moreover, Altium Designer allows to create a general project, called Multi-board project (Fig.2.2). Within that, the logical system design is drawn up by placing the modules on a Multi-board schematic. Hence the Multiboard contains all the PCB projects, generating the 3D structure of the converter, verifying the matings and connections and making available unified project outputs.

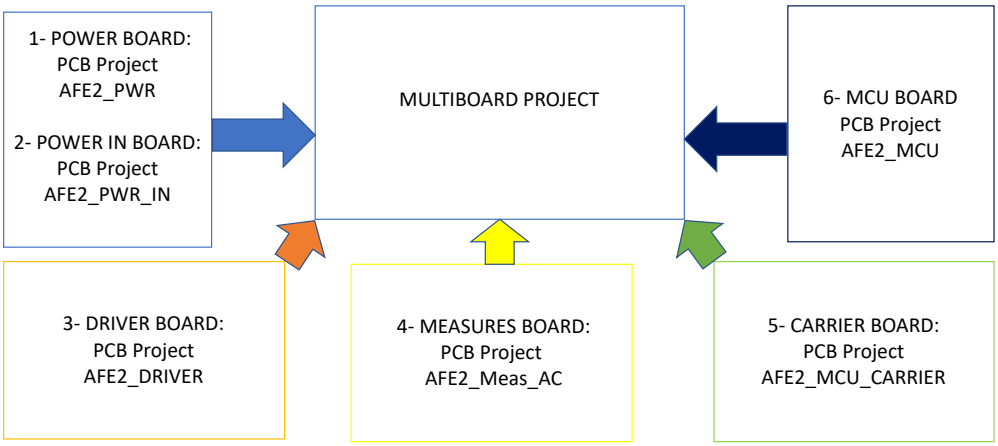

Figure 2.2: AFE PCB Multiproject block scheme.

Each sub-module is linked with the others both with power and signal interconnections that are managed with the logical names, the nets, inside the schematics and physically with the mechanical design of connectors in the PCB documents. It is important to work in an organized and structured way, in order to have the ability to manage multiple schematic of different PCB projects and their links.

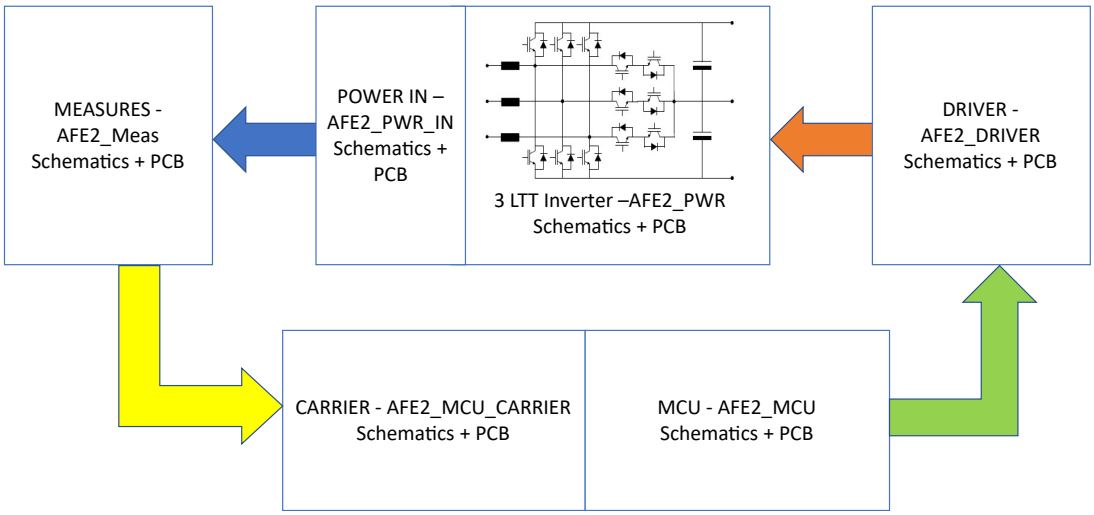

Figure 2.3: AFE PCB projects logic scheme.

In Fig. 2.3 is represented part of signal and logical connections between the parts of AFE, where every board is interconnected with others.

In the following sections of this chapter, the main results of the schematic and PCB design will be reported. However, the work presented in the thesis is about

the results, but the process behind the development of the prototype consisted in a series of iterations that has led to multiple changes in order to obtain the final version. Indeed, it is possible to give a definition of what hardware design is: iterative process with modifications of physical and schematic layout and variations in the choice of components, until a compromise that satisfies all electrical and mechanical constraints for the final PCB to be printed and the BOM (bill of materials, which is the list of components to be bought) is reached.

2.2 Design of the Schematics and Components Choice

In this part of my master thesis the contents and the structures of each PCB project will be presented, with the selection of the main components. In particular, the first step of the hardware design of a converter is the definitions of the electrical schematics, which are the backbone of each PCB project.
In Altium Designer, the production of a schematic is the process of creating a logical representation of an electronic circuit. This means connecting a group of symbols (components) together in a unique way, creating an electronic prototype. When the schematic is completed it is possible to import the design to a PCB layout tool which makes a new PCB file inside the project.

The process seems to be quite simple: place the components and wire them up. Once that a schematic is started, it is possible to understand that the process of creating an electronic circuit is iterative. The reason is that every detail can bring to a complication inside the placing and routing of the components, and on the other hand, having a large number of components connected by hundreds of net, introduces an issue of correct wiring and connections management.

Therefore, the circuit is typically designed with modular approach: the microcontroller, the analog to digital processing, the communication interfaces, the power supply, and all the other parts composing each module. Altium Designer allows to organize the sections on separate schematic sheets and then build the overall design, as for the PCB project and the Multiboard project. It is possible to transfer a section of the design to the PCB editor and then manage additional sections. It is also really important the capability of the program to re-use an existing circuit both schematic and PCB part, only using a copy/paste process.

Schematic organization means that a design can be more easy to be managed and understood if it is presented on multiple schematic sheets. Even if the design is not complicated, there can be advantages in organizing it across multiple sheets, in particular when there are more instances of the same block. Logical modules composing the design of a part of the converter, represented inside the schematic sheets, improve the possibility of easily read the project and the iterative improvement of the PCB structure, by changing, substituting or updating the part under design. Other advantages of organizing each PCB project schematic in multiple sheets are the possibility of edit the components inside the PCB document and placing them inside rooms, that correspond to the sheet themselves, allowing the use of the rooms properties.
If a PCB project is managed in multiple sheets it is necessary to decide the structural relationship of the sheets and the method used for electrical connectivity

between the circuitry inside those sheets (taking also in consideration the outgoing connections and their matings in other PCB projects).
There are two approaches regarding the structuring of a multi-sheet design:

- Flat approach: all the sheets exist on the same level where the connectivity between the sheets is created directly from any sheet to any other sheet. This approach can be used when the sheets of the schematic are few but if the number gets higher, a top sheet can be useful to understand the functionality of the circuit.
- Hierarchical approach: sheet symbols makes the parent-child relationships between the sheets, and the connectivity is managed through the sheet Entries in the sheet Symbols, not directly from the ports on one sheet to the ports on another sheet such is for the flat approach. The child sheet is identified by defining its filename in the sheet symbol and can also include sheet symbols, referencing lower-level sheets, creating another level in the hierarchy, as represented in Fig.2.4, where there are 3 levels.

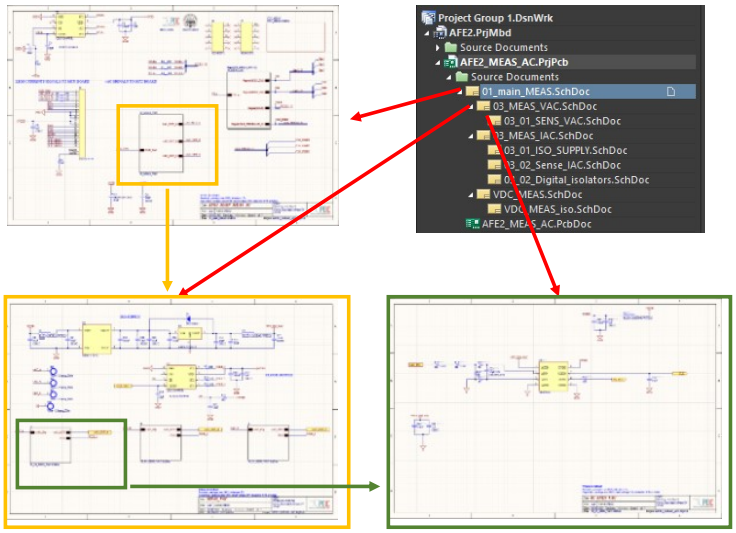

Figure 2.4: Hierarchical Design.

Another crucial aspect related to the design of schematic are the components. Components are represented with two main features, as symbols that can be placed and wired in the sheets of the schematic and also as PCB parts with their specific footprints and step models. They can be manually created as component models and stored inside libraries, downloaded by online sources (provided either by component manufacturers and distributors) or selected from the Altium libraries. Components are connected by wiring the pins together or by placing net identifiers

to connect the pins in that net.

Moreover, if the design includes high pin-count components, it is not practical to create all of the connectivity using individual wires. Hence, multiple nets can be managed into a bus. As an alternative to buses, that can be useful in hierarchical design, is the combination of nets and buses that can be organized into a Signal Harness, which offers a visually and logically way of transferring multiple nets throughout the design and between parent-child sheets, as is presented in Fig.2.5.

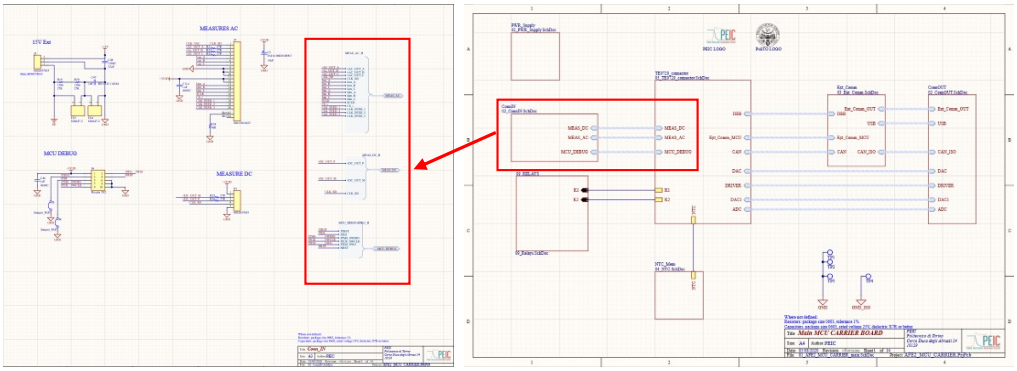

Figure 2.5: Example of harness inside hierarchy.

Besides the management of nets through the sheets, it is important to introduce a fundamental feature available for the design of schematic in Altium Designer, which is the Repeat function. This can be used inside a hierarchical design in order to avoid manual repetition of same child sheets. Indeed, the repetition of same channels and sheets can be made both by adding sheet symbols in the parent sheet, or by including the Repeat keyword in the sheet symbol's Designator field.

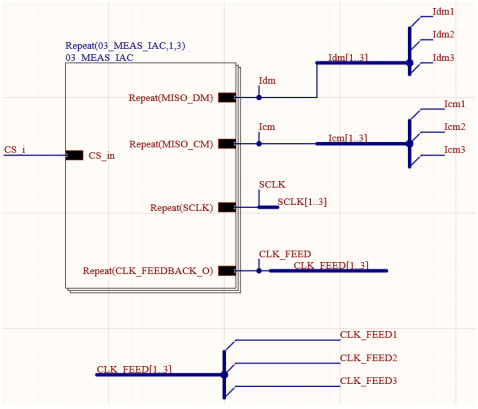

Figure 2.6: Example of buses and Repeat function.

These are the main common features that are represented inside the schematic design which will be presented in the following sections, where the schematics of each board of the AFE will be analyzed.

2.2.1 Power Input Board Schematic

The power input stage of the battery charger AFE is managed in a PCB project called *AFE2_PWR_IN.PrjPcb*, which is organized with the following documents:

- Schematic sheets managed with hyerarchical design, containing the listed parts, schematically described in Fig.2.7:
  - Power connectors;
  - PTCs for the precharge;
  - AC side input filters;
  - Shunt resistors for AC current measure;
  - Output inductors.
- PCB document.

In this case the schematic is composed by two sheets with a two levels hierarchy. The parent sheet is named as MAIN, while the child sheet, on which the Repeat function has been used, is called *01_IAC_MEAS*.

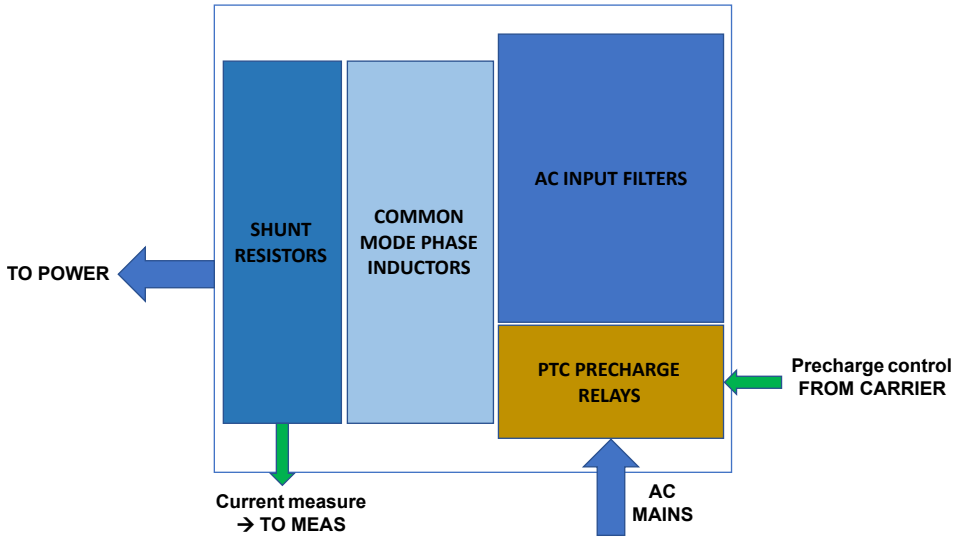

Figure 2.7: Power input board functional scheme.

Starting from the top left of Fig. 2.8, there are three components which are the input connectors coming from the low voltage distribution grid. The connectors chosen are female shank terminals, whose section has to be sized in order to be compatible with the input current. As a consequence, the section of the contacts, the screw and washer related to the connectors are defined.

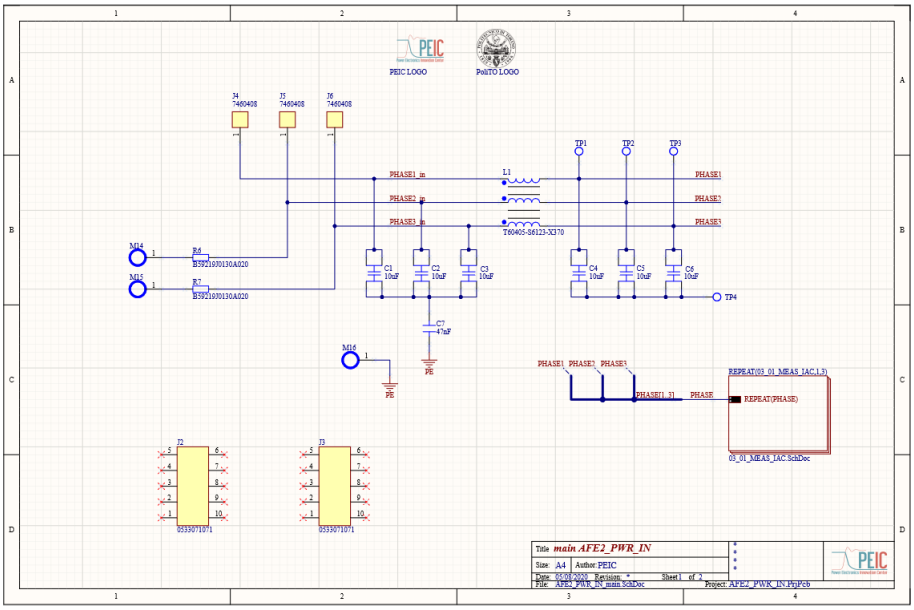

Figure 2.8: Power input parent sheet schematic.

The methodology used for computing the section is based on the thermal considerations for the cables ageing due to overcurrent events, defined by the Italian standard CEI 20-21 [11]. According to this standard, the starting point is the rated power of the converter, which is approximately 50 kVA, considering a unitary power factor. The mains input phase voltage is 230 V. Hence the phase input current can be computed as in (1.1).

The current considered is 72.5 A_{rms}, assumed as the operating current.

Hence, it is possible to choose the parameters k_1 and k_2 in order to provide the sizing current, representing the thermal limit of the cable I_z.

$$I_z = k_1 \cdot k_2 \cdot I_0 \tag{2.1}$$

Where:

- I_0: conductor current rate at ambient temperature of 30° C, without the presence of additional circuits (considering unipolar cables, free air and EPR sheath).

- k_1: incremental or reductive coefficient, function of the ambient temperature.
- k_2: reduction coefficient, function of the number of circuits in the installation.

The section can be obtained from normalized tables considering the rule suggested by the standard:

$$I_b \leq I_z \tag{2.2}$$

Where I_b is the operating current.

It is possible to select the following data from the tables presented in the standard CEI UNEL 35024 [12]:

Table 2.1: Parameters chosen.

Parameter	**Value**	**Parameter**	**Value**
k_1	1	k_2	1
I_0	88 A	S	16 mm^2

It has to be verified the percentage of industrial voltage drop per length unit in order to not exceed 4% (assuming cables of $L = 1$ m).

$$\Delta V_{\%} = \sqrt{3} \cdot \frac{r \cdot L \cdot I_b \cdot cos\phi + x \cdot L \cdot I_b \cdot sin\phi}{V_{ph-ph}} \cdot 100 \tag{2.3}$$

Where:

- r: specific resistance per km;
- x: specific reactance per km;
- V_{ph-ph}: line to line voltage (rms).

It has been assumed a power factor of 1, hence the reactive voltage drop term is neglected. The value of the specific resistance is selected from the table given in the standard CEI UNEL 35023 [13] for unipolar cables. Therefore the $\Delta V_{\%}$ per meter unit is equal to 0.044% which is a reasonable value.

The section chosen of 16 mm^2 has a diameter of 2.26 mm. The compatible contacts, screw and washer of the connector selected must have an external unified diameter of 5 mm, where in ISO metric, the screw thread is M5. Therefore, the M5 screw terminal shank connector can support a maximum current of 175A as stated in the datasheet.

Two of the three phases are linked in series to PTC resettable fuses which are chosen for the precharge of the DC-link capacitors as inrush current limiters, with a resistance of 100 Ω each. The PTC chosen are B59219J0130A020 produced

by TDK. The code after B59, which is 219 is the representative number of the thermistor housing version, with the features obtained from the datasheet (Fig.2.9) [14].

Inrush current limiters

PTC thermistors in housing

Electrical specifications and ordering codes

Type	V_{max} V AC	$V_{link,max}$ V DC	R_R Ω	ΔR_R %	T_{ref} (typ.) °C	C_{th} (typical) J/K	τ_{th} (typical) s	Circuit diagram	Ordering code
PBT plastic case, preferred types for new designs									
J213	280	400	33	25	130	1.1	140	2	B59213J0130A020
J215	280	400	22	25	130	2.3	150	2	B59215J0130A020
J217	440	620	56	25	130	2.3	150	1, 2, 3	B59217J0130A020
J219	560	800	100	25	130	2.3	150	1, 2, 3	B59219J0130A020
Phenolic resin plastic case									
J105	280	400	22	25	130	2.3	150	2	B59105J0130A020
J107	440	620	56	25	130	2.3	150	1, 2, 3	B59107J0130A020
J109	560	800	100	25	130	2.3	150	1, 2, 3	B59109J0130A020

Figure 2.9: PTC electrical characteristics.

In addition the datasheet provides an equation useful for determining the numbers of PTC suggested as a function of the input layout and converter, reported in Fig.2.10.

Hence, in this case K=0.96, while the other parameters can be selected from the table reported in Fig.2.9. The DC-link capacitace is provided by 8 capacitor of 1000 µF, divided in a series of four capacitors in parallel, with a total capacitance of 2 mF. The number of PTC necessary for the precharge is 1 per phase (estimating a maximum ambient temperature of 50° C and DC-link voltage of 800 V).
The precharge is set in order to use two phases to the DC-link instead of three, reducing the number of components.

The inlet filters are located downstream of the pre-charge part, which are made by input capacitive filters (film capacitors), with a capacitance of 10 µF, followed by a conventional second order low pass filter LCL. The cut-off frequency is set around 2 kHz. This is made by a common mode choke of 500 µH (at 500 kHz), followed by star-connected capacitors of 10 µF. All the components are 250 V_{rms} rated. Afterwards, the phase wires nets are linked to the sheet Ports of the child sheet symbol, where it is inserted the connection with the inductances and the shunt resistors (Fig. 2.11).

Calculation of the number of required PTC elements

Number of required PTC elements (connected in parallel) as function of capacitance and charging voltage of smoothing or DC link capacitor:

$$N \geq \frac{K \cdot C \cdot V^2}{2 \cdot C_{th} \cdot (T_{ref} - T_{A,max})}$$

K	K factor K = 1 for DC source K = 0.96 for 3-phase bridge rectifier K = 0.76 for single phase bridge rectifier
N	Number of required PTC thermistors connected in parallel
C	Capacitance of smoothing or DC link capacitor in F
V	Charging voltage of capacitor in V
C_{th}	Heat capacity in J/K
T_{ref}	Reference temperature of PTC in °C
$T_{A,max}$	Expected maximum ambient temperature in °C

Figure 2.10: Number of PTC evaluation.

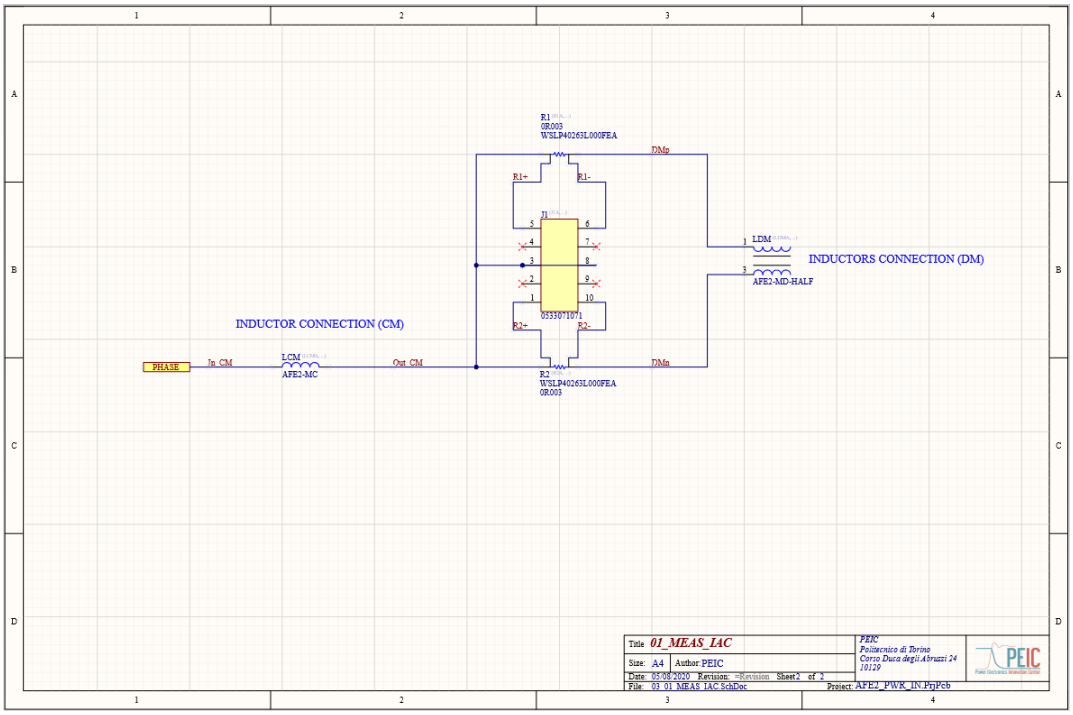

Figure 2.11: Power input child sheet with shunt current measurement.

The schematic can be easily understood with the simplified Fig. 2.12, where the scheme of one phase is shown (repeated for the others).

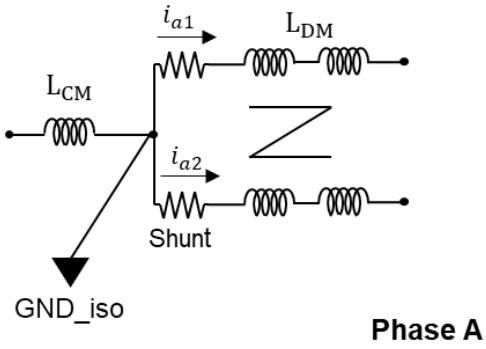

Figure 2.12: Power input schematic simplified (Phase A example).

The input connection comes from the parent sheet and it is the filters' output. The phase current flows trough a first inductor, which is sized in order to sustain the entire current of one phase and it is called common mode inductor L_{CM}.
Then, the wiring is splitted up into two parallel legs, where the shunt resistors are placed. Downstream of this link it is possible to notice the presence of one series inductance, called differential mode inductance L_{DM}, which is the one that makes possible the interleaving of the legs. In particular, this inductance has the pins soldered both in this board and on the power boards, creating also a mechanical coupling.
The current measures of each phase are isolated, with imposed reference for the analog conditioning stage and the ADC, corresponding to the bifurcation of the connection between the two legs of the same phase.

In this part of the schematic the shunt resistor needed for the current measures has been sized.
The reason of using a shunt measure is due to the fact that the shunt allows to obtain high bandwidth, avoiding delays in the measure.
On the other hand, other measurement modes, such as current sensors, which have been evaluated, do not have a sufficient bandwidth, considering the control frequency. This causes a loss of controllability, preventing the average zero differential current value from being obtained.
The currents that have to be measured are the phase currents of the parallel legs. It is always possible to measure them during the switching period and it can be computed in an analog way the common mode current and differential mode current, in order to feedback directly those values to the control.

- Common mode current

$$i_{CM} = \frac{i_{a1} + i_{a2}}{2} \tag{2.4}$$

- Differential mode current

$$i_{DM} = \frac{i_{a1} - i_{a2}}{2} \tag{2.5}$$

To summarize, the main features of the shunt based measurement of an electric quantity are:

- Low inductance (high bandwidth for the current measure).
- Low power losses (due to the choice of the resistance value).
- Robust measure with high bandwidth.

The sizing of the shunt is based on the following issues:

- The peak current value to be conduced, that represent the full scale of the measure.
- The power losses of the shunt during the current conduction.
- The scale factor that it is accepted, considering the subsequent analog conditioning.

The sizing of the shunt has been based on the four-wire voltamperometric measurement, knowing the peak values of the currents to be measured and computing the maximum Joule losses over the component.

$$\hat{i}_{leg,max} = \frac{\hat{i}_{ph,max}}{2} = \frac{\sqrt{2} \cdot 72.5}{2} = 51.3 \text{ A}_{\text{pk}} \tag{2.6}$$

The value chosen is R_{shunt} =3 mΩ, therefore the following voltages and the power losses can be evaluated in the worst case scenario of maximum phase current:

$$V_{shunt} = R_{shunt} \cdot I_{leg,max} = 3 \cdot 10^{-3} \cdot \frac{51.3}{\sqrt{2}} = 109 \text{ mV}_{\text{rms}} \tag{2.7}$$

$$\hat{V}_{shunt} = R_{shunt} \cdot \hat{i}_{leg,max} = 3 \cdot 10^{-3} \cdot 51.3 = 109 \text{ mV}_{\text{pk}} \tag{2.8}$$

$$P_{Joule} = R_{shunt} \cdot I^2_{leg,max} = 3 \cdot 10^{-3} \cdot \left(\frac{51.3}{\sqrt{2}}\right)^2 = 3.95 \text{ W} \tag{2.9}$$

Hence, the value is reasonable and the component selected is WSLP40263L000FEA, manufactured by Vishay Dale. The component has the following main features [15]:

- Very low inductance, 0.5 nH to 5 nH;

- Low thermal EMF (< 3 µV/°C);
- Tolerance ±1%.

The voltage signal is conducted through a connector chosen to reduce the overall dimensions, to the Measures board where the conditioning and digital conversion circuits have been designed.

2.2.2 Power Board Schematic

The PCB project of the power board, which is the Active Front End power stage, it is organized as follows:

- Schematic sheets, containing the following parts (Fig. 2.13):
  - DC-link;
  - DC output power connectors;
  - AFE Three Levels T-Type;
  - Desaturation circuit (power side).
- PCB document.

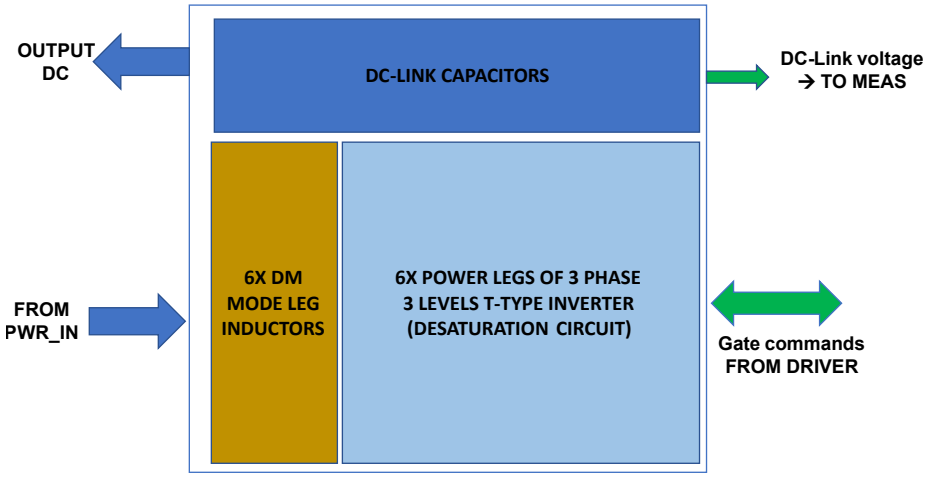

Figure 2.13: Power board functional scheme.

Also in this case the schematic shows a hyerarchical structure. In fact, inside the PCB project folder, two sheets can be found.
In the parent sheet (Fig.2.14), the AC three phase inputs coming from the Power input board and passing through the second part of the differential mode inductances, are placed and wired. The nets outgoing from the inductances are brought

into the child sheet Ports of the central sheet symbol. This sheet symbol is repeated with the function Repeat (also used in net Ports) three times, in order to represent the three phase inputs of AFE in a more compact way.

In the parent sheet it is inserted the entire DC-link, composed by 8 electrolytic capacitors. As said in the previous paragraph, the DC-link is designed with a total capacitance of 2 mF, divided into a series of two blocks of four parallel capacitors of 1000 µF each. The mid-point is connected, as made with the positive and negative pins of the DC-link, to the ports of the child sheet symbol.
There are discharging resistors connected in parallel to the DC-link, whose footprint for the PCB is created but are not then mounted (N.M.). Moreover, there are both the heatsink symbols for dissipating the thermal losses (whose model has been created and inserted in the library) and the DC-link output power connectors.

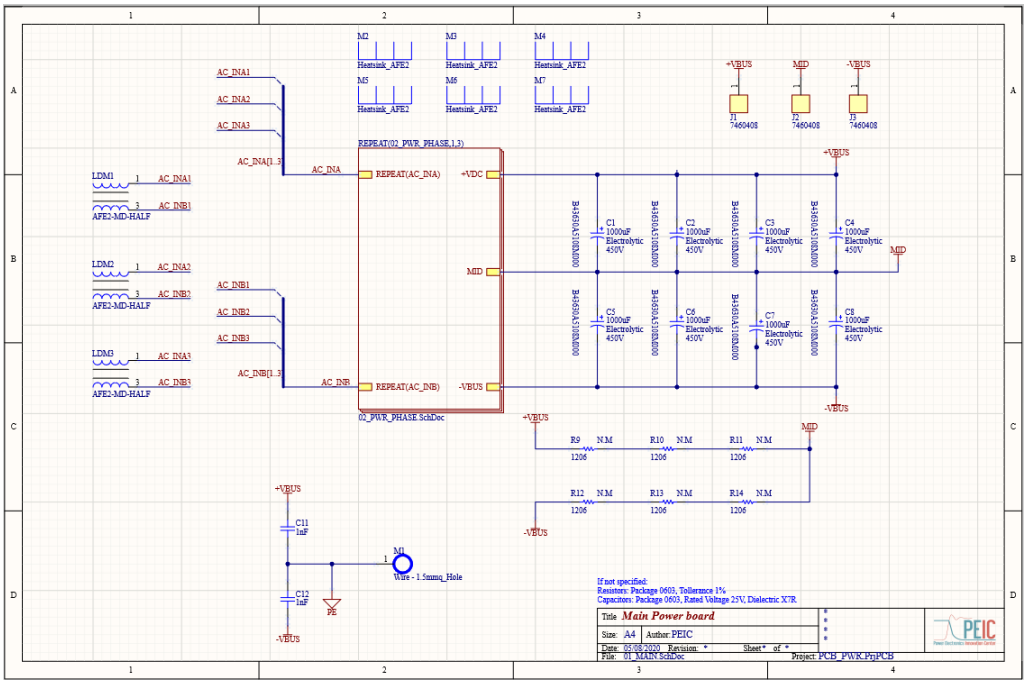

Figure 2.14: Power board main (parent sheet).

Those connectors are chosen to be equal to the ones designed for connection with the mains. The reason of this choice are two. The first is related to the maximum current flowing out from the DC-link, the second one is due to the standardization of the choice of components.
In order to verify that the outgoing DC current is lower than the AC input side, it

is possible to make the following computation:

$$I_{DC} = \frac{P_{max}}{V_{DC}} = \frac{50 \cdot 10^3}{800} = 62.5 \text{ A} \tag{2.10}$$

Therefore the DC side current is lower than AC side.

Inside the child sheet (Fig.2.15), the heart of the power converter has been designed. It represents one phase and it has been repeated.
The structure is divided in two identical parts. The AC inputs, coming from the upper and lower L_{DM}, are both connected to the inverter legs in parallel. The leg is the one described for the Three Level T-Type, with the upper and lower side MOSFETs and the mid-point of the leg, connected to a series of two MOSFETs, which regulate the mid-point current in order to balance the DC-link voltages.

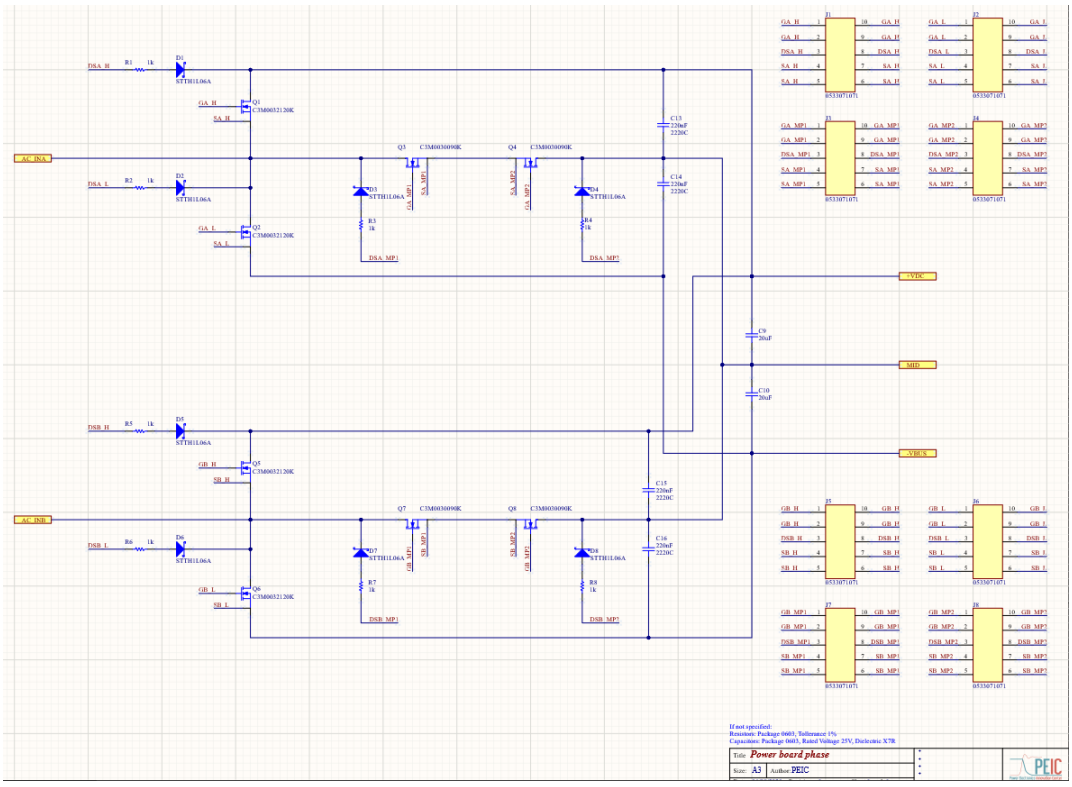

Figure 2.15: Power board phase (child sheet).

Going more in detail with the inverter leg description, referring to Fig. 2.16, other components are part of the layout. Indeed, for each drain side of the MOSFETs is connected a series of one Shottky diode and a resistor. These components are

the power side part of the desaturation detection of the transistor, which prevents from destructive short circuit events.
The other relevant components are the ceramic capacitors connected as output of each leg and then cascaded into two film capacitors that make the output partition of the DC-link outside the sheet. This is a fixed design in the hard switching power. The reason is to replicate the DC-link function of sustain in a voltage and forming a capacitive output. The film capacitors are sized in order to absorb the switching ripple of the current, while the electrolytic capacitors of the DC-link are needed to filter the low frequency current noise. Therefore, this solution can prevent dangerous overvoltages generated by the derivative response of parasitic inductances in the conduction path, containing the multi-resonant response of the system to the switching for a large range of frequencies.

The power switches used are N-channel Silicon Carbide (SiC) MOSFETs manufactured by CREE. The inverter leg high and low side transistors are 1200 V C3M0032120K (it has to be considered at least a 400 V margin for overvoltage respect the maximum DC-link voltage). Instead, the other two switches composing the mid-point connection are in series, hence the voltage sizing is halved. The chosen components are 900 V rated due to the available devices, C3M0030090K.

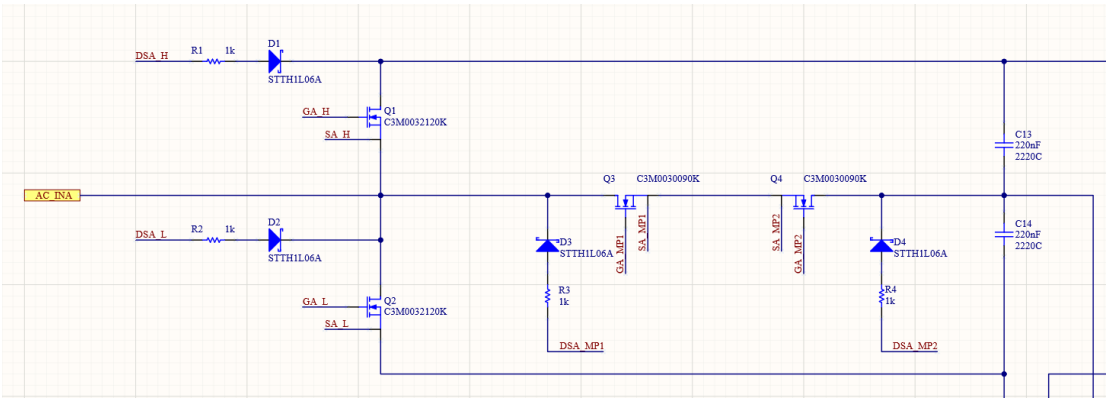

Figure 2.16: Inverter leg.

The choice to use SiC MOSFETs is due to the 72 kHz switching frequency set by the control. The device chosen has a current rating of 63 A (at 25 °C), which is suitable for the application. Moreover, the package TO 247-4 has Kelvin source contacts available, as shown in Fig.2.17.

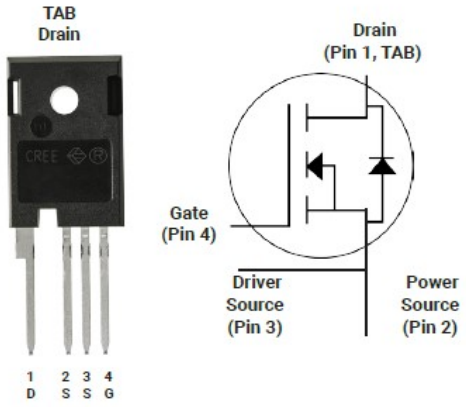

Figure 2.17: CREE SiC MOSFET - TO 247-4.

The Kelvin source is very important in fast switching applications, because in the 3-pin devices, during every switching cycle, the parasitic inductance of the source wire bonding coupled with the current derivative slope generates a voltage opposite to the driving signal of the MOSFET. The effect of this signal is to slow down the switching cycle, increasing the switching losses and it also could make a critical disturb voltage that can lead to the rise of the gate voltage. Then it is possible a re-switch of the transistor, due to the abrupt change in current in the source.
The Kelvin source pin allows to divide the path of the power from that of the driving signal and referring the driver potential to the Kelvin source, where the current is supposed to not pass. Hence, the main advantage is that the driving signal is immune to the disturbance due to the switching current flowing through the power circuit. As a consequence, the power loss in the transistor is reduced, lowering the junction temperature, while the signal path is immune to disturbances. Moreover, in the board, each transistor is driven with signals wired to the related female connector, which is interfaced with its male mate placed on the Driver board.

2.2.3 Driver Board Schematic

The Driver board is a PCB project containing the gate drivers and the related circuitry for each transistor of one phase. The choice of designing one phase drivers is related to the possibility of easy repetition of the PCB.
The PCB project contains the following parts referred to the drivers of one phase (as can be seen in Fig. 2.18):

- Schematic sheets organized with a hyerarchical approach:

  - Parent sheet, with connector interfacing with Carrier board and child sheets;
  - Child sheets in which are inserted the connectors for the outgoing signals to Power board;
  - Power supply;
  - Leg drivers and mid-point drivers and related circuitry.

- PCB document.

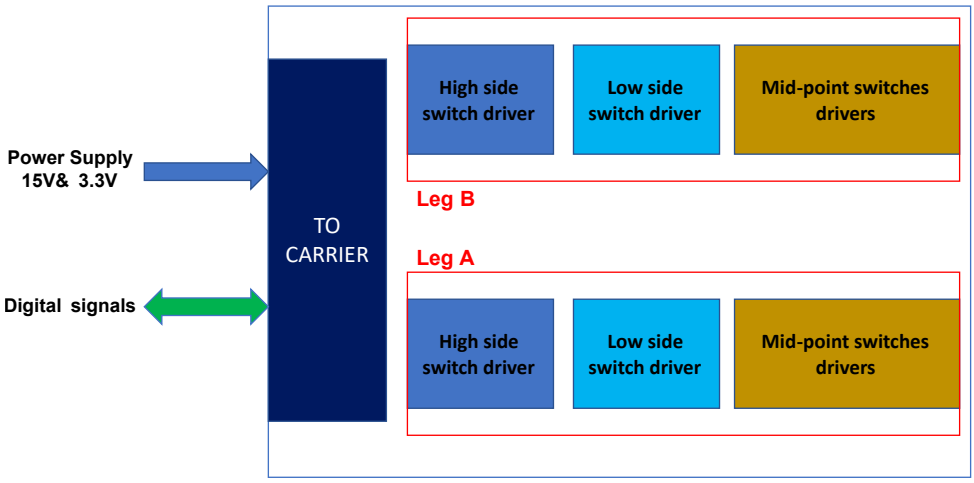

Figure 2.18: Driver board functional scheme.

According to the schematic realization it has been decided the typology of the driver, the supply system, the connections to the other boards and it has been sized both the gate resistors and the desaturation circuit.

The following figures represent in order: the parent sheet of the schematic, the second level sheet, the high side or low side switch driver indifferently and the last figure are the drivers of the mid-point switches.

Inside the *main* sheet, it is possible to underline the following elements:

- Two child sheets, containing the driver circuits for the parallel legs of one phase;
- The connector with the signals and supply voltages brought from the Carrier board;

- Two capacitors for each supply voltage (+15 V, +3.3 V) necessary to sustain the potential. The connector chosen for the interface with the Carrier board, is a 20 positions female FPC connector, whose main features are the horizontal assembly, which reduces the overall thickness of the boards and the type of cable FFC (flexible flat cable), that is both flat and flexible, with thin conductors.
  Each supply voltage given by an external connection is empowered and stabilized by a parallel of two capacitors, whose one is ceramic (X7R) and SMD (surface mounted) with a capacity of 100 nF, while the other is electrolytic (more energy density) of 22 µF.

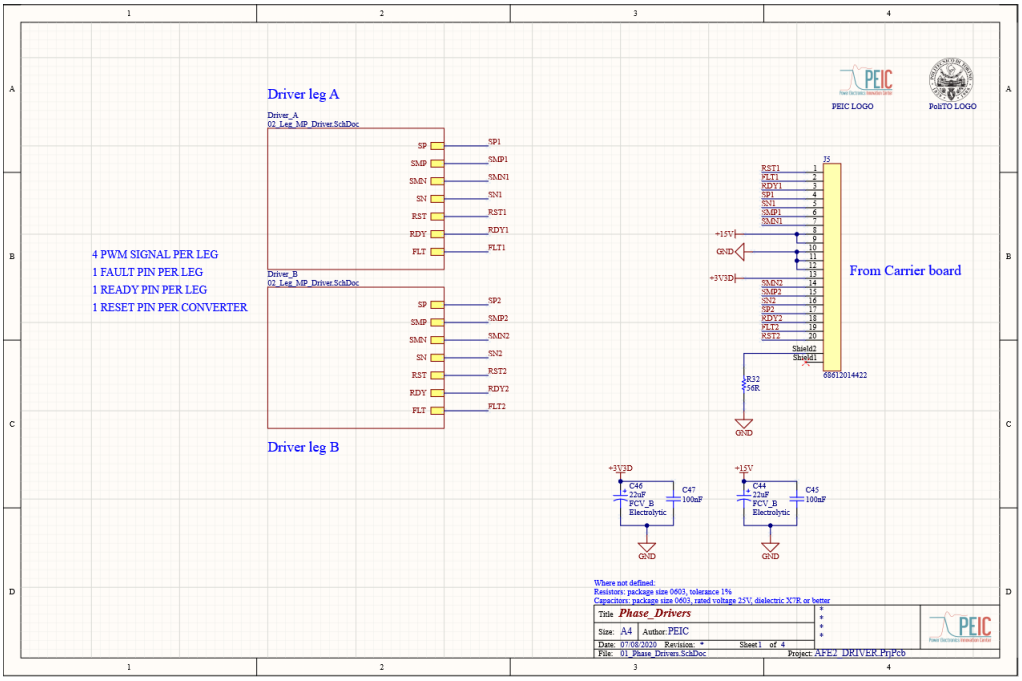

Figure 2.19: Driver board schematic main.

The digital signals exchanged with the Carrier board for each leg drivers are:

- 4 PWM signals per leg (high side and low side switches and mid-point (MP) switches);
- One fault signal;
- One ready signal;
- One reset signal (in common for the entire equivalent converter composed by the three half splitted phases).

The child sheet has been designed in order to represent the parallel leg phase drivers and place the mate 10 positions male connectors, which carry the pilot signals of the power board MOSFETs.

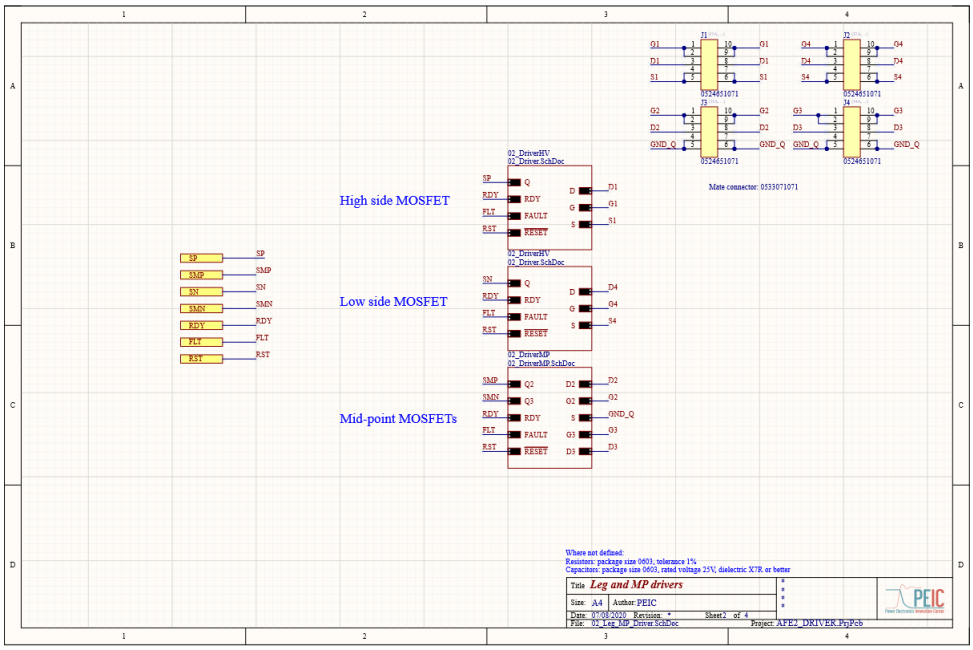

Figure 2.20: Driver board child sheet.

Moving towards the description of the sheet with the driver circuitry, it can be seen that the layout is the same for each driver:

- Insulated power supply;
- Driver insulated interface;
- Filters and gate resistors;
- Desaturation circuit;
- Fault and ready pull-up resistors (for the MP drivers is used an OR structure).

The layout presented in Fig.2.21 refers to the leg switches' driver, which is the same for both transistors. Instead, Fig.2.22 shows the schematic of the mid-point switches' drivers. Each driver and power supply component is equal, while the main difference is linked to the layout. In fact the leg drivers need a separated and insulated power supply, while the MP drivers can share the same power supply potential, but they have independent gate command allowing multiple modulation techniques.

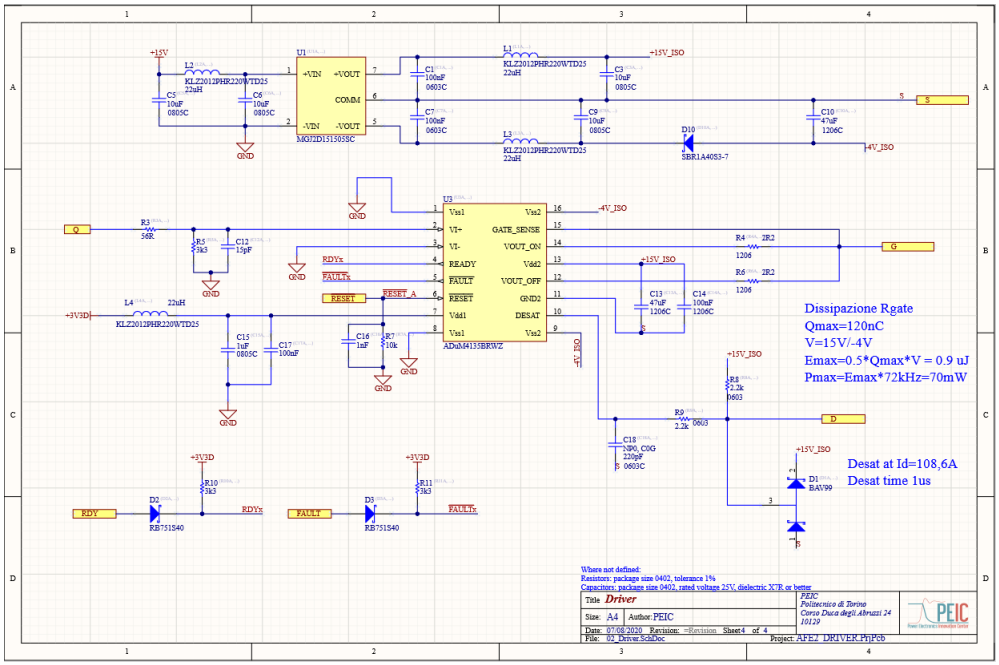

Figure 2.21: Leg switch driver.

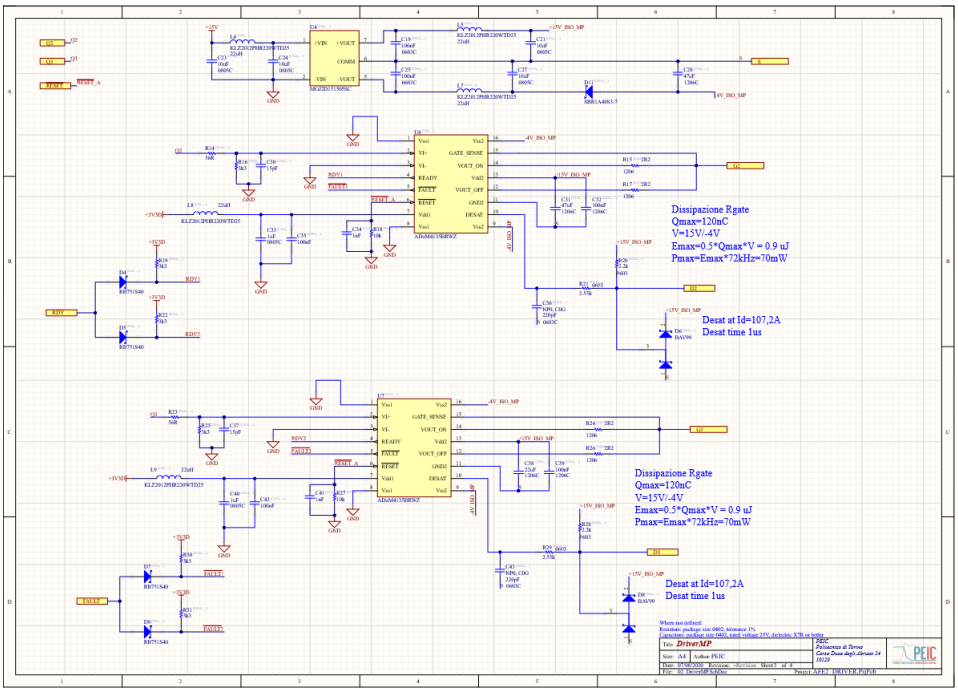

Figure 2.22: Mid-point switches' drivers.

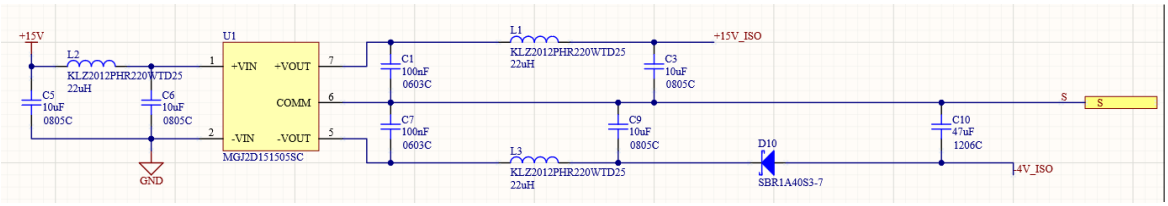

Figure 2.23: Power supply detail.

Fig.2.23 shows the power supply circuit in detail, where LC filters are applied in order to stabilize the potential. The input voltage is +15 V, while the 2 W DC/DC converter (MGJ2D151505SC manufactured by Murata) creates insulated voltages with +15 V_{ISO} to -4 V_{ISO}.
The components chosen for the filters are SMD, with an inductance of 22 µH and a capacitance of 10 µF. The cut-off frequency is around 10.7 kHz. The capacitors and inductors packages are standardized with imperial size 0805 with a rated power of 1/8 W. In addition the 1 A diode is chosen to protect the negative side of the supply.

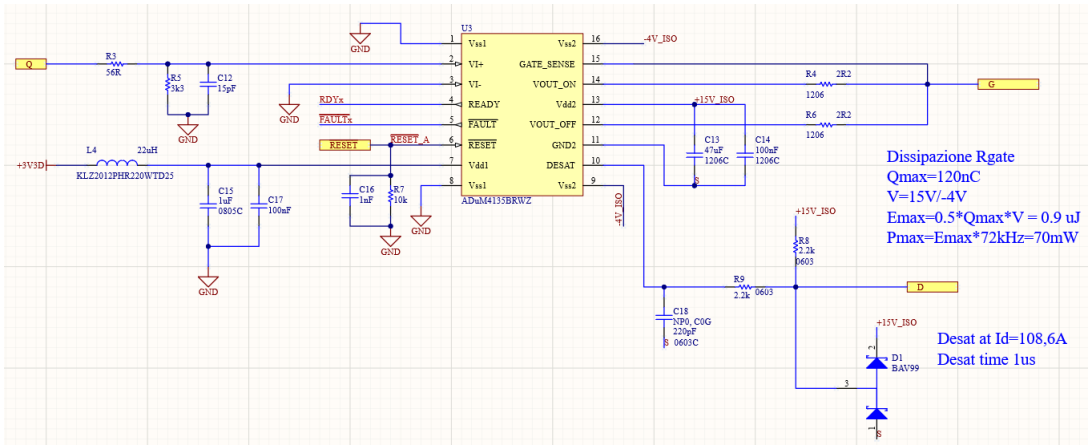

Figure 2.24: Driver layout detail.

The driver chosen is ADuM4135BRWZ manufactured by Analog Devices.
It is a single-channel gate, with included Miller clamp which provides robust turn-off with a single-rail supply when the gate voltage drops below 2 V.
The Analog Devices chip provides isolated communication of control information between the high voltage and low voltage domains of the chip. The reset of the device after a fault on the secondary is performed on the primary side of the device with the fault signal.
Moreover, integrated onto the ADuM4135 is a desaturation detection circuit that provides protection against high voltage short-circuit [16]. As can be seen in the

schematic, in the not isolated part of the driver, which is supplied with 3.3 V, an additional power supply LC filter has been applied. The designed main parameters are an inductance of 22 µH and a shunt equivalent capacitance of 1.1 µF (composed by a parallel of 1 µF with package 0805 and 100 nF with package 0603, whose rated power is 1/10 W). The cut-off frequency of this filter of 10.2 kHz can be evaluated. This supply filter layout has been applied in other boards, where integrated circuits are used.
In addition, in the not isolated part, the resistors and capacitors filters used for the signal wires, have the imperial package 0402, which is rated with 1/16 W, in order to reduce the space occupied.

Furthermore, when integrated circuits with digital signals are implemented, it is necessary to take care of the signal quality. In fact, as a general hardware design rule, it can be used the following guideline:

- Incoming signals: a capacitive low pass filter, considering the resistance of the transmission line, can be applied, in order to clean the high frequency disturbances and stabilize the signal voltage, making a RC filter (the parasitic inductance is tough to estimate). Suitable values applied into the projects are 12-15-22 pF. The cut-off frequency can be evaluated with the equation:

$$f_{cut-off,RC} = \frac{1}{2\pi R_{filt} \cdot C_{filt}} \tag{2.11}$$

- Outgoing signals: a resistive low pass filter can be added in order to clean the output of the IC (integrated circuit), making with the capacitive transmission line another RC filter. Suitable values of the resistance can be 10-27-56-100 Ω. The filter cut-off frequency can be evaluated with the previous equation.

In both the filters, the cut-off frequency can be estimated. The filters reduce digital noise with magnitude of hundreds of MHz.

The design of the gate driver circuit and the desaturation detection circuit has been made for each transistor, using Excel sheets in order to create a general file where input data can be inserted and the main parameters can be verified.

- **Gate driver check**
  ADuM4135 has two inputs, V_{I+} and V_{I-}, while to control the gate driver signals it uses V_{OUT_ON} and V_{OUT_OFF}. Both the V_{I+} and V_{I-} inputs use CMOS logic. The input logic can be controlled by imposing the V_{I+} pin high or the V_{I-} pin low. If a fault is asserted, transmission is blocked until the fault is cleared by the $RESET$ pin. The ADuM4135 provides two output nodes for driving the switches. The benefit of this approach is that two different

resistances for the turn-on and turn-off can be selected. It is desired to have the turn-off faster than the turn-on. Moreover, knowing the voltage swing on the gate, as well as the internal resistance of the gate driver, an external resistor can be chosen [16]. The resistance chosen to drive the MOSFET is equal both for $R_{g,ON}$ and $R_{g,OFF}$ to 2.2 Ω.

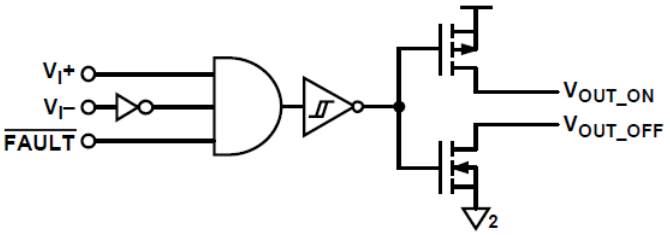

Figure 2.25: Gate driver output block diagram with NMOS and PMOS.

In order to verify the suitability of the driver and the values chosen for the external gate resistance, the following procedure can be considered [9].

First of all, checks must be made regarding the power absorbed by the driver for operation and losses inside the driver itself:

$$P_{tot} = N_{MOS} \cdot Q_g \cdot (V_+ - V_-) \cdot f_{sw} \tag{2.12}$$

$$P_{drv,loss} = P_{tot} \cdot \frac{1}{2} \cdot \left(\frac{R_{MOS,ON}}{R_{g,ON} + R_{MOS,ON}} + \frac{R_{MOS,OFF}}{R_{g,OFF} + R_{MOS,OFF}} \right) \tag{2.13}$$

The thermal limit of the driver has to be considered:

$$P_{drv,loss,max} = \frac{T_{j,max} - T_{a,max}}{R_{th,j-a}} \tag{2.14}$$

In addition, the current capability has to be controlled. Indeed, the driver has to sustain sufficient current during the Miller plateau (i.e. the voltage rise and fall phase).

$$I_{g,ON} = N_{MOS} \frac{V_+ - V_{Miller}}{R_{MOS,ON} + R_{g,ON} + R_{g,int}} \tag{2.15}$$

$$max(I_{g,ON}) = N_{MOS} \frac{V_+ - V_{th}}{R_{MOS,ON} + R_{g,ON} + R_{g,int}} \tag{2.16}$$

$$I_{g,OFF} = N_{MOS} \frac{V_{Miller} - V_-}{R_{MOS,OFF} + R_{g,OFF} + R_{g,int}} \tag{2.17}$$

$$max(I_{g,OFF}) = N_{MOS}\frac{V_{th} + \frac{I_{max}}{g} - V_{-}}{R_{MOS,OFF} + R_{g,OFF} + R_{g,int}} \tag{2.18}$$

Where:

- P_{tot}: power necessary for the driver's operations (W);
- N_{MOS}: number of MOSFETs driven by the driver;
- Q_g: MOSFET gate charge (nC);
- V_+ and V_-: driver +/- supply voltages (V);
- f_{sw}: switching frequency (kHz);
- $P_{drv,loss}$: power lost inside the gate driver itself (W);
- $R_{MOS,ON}$: P-channel MOSFET internal resistance (Ω);
- $R_{MOS,OFF}$: N-channel MOSFET internal resistance (Ω);
- $R_{g,ON}$:external gate ON resistance (Ω);
- $R_{g,OFF}$: external gate OFF resistance (Ω);
- $T_{j,max}$: maximum absolute junction temperature ($^{\circ}C$);
- $T_{a,max}$: maximum absolute ambient temperature (°C);
- $R_{th,j-a}$: junction to ambient thermal resistance (K/W);
- $I_{g,ON}$: ON status gate current (A);
- V_{Miller}: Miller-plateau voltage (load dependent) (V);
- $R_{g,int}$: internal gate resistance (Ω);
- I_{max}: maximum load current (A);
- g: MOSFET transconductance (S).

The input parameters evaluated to verify the power and the current capabilities related to the gate resistance chosen are:

Table 2.2: Driver check input data.

MOSFET	**C3M0032120K**	**C3M0030090K**
N_{MOS}	1	2
Q_g (nC) (@ 15 V)	118	90
V_+ (V)	15	15
V_- (V)	-4	-4
V_{th} (V)	2	2
f_{sw} (kHz)	72	72
$R_{MOS,ON}$ (Ω)	0.975	0.975
$R_{MOS,OFF}$ (Ω)	0.625	0.625
$R_{g,ON}$ (Ω)	2.2	2.2
$R_{g,OFF}$ (Ω)	2.2	2.2
$R_{g,in}$ (Ω)	1.7	3
g (Ω)	27	22
I_{max} (A)	51.24	51.24
$R_{th,j-a}$ (K/W) (4 layer PCB)	75.4	75.4
$T_{a,max}$ (°C)	40	40

The main outputs are:

Table 2.3: Driver check output data.

MOSFET	**C3M0032120K**	**C3M0030090K**
P_{tot} (W)	0.161	0.246
$P_{drv,loss}$ (mW)	42.64	65.05
$T_{j,max}$ (°C)	43.2	44.9
$max(I_{g,ON})$ (A)	2.67	4.31
$max(I_{g,OFF})$ (A)	1.75	2.76

The maximum driver current, which is equal to 4.61 A is upper than the current needed in the application. Therefore, the driver chosen is suitable and the external ON and OFF gate resistors are correctly sized (the package in imperial measure is 1206 with power rating of 1/4 W, because of the power losses that the resistors have to sustain).

- **Desaturation detection**
  The desaturation detection is the active protection against short circuit and closure of the MOSFET on the short circuit itself. This measurement should

be carried out only when the transistor is conducting and the diode is on. If the measured signal has a voltage higher than the threshold, the protection is activated. The threshold is calculated as the voltage drop due to the equivalent conduction resistance R_{ON} and the minimum short-circuit current. The hardware solution for the desaturation is the open-drain FAULT pin of the driver, which is an output communicating that a desaturation fault has occurred. When the FAULT pin is low, the gate is driven low. If a desaturation event occurs, the RESET pin must be driven low.
The desaturation detection circuit is shown in the following Fig.2.26.

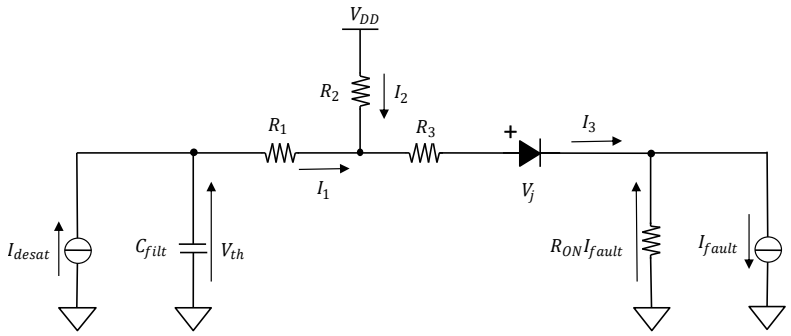

Figure 2.26: Desaturation detection schematic.

It has been produced an Excel file in which it is possible to select and iteratively optimizes the resistance values needed in the desaturation circuitry.

Considering Fig.2.26, it is possible to introduce the main variables. Moreover, resolving the circuit a general sizing equation can be found.

- V_{th}: threshold voltage, it is fixed to 9 V by the driver;
- I_{desat}: internal current source of 500 µA;
- C_{filt}: filter capacitor needed to stabilize the signal, in steady state its voltage is the threshold one;
- R_1, R_2, R_3: desaturation detection series resistors and pull-up resistor to be determined;
- V_j: diode voltage drop, assumed 0.7 V;
- $R_{ON}I_{fault}$: voltage signal (V_{DS}) which carries the possible short-circuit event information. R_{ON} is the internal equivalent resistance of the transistor, while I_{fault} is the drain-source current conduced by the switch that is fixed to a maximum value in order to control and protect the leg from failures;

– V_{DD}: supply voltage of the isolated part of the driver, it is chosen equal to 15 V.

By imposing the voltage loop balances and the nodal equation, the following system can be written in the following way:

$$\begin{cases} V_{DD} = V_{th} - R_1 I_1 + R_2 I_2 \\ V_{DD} = V_{DS} + V_j + R_3 I_3 + R_2 I_2 \\ I_1 + I_2 = I_3 \end{cases} \tag{2.19}$$

By imposing the values of R_2 and R_3, it can be obtained R_1, assuming at steady state $I_1 = I_{desat}$. If the resistances are changed, the more suitable choice can be done, taking in consideration the current I_{fault} that cannot overcome a certain level.

$$R_1 = \frac{(R_2 + R_3)V_{th} - (R_2 R_{ON} I_{fault} + R_2 V_j + R_2 R_3 I_1 + R_3 V_{DD})}{(R_2 + R_3) I_1} \tag{2.20}$$

The design of the resistors has been made with the following input data and choices. It has to be underlined the fact that from the MOSFETs datasheet the maximum current value allowed by the SOA (safe operating area) is 110 A, while the desaturation protection is triggered with current values lower than the maximum one.

Table 2.4: Desaturation circuit design.

MOSFET	**C3M0032120K**	**C3M0030090K**
R_{ds}^{on} (mΩ)	0.032	0.03
I_{fault} (A)	108.6	107.2
R_1 $(k\Omega)$	2.2	2.55
R_2 $(k\Omega)$	2.2	2.2
R_3 $(k\Omega)$	1	1

The resistor values chosen are EIA E96 standard values with 1% tolerance and the imperial package is 0603, with power rating of 1/10 W.

2.2.4 Measures Board Schematic

The Measures board is a PCB project containing the following parts (as can be seen in Fig. 2.27):

- Schematic sheets managed with hyerarchical design:

  - Power supply stage;
  - AC voltage measures, which are brought to the Carrier board through a FFC cable;
  - DC-link voltage measures, that are carried out with a small horizontal connector.

- PCB document.

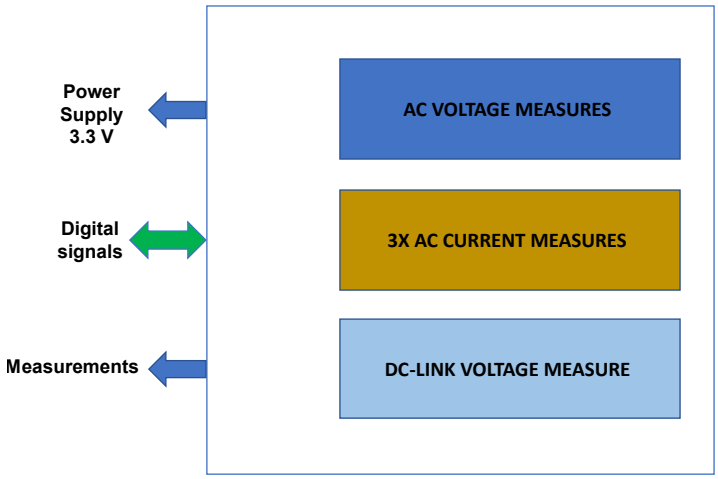

Figure 2.27: Measures board functional scheme.

The choice of inserting all the electrical measures inside a single board is due to compactness.
The main advantages are the identical layout of the phase current measures, the technology chosen for the voltage measures that allow a simpler and more compact solution. The analysis of each measure can be based on the technology adopted, which is different for the currents and the voltages:

- **Current measure**
  The signals for the current measure of one phase, coming from the Power board, through the mate 10 positions SMD connector, are divided into three potentials. The positive ones from the conventional positive side of voltage drop, $V_{sh1}+$ and $V_{sh2}+$ (called in the schematic sheets R_1+ and R_2+), the negative $V_{sh1}-$ and $V_{sh2}-$ (also called R_1- and R_2-) and the voltage reference for the measure, which is the GND_{iso} shown in Fig.2.12. The approach used is a differential measure, where the sensed signals are properly combined, with reference to (2.4) and (2.5), obtaining the common mode current analog signal and the differential mode one. This stage is followed by the analog conditioning circuit, which has been sized and the resulting signal is driven

to the ADC converter. Therefore, the digital signals of the two currents are managed by a digital isolator.
The main feature of using this design is the fact that the analog propagation delay is avoided with respect to a general isolated operational amplifier, while the sampling delay is known *a priori* and it can be compensated. In addition, the isolation stage is not made with the analog circuit, but through the digital isolator.
The digital signals outgoing from the isolator are managed as SPI (signal peripherals interface which is a serial communication protocol between MCU and the integrated circuits).

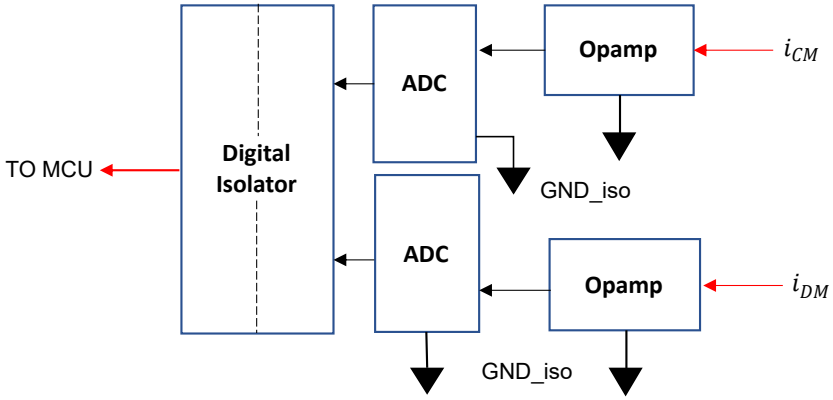

Figure 2.28: Current measure block scheme for one phase.

The digital signals needed for the functionality of this system are the following:

- Chip Select (CS): this is the synchronization signal of the ADC sampling sequence, which samples on the CS falling edges. The frequency of this signal is $2f_{sw} = 144$ kHz, being the current sampled once per switching period.
- Signal Clock (SCLK): these are the signals that manage data synchronization from the MCU. The maximum frequency of the signals is 47 MHz.
- Serial data (SDATA): these are the signals with the digital information of the CM and DM currents.

Moreover, the energy consumption of the digital isolator introduces a problem. It cannot drive the high frequency signal of the SCLK without the deterioration of the measure.
The solution is the adoption of clock buffers that are integrated circuits, who replicate the clock signal and propagate it in the same way, introducing a

negligible delay.

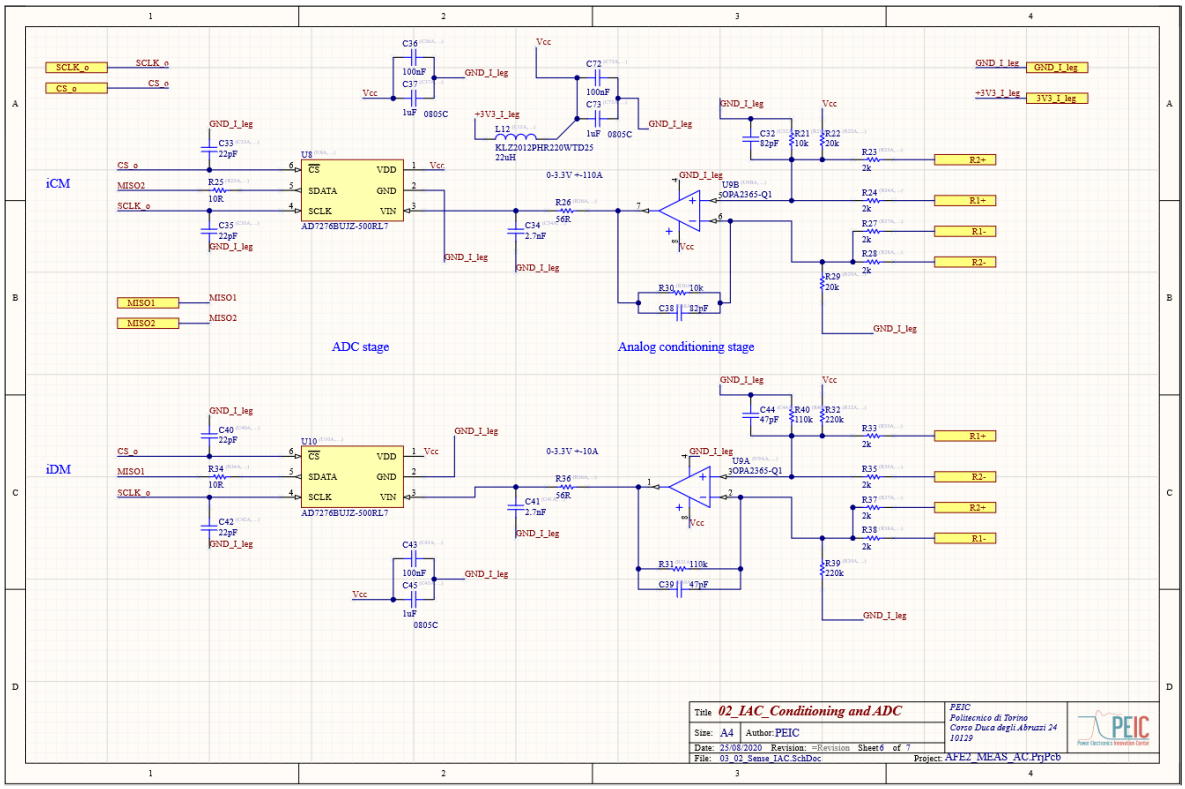

Figure 2.29: Conditioning and ADC for CM and DM of one phase.

Analog conditioning design

Signal conditioning is the manipulation of an analog signal in order to adapt the signal voltage scale to the one requested by the next stage.
In the application, the scale of the ADC stage, which is related to the one allowed by the MCU, is $0 - 3.3$ V, while the incoming signals from the Power board have different scaling.

- CM current full-scale: sum of the leg currents with $\hat{i}_{CM} = \pm$ 110 A_{pk}.
- DM current full-scale: difference of the leg currents with $\hat{i}_{DM} = \pm$ 10 A_{pk}.

Remembering the shunt resistance chosen of 3 mΩ, the voltage full-scale of the analog measured signal can be easily obtained:

- CM signal full-scale: $\hat{V}_{sh,CM} = \pm$ 330 mV_{pk}.

– DM signal full-scale: $\hat{V}_{sh,DM} = \pm$ 30 mV_{pk}.

Therefore, two different gains have to be evaluated, while the offset is the same, 1.65 V.

In Fig.2.29 it is drawn the conditioning circuit for both the signals. With that layout and referring to the following simplified schematic, the output voltage can be obtained from the voltage divider and Opamp theory.

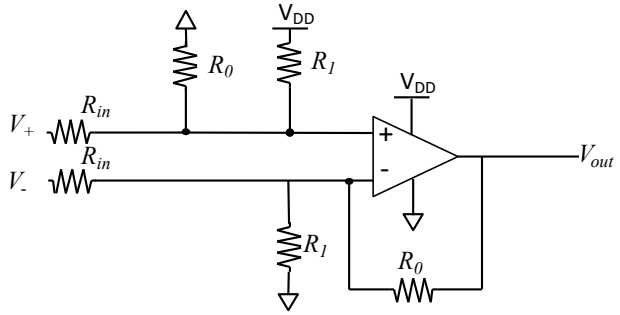

Figure 2.30: Conditioning stage schematic.

$$V_{out} = \frac{\frac{R_1 R_0}{R_1+R_0}}{\frac{R_1 R_0}{R_1+R_0} + R_{in}}(1+\frac{R_0}{R_{in}})V_{sh} + \frac{\frac{R_{in} R_0}{R_{in}+R_0}}{\frac{R_{in} R_0}{R_{in}+R_0} + R_1}(1+\frac{R_0}{R_{in}})V_{DD} = G \cdot V_{sh} + O \cdot V_{DD} \tag{2.21}$$

Where $V_{DD} = 3.3$ V, G is the gain and O is the offset.
According to the input scaling, the following sizing is chosen, considering that the gain can be assumed as the ratio $\frac{R_0}{R_{in}}$. Moreover, R_1 must be double of R_0 to polarize the output signal at half full scale

Table 2.5: Analog conditioning design.

Signal	**CM**	**DM**
Gain	5	55
Offset	0.5	0.5
R_{in} (kΩ)	2	2
R_0 (kΩ)	10	110
R_1 (kΩ)	20	220

Circuit capacitors are placed in order to filter the high frequency noise, considering cut-off frequency around 120 kHz.
The Opamp chosen is a two channels OPA2365, which is a compact solution, while all the resistors of the conditioning stage are standard values with 0.1% tolerance.

ADC and Digital isolator

ADC is AD7276 manufactured by Analog Devices. It is a 12 bits resolution AD converter with operation capability up to 3 MSPS and it is sized for high speed serial interface SPI.
The power supply of the ADC is filtered by the usual LC structure, in order to have immune voltage supply. The input clocks, CS and SCLK are stabilized by 22 pF filter capacitors. The outgoing sampled signal SDATA is filtered by the usual 10 Ω resistor.

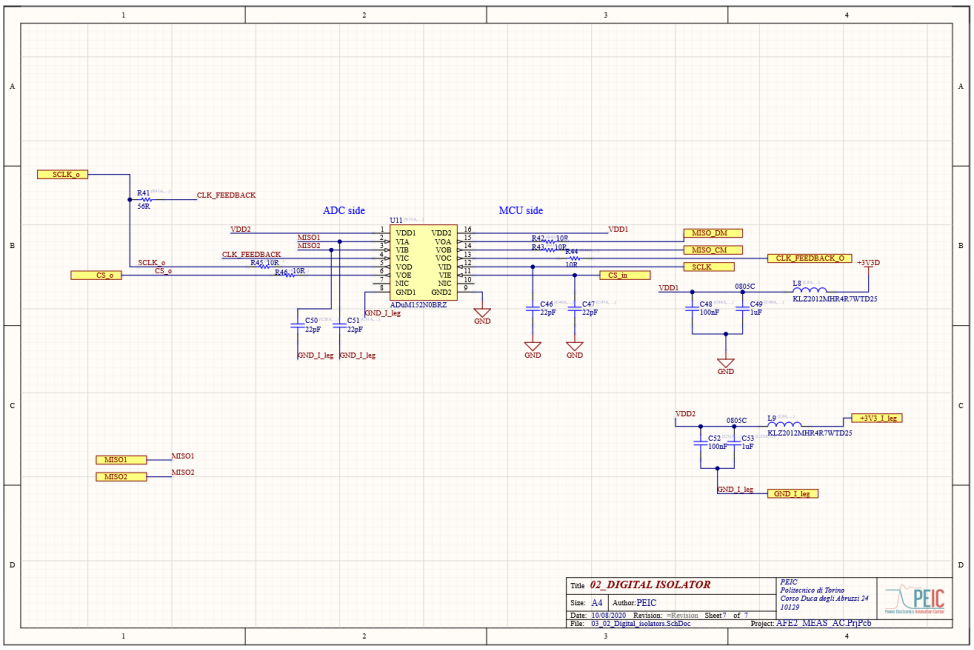

Figure 2.31: Digital isolator stage schematic.

Fig.2.31 shows the schematic of the digital isolator. The signals are filtered with the previous considerations and the isolated power supply stages are both low pass filtered as well.
The digital isolator is provided by Analog Devices and the final product chosen has been Adum163, due to its availability. The component main features are: 5-channels, high speed, complementary metal-oxide semiconductor (CMOS) logic, and monolithic air core transformer forming the isolation barrier and

delay time of 13 ns.

- **AC and DC voltage measures**
  The voltage measure structure is equal both for AC phase voltages and DC-link voltage. The reason is linked to the technology applied, which is a resistive voltage divider whose signal is managed by an insulated ADC, Sigma-Delta modulator. The modulator chosen is AMC1336 manufactured by Texas Instruments.
  The measure is directly digital and additional conditioning stage or an AD converter is not needed.

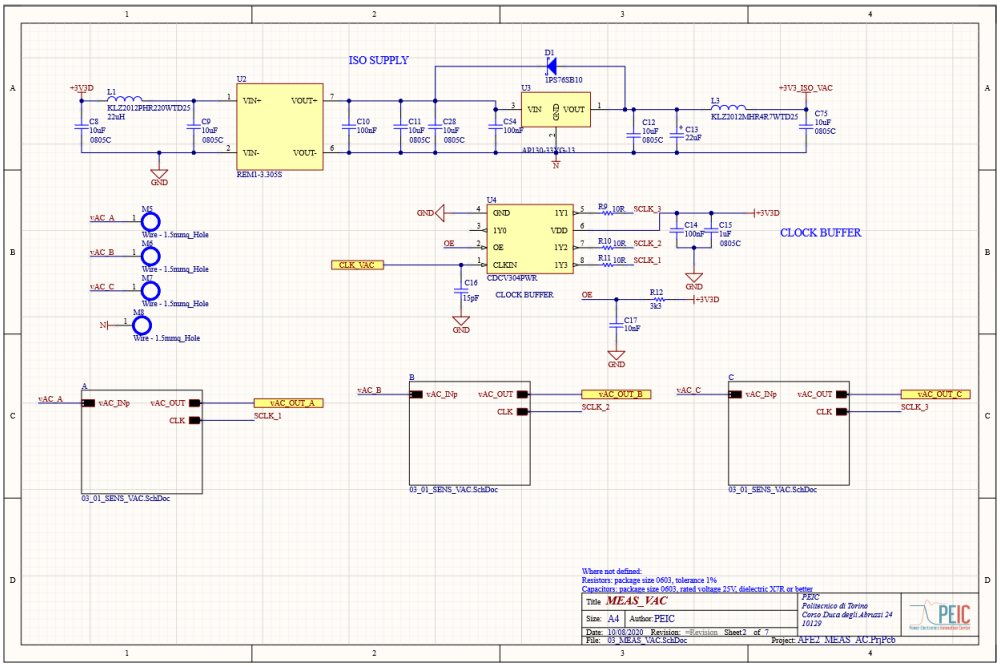

Figure 2.32: AC phase voltages measure schematic.

As can be seen in Fig. 2.32, where the upper level part of the AC voltage measure schematic has been designed, both clock buffer and insulated supply scheme are needed.
The reason of the presence of an additional clock buffer, used to replicate the high frequency signal clock for all the three modulators of the AC voltages, is that the not negligible power consumption of the integrated circuits introduces a delay in the signal transmission that must be compensated, with the detection of the signal clock as a feedback sent back to MCU.
Moreover the modulator introduces digital isolation. Therefore, it is necessary to provide the isolated power supply, with the circuit shown and that will be

explained at the end of the paragraph.
The Sigma-Delta modulator circuitry, can be seen in Fig. 2.35, where digital signal filters are applied, as it has been done for the power supply.
This solution has been applied because the MCU has 6 SPIs occupied by the current measures. Therefore, voltage measurements with the modulators are precise, compact and additional conditioning is not needed.
In fact, the AMC1336 modulator, as can be seen in Fig.2.33, is a second-order, switched capacitor, feed-forward sigma-delta modulator. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are subtracted, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in an output voltage V_3 that is again subtracted with both the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. The DAC responds on the next clock pulse by changing the associated analog output voltage V_5, causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input. The modulator can shift the quantization noise to high frequencies. Therefore, using a low pass digital filter at the output of the device improves the overall performance [17].

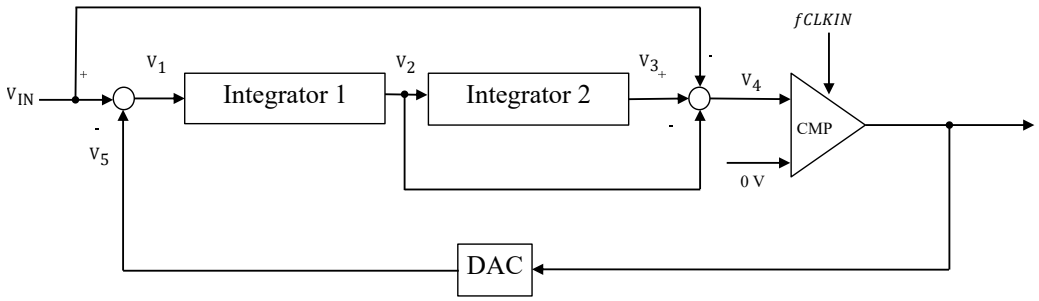

Figure 2.33: Block Diagram of Second-Order Modulator.

Starting from the voltage divider, the datasheet [17], suggests the methodology for designing the resistors. The AC input voltages, who have the common neutral point *N*, are scaled by the divider from their potential to 1 V full-scale. This lead to the resistors' values choice, which is tabulated, referring to Table 3 and Fig.51 of the datasheet and to Fig. 2.35.

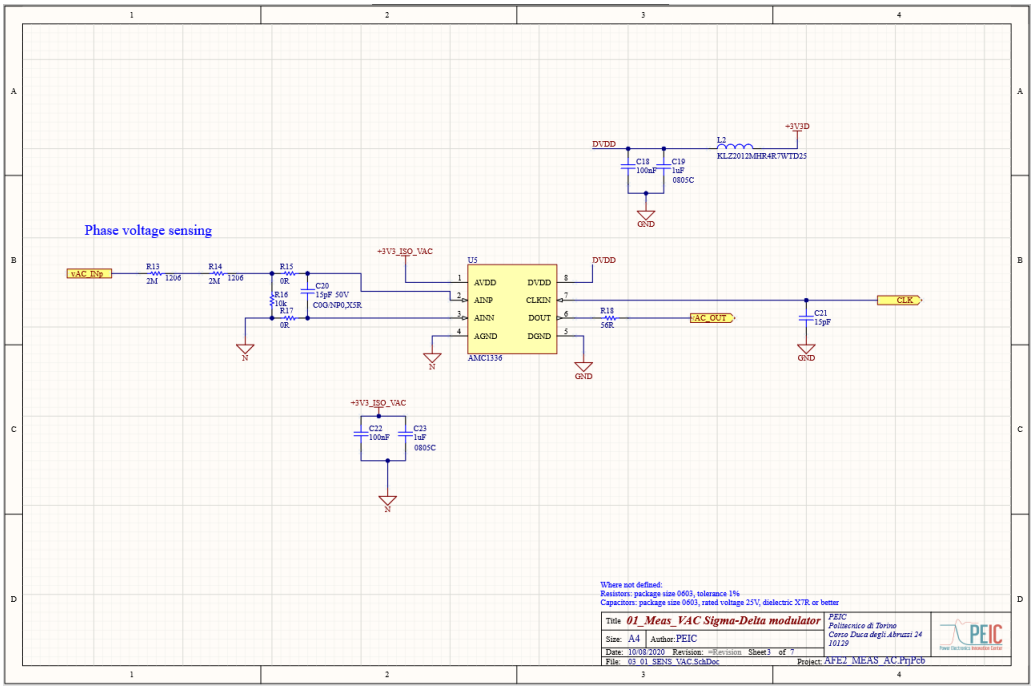

Figure 2.34: AC phase voltage measure with Sigma-Delta modulator.

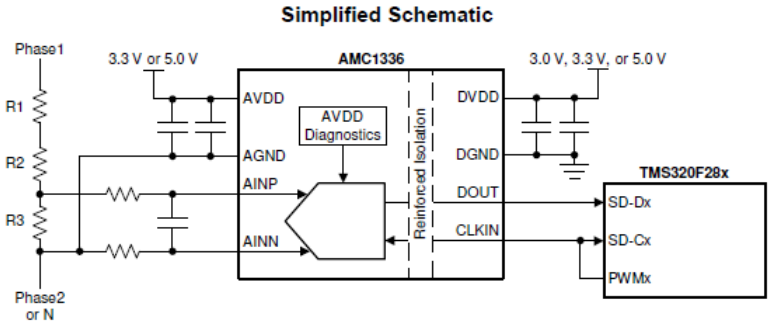

Figure 2.35: Simplified Schematic from the datasheet.

Table 2.6: AC voltage measure resistive divider.

Parameter	Value
R_1	2 MΩ
R_2	2 MΩ
R_3	10 kΩ

The two cascaded resistors after R_3 are used as filters and their resistance value is 0 Ω, while the shunt capacitor is a ceramic SMD 15 pF filter, with dielectric code C0G which means to the most stable capacitor.

A similar procedure has been followed for the DC-link voltage divider. The voltage from the positive potential to the mid-point and from the mid-point to the negative pole of the DC-link are detected. The measure layout is the same explained, but the size of the resistors is different.
The reference is Table 2 of the datasheet, but the full-scale of the input voltage is V_{in} = 450 V for both the measures. The ADC full-scale is always ±1 V. It has been decided to add to the two suggested series resistors of the divider, another one in series, called R_4. This lead to lower resistance and more standardized values.

$$V_{R_3} = \frac{R_3}{R_1 + R_2 + R_4} V_{in} \tag{2.22}$$

V_{R_3} is the ADC input voltage which is fixed, R_3 is chosen to be the same value, while the divider series resistors are equal in order to balance the voltage.

Table 2.7: DC voltage measure resistive divider.

Parameter	**Value**
R_1	1.6 MΩ
R_2	1.6 MΩ
R_3	10 kΩ
R_4	1.6 MΩ

The voltage divider resistors R_1, R_2, R_4 are sized with a standard imperial package of 1206, considering their power losses, while R_3 is chosen 0603. The tolerance of 1% has been chosen (E96 Standard Value).

To sum up, AMC 1336 Sigma-Delta modulator allows to have high resolution measurement of voltages, up to 16 bits, through a second order feedback analog comparator, which cancels the error with respect to the input signal.

Isolated power supply layout

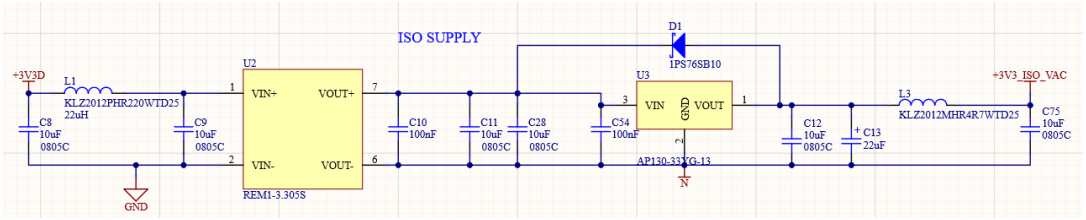

Figure 2.36: Isolated Supply Schematic.

The voltage and current measures need appropriate isolated supply, because the presence of digital isolation provided by integrated circuits. Hence, the isolated voltage is provided by the common power supply of the board, which is at 3.3 V. The usual input LC filter is used and then a switching isolated DC/DC converter, REM1-3.305S, makes the desired isolated potential. The outgoing voltage is then stabilized by a parallel of capacitors and filtered by a linear voltage regulator diode, AP130-33YG-13. The usual protection diode is added, and the output potential is empowered and more filtered by capacitors and another LC filter.
This structure has been used for the 5 different isolated power supplies on the board.

2.2.5 Carrier Board Schematic

Carrier board is a PCB project containing the following parts (as can be seen in Fig. 2.37):

- Schematic sheets managed with hyerarchical design:
  - Power supply stage;
  - Incoming and outgoing communications (UART, USB, CAN);
  - Incoming and outgoing signals exchanged with the other boards (Measures board, Drivers, Power In);
  - Precharge relays;
  - NTC predisposition for the temperature measurement;
  - Debug signals and internal communications (I2C, DEBUG, JTAG);
  - Connectors interfacing MCU board.
- PCB document.

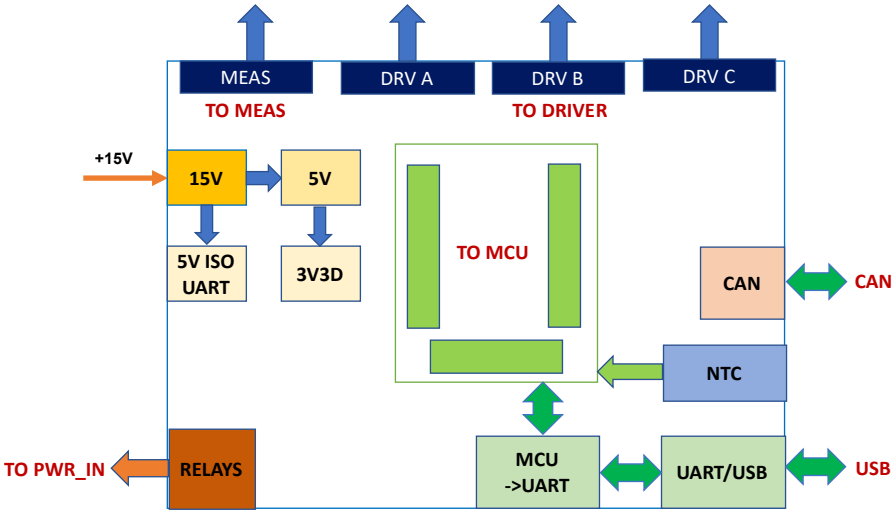

Figure 2.37: Carrier board functional scheme.

The reasons why it has been decided to exclude from Carrier board the MCU and its filters are the following:

- High degree of freedom in the implementation of the control technology, with the possibility to use MCU and also FPGA (Zynq), considering future developments;
- Carrier board contains all communication elements, connectors and signals from other boards, power supplies and NTC measurement, easily interfaces with the MCU board via connectors carrying digital signals and power supplies.

The connector must be designed with the constraints imposed by the FPGA, which must have pins dedicated to the power supplies and to the correct functioning of the FPGA itself, while MCU does not introduce particular problems.

Power Supply

The power supply voltage levels needed by the electronic parts of the converter's modules are the following:

- 15 V;
- 5 V;
- 3.3 V.

As seen in the Driver board, 15 V is necessary for the drivers. But in general 15 V is the input power supply voltage for the entire control circuitry. From that,

the other two voltage levels have been obtained via DC/DC converter, as can be noticed in Fig. 2.38.
Analyzing in more detail, the 15 V level is regulated to 5 V by a SMD step-down DC/DC switching converter, TPS565208 manufactured by Texas Instruments. Its input is filtered as usual, while the output voltage is heavy filtered and stabilized by a second order RLC filter and cascaded capacitors.
The more used 3.3 V voltage level, which is brought to all the boards from the Carrier, to supply all the electronic circuits and impose the full-scale of the signal conditioning, is obtained from the 5 V. A DC/DC linear not isolated converter has been used in order to clean more the voltage (LM1084ISX-3.3/NOPB by Texas Instruments). The output voltage is stabilized by a RC filter (with cut-off frequency around 14 kHz) and it is called inside the schematic *3V3D*, which meas that this is the supply of the digital part of the electronic circuits. Instead, the analog 3.3 V is obtained by LC filters (already seen in the previous paragraphs for the integrated circuits supply) which decouple the two voltage levels.

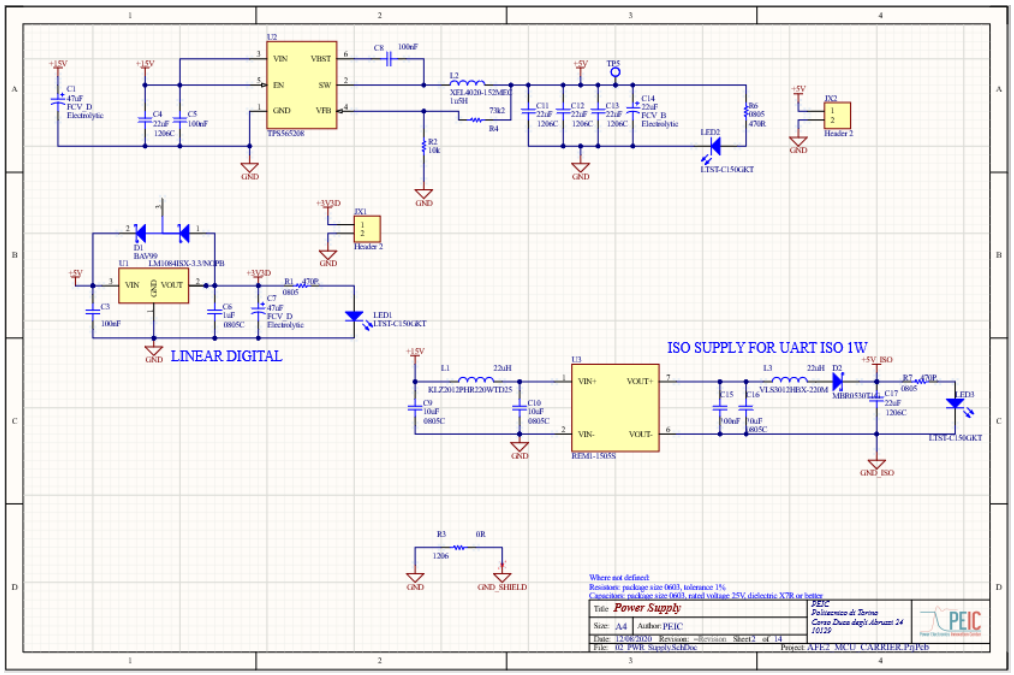

Figure 2.38: Carrier board power supply voltage levels.

Moreover, an isolated 3.3 V power supply has been designed with the same layout seen for the isolated power supplies of the Measures board and the Driver board. This is needed for the communication circuitry that is isolated (CAN, UART, USB).

UART, USB and CAN Communications

The user-side communication protocols and the relative circuits, designed in the Carrier board, are as follows:

- UART: Universal Asynchronous Receiver-Transmitter is a serial communication using two transmission/reception lines (Tx and Rx), where data are transmitted asynchronously without a signal clock (Tx and Rx signals are mirrored if considered by MCU or user point of view);
- USB: from the UART, USB communication has been derived, in order to allow the direct connection of a PC via micro-USB connector;
- CAN: Controller Area Network, is a serial field bus standard that is designed to operate in environments strongly disturbed by the presence of electromagnetic waves (EMI immunity increased if twisted pair cables are used). It is adopted for the communication with the external LLC stage of the battery charger.

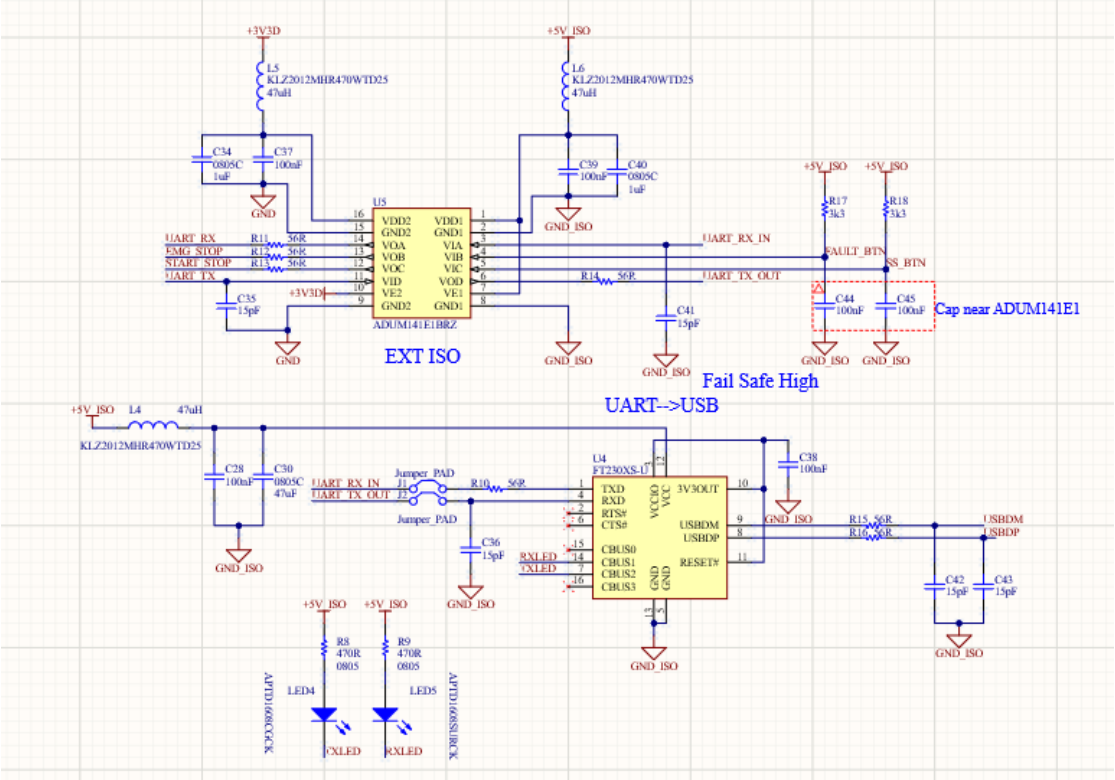

Figure 2.39: UART and USB Schematic.

As can be noticed in Fig. 2.39, UART signals coming from MCU board are isolated by a digital isolator (ADUM141E1BRZ manufactured by Analog Devices), then

the signals are brought to a four positions horizontal header (22-05-7045) and to the USB digital converter (which transforms the USB signals to UART and vice versa).

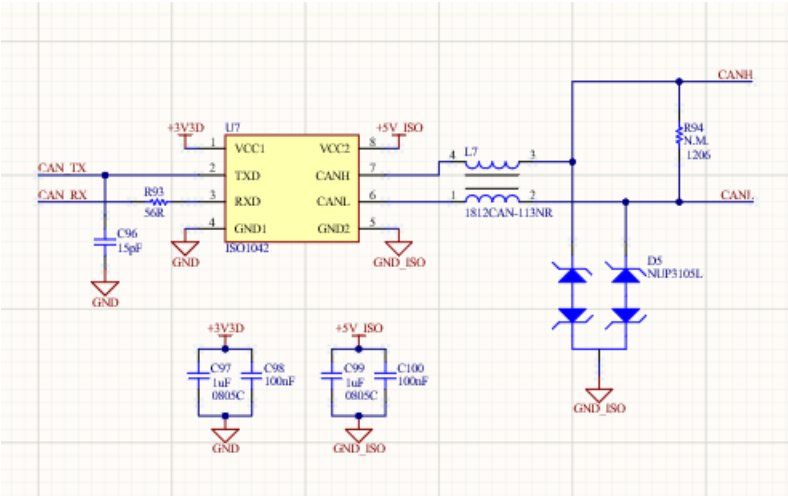

Figure 2.40: CAN Schematic.

CAN signals coming from MCU board pass through an isolated CAN transceiver (ISO1042 provided by Texas Instruments), which makes the communication isolation. Then the outgoing signals are exported with the same horizontal connector used for UART.
For each circuit the filters for the digital signals are implemented (resistors for output signals, capacitors for input signals and LC filters for the power supply).

Interface with other boards

The Carrier board's interface with the other boards has been realized as much as possible with the same connector typology. In fact, for the three Driver boards and the Measures board, signals and power supplies are exchanged via the 20 positions FPC horizontal connector seen in paragraph 2.2.3 (see Fig. 2.41). However, for the DC-link voltage measure signals it has been adopted an additional horizontal connector (22-05-7055) because of the large number of signals from the Measure board and spaces on the board.

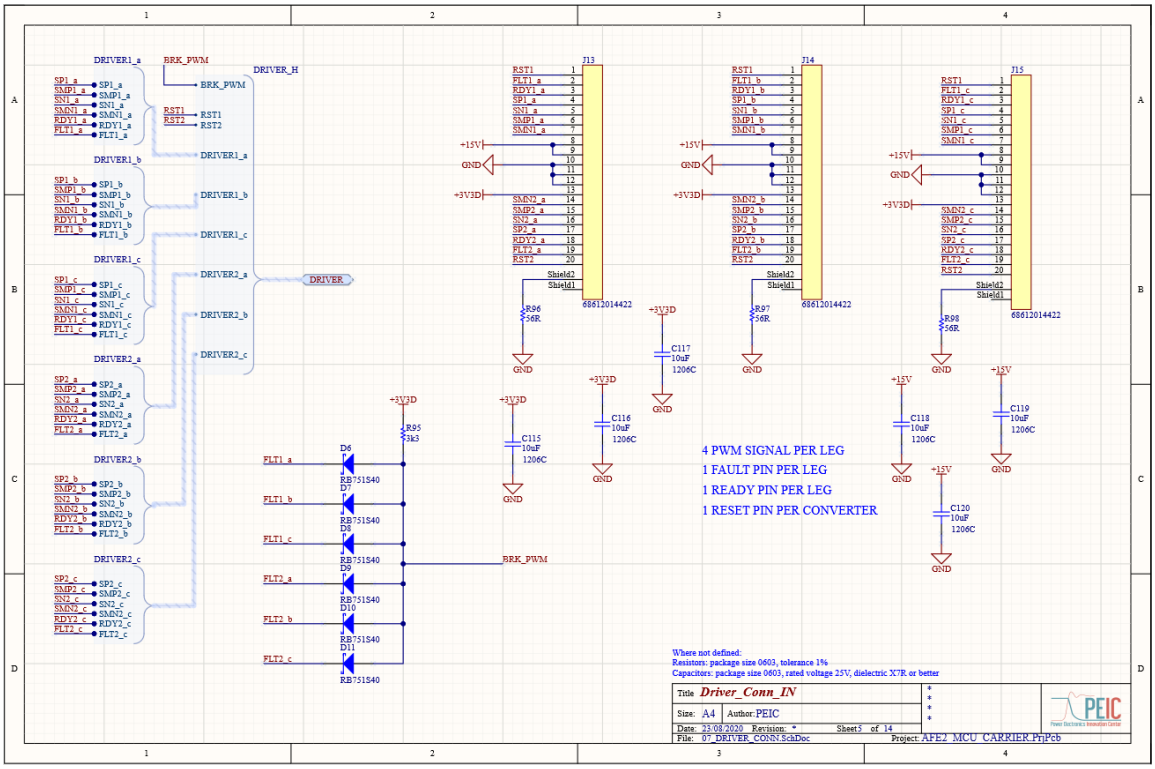

Figure 2.41: Connectors and signals to Driver boards.

Precharge Relays

The precharge relays, which are the PTC resettable resistors inserted in the Power board, are controlled through two signals outgoing from optoisolator triacs (VOT8024AM-T), whose voltage reference in the isolated part is the mains' voltage. The triac are isolated with the zero voltage detection circuit integrated. When the primary side is supplied with a current over 5 mA, the secondary is isolated. The main advantages of this solution are that the supply is the usual 3.3 V, the compactness and the absence of mechanical parts.
The trigger for the precharge control comes from the two NPN bipolar transistors, driven with two signals *K1* and *K2*, coming from the MCU board.

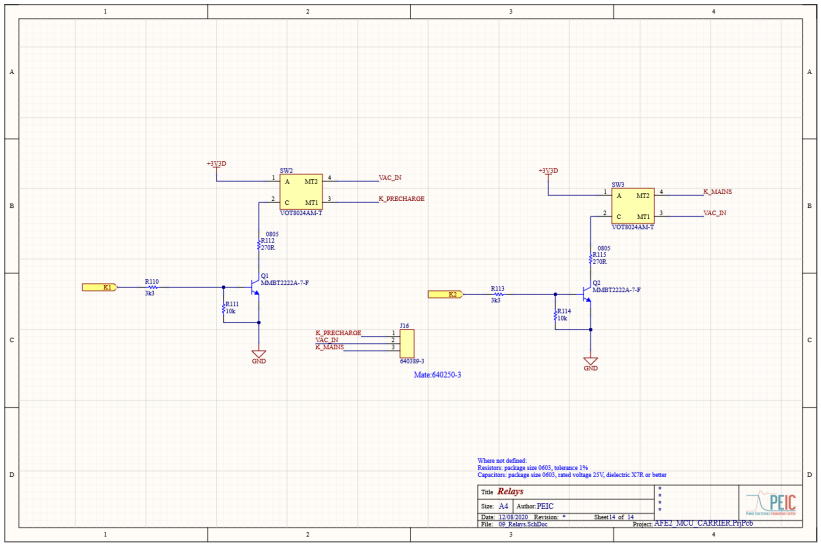

Figure 2.42: Precharge and overcurrent protection relays.

NTC predisposition

NTC (Negative Temperature Coefficient) thermistor are variable resistors with the temperature. If the thermal equilibrium is reached, a voltage signal is obtained through voltamperometric measurement of the voltage drop over the thermistor, which is fuction of the temperature. Being an analog signal it has to be conditioned with the circuit shown in Fig. 2.43. This stage is a predisposition for future implementation of NTC measure inside the Power board.

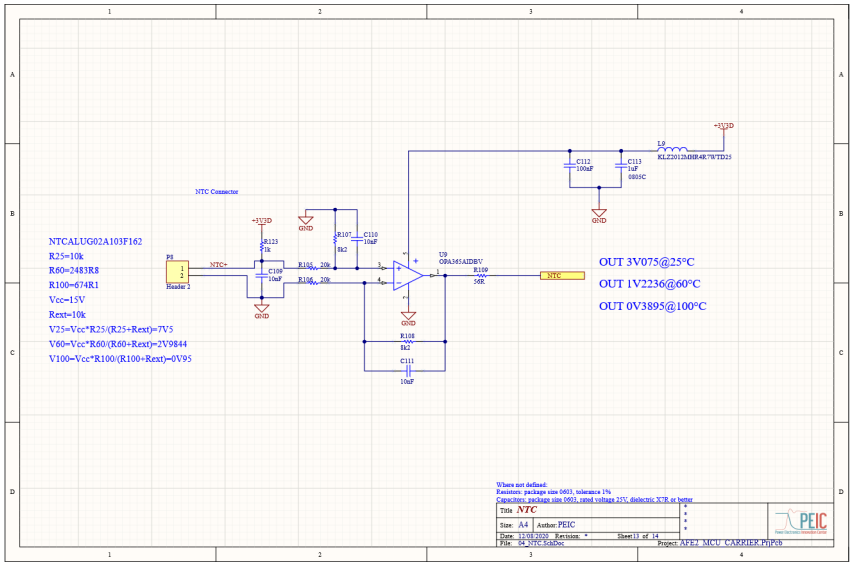

Figure 2.43: NTC schematic.

Debug signals and internal communications

As usual for the control boards, also in the Carrier board debug signals coming from the MCU board are present, carried to reserved headers.
The debug signals that can be noticed inside the schematic sheets are referred as:

- Debug: general programmable debug signals, routed from reserved pins of the interface connectors with MCU;
- JTAG: hardware interface to communicate directly with the MCU or the FPGA.

Additional signals used for communications and external setting of the MCU (or the future FPGA) are inserted and wired up.
Moreover, it has been decided to add an external DAC (digital to analog converter), which is useful for debugging and measuring purposes, with digital signals that can be managed as analog ones (Fig.2.44).
The communication with the microcontroller is made with two digital lines (SCL and SDA). MCP4728 DAC (4 channel 12 bit) has been selected,whose pins are open drain, therefore, pull-up resistors (between the pin and 3V3D) are needed. The power supply is provided by the usual LC filter, then the analog outputs are carried to an 8 pin header (4 signal pins and 4 GND pins) via a RC filter (R=56 Ω and C=10 nF).

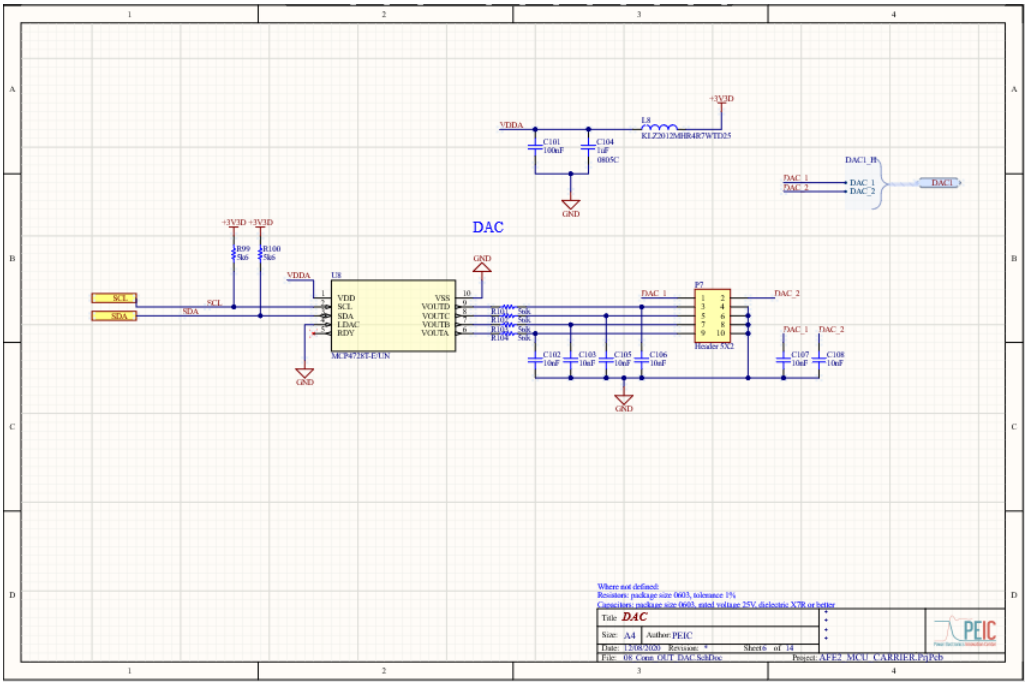

Figure 2.44: External DAC schematic.

Connectors interfacing MCU board

The connectors shown in Fig.2.45 are the most critical component of the Carrier board, because they make possible the exchange of a large number of signals and also the power supply with the MCU.
These connectors are three, two of them are the same component (called Part A and Part B) LSHM-150-04.0-L-DV-A-S-K-TR manufactured by Samtec, with 100 pins, divided by 50 per row, while the third is LSHM-130-04.0-L-DV-A-S-K-TR by Samtec, with 60 pins, whose 30 per row (called Part C). The main feature of these connectors is that they are self-mating and non-gendered, which means that there is not a male or a female part, but one component can be both of them and provides an easier mating (odd pins must be connected with even ones).

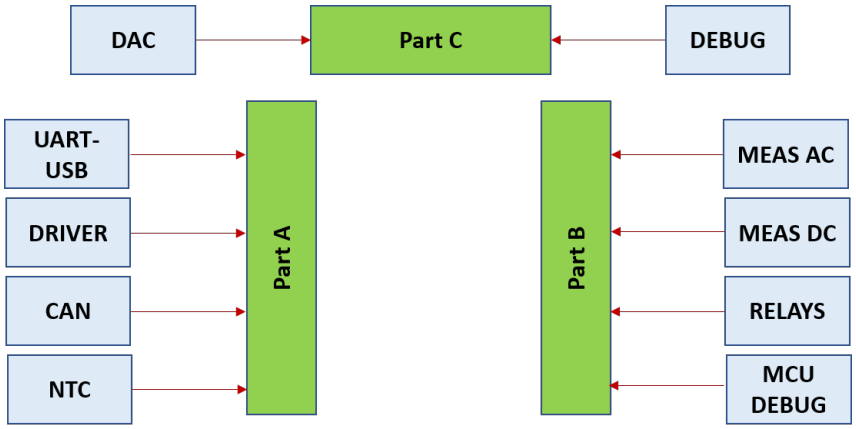

Figure 2.45: Connector to MCU Block Scheme.

The most critical issues are the constraints on connectors' footprint which must have very precise mechanical measurements, in order to allow the correct coupling with the MCU board. It has been necessary to make the component symbol and PCB model.
Moreover, it has to be underlined that the signals for MCU and FPGA are different. FPGA has all accessible pins for the signals, with some signals reserved (requested for the complete functionality and setting) that need dedicated pins. MCU, on the other hand, has different reserved pins. Hence, it is necessary to verify the pinout of connectors, which must allow to use both solutions. In addition, the power supply pins must be the same.

In Fig.2.46, the schematic of Part A connector is shown. The layout of the schematic is the same for the other two connectors.
It is possible to notice that the usual digital signals' RC filters are placed in the Carrier board, near the connectors, because the MCU board is really small.

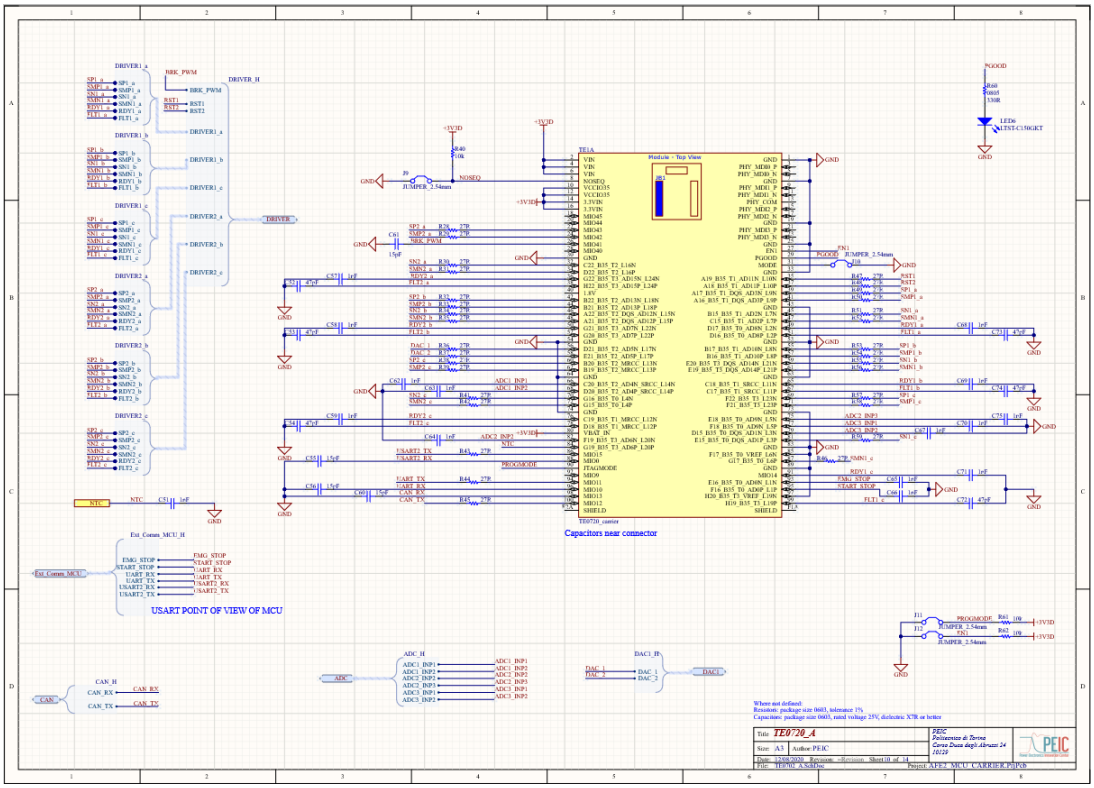

Figure 2.46: Connector to MCU Part A

2.2.6 MCU Board Schematic

MCU board PCB project is composed as usual by the following files:

- Schematic sheets managed with hyerarchical design.
  MCU (microcontroller unit) board schematic is quite simple. As can be noticed in Fig. 2.47, which shows the blocks composing the board, where only two main components are part of it:
  - Connector interfacing Carrier board;
  - MCU.
- PCB document.

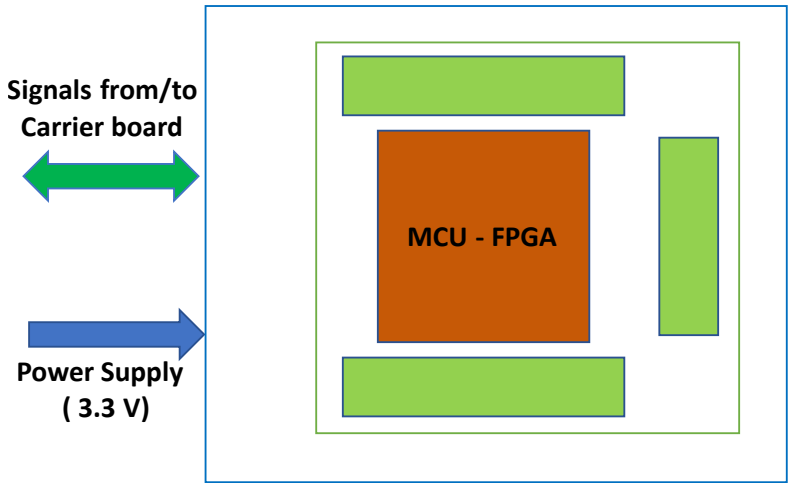

Figure 2.47: MCU board Block Scheme.

Connectors interfacing Carrier board

The three connectors that allows the coupling of the board with the Carrier board are the same described in the previous paragraph. The reason is due to the technology of the connectors produced by Samtec, which are self-mating and not-gendered. Therefore, it is simple to connect them if the mechanical measurements are precise, because with the same two components, the mating is possible by mirroring them. This leads to the necessity of taking care of the signal wiring in both the boards, MCU and Carrier, because the odd pin of one board will be connected to the even pin of the other one (i.e. pin 1 of Carrier board will be mated to pin 2 of MCU board).
Moreover, in order to guarantee the correct measurements, it has been created a unique component in the library containing the three connectors (with the symbol for the schematic and the PCB model), which is the mirrored version of the one made for the Carrier board.
The schematic is organized in different sheets, which represent the parts of the connectors and the units of the MCU. Hence, the large number of signals that has to be wired up, needs to be managed with harnesses, which make the schematic more compact and easy to read.
All the pins of the MCU have been brought to the connectors' child sheets, including the free pins of the MCU. These could be connected to the free pins of the connectors for future variations, so to have freedom to change the layout of the MCU if it is used in other projects, but for this project they are not routed.

Fig. 2.48, shows one of the three connectors, called Part A, which can be compared to its mate represented in Fig. 2.45. As can be noticed, all the filters are

placed into the Carrier board, while the MCU one is pretty empty for size reasons.

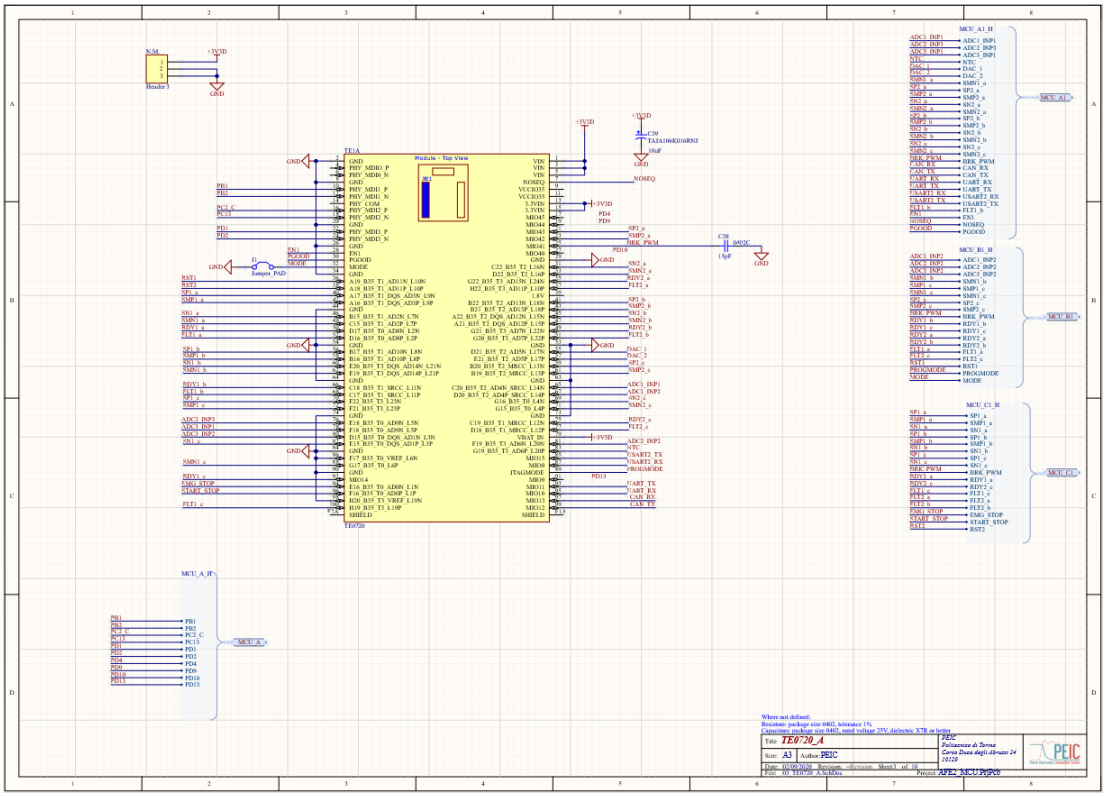

Figure 2.48: Connector to Carrier board Part A

MCU

The MCU needed in the project, had the specification of being dual core, in order to perform all the code computations with limited timing and reach the requested switching frequency. The problem was that it has to manage a very large number of signals. Hence, the component selected has been the STM32H745XIH6 manufactured by STMicroelectronics, with package TFBGA240. It is a thin BGA (ball grid array) which is a type of surface-mount packaging. It is used to permanently mount the device, in order to provide more interconnection pins. In particular, the whole bottom surface of the device can be used, with the distributed ball pins (i.e. 240 pins available).
MCU has reserved pins with signals that are carried to the connectors in order to guarantee the correct functionality, and these in some cases, such as the debug signals, are in common with the FPGA selected for future applications (i.e. one of the Zynq architectures manufactured by Xilinx).

In the schematic sheets additional components used are needed by the MCU

itself. These are the following (referring also to Fig. 2.49, where the channel B of the I/O ports schematic is presented) :

- Resistors and capacitors used as filter of the outgoing and incoming signals to MCU;
- External SMD 25 MHz oscillator, ECS-TXO-2016-33-250-TR manufactured by ECS (see Fig. 2.49);
- Capacitors needed for stabilizing the power supply voltage for the power pins of MCU;
- LC filters making the analog power supply needed by the MCU from the digital 3.3 V.

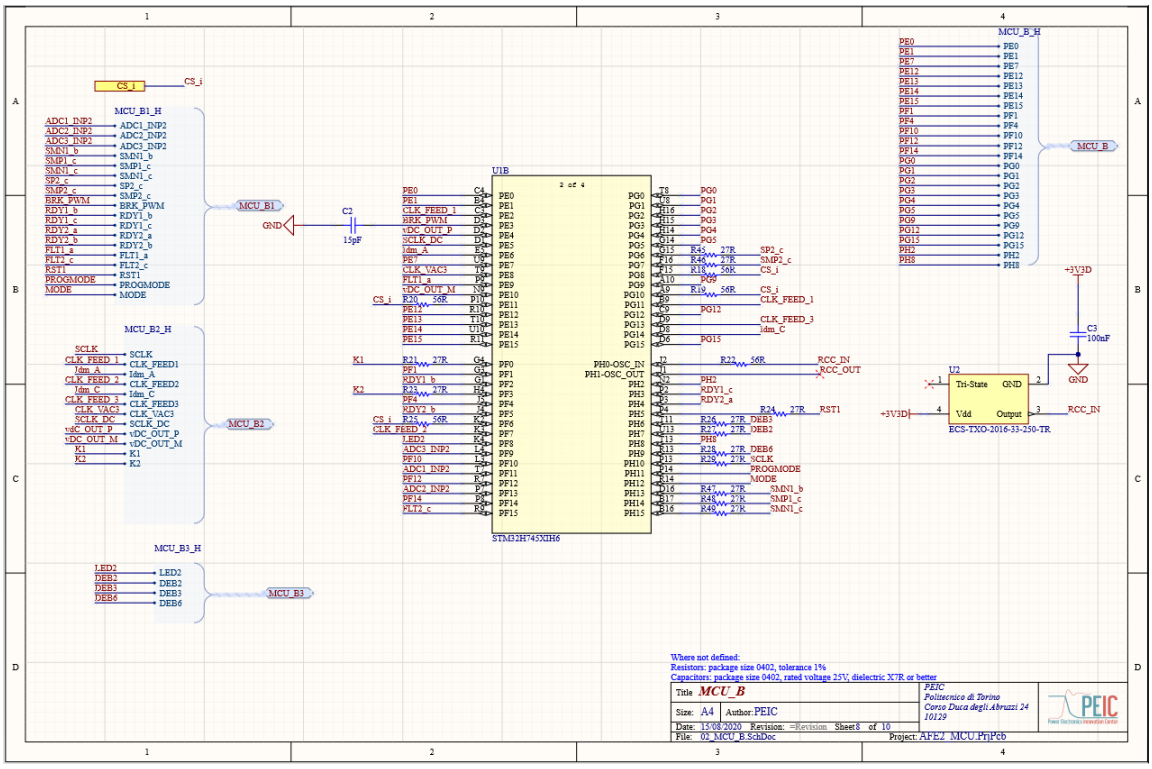

Figure 2.49: Channel B of the MCU.

2.3 Design of the Printed Circuit Boards

In this part of the master thesis the PCB document design of each project will be presented, with the description of the main processes and critical issues encountered. Indeed, the second step of the hardware design of a converter is the creation of the boards, while the third is the definition of the list of components needed to be acquired, called Bill of Materials (BOM).
A printed circuit board (PCB) is a mechanical support and allows electrical connections for electronic components, through conductive tracks, pads, vias and other features, in order to manage the connections between one or more sheet layers of laminated copper between sheet layers of non-conductive material (due to the copper planes extraction). The components chosen in the schematic design stage, are in general soldered on the PCB to create electrical and mechanical connection. Moreover, the PCB design has a high degree of freedom, because a board can be made in any shape, and designed as a rigid board, rigid-flex or pure flex. PCBs can be made single-sided (i.e. one copper layer), double-sided (two copper layers on both sides of one non-conductive layer), or multi-layer (inner and outer layers of copper, alternated with non-conductive layers). Multi-layer structure allows a higher component density, because the components can be both placed on the top and bottom layer, while the traces can pass through the inner layers, not only on the external surfaces.
Multiple layer design is the one adopted for the project, the most used is a four layers layout, while in two particular cases, characterized by a large number of components or pins to be connected, six layers have been used.
The PCB design is a process formed by a sequence of stages that lead to the final result. Some of them are fixed and are the base of the design, with the definition of the dimensions, rules, grids. The two main stages, which are the components' placing over the board and the routing of the tracks, are iterative, because the creation of the board to be printed it is not a one shot procedure but it is the result of a process of optimization of space, improvement of electrical connections and the need to meet the constraints, so as to achieve the final goal, as is schematically explained in Fig.2.50.

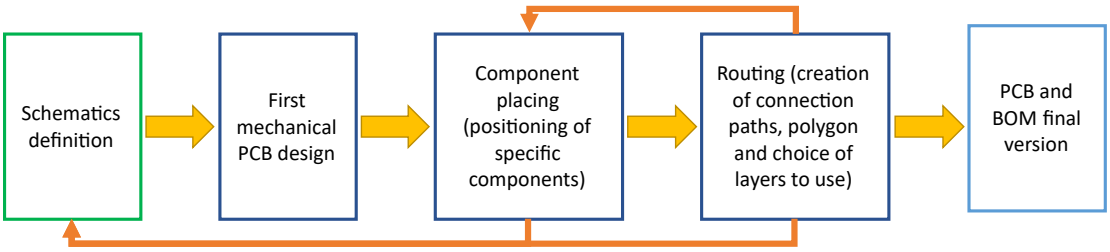

Figure 2.50: Hardware Design process.

In fact, the first step after the creation on Altium Designer of an empty PCB document, is the definition of rules, which sets the constraints to be respected both electrical and mechanical. Rules are defined independently of the objects. During editing or rule checking, the program automatically identifies the highest priority rule that has to be applied to each object and verifies the correctness of every action.
The PCB editor is a workspace where it is possible to toggle between the 2D and 3D display of the board. It is possible to work with metric or imperial, cartesian or polar grids, where multiple snap grids can be overlaid.

After the definition of the board size and the setting of rules and grids, the design stage starts with the components' placing.
Firstly, the design is transferred directly from the schematic editor to the PCB editor. When the schematic is imported inside the PCB editor, the project is compiled and the following lists are created and added to the document:

- List of components used in the schematic and related footprints (which must be present in the library);
- List of all nets (connected component pins) which is the guide for the tracks routing stage;
- Additional design data, such as rooms and net or component classes.

After this actions, the components are arranged inside rooms, which are objects corresponding to the sheets of the schematic and have useful features:

- If components are placed and routed inside the room, it is possible to copy the layout to other replicated rooms (when the Repeat function is used in the schematic);
- The components belonging to a room can be moved at the same time if the room is moved;
- Each room can be edited and modified.

Therefore, the placing can be performed both moving and managing a room or directly moving, rotating and arranging each component.
Additional components can be added even if not present inside the schematic, which are designed for the PCB editing and are called primitive objects:

- Vias: primitive design object, used to form a vertical electrical connection between two or more electrical layers of a PCB;

- Pads: primitive design object, used for fixing the component to the board and for creating the interconnection points from the component pins to the routing on the board or to create holes;
- Cutouts: it is a cutout of the board, where the material is exported. They are used to mechanically guarantee the insulation;
- Polygon pours: object that is made up of simpler primitive objects. Polygon pours are used to create a solid area on a PCB layer that can be assigned to a net class.

The second stage is the track routing. It can be stated that a good component placement is the most important aspect to good board design, because with a good placing, routing is not a tough task. Routing is the process of laying tracks and vias on the board to connect the component pins.
Also the routing process is characterized by a set of rules that have to be correctly designed. These are needed to impose the main features of the tracks and the isolation of each part, avoiding unexpected fails and critical behaviours.

- Routing Width: maximum, minimum and preferred routing width for each track class can be edited;
- Electrical Clearance Constraint: minimum clearance allowed between any two primitive objects on a copper layer. Both single value for clearance or different clearances for different object pairings can be specified;
- Routing Via Style: style of vias that can be used when routing. Both specific values for the via's diameter and hole size, or via templates can be selected.

Before the description of the AFE PCB design a series of fundamental rules that have to be taken into account when the hardware design is performed.

General features of the PCB design and guidelines for reduced EMI
The design of a PCB is a complex task, where many aspects related to different engineering fields must be considered. In this master thesis a number of aspects of the electrical and electronic design of a PCB have been explained, while others will be analyzed in the following paragraphs.
It is possible to summarize additional features related to the PCB design, before starting with the description of the boards of the AFE. In particular, an in-depth examination can be made of some of the technologies used most in this project and a focus on problems related to electromagnetic interference, which are common inside every electric and electronic circuit [18].
The components used for the electronic circuits and the PCBs in general are divided in two categories: the through hole mounted devices and the usually

adopted surface mounted devices (SMD). The through-hole mounting is the process where the component pins are placed into drilled holes which go through the inner layers of the PCB. On the other hand, the surface mounting is the soldering of the pins directly onto the surface of the PCB, avoiding the use of holes. Both the technologies have advantages and disadvantages, that can be summarized:

- Advantages:
  - Through hole mounting is featured by mechanical strength and easy replacement which makes the devices preferable for testing prototypes. When the mechanical stress could be an issue, this kind of components are the most suitable (i.e. connectors, high power switches, transformers, electrolytic capacitors).
  - Surface mounting is characterized by smaller size of the devices lead to a reduction of the board dimensions. As a consequence an higher component density can be reached. SMDs are characterized by reduced parasitic parameters (such as the reduced inductance of the shorter pins), which is a crucial factor. Moreover, less drilling holes are required that reduce the PCB manufacturing, that becomes less expensive and allows a faster automated production. The soldering is more reliable and repeatable because of the use of automatic machines. This allows to provide an higher performance for the reliability against the vibrations.
- Disadvantages:
  - Through hole mounting requires the drilling holes, which is expensive and leads to much longer times for the manufacturing. In addition the holes reduce the available routing area on the multilayer boards, causing a non optimized components density.
  - Surface mounting is less reliable respect the through hole one when used for components which are subject to mechanical stress or are in a harsh environment. Besides, these components are less easy to handle for reworking and prototyping purposes.

Hence, the SMDs have been preferred for the possibility to contain the dimensions of the PCBs, while the through hole devices are used when the reliability and the mechanical strength have to be assured.
The SMD devices are characterized by standardized packages and footprints. Different codes related to the package of ICs, switches, power supply and passive elements, such as resistors, capacitors and inductors can be encountered. In particular, a focus on the passive components can be made, while the sizing factors are as usual the power that can be dissipated, the voltage that can be sustained and

the current that can be conduced. The SMD passive devices packages are listed in standard tables, while are different from the point of view of the parameter's tolerance. The imperial sizing is the most widespread and the code explains the component's dimensions width x height in mils (0402 and 0603 are adopted both for imperial and metric codes but define different sizing). The most used components have the following imperial codes:

- 0402: used for the filters of the signals and bypass capacitors, which do not require high power to be dissipated;
- 0603: used for the filters of the signals, the power supply capacitors and for the feedback networks, not requiring high power to be dissipated;
- 0805: used for power supply low pass filters, when it is necessary to introduce a dynamic separation in the supply system. Moreover, this size can be adopted for components where the power to be dissipated or the voltage to be sustained are not negligible terms;
- 1206: used for the power supply system or the measure of the power part's electric quantities because of the higher voltage rating requested by the application.

Another aspect of the PCB design is related to the electromagnetic interference (EMI). The reason to analyze in depth the techniques to contain the interference is that the radio-frequency noise is present in every output, input, power supply and ground itself at the same time when an electronic device is part of a circuit. The most relevant noise is the one generated by the integrated circuits' (ICs) I/O pins, because the area covered by the traces of the PCB forms a large antenna. In particular, the noise coming from the clocks and the switching signals of the IC appears as glitches at the output, which are due to common impedances to the pins of the IC itself.
The power supply system is another source of noise because of the voltage regulation and the bypassing capacitors (which are needed to supply the high frequency current used by the integrated circuit for its operations, making the power supply immune from high frequency currents).
In fact, every edge variation of the signal transmitted or received by an electronic device makes a current pulse. This current follows a path between the transmitter and receiver devices through the copper tracks. The return path is represented by the ground pin of the device, ground traces and polygons. This current pulse travels in a loop with the lower impedance to return where it is originated. These loops are present everywhere inside a PCB and the main strategy to control the return paths is to design and manage the lower impedance route. Hence, with particular reference to the 2D view of each PCB the following features can be

noticed.
Starting from the minimization of the impedance in the signal path, it is important to have short loops for reducing the parasitic inductance which is a parameter that gets worsen the noise and higher the impedance. The most used technique is to insert copper polygons under the ICs to close the return path near the device. This is the reason why the ground is made by an extended polygon all over the board, mainly arranged in the inner layers.
A similar strategy can be adopted for distributing the power supply, making the region equipotential through a polygon and eventually vias. In addition it is better to add filters for digital and analog power supplies in order to contain the disturbance that can be transmitted inside the supply system (as seen in the paragraphs about the schematics), such as a parallel of capacitors in a 0603 package, with a value of 100 nF near the supply pin of the IC, while the second one can be positioned more distant and has bigger dimensions i.e. 0805 and 1 µF sizing. The smaller capacitor, with the 0603 package is needed as a filter for the high frequency noise, because it shows a reduced high frequency impedance. The other capacitor with a value of 1µF requested for ensuring the local energy storage.
Moreover list of useful guidelines can be followed to reduce noise inside regions where copper polygons are used:

- Avoid internal divisions inside the board's planes with holes and cutouts that could make loops longer;
- Avoid buried traces in the ground polygon. It is better to put them in the 3.3 V plane;
- When an isolated area is defined, it is important to integrate all the components of that part;
- The connection between a device terminal and a polygon should be made with vias close to the device.

The disturbances that can affect the signals managed by the I/O pins of integrated circuits are coupled internally to the device through different paths. Therefore, a general methodology to contain the interference and guarantee the quality of the signals transmitted or received (avoiding possible unwanted triggers of control functions due to a glitch of the signal), is the adoption of local filters which are used to keep the noise close to the chip. These RC filters are the ones analyzed in section 2.2.3, that can be described with a PCB oriented view:

- Resistors (10 Ω to 100 Ω) in series with every output pin, to be arranged as close as possible to the IC pins. In general, a package 0603 and 56 Ω is used;

- Capacitors (12 pF to 1 µF) tied to the receiver input pins. The capacitor has to be placed nearest as possible to the pin and the other end of the capacitor is grounded. The most adopted is a 0603 package with 15 pF.

In the next sections the main results and features of every designed board of the AFE, will be discussed, following the same order of presentation as the schematics.

2.3.1 Power Input PCB

The Power Input board is the first module of the AFE which is connected to the LV grid. This connection is made with wires, whose section has been sized. The input connectors are arranged on the bottom side of the board but the footprint can be seen in the bottom right corner of Fig.2.51 and Fig.2.52. Downstream of the entrance, the other main parts of the board are underlined in Fig.2.51. The board has an overall dimension of 210x206.5 mm and has been realized with 4 layers, which are linked to different colors inside the 2D view of the editor of Altium Designer:

- Top Layer (red);
- Mid Layer 1 (brown);
- Mid Layer 2 (light blue);
- Bottom Layer (blue).

The availability of multiple layers is useful both for the placing of the components, but in particular for the tracks routing. In fact, the common mode inductors and the differential mode inductors are the components that fix the positioning of the others on the board. Therefore, the most of them have been arranged on the Top Layer, while the star-connected capacitors and the shunt resistors with the related connectors are placed on the Bottom Layer.
Moreover, the power connections have been realized with equipotential copper made polygons on several layers, arranged two by two in order to reduce possible parasitic couplings and distribute the current as much as possible.
Stitchings inside the polygons have been added, through a specific function of the editor, where it is possible to fix the dimension of the vias and of the grid. The most suitable dimension of the vias is related to the size of the polygon itself, while the stitching has to be concentrated near the pads of the components. The reason is that the vias introduce multiple crossings of the board between the polygon layers, which increase the equipotentiality of the polygon itself, distributing the current density in the best way. However, they also introduce copper shrinkage and parasitic inductance, so they should be limited to the areas where they are needed and should not be inserted in the central areas of the copper. The connections between the filter capacitors are made through copper tracks with a thickness of 2 mm, because the flowing current is a reduced percentage with respect to the power one. Besides, the tracks which carry the current measure signals are sized as 0.5 mm thick. The main rules set for the PCB concern the clearance between electrical objects, such as components, traces and polygons, that is needed to ensure the correct isolation. In general, the clearance of the power parts is fixed at 2.5 mm.

On the other hand, for signal tracks and shunts, the clearance is reduced to 0.25 mm. In addition, the outline board clearance of each board is set at 0.5 mm, to guarantee minimum insulation with respect to the outer edges.

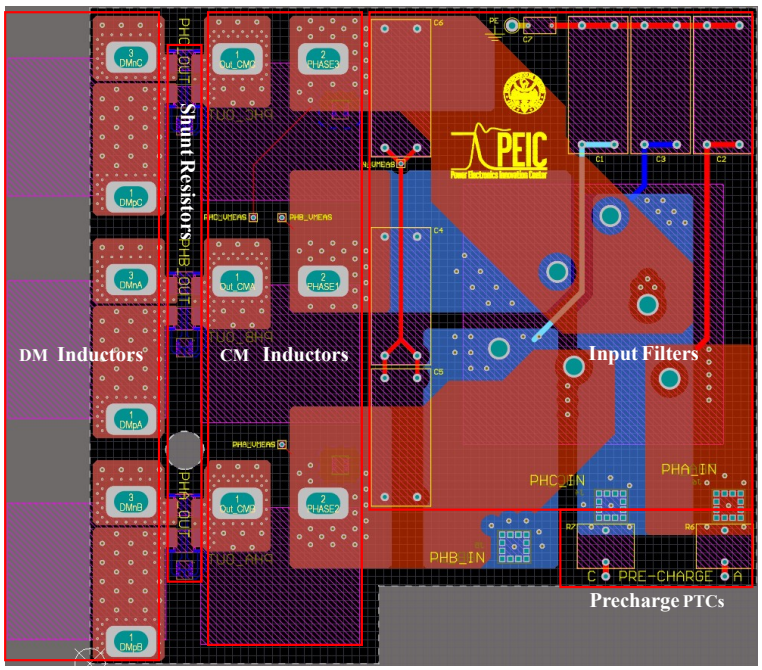

Figure 2.51: Power Input PCB 2D Layout.

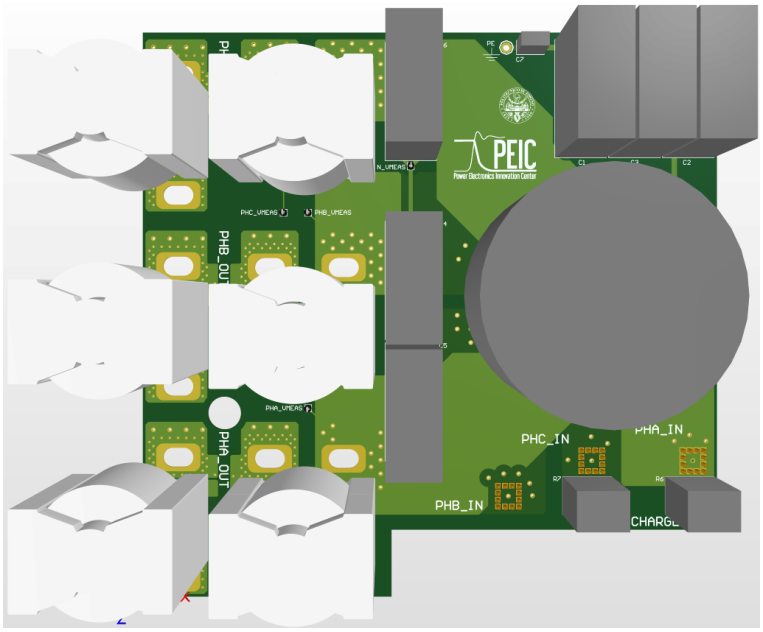

Figure 2.52: Power Input PCB 3D Layout.

2.3.2 Power PCB

The Power board is the power module of the AFE containing the Three Level T-Type Inverter and the DC-link as can be noticed in Fig.2.53 and in the 3D top and bottom side views (Fig.2.56 and Fig.2.57). The board has an overall dimension of 202x293.5 mm and has been realized with the conventional 4 layers:

- Top Layer (red);
- Mid Layer 1 (brown);
- Mid Layer 2 (light blue);
- Bottom Layer (blue).

The connections are realized mainly through copper polygons arranged in every layer, as can be noticed in Fig.2.53.

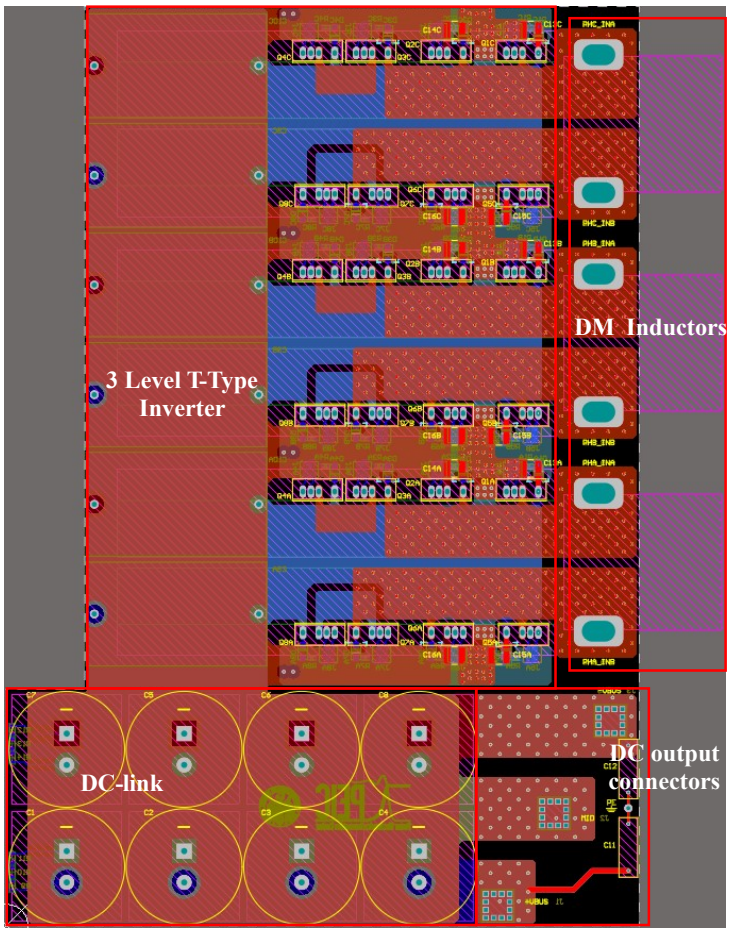

Figure 2.53: Power PCB 2D Layout.

A general rule for the polygon design and the tracks' routing is that sharp edges must be avoided and therefore, bevels in the polygons' corners are created. This reduces the noise in signals and EMI radiation.

Starting from the board layout and the components' placing, it can be underlined that the edge of the board is designed in order to reduce the space occupied for the mechanical coupling with the other boards. In fact, under the PCB, three drivers boards, one per phase, will be arranged. In the small compartment on the left, above the DC-link capacitors, the fans for cooling will be inserted. On the righ side, instead, the DM inductors will be mechanically mounted creating the coupling with the Power input board.

Downstream the differential mode inductors, each phase of the inverter is splitted up in two legs in parallel. The legs of one phase are mirrored respect the central horizontal axis of symmetry and the four switches of one leg are mounted on a 140 mm long heatsink as shown in Fig.2.54. The two ceramic capacitors needed to cut the switching loop are placed near the upper side switch drain pin and the lower side switch source pin. All those power devices are arranged on the top layer. The mate connectors carrying the gate commands from the driver boards and the desaturation resistors and diodes are arranged on the bottom layer.
Hence, the AC input is replicated in two polygons on the Top Layer and Mid Layer 1. Instead, the DC-link electrolytic and film capacitors are connected to the three phases with extended polygons, divided as follows:

- +VBUS: Bottom Layer;
- MID: Mid Layer 1;
- -VBUS: Top Layer.

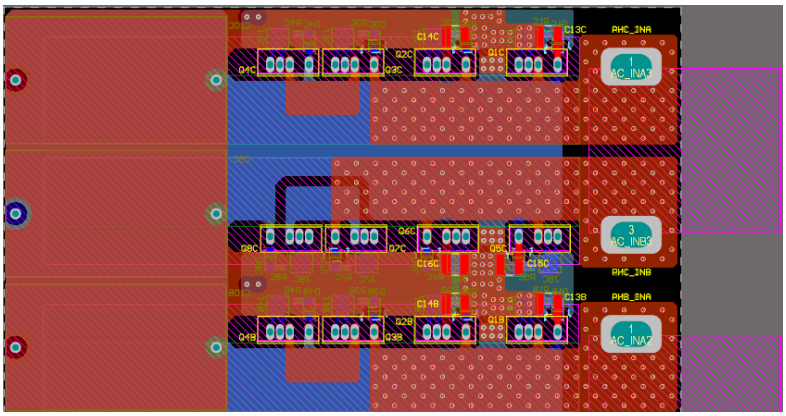

Figure 2.54: Inverter's phase detail.

The electrical isolation between the input voltages is set by rule as 2.6 mm and between the pins of the MOSFET as 1.5 mm. The signal tracks clearance is imposed as usual as 0.2 mm.

The AC incoming polygons have vias which make the stitching in order to better balance the potential inside the conductive area and provide multiple routes where the input current can flow, improving the thermal conduction and reducing the possibility of hotpots. Moreover polygon cutouts are added in the Mid Layer 2 over the drain of each MOSFET. This is a solution needed to shield the switching pin and its nearest path to the diode from superimposed disturbances that can be induced by an adjacent copper polygon which is at a different potential and is part of the switching loop. The local power connections of the pins of the four switches to the DC-link potential is splitted in a second layer in order to increase the conduction path and improve the reliability related to thermal dissipation.

Fig.2.55 shows the overlook of two legs of different phases linked to the same DC voltages. This is due to the optimization of the tracks and the spaces, exploiting the fact that the two legs can share the same power polygons that are connected to the related DC-link film capacitors.

The layout chosen for the power devices of the board has been necessary because of the placing of the capacitors near the transistors to reduce the effects of the switching and because of the position of the connectors towards the driver board, along with the heatsink size, which fixes the positioning of the components and the geometric dimensions of the board itself.

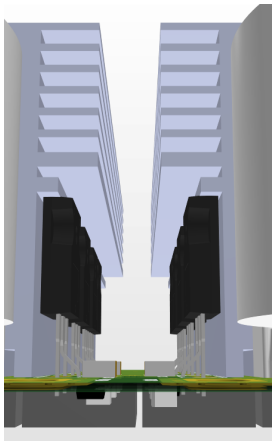

Figure 2.55: Mirrored legs of two phases.

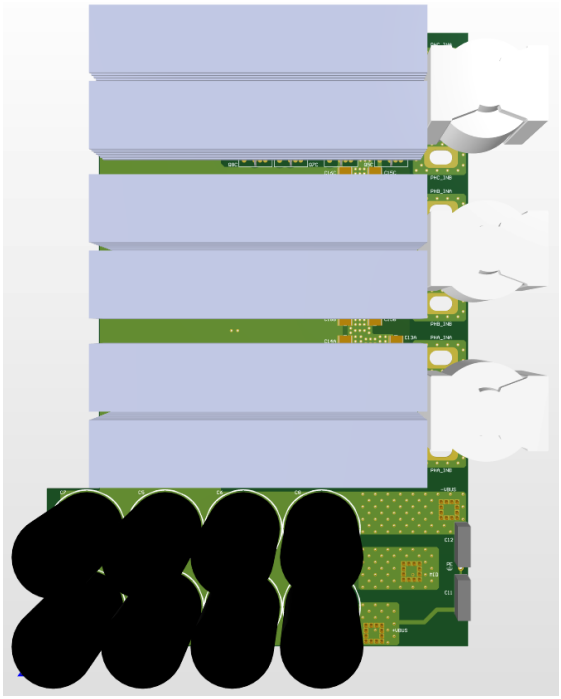

Figure 2.56: Power Input PCB 3D Layout (top layer).

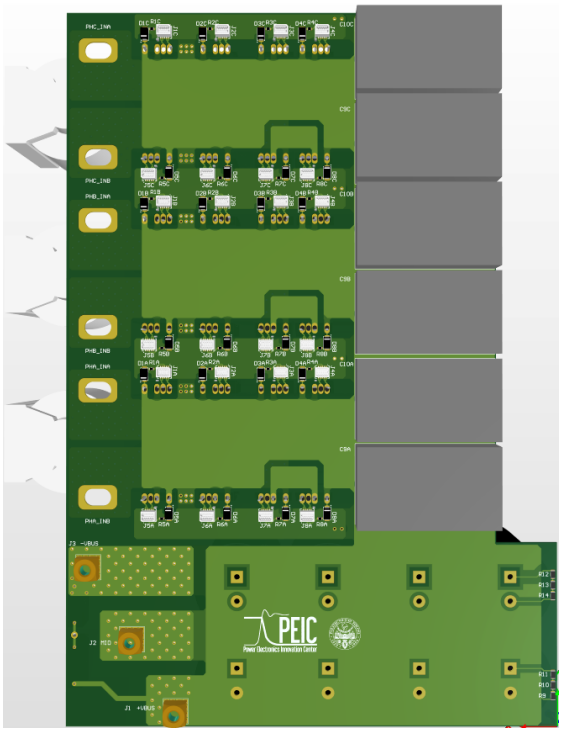

Figure 2.57: Power Input PCB 3D Layout (bottom layer).

2.3.3 Driver PCB

The Driver board is the module of the AFE representing the drivers of the two parallel legs of one phase, as it can be seen in Fig.2.58, Fig.2.59 and Fig.2.60. The board is repeated three times in the Multiboard project, because it is necessary to drive the switches of the three phase inverter. Moreover, each board has a size of 99x68 mm and has been realized with the usual 4 layers:

- Top Layer (red);
- Mid Layer 1 (brown);
- Mid Layer 2 (light blue);
- Bottom Layer (blue).

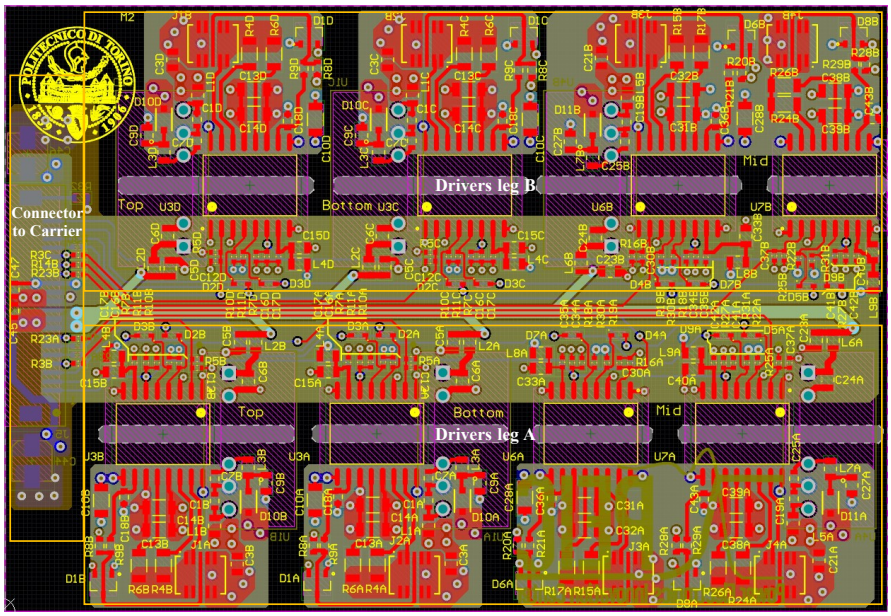

Figure 2.58: Driver PCB 2D Layout.

As can be noticed in Fig.2.58 the drivers of the two legs have a similar layout but mirrored respect to the horizontal axis. The upper and lower switches' drivers have an isolated supply, while the mid-point switches' drivers share the same power supply, as represented by the copper regions in the board. Instead, in the central part of the PCB a non isolated region is arranged, where the drivers' power supply of 15 V is conduced through a track with a width of 1.5 mm in the Mid Layer 2, which divides the board itself in two parts. The Top and Bottom layers are used in the central part to route the 0.3 mm thick signal traces between the drivers and

the connector towards the Carrier board (arranged with the bypass electrolytic capacitors on the bottom side of the board), where for the signals a minimum clearance of 0.2 mm has been set. In this part, the capacitors and resistors used for incoming and outgoing signals of the non isolated side of the driver are chosen with imperial size 0402, because of the reduced space, while the other components needed for the power supply and for the isolated areas are sized 0603. Moreover, the internal layers of the central region of the board are used for the ground and the 3.3 V voltages.

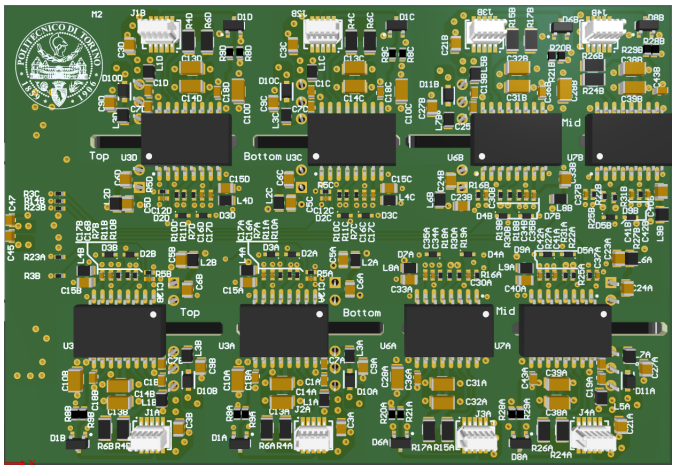

Figure 2.59: Driver PCB 3D Layout (top layer).

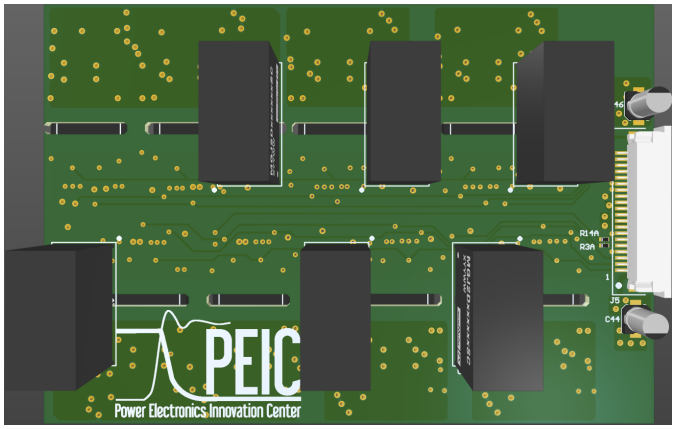

Figure 2.60: Driver PCB 3D Layout (bottom layer).

The isolated voltage regions on the output side of each driver are managed through copper polygons in the three layers available, excluding the Top Layer, which has been reserved to the components' placing and signal tracks:

- Mid Layer 1 polygon: 15 V isolated;

- Mid Layer 2 polygon: source pin isolated potential;
- Bottom Layer polygon: -4 V isolated.

The SMD connectors used to carry the gate signals to the switches, are positioned with very precise geometric measurements, which are defined by the mates of the Power board. In addition, cutouts of the board are needed to mechanically enforce the isolation of each driver.

2.3.4 Measures PCB

The Measures board is the module of the Active Front End containing the circuitry through which the three phase voltages are measured and managed, the DC-link voltage is detected and converted to digital signal and where the current analog conditioning, sampling and conversion to digital is performed, as presented in Fig.2.61 and in the 3D views Fig.2.62 and Fig.2.63. The board has a rectangular shape of 165x60 mm and has been realized with 4 layers.

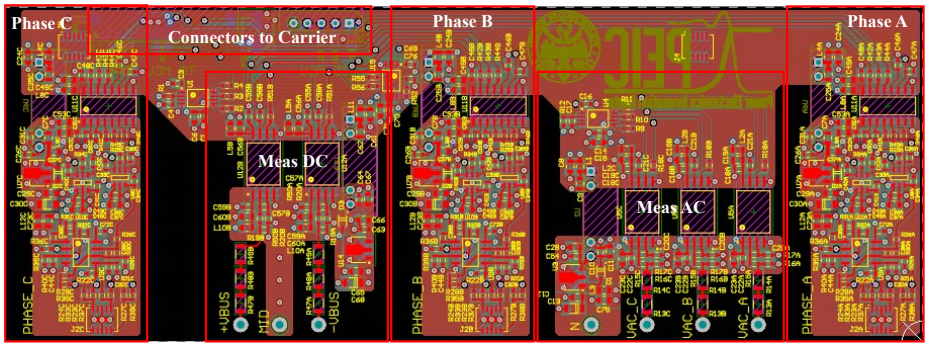

Figure 2.61: Measures PCB 2D Layout.

The board is organized with the isolated part of each measure on one side, while the non isolated part is managed with polygons and with the grouping of signals that are placed at a distance of 0.2 mm from each other, to create signal buses. This region of the board is the digital one, with the 3.3 V supply, a shared ground and the signals carried to the two connectors that make the communication towards the Carrier board and then the MCU. The signals are arranged mainly near the outer border of the PCB, in order to not cut the polygons.
The clock buffers can be noted easily because show identical placing and they are placed far enough away from the signal paths to avoid possible undesired couplings that generate interference.
The availability of 4 layers makes possible the division of the non isolated region with copper areas that distribute the power supply and the ground so as to reduce the return path of the signals, through the use of vias close to the grounded pins.

- Top Layer: Signals and digital ground (GND);
- Mid Layer 1: GND;
- Mid Layer 2: Power supply 3.3 V;
- Bottom Layer: Signals and GND.

The ground polygons arranged on the Top and Bottom layers are used to create a shielding of the board. In this way the board is ore immune to external disturbances and reduces the irradiated noise.

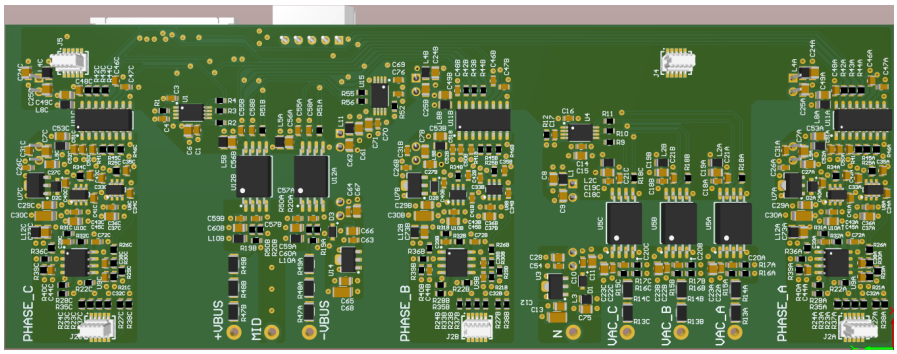

Figure 2.62: Measures PCB 3D Layout (top layer).

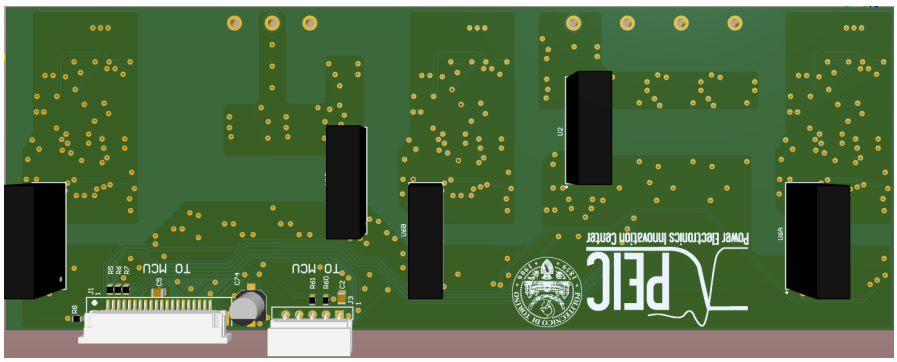

Figure 2.63: Measures PCB 3D Layout (bottom layer).

The isolated parts of the board, which are specific for each measure, have common features. In facts, the devices are arranged so to be compact and the filtering resistors and capacitors are placed near the pins of the integrated circuits and connector. Besides, extended polygons are created so to generate islands which are referred to different grounds:

- for the current is the common mode point where the phase is split up in two legs;

- for the phase voltages is the neutral point;
- for the DC-link voltage is the mid-point.

Dealing with a three-phase system, the measurement circuits can be repeated multiple times for each phase. In this case, a single current measurement circuit shown in Fig.2.64 and the AC voltage circuit of Fig.2.65 will be analysed in detail. The other channels (phases B and C) are an exact copy.

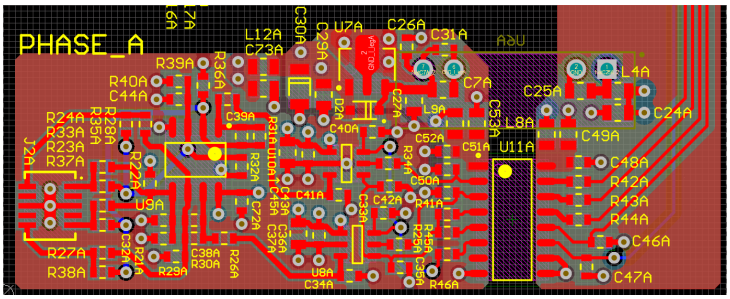

Figure 2.64: Current measure detail.

The components are arranged as usual on the Top Layer, but for spacing reasons the isolated DC/DC power supply devices are positioned on the bottom layer, by exploiting the fact that they have through hole pins. The polygons are drawn by incorporating all components and remaining at the pin level, so as to guarantee the insulation given by digital isolators and ADC sigma delta. Moreover, analog signals are routed with 0.5 mm thick traces, while the digital signals have a signal width of 0.3 mm.

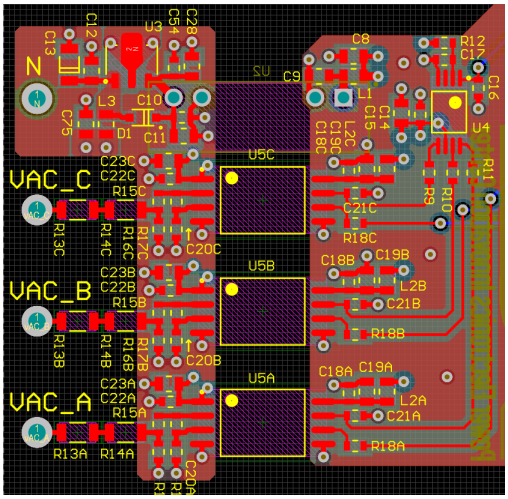

Figure 2.65: Phase voltage measures.

Another important point in the Measures board is the isolation between the adjacent blocks containing the measures and also the isolation inside the voltage measures. In fact additional constraints related to the clearance have been fixed, with a minimum isolation between the blocks of 4.5 mm and minimum clearance between the of the AC phase voltages and also the DC voltage levels of 3 mm.

2.3.5 Carrier PCB

The Carrier board is the part of the Active Front End that contains the low voltage DC power supply system for all the electronic devices, the communication circuitry, the relays driving circuit, the debug connectors and the three central connectors which communicate with the MCU board. These elements are managed in specific regions of the board, according to the zoning guideline, so as to have a well organized division of the board in order to reduce disturbances, as is underlined in the 2D view of the board in Fig.2.66, while the the 3D view is presented in Fig.2.67. As can be noticed, the board shows a rectangular shape of 120x101 mm and has been realized with 6 layers. This choice has been necessary because of the very large number of signal tracks running through the board and ranging from the three central connectors, which communicate with the MCU board, to the connectors arranged at the outer edges of the board, which interface with the other PCBs.

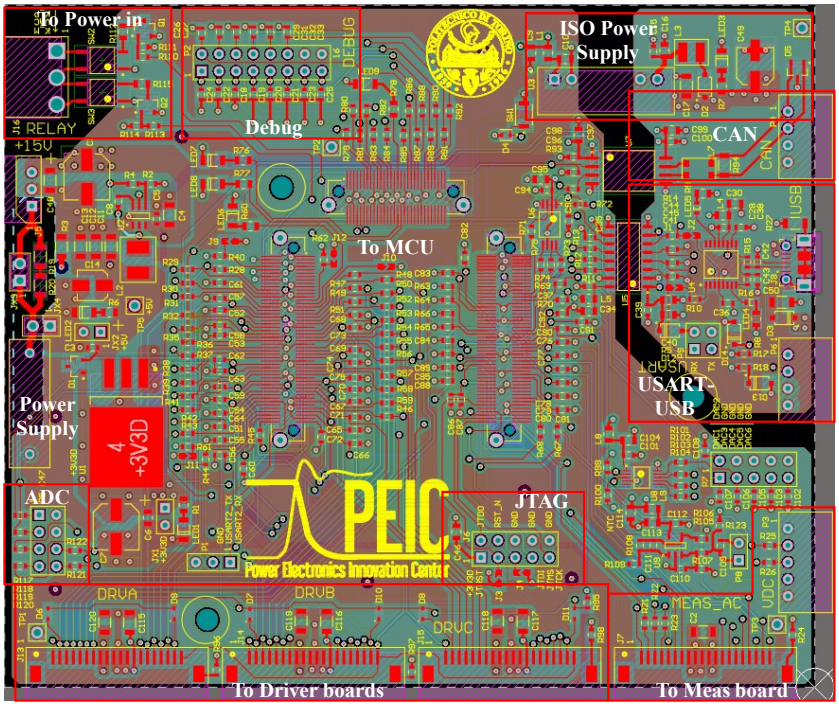

Figure 2.66: Carrier PCB 2D Layout.

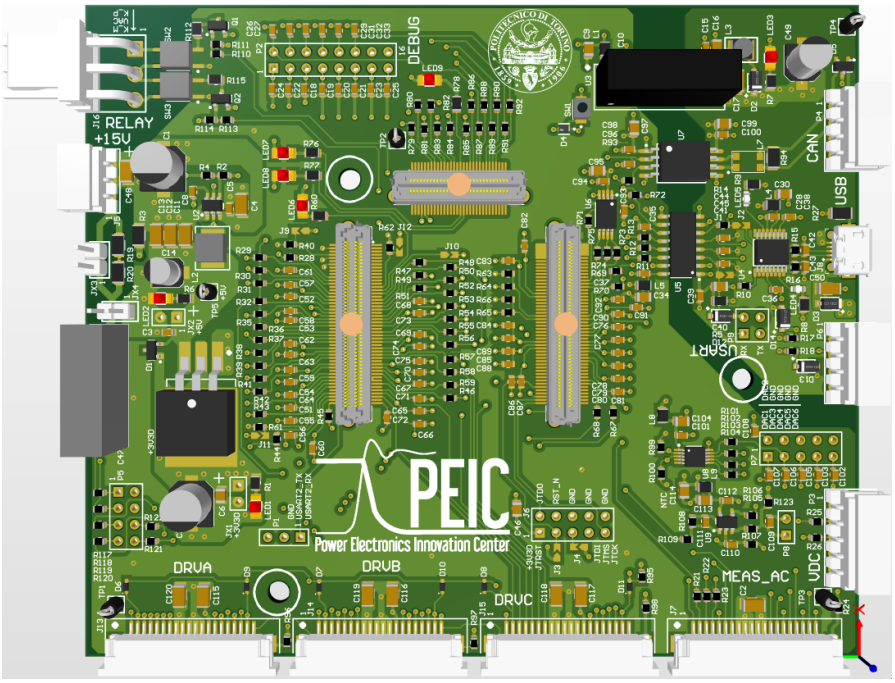

Figure 2.67: Carrier PCB 3D Layout (top side).

The layers are managed both with copper polygons that distribute the power supply and the signal ground. They are also used to carry the signals in an organized way across the board. In particular, the layers are managed as follows:

- Top Layer (red): it is the layer where all the components are arranged. In this layer it is inserted the ground which makes the shielding of the board and also some polygons at 15 V and 5 V in order to distribute the voltage and make the region more equipotential (with the adoption of vias as stitching);
- Layer 1 (light blue): this layer is used mainly for distributing the digital system's power supply at 3.3 V. The layer is free of signal paths so as to keep one power supply plane immune to the noise and using it as an internal screen between the layers also used for signals;
- Mid-Layer 1 (brown): layer managed both for the signals and the GND plane;
- Mid-Layer 2 (green): this layer has been used for some digital signals but mainly for the power supply. In fact, a 15 V plane has been designed in the outer area on the left of the board, having a horseshoe shape, in order to carry this supply both to the non isolated part of the DC/DC converter of the island (on the right of the board), but also to the three connectors which make the coupling with the Driver boards. In the central part of this layer another 3.3 V plane han been sized;

- Layer 2 (purple): this layer has been reserved for a plane that distributes the GND and as well as the Layer 1 is signal free;
- Bottom Layer (blue): in this layer another ground plane which is shielded has been set and it has been also used for the tracks.

Besides, as can be seen from the previous views of the board, there is an island which is electrically isolated from the other part of the board. This is necessary for the communication systems, which are CAN, USART and USB. The circuitry that manages these protocols has to be carefully separated from the external power supply, ground and signals, because the communications have to be immune from any digital noise and also for safety reasons according to the electrical protection of the external devices connected. Therefore, a physical division is needed and can be detected through the pins on the primary and secondary sides of both the isolated power supply device and the integrated circuits, that guarantee the digital isolation. In this area, copper polygon have been set, distributing the power supply to all the components. Two layers are used for the 5 V isolated, while the other four have been adopted for the isolated ground planes.

The power supply of this board is carried with a +15 V system, through an horizontal connector, as can be seen in the 3D view on the left of Fig.2.67. That area of the board is reserved for the power supply circuitry. In fact, starting from the 15 V voltage, the other voltage levels are obtained. Firstly, the 5 V is regulated through a DC/DC buck switching converter and filtered with bypassing capacitors and through a LC low-pass filter. Then, a linear DC/DC converter gives the 3.3 V level, which is stabilized with capacitors. A similar layout has been designed for the isolated converter which makes the 5 V isolated in the upper right corner of Fig.2.67. The placing and the routing of the DC/DC buck converter circuit had to be made carefully. Indeed, the datasheet of the converter adopted [19] (i.e. TPS565208) provides useful guidelines for the system, as can be noticed in Fig.2.68. Moreover, the datasheet lists also the following suggestions:

- VIN and GND traces should be as wide as possible to reduce track impedance. The wide areas are also of advantage from the view point of heat dissipation;
- The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance;
- Sufficient vias for the input and output capacitors must be ensured;
- The switching trace must be sized physically short and wide to minimize radiated emissions;
- The switching path should not pass under the device;

- A separated VOUT path should be connected to the upper feedback resistor;
- A Kelvin connection to the GND pin for the feedback path is recommended;
- The voltage feedback loop should be placed away from the high-voltage switching trace and ground shielded, in order to be immune from disturbances;
- The GND track between the output capacitor and the GND pin should be as wide as possible to minimize the impedance.

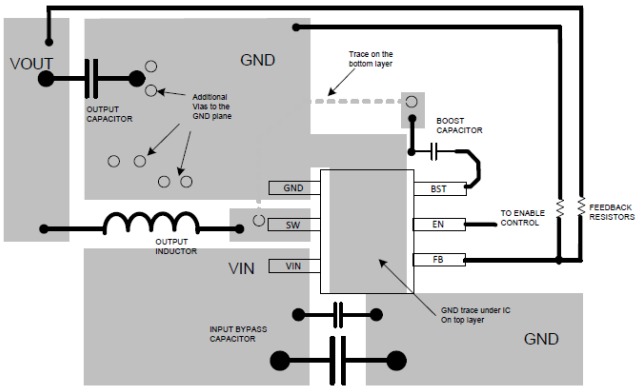

Figure 2.68: DC/DC converter layout example.

The listed guidelines have been adopted in the design so to avoid problems with the switching circuit and guarantee as much as possible a power supply immune from the noise. The detail of the board where the 5 V system has been designed is reported in Fig.2.69.

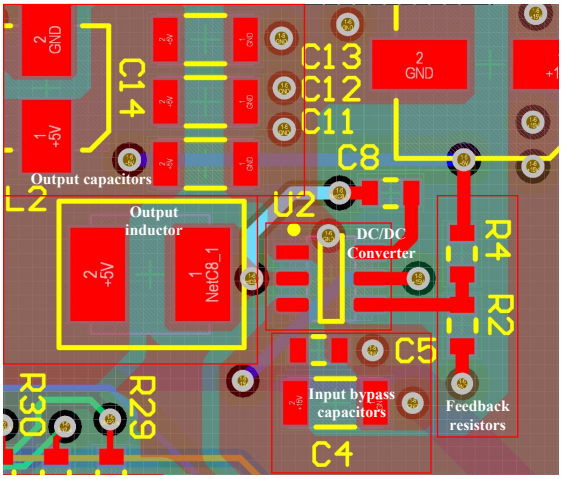

Figure 2.69: 5 V supply system.

The large number of pins both of the connectors and ICs used for the digital signals, has made the PCB design more difficult because it has been necessary to follow the guidelines for avoiding disturbances between the signals. Therefore, the capacitors and the resistors are arranged near the pins of the connectors, headers and ICs, in order to better filter the signals. Vias are used to reduce the return paths through the ground planes. While the signals are managed with a width of 0.25 mm and a minimum clearance of 0.2 mm. Moreover the tracks are collected and sorted, generating bus channels. This was useful when it has been necessary to cross the tracks passing in two adjacent layers, so to avoid the cross coupling effect. Instead, the layers reserved for the power supply plane and the ground has been used as shields for the EMI.

The last part of the board that has to be analyzed is the one with the driving circuits for the PTC precharge relays, discussed in the paragraph with the Power in board description. This region of the PCB has been well isolated from the other parts, because the mains potential is conduced through the connector. In fact, as shown in Fig.2.66, the switches that regulate the precharge operations, have a large footprint, with well spaced pins to ensure insulation. On the other side, instead, which is not isolated, the components are arranged as usual and the power supply and the GND are carried by the copper planes.

2.3.6 MCU PCB

The MCU board is the "brain" of the Active Front End because contains the microcontroller unit. The only additional elements are the three connectors (which are the mates of the ones mounted on the Carrier board) and bypass capacitors for the power supply pins and the signal clock pins. In Fig.2.70 is shown the 2D view of the board provided by the editor, while in Fig.2.71 and in Fig.2.72 the two sides mirrored of the 3D view are presented. As can be noticed, the board shows a rectangular shape with very small sizes of 48x55 mm. As said for the Carrier board, also in this case, even if the components are few, the very large number of pins to be connected between the connectors and the pins of the MCU makes necessary the use of 6 layers.

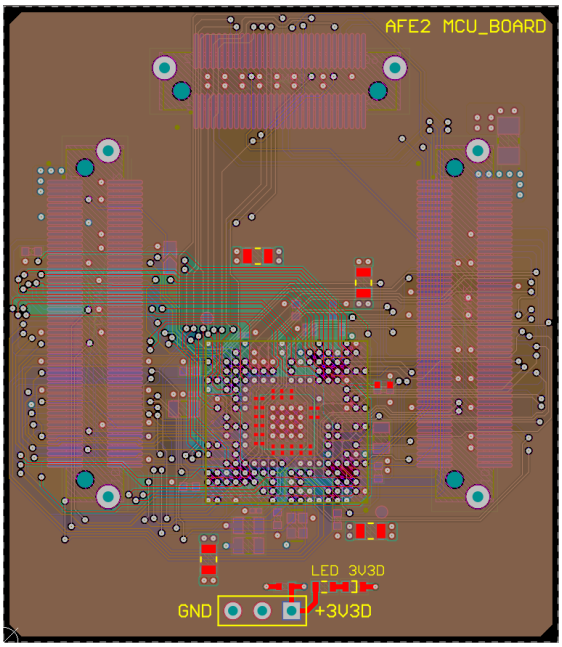

Figure 2.70: MCU board 2D view.

According to the number of signals that travel through the board, almost all the layers have been used to carry some signals. In fact, the free region of each layer has been reserved to an extended copper plane, designed as a bevelled polygon, which is needed to expand the power supply and the signal ground all over the board. As usual those planes have been used also for shielding the signals between non adjacent layers. Three layers have been allocated to the 3.3V supply voltage, while the others, which have been interspersed with the first, are at GND.
The power connections have been made mainly through vias connected to the polygons, while the tracks have been used to connect the signal pins. In fact, the

electrical isolation has been fixed with two main rules. The clearance between signals and polygons is 0.3 mm, while the minimum clearance between signals is 0.1 mm, because the signals' width has been imposed to 0.1 mm.

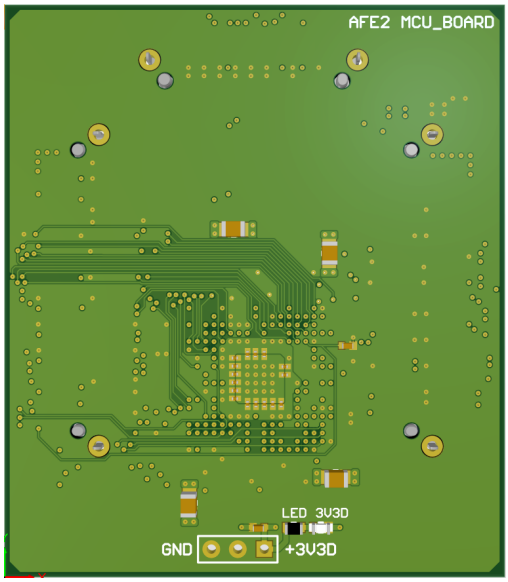

Figure 2.71: MCU PCB 3D Layout (top side).

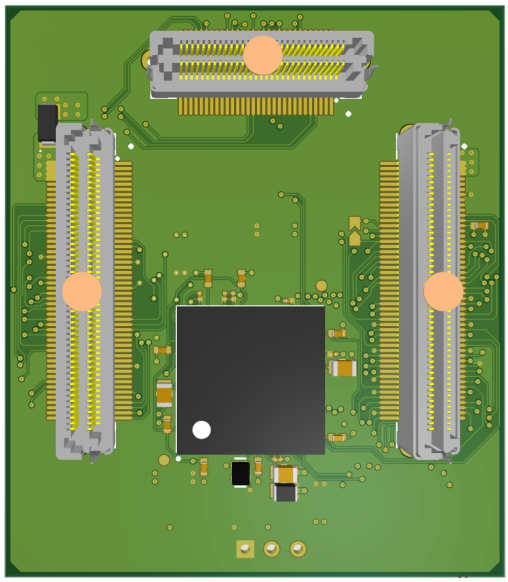

Figure 2.72: MCU PCB 3D Layout (bottom side).

As can be seen in Fig2.71, the board can be supplied with wires connected

to a three positions' header. This is useful when the MCU has to be tested and debbuged and it is not connected to the Carrier board.

The most critical point of the MCU board has been related to the routing. In fact, the microcontroller selected is characterized by a BGA package, which requires particular attention both from the point of view of the routing of the tracks and the management of the signals and layers, with specific measures to be respected to and sizing of the vias.

The management of a BGA component must respect some important guidelines, suggested by Xilinx in its technical report "Recommended Design Rules and Strategies for BGA Devices" [20] and summarized as follows:

- The first recommendation is related to the BGA landing pads, which should be designed as Non-Solder Mask Defined (NSMD) copper pads. This meas that the pads are not covered by any solder mask, while on the opposite, the commonly used pads for the other components are Solder Mask Defined, with a small amount of solder mask covering the pad itself. The solder mask is a thin polymeric layer applied over the outer layers of the board for mechanical and chemical protection.
- Routing channels are the number of available routing paths out of the BGA area. These have been managed by an Altium Designer function, called "Fanout", which automatically creates internal escaping vias at the center of the BGA internal pads, while the two outer rows are routed until the board of the component. Hence, the routing of the tracks can be organized collecting as much as possible the signals, exploiting the available layers.
- The amount of space available for routing under the BGA component is dependent on the area between the balls in the BGA area (for top and bottom layers), as well as the area between vias (for inner layers). The typical dimensions of the ball pads and vias for 0.8 mm pitch is shown in Fig.2.73.
- The ball pitch and both the pads and vias diameters determine how much space is available to route traces between pads or vias. Therefore, for 0.8 mm pitch components, only one track can be routed between the vias, according to the drill-to-copper requirements, as underlined in Fig.2.74.
- Additional suggestions for the design of a BGA component are:
  - Track to track isolation gap (i.e. electrical clearance) is 0.1 mm;
  - Track to pad isolation gap is again 0.1 mm;
  - Track width is fixed as 0.1 mm.

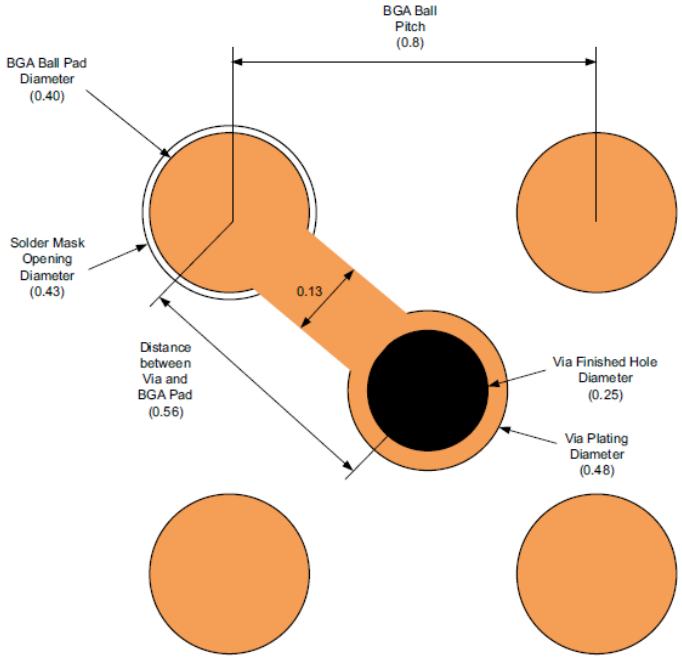

Figure 2.73: Ball and via dimensions for 0.8 mm pitch.

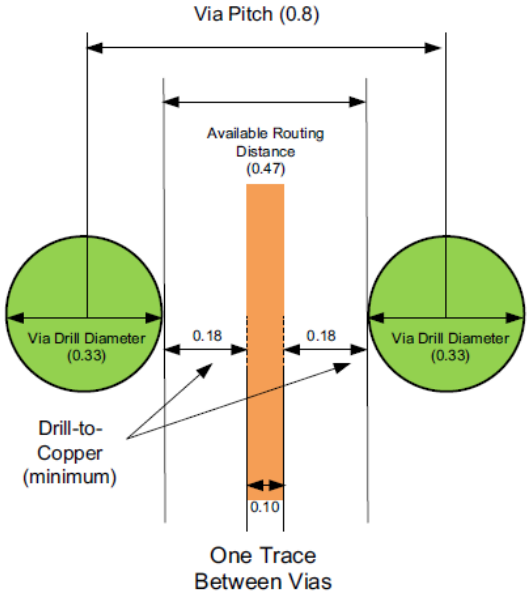

Figure 2.74: Track routing between vias for 0.8 mm pitch devices.

- The escaping vias have to be designed not with a fixed pad size through the layers, but with a variable one, in particular for the inner layers. In fact the via holes have a diameter chosen to be 0.15 mm, while the pad diameters are different:
  - Outer layers pad size of 0.45 mm for a 0.15 mm finished hole size;
  - Inner layers pad size of 0.5 mm for a 0.15mm finished hole size.

These guidelines have been applied in the MCU board design and Fig.2.75 shows the results. The MCU has been placed on the bottom layer, as well as the main signals' bypass capacitors, while the capacitors needed by the power supply pins, which are arranged in the inner rows of the device, have been positioned in the top layer. In this way they can stabilize the supply voltage of the MCU and can be as near as possible to the related pins.

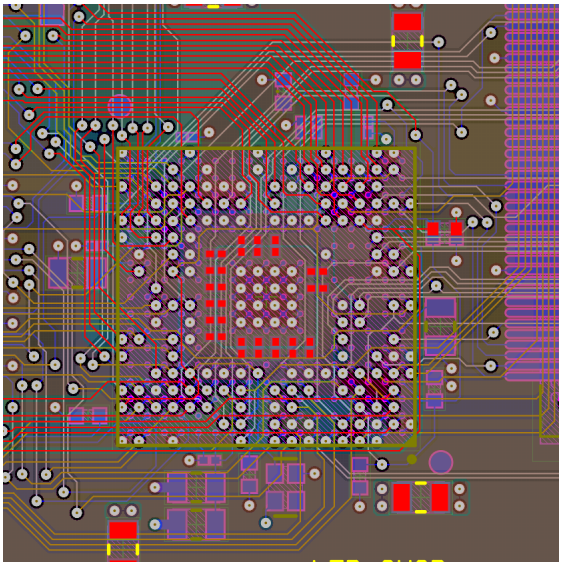

Figure 2.75: BGA and signals management.

The signals are arranged as data buses, in order to reduce the space occupied for the connections to the connectors' pins. The guidelines to avoid EMI problems have been applied, with particular focus on the correct crossing of the traces arranged in adjacent layers. Moreover, as can be noticed in the bottom of the image, a four pads component is placed near the MCU but the signals of the nearest layers are kept away. This is due to the fact that it is needed to avoid irradiated disturbances that can be generated by this external oscillator.

Once that the PCB design is finished, it is necessary to run the Design Rule Check function available in the Altium Designer editor. This tool checks that all the rules are respected, providing a list of possible errors and a graphical output to easily correct any problems. In addition, the mechanical tightness of the PCBs must be checked and the mechanical assembly of the boards must be designed.

The list of all components needed for each PCB is then created, with the grouping of devices of the same type. In fact, an Excel file for each PCB has been added to the project, that lists the components and all their main features. This will be used as a guide for the correct selection and mounting of the devices on each board. After that, each bill of material is merged in a unified one for the entire prototype. From that, the components of the MCU, Carrier and Driver boards are excluded because these PCBs have been chosen to be externally manufactured, because of their complexity and the importance of the precision in the soldering. The other listed components have been selected from distributors such as RS, DIGI-KEY and MOUSER. Therefore, the BOM has been completed with the codes of both producers and distributors. Then a shop chart has been sent to each distributor and the tasks of construction and testing of the boards can be carried out.

In this chapter the hardware design has been analyzed, starting from the drawing of the schematic of each sub-module, the choice of the main components, until the creation of the PCBs. The prototype of the AFE has been designed with overall reduced dimensions, because the initial choice, which has been respected, was insert the converter and all the control boards inside a mobile rack. This solution ensures simplicity of transport and installation, but above all high power managed with a high-tech device that is also small in size. Therefore, as a conclusion of this chapter, a 3D rendering of the entire project can be seen in Fig.2.76, which has been provided by the PEIC team (made with SolidWorks). The image shows all the parts of the prototype, which is contained in a rack having a size of 423x333x83 mm.

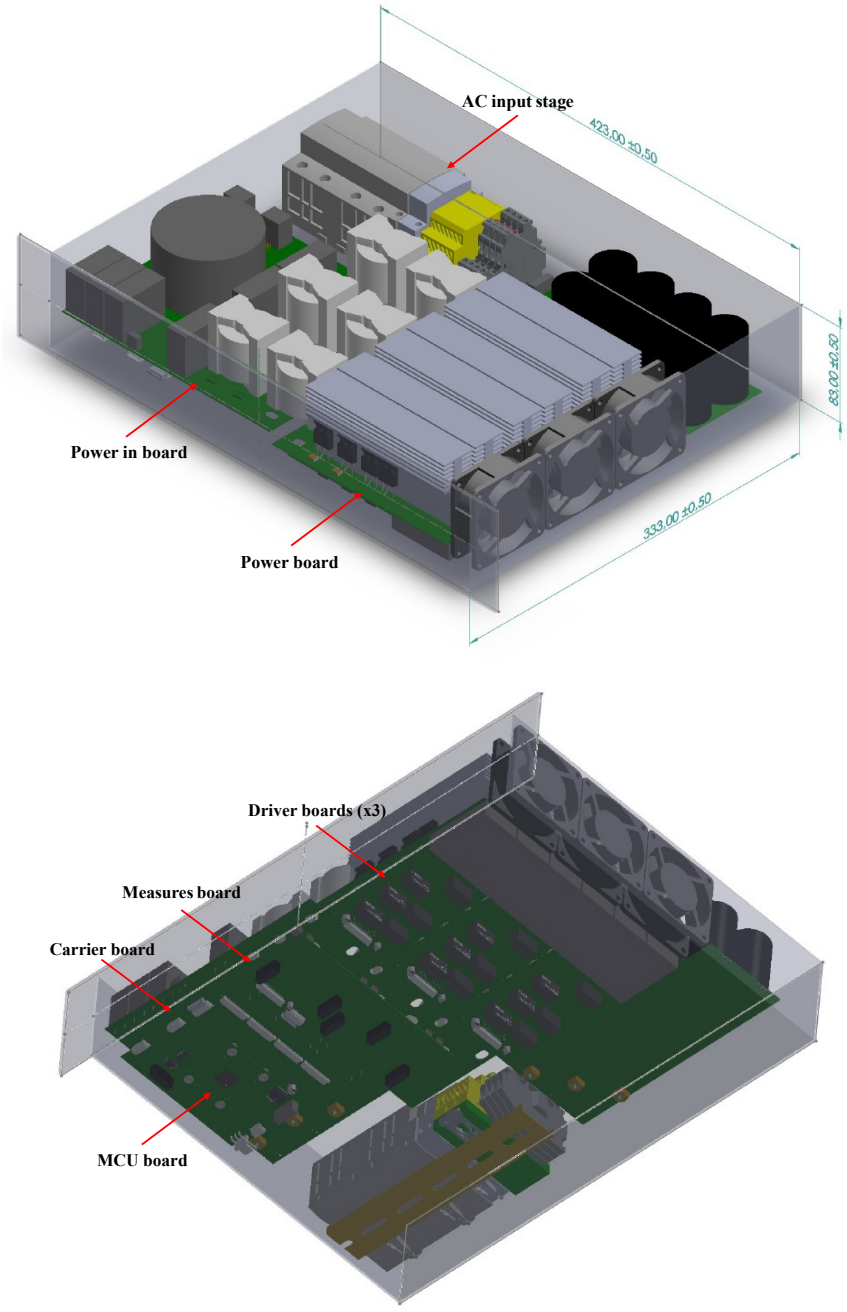

Figure 2.76: Active Front End 3D rendering

Chapter 3

Preliminary Testing and Assembly of the Converter

In this chapter, the last steps of the thesis work will be described. In particular, the main activities carried out in laboratory are the following:

- Shipment management, with checking and arranging of the components of the prototypes (with the help of the order list and the AFE BOM);
- Assembly of the PCBs, soldering of the components and wiring of the cables;
- Test bench setup and testing of the main functionalities of the signal boards.

These tasks have been executed in part with the other members of the PEIC team, in particular with the the graduating student who was responsible for writing the MCU firmware and designing the communication part. In laboratory, my main responsibility was to manage the hardware, i.e. the management of the boards, the components and the setup to proceed with the tests. However, I was supported in the component selection phase for the various boards of the AFE but also in other projects (having to check the distributor codes and the BOM) and also in the soldering phase of some power components.

The activities have been slowed down by delays in shipments, due to problems related to the pandemic and the difficulty for distributors to find some material. In fact some PCBs, in particular the Power Input board, the Power board and the Measures board were not completely assembled and therefore could not be tested due to the lack of some components. Therefore the complete prototype will be completed in the days following the conclusion of this thesis.

3.1 Power Input and Power boards

The PCBs which manage the power part of the AFE have been manually assembled. In fact, starting from the Power Input board, the available components that have been soldered on the top side (Fig.3.1) are the PTCs used for realize the precharge circuit. The common mode chocke inductor and the common mode and differential mode inductors (i.e. also referred as longitudinal and transversal inductors) have been only arranged over the board in order to verify the distances and to have an idea of the spacing.

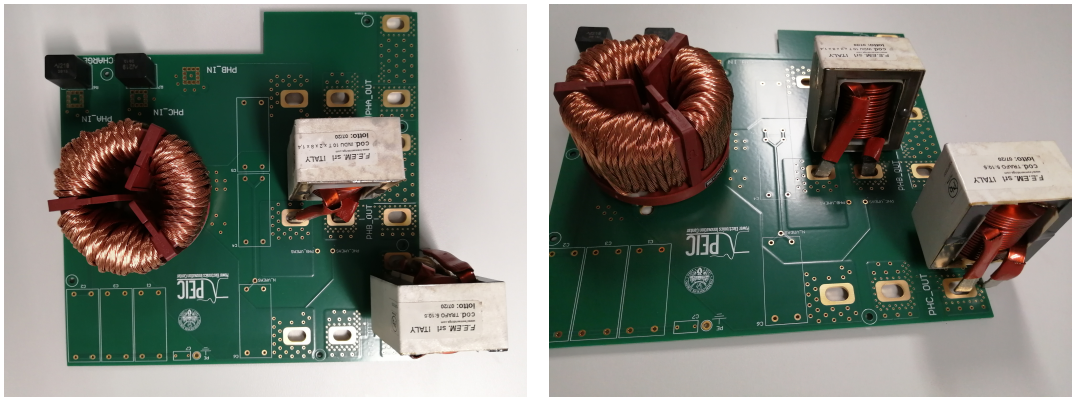

Figure 3.1: Views of the Power in PCB with the example of the inductors.

The shunt resistors have been mounted on the bottom side of the board, as can be noticed in Fig.3.2.

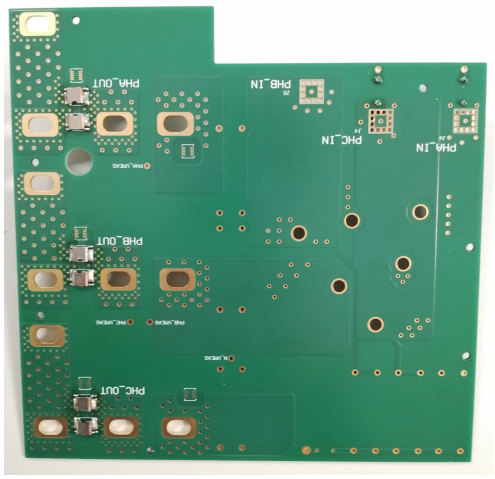

Figure 3.2: Bottom view of the Power Input board with the shunt resistors.

The Power board is reported in Fig.3.3. On the top side the DC-link electrolytic capacitors and the ceramic capacitors, with imperial size of 2220, which are necessary to reduce the switching path, have been soldered.
On the bottom surface have been mounted the diodes belonging to the power part of the desaturation circuit of each MOSFET and also the shank terminals that are the power output of the AFE.

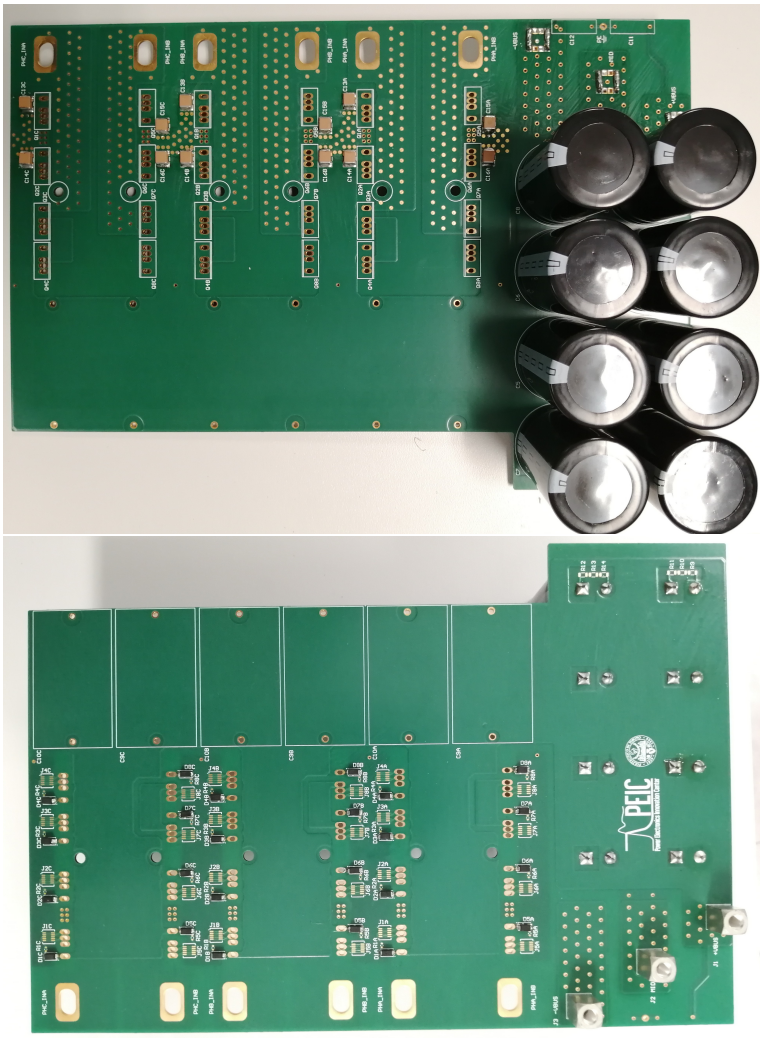

Figure 3.3: Power board top and bottom view with the components soldered.

The transistors and the heatsinks were available for the assembly, but because of the lack of the 0603 resistors of 1 kΩ and of the other film capacitors it has not been possible their arranging, because they must be the last components to be mounted and verified over the Power board.

3.2 Driver boards and Measures board

The Driver boards were made by the external manufacturer Eurocircuits, but the drivers ADUM4135BRWZ have been purchased by RS and have been manually soldered on the three PCBs shown in Fig.3.4.

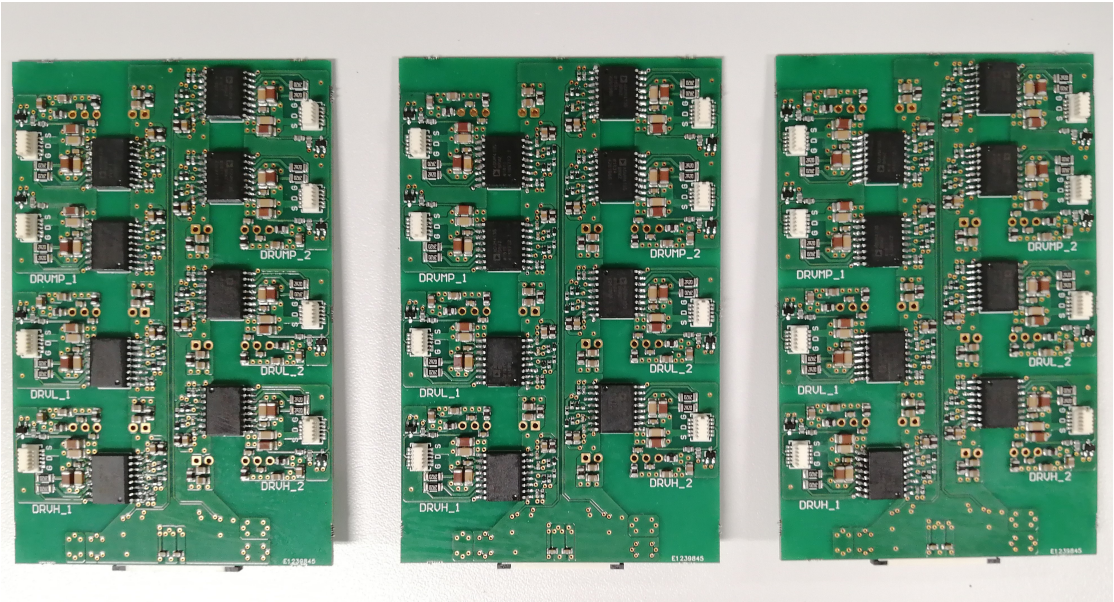

Figure 3.4: Driver boards for the three phases.

The 80% of the components necessary for assembly the Measures board were available in laboratory but the last shipments delayed. Hence, the PCB could not be finished because the components are SMDs and they must be soldered using a reflow oven.

3.3 Carrier and MCU boards

The Carrier board has been manufactured by Eurocircuits and the result is reported in Fig.3.5. The only component that have been manually soldered has been the UART-USB converter FT230XS-U with standardized package TSSOP16.

The MCU board has been made externally by Eurocircuit and the result is presented in Fig.3.6, where the bottom side of the PCB shows the MCU itself, the three connectors and the components such as the bypass capacitors and the external oscillator.

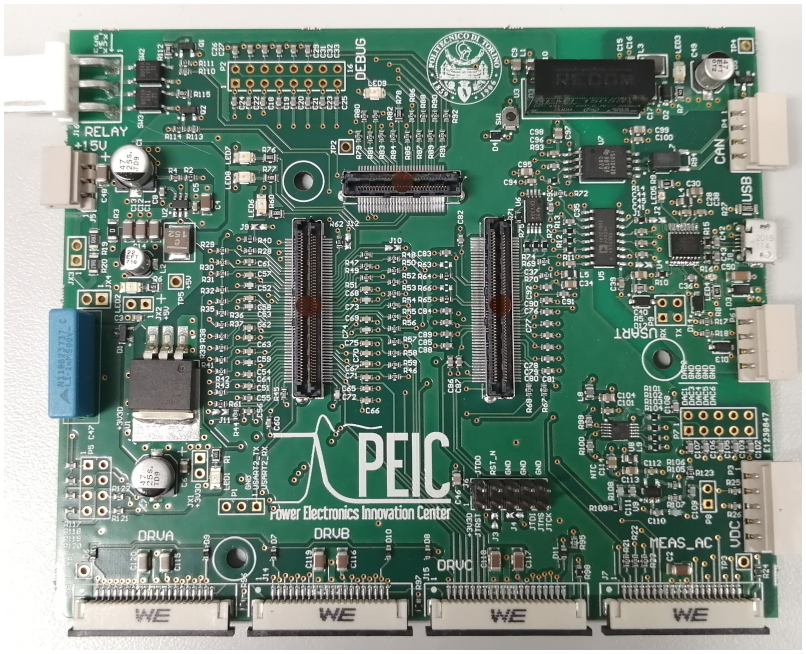

Figure 3.5: Carrier board PCB top view.

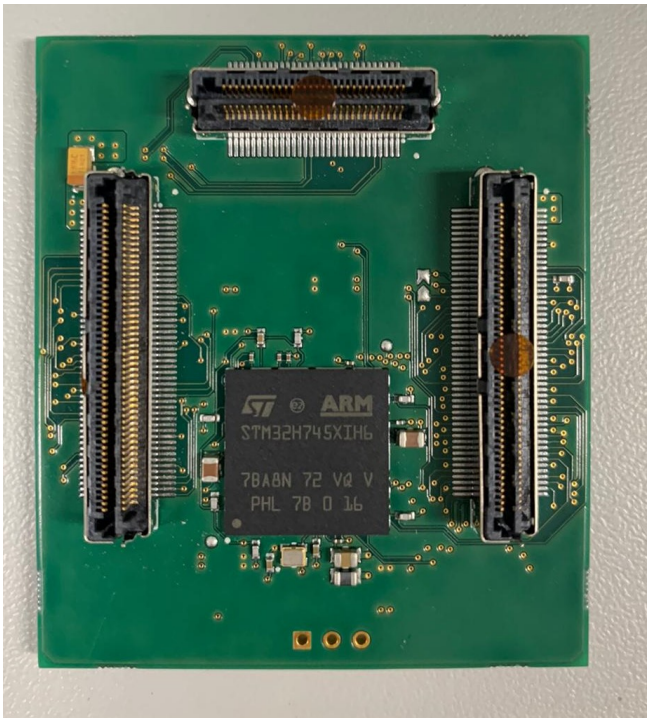

Figure 3.6: MCU board bottom view.

3.4 Preliminary testing

Once the Carrier board has been available, it has been supplied with the input voltage of 15 V and it has been verified that the power supply leds were on. The circuits that perform the DC/DC convertion, stepping down the input voltage to 5 V and 3.3 V are correctly working. Moreover, the initial configuration of the MCU has been successfully. In particular, the MCU communicated with the PC through the JTAG signals passing on wires that have been connected between the the header on the Carrier board (named J6) and the pins of the external ST-Link V.2, which makes the conversion USB-JTAG (Fig.3.7).

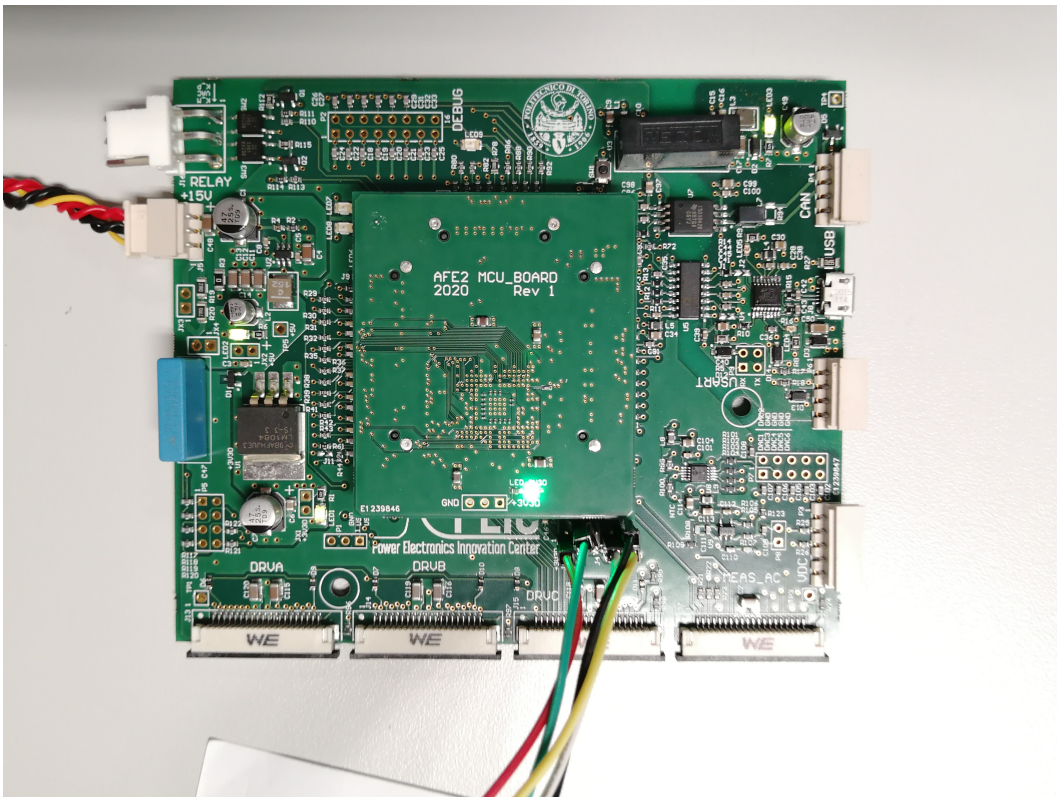

Figure 3.7: Carrier board power supply test and preliminar debugging.

Therefore, the test bench for the control system has been prepared. In fact, as can be noticed in Fig.3.8, the Carrier board has been connected to the three Driver boards through the FFC cables. Then the buttons which manage the fault signal and the start signal have been created, using wires that must be twisted and creating the correct terminations for the mate connector of the one mounted on the Carrier board. Moreover, the wires needed for the debugging system have been arranged forming a twisted cable with the terminals that can be connected with

the ST-Link and the 10 pins header on the Carrier board.

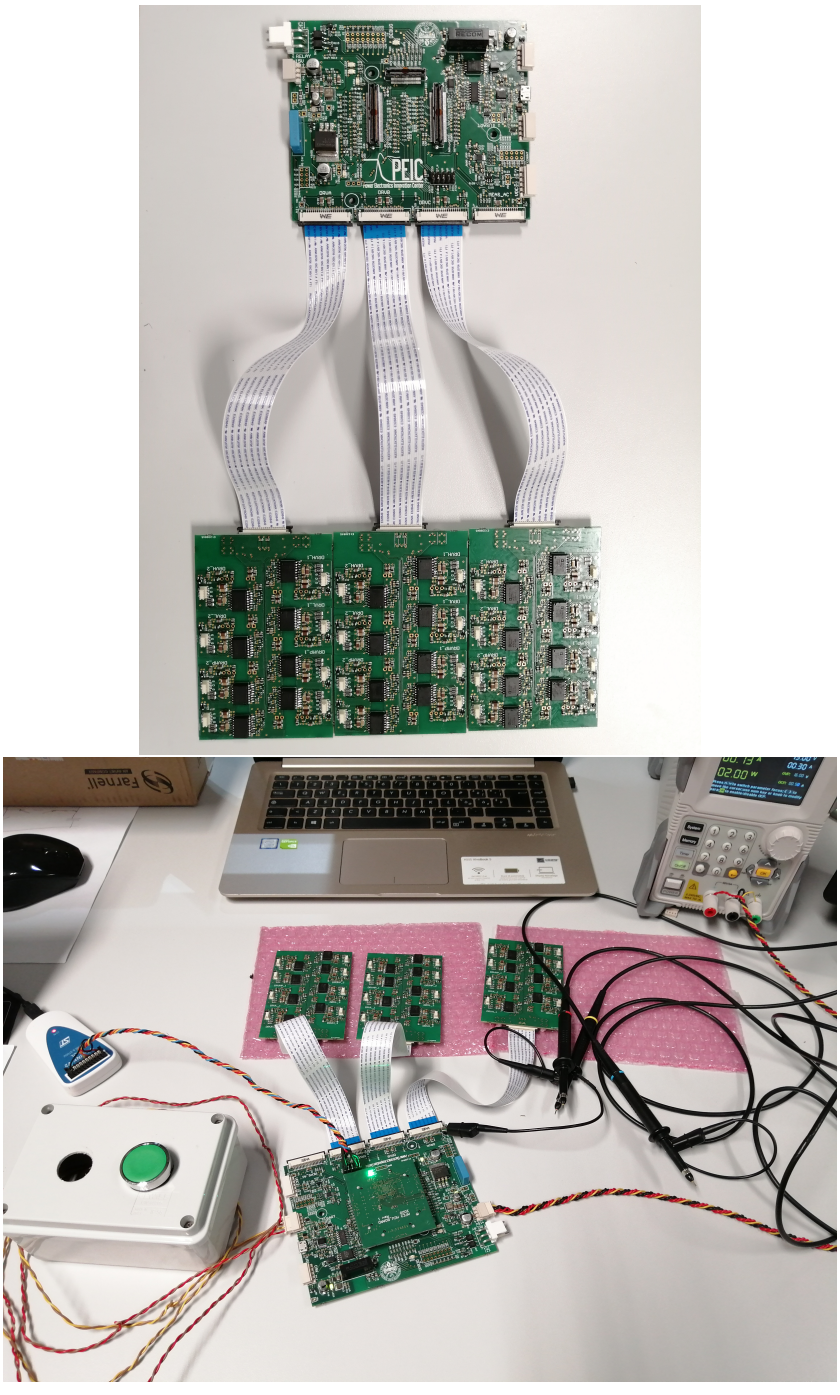

Figure 3.8: Test bench setup of control boards and drivers.

The wiring between the boards has been performed, the test points, connected to the GND, necessary for the oscilloscope probes have been soldered on the Carrier board and the test bench setup has been realized.

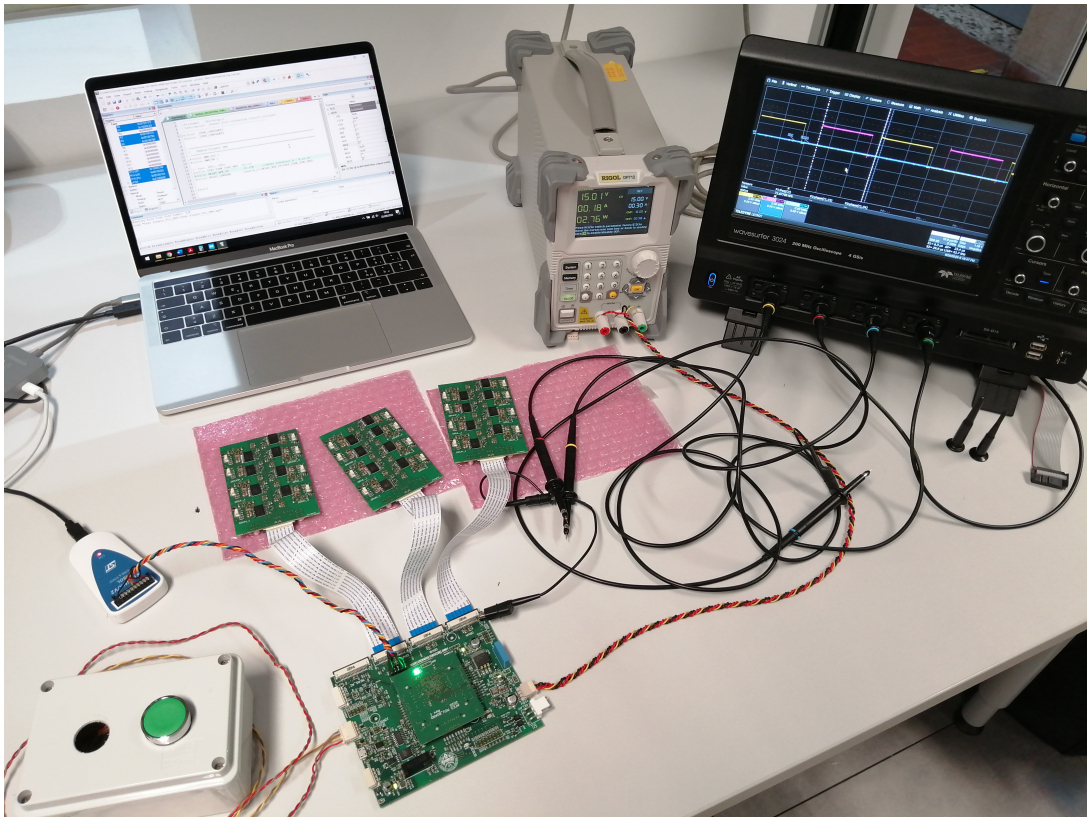

Figure 3.9: PWM signals and interleaving testing.

Therefore, since the debugging was available, the PWM signals (realized by the MCU), which are carried to the Driver boards, have been tested, by measuring the voltages of the signals on the primary pins of the drivers of each switch of every converter leg. What has been verified by the results of the tests is that the control system is completely working and the interleaving between the legs of each phase can be correctly obtained.

Chapter 4

Conclusions

This master thesis analyzed the schematic and PCB design process of the active rectifier for an ultra fast battery charger for electric vehicles. Ultrafast chargers, as mentioned in the Introduction, are and will increasingly be a key technology, being at the heart of the transportation electrification.
The hardware development of this prototype is a work carried out in sequential stages and requires transversal engineering skills, both electrical, electronic and mechanical. The master thesis has been an opportunity for both academic, professional and personal development.
In fact, my personal contributions and acquired knowledge were as follows:

- The theoretical study phase of the active rectifiers, the design of the schematic and PCBs, which allowed me to understand what the hardware design of power electronics devices is. I have acquired indispensable notions for the development of PCBs, both theoretical, technical and practical;
- The study of the specifications and the choice of the suitable components, analyzing the datasheets and the main features of each device implemented. Related to that I understood how it is often necessary to retouch already validated schematics, both to correct their functioning and to develop and implement new technologies. In addition, I started to have a critical eye on the choices and how to approach design issues;
- The compilation of the BOM with the support on the choice of components to buy from distributors, mediating both between a choice linked to costs and the need to have a defined number of certain components;
- The assembly of the main components to be soldered and tested.

I learned what an iterative process means, how was the work of this thesis, in which some hardware choices or implementations have been modified or completely

overturned, to obtain better results or implement different technologies. Hence this thesis, which presents the main results of my work, has served to start learning a job, which is the hardware engineer in all its aspects.

Moreover, no less important, the thesis work has been an opportunity for grow as a person. In fact, from the very first day, I got in touch with the members of the PEIC team, mainly with my supervisor Fabio and his colleague Stefano, who guided me in the technical development of the converters, teaching me their know-how. Therefore, to sum up my hard and soft skills learning outcomes from this thesis were:

- Approaching problems on my own, so in order to be independent in finding suitable solutions;
- I learned how the work should be approached and to develop the hardware design of a converter like the AFE;
- The regular meetings with the other team members, where there was a presentation of the work carried out by each one, has been formative as they were an opportunity for technical debate on the progress of the project and see how is the organization of a research and development team.

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