POLITECNICO DI TORINO

Master's Degree in Electronic Engineering

Master's Degree Thesis

Design of Flip-flops and Latches using Advanced technological field effect Transistors

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Summary

In this thesis, the design of Flip-Flops and Latches with different types of technological transistors are discussed. Flip-flops and latches being the fundamental building blocks of Digital Electronics Systems are used in Computers, Communications, and many other types of systems. This work targets the calculation of propagation time delay and power losses in a Flip-flop and latches circuit. In silicon industries, the above-mentioned parameters (propagation time delay and power loss) play a vital role in the commercial manufacturing of the Flip-Flops. So, a formal procedure and step by step process will be set and aligned in a particular order to get the desired results. Flip-flops and Latches are a combination of Inverters, NAND gates, Transmission gates which are further made up of a combination of different transistors. There are many different types of Transistors. Each Transistor type affects the functionality of an inverter which eventually impacts the change in the output of a Flip-Flop. In this thesis firstly, we will focus on different types of Transistors, their analytical modeling for their figure of merits (On Currents, Off Currents, Thresh hold voltage, mobility, Capacitances). Considering their figure of merits, we will move towards leakage currents and delay of transistors. These delays and leakage currents of single transistors will help us in the calculation of propagation delay and power losses of a Flip-flop, which is the basic goal of our work.

There are many types of Emerging devices like FinFet Transistors, Fully Depleted SOI Transistors, UTBB FD SOI Transistors, Tunnel Gate Field-Effect Transistors. A brief study of the architecture and investigation of the mentioned transistors will be carried out in accordance with different technological nodes in Chapter 1. We will further discuss a tool, developed by Politecnico di Torino, named "TAMTAM" which analyzes and compares the emerging devices, as mentioned above, with the Flip-Flop and suggests the compatible device for the Flip-Flop under observation.

Firstly, I started from FinFET Transistor which is an advanced type of technological transistors based on Triple-gate. I developed a simulation of its main figure of merit (ON current, OFF current, threshold voltage, electron mobility) on MATLAB. I verified the results of simulated numerical expression in accordance with the international road map. This module is based on a compact Model of

Drain Current in Short-Channel Triple-Gate FinFETs presented by Fasarakis [1]. Triple-gate FinFET is studied according to nodes 22nm, 16nm, 14nm, 10nm, 7nm, 5nm, and 3nm respectively. The starting analyzed node is 22nm since it is the first one in which tripe-gate FinFETs have been introduced by (Intel,2011). 5nm and 3nm are still under research by technology manufacturers. So, no solid results are obtained for these nodes (5nm and 3nm). But, FinFet is also implemented for these nodes as per my analysis and research. These FinFETs are simulated, by considering the approximation of the Lambert W function. After thoroughly checking and verifying data on MATLAB, I put these modules for different technological nodes in TAMTAM. TAMTAM provided reasonable results which are illustrated at the end of Chapter 2. The same chapter, Chapter 2, also contains a detailed description of FinFET's channel length modulation and Quantum Mechanical effects.

Secondly, I designed simulations for Fully Depleted SOI. These fully depleted SOI are valid only for specific technology and only for a single gate structure with a channel length higher than 22nm. The precision of the scripts and the computed quantities are not ensured below this technological node. Moreover, some assumptions have been done during the modeling which will be revealed during the discussion. By solving the two dimensional (2D) Poisson, implementation of thresh hold voltage is done in MATLAB considering different channel lengths. A detail of FD SOI is described in Chapter 3, that what terms will make effects on FD SOI like short channel effects, strained silicon thin-film doping, strained silicon thin-film thickness, Gate work function and also other parameters, Mobility is computed in the MATLAB. This particular model takes into account the Mobility Attenuation Phenomena, which takes place when down-scaling occurs, and the transverse electric field increases. Drain to Source current Ids is calculated for different Vds. Finally, including the effect of parasitic BJT, channel length modulation, and impact ionization channel inversion current is calculated. After correctness of these modules, I put these modules in TAMTAM, and TAMTAM gives results for these modules on different technological nodes 65nm, 22nm, 18nm, 12nm, 10nm.

Fully depleted low-doped channel technology is exploited in sub-20-nm devices due to the fact that excellent electrostatic control can be obtained. Among this kind of device architecture, MOSFETs based on ultra-thin body and buried oxide fully depleted silicon-on-insulator (UTBB-FDSOI) technology have two great advantages: they are planar and their architecture is similar to the one used for traditional bulk devices (simpler process with respect to FinFETs), and second, their performance can be efficiently tuned by applying a bias through the BOX (which enables a dynamic modulation of the speed/power trade-off). Drain current modeling and mobility modeling is done for 28nm and 20nm technological nodes, and finally these modules or illustrated in TAMTAM software.

In the Fifth chapter analytic model is described for single and double gate Tunnel FET. This chapter offers an analytic model to describe the current of a

Single Gate n-TFET(SGTFET) based on the Kane-Sze for the tunneling current, and Double Gate Tunnel FET. Firstly For (Single Gate Tunnel FET)After a brief introduction to the working principles of the TFET, this model will be compared to the result obtained in the Praveen model, some figures of merit will be highlighted in order to be compared to the traditional FET. In addition, a parametric analysis is performed to describe the influence of temperature and gate oxide on the device. In conclusion, some hints will be given to improve the TFET structure and optimize its characteristics. In the last years, the scaling of MOSFET technology has experienced a boost in reaching the dimension of the order of the nanometer. Further scaling of MOSFET gives rise to a number of issues such as gate tunnel current, parasitic effects, short channel effects, increase in the leakage current, and low value of the ON to OFF current ratio. All those effects contribute to the high level of static power consumption, even in the OFF operation condition. In a low power electronic device, such conditions must be at least minimized such that alternative designs to the traditional MOSFET are required to increase the performances of the device. Tunnel Field effect transistors (TFET) have been deeply investigated as a valid alternative to MOSFETs for low power digital applications in order to overcome the scaling limitation of standard CMOS technology. The figure of merit for these Tunnel FETs are set into TAMTAM.

In chapter 6, analysis and discussions are carried out on the deep understanding of Transistor, delay of an inverter, and NAND gates. Flip-Flops are formed using cross-coupled NAND gates which are made from nMOSFET and pMOSFET transistors. An analysis of transistors paves the way to approach the calculation of static power consumption and the amount of time it will take to make a change in the output of Flip-Flop, which is called the delay of Flip-Flops. Transistor level analysis is done with the help of Professor Mario Casu's lectures and with helping materials given by my supervisor Professor Marco VACCA. On the other hand delay of single transmission, the gate is calculated by me from studying Marco Vacca helping materials and of course by doing study research on many universities research papers for transmission gate. The calculations for propagation delay and static power consumption of SR flip-flop, mux based flip-flop, and mux based master-slave flip-flop were able to be performed by studying transmission gate, transistors, inverter, and NAND gate.

In chapter 7, the analysis of Flip-Flops is carried out with respect to the results obtained in Chapter 6. As we know that SR Flip-flop is a combination of two inverters. So, change in its state at output defines which transistors will be ON and OFF respectively. In this way, we calculated the propagation delay as a sum of transistors' delays. For Mux based Flip-flops, we calculated propagation delay as a sum of inverter delays and also delays of transmission gate, which is described in chapter 6. The calculation of static power consumption for Flip-flops depends on the sum of power consumed by the Inverters. Finally, a reflection of the whole

work is described in the Conclusion section and the future work arising from these studies is also discussed.

Acknowledgements

First and foremost, I would thank God for giving me this opportunity to undertake this research and courage to accomplish the results. Thereafter, I would like to offer my distinctive gratitude to my supervisors: Prof.Marco Vacca, Gianluca PICCININI, and Engr.Luca Gnoli.Their support, guidance, and patient supervision throughout my thesis was invaluable.
Discussions about the problems in the thesis during the meetings with Prof: Marco VACCA and his valuable advice proved helpful for me. Working in the VLSI lab with the supervision of Luca Gnoli during my thesis period enhanced my practical skills. Sharing his knowledge and concepts on software with me during discussions were always fruitful for me.
Also, I would like to extend my distinctive gratitude to my parents, family, and friends for always being there for me through thick and thin. I am grateful for their love and support, and for putting their trust in me, and for encouraging me to pursue my dreams.
Finally, thanks to this research activity for realizing me that, Engineering is like a big Galaxy and we all engineers are like small stars in this Galaxy. Overall there is still a lot more to learn to engineer.

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Acronyms

Chapter 1

Introduction

Flip-flops and latches are the building blocks of Digital Electronics Systems are used in Computers, Communications, and many other types of systems. In silicon industries, when they make a chip, they face important parameters which should be concerned are the propagation delay, Static Power losses, and Dynamic Power losses. These parameters (propagation time delay and power loss) play a vital role in the commercial manufacturing of the Flip-Flops. To calculate these parameters, firstly we should get a piece of knowledge about Transistors because Transistors are basics of Flip-flops. Flip-flops and Latches are a combination of Inverters, NAND gates, Transmission gates which are further made up of a combination of different transistors. There are many different types of Transistors. Each type of Transistor has its own performance level. The performance of Transistors depends on the structure of this transistor, and technological nodes. Technological node is a term in CMOS Technology, in which we consider length, width, and other physical dimensions. So we will start from Transistor level analysis, and a formal procedure and step by step process will be set and aligned in a particular order to get the desired results for Flip-flops and Latches. We will do analytical modeling for their figure of merits (On Currents, Off Currents, Thresh hold voltage, mobility, Capacitances). Considering their figure of merits, we will move towards leakage currents and delay of transistors. These delays and leakage currents of single transistors will help us in the calculation of propagation delay and power losses of a Flip-flop, which is the basic goal of our work. In this chapter, we will discuss the generic structures of emerging devices (Advanced types of Technological Transistors) like FinFET, FDSOI, UTBB, Single gate, and double gate field-effect transistors. In the last of this chapter, we will see that how a TAMTAM tool works, made up by our university Politecnico di Torino. TAMTAM is a tool to analyze the performance of a device on a different figure of merits based on different technological nodes according to the international road map.

1.1 Geometry of FinFET

FinFET is a promising architecture for MOS transistors with gate lengths of 22 nm and smaller. The main feature of the FinFET is that the active area of the transistor is realized as a thin silicon wire between the source and drain contacts. Technologically, the silicon fin is cut-out by an etching process from a silicon-on-oxide layer. The simplest gate design consists of a deposition of the gate material on the silicon fin after the gate oxidation and a subsequent structuring of the gate material to define the gate length. In the triple gate FinFET which results in this case, the gate wraps around the rectangular silicon fin from three sides. The triple gate FinFET has a large effective channel width: as will be illustrated below, the effective gate width of the transistor is equal to two times the thickness of the silicon-on-oxide layer plus the width of the silicon fin, $W_{eff} = 2T_{fin} + W_{fin}$. An alternative and more conservative gate architecture includes the preservation of a hard mask on top of the silicon fin before the gate deposition. In this case, there is no direct contact between the gate electrode and the gate oxide on top of the silicon fin and this part of the fin does not contribute to the effective gate width of the transistors, $W_{eff} = 2T_{fin}$. For a square cross section of the fin, one third of potentially usable gate width is lost if this transistor design is used, and consequently, a drive current which is about 1/3 lower is expected. The geometrical shape of transistor structures with gate wrap around triple gate FinFET is depicted in Figure in 1.1

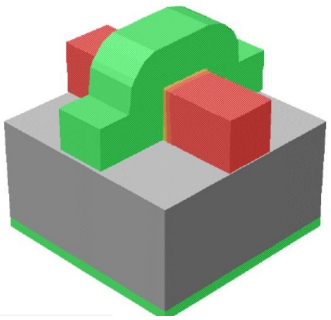

Figure 1.1: Geometrical shape of triple gate FinFET.

Now we will see the internal structure of Triple gate FinFET . In its structure hight of Fin and Width of Fin plays a vital role for its performance.We can changes these parameters according to International road map.Structure of Triple gate FinFET is shown in Figure 1.2

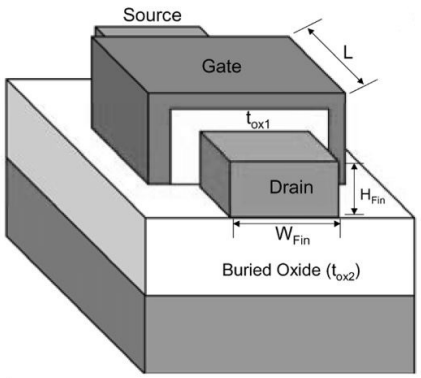

Figure 1.2: Structure of triple gate FinFET.

Figure 1.2 illustrate a structure of Triple gate FinFET. Parameters for this structure vary for different technological nodes. We will present here some parameters

- supply voltage V_{DD};
- fin top-base width W_{fintop} ;
- fin bottom-base width W_{finbot} ;
- fin height H_{fin};
- gate length L;
- gate oxide t_{ox}, which represents the Equivalent Oxide Thickness (EOT) and whose value is chosen to be around the minimum one preventing gate tunnelling, since no data from the manufacturers are available.

Analytical modeling of this structure(FinFET) is done in chapter 2 with a detail description.These Analytical models conclude results for FinFET,s figure of merits (On Currents , Off Currents, Thresh hold voltage, mobility).TAMTAM tool will gives us result of these figure of merits for different technological nodes simultaneously.

1.2 Fully Depleted Silicon on Insulator (FDSOI) CMOS Transistors

Here we will see the generic structure of Transistor, one from advanced technological Field Effect Transistors. Fully Depleted Silicon on Insulator, or FD-SOI, is a planar process technology that relies on two primary innovations. First, an ultra-thin layer of insulator, called the buried oxide, is positioned on top of the base silicon. Then, a very thin silicon film implements the transistor channel. Thanks to its thinness, there is no need to dope the channel, thus making the transistor Fully Depleted. FDSOI technology exhibits major benefits for advanced and future technology nodes. Thin silicon film technology allows superior electrostatic control of the gate on the channel of the transistor, compared to conventional architectures (like FinFETs). This control is accomplished by efficient body biasing, which provides faster switching speeds, and provides a good compromise between performance and power consumption at the circuit level.FDSOI Transistor geometry is shown in figure 1.3

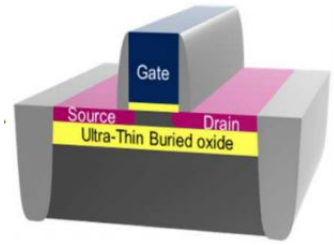

Figure 1.3: Geometry of Fully depleted SOI Transistor

Ultra-Thin Buried oxide gives benefits in its performance e.g Its reduces short channel effect(SS,Drain induced barrier lowering effect).Because of Ultra-Thin Buried oxide there will be no History effects,and of course also lower SER(Soft Error Rates).

The key feature of the SOI structure is the layer of silicon dioxide below the surface. In particular, the buried oxide (BOX) is made by the oxidation of silicon (Si) or by oxygen (O) implantation into this latter. For what concern the notation used, with Si substrate is indicate the supporting substrate, while with Si body or SOI body is refer to the SOI layer that constitute the body of a MOSFET. The cross section of the structure of a single-layer fully depleted SOI (FD-SSOI) MOSFET is reported in figure 1.4

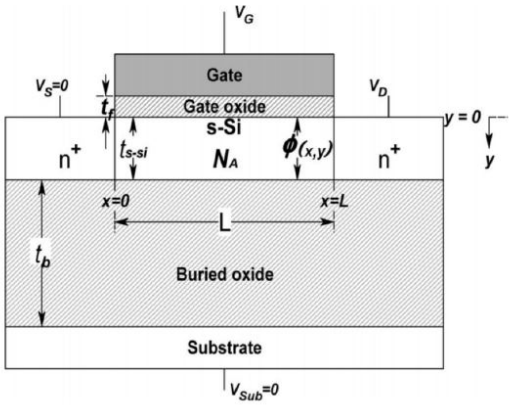

Figure 1.4: Cross section of single layer FD SOI MOSFET

In particular the full dielectric isolation of the device prevents the occurrence of most of the parasitic effects. Circuits based on this technology have the maximum capacitance between the junctions and the substrate equal to the capacitance of the buried insulator. It is proportional to the dielectric constant ("$\epsilon_{ox} = 3.9\epsilon_o$"0 in case of Silicon Dioxide) that is approximately three times smaller with respect to the silicon one ($\epsilon_{Si} = 11.7\epsilon_o$). As consequence this parasitic capacitance becomes smaller than that of a bulk junction.Furthermore, a further advantage is that circuits fabricated with SOI technology require fewer processing steps than bulk CMOS technology.Buried oxide (BOX) is made by the oxidation of silicon (Si) or by oxygen (O) implantation into this latter. For what concern the notation used, with Si substrate is indicate the supporting substrate, while with Si body or SOI body is refer to the SOI layer that constitute the body of a MOSFET.A complete modeling of FD SOI Transistor is discussed in Chapter 3.

1.3 Structure of UTBB FDSOI TRANSISTOR

In chapter 4 there is modeling for UTBB FDSOI TRANSISTOR .But here We will discuss a generic structure of UTBB FDSOI.In chapter 3, we will explore fully depleted low technology on 22nm Technological.No doubt, FD SOI has excellent electrostatic control.But Among this kind of device architecture, MOSFETs based on ultrathin body and buried oxide fully depleted silicon-on-insulator (UTBB-FDSOI) technology have two great advantages: they are planar and their architecture is similar to the one used for traditional bulk devices (simpler process with respect to FinFET), and second their performance can be efficiently tuned by applying a bias through the BOX (which enables a dynamic modulation of the speed/power trade-off).A geometry of UTBB FD SOI Transistor is depicted in figure 1.5.

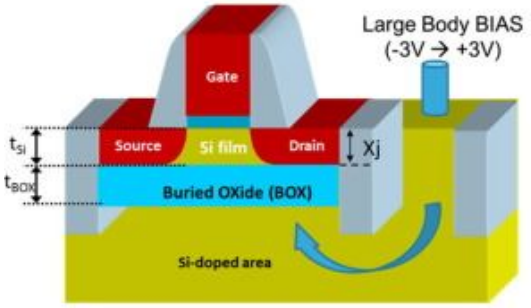

Figure 1.5: Geometry of UTBB FD SOI MOSFET

UTBB FD-SOI technology is a very interesting solution that provides flexibility between high performance and low leakage. By applying a second voltage to the bottom of the transistor, we can cut the leakage or improve the speed of the transistor. Moreover, as FD-SOI is a planar technology, it is cheaper as compared to the 3D FinFET technology.Here Body biasing plays vital role in improvement of Transistor performance.Efficient Body Biasing for Selectable Lower Power or Improved Performance is done.

In Chapter 4, We will describe and implement a model developed by Leti, a technology research institute at CEA Tech, valid for low-doped UTBB transistors. The system under study is the one in figure 4.1:

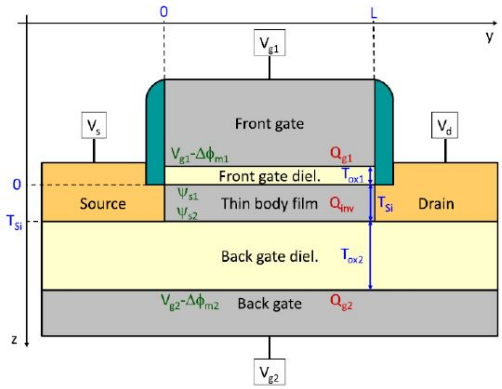

Figure 1.6: Internal structure of UTBB FD SOI MOSFET

The main initial input parameters are listed in the table of Fig. 1.7, together with their dimensionless counterparts.

Symbol	Unit	Definition	Dimensionless counterpart
ϕ_T	V	Thermal potential	
ψ_{s1}	V	Front interface electrostatic potential	$x_1 = \psi_{s1}/\phi_T$
ψ_{s2}	V	Back interface electrostatic potential	$x_2 = \psi_{s2}/\phi_T$
$\Delta\phi_{m1}$	V	Front gate workfunction with respect to midgap level of channel material	
$\Delta\phi_{m2}$	V	Back gate workfunction with respect to midgap level of channel material	
V_{g1}	V	Front gate voltage	$x_{g1} = (V_{g1} - \Delta\phi_{m1})/\phi_T$
V_{g2}	V	Back gate voltage	$x_{g2} = (V_{g2} - \Delta\phi_{m2})/\phi_T$
ϕ_{im}	V	Carrier quasi-Fermi level	$x_n = \phi_{im}/\phi_T$
V_s	V	Source bias	$x_s = V_s/\phi_T$
V_d	V	Drain bias	$x_d = V_d/\phi_T$
ε_{ch}	F/m	Permittivity of thin body film	
C_{Si}	F/m^2	Depleted body capacitance (ε_{ch}/T_{Si})	
C_{ox1}	F/m^2	Front gate dielectric capacitance	$k_1 = C_{ox1}/C_{Si}$
C_{ox2}	F/m^2	Back gate dielectric capacitance	$k_2 = C_{ox2}/C_{Si}$
Q_{g1}	C/m^2	Front gate charge density	$q_1 = Q_{g1}/(C_{ox1}\phi_T)$
Q_{g2}	C/m^2	Back gate charge density	$q_2 = Q_{g2}/(C_{ox2}\phi_T)$
Q	C/m^2	Coupling charge (real or imaginary)	$q = Q/(C_{Si}\phi_T)$

Figure 1.7: Initial input parameters

1.4 Tunnel Gate Field Effect Transistors

In chapter 5,We will do modeling for Tunnel gate field effect transistors.Even though its structure is very similar to a metal-oxide-semiconductor field-effect transistor (MOSFET), the fundamental switching mechanism differs, making this device a promising candidate for low power electronics. TFETs switch by modulating quantum tunneling through a barrier instead of modulating thermionic emission over a barrier as in traditional MOSFETs. Because of this, TFETs are not limited by the thermal Maxwell–Boltzmann tail of carriers, which limits MOSFET drain current subthreshold swing to about 60 mV/decade of current at room temperature.The device is operated by applying gate bias so that electron accumulation occurs in the intrinsic region for an n-type TFET. At sufficient gate bias, band-to-band tunneling (BTBT) occurs when the conduction band of the intrinsic region aligns with the valence band of the P region. Electrons from the valence band of the p-type region tunnel into the conduction band of the intrinsic region and current can flow across the device. As the gate bias is reduced, the bands becomes misaligned and current can no longer flow.A structure of Tunnel field effect transistor is depicted in fig 1.8.

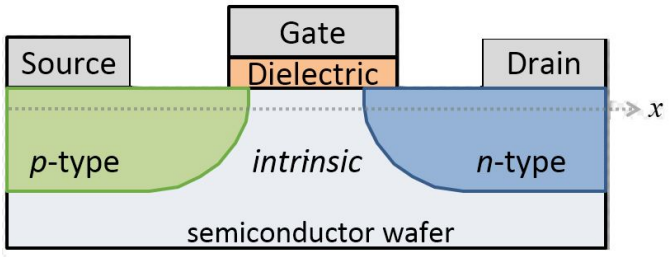

Figure 1.8: Basic lateral structure of Tunnel Field effect transistor

The basic TFET structure is similar to a MOSFET except that the source and drain terminals of a TFET are doped of opposite types (see figure 1.8). A common TFET device structure consists of a P-I-N (p-type, intrinsic, n-type) junction, in which the electrostatic potential of the intrinsic region is controlled by a gate terminal.This is a promising device but still it is not developed and many studies are still in progress to find how to improve its characteristics: MOSFETs are still better devices whereas high currents are needed and up to now TFETs are not able to reach high ON currents keeping a very low OFF current.There are two types of Tunnel gate field effect transistore, one is single gate tunnel field effect transistor and other is double gate field effect transistors.

A comparison of n-mosfet and n-tfet is depicted in figure 1.9.

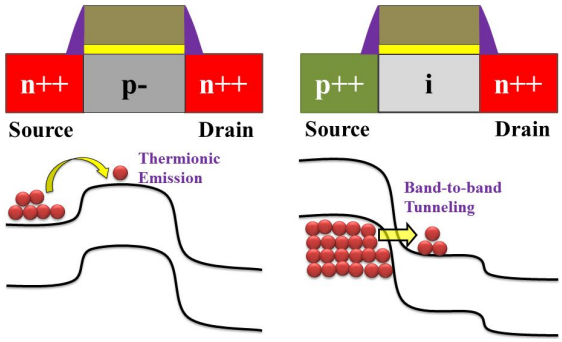

Figure 1.9: MOSFET and TFET comparison

The difference between the two devices is that, even though the structure is the same of the MOS, the source and drain terminals are doped of opposite type. This gives rise to the so called Band-To-Band Tunneling (BTBT) when a gate bias is applied. The TFET exploits this effect because it can be seen as a gated p-i-n diode in reverse bias where, under a gate a bias applied to the gate terminal, the conduction band edge of the source shifts below the valence band of the channel creating the so called tunneling window.that allow the electrons tunneling current (Zener tunneling). This current is modelled by the transmission probability across the tunneling barrier that can be described by the Wentzel-Kramers-Brillouin (WKB) approximation (1.10), that approximates the barrier in the ON state as a triangle of height equal to the energy gap EG and width equals to the parameter λ (also called screening λ). The TFET exploits band-to-band tunneling instead of thermal injection of electrons and this allows to break the limit of the 60mV=dec in the sub threshold swing of the conventional MOSFET.

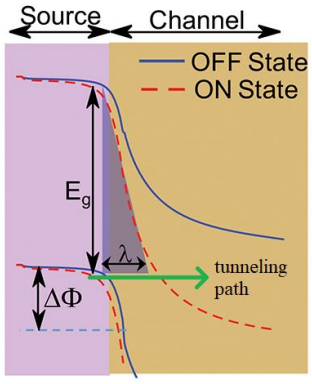

Figure 1.10: Tunneling barrier approximation

1.5 Flip-flops overview for advanced technological FET,s

Up to chapter 5, we will do the modeling for these above described advanced types of technological transistors. After that in chapter 6, we will do calculations for transistor leakage current and static power consumption.Static power consumption and Dynamic power consumption are major things to be understood in the silicon industry. A transistor-level study will reveal the relationship between leakage current and power consumption. As the leakage current is different for different technological transistors so is the power consumption of such transistors. For flip-flop propagation delay, we should know the delay of a transistor, delay of an inverter, and delay of a NAND Gate because these are all the building blocks for flip-flops. Some flip flops are made from cross-coupled NAND Gates. So, it is imperative to focus on the derivations of a cross-coupled NAND gate. Also in chapter 7, We will study about Transmission gate. A transmission gate (TG) is an analog gate similar to a relay that can conduct in both directions or block by a control signal with almost any voltage potential. It is a CMOS-based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1. These calculations will be done for the purpose to calculate the Static Power consumption of Flip-flops. We will calculate propagation delay and static power consumption for SR Flip-flop, Multiplexer based Flip-flop, and Multiplexer based master-slave flip-flops.A transistor based SR Flip-flop is depicted is shown in fig 1.11 Our TAMTAM software will calculate propagation delay and static

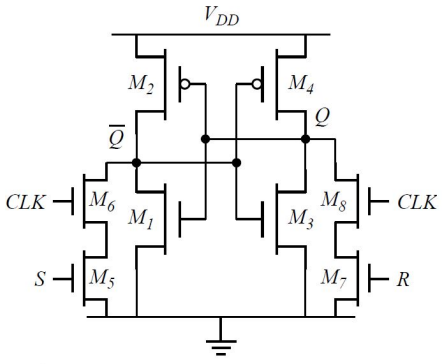

Figure 1.11: Structure of SR Flip-flop

power consumption for above all field effect transistors with different technological nodes.About TAMTAM software made by Politecnico di Torino, We will discuss in next section.

1.6 Introduction to TAMTAM Software

TAMTAM is a tool which is made by Politechnico di Torino. TAMTAM estimates the performance of devices. TAMTAM can give us an estimation of performance by examining the modules created for emerging devices, considering different Technological nodes simultaneously. It's can give us result in chart form or also in values if we want to check a single parameter in our modules like mobility, Potential, or effective capacitance. Let suppose we want to select a device for our digital system on Ion/Ioff basis from many technological nodes, so we will select the Transistor type and the TAMTAM tool will give us a chart of Ion current for different technological nodes. In this way, we can see from our chart that, which technological nodes will be efficient for our device manufacturing. TAMTAM tools have many features. There are sections in this tool, where we can put our modules and technological bottoms separately. In the module section, we will put our codes which are made in MATLAB software, also we can write the code in TAMTAM itself. In the Technology bottoms section, we will put of technological nodes, which we will study in the next chapters in detail. TAMTAM will run the module section and technological bottoms section simultaneously. From seeing the graph, we can estimate that which node is efficient in a better performance way.TAMTAM tool home page view is depicted in figure 1.12

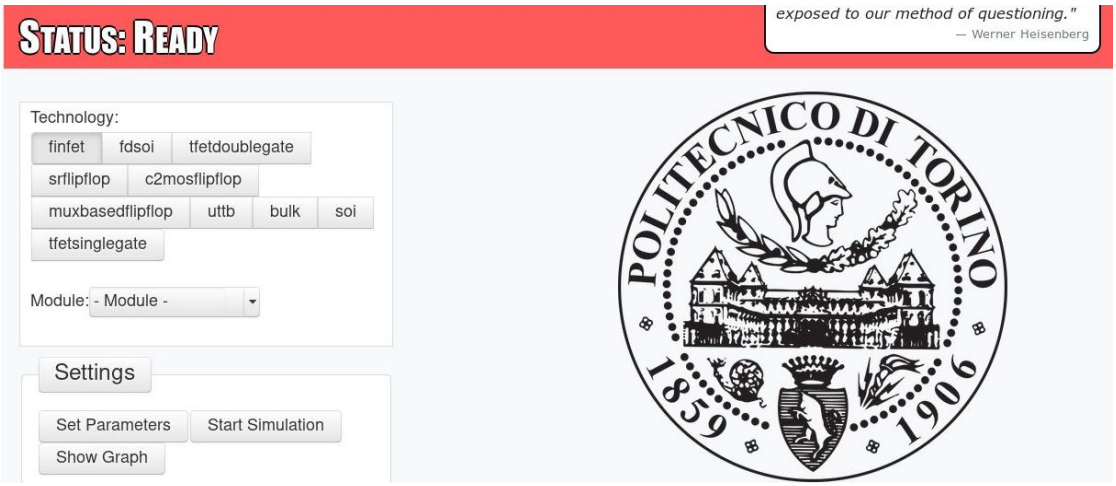

Figure 1.12: TAMTAM tool window view

In the module section, we will put our modules which are also simulated on MATLAB. But on MATLAB these modules are simulated for one node, TAMTAM gives us feature to simulate these modules simultaneously. Modules for an advanced type of technological transistor-like On current, Off current, gate current, threshold voltage, and all other modules will be put into the modules section. A picture of the module section is shown in figure 1.13 In the Technology bottom section, we will

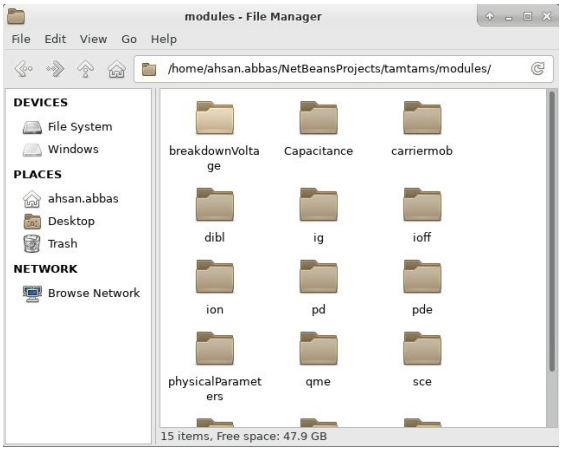

Figure 1.13: View of Module section in TAMTAM

put our technological nodes which are taken from companies' research and many articles. In different years, different nodes were made according to the International road map. A picture of the bottom section is shown in figure 1.14

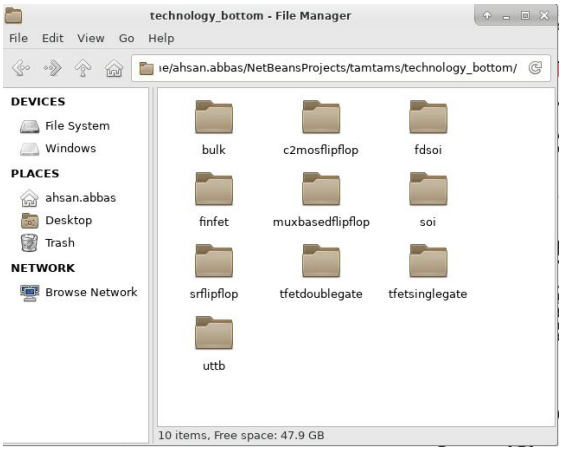

Figure 1.14: View of Technological nodes section in TAMTAM

TAMTAM has amazing features. Suppose we want to calculate the threshold voltage of the Transistor making other potentials like Vgs(gate to source voltage) constant so we have to set a parameter Vgs to a fixed value. And TAMTAM will give us all results considering the Vgs fix, which we set before simulation. Other Parameters also we can fix whatever we want. Sometimes we make a drain to source voltage fix and we can calculate gate to source voltage also vice versa.A picture from TAMTAM tool is given below for better understanding.
in the window given in above figure 1.15 we can set parameters. usually, we use

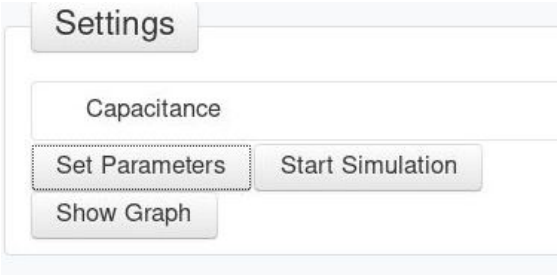

Figure 1.15: window for Setting the parameters

this feature of TAMTAM. Because in many codes we need to fix the values of some parameters. **Dependency** is another feature of the TAMTAM tool. Let suppose sometimes our Threshold voltage is dependent on electron mobility. So we cant write all code of mobility in the Threshold module, we will just make Threshold voltage dependent on electron mobility.TAMTAM will automatically calculate electron mobility for device and then TAMTAMM will simulate the Threshold module dependent on electron mobility. In this way, if we want to make one module dependent on others so we can use this feature of TAMTAM.When we put our modules in the module section and technological nodes in the technological bottoms section, so it's also necessary to tell the TAMTAM which technological nodes it should select for a specific module. For example, if we want to run the module of FinFET transistor, But there are technological nodes of FinFET, FDSOI, UTBB FDSOI.So how TAMTAM will just select FinFET technological nodes, it will be done by a **(.xml)** file containing the direction of FinFET technological nodes for FinFET modules and other modules also in the same way. **(.xml)** file will contain necessary data like Name to be shown for a module, technological node file for the specific module, and also dependency information if there is anyone in our modeling. In this way, TAMTAM will work and gives us the result in chart form and figure forms. In the next chapter, we will depict figures for different modules of advanced types of technological Transistors.

Chapter 2

FinFet Transistors

2.1 Modules to be integrated for different technological bottoms

In this model,Triple-gate FinFET is analyzed ,first of all its main figures of merit (ON current, OFF current, threshold voltage, electron mobility) are simulated on MATLAB and then these are simulated on TAMTAM software,on which we are working.All results are analyzed according to International road map.Triple gate FinFET is studied according to nodes 22nm,16nm,14nm,10nm,7nm,5nm,and 3 nm respectively.The starting analysed node is 22nm,since it is the first one in which tripe-gate FinFETs have been introduced by (Intel,2011).It is also important to observe that actually there are no manufacturer data related to 5 nm and 3 nm technologies available: the reason is to be traced to the fact that these two technology nodes are still under development and therefore there are neither commercial devices based on these nodes nor precise information about their key features.

The MATLAB modules are based on the Compact Model of Drain Current in Short-Channel Triple-Gate FinFETs presented by Fasarakis et al [1].,already studied and implemented in MATLAB by Amato et al.[2].In particular,the developed modules are built starting from [1], whose MATLAB code is (slightly) modified according to [3] and implementing the approximated Lambert W function with different and faster algorithms, which work in a mutually exclusive fashion, according to the value of the input argument as shown in [4] and [5].As in [2] , the modules give the possibility to take into account SCEs such as quantum-mechanical effects, channel length modulation and mobility degradation, depending on the activation of the corresponding flags. Moreover, in order to work properly, each module requires an input set of parameters. Parameters are listed below

- supply voltage V_{DD};

- fin top-base width W_{fintop} ;
- fin bottom-base width W_{finbot} ;
- fin height H_{fin};
- gate length L;
- gate oxide t_{ox}, which represents the Equivalent Oxide Thickness (EOT) and whose value is chosen to be around the minimum one preventing gate tunnelling, since no data from the manufacturers are available.We will see above terms in the structure of FinFET.Generic structure of FinFET is shown in figure 2.1

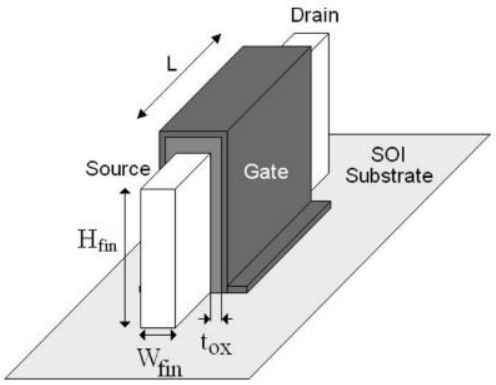

Figure 2.1: Schematic representation of a TG FinFET

In figure 2.1 we can see that there is a Buried oxide layer, FinFET height, FinFET width. These parameters will define our technological nodes.

2.1.1 Drain current model of Ideal rectangular FinFETs

The MATLAB modules are based, as previously mentioned, on the model derived by Fasarakis et al. [1], [3] and [6]. This compact model is fully analytical and valid in all the operating conditions of the triple-gate FinFET, taking also into account SCEs, such as Channel Length Modulation (CLM), Mobility Degradation (MoD) and Quantum Mechanical Effects (QMEs). In addition to this, the model can deal with a trapezoidal geometry by including equivalent corner effects.If no SCEs are considered, the formula for I_{DS} is the following:

$$I_{ds} = \mu_0 \frac{Weff}{L} \frac{\epsilon_{ox}}{t_{ox}} (2V_T)^2 \left((q_{iS} - q_{iD}) + \frac{1}{2} (q_{iS}^2 - q_{iD}^2) \right) \qquad (2.1)$$

where Wt_{eff} is the effective width of the gate, which in a triple-gate FinFET is defined as

$$W_{eff} = 2H_{fin} + W_{fin} \qquad (2.2)$$

The first charge term in the brackets of (2.1) dominates in the sub-threshold region while the second charge term is dominant in the super-threshold region. q_{iS} and q_{iD} are the normalized inversion sheet charge densities calculated with the formula:

$$q_i\left(V\right) = LambertW\left(\frac{V_G - V_{th} - V}{2V_T} \quad \frac{e^{\frac{V_G - V_{th} - V}{2\eta_{TG} V_T}}}{A + e^{\frac{V_G - V_{th} - V}{2\eta_{TG} V_T}}}\right) \qquad (2.3)$$

Given this formula, the computation of q_{iS} and q_{iD} is simply:

$$q_{iS} = q_i(VS) \qquad (2.4)$$

and same like that

$$q_{iD} = q_i(VD) \qquad (2.5)$$

The first term of the Lambert W function dominates in the above-threshold region, whereas the second termdominates in the subthreshold region. The argument of the function (2.3) also contains terms accounting for the channel charge control such as the parameter A, the subthreshold swing coefficient η_{TG} and the threshold voltage V_{th}, which are computed as follows:

$$A = 4e^{\frac{v_{th} + V_{FB}}{V_O} - c_1} \qquad (2.6)$$

where $V_0 = 1V$ is a normalising factor and c_1 is a fitting parameter,

$$\eta_{TG} = \frac{1}{1-2(A1,_{TG}+A2,_{TG})} \qquad (2.7)$$

and Threshhold voltage will be

$$V_{th} = V_{FB} - \frac{A1,_{TG}(V_{bi}+V_{DS})+A2,_{TG}V_{bi}}{1-(A1_{TG}+A2,_{TG})} + \frac{V_T \ln\left(\frac{N_A}{n_i^2}\ \frac{Q_{th}}{W_{thin}}\right)}{1-(A1_{TG}+A2,_{TG})} \qquad (2.8)$$

The expression (2.8) includes the flat band voltage, which is computed as

$$V_{FB} = \Phi_M - \chi_{Si} - \frac{E_g}{2q} + \frac{V_T}{2}\ln\left(\frac{N_v}{N_c}\right) - V_T \ln\left(\frac{N_A}{n_i}\right) \qquad (2.9)$$

and the minimum carrier sheet density Q_{th}

$$Q_{th} = \frac{2V_T}{q}\left(\frac{C_{ox}^2}{C_{Si}}\right) \qquad (2.10)$$

where $C_{Si} = \frac{\epsilon_{Si}}{W_{fin}}$ Both equation (2.7) and (2.8) contain the parameters $A1_{TG}$ and $A2_{TG}$, which are geometrical factors expressed as

$$A1,_{TG} = \frac{2H_{fin}A_{1,sym}+W_{fin}A1,_{sym}}{W_{fin}+2H_{fin}} \qquad (2.11)$$

$$A2,_{TG} = \frac{2H_{fin}A_{2,sym}+W_{fin}A_{2,sym}}{W_{fin}+2H_{fin}} \qquad (2.12)$$

$A1_{sym}$, $A1_{asym}$, $A2_{sym}$ and $A2_{asym}$ depend on y_m, which is the position where the potential reaches its minimum value ("virtual cathode"),

2.1.2 Channel Length Modulation

Considering the CLM effect, the drain-current equation (2.1) becomes:

$$I_{DS} = \mu_o W_{eff} \frac{\epsilon_{ox}}{t_{ox}} (2V_T)^2 \left(\frac{q_{iS} - q_{iD}}{L} + \frac{1}{2} \frac{q_{iS}^2 - q_{iD}^2}{L - \Delta L} \right) \qquad (2.13)$$

In fact, when the CLM effect occurs, the effective channel shortens of a quantity ΔL with respect to its physical length L. This quantity is evaluated as

$$\Delta L = \lambda_{eff} \ln \left(1 + \frac{V_{d,eff} - V_{od}}{V_E} \right) \qquad (2.14)$$

Where

$$\lambda_{eff} = \frac{1}{\sqrt{\frac{1}{\lambda_{sym}^2} + + \frac{0.25}{\lambda_{sym}^2}}} \qquad (2.15)$$

and

$$V_{d,eff} = V_{od} + (V_{DS} - V_{od} + 0.25) \tanh \left(\frac{V_{DS}}{V_{OD} + 0.25} \right)^2 \qquad (2.16)$$

2.1.3 Mobility Degradation

The effects of series resistance and saturation velocity, due to the horizontal field and to the surface roughness scattering, can be included in the electron mobility expression through the mobility attenuation factor of the first order (the_1)

$$\mu = \frac{\mu_o}{1 + \theta_1 V_T q_{iS}} \qquad (2.17)$$

Where

$$\theta_1 = \theta_{1,0} \left(1 + \frac{\mu_0 V_{DS}}{\nu_{sat}(L - \Delta L)} \right) + \frac{\mu_0 W_{eff} C_{ox}}{L - \Delta L} R_{sd} \qquad (2.18)$$

This expression contains the linear mobility attenuation coefficient $\theta_{1,0}$,the electron saturation velocity ν_{sat} and the series resistance R_{sd}.

2.1.4 Quantum Mechanical Effects

QMEs mainly consist of two different contributions: structural confinement, which results in a quantum threshold-voltage shift, and gate capacitance degradation, leading to an increased value of the gate oxide thickness. The former accounts for an increase of V_{th}. equal to

$$\Delta V_{th}^{QM} = \frac{\alpha(\pi h)^2}{2qm_{eff}W_{fin}^2} \qquad (2.19)$$

Where $\alpha = 1$ for double-gate ($H_{fin} >> W_{fin}$)$\alpha = 2$ for triple-gate(square cross section) FinFET and $\alpha = 1.5$ in the case of rectangular triple-gate structure. The latter contribution can be introduced in the model by substtuting t_{ox} with t_{ox}^{QM}.

$$t_{ox}^{QM} = t_{ox} + \Delta z \, \frac{\epsilon_{ox}}{\epsilon_{Si}} \qquad (2.20)$$

where Δz is the "dark space". Also this modification increases the threshold voltage V_{th} and therefore the final expression is the following:

$$V_{th}^{QM} = V_{th}\left(t_{ox}^{QM}\right) + \Delta V_{th}^{QM} \qquad (2.21)$$

2.2 Modules Integration on Matlab

The input variables for each MATLAB code are consistent with the parameters provided by the chosen manufacturer for the 22 nm node [7], [8]. In this specific case, it is useful to notice that the cross section of the fin is trapezoidal (6:8 top/bottom base ratio). First of all, the transcharacteristics and the output characteristics are evaluated using a proper MATLAB script and shown in figures 2.2 and 2.3

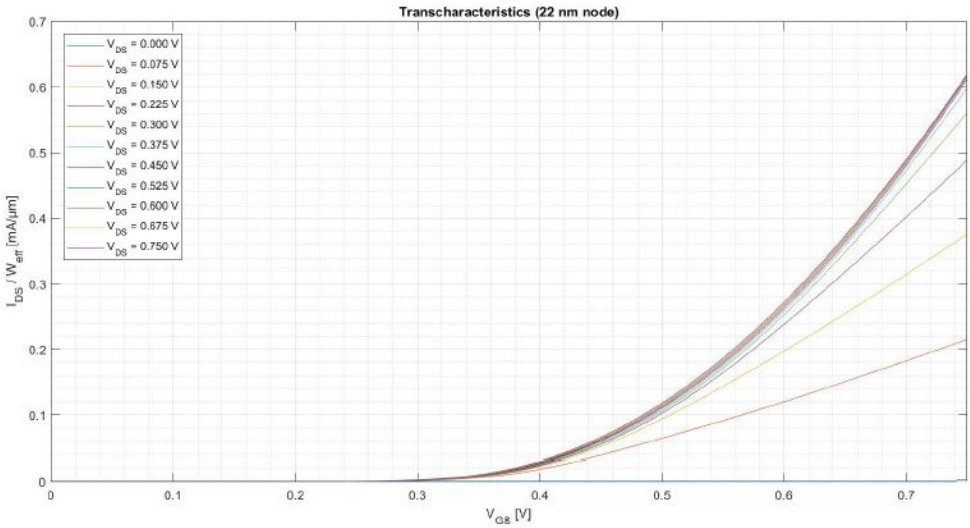

Figure 2.2: Transcharacteristics of the 22 nm device for different V_{DS} values.

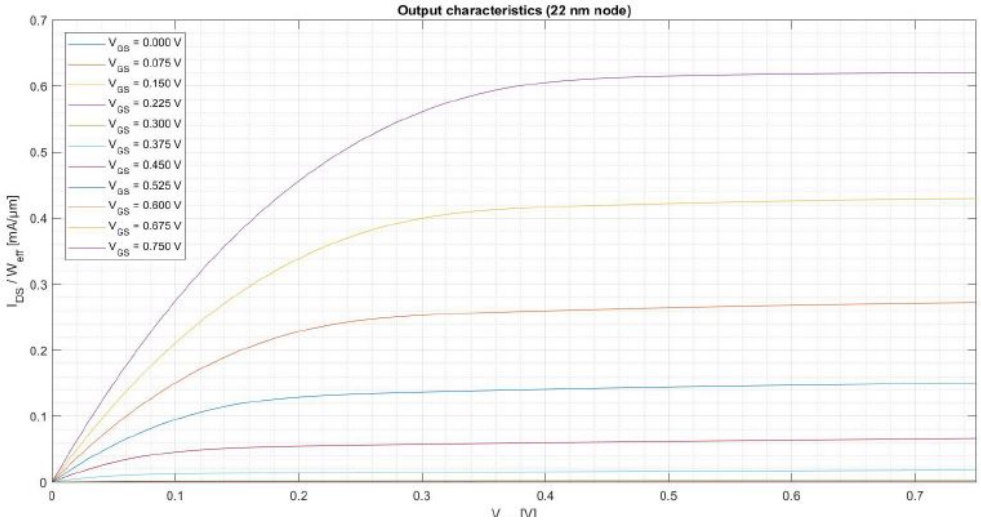

Figure 2.3: Transcharacteristics of the 22 nm device for different V_{GS} values.

The input variables for each MATLAB code are consistent with the parameters provided by the chosen manufacturer for the 16 nm node [9], [10] In this particular case, it can be observed that the geometry of the fin is rectangular. Firstly, the transcharacteristics and the output characteristics are evaluated using a proper MATLAB script and shown in figures 2.4 and 2.5.

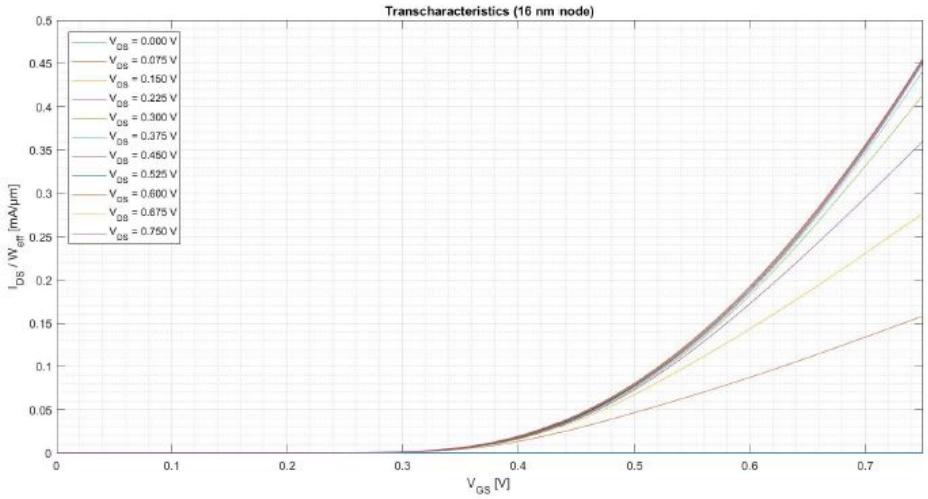

Figure 2.4: Transcharacteristics of the 16 nm device for different V_{DS} values.

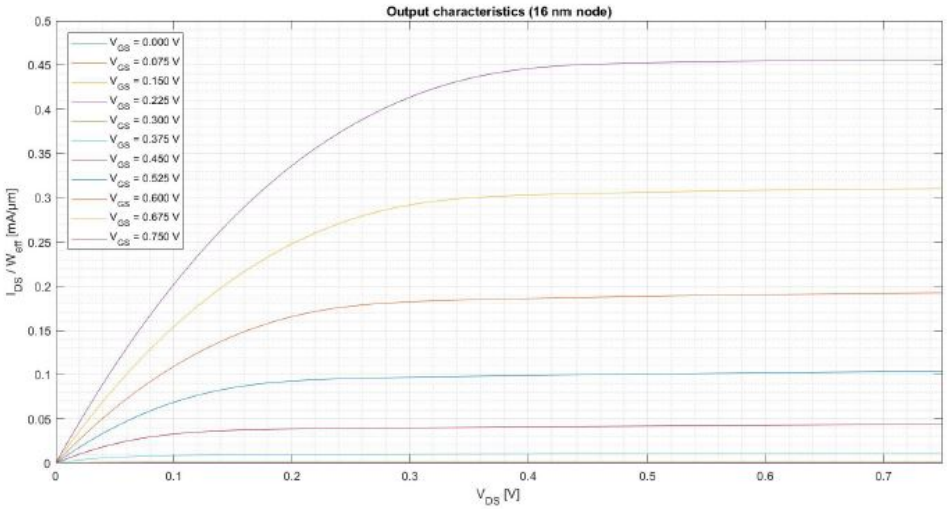

Figure 2.5: Transcharacteristics of the 16 nm device for different V_{GS} values.

The input variables for each MATLAB code match the parameters provided by the chosen manufacturer for the 14 nm node [11], [12]. In this particular case, it can be observed that the geometry of the fin is rectangular. First, the transcharacteristics and the output characteristics are evaluated using a proper MATLAB script and shown in figures 2.6 and 2.7.

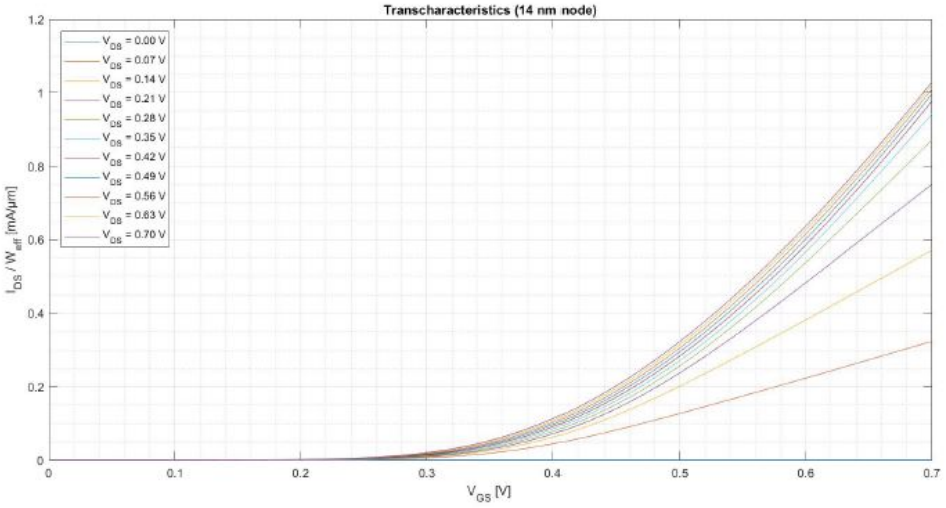

Figure 2.6: Transcharacteristics of the 14 nm device for different V_{DS} values

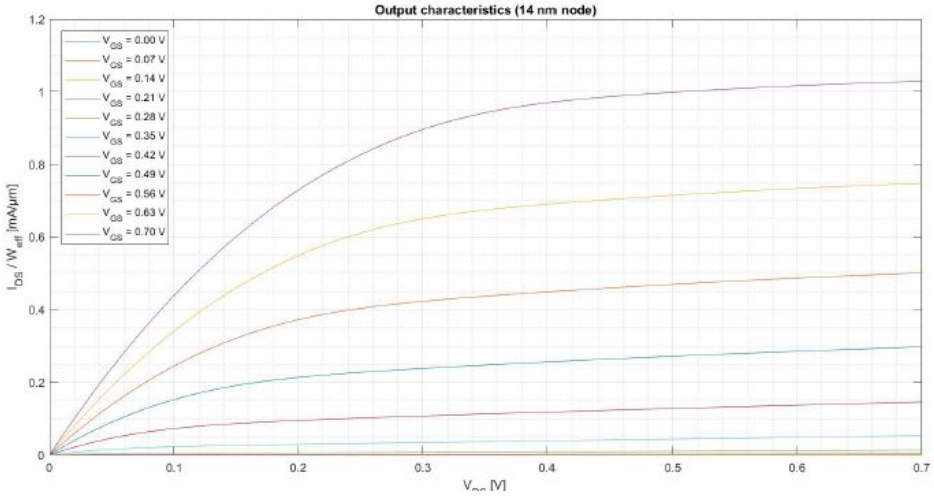

Figure 2.7: Transcharacteristics of the 14 nm device for different V_{GS} values

The input variables for each MATLAB code are in agreement with the parameters provided by the chosen manufacturer for the 10 nm node [13], [14]. In this particular case, it can be noticed that the geometry of the fin is rectangular. Firstly, the transcharacteristics and the output characteristics are evaluated and plotted using a proper MATLAB script and shown in figures 2.8 and 2.9.

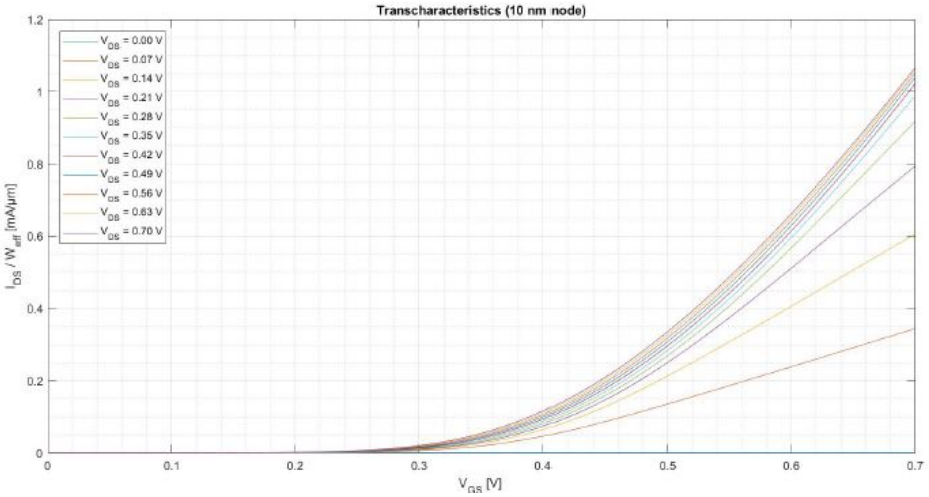

Figure 2.8: Transcharacteristics of the 10 nm device for different V_{DS} values

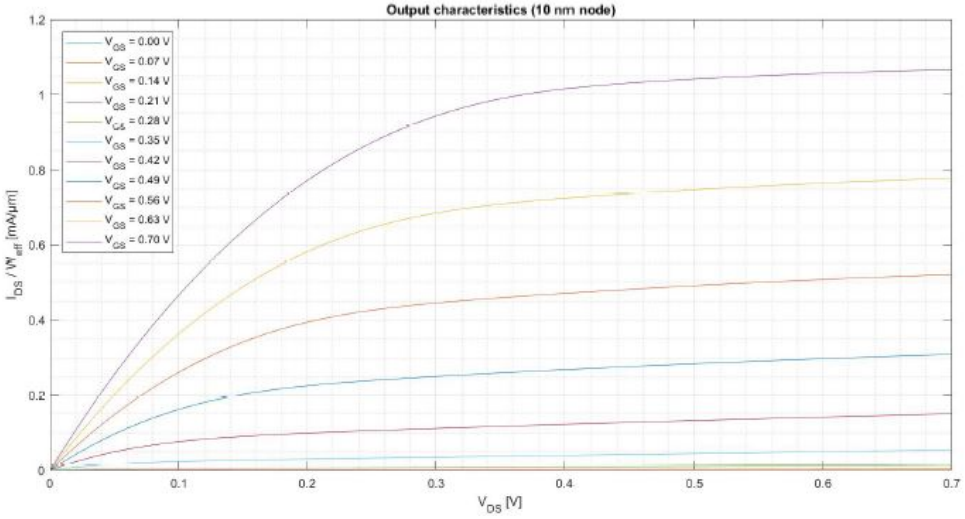

Figure 2.9: Transcharacteristics of the 10 nm device for different V_{GS} values

The input variables for each MATLAB code are chosen accordingly to the parameters provided by the manufacturers for the 7 nm node: due to the lack of a complete set of data from a single manufacturer, results are taken both from Global Foundries . Moreover, given the impossibility to find an actual value of the gate length for this node, the same length as in the previous section (10 nm node) is used. Also in this case, it can be observed that the geometry of the fin is rectangular. As usual, the transcharacteristics and the output characteristics are evaluated using a proper MATLAB script and shown in figures 2.10 and 2.11.

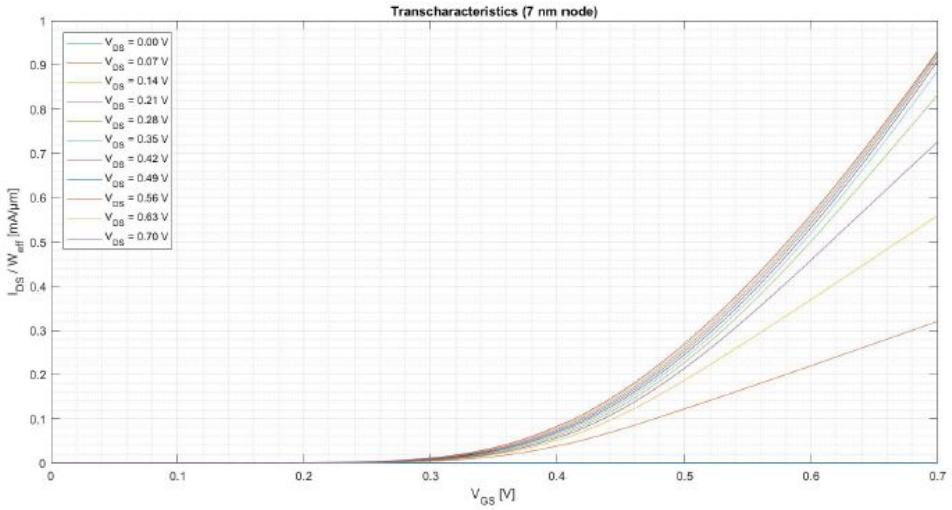

Figure 2.10: Transcharacteristics of the 7 nm device for different V_{DS} values

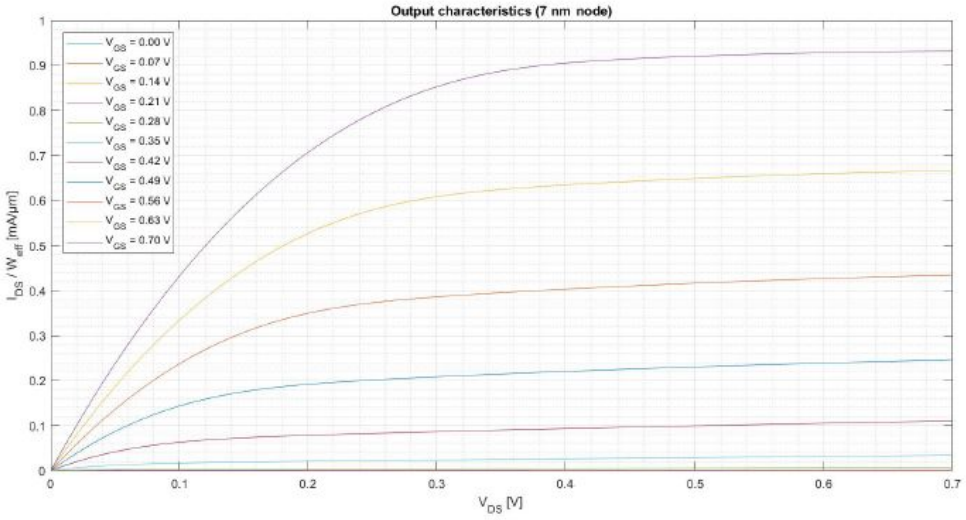

Figure 2.11: Transcharacteristics of the 7 nm device for different V_{GS} values

2.3 Modules Integration on TAMTAM

In figure 2.12 here are results from TAMTAM tool for FinFET transistors for different technological nodes,like 22nm,16nm,14nm,10nm,7nm,5nm.Its clearly seen that when we are going towards short channel width,the On current Ion is increasing.For 22nm Ion is $4.65e^{-5}$ A/um and for 3nm is $1.407e^{-4}$ A/um

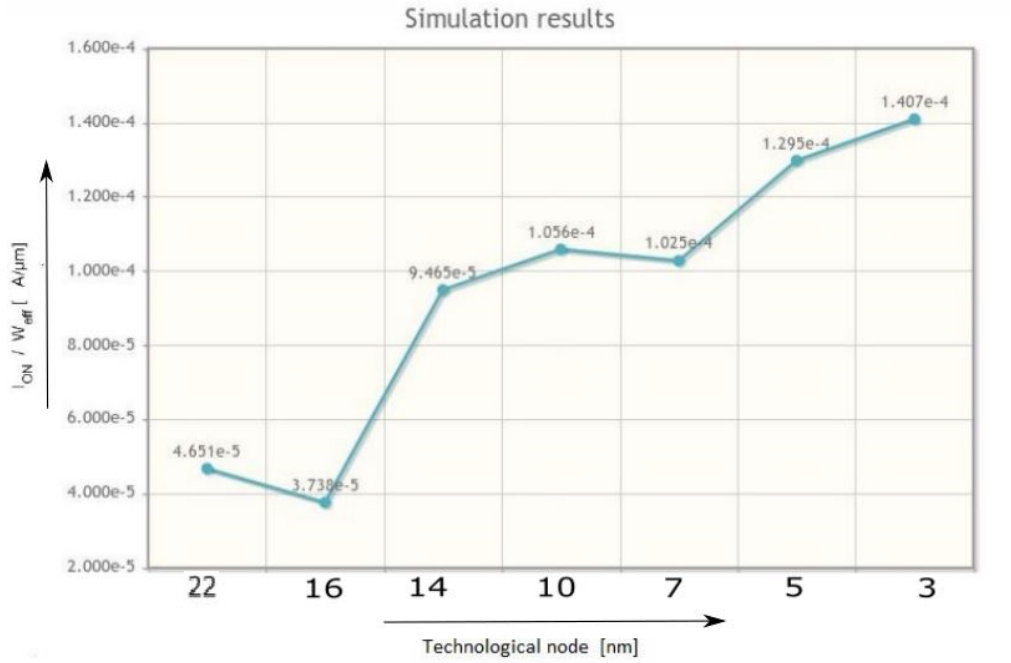

Figure 2.12: On current of FinFET for different technological bottoms

In figure 2.13 here are results from TAMTAM tool for FinFET transistors for different technological nodes,like 22nm,16nm,14nm,10nm,7nm,5nm.Off current is pictured here from TAMTAM

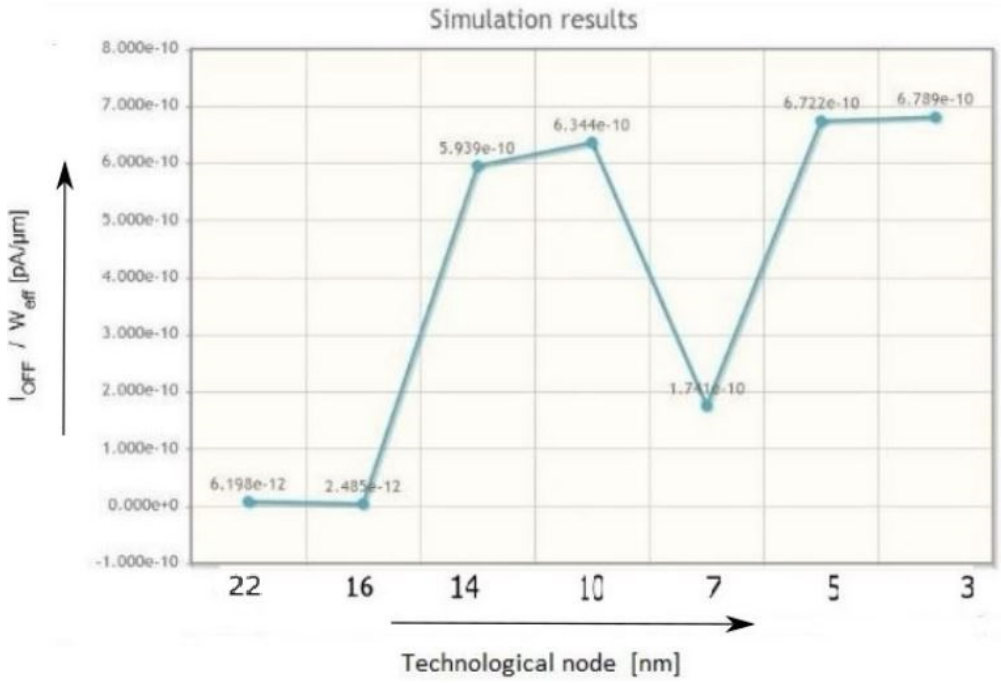

Figure 2.13: Off current of FinFET for different technological bottoms

In figure 2.14 here are results from TAMTAM tool for FinFET transistors for different technological nodes,like 22nm,16nm,14nm,10nm,7nm,5nm.Electron mobility is pictured here from TAMTAM.We can see a huge decrease in electron mobility from 22nm towards 3nm.

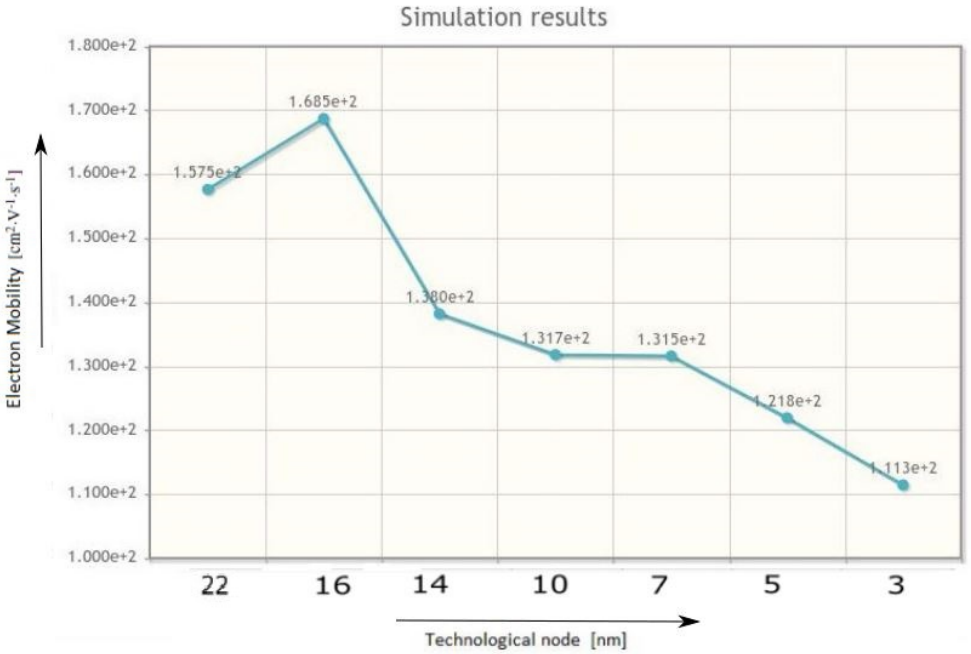

Figure 2.14: Electron mobility for different Technological nodes

In figure 2.15 here are results from TAMTAM tool for FinFET transistors for different technological nodes,like 22nm,16nm,14nm,10nm,7nm,5nm.Threshhold voltage is pictured here from TAMTAM.

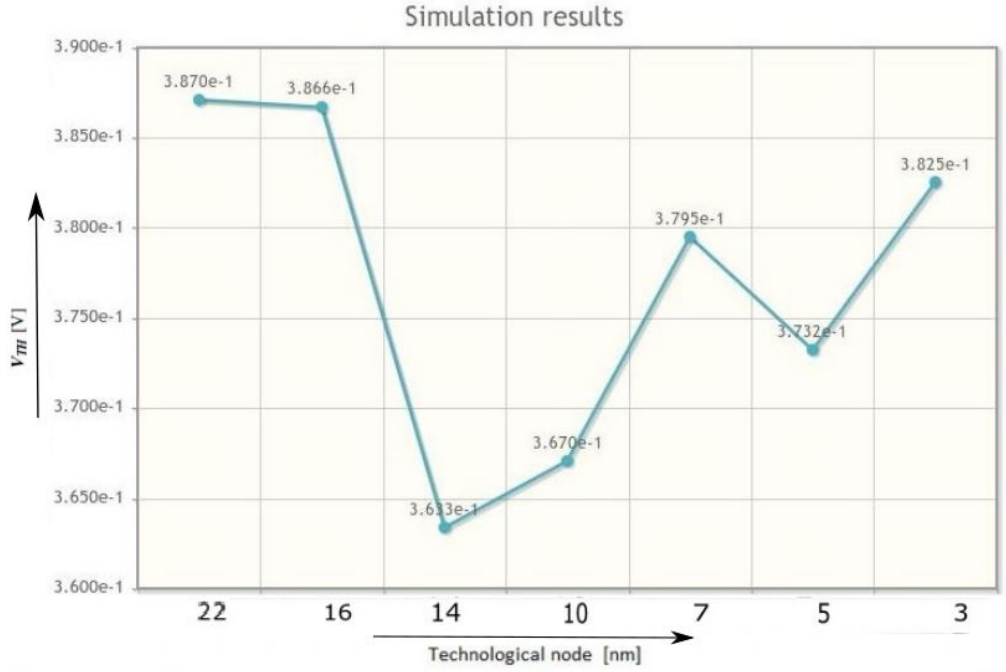

Figure 2.15: Threshhold voltage for different Technological nodes

Chapter 3

Fully Depleted SOI

In this chapter we present the models used and implemented on MATLAB for the estimation of the main FoM concerning FD-SOI MOSFETS. We remember to the reader that such models are valid only for this specific technology and only for a single gate structure with a channel length higher than 22 nm. The precision of the scripts and the computed quantities are not ensured below this technological node. Moreover, some assumption have been done during the modeling which will be announced during the discussion.

3.1 Modules to be integrated for different technological bottoms

Here we will discuss different modules for Fully depleted SOI.Firstly analyrical modeling is done for different modules,then these modules are implemented on MATLAB,and then these modules are implemented on TAMTAM for different technological node.In MATLAB we solved two-dimensional poisson equation and calculated our threshhold voltage.

3.1.1 Threshold Voltage

By solving the two-dimensional (2D) Poisson, we have implemented the model for the threshold voltage in the MATLAB considering different channel lengths.

An analysis concerning the variations on the threshold voltage with the exploitation of strained silicon technology is also reported, following the procedure used in reference [15].And its schematic is shown in figure 3.1.

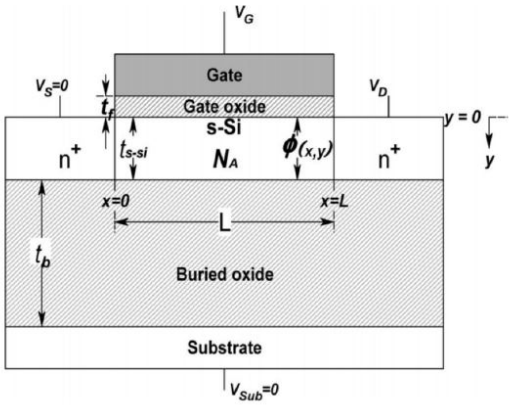

Figure 3.1: Schematic representation of Fully depleted SOI

This latter case is analyzed due to its compatibility with conventional silicon processing and its higher performance in terms of carrier transport properties, and refers to Si epitaxial layers grown on top of relaxed SiGe alloys. This specific model takes into account:

- The effect of strain, in terms of equivalent Ge mole fraction, on the bandgap and flatband voltage
- Short-channel effects
- Strained Silicon thin-film doping
- Strained Silicon thin-film thickness
- Gate work function and other device parameters

We have decided to compute and plot the variations of threshold voltage as a function of gate length, as well as Ge effective mole fraction for a strained Silicon device.As per its definition, the threshold voltage is computed as the value of V_{GS} at which the minimum surface potential $\phi_{s,\min}$ $equals$ ϕ_{th}, the threshold potential. Its explicit formulation is the following:

$$V_{th} = k\left(\frac{-V_{\phi 1}+\sqrt{V_{\phi}^2{}_1-4V_{\phi 2}\xi}}{2\xi}\right) \qquad (3.1)$$

The terms in this equation contain all of the contributions mentioned above, and the details about the procedure can be found in reference [15]. Briefly put:

• strain increases the electron affinity of Si, and decreases both the bandgap and the effective mass of carriers. It also modifies flatband voltage by a factor ΔV_{FB};

• the flatband voltage variation causes the built-in voltage across the source-body and drain-body junctions to change as well;

• the surface potential at the source end takes the value of the built-in voltage, and this becomes important when solving the 2-D Poisson equation;

• the minimum surface potential is set equal to the threshold potential.

The resulting threshold voltage vs. channel length is pictured in figure 3.2. The curve for the non-strained Silicon device has been obtained by setting the Ge mole fraction, x, equal to 0:

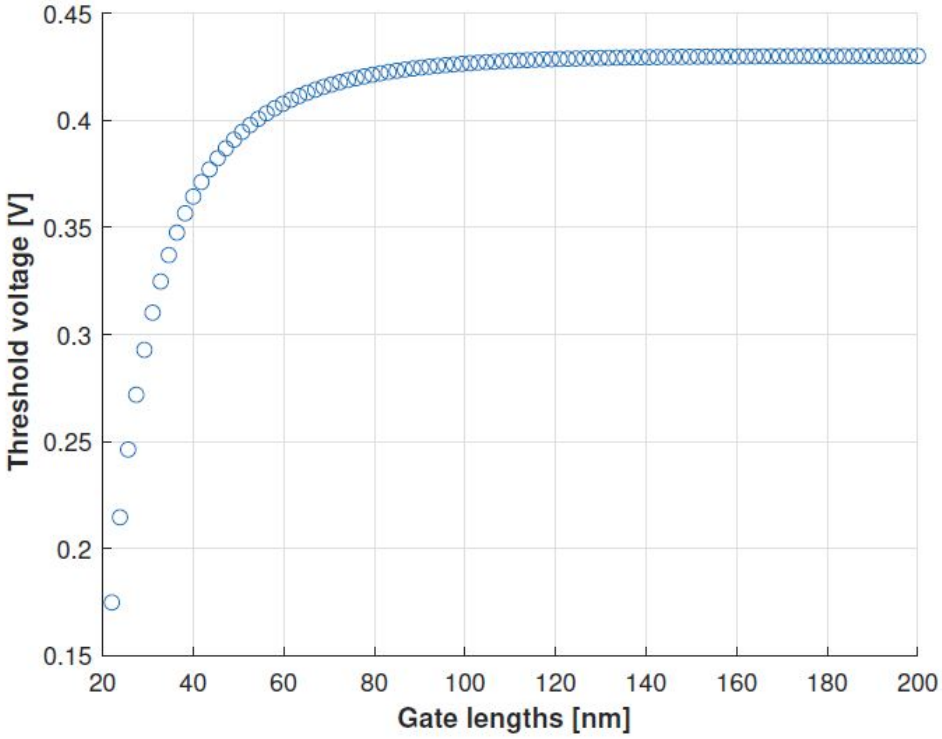

Figure 3.2: Threshold voltage as a function of gate length (Ge mole fraction x=0)

The curves obtained are in accordance with the expected outcome: V_{th} is reduced for values of the channel length lower than 70-80nm, due to short channel effects. Additionally, the threshold voltage is reduced as the strain in the silicon film increases, for a fixed channel length. This is due to the decrease in flatband voltage that stems from the increase of Ge content x.

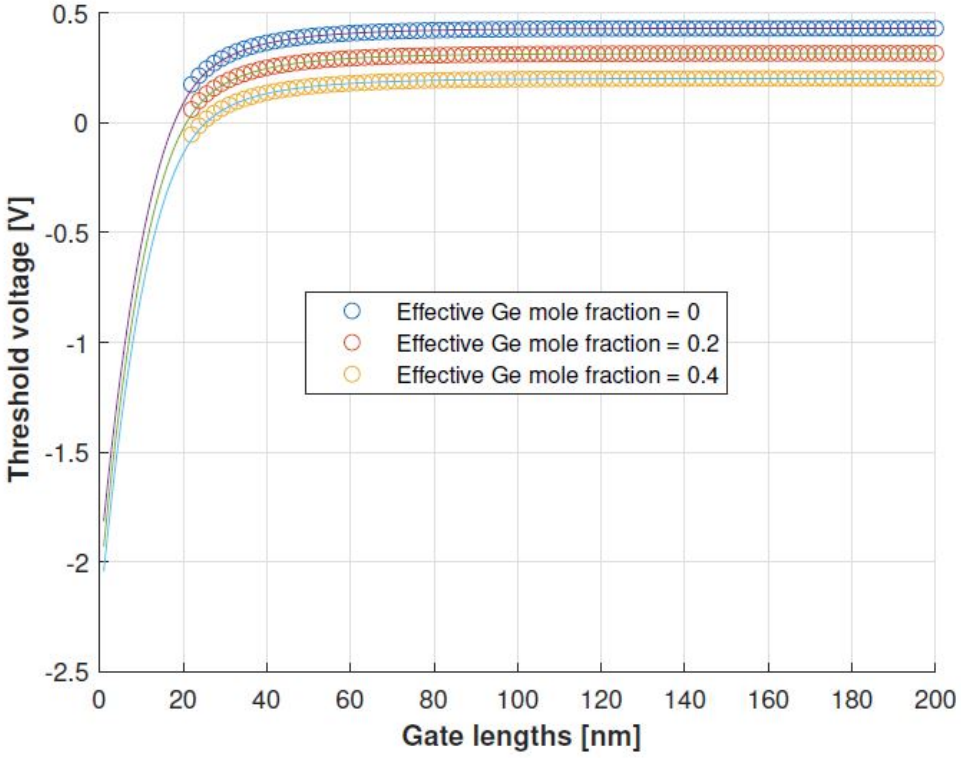

Figure 3.3: Threshold voltage as a function of gate length, for x=0, x=0.2 and x=0.4

3.1.2 Mobility

The mobility is computed in the MATLAB file "Mobility" using the model presented in the reference [16]. This particular model takes into account the Mobility Attenuation Phenomena, which takes place when down-scaling occurs and the transverse electric field increases. This increase in transverse electric field is directly related to the surface roughness of the MOSFET channel, and literature has shown (ref.1 di mob3) that mobility decreases when the former increases. The first order mobility low approximation for not high electric field is given by:

$$\left(\frac{1}{\mu_{eff}}\right) = \left(\frac{1}{mu_0}\right)[1 + \theta_1(V_g - V_t] \qquad (3.2)$$

where 0 is the low gate voltage mobility, θ_1 is mobility attenuation parameter, and finally V_g and V_t are the gate and threshold voltage. Anyway, this approach doesn't

describe in accurate way the devices with short channel length. So we start by defining the carrier distribution in a TMOS inversion layer, in particular,can be describe by the exponential function of the effective electric field:

$$n(x) = n_s.exp(-\beta.F_{eff}.x) \qquad (3.3)$$

with n_s being the surface carrier concentration and $\beta = q/kT$ is the thermal voltage.
It is also possible to define the local average mobility on all the space:

$$\mu_e ff = \left(\frac{\int_0^\infty u_b n(x)dx}{\int_0^\infty n(x)dx}\right) \qquad (3.4)$$

in which μ_b represent the bulk silicon mobility when there is no surface roughness. In our case, considering surface roughness, the mobility (x) vanishes close to the interface, so we can write it as a step function:

$$\mu_e ff = u_b. \exp(-\beta\Delta.F_{eff}) \qquad (3.5)$$

where Δ is the surface roughness amplitude.
From this equation it is possible to notice that the effective mobility has an exponentially decreasing trend due to the effective field and interface micro roughness. The effective field F_{eff} is however a function of the inversion charge Q_i and depletion charge Q_d, in the following way:

$$F_{eff} = \frac{\eta Q_i + Q_d}{\epsilon_{Si}} \qquad (3.6)$$

where ϵ_{Si} is the Silicon permittivity and η is the weighting factor equal to 1/2 for electrons and 1/3 for holes. If we put ourselves in strong inversion condition, meaning above the threshold voltage V_t, we can express the inversion charge Q_i as a linear function of the gate voltage V_g:

$$Q_i \cong C_{ox}(V_g - V_t) \qquad (3.7)$$

This two parameters,θ and μ_0 are directly related to the intrinsic parameters of component. This allows us to express the effective mobility μ_{eff} as:

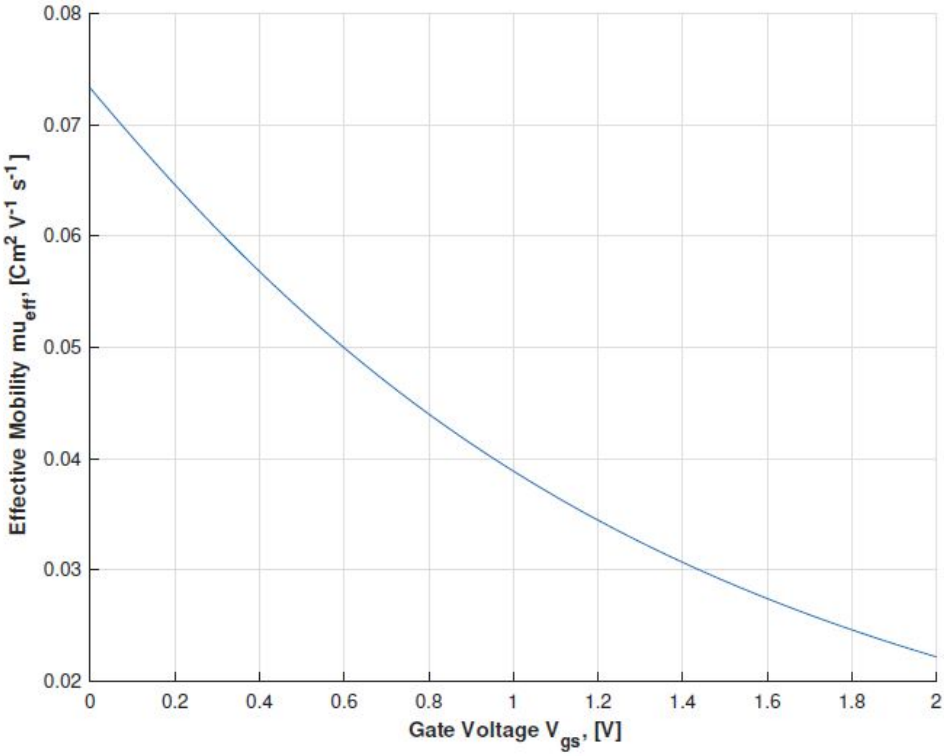

Figure 3.4: Effective mobility vs. the gate voltage

$$\mu_{eff} = \mu_0.exp[-\theta.(V_g - V_t)] \quad (3.8)$$

where $\theta = \beta.\eta\Delta C_{ox}/\epsilon_{Si}$ is the mobility attenuation factor and $\mu_0 = u_b.exp(-\beta.\Delta Q_d/\epsilon_{Si})$ is the low gate voltage mobility. Finally, we can write the expression for the effective mobility, also used in our code, as:

$$\mu_{eff} = \frac{u_b}{exp[\theta.(V_g - V_t)] + \frac{K}{V_d} R_s d(V_g - V_t)} \qquad (3.9)$$

with $K = (W/L)u_0 C_o x V_d$ and V_d is the drain voltage. In particular, the presence of the resistance modify the effective mobility behaviour: it exponentially decrease with the inversion charge, figure 3.4. Beyond the surface roughness scattering events, carrier mobility is affected by three major factors: lattice heating, carrier mobility degradation due to high gate field (as mentioned before) and carrier velocity saturation. Lattice heating assume high importance with respect to the case of bulk mobility, due to the presence of buried oxide that acts as insulator. The dependency of mobility from temperature is expressed as:

$$u_0 = u_a mb(\frac{T_{amb}}{T_0})^Z \qquad (3.10)$$

where μ_0(amb) is the maximum values of the low-field carrier mobility in the inversion channel at temperature T_0 (Tamb). Z is an empirical coefficient which value is in a range from 1.2 to 2. The effect of carrier velocity saturation (vsat) can be calculated as:

$$u_n = \frac{u_{n0}}{1 + \frac{u_{n0}}{vsat} \frac{dV_{CS}(y)}{dy}} \qquad (3.11)$$

3.1.3 Drain to Source Current Ids

We can calculate Drain to Source current from derivations . current by starting from the drift-diffusion model and accounting the total series resistance of the device RT = RS + RD with RS and RD source and drain resistances respectively . From this we will be able to compute the ON (ION) and OFF (IOFF) currents but setting the suitable conditions.

$$I_{ds} = \frac{-P_1 - \sqrt{P_1^2 - 4P_2P_0}}{2P_2} \qquad (3.12)$$

where the parameter are:

$$P0 = H(VGST_{\eta} - \frac{V_{ds}}{2})V_{ds} \qquad (3.13)$$

$$P_1 = -HR_T(V_{GST\eta} - \frac{VdsR_D}{R_T}) - L - \frac{Vds_{n0}}{vsat} \qquad (3.14)$$

$$P2 = \frac{HR_T(R_S - R_D)}{2} + \frac{R_{Tn0}}{vsat} \qquad (3.15)$$

with $H = W_{n0}C_{fox}$,$VGST_{\eta} = VGST - \eta$
In order to find the saturation current Ids,sat, we need to express the drain-to-source saturation potential (Vds,sat) as in term of some parameters reported in the model.

$$Ids, sat = \frac{V_{GST\eta} - V_{ds,sat}}{\frac{n0}{Hvsat} - R_D} \qquad (3.16)$$

The result of this implementation is reported in figure 3.5 where we have decided to show the difference in the current behaviour for different V_{GST} values.

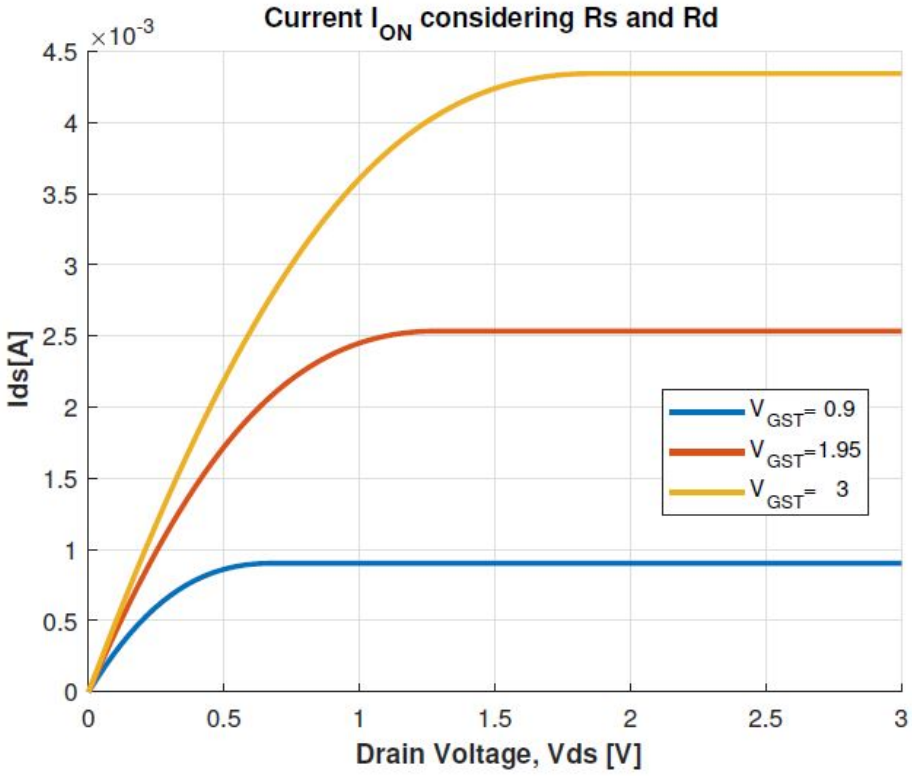

Figure 3.5: Ids current considering different VGST

Just for sake of completeness we have also reported in Fig 3.6 the comparison among $V_{ds,sat}$ calculated using empirical approximation (dotted line) and quadratic solution (solid line). Here it is clearly shown that the empiric approximation maintains a very good agreement with the quadratic solution and thus, being much simpler see equation 3.9, it can be used instead of quadratic expression.

$$V_{ds,sat} = 0.66_{VGST_\eta} + 8\Phi_t \qquad (3.17)$$

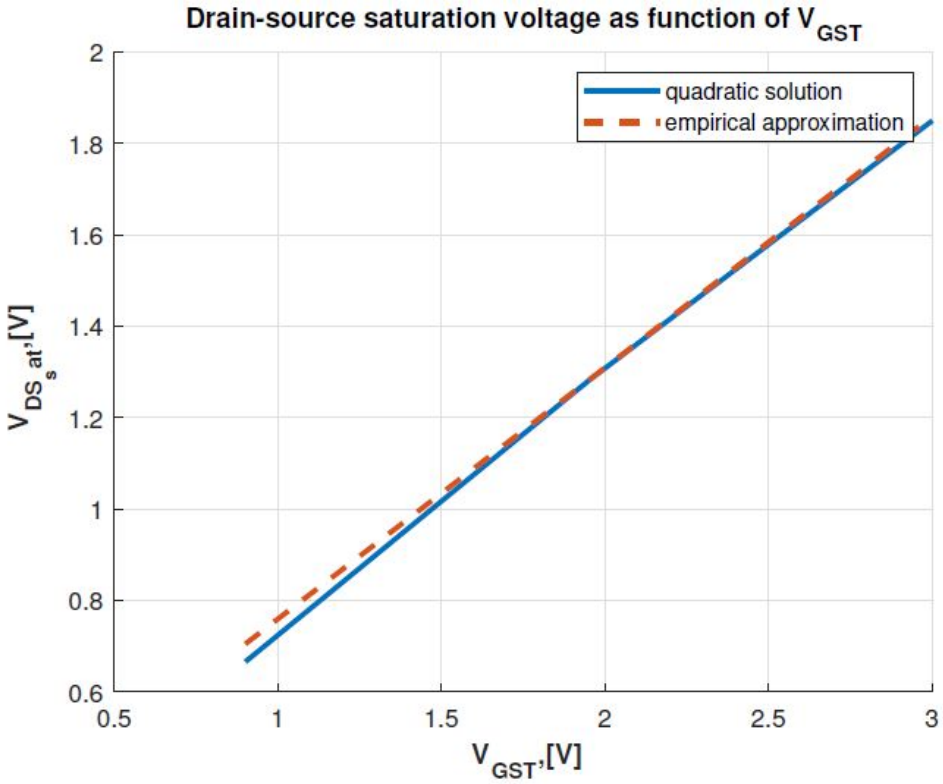

Figure 3.6: Saturation voltage: comparison among the quadratic solution and empirical approximation

Finally, we have included the effect of the parasitic BJT, channel length modulation and impact ionization reaching the expression for channel inversion current:

$$I_{ch} = \frac{I_{ds}}{1+\exp\left(\frac{V_{ds}-V_{ds,sat}}{\Phi_t}\right)} + \frac{I'_D}{1+\exp\left(\frac{V_{ds}-V_{ds,sat}}{\Phi_t}\right)} \qquad (3.18)$$

where I'_D is a function which assumes two different values depending on the working region, i.e. o the value of V_ds. The results are reported in Fig. 2.10 where the solid and dotted lines identify the current obtained with and without considering the parasitic BJT, respectively. It can be noticed that for low values ofV_{GST} the error introduced by neglecting this contribution is negligible but becomes more and more important increasing it. The effect of channel length on the on current is also investigated in Figure. This model well recover the experimental value thanks to its capability to account the main contribution to the overall resistance of the

device. However, some improvement could be done introducing in the treatment other contributions (like the extension resistances). As a final step of this script we have performed the calculation of the subthreshold from [17] slope (SS) obtained from using the formula:

$$S = \frac{K_B T}{q} \ln(10) \left(1 + \frac{1}{C_{ox}} \frac{C_{Si} C_{BOX}}{C_{Si} + C_{BOX}}\right) \qquad (3.19)$$

SS is an indicator of how "quickly" the transistor goes from the subthreshold to the above-threshold region; it is essentially the inverse of the slope of IDS when $V_{GS} < V_{th}$.

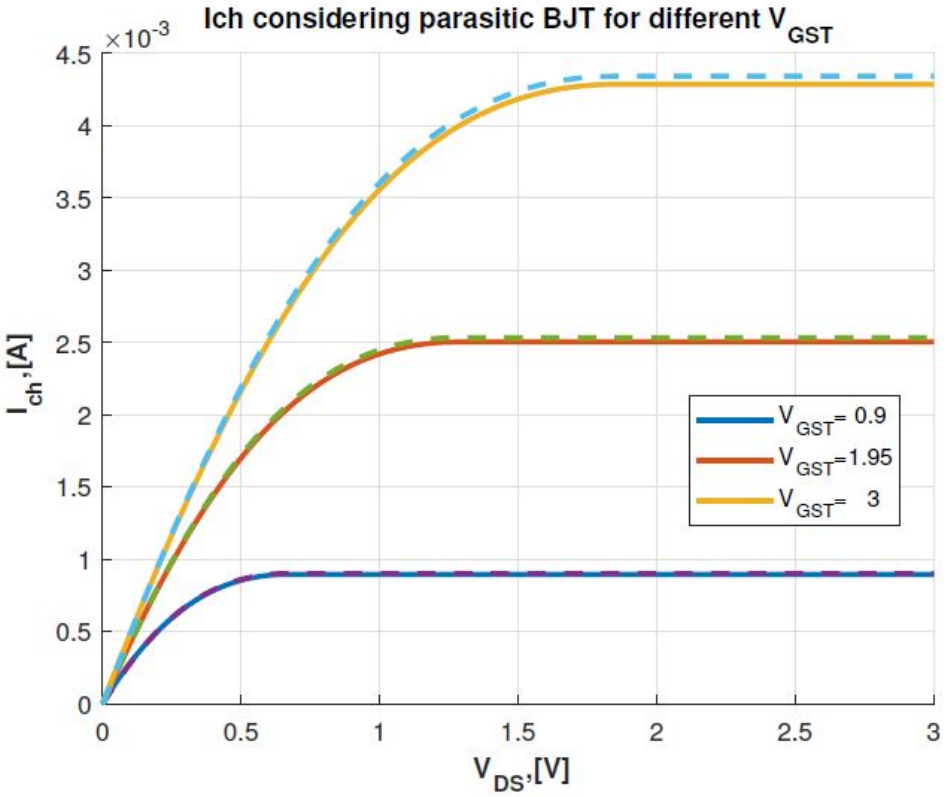

Figure 3.7: Channel inversion current.

Ideally, SS should be as small as possible in order to have the highest slope in the IDS curve, therefore implying a quicker transition between regions. The result is a subthreshold slope $(SS)\ of\ \approx 61 \frac{mV}{dec}$ which is in quite perfect agreement

with the theroy. In fact, we know that thanks to the structure of FD-SOI devices, an almost perfect SS shall be obtained but it is physically impossible go down $\approx 59\frac{mV}{dec}$ dec .

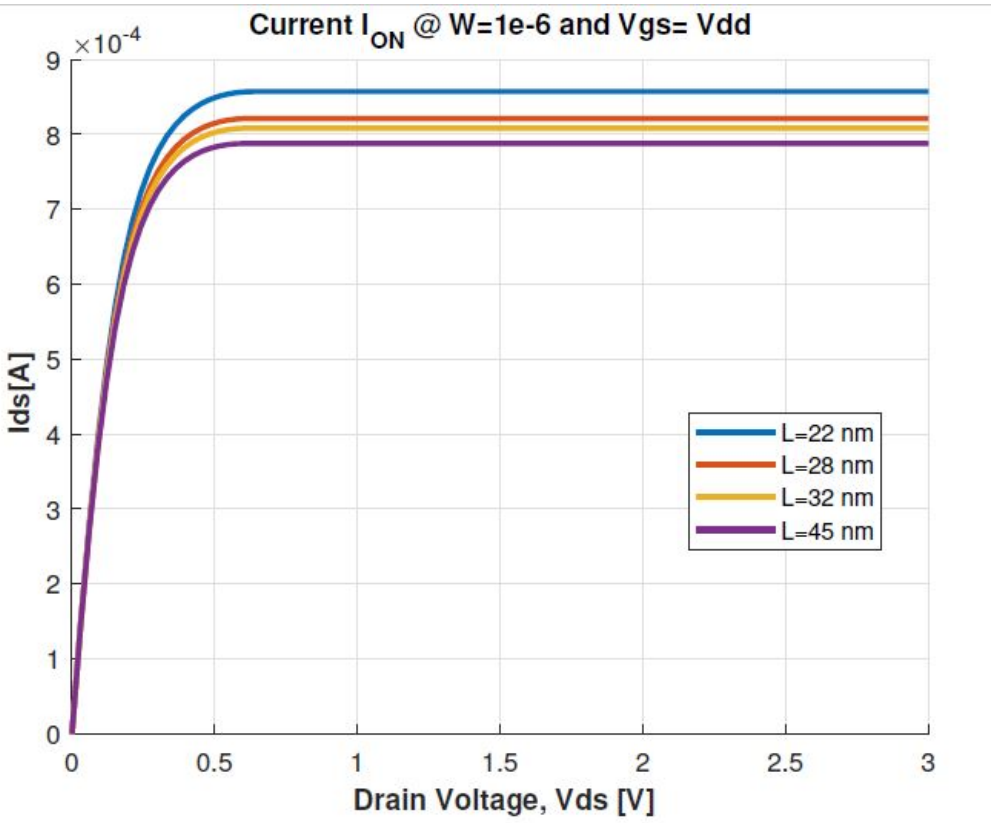

Figure 3.8: Current Ids vs the drain-to-source potential obtained at different channel lengths..

In order to conclude this section we present also the results obtained for the I_{OFF} current. In fact, the I_{OFF} current is defined as the current flowing when $V_{gs} = 0V$ and $V_{ds} = V_{dd}$. Moreover, under some simplifications (like the assumption of $V_{ds>>V_t}$) we can write it as follow:

$$IOFF = \mu_{n0} C_{dep} \frac{W}{L} V_t^2 \frac{\exp(V_{gs} - V_{th})}{mVt} \tag{3.20}$$

The result is reported in Fig. 3.9. The behaviour is linear in logarithmic scale, as expected from the theory but we weren't able to check the values due to lack of

information. However, it seems to be quite reasonable for what seen during Prof. Casu lectures.

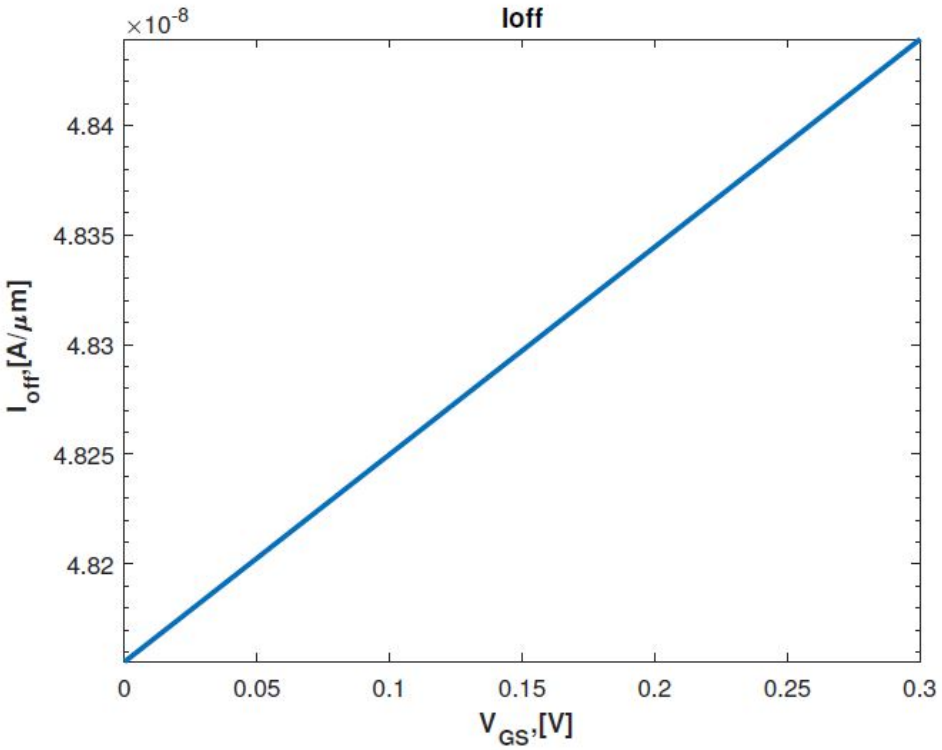

Figure 3.9: OFF current obtained for different Vgs values.

3.1.4 Gate Current

The gate current is an unwanted effect that occurs when charges are able to 'break' the oxide layer. The two main triggers for it are:

- low barrier between semiconductor and oxide, which results in Fowler-Nordhelm tunneling of charges through the oxide and into the gate;
- low thickness of the oxide layer, which allows the charges to go through the oxide by direct tunneling.

Lets start saying that there are mainly two tunneling mechanisms: Fowler-Nordheim and Direct. However, since the focus is on the above threshold region, the trap assisted tunneling (TAT), relevant in sub-threshold, is ignored. This model, extracted from [18] and implemented with the notes of the course (see Piccinini's Handbook), is valid also for devices with channel length lower 20nm (down to 14 nm). The

main parameters to deal with to reduce this effect are therefore barrier height and oxide thickness. In fact, higher is the thickness, lower will be the probability of tunneling by the particles which is expressed as:

$$T = \exp\left\{\frac{4}{3}\sqrt{\frac{2q\mu_{eff}\epsilon_{gs}}{h^2}}\left[\left(-t_{ox} + \frac{\Delta E_c - E_0}{q\epsilon_{ox}}\right)^{\frac{3}{2}} \left(\frac{\Delta E_c - E_0}{q\epsilon_{ox}}\right)^{\frac{3}{2}}\right]\right\} \tag{3.21}$$

where μ_{eff} is the effective mobility computed in preceding section, ΔE_c is the barrier height given at the gate oxide interface, E_0 is the energy of the first electron level due to the quantum confinement,ϵ_{ox} is the electric field across the dielectric and t_{ox} is its thickness.

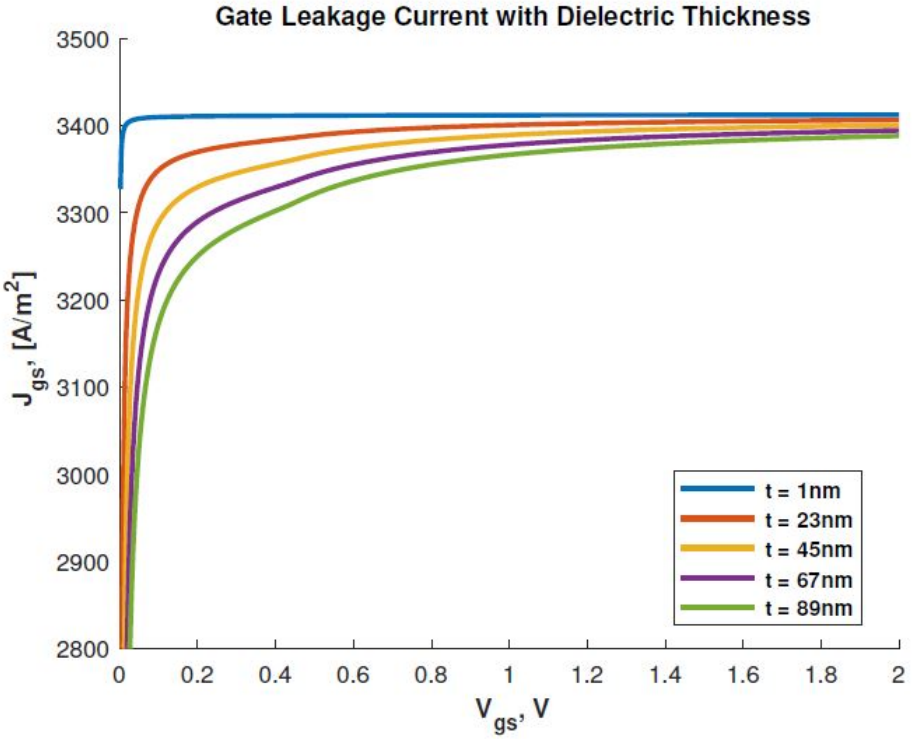

Figure 3.10: Gate current as a function of Vgs.

Now we can compute the gate current density $\left(\frac{A}{m^2}\right)$ using the formula:

$$j_g = fQ_iT \qquad (3.22)$$

where f is the electron escape frequency set to the value of reference. The results are reported in Fig. 3.10 showing the influence o dielectric thickness and gate-to-source voltage on the leakage.

3.2 Modules Integration on TAMTAMS

In figure 3.11 here are results from TAMTAM tool for FD SOI transistors for different technological nodes,like 65nm,22nm,18nm,12nm,10nm.Its clearly seen that when we are going towards short channel width,the On current Ion is increasing.For 65nm Ion is $2.94e^{-4}$ A/um and for 10nm is $4.25e^{-4}$ A/um

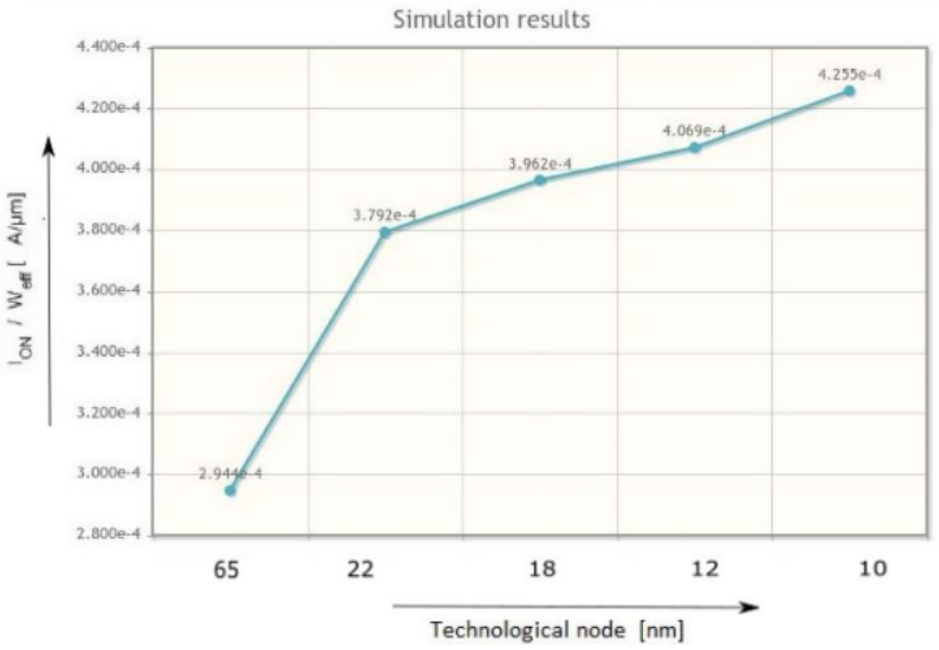

Figure 3.11: On Current for different Technological nodes

In figure 3.12 here are results from TAMTAM tool for FD SOI transistors for different technological nodes,like 65nm,22nm,18nm,12nm,10nm.Off current Ioff is pictured here from TAMTAM simulator.

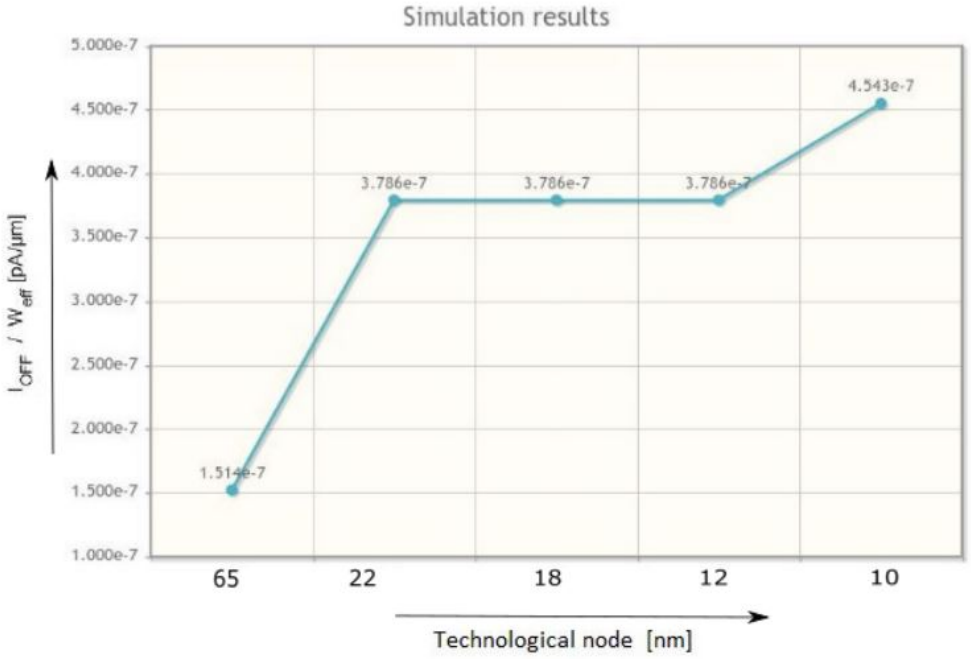

Figure 3.12: Off Current for different Technological nodes

In figure 3.12 we can see results from TAMTAM for Off current.

In figure 3.13 here are results from TAMTAM tool for FD SOI transistors for different technological nodes,like 65nm,22nm,18nm,12nm,10nm.Electron mobility is pictured here from TAMTAM simulator.Electron mobility is decreased for short nodes.

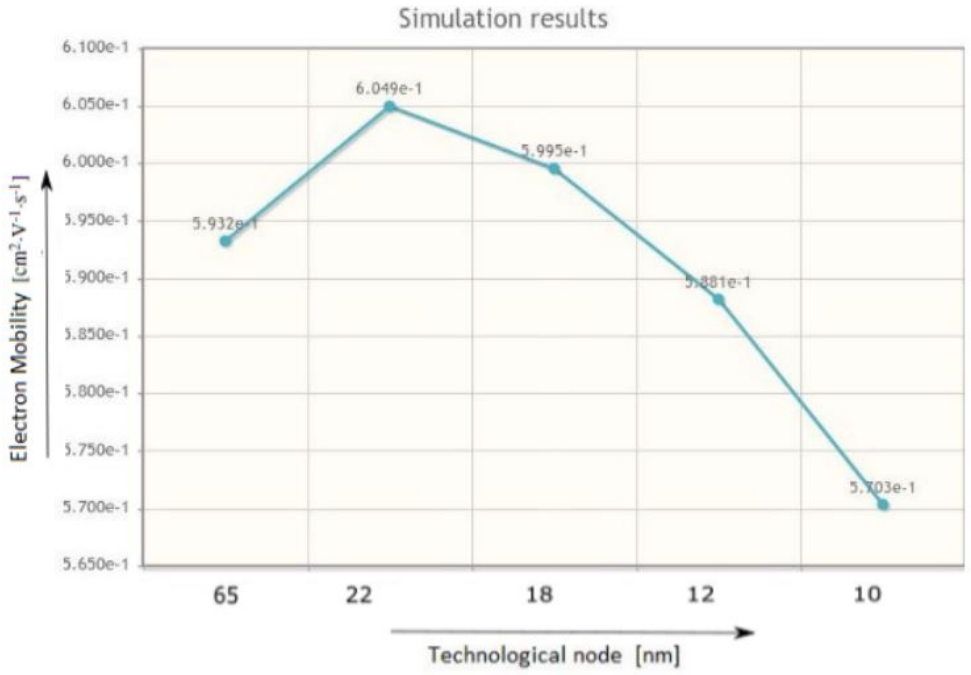

Figure 3.13: Electron mobility for different Technological nodes

In above figure 3.13 Electron mobility is shown from TAMTAM tool for different nodes.We can see that when node is going to be changed so electron mobility is also going to be decreased.For 65nm node mobility is greater than 22nm,18nm,12nm,10nm.For node 10 nm mobility is low.After 10nm , technological nodes are under study.

In figure 3.14 here are results from TAMTAM tool for FD SOI transistors for different technological nodes,like 65nm,22nm,18nm,12nm,10nm.Threshhold voltage Vth is pictured here from TAMTAM simulator.Vth is decreased for short nodes.

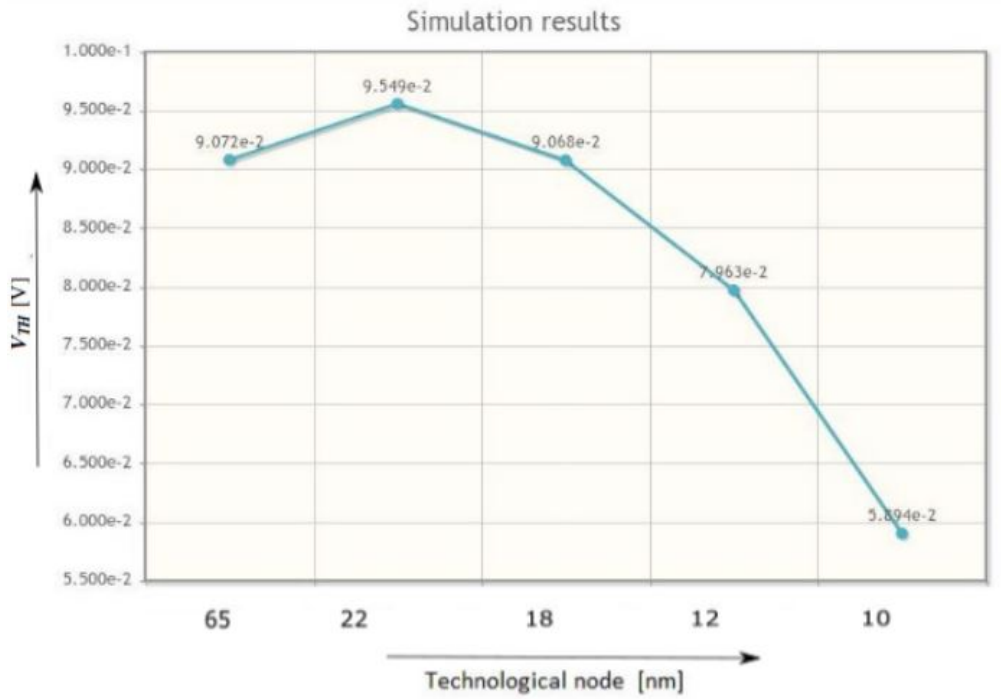

Figure 3.14: Threshhold Voltage for different Technological nodes

In above figure 3.14 threshold voltage is depicted from TAMTAM tool.We can see that when node is going to be changed so threshold voltage is also going to be decreased.For 65nm node Threshold voltage is greater than 22nm,18nm,12nm,10nm.For node 10 nm Threshold voltage is low.After 10nm , technological nodes are under study.

Chapter 4

UTBB FD SOI TRANSISTOR

Fully depleted low-doped channel technology is exploited in sub-20-nm devices due to the fact that excellent electrostatic control can be obtained. Among this kind of device architecture, MOSFETs based on ultrathin body and buried oxide fully depleted silicon-on-insulator (UTBB-FDSOI) technology have two great advantages: they are planar and their architecture is similar to the one used for traditional bulk devices (simpler process with respect to FinFET), and second their performance can be efficiently tuned by applying a bias through the BOX (which enables a dynamic modulation of the speed/power trade-o).A schematic of UTBB FD SOI is shown figure 4.1.

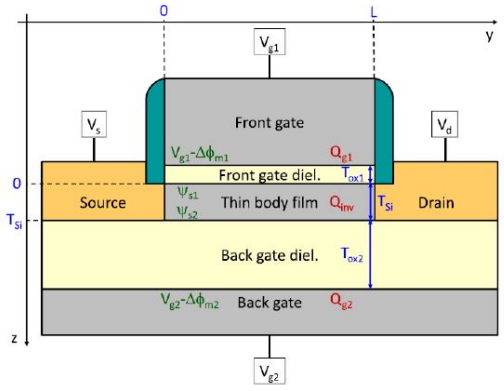

Figure 4.1: Schematic representation of UTBBS Fully depleted SOI

Compact models are needed in order to describe the transistor behaviour on a wide range of back biases, and such models must consider the fact that inversion charge can take place at the back interface of the thin body when applying a strong forward back bias. Analytical computation of front and back interface potentials, efficient and accurate in all cases, is required. Finding a general procedure to determine interface potentials in independent double-gate devices is not immediate, since the nature of the equation set to be solved changes from hyperbolic to trigonometric form, depending on the applied biases. The resolution procedures proposed rely on the numerical res- olution of huge sets of equations, on interpolation functions between the transistor operation regimes,or on approximation of the potential pro

le in the thin body; but they require an a priori calculation of the boundaries between hyperbolic and trigonometric modes, which involves the use of complicated Lambert functions.Here we will describe and implement a model developed by Leti, a technology research institute at CEA Tech, valid for low-doped UTBB transistors. The system under study is the one in Fig.4.1: The main initial input parameters are listed in the table of Fig 1.7, together with their dimensionless counterparts.

4.1 Modules to be integrated for different technological bottoms

4.1.1 Drain Current Modeling

Charge sheet approximation cannot be used for UTBB MOSFETs, since inversion charge centroid can be anywhere within the

lm in transverse direction, depending on the applied voltages and on the position along the channel. As a consequence, the drift component of the current cannot be expressed in terms of front- or back-surface potential gradient, as in bulk transistors.A drain current expression valid in all cases can be obtained by separating the inversion charge in two parts related to the front and back interfaces. To ease the implementation of velocity saturation effect, another approach can be followed, starting from the general drain current equation, in which an effective mobility μ_{eff} is introduced, averaged over inversion charge and along channel length:

$$I_{ds} = -\frac{W_E}{L_E}\mu_{eff}\int_0^{L_E} Q_{inv}(y)\,\frac{d\Phi_{im}}{dy}(y)\,dy \qquad (4.1)$$

Where L_E and W_E are the electrical channel length and width, respectively. Using dimensionless notation:

$$i_{ds} = \frac{I_{ds}}{\left(\frac{W_E}{L_E}\right)\mu_{eff} C_{Si} \phi_T^2} \qquad (4.2)$$

Drift and diusion components can be separated exploiting the equality $d_{qi} = q_i d(\ln(-q_i))$:

$$i_{ds} = \int_{x_s+\ln(-q_{is})}^{x_d+\ln(-q_{isd})} (-q_i) d(x_n + \ln(-q_i)) + \int_{q_is}^{q_{isd}} dq_i \qquad (4.3)$$

From equation 4.3, an effective electrostatic potential is defined, whose gradient governs the drift component, no matter the position of the inversion charge centroid in the thin body:

$$x_{drift} = x_n + \ln(-q_i) \qquad (4.4)$$

The dependence of inversion charge density with this effective potential along the channel is linear in most cases, except when both the front and back interface channels are created at source side and pinched off at different points; in that case, inversion charge density dependence with xdrift presents two dierent slopes (before and after the pinch o of the weakest channel). The principle of inver- sion charge linearization is generalized by approximating the inversion charge density as a smooth and integrable function of two linear dependence values, calculated at source and drain sides. This expression requires as inputs the inversion charge density and of its derivative with respect to x_{drift} at both the ends of the channel.

4.1.2 Drain Current considering velocity saturation

When velocity saturation of mobile carriers is accounted for, the following drain current expression is obtained:

$$I_{ds} = \frac{W_E}{L_E} \frac{\mu_{eff}}{\sqrt{1+\frac{\mu_{eff}\phi_T}{v_{sat}} . \frac{\delta x_{ds}}{L_E}^2}} C_{Si} . \phi_T^2 . i_{ds} \qquad (4.5)$$

Where v_{sat} is the saturation velocity and x_{ds} is the difference of effective electrostatic potential x_{drift} between source and drain. Saturation drain voltage can be

calculated by determining the $\delta_{x_{ds}}$ value for which the drain current given by equation (4.5) reaches its maximum. After the calculation of inversion charge density qis at source side, its derivative ds with respect to eective electrostatic potential, and eective source-drain voltage, we can compute interface potentials, inversion charge density q_{id}, and its derivative d_d at drain side. Then, knowing the value of eective potential $x_{drift,s}$ and $x_{drift,d}$ at the source and drain sides, respectively, the evolution of inversion charge density along the channel is approximated as a function of two values of linear dependence with respect to x_{drift}. Defining:

$$L(x_{drift}) = q_{is}q_{id} + d_d(x_{drift} - x_{(drift;d))} - ds(x_{drift} - x_{(drift;s)}) \tag{4.6}$$

$$Ls = L(x_{drift;s}); Us = \sqrt{L_s^2 + 36(d_d - d_s)2} \tag{4.7}$$

$$L_d = L(x_{_{drift;d}}); Ud = \sqrt{L_d^2 + 36(d_d - ds)^2} \tag{4.8}$$

Inversion charge density is expressed as a function of x_{drift}:

$$-q_i = -q_{im} + \frac{(d_s+d_d)}{2}(x_{drift} - x_{driftm}) + \frac{\sqrt{L_{\left(x_{drift}\right)}^{2}+36\left(d_d-d_s\right)^2}}{2} - \frac{U_s+U_d}{4} \tag{4.9}$$

With $q_{im} = \frac{(q_{is}+q_{id})}{2}$ *and* $x_{driftm} = \frac{\left(x_{(drift;s)}+x_{drift;d}\right)}{2}$ equation (4.9) is written in such a way that q_{im}, mean value between q_{is} and q_{id}, is exactly preserved despite the approximation made on $qi(x_{drift})$. Equation (4.9) can be analytically integrated against x_{drift}.

$$i_{ds} = \left(\left(-q_{im} - \frac{U_s+U_d}{4}\right)\delta_{x_{ds}} + \frac{L_dU_d-L_sU_s}{4(d_d+d_s)} + 9\left(d_d - d_s\right)\right)\ln\left(\frac{L_d+U_d}{L_s+U_s}\right) - \left(q_{is} - q_{id}\right) \tag{4.10}$$

Introducing equation (4.10) into equation (4.5), gives the final drain current model, valid in all the bias configuartion.

4.1.3 Mobility

In our model, we considered only one eective mobility in the entire channel, but it is possible to encounter the case where two channels with dierent eective

elds can coexist at front and back interfaces, thus the repartition of inversion charge between the interfaces is not symmetric. If one would want to consider two different effective mobilities in the two channels, from known front- and back-gate charge densities q_1 and q_2, the following dimensionless quantities corresponding to the positive value of surface transverse electric fields are obtained:

$$e_{surf1} = 2.\ln(1+\exp(\tfrac{k_1q_1}{2})); e_{surf2} = 2.\ln(1+\exp(\tfrac{k_2q_2}{2})); \tag{4.11}$$

Then, the fractions r_1 and r_2 of inversion charge at the front and back interfaces can be expressed, respectively, as:

$$r_1 = \frac{e_{surf1}}{e_{surf1}+e_{surf2}}\ , r_2 = \frac{e_{surf2}}{e_{surf1}+e_{surf2}} \tag{4.12}$$

At the end, front- and back-channel mobilities, are combined together by considering the two channels as conductors in parallel:

$$\mu_{eff} = r_1\mu_{eff1} + r_2\mu_{eff2} \tag{4.13}$$

4.2 Module Integration on TAMTAMS

In figure 4.2 here are results from TAMTAM tool for UTBB transistors for different technological nodes,like 24nm,20nm,18nm,10nm .On current Ion can be seen that its greater in short node 10nm relative to 24nm.

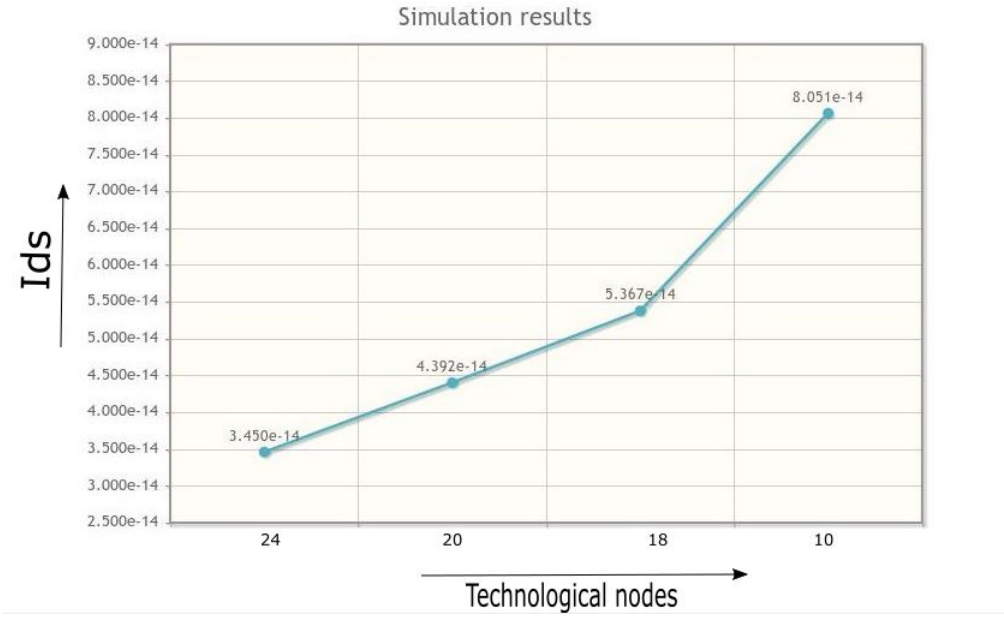

Figure 4.2: Drain to source current for UTBB

Chapter 5

Tunnel Gate Field Effect Transistor

This chapter offers analytic model to describe the current of a Single Gate n-TFET (SGTFET) based on the Kane-Sze for the tunneling current,and Double Gate Tunnel FET.

Firstly For (Single Gate Tunnel FET)After a brief introduction on the working principles of the TFET, this model will be compared to the result obtained in the Praveen model described in [19], taken from [20] for what concerning the current behaviour and furtherly some figures of merit will be highlighted in order to be compared to the traditional FET. In addition a parametric analysis is performed to describe the influence of temperature and gate oxide on the device. In conclusion some hints will be given to improve the TFET structure and optimize its characteristics.

5.1 Single Gate Tunnel Field Effect Transistor

The unstrained downscaling of electronics led to more and more performant circuit and devices, but with the urgent need for power dissipation reduction. In the last years new devices entered in play: one of them is the Tunnel Field Effect Transistor (TFET), proposed to overcome conventional MOSFET limits and able to offer lower power consumption. The difference between the two devices is that, even though the structure is the same of the MOS, the source and drain terminals are doped of opposite type. This gives rise to the so called Band-To-Band Tunneling (BTBT) when a gate bias is applied. The TFET exploits this effect because it can be seen as a gated p-i-n diode in reverse bias where, under a gate a bias applied to the gate terminal, the conduction band edge of the source shifts below the valence

band of the channel creating the so called tunneling window DF or qVTW, that allow the electrons tunneling current (Zener tunneling). This current is modelled by the transmission probability across the tunneling barrier that can be described by theWentzel-Kramers-Brillouin (WKB) approximation , that approximates the barrier in the ON state as a triangle of height equal to the energy gap EG and width equals to the parameter l (also called screening l). The TFET exploits band-to-band tunneling instead of thermal injection of electrons and this allows to break the limit of the 60mV=dec in the subthreshold swing of the conventional MOSFET. This is a promising device but still it is not developed and many studies are still in progress to find how to improve its characteristics: MOSFETs are still better devices whereas high currents are needed and up to now TFETs are not able to reach high ON currents keeping a very low OFF current.

5.1.1 Drain Current modeling by Kane-Sze and a comparison with Parveen model

The TFET device exploits the gate control to push the conduction band of the source below the valence band of the drain, allowing for Band-To-Band Tunneling (BTBT) through the narrow potential barrier given by the quasi-intrinsic layer. The difference between the drain VB and source CB is called tunneling window, qVTW. The main expression that describes the phenomenon is the band-to-band tunneling Zener equation for p-n junctions [21]. Then the expression is completed by adding the dependence of the tunneling window on the gate bias and a dimensionless factor f to account for the superlinear current onset in the output characteristic. A characteristic of the TFET is the decrease of the Subthreshold Slope (SS) with decreasing drain current: the model assumes that this is caused by exponential bands tail (Urbach Tail) due to lattice imperfections (impurities, dopants and phonons), that imposes a limit to the SS achievable [**e6**] and [22]. These last effects are not included in the model. The model describes a n-TFET with gate length of 20 nm and first obtains the $I_D - V_{GS}$ characteristic to be compared with the one from Praveen model [20], then it calculates the behaviour of the current at different temperatures. Relevant parameters concerning the subthreshold current are later calculated and the output characteristic will be shown. In the end it will be performed an analysis of the current with different gate oxides and of the gate capacitance. The model describes the current in a p+-n+ junction integrating the product of the charge flux and the tunneling probability, calculated with the WKB approximation, in the tunneling window, according to the Kane-Sze formula:

$$I_D = W t_{ch} a f V_{TW} \xi \exp\left(-\frac{b}{\xi}\right) \qquad (5.1)$$

Figure 3.1 shows the transcharacteristic of the TFET implemented with this model compared with the Praveen model curve: the two models are computed using H fO2 as gate oxide, setting the threshold voltage at 0:35V and the drain voltage at 1 V, at a temperature of 300 K, (hereinafter these will be the default settings).

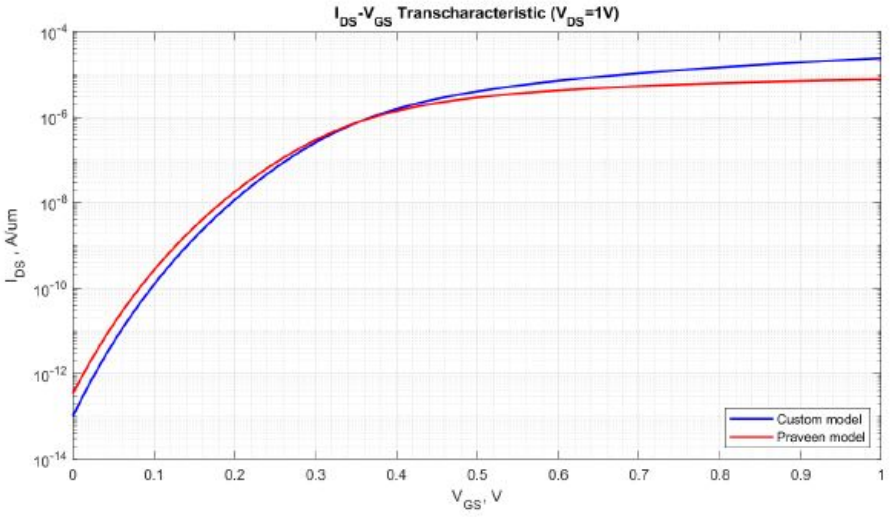

Figure 5.1: Transcharacterstics with Parveen Model

figure 5.1 shows the same plot highlighting the average subthreshold slope, built taking the straight line through the points $I_D(V_{TH}$ and $I_D(0)$. As it can be seen, the SS is not constant in a TFET, since it depends on the gate bias: the tunneling window continuously reduces by reducing VGS and so does SS. Therefore the average SS value is the slope of the dotted lines, computed as:

$$SS_{av} = \frac{V_{TH}}{\log_{10}\left(\frac{I(V_{TH})}{I(0)}\right)} \qquad (5.2)$$

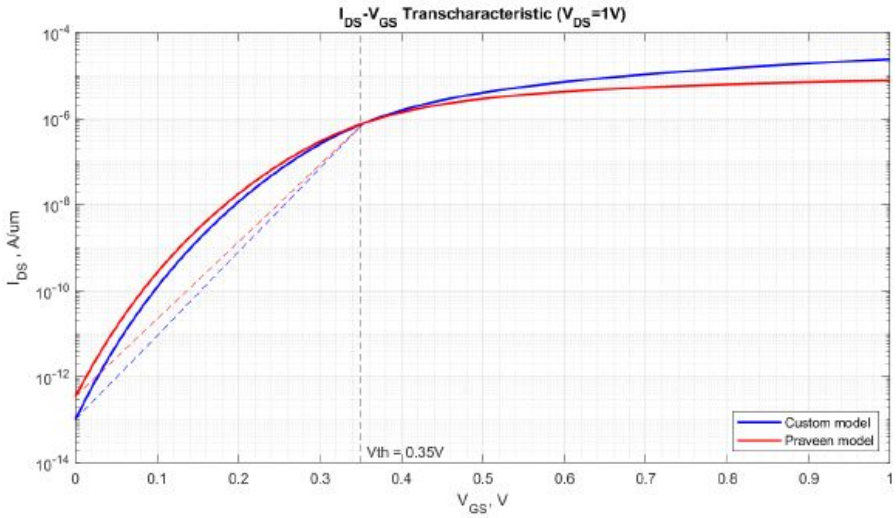

Figure 5.2: Transcharacteristic and SS, comparison with Praveen model.

The custom model seems to be more performant than the Praveen model, probably due to the choice of different fitting parameters: both models show a subthreshold slope below the physical limit of $\frac{60mV}{dec}$ of the classical MOSFET and the custom model has a SSav smaller and a $\frac{ION}{IOFF}$ ratio one order of magnitude higher than the Praveen model. The next plot describe the behaviour of the custom model trans characteristic varying the temperature in figure 5.3 and the gate oxide in figure 5.4.

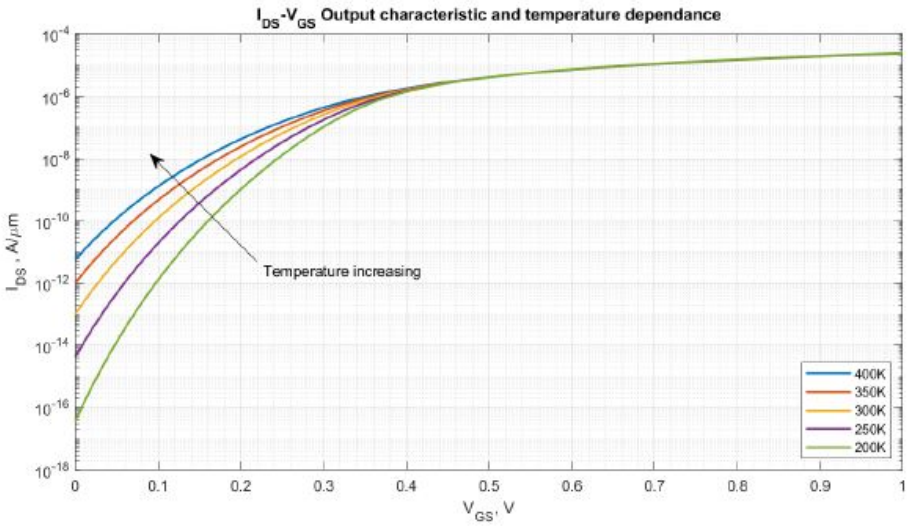

Figure 5.3: Transcharacteristic and temperature variations.

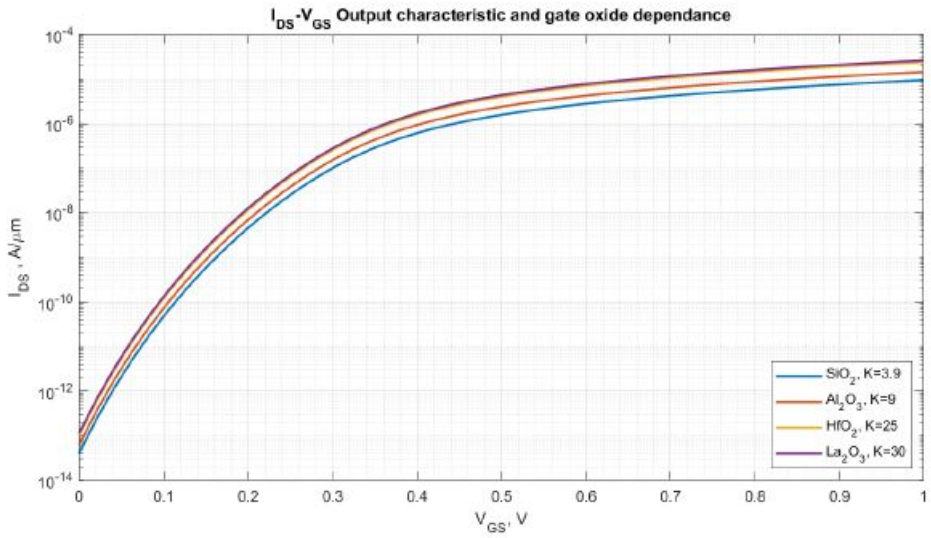

Figure 5.4: Transcharacteristic and gate oxide.

It can be seen that the temperature affects only the subthreshold current since the tunneling mechanism in the ON state does not depend on temperature, while in the OFF state I_D is constituted by a leakage current,and its change with temperature is mainly contributed by thermal generation in the depletion region [11]. For what concerns the gate oxide, it can be seen that by choosing an higher-K material both ION and IOFF increase keeping the same ratio. This behaviour is due to the increased gate capacitance with higher-K material, and so due to better electrostatic control of the current. The next plot shows the output characteristic I_D as a function of V_{DS} for different values of V_{GS} from 0V to 1 V.

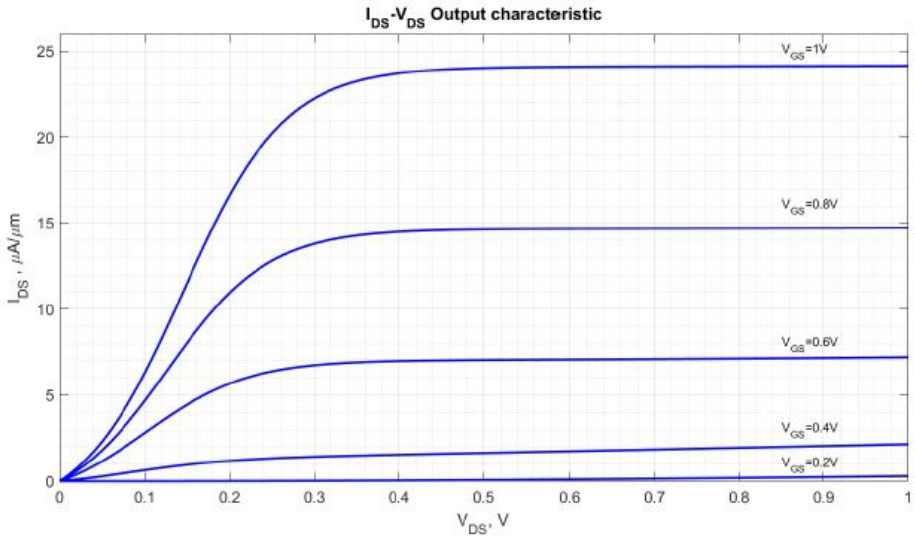

Figure 5.5: Output characteristic.

5.1.2 Analysis of Capacitance between Gate and Inversion Layer Cgd

C_{GS} and C_{GD}; the curves are normalized to C_{GG}. The curves correspond to values of V_{DS} from 0V to 1V with step of 0:2 V. In this model the C_{GS} is considered constant because it is much smaller compared to C_{GD} and is dominated by interconnect capacitance. In a traditional MOSFET the inversion layer is roughly uniformly distributed along the channel and therefore the gate capacitance halves among source and drain region. In a TFET only the drain is connected to the inversion layer and the partitioning of the capacitances is different: before inversion occurs (low V_{GD} or negative V_{GD}), C_{GD} or C_{GS} comprises parasitic capacitance components (not shown). After the inversion layer is formed underneath the gate dielectric, C_{GD} is dominated by the capacitance between the gate and the inversion layer. At a fixed V_{DS}, the inversion layer is first formed near the drain side at lower V_{GS}, and it extends toward the source with increasing V_{GS}. For a given gate bias in ON-state, increasing V_{DS} pinches the TFET inversion layer off at the source side, in contrast to a MOSFET where the pinch-off occurs at the drain side [12].

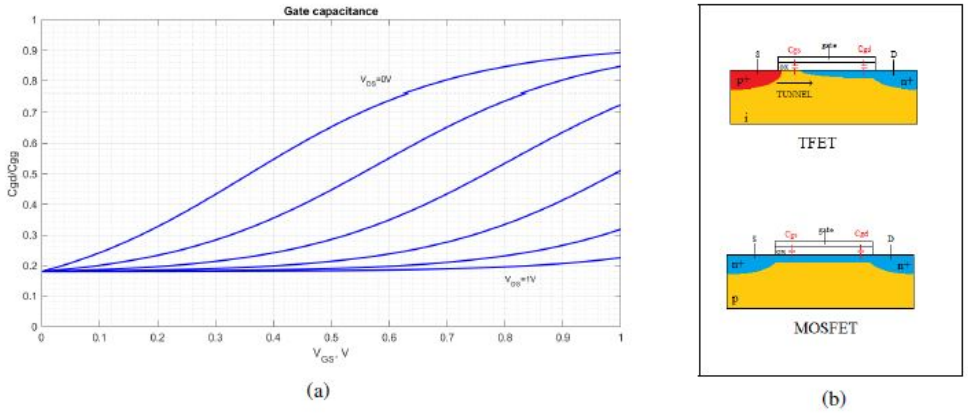

Figure 5.6: Left: gate capacitance in a TFET. Right: depletion region in TFET and MOSFET

5.2 Double Gate Field Effect Transistor

In the last years, the scaling of the MOSFET technology has experienced a boost reaching dimension of the order of the nanometer. In such conditions the management of power becomes one of the main challenges to overcome. Further scaling of MOSFET gives rise to a number of issues such as gate tunnel current, parasitic effects, short channel effects, increase in the leakage current and low value of the ON to OFF current ratio. All those effects contribute to the high level of static power consumption, even in the OFF operation condition. In a low power electronic device, such conditions must be at least minimized such that alternative designs to the traditional MOSFET are required to increase the performances of the device. Tunnel Field effect transistors (TFET) have been deeply investigated as a valid alternative to MOS-FETs for low power digital applications in order to overcome the scaling limitation of standard CMOS technology.A very useful figure of merit, used to describe the switching capability of logic gates, is the so called subthreshold slope, defined as the slope of the linear region of the $log(Ids)V_{gs}$

It is customary to express this parameter in terms of subthreshold swing, defined as the inverse of the subthreshold slope

$$SS = \frac{1}{subthreshold\ \ slope} = \lceil \frac{mv}{dec} \rceil \qquad (5.3)$$

The smaller the SS, the lower is the amount of power required by the logic gate to perform a switch.

In MOSFETs, due to physical limitations related to charge diusion mechanism (in OFF state, i.e. Vgs < Vth, the only contribution to the overall current comes from diffusion of carriers from source and channel) and to Boltzmann Statistics, SS has a lower boundary approximately equal to 60 mv/dec. Furthermore, the channel length scaling heavily effects the performances of the MOSFET due to the arise of short channel effects (SCEs), such that the SS_{min} becomes an ideal value. Since a TFET has a completely different mechanism of charge injection into the channel, the limit of SS calculated for MOSFETs does not hold anymore. In fact, while in MOSFET the action of the gate shifts the bands below it, allowing for thermionic emission of charges from the source to the channel, in a TFET the band shifted below the gate is engineered in order to allow a strong quantum tunneling from the source to the channel. As a consequence, for values ofV_{gs} below the threshold, the output current I_{off} results to be several orders of magnitude lower with respect to the MOSFET's one; on the other hand, the tunneling mechanism limits a lot the drain current in the ON condition, such that the maximum Ion achieved so far in thus kind of devices is significantly lower than the one measured in MOSFETs.

If we talk about TFET Structure so ,the simplest TFET structure is composed by a p-i-n junction in which the gate terminal is in charge of controlling the carriers injection through a band-to-band tunneling mechanism. A n-type TFET has a p-doped source and a n-doped drain, while the region controlled by the gate terminal is intrinsic; the opposite holds for p-TFET, as summarized in fig The channel is intrinsic or lightly doped, with typical lengths lower than 50 nm, thus allowing for considering the carriers transport in the channel in the ballistic approximation. As a consequence of the very small dimensions of the system, a quantum theory should be used rather than a classical one to describe the transport mechanism in TFETs. In a quantum-mechanical description of electronic bands in semiconductors, the current owing in the device is proportional to the tunnelling probability. The main mechanism that governs the operation of a TFET is the interband tunnelling, that in case of a nTFET allows an electron in the source to pass from the valence band to the channel conduction band indeed by tunnelling. The main advantage of TFET is the suppression of the tails of the carriers distributions due to the high energy barrier that carriers see from source/drain to the channel. This mechanism of tails suppression allows for a strong reduction of leakage current, with a consequent increase in the subthreshold slope that appears to be ideally non related to $\kappa_B T$.The operation region is controlled by the gate voltage which is responsible of the switching of the device. In the OFF state (Vgs = 0 V) the tunneling path from the source into the channel is exponentially suppressed by the long tunneling distance, while in the ON state the BTB tunneling probability is exponentially enhanced allowing for the passage of carriers from the source into the channel. In the case of an n-TFET, by increasing the gate voltage (Vgs > 0

V) the channel conduction band is brought below the valence band of the source and band-to-band tunnelling (BTBT) is allowed. The p-type TFET has a dual behaviour: by applying a negative gate voltage the channel valence band is pushed above the source conduction band and BTBT starts. By applying a potential dierence between drain and source a drift current ows into the device allowing for conduction.

Since BTBT is the main carrier injection mechanism, the energy band gap of the semiconductor used for the TFET is a crucial parameter and it has to be properly engineered in order to enhance the ON current and increase the performances of the TFET. As a consequence, narrow band gap materials are preferred. Silicon is the most widely used semiconductor in electronic devices, but its wide and indirect band gap (Eg = 1:12 eV) makes it not suitable for a TFET device. On the other hand, InAs has a very small (Eg = 0:35 eV) and direct band gap, so that phonon-mediated processes are not required.

In the following sections, we will present three models used to implement some simulations on a double-gate tunnel FET (DG TFET). The

rst one, namely the Hao Lu model, is the simplest and most used one. It is based on some

tted parameters included in rather basic and common formulas for tunneling. Its main issue, as it will be better described in section 2.1, is that the parameters are

tted for a given channel length. We were not able to

nd a way to

t the needed parameters for gate lengths dierent from the ones already evaluated in literature. As a consequence, it has revealed useless when dealing with dierent technological nodes. Therefore, our work has proceeded towards the search of more sophisticated models, from which extract the quantities required to fully describe each technological node. Thus, in sections 2.2 and 2.3, we present two alternatives that look appealing as analytic models for DG-TFETs. As described, however, sometimes we were not even able to re- produce the results presented in the corresponding papers, so it was not possible to perform a proper analysis of other technological nodes.

5.2.1 Hao Lu model

As mentioned before, currently the most used analytic model used for the circuital description of TFETs is the one developed by Lu et al. (2015) [3]. The model is simply based on the Kane-Sze formula and it is exploited to evaluate the current-voltage characteristic of such devices. The main advantage of the model relies in this exibility, since the description can be applied to all the different gates configurations (single gate, double gate, gate-all-around). In particular, since TFET working

principle is based on tunnelling current through the source to the channel (as clear from

g. 1.3), Hao Lu model is based on the Kane-Sze expression of the current in a tunnel junction. In such a framework, the current owing from source to drain is calculated by integrating the product between the charge flux and the tunnelling probability in the tunnelling window qV_R (with V_R equal to the reverse bias applied to the tunnel junction allowing for tunnelling of carriers), thus obtaining:

$$J_D = aV_R\xi \exp\left(-\frac{b}{\xi}\right) \qquad (5.4)$$

where qV_R is the reverse bias range applied between the drain and source terminals over which the tunneling occurs, ξ is the maximum electric field in the reverse biased junction, and the two parameters a and b are coefficients describing material properties of the junction and can be calculated as:

$$a = \frac{q^3}{8\pi^2\hbar^2}\sqrt{\frac{2m_R^{\cdot}}{E_G}} \qquad (5.5)$$

$$b = \frac{4\sqrt{2m_R^{\cdot}}E_G^{\frac{3}{2}}}{3q\hbar} \qquad (5.6)$$

where $m_r\cdot = \left(\frac{1}{m_e^{\cdot}} + \frac{1}{m_h^{\cdot}}\right)^{-1}$ is the reduced eective mass, EG is the energy gap of the semicon- ductor, is the reduced Plank's constant. Tunnelling probability is described in the WBK (Wentzel- Kramers-Brillouin) approximation, which means that the tunnelling process has been approximated by a particle tunnelling through a triangular barrier, whose slope is given by the quantity qE. In the Hao Lu model, the Kane-Sze formula already described in equation equation 5.4 formula is modified by splitting VR into two contributions. A dimensionless factor f which includes information about both the current onset and saturation versus the drain-source voltage V_{ds} and that is proportional to the Fermi function taking into the occupancy probability of the filled states in the valence band and the unfilled states in the conduction band; and the tunnelling window V_{tw}, in V , related to the crossing of the energy bands, thus taking into account the energy regions where tunnelling could occur:

$$J_D = afV_{tw}\xi \exp\left(-\frac{b}{\xi}\right) \qquad (5.7)$$

Furthermore, the maximum electric field E is assumed to be linearly dependent on the gate-source bias and drain-source bias:

$$\xi = \xi_0(1 + \gamma_1 V_{ds} + \gamma_2 V_{gs}) \qquad (5.8)$$

where the parameter ξ_0 is the built-in electric field at the source-channel junction at zero bias applied between both gate and drain terminals, while 1;2 are two fitting parameters. The first limitation of Hao Lu model actually is due to the latter parameters. In fact, they cannot be computed starting from some physical constants or from material parameters; on the contrary, they are purely mathematical quantities obtained for specific values of gate length. In fact, these are no more valid when moving to smaller Lg, meaning that a fitting on the values of the electric field needs to be performed before moving to the new technological node. Furthermore, it is straightforward to notice that as the gate voltage is increased the electric field increases as well, leading to two effects: the voltage drop at source-channel junction is enhanced compared to the built-in voltage and the tunnelling barrier region is reduced, narrowing the distance between the conduction and valence band edges. Similarly, by increasing the drain-source bias the eect is the same and the electric

eld increases as well, but the relative increase is smaller compared to the one obtained by tuning the gate voltage, because of the screening effect of the gate on the drain field. The second new term appearing in the Hao Lu current formula is the tunnelling window Vtw, which takes dierent definitions according to the working region the TFET is working into. In particular, in the subthreshold region it can be expressed by

$$V_{tw} \approx U \exp\left(\frac{Vgs - Vth}{U}\right) \qquad (5.9)$$

where U is the Urbach factor, defined as

$$U = \gamma_0 U_0 + (1 - \gamma_0) U_0 \left(\frac{V_{gs} - V_{off}}{V_{th} - V_{off}} \right) \qquad (5.10)$$

$$U0 = \frac{n k_B T}{q} \qquad (5.11)$$

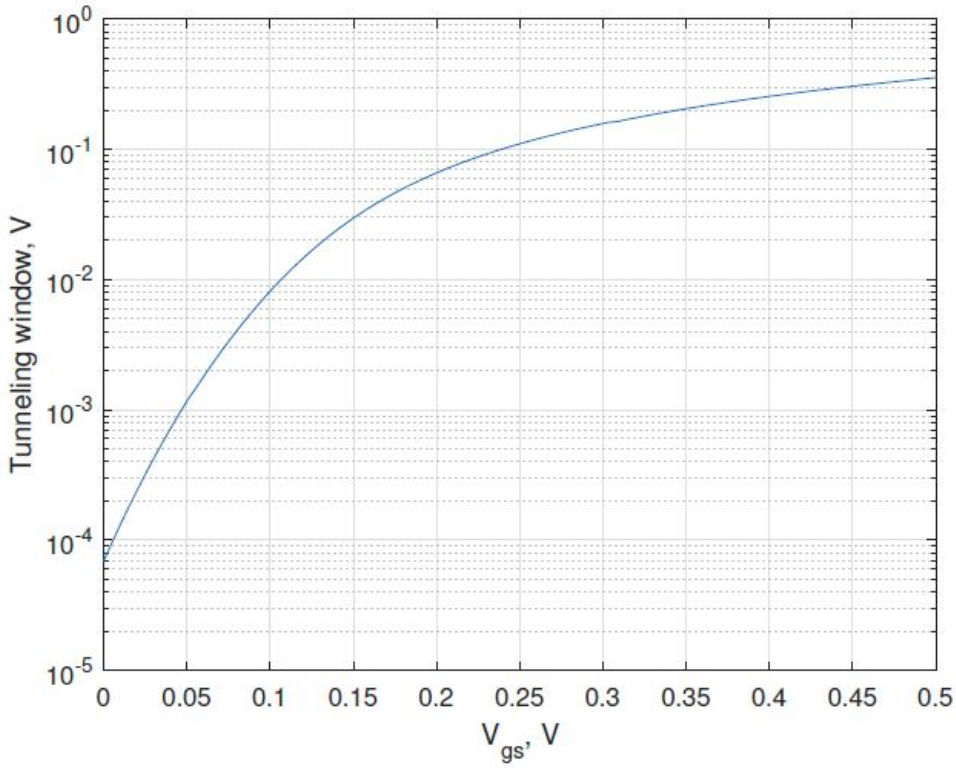

Figure 5.7: Tunneling window as a function of Vgs

The parameter γ_0 controls how fast the tunnelling window reduces with gate bias, n is the subthreshold ideality factor, Voff is the minimum Vgs for which equation (5.10) is still valid, Vth is the threshold voltage, namely the Vgs at which the maximum of the valence band in the source is equal to the minimum of the conduction band edge in the channel (for an n-channel TFET). Expression (5.10) makes the subthreshold swing (SS) to decrease linearly with the gate bias. Again, Voff , Vth and n all come from a fitting process performed for Lg = 20 nm, and

are no more valid for different gate lengths.On the other hand, in above-threshold conditions the tunneling window becomes linearly dependent on gate bias, meaning that drain current is directly controlled by Vgs:

$$Vtw \approx V_{gs} - V_{th} \qquad (5.12)$$

For this reason, Vtw can be called overdrive voltage in this operating region. Eventually, a definition of the tunneling window is required to connect the sub and above-threshold conditions smoothly. As suggested by Hao Lu, a good choice is the following:

$$V_{tw} = U \ln\left(1 + \exp\frac{V_{gs}-V_{th}}{U}U\right) \qquad (5.13)$$

Tunneling window dependence on gate voltage is plotted in fig it is clear that in subthreshold regime it shows an exponentially decreasing behaviour with the gate-source voltage, while above threshold it tends to a linear dependence on V_{gs}.The last term to define to have a complete description of the Hao Lu current formula (5.7) is the f parameter. Taking into account the dependency on the Fermi statistics and including the saturation effect of the drain current, it can be calculated as follows

$$f = \frac{1-\exp\left(-\frac{V_{ds}}{\Gamma}\right)}{1+\exp\left(\frac{\lambda\tanh(V_{gs}-Voff)-V_{ds}}{\Gamma}\right)} \qquad (5.14)$$

where Γ and λ are constant factors expressed in units of volts depending on the structure and of the materials.
The main limitation of the Hao Lu model described in this section is that all the parameters appearing in the model are strictly dependent not only on the materials but also on the considered technological node (so on the channel length) and on the doping levels. For this reason new models are required in order to investigate the behaviour of a tunnel FET at different channel lengths.Before moving to the study of alternative models for TFET analysis, results obtained by using Hao Lu model [3] are reported in this section in order to test its validity for a channel length of Lg = 20 nm. The analyzed structure is an InAs-based double gate n-type TFET.

InAs is characterized by an energy gap of Eg = 0:354 eV and a reduced effective mass$m_r^* = 0.0218.m_0$. As a consequence, the BTBT parameters take the following values: a = 99:2523 and b = 33:81 MV/m. The drain and the source doping levels are symmetric and equal to $ND = NA = 1.10^{20} cm^{-3}$, while the channel doping concentration is very shallow and set to $1.10^{15} cm^{-3}$ The channel has a width of 1um and a thickness of 5nm, such that its cross section has an area equal to $5000 nm^2$. The fitted parameters are taken from [3], and reported in table 2.1. In fig. 2.2 the curve showing the drain current as a function of the drain bias is reported, for different gate voltages. For low gate bias values the current remains rather low. Increasing the Vgs up to the threshold voltage, the drain current steeply increases for low Vds values, reaching then saturation.Nevertheless, the most important plot is the one including the transcharacteristic of the TFET,which is reported in fig 2.3 and shows the drain to source current as a function of the drain voltage. The results are computed for two drain-source bias voltages: Vds = 0:1 V and Vds = 0:5 V. The result almost perfectly reproduces the one obtained in [**e3**]: there is a clear shift of the current when different drain bias are applied. For higher Vds both ION and IOFF increases, but at dierent rates such that for bigger applied voltages an higher ION=IOFF ratio is achieved. Looking at the transcharacteristic in linear scale the typical exponential trend in subthreshold condition can be recognized, which then tends to a linear behavior above threshold. ON and OFF current can be obtained from the curve obtained for Vds = 0:5 V, by taking the values of the current at zero drain-to-source bias and in saturation conditions:

$$I_{OFF} = 7.413 \times 10^{-4} \frac{\mu A}{\mu m}$$
$$I_{ON} = 9.772 \frac{\mu A}{\mu m}$$

which thus provides a very large ON/OFF ratio.

5.2.2 Samuel-Balamurugan

In Samuel et al. (2013) [**4**] a 2D surface potential model for a dual metal double-gate tunnel Field-effect-transistor is implemented. The idea is to solve the 2D Poisson's equation

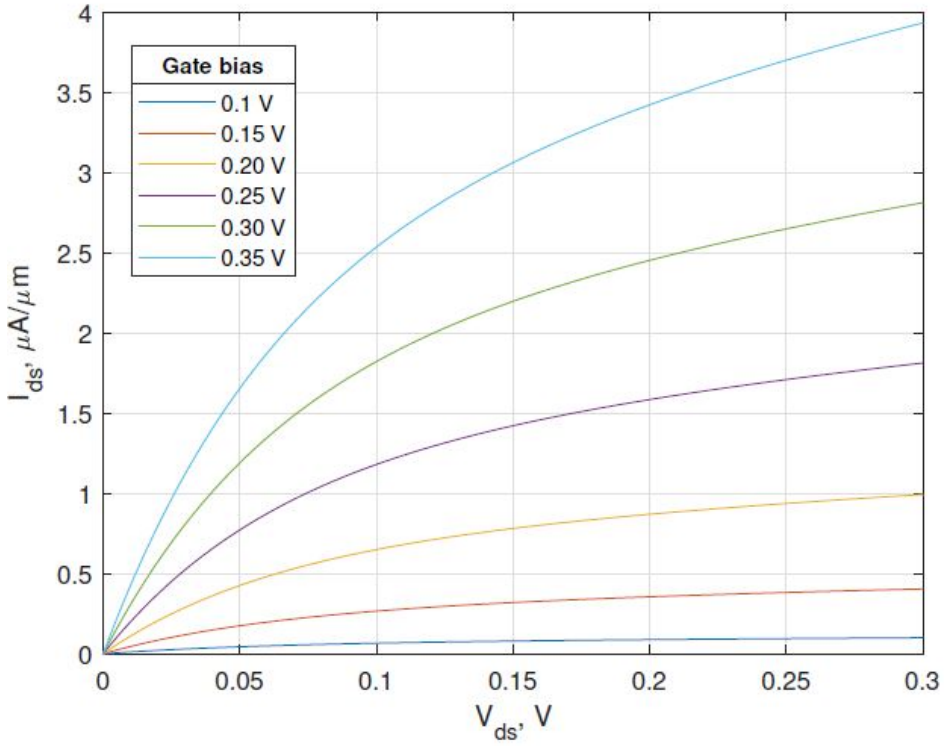

Figure 5.8: Ids-Vds of the DG-TFET InAs with Lg = 20 nm, obtained by means of Hao Lu model, for different gate bias values.

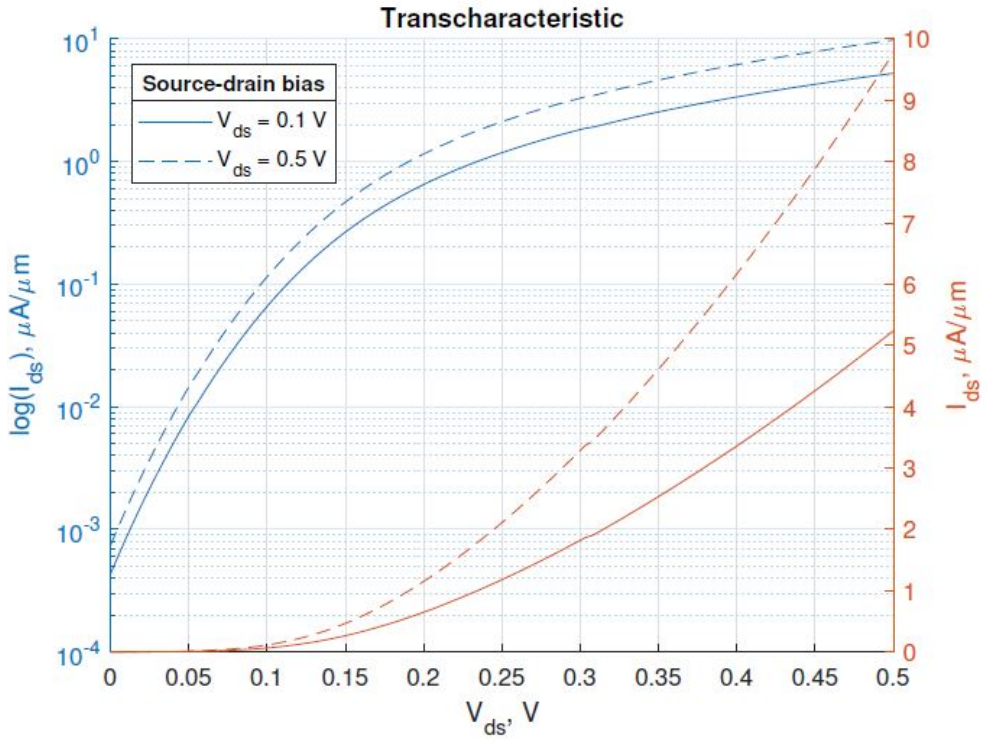

Figure 5.9: Transcharacteristic of the DG-TFET InAs with Lg = 20 nm, obtained by means of Hao Lu model

in the parabolic approximation deriving analytical expressions for the electrostatic potential, electric field and tunneling generation rate over proper boundary conditions and use them to numerically compute the tunneling current by integrating the band-to-band generation rate over the volume of the device.The considered structure is reported in figure 5.9. It is composed by a dual material Gate, controlled by a common electrode. In order to adapt it to the structure studied with the Hao Lu model, the two materials of the gate are taken as equal, such that M1=M2 and L1=L2=L/2.

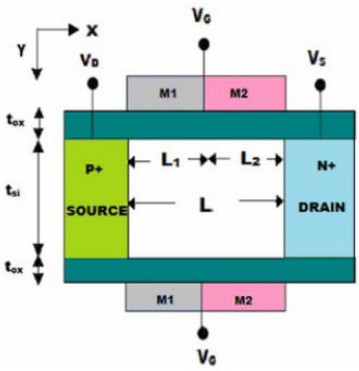

Figure 5.10: Schematic diagram of a DMDG nTFET

The electric field in the structure is evaluated by solving a 2D Poisson equation with a parabolic approximation of the potential. The electric field distribution is then used to compute the drain current Ids. The latter is due to band-to-band tunneling (BTBT), which is modeled by means of the simple Kane's model

$$G_{btbt}(x, y, \xi) = A_k . \frac{|\xi|^2}{\sqrt{E_g}} . e^{-B_k \frac{E_g^{\frac{3}{2}}}{|\xi|}} \qquad (5.15)$$

where ξ is the magnitude of the electric field on x and y direction and E_g is the energy band gap. A and B are the so called Kane's parameters and are set to: $A_k = 8.1 \times 10^{17} \frac{eV^{\frac{1}{2}}}{(cm.s.V^2)}$ and $B_k = 3.057 \times 10^7 \frac{V}{\left(cm.e.V^{\frac{3}{2}}\right)}$, where the latter can be considered as a sort of critical value of electrical field above which tunneling of carriers starts to play a significant role. Current is eventually computed by integrating the generation term calculated by eq (5.15) over the section of the TFET channel:

$$I_{ds} = q \int_0^{t_{st}} \int_0^{L_{ch}} G_{btbt}(x, y)\, d_x d_y \qquad (5.16)$$

5.2.3 Bardon et al

The last investigated model for Double-Gate TFET modeling is the one developed by Bardon et al. (2010) [22], in which a pseudo-2D surface potential model is

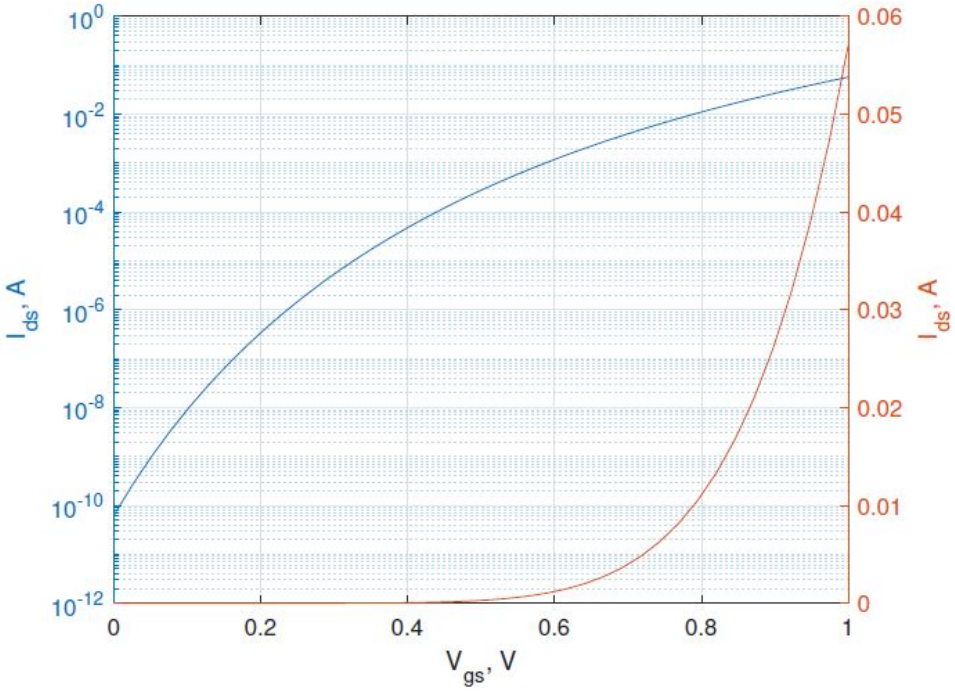

Figure 5.11: Transcharactersitics of nTFET modeled

developed to extract analytical expressions of the potential, electric field and generation rate. The drain-to-source current is then computed by numerically integrating the band-to-band generation rate on the volume of the device, just like done in (5.17). The main advantage of this model is the fact that it includes the effects of the depletion of drain and source (regions R1 and R3), whose presence becomes critical when the device is scaled down. Moreover, being the model directly dependent on the channel length it allows in principle for the investigation of several technological nodes. The device structure is reported in figure **??**. The Poisson's equation is solved separately in each secttion of the device (R1, R2, and R3), by imposing proper boundary conditions to ensure the continuity of the electrostatic potential and of the electric field along the channel.

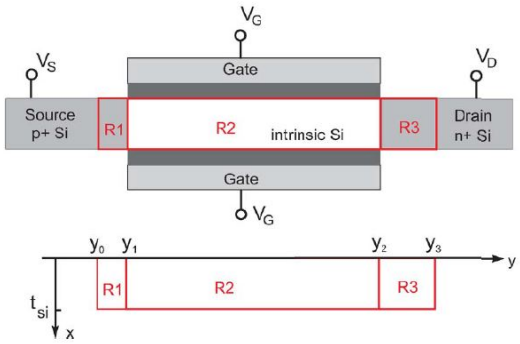

Figure 5.12: Structure of the Double-Gate TFET studied

The model is used to study the characteristics of the device from the OFF state up to the onset of the ON state. In this regime of operation the mobile charges in the channel have a negligible influence on the electrostatic of the device, so that the Poisson's equation can be written as:

$$\frac{\delta^2\psi(x,y)}{\delta x^2} + \frac{\delta^2\psi(x,y)}{\delta y^2} = \frac{qN_s}{\epsilon_s} \qquad (5.17)$$

where $\psi(x,y)$ is the electrostatic potential in the substrate measured with respect to the Fermi level, Ns is the film effective doping level (being N1 in the p-type doping in the source region, positive and negative $\pm N2$ is the lightly doping in the intrinsic channel and -3 in the n-type drain) and ϵ is the semiconductor dielectric constant. Assuming the potential to be parabolic in the vertical direction x, the electrostatic potential for a double-gate device can be approximated in a second-order polynomial [23], [**e9**]

$$\psi(x,y) = a_0(y) + a_1(y)\,x + a_2(y)\,x^2 \qquad (5.18)$$

As boundary conditions the continuity of the electrostatic potential and of the electrostatic displacement at the surfaces of the thin

lm are imposed (at x = 0 and x = ts):

$$\psi(0;y) = \psi_s(y) \qquad (5.19)$$

$$\psi(t_s;y) = \psi_b(y) \qquad (5.20)$$

$$E_x(0,y) = -\frac{\eta}{ts}(\psi_g - \psi_s(y)) \qquad (5.21)$$

$$E_x(ts,y) = -\frac{\eta}{ts}(\psi_b(y) - \psi_G(y)) \qquad (5.22)$$

where $\psi_s(y)$ and $\psi_b(y)$ are the front and the back-side surface potentials, respectively, while $\psi_g = V_{gs} - \phi_M - \chi + \frac{E_g}{2}$ is the gate potential, as already de
ned in the previous section. The coefficient η is the ratio between gate and thin-film capacitance, and it is equal to:

$$\frac{\eta}{R_2} = \frac{\epsilon_r t_s}{t_r \epsilon_s} \qquad (5.23)$$

doing calculations final equation is

$$\frac{d\psi_{si}}{dy} = \frac{d\psi_s(i+1)}{dy} \quad (i = 1.....n-1) \qquad (5.24)$$

5.3 Module Integration on TAMTAMS

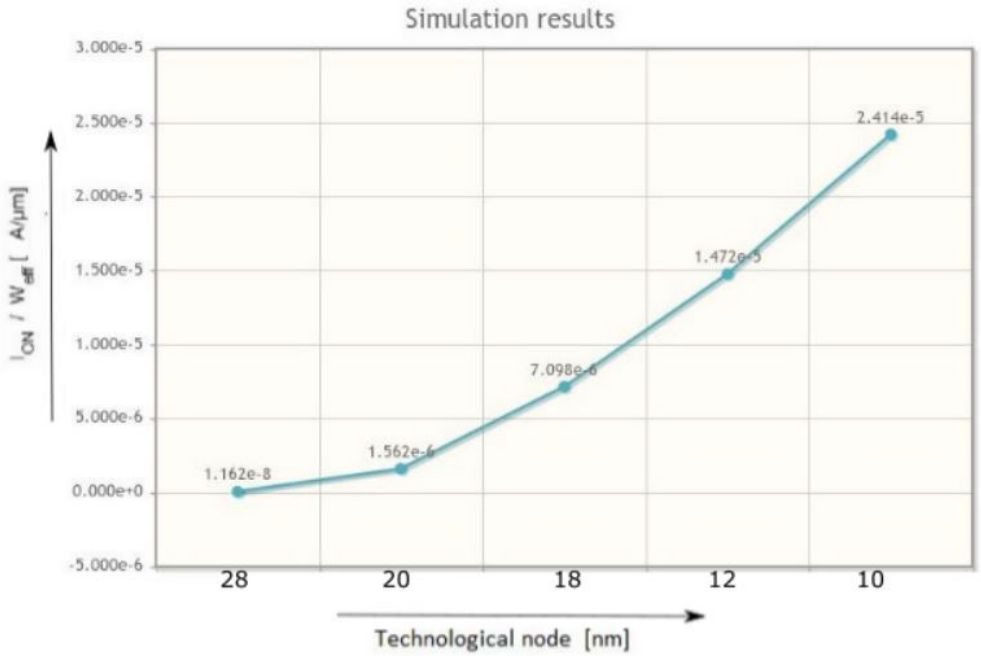

Figure 5.13: On Current for different Technological nodes

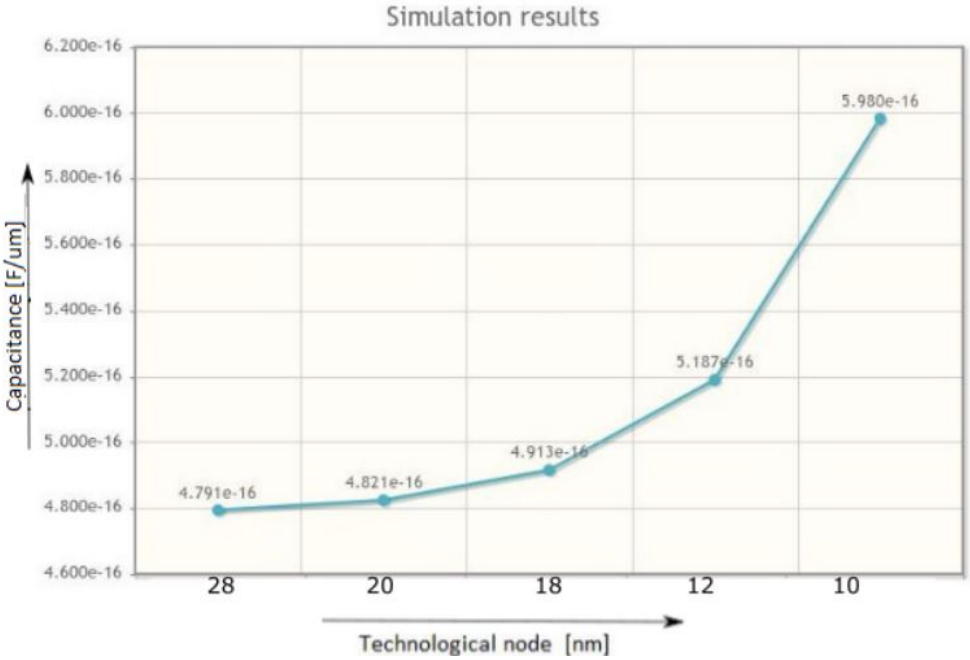

Figure 5.14: Capacitance between gate and drain for different Technological nodes

Chapter 6

Analysis Of Transistors and Basic Gate

6.1 Introducation

In this chapter, we will analyze the Transistor and its leakage currents..I_{OFF_n}, I_{OFF_p} and I_{Gate_n},I_{Gate_p} A formula derivation will be carried out to explore characteristics of flip flops in the next chapter. Our main objective is to calculate the static power while the flip flop is in one state and time delay in changing the state from one to zero. A transistor-level study will reveal the relationship between leakage current and power consumption. As the leakage current is different for different technological transistors so is the power consumption of such transistors. For flip-flop propagation delay, we should know the delay of a transistor, delay of an inverter, and delay of a NAND Gate because these are all the building blocks for flip-flops. Some flip flops are made from cross-coupled NAND Gates. So, it is imperative to focus on the derivations of a cross-coupled NAND gate.

6.2 Transistor Level Analysis

In this section, we will calculate the leakage current in transistors. Leakage current w.r.t the states of a Transistor is termed as either OFF current when the transistor is in OFF state or as Gate current when the transistor is in ON state. For the leakage current we consider the below two factors;

Subthreshold current:is the leakage current that flows drain/source when $V_{gate_{nMOS}} = 0$ and $V_{gate_{pMOS}} = V_{DD}$ as shown in figure 6.1
Gate Current:is the leakage current that flows from drain and source to gate or vice versa when drain and source are tied at the same potential and gate is tied at

the opposite potential for nMOS and pMOS as shown in figure 6.2

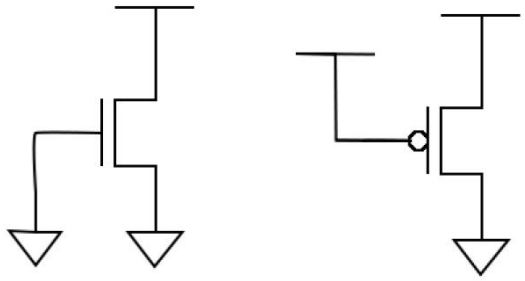

Figure 6.1: Leakage drain/source current when MOS are off

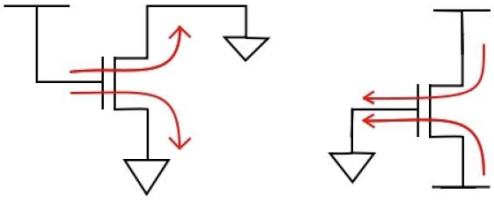

Figure 6.2: Leakage gate current

6.3 Theoretical analysis for Single MOSFET

we will estimate necessary technological parameters in order to evaluate
Static power
Dynamic power
Input-to-output delay
Maximum frequency
The static power can be evaluated as shown below

$$P_{static} = V_{DD}.I_{leak} \qquad (6.1)$$

where I_{leak} is the leakage current and V_{DD} is the voltage supply.The dynamic power can be computed as

$$P_{dynamic} = \alpha.C_{gate}.V_{DD}^2.f \qquad (6.2)$$

where α is the switching activity, $\alpha.C_{gate}$ is the switching capacitance and f is the frequency.The oxide capacitance per unit length is the same for pMOS and nMOS transistors.

$$C_{ox} = \frac{10^9(\epsilon_0.\epsilon_r)}{t_{ox}}.L_{eff} \quad \left[\frac{\rho F}{\mu m}\right] \qquad (6.3)$$

where L_{eff} is the effective gate length and t_{ox} is the thickness of the oxide. The input capacitance of nMOS and pMOS transistors per unit length are:

$$C_{in_N} = C_{OX} + C_{overlapN} \qquad \left[\frac{\rho F}{\mu m}\right] \qquad (6.4)$$

In this equation for input capacitance at n channel $C_{overlapN}$ is overlap capacitance in transistor at n channel.

$$C_{in_P} = C_{OX} + C_{overlapP} \qquad \left[\frac{\rho F}{\mu m}\right] \qquad (6.5)$$

In this equation for input capacitance at p channel $C_{overlapP}$ is overlap capacitance in transistor at p channel. where the two overlap capacitances are due to the overlap size between the gate and drain/source areas:

$$C_{overlapN} = 10^6.C_{GDO_n} \qquad \left[\frac{\rho F}{\mu m}\right] \qquad (6.6)$$

in equ (6.6) C_{GDO_n} capacitances is due to the overlap size between the gate and drain/source areas and overlap capacitance is scaled on these value.

$$C_{overlapP} = 10^6.C_{GDO_p} \qquad \left[\frac{\rho F}{\mu m}\right] \qquad (6.7)$$

in equ (6.7) C_{GDO_p} capacitances is due to the overlap size between the gate and drain/source areas and overlap capacitance is scaled on these value.

The junction capacitances between source and drain are:

$$C_{jN} = C_{bottomN} + C_{sidewallN} \qquad \left[\frac{\rho F}{\mu m}\right] \qquad (6.8)$$

C_{jN} is the junction capacitance on n channel.

$$C_{jP} = C_{bottomP} + C_{sidewallP} \qquad \left[\frac{\rho F}{\mu m}\right] \qquad (6.9)$$

C_{jP} is the junction capacitance on p channel
$C_{bottomP}$ is the capacitance due to the area of the pool of the source/drain and $C_{sidewal}$l is the one due to the edge of the same pool.

$$C_{bottomN} = C_{j0_N}.\left(\left(1 + \frac{V_{DD}}{2.P_{bN}}\right)^{-M_{jN}} .2.5.L_{drawn} \qquad \left[\frac{\rho F}{\mu m}\right]\right) \qquad (6.10)$$

$$C_{bottomP} = C_{j0_P}.\left(\left(1 + \frac{V_{DD}}{2.P_{bP}}\right)^{-M_{jP}} .2.5.L_{drawn} \qquad \left[\frac{\rho F}{\mu m}\right]\right) \qquad (6.11)$$

$$C_{sidewallN} = 10^6 \quad C_{swN}.\left(\left(1 + \frac{V_{DD}}{2.P_{b_{swN}}}\right)^{-M_{jswN}} \qquad \left[\frac{\rho F}{\mu m}\right]\right) \qquad (6.12)$$

$$C_{sidewallP} = 10^6 \quad C_{swP}.\left(\left(1+\frac{V_{DD}}{2.P_{b_{swP}}}\right)^{-M_{jswP}} \qquad \left[\frac{\rho F}{\mu m}\right]\right) \qquad (6.13)$$

Moreover for the estimation of parasitic capacitances C_{jN} and C_{jP} , it is necessary to evaluate the perimeter.

$$perim_N = 2.lungh - diff + W_N\,[[\mu m]] \qquad (6.14)$$

$$perim_P = 2.lungh - diff + W_P\,[[\mu m]] \qquad (6.15)$$

We consider only one side for the W, because the internal one doesn't touch a conductor, but just a spatial charge. Therefore C_{jN} and C_{jP} are:

$$C_{jN} = C_{bottomN}.W_N + C_{sidewallN}.perim_N\,[pF] \qquad (6.16)$$

$$C_{jP} = C_{bottomP}.W_P + C_{sidewallP}.perim_P\,[pF] \qquad (6.17)$$

6.4 Analysis for 2-input NAND Gate in CMOS Technology

In order to compute dynamic power,

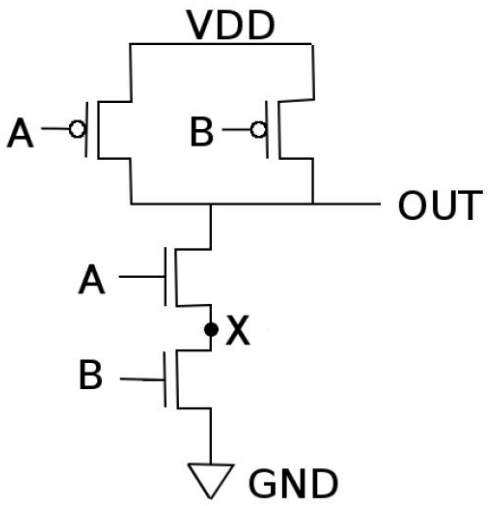

Figure 6.3: CMOS 2-input NAND architecture

we have to calculate switching capacitance we have to consider three different capacitance:

C_{IN} is the input capacitance associate at only one input

$$C_{IN} = C_{OX}.2W_N.Leff + C_{OX}.W_P.L_{eff} + 2C_{overlapN} + 2C_{overlap} \qquad (6.18)$$

C_{OUT} is the output capacitance

$$C_{OUT} = C_{jN} + 2C_{jP}\,[pF] \qquad (6.19)$$

C_{jP} is multiplied by 2 because we have different pools for the two drains. C_{IN} is the internal capacitance between the two nMOS transistors in the pull-down network

$$C_{INT} = C_{jN}\,[pF] \qquad (6.20)$$

We have only one C_{jN} because we consider that source and drain are common for the two nMOS.

To calculate the dynamic power is necessary to compute the switching activity for each node, using the probability that each node is equal to one.

$$P_{X1} = \frac{P_A.(1-P_B)}{1-(1-P_A).(1-P_B)}] \qquad (6.21)$$

P_{X1} is the probability that the internal node in equal to one. The probability P_{OUT} at the output node is

$$P_{OUT} = 1 - (1 - P_A)\,.\,(1 - P_B) \qquad (6.22)$$

The switching activities are computed from probabilities as follow

$$\alpha_A = P_A.\,(1 - P_A) \qquad (6.23)$$

$$\alpha_B = P_B.\,(1 - P_B) \qquad (6.24)$$

$$\alpha_{X1} = P_{X1}.\,(1 - P_{X1}) \qquad (6.25)$$

$$\alpha_{OUT} = P_A.\,(1 - P_{OUT}) \qquad (6.26)$$

where P_A and P_B are the probabilities of the two inputs. Finally, the total switching capacitance is

$$C_{NAND-2} = C_{IN}.\,(\alpha_A + \alpha_B) + C_{X1}\ .\ \alpha_{X1} + C_{OUT}\ .\alpha_{OUT}\ \ [pF] \qquad (6.27)$$

6.5 Static Analysis for leakage current of a NAND Gate

Considering the status of inputs of NAND Gate we make a table,that what will be leakage currents.When both inputs are low logic or high logic,and when these are opposite.At every state of inputs, from some transistor there will be gate leak current or off current.

A	B	Y	I_{leak}
0	0	1	$I_{OFF_n} + 2I_{GATE_p}$
0	1	1	$2I_{OFF_n} + 2I_{GATE_n} + I_{GATE_p}$
1	0	1	$2I_{OFF_n} + I_{GATE_p}$
1	1	0	$2I_{OFF_p} + 2.2I_{GATE_n}$

Table 6.1: Analysis of leakege current for NAND gate .

By the above table (6.1) we make the equation for leakage current for a NAND Gate. This Leakage current can be used in the calculation of static power consumption. We will use the same topology to calculate static power for Flip-flop in the next chapter.

$$\begin{gathered} I_{leak} = (1 - P_A)(1 - P_B)\left(I_{OFF_n} + 2I_{GATE_p}\right) + \\ (1 - P_A) P_B \,.\left(2I_{OFF_n} + 2I_{GATE_n} + I_{GATE_p}\right) + \\ P_A (1 - P_B)\left(2I_{OFF_n} + I_{GATE_p}\right) P_A P_B \left(2I_{OFF_p} + 2.2I_{GATE_n}\right) \end{gathered} \quad (6.28)$$

6.6 Delay Analysis

The 2-input NAND gate, is projected starting from inverter gate

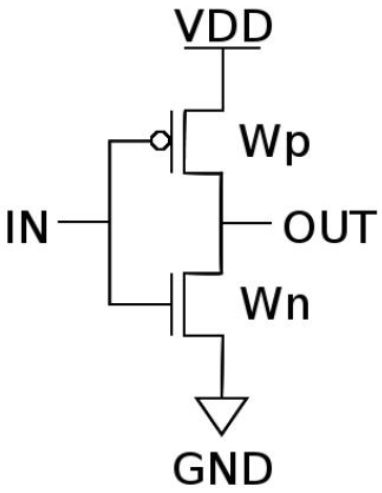

Figure 6.4: Architecture of CMOS inverter

that is made to have the same rise and fall time obtained dimensioning $W_P = 1:29W_N$ to compensate different mobility between electrons and holes. Now, from inverter in figure 4, imposing $I_{INV} = I_{NAND2}$ we obtain

$$C_{INV}\frac{V_{DD}}{t_{INV}} = C_{NAND2}\ \ \frac{V_{DD}}{t_{NAND2}} \qquad (6.29)$$

simplifying V_{DD} we obtain

$$\frac{C_{INV}}{t_{INV}} = \frac{C_{NAND2}}{t_{NAND2}} \qquad (6.30)$$

$$t_{NAND2} = t_{INV}\ \frac{C_{NAND2}}{C_{INV}} \qquad (6.31)$$

where t_{INV} is calculated in the same way as

$$t_{INV} = t_{MOS} \frac{C_{INV}}{C_{MOS}} \qquad (6.32)$$

where t_{MOS}can be computed as τ

$$t_{MOS} = C_{MOS} \frac{V_{DD}}{I_{ON_n}.W_N} \qquad (6.33)$$

The capacitances are:

$$C_{MOS} = C_{OX} \ . \ L_{eff} \ . \ W_N \qquad (6.34)$$

$$C_{INV} = C_{nN} + C_{jP} + C_{f01} \qquad (6.35)$$

$$C_{NAND2} = C_{OUT} + C_L \qquad (6.36)$$

From t_{NAND2}, maximum frequency can be computed as

$$f_{\max} = \frac{1}{t_{NAND2}} \qquad (6.37)$$

6.7 Analysis of Transmission gate delay

Transmission Gate is mainly used in sequential circuits, It builds on the complementary properties of NMOS and PMOS transistors:

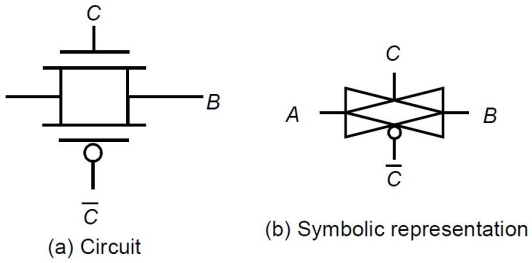

Figure 6.5: Transmission gate

NMOS devices pass a strong 0 but a weak 1,while PMOS transistors pass a strong 1 but a weak 0. The ideal approach is to use an NMOS to pull-down and a PMOS to pull-up. The transmission gate combines the best of both device flavors by placing a NMOS device in parallel with a PMOS device.The control signals to the transmission gate (C and C^{-}) are complementary. The transmission gate acts as a bidirectional switch controlled by the gate signal C. When C =1, both MOSFETs are on, allowing the signal to pass through the gate. In short

$$A = B \text{ if } C = 1$$

On the other hand, C = 0 places both transistors in cutoff, creating an open circuit between nodes A and B.Consider the case of charging node B to VDD for the transmission gate circuit in Figure 6.45a. Node A is driven to VDD and transmission gate is enabled (C = 1 and C= 0). If only the NMOS pass-device were present, node B charges up to V_{DD}-V_{Tn} at which point the NMOS device turns off. However, since the PMOS device is present and turned on ($V_{GSp} = -V_{DD}$), charging continues all the way up to VDD. Figure 6.45b shows the opposite case, this is discharging node B to 0. B is initially at V_{DD} when node A is driven low. The PMOS transistor by itself can only pull down node B to V_{Tp} at which point it turns off. The parallel NMOS device however stays turned on (since its V_{GS}= V_{DD}) and pulls node B all the way to GND. Though the transmission gate requires two transistors and more control signals, it enables rail-to-rail swing.

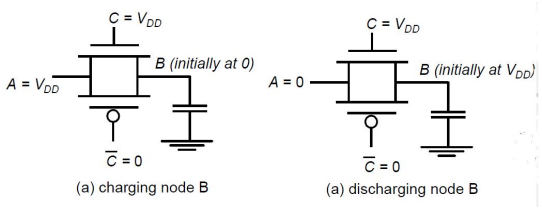

Figure 6.6: Transmission gates enable rail-to-rail switching

Performance of Transmission Gate The pass-transistor and the transmission gate are, unfortunately, not ideal switches, and have a series resistance associated with it. To quantify the resistance, consider the circuit in Figure 6.48, which involves charging a node from 0 V to VDD. In this discussion, we use the large-signal definition of resistance, which involves dividing the voltage across the switch by the drain current. The effective resistance of the switch is modeled as a parallel connection of the resistances R_n and R_p of the NMOS and PMOS devices, defined as $\frac{V_{DD}-V_{out}}{I_n}$ and $\frac{V_{DD}-V_{out}}{I_p}$, respectively. The currents through the devices are obviously dependent on the value of Vout and the operating mode of the transistors. During the low to high transition, the pass-transistors traverse through a number of operation modes. For low values of V_{out}, the NMOS device is saturated and the resistance is approximated as:

$$R_n = \frac{V_{DD}-V_{out}}{I_N} = \frac{V_{DD}-V_{out}}{K_n'\left(\frac{W}{L}\right)_N (V_{DD}-V_{out}-V_{Tn})V_{DSAT}-\frac{V_{DSAT}^2}{2}}$$

$$\approx \frac{V_{DD}-V_{out}}{K_n(V_{DD}-V_{out}-V_{Tn})V_{DSAT}} \qquad (6.38)$$

The resistance goes up for increasing values of V_{out}, and approaches infinity when Vout reaches $V_{DD} - V_{Tn}$, this is when the device shuts off. Similarly, we can analyze the behavior of the PMOS transistor. When V_{out} is small, the PMOS is saturated, but it enters the linear mode of operation for Vout approaching V_{DD}, giving the following approximated resistance:

$$R_p = \frac{V_{DD}-V_{out}}{I_P} = \frac{V_{DD}-V_{out}}{K_p'^N\left(-V_{DD}-V_{Tp}\right)(V_{out}-V_{DD})-\frac{(V_{out}-V_{DD})^2}{2}}$$

$$\approx \frac{1}{k_p\left(V_{DD}-|V_{Tp}|\right)}$$

(6.38)

The simulated value of Req = Rp || Rn as a function of V_{out} is plotted in Figure 6.48. It can be observed that Req is relatively constant ($\approx 8k\Omega$ in this particular case). The same is true in other design instances (for instance, when discharging C_L). When analyzing transmission gate networks, the simplifying assumption that the switch has a constant resistive value is therefore acceptable.

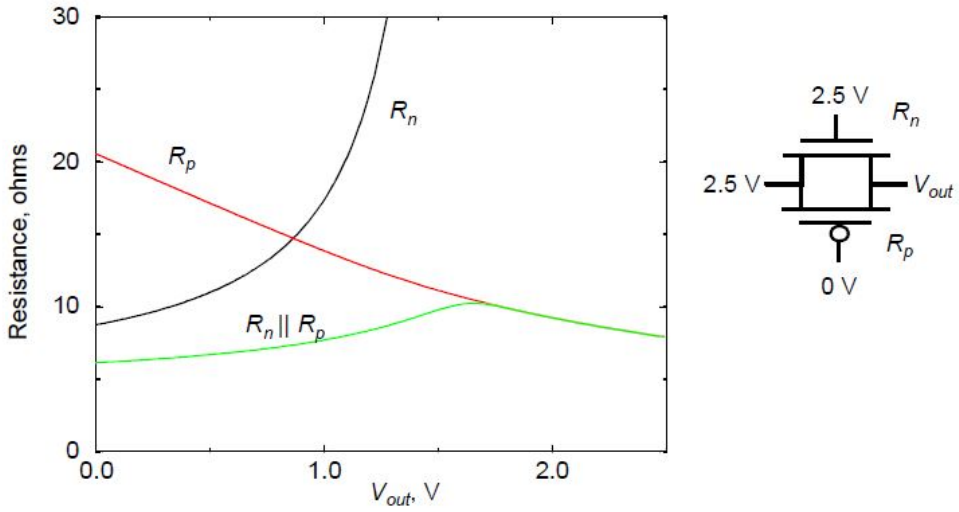

Figure 6.7: Simulated equivalent resistance of transmission gate for low-to-high transition (for (W/L)n = (W/L)p = 0.5mm/0.25mm). A similar response for overall resistance is obtained for the high-to-low transition

The transmission gates are replaced by their equivalent resistances Req. This produces the network. The delay of a network of n transmission gates in sequence can be estimated using the Elmore approximation

$$t_p\left(V_n\right) = 0.69 \sum_{k=0}^{n} CR_{eq}k = 0.69CR_{eq}\,\frac{n(n+1)}{2} \qquad (6.38)$$

This means that the propagation delay is proportional to n^2 and increases rapidly with the number of switches in the chain.

Chapter 7

Flip-Flops and Latches Using above all advanced types of Transistors

7.1 SR Flip Flop with cross coupled NAND

SR or Set Reset is one of the most basic sequential logic circuits.This is a combination of two NAND gates cross-coupled to each other.Both outputs are going as feedback to opposing inputs. This basic sequential circuit is commonly used in memory circuits to store a single bit of data. On Clock rising edge this flipflop shows changes in its output. When Set input is high and Reset is Low so Q output shows high bit 1, and Q- shows low bit 0, When Set is low, and Reset is high so Q is low bit 1 and Q- is high bit 1. When Set and Reset are both at low logic value then Q and Q- shows previous states. One thing here to be noted that both Set and Reset can not be at High logic value, this is a forbidden state. For Propagation delay and Static Power losses, Flip Flop internal transistor-level schematic is necessary to explain.

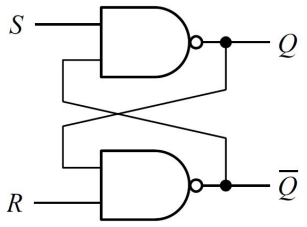

Figure 7.1: SR flipflop with cross coupled NAND gate

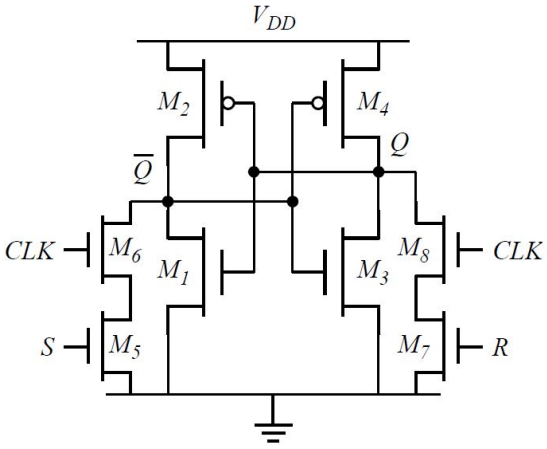

Figure 7.2: SR flipflop combination of two inverters

From this figure, we can see that here two cross-coupled inverters are together. plus 4 extra transistors to drive the flip-flop from one state to another and to provide clocked operation. Observe that the number of transistors is identical to the implementation of Figure .But the circuit has the added feature of being clocked. The drawback of saving some transistors over a fully-complimentary CMOS implementation is that transistor sizing becomes critical in ensuring proper functionality. Consider the case where Q is high and an R pulse is applied. The combination of transistors M4, M7, and M8 forms a ratioed inverter. To make the latch switch, we must succeed in bringing Q below the switching threshold of the inverter M1-M2. Once this is achieved, the positive feedback causes the flip-flop to invert states. How this SR Flip works? Now we will see that how this circuits will work ,when CLK =1 ,S =1 ,R =0, we can see that M_5 and M_6 NMOSFET transistors are on and Q^- will be direct to connected to ground and makes $Q^- = 0$.This Q^- output is feedback for opposing PMOSFET transistor M_4,its force M_4 to be ON state .When M_4 is ON its acts like a closed switch and Q output will be directly connected to V_{DD} supply voltage, it's mean now Q =1. This Q =1 will not be connected to ground because M_7 is acting as an open switch because of R =0 and of course M_8 is also open because both are in series, and M_3 is also acting as an open switch because of $Q^- = 0$. when CLK =1 ,S =0 ,R =1, we can see that M_7 and M_8 NMOSFET transistors are on and Q will be direct to connected to ground and makes Q =0.This Q output is feedback for opposing PMOSFET transistor M_2,its force M_2 to be ON state .When M_2 is ON its acts like a closed switch and Q^- output will be directly connected to VDD supply voltage, it's mean now $Q^- = 1$.This $Q^- = 1$ will not be connected to ground because M_5 is acting as an open switch because of S =0 and of course M_6 will be open because both are in series, and M_1 is also acting as an open switch because of Q =0.

S	R	I_{leak}
1	0	$2I_{GATE_n} + I_{GATE_n} + I_{GATE_p} + I_{OFF_p} + I_{OFF_n} + I_{OFF_n}$
0	1	$2I_{GATE_n} + I_{GATE_n} + I_{GATE_p} + I_{OFF_p} + I_{OFF_n} + I_{OFF_n}$
0	0	$I_{OFF_n} + I_{OFF_p} + I_{GATE_n} + I_{OFF_n} + I_{OFF_n} + I_{GATE_p}$

Table 7.1: Analysis of leakege current for SR Flip-flop

In Table (7.1) SR Flip-flop is analysed on transistor level,and its all is result of concept which is described above in detail.By using this Leakage currents ,we will calculate static power losses in SR Flip-flop.

7.1.1 Propagation delay of SR Flip Flop

Now we will calculate the Propagation delay. For Setting Q=1 at the high state our S=1, and CLK=1.M_5,M_6 will be ON which will make Q- connected to ground.Q- will be 0 Q-=0, This Q-is now input of M_4 and its makes M_4 ON, in this way Q will be connected to VDD and becomes 1. It means C_L becomes charges, So we will see that which transistors will be included in the L-H transition. Delay of M5 and M6 in series then the addition of M4 delay so CL will be charged R1 is parallel to R_5+R_6

For Setting Q=0 at low state our S=0 ,and CLK=1.we will get delay of M_7,M_8 and M_2.and capacitor will be discharged which is connected to C_L

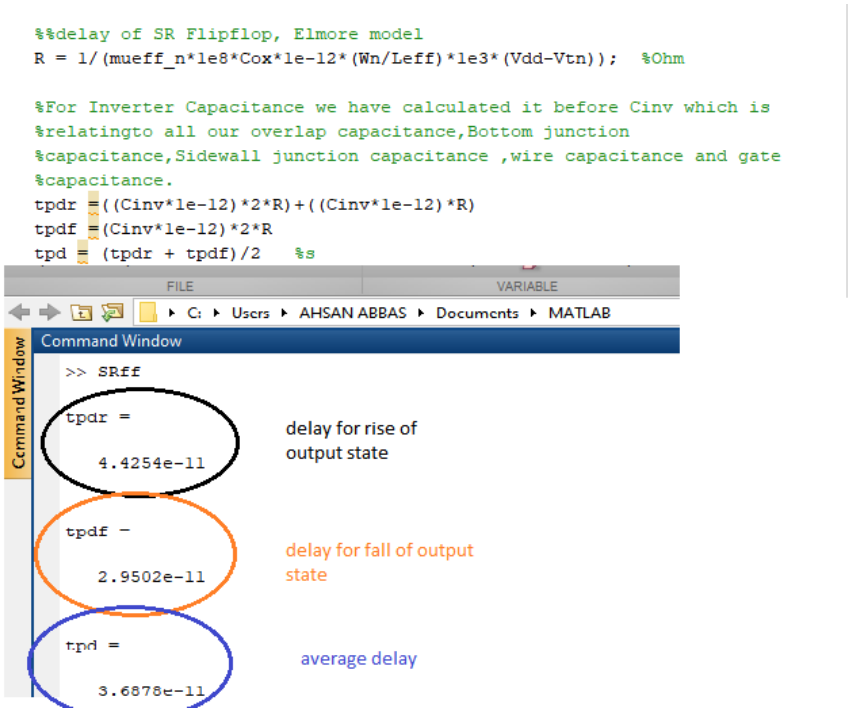

Figure 7.3: MATLAB code and result for delay of SR flip-flop

7.1.2 Static Power Consumption

Now using table (7.1) we can calculate static power consumption in SR Flip-flop.

$$P_{SRFF} = Vdd * ((3 * Ioff_{nmos} + Ioff_{pmos} + Igate_{pmos} + Igate_{nmos}) + (2 * Ioff_{n}mos + Ioff_{p}mos + 3 * Igate_{n}mos + Igate_{p}mos) + (2 * Ioff_{nmos} + Ioff_{p}mos + 3 * Igate_{nmos} + Igate_{pmos})) * (1/3) * 1e - 9 \qquad (7.1)$$

In equation(7.1) we calculated static power consumption by finding Leakage currents in the table (7.1). Table (7.1) is made by considering all possible states of SR Flip-flop. One state is forbidden in the SR flip-flop when SR flip-flop has both 1 at Q and Q-. Because Q and Q- always have opposite logic.

7.2 Multiplexer based Latch

A multiplexer based Latch is type of Latch which consists of three inverters and two transmission gates.How its works ?

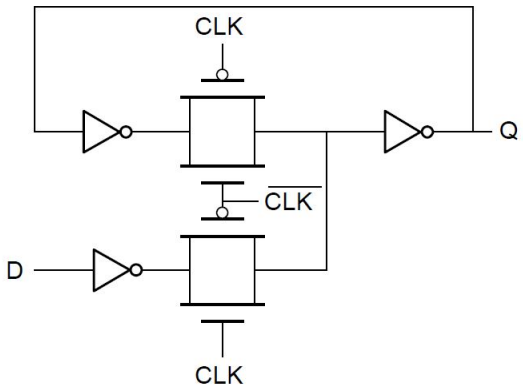

Figure 7.4: Multiplexer based Flip-Flop

We can discuss that multiplexer based latch in two portion one is the upper portion, where output is going to be feedback as input. Second is the lower portion, where output is going to show a bit of input D. When the clock is low logic 0 upper transmission gate will conduct because PMOSFET will also be ON. After all, it will be ON with logic 0 at gate and NMOSFET will also be ON because there is inverted clock mean logic high or 1and NMOSFET will be ON at inverted clock which is 1. In this way, the previous output will be feedback and we can say that Q will be Q_n^{-1}.

When the clock is low logic 1 Lower transmission gate will conduct because PMOSFET will also be ON. After all, it will be ON with logic 0 at the gate and the clock will be inverted and becomes 0, and NMOSFET will also be ON because NMOSFET will be ON at clock 1. In this way, input D will be sampled on output D.

7.2.1 Propagation Delay of Multiplexer based Latch

Now we will already have seen that what will be expression of time delay of Inverter and Transmission gate ,so we can see that Mux based Latch is nothing else, just combination Inverters and Transmission gates.

```
Req=8000;%This value is calculated in Rabey Book on VLSI

t_tg=Req*Cmos*1e-12;%This is propagation delay for Transmission gate

tpd=(t_inv)+(t_tg)+(t_inv)
```

```
Command Window

>> Muxbasedff

t_inv =

   2.2648e-12

t_tg =

   1.7793e-11

tpd =

   2.2323e-11

fx >>
```

inverter delay

Transmission gate dealy

delay of Mux Flip-flop

Figure 7.5: Matlab code and delay of Multiplexer based Flip-Flop

When clock is low logic 0, Upper transmission gate will conduct and Output Q will be feedback to input, and in circuit total propagation delay will be sum of two inverter and one transmission gate. When clock is low logic 1, Lower transmission gate will conduct an input D will be sampled on output Q, and in-circuit total propagation delay will be the sum of two inverters and one transmission gate.

$$t_{pd} = 2T_{inv} + 1T_{tg} \qquad (7.2)$$

In equation (7.2) we can see that clock is low logic or high logic, but the final equation for propagation delay is the sum of two inverter gates, and one is the

transmission gate. The transmission gate delay is detailed in chapter 6.

7.2.2 Static Power Consumption

It's easy for us now to calculate static power consumption for the Multiplexer based Latch because we already derived expression of static power for inverter in detail in the previous section and Mux based Latch is a combination of inverters and transmission gates. When the clock is at low logic value or at high logic value, but static power consumption will be the sum of two inverters. Here one thing is important to know that static power consumption for transmission gate will be zero because in transmission gate there will be no leakage current and of the current. The transmission gate will just act as a switch open or closed. So static power consumption will be just a combination of two inverters.

$$Pinv = Vdd * ((Ioff_nmos + Igate_pmos + Ioff_pmos + Igate_nmos)/4) * 1e - 9 (7.3)$$

$$P_{mux} = P_{inv} + P_{inv} \qquad (7.4)$$

7.3 Multiplexer based Master Slave Flip Flop

Multiplexer based Flip Flop is combination of two Mux based Latches.Its schematic is in figure below

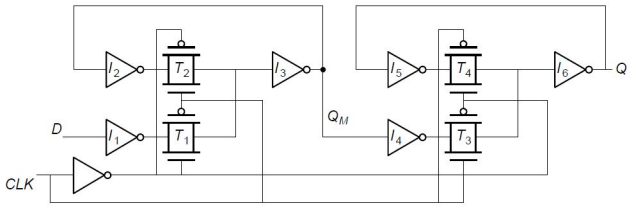

Figure 7.6: Multiplexer based Master Slave Flip Flop

We have seen Mux based Latch in previous section that how its works,now we will see that when clock is at high logic 1 ,so transmission gates T_2 and T_3 will conduct bit will be transferred through Inverters I_2,I_3,I_4,I_6 at output Q.For clock 1 schematic is given below For clock 1

Figure

When clock is at low logic value 0, so transmission gates T1 and T4 will conduct. D bit will be sampled through Inverters I_1,I_3,I_5,I_6 at output Q.For clock 0 schematic is given below

7.3.1 Static Power Consumption

It's easy for us now to calculate static power consumption for the Multiplexer based Master Slave Flip Flop, because we already derived the expression of static power for inverter in detail in the previous section and Mux based Master Slave Flip Flop is the combination of inverters and transmission gates. When the clock is at low logic value or at high logic value, but static power consumption will be a sum of four inverters. Here one thing is important to know that static power consumption for transmission gate will be zero because in transmission gate there will be no leakage current and of the current. The transmission gate will just act as a switch open or closed. So static power consumption will be just a combination of four inverters.

$$Pinv = Vdd * ((Ioff_nmos + Igate_pmos + Ioff_pmos + Igate_nmos)/4) * 1e - 9 (7.5)$$

$$P_{mux} = P_{inv} + P_{inv} + P_{inv} + P_{inv} \qquad (7.6)$$

7.4 Clocked C2MOS Flip Flop

In this figure a positive edge-triggered register,based on a Master-Slave concept insensitive to clock overlap.This circuit is called C2MOS Flip Flop.

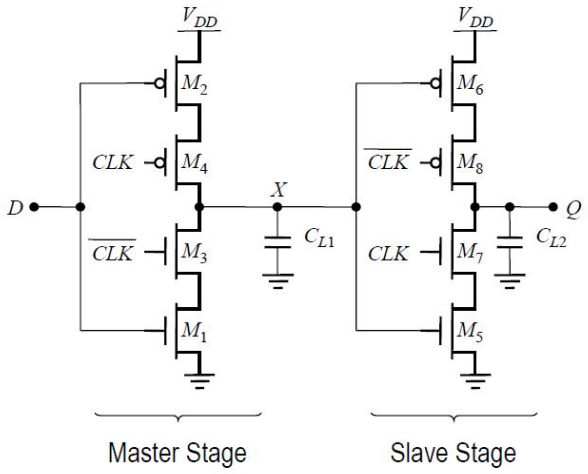

Figure 7.7: Multiplexer based Master Slave Flip Flop

When CLK= 0 The first tri-state driver is turned on, and the master stage acts as an inverter sampling the inverted version of D on the internal node X. The master stage is in the evaluation model. Meanwhile, the slave section is in a high-impedance mode, or in a hold mode. Both transistors M7 and M8 are off,

decoupling the output from the input. The output Q retains its previous value stored on the output capacitor C_{L2}. when CLK = 1 The master stage section is in hold mode (M_3 - M_4 off), while the second section evaluates (M7-M8 on). The value stored on C_{L1} propagates to the output node through the slave stage which acts as an inverter.

7.4.1 Propagation Delay of C2MOS Flip Flop including Setup and Holding Time

We have already seen that what will be the time delay of Inverter, here in this type of Flip Flop we will see that total delay will be the sum of two inverters and also setup and hold time. When Clock is 0, then we see that the Master stage act as an inverter sampling the inverted version of D on internal node X. The master stage is in evaluation mode. Meanwhile, the slave section is in a high-impedance Mode, or in a hold mode. Both transistors M7 and M8 are off, decoupling the output From the input. The output Q retains its previous value stored on the output capacitor C_{L2}.When the clock is 1 then the master stage section is in hold mode (M_3 - M_4, while the second section evaluates (M7-M8 on). The value stored on C_{L1} Propagates to the output node through the slave stage which acts as an inverter. The time delay will be the sum of master stage inverter, slave stage inverter, and setup and hold time.

$$T_{pd} = 2T_{inv} + 1T_{su} + 1T_h \qquad (7.7)$$

```
%
tpd=(t_inv)+(tsu)+(t_inv)+(th)%

Pinv=Vdd*((Ioff_nmos+Igate_pmos+Ioff_pmos+Igate_nmos)/4)*1e-9;
Pff=Pinv+Pinv
```

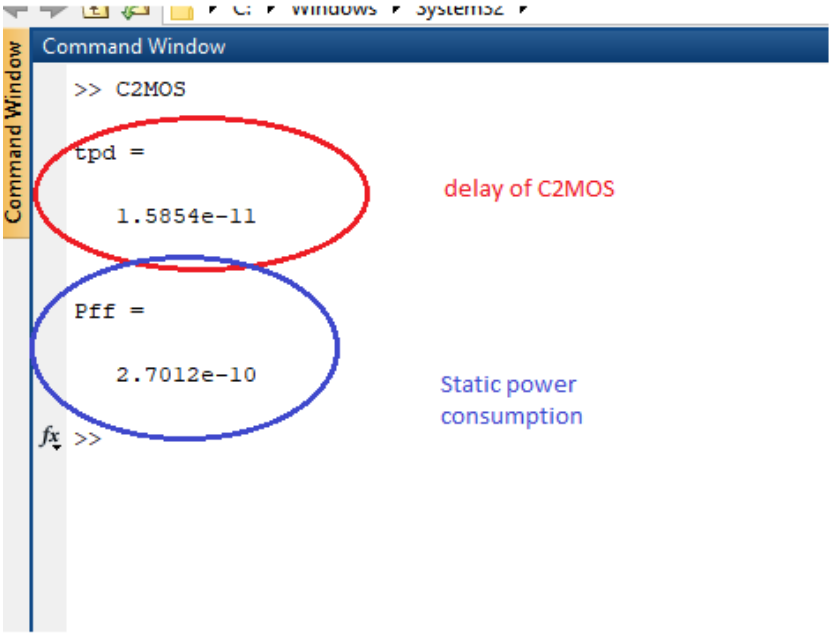

Figure 7.8: Matlab code and delay,Power of C2MOS based Flip-Flop

7.4.2 Static Power Consumption

It's easy for us now to calculate static power consumption for the C2MOS Flip Flop, because we already derived expression of static power for inverter in detail in previous section and C2MOS Flip Flop is combination of inverters.

$$Pinv = Vdd * ((Ioff_nmos + Igate_pmos + Ioff_pmos + Igate_nmos)/4) * 1e-9 \quad (7.8)$$

$$P_{c2mos} = P_{inv} + P_{inv} \quad (7.9)$$

Chapter 8

Conclusions

The work of thesis is done in two main parts, Simulations for emerging devices like FinFet Transistors, Fully Depleted SOI Transistors,UTBB FD SOI Transistors, Tunnel Gate Field Effect Transistors is done in MATLAB.Analytical models for different devices like Gate Current, Drain Current, Off Current, Threshold voltage, and mobility are derived which will be necessary parameters for design of very large scale integrated circuits as Flip Flops and Latches in our case. We validate a correctness of these models taking consideration of International Road Map. After that some new models were done on MATLAB, these models were basic building blocks for memories which are Latches and Flip Flop. Static Power Consumption is main role in modeling of Flip Flop and Latches. We started from low level simulation from PMOS and NMOS Transistors and we go towards high level simulations like Inverters and Transmission gates. Then we see that Flip Flop and Latches are combination of Transistors and Transmission gates. Static Power consumption for Flip Flops and Latches is calculated. Time delay for these basic building blocks is also calculated, that in how much time output of Flip Flop or Latch will be changed if input of Latch will be changed. For all Flip Flops and latches Propagation delay is calculated and also in the presence of setup and hold time, if in any case Master stage and Slave stages included these Setup and Hold time.

Secondly all these modules which are derived on MATLAB,are integrated with TAMTAM.TAMTAM is a web based tool made by Politecnico Di Torino,For all emerging devices models were integrated with different technological nodes taken by international Road Map. For different technological bottoms, these simulations can be seen on TAMTAM at same time. Anyone can take an idea that which device can be a better solution for their design of an Integrated circuit. Technological bottoms are made by many researchers in universities and companies like ST Microelectronics and Silicon foundries. When we put our Simulations of Flip Flops and Latches in TAMTAMS.Its take data of emerging devices for different

technological bottoms and will gives result in form of Time delay and Static Power Consumptions.

8.1 Future Works

Future work behind the presented thesis could focus on analytical modeling of Area and Dynamic Power consumption of Flip Flops and Latches and integration of all these parameters in TAMTAMS. These modeling will be simulated on MATLAB. Different technological nodes will be made. These technological nodes also should obey the International Road Map. When these nodes will be made, So Matlab module simulations should be put in TAMTAM and TAMTAM will give us results of device modelings and technological nodes simultaneously. As I worked on the technological nodes of Transistor and TAMTAM, In the future there can be work on basic gates. The rule will be the same, that we will start from Transistor level Analysis, and then we can target our calculations for basic gates.

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