POLITECNICO DI TORINO

Master's degree
in Electronic Engineering

Master's thesis

Analysis and design of half-bridge LLC resonant power converters

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Chapter 1

Introduction

The field of power electronics mainly covers the control and the conversion of electric power. In order to fulfil these tasks, solid-state devices of power electronics (power diodes, thyristors, power MOSFETs, IGBTs, etc..) generally differ from the ones typical of analog and digital electronics (usually CMOS-based): this is due to the fact that operating voltages, currents and even frequencies are very different in these two fields of electronics. In fact, while analog and digital electronics deal with low levels of power (generally, currents less than some amperes and voltages less than some tens of volts) with the objective of transmitting some information, power electronics usually handles higher or even much higher (in the case of industrial applications) power levels, which need properly suited devices. One of the most typical power application is the AC-DC converter (rectifier), which is required for correctly supplying many consumer electronic devices (such as TVs, PCs, battery charges, etc...), starting from the conversion of mains electricity. Other power conversion systems include DC-AC, AC-AC and DC-DC devices. In particular, one of the possible DC-DC converters, namely the LLC one, is the main focus of the following chapters. Its many benefits and few drawbacks result in an increasingly use of this converter in many applications, such as flat-panel TVs, ATX power supplies, small form factor PCs, high-efficiency solar PVs [1] etc... However, the design of the LLC converter is unfortunately very hard to be performed accurately due to its strong nonlinearity and to the reactive effects of the system. The thesis focuses on analysis and design techniques, oriented towards the LLC converter (rather than on control techniques), trying to give a detailed analysis and an organic presentation of the state-of-the-art knowledge of the LLC converter operation. Moreover, it is shown how the existing design methods try to exploit different approaches for the optimal choice of the components. Therefore, state-of-the-art methods are compared making uniform as much as possible the descriptive notations, in order to obtain a better overall understanding and to underline the main advantages and drawbacks of each approach. Finally, the last contribution of this thesis is the attempt to go a little further by exploiting an accurate description of the converter to analyse and design it, considering the effect of parasitic elements, e.g. resistances. In particular, the developed analysis and design of the converter are carried out through several MATLAB scripts, comparing the obtained results with the ones extracted from LTspice simulations of the converter schematic.

Chapter 2

The LLC resonant power converter

2.1 Resonant conversion

Two distinct family of solutions exist in power electronics when the driving of a load is required and they, respectively, resort to linear circuits and switching ones. The main problem of linear topologies is that generally there is a high power loss across the transistor (e.g. working as a current generator) which is used to regulate the output load current: in fact, in all these circuits, the transistors work in saturation mode thus being characterised by a large voltage drop between the drain and source terminals.

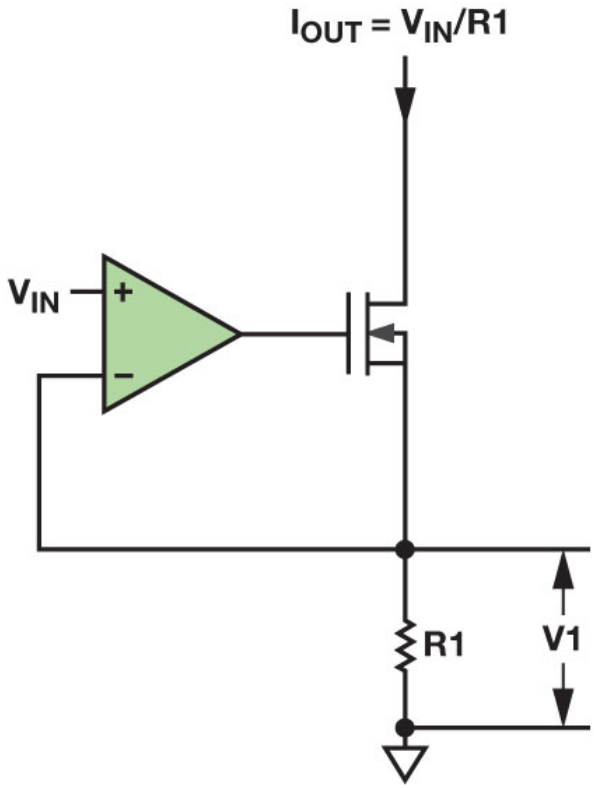

Figure 2.1: Circuit for current control through the use of a MOSFET working in saturation

This issue practically limits the maximum output power that can be handled by this class of circuits, which can achieve low levels of efficiency. Switching topologies, instead, exploits power switches (generally MOSFETs) able to cyclically turn on and off at high frequencies (kHz-MHz) in order to fix the mean value of the load current, which can then be modulated through e.g. the duty cycle of the command signal applied to the gate of the transistor.

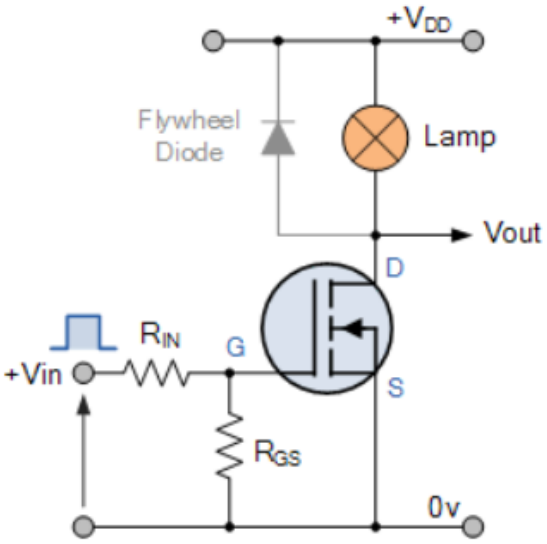

Figure 2.2: Switching circuit for the driving a resistive load

This solution drastically reduces power losses across transistors, since they are used in triode region and therefore their drain-to-source voltage is negligible (ideally zero).
One of the possible applications of switching configurations is in circuits of static conversion like DC-DC converters. These switching converters are characterised by high conversion efficiency (usually higher than 80%) since power losses are confined only to switching transitions, on-state resistance of power transistors and parasitic resistances of reactive elements. It is important to underline that every DC-DC converter can be used as a building block for a switching voltage regulator, i.e. a circuit which keeps constant the output voltage despite the variations of input voltage, load current, environmental parameters (e.g. temperature), etc... Of course, in order to obtain an actually working voltage regulator, a DC-DC converter has to be integrated with a control circuit [2] able to modulate the duty cycle or the frequency of the signal driving the power MOSFETs, depending on the measurement of some "error" signal (e.g. the difference between the output voltage and a reference voltage).

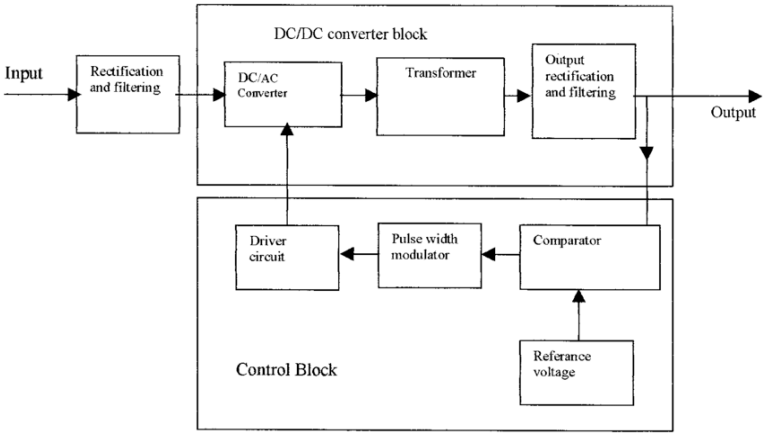

Figure 2.3: Block diagram of a voltage regulator

The design of this control circuit is critical as well as the one of the converter and it is rather difficult because of the fact that switching converters are time-varying non linear circuits. Finally, switching regulators can be embedded in more complex systems in order to build switched-mode power supplies (SMPS).
Focusing on DC-DC converters, they can be classified as follows [3], depending on their architecture and on their working principle:

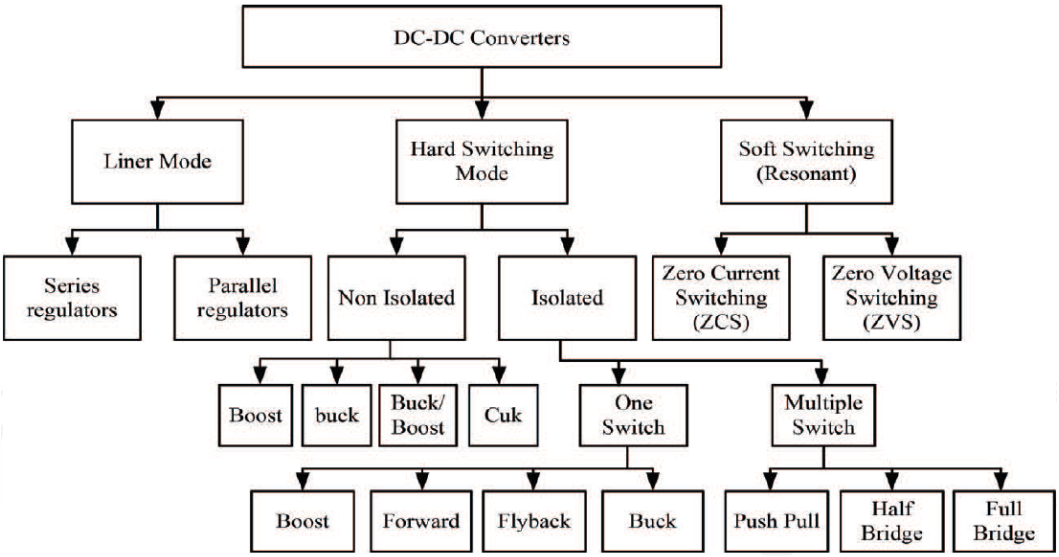

Figure 2.4: Classification of DC-DC converters

As clear from the figure above, many different families of DC-DC converters can be found in literature, each characterised by different topologies and characteristics.
The class of soft-switching (resonant) converters (SSCs), in particular, has received more and more attention and interest in nowadays electronics. This is due to the fact that these converters are able to overcome the limitations which are typical of the converters working in hard-switching mode. This last group of circuits make use of switching devices to increase the conversion efficiency (as in the case of soft-switching converters) but they are characterised by non-negligible power losses associated to the switching transitions which can lead to limited values of efficiency. A reduction of the power losses can be obtained by the use of appropriate circuits, e.g. snubbers that reduce the stress on power switches or simply by choosing devices able to perform with lower switching time: the former solution is able to effectively limit switch losses but also implies a constraint on the maximum frequency at which the converter can work; the latter one, instead, causes an increase of time-derivative voltages and currents, eventually resulting in a higher electromagnetic interferences (EMI). In order to surpass the frequency limitations and further reduce power losses, soft-switching converters are used: in particular, the idea is to turn on and off switching devices when either their voltage or current is zero (Zero-Voltage-Switching, ZVS, and Zero-Current-Switching, ZCS)

and, possibly, with zero (low) time-derivative (Zero-Voltage-Derivative-Switching, ZVDS, and Zero-Current-Derivative-Switching, ZCDS). Of course, in practical applications, zero voltage/current actually means a very low/low value compared to the other voltages/currents characterising the circuit.

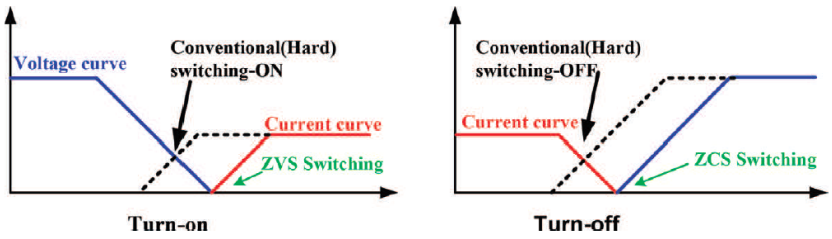

Figure 2.5: Current and voltage waveforms of hard-switching and soft-switching

The benefits of a soft-switching topology (with respect to hard-switching ones) are several and are summarised in the following list:

- absence of Miller plateau (which means less energy required to drive power switches);
- lower noise;
- lower EMI (smoother waveforms);
- lower switching losses;
- higher operating frequencies (resulting in a reduced components size, i.e. higher power densities);
- increased efficiencies at higher frequency;

SSCs are very often also named Resonant Power Converters (RPCs), since, in order to obtain soft-switching (either ZVS or ZCS), resonant circuits have to be used. RPCs are, in turn, divided in two more sub-categories: resonant tank converters and resonant switch converters (also called quasi-resonant converters, QRCs). In particular, QRCs are obtained by substituting the "simple" power switches of hard-switched converters with resonant ones [4], which consist of one switch, one diode and one resonant LC network, in a basic configuration.

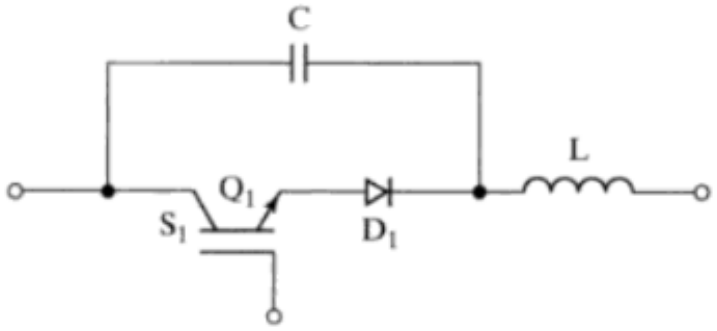

Figure 2.6: Example of a resonant switch

This last solution allows the power switches to reach the ZVS or ZCS condition thus bringing all the benefits previously discussed.
Resonant tank converters are instead modelled as 2-stage networks: the first stage is a DC-AC resonant inverter (which consists of a control switching network and a resonant tank) while the second one is made of a high-frequency rectifier followed by a low pass filter (LPF).

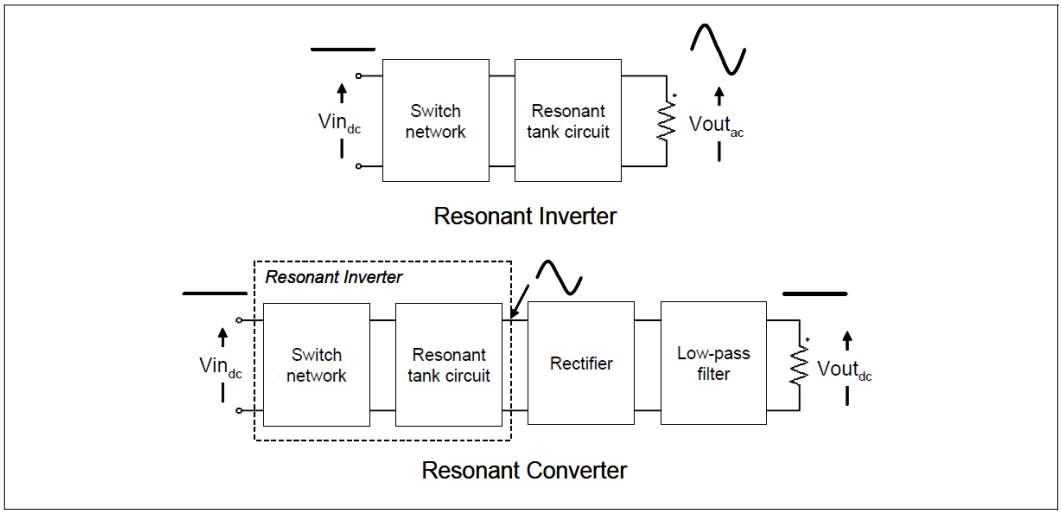

Figure 2.7: General block scheme of a resonant tank converter

In particular, the switching network is typically a half-bridge or full-bridge configuration able to generate a square wave voltage from a DC input. The generated square wave, in turn, becomes the input of the resonant tank (i.e. a circuit made of reactive elements based on a LC configuration), generally tuned to the fundamental component of the square wave voltage in order to produce a low-harmonic content AC voltage (e.g. sinusoidal). Then, in most cases, the rectifier stage is coupled to the inverter through a transformer to guarantee galvanic isolation required by safety regulations: in these cases, the rectifier devices are usually referred to as "secondary rectifiers" because they are located at the secondary side of the transformer. The rectification is usually achieved through the use of power diodes (full wave

or bridge rectifier) or more complex switched circuits (active or synchronous rectification) and it is useful to convert the AC voltage from the resonant network to the output DC voltage. Moreover, rectifiers are needed to provide DC power to the load. As usual, the power flow from input to output can be controlled by the switch network either by changing the frequency of the square wave voltage or its duty cycle.
Resonant tank converters can be divided in three main groups: series load resonant converters (SLRCs), parallel load resonant converters (PLRCs) and hybrid (or series-parallel) load resonant converters (SPLRCs).

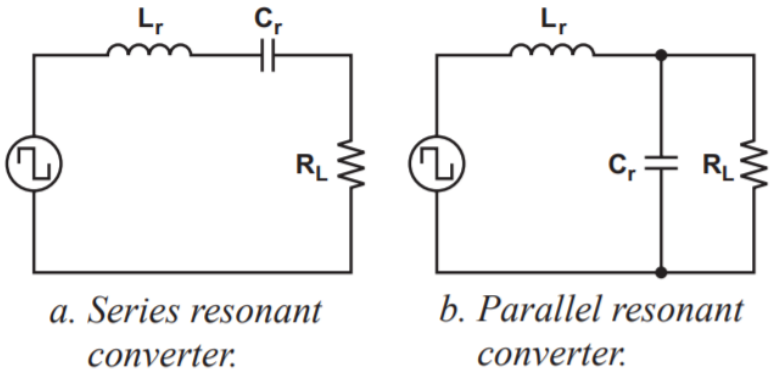

Figure 2.8: Basic series and parallel resonant converters

This very last group of converters (SPLRCs) is able to combine the principal advantages of SLRs and PLRs (i.e. limited short-circuit currents and constant voltage generation) [5]: that is the very reason they are so much studied and analysed. Two main hybrid resonant converter topologies can be found: the LCC converter and the LLC one, which is, in the end, the focus of this thesis work.

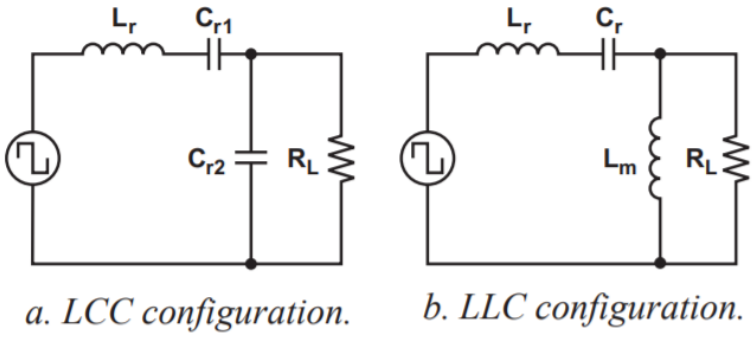

Figure 2.9: Basic hybrid load resonant converters

In order to get a complete look on resonant conversion, not only advantages should be highlighted but also weaknesses. Indeed, many problems affect the resonant conversion technique: first of all, the design can be optimised only for a specific operating point and

not for wide voltage/frequency/load variations; high (or even very high) levels of current can flow into the resonant network when load resistance is very low; efficiency rapidly drops at low output power; sinusoidal or quasi-sinusoidal waveforms yield higher peak values than corresponding triangular ones (typical of hard-switching converters), leading to an increase of conduction losses (i.e. losses across parasitic resistances); the control technique is usually based on a frequency modulation (PFM) rather than a duty-cycle modulation (PWM) and the range of involved frequencies can be very wide; last but not least the complexity of the analysis (and therefore of the design) is substantial with respect to linear and hard-switched solutions.

2.2 LLC overview

Among all the existing resonant converters, the LLC topology, especially in its half-bridge implementation, has experienced growing popularity in the last decades [6]. The schematic of the circuit (without the presence of the control circuitry) is shown in Figure 2.10.

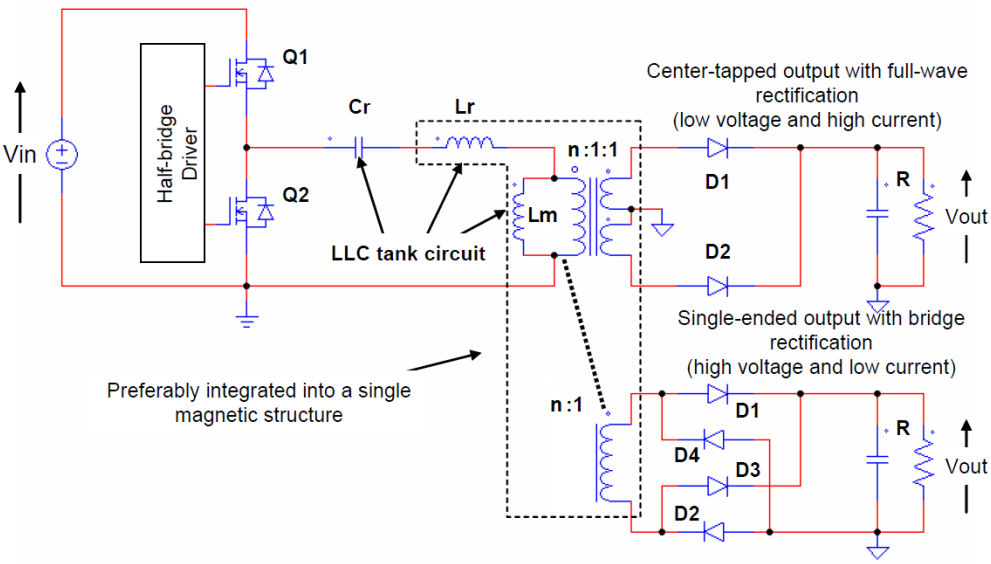

Figure 2.10: LLC circuit schematics

As highlighted in the figure above, for what concerns the rectifier stage, a full-wave (centre-tapped) rectifier is preferred for low-voltage/high-current applications, while a bridge rectifier can be the optimum choice in high-voltage/low-current applications. In fact, in the first case, there is only the voltage drop of one power diode from the secondary windings of the transformer to the output load whereas, in the second case, where the voltage drop across two diodes is not a significant problem, the use of a bridge configuration allows to reduce overall size of the device (four diodes and two windings generally prove to be less bulky than two diodes and three windings). For the sake of completeness, it must be said that some

implementations even exploit synchronous rectifiers instead of power diodes in order to better the LLC converter performances [7].
As in all the other resonant converters, also in the case of the LLC, the typical cascade of blocks can be noticed:

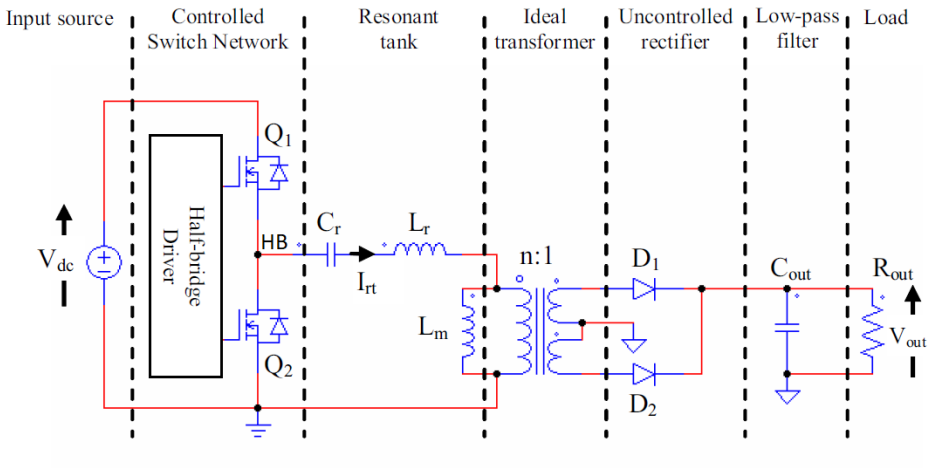

Figure 2.11: Detailed blocks cascade in the case of LLC converters

Despite its increasing use, the main problem regarding the LLC converter is still the absence of precise information about the way it works and, as a consequence, the lack of a systematic, accurate and general design technique. The reasons behind this fact are to be traced mainly to the intrinsic nature of the converter: in fact, another possible classification of the LLC is that of a multi-resonant converter [8]. This class of converters can be considered a particular case of the RPCs, since it includes circuits characterised by more than one resonant frequencies (i.e. where the resonant tank is made of three or more reactive elements). In the specific case of the LLC, given the fact that the resonant circuit consists of two inductors and one capacitor, there are two resonant frequencies associated to the converter:

$$f_{R1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2.1}$$

$$f_{R2} = \frac{1}{2\pi\sqrt{(L_r + L_m) C_r}} \tag{2.2}$$

The first one, i.e. the main resonance frequency (f_{R1}), is related to the condition of secondary winding(s) conducting while the second one, i.e. the second (or lower) resonance frequency (f_{R2}) corresponds to the condition of secondary winding(s) not conducting (i.e. open circuit). Because C_r and L_r characterise the main resonance frequency, they are referred to as resonant capacitor and resonant inductor. It is apparent from eq. (2.1) and (2.2) that $f_{R1} > f_{R2}$: in particular, the distance between the two frequencies depends on the inductance ratio $l_m = L_m/L_r$, as shown in the following equation:

$$\frac{f_{R1}}{f_{R2}} = \sqrt{1 + l_m} \tag{2.3}$$

Therefore the inductance ratio, which is typically set above one, can be a key design parameter since it fixes the ratio between the main resonance frequency and the second one.
Focusing on the switch network, it is interesting to notice that the input signal to the half-bridge (composed by a high-side and a low-side power MOSFETs) is almost always characterised by a 50% duty cycle (apart from special cases, e.g. [9]): this is due to the fact that only this duty cycle is able to equalise, under all operating condition, the electrical stress on the secondary rectifiers (both in terms of reverse voltage and of forward conducting current) since each rectifier carries half of the total output current. Actually, to be precise, a small dead-time is inserted between the on time of the high-side MOSFET and the one of the low-side one: this is of critical importance for the correct (and efficient) behaviour of the converter. Another important aspect to be observed is that the energy-taking (from the input) phase covers a little portion of the whole period in the case of a half-bridge LLC: this can result in poor power handling capability, if the input voltage is low. For this reason, the half-bridge switch network is usually exploited in high input voltage applications (e.g. with a PFC front-end, which provides a 400 V input bus [10]). This limitation can be overcome by using a full-bridge configuration which then allows to improve the operation of the converter.
Moving to the resonant tank, it is useful to point out that the capacitor C_r does not only contributes to the main resonance frequency but it also works as a DC blocking capacitor. In fact, writing the Fourier series expansion of the input square wave excitation (applied to node HB), i.e the bridge leg voltage:

$$V_{HB} = \frac{V_{in}}{2} + \frac{2V_{in}}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin(2\pi n f_{sw} t) \tag{2.4}$$

it is clear that the DC component is equal to $V_{in}/2$. In addition, at steady-state (namely periodic waveforms) the average voltage across inductors is zero which leads to the conclusion that the average voltage across the resonant capacitor is $V_{in}/2$. One of the advantages of the LLC topology comes from the use of the so-called "magnetic integration" [10]: through this technique, not only the ideal transformer but also L_r and L_m can be implemented by a single physical device (a "real" transformer), thus helping to further decrease the converter size. In particular, this is probably the main benefit of the LLC configuration over the LCC one. This is also one of the reasons that lead to the adoption of the all primary referred (APR) model of the transformer in the circuital scheme of the LLC converter, where L_r represents the primary leakage inductance, L_m stands for the magnetising component and there is an ideal transformer (fully described by the number of turns) which regulates the coupling between primary side and secondary side.

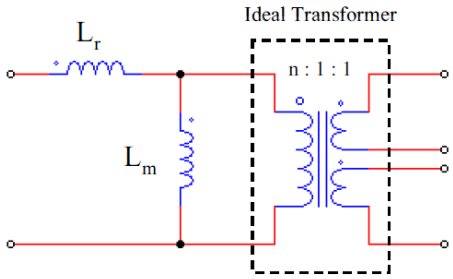

Figure 2.12: APR model of the lossless transformer

Actually, the APR model is derived from the complete lossless physical model of the transformer:

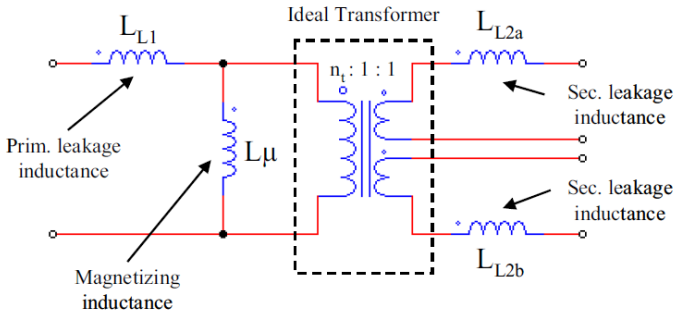

Figure 2.13: Physical model of the lossless transformer

Of course, it is possible to extract the physical parameters of the actual transformer (Figure 2.13) from the "artificial" ones of the APR model (or vice versa), by means of the following relationship:

$$L_r + L_m = L_{L1} + L_\mu \tag{2.5}$$

with the additional assumption of magnetic circuit symmetry, meaning:

$$L_{L2a} = L_{L2b} = \frac{L_{L1}}{n_t^2} \tag{2.6}$$

from which the physical number of turns can be found:

$$n_t = n\sqrt{\frac{L_m + Lr}{L_m}} = n\sqrt{1 + \frac{1}{l_m}} \tag{2.7}$$

Fortunately, it is possible to find many existing transformer structures where the magnetic symmetry is respected (e.g. the ferrite E-core plus slotted bobbin assembly, with an air gap

between the windings [10]). It is useful to point out that secondary leakage inductances are undesired parasitic elements and their effect will be discussed in one of the following sections.
Moving to the rectifier stage, it is useful to underline that, in the LLC converter, also the soft-switching of the secondary rectifiers is achieved, in terms of ZCS (both at turn on and turn off): moreover and more importantly, this property does not depend on the design or on the operating condition.
Finally, it is useful to point out that, when closed in a loop for the control of the output voltage, the LLC allows to increase the level of power by reducing the switching frequency and vice versa (negative feedback), during normal and correct operation.

2.3 The switching procedure

Power MOSFETs are an optimum fit to implement power switches in the case of the LLC switch network because of body diodes and parasitic capacitances [11]. In fact, these two additional devices are naturally embedded into power MOSFETs and they prove particularly useful during the dead-time. Indeed, half-bridge resonant LLC also belongs to the family of resonant-transition converters, i.e. devices where the driving of power switches is such that it produces an excitation of the resonant tank which then offers a zero-voltage drain-to-source condition at their turn on, thus achieving the already mentioned ZVS [8]. In particular, this condition is met by inserting a small dead-time between the conduction of power MOSFETs: therefore, in this case, the dead-time does not simply avoid the conduction overlap of the switches (cross-conduction) but it plays a much more important role.

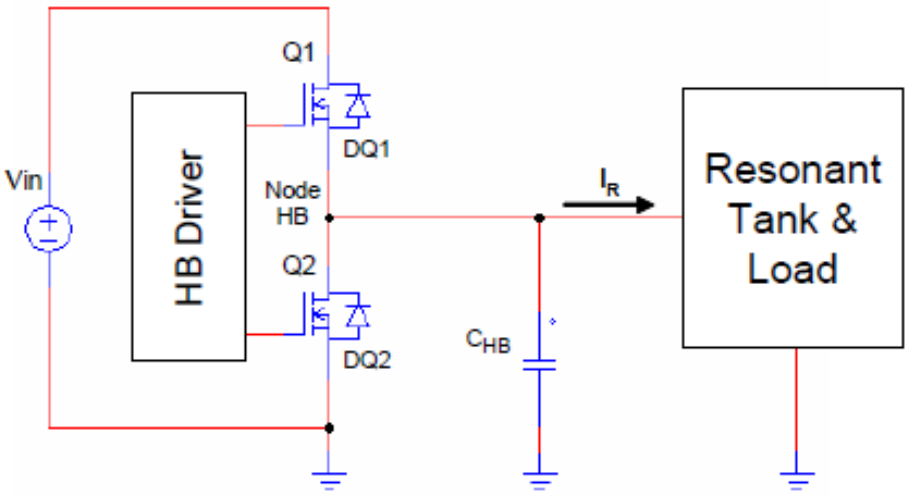

Figure 2.14: Reference scheme for the study of the switching mechanism

In order to better analyse what happens during the dead-time and how ZVS can be achieved,

it is convenient to suppose that initially the high-side MOSFET (Q1) is on and the low-side one (Q2) is off (Figure 2.14). Let's now consider the instant in which Q1 turns off and let's suppose that at this point the current is entering the tank circuit (positive current); since M1 is turning off, its drain-to-source current is rapidly decreasing down to zero; in addition to that, Q2 is still off because of the dead-time; the tank current, however, keeps on flowing with little changes because of the inductance of the resonant tank (L_r) which acts as a current flywheel. The electrical charge needed to maintain this current flow comes initially from C_{HB}, which is initially charged at V_{in} and that therefore starts to discharge. The capacitor C_{HB} simply models all the capacitive contributions at node HB. In this phase, it is as if the inductive portion of the resonant tank resonates with C_{HB} rather than with C_r (this is the concept of resonant transition). Given the fact that the value of the tank current (I_r) at Q1 turn off is large enough, the voltage at node HB (V_{HB}) is able to decrease, within the dead-time, until the turn on of the body diode of Q2 (DQ2), which clamps V_{HB} to $-V_F$ (where V_F is the forward voltage of the body diode): from this instant on, the tank current continues to flow through DQ2 until the end of the dead-time. Finally, when Q2 turns on, its on-state resistance shunts the body diode. Of course, considering the Q2 turn off transition, the reasoning is similar since in that case the only difference is that the tank current is negative and the starting value of V_{HB} is zero. To sum up, it is possible to observe that both Q1 and Q2 turn off with their V_{DS} equal to V_F, which is a voltage negligible with respect to V_{in}, thus achieving ZVS. As a consequence, the turn on transition of the power MOSFETs is performed with negligible dissipation but, on the other hand, the turn off is instead characterised by a non-negligible power dissipation (since in that case $V_{DS} = V_{in}$). Stemming from all these considerations, it can be concluded that a necessary condition for obtaining soft-switching in terms of ZVS at the turn on of the transistors is that the tank current is positive whenever $V_{HB} = V_{in}$ and negative when $V_{HB} = 0$. This condition can be achieved only if the tank current lags the bridge leg voltage V_{HB}. It is useful to highlight that this phase lag is a typical condition in case of inductors. Of course, this is only a necessary condition: the sufficient one is that the inductive energy level associated with the resonant tank (which depends on the resonant current) must be higher than the capacitive energy level of C_{HB} (which is a function of V_{in}) so that the capacitor C_{HB} can be completely discharged before the end of the dead-time. In fact, in order to achieve ZVS at turn on, the transition of the node HB has to be completed within the dead-time.

2.4 Main operating modes

The LLC converter is characterised by a considerable number of different operating modes [12], principally due to its multi-resonant nature: depending on the switching frequency (f_{sw}), on the resistive load and on the characteristics of the resonant tank, the secondary rectifiers can always conduct (Continuous-Conduction-Mode, CCM) or there can be a finite amount of time in which none of them is conducting (Discontinuous-Conduction-Mode, DCM). In a

lossless LLC (as the on the depicted in Figure 2.11), the CCM condition is characterised by the fact that the inductance L_m is always shunted by the load resistance reflected to the primary side (which has the effect of excluding the magnetising inductance from the resonance) while in a DCM condition, there are time intervals in which L_m becomes an active part of the resonance. Given the multi-resonant nature of the converter, it is rather difficult to get a comprehensive picture of all the possible operating modes. Nonetheless, in order to better understand and to put more in detail the main differences in the behaviour of the converter working in the principal operating modes, it is useful to analyse the the main characteristics of an LLC:

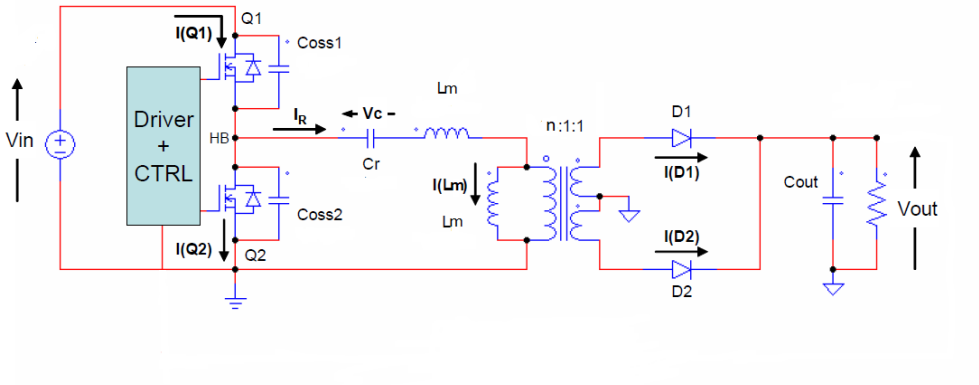

Figure 2.15: LLC reference schematic for the analysis of main operating regions

The figure above shows the schematic of LLC converter (with a full-wave rectifier), that can be therefore simulated (e.g. through a *.tran* simulation performed in LTspice) under difference frequency and load conditions, imposing typical values of the components.

2.4.1 At resonance

Starting from resonance (i.e. fixing the switching frequency to f_{R1} and having a sufficient level of power), it is possible to notice that the operation is always CCM which means that there is always one diode conducting. This also means that the voltage across L_m is constant, resulting in a triangular current flowing on it. Another important consequence of this fact is that the value of L_m does not influence the behaviour of the waveforms at resonance (outside the dead-time) in any significant way because it is always ac-shorted. On the other hand, the presence of L_m is of paramount importance: in fact, the circuit can be seen composed by an LC tank supplying an RL load (where R is represented by the load resistance reflected to the primary side and L is the magnetising inductance), whose effect is the phase-shifting between current and voltage, necessary to achieve ZVS. Without L_m, ZVS could not be reached, not even at resonance because in an LC circuit with a purely resistive load, voltage and current are exactly in phase. The most important relationship characterising the resonance region, in the ideal case, is the following:

$$M(f_{R1}) = \left.\frac{V_{out}}{V_{in}}\right|_{f_{sw}=f_{R1}} = \frac{1}{2n} \tag{2.8}$$

which ties the conversion ratio ($M = V_{out}/V_{in}$) with the turns ratio (n). Of course,as usual in converter applications, as the load resistor value is increased, the CCM operation gradually transforms into DCM.

2.4.2 Above resonance

In this operating mode, which characterises the converter for frequencies above f_{R1}, CCM operation progressively turns into DCM as the output power is reduced and/or the frequency is increased. Furthermore, The conversion ratio is modified with respect to the resonance value: in particular,

$$M(f_{sw} > f_{R1}) = \left.\frac{V_{out}}{V_{in}}\right|_{f_{sw}>f_{R1}} < \frac{1}{2n} \tag{2.9}$$

and the operation of the LLC is referred to as step-down or buck-like, since there is a progressive decrease of the conversation ratio with respect to its value at resonance.

2.4.3 Below resonance

When decreasing the frequency below f_{R1}, the converter enters the most risky operating mode, since only DCM is possible and soft-switching can be more easily lost. The conversion ratio is again modified but in a different direction, meaning that

$$M(f_{sw} < f_{R1}) = \left.\frac{V_{out}}{V_{in}}\right|_{f_{sw}<f_{R1}} > \frac{1}{2n} \tag{2.10}$$

and therefore the LLC is characterised in this region by a step-up or boost-like behaviour. To be precise, this is true for the switching frequencies that can be actually applied to the converter (i.e. that ensure ZVS): instead, when moving to deep below resonance regions, the conversion ratio starts to decrease, just like above resonance.

2.4.4 Cut-off mode (zero output current mode)

This region is entered when an open circuit load is taken into account: in that condition, the current flowing into secondary rectifiers is zero throughout the whole switching cycle. The LLC is ideally able to regulate the output voltage even in cut-off mode at a finite frequency (with proper design of L_m) and this is often considered one of the main benefits of this topology. Of course, this property actually means that the LLC converter is able to control the output voltage even at low output power levels (i.e. with high resistive loads).

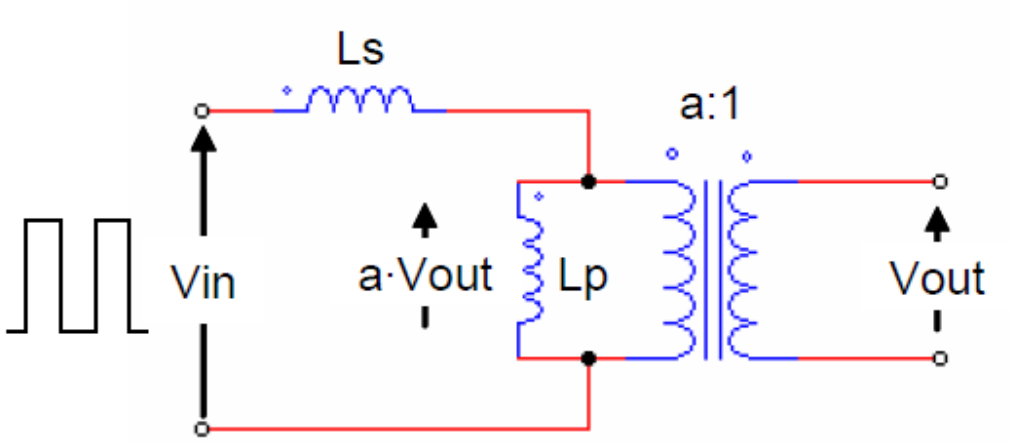

Figure 2.16: Circuit schematic in the case of open-circuit load

2.4.5 Short-circuit load

In this operating mode, L_m is shunted by the short-circuit load reflected back to the primary side: this means that the LLC actually degenerates into a simple LC circuit. As a consequence, the output current will simply be n times the input current. Two major issues afflict this operating region: very high current levels and likely loss of ZVS. In order to limit these problems, overcurrent protection (OCP) circuits are used: they also allow to avoid too high heat dissipation and malfunctioning of the whole system.

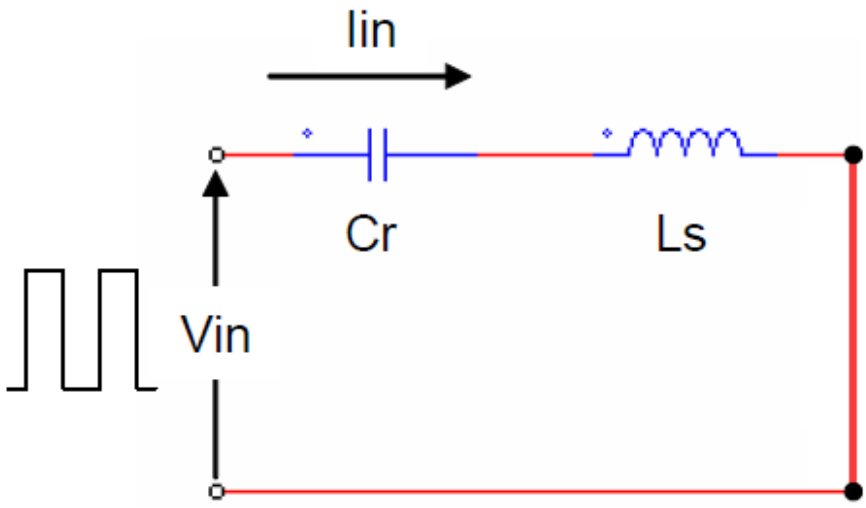

Figure 2.17: Circuit schematic in the case of short-circuit load

2.5 Reactive parasitic elements

Many different reactive parasitic contributions can be found in the circuit. For example, the so-called stray capacitance (depicted in Figure 2.18), which is connected between node HB and ground, includes capacitive effects between the power MOSFETs case and the heat sink, the intra-winding capacitor of the resonant inductor, etc.. This parasitic capacitance is very important especially together with other capacitive contributions related to the non linear time-varying gate-to-drain and drain-to-source capacitors (C_{GD} and C_{DS}) of the high-side and low-side power switches. In fact, as far as voltage variations of node HB are concerned, C_{GD} and C_{DS} are effectively in parallel, which allows to write an overall equivalent expression

$$C_{oss_{1,2}} = C_{GD_{1,2}} + C_{DS_{1,2}} \tag{2.11}$$

In particular, this capacitors can be modelled through an effective constant value, depending on the switching conditions (as shown e.g. in [13]). These equivalent capacitors are present as well in Figure 2.18 and it can be noticed that also C_{oss_1}, C_{oss_2} and C_{stray} are in parallel, when considering voltage variations at node HB. This consideration allows to further lump them all together in a single effective capacitive contribution, useful to analyse the circuit in terms of the soft-switching:

$$C_{ZVS} = C_{HB} = C_{oss_1} + C_{oss_2} + C_{stray} \tag{2.12}$$

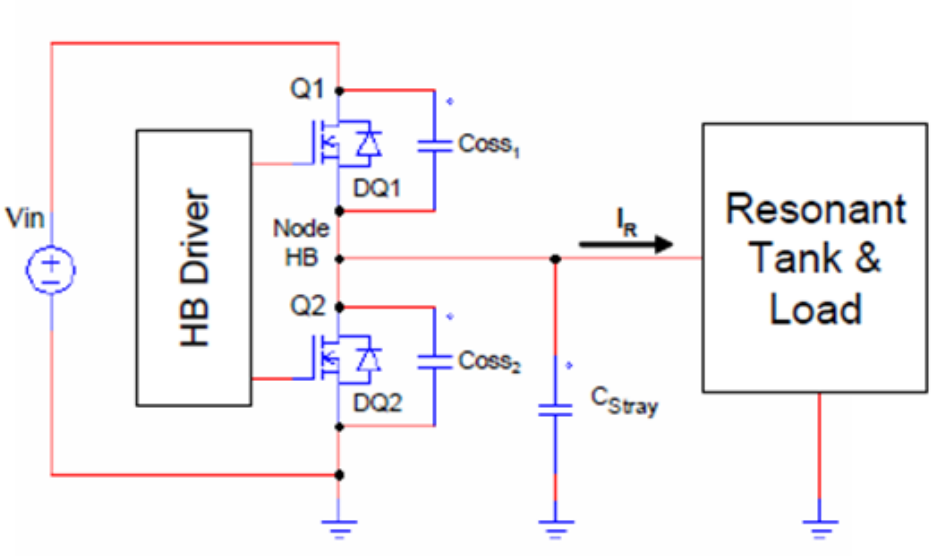

Figure 2.18: Capacitive contributions at node HB

This lumped contribution (C_{ZVS}) is usually referred to as capacitance of the midpoint of the half bridge LLC: this capacitance is the very reason why the transition of this midpoint node (HB) requires energy and therefore takes a finite amount of time to complete.

Another reactive parasitic element consists of the contributions coming from the distributed capacitance of the transformer windings and junction capacitances of secondary rectifiers (reverse-biased power diodes): in combination with the windings inductances, these additional capacitive elements give rise to the so-called transformer «self-resonance» effect. In fact, the contributions of all this parasitic capacitance can be modelled with a single capacitor C_p connected in parallel to Lm.

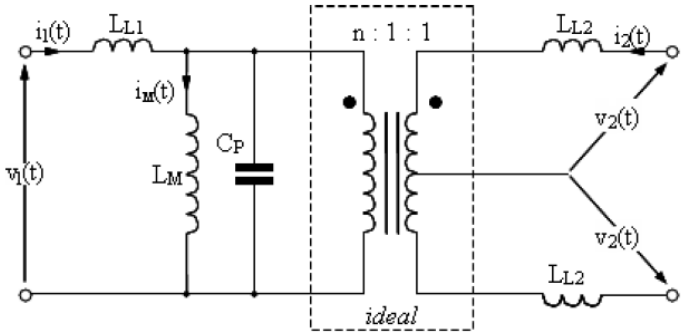

Figure 2.19: Equivalent schematic of a transformer including self-resonance capacitor

Starting from this model, it can be easily seen that the resonant tank circuit turns from a third-order reactive network (LLC) to a fourth-order one (LLCC): this modification leads to the origin of a third resonance frequency, namely f_{LSR}, which is higher than f_{R1}). It is very important to stress the influence of this effect. In particular, when $f_{sw} \ll f_{LSR}$, the impact of C_p is negligible while for $f > f_{R1}$ and for high enough load impedances, its effect becomes relevant eventually resulting in reversing the output power vs frequency relationship. In closed-loop operation, the result of the fact that the power increases with frequency is the so-called «feedback reversal» (i.e. the negative feedback turns into a positive), ultimately meaning the loss of control of the output voltage. Therefore, the converter must always work with $f_{sw} \ll f_{LSR}$: this effect sets the practical upper limit to the maximum operating switching frequency of the LLC converter.
Finally, focusing on secondary leakage inductances, it is worth to underline that they decrease the voltage actually available at the secondary side of the transformer. Furthermore, another drawback shows up when the LLC converter is exploited to drive more loads, through the use of more secondary sides of the transformers. In all of these multi-output LLC converters, cross-regulation between the different outputs is negatively affected because of decoupling effect operated by the secondary leakage inductors.

2.6 Power losses

In order to get a more accurate and realistic analysis of the converter operation, it is certainly very useful to study and design the LLC behaviour considering parasitic resistive

components. In fact, despite the fact that switching losses are very much reduced in the case of the LLC (thanks to soft-switching), conductive power losses may be still present and, since they are the main cause of efficiency drop, it is important to understand where they are located, what is their effect and how they can be reduced. Several factors of conduction power losses can be found in the physical LLC circuit.
In particular, starting with conduction losses at the primary side, it is possible to list the following contributions:

- on-state resistance of the power MOSFETs (R_{on});
- equivalent series resistance (ESR) of C_r;
- high frequency copper losses associated to the primary side of the transformer.

Moving to the secondary side of the transformer, other contributions to the overall conduction losses can be found:

- parasitic resistive losses corresponding to the secondary side of the transformer;
- power diodes series resistances;
- output capacitor resistive effects.

Of course, measured efficiencies of the LLC converter are in any case high/very high, being in the range of about $90 \div 97$ % [10].

Chapter 3

First Harmonic Approximation (FHA)

3.1 FHA analysis

The First (or Fundamental) Harmonic Approximation (FHA) is the most common and easy model which is typically used to obtain a fast (even though strongly approximated) analysis of any resonant power converter [14]. In particular, it can be successfully exploited whenever the input-to-output power transfer is almost completely dependent on the fundamental harmonic component of currents and voltages of the circuit. In the specific case of the LLC converter, as a consequence of the frequency-selective behaviour of the resonant tank, the FHA modelling approach can be exploited, thus neglecting all the higher harmonics of the waveforms ([5] and [10]). This simplification also allows to analyse the circuit in terms of the impedances and transfer functions. The FHA gives quite accurate results for operating points characterised by a $f_{sw} \geq f_{R1}$ and CCM operation (i.e., typically, high power levels). On the other hand, its accuracy decreases moving to DCM operation and in particular moving the switching frequency below resonance. Furthermore, many details of circuit operation are not addressed in any way by the FHA, e.g. the ZCS of the secondary rectifiers. One of the main problems of these approximations is that it is not able to provide a sufficient condition for ZVS across the whole operating curve of the converter.
In order to show how the converter can be modelled through the FHA, it is convenient to start from the ideal schematic of the LLC (show in the following figure), assuming zero dead-time:

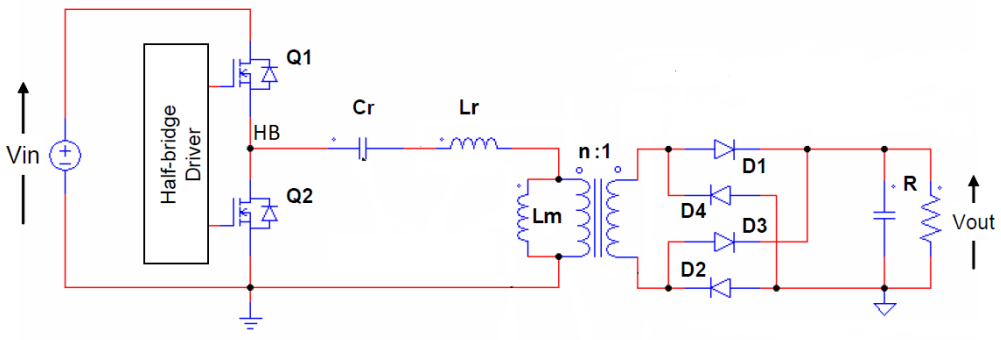

Figure 3.1: LLC starting schematic for the FHA analysis

Since power MOSFETs are driven alternatively with a 50% duty cycle, the voltage at the input of the resonant tank is a square wave (as already mentioned in the previous chapter), whose Fourier series expansion is represented in the following equation:

$$V_{inv} = \frac{V_{in}}{2} + \frac{2V_{in}}{\pi} \sum_{n=1,3,5}^{\infty} \frac{1}{n} \sin(2\pi n f_{sw} t) \tag{3.1}$$

Of course, $V_{inv} = V_{HB}$ but the subscript "inv" specifies, in this case, that this is the voltage at the input of the inverter stage. As can be seen in the equation above, the fundamental component of V_{inv} is

$$V_{inv_{FHA}} = \frac{2V_{in}}{\pi} \sin(2\pi f_{sw} t) \tag{3.2}$$

which is, as expected, a function of the switching frequency (controlling the power MOSFETs). In particular, its root mean square (RMS) value is important for the following computations and it is equal to:

$$V_{inv_{FHA,RMS}} = \frac{\sqrt{2}}{\pi} V_{in} \tag{3.3}$$

Focusing on the secondary side, it can be noticed that also the resulting voltage across the output rectifier is a square wave, whose Fourier expression is

$$V_{rect} = \frac{4V_{out}}{\pi} \sum_{n=1,3,5}^{\infty} \frac{1}{n} \sin(2\pi n f_{sw} t - \psi) \tag{3.4}$$

neglecting the voltage drops across the power diodes. ψ represents the phase shift with respect to V_{inv}. As in the case of inverter input voltage, also for V_{rect}, it is useful to highlight its fundamental component:

$$V_{rect_{FHA}} = \frac{4V_{out}}{\pi} \sin(2\pi f_{sw} t - \psi) \tag{3.5}$$

whose RMS value is

$$V_{rect_{FHA,RMS}} = \frac{2\sqrt{2}}{\pi} V_{out} \tag{3.6}$$

Moreover, the current flowing into the secondary rectifiers is quasi-sinusoidal (actually it is a sine wave plus a linear curve) and, in the frame of the FHA, it is approximated as well with its fundamental component (which is in phase with $V_{inv_{FHA}}$):

$$I_{rect_{FHA}} = \frac{\pi I_{out}}{2} \sin(2\pi f_{sw} t - \psi) \tag{3.7}$$

where the RMS value is represented by:

$$I_{rect_{FHA,RMS}} = \frac{\pi I_{out}}{2\sqrt{2}} \tag{3.8}$$

Due to the zero phase lag between V_{rect} and I_{rect}, the rectifier stage can be simply modelled by an effective resistive load, equal to:

$$R_{o,ac} = R_{o,rect_{FHA}} = \frac{V_{rect_{FHA}}}{I_{rect_{FHA}}} = \frac{8}{\pi^2} R_{out} \tag{3.9}$$

Therefore, as a consequence of all this chain of definitions and approximations, the circuit can be represented with the following two-port model:

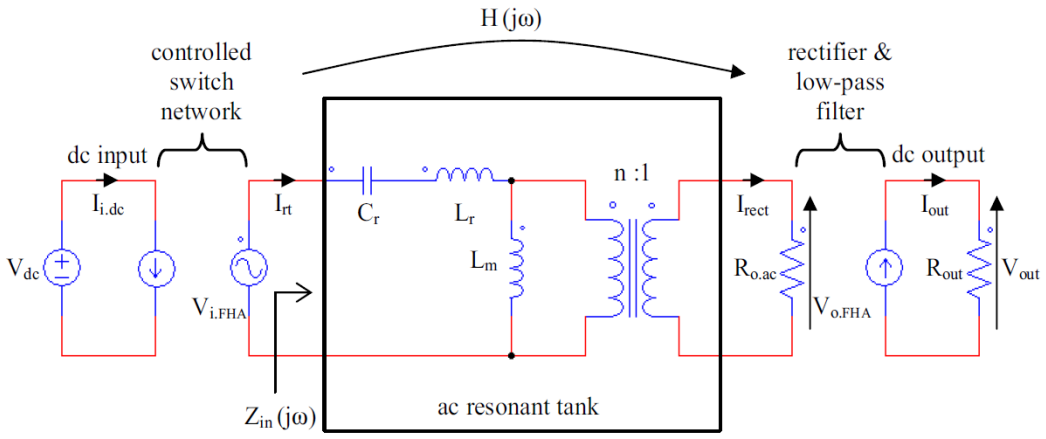

Figure 3.2: Linearised model of the LLC under the FHA

where the input current to the resonant tank (i.e. the resonant current) is denoted as I_{rt}, the voltage at the input of the inverter as $V_{i,FHA}$ and the rectifier voltage as $V_{o,FHA}$. The advantage of analysing the approximate circuit shown in Figure 3.2 over the complete one contained in Figure 3.1 is that the former is fully linear: in particular, it is driven by an effective input sine voltage source and supplies an effective resistive load. Moreover, the resonant tank can be easily analysed in terms of input impedance ($Z_{in_{tank}}$) and voltage forward trans-characteristic (FTC), H_{tank}:

$$Z_{in_{tank}} = V_{i,FHA}/I_{rt} = \frac{1}{sCr} + sL_r + n^2 R_{o,ac}//sL_m \tag{3.10}$$

$$H_{tank} = V_{o,FHA}/V_{i,FHA} = \frac{1}{n}\frac{n^2 R_{o,ac}//sL_m}{Z_{in}} \tag{3.11}$$

The FTC of the tank (also referred to as $H(j\omega)$) is particularly important since its absolute value can be related to the RMS values of V_{rect} and V_{inv} and therefore, indirectly, to V_{out} and V_{in}. Moreover it is possible to write the input-to-output DC-DC voltage conversion ratio as a function of the magnitude of this FTC:

$$M(fsw) = \frac{V_{out}}{V_{in}} = \frac{\left\|H(j2\pi f_{sw})\right\|}{2} \tag{3.12}$$

and, considering the normalised conversion ratio (also named "voltage gain", defined as:

$$m(f_{sw}) \triangleq \frac{M(f_{sw})}{M(f_{R1})} = 2n\frac{V_{out}}{V_{in}} \tag{3.13}$$

the relationship is simply modified as:

$$m(f_{sw}) = n\left\|H(j2\pi f_{sw})\right\| \tag{3.14}$$

The following idea is to compute the expression of the modulus of $H(j\omega)$ with the objective of obtaining the normalised conversion ratio (m) as a function of the switching frequency and other circuital parameters. To do that, the following set of definitions can be exploited:

- resonance frequency,

$$f_r = \frac{1}{T_r} = f_{R1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{3.15}$$

- normalized switching frequency,

$$f_n = \frac{f_{sw}}{f_r} \tag{3.16}$$

- characteristic impedance,

$$Z_0 = \sqrt{\frac{L_r}{C_r}} \tag{3.17}$$

- quality factor of the loaded filter composed by the resonant tank and the load resistance moved to the primary side (i.e. in parallel with L_m),

$$Q = \frac{Z_0}{n^2 R_{o,ac}} \tag{3.18}$$

- inductance ratio,

$$l_m = \frac{L_m}{L_r} \tag{3.19}$$

Combining (3.14) with these definitions, it is possible to find the following expression of the normalized conversion ratio:

$$m(f_n, l_m, Q) = \frac{1}{\sqrt{\left(1 + \frac{1}{l_m} - \frac{1}{l_m f_n^2}\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}} \tag{3.20}$$

Once the explicit expression of m is obtained, it is useful to plot it (e.g. through MATLAB) versus f_n and for different values of Q, fixing a certain inductance ratio (l_m):

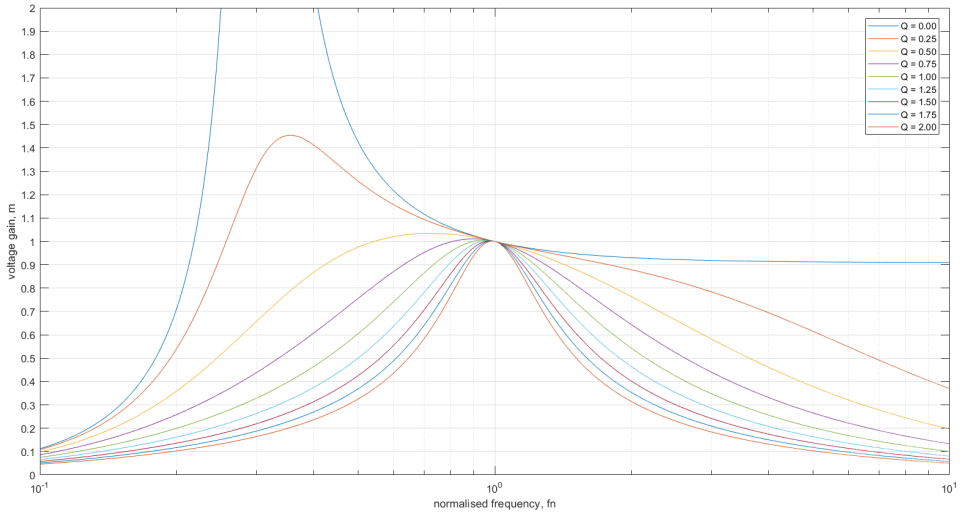

Figure 3.3: Voltage gain characteristics for different values of Q and $l_m = 10$

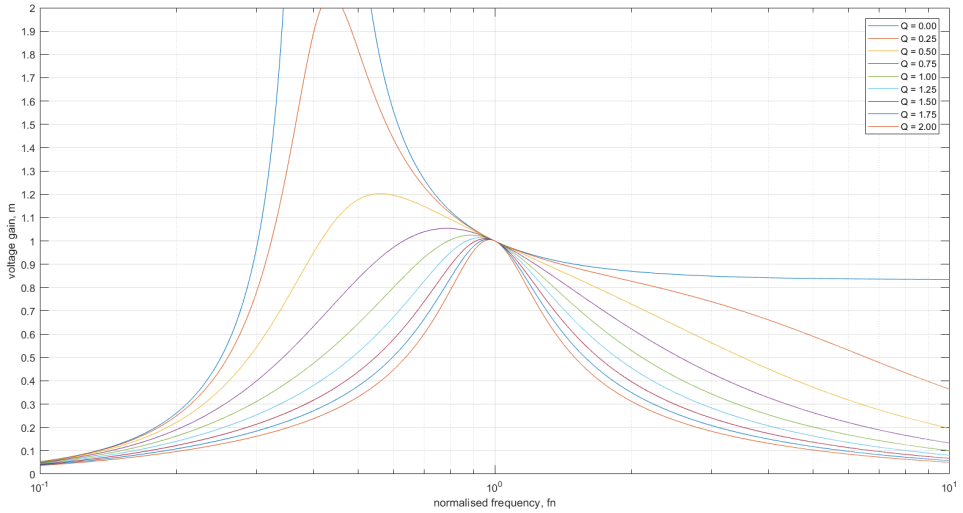

Figure 3.4: Voltage gain characteristics for different values of Q and $l_m = 5$

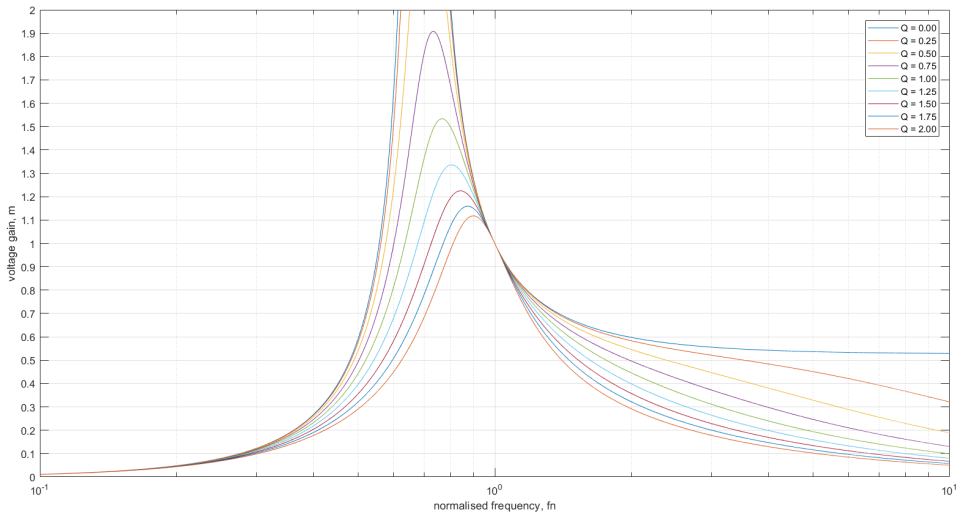

Figure 3.5: Voltage gain characteristics for different values of Q and $l_m = 1.1$

The analysis of the normalised conversion ratio allows to understand how the regulation of the converter output voltage is achieved by changing the switching frequency in response to e.g. a increase/decrease of the input voltage. In fact, the effect of varying the frequency is a variation of the input-to-output voltage gain and therefore it is evident how the output voltage can be kept (almost) constant despite the variations of the input voltage. Of course, the higher the input voltage swing, the wider the frequency range required to restore the desired output voltage. Moving to the influence of the load resistance on the regulated output voltage, the most notable aspect that can be deduced from all the previous plots is the presence of a load-independent point corresponding to the resonance frequency (i.e. $f_n = 1$), where the normalized conversion ratio is obviously equal to 1. Another important remark on the figures is that, once Q (i.e the load resistance) and l_m are fixed, the voltage gain initially increases with frequency until it reaches a peak, after which it starts decreasing with a further frequency rise. The shape of the curves therefore follows a bell-like behaviour. Fixing the inductance ratio and varying the quality factor generates instead a family of curves characterised by different peaks (of m) and different frequencies associated with these peaks: in particular, a reduction of Q (i.e. an increase of the load resistance) causes a left-shift and a rise of the m peak value, eventually leading (for a zero quality factor) to an infinite m value in correspondence of the lower resonance frequency (f_{R2}). The position of this second resonance frequency depends, in turn, on the inductance ratio, as demonstrated by the following equation:

$$f_{n2} = f_{R2}/f_r = \sqrt{\frac{1}{l_m + 1}} \tag{3.21}$$

Therefore, the effect of decreasing l_m is a horizontal shrink of all the curves towards the resonance frequency (f_r) and a resulting increase of the peak values of the voltage gain.

3.1.1 Inductive and capacitive modes

Understanding the behaviour of the conversion ratio is, of course, very important to obtain a clearer picture of how a frequency change can vary the input-to-output relationship but it is not enough. The key idea which allows a more comprehensive analysis of the converter operation is the study of the input impedance of the resonant tank. In fact, the LLC is normally operated in the region where the input impedance of the resonant tank has an inductive behaviour (i.e. it increases with f_{sw}): this means that the power flow can be controlled by changing the operating frequency so that a higher output power is obtained by reducing the frequency and vice versa. This is due to the fact that soft-switching must be ensured in every operating point and in order to reach a ZVS the tank current must lag the impressed voltage which is, as already mentioned, a behaviour typical of inductors. In other words, ZVS occurs only if the tank input impedance is inductive (necessary but not sufficient condition). For this reason, it is very useful to find the boundary (in the conversion ratio vs frequency plot) between the so-called inductive region (i.e. where the input impedance is characterised by an inductive nature) and the so-called capacitive region (i.e. where the input impedance follows a capacitive behaviour and ZVS cannot be certainly ensured).
The first step is to write the normalized input impedance Z_n as a function of f_n, l_m and Q, starting from the expression contained in (3.10):

$$Z_n(f_n, l_m, Q) = \frac{Z_{in}}{Z_0} = \frac{jf_n}{1/l_m + jf_nQ} + \frac{1 - f_n^2}{jf_n} \tag{3.22}$$

By manipulating this expression, it is possible to compute the modulus (magnitude) of Z_n and therefore plot it versus the normalised switching frequency for different values of the quality factor:

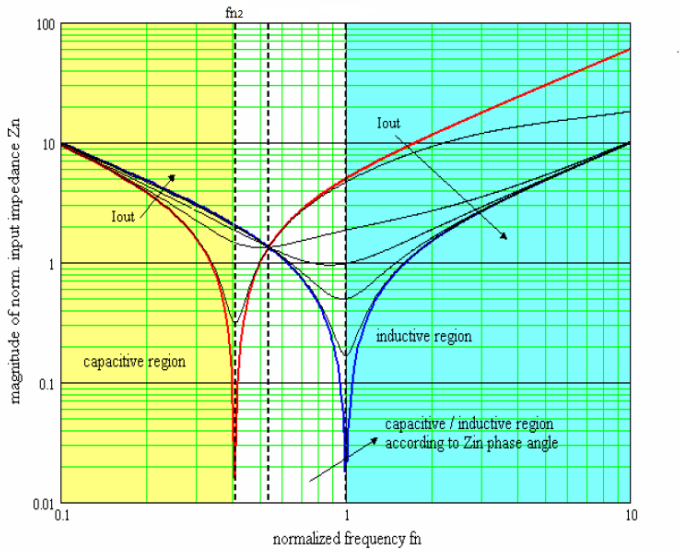

Figure 3.6: Study of the normalised input impedance behaviour

The above plot clearly shows that, for frequencies higher than the resonance one ($f_{sw} > f_{R1}$), the behaviour of Z_{in} is inductive (i.e. the magnitude of the input impedance increases with the switching frequency) while, for frequencies below the second resonance one ($f_{sw} < f_{R2}$), Z_{in} has capacitive nature (i.e. its absolute value decreases with frequency). Between the two resonance frequencies ($f_{R2} < f_{sw} < f_{R1}$), there is a middle region in which Z_{in} can assume either inductive or capacitive behaviour depending on the specific Q value, which tunes the Z_{in} phase angle. This means that for each switching frequency of these middle region, there is a critical maximum quality factor (meaning a critical load resistance), above which the behaviour of Z_{in} can only be capacitive. In order to find the borderline between the capacitive and inductive regions in terms of normalized conversion ratio, it is enough to impose that the imaginary part of Z_n is zero (meaning that Z_n is purely real, which is exactly the boundary between capacitive and inductive behaviour, characterised by a zero phase shift between voltage and current). The result in terms of the critical quality factor, as a function of f_n and l_m, is contained in the following equation:

$$Q_{crit} = \sqrt{\frac{1/l_m}{1 - f_n^2} - \left(\frac{1/l_m}{f_n}\right)^2} \tag{3.23}$$

From this expression, the critical value of the load resistance (above which the operation of the converter lies in the inductive region, even below resonance) can be immediately found:

$$R_{crit} = \frac{\pi^2}{8} \frac{Z_0}{n^2 Q_{crit}} \tag{3.24}$$

As a consequence, it is also possible to find the expression of the critical conversion ratio as a function of the frequency. In particular, in terms of voltage gain:

$$m_{crit} = \frac{f_n}{\sqrt{f_n^2 \left(1 + \frac{1}{l_m}\right) - \frac{1}{l_m}}} \tag{3.25}$$

Therefore the capacitive and inductive region can finally be represented in the m-fn plane:

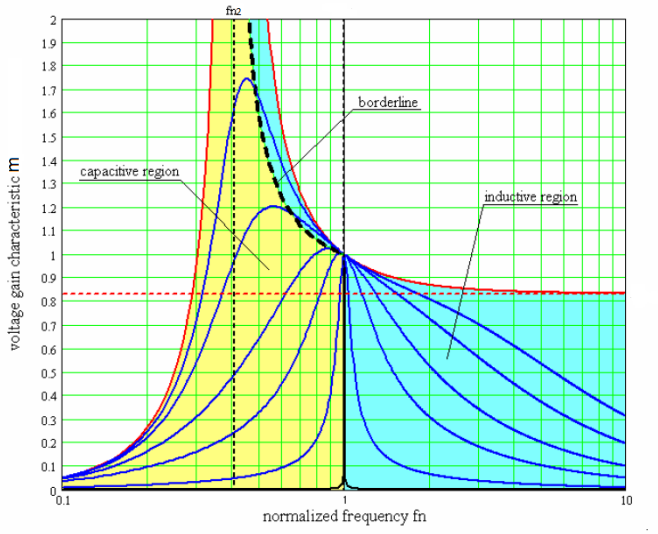

Figure 3.7: Inductive and capacitive regions in the voltage gain characteristic

It is important to point out that as converter operation is moved away from the capacitive inductive boundary towards the inductive region, there is a gradual (not abrupt) passage from hard switching to soft switching.
One important feature of the above plot is that it clearly shows that the peak value of each conversion ratio curve lies inside the capacitive region. This justifies what described in the previous chapter, i.e. the fact that the converter is always used in step-up mode for frequencies below the resonance: in fact further moving below resonance would allow step-down operation at the unbearable cost of losing ZVS (thus losing all of the advantages of using a soft-switching converter). Fortunately, the above resonance region can be successfully used for step-down operation since Z_{in} has inductive behaviour regardless of the output load resistance. Because of this, it is useful to impose that the minimum required voltage conversion ratio (corresponding to the maximum expected input voltage) can be reached at the extreme condition of infinite load resistance (zero quality factor) and at a maximum finite frequency. In particular, starting from the expression of m, evaluated at $Q = 0$:

$$m_{0Q} = \frac{1}{\left|1 + \frac{1}{l_m} - \frac{1/l_m}{f_n^2}\right|} \tag{3.26}$$

and defining:

$$m_{min} = 2n\frac{V_{out}}{V_{in,max}} \tag{3.27}$$

the maximum required normalised frequency found to be equal to:

$$f_{n,max} = \frac{f_{max}}{f_r} = \sqrt{\frac{1}{1 + l_m \left(1 - \frac{1}{m_{min}}\right)}} \tag{3.28}$$

Furthermore, eq. (3.25) can be exploited to find the minimum operating frequency, imposing $m_{crit} = m_{max} = 2n\frac{V_{out}}{V_{in,min}}$ (max required voltage gain, corresponding to the minimum expected input voltage). The minimum required normalised frequency is described by the following equation:

$$f_{n,min} = \frac{f_{min}}{f_r} = \sqrt{\frac{1}{1 + l_m \left(1 - \frac{1}{m_{max}^2}\right)}} \tag{3.29}$$

This expression can be in turn substituted in eq. (3.23) to find the maximum allowed quality factor as a function of m_{max} and λ:

$$Q_{max} = \frac{1/l_m}{m_{max}} \sqrt{l_m + \frac{m_{max}^2}{m_{max}^2 - 1}} \tag{3.30}$$

As a result from all these considerations, it can be concluded that operation at resonance (in CCM) must be preferred because load regulation is ideally zero and tank waveforms are maximally sinusoidal. Therefore the converter must be designed to work at resonance under nominal conditions, below resonance operation must handle input voltage dips and above resonance can well deal with input voltage rises. Lastly, one the most critical aspects of this analysis is that capacitive region must be avoided in every possible way.

3.2 FHA design technique

Based on the analysis conducted on the linearised circuit (Figure 3.2) in the previous section, many different design procedures can be extracted (e.g. the ones described in [15] and [16]). However, one of the most interesting and complete is the one described in [10] and [17], since it exploits the FHA to find also some conditions for imposing ZVS at maximum and minimum frequencies. In particular, given the following list of specifications:

- nominal input voltage, $V_{in,nom}$;
- input voltage range, [$V_{in,min}$, $V_{in,max}$];
- regulated output voltage, V_{out};
- nominal operating frequency, f_r;
- maximum operating frequency, f_{max};

- maximum output power, P_{out};
- total parasitic capacitance at node HB, C_{ZVS};
- dead-time, T_D,

the proposed design flow follows three main general design criteria:

1. the converter is designed to work at resonance under nominal input voltage;
2. the converter must be able to regulate V_{out} even when $P_{out} = 0$ and $V_{in} = V_{in,max}$;
3. the converter must work in ZVS across all the operating range (from a certain f_{min} to a f_{max}).

These three criteria are the guidelines used to find the constraints useful to obtain a complete design of the converter components and they are detailed in the following sections.

3.2.1 Nominal operation

The first criterion simply translates in imposing the nominal normalized voltage conversion ratio at resonance to one ($m(f_n = 1) = 1$), from which the turns ratio of the transformer can be derived:

$$n = \frac{1}{2}\frac{V_{in,nom}}{V_{out}} \tag{3.31}$$

3.2.2 Inductor ratio selection

The second criterion imply that the converter must work at a maximum switching frequency (f_{max}) when regulating the output voltage in the extreme condition of zero output power (open circuit load) and maximum input voltage. Therefore, resorting to eq. (3.28), the inductor ratio can be found as:

$$l_m = \frac{m_{min}}{1 - m_{min}}\frac{f_{n,max}^2 - 1}{f_{n,max}^2} \tag{3.32}$$

3.2.3 Zero-voltage switching condition

The third and last criterion is the most difficult to be fulfilled. To begin with, the ZVS condition can be translated in terms of the phase angle of the input impedance: in fact, this angle equals the shift between the bridge leg voltage and the resonant current (namely ϕ) and therefore it must as well be enough to ensure that V_{HB} is able to reach ground within the end of the dead-time. Moreover, assuming that the duration of the dead-time is negligible with respect to the the switching period, the value of the resonant current can be approximated as a

constant value throughout the whole duration of the dead-time. Following this approximation (and therefore assuming a linear discharge of C_{ZVS}), a condition for the minimum tank current value at the end of the first half-cycle (i.e. when the high-side MOSFET turns off) can be easily found:

$$I_{ZVS} = \frac{C_{ZVS} V_{in}}{T_D} \tag{3.33}$$

In particular, in the FHA model, this current corresponds to the peak amplitude of the reactive component of the overall resonant current:

$$I_{react} = I_{res} sin(\phi) = \frac{I_{ZVS}}{\sqrt{2}} \tag{3.34}$$

while the active component is related to the input active power (which can be assumed equal to the output power in a lossless system):

$$I_{act} = I_{res} sin(\phi) = \frac{P_{in}}{V_{i,FHA}} = \frac{P_{in}}{\frac{\sqrt{2} V_{in}}{\pi}} \tag{3.35}$$

From the active and reactive components, magnitude and phase angle of the resonant current can be found. The phase angle is the element of major interest because, as already stressed, it corresponds to the phase angle of the input impedance. Therefore:

$$I_{res} = \sqrt{I_{act}^2 + I_{react}^2} \tag{3.36}$$

$$tan(\phi)_{min} = \frac{V_{in} I_{ZVS}}{\pi P_{in}} = \frac{C_{ZVS} V_{in}^2}{\pi T_D P_{in}} \tag{3.37}$$

This equation provides the minimum allowed phase angle ensuring ZVS and therefore the sufficient condition for imposing ZVS is the following:

$$tan(\phi) = \frac{Im[Z_n]}{Re[Z_n]} > tan(\phi)_{min} \tag{3.38}$$

However, the solution of the above-equation for obtaining the maximum allowed quality factor at minimum input voltage is not straightforward thus leading to the need of finding an approximate workaround to impose the ZVS condition.
First of all, the idea is to start with the value of the quality factor at the inductive-capacitive border, at minimum input voltage (i.e. Q_{max}, eq. (3.30)). In correspondence of Q_{max}, the input impedance exhibits zero phase angle, meaning that is is purely resistive. Therefore, in order to ensure some phase margin to reach the ZVS condition, the simple idea is to compute a possible quality factor ensuring the expected ZVS as:

$$Q_{ZVS1} = 90\% \div 95\% Q_{max} \tag{3.39}$$

This is the first of the two constraints on the quality factor. In fact, in order to ensure ZVS across the whole operating region, the other extreme condition to be imposed is the one regarding zero output power (i.e. zero quality factor) and maximum input voltage. In this particular operating point, a sufficient constraint can be successfully found since the expression of the input impedance at zero output power can be manipulated more easily. Therefore it is enough to impose:

$$\frac{V_{i,FHA,max}}{\left\|Z_{in,0Q}(f_{n,max})\right\|} \geq \frac{I_{ZVS}(V_{in,max})}{\sqrt{2}} \tag{3.40}$$

with

$$Z_{in,0Q}(f_{n,max}) = Z_{in}(Q=0, f_{n,max}) = jZ_0\left[f_{n,max}\,(1+l_m) - \frac{1}{f_{n,max}}\right] \tag{3.41}$$

Finally the other constraint on the quality factor is found:

$$Q_{ZVS2} = \frac{2}{\pi}\frac{f_{n,max}}{(1+l_m)f_{n,max}^2 - 1}\frac{T_D}{R_{ac}C_{ZVS}} \tag{3.42}$$

Therefore, in order to guarantee full ZVS, the chosen quality factor must fulfil the following condition:

$$Q_{ZVS} \leq min(Q_{ZVS1}, Q_{ZVS2}) \tag{3.43}$$

At this point, it is also possible to compute the corresponding minimum switching frequency, through the following approximate equation:

$$f_{min} \approx f_r \sqrt{\frac{1}{1+l_m\left(1 - \frac{1}{M_{max}^{1+\left(\frac{Q_{ZVS}}{Q_{max}}\right)^4}}\right)}} \tag{3.44}$$

Once all this procedure has ended, the input impedance must be evaluated at $f_{n,min}$, l_m and Q_{ZVS}:

$$Z_n(f_{n,min}, l_m, Q_{ZVS}) = \frac{jf_{n,min}}{1/l_m + jf_{n,min}Q_{ZVS}} + \frac{1 - f_{n,min^2}}{jf_{n,min}} \tag{3.45}$$

in order to check if the sufficient condition for ZVS (eq. (3.38)) is actually respected at minimum frequency, with the chosen quality factor. If the inequality is found to be unverified, a wider margin should be chosen in the computation of Q_{ZVS1}, re-iterating all the procedure previously detailed until the sufficient condition for ZVS is met.

Finally, the values of the converter components can be computed, starting from the computation of

$$R_{ac} = n^2 R_{o,ac} = \frac{8}{\pi^2} n^2 \frac{V_{out}^2}{P_{out}} \tag{3.46}$$

and

$$Z_0 = Q_{ZVS} R_{ac} \tag{3.47}$$

In the end:

$$C_r = \frac{1}{2\pi f_r Z_0} \tag{3.48}$$

$$L_r = \frac{Z_0}{2\pi f_r} \tag{3.49}$$

$$L_m = l_m \cdot L_r \tag{3.50}$$

Following this design methodology leads to the possibility of working with the LLC in the operating region coloured in light blue in the following figure, where the ZVS is always ensured.

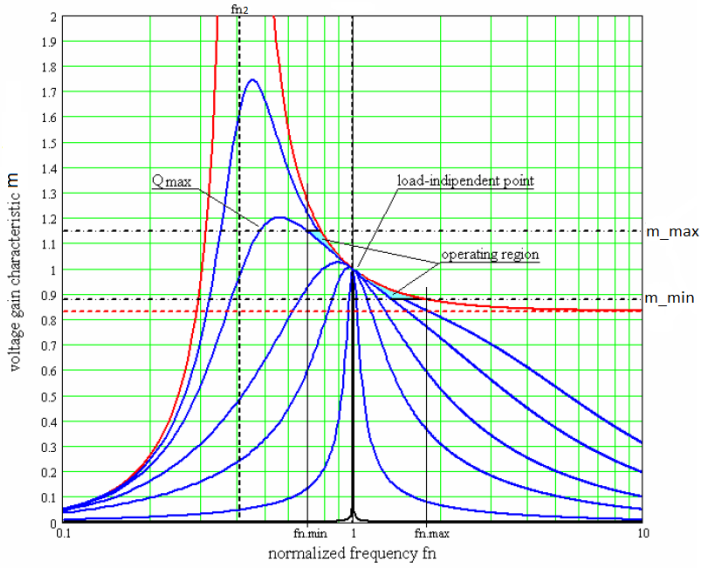

Figure 3.8: Operating region of the LLC converter in the voltage gain characteristic

At this point the design is complete since the LLC is completely determined. A MATLAB script implementing the just described design method is proposed in Appendix A.1, where the re-iteration process is performed through the use of a "for" loop.

3.2.4 Design example

A design example is now provided starting from the following table, where a set of possible design specifications is summarised:

$\mathbf{V_{in,nom}}$ [V]	400
$\mathbf{V_{in,min}}$ [V]	380
$\mathbf{V_{in,max}}$ [V]	420
$\mathbf{V_{out}}$ [V]	30
$\mathbf{P_{out}}$ [W]	300
$\mathbf{f_r}$ [kHz]	120
$\mathbf{f_{max}}$ [kHz]	150
$\mathbf{C_{ZVS}}$ [nF]	400
$\mathbf{T_D}$ [ns]	200

Exploiting the MATLAB script presented in Appendix A.1, the converter components are found and gathered together in the table below:

n [none]	6.67
$\mathbf{C_r}$ [nF]	40
$\mathbf{L_r}$ [µH]	44
$\mathbf{L_m}$ [µH]	315

This example is also useful because it allows to understand the order of magnitude of the typical components of the LLC converter. For instance, for operating frequencies of the order of 100 kHz, the value of the resonant capacitor is generally of the order of tens or hundreds of nF while the resonant inductor assumes values between tens and hundreds of uH. Moreover, the magnetizing inductance is almost always a multiple of Lr but usually does not exceed 10 times the value of the resonant inductor. Finally, as regards the ideal transformer, the turns ratio is often about 10 because the LLC converter, as already highlighted, is usually put at the output of a PFC pre-regulator, which provides a high voltage (generally about 400 V) and the desired LLC output voltage is usually much lower.

Chapter 4

Sequence of switching states approach

As highlighted in the previous chapter, the FHA leads to a strongly simplified model which has the advantage of being very easy analysed but it is not able to accurately match the behaviour of the converter, especially when away from resonance. It is possible to complicate the FHA model by limiting the number of waveforms to be approximated as sinusoidal. This is certainly an improvement and it allows a more realistic description of the converter. However, given the strong non-linearity of the LLC, even this model (namely extended FHA, *eFHA*) is not enough to obtain an accurate description of the circuit. In particular, this is demonstrated by the work of [18]. Furthermore, the FHA analysis is based on the linearised model of Figure 3.2 and on the definition of quality factor and input impedance: this prevents the possibility to compare the approximate model with the signals (voltages and currents) of the physical device. Therefore, a more analytical approach should be followed, resorting to the exact time-domain solution of the LLC converter. One of the most notable attempt pointing in this direction is found in [19], where the main advantage of the developed model is its accuracy, which is independent on the frequency or on the output load, since the full non-linear model is taken into account instead of just its linearised version. Here, this analysis is presented with some variations in the notation and some additional remarks, which are consistent to the work presented in the previous chapter and the following one.
Going more in detail, the analysis procedure starts from the schematic of the converter shown in Figure 4.1 which is manipulated to refer every component to the primary side (APR equivalent model, Figure 4.2) of the transformer with the objective of getting more readable circuital equations.

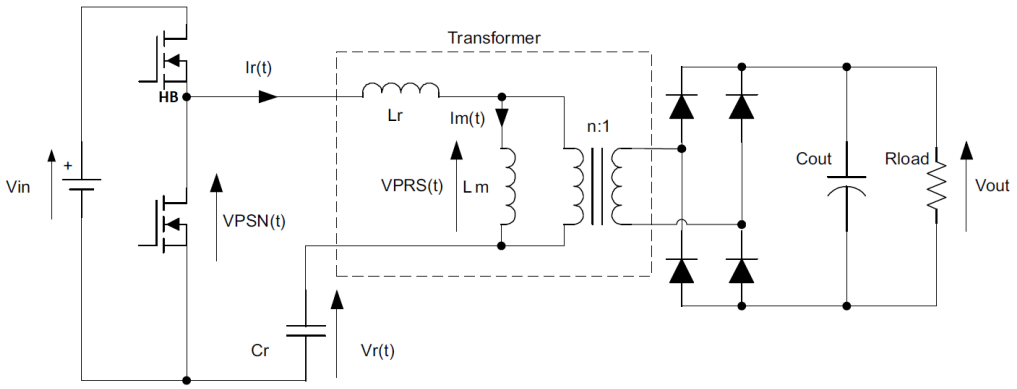

Figure 4.1: LLC converter schematic

Moreover, the APR equivalent circuit is described in terms of normalised voltages and

currents to get a more general analysis. In particular, the adopted normalisation is detailed in the following:

- $Z_0 = \sqrt{\frac{L_r}{C_r}}$
- $\omega_r = \frac{1}{\sqrt{L_r C_r}}$
- $\theta = \omega_r t$
- $m = 2n\frac{V_{out}}{V_{in}}$
- $l_m = \frac{1}{\lambda} = \frac{L_m}{L_r}$
- $I_{rn}(\theta) = I_r(\theta)\frac{Z_0}{V_{in}}$
- $I_{mn}(\theta) = I_m(\theta)\frac{Z_0}{V_{in}}$
- $V_{rn}(\theta) = V_r(\theta)\frac{1}{V_{in}}$

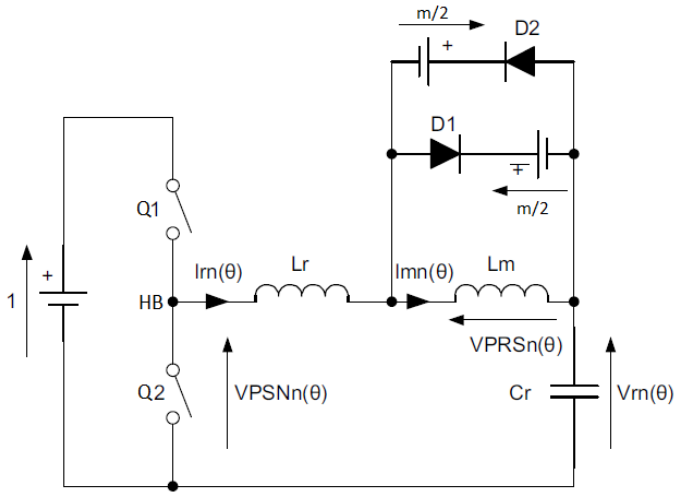

Figure 4.2: LLC converter normalised APR equivalent circuit

Then, the core of the analysis consists in breaking one switching period of the converter (at steady-state) into a sequence of the so-called "switch states", i.e. zones in which the circuit can be fully described and characterised by one or more switching devices in the on state while the remaining ones are off. Each switch state of the circuit can be analytically solved for obtaining the exact expression of all the signals. In particular, assuming to neglect the

duration of the dead-time, there is always one transistor on (at a time) while the power diodes can be on or off, depending on the operating point (e.g. CCM or DCM operation). Therefore, two different circuits (branching from the one depicted in Figure 4.2) can be found to describe the conditions in which one rectifier is on (*MD* equivalent circuit) or both rectifiers are off (*M* equivalent circuit), independently on which MOSFET (high-side or low-side) is on. These schematic are shown in Figure 4.3 and Figure 4.4 while, in the following, the differential equations describing each equivalent scheme are presented and then analytically solved. It is important to underline that the two MOSFETs can be replaced by an ideal normalised voltage source $V_{PSNn} = V_{HB}/V_{in}$ whose value can be either one or zero depending on which transistor is actually on in that particular zone ($V_{PSNn} = 1$ when Q1 is on and $V_{PSN} = 0$ when Q2 is on). Moreover, the rectifiers (moved to the primary side) and the ideal transformer can also be modelled through an ideal normalised voltage source, V_{PRSn}, which assumes the value of $+m/2$ when D1 is on and $-m/2$ when D2 is on while it is disconnected when both rectifiers are off (*M* states). Of course, there can be four possible *MD* states (Q1 on with D1 or D2 on and the analogous with Q2 on) and only two possible *M* states (D1 or D2 on).
Starting from the *MD* equivalent circuit, the following table summarises the values of V_{PSNn} and V_{PRSn} for each different MD state. Each specific *MD* state is referred to as *xMyD*, where $x = 1$ if the high-side MOSFET is on and $x = 2$ if the low-side MOSFET is on, while $y = 1$ if the high-side rectifier is on and $y = 2$ if the low-side diode is on.

	1M1D	**1M2D**	**2M1D**	**2M2D**
$\mathbf{V_{PSNn}}$	1	1	0	0
$\mathbf{V_{PRSn}}$	+m/2	+m/2	-m/2	-m/2

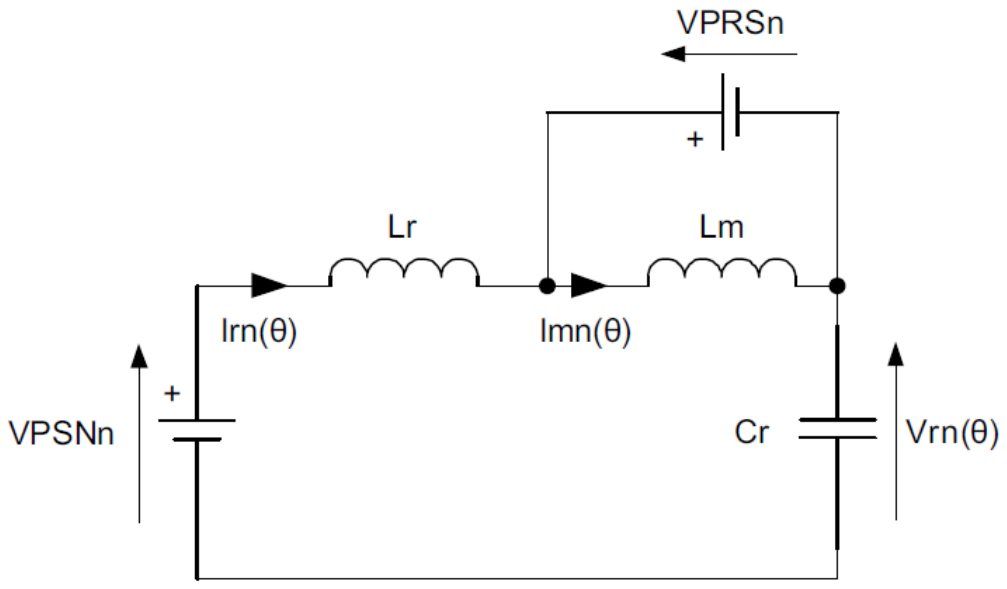

Figure 4.3: *MD* equivalent circuit

The circuit in the above figure is described by the following system of differential equations constraining the main variables:

$$\begin{cases} I_{rn} = \dfrac{\mathrm{d}V_{rn}}{\mathrm{d}\theta} \\ V_{PSNn} = V_{rn} + V_{PRSn} + \dfrac{\mathrm{d}I_{rn}}{\mathrm{d}\theta} \\ V_{PRSn} = l_m \dfrac{\mathrm{d}I_{mn}}{\mathrm{d}\theta} \end{cases}$$

The solution of this system can be found in closed-form and it is reported in the following expressions:

$$I_{rn}(\theta) = (V_{PSNn} - V_{PRSn} - V_{r0n})sin(\theta) + I_{r0n}cos(\theta) \tag{4.1}$$

$$I_{mn}(\theta) = \frac{V_{PRSn} \cdot \theta}{l_m} + I_{m0n} \tag{4.2}$$

$$V_{rn}(\theta) = (V_{PSNn} - V_{PRSn}) - (V_{PSNn} - V_{PRSn} - V_{r0n})cos(\theta) + I_{r0n}sin(\theta) \tag{4.3}$$

where I_{r0}, I_{m0} and V_{r0} are the values of the corresponding variables evaluated at $\theta = 0$. Moving to the *M* equivalent circuit (Figure 4.4), the following table contains the values of V_{PSNn} for each *M* state (V_{PRSn} is not defined in this case). Moreover, since diodes are always off, the states are simply referred to as *xM*, where $x = 1$, if the high-side MOSFET is on, and $x = 2$, if the low-side MOSFET is on. The system of equations characterising *M* states is modified (with respect to the previous case) as follows:

	1M	**2M**
$\mathbf{V_{PSNn}}$	1	0

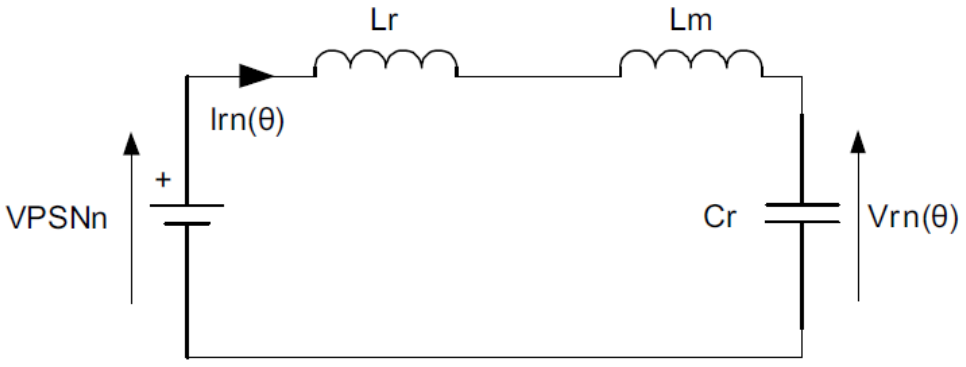

Figure 4.4: *M* equivalent circuit

$$\begin{cases} I_{rn} = \dfrac{\mathrm{d}V_{rn}}{\mathrm{d}\theta} \\ V_{PSNn} = V_{rn} + l_m \dfrac{\mathrm{d}I_{rn}}{\mathrm{d}\theta} + \dfrac{\mathrm{d}I_{rn}}{\mathrm{d}\theta} \end{cases}$$

Since both rectifiers are off in the M states, $I_{rn} = I_{mn}$ (meaning also that current at the secondary side is zero). Therefore, solving the above system of differential equations:

$$I_{rn}(\theta) = \frac{V_{PSNn} - V_{r0n}}{\sqrt{1+l_m}} sin\left(\frac{\theta}{\sqrt{1+l_m}}\right) + I_{r0n} cos\left(\frac{\theta}{\sqrt{1+l_m}}\right) \tag{4.4}$$

$$V_{rn}(\theta) = V_{PSNn} - (V_{PSNn} - V_{r0n}) cos\left(\frac{\theta}{\sqrt{1+l_m}}\right) + I_{r0n}\sqrt{1+l_m} sin\left(\frac{\theta}{\sqrt{1+l_m}}\right) \tag{4.5}$$

4.1 Main operating regions

The equations previously found are very useful to describe the waveforms periodic evolution if the exact sequence of zones is known. In particular, four main operating modes can be found, each of the ones characterised by a different sequence of states:

- above resonance high power (ARHP);
- above resonance low power (ARLP);
- below resonance high power (BRHP);
- below resonance low power (BRLP)

Each of these regions is detailed in the following sub-sections, considering the behaviour of the lossless converter. It is interesting to notice that *M* states start to characterise the operating regions as the output power level decreases (or the frequency is lowered): this is in agreement with the fact that, as already highlighted, CCM operation (i.e. no *M* states) is associated with a higher output power level while DCM (i.e. presence of *M* states) operation is usually found when the output power becomes lower.

4.1.1 Above-Resonance-High-Power (ARHP)

In this region, where the switching frequency is higher than the resonance one (f_r) and the output power level is high, no *M* states are present within a cycle period, meaning that there is always one diode rectifier in the on state (CCM operation). Moreover, at the beginning of each half-period (identified by one of the two MOSFETs in the on state), there is a small

time interval (i.e. angle interval in the normalised model) in which the rectifier forward biased at the end of the preceding half-period stays still on. In other words, the on times of MOSFETs and the ones of the rectifiers are shifted in time (angle), ones with respect to the others. Therefore, in terms of switch states, a complete switching cycle is characterised, in this region, by the following sequence:

	1M2D	**1M1D**	**2M1D**	**2M2D**
$\mathbf{V_{PSNn}}$	1	1	0	0
$\mathbf{V_{PRSn}}$	-m/2	+m/2	+m/2	-m/2

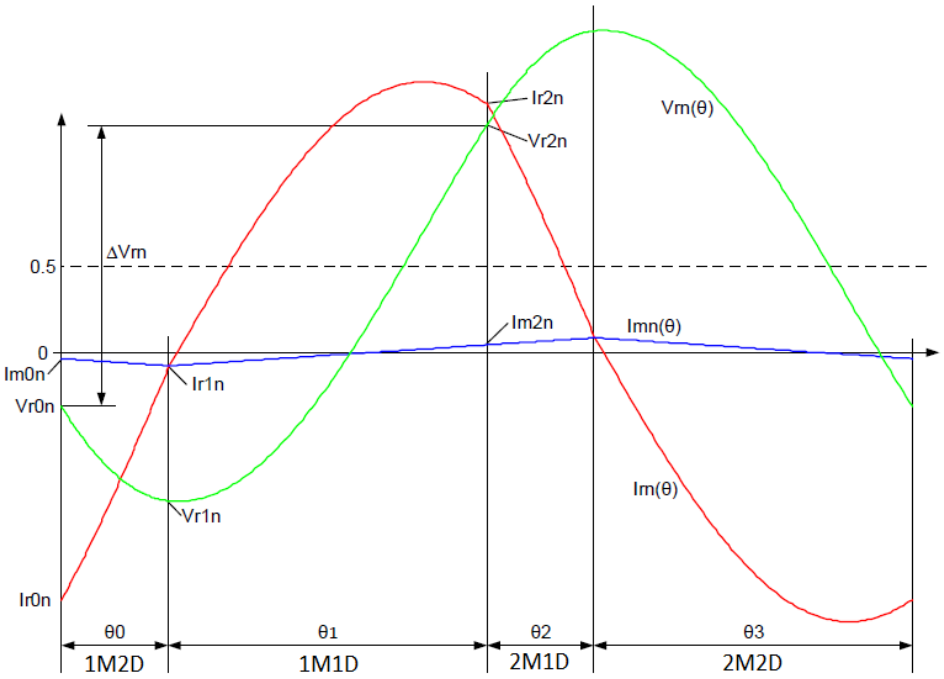

Figure 4.5: Normalised waveforms example (ARHP region: $m = 0.6$, $l_m = 5$, $\Delta V_{rn} = 1.642$)

The main waveforms of the converters, working in the ARHP region, are shown in the figure above. A MATLAB script which is able to find of all the unknowns (I_{m0n}, I_{r0n}, $\theta 0$, $\theta 1$) needed to plot the above-shown waveforms, once a given triple (m, l_m, ΔV_{rn}) is chosen, is provided in Appendix A.2. Finally, it is useful to point out that ΔV_{rn} simply represents the gradient of V_{rn} between its value at half-period and its initial one (V_{r0n}): therefore, once ΔV_{rn} is set, V_{r0n} can be simply found computing $\dfrac{1 - \Delta V_{rn}}{2}$.

4.1.2 Above-Resonance-Low-Power (ARLP)

Keeping the frequency above the resonance value and moving towards lower output power levels allows to simulate a different operating region. In this case, the sequence of states

describing one complete period is different from the one described in the previous subsection: in particular, with respect to the ARHP sequence, each half-cycle simply integrates an additional *M* state. This modification suggests that there are time (angle) intervals in which none of the rectifiers is on (DCM operation). The exact sequence of states characterising this region is summarised in the following table and then an example showing the main waveforms is provided:

	1M2D	**1M**	**1M1D**	**2M1D**	**2M**	**2M2D**
$\mathbf{V_{PSNn}}$	1	1	1	0	0	0
$\mathbf{V_{PRSn}}$	-m/2	NaN	+m/2	+m/2	NaN	-m/2

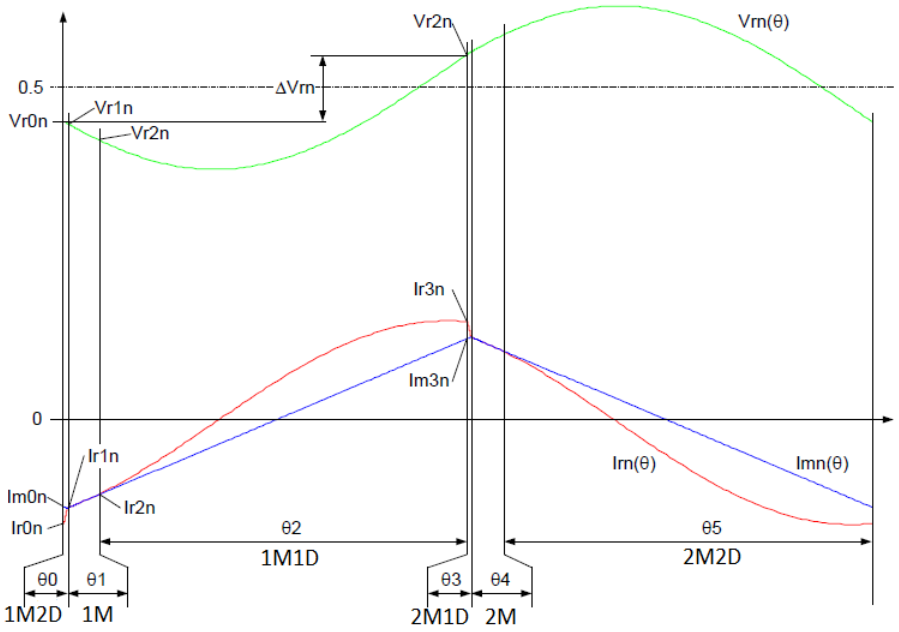

Figure 4.6: Normalised waveforms example (ARLP region: $m = 0.94$, $l_m = 5$, $\Delta V_{rn} = 0.1$)

4.1.3 Below-Resonance-High-Power (BRHP)

Lowering the input frequency below f_{R1} leads the LLC converter into different operating regions. In particular, in agreement to what said in the previous chapter, there is no CCM possible below resonance that allows at the same time ZVS. Therefore, independently on the output power level, the operation of the converter, below resonance, will happen in DCM. This consideration justifies the presence of *M* states in both BRHP and BRLP regions. On the other hand, even below resonance there is a difference in terms of sequence of states when varying the output power level. Starting from the BRHP region, it is possible to notice the presence of only one *M* state in each half-cycle, leading to the following sequence:

	1M1D	1M	2M2D	2M
$\mathbf{V_{PSNn}}$	1	1	0	0
$\mathbf{V_{PRSn}}$	+m/2	NaN	-m/2	NaN

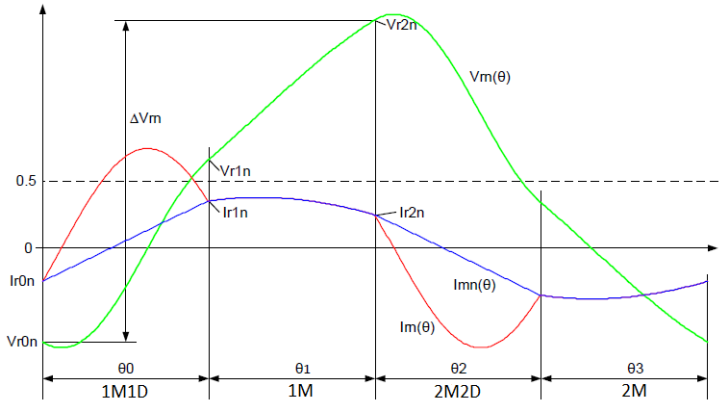

Figure 4.7: Normalised waveforms example (BRHP region: $m = 2$, $l_m = 5$, $\Delta V_{rn} = 2.4$)

4.1.4 Below-Resonance-Low-Power (BRLP)

Moving to the condition of low output power (always staying below resonance), the number of *M* states per half-period increases to two (which is consistent with the fact that DCM operation becomes more pronounced when lowering the output power). In particular, the sequence of zones describing the evolution of LLC waveforms at BRLP is shown in the following table:

	1M	1M1D	1M	2M	2M2D	2M
$\mathbf{V_{PSNn}}$	1	1	1	0	0	0
$\mathbf{V_{PRSn}}$	NaN	+m/2	NaN	NaN	-m/2	NaN

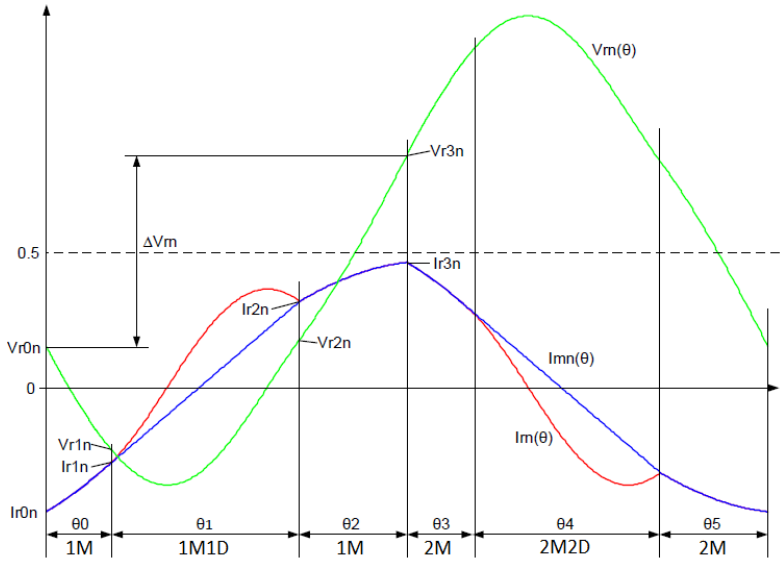

Figure 4.8: Normalised waveforms example (BRLP region: $m = 2$, $l_m = 5$, $\Delta V_{rn} = 0.7$)

4.2 Region boundaries

As shown in all of the previous figures containing examples of normalised waveforms, a steady-state operating point can be fully defined by a set of three main variables (namely m, l_m, ΔVrn). Then, imposing several constraints (e.g. Appendix A.2) regarding the periodicity of the signals and the proper sequence of zones, the evolution of the waveforms (for that specific operating point) can be represented. Therefore, the main issue is to find the correct sequence of states corresponding to each possible triple of m, l_m, ΔVrn. With the objective of finding this correspondence, the idea is to compute all the boundaries between different regions and obtain, as a consequence, a chart able to map any given set of LLC main parameters onto a specific region (i.e. a specific sequence of zones). In particular, each boundary is expressed in terms of ΔV_{rn} as a function of m, for a given l_m.

4.2.1 ARHP-BRHP (Resonance-High-Power, RHP)

The most important boundary is the one related to the resonance operation ($f_{sw} = f_{R1}$) at high power (CCM), that is the nominal condition for which the converter is usually designed. This fundamental border can be characterised by considering the switching states in common between ARHP and BRHP regions: therefore, the RHP sequence of states simply consists of two *MD* zones (as shown in the following table).

	1M1D	**2M2D**
$\mathbf{V_{PSNn}}$	1	0
$\mathbf{V_{PRSn}}$	+m/2	-m/2

It is apparent from the table above that the RHP boundary is the only possible condition in which on states of the power MOSFETs and the ones of the corresponding power diodes are exactly in phase (that leads to smoother and maximally sinusoidal waveforms).

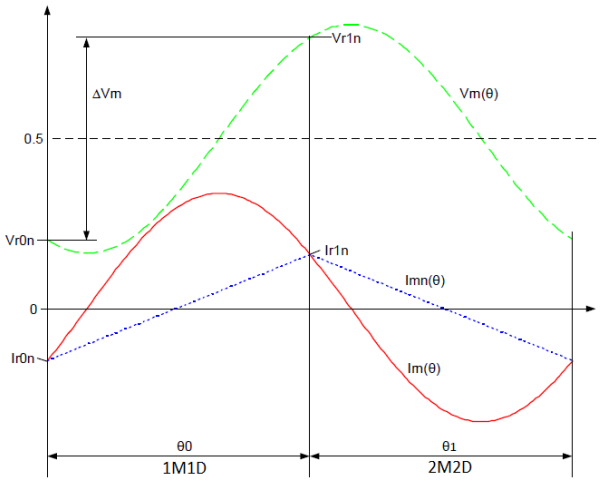

Figure 4.9: Normalised waveforms example (RHP boundary: $m = 1$, $l_m = 5$, $\Delta V_{rn} = 0.6$)

Moreover, along the RHP boundary, some additional constraints on the differential equations can be found:

$$\theta 0 = 2\pi \frac{1}{2f_r} f_r = \pi \tag{4.6}$$

$$I_{r0n} = I_{m0n} \tag{4.7}$$

$$I_{r1n} = -I_{r0n} = I_{m1n} = I_{r0n} + \frac{m}{2}\frac{\pi}{l_m} \tag{4.8}$$

from which, the following equation is extracted:

$$I_{r0n} = -\frac{m}{4}\frac{\pi}{l_m} \tag{4.9}$$

Another peculiarity of the RHP border is the fact that $m = 1$ independently on the output power (in agreement to what seen within the frame of the FHA model). In fact, starting from eq. (4.3), the following limit can be computed:

$$\lim_{\theta \to \pi^-} V_{rn}(\theta) = V_{rn}(\pi^-) = 2 - m - V_{r0n}$$

Then, exploiting the following relationship:

$$\lim_{\theta \to \pi} V_{rn}(\theta) = V_{r1n} = V_{r0n} + \Delta V_{rn} = -V_{r0n} + 1$$

(which simply tells that the limit exists and it returns its value), it can be concluded that

$$V_{r1n} = V_{rn}(\pi^-) \tag{4.10}$$

thanks to the theorem on the uniqueness of limits. This last equality finally leads to $m = 1$. It is interesting to observe that, since the voltage gain is fixed at one along the RHP border, both I_{r0n} and I_{r1n} are only dependent on l_m (eq. (4.9)). In particular, it can be useful to compute the de-normalised value of I_{r1n}:

$$I_r(T_r/2) = I_{r1n}\frac{V_{in}}{Z_0} = \frac{\pi V_{in}}{4}\frac{L_r}{L_m}\sqrt{\frac{C_r}{L_r}} = \frac{V_{in}}{8L_m}\frac{1}{f_r} \tag{4.11}$$

In order to achieve ZVS, this current level must be higher than the minimum one required to switch the voltage at node HB within the specified dead-time (i.e. I_{ZVS}, eq. (3.33)). Imposing this condition, a constraint on the maximum magnetising inductance can be found:

$$L_m \leq \frac{T_D}{8f_r}\frac{1}{C_{ZVS}} \tag{4.12}$$

4.2.2 ARHP-ARLP

The boundary between ARHP and ARLP regions can be characterised in terms of voltage constraints. In particular, starting from the sequence of states of ARHP and imposing that the de-normalised voltage across L_m is at the minimum possible value able to turn on the secondary rectifier D1 at the end of the *1M2D* state allows to simulate this border condition. Therefore, the following constraint must be added to the system of equations for finding the unknowns (ΔV_{rn}, in particular):

$$V_{r1n} = 1 - \frac{m}{2}\left(\frac{l_m + 1}{l_m}\right) \tag{4.13}$$

Further lowering the output power would lead to an insufficient voltage on the anode of D1 so that the *1M2D* zone would be followed by a *1M* state (ARLP region) rather than a *1M1D* one (ARHP region).

4.2.3 BRHP-BRLP

This boundary simply represents the condition in which the converter operation switches from a high-power region to a low-power one, when the frequency is above the resonance value and it is therefore analysed in a similar way with respect to the border of the previous sub-section. In particular, to find the corresponding steady-state operating points, it is enough to consider as a constraint the voltage across D2. In fact, if this voltage is exactly equal to $V_{out} + V_{D2,on}$ (in terms of de-normalised values) at the start of the first half-cycle of BRHP operation, it means that the output power level is just enough for starting the sequence of

states with an *MD* state. This considerations translates into the fact that the BRHP-BRLP is represented by the following relationship:

$$\Delta V_{rn} = m\left(\frac{l_m + 1}{l_m}\right) - 1 \tag{4.14}$$

By further reducing the power level, the sequence of zones is modified as it begins with an *M* state (*1M*) meaning that BRLP region is entered.

4.2.4 Zero-Current-Switched (ZCS)

This is the non-linear equivalent of the inductive-capacitive boundary computed within the FHA frame and therefore mainly concerns below-resonance operation. In particular, the ZCS border can be found by imposing that the resonant current at the end of the first half-period (considering BRHP operation) is zero (i.e. $I_{r2n} = -I_{r0n} = 0$). This condition is the one in which the resonant current flowing in the tank and the V_{HB} voltage are exactly in phase and therefore ZVS has already been lost (because there is certainly not enough current to discharge C_{HB}).

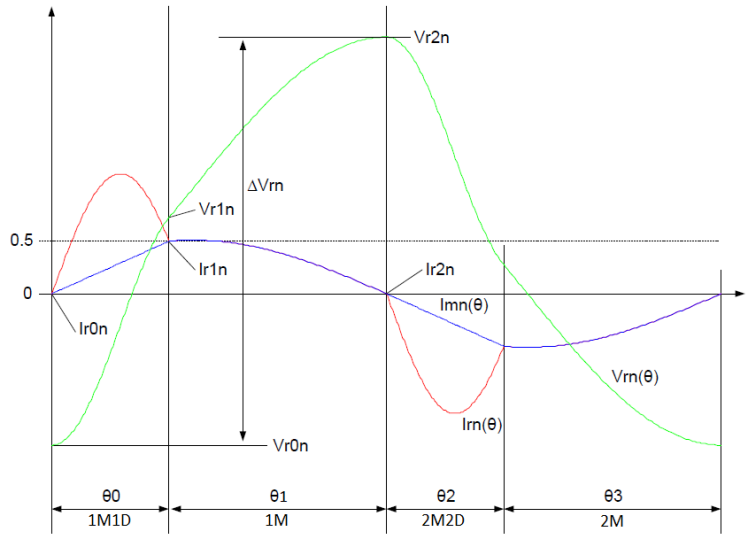

Figure 4.10: Normalised waveforms example (ZCS border: $m = 2.6$, $l_m = 7$, $\Delta V_{rn} = 3.88$)

4.2.5 Resonant-Reversal (RR)

This condition is also mainly related to the most risky operating region (BRHP) and it is found as a boundary with higher-power/lower-frequency regions, characterised by the presence of one *1M2D* state at the end of the first half-period. Therefore, in order to compute the RR boundary, it must be imposed that the voltage across D2 is just enough to turn it on at the end of the first half-cycle. In particular, the relationship characterising this boundary is the following:

$$\Delta V_{rn} = m\left(\frac{l_m + 1}{l_m}\right) + 1 \tag{4.15}$$

Actually the RR boundary gives looser constraints than ZCS for the most part of the below-resonance region but it is used as an actual upper boundary for ensuring ZVS operation for the remaining parts of the below-resonance and also above-resonance. In fact, when a *1M2D* state is found at the end of the first half-period, there is a corresponding drop of the resonant current which, as soon as the frequency is reduced or the power increased, can rapidly lead to the loss of ZVS. Since ZCS and RR boundaries can give more or less tight constraints on the maximum ΔV_{rn}, it is recommended to consider a mix of the two, named ZCS/RR boundary, which simply consists of the minimum between $\Delta V_{rn,ZCS}$ and $\Delta V_{rn,RR}$.

4.2.6 Map of operating regions

Computing the values of ΔV_{rn} as a function of m (for different l_m), corresponding to the previously-described boundary conditions, leads to the map addressed at the start of this section. This chart (shown in the figure below) is very useful to analyse the converter across different operating regions but it is also important as a starting point for building a more precise design procedure.

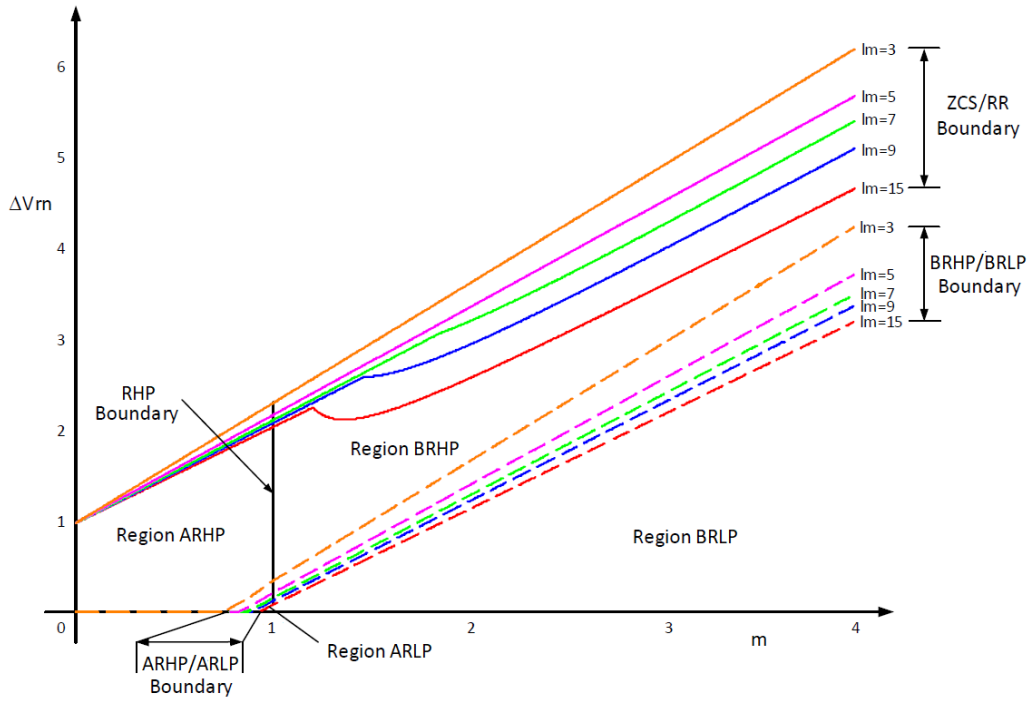

Figure 4.11: Plot of operating regions and boundaries

One of the limitations of this model is that it does not address what happens at the boundary between ARLP and BRLP regions. Another issue is that the map of the regions does

not explicitly contains any quantitative frequency information. Furthermore, the use of ΔV_{rn} as a characterising parameter is not very practical because it is a quantity related to the voltage gradient of the resonant capacitor rather than a parameter coming from a specification. However, ΔV_{rn} gives a rough estimate of the output power (current) level, for a given a voltage gain, as can be qualitatively seen from Figure 4.11. This statement can be easily demonstrated in the case of the RHP boundary, by relating the expression of the de-normalised output current (I_{out}) to ΔV_{rn}. In particular, referring to the de-normalised circuit (Figure 4.1), I_{out} can be found as:

$$I_{out} = \frac{P_{out}}{V_{out}} = n \cdot mean(I_r - I_m) = \frac{2n}{T_r} \int_0^{T_r/2} (I_r - I_m) dt \tag{4.16}$$

Considering that

$$\int_0^{T_r/2} I_r dt = C_r[V_r(T_r/2) - V_r(0)] = C_r \Delta V_{rn} V_{in} \tag{4.17}$$

and that, for $0 < t < \frac{T_r}{2}$, the integral of I_m is zero, the integral of eq. (4.16) can be easily solved and, re-arranging the terms, it is possible to write the expression of ΔV_{rn} as a function of I_{out}:

$$\Delta V_{rn} = \frac{I_{out}}{2n} \frac{T_r}{C_r} \frac{1}{V_{in}} \tag{4.18}$$

This expression can be also used to compute the minimum current level ensuring to work at resonance in CCM (i.e. along the RHP boundary). In particular, writing I_{out} as a function of ΔV_{rn}:

$$I_{out} = 2nV_{in} \frac{C_r}{T_r} \Delta V_{rn} \tag{4.19}$$

and imposing the value of ΔV_{rn} at the boundary between BRHP and BRLP (eq. (4.14)) for $m \to 1$, it is found that the value of $I_{out,min}$ is:

$$I_{out,min} = 2nV_{in} \frac{C_r}{T_r} \frac{L_r}{L_m} = n \frac{V_{in}}{\pi} \frac{\sqrt{C_r L_r}}{L_m} \tag{4.20}$$

4.3 Design proposal

Also in this case, a design procedure can be based on the analysis: the advantage is its level of accuracy, since it can make use of the exact expression of voltages and currents (of the lossless converter). This design method is explicitly proposed as an alternative the one derived from the FHA in [20]. In particular, it useful to notice that, once a steady-state operating point has been computed through the previously described analysis, any circuital signal (voltage, current, power etc..) can be computed. Therefore, the idea proposed in [19]

is to compute the so-called "current loss factor" (CLF) and to use it as a figure of merit for narrowing the design choice. This parameter is in fact a rough qualitative measurement of the conduction losses inside the circuit and it is defined as follows:

$$CLF = \frac{I_{pri,RMS}^2 + I_{sec,RMS}^2}{I_{in,avg}^2} \tag{4.21}$$

where $I_{pri,RMS}$ and $I_{sec,RMS}$ are the RMS values of the primary and secondary side currents while $I_{in,avg}$ represents the input average current. Therefore, CLF is evaluated for different operating points in order to understand its behaviour. The main results are summarised in the following two figures:

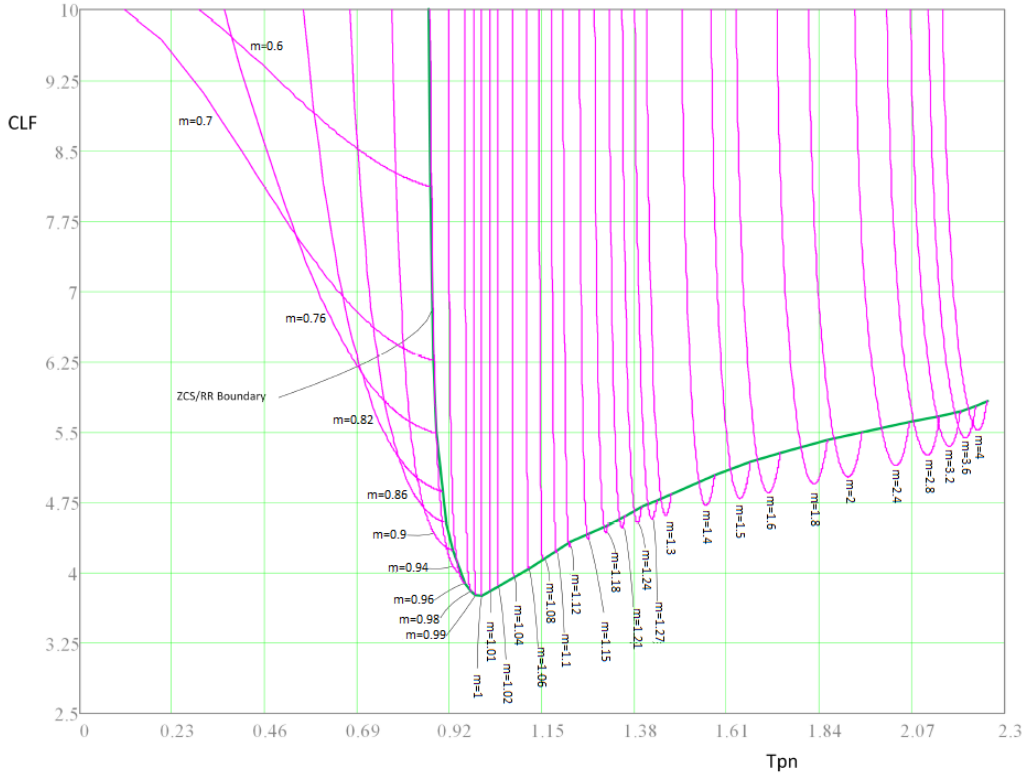

Figure 4.12: Plot of CLF as a function of normalised switching period ($T_{pn} = T/T_r$) for different values of ΔV_{rn} (pink curves) and $l_m = 5$

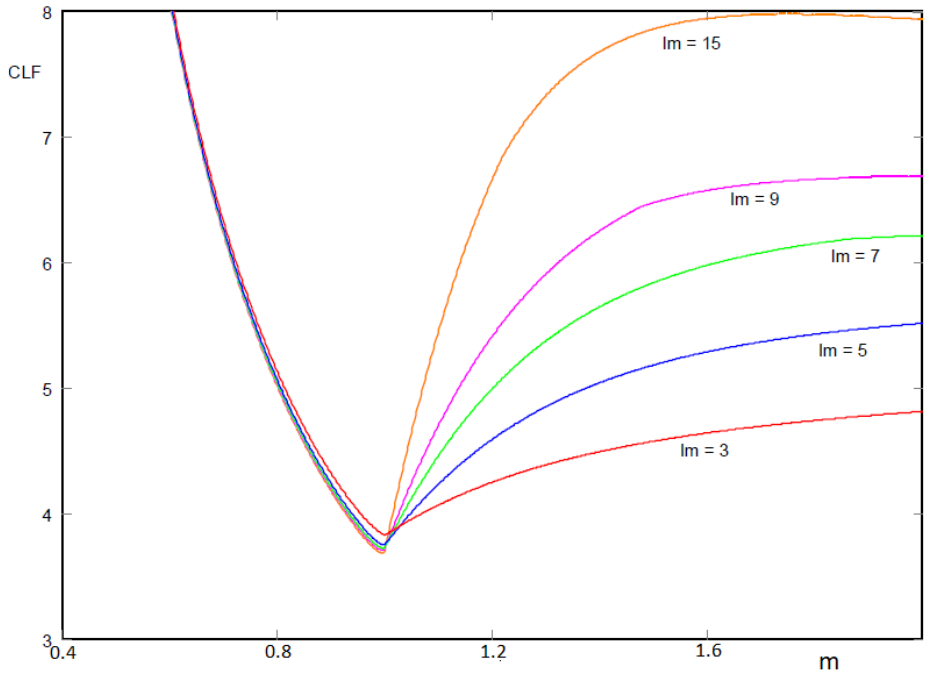

Figure 4.13: Plot of CLF as a function of m, for different values of l_m

In particular, from Figure 4.12, it can be understood that, for a given inductor ratio, the most efficient region in which the converter can operate is close to the ZCS/RR boundary, where conduction losses are at their minimum value. Furthermore, Figure 4.13 clearly shows that a lower value of l_m must be preferred in order to minimise power losses in the region above-resonance. The last important consideration which can be derived from both Figure 4.12 and Figure 4.13 is that losses rapidly increases when moving away from resonance (particularly in the below-resonance direction) and it is therefore recommended to limit the switching frequency range (which unfortunately results in a reduced m range). As a consequence of all these considerations, the actual design flow can be presented. In particular, the procedure is detailed in three main steps, described in the following.

4.3.1 Turns ratio selection

The LLC is usually expected to regulate the output voltage to a fixed value, regardless of input voltage variations $[V_{in,min}, V_{in,max}]$. The actual voltage conversion ratio of the converter depends on both turns ratio and normalised conversion ratio m. As underlined before, the m range should be very limited with the objective of limiting conduction losses. In particular, a reasonable choice is to choose constrain m inside the range of $[0.7, 4]$. Therefore, the turns ratio of the transformer can be chosen through the following equation:

$$n = \frac{m_{min}}{2} \frac{V_{in,max}}{V_{out}} \tag{4.22}$$

4.3.2 Inductor ratio selection

The inductor ratio is selected to minimise the CLF: in particular, the range of possible l_m can be reasonably limited to $[3, 7]$. As a matter of fact, this consideration alone is not enough to choose the inductor ratio. In fact, this parameters also strongly impacts on the ZVS condition. In particular, the maxim dead-time (needed at maximum frequency) for ensuring ZVS can be related to l_m through the following equation:

$$T_{D,max} = \sqrt{\frac{1+l_m}{C_{rn}}} \left[\arccos \left[\frac{-0.5}{\sqrt{0.25 + (1+lm) C_{rn} I_{r,pk}^2}} \right] - \arctan \left[\frac{I_{r,pk}\sqrt{1+l_m} C_{rn}}{0.5} \right] \right] \tag{4.23}$$

where $C_{rn} = \dfrac{C_r}{C_{HB}}$ and $I_{r,pk} = \dfrac{T_{min}}{4(1+l_m)}$. Therefore, it must be checked if the actual dead-time (which is usually an a-priori set) is higher than $T_{D,max}$, for the chosen inductor ratio. If not, l_m must be further reduced and/or the value of C_{HB} must be increased.

4.3.3 Remaining components selection

As previously stated, given an operating point, each signal of the circuit can be computed, if the corresponding operating region is known. In particular, this can be applied to the computation of the normalised average input current ($I_{inavno} = I_{in,avg} \dfrac{Z_0}{V_{in}} \dfrac{2}{m}$), whose value is represented in the figure below, as a function of the normalised period ($T_{pn} = T/T_r$)and for different values of m and ΔV_{rn} (pink curves),

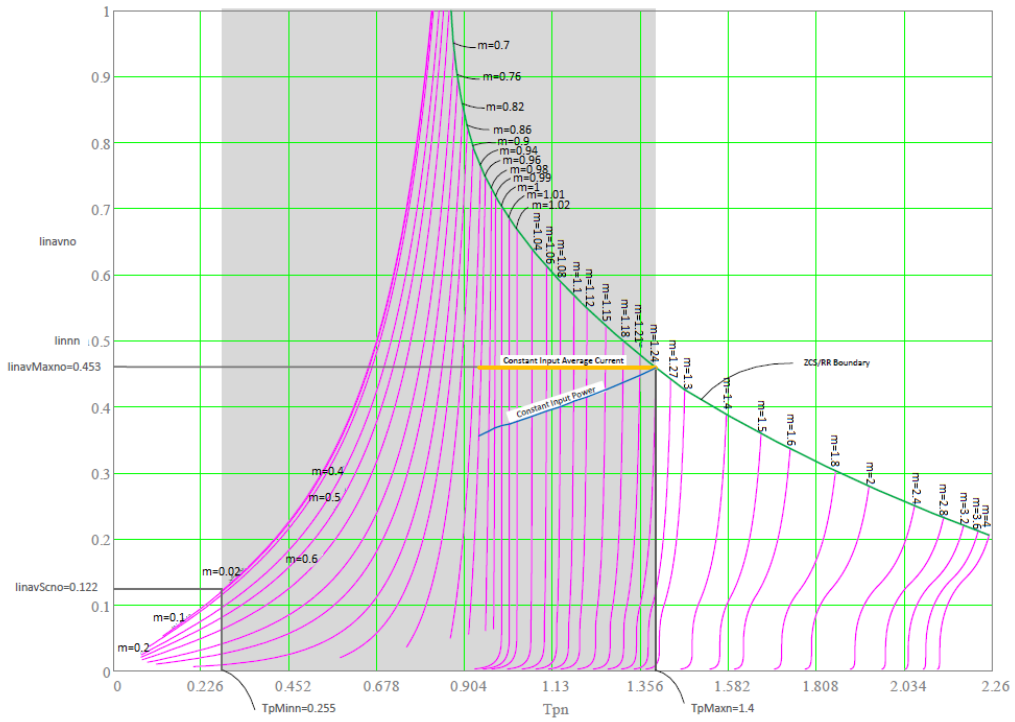

Figure 4.14: Plot of I_{inavno} as a function of T_{pn} for different values of ΔV_{rn} (pink curves)

Focusing on the ZCS/RR border, Figure 4.14 clearly shows that the normalised average input current increases with the rise of the frequency. Therefore, the design suggests to choose the maximum allowed normalised average input current ($I_{inavMaxno}$) in correspondence of m_{max}, along the ZCS/RR border (which also sets the maximum normalised switching period, $T_{pn,max}$). Of course, this means that the converter should not work above the orange line. As a consequence of the choice of $T_{pn,max}$, the resonance frequency can be found through the following expression (assuming that f_{min} is a specification):

$$\omega_r = 2\pi T_{pn,max} f_{min} \tag{4.24}$$

Then, the actual un-normalised value of the maximum input average current can be roughly evaluated starting from the specifications and considering an efficiency (η) of the converter of e.g. 90%:

$$I_{in,avg,max} = \frac{1}{V_{in,min}} \frac{P_{out,max}}{\eta} \tag{4.25}$$

Combining this value with its normalised version ($I_{inavMaxno}$), it possible to evaluate the characteristic impedance Z_0:

$$Z_0 = nV_{out} \frac{I_{inavMaxno}}{I_{in,avg,max}} \tag{4.26}$$

Finally, the values of C_r, L_r, L_p can be found:

$$C_r = \frac{1}{Z_0 \cdot \omega_r} \tag{4.27}$$

$$L_r = \frac{Z_0}{\omega_r} \tag{4.28}$$

$$L_p = l_m \cdot L_r \tag{4.29}$$

Chapter 5

Modelling and design with parasitic effects

In this chapter, the idea is to complicate a bit the previous model with the introduction of parasitic elements (in order to get a more realistic description of the LLC converter) while maintaining the analytical approach and following the strategy described in [21], for the design of Class-E resonant converters. In particular, the effect of parasitic resistances at the primary and secondary side is studied. A first attempt was made to describe the converter periodic evolution by considering even the dead-time: however that model led to a very complex analysis (too many different zones involved) which simply was not worth it because the resulting variations introduced by the dead-time (always very short with respect to the switching period) were not very significant. Therefore, in the following, the duration of the dead-time is never taken into account in the sequence of states characterising an operating region. This assumption allows to approximate the lossy circuit as follows:

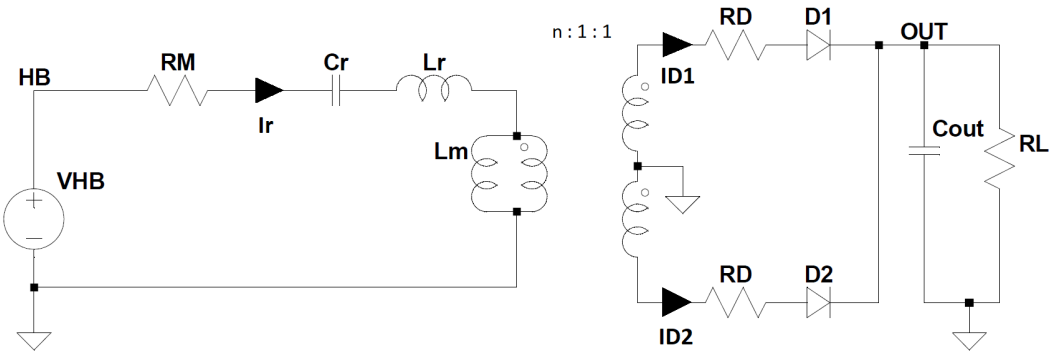

Figure 5.1: Lossy LLC schematic under the assumption of zero dead-time

As visible in the figure above, the lossy LLC schematic under exam presents a square wave generator (V_{HB}) at its input: in particular, this voltage source models the behaviour of the two power MOSFETs (as shown in the previous chapter). In fact, neglecting the dead-time (i.e. assuming instantaneous switching), the voltage at node HB is simply V_{in}, when the high-side transistor is on, while node HB switches to zero voltage, when the low-side MOSFET is on. Moreover, a resistor (R_M) is added at the primary side, in series with the resonant tank: this resistor is actually an effective element which lumps together all the parasitic resistive contributions at the primary side, i.e. the on-resistance of the power transistors, the ESR of C_r and the series resistance of L_r. At the secondary side of the transformer, another effective resistance (R_D) is inserted in series with the power diodes to model the leakage effects of the secondary windings and the finite transconductance of the diodes. This modification leads to systems of Ordinary-Differential-Equations (ODEs) (describing

the circuit relationships) which are not solvable in closed-form, thus requiring the need of numerical solutions. In particular, the MATLAB environment has been exploited for the manipulation of the differential equations coming from the analysis of the lossy LLC. At first, the symbolic computation was chosen for obtaining solutions of the systems of first-order ODEs but its computational effort was found to be too high, resulting in very slow simulations of each operating point. Therefore, given the high nonlinearity of the non-ideal LLC, the next idea was to move onto a purely numerical approach, by exploiting a proper MATLAB function, e.g. *ode45*. This last method can be effectively used for the solution of few operating points since it gives better performances (in terms of computational time) with respect to the symbolic approach. However, a different solution has been eventually exploited, based on the theory of matrix differential equations, which allows to further reduce the computational effort required by the LLC analysis (e.g. by directly computing the value of an integral rather than exploiting MATLAB functions such as *trapz*). As a consequence, simulations of a considerable number of operating points can be carried out more easily, with the objective of getting a more complete description of the converter behaviour.

5.1 Design at resonance

Given the fact that, as already stressed, the design of the converter can be optimised just for one single operating point, the idea is to focus the attention only to resonance operation (in CCM), which is usually the preferred condition in which the LLC has to work. Therefore, the first aspect is to fix the sequence of states characterising the RHP boundary: as shown in the previous chapter, this sequence consists of just two states and the turn on and turn off of each power MOSFET are exactly synchronised with the ones of the corresponding power diode. In terms of the previously-introduced notation, this means that the sequence under exam is 1M1D-2M2D (Figure 4.9). The next step is to find the systems of first-order ODEs describing these two states. In particular, choosing as state variables the resonant current I_r, the resonant capacitor voltage V_r, and the secondary-side current (either I_{D1} or I_{D2}), the following system is obtained, in the case of the 1M1D state:

$$\begin{cases} I_r = C_r \dfrac{\mathrm{d}V_{Cr}}{\mathrm{d}t} \\ V_{in} = R_M I_r + V_r + L_r \dfrac{\mathrm{d}I_r}{\mathrm{d}t} + L_m \dfrac{\mathrm{d}(I_r - I_{D1}/n)}{\mathrm{d}t} \\ V_{out} = \dfrac{L_m}{n} \dfrac{\mathrm{d}(I_r - I_{D1}/n)}{\mathrm{d}t} - R_D I_{D1} - V_{D1,on} \end{cases}$$

while in the case of the 2M2D state:

$$\begin{cases} I_r = C_r \dfrac{\mathrm{d}V_{Cr}}{\mathrm{d}t} \\ 0 = R_M I_r + V_r + L_r \dfrac{\mathrm{d}I_r}{\mathrm{d}t} + L_m \dfrac{\mathrm{d}(I_r + I_{D2}/n)}{\mathrm{d}t} \\ V_{out} = -\dfrac{L_m}{n} \dfrac{\mathrm{d}(I_r + I_{D2}/n)}{\mathrm{d}t} - R_D I_{D2} - V_{D2,on} \end{cases}$$

As shown above, both the half-periods of resonance operation are characterised by a III order system of first-order ODEs (where also the forward voltages of the power diodes are taken into account). The only differences between the two differential systems are the value of the voltage at node HB (which is either V_{in} or zero) and the quantities regarding the secondary diode which is actually on (either D1 or D2). It is important to notice that the choice of the above-cited state variables is different from the one exploited in the previous chapter. The reason behind this choice lies in the will of allowing for a more practical design: in fact, for instance, the output current flowing in the resistive load can be simply obtained starting from I_{D1} and I_{D2}. The above-shown systems of ODEs are rearranged and written in MATLAB in matrix form, i.e. $\underline{\mathbf{y}} = A \cdot \underline{\mathbf{x}} + b$, where $\underline{\mathbf{y}}$ is the vector of the derivates of the state variables while $\underline{\mathbf{x}}$ represents the vector of the state variables themselves. In particular, the matrices A and B are found through the use of symbolic computations. Then, assuming that the initial values of the state variables are known, it is possible to plot their periodic evolution, by exploiting the matrices A and B inside the *ode45* MATLAB function:

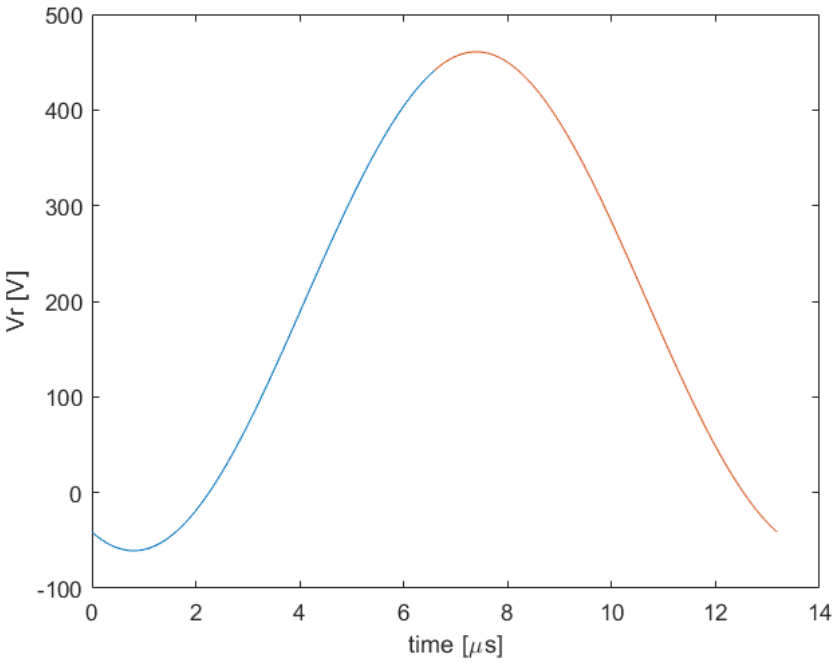

Figure 5.2: Example of the periodic evolution of V_r

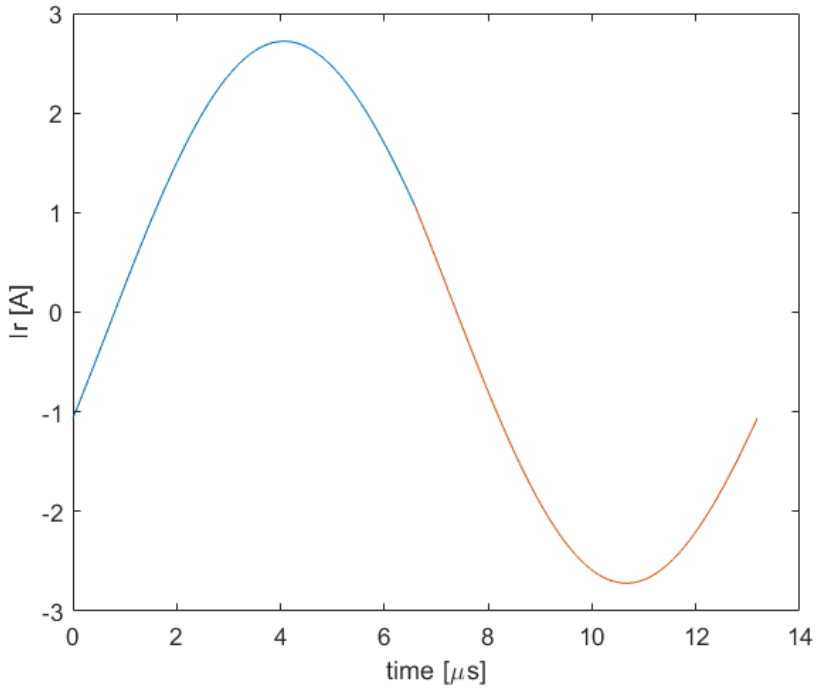

Figure 5.3: Example of the periodic evolution of I_r

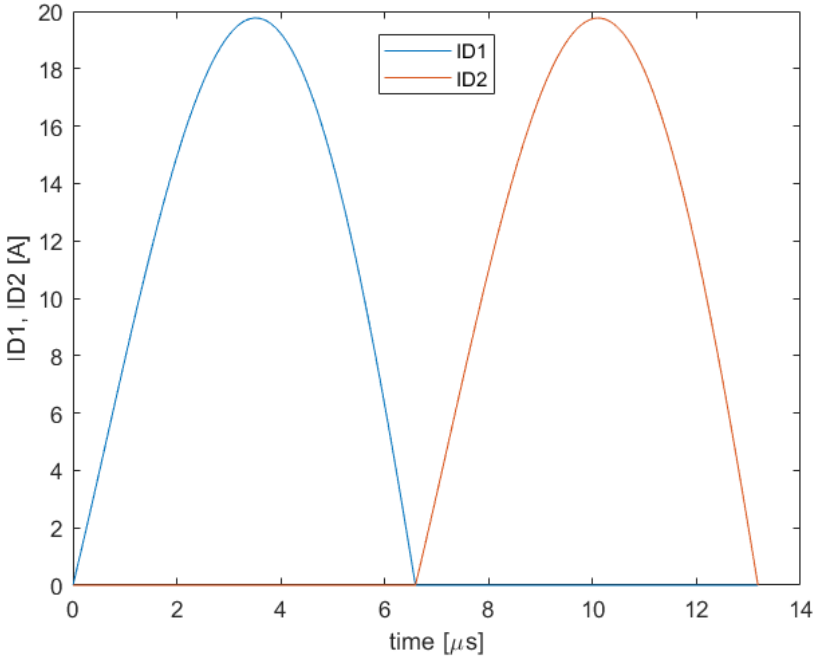

Figure 5.4: Example of the periodic evolution of I_{D1} and I_{D2}

The plot of the lossy converter waveforms can be useful but it is even more useful to find a

design approach capable of imposing some analytical constraints on the system starting from a set of specifications. In particular, in order to find the optimal choice of the LLC elements, the following specifications are taken into account:

- input voltage, V_{in};
- output voltage, V_{out};
- either the nominal operating frequency, f_r, or the values of L_r and C_r;
- output load, R_L (or output power or output current);
- overall parasitic capacitance at node HB, C_{ZVS};
- dead-time, T_D,

The above-listed specifications are used to impose a set of four main constraints:

1. periodicity of V_r, i.e. $V_r(T/2) = V_{in} - V_r(0)$;
2. periodicity of I_r, i.e. $I_r(T/2) = -I_r(0) = 1.2 \cdot I_{ZVS}$;
3. periodicity of I_{D1}, i.e. $I_{D1}(T/2) = I_{D1}(0) = 0$;
4. average value of the diode current equal to the output current, i.e. $mean(I_{D1}) = \dfrac{V_{out}}{R_L}$

As shown above, the converter can be constrained simply resorting to its first half-period (*1M1D* state), since the second one (*2M2D* state) is redundant. In fact, since the duty cycle of the signals driving the power MOSFETs is exactly 50%, during the second half-cycle, the evolution of I_{D2} is exactly equal to the one of I_{D1} in the first half-cycle, the plot I_r equals $-I_r(0 < t < T/2)$ and V_r can be found as $V_{in} - V_r(0 < t < T/2)$. Furthermore, the output current (i.e. $\dfrac{V_{out}}{R_L}$) can be found as integral mean of I_{D1} over the first half-cycle. This consideration remains valid also away from the RHP border and it allows for faster simulations, since, for each operating region, it is enough to simulate only half of the sequence of states. Another important aspect to be clarified is the one regarding the initial value of the resonant current: this value must be imposed lower than $-I_{ZVS}$ so that $I_r(T/2)$ is, in turn, set higher than the minimum value required to reach ZVS. On the other hand, the value of $I_r(T/2)$ must not be too far from the minimum allowed one because, otherwise, turn off losses are heavily increased: this is the why $I_r(T/2)$ is chosen to be only e.g. 20% higher than the minimum value (meaning $1.2 \cdot I_{ZVS}$).
These four constraints are exploited inside a MATLAB script for the choice of a corresponding number (i.e. four) of LLC parameters to be optimised for working at the RHP boundary, with the given specifications. In particular, the MATLAB optimiser tries to minimise the norm of the difference between the vector:

$$[V_{in} - V_r(T/2), I_{D1}(T/2), -I_r(T/2), mean(I_{D1})] \tag{5.1}$$

computed starting from a random set of the LLC parameters to be found, and the vector:

$$\left[V_r(0), 0, -1.2 \cdot I_{ZVS}, \frac{V_{out}}{R_L}\right] \tag{5.2}$$

By tuning the values of the LLC parameters to be optimised, the norm is modified until it is found to be lower than a certain threshold, meaning that the optimisation process is over.
In the first place, $V_r(0)$, L_m, n and the effective resonance period ($T_{r,eff}$) are chosen as parameters to be found by the optimiser, which means that, instead, the resonant components (inductor L_r and capacitor C_r) are already fixed. This approach is useful for understanding the effect of parasitic elements on the turns ratio, on the magnetising inductance and on the effective resonance frequency ($1/T_{r,eff}$). The results of this design approach show that the effective value of the resonance frequency slightly differs from f_{R1}. Moreover, once the converter has been designed, the full RHP border operation can be simulated, e.g. by sweeping the output load and finding the remaining unknowns ($V_r(0)$, $I_r(0)$, V_{out}, $T_{r,eff}$): the simulations show that the deviation of the effective resonance frequency from its ideal value is more marked at high output loads (i.e. lower output power levels). This is clearly shown from the following figure, containing an example of RHP border (described in terms of output voltage, V_{out} as a function of the normalised switching frequency, $f_n = f_{sw}/f_{R1}$) in the case of a lossy LLC converter. In particular, the converter under exam is characterised by $V_{in} = 400$ V, $n = 7.73$, $T_D = 90$ ns, $C_{ZVS} = 200$ pF, $L_r = 201$ µs, $L_m = 603$ µs, $C_r = 22$ ns and it is simulated (Appendix A.3) by sweeping the output load from approximately $8\ \Omega$ (top) to $0.1\ \Omega$ (bottom):

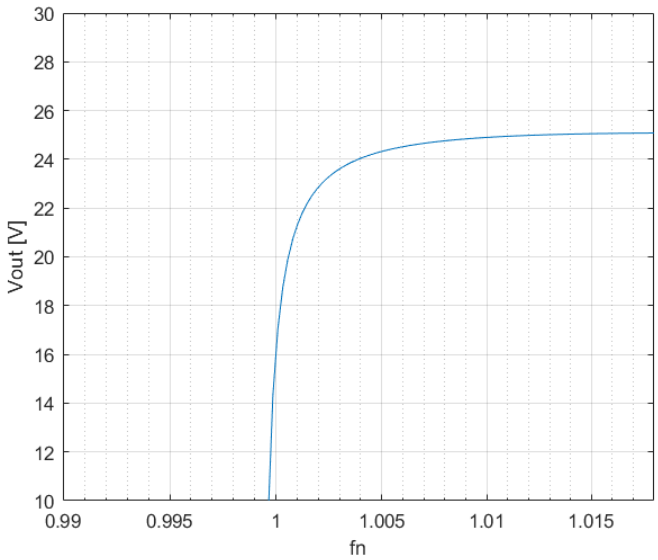

Figure 5.5: RHP border of the lossy LLC ($R_M = 1\ \Omega$ and $R_D = 0.1\ \Omega$)

The same kind of simulation can be used to understand how the parasitic resistances affect the dependency of the output voltage (and therefore the conversion ratio) on the output load: as seen in the ideal lossless case, working at resonance means working in a load-independent point. However, this is no more true in the case of the lossy converter (as already evident from Figure 5.5), where the degree of load-dependency can therefore be a key parameter. In particular, the RHP boundary can be simulated with lower values of parasitic resistances (for the same range of output loads) to evaluate how much the ideal operation at resonance is impacted when changing the output resistive load. The results are shown in the following:

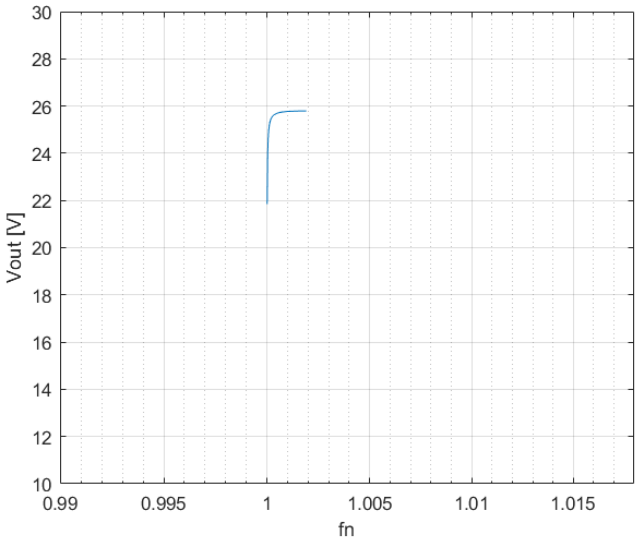

Figure 5.6: RHP border of the lossy LLC ($R_M = 0.1\ \Omega$ and $R_D = 0.01\ \Omega$)

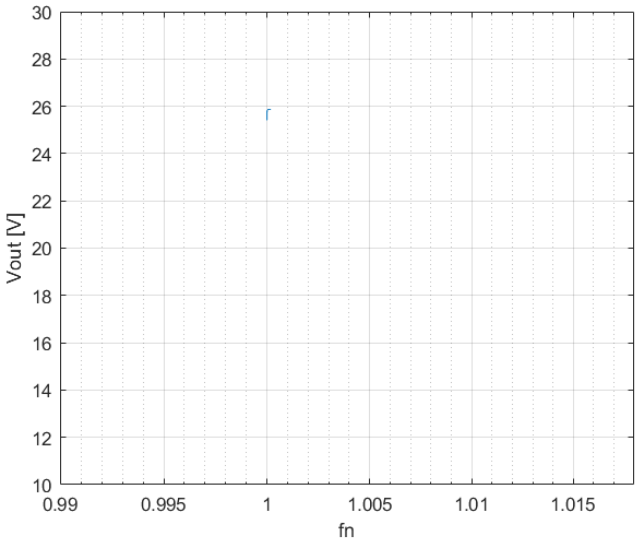

Figure 5.7: RHP border of the lossy LLC ($R_M = 0.01\ \Omega$ and $R_D = 0.001\ \Omega$)

As expected, lower parasitic resistances lead to a reduced dependency of the output voltage on the output load: the proposed approach has the advantage of quantitatively evaluating this dependency.
In addition, similarly with the reasoning followed in the previous chapter, it is possible to compute the maximum output resistive load (i.e. the minimum output current) which allows to work along the RHP boundary, exploiting another strategy derived from the previous one: in fact, in this case, the output load becomes one of the values to be found by the optimiser and therefore an additional constraint must be added. In particular, the voltage across D1 must be imposed just enough for it to turn on (i.e. $V_{D1,on}$) at the beginning of the switching period, in order to obtain the above-mentioned threshold load. This threshold output load is also useful to understand where to stop the sweep of the output loads when simulating the RHP border.
A similar but more effective approach to the design consists of starting from a specification on the operating frequency (which is usually the case) and to find, as a result of the MATLAB optimisation, the value of C_r, in addition to n, L_m and $V_r(0)$. It is useful to point out that the inductor ratio ($l_m = \frac{L_m}{L_r}$) remains a degree of freedom in this model and therefore it could be optimised for other specifications. In this case, since it is known from the ideal lossless circuit that l_m controls the distance between the main resonance frequency and the secondary one (eq. (2.3)) and that a lower value of l_m allows to limit conduction losses (Figure 4.13), it seems reasonable to choose $l_m = 3$. Of course, while in the ideal model, this would imply that the ratio between the main resonance frequency and the lower one is exactly two, this is no more true with exact precision, in the case of the lossy converter. Therefore a modified MATLAB script is used to perform the proposed design (Appendix A.4). This design approach allows to easily and rapidly find the values of all the LLC components without strong approximations and also taking into account the modifications introduced by the parasitic losses. Of course, a similar procedure could also be applied to design the lossy converter to work in regions different from the RHP border (when required): in that case, the MATLAB model must be modified accordingly to the correct sequence of zones characterising the desired operating region.

5.1.1 Design example

A design example is now provided starting from a set of specifications, summarised in the table below:

$\mathbf{V_{in}}$ [V]	400
$\mathbf{V_{out}}$ [V]	24
$\mathbf{R_L}$ [Ω]	1.92
$\mathbf{f_{nominal}}$ [kHz]	75.874
$\mathbf{C_{ZVS}}$ [nF]	200
$\mathbf{T_D}$ [ns]	90

Exploiting the MATLAB script presented in Appendix A.4, the converter components are optimised for the given specifications and for RHP operation and then listed together in the following table:

n [none]	7.73
$\mathbf{C_r}$ [nF]	22
$\mathbf{L_r}$ [µH]	201
$\mathbf{L_m}$ [µH]	603

5.2 Generalised model

The arrangement of the operating regions appears slightly modified in the case of the lossy LLC with respect to what seen regarding the lossless converter in the previous chapter (Figure 4.11). In particular, this result is found from the analysis of the lossy LLC schematic under different switching frequencies and output loads, performed through LTspice simulations.

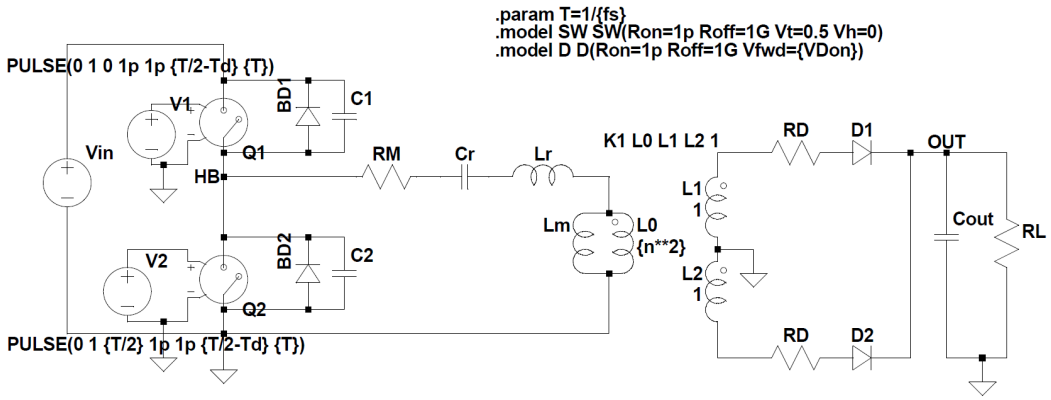

Figure 5.8: LTspice schematic of the complete lossy LLC converter

The approach oriented towards the design and followed in the previous section can be however exploited, with proper modifications, to obtain a complete description, in terms of operating regions, of an already-designed converter. This can be, of course, very useful since, as already underlined, the converter can be used to build more complex circuits for voltage regulation, through feedback control, tuning the switching frequency of the LLC in order to maintain constant the output voltage, when the input voltage or the output load vary. In particular, through the proposed method of analysis, it is possible to generate the complete map of all the main operating regions in a output voltage vs normalised frequency plot (similar to the one obtained in the case of the FHA model, Figure 3.7, but more accurate and complex). Of course, this requires, first of all, to find the systems of ODEs characterising all the states involved in the principal regions of interest, which are: *1M2D*, *2M1D*, *1M* and *2M* (apart from the already described *1M1D* and *2M2D*). In particular, referring to the circuit in Figure 5.1 and starting from *1M2D*, the system of ODEs is the following:

$$\begin{cases} I_r = C_r \dfrac{\mathrm{d}V_{Cr}}{\mathrm{d}t} \\ V_{in} = R_M I_r + V_r + L_r \dfrac{\mathrm{d}I_r}{\mathrm{d}t} + L_m \dfrac{\mathrm{d}(I_r + I_{D2}/n)}{\mathrm{d}t} \\ V_{out} = -\dfrac{L_m}{n} \dfrac{\mathrm{d}(I_r + I_{D2}/n)}{\mathrm{d}t} - R_D I_{D2} - V_{D2,on} \end{cases}$$

while in the case of *2M1D*:

$$\begin{cases} I_r = C_r \dfrac{\mathrm{d}V_{Cr}}{\mathrm{d}t} \\ 0 = R_M I_r + V_r + L_r \dfrac{\mathrm{d}I_r}{\mathrm{d}t} + L_m \dfrac{\mathrm{d}(I_r - I_{D1}/n)}{\mathrm{d}t} \\ V_{out} = \dfrac{L_m}{n} \dfrac{\mathrm{d}(I_r - I_{D1}/n)}{\mathrm{d}t} - R_D I_{D1} - V_{D1,on} \end{cases}$$

Moving to the *M* states, the systems of ODEs are simply of the II order. In particular, concerning *1M*:

$$\begin{cases} I_r = C_r \dfrac{\mathrm{d}V_{Cr}}{\mathrm{d}t} \\ V_{in} = R_M I_r + V_r + (L_r + L_m) \dfrac{\mathrm{d}I_r}{\mathrm{d}t} \end{cases}$$

while in the case of *2M*:

$$\begin{cases} I_r = C_r \dfrac{\mathrm{d}V_{Cr}}{\mathrm{d}t} \\ 0 = R_M I_r + V_r + (L_r + L_m) \dfrac{\mathrm{d}I_r}{\mathrm{d}t} \end{cases}$$

It is important to notice that, through LTspice simulations, two new operating regions are found, in addition to the ones already shown in the previous chapter (i.e. ARHP, BRHP, ARLP, BRLP). These two additional regions are both found below-resonance and are named Below-Below-Resonance-High-Power (BBRHP) and Below-Resonance-Very-High-Power (BRVHP). In particular, the sequences of states characterising these two additional regions are summarised in the following tables. For what concerns BBRHP:

1M1D	**1M**	**1M2D**	**2M2D**	**2M**	**2M1D**

while, in the case of BRVHP:

1M1D	**1M2D**	**2M2D**	**2M1D**

These two new operating regions are rather important because they can be used as a starting point for the computation of the ZCS boundary, differently from what seen in the previous chapter (lossless converter), where the BRHP region is used. In particular, it is observed that,

for lower output loads, a decrease of the frequency moves the LLC from the RHP boundary to the BRVHP region while, in the case of higher output loads, the BBRHP region is entered. As a final remark, it is useful to point out that the BRLP region described in the previous chapter is found to actually characterise both below-resonance and above-resonance operation of the lossy LLC, when the output power is rather low. Therefore, in this chapter, the sequence of states corresponding the BRLP region is referred to as Low-Power (LP) region. The following sub-sections describe in detail each main boundary: as usual, in order to impose some constraints on the converter waveforms, it is enough to focus on the first half-period. Moreover, the MATLAB code for imposing these constraints is detailed (Appendix A.4) only for the first analysed boundary: in fact, the other borders can be simply simulated through properly modified versions of the same code.

5.2.1 ZCS from Below-Resonance-Very-High-Power (BRHVP)

At low output voltages (corresponding to low resistive loads), this boundary approaches the RHP one and therefore values extracted from the RHP simulation can be used as input values to be tuned for characterising this boundary. In particular, the sequence of states is to be exploited in this case is *1M1D-1M2D* while the parameters to be optimised are the following:

1. duration of the *1M1D* state, T_{D1};
2. duration of the *1M2D* state, T_{D2};
3. $V_r(0)$;
4. $I_{D1}(0)$;
5. R_L

These values are optimised by a proper MATLAB script (Appendix A.5), imposing several constraints:

1. $V_{in} - V_r(T_{D1} + T_{D2}) = V_r(0)$;
2. $I_{D2}(T_{D1} + T_{D2}) = I_{D1}(0)$;
3. $I_r(T_{D1} + T_{D2}) = -I_r(0)$;
4. $I_{D1}(T_{D1}) = 0$;
5. $R_L \cdot mean(I_{D1} + I_{D2}) = V_{out}$

In order to move along the boundary, either V_{out} or R_L could be swept: in this case, it is convenient to sweep V_{out} and finding the corresponding R_L in order to get faster simulations. Moreover, the upper value of V_{out} for the computation of this boundary can be computed with a dedicated MATLAB script, imposing an additional constraint for taking into account the approaching of the BBRHP region.

5.2.2 ZCS from Below-Below-Resonance-High-Power (BBRHP)

This boundary can be seen as the prosecution of the previous one but, since there happens a change of regions,a different sequence of states must be exploited in the optimisation. In particular, in this case the MATLAB code exploits the *1M1D-1M-1M2D* sequence of states. Again, V_{out} is swept for moving along the boundary. Going more in detail, the values to be found by the MATLAB optimiser are:

1. duration of the *1M1D* state, T_{D1};
2. duration of the *1M* state, T_{D0};
3. duration of the *1M2D* state, T_{D2};
4. $V_r(0)$;
5. $I_{D1}(0)$;
6. R_L

while the constraints to be imposed are:

1. $V_{in} - V_r(T_{D1} + T_{D0} + T_{D2}) = V_r(0)$;
2. $I_{D2}(T_{D1} + T_{D0} + T_{D2}) = I_{D1}(0)$;
3. $I_r(T_{D1} + T_{D0} + T_{D2}) = -I_r(0)$;
4. $I_{D1}(T_{D1}) = 0$;
5. $V_{D2}(T_{D1} + T_{D0}) = V_{D2,on}$;
6. $R_L \cdot mean(I_{D1} + I_{D2}) = V_{out}$

5.2.3 BVRHP-BBRHP boundary

This edge occurs between the new introduced operating regions (BVRHP and BBRHP). In order to simulate this condition, the idea is to start from the sequence states of BVHP (i.e. *1M1D-1M2D*) and to impose the following set of constraints:

1. $V_{in} - V_r(T_{D1} + T_{D2}) = V_r(0)$;
2. $I_{D2}(T_{D1} + T_{D2}) = I_{D1}(0)$;
3. $I_r(T_{D1} + T_{D2}) = -I_r(0)$;
4. $I_{D1}(T_{D1}) = 0$;

5. $V_{D2}(T_{D1}) = V_{D2,on}$;
6. $R_L \cdot mean(I_{D1} + I_{D2}) = V_{out}$

with the objective of find, as outputs of the MATLAB optimiser, the following parameters:

1. duration of the *1M1D* state, T_{D1};
2. duration of the *1M2D* state, T_{D2};
3. $V_r(0)$;
4. $I_{D1}(0)$;
5. $I_r(0)$;
6. R_L

In this case, it is convenient to start from the set of initial parameter values corresponding to the passage between ZCS-BBRHP and ZCS-BVRHP and then to sweep the output voltage, stopping at the RHP boundary.

5.2.4 BBRHP-BRHP boundary

This boundary marks the entering of a more "stable" region (i.e. characterised by a frequency closer to the resonance one and/or lower output power). In order to simulate the operation along the BBRHP-BRHP boundary, it is practical to start from the BRHP region (characterised by a *1M1D-1M* sequence of states) and to impose the below shown constraints:

1. $V_{in} - V_r(T_{D1} + T_{D0}) = V_r(0) = R_M \cdot I_r(0) - n(V_{out} + V_{D1,on})\dfrac{L_m + L_s}{L_m}$;
2. $I_{D1}(T_{D1}) = I_{D1}(0) = 0$;
3. $I_r(T_{D1} + T_{D2}) = -I_r(0)$;
4. $R_L \cdot mean(I_{D1}) = V_{out}$

The implementations of these constraints in a proper MATLAB script allows to evaluate the optimised value of the following set of parameters:

1. duration of the *1M1D* state, T_{D1};
2. duration of the *1M* state, T_{D0};
3. $I_r(0)$;
4. R_L

As a starting point of the simulation, the cross point between RHP and BVRHP-BBRHP boundary could be used.

5.2.5 BRHP-LP boundary

In this sub-section, the border between BRHP and LP regions is analysed. In order to simulate this condition, it can be useful to start from the upper limit of RHP boundary, exploiting the sequence of states characterising the BRHP region (i.e. *1M1D-1M*). Then, V_{out} can be swept (increased) to move along the BRHP-LP border, imposing the following constraints:

1. $V_{in} - V_r(T_{D1} + T_{D0}) = V_r(0) = V_{in} - R_M \cdot I_r(0) - n(V_{out} + V_{D1,on})\dfrac{L_m + L_s}{L_m}$;
2. $I_{D1}(T_{D1}) = I_{D1}(0) = 0$;
3. $I_r(T_{D1} + T_{D2}) = -I_r(0)$;
4. $R_L \cdot mean(I_{D1}) = V_{out}$

in order to obtain the optimisation below-shown parameters:

1. duration of the *1M1D* state, T_{D1};
2. duration of the *1M* state, T_{D0};
3. $I_r(0)$;
4. R_L

5.2.6 ARHP-ARLP boundary

This limit marks the passage from a high-power region to a low-power region, when above resonance. Therefore, in order to simulate it, the idea is to exploit the sequence of states characterising the ARHP region (*1M2D-1M1D*) and to impose the following constraints:

1. $V_{in} - V_r(T_{D2} + T_{D1}) = V_r(0)$;
2. $I_{D1}(T_{D2} + T_{D1}) = I_{D2}(0)$;
3. $I_r(T_{D2} + T_{D1}) = -I_r(0)$;
4. $I_{D2}(T_{D2}) = 0$;
5. $V_{D1}(T_{D2}) = V_{D1,on}$;
6. $mean(I_{D2} + I_{D1}) = \dfrac{V_{out}}{R_L}$

with the aim of optimising the value of the following quantities:

1. duration of the *1M2D* state, T_{D2};

2. duration of the *1M1D* state, T_{D1};
3. $V_r(0)$;
4. $I_{D2}(0)$;
5. $I_r(0)$;
6. V_{out}

It is useful to notice that, in this case, the output load can be swept rather than V_{out}.

5.2.7 ARLP-LP boundary

At frequencies higher than the resonance one, there is a gradual passage to the LP region, when increasing the output load. In particular, in order to find the border between ARLP and LP regions, it is possible to exploit the sequence of states which exactly characterises this boundary, i.e. *1M-1M1D*. Moreover, a set of constraints must be imposed:

1. $V_{in} - V_r(T_{D0} + T_{D1}) = V_r(0)$;
2. $I_{D1}(T_{D0} + T_{D1}) = 0$;
3. $I_r(T_{D0} + T_{D1}) = -I_r(0)$;
4. $V_{D1}(T_{D0}) = V_{D1,on}$;
5. $mean(I_{D1}) = \dfrac{V_{out}}{R_L}$

As a result of the MATLAB optimisation, the following parameters are found:

1. duration of the *1M* state, T_{D0};
2. duration of the *1M1D* state, T_{D1};
3. $V_r(0)$;
4. $I_r(0)$;
5. R_L

5.2.8 LP boundary

Depending on the lowest expected output power level, the LP boundary can be computed. In fact, this border simply represents the operating curve of the LLC converter corresponding to the highest resistive output load. As already underlined, at very low output power, there is no difference between the behaviour above or below resonance, in terms of operating regions: in particular, the sequence characterising the LP region is *1M-1M1D-1M*. Therefore, fixing a rather high output load, it is possible to simulate this boundary by imposing the following expressions:

1. $V_{in} - V_r(T_{D01} + T_{D1} + T_{D02}) = V_r(0)$;
2. $I_{D1}(T_{D01} + T_{D1}) = 0$;
3. $I_r(T_{D01} + T_{D1} + T_{D02}) = -I_r(0)$;
4. $V_{D1}(T_{D01}) = V_{D1,on}$;
5. $mean(I_{D1}) = \dfrac{V_{out}}{R_L}$

and finding an optimisation of the following set of parameters:

1. duration of the first *1M* state, T_{D01};
2. duration of the *1M1D* state, T_{D1};
3. duration of the second *1M* state, T_{D02};
4. $V_r(0)$;
5. $I_r(0)$

5.2.9 Complete map of regions and operating curve

Putting together all the previously-analysed boundaries, it is possible to get the map of all the main operating regions of the converter. In particular this is performed for the LLC circuit characterised in the design example of the previous section and the results are shown in the following.

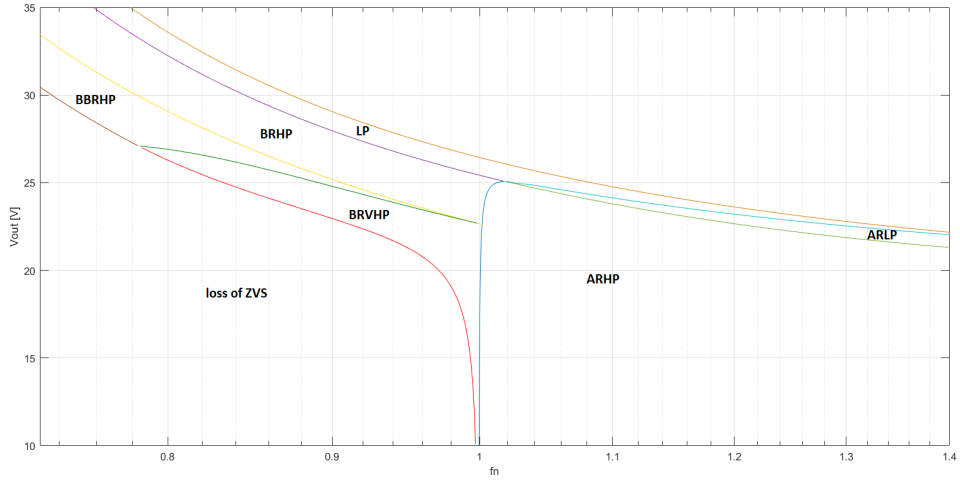

Figure 5.9: Map of regions of the designed converter

The computational effort required to find this chart is rather heavy but the advantage is that then every signal can be quantitatively evaluated as a function of the frequency and/or of the output load. Moreover, once the map of operating regions is obtained, it is easy to plot the operating curve of the LLC converter, i.e. the behaviour of the output voltage as a function of the frequency, for a fixed value of the output load. In particular, considering $R_L = 1.92$ (which is the value resulting from the specifications of the design example under exam), the following plot is obtained:

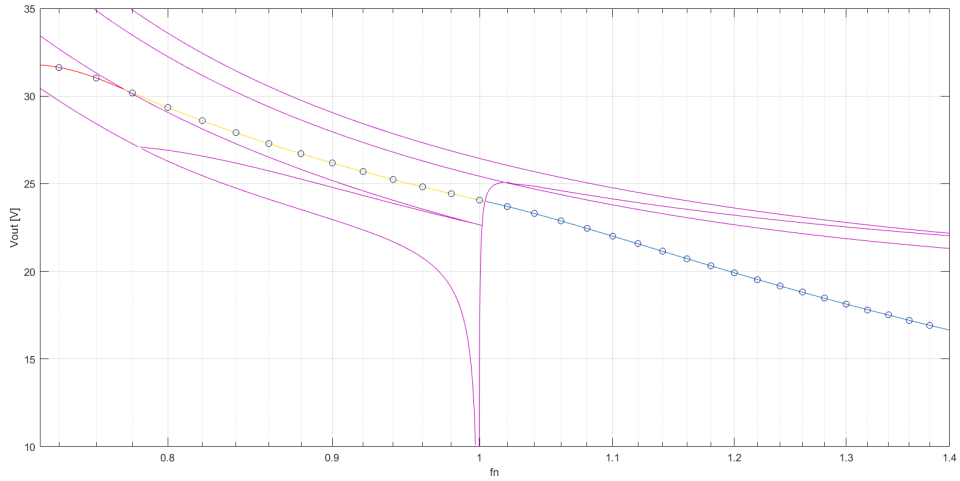

Figure 5.10: Operating curve of the designed LLC

The circles on the operating curve represent the values extracted from LTspice simulations of the LLC lossy schematic, taking into account the duration of the dead-time (Figure 5.8): as clearly evident, the MATLAB model is able to accurately predict the behaviour of the

converter. Of course, as already highlighted, any other signal of the circuit can be studied as a function of the frequency and/or the output load. For example, it is possible to evaluate the frequency trend of the resonant current magnitude at half-period (i.e. $I_r(T/2)$), useful to understand at what frequencies the LLC is able to work in ZVS. An example of this kind of study (referring to the already quoted designed LLC converter) is shown in the following figure, where the data obtained from the MATLAB model (solid lines) are also compared to the corresponding values (evaluated at $T/2 - T_D$) extracted from LTspice simulations (circles):

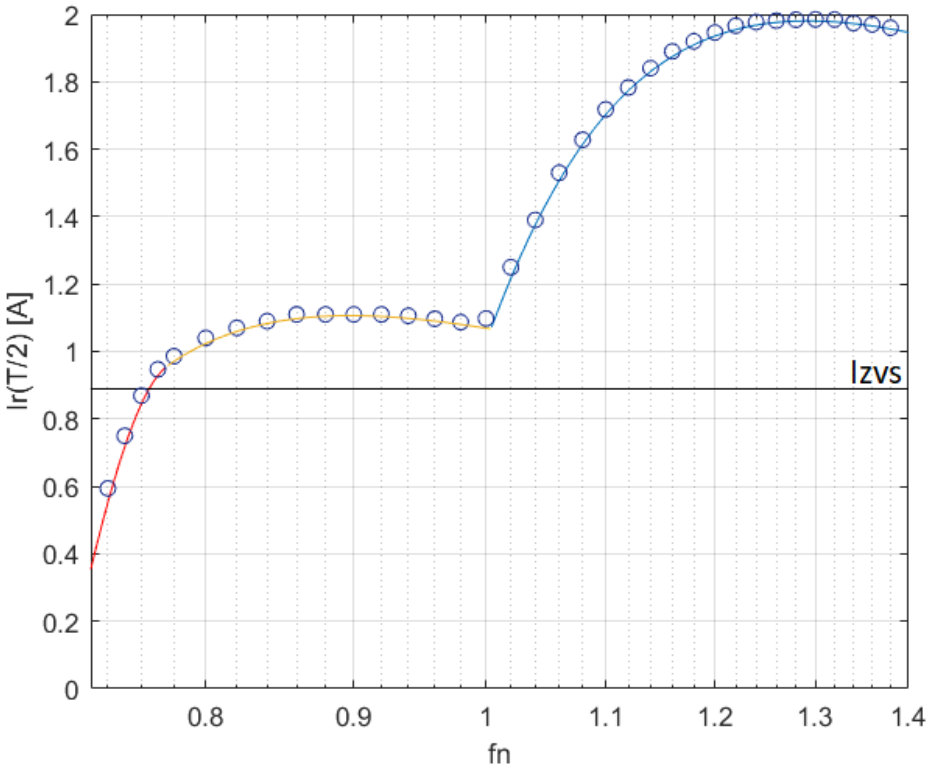

Figure 5.11: Trend of $I_r(T/2)$ as a function of the normalised frequency

Chapter 6

Conclusion

Different approaches to the analysis and design of half-bridge LLC resonant power converters has been shown, highlighting differences, advantages and limitations. In the first place, the FHA model has been studied in detail, showing how it can be used to approximately describe the LLC operation and how a design flow can be based on it. Then, a less approximate analysis has been described, based on the exact time-domain solution of the differential equations characterising the lossless converter. Also in this case, a design flow has been provided. Finally, the influence of parasitic elements (resistances, in particular) has been studied. Hence, an exact design method oriented to the optimal operation of the lossy converter in one specific operating point has been developed. Then, the same analytical approach exploited in this design procedure has been modified to find a thorough and rather accurate description of the signals of the lossy converter circuit when changing the switching frequency and/or the output power. The main results of this analysis have been compared to LTspice simulations of the lossy LLC converter, in order to prove the high accuracy level reached through the developed model. Possible improvements of the presented design and analysis methods concern the development of an enhanced design procedure (always based on the accurate description of the lossy LLC converter) capable of ensuring soft-switching (in terms of ZVS) despite the variations of the input voltage in a limited range and the choice of a circuital normalisation able to provide a more general description. Moreover, the presented approach could also be used for the study of other non-idealities afflicting the LLC converter.

Appendix A

MATLAB scripts

A.1 FHA design

```
global Q_max Q_ZVS2 fr lambda m_max C_ZVS Vin_min T_D Pout

Vin_nom = 400;
Vin_min = 380;
Vin_max = 420;
Vout = 30;
Iout = 10;
Pout = Vout*Iout;
fr = 120e3;
fmax = 150e3;
C_ZVS = 400e-12;
T_D = 200e-9;
perc_0 = 0.95;

% A)

n = (1/2)*Vin_nom/Vout;

% B)

m_min = 2*n*Vout/Vin_max;
fn_max = fmax/fr;

lambda = ((1 - m_min)/m_min)*(fn_max^2)/(fn_max^2 - 1);
lm = 1/lambda;

% C)

m_max = 2*n*Vout/Vin_min;
Q_max = (lambda/m_max)*sqrt(1/lambda + (m_max^2)/(m_max^2 -
    1));

```

```
32 Rac = (8/(pi^2))*(n^2)*((Vout^2)/Pout);
33
34 Q_ZVS2 = (2/pi)*(lambda*fn_max/((lambda + 1)*fn_max^2 -
       lambda))*T_D/(Rac*C_ZVS);
35
36 f = @Q_ZVS_eval;
37 perc = fzero(f,perc_0);
38
39 Q_ZVS1 = perc*Q_max;
40
41 Q_ZVS = min([Q_ZVS1 Q_ZVS2]);
42
43 % Final computation of LLC components
44
45 Zo = Q_ZVS*Rac;
46
47 Cr = 1/(2*pi*fr*Zo);
48 Lr = Zo/(2*pi*fr);
49 Lm = Lr/lambda;
50
51 % Check if ZVS constraint is actually respected
52
53 function y = Q_ZVS_eval(x)
54
55 global Q_max Q_ZVS2 fr lambda m_max C_ZVS Vin_min T_D Pout
56
57 Q_ZVS1 = x*Q_max;
58
59 Q_ZVS = min([Q_ZVS1 Q_ZVS2]);
60
61 f_min = fr*sqrt(1/(1 + (1/lambda)*(1 - 1/power(m_max,1 + (
       Q_ZVS/Q_max)^4))));
62 fn_min = f_min/fr;
63
64 %% ZVS check at full load and fmin
65
66 Zn = 1j*fn_min/(lambda + 1j*fn_min*Q_ZVS) + (1 - fn_min^2)/(1
       j*fn_min);
67 y = imag(Zn)/real(Zn) - C_ZVS*(Vin_min^2)/(pi*T_D*Pout);
68 y = y - 0.1; %(to impose some margin)
69
```

```
end
```

A.2 ARHP steady-state analysis (lossless LLC)

```
global x lm Vr0n Vr2n

% Definition of main variables
m = 0.6;
x = m/2;
lm = 5;
AVrn = 1.642;

Vr0n = (1 - AVrn)/2;
Vr2n = Vr0n + AVrn;

fun = @root4d;

% Vector of initial guess
x0 = [-1.5,-0.05,0.7,2];

y = fsolve(fun,x0);
Ir0n = y(1)
Im0n = y(2)
theta0 = y(3)
theta1 = y(4)

fswn = pi/(theta0+theta1)

% AH constraints implemented in a function
function F = root4d(y)

% y(1)=Ir0n; y(2)=Im0n; y(3)=theta0; y(4)=theta1

global x lm Vr0n Vr2n

Ir1n = (1+x-Vr0n)*sin(y(3))+y(1)*cos(y(3));
Im1n = -x*y(3)/lm+y(2);
Vr1n =(1+x)-(1+x-Vr0n)*cos(y(3))+y(1)*sin(y(3));

F(1) = (1-x-Vr1n)*sin(y(4))+Ir1n*cos(y(4)) + y(1);
F(2) = x*y(4)/lm+Im1n + y(2);
```

```
F(3) = (1-x)-(1-x-Vr1n)*cos(y(4))+Ir1n*sin(y(4)) - Vr2n;
F(4) = Ir1n-Im1n;

end
```

A.3 RHP border (lossy LLC)

```
global Vin VD1_on VD2_on R_M R_D Lr Lm Cr n

% Parameters of the converter under exam
Vin = 400;
Td = 90e-9;
C1 = 100e-12;
C2 = 100e-12;
Cr = 2.206720338616694e-08;
Lm = 6.028295474562004e-04;
Lr = Lm/3;
VD1_on = 0;
VD2_on = 0;
n = 7.728849370975870;
Tr = 2*pi*sqrt(Lr*Cr);
R_M = 1;
R_D = 0.1;

% Inital guess of unknowns
Vr_0 = -41.221126719601630;
Ir_0 = -1.2*(C1+C2)*Vin/Td;
Vout_0 = 24;
fr_eff = 75.874e3;
T_0 = 1/fr_eff;

fn = zeros(1,83);
Vo = zeros(1,83);

options = optimset('Display','iter','PlotFcns',@optimplotfval
    ,'TolFun',1e-9,'MaxFunEvals',2500);

tic
for i=1:83
R1 = 8.278152940170909-0.1*(i-1);

```

```
34 f = @(x) norm(end_cond_finder(x(1), x(2), x(3), x(4))-[x(1),
       0, x(2), x(3)/Rl]);
35 [X_start,fval,exitflag,output] = fminsearch(f,[Vr_0,Ir_0,
       Vout_0,T_0],options);
36
37 Vr_0 = X_start(1);
38 Ir_0 = X_start(2);
39 Vout_0 = X_start(3);
40 T_0 = X_start(4);
41
42 fn(i) = Tr/T_0;
43 Vo(i) = Vout_0;
44 end
45 toc
46
47 plot(fn,Vo);
48 xlabel('fn');
49 ylabel('Vo');
50
51 function y = end_cond_finder(Vr0,Ir0,Vout,T)
52
53 global Vin VD1_on R_M R_D Lr Lm Cr n
54
55 % ZONE 1MD
56
57 A1 = [          0,                                          0,
       1/Cr;
58  -n/Lr, -(n*(Lm*R_D*n + Lr*R_D*n))/(Lm*Lr), -(R_M*n)/Lr;
59  -1/Lr,                          -(R_D*n)/Lr,      -R_M/Lr];
60
61 b1 = [

       0;
62         -(n*(Lm*VD1_on*n - Lm*Vin + Lr*VD1_on*n + Lm*Vout*n +
             Lr*Vout*n))/(Lm*Lr);
63                                                  -(VD1_on*n -
                                                       Vin +
                                                     Vout*n)/
                                                     Lr];
64
65 xp1 = -A1\b1;
```

```
66
67 [EVEC, EVAL] = eig(A1);
68 x0 = [Vr0; 0; Ir0];
69 K = eye(3)*(EVEC\(x0-xp1));
70 x1_end = real(EVEC*(diag(exp(diag(EVAL)*(T/2)))*K) + xp1);
71
72 y(1) = Vin - x1_end(1);
73 y(2) = x1_end(2);
74 y(3) = -x1_end(3);
75
76 k1 = K(1)*EVEC(2,1)/EVAL(1,1);
77 k2 = K(2)*EVEC(2,2)/EVAL(2,2);
78 k3 = K(3)*EVEC(2,3)/EVAL(3,3);
79 y(4) = (real(k1*(exp(EVAL(1,1)*T/2)-1) + k2*(exp(EVAL(2,2)*T
       /2)-1) + k3*(exp(EVAL(3,3)*T/2)-1)) + xp1(2)*T/2)/(T/2);
80
81 end
```

A.4 Proposed design (lossy LLC)

```
1  global Vin VD1_on VD2_on Vout Td C1 C2 R_M R_D T Ir_0
2
3  % Specifications
4  Vin = 400;
5  Td = 90e-9;
6  C1 = 100e-12;
7  C2 = 100e-12;
8  Ir_0 = -1.2*(C1+C2)*Vin/Td; % -IZVS
9  VD1_on = 0;
10 VD2_on = 0;
11 Vout = 24;
12 f_op = 75.874e3;
13 T = 1/f_op;
14 R_M = 1;
15 R_D = 0.1;
16 Rl = 1.92;
17
18 % Initial guess of unknowns
19 n_0 = 7.728849370975870;
20 Vr_0 = -41.221126719601630;
21 Lm_0 = 6.028295474562004e-04;
```

```
22 Cr_0 = 2.206720338616694e-08;
23
24 f = @(x) norm(end_cond_finder(x(1), x(2), x(3), x(4))-[x(2),
       0, Ir_0, Vout/Rl]);
25
26 options = optimset('Display','iter','PlotFcns',@optimplotfval
       ,'TolFun',1e-9,'MaxFunEvals',2500,'MaxIter',2500);
27 tic
28 % Minimisation of the norm
29 [X_start,fval,exitflag,output] = fminsearch(f,[n_0,Vr_0, Lm_0
       ,Cr_0],options);
30 toc
31
32 % Final values
33 n = X_start(1);
34 Vr = X_start(2);
35 Lm = X_start(3);
36 Lr = Lm/3;
37 Cr = X_start(4);
38
39 function y = end_cond_finder(n,Vr0,Lm,Cr)
40
41 global Vin VD1_on Vout R_M R_D T Ir_0
42
43 Lr = Lm/3;
44
45 % ZONE 1M1D
46
47 A1 = [          0,                                          0,
       1/Cr;
48  -n/Lr, -(n*(Lm*R_D*n + Lr*R_D*n))/(Lm*Lr), -(R_M*n)/Lr;
49  -1/Lr,                                -(R_D*n)/Lr,      -R_M/Lr];
50
51 b1 = [

       0;
52         -(n*(Lm*VD1_on*n - Lm*Vin + Lr*VD1_on*n + Lm*Vout*n +
              Lr*Vout*n))/(Lm*Lr);
53                                                          -(VD1_on*n -
                                                              Vin +
                                                             Vout*n)/
```

```
                                                    Lr];

xp1 = -A1\b1;

[EVEC, EVAL] = eig(A1);
x0 = [Vr0; 0; Ir_0];
K = eye(3)*(EVEC\(x0-xp1));

x1_end = real(EVEC*(diag(exp(diag(EVAL)*(T/2)))*K) + xp1);

y(1) = Vin - x1_end(1);
y(2) = x1_end(2);
y(3) = -x1_end(3);

k1 = K(1)*EVEC(2,1)/EVAL(1,1);
k2 = K(2)*EVEC(2,2)/EVAL(2,2);
k3 = K(3)*EVEC(2,3)/EVAL(3,3);
y(4) = (real(k1*(exp(EVAL(1,1)*T/2)-1) + k2*(exp(EVAL(2,2)*T
    /2)-1) + k3*(exp(EVAL(3,3)*T/2)-1)) + xp1(2)*T/2)/(T/2);

end
```

A.5 ZCS from BVRHP (lossy LLC)

```
% 1M1D-1M2D

global Lr Cr Lm Vin VD1_on VD2_on R_M R_D n Vout

% Parameters of the converter under exam
Cr = 2.206720338616694e-08;
Lm = 6.028295474562004e-04;
Lr = Lm/3;
Vin = 400;
VD1_on = 0;
VD2_on = 0;
n = 7.728849370975870;
R_M = 1;
R_D = 0.1;
fn = zeros(1,170);
R1_v = zeros(1,170);
Vo = zeros(1,170);
```

```
18
19 % Inital guess of the unknowns
20 TD1_0 = 5.943069283280934e-06;
21 TD2_0 = 2.350478204968577e-06;
22 Vr_0 = -4.024684998907401e+02;
23 ID1_0 = 5.349257817509883;
24 Rl_0 = 1.685178671533467;
25
26 options = optimset('Display','iter','PlotFcns',@optimplotfval
     ,'TolFun',1e-9,'MaxFunEvals',2500,'MaxIter',2500);
27 tic
28 for i=1:170
29 Vout = 27.1 - 0.1*i;
30 f = @(x) norm(end_cond_finder(x(1), x(2), x(3), x(4), x(5))-[
     x(3), x(4),0, 0, Vout]);
31 [X_start,fval,exitflag,output] = fminsearch(f,[TD1_0,TD2_0,
     Vr_0,ID1_0,Rl_0],options);
32 TD1_0 = X_start(1);
33 TD2_0 = X_start(2);
34 Vr_0 = X_start(3);
35 ID1_0 = X_start(4);
36 Rl_0 = X_start(5);
37 Rl_v(i) = Rl_0;
38 fn(i) = pi*sqrt(Lr*Cr)/(TD1_0+TD2_0);
39 Vo(i) = Vout;
40 end
41 toc
42
43 plot(fn,Vo)
44 xlabel('fn')
45 ylabel('Vout [V]')
46
47 function y = end_cond_finder(TD1,TD2,Vr0,ID10,Rl)
48
49 global Lr Vin VD1_on VD2_on R_M R_D Lm Cr n Vout
50
51 y(1) = 10;
52 y(2) = 10;
53 y(3) = 10;
54 y(4) = 10;
55 y(5) = 10;
```

```
56
57 if TD1 > 0
58         if TD2 > 0
59             if R1 > 0
60
61 x0 = [Vr0; ID10; 0];
62
63 % ZONE 1M1D
64 A1 = [          0,                                          0,
       1/Cr;
65  -n/Lr, -(n*(Lm*R_D*n + Lr*R_D*n))/(Lm*Lr), -(R_M*n)/Lr;
66  -1/Lr,                                -(R_D*n)/Lr,      -R_M/Lr];
67
68 b1 = [

       0;
69         -(n*(Lm*VD1_on*n - Lm*Vin + Lr*VD1_on*n + Lm*Vout*n +
           Lr*Vout*n))/(Lm*Lr);
70                                                          -(VD1_on*n -
                                                              Vin +
                                                             Vout*n)/
                                                             Lr];
71
72 xp1 = -A1\b1;
73
74 [EVEC, EVAL] = eig(A1);
75 K = eye(3)*(EVEC\(x0-xp1));
76 x1_end = real(EVEC*(diag(exp(diag(EVAL)*TD1))*K) + xp1);
77
78 k1 = K(1)*EVEC(2,1)/EVAL(1,1);
79 k2 = K(2)*EVEC(2,2)/EVAL(2,2);
80 k3 = K(3)*EVEC(2,3)/EVAL(3,3);
81 int1 = (real(k1*(exp(EVAL(1,1)*TD1)-1) + k2*(exp(EVAL(2,2)*
       TD1)-1) + k3*(exp(EVAL(3,3)*TD1)-1)) + xp1(2)*TD1);
82
83 % ZONE 1M2D
84 A2 = [       0,                                          0,          1/Cr;
85    n/Lr, -(n*(Lm*R_D*n + Lr*R_D*n))/(Lm*Lr), (R_M*n)/Lr;
86  -1/Lr,                                (R_D*n)/Lr,      -R_M/Lr];
87
88 b2 = [
```

```
    0;
89  -(n*(Lm*Vin + Lm*VD2_on*n + Lr*VD2_on*n + Lm*Vout*n + Lr*
      Vout*n))/(Lm*Lr);
90                                                  (Vin + VD2_on*n
                                                      + Vout*n)/
                                                    Lr];
91
92  xp2 = -A2\b2;
93
94  [EVEC, EVAL] = eig(A2);
95  K = eye(3)*(EVEC\(x1_end-xp2));
96  x2_end = real(EVEC*(diag(exp(diag(EVAL)*TD2))*K) + xp2);
97
98  k1 = K(1)*EVEC(2,1)/EVAL(1,1);
99  k2 = K(2)*EVEC(2,2)/EVAL(2,2);
100 k3 = K(3)*EVEC(2,3)/EVAL(3,3);
101 int2 = (real(k1*(exp(EVAL(1,1)*TD2)-1) + k2*(exp(EVAL(2,2)*
      TD2)-1) + k3*(exp(EVAL(3,3)*TD2)-1)) + xp2(2)*TD2);
102
103 y(1) = Vin - x2_end(1);
104 y(2) = x2_end(2);
105 y(3) = -x2_end(3);
106 y(4) = x1_end(2);
107 y(5) = Rl*(int1+int2)/(TD1+TD2);
108
109             end
110         end
111 end
112
113 end
```

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