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Gate driver with an improved short circuit detection method for enhanced SiC MOSFET reliability

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Ringraziamenti

Ci siamo, finalmente, dopo sei mesi di tesi in Danimarca, scrivo la pagina piu' attesa. Quella che chiude un capitolo ma ne apre un'altro. Chi mi conosce sa che questa per me sarà anche la pagina più complicata. Le persone da ringraziare sono tante, ma il ringraziamento più grande va indiscutibilmente a mia mamma, che non si è limitata a fare tutto il necessario per garantirmi l'istruzione, ma con la forza che solo una madre può avere mi è sempre stata vicina credendo in me e motivandomi. Grazie Mamma, una pagina non basterebbe per spiegare quanto sei importante.
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A voi tutti, Grazie.

Abstract

The purpose of this Thesis is to research a new method for the detection of the Short circuit for SiC MOSFET. Currently, the existing methods to detect a Short Circuit or a system malfunction are not perfectly suitable for new technologies such as the SiC (Silicon Carbide), mainly because those types of devices are faster than the currently used methods to detect Short circuits. The protection must be as fast as the new technologies. Through this thesis, the need for a new method to detect Short circuits in SiC MOSFET will be justified. At the same time, the reader will be gradually introduced to and guided through this newly devised method of detection. In fact, the thesis will initially present the motivation of this research. As a brief introduction, the first chapter will be dedicated to explain the physics of electronic devices (material science) and the technology of the device, while the second one will focus on the Short Circuit phenomena in the SiC MOSFET. The goal is to gradually guide the reader through the analysis of the problem, to allow a better comprehension of the limits of the new device (SiC MOSFET) and to compare the pros and cons of it. The second chapter will also detail the need and the importance of researching a new and faster method to detect short circuits. The third chapter will be dedicated to analyse the existing methods used to detect the presence of a Short Circuit. Within the literature, many references can be found of existing circuits that claim to monitor different parameters. Aware of the existing gap in the literature and especially in the results, this chapter will illustrate and discuss the various advantages and disadvantages of using existing circuits to detect Short Circuits. Starting from this point, the fourth chapter will go more in depth. Indeed, the focus will be put on the SiC MOSFET and on the effectivity (or the lack thereof) of the existing methods used to detect Short Circuits within it. In the end, these methods will be compared with the newly devised Method at the centre of this research. Initially, the goal of the research was to detect short circuits only by monitoring the Gate, i.e. by using the parasitic inductance on the Source as a discriminant. Eventually a positive outcome would have had a considerable influence, since in this case, this newly tested method to detect short circuits would not have had to work with the power

section. Unfortunately, the effects of the parasite inductance did not lead to a significant variation of the Gate voltage. Due to this, non-functional methods will also be examined in detail, in order to highlight the reasons behind their malfunctioning and their lack of capacity to detect different types of short circuits (i.e. leg short circuits but not Load faults). The project adapted to the unsuccessful outcome and therefore other possibilities were taken into consideration. Indeed, the newly devised method, which will be detailed in the Thesis, exploits the variation of the drain voltage to determine the voltage on the drain itself using the concept of impedance or by indirect measurement. Using this information, it will be possible to understand if the Circuit is working properly. Finally, Chapters five and six will be dedicated to the design and the implementation of a method of validation. Two chapters are necessary to explain in details the adopted methodology and the results of the experiment. Indeed, the fifth Chapter will be dedicated to describe the design of the circuit built with the aforementioned newly devised method, as well as to describe the design of the system for the verification. On the other hand, the sixth Chapter will detail, explain and justify the results of the experiment and the actual advantages that this method can bring to existing systems like Inverters, DC/DC Converters and Motor Drivers. The prospective thesis aims to allow the academic community to better understand the use and peculiarities of the SiC MOSFET device and especially how to safeguard it. The device is worth of attentive protection due to its price, its fragility and especially its vital importance, as it has to maintain the entire circuit as reliable as possible. The validation of the new method described in this thesis will lead to considerably faster and more reliable detections of short circuits, especially considering the lacking current performances of more traditional methods eg. DESAT, Current monitoring, SenseFET, ecc. Obviously it is important to take into account the research limitations: a surge of the losses (Eon and Eoff) caused by using this method has to be considered. For example, the current that is taken by the measure circuit reduces the velocity of the turn on. Consequently, a slightly slower turn ON will compromise its efficiency performance. Consequently, further research to reduce the losses without decreasing the performances will have to be conducted in order to improve reliability of the aforementioned new method described in this Thesis.

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CHAPTER 1

SiC technology

1.1 SiC Power Semiconductor Devices

Within the power system, one of the most important figures of merit is efficiency. Even though this is related to several factors, the main one is related to the losses of the switch device.

There are several options to increase the efficiency of a power system. For instance, to devise a better topology for the circuit or to optimize some parameters, like increase the frequency of the switching or inject harmonics. Some methods are complicated, but they have a big effect. Otherwise other require less effort, but it has also a small effect. Certain methods used to increase the efficiency/to improve the performance of the parameters of a power circuit can be more complicated to devise but can lead to better results (i.e. Space vector modulation). On the other hand, certain solutions can be easier to devise but could lead to under-performing power systems. For example, use a device with fewer losses. For designers, sometimes one of the easiest options is simply to upgrade the technology of the Switch. Indeed, the biggest drawback for designers to devise solutions that are more complicated for a technological point of view is an higher cost, while for the manufacturer this requires a great commitment. The manufacturers are motivated to look for new technologies not only to increase the cost of the device, but also to be more competitive towards other manufacturers. Within this philosophy, the new era of Silicon Carbide (SiC) technology was born.

Silicon Carbide MOSFET is a device that exploits the Wide Band Gap technology. The polymorphism of SiC is characterized by a large family of similar crystalline structures called poly-types. They are variations of the same chemical compound that is identical in two dimensions and differs in the third one. Thus, these variations can be viewed as layers stacked in a certain sequence. Alpha silicon carbide ($\alpha - SiC$) is the most commonly encountered polymorph, and is formed at temperatures greater than 1700 °C and it has a hexagonal crystal structure. [23] The beta modification ($\beta - SiC$), with a zinc blende crystal structure, it is formed at lower temperatures.[13] SiC exists predominantly in 3 poly-types, according to its crystal arrangement: 3C, 4H and 6H. 4H-SiC is preferred over the other poly-types because it has the highest mobility and bandgap among the three. The different types are visible in the Figure 1.1.

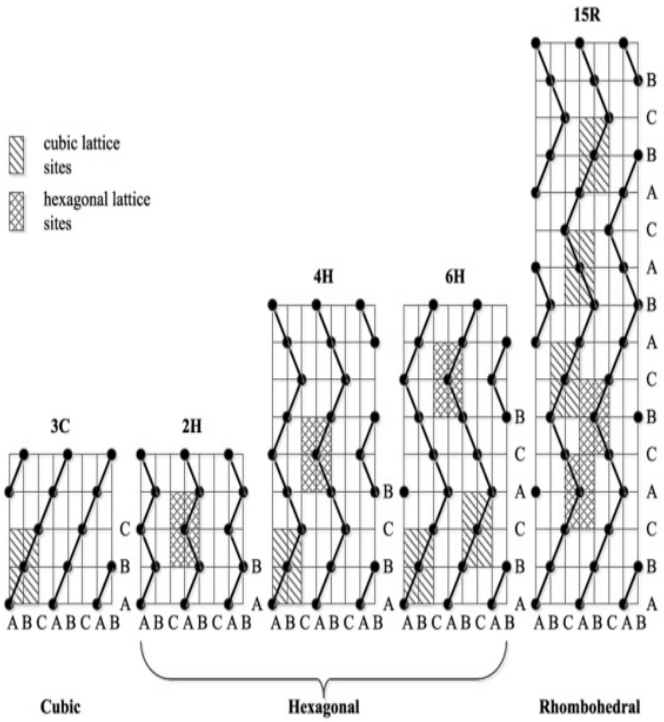

Figure 1.1: Polytypes of SiC [18]

1.2 Band Gap

The first difference between SiC and Si is their energy band gap. Indeed, the silicon carbide has a band gap
larger than the one for silicon, for this reason it is classified as a wide band gap semiconductor. The band gap for 4H-SiC is 3.26 eV, which is three times larger than that for silicon (1.1 eV)[13]. A larger band gap is also favourable for producing Metal-Semiconductor contacts with larger Schottky barrier heights. Consequently a larger band gap results in a smaller thermal generation of carriers in the depletion region. Since thermally generated carriers cause current leakages in the off-state, SiC has considerably lessen this problem by blocking voltage, especially when compared to Si.[4] The concentration of thermally generated electron-hole pairs at any given temperature determines the intrinsic carrier concentration. Furthermore, electron-hole pairs are one of the main functions of the bandgap. For example, by looking at Fig. 1.2, it can be stated that the the intrinsic carrier concentration of Si increases from $1.4 \times 10^{10} cm^{-3}$ at room temperature to $1 \times 10^{15} cm^{-3}$ at 600K. Instead, SiC has a very low intrinsic carrier concentration, in the order of $6.7 \times 10^{11} cm^{-3}$ at room temperature, and it increases to only about $3.9 \times 10^{7} cm^{-3}$ at 700 K. This low carrier concentration at elevated temperatures enables SiC devices to retain their doped region properties over a wide range of temperature. [13]

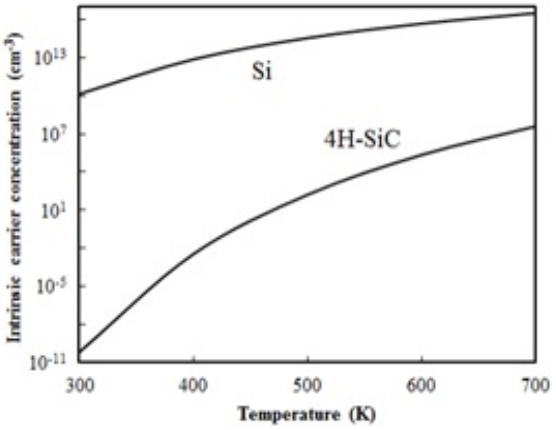

Figure 1.2: Intrinsic carrier concentration vs Temperature [13]

1.3 Critical Breakdown Electric Field

One of the main advantages offered by SiC is a high value of the critical breakdown electric field. The higher critical electric field is the reason why SiC device has higher working voltage. Moreover, with the same working voltage, the drift region of SiC devices had lower resistance because the thickness could be less than Si. It is possible to evaluate the maximum electric field by analysing the impact ionization process of a material, which forms in presence of an electric field. Indeed, under the influence of an electric field a positive or negative particle would accelerate, as an electron would be accelerated in the opposite direction of the applied field. As the particle accelerates through the material, it will eventually collide with a lattice atom. With the collision, the particle will transfer some of its energy to the atom. If the imparted energy is higher than the bandgap of the material, an electron inside the atom will absorb the excess energy and it will jump to the conduction band, thus creating an electron-hole pair. Hence, the newly-generated pair of e-h accelerates due to the presence of the external electric field. If the electric field is big enough, the particles could collide with the lattice and could create a chain effect. The critical breakdown electric field is defined as the maximum electric field that can be sustained across the material before the generation of electron-hole pairs (due to impact ionization) and becomes a destructive process, which will result in a sudden large increase in current through the material. [18]

1.4 Electron Mobility

In silicon carbide the mobility for electrons is much bigger than holes because of the holes. It is therefore favourable to create unipolar devices using N-type drift regions instead of P-type drift regions. The resistivity of the drain to the Source device is mainly due to the conductivity of the drift region. It follows the eq:

$$\rho_N = \frac{1}{qN_D\mu_N}$$

where μ_N is the mobility for electrons, which is a function of doping concentration N_D, and temperature T. The electron mobility also depends up on the temperature.

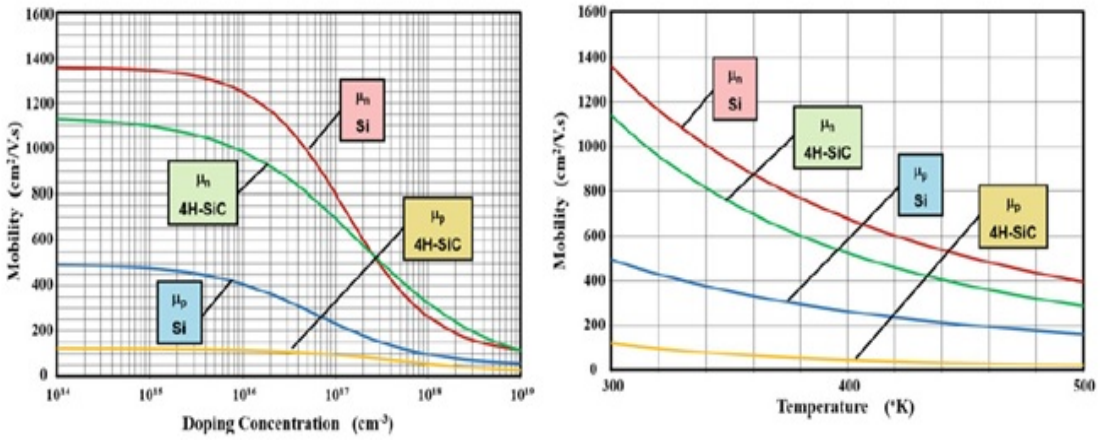

Figure 1.3: Mobility vs Doping concentration and Temperature

As it can be seen, the mobility decreases in semiconductors when the temperature is increased, due to the enhanced photon scattering. This holds true for Silicon and 4H-SiC. Once understanding the electron Mobility, the R_{on} resistance can be easily calculated with the following formula:

$$R_{on} = \frac{4 \cdot V_B^2}{\epsilon \mu_N E_C^3}$$

Where V_B is the breakdown voltage and E_c is the critical electrical field, the unit of measurement for the on-resistance is $m\Omega \cdot cm2$. Based on the equation above, Ron is reversely proportional to E_c, which means an higher E_c leads to a much lower R_{on} for 4H-SiC. It is important to acknowledge that also the saturation velocity phenomena influence the resistivity. In the Fig. 1.4 is showed the Carrier velocity of Si and SiC depending on the electric field.[13]

$$E_c = \frac{\upsilon_{sat}}{\mu}$$

It can been noticed that in 4H-SiC's saturated electron drift velocity of $2 \times 10^7 cm/s$ is about twice than silicon's. [13]

1.5 Higher Temperature

The thermal conductivity of the semiconductor is highly important where the heat generated from the device losses needs to be dissipated and the junction temperature

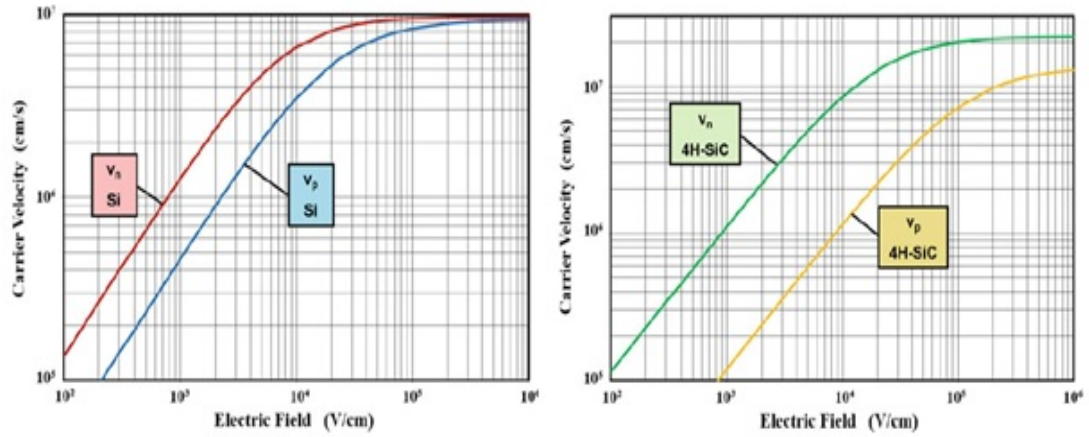

Figure 1.4: Carriers velocity Si (left graph) vs Carrier velocity SiC(right graph)

of the junction kept low. Considering high power applications, especially in the case of high ambient temperatures, good heat dissipation is highly desirable as this would result in a lower junction temperature and a higher power density. In addition, the thermal conductivity of the SiC-based devices, is 4.9 W/cmK, which is many times higher than the one of Si (1.5 W/cmK). For this reason, the thermal conductivity of the SiC device allows a greater power density when compared to Si. [16] In conclusion, critical electronic breakdown, electron mobility and better response to higher temperatures are only some of the most important benefits that can be obtained when using SiC devices instead of Si. There are others like recombination lifetimes and the Metal-Semiconductor Contact that make the SiC device attractive. To sum up, there are many benefits to use a wide band gap (SiC) rather than a Si material. SiC possess ten times the dielectric breakdown field strength, three times the bandgap, and three times the thermal conductivity. Moreover, the Electron Mobility of the SiC device but it is not very low ($1000\frac{cm^2}{V_S}$). Both p-type and n-type regions, which are necessary to make device structures in semiconductor materials, can be formed in SiC. These properties make SiC an attractive material, from which it is possible to manufacture power devices that can far exceed the performances of their Si counterparts. In the table below shows a comparison between the properties of different materials. By looking at the table, the possible advantages for using SiC devices in power device applications are remarkable. Indeed, the dielectric breakdown field strength is approximately 10 times higher than the one for Si. SiC devices

can be designed to have much thinner drift layer and/or higher doping concentration than Si technology, i.e. Sic devices have very high breakdown voltage (600V and up) and yet a very low resistance when compared to silicon devices. Moreover also the Drain to Source resistance could be lower than Si devices for the same reason. In fact in Power devices the resistance of high-voltage devices is predominantly determined by the thickness of the drift region. In theory, SiC can reduce the resistance per unit area of the drift layer to 1/300 compared to Si, at the same breakdown voltage. [13] It is important to notice that these material properties support the use of SiC for electronic devices, which are operated at high temperature, high power and/or high frequency. However it is recommended not to exceed operating temperatures of about 600 °C. In literature operation temperature devices up to 300°C could be found. Obviously the estimated life time is only 1 year.[12] Si devices, on the other hand, can operate at a maximum junction temperature of only 150°C. [16]

1.6 Overview of SiC Device

The benefits of using its materials are different, but there are also several downsides. One of most critical is related to the fragility of the gate oxide. This technology is currently used on different device. Bipolar Junction Transistor (BJT), Junction Field Effect Transistor (JFET), Insulated Gate Bipolar Transistor (IGBT) and Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are the major types of structures that are usually employed in power circuits. BJT is a bipolar device, in which the conductivity of a part of the collector region is modulated by the minority carrier injection at on-state, which can lead to have a reduced resistance. However, in SiC BJT, the forward voltage drop increases significantly after high current stress, due to recombination-induced stacking faults migration in the drift layer [18]. Therefore, minority carrier injection should be avoided in SiC-based power devices unless material quality has been greatly improved. The bipolar nature of BJT also limits the switching frequency because of charge storage in the device. Furthermore, as a current-driven transistor with a relatively low current gain, the device shall be controlled by complicated gate drive circuit [16]. On the other hand, JFET is not used because it is a device that normally has to stay switched on. For this reason

it is not safe to use it in power applications. However, IGBT is basically a bipolar transistor driven by a power MOSFET. It has the advantages of being a bipolar device, and low impedance of the insulated gate, which requires simple gate drive circuits. But on the other hand, similarly to BJT, its bipolar nature gives rise to the recombination-induced stacking faults migration, and the switching speed is limited as well. Moreover, it causes forward voltage drop greater than 2.7 V due to the built-in voltage in the SiC p-n junction, which confines the practical use of SiC IGBT to applications where the blocking voltage is higher than 5 kV. MOSFET structure is advantageous over other devices. The gate input impedance is much smaller even when compared to JFET, therefore the gate drive circuit requires very little power to be controlled. The uni-polar nature permits faster turn-on and turn-off speed compared to BJT and IGBT, and there is no stacking faults migration problem. In contrast to IGBT, there is no built-in forward voltage drop. The two most favourable power MOSFET structures are DMOSFET and UMOSFET. Their structures are depicted in Fig.1.5. The main difference between them is the placement of channel region. In DMOSFETs, the inversion channel is located laterally on the surface of the implanted pwell region, whereas in UMOSFETs, the channel is located vertically on the surface of the trench in the epitaxial p layer. UMOSFETs has lower on-resistance compared to DMOSFETs due to the absence of the JFET region and higher channel mobility. However, the blocking voltage is limited by the oxide breakdown at the trench corners.

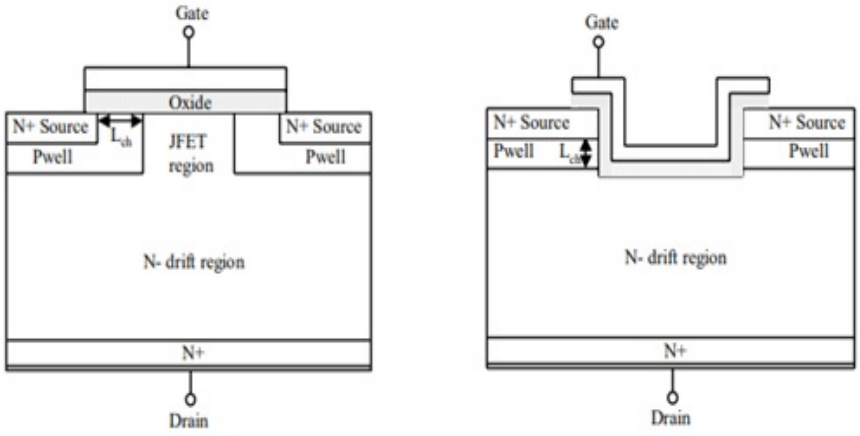

Figure 1.5: Section DMOSFET and UMOSFET

The SiC MOSFET works in the same way to Si MOSFET. There are differences between the two systems on the topic of physical properties of the material or construction; however they will be explained in the next chapter. Some of the main properties of silicon and silicon carbide relevant to power devices have been reviewed and compared in this chapter. Particularly important the analysis and operation of power devices, and they are the impact ionization coefficients, which determine the breakdown voltage capability. Or the carrier mobility, in the bulk and at inversion layers formed at the oxide interface, is another important parameter that is required for the analysis of unipolar and MOS-bipolar structures.

CHAPTER 2

Short circuit

2.1 Statistic Short circuit fault

Silicon Carbide has features that make technology attractive when devising power systems. But the same peculiarities make SiC technology more sensitive. For instance, the value of the critical breakdown electric field allows a thin drift region. It is therefore possible to have a lower Drain-Source resistance for the same amount of breakdown voltage compared to Si technology. On the other hand, to have a thinner drift region causes problems in critical conditions especially in the short circuit condition. There are several articles in the literature discussing the fragility of SiC devices. In figure 2.1 are showed the most probable scenarios of failure in case of Short circuit. [3]

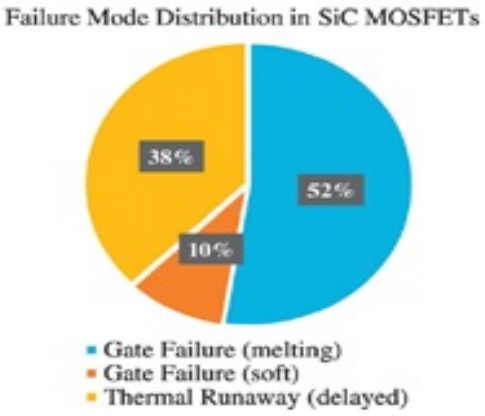

Figure 2.1: Percentage Fault Short Circuit

The most accredited theory links the fragility of the device to the rising in temperature in the drift region in the event of a short circuit. In addition, with the small thickness of Drift layers warms up the interface between the channel and the gate. The damage due to the heating of this region can create three different phenomena, which can result to the total or partial destruction on the circuit. [6]

2.1.1 Gate oxide breakdown (melting)

The most common failure caused by the overheating of the SiC device is the Gate oxide breakdown. It occurs when the junction temperature increases, causing a short circuit. Hence, the Oxide layer deforms and defects are created. Initially the result of this condition is an increase of the leakage current and a degradation of the threshold voltage. But if the short circuit is not interrupted, the temperature reaches values that break the Oxide of the Gate. Figure 2.2 shows a real waveform of the gate oxide failure.[15]

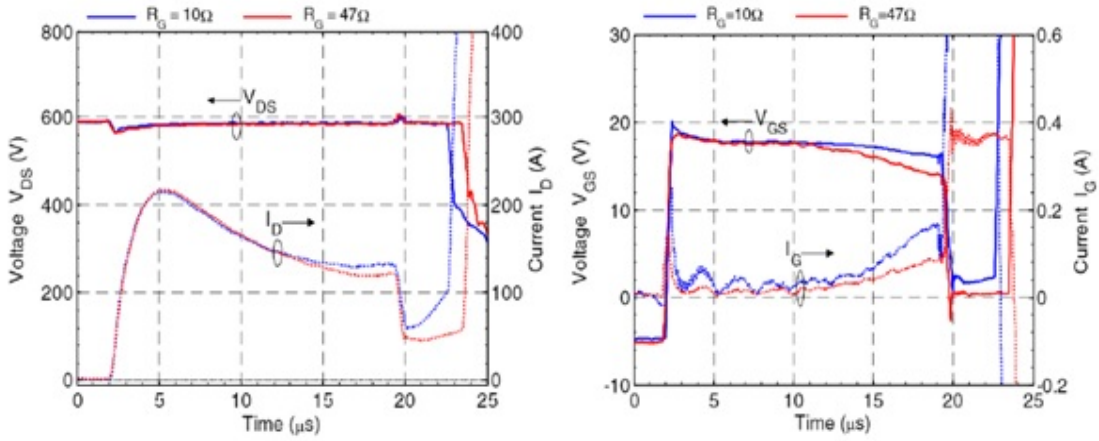

Figure 2.2: Typical Gate oxide breakdown Short Circuit Failure [8]

This is a typical reaction during a short circuit, the Drain to Source voltage does not drop because there is not load. Therefore, the Drain current rises very fast above the nominal value of the device. The energy involve is very high and in few micro seconds the temperature inside the device reaches high values. The junction is able to work at high temperatures, but not the gate. The leakage current starts to increase when the junction Temperature around 700°C [22]. It can been see that looking the Gate leakage current, it increases during the short circuit. It reaches high value in

static condition before the device failure. It is very important to detect the short circuit as quickly as possible. The failure can occur also after the detection and after the shutdown of the device, since the energy inside the device could have previously reached high peaks. Heat propagates slower than electricity. For this reason it is very important to quickly detect short circuits.[8]

2.1.2 Gate oxide breakdown (soft)

As already mentioned the first effect of the short circuit is the degradation of the threshold voltage and the increase of the leakage current. If one device s short circuits, it can still continue its operations, but the reliability of the system it suffers. [2] This is visible in figure 2.3 (on the left), which represents it can see the degradation of the device after short circuits, while figure 2.3 (on the right) shows the value of the threshold after repetitive test. [5] Tests are performed always with the same pulse width of 14µs and a V_{ds} much smaller much smaller than the one necessary to cause a wider pulse width.

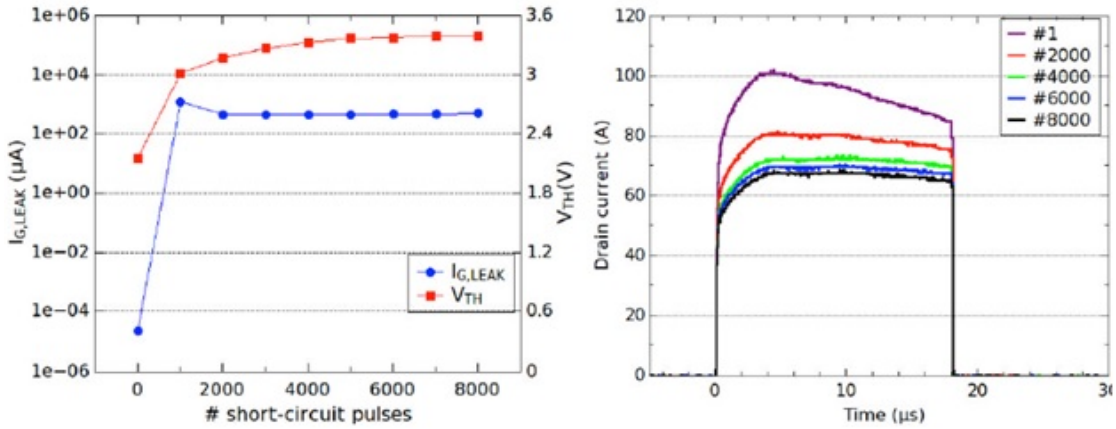

Figure 2.3: (left) Degradation of Threshold and leakage current Pulse after #n cycling (right)[5]

The following graph represents a relation between the short circuit pulse and the leakage current for different Gate Driver voltage.[2]

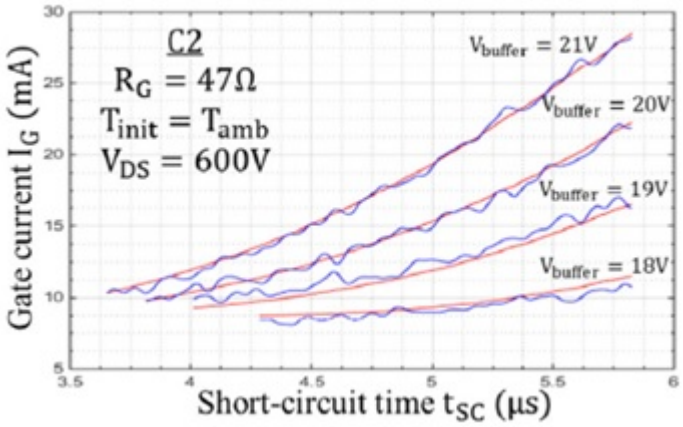

Figure 2.4: Leakage Current [2]

The devices under test are 1200 V, 50 A (DUT1: 4 × 4 × 0.4 mm) and 1200 V, 28 A (DUT2: ca. 3.1 × 3.1 × 0.4 mm) rated, vertical SiC power MOSFETs.

2.1.3 Thermal Runaway

In more details, the high energy released in the MOSFET channel region increases temperature. Than the thermal generation carriers generated in the Body in addition with the carriers in the carriers in Drift region creates a drain leakage current, which can reach considerable values. As already mentioned, the SiC MOSFET cell structure is much thinner and narrower compared to Si devices, which make higher power densities. Thus, the energy density is relatively high and the junction temperature during short circuit can even reach 1000°C. The leakage current starts to increase with junction Temperature around 700°C [22]. The heat dissipation is slower than the leakage current increasing rate. The combination of these two effects delays the failure after the turn off of the device. Local defects or slight manufacturing differences can induce a weaker cell to absorb more current than the other nearby. The process is irreversible and causes the formation of a hot spot in the die with uneven current density and temperature, which leads to the melting of the structure with a drain-to-source shorting as a result. In power modules, manufacturing mismatches are a lot of involve in this phenomenon, it is worsened by the unbalanced current sharing among the parallel dies. Due to high temperature the depletion region creates intrinsic carrier, it carrier density increases the temperature so the car-

rier density leads to a thermal generation current. [22] The injection of minority carriers (holes) in the p-body region can also trigger another mechanism: the turn-on of the parasitic bipolar transistor. Amplified by the leakage current, it determined by the activation of the BJT accelerates the thermal runaway failure process.[7] This happens because in short circuit conditions, the drain–source voltage after a small initially drop due to the inductance and then recovers again to the input source voltage quickly. As a result, the temperature rise inside the device becomes quite severe due to the large power dissipation. As the temperature increases, the impedance inside the device also arises quickly, causing thermally negative feedback which reduces the drain-to-source current. This negative feedback does not save the device, since it does not stop the temperature from rising. [6]

2.2 Classification of Short Circuit types

To have a better classification of short circuits, the literature subdivides this phenomenon in three classes.

2.2.1 Hard Switch Fault

- **HSF** (Hard Switch Fault.): When a SC load is applied during the off-state of SiC MOSFET, following the turning on of the device under Short Circuit load [21]. When the switch is turned-on, the current through the device arises, as determined by the gate voltage and the chips trans-conductance. The device can not commute, so the voltage V_{ds} is under full DC-link voltage.

The failure happens when the device is switched off. Therefore, when it will start again to conduct current, there will be a high slope. During t_1 to t_2, due to the positive di/dt, there is a voltage drop on stray inductance, which causes a voltage undershoot on the device drain source voltage. At t_2, the device is in

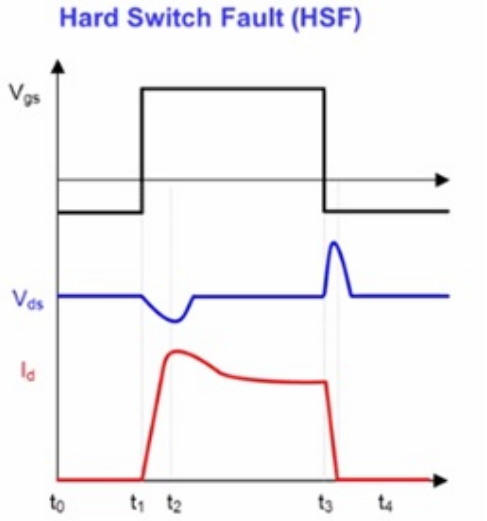

Figure 2.5: Simplified waveform Hard Switch fault [20]

saturation mode, as if it was undergoing load fault. There is a significant amount of heat generated during phases t_2 to t_3. The self-heating process provoked by high current density causes a reduction of carrier mobility in the drift region.
Thus, as in FUL situations, the current decreases. It is important to remark that during the switching under short circuit condition, there is not Miller Plauteu. Factors such as the changing of slope after the switch off (t_3) and the tail current due to high concentration of minority charges (due to high temperature) have not been taken into account in this paragraph to have a simplification of the process.[1]

2.2.2 Fault Under Load

- **FUL**(Fault Under Load):It occurs when the complementary switch fails or the complete load inductance is short-circuited, while the DUT is already fully turned-on and conducting current.

Between t_0 to t_1, the MOSFET is in on state and it works in linear region. The fault happens at t_1 V_{ds} is determined by the $R_{DS(ON)}$ and by the drain current. After t_1, a short circuit event happens and the device transits from the linear region to a saturation region in a short time. During t_1 to t_2, the I_D and V_{DS} increases quickly and this event generates high dV/dt and dI/dt. Consequently, an high dV/dt generates a current through Miller capacitor to the gate loop, which may cause overshoot voltage on V_{GS}, which could break the device. At t_2, the device is in saturation mode.

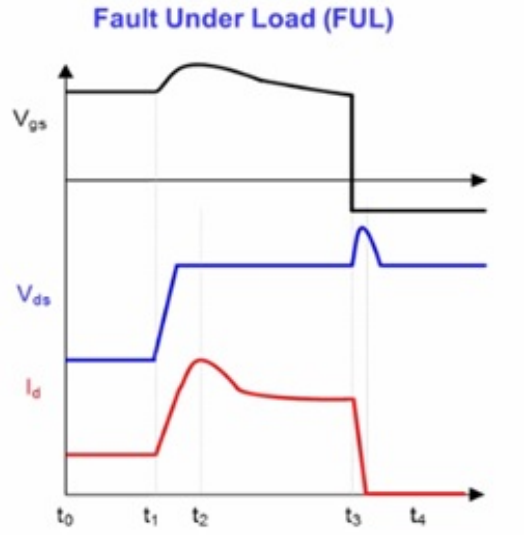

Figure 2.6: Simplified waveform Fault under Load [20]

A significant amount of heat is generated during t_2 to t_3. Therefore, the I_{value} begins to decrease with the reduction of the carrier mobility, which itself has been caused by the rapid self-heating.
At t_3, the device is shut down by the gate driver. From t_3 to t_4, the drain current is cut off and a significant high di/dt is generated, which causes a large voltage spike on the device. The voltage spike can be as high as the DC bus voltage, which can cause the device breakdown. For this reason, it is important to have a slow turn-off. Compared to IGBT, this fault is more difficult to detect: the characteristic Vds/Id causes a smaller variation of drain-source voltage.[1]

2.2.3 Over Current

- **OC**(Over Current):It happens when a load partition is short-circuited. This phenomenon can occur also in case of a diverse range of intensities. Notwithstanding that, a threshold are is always required, since not all over currents are destructive.

When the Partial Fault happens, in t_1 the Drain Voltage rises. Hence, the Gate voltage has an positive over voltage due to C_{gd}.

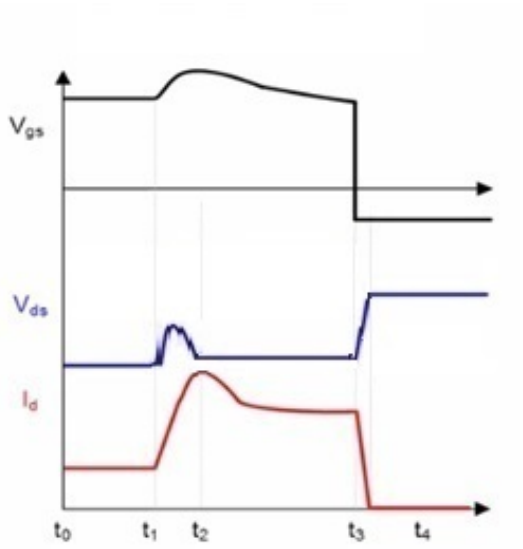

Figure 2.7: Simplified waveform Over Current

CHAPTER 3

Fault Detection and Protection

3.1 Fault detection

Engineers always try to avoid possible malfunctions of their devices. But it is also the task of them to protect devices from possible failures. The only way to be sure not to run into it is avoiding the problems, foresee devising circuits that are able to recognise the presence of a short circuit and that can automatically intervene by deactivating power. Obviously the faster is the method, the higher are the chances to save the device. There are currently various methods: The most common are Desaturation Method, Parasitic Inductance Method, Gate Charge Method and other methods that directly measure the Drain Current.

3.1.1 Desaturation Detection Method

The Drain-Source voltage is used as an indicator of a short circuit. This method does not measure the Drain voltage directly, but it measures indirectly using a Diode. Fig. 3.1. shows the circuit of principle.
The advantages of using this method are its simplicity, the low system losses and the protection time tuneable. While the challenges related to the use of this method are HV fast recovery diodes: multiple HV diodes are needed in high voltage application, therefore response time is could be too long for SiC technology and accuracy is lower. The operating principle of a circuit entails that when a device is turned on, a current source charges the blanking capacitor and the diode is conduce. During normal oper-

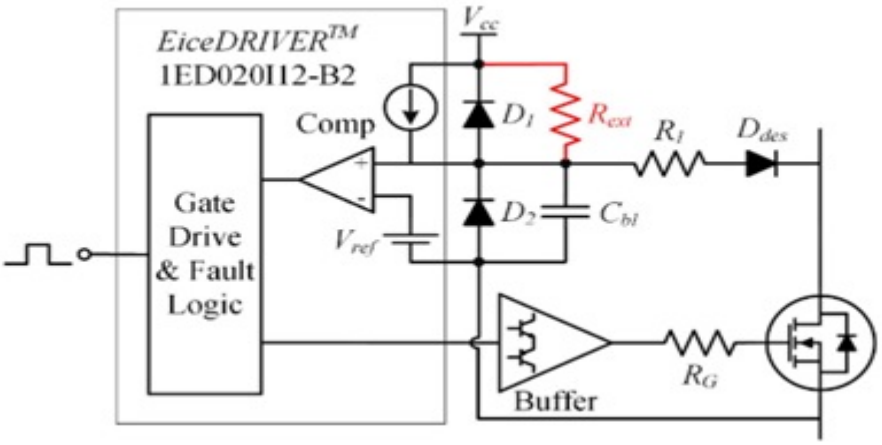

Figure 3.1: Principle of operation Desat [24]

ations, the capacitor voltage is clamped at the forward voltage of the device. When short circuit occurs, the voltage on the drain does not reach the forward voltage, so diode is in reverse. The capacitor voltage is quickly charged to the threshold voltage, which triggers the device shutdown. The capacitor charging time is called blanking time. By changing R_{ext}, it is easy to modify blanking time. [24] In general the threshold is around 7V-9V.

3.1.2 Shunt resistor sensing

Probably the easiest one, because it requires a resistance and an amplifier. As shown in Fig. 3.2, a very small resistor is connected in series within the power loop, to sense the current. This method obviously leads to efficiency losses in power loops. It is used in low performance applications. The accuracy of this method is mainly determined by the sensing resistor. Moreover, during switching transients, large current causes voltage spike on parasitic inductance of sensing resistor and on the PCB traits. In this case, false poles can be produced in gate driver loops. For high power applications there are devices, such as the Rogowski coil, capable of measuring currents indirectly by using magnetic fields. But typically, their responses are not fast enough, therefore such device should not be used as HSF or FUL short circuit protections. Eventually, these methods could be more suitable to over current. [9]

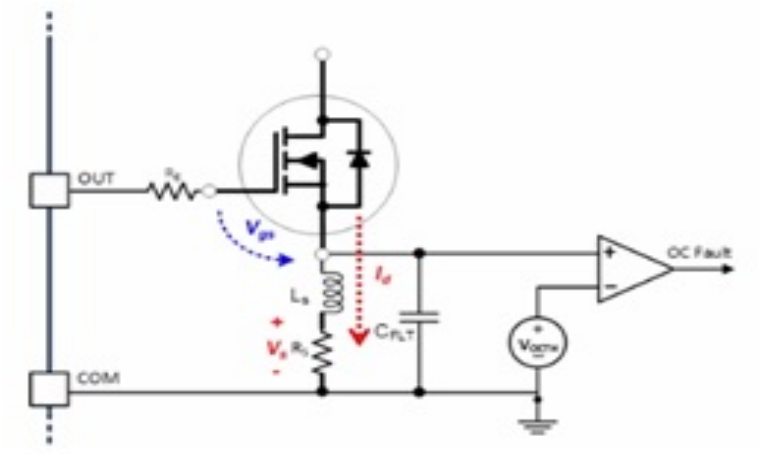

Figure 3.2: Principle of operation Shunt Resitance [9]

3.1.3 SenseFET/Current Mirror

The senseFET is normally integrated within the power module, connecting in parallel with the main device to scale down the device current. The scaled down current is then measured by an accurate shunt resistor. It has the fastest protection speed, moreover it is also accurate for both AC and DC current sensing. The biggest challenge for this method is cost. To guarantee an accurate current scaling, the SenseFET or Current Mirror should be located as close as possible to the main device and this requires specific design modules. Furthermore, it is very similar to a shunt resistor, except for the loss of efficiency. [9] Fig. 3.3 shows a simplification of the circuit.

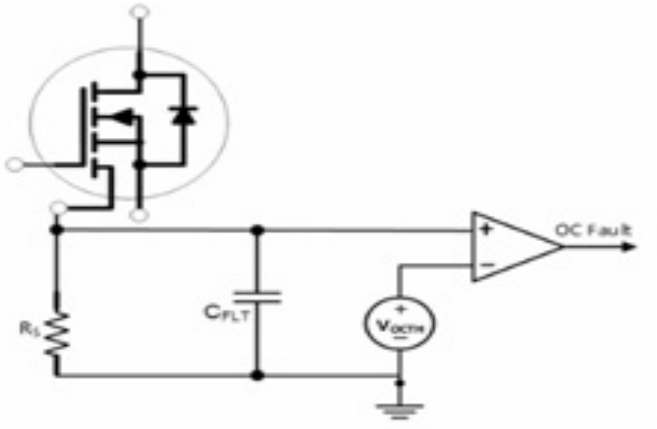

Figure 3.3: Principle of operation SenseFET [9]

Currently on the market there are few devices that implement this current mirror.

3.1.4 Gate Charge/voltage

This method uses the possibility to detect the short circuit only by looking at the gate charge. In fact, as it can be noticed in Fig. 3.4, the gate charge changes in case of a short circuit. [19] This method can detect the short circuit before gate source voltage reaches 15V, so that it achieves a shorter protection time compared than the previous method. The gate-charge monitoring method (Q_g-monitoring method) detects the HSF because the amount of gate charge under HSF conditions is smaller than that under normal turn on conditions[25]. In addition, this method generates unnecessary power dissipation because it uses a current mirror circuit. In SiC MOSFETs, the Gate–Source voltage V_{gs} rises gradually during Miller plateau, so that the reference value of the Gate–Source voltage to detect the HSF can be set to an arbitrary voltage in Miller plateau. Hence, this protection method is suitable for SiC MOSFETs. [11] Fig. 3.4 depicts a comparison between gate charge characteristics under normal conditions and HSF conditions. When the Gate–Source voltage is lower than $V_{miller1}$ which corresponds to the voltage at the beginning of the Miller plateau, no difference is found in gate charge characteristics between normal turn-on conditions and HSF conditions.

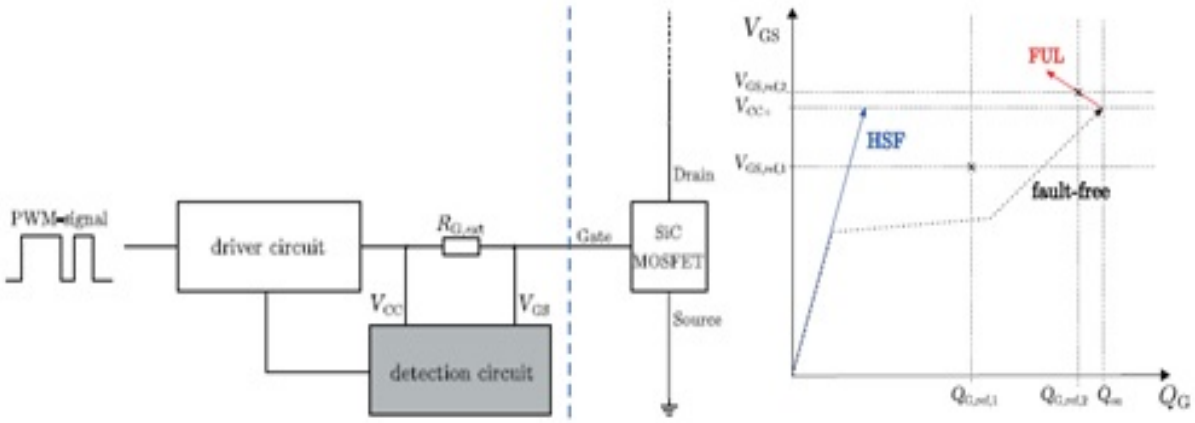

Figure 3.4: Principle of operation Gate Charge/Voltage [17]

Indeed, the gate charge inspects the connection from the driver to the gate of the MOSFET. Moreover, this method does not require a high voltage diode or a current to sense as the Desat or the Shunt method actually do. The Miller effect, which can be detected during fault-free switch-on processes, is omitted in case of a HSF, since

the voltage does not change significantly. Experiments has have confirmed that the proposed circuit can detect the HSF within only $1\mu s$. [14] But this could be a problem in case of a circuit that works also in soft switch: in this case, the Miller Platue would not be present, but short circuit maybe is not present.

3.1.5 Parasitic inductance method

This circuit exploits the presence of the parasitic Source inductance between the Source power pin and the Kelvin Source. Figure 3.5 shows a more complicated schematic of the method compared to the previous one. The method is the most complicated and expensive, but the detection speed is good. The circuit measures the voltage variations between the Kelvin source and the Source power pin, which are caused by the parasite inductance. For this reason, it is mandatory to have the Kelvin Source available. Whenever there is a variation of the drain current, the drain current also passes through the parasitic, which reacts by imposing a voltage drop. Subsequently, this voltage drop can be measured and related to the current difference. This method requires a calibration to know exactly what is the value of the parasitic and to compensate the other unwanted components that might influence the data. [21]

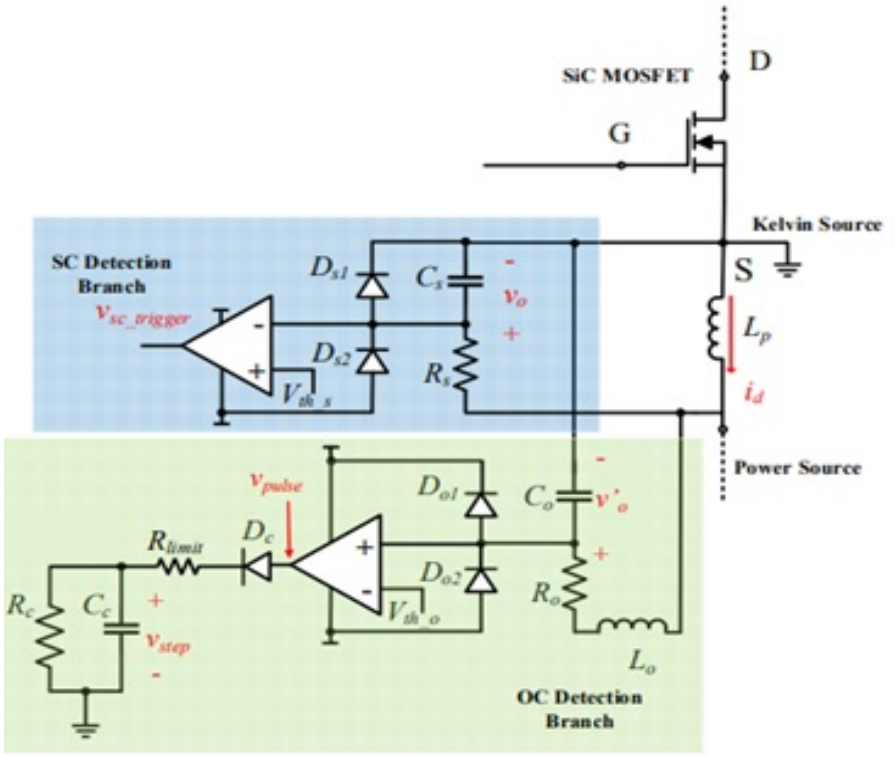

Figure 3.5: Principle of operation Parasitic inductance method [21]

3.2 Fault Protection

Once the short circuit has been identified, action must be taken and therefore the device must be switched off. There are several ways to turn off the device in this case. It depends on the implementation, sometimes it is preferable to have a very fast turn off, while other times it is preferable to avoid fast transitions. The easiest one it is using only a MOSFET connects in parallel to the C_{gs}. This is also the fast one. However, for high power budget application a suddenly turn-off could create side effects. In fact, when a device is fully conducting with a very large Drain current because of the presence of SC, a sudden switch-off would cause great voltage spike. Figure 3.6 shows a typical implementation in case of a gradual turn off in two levels of a device.

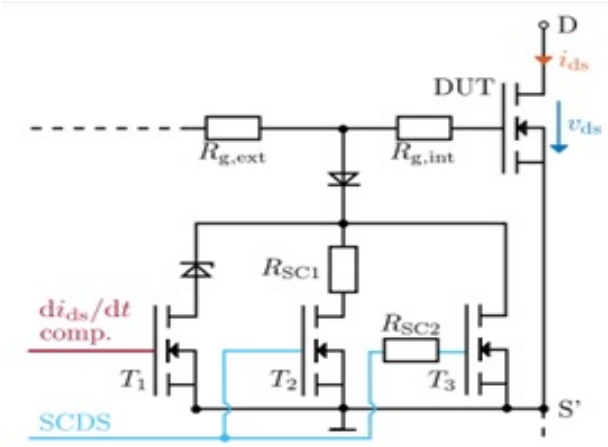

Figure 3.6: Principle of operation two levels fault protection. [10]

When the DUT has to switch off, the SCDS increases, then T_2 is the first device that turns on and consequently, the gate capacitance of the DUT will be discharged softly. After a certain amount of time (defined by R_{sc2}) the DUT will be quickly discharged. [10]

3.3 Overview

In table 3.7 there is an overview of the discussed methods used to detect short circuits. It is also shown the typical detection times and the Advantages and the disadvantages in using one method over the other.

Method	Implementation effort	Advantages	Disadvantages	Influence on power circuit	Typical detection times
Desaturation detection	Low	Shorter blanking time compared to Si modules	Temperature dependent; Fixed delay	Low	120 ns (HSF) 20 ns (FUL) [14]
Parasitic inductance	Very low	direct information about I_D	Only for 4-pin modules; Difficult determination of stray inductance	Low	80 ns (HSF) [12]
Gate charge/voltage	Medium	Non invasive detection	Strongly dependent on exterior circuit	None	1 µs (HSF) [13]
Shunt Resistance	Low	Easy implementation Low cost	Efficiency Accuracy	High	Not verified for High Power
SenseFET/Current Mirror	Medium	Fast detection	Requires specific devices	Low	Not verified

Figure 3.7: Summary table Fault detection Method [17]

As it can be deduced from the table, the fastest HSF method to detect short circuits is Parasitic inductance. Given this conclusion, the first method that was analyzed during the thesis to develop a study with the aim to improve this method, in order for it to be used only with 3 Pin, without the Kelvin Source. Ideally it would be feasible to do so: in case of a voltage perturbation, the capacitor located between the source and the gate would report for a short time the perturbations of the source, and it would also do so on the gate.

CHAPTER 4

Analysis Fault detection Method

During the thesis several methods were analyzed. However, not all of them turned out to work properly. In the first part of this chapter the two not-working methods have been reported. In the second, the method used in the thesis to detect the short circuit will be reported. This method was called "RC method".

4.1 Fault detection method rejected

4.1.1 Parasitic method without kelvin Source

As mentioned in the previous paragraph, given the existing literature analysing possible methods to detect short circuits, the aim of the further research that will be presented focuses on the possibility to use the parasitic inductance without the Kelvin Source pin to detect short circuits. As it can be seen in Figure 4.1, the parasitic inductance is in the loop of the gate driver. The voltage drop on the parasite inductance of the source influences the effective voltage between the gate and the source. 4.1 therefore, an excessive variation of the drain current will consequently influence the gate-source voltage.

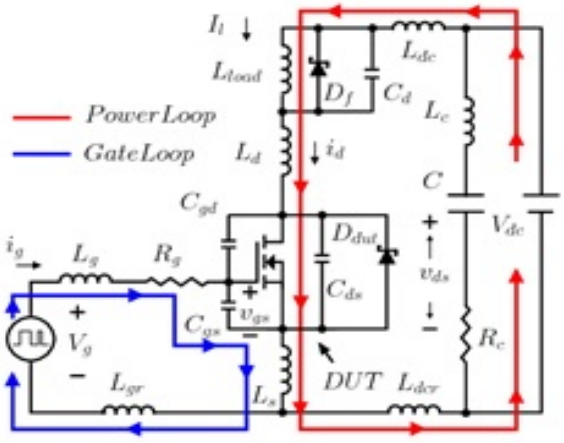

Figure 4.1: Power Loop and Gate Loop current

Analytical verification of the influence of the parasitic inductance can be performed by doing KVL at the Gate Loop. It showed in the equation 4.1 the dependency. The dependency of the parasitic represented in figure 4.1 can be described with the following equation:

$$V_g = L_g \frac{\delta V_{Lg}}{\delta t} + R_g \cdot I_g + v_{gs} + L_s \frac{\delta V_{Ls}}{\delta t} \tag{4.1}$$

Moreover, to verify how the terms related to L_s influence the v_{gs}, parametrization simulation was performed. With this test the parasitic inductance changed the effective gate source voltage. An LTspice circuit is shown in figure 4.2, while the results of the simulation are shown in Figure 4.3.

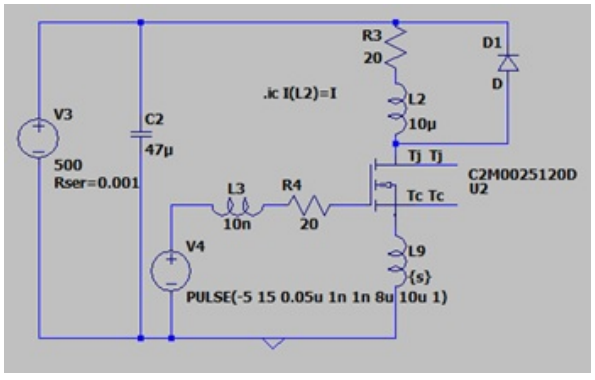

Figure 4.2: Circuit used for simulation

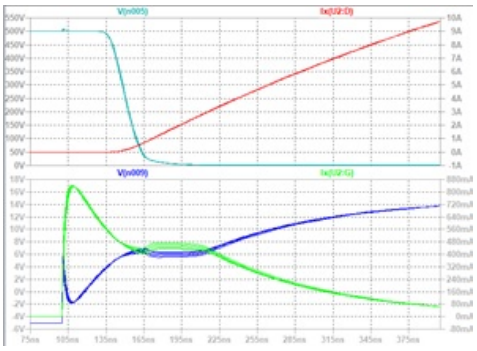

Figure 4.3: Simulation showing the correlation

Legend Fig 4.3: BlueL: Drain Voltage, Red: Drain Current (SWP), Blue: Gate Volt-

age, Green: Gate Current

Inductance L_d was varied between 5nH and 50nH, with a step of 5nH, while $R_l = 20\Omega$, $R_{sc} = 0.5\Omega$, $V_{dc} = 500V$, $R_g = 20\Omega$ and $L_s = 5nH$. The DUT is C2M0025120D, while the model of the represented was downloaded from the manufacturer's website (http://go.wolfspeed.com/all-models). By analysing the results of simulation in Figure 4.5, it can be deduced that there is a variation of the voltage, as it was expected. But in order to distinguish the short circuit, it is necessary to identify the variation as a function of the drain current. Hence, it is necessary to determine if the short circuit is recognisable. The circuit in figure 4.4 simulates the possibility to recognize the amount of current flowing in the drain by looking at the gate voltage.

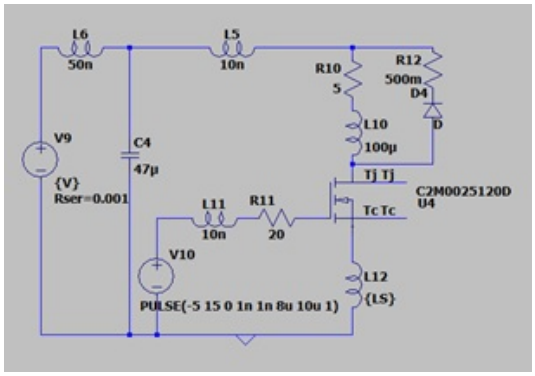

Figure 4.4: Circuit used for simulation

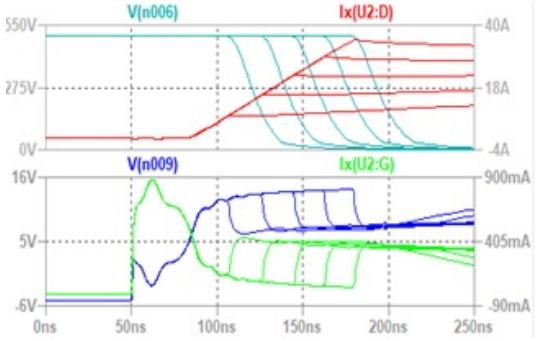

Figure 4.5: Simulation showing the correlation

The simulation was performed by parameterising the Drain current between 10A and 50A. With reference to the graph above, it can be noticed that during the first period of the transient, the voltage does not endure significant differences. Nevertheless, it is possible to notice a delay in the decrease of the Drain Voltage. It is due to the different value of the load current, which is gradually larger and therefore takes longer to turn off the Free Wheeling Diode. Interestingly, this phenomenon can be useful when considering the value of the load current during ignition. In fact, by measuring how long it takes for the value of the Drain voltage to drop, the intensity of the drain current can be estimated. However, in case of a short circuit during the conduction of the Device, it is not suitable to monitor the drop of the gate voltage, as it would not detect the short circuit. In fact, the negative drops of the Gate voltage are caused by the high dV/dt of the Drain voltage. In conclusion, following

this experiment, it can be stated that it is impossible to detect a short circuit only by monitoring the parasitic inductance, without resorting to the Kelvin Source. Because there is a relation between them, but it is too small and it almost impossible to recognize, considering also the possible noise.

4.1.2 Injection Method

Given the unsuccessful attempt to detect short circuits only by monitoring the parasitic inductance, an alternative method to detect short circuits has been devised: impedance measurement. The experiment required the injection of a high frequency signal on the Drain just before the turning on the device and the measurement of the impedance. Hence, it is useful to avoid Turn on in case of detection of the short circuit before the switching. In the case of correct behaviour, the same principle could also be applied during the conduction state. To evaluate the load in online mode, or the value of the Drain to Source capacitance. In order to quickly evaluate of the impedance and to reduce the load disturbance, it was decided to use a high frequency and small amplitude signal component. Thus, in this case a linearization of the problem could also be applied, to analyse more easily the results. Hence, small signal model was used to perform this experiment. During the initial analysis, the possibility for the experiment to work seemed feasible. Therefore, the next step was to perform simulations on LTSpice. Figure 4.6 shows the schematic that was used to perform these simulations.

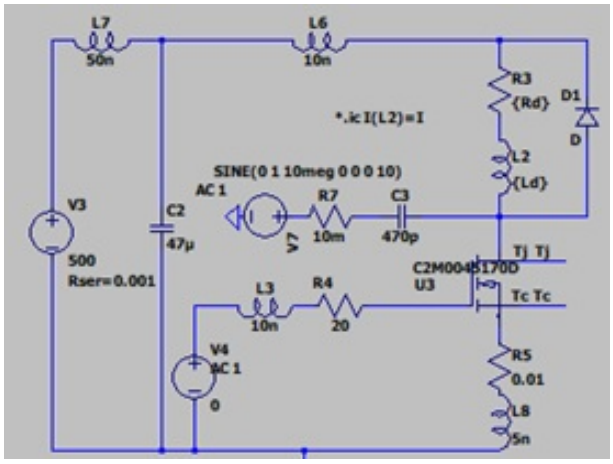

Figure 4.6: Simulation Circuit for Injection Method

The capacitor C_3 works as an insulator and therefore it must be able to carry high voltage. Moreover, it can be big otherwise the efficiency of the system decrease. In all simulations the circuit will always be compared the circuit with short circuit and those with the standard load. For this experiment, the load parameters were set to $100\mu H$ and 5Ω. Figure 4.7 shows the simulation of a simple low side switch with the load on the drain. Within this simple circuit configuration, the injection method responded positively, as it was foreseen.

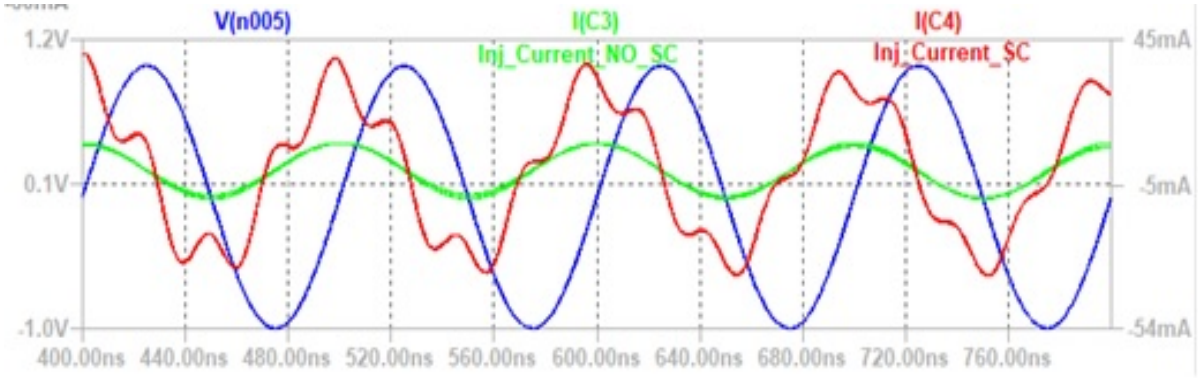

Figure 4.7: Simulation Result Injection method varying Load

The waveform shows that in case of a short circuit, the injected current is significantly higher than the case with nominal load. In fact, the impedance of the short circuit is lower than compared to C_{ds}. It is important to notice that in case of short circuit, the injected Current would go into the load shorted, while in case of a normal load it would go to the C_{ds}. In fact, in normal conditions the impedance of the load is very high at that frequency. The outcome of this part of the experiment was positive. Following this result, a parameterization of the rated current will be performed to ensure that the method works even with different loads. In Figure 4.8 the results of this second part of the experiment are shown. Load inductance was parameterised between $10\mu H$ and $1mH$, and the load resistance between 1Ω and 20Ω.

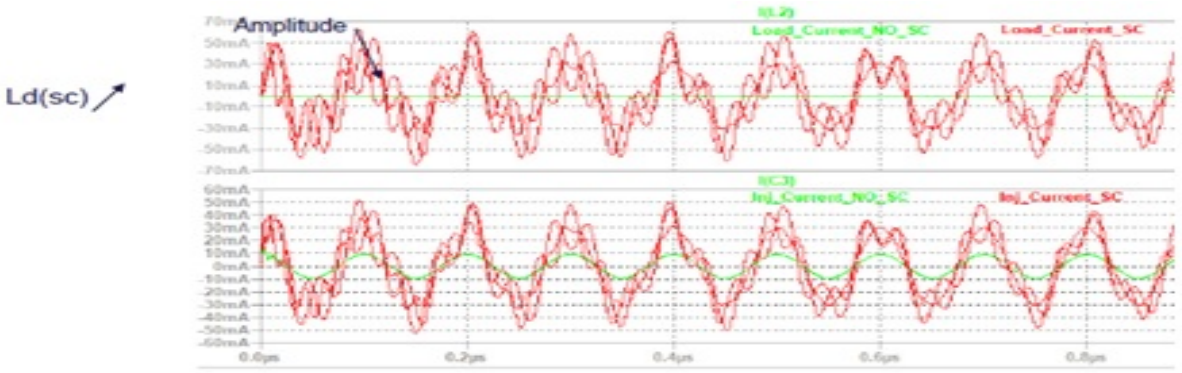

Figure 4.8: Short Circuit Load Sweep Simulation

As it can be deduced looking Fig 4.8, with different values for the parasitic short circuit inductance, the shape of the oscillation changes. But more important is to see the oscillation slightly reduces its amplitude due to the increase of the impedance at the frequency signal. Hence, in case the inductance of a parasitic short circuit is too high, the signal becomes comparable with the nominal condition. However, in the simulation the minimum impedance reached as a minimum 10µH, but even with this inductance the signal was still recognisable. Furthermore, in this first simulation an ideal diode was used, but the reaction of the injection method to a real diode has also been simulated. The positive outcome of the experiment seemed feasible also when introducing this variable. Subsequently, more complex configurations were simulated, in order to verify if the method would equally be successful even when introduced in some of the most common implementation. For example, a Leg and an Inverter were introduced in the circuit figure 4.9 represents a Full Bridge.

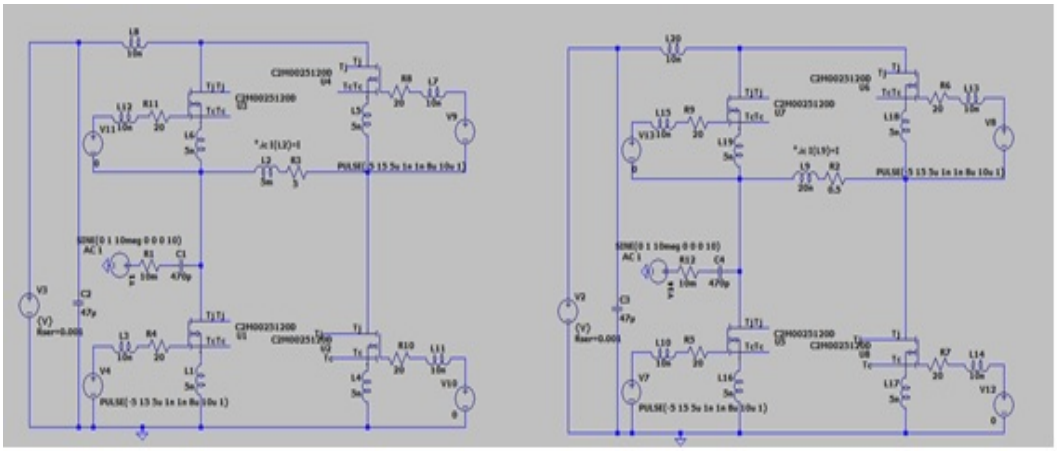

Figure 4.9: Comparison between short circuit and normal operation

In the circuit shown above, the high frequency analysis signal is injected during the dead time between the turning on of various switches. The result of this simulation is shown in Fig 4.10.

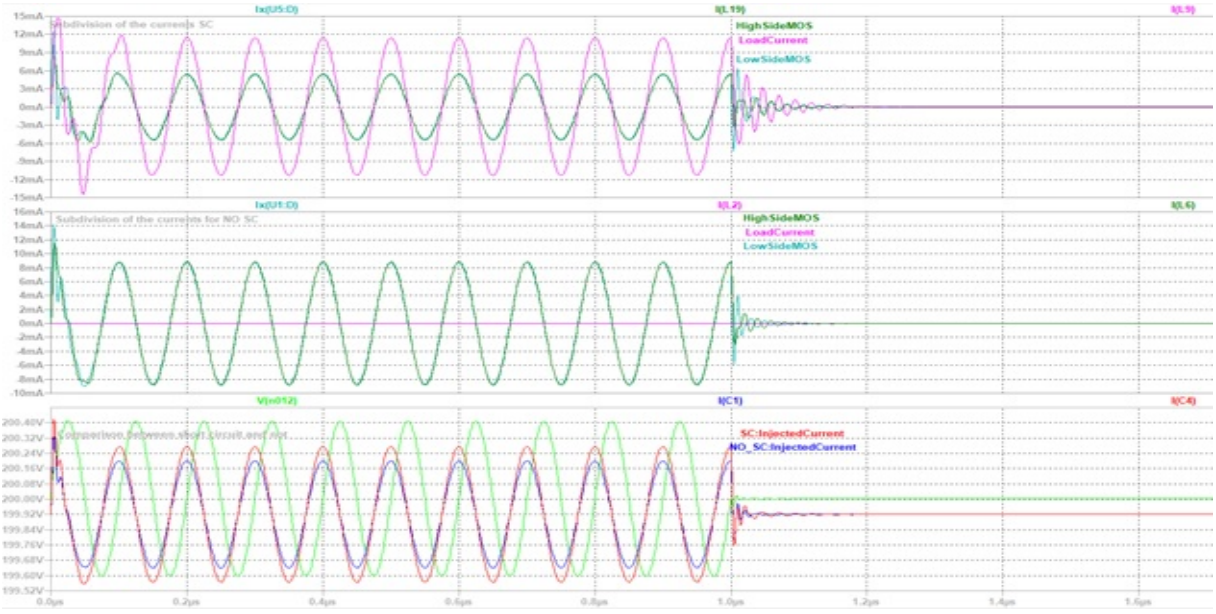

Figure 4.10: Result analysis in Full Bridge circuit

The simulation shows that there is not a substantial difference between the event of a Short circuit and in case of its absence. A very (strong) short circuit has been caused for this experiment. The graph shows in the first row how the current splits among the three main branches due to the Free Wheeling diode on forced by the

re-circulation current. It is also important to notice that in both cases (short circuit and not) the current flows greatly both in the high side and low side of the Leg. Only in case of a Short circuit there is a contribution of current into Load. Because for high frequency signal, the impedance of the load is very big. Hence, there is not a significant amount of current in it.
Other simulations clarify that instead to try to analyse the impedance of the load it was better to analyse the Impedance of the Drain to Source capacitance because it changes in according with the Drain to Source Voltage. This simulation focuses only in one Leg are done to better understand the phenomena. In figure 4.11 there is a simplification of the system. And it is explain also what was expected and why it was not verified.

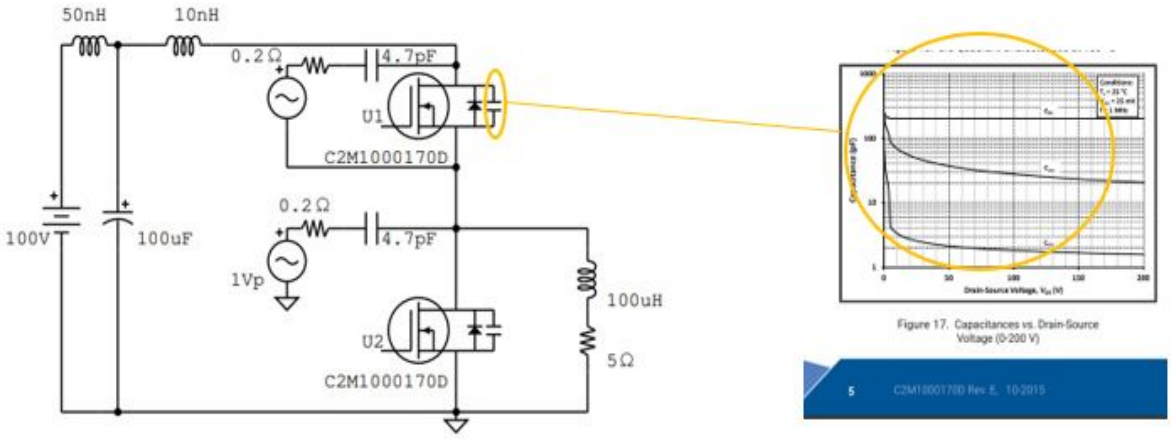

Figure 4.11: Simplification circuit with dependency of C_{ds} on V_{ds}

In LEG case, when the signal is injected, during the death time, there is different value of the C_{ds} capacitance according to the Voltage across it. In normal cases, if there is no SC:

- **Phase 1**: *HighSwitch* ON. (C_{ds1}= HighValue & C_{ds2}=LowValue)
- **Dead time**:*HighSwitch* after it is turned OFF, while *LowSwitch* ON. the signal is now injected. (C_{ds1}=LowValue & C_{ds2}= HighValue)
- **Phase 2**: After dead time, *LowSwitch* ON. (C_{ds1} =LowValue & C_{ds2}= HighValue)

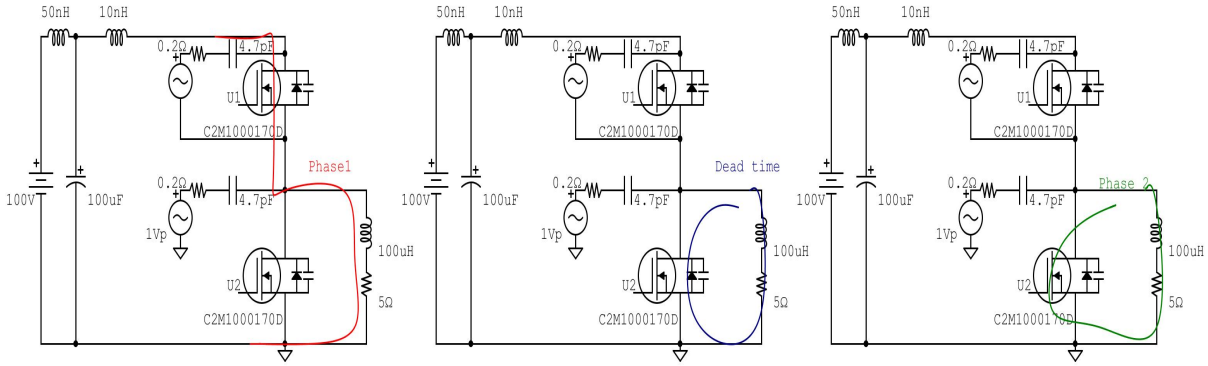

Figure 4.12: Paths Current without Short Circuit

Instead in case there is a HSF SC:

- **Phase 1**: *HighSwitch* ON. (C_{ds1}= HighValue & C_{ds2}=LowValue)
- **Dead time**:*HighSwitch* still ON, *LowDiode* OFF. The signal is now injected. (C_{ds1}=HighValue & C_{ds2}= LowValue)
- **Phase 2**: After dead time, *LowSwitch* ON with *HighSwitch* ON. (C_{ds1} =HighValue & C_{ds2}= HighValue)

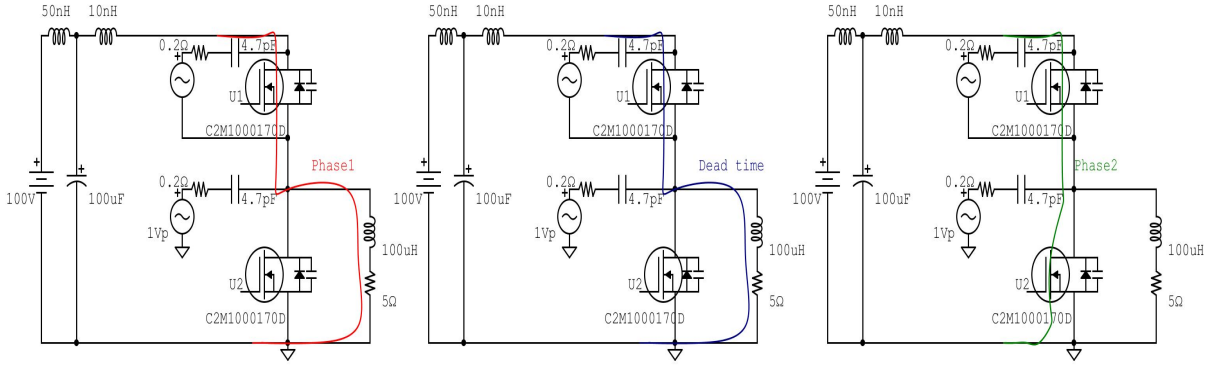

Figure 4.13: Paths Current in Short Circuit

The experiment aimed to investigate the variation of the capacitance between the Drain and the Source of the device. In case of a Short circuit, since both the Drain and the Source were turned ON, a different outcome was expected. In fact, when the Device is in ON condition, the Capacitance should be higher. By analyzing the model, it can be seen that the dependence on capacity linked to V_{ds} has not been

taken into consideration. Furthermore, before repeating the experiment, also the capacitance of the Body Diode has been fixed, as shown in Figure 4.14.

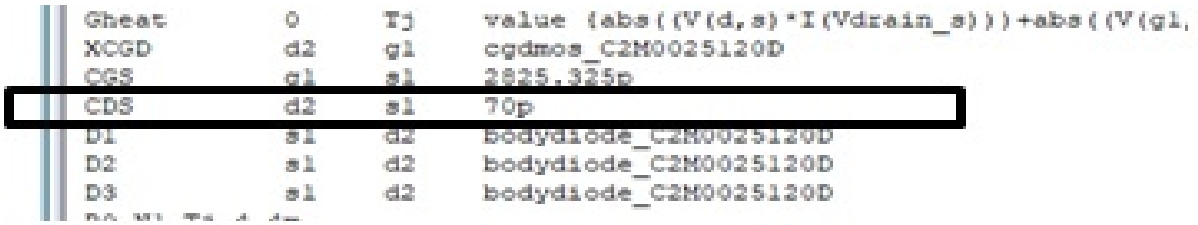

Figure 4.14: Dependency of C_{ds} in the Model of the DUT

Following these adjustments, the simulations were repeated with a model that also took into account the variation of the drain source capacitance. But even in that case, the predominant contribution of the value of the injected current was not caused by the impedance of the Drain Source's capacitance. Instead, it was caused by the value of the DC-Link capacitance and the body diode, keeping on from the load current. This path is visible in figure 4.15. Only forcing ah high value of series parasitic inductance the current goes in the D_{DS}. Probably inside the device model there is a series inductance compared to the value used between the DC-link and the leg.

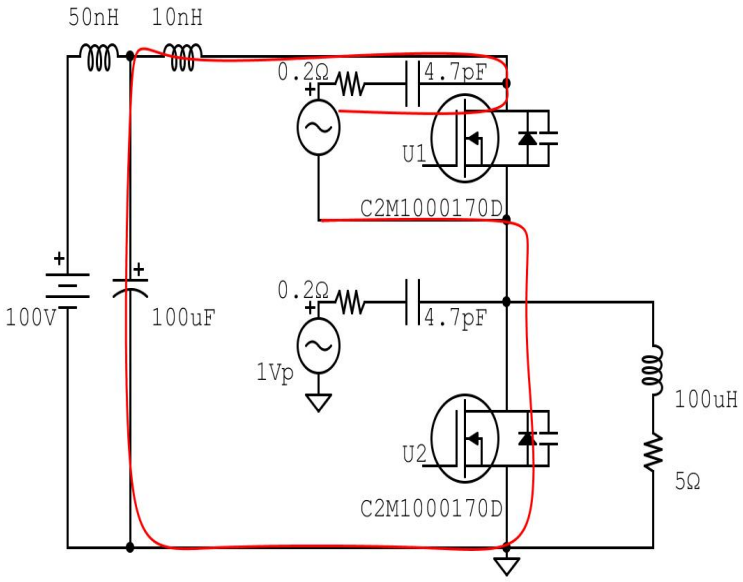

Figure 4.15: Injected current path

In conclusion, it is possible to state that it is not feasible to detect short circuits

with the Injection Method, due to the forced re-circulation of the load current (which turns on the Body Diode) and due to the low impedance of the Dc-link capacitance. In this case it would expect the current to go into the capacitor. Since in the simulation was considered all the parasitic impedance passing through the DC-link. Possibly within the CREE model there is some limitation or restriction. Nevertheless, the voltage range involved to be processed would be too small. Especially adding the noise, it would be very complicated to implement.

4.2 Fault detection method accepted

The first two methods analyzed have limitations. For different reasons, they did not have much possibility to work. For this reason the third method, it was decided to carry out is in a different section.

4.2.1 Derivative Drain voltage (RC method)

During the simulations performed on the previous circuits, it is possible to notice that the capacitor used to injected the signal was affected by the variations of the drain voltage. Therefore, is reacts to voltage variations by imposing a current that is proportional to the derivative of the variation, following the well known equation represented below, with reference 4.2.

$$i(t) = C\frac{dv_c(t)}{dt} \tag{4.2}$$

Starting from the reaction of the capacitors, the first idea was to only see the peak of the current to understand if there has been a voltage variation due to normal operation or due to short circuit. As previously analysed, in case of HFS, the variation of drain voltage is very small and consequently. The amount of current that passes into the capacitor is really small as well. However, this rather simple solution is not feasible: in fact, following this method it is impossible to detect the FUL scenario (Fig. 4.16). The difference is that on the left side in the Figure 4.16 the MOSFET is kept on, while the right side it becomes off.

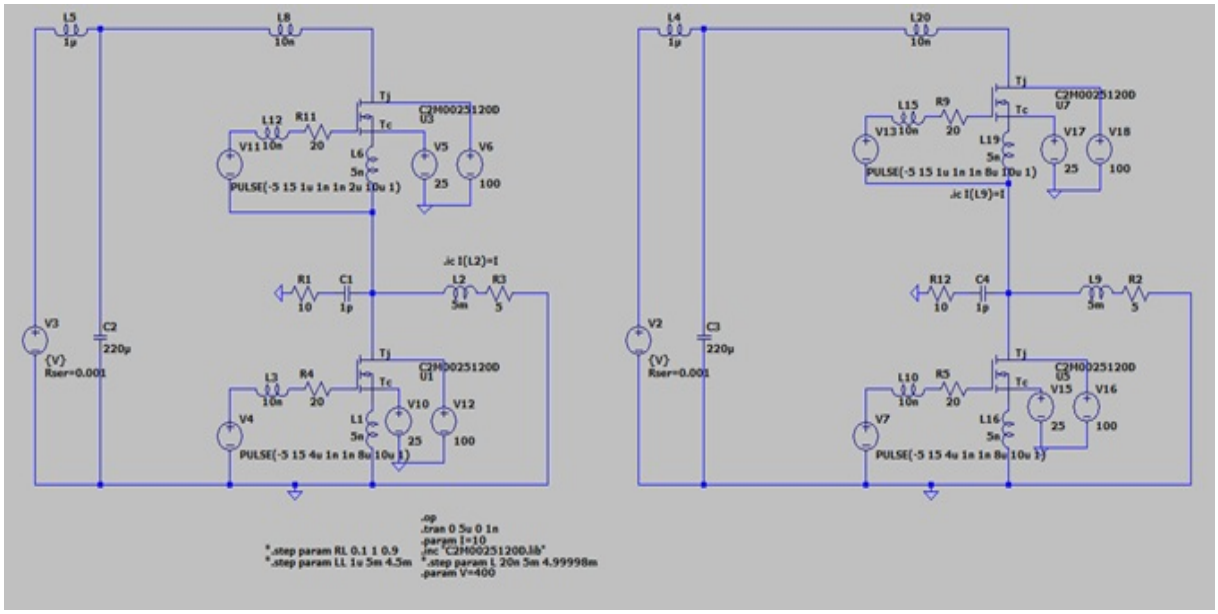

Figure 4.16: Comparison between short circuit and not (right up switch kept on)

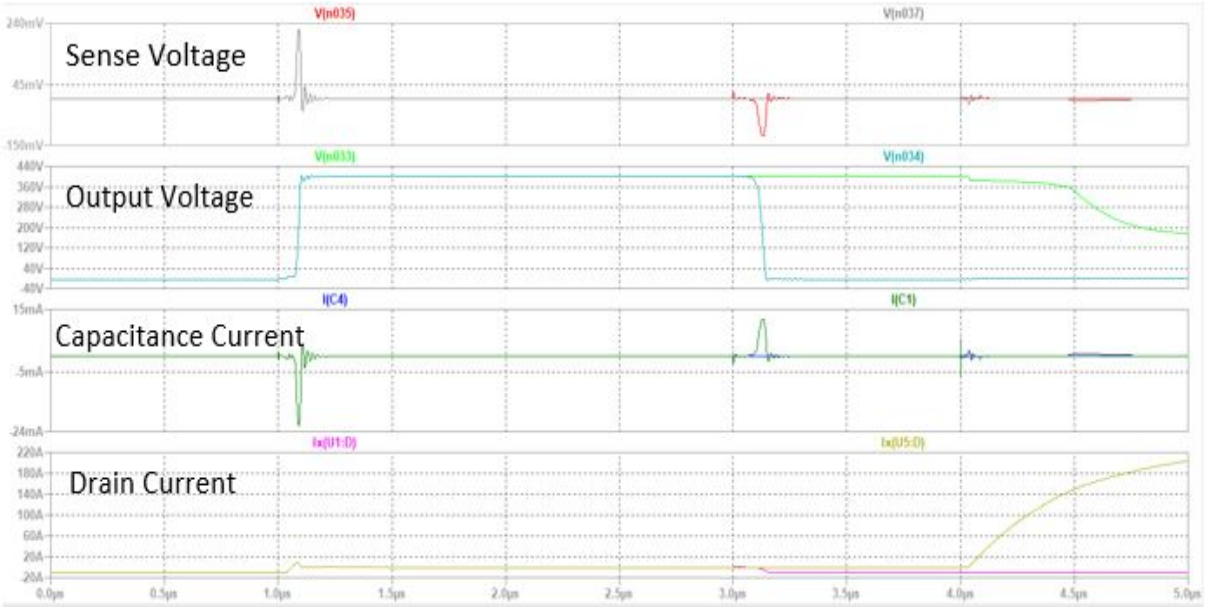

Figure 4.17: Relevant waveform of simulated circuit.

The Figure 4.17 shows different waveforms, the Output Voltage is the voltage in the middle to two devices. In fact, when the upper switch is on, the output voltage goes to DC voltage. Instead, when the upper device is switched off the output voltage becomes clamped (to GND) by the Body Diode of the down MOSFET. The variation (or not) of the Drain voltage is recorded thanks to the sense capacitor on the Drain.

As it can be noticed in Figure 4.17, when there is a variation of the Output voltage, the capacitor causes a current following Eq. 4.2. Indeed, during the first transition both output voltages (Left and Right circuit) go to DC voltage. While for the second transition (where only the left circuit is switched off) only the sense capacitor on the left circuit induces a current. So, looking at to the current of the sense capacitor it is possible to understand if the Output voltage changed. Therefore, it is possible to understand if the MOSFET has turned off or not. This is the principle of the method. Initially, only the presence of the current induced by the sense capacitor was considered and measured as a mean to verify whether the output voltage changed. However, by following this method it was difficult to distinguish FUL. Hence it was decided to rebuild the drain voltage for more flexibility. This method has several potential, in fact, different types of short circuit can be identified. It is possible to know if the up MOSFET has actually turned off before it even turned on the MOSFET below. In this case is it possible to avoid the short circuit condition before the turn on of the down Switch. Instead to switch on and then realize that there is a short circuit. But it is difficult to create an algorithm hardware with this type of logic. Therefore, for the thesis was realized a method that look only device for device, it analyses when the single device turns on or it is on. Given this negative limitation of the experiment, the next step that was taken was to try to include more short circuit cases. By reconstructing the drain voltage using an integrator. Following the principle shows in the Eq. 4.2. and Fig. 4.18 in theory also a RC network could have been used, but in this case, it had to be discarded in order to avoid the loss of efficiency in the circuit. Indeed, the current that the sense capacitor absorbs must be small. Furthermore, the sense capacity must also be small in order not to lose switching speed. In fact, in all simulations a capacity 10% of the minimum C_d has always been considered, allowing a small induction of current in the sense capacitor. In addition, the voltage induced in the shunt resistance is also small, for this reason it is necessary to insert an integrator with a gain. The advantage of using this method is that it is possible to obtain an estimate of the Drain voltage. It is impossible to measure it with normal methods, since the Drain voltage can measure thousands of Volts. The loss of efficiency due to the additional sense capacity was also simulated. When choosing a sense capacity lower than C_{ds}, the loss of effi-

ciency is negligible, as it can be seen in figure 4.17. The graphical representation of a circuit here below can be used to compare the losses between the circuit with the sense capacitor and without it. Figure 4.19 shows the two circuits compared. The demonstration was done considering a small voltage across R_s, in order to neglect its voltage.

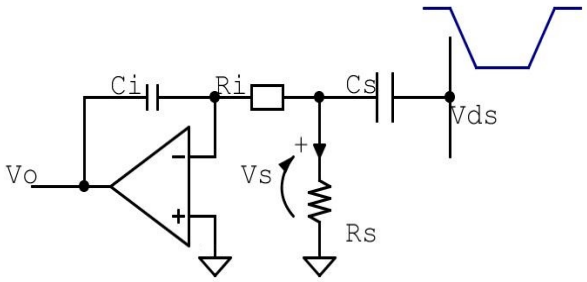

Figure 4.18: Sensing Drain Voltage Circuit

$$V_c \simeq V_{ds} \tag{4.3}$$

$$i_{Cs} = C_s \frac{dv_c}{dt} \simeq C_s \frac{dv_{DS}}{dt} \tag{4.4}$$

$$V_s = i_{Cs} \cdot R_s = C_s \frac{dv_{DS}}{dt} \cdot R_s \tag{4.5}$$

$$V_o = \frac{-1}{R_i C_i} \int V_s(t)dt = \frac{-1}{R_i C_i} \int C_s \frac{dV_{ds}(t)}{dt} R_s dt = \frac{-C_s R_s}{C_i R_i} \int \frac{dV_{ds}(t)}{dt} dt \tag{4.6}$$

$$V_o = kV_{ds}, \qquad with \qquad k = \frac{-C_s R_s}{C_i R_i} \tag{4.7}$$

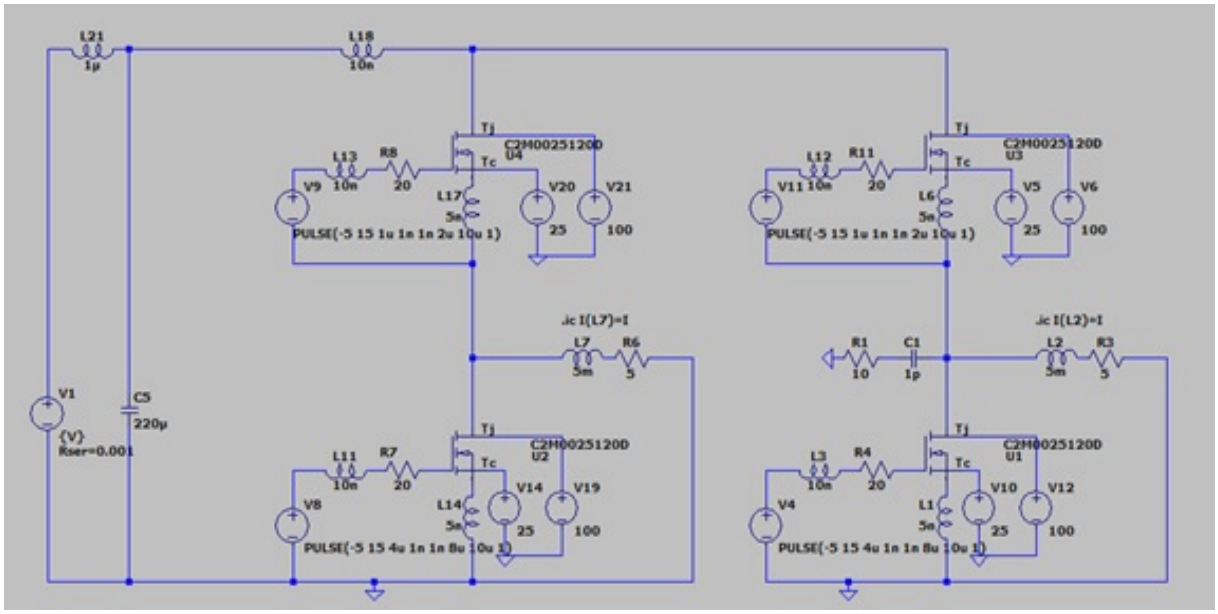

Figure 4.19: Comparison between circuit with sense capacitance and not to evaluate losses

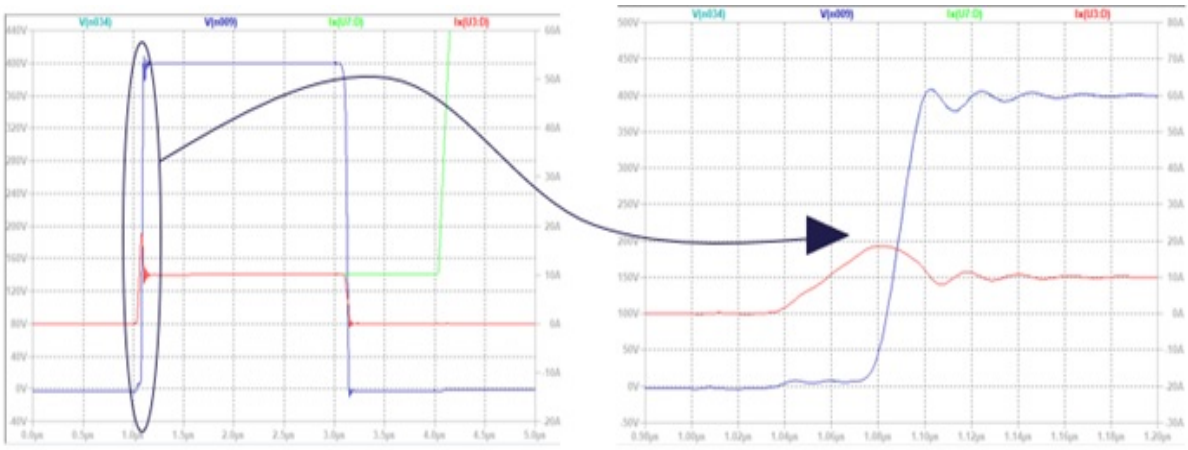

Figure 4.20: Compared waveform with and without sense capacitor

As it can be seen in the graph 4.20, the two waveforms representing the drain current and voltage of the two circuit. Namely, the circuit with the sense capacitance on the Drain and the other one without it. To show that there is not a considerable increase of the losses. The two waveforms are perfectly identical. To obtain this data, an automatic tool to analyse the losses implemented in LTSpice has been used. (Pressing Alt and Right Click) As it can be deduced, there is not a significant variation between them. Looking at the principle, it works properly in each situation.

Because it is as if I had the opportunity to know exactly Drain's voltage., Therefore, it was then possible to design a circuit that automatically detects short circuits and consequently turns off the MOSFET. A further action from the controller was not needed, hence the turn off time can be minimised. The circuit was designed to obtain a voltage that is in scale with the Drain voltage (Equation 4.7). Then, the obtained voltage has to be compared to threshold voltage, as for the Desat method. The current flowing through the sense capacitor is in the order of microamps to do not lose efficiency. Moreover, to have a small impedance and an accurate resistance, the shunt cannot be too high. The small resistance impedance is mandatory to have a small value across it, so to have Eq. 4.3 respected. For these two reasons, in the middle of the integrator and the shunt resistance was inserted an amplifier to obtain an output between 0-5V, with a Drain voltage range between 0 and 1000V. In figure 4.21 shows the circuit designed to obtain the reconstruction of the drain voltage with a simulation of the operation.

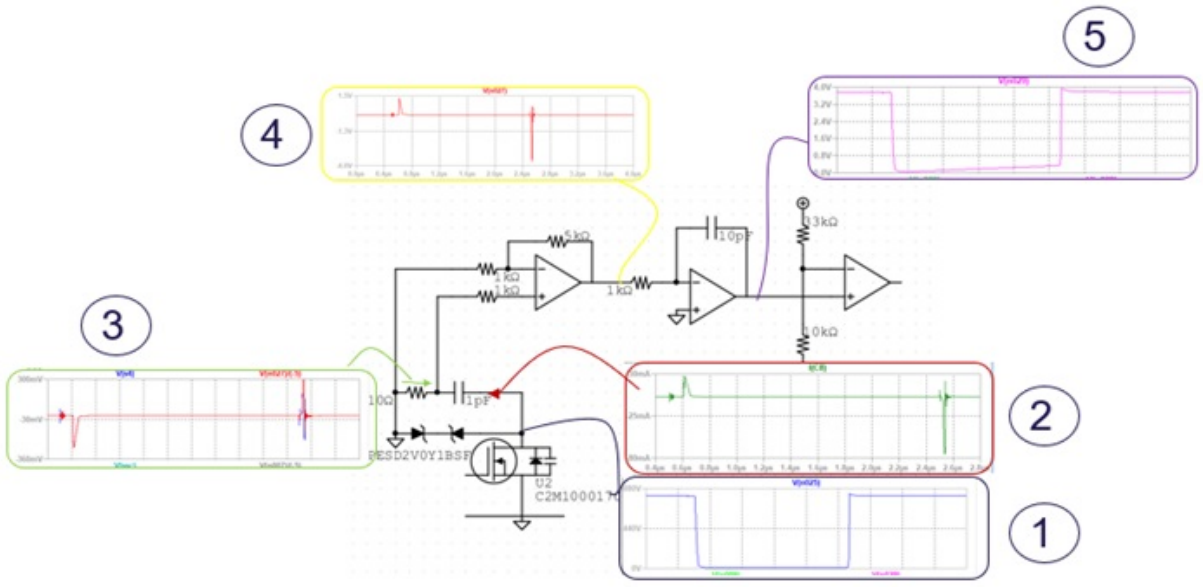

Figure 4.21: Working principle sensing voltage and comparator

1. The Variation of the Drain voltage induces a current in the RC node.
2. The current is measured using the resistance itself. (The exact value must be measured).
3. Voltage induced by the current measurement.

4. The voltage induced will be amplified -5 times. In this way the negative coefficient in Eq. 4.7 is compensated.

5. The amplified voltage is integrated to obtain an equivalent voltage to the original one. Finally, very similar replica of the original Drain voltage is obtained.

The Drain voltage is measured until the dead time. It is important to remember that the dead time can be reduced, as well as the threshold, in order to increase detection speed. In conclusion, the experiments prove that it is possible to use derivative drain voltage to detect short circuits, and that the method works well in different situations and with different variables A simulation circuit of the entire system is shown in Fig 4.22. The circuit is composed of three main parts. The first one reconstructs the drain voltage in a low voltage range. The second one compares the generated Drain voltage with a threshold. If the generated Drain Voltage is below the threshold, the compared output is 0V, otherwise it should be 5V. The third part of the circuit generates a delay of the DUT Gate signal. Only the rising edge is delayed. In fact, after the DUT Gate voltage becomes high the output of the retarder is 0V, while after the delay the output becomes 5V. In the end of the circuit, these two output are sent to an AND logic in case of a short circuit. In this first version the reset of the integrator is not present, in future version it will be present. The reset will be active whenever the DUT is off. Instead, in this first version the reset is forced by the offset. Therefore, if the Drain voltage does not fall below the threshold after the delay time, both outputs have to be at 5V. The output of the circuit increases and turns on a small MOSFET, which will turn off the DUT. A complete simulation of the circuit both in short and non-short circuit operations will also be reported. the simulation in normal condition, without a short circuit, is shown in Figure 4.23. On the other hand, the short circuit condition is reported in Figure 4.24

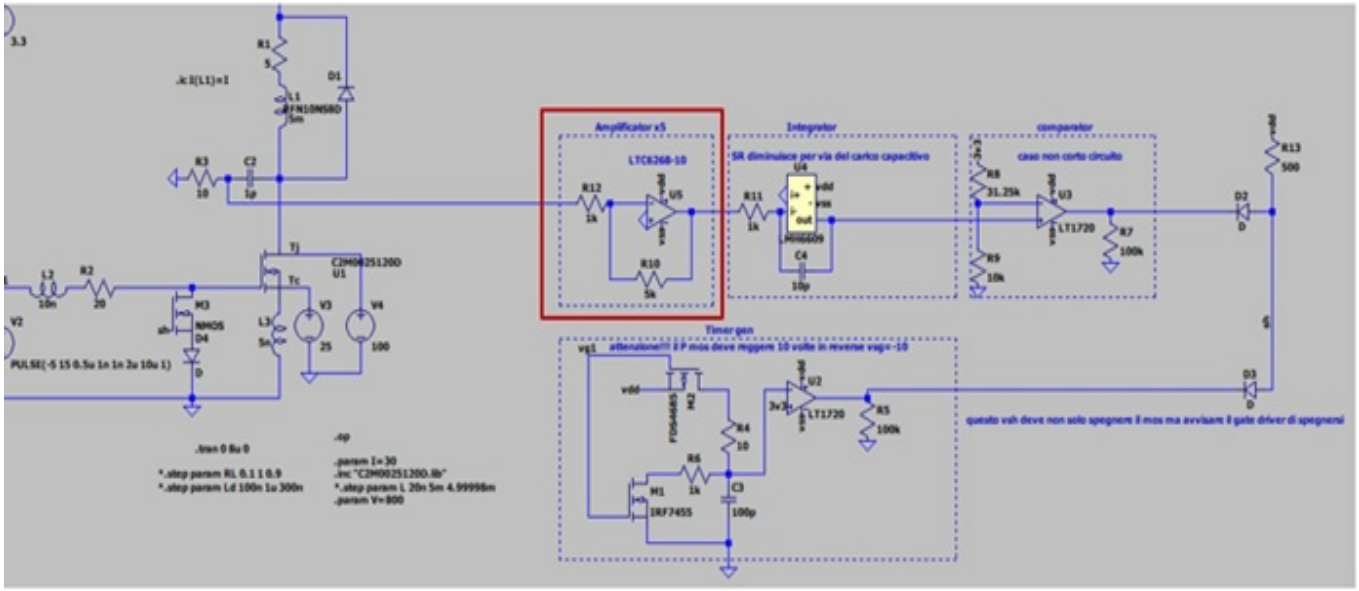

Figure 4.22: Circuit for simulating the entire Drain voltage acquisition

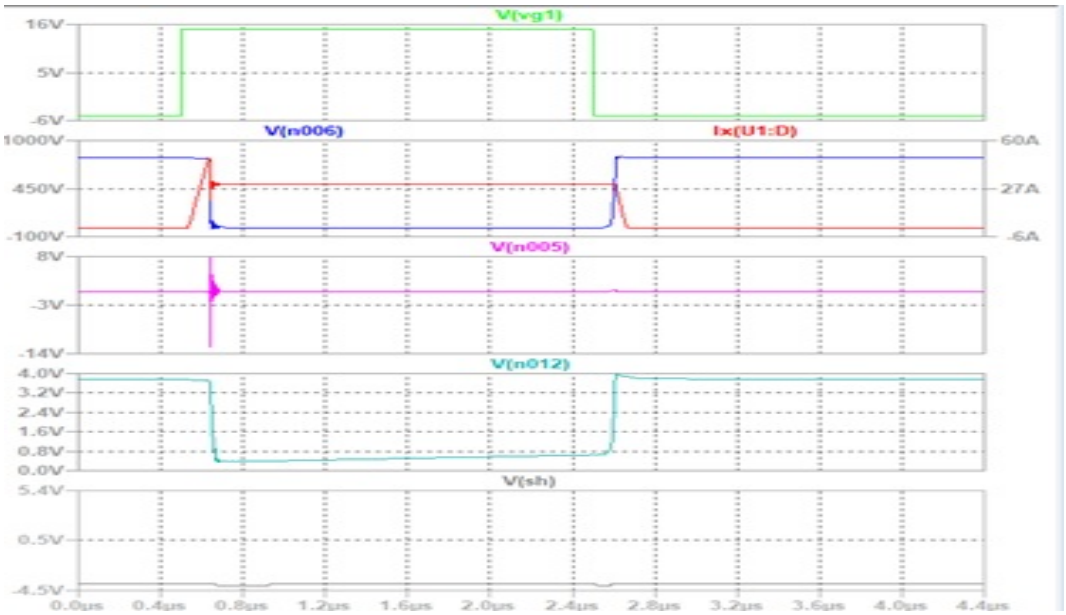

Figure 4.23: Output waveform of the complete simulation in standard condition

Legend Waveform:

Green: Gate Voltage

Blue: Drain Voltage

Red:Drain current

Violet: Current injected in RC

Litgh Blue: Integration voltage

Grey: Voltage output of RC method

The increase of the V_{sh} entails a short circuit. The RC method does not disturb normal operation without short circuit. In normal cases the V_{ds} drops below the threshold before the delay circuit becomes high. So, since there is no superposition of its high signals, the short circuit is not detected and V_{sh} remains low.

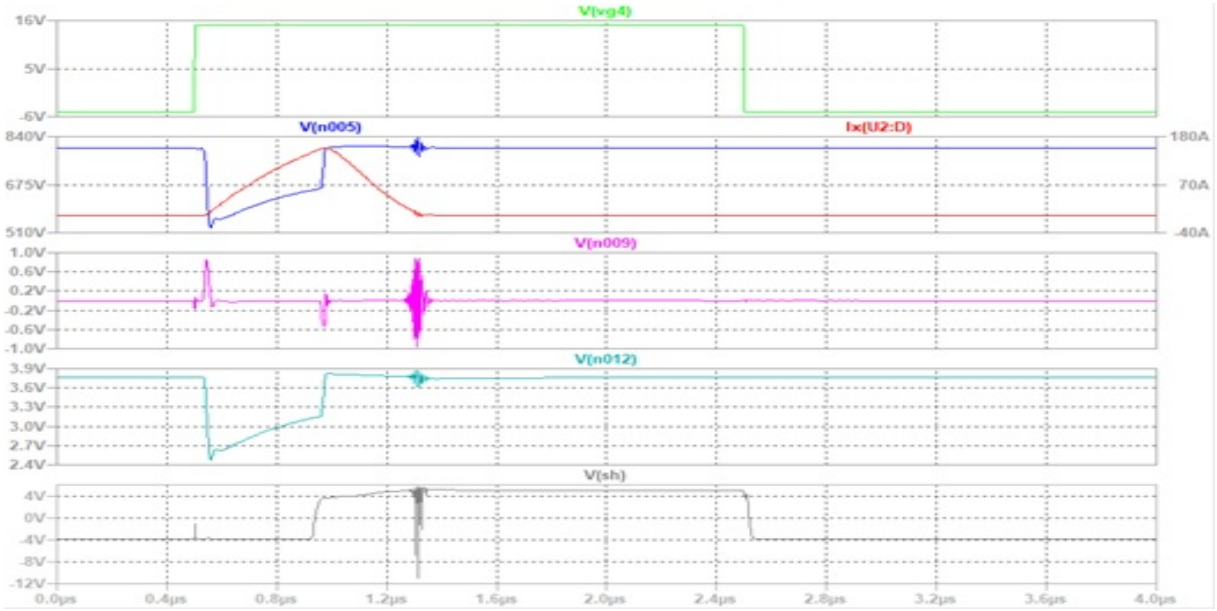

Figure 4.24: Output waveform of the complete simulation in Short circuit condition

Legend Waveform:

Green: Gate Voltage

Blue: Drain Voltage

Red:Drain current

Violet: Current injected in RC

Litgh Blue: Integration voltage

Grey: Voltage output of RC method

V_{sh} is the logic AND between the lowering of the Drain voltage below a specific threshold and the dead time needed for the Drain voltage to decrease. So when the $V_{shvalue}$ became high, a short circuit is detected and consequently the device will be switched off. The spike around 1.2us can be justified by the complexity of the circuit in LTSpice: in fact, a complex model was used for all components. To verify the working

principle of the circuit, it can be see that the V_{ds} voltage and the reconstructed Voltage are very similar. In this case the dead time is around 400ns. But it can still be lowered and this makes this method faster than the usual Desat or other methods. In case of short circuit conduction, V_{ds} never reaches the threshold, therefore the output voltage of the comparator remains high. When the delay circuit reaches the programmed dead time it also goes high and the output of the two signal becomes high (AND logic of the two signal). Therefore, the short circuit is detected. Subsequently V_{sh} goes to the small MOSFET which switches off the DUT directly.

CHAPTER 5

Design Board for verification Method

5.1 Verification of the method Implementation method

To verify the effective functioning of the RC method, it was decided to create a board. The board includes both the setup for the realisation of a double test pulse with HSF and FUL short circuit, but also the short circuit detection method with also a short circuit protection. The protection is driven by the Detection method. In this way the DUT will be automatically turned off . The design of the board will be disclosed in the following paragraphs. The test circuit is one leg, where the DUT is the low side switch, while the high side device is an IGBT that simulates a short circuit. The inspiration is taken from the literature. [14]

5.1.1 Double Pulse Test

The double pulse test is one the most use way to verify the proper operation. In my cases it was necessary to modify slightly, it was added a section to simulate the short circuit. This part is called Shorter, it is an high side IGBT that it shorts the load. The energy require for the test initially it is provided from the DC-licks. It was chosen to meet the charge requirements for the test and the RMS current they have to endure. To comply with the specifications, a 160A and a 100uF ($100A * 10\mu s = 1mC \rightarrow DC_{CAP} = \frac{1mC}{10V_{ripple}} = 100\mu F$) charge were required. Where 100A are the average current require Durant a typical Short Circuit test for a pulse of $10\mu s$. The product is the charge, to obtain the capacitance knowing the charge it was imposed a

ripple of 10V. The number of capacitors has subsequently been increased to increase the system reliability. To simulate the short circuit, it was decided to use some robust devices, such as IGBT, to ensure that the DUT limit conditions could be repeated several times. The choice fell on two in parallel IGBT, because of a reduced cost and because of an external free wheeling Diode. The load is a coil in air that has been found in the laboratory, with an inductance of $100\mu H$ and a resistance of 5ω. The load is represented in Figure 5.2 and its value 5.3. The double pulse Block are showed in figure 5.1

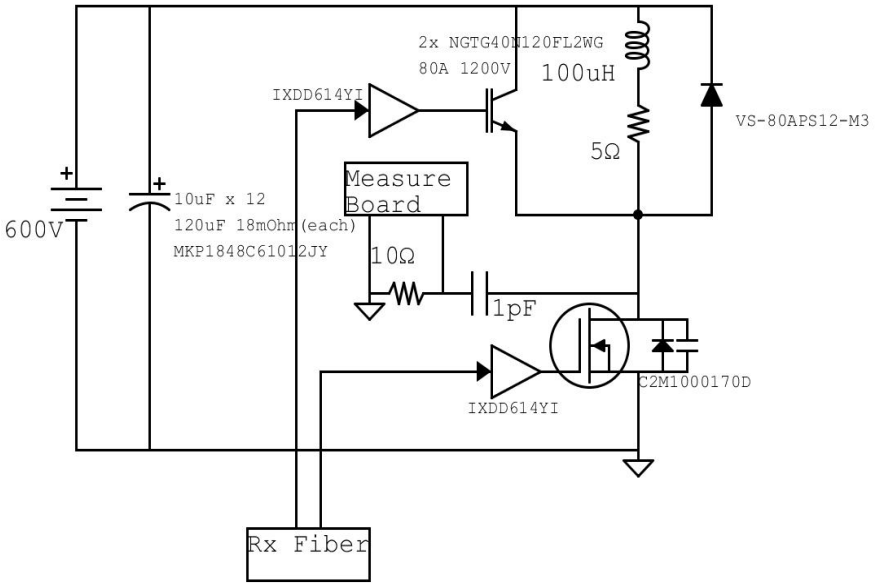

Figure 5.1: Double pulse setup board

Figure 5.2: Load

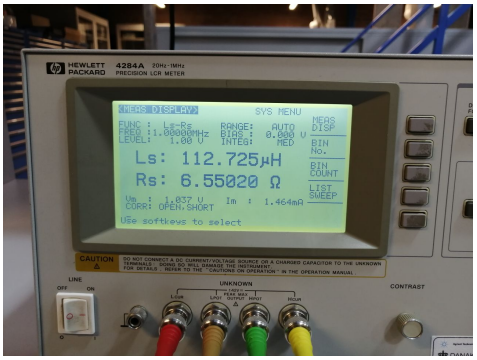

Figure 5.3: Value of Load

An IYXS Gate driver is used to drive the circuit. The IYXS Gate Driver IXDD614YI is not isolated with any security (such as Desat or Clamping voltage), since it does not intervene in case of short circuit. To control the signal, an FPGA has been programmed to send signals to the board through optical fibre cables. Two control signals are required: one for the DUT and another for the Shorter. The Shorter is an High Side, therefore its Gate Driver was not related to fixed voltage. Because Emitter voltage of the high side device (IGBT – Shorter) changes. To ensure the correct operation, the supply voltage of the HS GD has to be isolated. Indeed, one isolated DC/DC converter was used. Only some reference voltages are generated with an analog circuit inside the board. The IGBT are two ON Semiconductor NGTG40N120FL2WG (1200V 80A). Instead the Diode is a Vishay VS-80APS12-M3 (1200V 80A). The DC-Link Capacitors are twelve Vishay MKP1848C61012JP4 (10uF, 1200V, $9m\Omega$).

5.1.2 RC Method

An important section of the board has been reserved for the RC Method. In this part many components have been added to ease operations such as debugging or possible changes within the circuit configuration. The most critical part in designing this section has been the finding of an amplifier that could perfectly follow the signal the signal to be amplified, since the Drain voltage excursions are very fast and can cause a current in the fast sense capacitor.

Like the simulation shows, to reconstruct a Drain voltage very similar to the original an inverting amplifier was mandatory. To resize in proper way the range of the reconstructed voltage with the real Drain voltage (Fig. 5.4) , having the value of the RC sensor was 10Ω and 1pF the gain of the first amplifier was set 5. One of the drawbacks was that it requires a high bandwidth and slew-rate. It was chosen the OPA6268-10.

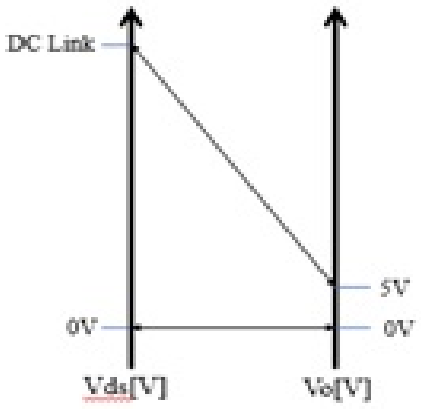

Figure 5.4: Range voltage

To be able to generate a waveform as correct as possible is a critical point, since every offset created by the circuit are adds into the previous ones thanks the integrator. For this reason, for long pulses there is the risk of corrupting the output due to the offsets. A schematic of this section of the board is represented in Figure 5.5. The section, due to the analog components, can be easily integrated inside a Silicon chip, maybe also in the same chip of the gate driver. Only the sense capacitor to connect on the Drain must be connected from outside.

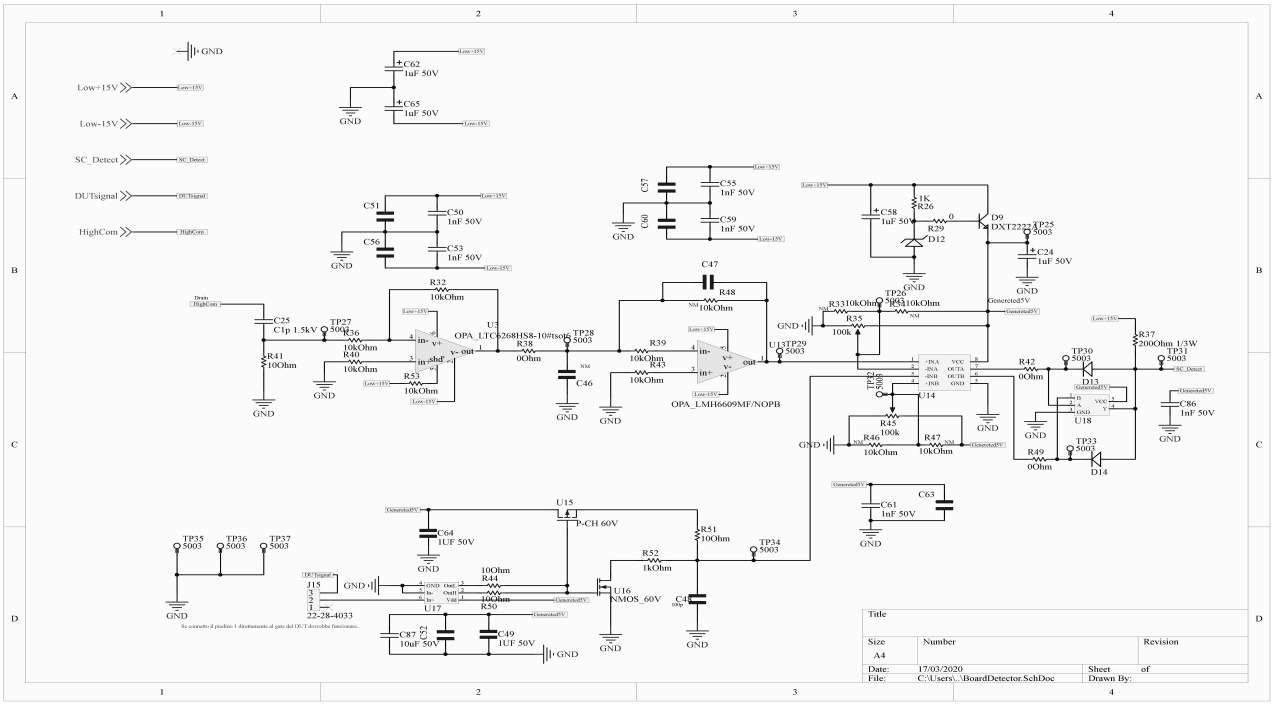

Figure 5.5: RC Circuit Method

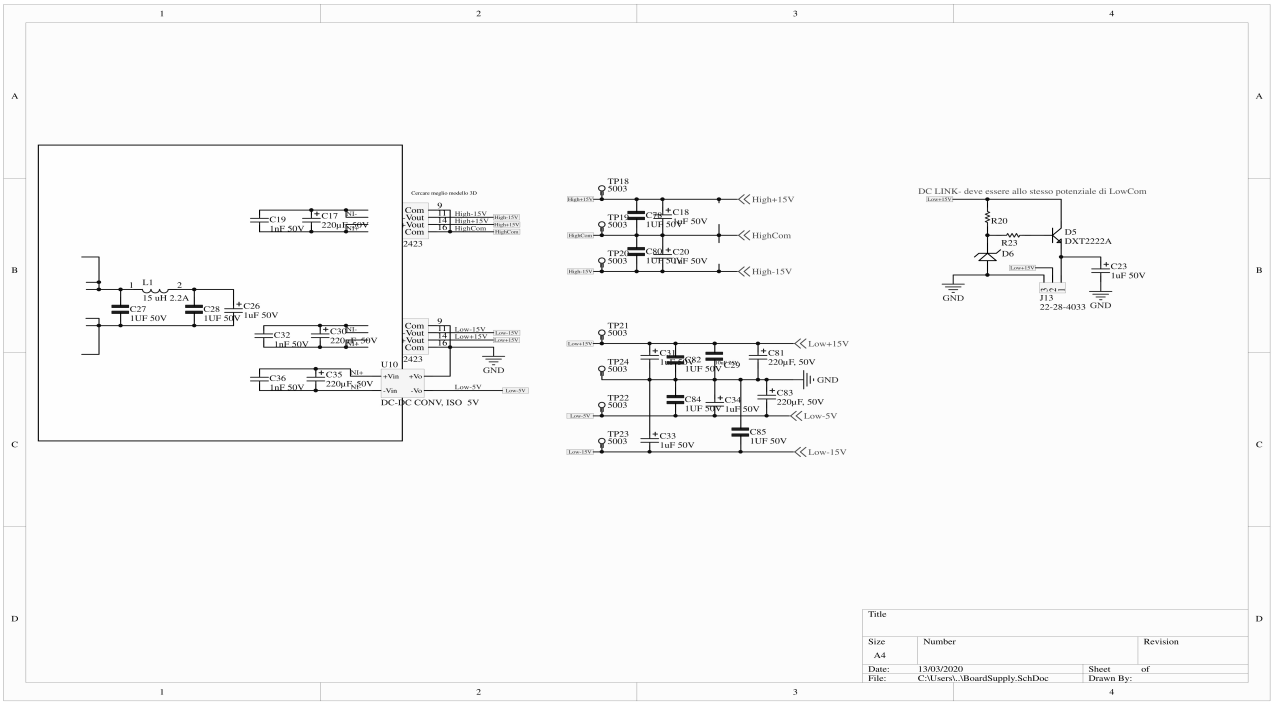

Figure 5.6: Supply Part of the Board

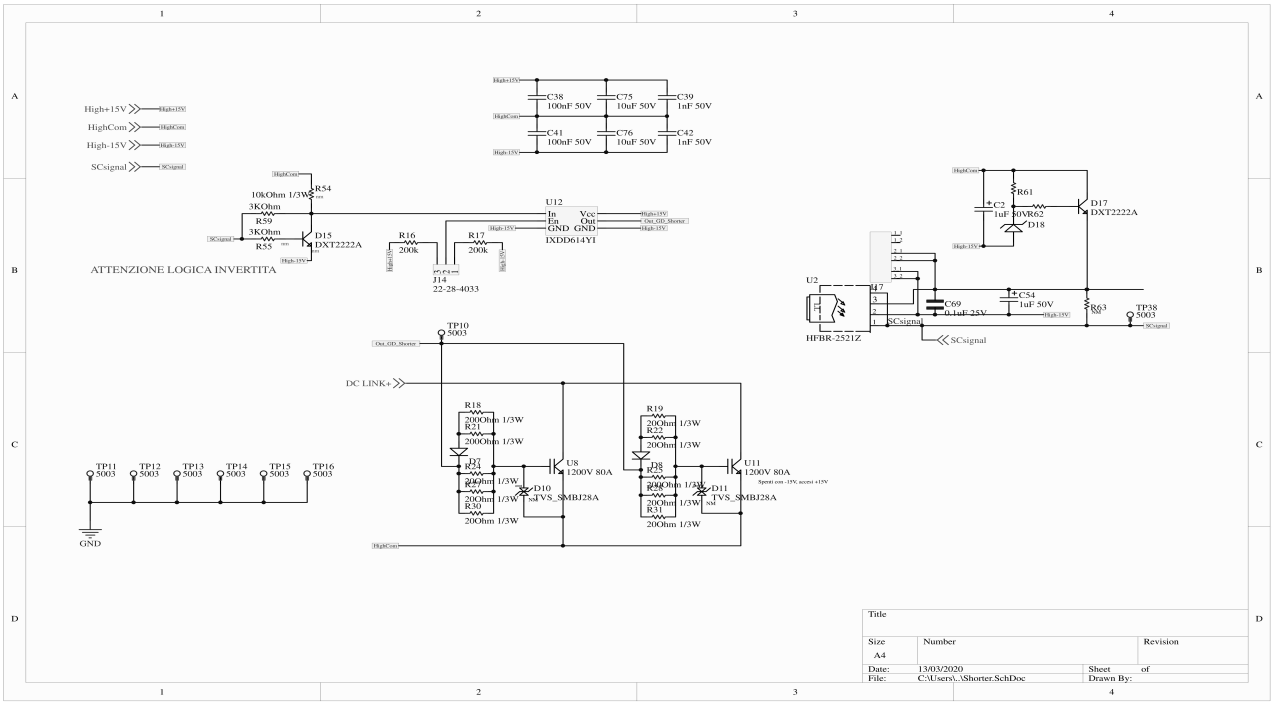

Figure 5.7: Shorter Part of the Board

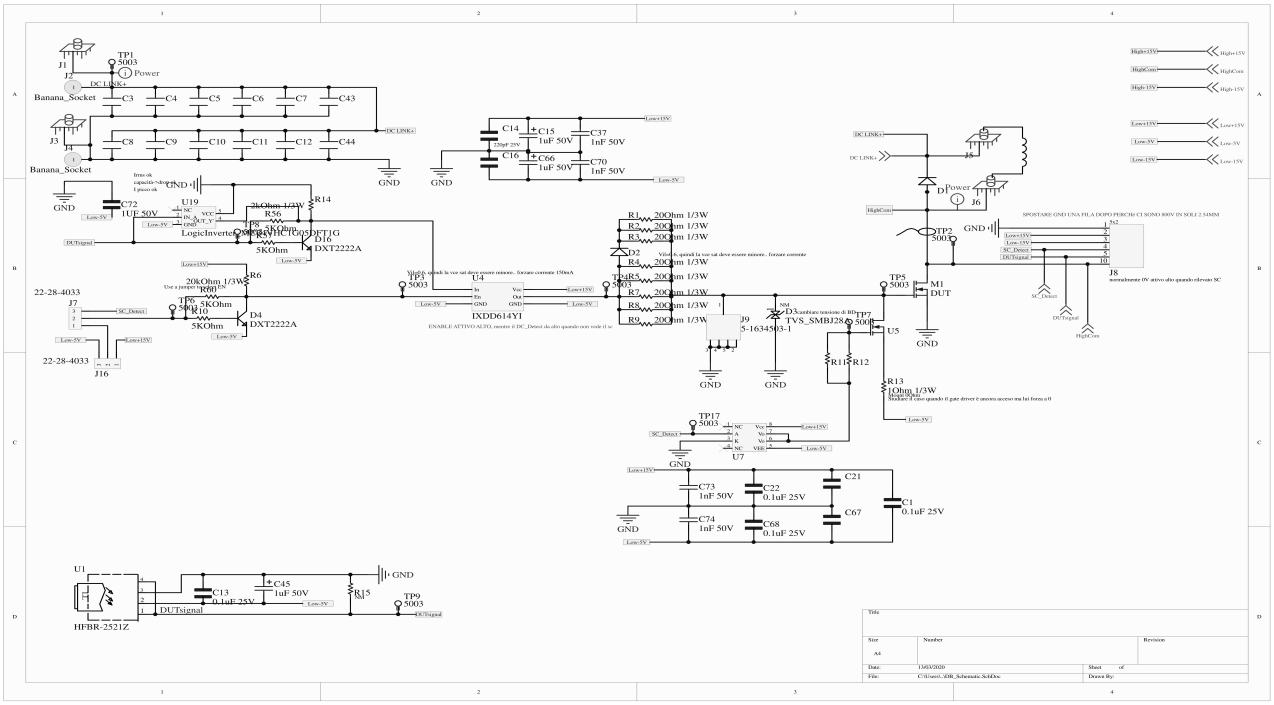

Figure 5.8: Double Pulse Setup Board

The various parts of the circuit have been divided into several sheets for better understanding.

5.2 Board

The design of the board has been implemented on Altium Designer. Below, the sheets of the Project and the Picture of the 3D model are included. To connect the Load some screw connector was inserted. The RC method can be incorporated with silicon within a single Gate Driver, except for the sense capacitor, whose dimensions are excessive. Unfortunately layout was not optimized, there are a lot of waste space. Because the time to complete was over.

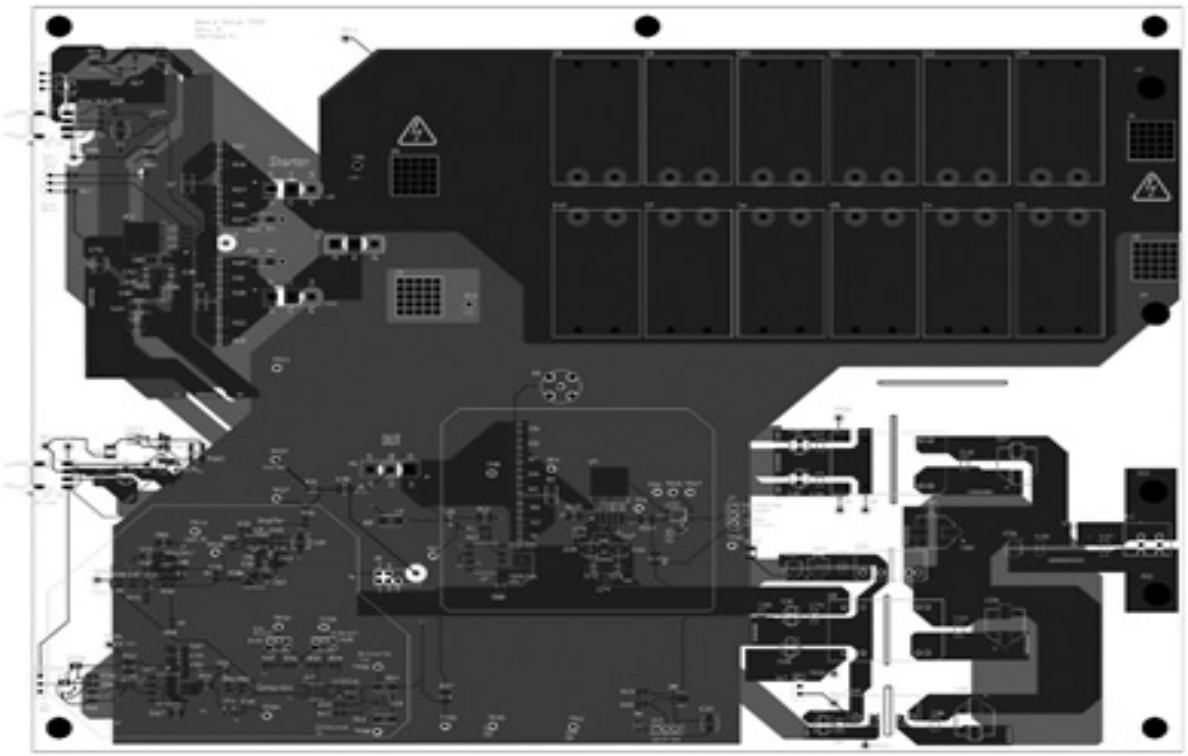

Figure 5.9: Board Layer

The Drill and Gerber was extracted ant the board was sent to print 19th December 2019. Unfortunately to get the circuit on time and have enough time to work on it. The order had to be sent before the finish of the period abroad. This time limitation made it impossible to optimize spaces and make the board smaller. However, having

simulated the whole circuit with the models of the individual devices, the system had a good probability to work properly.

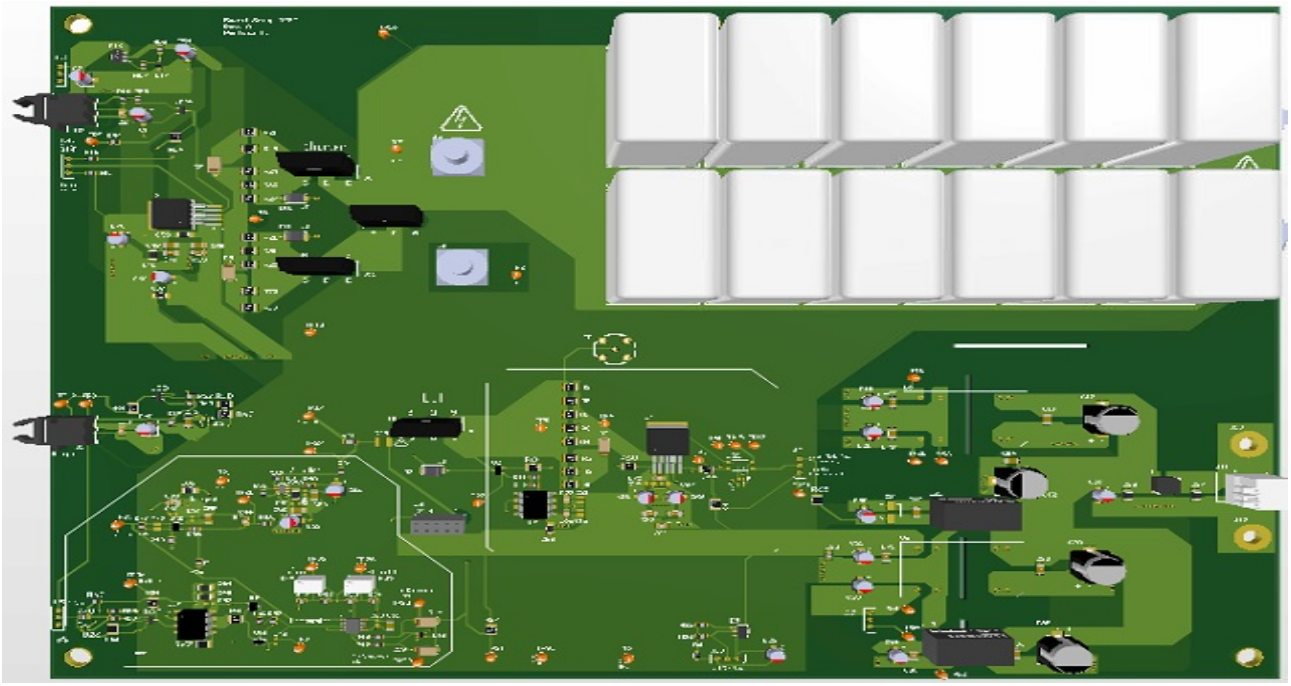

Figure 5.10: 3D Top view Board

Figure 5.11: 3D Front View Board

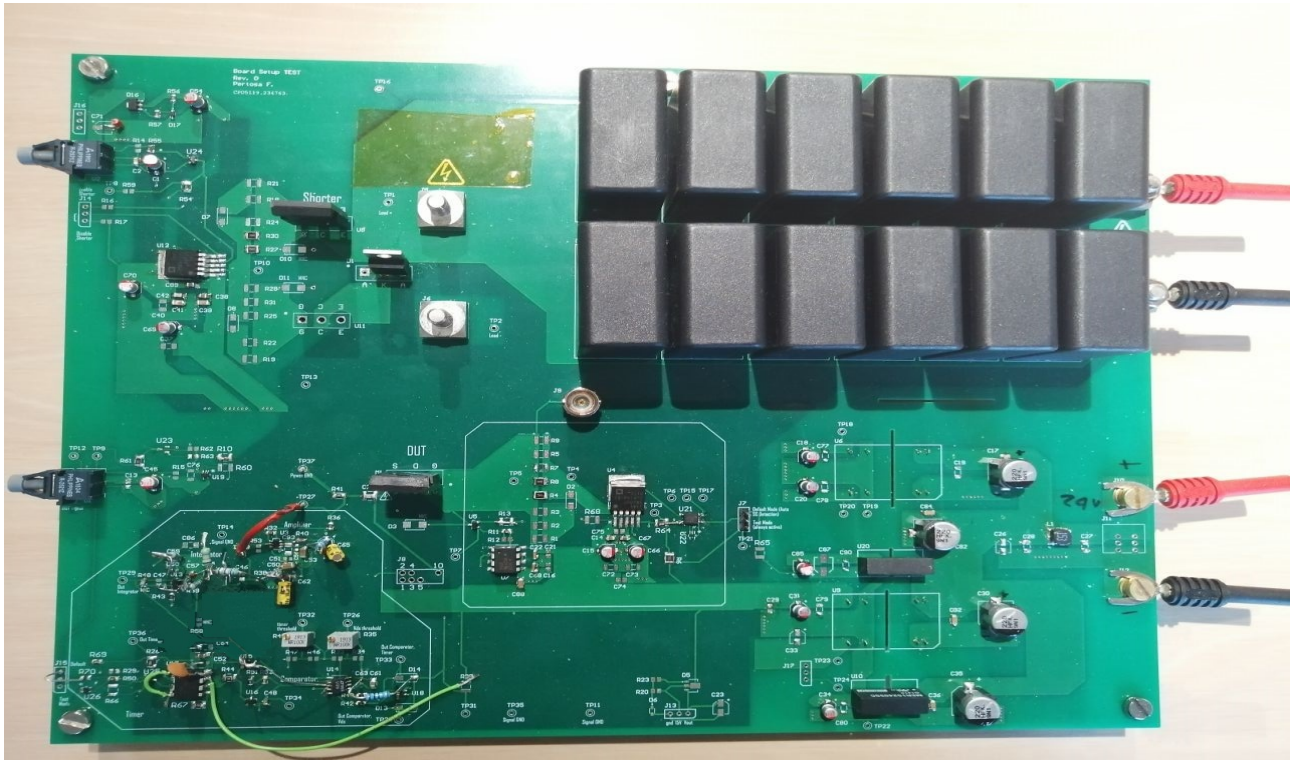

Figure 5.12: Picture board

CHAPTER 6

Verification Method

6.1 Debug Board

To verify the efficiency of the Method illustrated in the previous chapters, a Board has been designed. Such Board is inclusive of the Double Pulse test Setup and of the Short Circuit Method. Within this chapter, the waveform obtained from the experiment of the board will be illustrated. Moreover, some adjustments were made during the debugging phase: For instance, some improvement has made to allow a robuster operation or less losses. One of the most important improvement i,e. resetting the integrator when the DUT is off or eliminating the inverting operational amplifier.
To begin, the Double Pulse set-up was welded with the Shorter and tested. Two main tests were performed: a static one at high voltage and a dynamic one while running the Double Pulse, with and without the Shorter Enable (Short Circuit condition). To test the DC isolation, each DC-Capacitor was removed and substituted with a high value resistor. Then, a voltage of 600V was applied on the board. A tester was connected in series to the DC-Source to monitor the current leakages.

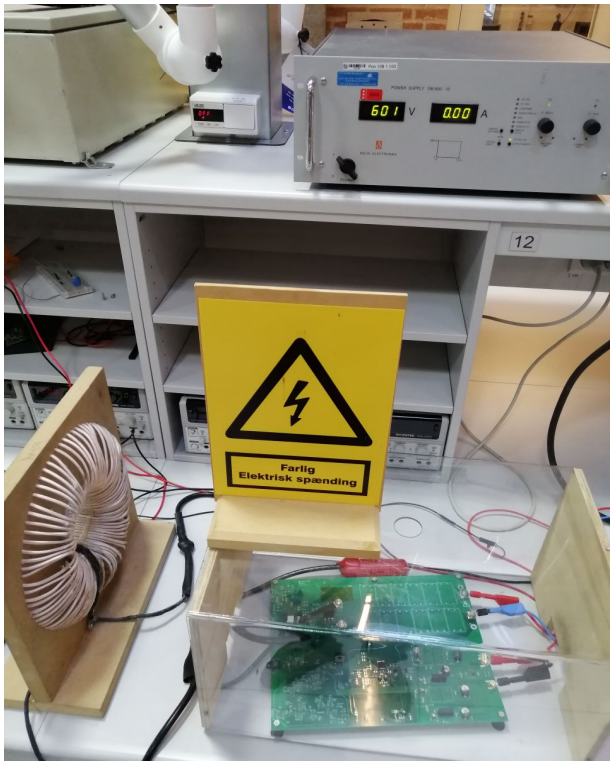

Figure 6.1: DC Isolation Test

Even though the current read from the DC-Source was 0A, the tester revealed a constant current, similar to the one flowing through the resistor in parallel to the Power-Supply.

Fig.6.2 and Fig.6.3 show the waveforms obtained while running the Double Pulse test in presence and in absence of a Short Circuit. Initially, the Free-wheeling Diode that was selected presented a an excessive reverse current after the second turn-on of the device. Therefore, it was changed with a SiC schottky diode (Model) to minimize the Q_{rr}.

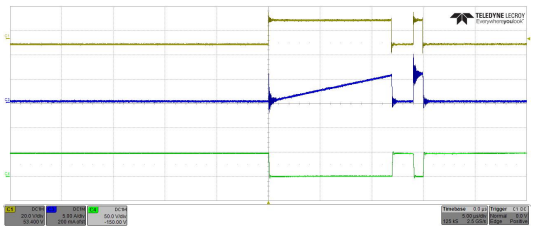

Figure 6.2: Double Pulse without S.C.

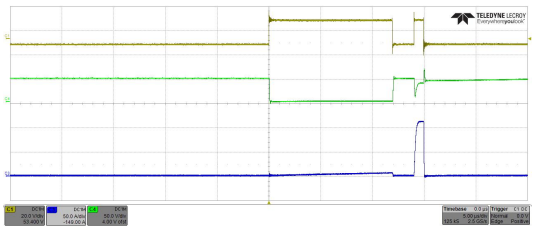

Figure 6.3: Double Pulse with S.C.

Nevertheless, as the Method needs to be effective in a realistic situation an Isolated

Gate Driver should be used to drive two MOSFET at the same time. This G.D. introduced a delay also in the negative edge. As if the blue waveform was delayed due to Gate Driver's delay itself.
Consequently, the AND logic (output of the method) of the comparative Integrator Output and the Timer circuit has a glitch (for a short period of time it goes high). The Glitch occurred after the DUT turned off, i.e. when the Drain voltage went above the threshold. Yet, the timer was not already low, due to the delay. The Glitch does not influence the normal operations of the circuit, because the wrong fault detection was detected once the device was already turned off. Nonetheless, to solve the problem of the Glitch, a non-isolated Gate Driver should be used, initially the solution was fixed generating the timer externally from the FPGA. An FPGA has been used to control the timing of the signal. To transduce the electrical signal into an optical one a small board was designed. The FPGA software will be represented in the Appendix. Instead, a picture of the system controller and of Adaptor board is shown in Fig.6.4.

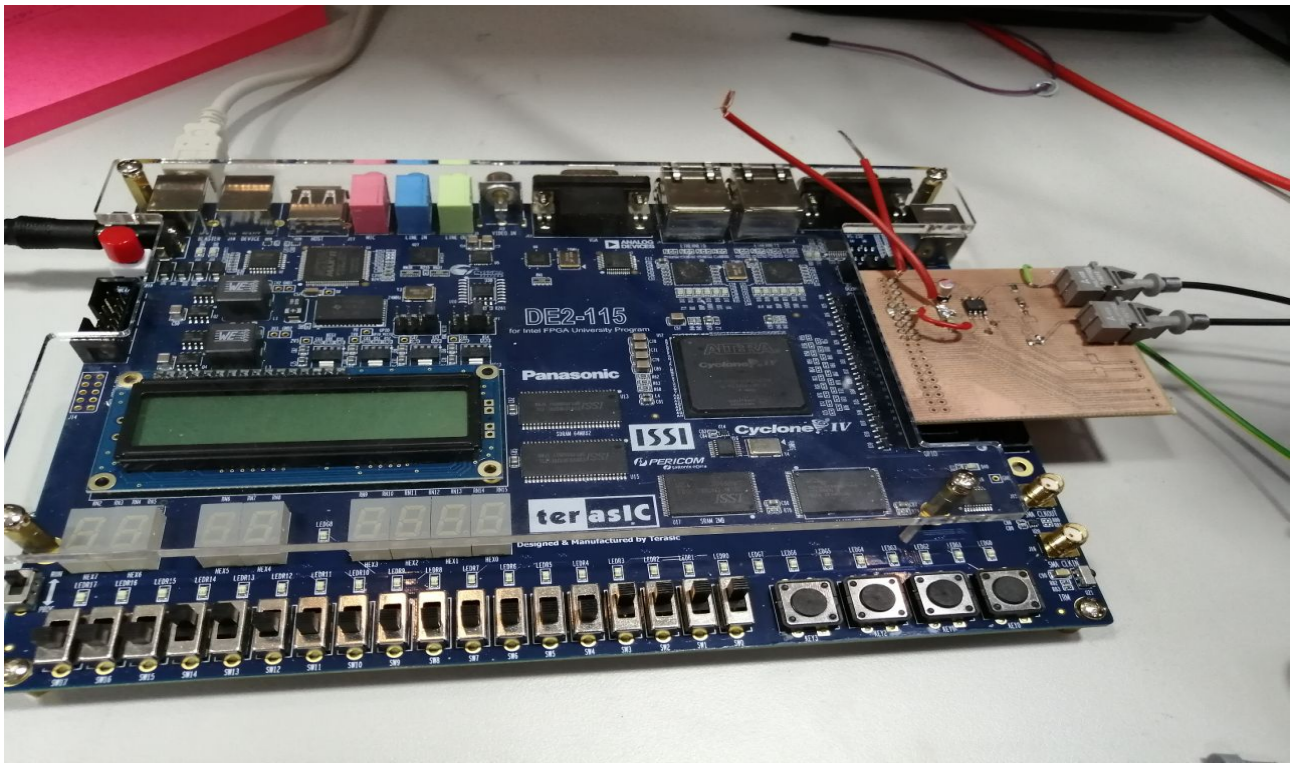

Figure 6.4: Method and System Controller

In addition to the two signals for the DUT and the Shorter, another signal was taken into account other fault feedback signal, in order to report a possible Short Circuit to the controller.

6.2 Verification Method

In this section it will show the tests performed to verify the correct working of the method. The circuit has been tested for both the main types of Short Circuit FUL (Fault under load) and HSF (Hard switch Fault). In both circumstances the protection works. The RC Method showed the right functionality.

6.2.1 Verification Fault Under Load (FUL test)

The Fault under load occurs if the Short Circuit verifies when the DUT is already fully turned-on and it is already conducting current.[21] To simulate this type of scenario during the normal conduction of the DUT (low side switch), the leg's high side switch was activated in a specific moment. This "Short Circuit moment" can be selected directly from the key switch of the FPGA. To configure it in a proper way, or else to run the FUL test, the FPGA SWITH[16:17] must be ON (High position). The pulse length of the first pulse, which can be used to later select the value of the Load current, can be selected using the SWITH[0:15] from 1us to 3.276ms with 50ns step. The test started only after the release of the KEY[0] and be has been performed once. The shorter pulse length was programmable to be 1µs in this test. It has been sufficient to allow the Drain current to reach the saturation value and to prevent the failure of the DUT. Fig. 6.5 illustrates the reaction of the setup with a disabled RC Method, while in Fig. 6.6 the same test was run with an enabled RC Method.

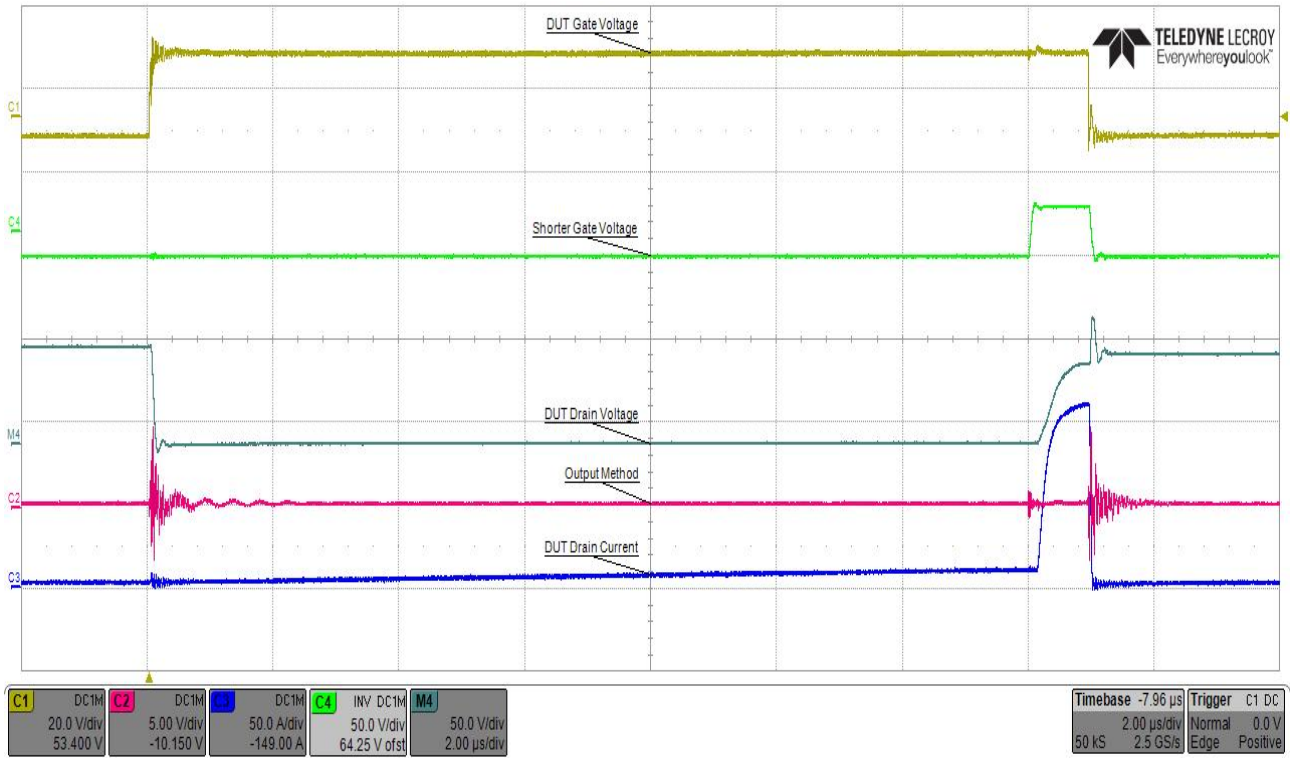

Figure 6.5: FUL Test with RC Method Disable

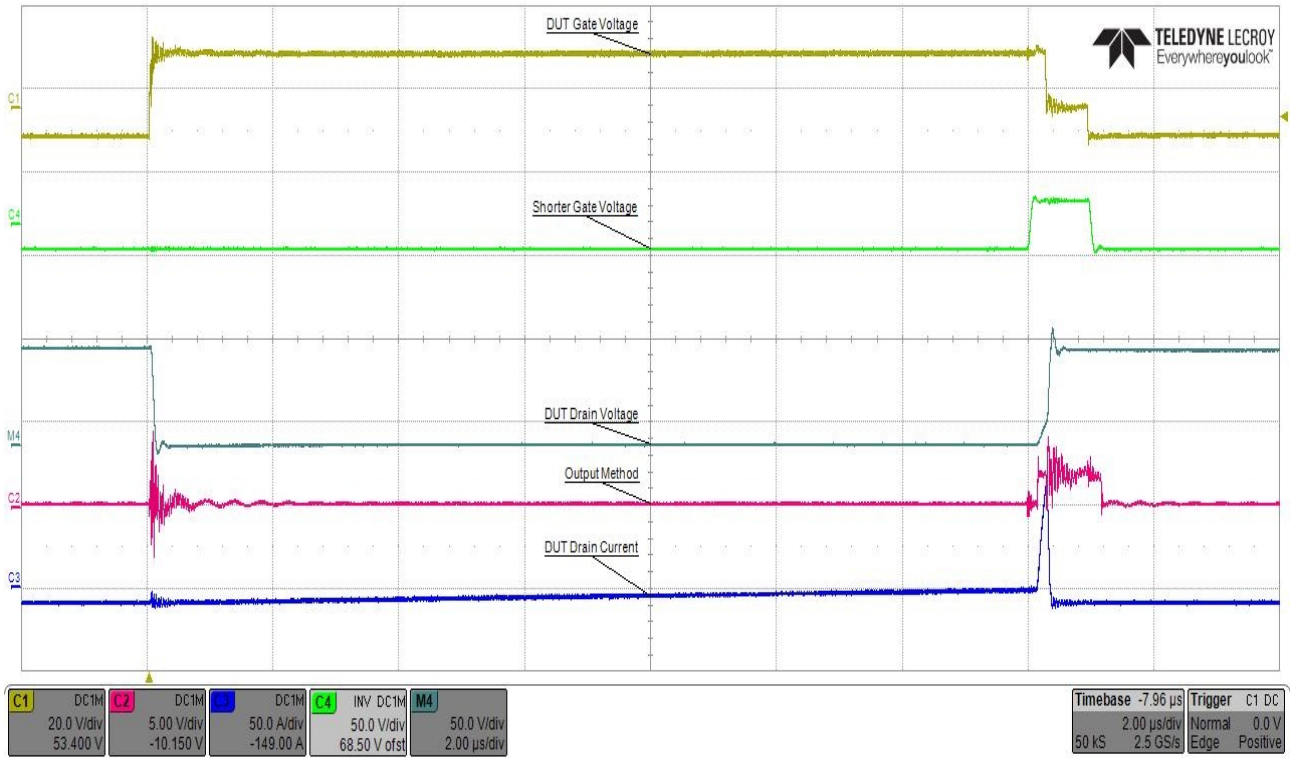

Figure 6.6: FUL Test with RC Method Enable

The test was performed at a low voltage (75V), i.e. the maximum value allowed in a laboratory without technician's supervision. The same test was also performed at higher voltage (200V). The purple waveform represents the output of the method: it was measured on the isolated Gate Driver input of the MOSFET, which discharged the DUT Gate Capacitance. In fact, when the Method detected the Short Circuit, the forward voltage of the Optocoupler LED rose to 2.5V. As illustrated in Fig. 6.7, when the Fault Gate Driver turned on the Fault MOSFET (2N7002), it started to conduct current, but its $R_{ds(on)}$ was too high, $2\Omega \leq R_{ds(on)} \leq 9\Omega$. Therefore, there created a partition between the R_g and $R_{ds(on)}$, whose value was about 1.5V, which is enough to switch off the DUT. To improve the Method, the Fault MOSFET should be substituted by a more technologically and advanced device with a lower $R_{ds(on)}$. In the board was already plan a signal to disable the DUT Gate Driver, but during the debugging some problem was discovered. Because the method was supply between 0V and 5V, while the DUT Gate Driver between -5V and 15V. Hence, the reference voltage was not the same.

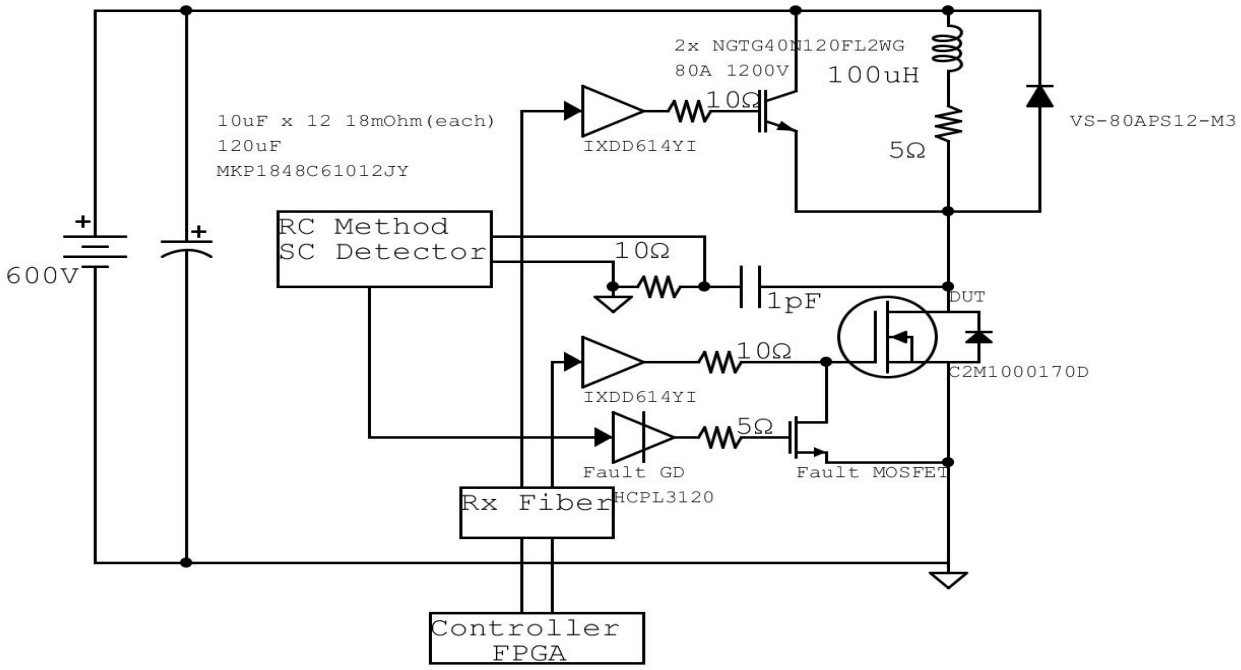

Figure 6.7: Simplified diagram of the system

It is important to quantify the actual speed of the Method. To have an estimation of the performance that it can be reaches. Fig. 6.8 shows the RC method detection time, while Fig. 6.9 shows how much time is required by this Method to initiate the SC protection after the Short Circuit event.

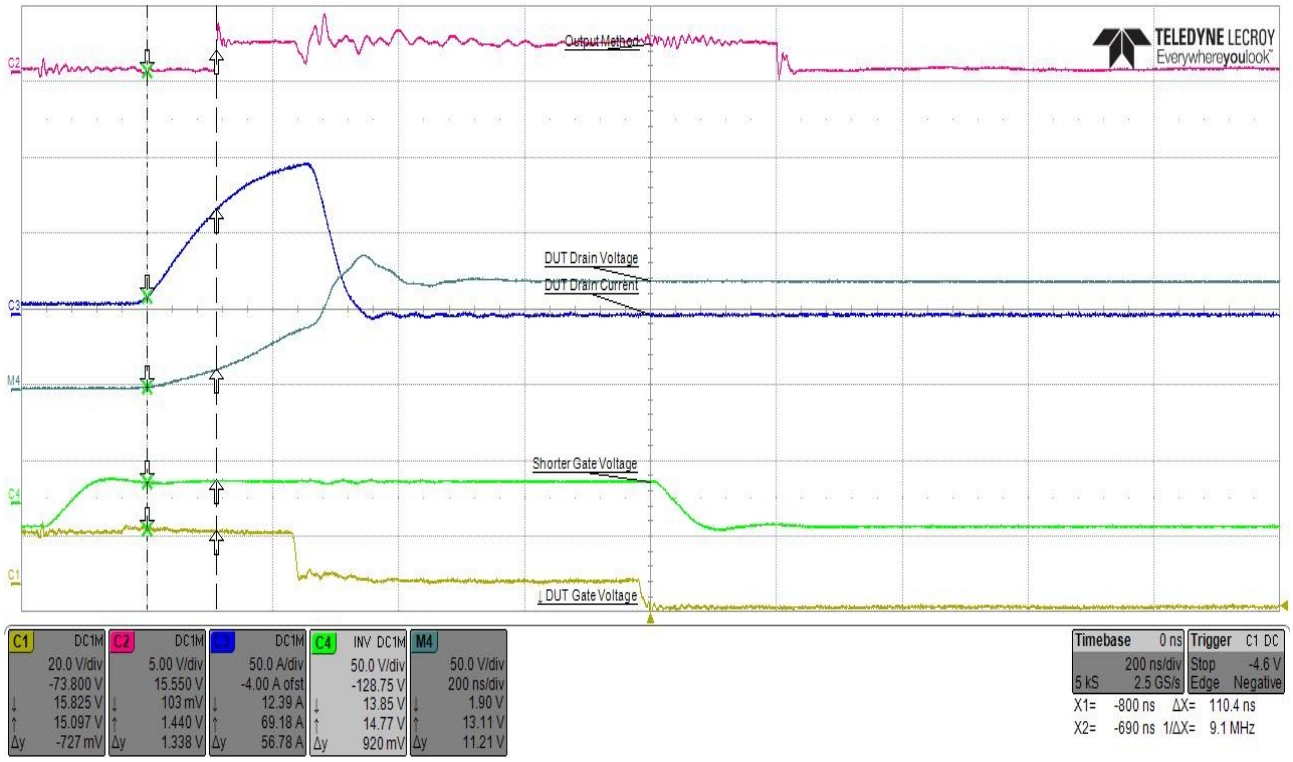

Figure 6.8: Detection speed Method

In Fig 6.8 it is possible to verify the Method's detecting velocity, which is around 110ns. It could be lowered by reducing the Timer threshold, or by using a trimmer to set the input threshold at the comparator.
Instead, Fig. 6.9 illustrates the detection time summed to the protection time. The protection time could be lowered for instance by using a not-isolated Fault Gate Driver. The time required for the Method to react to from the fault instant to the protection moment is about 230ns.

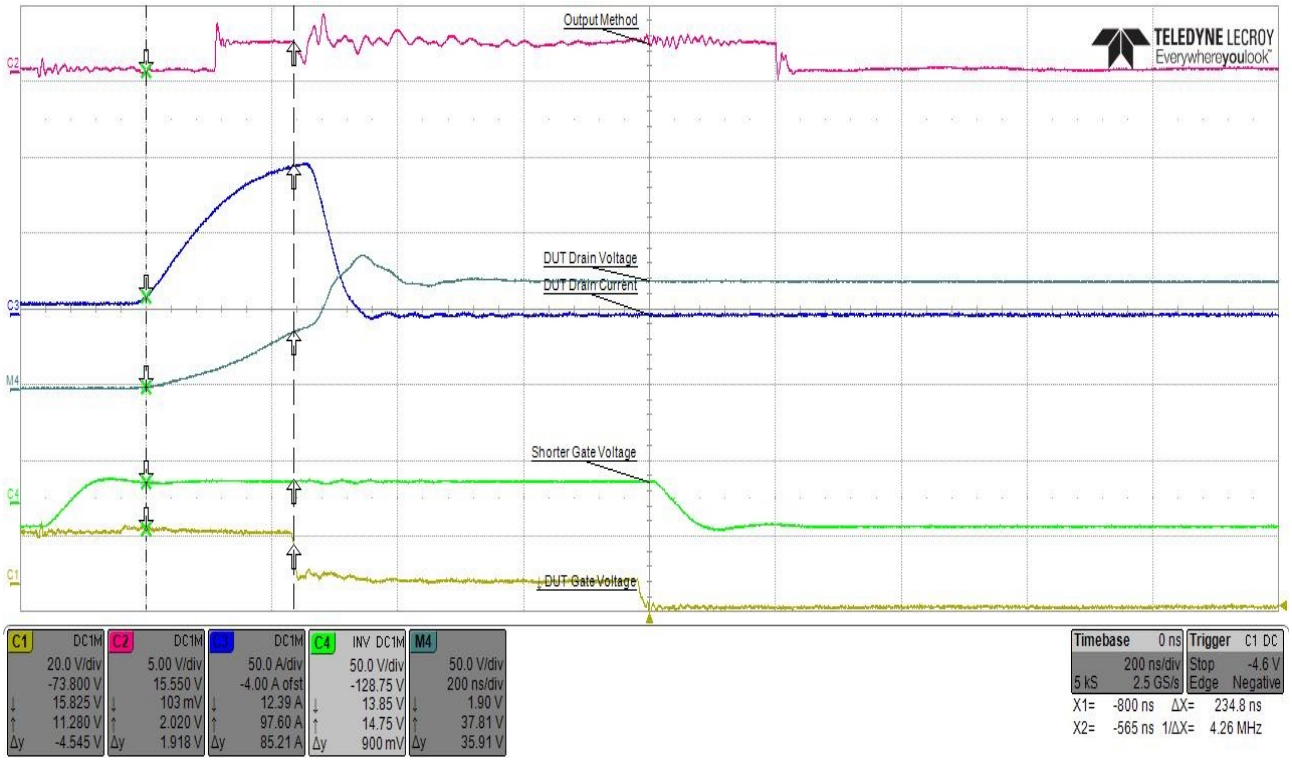

Figure 6.9: Detection plus Protection speed Method

6.2.2 Verification Hard Switch Fault (HSF test)

During this experiment, the fault verified while the DUT was turned off, i.e. before it switched back on. Hence, when the DUT was turned on, it was under Short Circuit conditions. The hold was set to throw the timer's trimmer around 100ns. To configure it adequately, or else to ran the HSF test, the FPGA SWITH[16:17] must be OFF (Low position). In this test the Shorter is enabled between the first and second pulse, the short circuit finishes at the end of the test. Fig. 6.10 shows the waveform registered from the Oscilloscope.

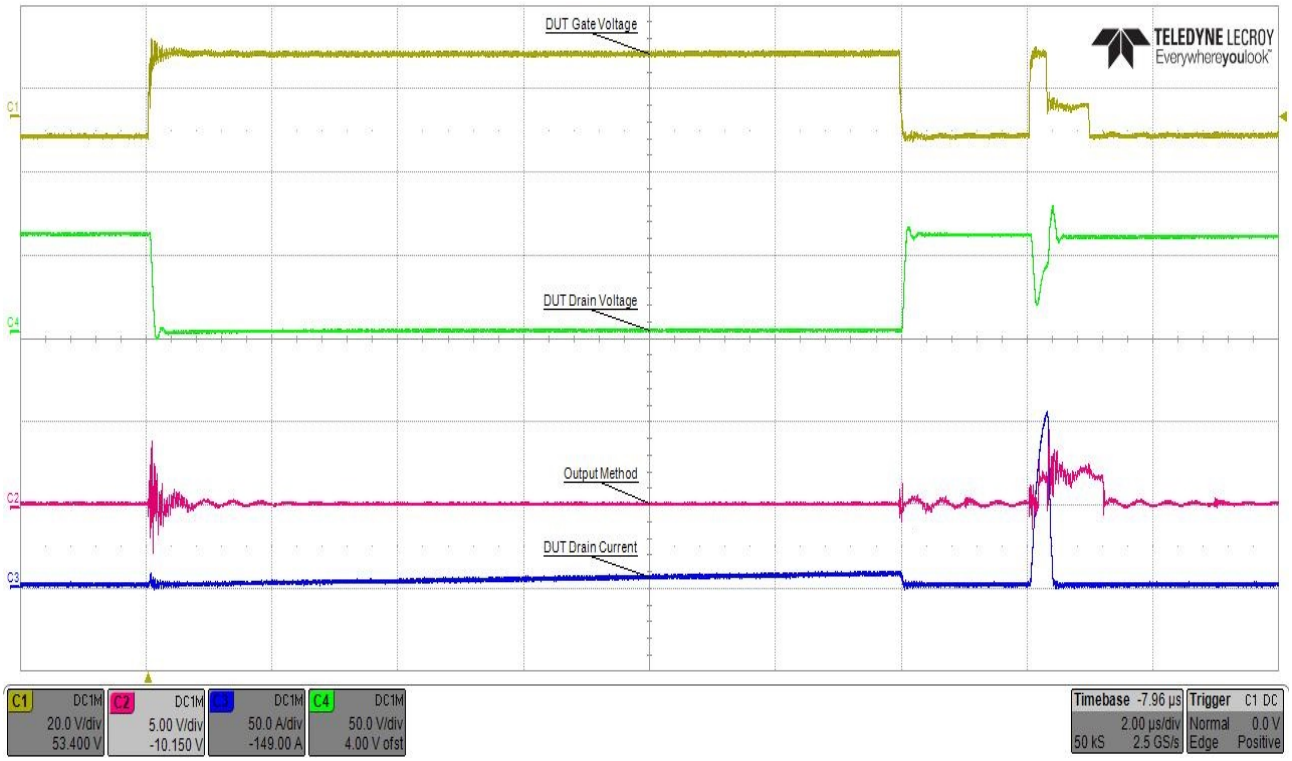

Figure 6.10: Double Pulse test in HSF

Also in this experiment, the Method has been able to detect the Short circuit and protect the DUT, even though the DUT was switched off with a voltage not exactly equal to 0V. As well as during the previous experiment, the Gate voltage located after the protection did not reach a low value (-5V), but it remained around 1.6V. Even so, it was enough to switch off the DUT. Fig. 6.11 illustrates the value of the Gate Voltage when it detected the Fault.

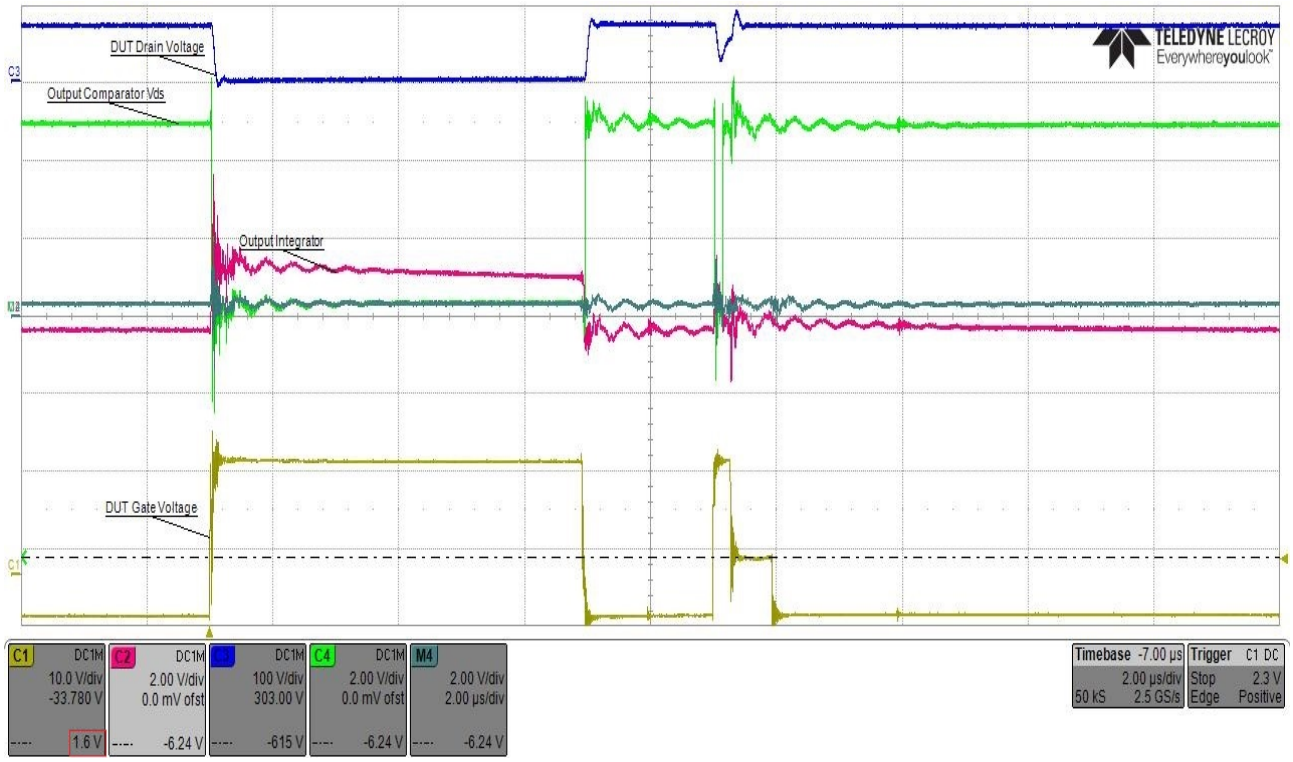

Figure 6.11: Value Gate Voltage under HSF Fault

6.3 Conclusion

Conclusively, within this Chapter various experiments were performed and various variables (such as different load current and source voltage) were taken into consideration to verify the effectiveness of the Method. It has been proved that the method to detect short circuit analysing the current induced by a capacitor on a Drain is possible. Moreover, the method is also faster than other more common method. As mentioned beforehand, various improvements need to be implemented, their outcomes will be detailed in a papers. At the moment this has been considered more than sufficient to demonstrate the validity of the method.

CHAPTER 7

Code

7.1 FPGA Programmable Double Pulse TEST

```
module test (
    input CLOCK_50, reset, // 50MHz clock
         input wire [17:0] SW,
         input wire [3:0] KEY,
    output [8:0] LEDG,
    output [35:0] GPIO
);

    reg [31:0] counter = 0;
         reg signal1;
         reg signal2;
         reg wt;
         reg wt3;
         reg value = 1'b1;
         reg [13:0] po;
         reg [24:0] LOAD;
         reg [24:0] EDGE1;
         reg [24:0] EDGE2;
         reg [24:0] EDGE3;
         reg [24:0] sc1;
         reg [24:0] sc2;
```

```
22          reg [24:0] STOP;
23          reg [6:0] ov;
24          reg [10:0] pc;
25          reg SEL;
26          reg SEL1;
27
28      assign LEDG[8] = 1'b1;
29          assign LEDG[1] = wt;
30          assign GPIO[1] = signal1;
31          assign LEDG[2] = signal2;
32          assign GPIO[2] = KEY[0];
33          assign GPIO[15] = signal2;
34
35         always @ (posedge CLOCK_50)
36         begin
37            SEL <=  SW[17] ;
38                 SEL1 <=  SW[17] ;
39                 po <= SW[13:0];
40                 if(SEL==0 & SEL1==0) begin
41                 EDGE1 <=5*50+(po*50);
42                 EDGE2 <=7*50+(po*50);
43                 EDGE3 <=8*50+(po*50);
44                 sc1 <= 6*50+(po*50);
45                 sc2 <= 0;
46                 STOP <= 10*50+(po*50);
47                 if (KEY[0] == 0)
48                 begin
49                       value <= 1;
50                                 counter <= 1;
51                                 signal1 <= 0;//0
52                                 signal2 <= 0;//0
53                                 wt <=1;
54                                 wt3 <= 1;
55                 end
```

```
56
57              if(wt==1 & KEY[0] == 1)
58              begin
59                      wt <= 0;
60                      signal1 <= 1;
61                      signal2 <= 0;
62              end
63
64              if (counter != 0 && wt == 0)
65              begin
66                      counter <= counter + 1;
67                      if(counter >= 1 && counter <= EDGE1)
68                      begin
69                              signal1 <= 1;
70                              signal2 <= 0;
71                      end
72
73                      if(counter >=EDGE1 && counter<=EDGE2)
74                      begin
75                              signal1 <= 0;
76                              signal2 <= 0;
77                      end
78                      if(counter >=sc1 )
79                      begin
80                              signal1 <= 0;
81                              signal2 <= 1;
82                      end
83                      if (counter >=EDGE2 && counter<=EDGE3)
84                      begin
85                              signal1 <= 1;
86                              signal2 <= 1;
87                      end
88                      if (counter ==STOP) begin
89                              signal1 <= 0;
```

```
                                signal2 <= 0;
                                counter <= 0;
                                wt<= 0;
                        end
                end
        end

        if(SEL==1 & SEL1==1) begin
        sc1 <= 7*50+(po*50);
        EDGE1 <=8*50+(po*50);
        //EDGE2 <=7*50+(po*50);
        //EDGE3 <=8*50+(po*50);
        sc2 <= 0;
        STOP <= 10*50+(po*50);
                if (KEY[0] == 0)
                begin
                      value <= 1;
                                counter <= 1;
                                signal1 <= 0;//0
                                signal2 <= 0;//0
                                wt <=1;
                                wt3 <= 1;
                end

                if(wt==1 & KEY[0] == 1)
                begin
                        wt <= 0;
                        signal1 <= 1;
                        signal2 <= 0;
                end

                if (counter != 0 && wt == 0)
                begin
                        counter <= counter + 1;
```

```
124                         if(counter >= 1 && counter <= sc1)
125                         begin
126                                 signal1 <= 1;
127                                 signal2 <= 0;
128                         end
129
130                         if(counter >=sc1 && counter<=EDGE1)
131                         begin
132                                 signal1 <= 1;
133                                 signal2 <= 1;
134                         end
135
136                         if(counter >=EDGE1)
137                         begin
138                                 signal1 <= 0;
139                                 signal2 <= 0;
140                         end
141
142                         if (counter ==STOP) begin
143                                 signal1 <= 0;
144                                 signal2 <= 0;
145                                 counter <= 0;
146                                 wt<= 0;
147                         end
148                 end
149         end
150 end
151
152
153 endmodule
```

7.2 Standoffs for PCB

The PCB to have a stable position required spacers from the ground and stability. Supports give stability and they isolate the components and the support desk surface. The components were designed with FreeCAD 3D and printed with a 3D printer. ($h = 25mm, d_i = 7.2mm, d_e = 11.5mm, d_{base} = 17.5$)

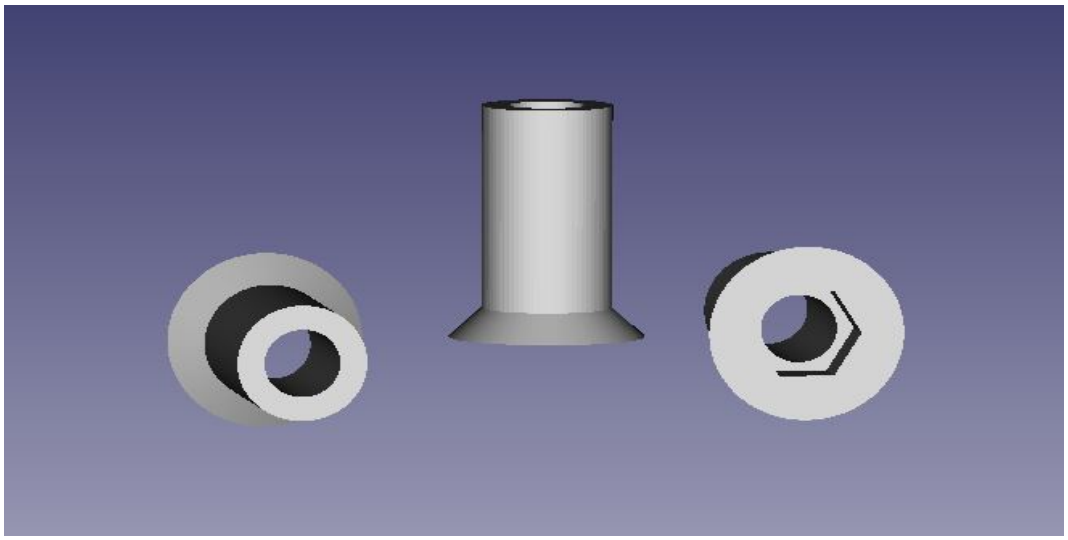

Figure 7.1: 3D Standoffs/Spacer

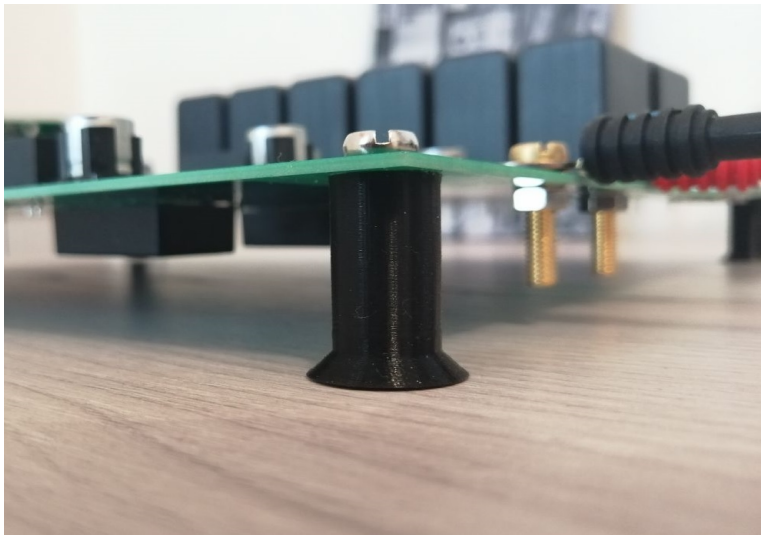

Figure 7.2: Picture Standoffs/Spacer

CHAPTER 8

Glossary Abbreviations

- **DUT**: Device Under Test
- **FUL**: Fault Under Load
- **GD**: Gate Driver
- **HSF**: Hard Switch Fault
- **MOSFET**: Metal Oxide Semiconductor Field Effect Transistor
- **OC**: Over Current
- **IGBT**: Insulated Gate Bipolar Transistor

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