POLITECNICO DI TORINO

MASTER'S THESIS

FPGA implementation of an A/D conversion and a Pulse Width Modulation with interleaving for a multiphase drive system

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Abstract

The scientific context in which the thesis project takes place, is that of electric machines. The work carried out is part of the realization of new configurations of asynchronous electric motors wound so as to allow the online change of the number of phases and poles generated. Such a type of motor is commonly referred to as WICSC (Wound Indipendently-Controlled Stator Coils). The main application to which we can refer for this type of engine is certainly the automotive field. The engine under study was designed to have a number of phases greater than or equal to three (commonly referred to as a multiphase machine).

The work presented in this thesis is based on the implementation on FPGA of two main structure preparatory to the realization of the complete control system of an induction machine with the capability of changing number of phases and poles. The first structure implemented is related to the acquisition of the samples provided by a dedicated measurement system able to measure the current flowing in each slot of the machine. The second structure implements the Carrier Based Pulse Width Modulation. In the implementation of the modulation section the technique of interleaving is used to improve the overall performace. The implementation of the structures for sampling and sample management and for PWM modulation was carried out on FPGA using the VHDL language. The realized structures are simulated first and subsequently verified with dedicated testbench. The work is completed by simulations in Matlab-Simulink in order to have This model offers the possibility of qualitatively evaluating the benefits introduced by the interleaving modulation technique.

All the work has been carried at the division of Electric Power and Energy Systems in the department of Electrical Energy Engineering at KTH Royal Institute of Technology (Stockholm).

Thesis Outilne

This thesis is divided in four main parts:

The firset part is devoted to a brief introduction on asynchronous electric machines with particular emphasis on the structure of a multiphase machine and its advantages. Finally, the structure of the engine involved in the thesis work is illustrated.

The second part concerns the two structures built for A/D conversion and for the implementation of Pulse Width Modulation. For both sections, the initial specifications and the proposed solutions are described by carefully analyzing the operation in detail and the techniques used. As for PWM modulation, the interleaving technique and its benefits are introduced.

The third part of the thesis illustrates the model created in matlab-simulink to evaluate the benefits introduced by the interleaving technique as a first approximation. In particular, the stress reduction on the DC-bus and the input capacitors of the inverters are presented, as well as the reduction of losses related to the THD improvements in the phase to phase voltage.

Last part expose the measurements obtained from two dedicated testbench for the analog to digital conversion and samples acquisition in the FPGA, as well as the verification of the functioning of the Pulse Width Modulation. The conclusion about the achievement obtained and the future development are finally presented.

Contents

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List of Abbreviations

A/D	Analog to Digital
ADC	Analog to Digital Converter
CG	Carrier Generator
CH	Configuration Handler
EVM	Evaluation Module
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
LVDS	Low Voltage Differential Signal
MPM	Multiphase Machine
mx-py	x-phase y-pole
PB	Power Board
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
qs	Slot per pole per phase
RF	Register File
RTL	Register Transfer Level
TB	Test Bench
TH	Transition Handler
THD	Total Harmonic Distortion
VHDL	Very High Speed Integrated Circuit Hardware Description Language

Chapter 1

Multiphase Machine

1.1 Electrical machine

An electric motor is an electrical machine that converts electrical energy into mechanical energy. Most electric motors operate through the interaction between the motor's magnetic field and electric current in a wire winding to generate force in the form of rotation of a shaft. Electric motors can be powered by direct current (DC) sources,such as from batteries, or by alternating current (AC) sources, such as a power grid, inverters or electrical generators.Electromechanical energy conversion takes place via the medium of a magnetic field or an electric field, but most practical converters use magnetic field as the coupling medium between electrical and mechanical systems, this is because the electric storing capacity of the magnetic field is much higher than that of the electric field.

The main elements that characterize an electric motor are the following:

- Stator
- Rotor
- Airgap
- Windings

Stator:
The stator is the stationary part of the motor's electromagnetic circuit and usually consists of either windings or permanent magnets. The stator core is made up of many thin metal sheets, called laminations. Laminations are used to reduce energy losses that would result if a solid core were used.

Rotor:
In an electric motor, the moving part is the rotor, which turns the shaft to deliver the mechanical power. The rotor usually has conductors laid into it that carry currents, which interact with the magnetic field of the stator to generate the forces that turn the shaft. Alternatively, some rotors carry permanent

magnets, and the stator holds the conductors.

Airgap:
The distance between the rotor and stator is called the air gap. The air gap has important effects, and is generally as small as possible, as a large gap has a strong negative effect on performance. It is the main source of the low power factor at which motors operate. The magnetizing current increases with the air gap. For this reason, the air gap should be minimal. Very small gaps may pose mechanical problems in addition to noise and losses.

Windings:
Windings are wires that are laid in coils, usually wrapped around a laminated soft iron magnetic core so as to form magnetic poles when energized with current.

1.1.1 Induction motor

An induction motor or asynchronous motor is an AC electric motor in which the electric current in the rotor needed to produce torque is obtained by electromagnetic induction from the magnetic field of the stator winding (fig. 1.1). An induction motor can therefore be made without electrical connections to the rotor. An induction motor's rotor can be either wound type or squirrel-cage type.

In both induction and synchronous motors, the AC power supplied to the motor's stator creates a magnetic field that rotates in synchronism with the AC oscillations. Whereas a synchronous motor's rotor turns at the same rate as the stator field, an induction motor's rotor rotates at a somewhat slower speed than the stator field. The induction motor stator's magnetic field is therefore changing or rotating relative to the rotor. This induces an opposing current in the induction motor's rotor, in effect the motor's secondary winding, when the latter is short-circuited or closed through an external impedance.

The induced currents in the rotor windings in turn create magnetic fields in the rotor that react against the stator field. Due to Lenz's Law, the direction of the magnetic field created will be such as to oppose the change in current through the rotor windings. The cause of induced current in the rotor windings is the rotating stator magnetic field, so to oppose the change in rotor-winding currents the rotor will start to rotate in the direction of the rotating stator magnetic field. The rotor accelerates until the magnitude of induced rotor current and torque balances the applied mechanical load on the rotation of the rotor. Since rotation at synchronous speed would result in no induced rotor current, an induction motor always operates slightly slower

than synchronous speed. The difference, or "slip," between actual and synchronous speed varies from about 0.5% to 5.0% for standard Design B torque curve induction motors. For rotor currents to be induced, the speed of the physical rotor must be lower than one of the stator's rotating magnetic field; otherwise the magnetic field would not be moving relative to the rotor conductors and no currents would be induced. Slip, s, is defined as the difference between synchronous speed and operating speed, at the same frequency, expressed in rpm, or in percentage or ratio of synchronous speed. [5]

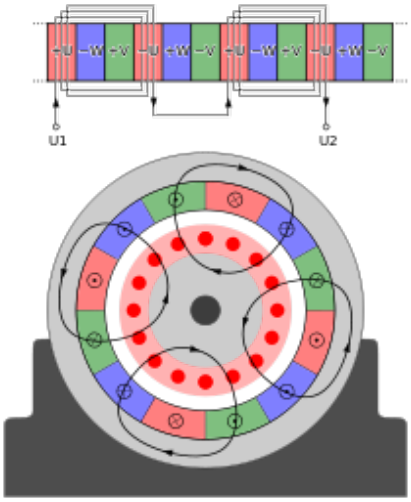


FIGURE 1.1: Typical winding pattern for a 3-phase 4-pole motor

1.2 Overview of Multiphase Machines

An electric machine with a total number of phases n > 3 is defined as multiphase. There exist two main types of multi-phase machines: the symmetric and the asymmetric ones. In symmetric multi-phase machines, the phases are equally distributed over the stator circumference with a displacement angle of $2\pi/n$ electric degrees. This machine type is an extension of the conventional symmetric three-phase machine shown in Fig. 1.2(a). The arrows represent the direction of the positive flux linkage in the machine phase, while the dashed lines indicate the negative flux linkage direction in the same phase. Fig. 1.3 shows the example of a six-phase symmetric multi-phase machine, where it is evident that the phase couples a-d, b-e and c-f contribute (with opposite sign) to the same flux linkage, respectively. Such machine is topologically not different from a three-phase counterpart, since producing positive flux linkage sequentially in the symmetric six-phase machine can be equally achieved in the three-phase machine with positive and negative

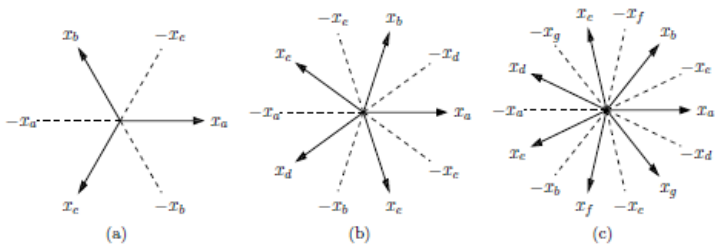


FIGURE 1.2: Examples of symmetric multi-phase machines: (a)three-phase, (b)five-phase, (c)seven-phase

flux linkage sequences [11],[8]. Similar considerations apply for other even-phase symmetric machines. For this reason, even-phase symmetric machines are not of significant importance. In asymmetric multi-phase machines (also

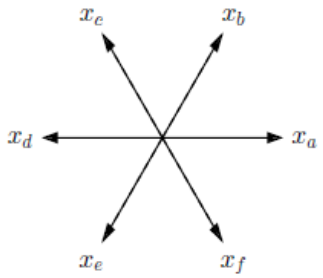


Fig. 2.2: A six-phase symmetric multi-phase machine ($n = 6$).

FIGURE 1.3: 6-phase symmetric multi-phase machine

known as split-phase or multiple-star machines), a number N of identical m-phase sets are geometrically distributed with a displacement of $180^\circ/(mN)$ electric degrees between the different sets. The most common case of split-phase machines considers m = 3, thus combining N identical three-phase sets with a displacement of 60=N electric degrees between the sets. The general displacement expression of $180^\circ/(mN)$ electric degrees comes into use when $m \neq 3$. An example of a ten-phase multi-phase machine with N = 2 identical sets of five phases is shown in Fig. 1.4, where the displacement between the two sets is $180^\circ/(5*2)$ = 18 electrical degrees. An interesting aspect is that all asymmetric multi-phase machines with m = 3, differently from the case of symmetric multi-phase machines, may be supplied by N three-phase converters [12]. Of course, this potential advantage does not exist for asymmetric multi-phase machines where $m \neq 3$.

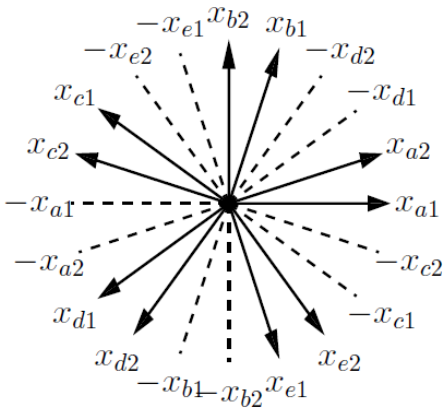


FIGURE 1.4: Ten-phase split-phase machine (n=10, N=2, m=5)

1.3 Virtues of MPM

This section summarises the main potential advantages of multi-phase machines and drives. Such benefits could translate into business advantages for some specific systems and applications, and therefore must be considered with the perspective of the application and not as statements valid for any drive system. In the last few years, a growing interest in multiphase machine has been observed. Different reasons can explain this, the main ones can be the following:

- The flied produced by stator excitation in a multiphase machine is characterized by a lower space-harmonic content, leading to an higher efficiency than in a three-phase machine;
- Multiphase machines are less susceptible than their three-phase counterparts to time-harmonic components in the excitation waveform;
- Multiphase machines have a greater fault tolerance than their three-phase counterparts [9].

1.3.1 The reduction of phase currents at constant power and voltage levels

The first, and probably most straightforward, advantage of multi-phase machines is the capability of lowering the current rating per phase by keeping the same voltage and power ratings of a conventional three-phase machine. This is well summarised by the well-known equation of the active power in

a n-phase balanced system [16]:

$$p = \frac{1}{2} uicos(\phi) \tag{1.1}$$

where p is the active power, u is the peak voltage, i is the peak current, and $cos(\phi)$ is the power factor. By keeping the same p and u values, and approximately a similar power factor, it is immediate that lower values of i are obtained by increasing the phase number n. In principle, the reduction of the current rating per phase allows the use of semiconductor technologies with lower current ratings as well. However, as the number of phases increase, also the number of frequency converters increase. This seem not to be a real issue in high-power systems, where already today several parallel converters are used to feed a high-power three-phase machine.

1.3.2 The machine manufacturing aspects

While the electric aspects of splitting the power among n phases is well described by eqn. 1.1, the effect of a multi-phase design on the manufacturing of an electric machine is not as straightforward. The work in [10] helps in giving a good overview of the relations between the design choices in an electric machine. One of the most important equations obtained from the analysis is the following:

$$pu = k(\frac{As}{Nt} bn) \tag{1.2}$$

where k is a coefficient that does not depend on the winding structure of the machine, but only the magnetic, thermal and electrical loading of the machine itself. Therefore, for machines with an homogeneous design in terms of thermal class, insulation technology, and effectiveness of the cooling system, k can be regarded approximately constant. This is actually confirmed in a series of design examples provided in [13]. The other parameters in eqn. 1.2 are defined as follows:

- As is the slot cross-section area;
- Nt is the number of turns per coil;
- b is the number of parallel ways per phase;
- n, as before, is the number of phases.

According to eqn. 1.2, keeping a constant voltage u and increasing the power p requires one of the following actions [12]:

- increase As: by increasing the slot cross-sectional area, it is automatic that the stator outer diameter is bound to grow too, in order to keep the yoke flux density within acceptable values. Therefore, the overall machine size increases too, making it not an optimal design choice;
- increase b: this strategy can be pursued as long as b is lower or equal to the number of poles 2p in the machine, which represents an upper limit for the application of this design choice;
- decrease Nt: this can be achieved until Nt = 1.
- increase n: after the limitation b = 2p is reached, the only suitable way left to increase the rated power without machine size increase is to increment of the number of phases.

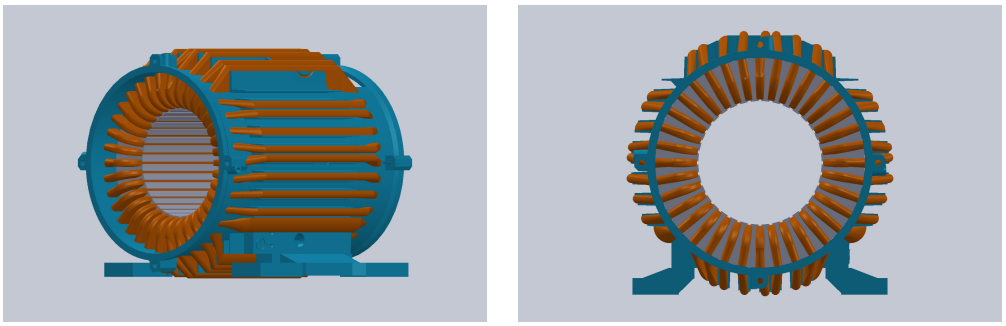
Thus, in some cases it may be useful to increase the power rating, at constant rated voltage, through an increment of n. In some high-power existing three-phase systems, where many converter modules are already placed in parallel to fulfil the current requirements of the three-phase machine, this design choice may lead to the use of the very same number of converters connected to a cheaper electric machine.

1.3.3 The fault handling

An important aspect when dealing with multi-phase machines is the potential of fault tolerance operation that could arise by the use of $n > 3$ phases. The principle is very basic and quite clear, as presented in [10],[9]: a multi-phase machine can continue to operate with a rotating field as long as no more than n-3 phases are faulted. In other words, as long as a minimum of three phases can be guaranteed, a rotating magnetic field can be produced to rotate the machine, although with different power/torque ratings. Clearly, the amount of power and torque that can be produced depends on the adopted fault strategy, on the system topology as well as on the machine design. However, most of the time this type of fault handling requires a detection and a reconfiguration of the control, in order to compensate for the physical absence of one phase in the control models.

1.4 Overview of the motor involved

In figure 1.5 a rapresentation of the machine involved in the thesis work is shown. The axial section of the machine is represented in fig. 1.6. It is possibile to observe the structure of the stator and the rotor.



(A) *Corner view* (B) *Axial view*

FIGURE 1.5: Corner and axial view of the machine involved in the project

This new configuration has been presented in [2]. The innovative topology takes place by replacing the multi-phase stator cage winding - presented in [4]- with multi-turn coils that are wound axially along the stator core and short-circuited at one axial end. In this way the advantage of having each slot corresponding to a potentially separate winding, individually supplied, is maintained. The structure of the stator winding in this machine design (define by the author wound independently-controlled stator coils - WICSC) facilitates the possibility of online changing of the number of pole-pairs as well as the number of phases [2]. Another reason that led to the choice of this new configuration is linked to the current levels required by the DC supply in the configuration described in [4]. In this way, a machine design that is compatible with the present-day high-voltage battery system can be produced, while the capabilities of pole-changing and phase-changing of the topology of [4] can still be achieved.

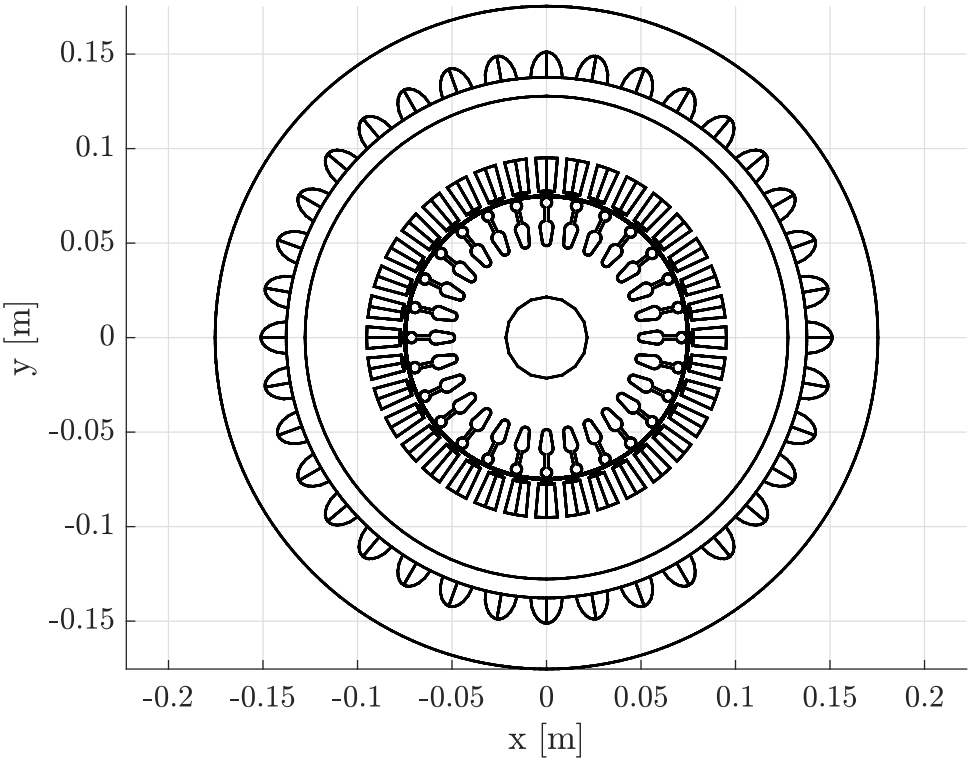


FIGURE 1.6: Axial section of the machine involved in the project

Chapter 2

Complete system overview

Below is an overall description of the system to be implemented. Complete driving of an engine requires several sections. Starting from a higher level of abstraction, the driving of a machine can be summarized as follows:

- Measurements of the quantities to be controlled;
- Processing of the control, starting from the physical quantities measured;
- Realization of the drive control signals.

In our case, as with all more complete control systems, two control levels are achieved: a current control and a speed control. The realization of these measures requires a section dedicated to the necessary sensors, the conditioning of the analog signals obtained in preparation for the analog-digital conversion and the electronics necessary for the AD conversion. Once the samples are obtained, it is necessary to use a section capable of communicating with the previous one, in order to acquire the digital signals and make it possible to process this information for the management of the machine control. The information above, once processed, provides the information necessary for the implementation of the modulation (in detail in the chapter 4). The modulation ends with the generation of the signals necessary for the inverters to suitably drive the machine. Considering that our multiphase machine is made up of 36 slots, each of which is independently controlled, and that the signals to be supplied to the inverters for driving the IGBTs are signals with a high switching frequency, a section is introduced for the transmission of these signals after a conversion of electrical information into optics. Everything is carried out mainly with a view to compliance with the electromagnetic compatibility criteria. Below is a diagram to provide an overview of the complete system (fig. 2.1): The realization of such a type of system requires knowledge that ranges from the theory of electrical machine design, to the knowledge of driving techniques for electric drives, passing through knowledge of firmware programming for control via an FPGA processor and knowledge of hardware description languages, like the VHDL for

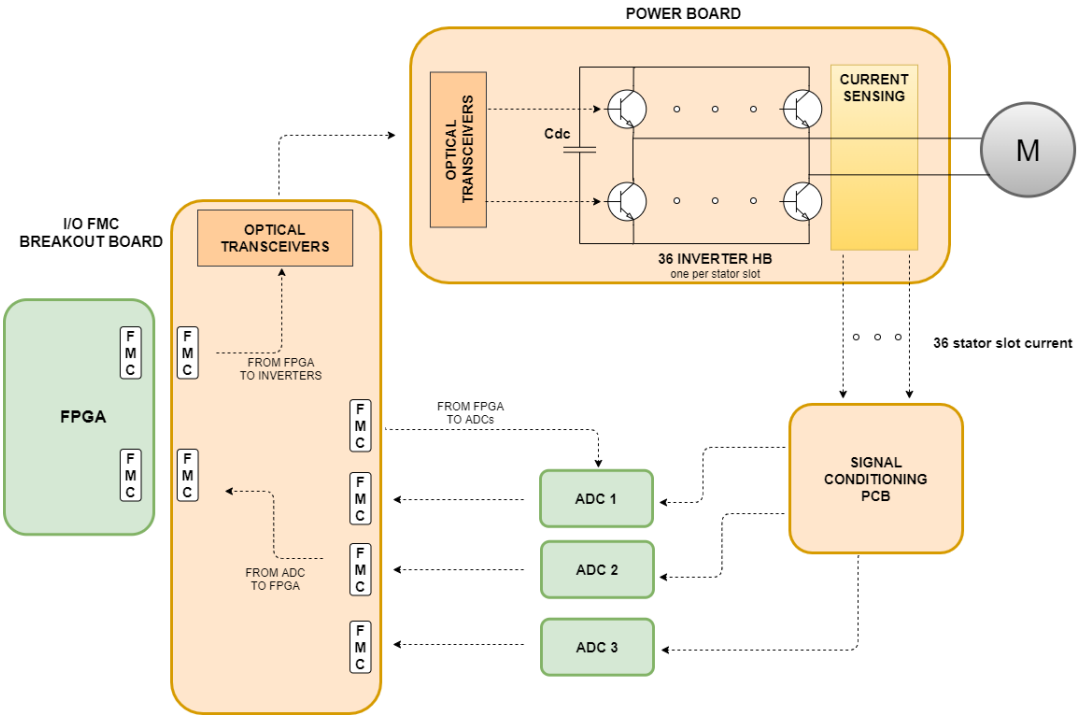


FIGURE 2.1: System overview diagram

the realization of dedicated hw. It was therefore necessary to set up a team able to combine the above skills. Below are the sections of the project under my responsibility:

- FPGA/ADC interface and ADC control;
- FPGA/ADC synchronization and acquisition of samples on FPGA;
- Carrier Based PWM modulation and IGBT driving.

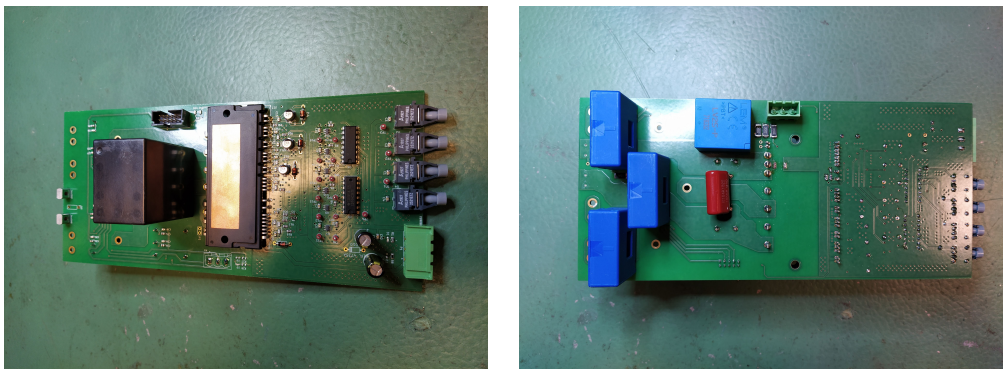
Chapter 3

A/D conversion

3.1 Current sampling

3.1.1 Overview of measurement system

Given the structure of the motor (36 slots stressed independently [2]), to carry out a control it is necessary to monitor and adjust the currents in each slot. This requires the construction of a measuring system organized in several parts. This system must be able to take the information relating to the slot currents and implement signal conditioning in order to adapt the dynamics of the output signal from the current sensor to the dynamics of the analog to digital converter. The inverters used to drive the machine are mounted on a dedicated PCB, hereafter a power board (PB). The inverter module has outputs for sensing the current flowing in each leg. These outputs are connected, again on the power board, to three current sensors (LEM sensors, in fig. 3.1). The LEM sensors offer the possibility to adjust the dynamics of the output



(A) *Power board, top view*

(B) *Power board, bottom view*

FIGURE 3.1: Power board, top and bottom view (LEM sensors on the left)

signal, considering the maximum current ranges to be measured, creating a

variable number of windings around the sensor. The output of the current sensors will go to the input of a PCB so that the conversion of the information from current to voltage is carried out, passing through the gain adjustment so as to adapt the dynamics with that of the ADC and introducing components for protection of the channels of the ADC.

3.1.2 ADC choice

The choice of the board was dictated by several specifications. The constraints introduced led to the choice of a card produced by analog devices: AD9249 [1]. A first factor was therefore constituted by the number of convert-

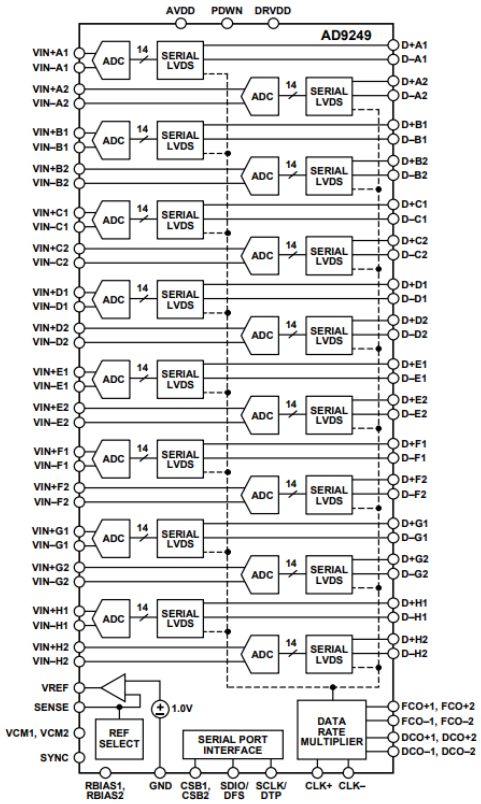


FIGURE 3.2: ADC, functional blockdiagram

ers that must be present on the board in order to have a reasonable number of boards, therefore also considering the practical implementation of the system and the physical footprint made up of the various components. Considering the need for at least 36 channels for the measurement of the slot currents, plus any other measures such as the voltage of the DC bus, the boards that mount less than 8 different A/D converters have been discarded. In this case,

the AD9249 has 16 channels per EVM (fig. 3.2). Consequently, 3 EVM were sufficient for the realization of the measurement system. Bandwidth is an equally important factor. A multiphase machine capable of operating up to 18 phases and with a configuration such as that under consideration requires a fine control of the harmonics [17]. As for the resolution, no restrictions were introduced by the specifications provided. A reasonable range of resolution bit values has been chosen. In our case, the AD9249 has a 14-bit resolution. The outputs of the conversion board are LVDS (low voltage differential signal, fig. 3.3) type. According to the standard in question, each output signal must therefore be interpreted as the difference of two single ended signals with dynamics ranging from 1.025V to 1.375V and average value equal to 1.2 V. Such information, also in relation to the information reported on the dasheet of the ZC702, allow to conclude that the electrical compatibility between the two devices is guaranteed.

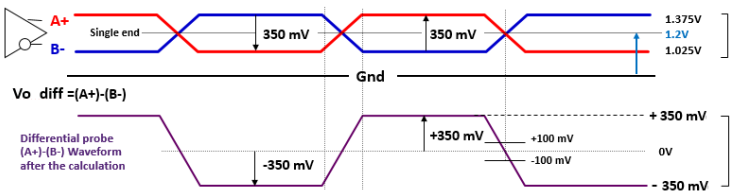


FIGURE 3.3: Low voltage differetnail signal electric levels

3.1.3 Communication protocol

The AD9249 needs a clock signal that can be internal or external. If several boards are used, if you use an internal clock rescaled by setting appropriate registers, it is necessary to provide an external synchronization signal to have simultaneous operation of the various cards. Having chosen to sample at a frequency of 10MHz it is sufficient to provide the same external clock signal to the various boards to have a simultaneous sampling. The AD9249 has a very simple operating principle. The internal or external clock signal is used to scan the sampling frequency. Each time the converter detects a rising edge of the clock, the input data on the various channels are sampled. Each individual sample, consisting of 14 bits, is not saved in a memory but is automatically sent to the outside. The communication of the AD9249 with the outside world is based on the serial sending of the samples of each channel. The clock that is supplied to the boards is internally multiplied by seven and is used to scan the sending via LVDS serial communication of the bits that

make up the single sample produced by each of the converters mounted on the board. In this way, in a complete clock period, the data is sampled and completely output on the serial line. The board provides, together with the sampled data, the signals preparatory for the synchronization necessary for the acquisition of these samples. These are 2 types of signals, also characterized by low voltage differential signal technology: FCO and DCO. The first is used to signal the beginning of a string of bits relating to a single sample. The second varies at a frequency 7 times greater than the clock frequency supplied to the board and signals the moment when the single bit can be acquired in correspondence with both a rising and falling edge. Figure 3.4 shows the timing diagram, extracted from the AD9249 datasheet [1], which describes the communication protocol of the board. A single AD9249 board

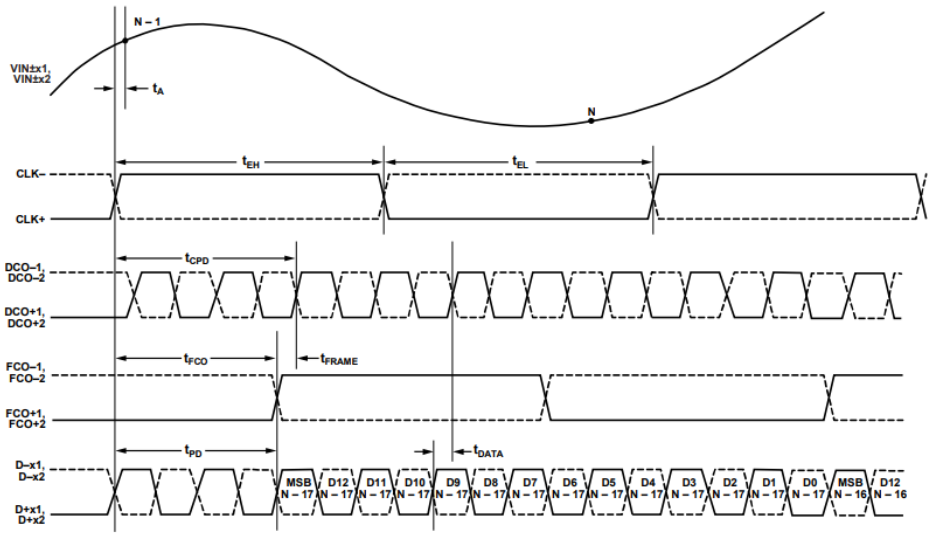


FIGURE 3.4: Communication protocol, timing diagram

is divided into two parts consisting of 8 ADCs each. Two signals are output, a DCO and an FCO, for each of the two sections. From an accurate analysis of the delays provided in the datasheet, it is possible to verify that, considering the frequency at which we operate the board, the use of the signals produced by only one of the two sections is sufficient. This reasoning is part of a pin-saving approach dictated by the need to fall within the limits, in terms of hardware resources, dictated by the FPGA used in the construction of our system.

3.1.4 Physical connection between FPGA and ADCs

The FPGA and AD9249 mount FMC type connectors for the outputs. Male type for the ADC, female for the FPGA. For the interfacing between the ADC

boards and the FPGA it was necessary to create a dedicated PCB capable of fulfilling the following functions:

- group the outputs of the three AD9249 (sampled data and synchronization signals) from three separate FMC connectors;
- sort the signals referred to in the previous point towards the two FMCs of the FPGA;
- routing a clock signal supplied by the zynq to the three adc boards (the clock signal is subsequently divided into three tracks each of which ends on SMA connectors compatible with the analog inputs of the ADC boards);
- connect the outputs of the zynq ZC702, dedicated to the production of the driving signals for the inverters, to the optical part which is responsible for transporting this information to the inverters.

3.2 Sample acquisition

3.2.1 Description of the structure created

The structure created for data acquisition and communication between FPGA and ADC is divided into two main sections: the clock generator and the sampling section. In the first section, two signals are generated starting from the zynq ZC702 clock. The first is a clock signal, at the desired sampling frequency, which will be routed to the ADC. The latter, as defined in the communication protocol, will sample the data at the rising edges of this clock. The other generated signal can be set at a frequency lower than or equal to the clock supplied to the ADC and is a signal that is used by the sampling section for the acquisition of the samples. The operation of the ADC provides that each time the clock is received, the data on the various channels are sampled synchronously and the samples of each channel are automatically sent in parallel via serial communication. The decision to operate the ADC at a certain frequency does not imply that there is always the need to acquire data at this frequency. The system created therefore allows to drive the ADC so that samples at a certain frequency and to set a frequency equal to or lower to which you want to acquire the data. The second signal generated by the clock generator will be the one capable of indicating to the sampling section the instant in which to start the data acquisition mechanism. As highlighted in section 3.1.3, the ADC sends synchronization signals indicating when the data on the serial line can be considered valid and therefore acquired. The synchronization signals DCO and FCO can be used directly as clock of a structure that

acquires the bits on the serial line. In that case, however, it could occur that the information is corrupt due to noise or disturbances related to electromagnetic compatibility. In the structure built, it was therefore decided to treat the DCO and FCO as normal data, acquired and sampled using the FPGA clock. Using synchronization signals as data acquired through normal flip-flops reduces the risk of malfunctions. If the signals are altered, they are sampled and kept until the next sampling, avoiding that they behave like a clock that starts certain operations every time a variation occurs. This decision allows for a more robust system at the expense of performance as a limit to the maximum operating frequency is introduced. The DCO signal is in fact generated by the ADC at a frequency equal to 7 times that of the clock. If you want to treat the DCO as a data, it will be necessary to acquire it on the FPGA. Considering therefore the frequency of 200MHz of the clock on the ZC702 it is obtained that 14.2MHz is roughly the upper limit for the clock that is sent to the ADC and therefore to sampling, in fact: 100MHz/7≈14.2MHz.

3.2.2 RTL view

The structure created is instantiated three times since only three A/D boards are used to measure the 36 currents flowing in the motor (one for each slot). For each of these there will be 12 channels for sending the bits that make up the samples via serial communication. In the same way it is necessary to acquire on FPGA the synchronization signals that each of the ADC boards sends. In figure 3.5 it is possible to observe a first scheme to get a general overview of the structure built. The structure in detail is shown below, remaining on an RTL abstraction level, and the operating principles that regulate the clock generator and the sampling section. The clock generator is divided into two blocks dedicated to the generation of two signals at different frequencies. Both frequencies can be changed by changing a parameter that indicates how many FPGA clock edges (200MHz) must be counted in order to rescale the clock at a lower frequency. The same structure is then repeated for both blocks and is as follows:

- Counter
- Comparator
- FSM

The counter is constantly enabled and each time the rising edge of the clock occurs it increases the value of its output signal by one. This output goes to the input of a comparator. The comparator has two inputs and one output. The two inputs consist of the counter output and a constant that is set according to the frequency of the signal to be obtained. The function of this block is

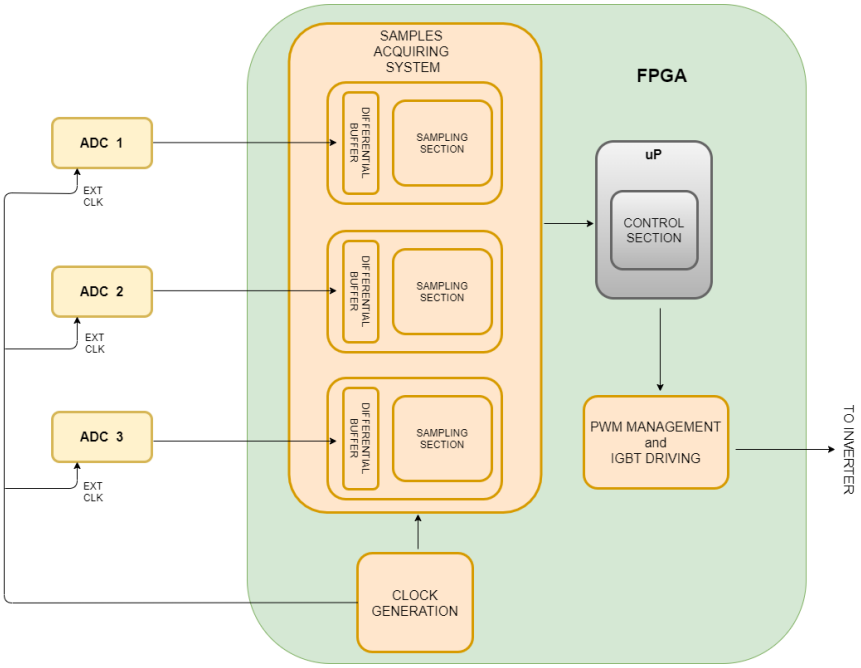


FIGURE 3.5: Samples acquiring system: overallview

to assert the output signal for a clock stroke when the comparison between the two inputs shows that these are the same. The output product data is sent to the finite state machine which, based on the outcome of the comparison, manages the counter by resetting it or letting it operate normally. Finally, the FSM does evolve between two states. In one state the signal generated by the FSM will be equal to 1, in the other it will be imposed equal to 0. In this way we describe a signal that alternately stands at 0 and 1. The FSM decides whether to stay iterating over the same state or whether to evolve in the other state according to the signal that is produced by the comparator. In this way it is sufficient to vary the input constant to the comparator to vary the width of the two sections.

The sampling section can be considered as the set of two sections: synchronization chain and data chain. These two sections dialogue with a dedicated FSM that guarantees the correct passage of control signals with adequate timing. The synchronization chain consists of four flip-flops connected in series two by two. The first pair is connected in input to the DCO signal while the other to the FCO. The series connection of two flip-flops allows the two most recent samples to be available simultaneously. In this way it is possible to determine a rising or falling edge of the DCO simply by detecting the discontinuity between the outputs of the two flip-flops. Similar reasoning can be done for the FCO signal. Finally, there is a 4-bit counter that is enabled by the FSM every time a rising or falling edge is detected on the

DCO. In this way, it is possible to keep track of the bits that are acquired and once the reception of 14 bits is detected, the shift-register acquisition process is interrupted and the counter is reset. In the data chain we find a structure consisting of 5 flip-flops and a shift-register connected as in figure 3.7. The 5 flip-flops are always enabled, this means that they sample the input data each time a clock edge is detected. The use of 5 flip-flops is explained in section 4.2.3 and is essentially due to the fact that a certain number of clock strokes are required before the synchronization signals are detected and the commands to manage the acquisition of the data are provided. The output of the last flip-flop is connected in input to a shift register on 14 bits. The shift-register is enabled by an enable signal asserted by the FSM every time that, after detecting a rising edge of the FCO, a variation of the DCO is detected. In figure 3.6 and 3.7 it is possible to observe a representation at RTL level of the two blocks just described.

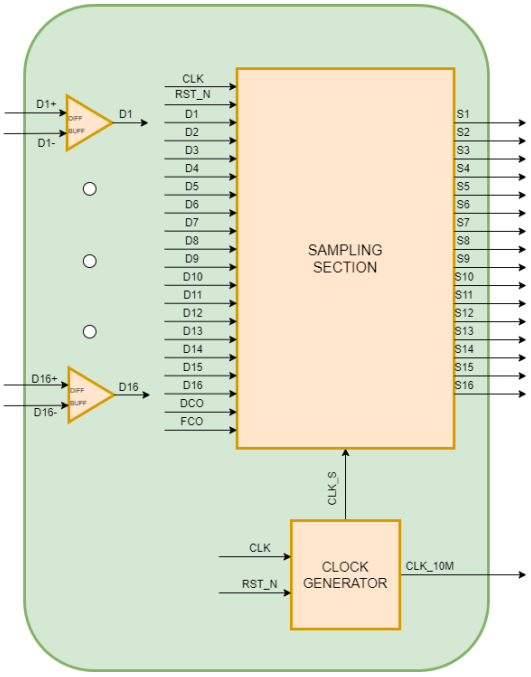


FIGURE 3.6: Sample acquiring system, high level RTL view

The fundamental element for the management of the sampling section is the FSM which appropriately drive all the blocks. The operation of this state machine can be described as follows:

1. Waiting for a signal indicating when to start the bit acquisition on the serial line;

2. Waiting for a rising edge of the FCO signal;

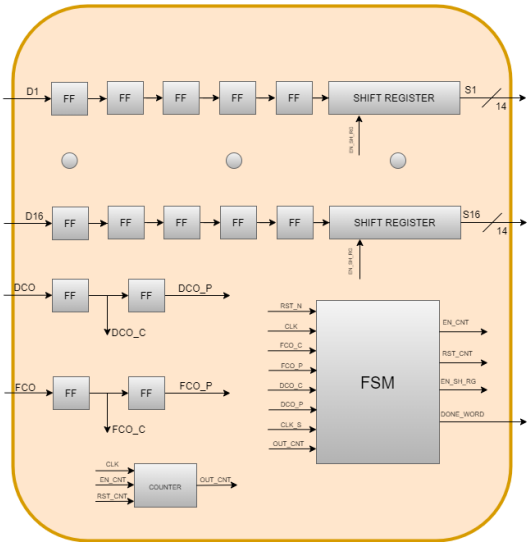


FIGURE 3.7: Sampling section, RTL view

3. Waiting for a change in the DCO signal;
4. Enable shift-register;
5. Verification of the acquisition of a complete word (14 bit).

The FSM Control Diagram of the built machine is shown below (fig 3.8).

3.2.3 Simulation results

Once the code for the clock generation and sample acquisition sections was created, a simple TB was created to check its operation before moving on to the actual operation check (in details in 6.1). For the simulation, it was assumed that the sent data and the synchronization signals were sent consistently with what was stated in the datasheets. With this in mind, a simulation was performed with perfectly synchronized data and DCO and then a second simulation in which the data were sent in advance and late considering the minimum and maximum delays that are declared in the datasheet. From the simulations it can be verified how the information is correctly reconstructed in all the imposed conditions. As explained previously, the system provides that the ADC samples each time it receives the 10MHz clock, however leaving the possibility of acquiring the samples at a lower or equal frequency. The frequency with which the samples are acquired is dictated by the second signal that is generated in the clock generator. The simulations were carried out in different conditions, assuming relaxed or not relaxed conditions on the latter signal. The simulations with the introduction of delays were carried out using 3 channels at a time. In this way the synchronization signals

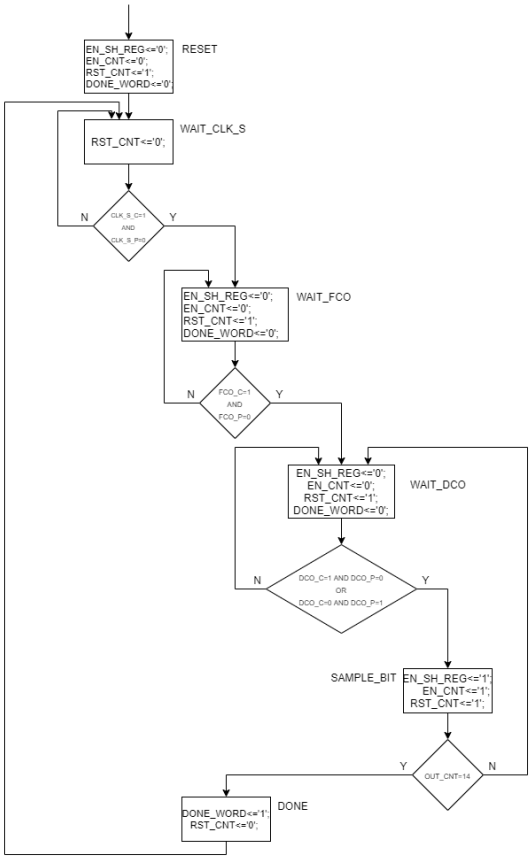


FIGURE 3.8: Sampling section. FSM chart

DCO and FCO with maximum delay and advance declared in the datasheet have been simulated. The delay simulations were made for acquisition at low and high frequencies. In detail, the conditions used for the simulations were the following:

- ideal case - no delay introduced
- introduction of delays with 8kHz acquisition
- introduction of delays with 5MHz acquisition

In all the above conditions, the correct functioning of the system was verified. Practical verification with dedicated TB is described in 6.1.

Chapter 4

PWM signals generation

4.1 Carrier Based PWM

As for single-phase inverters, in three-phase inverters with pulse-width modulation the purpose is to shape and control the amplitude and frequency of the three-phase output voltage, having a substantially constant input voltage Vd. To have balanced three-phase output voltages in a three-phase PWM inverter, the same voltage with the triangular shape is compared with three sinusoidal control voltages that are 120° out of phase with each other (fig. 4.1) [5].

In the practical implementation, integrated circuits are used for the construction of the inverters. These are 3-phase modules made up of 6 IGBT that make the 3 legs of the inverter. Having 36 slots independently driven, it is evident that 12 modules will be needed for the complete driving of the machine. Unlike a classic three-phase inverter described in literature, in which therefore the reference of each one used to generate the control signals of each leg is out of phase by 120 degrees, in the structure created there will not be this type of relationship between the 3 legs of one inverter. However, the flexibility obtained from the motor structure is based on the concept that different slots are considered virtually connected in series as they are driven so as to obtain the same current in a slot belonging to the same phase. A similar reasoning can be done for slots belonging to the complementary phase. Each configuration can therefore be described as many suitably driven three-phase systems. For example, in the 3-phase 2-pole configuration, neglecting considerations on interleaving, it would be a system equivalent to a simple three-phase. The number of equivalent inverters virtually used depends on the configuration. Consequently, the 9-phase 2-pole configuration, in spite of the 12 three-phase modules used, can be described in the first approximation as the combination of 3 three-phase inverter. The foregoing considerations hold in mind that all power modules are physically connected to the same DC bus. It can therefore be seen that in any case the one used is therefore a sinusoidal PWM modulation.The line voltages have the same continuous component measured with respect to the negative terminal of the DC-bus.

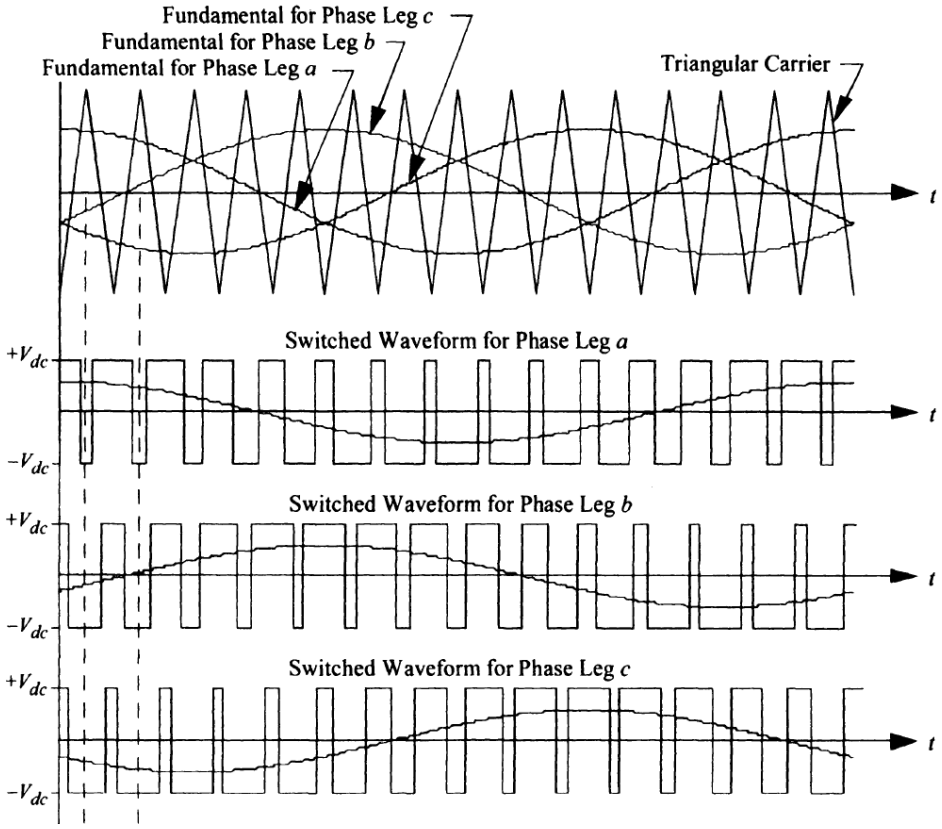


FIGURE 4.1: Sinusoidal carrier based PWM

This means that in calculating any line to line voltage there will be no continuous component [6]. The spectrum for the modulation chosen in the case of ma = 0.8 and mf = 15 is shown below(fig. 4.2).

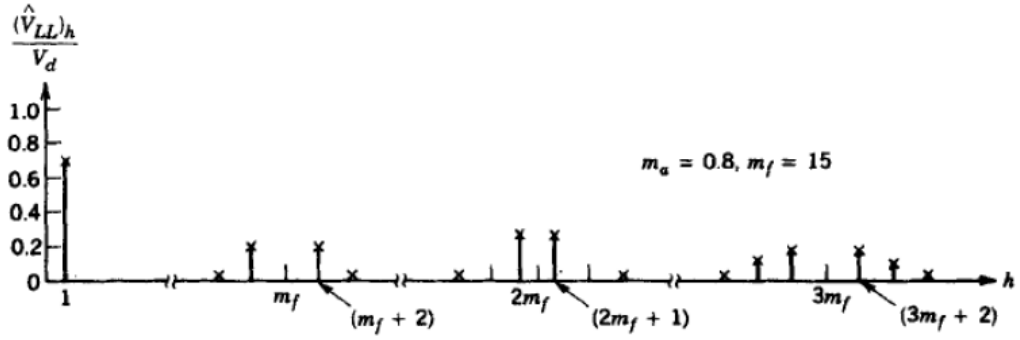


FIGURE 4.2: Line to line voltage spectrum in sinusoidal PWM

Mf indicates the frequency modulation index and is given by the ratio

between fsw and f01 (reference signal frequency). With appropriate precautions it is possible to alter the spectrum in order to reduce or eliminate some components. In three-phase inverters, only the harmonics in the connected voltages are affected. Considering only the mf harmonic (the same consideration can be applied for odd multiples), the phase shift between the mf harmonic of two line voltages is equal to 120°*Mf. This phase shift is zero if mf is odd and is a multiple of three. It follows that the mf harmonic in the line voltage is zero [6]. Similar reasoning can be done for the suppression of harmonics that are odd multiples of mf if an odd and multiple of three value of mf is chosen. In this way it is found that some of the dominant harmonics in a single-branch inverter can be eliminated from the connected voltage of a three-phase inverter.

4.2 Mapping of slots by configuration

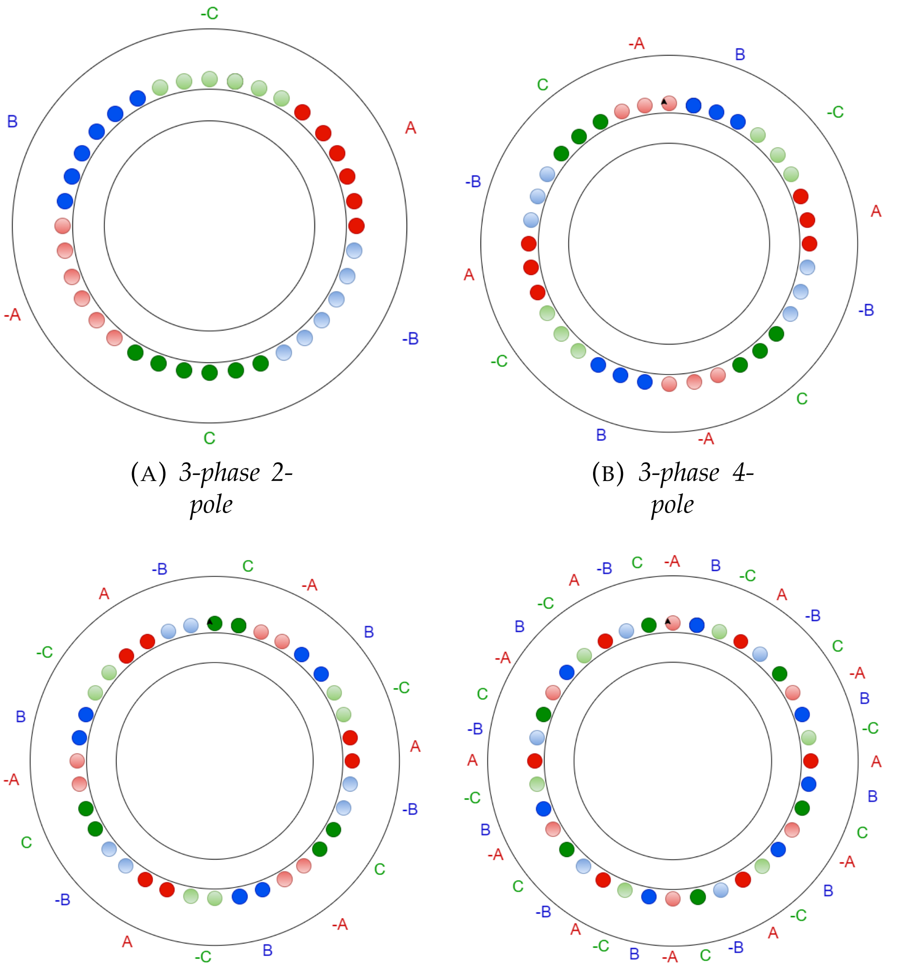
Before proceeding with the construction of the structure capable of generating the signals for the PWM, it was necessary to define the configurations in which the machine can operate. For the mapping, the number of slots available and the minimum physical limits on polar pairs were taken into consideration. The mapping process passes through the choice of the phases and poles to be obtained, thus defining a parameter for each configuration: the number of slots per pole per phase. A precise and more complicated control of the machine would allow to map configurations with number of slots per pole per phase non-integer . For a first phase of the project it was considered appropriate to limit to the configurations with an integer value of slots per pole per phase. In light of what has been outlined, the remaining possible configurations are 9:

- m3 p2 (6 slot per pole per phase);
- m3 p4 (3 slot per pole per phase);
- m3 p6 (2 slot per pole per phase);
- m3 p12 (1 slot per pole per phase);
- m6 p2 (3 slot per pole per phase);
- m6 p6 (1 slot per pole per phase);
- m9 p2 (2 slot per pole per phase);
- m9 p4 (1 slot per pole per phase);
- m18 p2 (1 slot per pole per phase).

Once the possible configurations were defined, the mapping has been performed. From the previous list it can be seen that all possible configurations are characterized by a number of phases equal to or multiple of 3. This facilitates us in some situations where, due to the geometry of the machine, redundant configurations would be obtained. An example is certainly the 6-phase case. In fact, a configuration with 6 phases cannot be realized with the same procedure with which the slots are assigned for a three-phase motor since it would be that a generic phase should be assigned to the slots to which the complement of a phase already assigned corresponds(1.3). In these cases, the machine is mapped as two three-phase systems out of phase with each other. The phase angle between the two systems is calculated as [12]: $360°/(Nmp)$, where N is the number of identical m-phase sets and p is the number of poles. In the case of m6p2 and m6p6 (fig. 4.4) therefore the two three-phase systems are out of phase with each other by 30 degrees and 10 degrees respectively. The same problem occurs in the case m18 p2 in which one proceeds by assigning the slots to six three-phase systems out of phase by 10 degrees. The graphs of the slot assignments for each configuration are shown below (figures 4.3, 4.4, 4.5, 4.6).

4.3 Interleaving and benefits

Pulse-width modulation (PWM) is the ground for control in power electronics. The vast majority of semiconductor power devices in power electronic circuits are controlled by pulse-width modulation signals of various forms. The fast rising and falling edges of the pulse-width modulation pulses ensure that the power semiconductor devices are turned on/off as quickly as possible to minimize the switching transition time and the associated switching losses. Pulse-width modulation can take different forms. When multiple PWM converters are connected in parallel with current sharing, it is advantageous to operate all converters at the same switching frequency but with controllable phase shift these PWM signals. This technique is referred to as interleaving PWM and has been widely used in power electronics [6],[7]. Interleaved techniques provide many benefits for power converters, such as improved efficiency with current sharing, reduction of output inductor with reduced inductor current ripples [14], [3], reduction of input DC-bus capacitor [15] with reduced input current ripples, and reduced common-mode voltage. FPGA-based digital control technique with its high accurate and programmable timing control capabilities exhibits significant advantages over conventional analog control technique when applying to multi-phase interleaved PWM inverter to achieving high power density inverter modules.



(A) 3-phase 2-pole

(B) 3-phase 4-pole

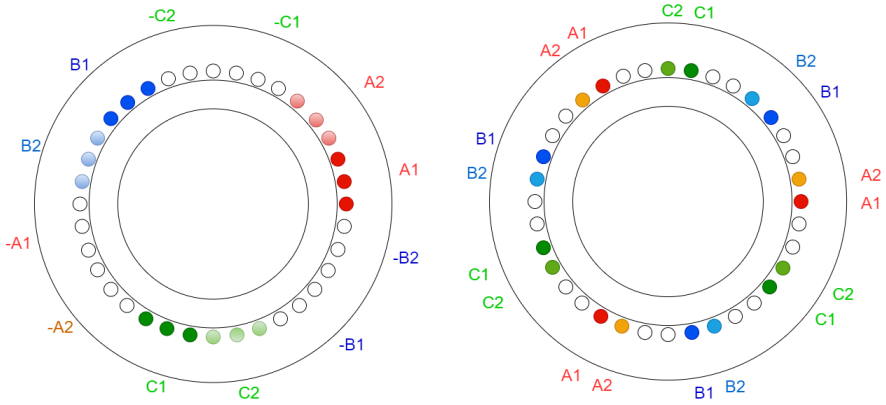
(C) 3-phase6-pole

(D) 3-phase 12-pole

FIGURE 4.3: Slot mapping for 3-phase configurations

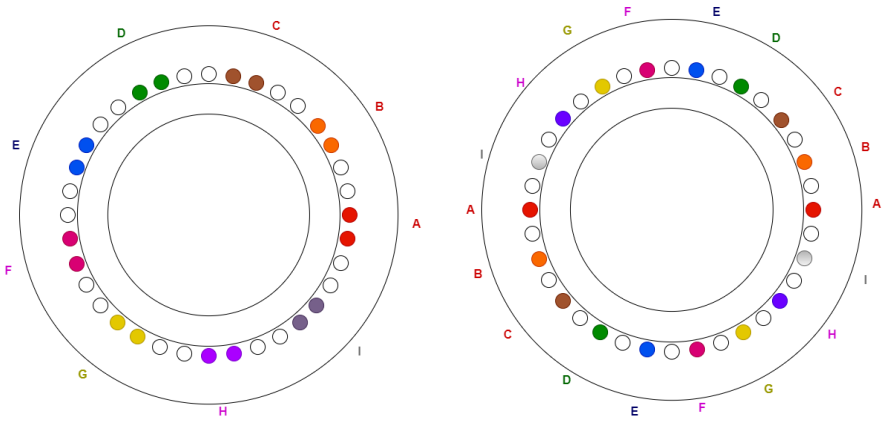
4.3.1 Interleaving inside the phases

In the literature it is easy to find information on the possible techniques that can be adopted to implement interleaving and the related advantages. In most cases it refers to an interleaving between the carriers of one phase and another. The nature and geometry of the engine under study, however, allows each slot to be driven independently beyond the fact that two or more slots, based on the current configuration, refer to the same phase. This allowed to carry out a further step, going to implement a finer interleaving internal to each phase. The driving signals of each leg of the inverters referring to the same phase will be derived from the comparison with the same reference and the carriers no longer the same but in turn out of phase. Below are the diagrams in which the association between a slot and the carrier



(A) *6-phase 2-pole* (B) *6-phase 6-pole*

FIGURE 4.4: Slot mapping for 6-phase configurations



(A) *9-phase 2-pole* (B) *9-phase 4-pole*

FIGURE 4.5: Slot mapping for 9-phase configurations

used to drive it when the configuration changes is defined (figures 4.7, 4.8, 4.9, 4.10):

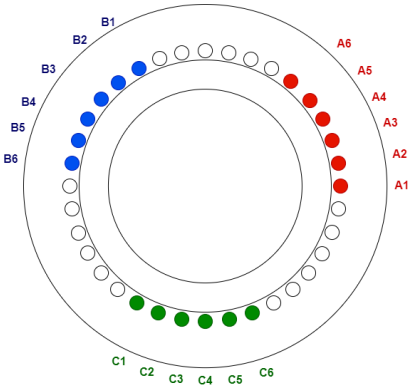
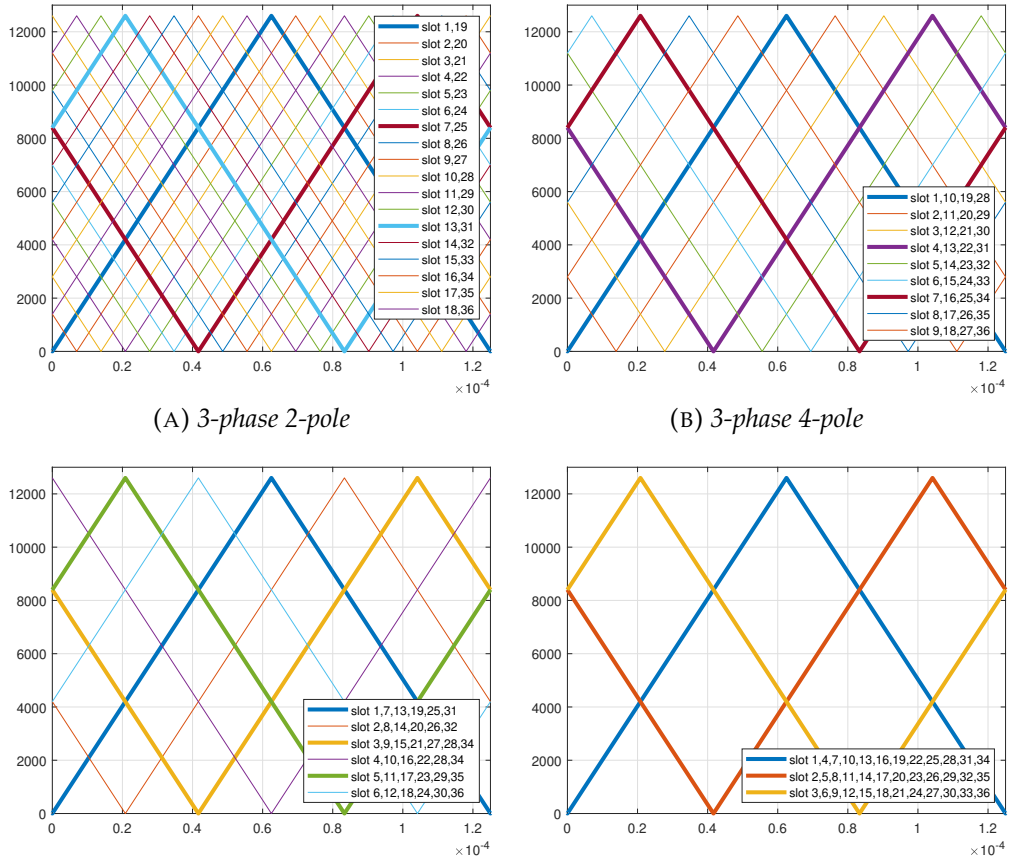


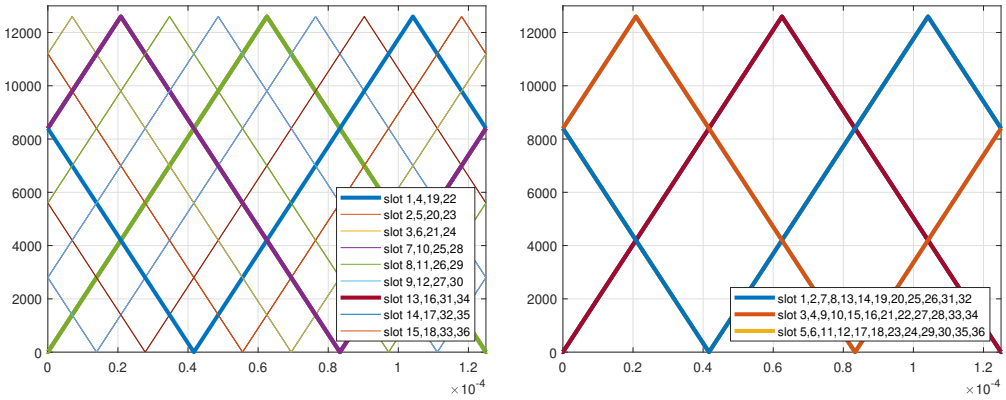
FIGURE 4.6: Slot mapping for 18-phase 2-pole configuration



(A) *3-phase 2-pole* (B) *3-phase 4-pole*

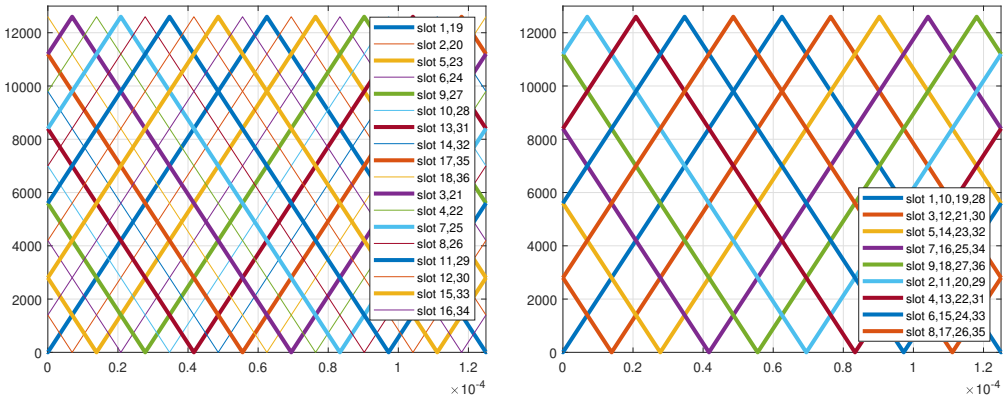
(C) *3-phase 6-pole* (D) *3-phase 12-pole*

FIGURE 4.7: Carrier to slot association in 3-phase configurations



(A) *6-phase 2-pole* (B) *6-phase 6-pole*

FIGURE 4.8: Carrier to slot association in 6-phase configurations



(A) *9-phase 2-pole* (B) *9-phase 4-pole*

FIGURE 4.9: Carrier to slot association in 9-phase configurations

4.3.2 Benefits

An interleaved inverter drive can also significantly reduce the size of the dc-link capacitor, and thus improve the system reliability [15]. The input current of the inverter, i , consists of a dc component I with related current harmonics resulted by the modulation frequency fm and the switching frequency fsw . The inverter input current can be expressed as [7]:

$$i_{inverter}(t) = I_{dc} + \sum_{k=0}^{\infty} \sum_{n=1}^{\infty} I_{n,k} sin[2\pi(nf_{sw} \pm kf_{sw})t + \alpha_{n,k}] \tag{4.1}$$

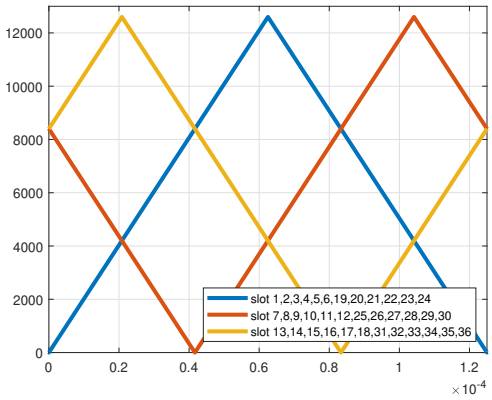


FIGURE 4.10: Carrier to slot association in 18-phase configuration

The interleaving technique can reduce both the output and input current ripples of a power converter. By controlling the interleaving angle some selected harmonics can be reduced or eliminated. It is important to notice that, the current ripples of the inductor do not always be eliminated by phase-shift of the carrier signals and may cause larger ripple magnitude because the superposition of the current ripples peak value will increase in certain condition. With the proposed implementation, the quality of the line-to-line output voltages is improved owing to the fact that switching occurs exclusively between adjacent levels. Because of the improvement in terms of line-to-line voltages [3], better THD values are achieved [7], which can lead to a reduction in the output filtering requirements.

4.4 Description of the structure implemented

The PWM section is divided into several levels. Below is a diagram summarizing the hierarchy of the structure built(4.11):

- Carrier generator
- Reference generator
- Comparator

More externally we find three fundamental blocks: a block capable of carrying out the 36 carriers for the 36 engine slots (Carrier generation), a block capable of producing the references for the phases (Referencies generator) and finally a block capable of carrying out the comparison between carrier and modulating and producing so square waves for pwm modulation (Comparator).

The most interesting and articulated structure consists of the block for the generation of the carriers. The latter in turn is divided into two levels (4.12):

- Generic Slot
- Carrier parameter generator

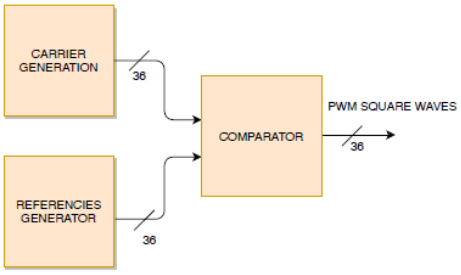


FIGURE 4.11: PWM section overview

The generic slot is the block that takes care of generating and managing the carrier for each slot based on the current configuration. It communicates with the carrier parameter generator which has the function of passing the parameters for the generation of the carrier during normal operation.

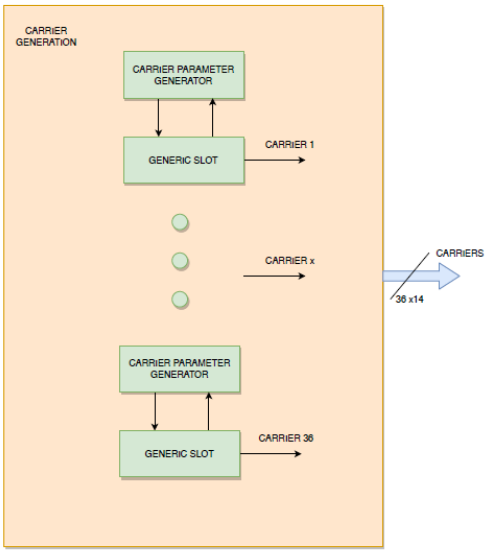


FIGURE 4.12: Carrier generation, block diagram view

The generic slot is in turn divided into three functional blocks(4.13):

- Carrier generator

- Configuration handler
- Transition handler

The carrier generator represents the elementary block, receives parameters and on the basis of these generates the carrier. The configuration handler receives the current configuration from the control and manages the parameters that the carrier parameter generator sends to the generic slot. The CH also takes care of detecting if a transition is requested by the control and starts the transition handler to manage a transition. The FSM implemented in the CH is shown in 4.14. The transition handler receives information on the current configuration and on what will be the new configuration, evaluates the type of transition and on this basis processes the parameters to be passed to the carrier generator in order to implement a gradual transition of the carrier.

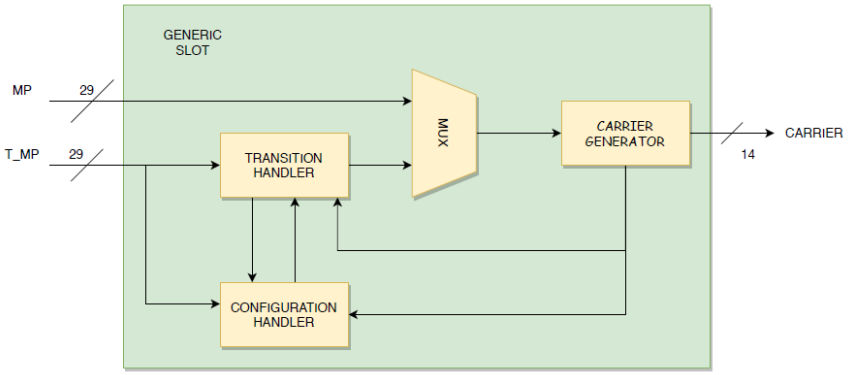


FIGURE 4.13: Generic slot, block diagram view

In an implementation on FPGA the carrier is obviously described by a binary number that evolves over time, varying from a maximum value to a minimum value. These limits are introduced by the switching frequency. The clock available on the FPGA is 200MHz and if you want to approximate a carrier with a variation as linear as possible (therefore by increasing or decreasing the carrier value by one bit with each clock stroke) it is obtained that an 8KHz carrier is described on a range 25000 points:
200MHz/8KHz=25000.
To implement interleaving, considering the cases in which there is the maximum number of different carriers per configuration equal to 18, it is obtained that the number of points with which a carrier is described must be a multiple of 18. It is therefore obtained that the achievable carrier will not be exactly at 8KHz as the first integer that can be obtained is equal to 25200 points which corresponds to a signal of about 7.94KHz. Referring to the graph in which the various carriers for each configuration are shown (fig. 4.7), it is clear that, in the face of interleaving, the carriers are out of phase and considering

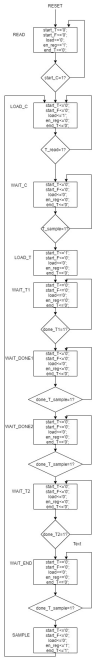
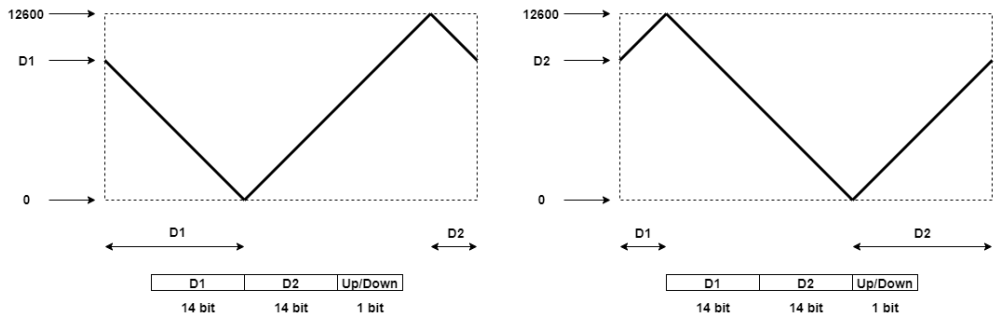


FIGURE 4.14: Configuration handler, FSM chart

an entire switching period they must be described differently. Considering the nature of the carrier to be created, a single carrier can be described with three parameters. Excluding some particular cases, a carrier will always be described in three different sections. A first section of variable duration and positive or negative slope, a second section in which a maximum variation of the carrier is covered and finally a section with the same initial slope with a duration equal to the maximum of the variation minus the duration of the first section. As explained in fig. 4.15 the first two parameters contain information on the duration of the external sections and the offset and the third indicates the slope.

4.5 RTL view

In fig. 4.16 is shown the register transfer level view of the 'generic slot' implemented in order to emphasize the transfer of parameters between the TH and the CH to and from the carrier generator. After reading the configuration, the configuration handler makes sure that the CG receives the corresponding parameters and forces the loading of these parameters on the CG via the LOAD signal. Once the parameters are loaded, the CG communicates to the CH that it has correctly acquired the information for generating the PWM signals according to the current configuration(T_READ). The CH, when a transition request is detected, informs the TH with the START_T signal. The TH waits



(A) *Down-Up-Down Carrier*

(B) *Up-Down-Up Carrier*

FIGURE 4.15: Carrier structure, Up and Down structures

for the DONE signal from the CG to force the loading of the new parameters at the beginning of a new switching period. This last operation is repeated until the TH detects that the generated carrier is close enough to the carrier that characterizes the new configuration.

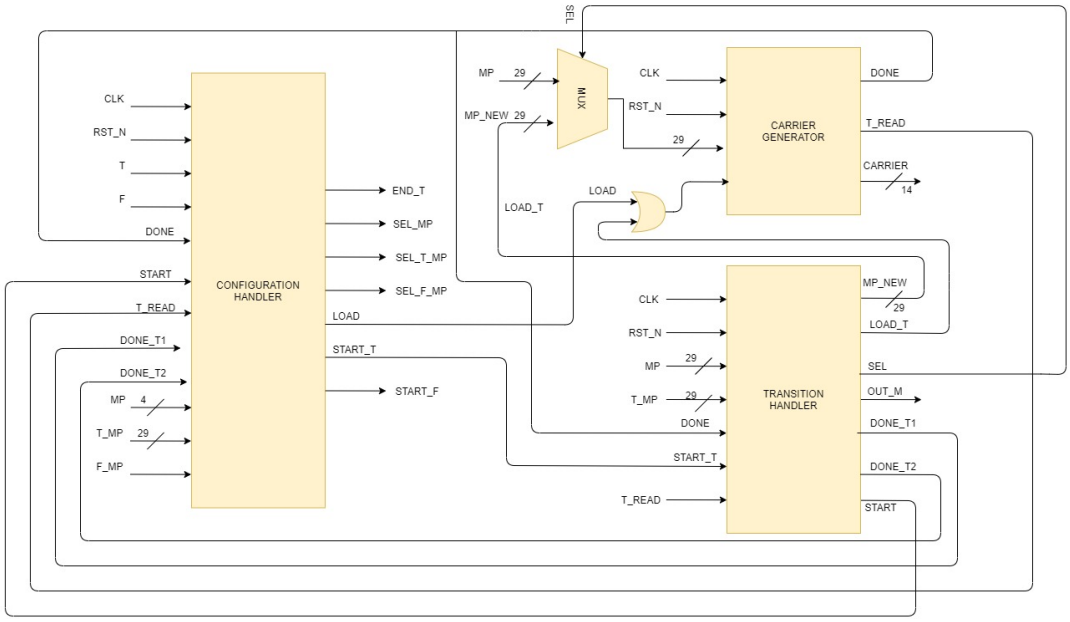


FIGURE 4.16: Generic slot, RTL view

4.6 Mechanism of configurations transition with smooth variation

Particular attention was paid to managing the transitions between the various configurations. A variation in the configuration can lead to a significant change in the electrical quantities to which a slot is subjected. Implementing a transition from one configuration to another without paying attention to how this occurs can create problems during the transient and give rise to considerable stress for the various components. Furthermore, the machine control will take some time to process the input measurements and produce the new commands according to the new configuration. In this context, a transition mechanism is created which distributes the configuration variation over a certain period of time. In practice, a structure is implemented which is able to implement the smoothest possible variation of the carriers. At the same time, a similar system is implemented for the generation of sinusoidal references. In fact, it may occur that a given sinusoid different in phase and or amplitude from the sinusoid which is associated with the same slot is initially associated with a slot following the transition to a new configuration. To gradually manage the reference transition, a new waveform is created by adding the two sinusoids weighed by two coefficients that vary linearly over time from 1 to 0 and from 0 to 1. In this way, the two sinusoids are weighed ensuring the continuity of the reference and having the opportunity to make the transition over an arbitrary time frame. The two operations described above, suitably coordinated, allow for a smooth transition of the machine configuration. A system has been developed that is able to evaluate, based on the transition, the variation of the offset between the carriers before and after the transition and to distribute the variation of the offset gradually over a certain number of switching periods. A dedicated block, the Transition Handler, takes care of managing the transition. TH is divided into several blocks:

- Transition type
- Standard transition
- Up to down transition
- Down to up transition
- Multiplexer

The Transition Type detects the type of transition and drives an internal multiplexer to the TH in order to provide the carrier generator with the right parameters based on the type of transition. This approach is necessary by

remembering the nature of the carrier generator. The latter, in fact, needs information on 29 bits to generate a carrier.
The operation principle of the transition handler is summarized by the FSM shown in 4.17 and explained below.

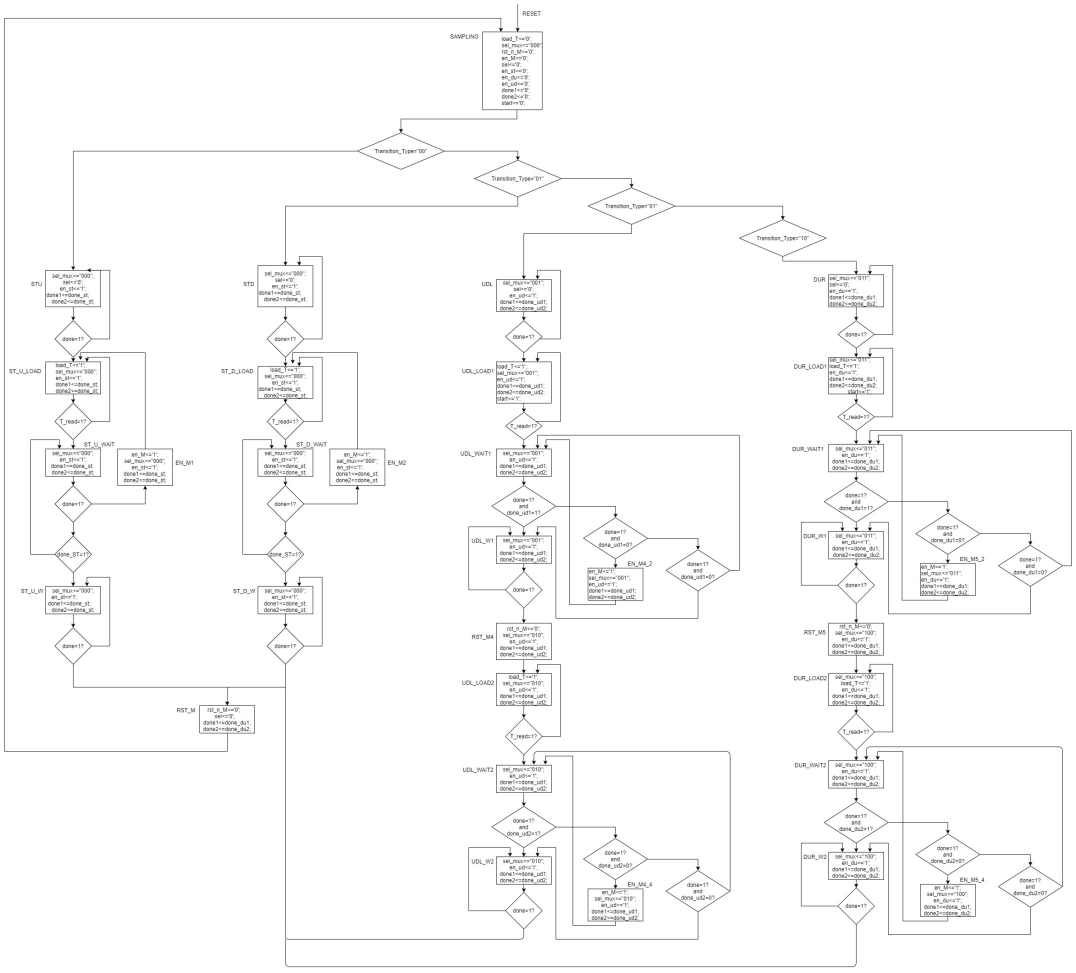


FIGURE 4.17: Transition handler, FSM chart

The TH receives two vectors containing information on the current configuration and on the one to which one wants to pass. The machine waits until the signal that triggers the transition process is detected. This signal is the START_T which is sent by the Configuration Handler which constantly reads the information sent by the processor, and therefore by the control, to the programmable logic of the FPGA. Once the start signal is received, the TH waits for the carrier generator to send a done signal. This done signal is sent at the end of the cycle which describes a switching period. In this way you can be sure that the transition always starts from the same point giving the possibility to easily process the parameters to be passed to the carrier

generator to make the transition. Immediately after the arrival of the start_t the machine evaluates the information provided by the transition type and on the basis of these transits into the corresponding wait state. By evaluating the waveforms of any carrier and considering the principle of operation of the carrier generator, it is possible to understand how it is necessary to operate differently according to the initial and final configurations. For example, in the transition from the m3p2 configuration to the m3p4 configuration the carrier associated with slot 3 will see a variation of its offset but the trend will remain the same, i.e. the slope will first be negative then positive and finally negative. Considering for the same transition, the carrier associated with slot 8 shows how the trend before and after the transition changes drastically (fig. 4.18). In the light of all this, it is evident that it is necessary to

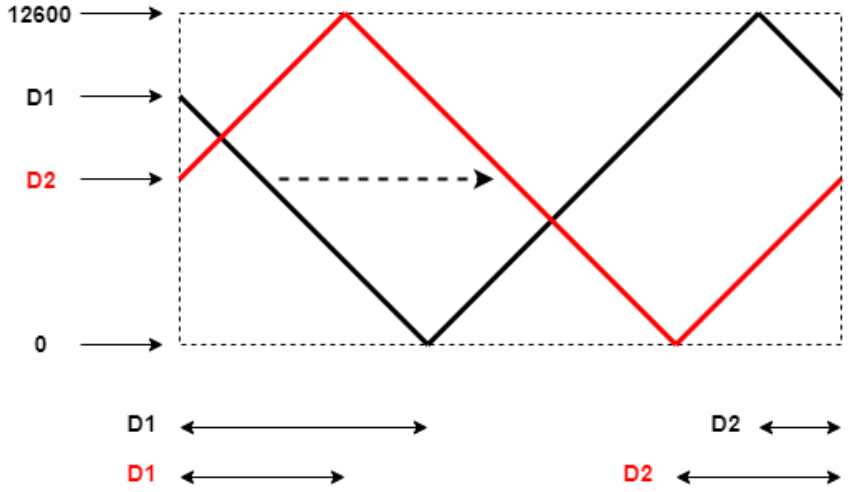


FIGURE 4.18: Carrier transition, m3p2 to m3p4, slot 8

detect the type of transition and to proceed in a different way on the basis of this. Everything can be traced back to the fact that the last bit of the vector that characterizes each carrier indicates the trend over time (for example, first positive then negative and finally positive slope) of the triangular wave. The transition type will then evaluate the last two bits of the vectors of the two configurations and provide the state machine in the TH with the information necessary to manage each type of transition. Transitions can be handled in four different ways. We have a standard transition in which there is no change in the trend but only in the offset of the triangular wave. This type of transition consists of two sub-categories, based on the positive or negative variation of the offset. Then there are two other types of transition, in which the trend varies. These two transitions, hereinafter UD and DU (up to down and down to up refer to the trend in the first section of the triangular wave)

are managed in two main processes. In practice, it is as if the single transition were divided into two smaller transitions, each of which is managed as a standard transition. Blocks dedicated to each type of transition have the task of detecting the moment in which the trend of the triangular wave must be reversed by generating control signals that will make the state machine evolve appropriately passing from the first standard transition cycle to the second. Referring to the transition m3p2 to m3p4 and once again considering the carrier associated with slot 8, we are referring to the states DUR, DUR_LOAD1, DUR_WAIT1, DUR_W1, EN_M5_2 and RST_M5 for the first part of the transition in which the initial trend is maintained . In this way the carrier maintains a down-up-down trend in which the offset gradually varies period after period. Once the offset has been varied up to the point where it is necessary to reverse the trend, the FSM will evolve into the states DUR_LOAD2, DUR_WAIT2, DUR_W2, EN_M5_4 and finally RST_M.

4.7 Simulation results

The carriers produced in the PWM section are displayed using the 'analog waveform' setting offered by the simulator in Vivado. In this way the numerical information that constitutes the carrier is reconstructed giving the possibility to have a comparison with the trend of an equivalent analog triangular wave. Below are two figures from two different simulation both related to the carriers generated ad associated to the slots 1 to 6. Fig. 4.19 contains the carrier generated while the machine is running in the 3-phases 2-poles configuration. It is possibile to have a qualitatively feedback on the gradual phase-shift between the carriers associated the phase A. A more complite view is offered in fig. 4.20. This latter represents the carriers associated to slots 1 to 7 when the MPM is made run in the 3-phases 6-poles configuration. It's possible to see that the behavior obtained is the one described in 4.3.1. The first six carriers are related to the phase A,B and C and the are shifted and distributed over an entire switching period. Finally, from the seventh carrier the behavior is repeated as for the previous carriers. In fig. 4.21 it is possible to observe the simulation result as regards the output of the PWM section for the configuration 3-phases 2-poles. In particular it's plotted the behaviour of phases A,B and C zooming in to appreciate the implementation of the interleaving inside each phase. Fig. 4.21 is obtained from a longer (over 20ms) simulation that allows to verify the correct operation of the PWM section. Fig. 4.22 offers the possibility to check the phase shit between phase A,B and C while the machine runs in the 3-phase 2-poles configuration.

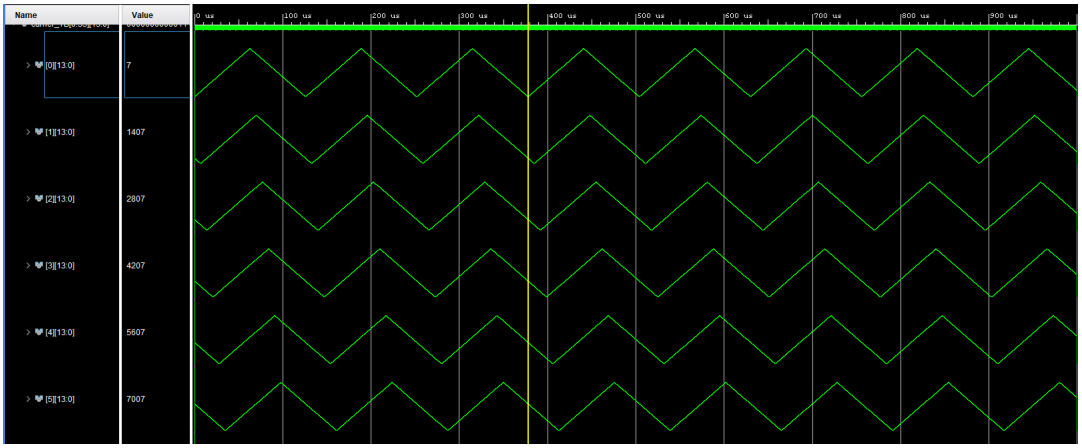


FIGURE 4.19: Carriers with interleaving, 3-phases 2-poles

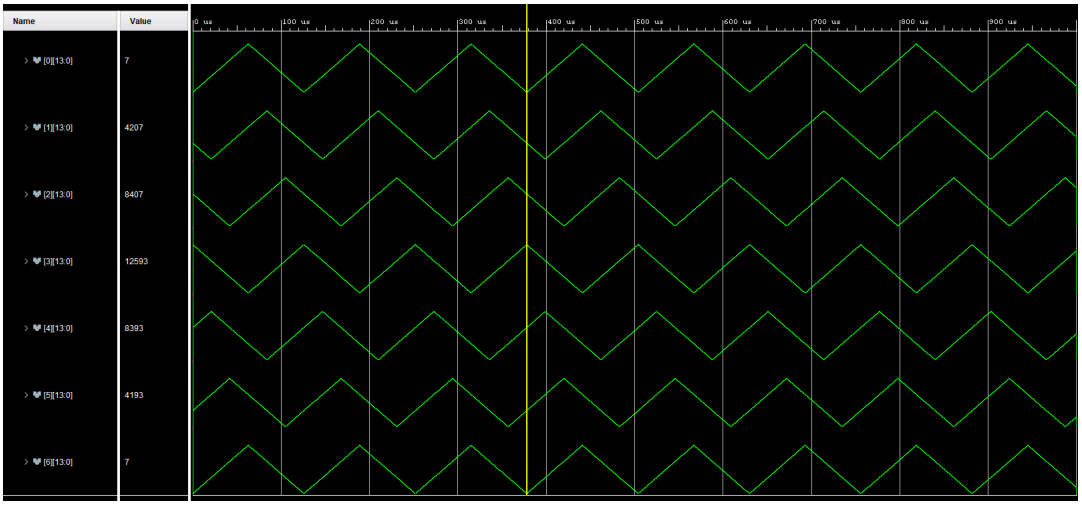


FIGURE 4.20: Carriers with interleaving, 3-phases 6-poles

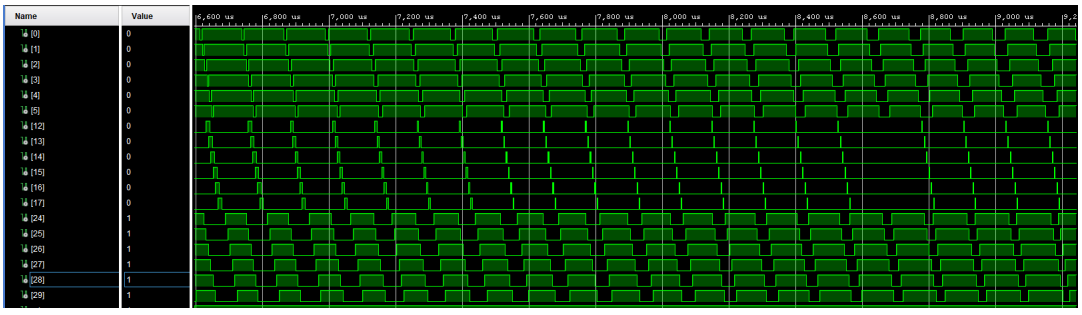


FIGURE 4.21: PWM waves with interleaving, 3-phases 2-poles

The waveforms of the carriers and the PWM signals that are obtained by

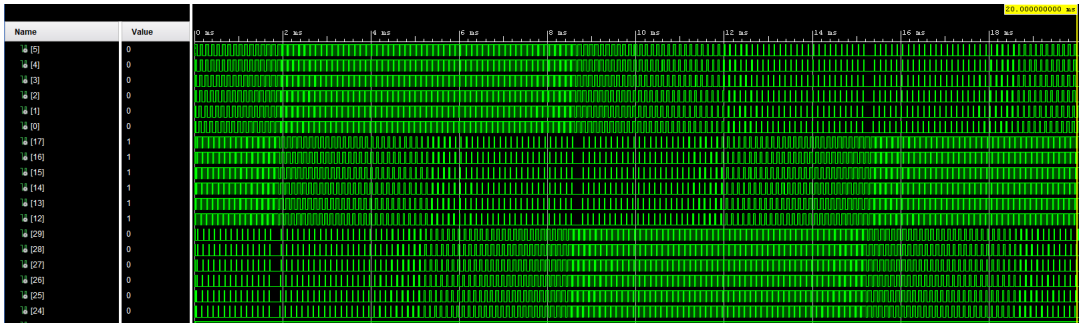


FIGURE 4.22: PWM waves, 3-phases 2-poles phase A,B and C

simulating a transition from the configuration 3-phase 2-pole to the configuration 3-phase 12-pole as regards the slots 2 to 6 are shown in fig. 4.23. In transition of fig. 4.23 the parameters are set so that the transition is qualitatively recognizable. In normal use, the transition is distributed over a much greater number of steps, making the variation smoother.

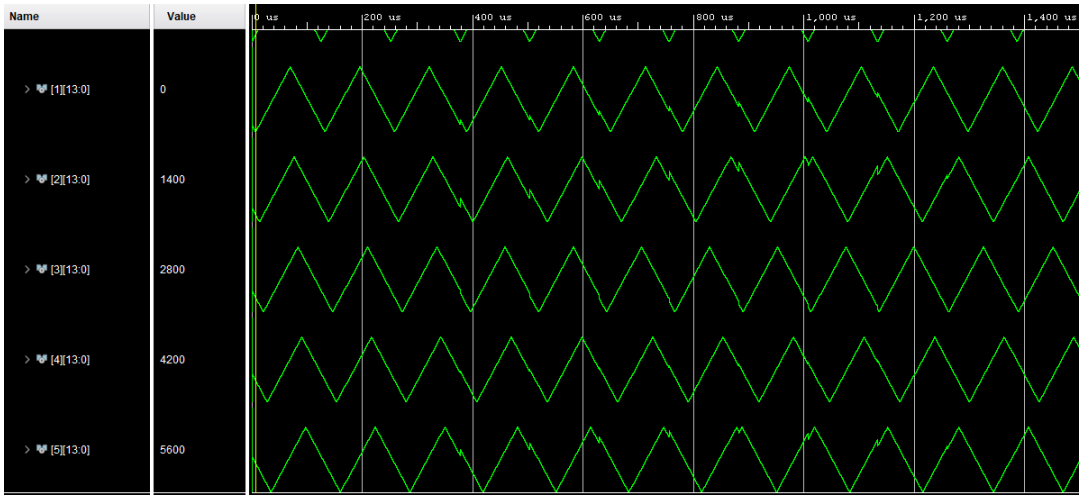


FIGURE 4.23: Carrier transition from m3-p2 to m3-p12 configuration (slot 2 to 6)

Chapter 5

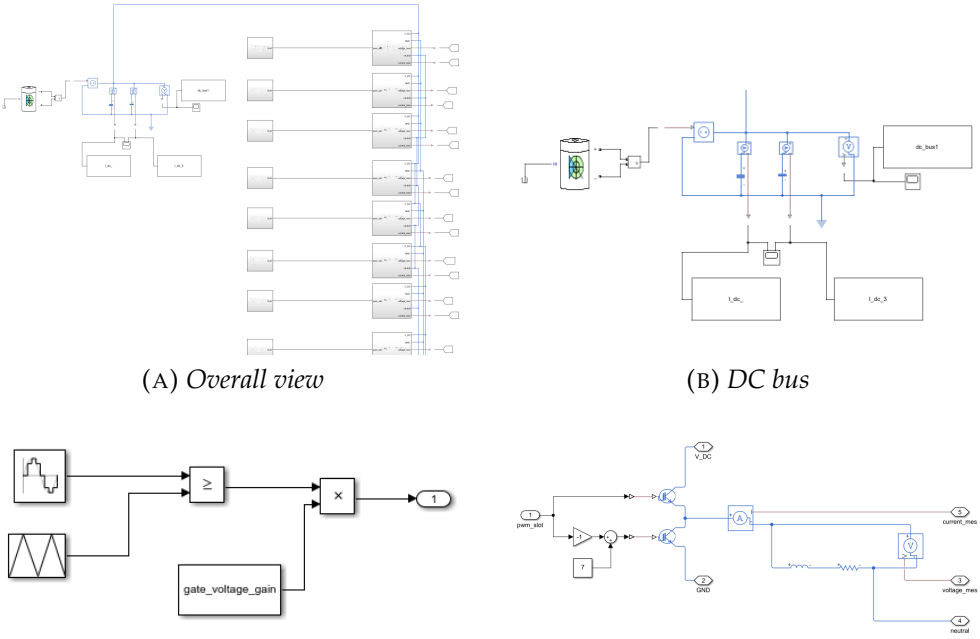
Simulink model for interleving benefits

5.1 Simulink model

The benefits of interleaving are well documented in the literature [3],[14],[15], [18]. Based on the applications and implementation methods, advantages can be obtained in one direction rather than another. In order to evaluate the extent of these benefits in the case of a multiphase machine with 36 slots driven independently and with interleaving inside the slots of the same phase, a simulink model is created. This model can be analyzed in several sections. A first section is created for the generation of carrier and modulating, from which comparison the control signals for each leg of the inverters can be produced. A section consisting of the IGBTs that model the power boards on which the inverters are mounted and finally a section in which a motor with 36 R/L loads suitably connected to each other is implemented in the first approximation. The way in which the multiphase machine is considered in this simulink model is certainly not the most faithful but it is not believed that this is a limit for verifying the benefits of interleaving. From the following images (fig. 5.1) you can have a complete view of the model created and the individual sections that make it up.

5.2 DC-bus and capacitors stress

A first parameter that is analyzed concerns the DC bus. Several simulations are performed in which the behavior of the DC bus is compared for the various configurations. The simulations can be traced back to three main cases: operation without interleaving, operation with standard intereaving and operation with interleaving internal to the phases. In this way it is possible to appreciate the impact on the DC bus in the various modes and highlight how the benefits are greater in the configurations that have fewer switching



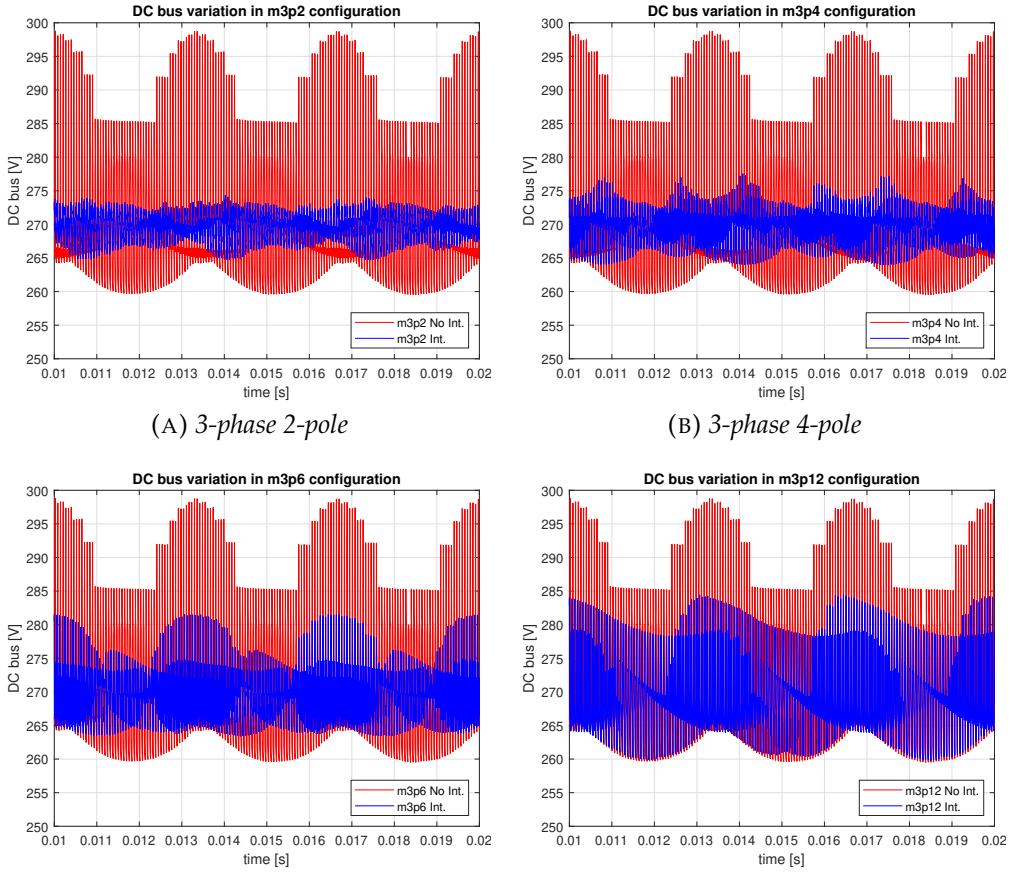
(A) *Overall view* (B) *DC bus*

(C) *PWM section* (D) *R/L load*

FIGURE 5.1: Simulink model for interleaving benefits verification

at the same time. The following graphs (5.2) show how, for each configuration, passing from a drive of the IGBTs without interleaving to one with interleaving there is a more contained variation of the voltage on the DC bus. A configuration with a greater number of different carriers will be characterized by multiple switching at different instants, thus maximizing the effects of interleaving. This means that the improvement in the performance of the DC bus that is found in the same configuration by introducing or not introducing interleaving can be found when the configuration changes. A useful comparison can be that between the m3p2, m3p4, m3p6 and m3p12 configurations (fig. 5.2).
Another aspect concerns DC capacitors. It can be seen that these are more stressed in the case of PWM without interleaving. The current flowing through them is assessed and from the simulations it is seen how evident improvements are obtained thanks to the use of interleaving. The amplitude of the current that flows through them is lower. Below are the simulation graphs for a comparison, of the m3p2 configuration, with and without interleaving (fig. 5.3), and two graphics for comparing the current through DC bus capacitor 1 (100nF) and DC bus capacitor 2 (25μF) in all the 3-phase configurations (figures 5.4 a and b respectively).

This improvement allows for more relaxed specifications on the choice of DC capacitors. In order to have more evidence of the interleaving benefits



(A) *3-phase 2-pole* (B) *3-phase 4-pole*

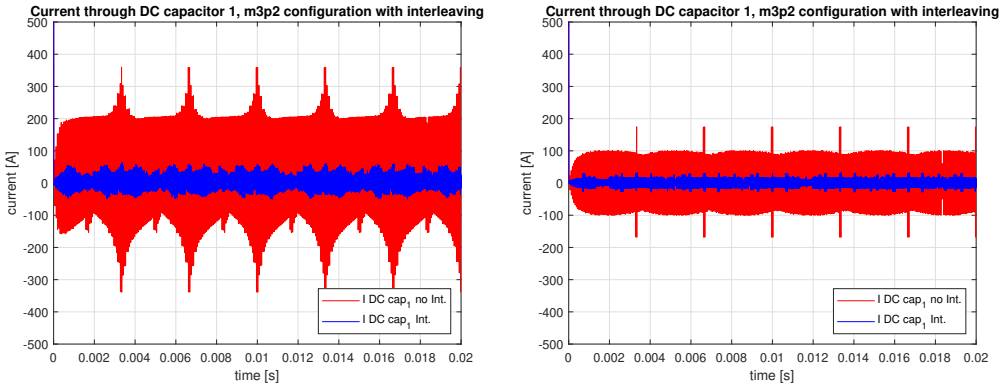
(C) *3-phase 6-pole* (D) *3-phase 12-pole*

FIGURE 5.2: DC-bus variation with and without interleaving

the rms value of the currents through the DC capacitors has been taken in consideration. In Tab. 5.1 are shown the values of the two currents flowing through the two DC capacitors of the inverter in the different 3-phase configurations.

5.3 THD in phase to phase voltage

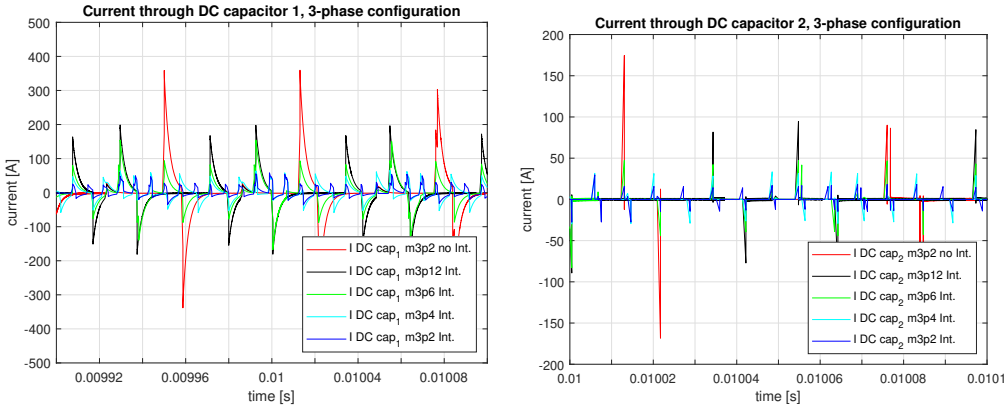
Another quantity that is monitored is that of phase to phase voltage. To calculate the phase voltage, considering the motor structure it is necessary to consider in series the slots belonging to the same phase and to add the voltage drops. The same is done for another phase and at that point the difference between the two tensions is assessed. The relevant data is that the trend over time is more 'clean' and more similar to that of a sinusoid. The phase to phase



(A) *DC bus capacitor 1 (100nF)*

(B) *DC bus capacitor 2 (25µF)*

FIGURE 5.3: DC-bus capacitors current comparison in 3-phase 2-pole configuration



(A) *DC-bus capacitor 1 (100nF)*

(B) *DC-bus capacitor 2 (25µF)*

FIGURE 5.4: DC-bus capacitors current comparison in 3-phase configurations

voltage between phases A and B of the m3p2 configuration are evaluated in three different conditions:

- 3-phases 2-poles configuration without interleaving (5.5)
- 3-phases 2-poles configuration with standard interleaving (5.6)
- 3-phases 2-poles configuration with interleaving inside the phases (5.7)

For the simulation, a DC bus value of 300Volt was used. For this reason, the overlapping of voltage drops on the various slots leads to obtaining a

TABLE 5.1: DC-bus capacitors current comparison in 3-phase configurations

Configuration	Interleaving	$IDC1_{rms}$ [A]	$IDC2_{rms}$ [A]
3-phase 2-pole	No	45.5	0.93
	Yes	14.0	0.15
3-phase 4-pole	Yes	21.8	0.31
3-phase 6-pole	Yes	30.3	0.52
3-phase 12-pole	Yes	41.2	0.81

waveform with a maximum value around $\pm$3600 Volts. This is a direct consequence of the fact that in the m3p2 configuration there is a number of slots per pole per phase equal to 6. In addition to having a graphic response,

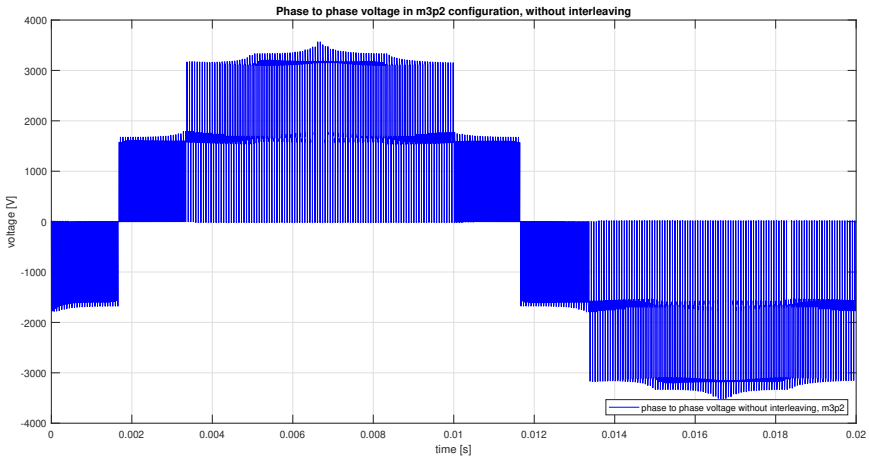


FIGURE 5.5: Phase to phase voltage, 3-phases 2-poles configuration without interleaving

the total harmonic distrotion for these signals in the various configurations was assessed. The THD in fact allows to quantify the goodness of a signal in terms of linearity. From the values in Tab. 5.2 it is possible to obtain further evidence of the benefits introduced by interleaving. It is also noted that these are more marked in the configurations in which interleaving is used the most.

A direct consequence of having a cleaner phase to phase voltage, therefore with a trend more similar to the sinusoidal one of the reference used for the modulation, concerns the losses. A signal characterized by a lower THD, as in the case in which interleaving is used, will have a reduced harmonic component. In this way it is possible to verify how a suitable use of interleaving can lead to a reduction of losses.

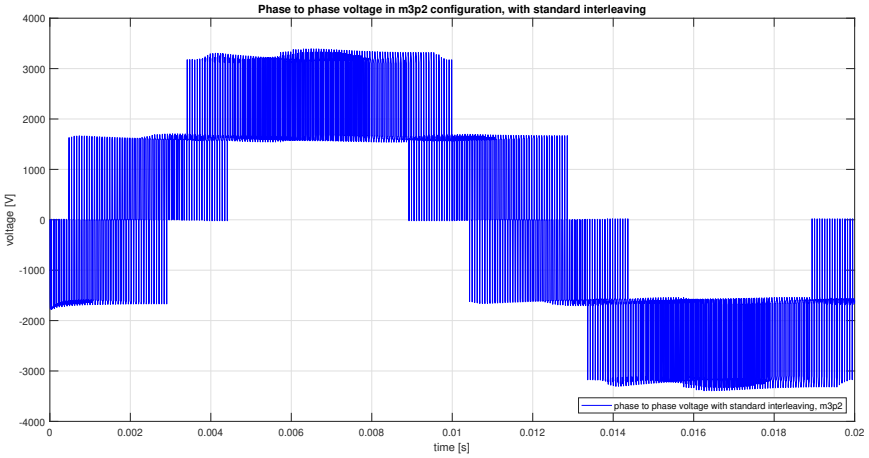


FIGURE 5.6: Phase to phase voltage, 3-phases 2-poles configuration with standard interleaving

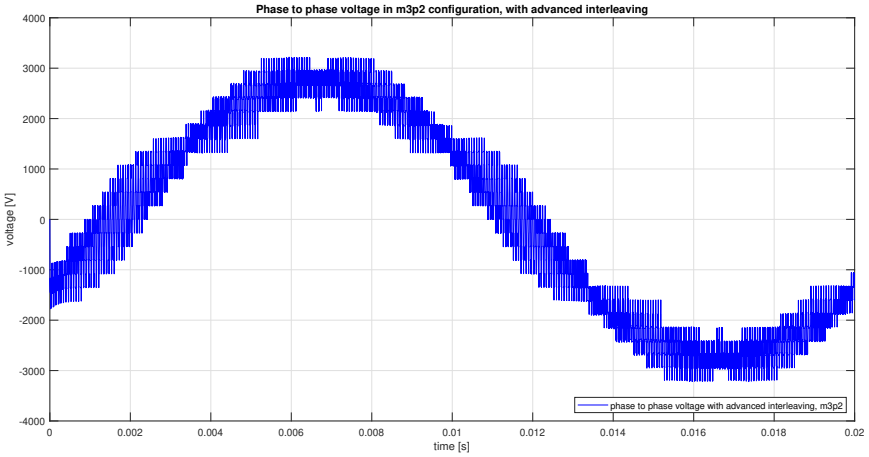


FIGURE 5.7: Phase to phase voltage, 3-phases 2-poles configuration with interleaving inside the phases

TABLE 5.2: THD comparison in 3-phase configurations

Configuration	Interleaving	THD
3-phase 2-pole	No	44%
	Standard	39%
	Inside phase	16%
3-phase 4-pole	No	44%
	Inside phase	20%
3-phase 6-pole	No	44%
	Inside phase	25%
3-phase 12-pole	No	44%
	Inside phase	39%

Chapter 6

Measurements and results

6.1 A/D conversion Testbench

A tailor-made testbench was created to test the correct functioning of the ADC and verify the correct acquisition of the samples on the FPGA. The setup involves the use of:

- A signal generator
- AD9249 EVM
- ZYNQ ZC702
- PC

The output 1 of a signal generator was connected to the input of channel 1 of the conversion board. To make this connection it was necessary to use dedicated SMA to BNC adapters. The same type of connection was made between output 2 of the signal generator and the ADC input dedicated to the clock. AD9249 outputs are available on a male FMC connector. This connector was then connected to one of the female FMC connectors on the FPGA. The zynq ZC702 was then connected to a terminal via a micro USB connector. The testbench just described expect that a signal is supplied to the converter input to be sampled. Sampling is scanned by the frequency of the clock signal which is supplied externally via the signal generator. The ADC samples and sends the data to the FPGA which constantly acquires them. The FPGA constantly acquires each sample through the mechanism illustrated in 3.2 and if no other operation is required at the next clock edge, the sample is overwritten. When desired, externally the FPGA can be communicated to start saving the samples in a register file. As soon as it comes the RF is completely filled, the RF will send the samples one at a time to the processor. At that point the samples are sent via UART on the terminal. Once printed on the terminal, the samples are collected and processed. The ADC sends the samples in twos complement notation. After collecting them, the samples are manipulated in order to reconstruct the original information. Once this is

done, the obtained samples are plotted in Matlab. The RF instanced in VHDL has a capacity of 30 samples. Consequently it will be necessary to vary the frequency of the signal that enables the shift-register of which we discussed in 3.2. This frequency is varied according to the signal being sampled in order to acquire one or more periods. In fig. 6.1 and 6.2 it is possible to observe the curve obtained by plotting the 30 samples acquired in the case of 1 and 2 observation periods respectively. The amplitude of the sinusoidal signal was kept in a range reasonably lower than the maximum expected in the converter datasheet [1].

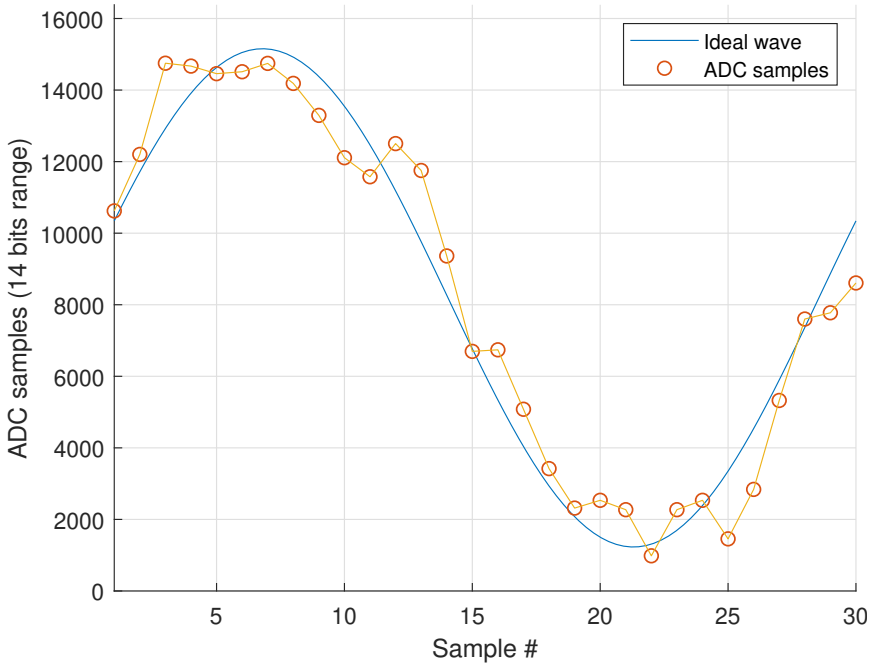


FIGURE 6.1: ADC samples - one period

6.2 PWM square waves analysis

The code for the PWM section was initially simulated in Vivado. As reported in 4.7 it was possible to verify that the structure created was able to correctly generate the output of the pwm section. In particular, the generation of carriers based on the configuration was verified, paying attention to the phase shift introduced to implement interleaving. Once a generic 50Hz sinusoidal reference with peak to peak amplitude corresponding to the entire carrier range was implemented and tested, it was possible to evaluate the waveforms obtained by the comparison between carrier and modulating. Finally, the behavior of the various carriers was simulated to verify correct operation

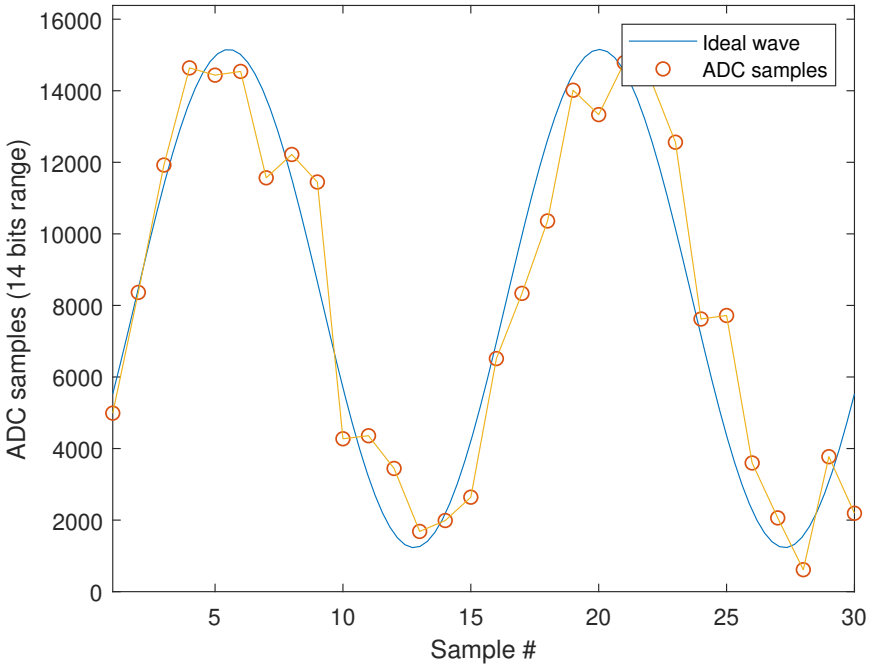


FIGURE 6.2: ADC samples - two period

during the configuration transition. Once the correct simulation operation was verified, it was possible to synthesize the hardware described in VHDL on the FPGA and experimentally evaluate its operation. For the acquisition of measurements on the waveforms, an oscilloscope and a logic state analyzer with 16 digital input channels were used. The first allowed to have a better resolution but offering the possibility to display only 4 channels at a time. With the logic state analyzer, it was possible to simultaneously display 16 signals thus allowing to evaluate a reasonable number of outputs of the PWM section and verify their correct operation.

6.2.1 Verification of PWM outputs

The nine predisposed configurations have been fully verified. Below are the waves acquired through the logic state analyzer of some of the configurations capable of offering feedback of the modulation carried out with particular attention to the behavior due to interleaving. The m3p2 configuration is characterized by a qs (slot per pole per phase) equal to 6. In figure 6.3 the square waves associated with phase A are shown. It can be seen that by introducing a phase shift of 20 degrees between the carriers , the square waves associated with the same phase and therefore with the same reference, are out of phase as expected for the interleaving used.

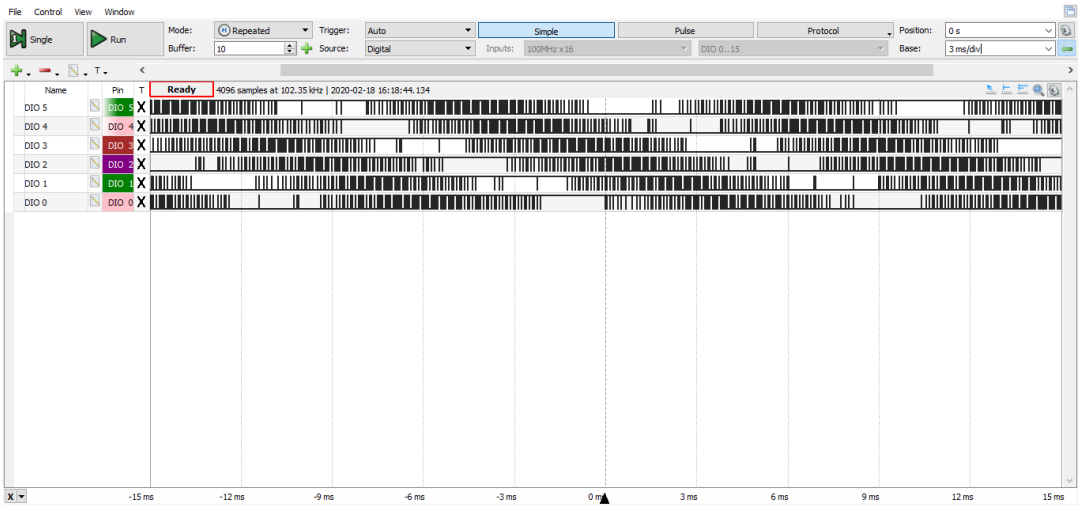


FIGURE 6.3: PWM signals (phase A, 3-phase 2-poles)

Figure 6.4 shows the waves associated with phases A, B and C in the m3p4 configuration. This configuration is characterized by a qs equal to 3. The period observed is equal to 30ms. In such a way it's possible to recognize the periodicity of 20ms (corresponding to a 50Hz signal) of the modulated signal. It is possible to recognize the three phases considering that each is out of phase of 120 degrees with respect the others. It is also possible to appreciate qualitatively at each phase the internal shift due to interleaving .

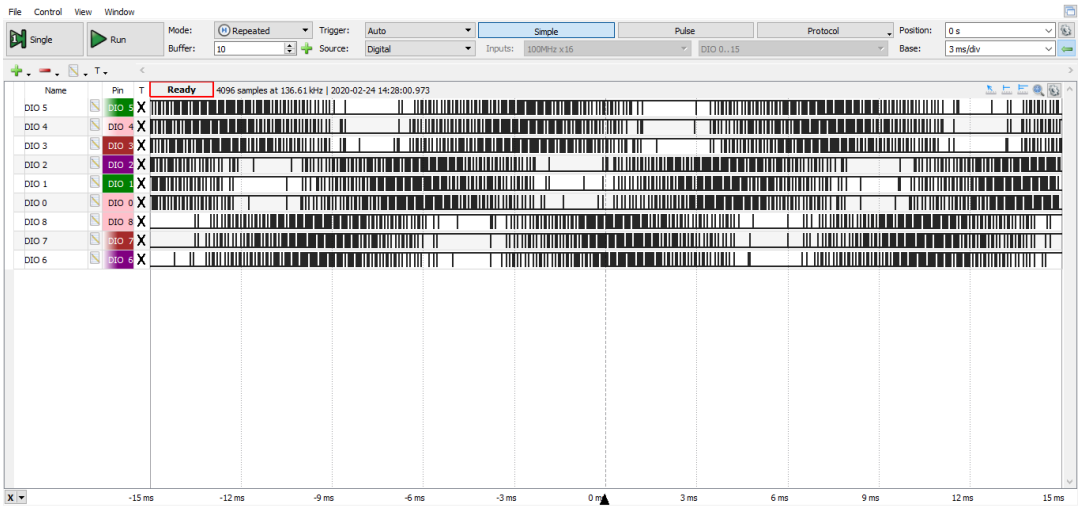


FIGURE 6.4: PWM signals (phase A B and C, 3-phase 4-poles)

The configurations characterized by m = 6 and the configuration m18p2 are made as several three-phase systems suitably phase-shifted. In fig. 6.5 it is possible to observe the waveforms associated with phases A1,A2,B1,B2,C1

and C2 in the m6p2 configuration. This configuration is characterized by a number of slots per pole per phase equal to 3 and is seen as the set of two three-phase systems out of phase with each other by 30 degrees. Since the number of channel available in the logic analyzer are equal to 16, in order to give an overall view as coplite as possibile, only two slot per phase are analyzed. In fig. 6.5 the phases from A1 to C2 are associated from channel 0 to channel 11.

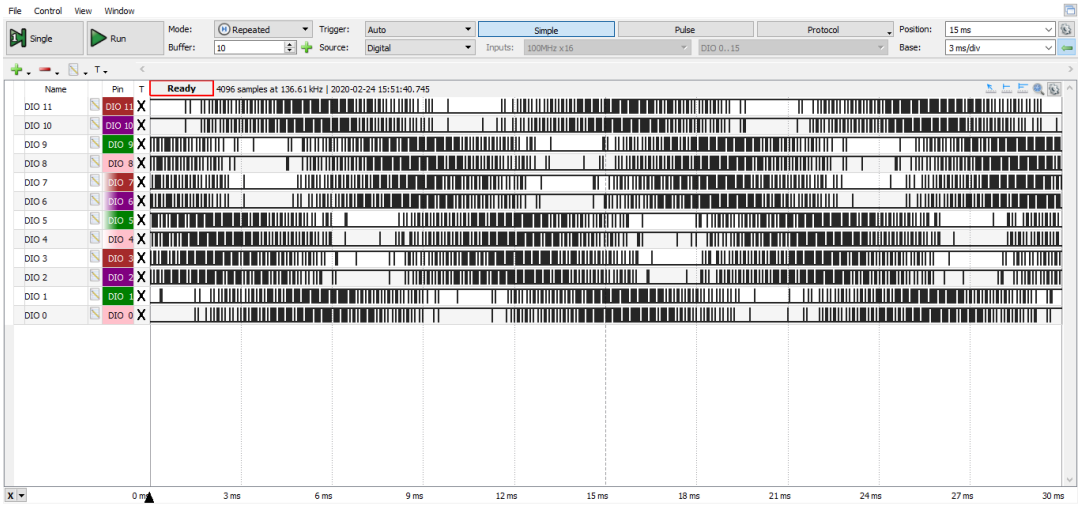


FIGURE 6.5: PWM signals, phase A1-A2-B1-B2-C1-C2, m3p2 (2 slots per phase)

Finally, the functioning of the transition mechanism from one configuration to another was observed. Figure 6.6 shows the performance of the PWM outputs associated with slots 1 to 6 of the machine during the transition from the m3p2 configuration to the m6p2 configuration. The time window has been set up to qualitatively observe the waves produced over 3 periods of the fundamental (3*20ms): one before the transition, one during and finally one after the transition.

6.2.2 FFT of PWM square waves

In addition to having a graphical feedback to verify the correct trend of square waves, the Fourier transform of some channels was evaluated. The oscilloscope turns out to be, in this type of application, a more powerful instrument than the logic state analyzer as it is capable of offering a higher resolution or a wider acquisition window. Once the data are acquired, they are imported in Matlab in order to perform the FFT. The goal is to verify that, for each pwm signal taken into account, the fundamental frequency corresponds to

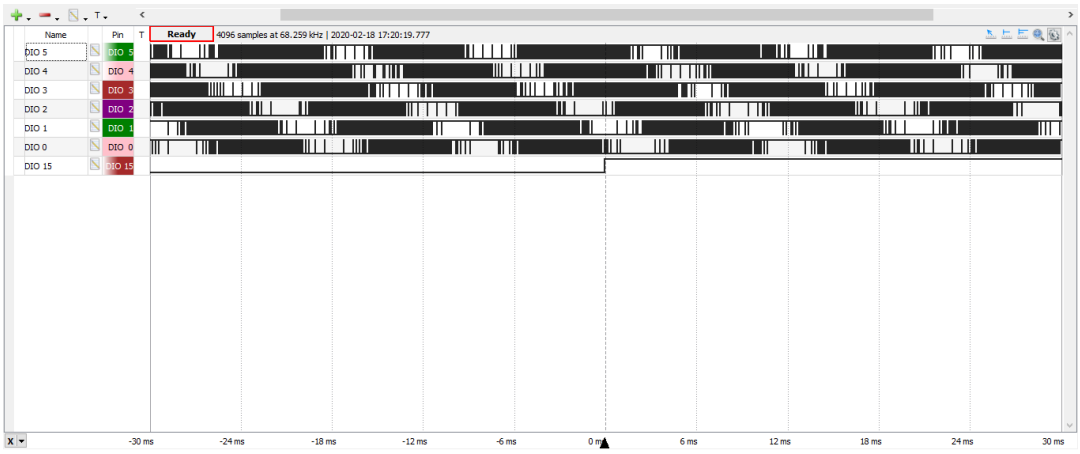
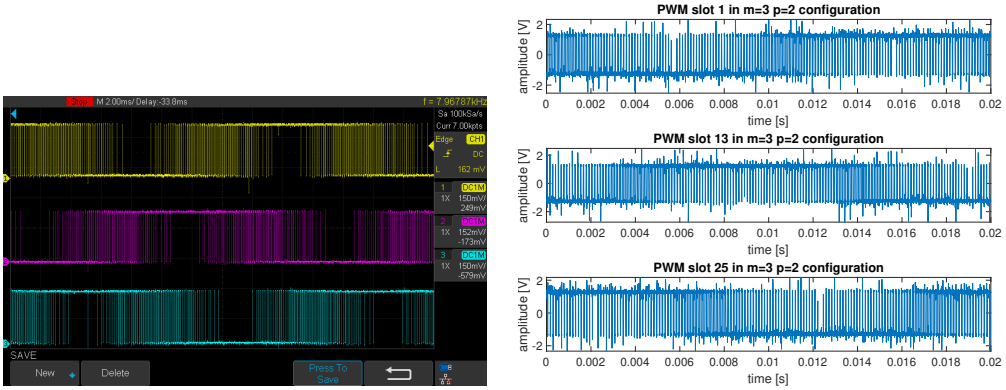


FIGURE 6.6: PWM signals, transition m3p2 to m6p2

50Hz. In addition to that, the FFT offers the possibility to check the phase shif of different signals comparing the phase associated to the fundamental components.

The analysis has been performed for all the possible configuration in order to verify the congruence with what is reported in the previous section. Below is reported the analysis for the configuration 3-phase 2-pole. In fig. 6.7 is possible to observe the waves observed.



(A) *PWM capture with the oscilloscope*

(B) *PWM processed in Matlab*

FIGURE 6.7: PWM output, m3p2 configuration, slot 1,13,25

In figure 6.8 it is possible to observe the Fourier transform of the PWM signal associated with the slot 1 in the configuration 3-phase 2-poles. The amplitude of the components is normalized with respect to the fundamental at 50Hz. It is also possible to observe that the dominant harmonics are found in multiples of the switching frequency of approximately 7.95KHz. Similar

results were obtained for all the other square waves of other configurations. Below are reported the figures corresponding to the case 3-phase 2-pole. In

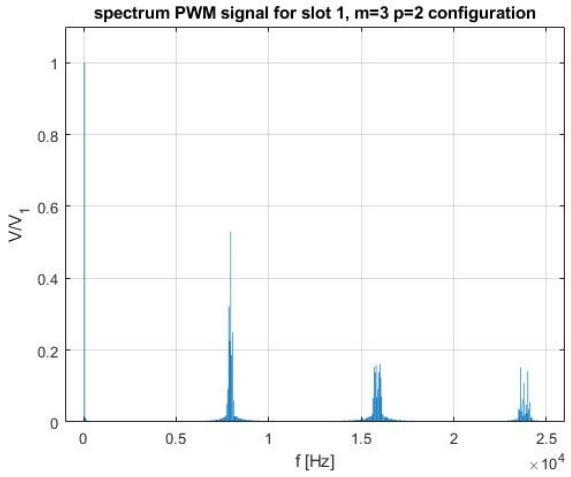


FIGURE 6.8: Amplitude spectrum of PWM output, slot 1 m3p2 configuration

particular, the signals analyzed are the one corresponding to the first slot of phases A, B and C (slot 1,13,25). In fig. 6.9 (a) is represented the amplitude spectrum of the three signals over a range of 25KHz. The same spectrum is zoomed in fig. 6.10 (b) over a range of 9kHz.

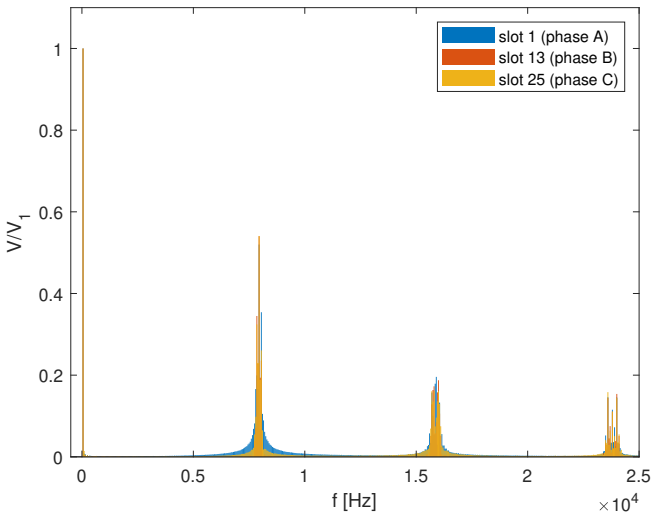


FIGURE 6.9: Amplitude spectrum of PWM output, m3p2 configuration, slot 1,13,25 (25kHz range)

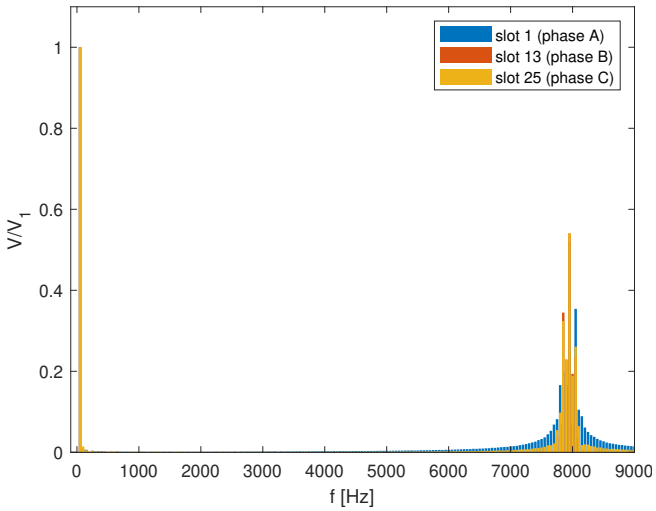


FIGURE 6.10: Amplitude spectrum of PWM output, m3p2 configuration, slot 1,13,25 (9kHz range)

As regards the phase shift,the phase of the FFT has been evaluated in order to verify the fundamental to be out of phase of 120°. In fig. 6.11 is possible to evaluate the phase shift between the fundamental components (50Hz). In fact, the phase associated to the fundamental are 77°, -41° and -163°.

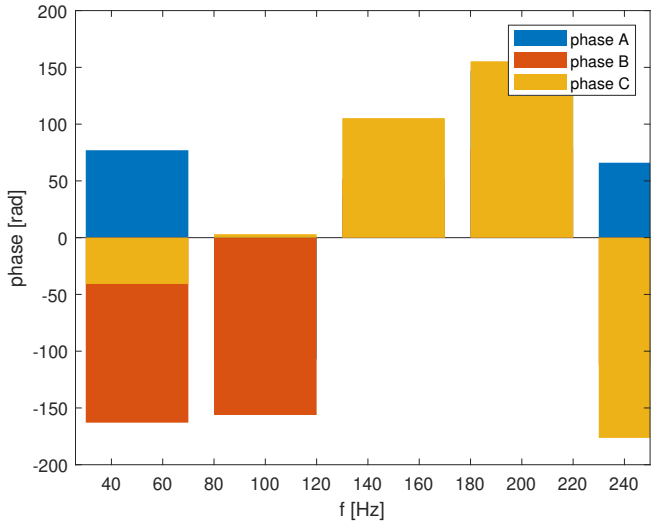


FIGURE 6.11: Phase spectrum of PWM output, m3p2 configuration, slot 1,13,25

Chapter 7

Conclusions

The work here presented described the implementation on FPGA of a Pulse Width Modulation integrating the interleaving technique and of a system able to handle the communication between FPGA and ADCs. As for the PWM, the implemented structure is characterized by an high level of flexibility. This flexibility is mainly related to the capability of online changing of the number of pole-pairs as well as the number of phases. This aspect is fundamental to meet specifications imposed by the configuration of the machine under study. The two structures implemented have been simulated and tested with dedicated testbench. At the end of the work, a Matlab-Simulink model is created (which represents the machine under study as a first approximation) in order to have concrete evidence of the improvements obtained. Thanks to the model created, it was possible to verify how the improvements are more consistent in the configurations that maximize the use of interleaving.

7.1 Improvement obtained

The improvements obtained are due to the implemented modulation technique, with reference to the advantages brought by the use of interleaving. This technique perfectly matched the structure of the motor, leading to a further step or rather the implementation of interleaving within the phases. The improvements obtained, documented in chapter 5, refer to the stress on the DC-bus and on the decoupling and bypass capacitors in the board with the inverters. Equally important results have been obtained with regards to the goodness of the phase-to-phase voltage, obtaining a remarkable feedback of the impact of interleaving on the Total Harmonic Distortion of this voltage. The latter result translates into an improvement in the overall efficiency of the system.

7.2 Future works

Future work will focus on perfecting the modulation technique to make the system able to deal with the fault of one or more slots. The algorithm may refer to the one already implemented for the management of transitions from one configuration to another. A further aspect to work on in the future will be that of the complication of the architecture implemented to obtain the management of the configuration characterized by a non-integer number of slots per pole per phase, leading to an even more flexible structure.

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