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Characterization of Highly Doped Si:P, Si:As and Si:P:As Epi Layers for Source/Drain Epitaxy

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Abstract

The downscaling of transistors allowed an exceptional miniaturization. This extreme scaling makes that the contact resistance a key contributor to the device parasitics.
This work reports the characterization of Phosphorus, Arsenic and Co-doped epitaxial layers (Si:P, Si:As, Si:P:As) for NMOS S/D. Chemical Vapor Deposition is employed for a selective process at 670 °C and a non-selective process at a lower temperature of 450 °C.
Physical properties such as morphology, crystalline quality, composition, dopant activation and contact resistivity are studied and the thermal stability was verified up to 700 °C. Different scenarios are explored as concentration ranges from 1% to 4%. Contact resistivity has been measured on Ti-silicidation stacks employing MR-CTLM technique.
The reported results show that layers, grown at 670 °C at high total concentrations ($\sim 3\%$), the active concentration of as-grown blanket Si:As and Si:P:As layers are lower compared to Si:P, furthermore Si:As shows a lower tensile strain compared to Si:P. Co-doped layers grown with the non-selective process at a low total concentration ($\sim 1.2\%$) are characterized by an enhanced active concentration due to a more efficient vacancy trapping mechanism, while there is no activation enhancement after laser annealing. Contact resistivity measured on the Ti-stacks reaches $2 \cdot 10^{-9} \Omega.cm^2$ for different process' conditions. As addition show beneficial effects in contact resistivity for as-grown co-doped layers $\sim 3\%$ for the selective process. Si:As and Si:P:As layers grown at 450 °C show ρ_c comparable to standard Phosphorus doped epi-layers. These properties together with reduced diffusion after additional thermal budgets make Si:As and Si:P:As as promising candidates for NMOS S/D.

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1 Introduction

The transistor was invented in 1948 at Bell Laboratories by William Shockley, John Bardeen and Walter Brattain. The transistor invention opened the digital era and nowadays it is used for a wide range of applications, from telecommunications to biomedics. Today, computational power is needed in every aspect of life.

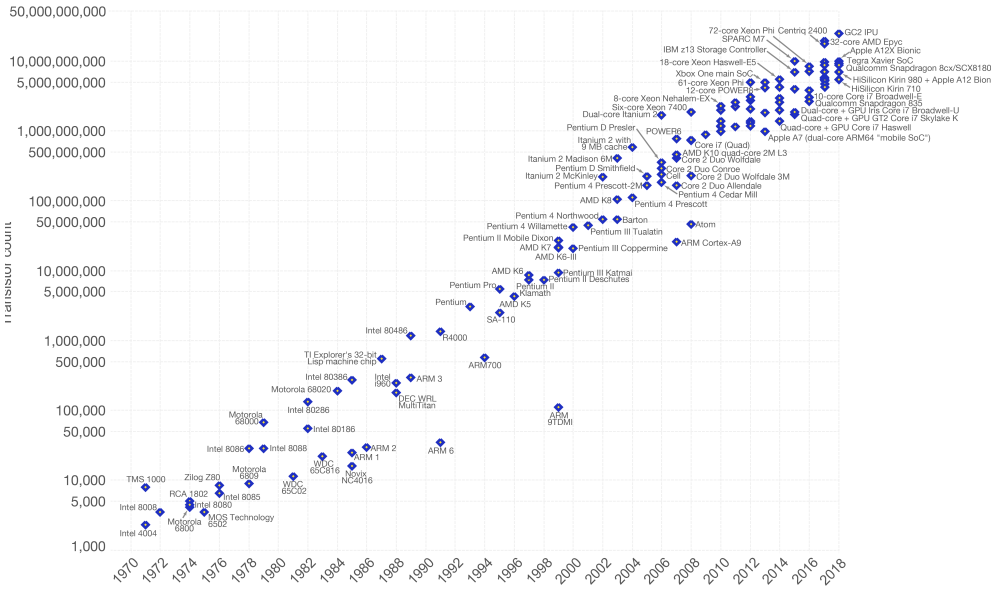


Figure 1.1: Number of transistor per year.

From the early beginning of the first Germanium based transistor till the Silicon-based technology, electronic industries and researchers cooperated to solve the challenges in both manufacturing processes and technology. Since the microelectronic device's integration became faster, manufacturing enabled an incredibly high computational power, nowadays available also in consumer electronics. From the early beginning of the '70s, the planar

Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) architecture evolved substantially during the last 50 years. Scaling procedures represented the path to reach a high miniaturization level.
In 1965 Gordon Moore observation [28], based on previous data of the electronics industry production, described the number of transistor in an integrated circuit (IC) doubling every two years. Later it became a prediction referred to as Moore's law.
Moore's law is still driving the microelectronics industry nowadays. In order to follow the trend, device shrinking was required. This quest led on one hand to improvements in photolithography techniques to reach a higher density on the silicon wafers and on the other hand to new architectures. The evolution of scaling started from the 2D planar MOS till the current generation of 3D FinFET (N20) and the next generation of Multi-bridge Gate All Around (GAA) FET (N5, N3).

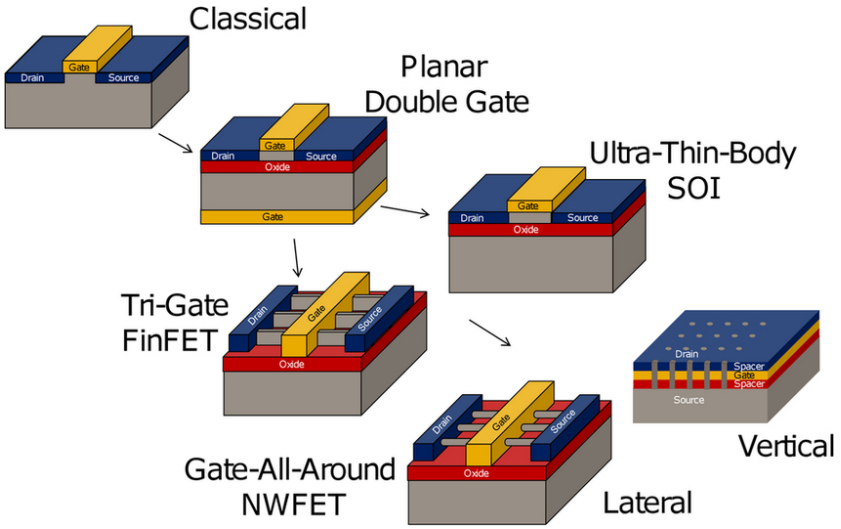


Figure 1.2: Transistor architecture evolution [16].

Scaling evolution relied not only on improving manufacturing steps but also on the integration of new technology and materials. The manufacturing improved in the lithography techniques resulting in a better controllability of the process enabling ultra-shallow S/D junctions and sharp profiles. On the technology side, to shrink physical dimensions, several material contributors can be cited, some of them provide a great boost in device performances such as TiSi and NiSi silicidation, high k dielectrics, strain technology and Cu Damascene. The new technologies played an important role since scaling down devices led to losing the electrostatic control of the MOSFET channel,

making short channel effects (SCE) causing current leakages, high power consumption in the OFF state and parasitics. So the device is now more complex, in the following picture, we have an overview.

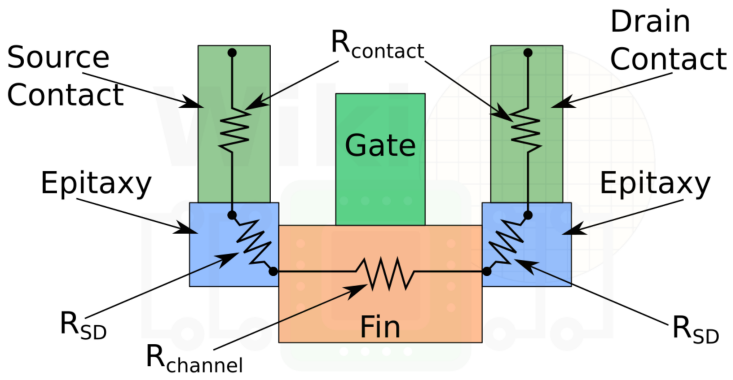


Figure 1.3: FinFET resistance contributors.

Entering the nano-scale era the contribution of the contact resistance related to the interfaces between metal and Source and Drain region (S/D) became relevant.

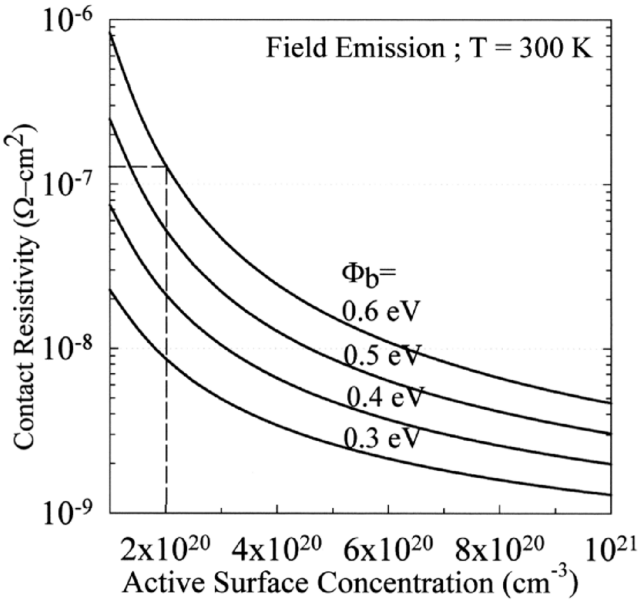


Figure 1.4: Contact resistivity vs. active concentration [44].

Many solutions have been adopted and proposed to mitigate parasitics.

The semiconductor industry needs low contact resistivity (ρ_c) in S/D regions to reach further technological nodes, as stated in the International Technology Roadmap for Semiconductors (ITRS)[1]. In fact, it is reported a degradation by more than the 40% of the saturation current with respect to the ideal case. As can be seen in figure 1.4, the target of ρ_c sub 10^{-9} Ωcm^2 requires high active doping concentration [44]. Reaching low S/D contact resistivity leads to several challenges involving metrology, materials and processing techniques [8] [19]. In the framework of this thesis some of these challenges are discussed, hence measurements techniques limits will be taken into account.

1.1 S/D epitaxial growth: Motivation

During the last decade, Si:P was extensively used for S/D n-MOSFET epitaxial growth, Chemical Vapor Deposition (CVD) guarantees high doping levels, far beyond the solid solubility of P in Si. The interest in highly doped Si:P increased because it combines high doping concentration with high tensile strain. As the resistivity reaches a minimum, corresponding to 3-4 % phosphorus total concentration, it starts to increase. Resistivity depends on N_D, and after a threshold, additional phosphorus does not occupy substitutional sites (ionized impurities), but it occupies interstitial sites or it results in vacancy complexes.
The active concentration seems to saturate in the as-grown layers. During the 1990s laser annealing technique (LA) was found to enhance active concentration enhancement, resulting in a decrease of resistivity. This additional thermal budget results also in thermal diffusion of dopants in the layer and enlarges the electrical thickness of the layer. Moreover this is a metastable condition and its benefits are reduced by post thermal budgets, like silicidation or Cu deposition. Some explanation of the phenomena observed will be discussed in the thesis through different characterization techniques.
In this work, the goal was to evaluate the effect of As in the epitaxially grown S/D regions. Blanket Si:P, Si:P:As and Si:As epi-layers with different concentrations were characterised and the impact of the As incorporation. Additionally, to the standard 670 °C process a novel low-temperature 450 °C process will be investigated as a possible way to reduce resistivity, the interest in low-temperature processes increased in the last decade since high activation level can be obtained avoiding laser annealing thermal budgets.

2 Theoretical background

Since metal contacts can be found in many parts of the electronic devices, Metal-Semiconductor junctions have been widely studied, especially for their importance in current driving. In this chapter, the ideal theory will be described and then some non-idealities will be discussed.

The performances of the device depend on the reduction of the series resistance. In fact, an *ohmic contact* is a metal-semiconductor junction where the junction resistance, as the metal-semiconductor junction at S/D, is much lower than the semiconductor device resistance (channel). The reason why we need a low contact resistance is straightforward. The higher is the contact resistance the higher will be the voltage drop on the M-S junction which means that a higher voltage is needed to drive the same current to the device leading to higher power consumption. Reducing this voltage drop is strongly beneficial since it will allow us to reduce the power dissipated by the device both in the ON and in the OFF state.

The following equation is the contact resistivity expression:

$$\rho_c = \lim_{\Delta A_c \longrightarrow 0} R_c \Delta A_c \; [\Omega \cdot cm^2] \tag{2.1}$$

In equation (2.1), R_c is the contact resistance and ΔA_c is the area of the contact. It will be the starting point for our discussion.

2.1 Metal-Semiconductor junction

Putting a metal and a semiconductor in contact leads to the formation of an energy barrier. This barrier height is very important since it is responsible of the carrier transport behaviour. By modifying the active concentration (N_D) the barrier can be tuned.
In order to understand the phenomena occurring in the Metal-Semiconductor

junction,the study of the band diagram of the resulting structure will be of primary importance.

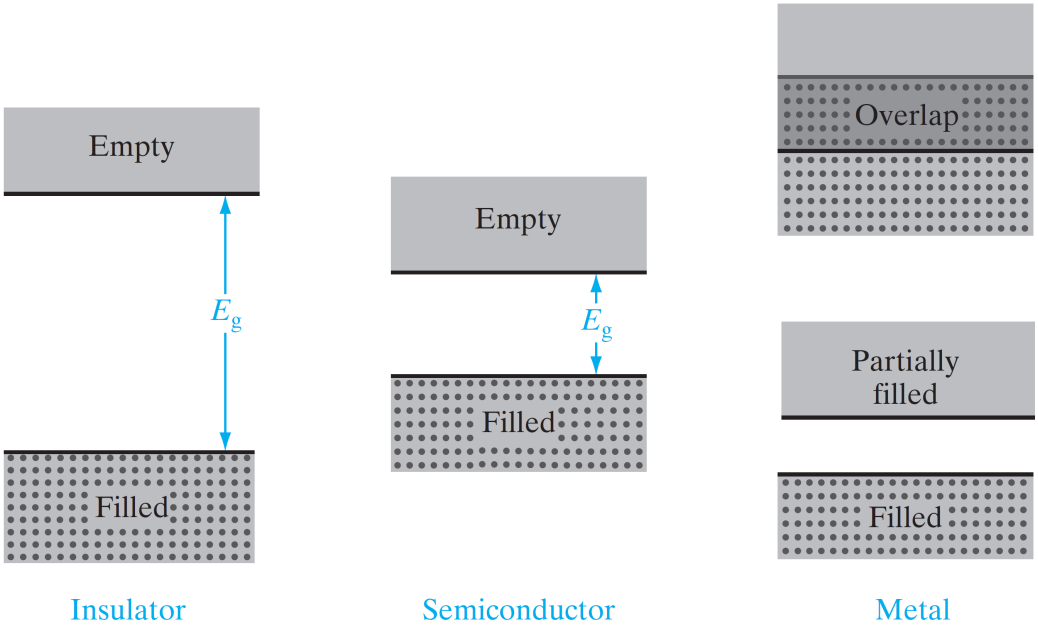


Figure 2.1: Typical energy gap for the insulators semiconductors and conductors. In metals valence and conduction band are overlapped [42].

To understand the resulting band-diagram it is useful to recall the electrical characteristics of solids, which depend on their band structure. Only a small number of bands is available for electrons. In this context the energy gap is an important figure of merit. It is, in fact, the energy required by an electron to overcome the valence band to reach the conduction band. It follows that an insulator will be characterised by a large energy gap, conductors do not have energy gap and semiconductors have a small energy gap, which can be overcome easily.

2.1.1 Band diagram

The band in the figure is related to an ideal metal-n-type silicon junction [44].

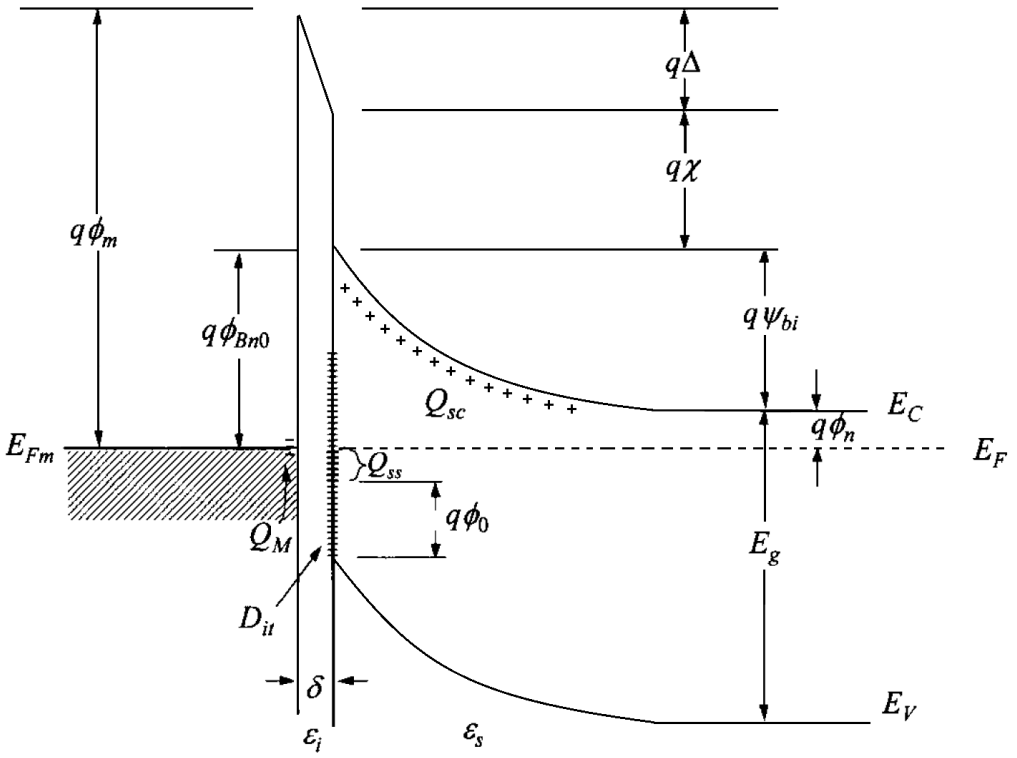


Figure 2.2: This is the band diagram of the metal-semiconductor junction, notice that on the sides the characteristic of the isolated material is kept, specifically the metal on the left side and the semiconductor on the right side.

Notice that at equilibrium E_F is constant through the structure [44].

The quantities shown are:

- E_F Fermi level it is the energy associated with 50 % probability of being occupied by a charge irrespectively of the temperature.
- E_{Fi} is the intrinsic Fermi level associated with the occupation probability of the un-doped semiconductor. It is located in the middle of the Bandgap (E_g).
- E_V is the valence band, the highest occupied energy level.

- E_C is the conduction band, the lowest unoccupied energy level.
- E_g is the energy gap, small in semiconductors, it is the energy difference between E_C and E_V.
- U_0 is the vacuum level. Beyond this energy, the charge is free.
- $q\phi_M$ is the metal work function
- $q\phi_S$ is the semiconductor work function
- $q\phi_{Bn}$ is the Schottky barrier
- qV_{bi} is the built-in potential

Notice that in semiconductors E_F lies inside the energy gap while in metals, since E_C and E_V are overlapped, the charge is available so the charge flow is possible also for moderate voltage drops. In semiconductors, the Fermi level can be tuned through the incorporation of dopants in the layers, which can be divided into two categories: donors and acceptors. The first ones provide an additional charge in the conduction band, while the second ones a hole in the valence band. In n-doped silicon it is:

$$E_F = E_c + k_B T ln \frac{N_c}{N_D} \tag{2.2}$$

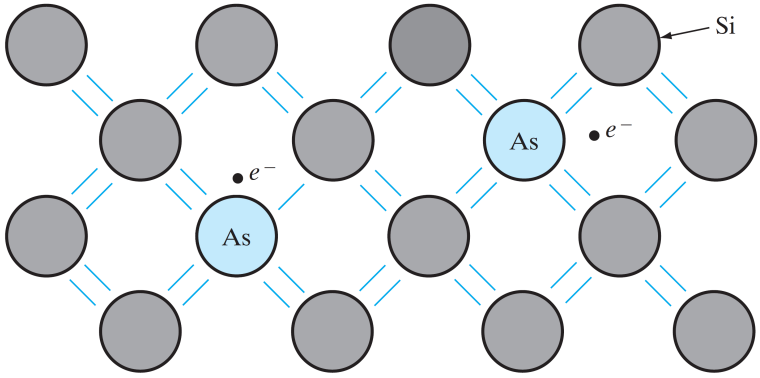


Figure 2.3: Incorporation of dopants in crystalline structure. Group V impurities, as As and P, have four electrons to complete the covalent bonds with Si and an extra electron which is loosely bound and promoted into the conduction band [42].

Putting in contact a metal and a semiconductor together will result in a charge flow from the semiconductor to the metal until the thermal equilibrium is established. Looking at the band diagram, reaching the thermal equilibrium results in E_F lining up on both sides of the M-S structure. Electrons are confined in the metal because of a potential energy barrier, which has the following expression:

$$q\phi_{Bn0} = q(\phi_M - \chi_S) \tag{2.3}$$

Where $q\phi_M$ is the metal work-function and $q\chi$ is the electron affinity of the semiconductor. The electron affinities of semiconductors and the work functions of metals are established. For metals, $q\phi_M$ is of the order of a few electron volts (2 - 6 eV), its values are generally very sensitive to surface contamination, so metal needs to be preserved.
Since the interface is formed a depletion layer is created in the semiconductor side, while on the metal side we'll have a delta charge, which compensate the net charge in the semiconductor.

$$W_D = \sqrt{\frac{2\epsilon_s}{qN_D}\left(V_{bi} - V - \frac{kT}{q}\right)} \tag{2.4}$$

$$|\mathcal{E}(x)| = \frac{qN_D}{\epsilon}(W_D - x) \tag{2.5}$$

$$E_C(x) = q\phi_{Bn} - \frac{q^2 N_D}{W_D x - \frac{x^2}{2}} \tag{2.6}$$

The maximum field is located at the interface, from (2.5) is:

$$|\mathcal{E}(x=0)| = \frac{2(V_{bi} - V - (kT/q))}{W_D} \tag{2.7}$$

2.1.2 Carrier transport mechanisms

Carrier transport in a semiconductor is due to majority carriers, in our case e^- since n-type semiconductors are taken into account.

It is possible to distinguish four different carrier transport mechanisms:

- Thermoionic emission
- Tunneling
- Recombination

- Diffusion of electrons

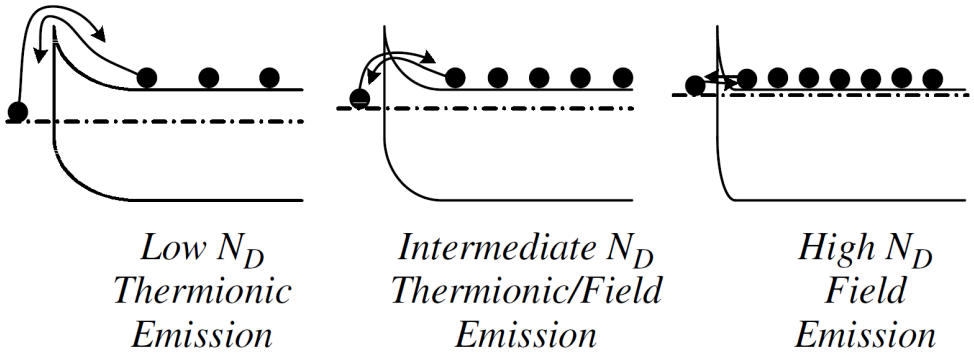


Figure 2.4: Behaviour of different transport mechanisms [44].

Emission of electrons from the semiconductor over the potential barrier into the metal the dominant process for Schottky diodes with moderately doped semiconductors.
Quantum mechanical tunnelling of electrons through the barrier, it is important for this study since it is the main phenomenon in ohmic contacts, high active concentration and thin interface layers are the conditions necessary to have effective ohmic contacts. Recombination can occur in the the space-charge region, similarly to what happens in the p-n junction. Recombination occurs in semiconductors while in metals, which lack a depleted region, we have an injection of carriers, for n-doped metal-semiconductor junction, it is possible to distinguish briefly between the two following cases:

- $q\phi_M > q\phi_S$ rectifying behaviour.
- $q\phi_S > q\phi_M$ ohmic behaviour.

In absence of voltages, diffusion is the main transport mechanism, it can have a role at high temperature.

For this study, we are mainly interested in the quantum tunnelling phenomenon, because it is the main transport mechanism in ohmic contacts, typical for highly doped Si, as in this case of study, the objective is lowering contact resistivity. Ohmic contacts are important since they provide a linear response between current and voltage.

2.1.3 Schottky theory

The different types of transport described above correspond to different I/V characteristics, these are important to understand the working point of our device.

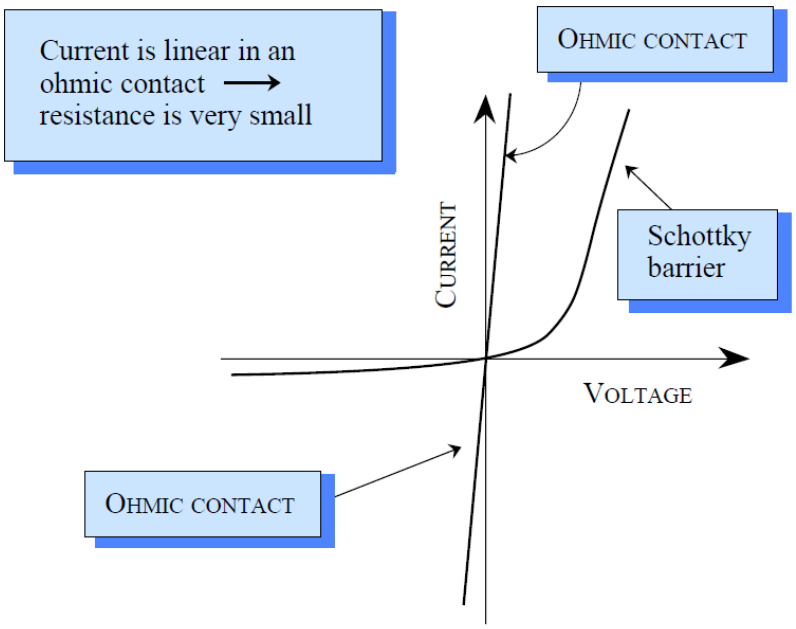


Figure 2.5: Typical I/V characteristic of an ohmic contact.

In rectifying contacts the I/V characteristic is represented by the following equation:

$$I = I_S\left[exp\left(\frac{qV}{nk_BT}\right) - 1\right] \tag{2.8}$$

As discussed before the ohmic contact relies on the tunnel effect, which is enhanced in thin barriers. An ohmic contact is an M-S junction characterised by a negligible junction resistance. Nowadays the contribution of the ohmic contact is not negligible compared to the channel resistance of a device, so this kind of parasitics should be reduced in order to maintain the control of the active region of our device. Ohmic contacts also make possible the linear response as can be seen in figure 2.5 corresponding to:

$$I = \frac{V}{R} \tag{2.9}$$

For an ohmic contact, the resistance can be defined as the reciprocal of the derivative of the current density with respect to the voltage across the interface. Here is the expression for zero bias condition:

$$R_C \equiv \left(\frac{dJ}{dV}\right)^{-1}_{V=0} \tag{2.10}$$

In case of low doping (far from this work) we have thermionic emission:

$$R_C = \frac{k}{A^{**}Tq} exp\left(\frac{q\phi_{Bn}}{kT}\right) \tag{2.11}$$

where A^{**} is the effective Richardson constant:

$$A^{**} = \frac{f_p f_Q A^*}{1 + (f_p f_Q v_R v_D)}; \;\; A^* = \frac{4\pi q m^* k^2}{h^3} \tag{2.12}$$

In the expression (2.11) the contribution of the potential barrier can be neglected, this expression suggests the need of small barrier height to have a small R_C.
For high doping levels (as in our case) the dominant transport mechanism is the field emission $kT << E_{00}$.

$$R_C = \frac{k\sqrt{E_{00}cosh(E_{00}/kT)coth(E_{00}/kT)}}{A^{**}Tq\sqrt{\pi q(\phi_{Bn} - \phi_n)}} exp\left[\frac{qq(\phi_{Bn} - \phi_n)}{E_{00}coth(E_{00}/kT)} + \frac{q\phi_n}{kT}\right] \tag{2.13}$$

In this last expression the most important role is played by E_{00}, which is given by the following expression:

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_D}{\epsilon_r \epsilon_0 m^*_{tn}}} \tag{2.14}$$

Where h is the Plank constant, N_D the donors active concentration, and m^*_{tn} the effective mass linked to electron tunnelling and ϵ_r ϵ_0 the relative and vacuum electric permittivity. For this kind of carrier transport, we have a dependence on the doping concentration $\propto exp(N^{-1/2})$.
Concerning the purpose of the thesis, in order to obtain low contact resistivity it is necessary to have high doping levels and low $q\phi_B$, but this last quantity is almost fixed. [1]

[1] It is considered fixed due to processing techniques, in fact, SiTi silicidation and Cu fix the height of the barrier, which depends on the workfunction of the metal and the semiconductor.

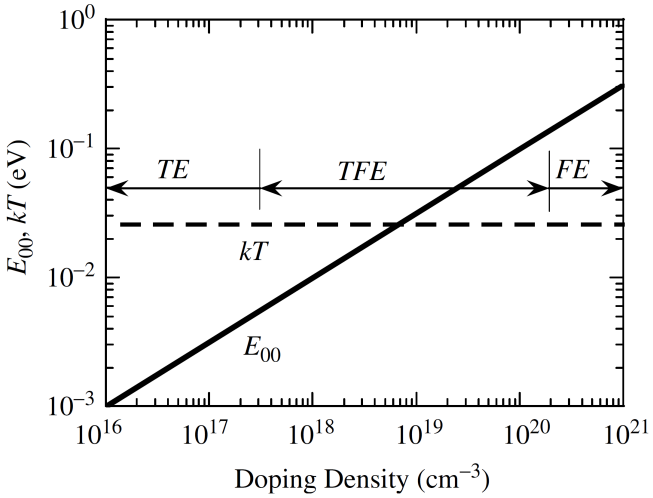


Figure 2.6: E_{00} behaviour vs doping concentration [44].

2.2 Non-idealities

The theory discussed is related to an ideal case, but in the real case, several non-idealities need to be taken into account:

- Surface states
- Image force lowering
- Barrier height adjustment

2.2.1 Surface states

In the ideal case, ϕ_{Bn}, the barrier confining the carriers is uniquely determined by the difference between metal work-function and semiconductor affinity. But in the real case, the interfaces are not perfectly free from defects leading to surface states, which are often called defect-induced states. Defects result in additional states available for charges, so these states contribute to determining the barrier height for electrons since they provide surface peaks.
The surface peaks can trap a charge, they are generally located slightly above the valence band E_V and an energy called $q\phi_0$, which is a figure of merit since above this energy level the states are acceptors type (negatively charged when occupied and neutral when empty), while below the states are donors type (neutral when full and positively charged when empty). The ideal case corresponds to the Fermi level coinciding with $q\phi_0$, this condition results in a

null interface-trap charge.
Surface states are difficult to be analysed and in general, only empirical pseudo-potential models provide reliable results. They are considered responsible for the Fermi level pinning, the phenomenon that leads to Fermi level being located slightly above E_V.

2.2.2 Image Force Lowering

The Image force Lowering is the image force-induced lowering of the barrier energy due to charge emission, in fact, the charge emitted in the semiconductor will induce a charge in the metal at a distance x from the surface.

This positive charge results in a lowering of the potential due to image force given by:

$$F = \frac{-q^2}{4\pi\epsilon_0 x^2} \tag{2.15}$$

This effect can also lead to changes in the static permittivity ϵ_s due to the electron transit time in the metal, but it is generally negligible for Si.

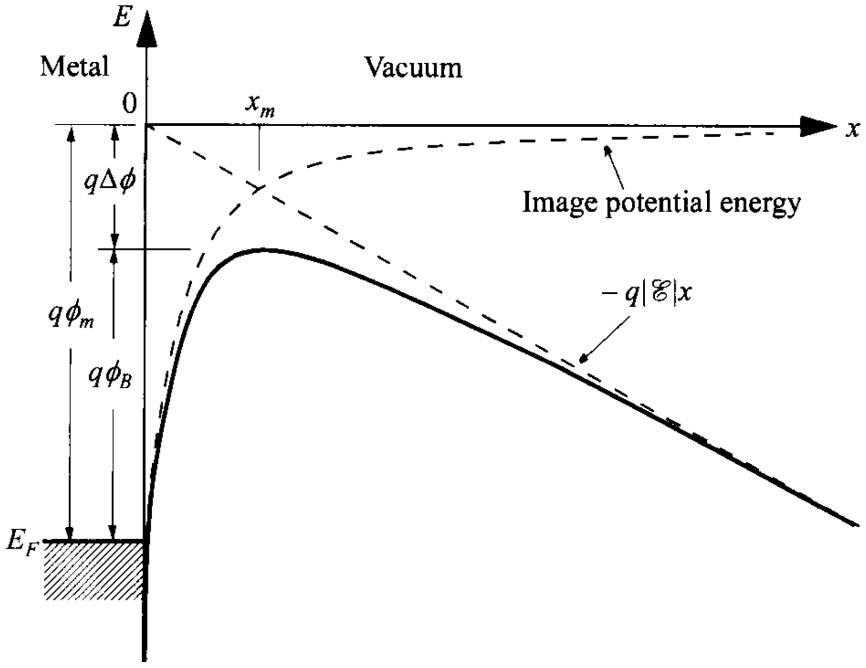


Figure 2.7: The image charge resulting in lowering the barrier in a position x from the barrier [44].

2.2.3 Barrier height adjustment

The Schottky barrier is ideally fixed by the metal and the semiconductor workfunctions, but considering interface states the barrier is less sensitive to doping. The deviation from the ideal case can be taken into account from the following equation:

$$S = \frac{d\phi_{Bn}}{d\phi_M} \tag{2.16}$$

The value of S is the numerical representation of how much the Fermi level changes varying metal work-function (so the metal itself). Making S equal to 1 it is possible to obtain an ideal contact, while a negligible value of S results in Fermi level pinning. This approach is useful because, taking into account non-idealities, is possible to choose the correct metal for device operation. Another additional consideration is related to Silicidation processes, whose implementation started in the early beginning of the 2000s, they have the important role to make the Schottky barrier stable and reproducible since the reaction chemistry is well defined for this class of contacts. However, this processing step will be taken into account in this discussion since it also adds a thermal budget, which induces changes in the grown layers.

3 Methodology

In this chapter, the experimental details are reported, in particular, the growth techniques and the metrological details.

Figure 3.1: ASM Intrepid XP^{TM} is the CVD reactor used for the depositions. It is designed for 300mm wafers production [32].

3.1 Epitaxy

Epitaxial growth is the deposition of a material on a crystalline substrate, such that the ordering of the underlying material is preserved. Epitaxy consists of two categories [24]:

- **Homoepitaxy** if the grown layer is characterized by the same material of the substrate: in this case, there is no lattice mismatch.
- **Heteroepitaxy** if the layers are realized by different materials, in this case, lattice mismatch needs to be taken under control.

In the case of this study, it is considered Group IV Homoepitaxy since n-Si epitaxial layers are grown on Si substrate. There are two main techniques: Chemical Vapor Deposition (CVD) and Molecular Beam Epitaxy (MBE), while the first one is the most used in consumer production, the latter is not suitable for production since it has a limited throughput and it requires a long time to process.

3.1.1 Chemical Vapor Deposition

CVD is a process in which a heated substrate is exposed to one or more volatile precursors. The deposition is controlled by chemical reactions and it can be employed in several conditions, such as dielectrics, conductors and coatings [24]. The result is a thin film. In case the film is epitaxially grown on a substrate the process is referred to as vapor phase epitaxy (VPE). Metal-organic (MO)CVD is a particular case of CVD characterised by a particular nature of the precursor, which are metal-organic compounds.

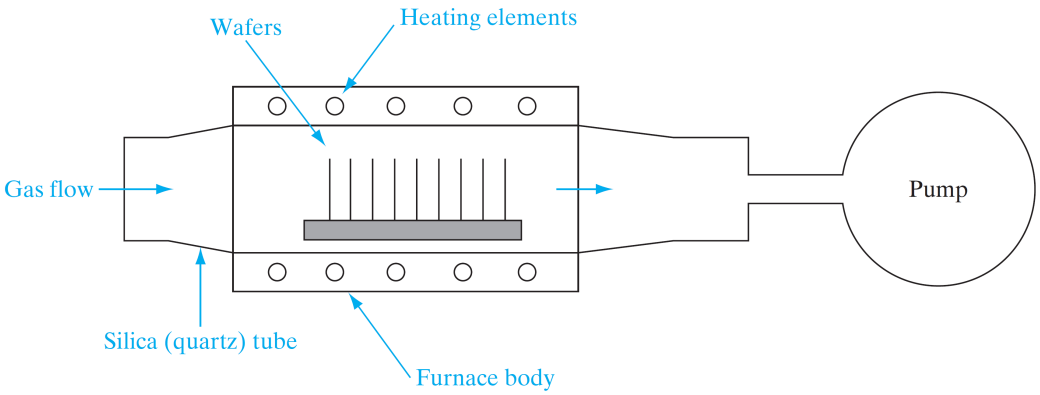


Figure 3.2: This is a general CVD reactor scheme [42].

CVD involves different steps:

- reactant introduction in the substrate region;
- adsorption of reactants on the substrate surface;
- chemical reaction and growth of the epitaxial layer;
- desorption of reactions material;
- transport of the by-products out of the reaction chamber.

Reactions are thermally driven, it is possible to use on a wide range of temperatures. Heating in this case is photo-assisted. The configuration is flexible, the number of chambers and reactants can be varied. This technique is versatile and cheaper, but it is based on complex chemical reactions, which are difficult to be tuned and affects the quality of the material grown.

3.1.2 Set-up

For this work, epitaxial layers are grown in a 300mm Intrepid XP RPCVD reactor. A new gas line was is added in order to use two dopant gases (1% AsH_3 in H_2 and 15% PH_3 in H_2) at the same time. Two different processes are investigated:

- A standard selective process 670 °C
- A non-selective process 450 °C

Both these two processes are run in a RPCVD reactor. For the selective process at 670 °C, $SiCl_2H_2$ (DCS) was used as the Si precursor combined with HCl. For the non-selective process at 450 °C, Si_3H_8 was used as Si precursor. For both processes H_2 was the carrier gas. Before the actual growth there is an in-situ H_2-bake at 1050 °C to remove the native oxide.
In this work two different types of wafers substrate are used:

- 300 mm $<100>$ PMON wafers used for blanket deposition (P type, $\rho = 1 \div 100\Omega.cm$).
- Calypso mask wafers used to implement Circular Transmission Line measurements (CTLM) to measure contact resistivity.

Calypso mask allows CTLM with only one additional lithographic step.

3.2 Measurement and analysis techniques

In this section measurement and analysis, details are discussed in order to provide the reader with the method used.

3.2.1 Atomic Force Microscopy

Atomic Force Microscopy (AFM) is a measurement technique which implies interatomic forces to reconstruct the surface topology of conducting and semiconducting materials.

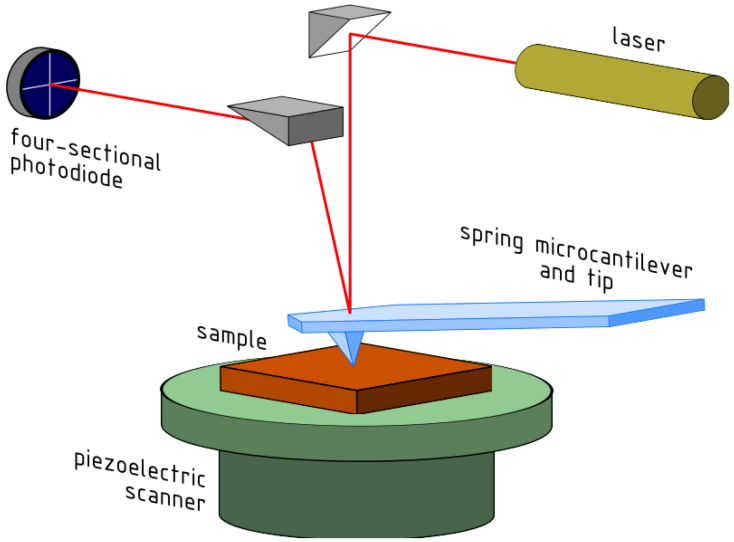


Figure 3.3: Atomic Force Microspopy block diagram.

It consists of a spring-like cantilever moved by a support with sharp edges, fixed to the free end of the cantilever. The role of the probe is to measure the Van der Waals forces between the probe and the sample.
The probe is placed at a short distance (10 nm) and it scans the surface area. A laser beam is directed towards the reflective cantilever on which the tip is placed and its reflection is detected by a photodiode. During the scan the cantilever bending, due to the surface roughness, affects the motion of the tip which is detected by the photodiode.
The image is created by scanning the sample on an X-Y grid and by reconstructing the surface pseudo-image. After sampling the tip is restored to its default position. It is important to have a constant deflection during the motion in order to have a correct measurement and not to damage the sample or tip.

3.2.2 Secondary ion mass spectrometry

Secondary ion mass spectrometry (SIMS) is a spectroscopy technique. It allows to characterise the composition of the layer through the detection of different elements with a high depth and density resolution. By measuring the depth of the signal using a detector, the thickness of the layer can be derived.

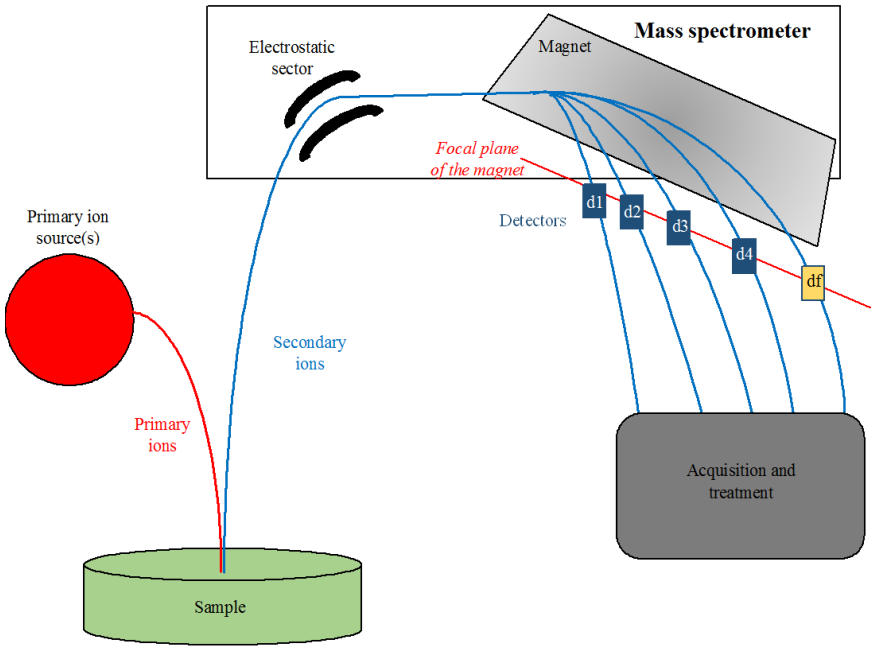


Figure 3.4: Secondary ion mass spectrometry block diagram.

An ion gun generates a primary beam accelerated towards the sample surface, the sample is kept under high vacuum. The ion beam hitting the sample leads to eject charged particles (Secondary Ions). The emitted ions are analysed using a high electrostatic potential slit and a mass spectrometer. Backscattered ions then pass through a magnetic field determining the mass charge ratio.

$$\frac{m}{q} = \frac{B^2}{2V} \times r^2 \tag{3.1}$$

Using a mass detector it is possible to determine elemental and isotopic composition. This technique is considered the most sensitive surface micro-analysis with a resolution of 0.5 to 5 μm and a depth resolution $\sim 1\ nm$.

3.2.3 Rutherford Backscattering Spectrometry

Rutherford Backscattering Spectrometry (RBS) is a quantitative technique to analyse the depth profiles of the atoms of a solid [17]. It is widely used to analyse thin films and ion implanted materials. This technique is based on the scattering of light particles.
A collimated beam of mono-energetic He^+ ions is accelerated by the Pelletron accelerator and brought into the scattering chamber, where the samples are located, mounted on a 3-axis goniometer. For well realized epitaxial thin films , only a small fraction of the impinging ions is backscattered. The backscattered ions are used to have an energy spectrum used to extract the energy transfer during the collision, which depends on the mass of the scattering atom M_{atom}, once M_{atom} is known, it is possible to find the information related to the depth profile related to electronic stopping and then the concentration of atoms in the sample, by means of the Rutherford cross-section formula.

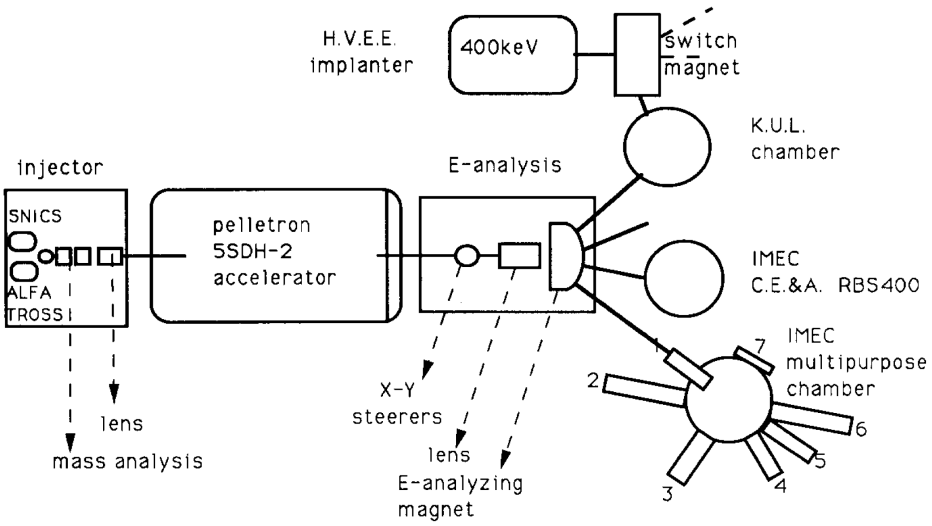


Figure 3.5: Rutherford Backscattering Spectroscopy set-up [4].

The energy of the backscattered He^+ ions is measured with two Silicon Surface Barrier detectors, placed at a fixed angle with respect to the incoming ion beam, for optimal mass resolution, and at a variable angle, for improved depth resolution.
If the incoming beam is aligned with a major crystallographic direction of a single crystalline target, the backscattered yield is decreased, because the incoming ions follow a path where the probability of a direct collision is reduced, this phenomenon is called ion beam channeling. From channeling

measurements, the information concerning the crystalline quality of the lattice is extracted. In fact this technique is used to determine the lattice site of the implanted impurities. For the purpose of this work RBS channeling measurements are used to determine the crystalline quality, so the minimum yield χ_{min} will be a figure of merit.

3.2.4 High resolution X-Ray Diffraction

High resolution X-Ray Diffraction (HR-XRD) is a versatile technique used to investigate the crystalline structure, the purity of the sample, the lattice mismatch and the related stress and strain of the layer.
Electrons in a crystalline structure scatter light coherently. This technique is based on constructive interference of monochromatic X-rays, produced by means of a cathode ray tube. Constructive interference occurs when Bragg's condition is verified, corresponding to the next equation:

$$n\lambda = 2dsin\theta \tag{3.2}$$

This condition is a strong statement involving the specific wavelength λ of the ray collimated on the sample and the diffraction angle θ. Since crystals are periodic structures so λ is similar to the distance between atoms, the X-rays are detected by scanning the sample of 2θ. Measured peaks can be compared to reference diffraction patterns.

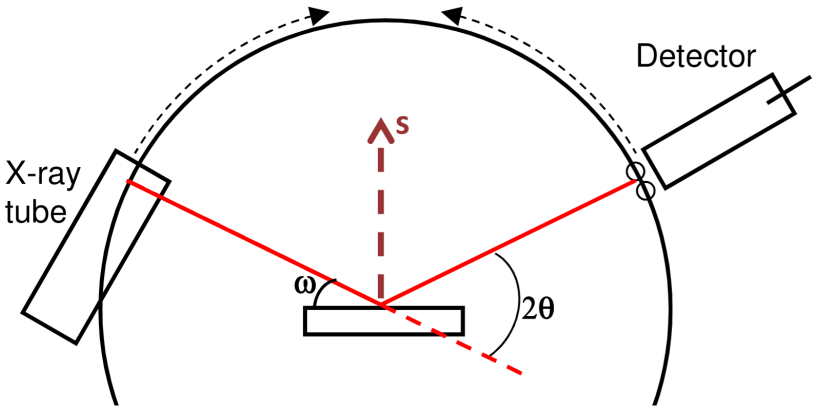


Figure 3.6: X-Ray Diffraction schematic.

The angle ω is the angle of the source and θ the angle of the detector which also scans the intensity, determining the presence of the specimens. Numerical analysis of the 1D diffraction pattern allows a refinement of the

lattice parameters.
Employing calibration curves based on the equivalent substitutional Carbon analysis is possible to investigate the abundance of substitutional dopants.

3.2.5 Micro-four-point probe measurement

Micro-four-point probe (M4PP) is a technique used to measure sheet resistance, in this case for blanket wafers since the thickness is uniform. After thickness measurement from i.e. SIMS it is possible to extract the resistance of the layer. Sheet resistance is expressed as follows:

$$R_S = \frac{\rho}{t} \tag{3.3}$$

Where t is the thickness of the layer.
This technique is useful to have a first idea of the characteristic of the layer since it can be done in-line. The set-up in figure 3.7 shows the configuration of the probes, 4 point measurements allows high precision since the parasitic contribution of the tip is removed due to the configuration and, if the spacing of the tip is smaller than the thickness layer, it is correct to assume the voltage located across the surface and the measured current free from leakages contributions due to bulk.

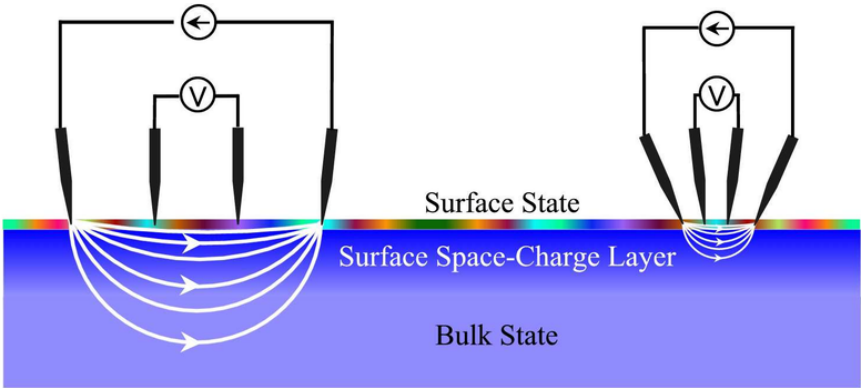


Figure 3.7: In this picture on the left there is macro 4 point probe, while on the right there is a micro 4 point probe configuration.

In addition to this measurement technique, Micro-Hall Effect (MHE) measurement are done on discrete samples using the CAPRES CIPtech-M300 tool [33].

3.2.6 Micro-Hall effect measurement

The Micro-Hall effect (MHE) measurement is a powerful technique which can be used to extract important quantities to characterise the layer, such as the sheet carrier density N_S, corresponding to the active fraction of the doping concentration and the mobility μ.
The MHE tool relies on a microscopic 7-point-probe, and a strain gauge for the surface detection. For each Hall measurement a series of 7 electrical measurements are performed using three different tip configurations. Each time a predefined current is pushed through two of the tips and the voltages are measured between the two other tips.

Figure 3.8: Hall measurement on a discrete coupon, 7-point-probe.

This technique is similar to the M4PP discussed in the previous section. But in this case the probe is parallel and near an insulating boundary and an orthogonal magnetic field is applied. Hence the resistance measured has three contributions: a drift term R_S, a term related to magnetic induced resistance and Hall term R_H. They can be expressed as follows [34]:

$$R_H = \frac{r_H B_Z}{Z_e N_S} \tag{3.4}$$

$$R_S = \frac{1}{e\mu N_S} \tag{3.5}$$

Where B_z is the orthogonal magnetic field, Z can assume a value equal to ± 1 depending on the charge type and e is the elementary charge, while r_H is the Hall scattering factor (HSF).
It is demonstrated by Del Alamo et al. [11] that HSF saturates to a value slightly higher than 0.9 for highly doped semiconductors with considerable error bars, it is necessary to notice that the article is related to a full ionization condition and to doping concentrations lower than the solid solubility of Si, hence in this work the HSF is considered equal to 1, measurements are performed on CAPRES CIPtech-M300, suitable for discrete and 300 mm wafers measurements.

3.2.7 Multi-Ring Circular Transmission Line Model

The MR-CTLM technique is among the TLM (Transmission Line Models) based measurement techniques [51]. Transmission models rely on a lumped model as the one proposed for transmission lines solutions, shown in figure 3.10. This method has been used to evaluate contact resistivity.

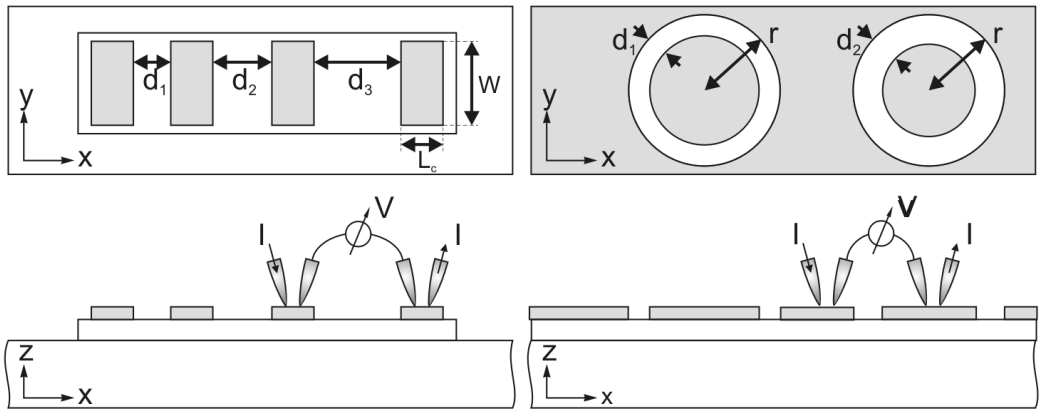


Figure 3.9: Test patterns for TLM (left) and Circular-TLM (right).

it is based on the solution of Telegrapher equations, which can be reduced to the following system:

$$\begin{cases} v(x) = v_1 \cdot cosh(\alpha x) - i_1 \cdot Z sinh(\alpha x) \\ i(x) = i_1 \cdot cosh(\alpha x) - \frac{v_1}{Z} \cdot sinh(\alpha x) \end{cases} \tag{3.6}$$

$v(x)$ is the voltage drop on the interface and $i(x)$ the current along the line, C and G are the admittance component, a capacitance and a conductance per

unit length, while the R_S is the resistance per unit length of semiconductor layer, which is the variable of interest, the metal resistance is considered negligible.

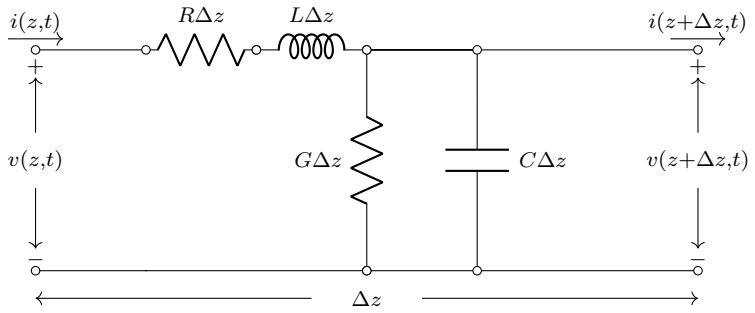


Figure 3.10: Lumped model for transmission lines.

where Z is the characteristic impedance:

$$Z = \frac{1}{w}\sqrt{R_s \rho_c} \tag{3.7}$$

and α the attenuation constant:

$$\alpha = \sqrt{\frac{R_s}{\rho_c}} \tag{3.8}$$

It is important to underline that this discussion is related only to this specific geometry, rectangular with length L and width W since the potential is derived from the model related to a rectangular transmission line:

$$V(x) = i_0 R_s \frac{L_T}{Z} \frac{cosh(x/L_T)}{sinh(W/L_T)} \tag{3.9}$$

Where L_T is the transfer length, it is an important figure of merit since it represents the portion of the contact where the majority of the carrier flows.

$$L_T = \sqrt{\frac{\rho_c}{R_s}} \tag{3.10}$$

From this expression is possible to extract the contact resistivity ρ_c. The previous steps are related to a rectangular structure, while in this work a circular structure is used (multi-ring), hence it is necessary to change the voltage expression:

$$\Delta V = \frac{i_0 R_s}{2\pi}\left[ln\left(\frac{r_1}{r_0}\right) + \frac{L_T}{r_0}\frac{I_0(r_0/L_T)}{I_1(r_0/L_T) + \frac{L_T K_0(R_1/L_T)}{r_1 K_1(r_t/L_T)}}\right] \tag{3.11}$$

In this last expression I_0, I_1 and K_0 K_1 are the modified Bessel Functions and r_0 r_1 are the radii spaced by S.

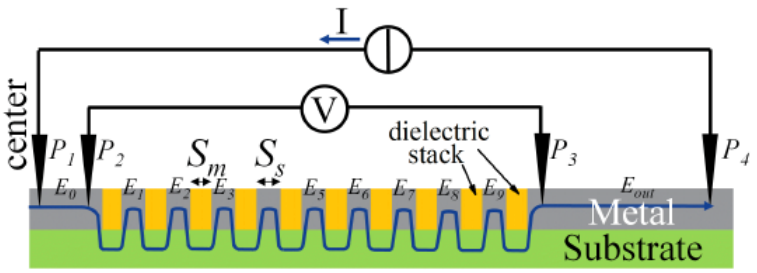


Figure 3.11: MR-CTLM measurement set-up, two probes inject current in the structure and two probes measure the voltage [51].

Multi-Ring Circular Transmission Line Model (MR-CTLM) represents a good compromise for contact resistivity extraction since it is more accurate than simple CTLM and much less complex than the Refined Transmission Line Model [51]. In figure 3.12 there is an example of a multi-ring structure.

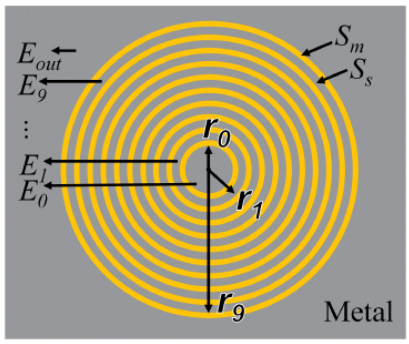


Figure 3.12: An example of multi-ring structure [51].

The resistance of 8 different multi-ring structure, characterised by different spacing, is measured. Practically a current flow is imposed through two probes, between the centre of the structure and the edge at $\approx 300\mu m$ and two additional probes measure the voltage. The resistances are data points for the extraction of the contact resistivity, in fact, for ohmic contacts, they will lay on a straight line where R_C will be the intercept since it is the limit

for the width tending to 0.
For such a small structure, the metal contribution cannot be considered negligible, so its contribution is taken into account by measuring six metal pads, which resistance is then averaged and subtracted to the final semiconductor one. In this work, a 10-ring structure is considered leading to the following computation [51].

$$R_t = R_e + R_p \tag{3.12}$$

where:

$$R_e = \frac{R_s}{2\pi}\Sigma_{i=0}^{9}\left[ln\left(\frac{r_i + S_m}{r_i}\right) + L_t\left(\frac{1}{r_i} + \frac{1}{r_i + S_m}\right)\right] \tag{3.13}$$

$$R_p = \frac{R_m}{2\pi}\Sigma_{i=0}^{9}\left[ln\left(\frac{r_i - L_t}{r_i}\right)\right] \tag{3.14}$$

Where R_p and R_e are, respectively, the parasitic resistance due to the metal and the effective resistance of semiconductor, these two terms can be decomposed since the metal resistance is much higher than the effective resistance.

4 Experimental Results

In this chapter, the experimental results are discussed. Experiments can be divided in two categories related respectively to the blanket layers and the patterned structures.

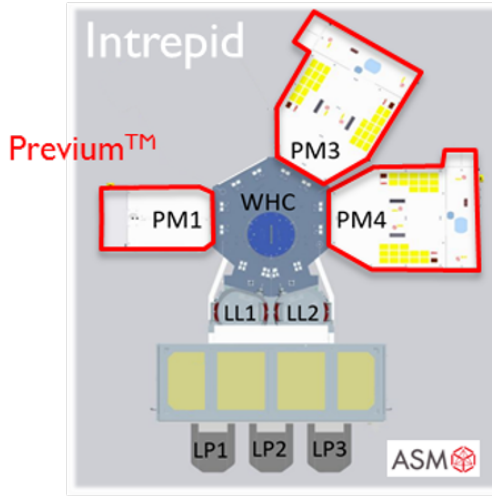


Figure 4.1: In this picture there is the ASM Intrepid XP™ configuration. PM4 is the chamber used for the experiments.

Samples can be divided into two classes: the layers grown at 670°C and 450°C, grown in 300mm ASM Intrepid XP. In both cases, samples range from pure As doping to pure P, in between several solutions of co-doping As + P are discussed. The total concentration ranges typically from 1% to 4% to cover a full spectrum of industrial purposes. Experiments in this work are focused on the characterization of the layers' morphological and electrical properties and the understanding of the undergoing physical phenomena.

4.1 Analysis on blanket layers

The samples analysed are listed in the following table, where LA refers to laser-annealing by Astra Vantage DSA at 1200 °C, $\tau = 0.5\ ms$. Part of the measurements are performed in-line while others are performed on cleaved samples.

Table 4.1: Blanket layers' Split table

670 °C		450 °C	
Condition	$D_{[chem]}$	Condition	$D_{[chem]}$
Si:As	1.2%	Si:As	1.2 %
Si:P/Si:As	Si:P(3%)/Si:As(1.2%)	Si:P:As	0.3 % P + 0.9 % As
Si:P:As	3% P + 0.2%	Si:P:As	0.55 % P + 0.65 % As
Si:P:As	3% P + 0.6%	Si:P:As	0.9 % P + 0.3 % As
Si:P	3% ref	Si:P	1.2%

4.1.1 Morphological and structural analysis

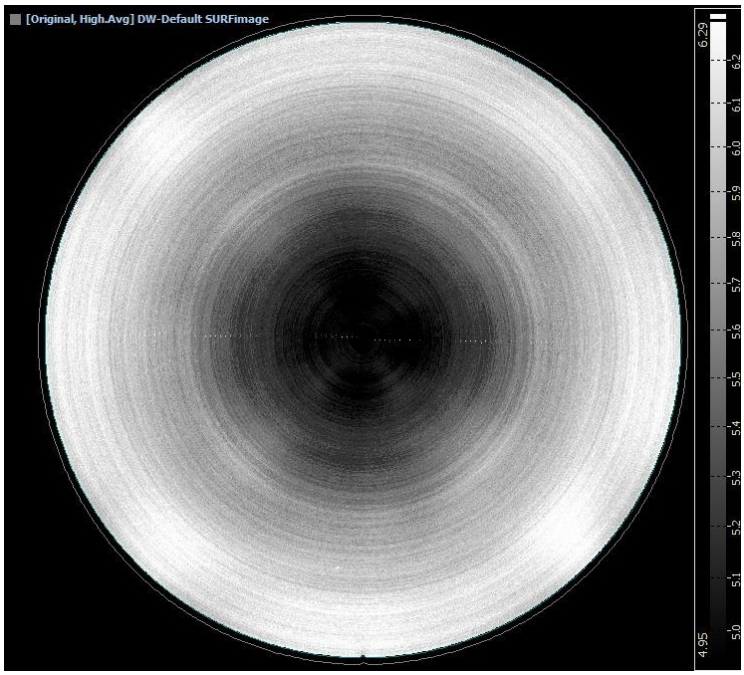


Figure 4.2: SP3 haze inspection, this sample is characterised by 3% P + 0.6% As, defectivity of the sample is not affected by As addition.

Morphological analysis requires different techniques. A first characterization is made by Haze maps, which are useful to understand if damages have occurred during processing, to detect defects and to understand the uniformity of the layers. Two kinds of data can be observed, the ones related to DN (narrow detector) and the ones related to DW (wide detector).
In figure 4.2 there is a scan related to 670 °C grown co-doped sample. At first, it is necessary to assess if the As addition in small quantities does affect the morphology and uniformity of the sample. There is a small variation in the thickness of the layers, it is comparable to the other conditions and it can be explained due to a small variability in the process and not to the co-doping technique, in 450 °C grown samples defectivity is lower due to both lower D_{chem} concentration and to the process conditions.

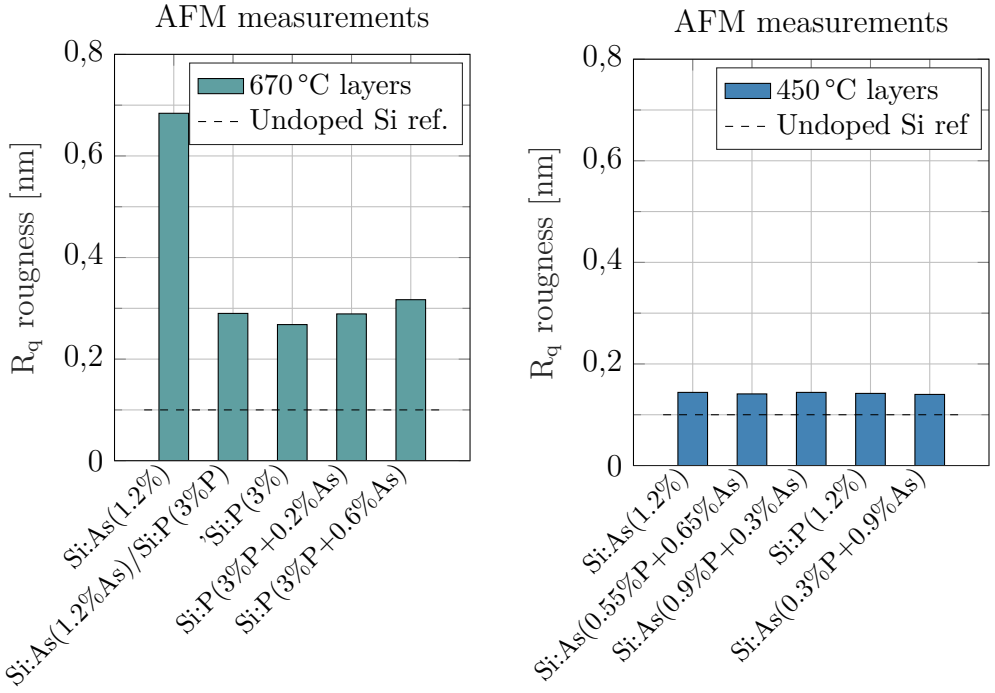
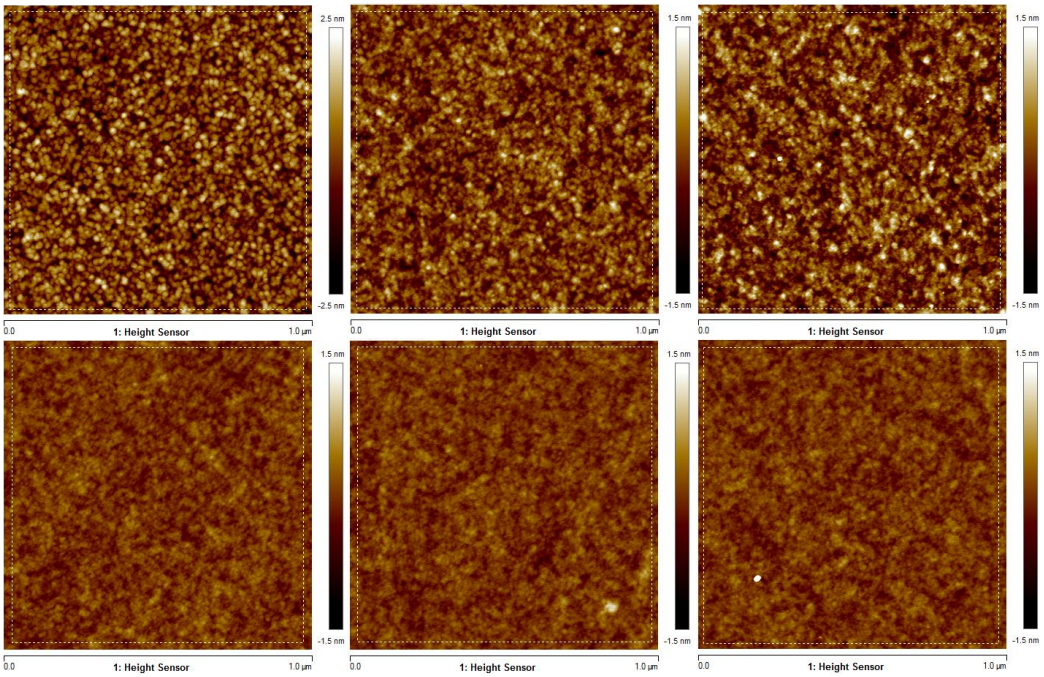


Figure 4.3: For 670 °C grown layers, co-doped layers are similar to P doped reference since the As addition is small, the variation in R_q can be related to the higher total concentration. All the layers grown at 450 °C show low roughness values, which can be attributed both to the low total concentration and the process conditions.

AFM is used to characterise the surface roughness of the samples (fig. 4.3). Pure Si:As grown at 670 °C layers are rougher than Si:P, which indicates that

the layers are slightly more defective. R_q is generally a bit larger compared to the un-doped Si reference. It is observed a slightly larger R_q for the selective process compared to the non-selective process.

Si:As(1.2%) 670 °C	Si:P(3%) 670 °C	Si:P:As(3%P+0.6%As) 670 °C



Si:As(1.2%) 450 °C	Si:P(1.2%) 450 °C	Si:P:As(.9%P+0.3%As) 450 °C

Figure 4.4: AFM surface reconstruction shows on top 670 °C grown samples and 450 °C on bottom.

The good crystalline quality is confirmed by the Rutherford backscattering analysis, from which the minimum channeling yield is extracted, this parameter represents the ratio between the ions backscattered from the layer and the ions which are channeling through the lattice. The minimum channeling yield (χ_{min}) is an important figure of merit and the smaller it is the better is the crystalline quality. It is of primary importance to understand the impact of As addition to the Si:P layers. Angular yield scans (AYS) have been done on the Si bulk. Once aligned, channeling measurements are done and compared to the random rotation measurement.

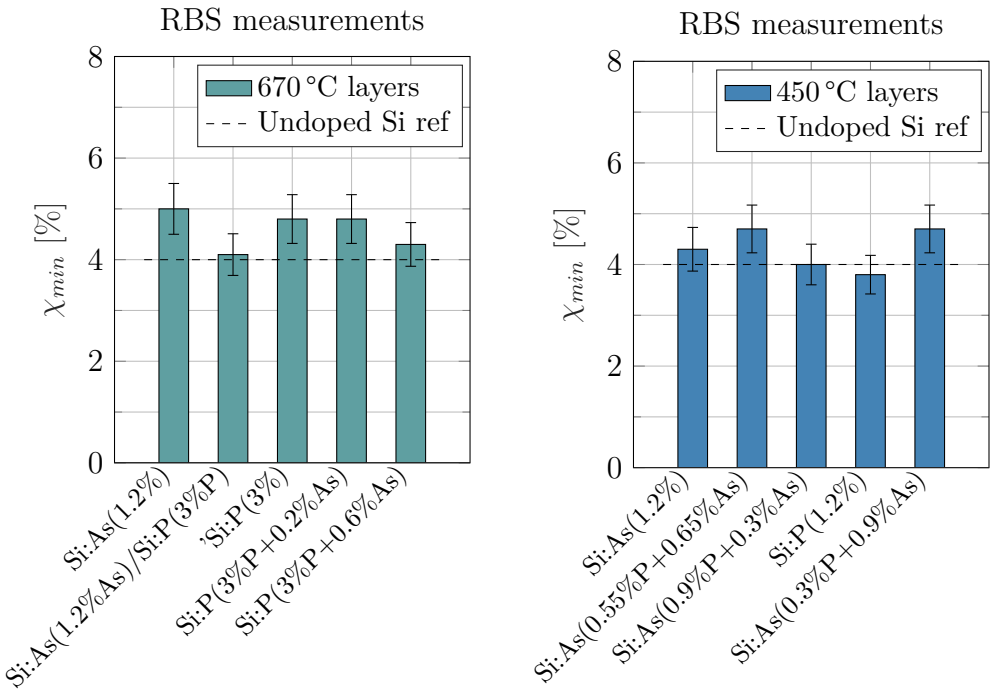


Figure 4.5: RBS minimum channneling yield.

From the analysis, shown in figure 4.5, we do not observe a very high difference between Si:As, Si:P:As and Si:P layers. Within the errorbars, the results are all comparable and are close to the value for a bare substrate ($\chi_{min} \sim 4\%$).

4.1.2 Compositional analysis

SIMS analysis is used to determine the composition of the layer. This kind of analysis is particularly useful for new processes to assess the output concentration with respect to the gas flow.
Doping profiles, extracted from SIMS analysis, confirm that the samples are on the target concentrations reported in table 4.1. Data refers both to the laser annealed and the as-grown region of the sample, which allows to understand the diffusion behaviour of the layer after the laser thermal budget. These conditions are chosen to restrict the field of interest since they are the most representative, in fact, for layers grown at 670°C laser annealing enhances the active concentration consistently, representing the

ideal case of use and LA provide a sufficient thermal budget to appreciate diffusion. Further considerations can be found in the section related to the Hall measurement.

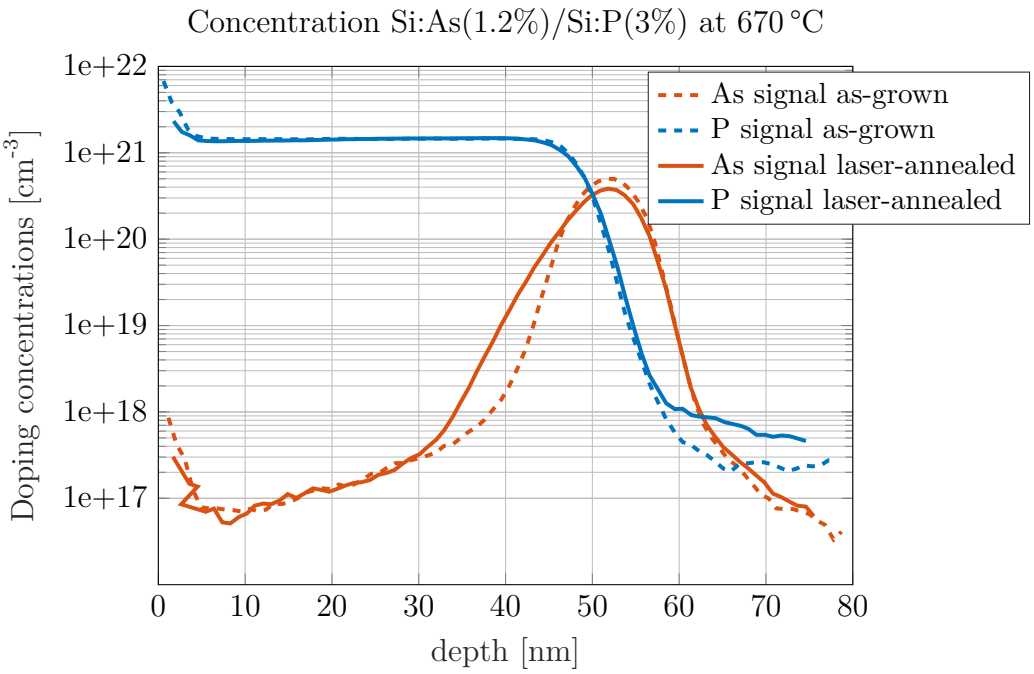


Figure 4.6: This image shows the SIMS profile for the bilayer, as-grown as dashed lines and laser-annealed as solid lines.

In figure 4.6 a bilayer is shown, it is characterised by $10nm$ Si:As at the bottom and $50nm$ Si:P on top. From this analysis, it is possible to notice that, after laser annealing, As diffusion occurs asymmetrically on the left-hand side. It is possible that As diffuse in the Si:P layer due to an excess of vacancies released by P-V complexes upon anneal as reported in [40]. This phenomenon make Si:As layers good candidates as stop liner, similarly to what is reported by Mochizuki et al. [26], where Si:As is used in modulating SCE, allowing the R_{ON} maintaining the DIBL behaviour.
In figure 4.7 and 4.8, it is possible to appreciate the smooth profile obtained with the current process. Even if in figure 4.7 is represented pure Si:P, a negligible As signal is present, depending on the impurities in the chamber. In all the images a small tail is present at the beginning, this is an artefact from SIMS measurements due to the windowing.

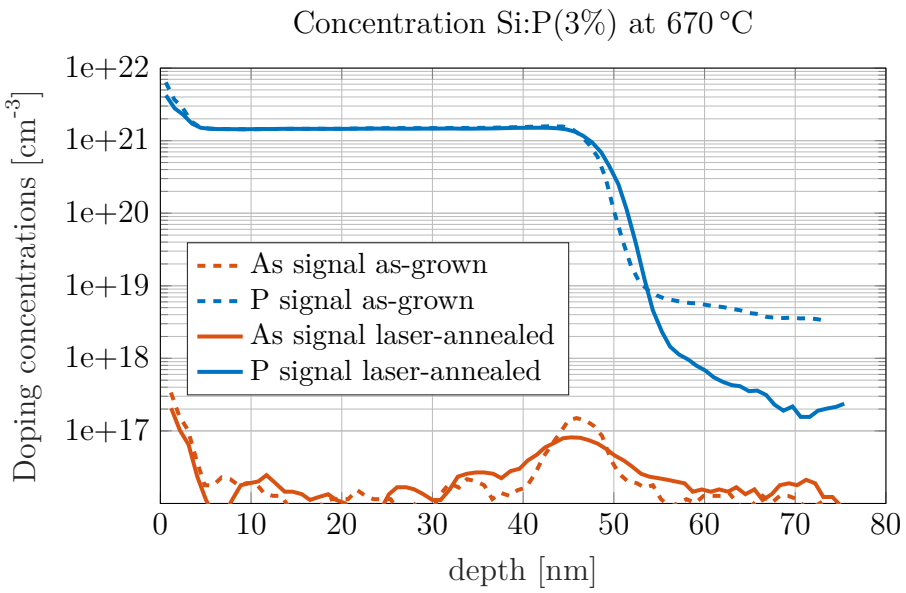


Figure 4.7: This image shows the Si:P(3%) reference layer.

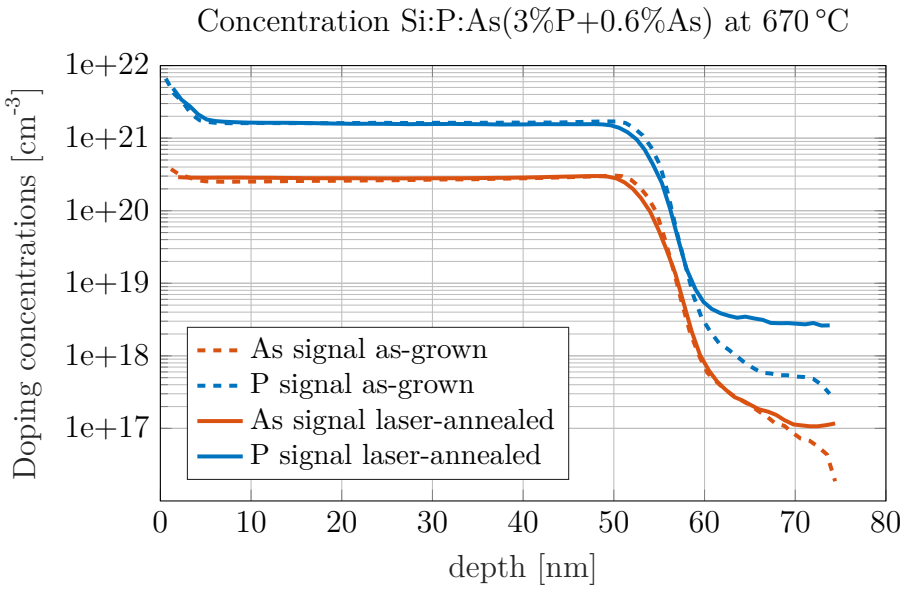


Figure 4.8: This image shows a co-doped layer characterised by a concentration 3% P and 0.6% As.

Table 4.2: Layers' thickness

670 °C				450 °C			
		Width [nm]				Width [nm]	
Condition	$D_{[chem]}$	LA	As-grown	Condition	$D_{[chem]}$	LA	As-grown
Si:As	1.2% As	30	29	Si:As	1.2% As	41	41
Si:P/Si:As	Si:P(3%)/Si:As(1.2%)	58	59	Si:P:As	0.3% P + 0.9% As	41	41
Si:P:As	3% P + 0.2% As	53	52	Si:P:As	0.55% P + 0.65% As	41	41
Si:P:As	3% P + 0.6% As	55	57	Si:P:As	0.9% P + 0.3% As	38	38
Si:P	3% P ref	52	49	Si:P	1.2% P	40	40

4.1.3 Thermal stability

Production of microelectronic circuits relies on multiple steps, after layers deposition, additional thermal budgets are required for oxide deposition, patterning and metalization. Understanding layers stability is of primary importance.
To understand thermal stability small coupons were cleaved and exposed to different temperatures and times using Rapid thermal annealing (RTA) in a AW Heatpulse 610 System. Annealing was done in N_2 at 400 °C, 500 °C, 600 °C, 700 °C for 15s, 30s and 60s. Afterwards micro-Hall measurements were performed to determine the active concentration.

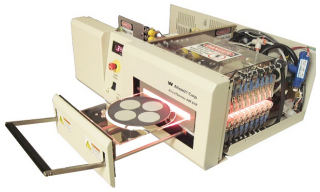


Figure 4.9: AW Heatpulse 610 System

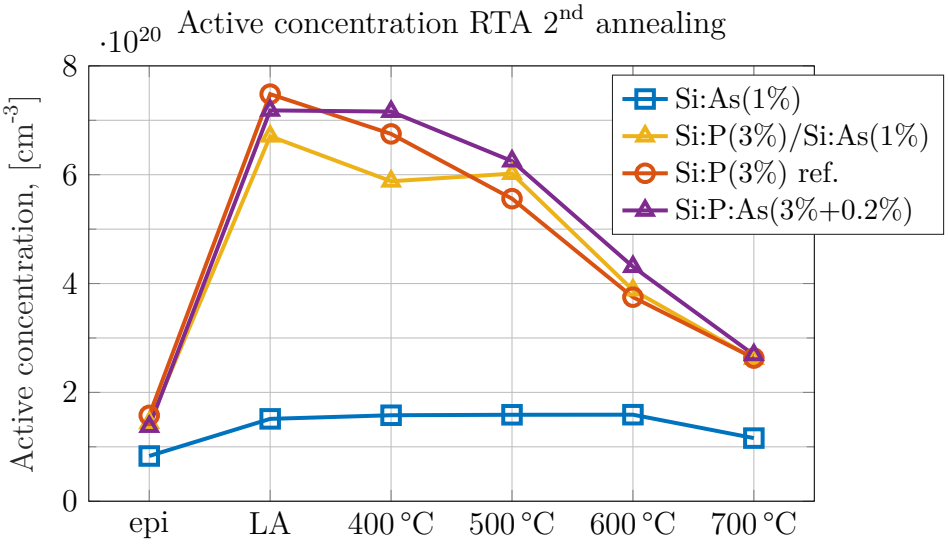


Figure 4.10: Active concentration decay for 60s RTA.

In figure 4.10 it is possible to observe the effect of laser annealing and RTA exposure at 400 °C ÷ 500 °C, 60s anneal after LA. It can be observed that LA increases the active concentration while post anneal reduces the active concentration, it is shown in figure 4.12 and 4.13 the active concentration decrease appears also for small time RTA exposure. As addition provide improved stability till 600 °C which are more representatives of silicidation procedures and in general post epitaxial growth processes. Purely Si:As layers seems to be highly stable, but the sample available was at lower total

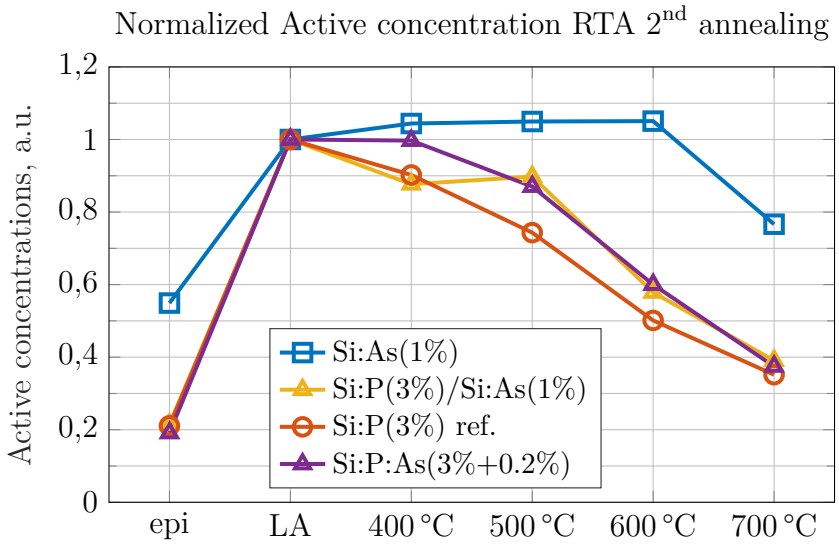


Figure 4.11: Normalized active concentration decay for 60s RTA.

concentration, for higher total concentration new experiments are needed. For what concerns 450 °C grown layers they are generally more stable with respect to the 670 °C grown counterparts.

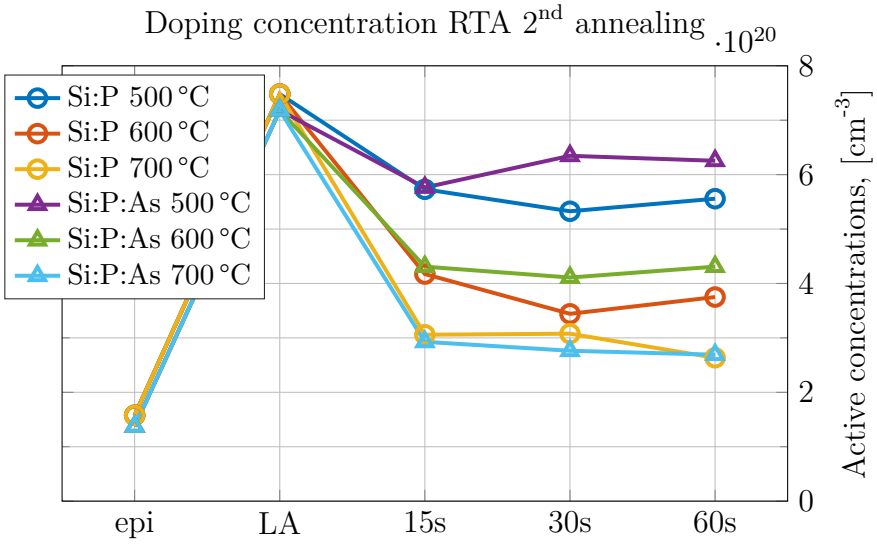


Figure 4.12: Active concentration after different times RTA exposure.

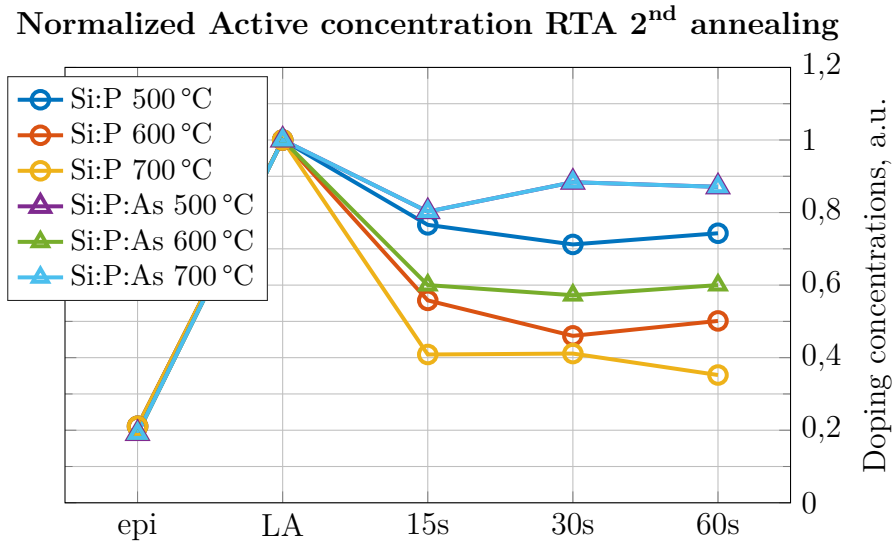


Figure 4.13: Normalized active concentration after different times RTA exposure.

4.2 Resistivity evaluation

In this section, resistivity is evaluated for blanket layers and MR-CTLM patterned structures. DSA 1200 °C (2x0.5ms) laser-annealing is applied on the north half of the wafer while the south half is kept as-grown. CTLM conditions are reported in the following table.

Table 4.3: CTLM Split table

670 °C		450 °C	
Condition	$D_{[chem]}$	Condition	$D_{[chem]}$
Si:As	1% As	Si:P	1% P
Si:P:As	0.5% P + 0.5% As	Si:P:As	0.75% P + 0.25% As
Si:P	1% P	Si:As	1% As
Si:As	2% As	Si:P	3% P
Si:P	3% P	Si:P:As	1.5% P + 1.5% As
Si:P:As	3% P + 0.3% As	Si:As	3% As
Si:P:As	3% P +0.6% As	Si:P	4% P

4.2.1 Blanket layers

Once the SIMS profile is measured it is possible to know the thickness of the layers, which is used to extract the resistivity. In fact, by means of MHE we measure the sheet resistance R_s and then the resistivity is extracted as follows:

$$\rho = R_S \cdot t \tag{4.1}$$

Figures 4.14 and 4.15 show the active concentration and resistivities related to layers grown at 670 °C. The measurements confirm that laser-annealing lead to beneficial effects both in terms of active concentration and resistivity. This indicates that the majority of the P is electrically inactive after epitaxial growth. As addition does not lead to strong improvements compared to the reference and LA on purely Si:As layers improve only slightly the active concentration. Si:As layers seem to be less sensitive to thermal budgets. Furthermore, it is worth to notice that even though the total concentration is higher in co-doped layers, active concentration seems to saturate in the range of $7 \div 8 \cdot 10^{20} cm^{-3}$. The trend seen for active concentration is found in the resistivity, so As addition slightly increases the resistivity [40].

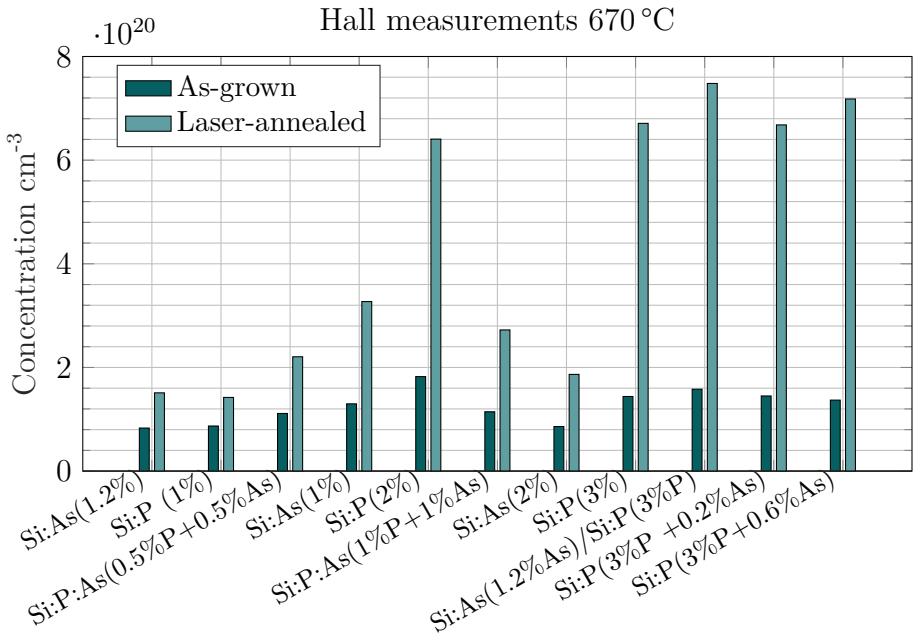


Figure 4.14: Active concentration related to layers grown at 670 °C

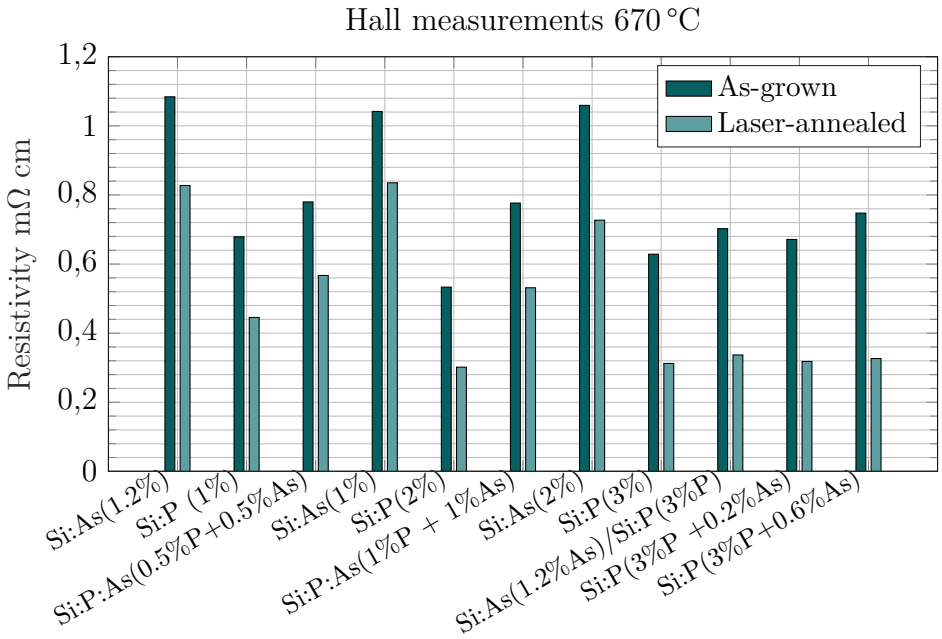


Figure 4.15: Resistivity related to layers grown at 670 °C

450 °C grown layers show a different trend since laser-annealing leads to an enhanced active concentration only for Si:P layers, but less effective compared to the previous case. In the other conditions, layers are stable or slightly deactivated after the thermal budget. Probably, this phenomenon is explained due to the high active concentration available after epitaxial growth, this will be confirmed also for higher total concentrations in the contact resistivity section. In layers at 1.2% total concentration, it is possible to observe an enhanced activation for Si:P:As(0.9% P + 0.3% As) corresponding to a minimum in resistivity [40], which can be attributed to a more efficient vacancy trapping mechanism by As in accord to the simulation reported by Nakazaki et al. [29].

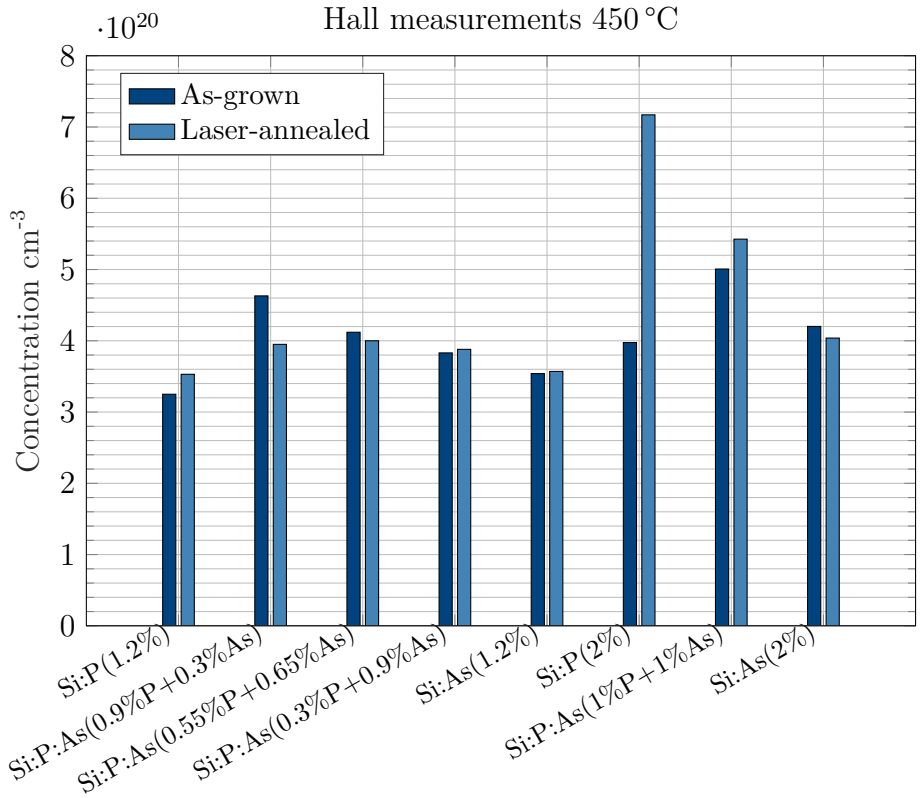


Figure 4.16: Active concentration related to layers grown at 450 °C

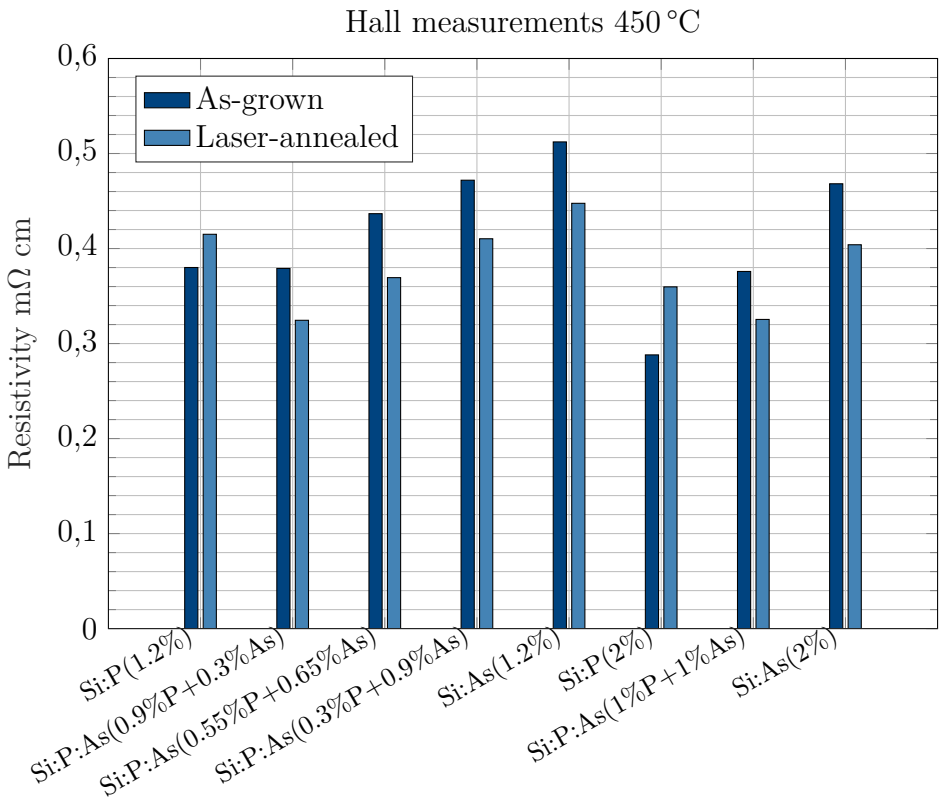


Figure 4.17: Resistivity related to layers grown at 450 °C

Ionized impurities in the crystalline structure are the principal source of scattering. It needs to be recalled that electrical inactive dopants do not affect the mobility since they result in vacancy complexes and interstitials, which are forms of precipitates [23], moreover that the theoretical solid solubility of P and As in silicon is different, respectively $2 \cdot 10^{20}$ at 600 °C and $7 \cdot 10^{20}$ at 700 °C [35].

Figure 4.18 show the mobility plotted with respect to the active concentration, the processes have different behaviours. From the data, it is possible to conclude that mobility in Si:As layers are generally lower compared to Si:P, while Si:P:As follows a similar trend to Si:P [40]. As modelled by Masetti et al. [23] mobility is a continuously decreasing function of the active concentration. For total concentration higher than the solubility limit, mobility in As-doped silicon decreases more rapidly than in P-doped silicon and the difference increases with the total concentration.

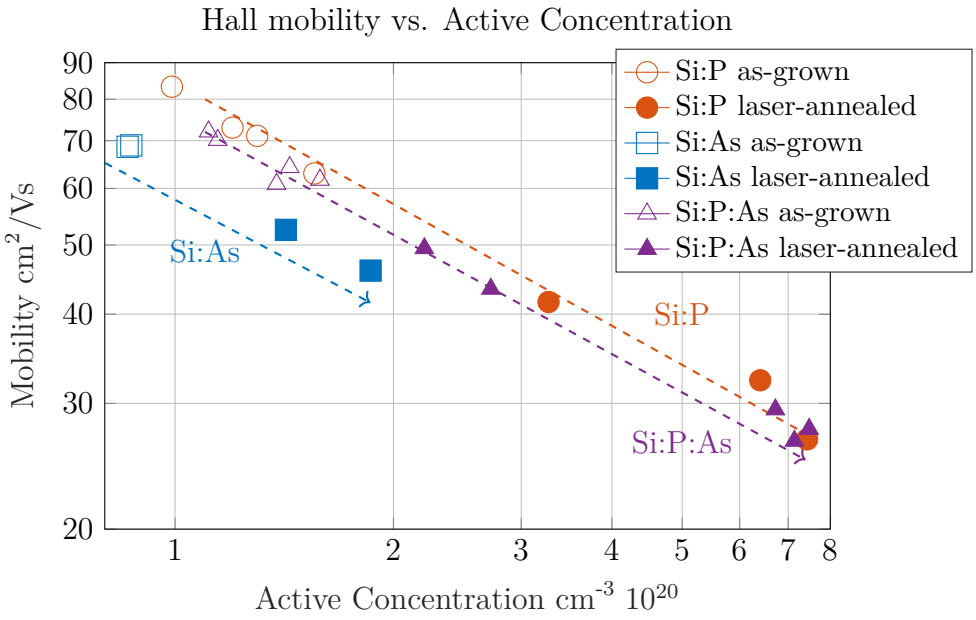


Figure 4.18: Mobility vs. Active concentration in Si:P, Si:As, Si:P:As.

4.2.2 Patterned structures

In this section measurements on the metal semiconductor junction are discussed. Contact resistivity evaluation is performed on the MR-CTLM patterned structure as previously discussed in section 3.2.7, the additional Ti silicidation and Cu deposition on n-Si epi-layers plays an important role on the resulting contact resistivity since silicidation fix the barrier height while Cu deposition establish the metal work-function determining the carrier transport mechanisms.

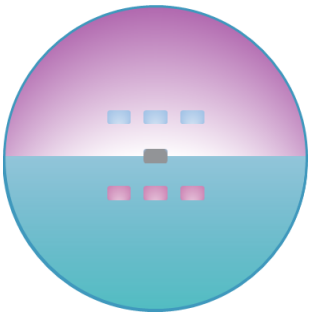


Figure 4.19: CTLM dies configuration.

The conditions used for this experiment are similar to the ones used for blanket layers characterization, previously discussed. Some additional conditions are added to complete the overview of these processes. Ti contact resistivity measurements are performed on six different dies in the laser-annealed (North) and the as-grown (South) region as shown in figure 4.19, then results are averaged. An additional centre die is measured to set-up the automated tool, which needs the centre die coordinates and the vertical and horizontal alignment.

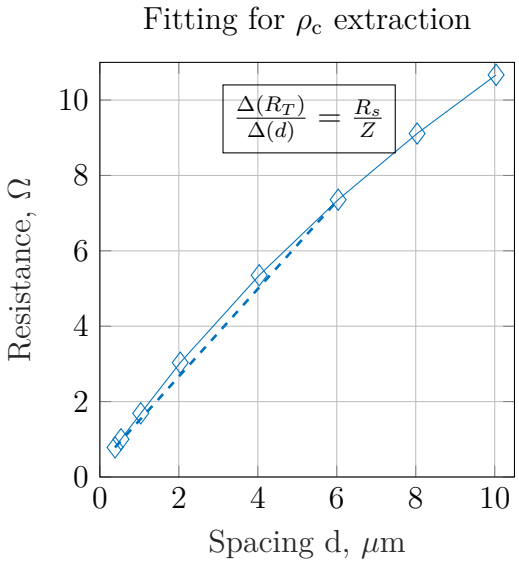


Figure 4.20: This is a typical graph of the total resistance as a function of the spacing distance d.

In figure 4.20 there is an example of the MR-CTLM measurements on an eight rings die. The resistance R_T of each ring is plotted with respect to the corresponding spacing distance d in μm on the abscissa. From this kind of plot it is possible to extract the contact resistance rho_c, in fact, the slope of the curve corresponds to $\Delta(R_T)/\Delta(d) = R_s/Z$, which is used to extract the sheet resistance R_s [14]. As the resistance approaches $d = 0$, it corresponds to $R_T = 2R_c$, the double of the contact resistance. For $R_T \to 0$ the spacing distance equals $-d = 2L_T$, hence, as the transfer length L_T is found, it is possible to extract the contact resistivity as in 3.10.
The raw data, especially considering different spacing distances, need to be fitted in order to obtain a reliable value of contact resistivity. In addition to the resistance measurements on the rings, it is measured the contribution of the metal, which is then subtracted from the total resistance in order to fit only the semiconductor contribution.

Pre-patterning measurements were performed to characterise the resistivity and eventual defects of the layer. The results are in line with previous blanket characterisation.
Contact resistivity, measured on the full Ti contact, shows a different picture with respect to the one seen for the blankets (fig. 4.15), in fact for layers grown at 670 °C the As addition lowers the contact resistivity. Several conditions meet the ITRS requirements, $\rho_c \leq 2 \cdot 10^{-9}$.
Co-doping seems to improve contact resistivity, the co-doped as-grown layers have lower resistivity with respect to the reference Si:P(3%). The additional thermal budgets and the silicidation may exploit improvements given by the As addition since Ti contact has an important role in fixing the barrier and this determine also the interface characteristics. Co-doped layers grown at 670 °C (fig. 4.21) show a slight improvement after laser annealing with respect to Si:P(3%) reference.

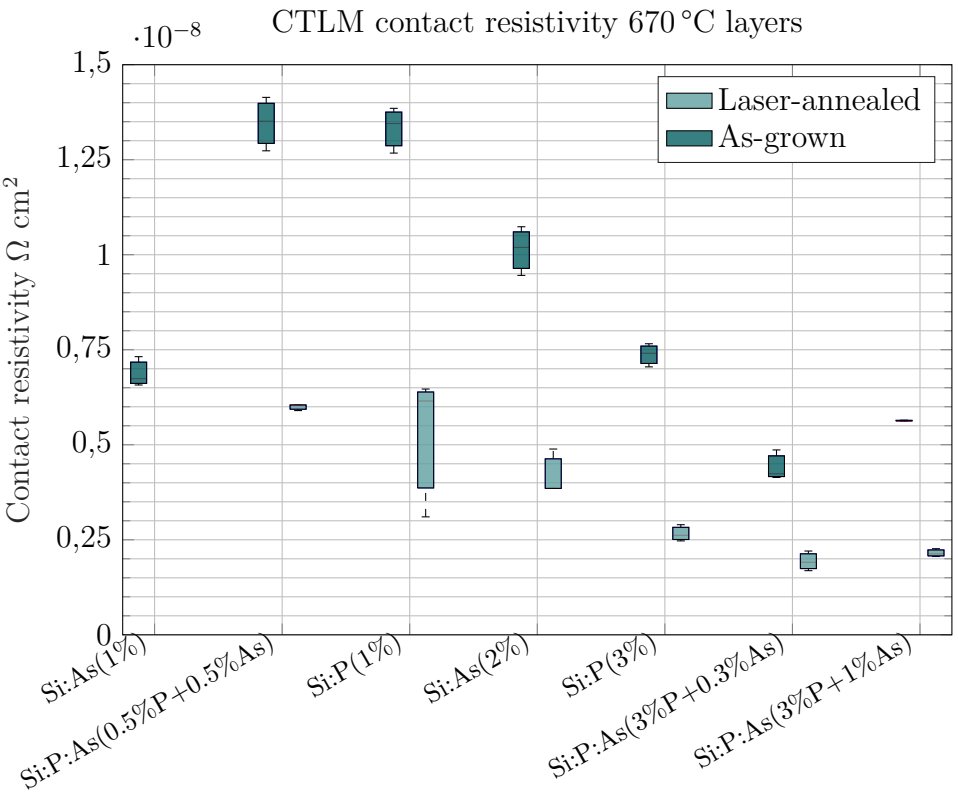


Figure 4.21: Contact resistivity of layers grown at 670°C

For what concerns 450 °C grown layers results, presented in fig. 4.22 are very interesting. It is confirmed that laser-annealing slightly improves Si:P contact resistivity at low total concentration, as seen for blankets (fig. 4.17), but differently from the previous case, Si:As epi-layers at high concentration give comparable contact resistivity to the Si:P reference, even though blanket resistivity was higher. Furthermore, Si:P(4%) show a decrease in contact resistivity demonstrating a saturation phenomenon for P concentration higher than 3%.

In this case Si:As layers are comparable to Si:P layers which can be linked to comparable active concentration, this is in contradiction with what we have seen in blanket layers. In this case, it should be useful to investigate the barrier formation in this kind of structure and the role of silicidation. A vacancy trapping mechanism for co-doped layers could lead to higher active concentration, especially for the as-grown region.

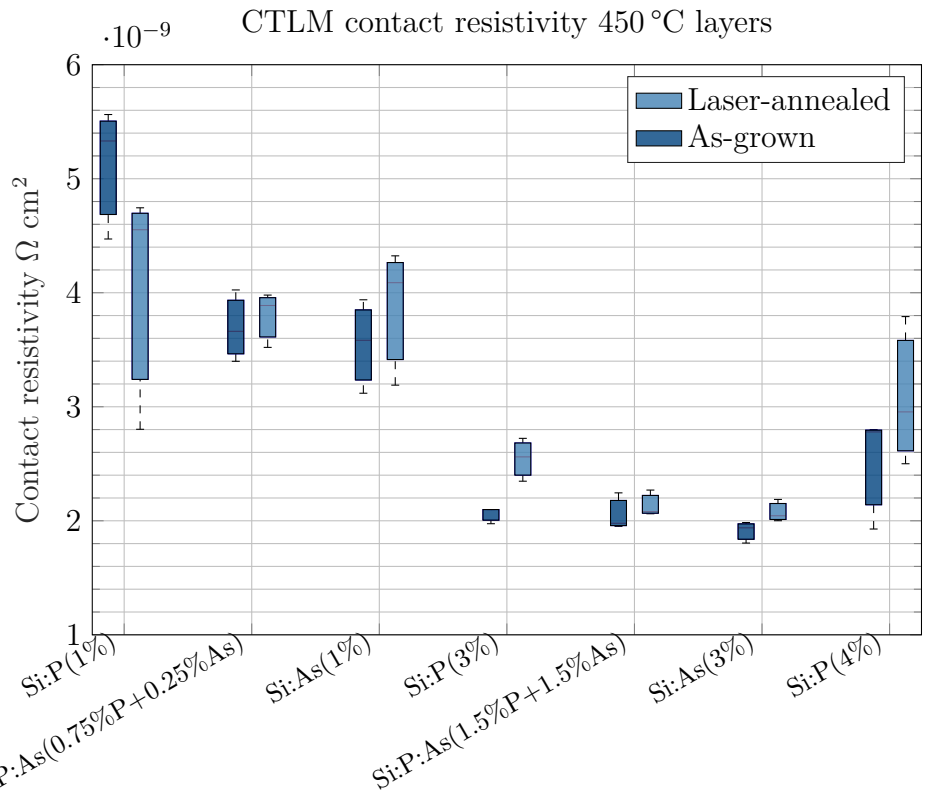


Figure 4.22: Contact resistivity for layers grown at 450 °C

In order to better understand the nature of the described phenomena, a TEM inspection has been requested on the most significant samples. The inspection is related to the smallest ring of the CTLM pattern, which has the highest impact in the resistivity extraction.
In figure 4.23 it is possible to observe the cross-section of the ring structure for Si:P(3%) and Si:P:As(3%P +0.3%As) grown at 670 °C and Si:As(3%As) grown 450 °C. The thickness as the width is close to the nominal value and there is no segregation of P or As. The Ti Si interface is well defined even though Ti close to the interface is amorphous, since the line-scan shows the presence of oxygen, hence Ti is likely to be TiOx. The considerations done are valid for P, As and co-doped layers. All the inspected conditions show sign of Cu corrosion which is, essentially, an artefact of the ion beam thinning and air storage.

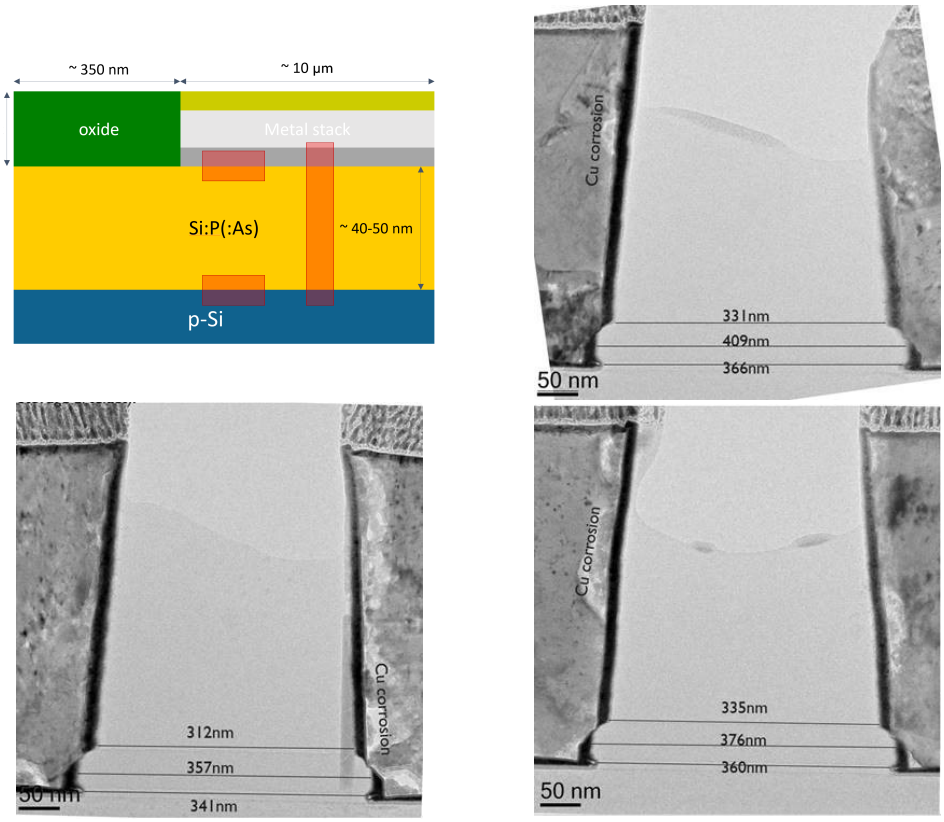


Figure 4.23: On top it is reported the schematic of the inspection (left) and the cross-section of the Ti-contact for Si:P(3%) layer grown at 670 °C (right), while on bottom it is reported the cross-section of the Ti-contact for Si:P:As(3%P +0.3%As) layer grown at 670 °C (left) and Si:As(3%) layer grown at 450 °C (right).

5 Conclusions

Highly doped epitaxial layers Si:P, Si:As and Si:P:As are compared for two types of process: a selective process at 670 °C using $SiCl_2H_2$ (DCS) and a non-selective process at 450 °C using Si_3H_8. The epitaxial quality of blanket layers is characterised using AFM, haze and RBS channeling measurements. Chemical doping levels and thicknesses are determined using the SIMS technique while the active dopant concentration is determined by micro-Hall measurements.

5.1 Results and discussion

The experiments confirmed several interesting characteristics of the P and As in-situ co-doped silicon for the next generation NMOS S/D layers.
Morphological and structural characterizations show low defectivity. From AFM and RBS channeling measurements it is possible to state that As addition does not significantly affect the crystalline quality of the layers. For the Si:As process at 670 °C it is observed a slight roughening while for the process at 450 °C there is no morphological difference. SIMS allowed to asses the controllability of the processes and the relevant incorporation of As as well as the benefits on the diffusion.
Resistivity characterisation shows two different pictures. On the blanket layers micro-Hall measurements show Si:As activation levels and resistivity worse with respect Si:P reference while Si:P:As layers with low [As] are comparable. The contact resistivity extraction on the patterned CTLM structures shows the beneficial effect of As addition leading to a relevant reduction of the contact resistivity on the Ti contacts. In fact, As addition leads to a relevant reduction of ρ_c for as-grown epi-layers, and it contributes to a reduction also after laser annealing. Furthermore in contact resistivity extraction Si:As layers are comparable to Si:P, which means that the active concentration is similar, moreover, it is demonstrated a saturation phenomenon around 4% P

concentration. Such low contact resistivity is worth to be noticed since they are obtained without laser-annealing.
Additional thermal budgets are employed to characterise the stability up to 700 °C. It is shown that Si:As and co-doped layers are possibly more thermally stable than reference Si:P layers.

5.2 Future work

It is proved that Si:As and Si:P:As layers are good candidates for the next generation S/D epi-layers. Several phenomena need to be explained, especially barrier formation of Ti contacts and the physics underneath the Si:As activation and the link between the blanket resistance and the resulting contact resistivity. Characterising the different species present in the layer could clarify their behaviour. Among the techniques, there is Positron Annihilation Spectroscopy (PAS) which can clarify how the dopants are incorporated, whether in substitutional or vacancy sites, and how the additional thermal budgets contribute in activation/deactivation. On the other hand, Density Functional Theory (DFT) simulations can clarify some aspects of the deactivation of layers grown at 670 °C and the stability of the 450 °C grown layers The behaviour of the 450 °C layers is promising in terms of active concentration, contact resistivity and the thermal stability. These layers are however not selective and works need to be done to use these in a cyclic-deposition and etch process to make them selective.

Bibliography

[1] "International Technoloy Roadmap for Seminconductors, More Moore", 2015. URL http://www.itrs2.net/itrs-reports.html.

[2] R. Alferness. "Bell System Technical Journal, 1922-1983", 2011. URL http://www.alcatel-lucent.com/bstj/.

[3] M. Bauer and S. Thomas. "Selective Epitaxial Growth (SEG) of Highly Doped Si:P on Source/Drain Areas of NMOS Devices Using Si". (January 2010):629–636, 2010. doi:10.1149/1.3487593.

[4] B. Brijs, W. Coster, and W. Vandervorst. "Various advanced capabilities of the RBS setup at IMEC". *Nuclear Instruments & Methods in Physics Research Section B-beam Interactions With Materials and Atoms, Physical Review B*, 64:825–831, 02 1992. doi:10.1016/0168-583X(92)95586-G.

[5] G. Celotti, D. Nobili, and P. Ostoja. "Lattice parameter study of silicon uniformly doped with boron and phosphorus". *Journal of Materials Science*, 9(5):821–828, 1974. ISSN 00222461. doi:10.1007/BF00761802.

[6] S. Chopra, Z. Ye, A. Zojaji, Y. Kim, and S. Kuppurao. "Heavily Phosphorus Doped Silicon Junctions for nMOS Applications". In *ECS Transactions*. ECS, 2008. doi:10.1149/1.2911511. URL https://doi.org/10.1149%2F1.2911511.

[7] S.-S. Chuang, T.-C. Cho, P.-J. Sung, K.-H. Kao, H. J. H. Chen, Y.-J. Lee, M. I. Current, and T.-Y. Tseng. "Ultra-Shallow Junction Formation by Monolayer Doping Process in Single Crystalline Si and Ge for Future CMOS Devices". *ECS Journal of Solid State Science and Technology*, 6 (5):P350–P355, 2017. ISSN 2162-8769. doi:10.1149/2.0011707jss.

[8] N. Collaert, A. Alian, H. Arimura, G. Boccardi, G. Eneman, J. Franco, T. Ivanov, D. Lin, R. Loo, C. Merckling, J. Mitard, M. A. Pourghaderi, R. Rooyackers, S. Sioncke, J. W. Sun, A. Vandooren, A. Veloso, A. Verhulst, N. Waldron, L. Witters, D. Zhou, K. Barla, and A. V. Thean.

"Ultimate nano-electronics: New materials and device concepts for scaling nano-electronics beyond the Si roadmap". *Microelectronic Engineering*, 132:218–225, 2015. ISSN 01679317. doi:10.1016/j.mee.2014.08.005.

[9] N. E. Cowern, G. Mannino, P. A. Stolk, F. Roozeboom, H. G. Huizing, J. G. van Berkum, F. Cristiano, A. Claverie, and M. Jaraíz. "Energetics of self-interstitial clusters in Si". *Physical Review Letters*, 82(22):4460–4463, 1999. ISSN 10797114. doi:10.1103/PhysRevLett.82.4460.

[10] J. M. David and M. G. Buehler. "A numerical analysis of various cross sheet resistor test structures". *Solid-State Electronics*, 20(6):539–543, 1977. ISSN 00381101. doi:10.1016/S0038-1101(77)81011-3.

[11] J. A. Del Alamo and R. M. Swanson. "Measurement of Hall scattering factor in phosphorus-doped silicon". *Journal of Applied Physics*, 57(6): 2314–2317, 1985. ISSN 00218979. doi:10.1063/1.334333.

[12] S. K. Dhayalan. *"Advanced Low Temperature epitaxy fo High mobility materials"*. PhD thesis, KU Leuven, Science, Engineering & Technology, 2017.

[13] S. K. Dhayalan, J. Kujala, J. Slotte, G. Pourtois, E. Simoen, E. Rosseel, A. Hikavyy, Y. Shimura, S. Iacovo, A. Stesmans, R. Loo, and W. Vandervorst. "On the manifestation of phosphorus-vacancy complexes in epitaxial Si:P films". *Applied Physics Letters*, 108(8), 2016. ISSN 00036951. doi:10.1063/1.4942605.

[14] K. S. Dieter. *"Semiconductor Material and Device Characterization"*. Wiley-Interscience, 2005. ISBN 9780471749097. doi:10.1002/0471749095.

[15] J.-L. Everaert, M. Schaekers, H. Yu, L.-L. Wang, A. Hikavyy, L. Date, J. Del Agua Borniquel, K. Hollar, F. Khaja, W. Aderhold, A. Mayur, J. Lee, H. Van Meer, Y.-L. Jiang, K. De Meyer, D. Mocuta, and N. Horiguchi. "Sub 10^{-9} Ω cm^2 contact resistivity on p-SiGe achieved by Ga doping and nanosecond laser activation". *Digest of Technical Papers - Symposium on VLSI Technology*, 36(6):2016–2017, 2017. doi:10.23919/VLSIT.2017.7998176.

[16] H. Fahad and M. Hussain. "Are Nanotube Architectures more advantageous than Nanowire Architectures for Field Effect Transistors?". *Scientific reports*, 2:475, 06 2012. doi:10.1038/srep00475.

[17] I. for Nuclear and K. L. Radiation Physics. "Rutherford Backscattering Spectrometry and Ion Channeling", 2017.

[18] F. Fujimoto, K. Komaki, M. Watanabe, and T. Yonezawa. "Behavior of phosphorous and arsenic diffused simultaneously into silicon crystals". *Applied Physics Letters*, 20(7):248–249, 1972. ISSN 00036951. doi:10.1063/1.1654132.

[19] S. W. King, H. Simka, D. Herr, H. Akinaga, and M. Garner. "Research updates: The three M's (materials, metrology, and modeling) together pave the path to future nanoelectronic technologies". *APL Materials*, 1 (4), 2013. ISSN 2166532X. doi:10.1063/1.4822437.

[20] A. N. Larsen, K. K. Larsen, P. E. Andersen, and B. G. Svensson. "Heavy doping effects in the diffusion of group IV and V impurities in silicon". *Journal of Applied Physics*, 73(2):691–698, 1993. ISSN 00218979. doi:10.1063/1.353324.

[21] H. S. Lee. *"Thermoelectrics: Design and materials"*. 2016. ISBN 9781118848944. doi:10.1002/9781118848944.

[22] R. Loo, A. Hikavyy, C. Porret, E. Rosseel, A. Vohra, Y.-H. Huang, M. Tirrito, W.-C. Wen, D. Rondas, J. Steenbergen, and R. Langer. "Group IV epitaxy". Nagoya University bilateral meeting: January 28. Bruker bilateral meting: March 28, 2019.

[23] M. Masetti, M. Severi, and S. Solmi. "Modeling of carrier mobility against carrier concentration in As, P and B-doped silicon". *IEEE Transactions on Electron Devices*, 30:764–769, 1983.

[24] G. S. May and S. M. Sze. *"Fundamentals of Semiconductor Fabrication"*. Wiley-Interscience, 2004. ISBN 9780471452386.

[25] M. Meier. "Measuring Crystalline Size Using X-Ray Diffraction, the Williamson-Hall Technique (Draft)". *Dept. of Chemical Engineering and Materials Science,*, 2005.

[26] S. Mochizuki, B. Colombeau, L. Yu, A. Dube, S. Choi, M. Stolfi, Z. Bi, F. Chang, R. A. Conti, P. Liu, K. R. Winstel, H. Jagannathan, H. J. Gossmann, N. Loubet, D. F. Canaperi, D. Guo, S. Sharma, S. Chu, J. Boland, Q. Jin, Z. Li, S. Lin, M. Cogorno, M. Chudzik, S. Natarajan, D. C. McHerron, and B. Haran. "Advanced Arsenic Doped Epitaxial Growth for Source Drain Extension Formation in Scaled FinFET Devices". *Technical Digest - International Electron Devices Meeting, IEDM*, 2018-December: 35.2.1–35.2.4, 2019. ISSN 01631918. doi:10.1109/IEDM.2018.8614543.

[27] A. Mokhberi, P. B. Griffin, J. D. Plummer, E. Paton, S. McCoy, and K. Elliott. "A comparative study of dopant activation in boron, BF2, arsenic, and phosphorus implanted silicon". *IEEE Transactions on Electron Devices*, 49(7):1183–1191, 2002. ISSN 00189383. doi:10.1109/TED.2002.1013274.

[28] G. E. Moore. "Cramming more components onto Integrated Circuits". pages 56–59, 1965. URL `http://dl.acm.org/citation.cfm?id=333067.333074`.

[29] N. Nakazaki, E. Rosseel, C. Porret, A. Hikavyy, R. Loo, N. Horiguchi, N. Horiguchi, and G. Pourtois. "Ab initio analysis of defect formation and dopant activation in P and As co-doped Si". 2019.

[30] C. N. Ni, X. Li, S. Sharma, K. V. Rao, M. Jin, C. Lazik, V. Banthia, B. Colombeau, N. Variam, A. Mayur, H. Chung, R. Hung, and A. Brand. "Ultra-low contact resistivity with highly doped Si:P contact for nMOSFET". *Digest of Technical Papers - Symposium on VLSI Technology*, 2015-August(2012):T118–T119, 2015. ISSN 07431562. doi:10.1109/VLSIT.2015.7223711.

[31] H. Niimi, Z. Liu, O. Gluschenkov, S. Mochizuki, J. Fronheiser, J. Li, J. Demarest, C. Zhang, B. Liu, J. Yang, M. Raymond, B. Haran, H. Bu, and T. Yamashita. "Sub-10 -9 Ω-cm^2 n-Type Contact Resistivity for FinFET Technology". *IEEE Electron Device Letters*, 37(11):1371–1374, 2016. ISSN 07413106. doi:10.1109/LED.2016.2610480.

[32] A. I. N.V. "Intrepid™ XP Epitaxy", 2017. URL `https://qa.asm.com/solutions/products/epitaxy-products/intrepid-xp-epitaxy`.

[33] D. H. Petersen, O. Hansen, R. Lin, and P. F. Nielsen. "Micro-four-point probe Hall effect measurement method". *Journal of Applied Physics*, 104 (1):013710, 2008. doi:10.1063/1.2949401.

[34] D. H. Petersen, P. Bøggild, O. Hansen, P. F. Nielsen, and W. Vandervorst. "Micro Four-Point Probe and Micro Hall Effect: Methods for Reliable Electrical Characterization of Ultra-Shallow Junctions". 2012.

[35] P. Pichler. *"Intrinsic Point Defects, Impurities, and Their Diffusion in Silicon"*. Springer-Verlag Wien, 2004. doi:10.1007/978-3-7091-0597-9.

[36] S. Prussin, J. Reyes, S. Qin, A. McTeer, J. Y. Hu, H. Onoda, N. Hamamoto, T. Nagayama, and M. Tanjyo. "Scatter defects and Hall scattering factor for the mobility of boron in silicon". *AIP*

Conference Proceedings, 1321(June):181–183, 2010. ISSN 0094243X. doi:10.1063/1.3548342.

[37] J. K. Prüßing, G. Hamdana, D. Bougeard, E. Peiner, and H. Bracht. "Quantitative scanning spreading resistance microscopy on n-type dopant diffusion profiles in germanium and the origin of dopant deactivation". *Journal of Applied Physics*, 125(8), 2019. ISSN 10897550. doi:10.1063/1.5066617.

[38] M. Ramamoorthy and S. T. Pantelides. "Complex dynamical phenomena in heavily arsenic doped silicon". *Physical Review Letters*, 76(25):4753–4756, 1996. ISSN 10797114. doi:10.1103/PhysRevLett.76.4753.

[39] E. Rosseel, M. Tirrito, C. Porret, B. Douhard, J. Meersschaut, A. Hikavyy, R. Loo, N. Horiguchi, G. Pourtois, N. Nakazaki, and J. Tolle. "Characterization of Highly Doped Si:P, Si:As and Si:P:As Epi Layers for Source/Drain Epitaxy". ISTDM/ICSI 2019 Conference, University of Wisconsin-Madison, 2019.

[40] E. Rosseel, M. Tirrito, C. Porret, B. Douhard, J. Meersschaut, A. Hikavyy, R. Loo, N. Horiguchi, G. Pourtois, N. Nakazaki, and J. Tolle. "Characterization of Highly Doped Si:P, Si:As and Si:P:As Epi Layers for Source/Drain Epitaxy". *ECS Transactions*, 93:11–15, 10 2019. doi:10.1149/09301.0011ecst.

[41] A. Schenk, P. P. Altermatt, and B. Schmithusen. "Physical Model of Incomplete Ionization for Silicon Device Simulation". *Simulation of Semiconductor Processes and Devices, 2006 International Conference on*, pages 51–54, 2006. doi:10.1109/SISPAD.2006.282836.

[42] B. Streetman and S. Banerjee. *"Solid State Electronic Devices"*. Pearson, 2015.

[43] O. Sugino and A. Oshiyama. "Microscopic mechanism of atomic diffusion in Si under pressure". *Physical Review B*, 46(19):12335–12341, 1992. ISSN 01631829. doi:10.1103/PhysRevB.46.12335.

[44] S. M. Sze and K. N. Kwok. *"Physics of Semiconductor Devices"*. Wiley-Interscience, 2006.

[45] A. Vohra, I. Makkonen, G. Pourtois, J. Slotte, C. Porret, E. Rosseel, A. Khanam, M. Tirrito, B. Douhard, R. Loo, and W. Vandervorst. "(Accepted) Source/Drain Materials for Ge nMOS Devices: Phosphorus

Activation in Epitaxial Si, Ge, $Ge_{1-x}Sn_x$ and $Si_yGe_{1-x-y}Sn_x$". *ECS Journal of Solid State Science and Technology*.

[46] K. Weeks, S. Thomas, P. Dholabhai, and J. Adams. "Characterization and analysis of epitaxial silicon phosphorus alloys for use in n-channel transistors". *Thin Solid Films*, 520(8):3158–3162, 2 2012. ISSN 0040-6090. doi:10.1016/j.tsf.2011.10.107.

[47] F. Wittel and S. Dunham. "Diffusion of phosphorus in arsenic and boron doped silicon". *Applied Physics Letters*, 66(11):1415–1417, 2002. ISSN 0003-6951. doi:10.1063/1.113219.

[48] A. Wocko, S. Radovanovic, and P. Dighe. "Study of relationship between 300 mm Si wafer surface and annealing temperatures for advanced semiconductor-based applications". *ASMC (Advanced Semiconductor Manufacturing Conference) Proceedings*, pages 154–157, 2010. ISSN 10788743. doi:10.1109/ASMC.2010.5551438.

[49] C. Xu, J. D. Gallagher, P. Sims, D. J. Smith, J. Menéndez, and J. Kouvetakis. "Non-conventional routes to SiGe:P/Si(100) materials and devices based on -SiH3 and -GeH3 derivatives of phosphorus: Synthesis, electrical performance and optical behavior". *Semiconductor Science and Technology*, 30(4), 2015. ISSN 13616641. doi:10.1088/0268-1242/30/4/045007.

[50] Q. Xu and C. Hu. "New Ti-SALICIDE process using Sb and Ge preamorphization for sub-0.2 μm CMOS technology". *IEEE Transactions on Electron Devices*, 45(9):2002–2009, 1998. ISSN 00189383. doi:10.1109/16.711367.

[51] H. Yu, M. Schaekers, T. Schram, E. Rosseel, K. Martens, S. Demuynck, N. Horiguchi, K. Barla, N. Collaert, K. De Meyerieee, and A. Thean. "Multiring circular transmission line model for ultralow contact resistivity extraction". *IEEE Electron Device Letters*, 36(6):600–602, 2015. ISSN 07413106. doi:10.1109/LED.2015.2425792.

[52] J. Zhang, K. Tse, M. Wong, Y. Zhang, and J. Zhu. "A brief review of co-doping". *Frontiers of Physics*, 11(6), 2016. ISSN 20950470. doi:10.1007/s11467-016-0577-2.

[53] P. Zhang, Y. Y. Lau, and R. M. Gilgenbach. "Analysis of current crowding in thin film contacts from exact field solution". *Journal of Physics D: Applied Physics*, 48(47):475501, 2015. ISSN 13616463. doi:10.1088/0022-3727/48/47/475501.

[54] Y. Zhao, M. J. Aziz, H. J. Gossmann, S. Mitha, and D. Schiferl. "Activation volume for boron diffusion in silicon and implications for strained films". *Applied Physics Letters*, 74(1):31–33, 1999. ISSN 00036951. doi:10.1063/1.123123.

[55] Y. Zhao, M. J. Aziz, N. R. Zangenberg, and A. N. Larsen. "Activation volume for phosphorus diffusion in silicon and $Si_{0.93}$ $Ge_{0.07}$". *Applied Physics Letters*, 86(14):1–3, 2005. ISSN 00036951. doi:10.1063/1.1896445.

List of Abbreviations

AFM	Atomic Force Microscopy
AsH_3	Arsine
CTLM	Circular Transmission Line Model
CVD	Chemical Vapor Deposition
DCS	Dichlorosilane
FINFET	Fin Field Effect Transistor
GAA	Gate All Around
HR-XRD	High Resolution X-Ray Diffraction
HSF	Hall Scattering Factor
ITRS	International Technology Roadmap of Semiconductors
LA	Laser Annealing
M4PP	Micro 4 point probe
MHE	Micro Hall Effect
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MRCTLM	Multi-Ring Circular Transmission Line Model
M-S	Metal Semiconductor
PH_3	Phosphine
RBS	Rutherford Back-Scattering
RPCVD	Reduced Pressure Chemical Vapor Deposition
RTA	Rapid Thermal Annealing
SCE	Short Channel Effects
Si_3H_8	Trisilane
Si:As	Silicon Arsenic
Si:P	Silicon Phosphorus
Si:P:As	Silicon Phosphorus Arsenic (Co-doping)
SIMS	Secondary Ion Mass Spectroscopy
SiTi	Titanium Silicidation
XTEM	Cross-sectional Transmission Electron Microscopy