Doherty Power Amplifier

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Abstract

In this thesis i have discuss the designed,implementation and experimental results of a hybrid Doherty power amplifier in 3-3.8 GHz band.In this work i used a Cree GaN HEMT device with a maximum power 40 dBm for the single device.Power amplifier designed with an Efficiency 64-68% in output power range 38-44 dBm. With respect to other designs this a simpler design and higher efficiency maintaining the maximum saturated output power.

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Chapter 1

Power amplifier introduction

1.1 What is a power amplifier

Wireless transmissions require modulated waves to be sent over long distances via air. The signals are transmitted using antennas and the range of transmission depends on the magnitude of power of signals fed to the antenna.

Antennas can require input signals till hundreds of watts of power. Radio Frequency Power amplifiers are employed to increase the magnitude of power of modulated waves to a level high enough for reaching required transmission distance. The power amplifier(PA) is a quasi-linear system used to amplify the power coming from other transmitter parts, transforming the DC power coming from DC source into a AC signal at the output.

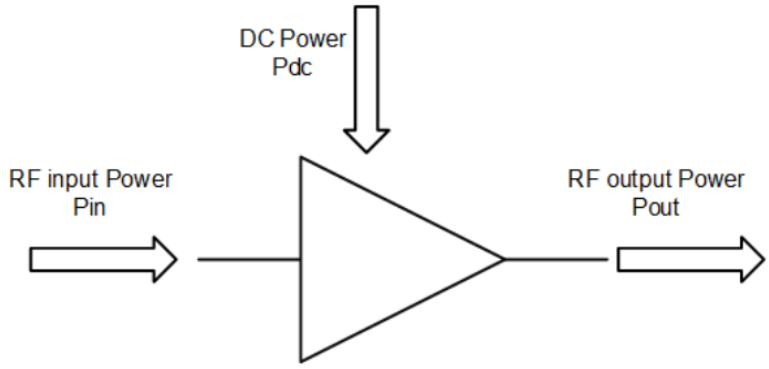


Fig. 1.1 Schematic representation of a power amplifier operation

The output power (P_{out}) is the AC signal power transmitted to the output load which is usually an antenna modelled in circuit level as a load resistance (R_L).

The main goal of the power amplifier is to transfer the maximum power that the device can deliver to the output load but at the same time since it is an amplifier it should introduce a gain of the input power. During PA design other parameters are important and should always be taken into account. Some of the most important parameters of a PA are :

Power Saturation P_{sat}

The power transfer at load is limited by the FET device used for the amplifier. The output power of active devices is, in fact, limited by the maximum voltage and current swing, in turn related to the drain breakdown voltage and to the maximum current, respectively.

Gain

A power amplifier should increase the power of the signal from input to output port, so it should introduce a gain larger than 1. Pa is quasi-linear or non linear system and having in input a signal centered at a frequency f_0 the output will consist in a signal centered at f_0 and other harmonics at nf_0.

Operation Gain G_{OP} is defined as:

$$G_{OP} = \frac{P_{OUT}(f_0)}{P_{in}}$$

where P_{in} is the power transferred from the input power generator to the device input.

Transducer Gain G_{tr} as:

$$G_{tr} = \frac{P_{OUT}(f_0)}{P_{av,in}}$$

where $P_{av,in}$ is the power available (generated) by the input power generator.

Efficiency η

The DC Power is transformed in one part in RF power and transferred to the load and in part dissipated by the FET device. So efficiency is defined as :

$$\eta = \frac{P_{OUT}(f_0)}{P_{DC}}$$

the ratio between RF power transferred at load and the power generated by the DC voltage supplier.

Power added efficiency, PAE

$$P_{AE} = \frac{P_{OUT}(f_0) - P_{in}(f_0)}{P_{DC}} = \eta(1 - \frac{1}{G_{OP}})$$

If gain is very high power added efficiency tends to efficiency.

Pin-Pout

Pin-Pout graph is a representation usually used for power amplifiers and it display the output powers,in logarithmic scale, of fundamental and harmonics.

In small signal conditions the output power of the harmonics $P_{out}(nf_0)$ can be modelled by the expression:

$$P_{out}(nf_0) = K_n P_{in}(f_0)^n$$

An important parameter that describes the nonlinearities is the *3rd Order Intercept Point* which is defined as the interception of the fundamental power $P_{out}(f_0)$ with third order harmonic $P_{out}(3f_0)$ in the graph $P_{in} - P_{out}$. In fig1.2 this interception is obtained extending the two straight lines of $P_{out}(3f_0)$, $P_{out}(f_0)$ measured in small signal, where they are still linear vs input signal.

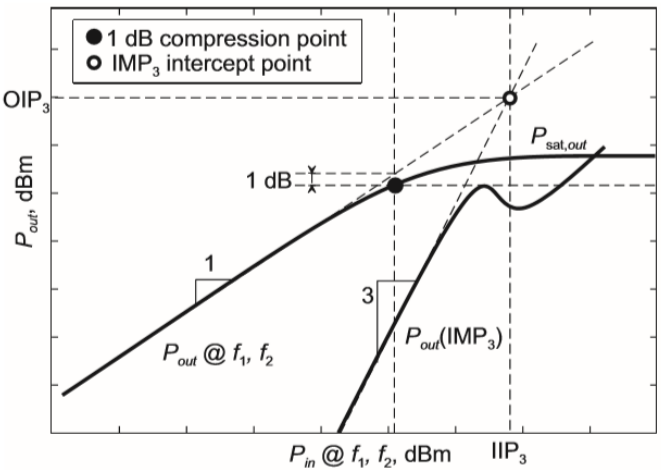


Fig. 1.2 Harmonic generation

It is considered the third order harmonics because since we are dealing with sinusoidal signals the odd power $(P_{out})^n$ are affecting the fundamental power and the third harmonic is even the most relevant.

Intermodulation product: CIM

Two tone test is made generating two input signals at central frequency f_1 and f_2.

The output includes signals at f_1 and f_2 and intermodulation products at frequencies $mf_1 + nf_2$ with m,n integers.

If $f_1 \approx f_2$ then the intermodulation terms of odd order follow near f_1 and f_2. In fig1.3 are shown the 3rd and 5th order intermodulation. The most relevant is the 3rd order called CIM_3 so it is usually the only one considered as a figure of merit of the linearity of the power amplifier. f_1 and f_2 are two input signals around a central band frequency f_0 with spacing

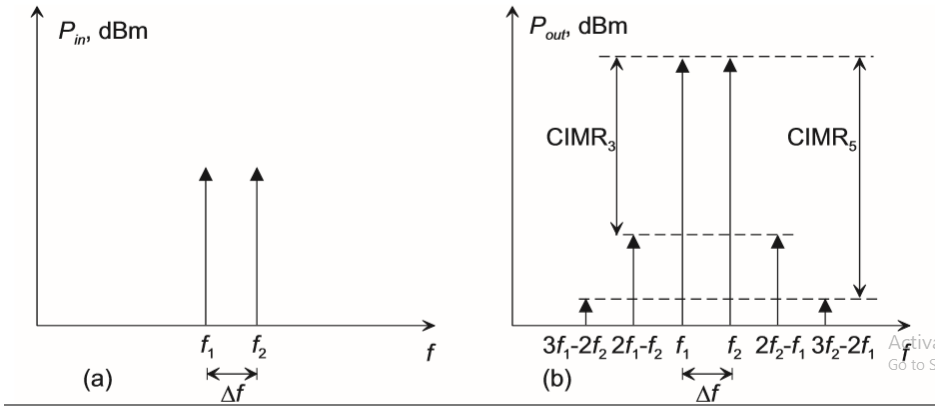


Fig. 1.3 Input (a) and output (b) spectrum for the two tone test

Δf«f_0. The 3^{rd} order intermodulation term are $f = 2f_1 - f_2 = f_0 - \Delta f_0$ and $f = 2f_2 - f_1 = f_0 - \Delta f_0$ that fall near the central frequency f_0.

$$CIM_3 = \frac{P_{out}(f_0)}{P_{int3}}$$

ACPR (Adjacent Channel Power Ratio) Usually in communication system at the input we have modulated signals which spectrum is spread over a band and not to a single frequency.Those intermodulation products give their effect even out of band (adjacent channel) and for this reason a figure of merit of this nonlinearity is defined as ACPR:

$$\mathbf{ACPR} = \frac{\int_{MC} p_{out}(f)df}{\int_{CK} p_{out}(f)df}$$

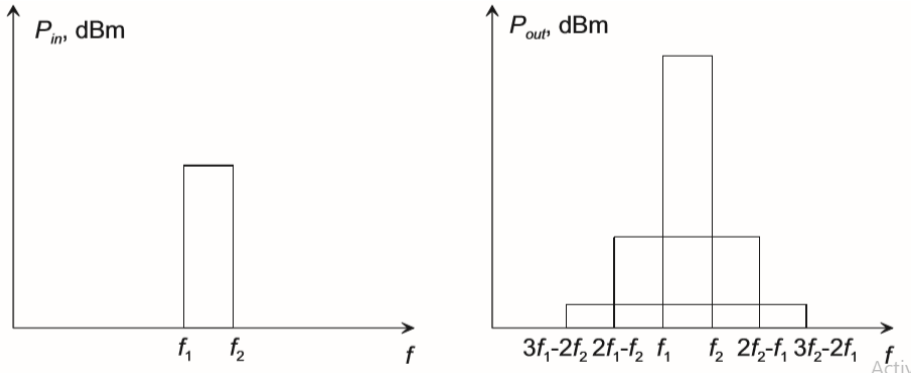


Fig. 1.4 Input (a) and output (b) spectrum for the two tone test of an input modulated signal

AM-AM and AM-PM distortion Testing the PA with an input signal at a single frequency f_0 can obtain the behaviour of the output magnitude and phase with respect to the input signal.

If we express the output signal as signal in time y(t) and input x(t), X and Y their phasors respectively where $P_{in} \propto |X|^2$ and $P_{out} \propto |Y|^2$. In frequency domain there is a relation between Y and X than can be defined as :Y=F(|X|)X=F(P_{in})X that contains the relation of Y with respect to phase and amplitude of X.

The magnitude |F(P_{in})|$with respect to P_{in}$ is the AM-AM distortion. In small signal this magnitude is a constant number equal to the SS gain. Since Pa is a non-linear system increasing the amplitude of input signal |F| changes and this represents AM-AM distortion.

The same consideration is done for the phase F(P_{in}) with respect to P_{in} which represents the AM-PM distortion.

1.2 PA Classes

To implement power amplifier a FET device is used (MESFet, HEMT...) which mode of operation is similar. The input voltage applied between gate-source of the device will give an controlled output current at the drain source node.Depending on the bias (DC) voltages of gate and drain, there are different topologies of traditional classes of PA.

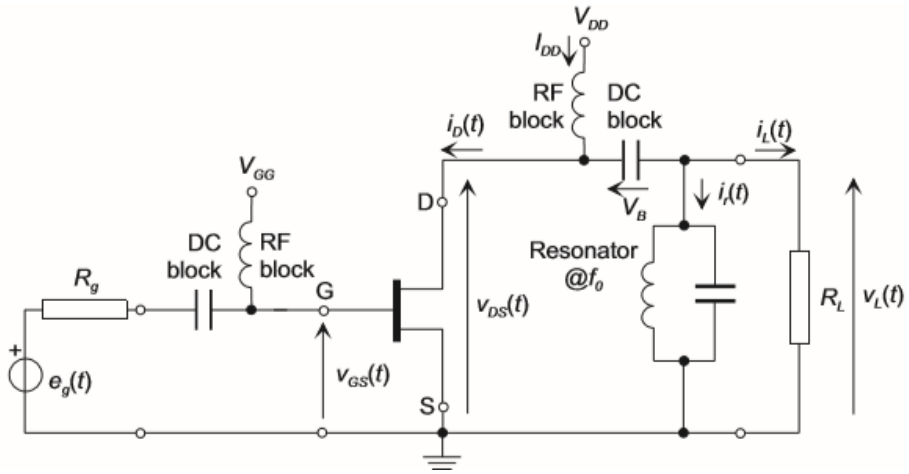


Fig. 1.5 Power amplifier schematic

- **Class A** The bias voltage is half the threshold voltage and output DC current is half the maximum current. Input voltage swing is limited between threshold gate voltage (V_{TH}) and 0 $V_{GG} \in [V_{TH}, 0]$ while output voltage will swing between 0 and $2V_{DD}$(two timed

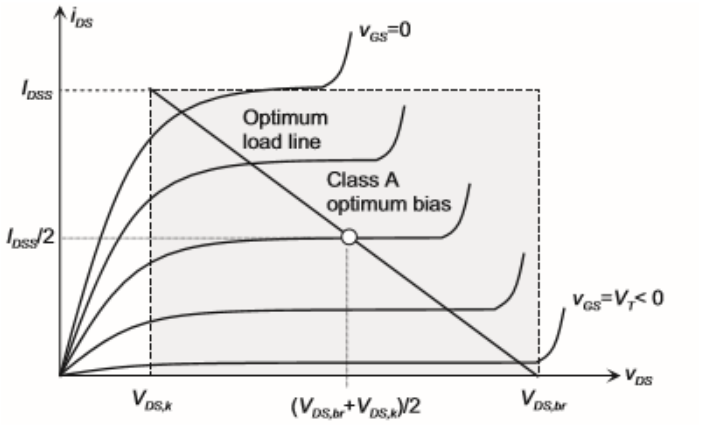


Fig. 1.6 Class A bias and dynamic load line

bias drain voltage) .Class A is a quasi-linear amplifier with sources of nonlinearities generated by the nonlinearities of the device itself.

The DC output bias current is ideally $I_{DSS}/2$ (where I_{DSS} is the maximum current that device can deliver ,for $V_{GG} = 0$). The current swing is $[0, I_{DSS}]$ and the sinusoidal current has an amplitude of $I_{DSS}/2$. To obtain maximum power delivered at load even the voltage should have the maximum swing [0,V_{DD}] at the same time with current maximum swing. So the optimum load that the device should see is $R_{OPT} = \frac{V_{br}-V_{knee}}{I_{DSS}/2}$ The maximum efficiency is

$$\eta_{max} = \frac{P_{RF}}{P_{DC}} = \frac{V_{DD}/2 * I_{DSS}/2}{V_{DD} * I_{DSS}/2} = \frac{1}{2} = 50\%$$

at maximum output power P_{sat}.

- **Class B**

This is a nonlinear amplifier class. The drain bias voltage is the same as the Class A but the gate voltage is equal to the threshold voltage $V_{GG} = V_{TH}$ so initially the device is turned off. With an sinusoidal input signal the output current is an half-wave rectified sinusoidal signal. It is reasonable to express the output current with the Fourier Series coefficient where the DC current is $I_{DS,DC} = \frac{1}{\pi} I_{DS,peak}$. and the fundamental coefficient is $I_L(f_0) = \frac{1}{2} I_{DS,peak}$. As the class A the optimum load is the same because the fundamentals $I_L(f_0)$ and the voltage swing are equal so $\Rightarrow R_{opt,B}$=$R_{opt,A}$.

The maximum efficiency is:

$$\eta_{max} = \frac{P_{RF}}{P_{DC}} = \frac{1}{2}\frac{V_{DD}/2 * I_{DSS}/2}{V_{DD} * I_{DSS}/\pi} = \frac{\pi}{4} \approx 78.5\%$$

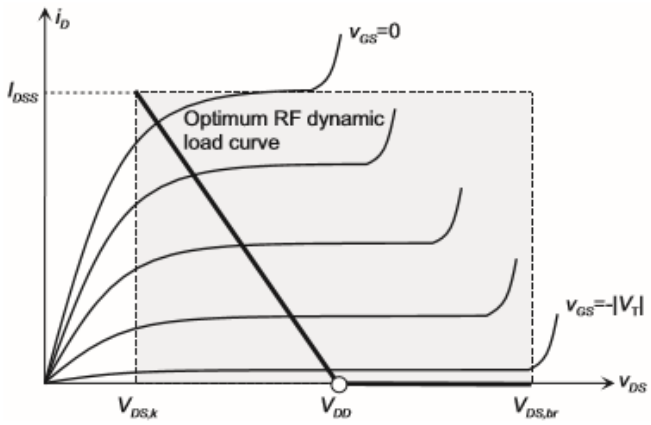


Fig. 1.7 Class B bias and dynamic load line

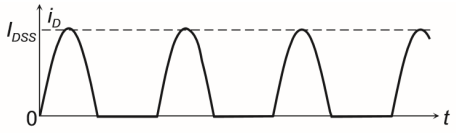


Fig. 1.8 Class B output current waveform

The Gain of Class B 6dB less then that of a Class A because twice the input voltage is needed in order to have the same output current so is needed 4 times the input power so the gain is -6dB with respect to Class A gain. While the efficiency is increased $\eta_{max} = 78.5\%$

The Class B is a non-linear amplifier by implementation and the harmonics need to be tuned by a parallel resonator at fundamental f_0. The calculations for R_{opt} and η_{max} are made considering the harmonics already tuned.

- **Class AB**

  It is an intermediate class between A and B. The gate bias point can be in the region $[V_{TH}, V_{TH}/2]$ and all the other parameters are intermediate between class A and Class B such as, gain which decreases from class A towards class B and also efficiency that increases decreasing the gate bias point.

  Circulation angle of a class AB is from $\alpha = 2\pi(class\,A)$ to $\alpha = \pi(class\,B)$

  Where circulation angle is defined as 2 times π per the ratio between the period of time where the output current is greater than 0 and the period of the periodic signal. $\alpha = 2\pi\frac{T_{ON}}{T_0} = 2\pi T_{ON} f_0$

- **Class C** Decreasing the gate bias voltage V_{GG} lower than V_{TH} we pass from Class B to Class C amplifier .The circulation angle is $\alpha \in [0, \pi]$. Same as for class AB

going towards deep Class C the fundamental and harmonics increases compared to the DC value so efficiency increases and gain decreases till point when device is turned off completely $\eta = 100\%$ but Gain=0 (that is a limit because it does not work as an amplifier).

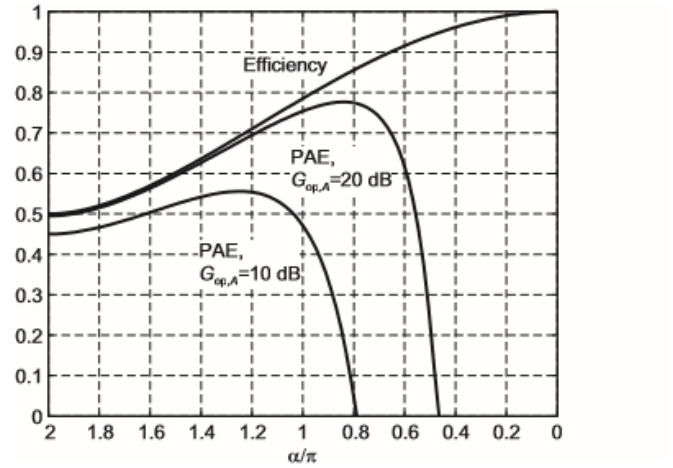


Fig. 1.9 Efficiency η and PAE for different classes of amplifiers
From class A ($\alpha = 2\pi$), class AB $2\pi < \alpha < \pi$, class B ($\alpha = \pi$) towards class C $\alpha < \pi$

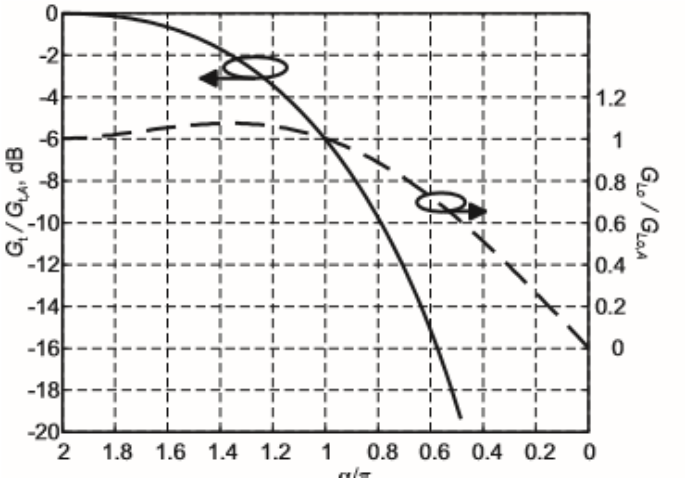


Fig. 1.10 Efficiency η and PAE for different classes of amplifiers
From class A ($\alpha = 2\pi$) , class AB $2\pi < \alpha < \pi$, class B ($\alpha = \pi$) towards class C $\alpha < \pi$

1.3 What is Doherty power amplifier?

Increasing the data rate of communications systems brings in increase of complexity of the signal modulation schemes such as quadrature amplitude modulation (QAM), a phase and amplitude modulation scheme.So we deal with variable envelope signals. In the conventional classes of PA (A, B, AB..) the efficiency is maximum only at saturation so the average efficiency is lower than maximum for signals with PAPR (Peak to Average Power Ratio) greater than 1.

A method to increase the efficiency even for powers lower than the maximum is the Doherty Power Amplifier .

Doherty is a PA design proposed by William H. Doherty [Doherty (1936)] with the goal of having the maximum efficiency of the class B not only at saturation but even at reduced power level with respect to maximum. .

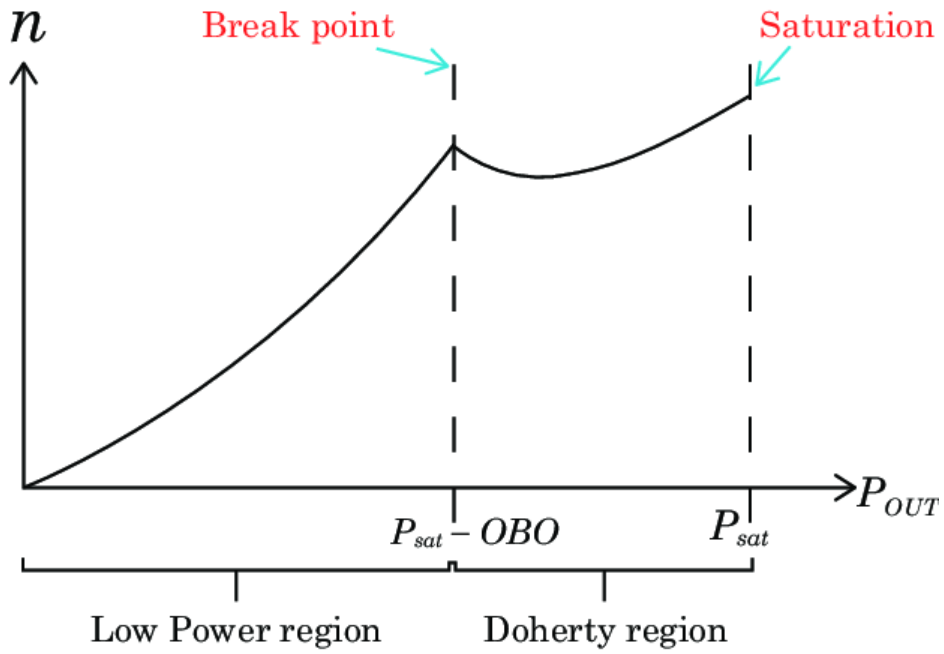


Fig. 1.11 Doherty Efficiency

1.4 Doherty principal of operation

A conventional class B efficiency increases with output power so it is lower than 78.5% for output powers lower than P_{sat}.

$$\eta = \frac{P_{RF}}{P_{DC}} = \frac{P_{RF}}{P_{DC}} \frac{P_{RF,max}}{P_{RF,max}} \frac{P_{DC,max}}{P_{DC,max}} = \eta_{max} \frac{P_{RF}}{P_{RF,max}} \frac{P_{DC,max}}{P_{DC}}$$

Since $P_{DC} \propto I_L * V_{DC}$ but $V_{DC} = V_{DD}$ constant $\Rightarrow P_{DC} \propto I_L \propto \sqrt{P_{RF}}$

$$\eta_{max} \frac{P_{RF}}{P_{RF,max}} \sqrt{\frac{P_{RF,max}}{P_{RF}}} = \eta_{max} \sqrt{OBO}$$

Where OBO (Output Power Back off) is called the level of a signal at the output of an amplifier relative to the maximum possible output level. In order to increase the efficiency equal to maximum efficiency of class B the Doherty idea of PA should be used.

To obtain class B η_{max} for a certain OBO when the biasing of the amplifier is that of class B then the load seen be the device should be different from R_{opt}. The output drain current (I_D) will be the same as that of a Class B amplifier since it does not depend on the load.With the same output current and different load the output voltage will change.
If the load is such that at OBO the drain voltage is saturated, $V_D(t)$ is a sinusoidal voltage that goes from 0 to $2V_{DD}$ and the fundamental voltage at load is $V_L(f_0) = V_{DD} \sin(2\pi f_0 t)$

$$I_{DC} = \frac{2}{\pi} I_{D,OBO,peak} \quad and \quad I_D(f_0) = \frac{1}{2} I_{D,OBO,peak}$$

.

$$\Rightarrow \eta_{OBO} = \frac{P_{RF}}{P_{DC}} = \frac{\frac{1}{2} I_D(f_0) * V_{DD}}{I_{DC} * V_{DD}} = \frac{\pi}{4} = \eta_{max}$$

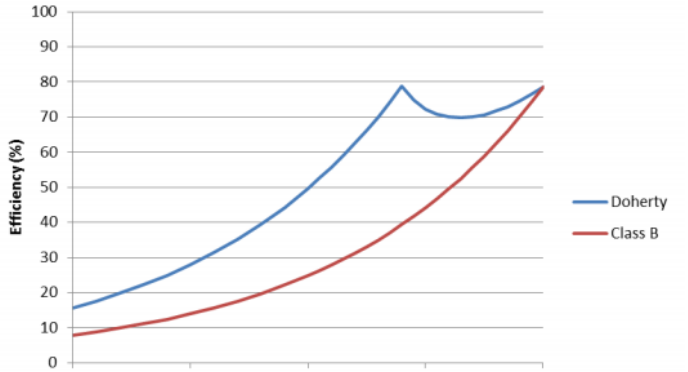


Fig. 1.12 Doherty and Class B efficiency vs P_{out}

In fig1.12 is shown the efficiency of a Doherty compared to a class B. With the correct load at OBO as described can be achieved maximum efficiency but at the same time there is the maximum efficiency even at saturation so the load at saturation should be the optimum load of a class B. $R_{L,sat} = R_{opt}$. **Dynamic load modulation** is needed (see fig1.13)

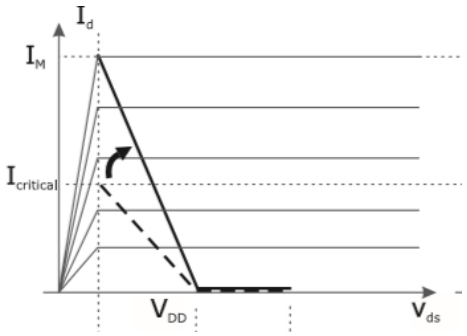
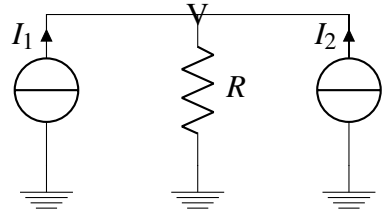


Fig. 1.13 Dynamic load line modulation of the main device

Dynamic load modulation is achieved using **active load pull** which principle is explained as follows:

Active Load Pull

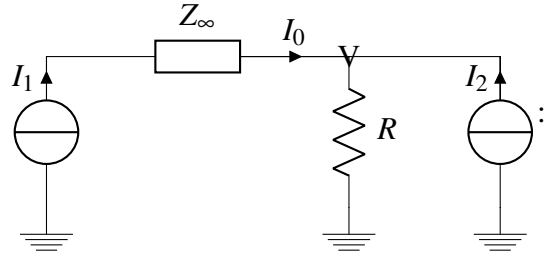


$$Active\ load\ pull:\ Z_1 = \frac{V}{I_1} = R\frac{I_1+I_2}{I_1} = R(1+\frac{I_2}{I_1}) \tag{1.1}$$

I_1 and I_2 are two independent current sources. Z1 is the load seen by the current source I1 node. By the formula can understand that if we increase I_2 in our case auxiliary current the load seen by main will increase. This is the active load pull that makes possible the dynamic load modulation but we need main impedance to decrease while I_2 is turned on and increasing its values.

A possible method to do it is **impedance inversion**. This is done by using a quarter wavelength transmission line in center frequency .

Active load Pull with impedance inversion



$$: Z_1 = \frac{Z_\infty^2}{R(\frac{I_0+I_2}{I_0})} = \frac{Z_\infty}{R}\frac{I_0}{I_0+I_2} = \frac{Z_\infty}{R}(1-\frac{I_2}{I_0+I_2}) \tag{1.2}$$

Z_∞- is a quarter wave transformer at center frequency.

Based on equation (eq1.2) we have to find the values of R and Z_∞ to match the Doherty requirements at a certain OBO.

Doherty amplifier is based on this idea and instead of the two current sources there are two active devices. The current I_1 is generated by the main device and current I_2 by the auxiliary device.(see fig1.14).

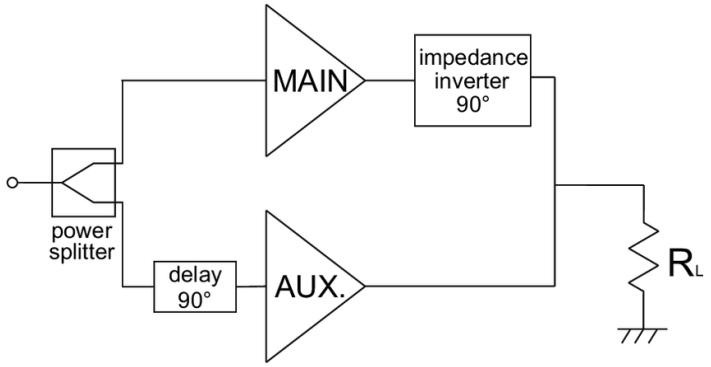


Fig. 1.14 Doherty amplifier scheme

Initially until back off the Auxiliary device is turned off (in this case modelled by I_2). At back off the main device current can be expresses as

$$1^{st} equation: \quad I_{main,backoff} = \alpha I_{dss,main} \ \ where \ \ \alpha = \frac{P_{out,main,backoff}}{P_{out,mainsat}} \tag{1.3}$$

and since the main drain voltage should be saturated V_{main}=$2V_{DD}$ Z_1 should be equal to $\frac{2V_{DD}}{I_{dss}}$ .Now we have the second equation :

$$2^{nd} equation: \quad Z_{1,Backoff} = \frac{Z_\infty^2}{R} = \frac{R_{OPT}}{\alpha} \tag{1.4}$$

We can obtain the third equation from the value of impedance at saturation which as we mentioned should be R_{opt} and from equation (eq1.2) is equal to :

$$3^{rd} equation: \quad Z_{1,sat} = \frac{Z_\infty^2}{R}(1 - \frac{I_2}{I_0 + I_2}) = \frac{R_{opt}}{\alpha}(1 - \frac{I_2}{I_0 + I_2}) = R_{OPT} \Rightarrow I_2 = I_0(1 - \alpha) \tag{1.5}$$

Also the current I_0 is unknown and some other condition should be imposed .The condition is that the both amplifier voltage saturation is equal to V_{br} so $2V_{DD}$ since they usually (and in our project case are similar technologies).

So at saturation since the power at both ends of the quarter wave transformer is equal (there are no losses) and the voltages are equal to $2V_{DD}$ then :

$$4^{th}equation: \quad I_{0,sat} = I_{1,sat} \tag{1.6}$$

In this project the design is made for optimization of efficiency at **OBO=6dB**. So solving the equations above the solutions are

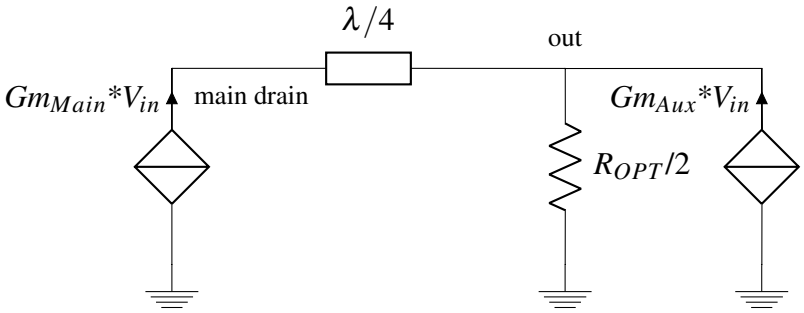
- $\alpha = 0.5$
- $Z_{\infty} = R_{opt}$
- $R_{Load} = R_{opt}/2$
- $I_{dssaux} = I_{dssmain}$

The auxiliary device should provide the same current at saturation as the main while instead at Back-off is turned off. If we use the same input voltage for both devices then $\Rightarrow g_{m,Aux}=2*g_{m,Main}$.

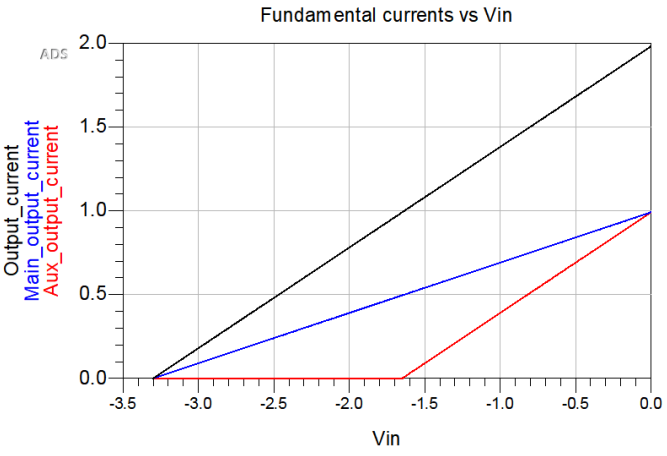
Also the current provided by the main has a phase delay of 90° with respect to the auxiliary drain current so a phase regulation is needed . We can add a 90° transmission line at output or input of the auxiliary. It is better to add at the input where we are dealing with lower powers so losses will be lower.

1.5 Ideal Doherty simulations

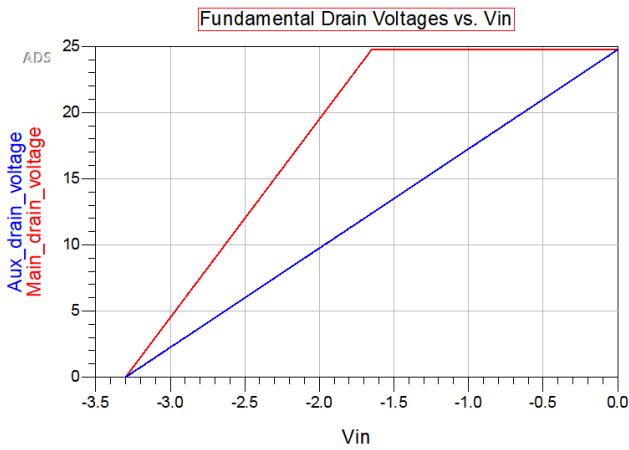
To better understand in detail the behaviour of the Doherty amplifier and its parameters an initial ideal circuits simulation si needed. The ideal Doherty can be designed replacing the real HEMT devices with ideal controlled current sources.



As we mentioned in the previous section we have to change the load seen by the main device dynamically. So we have to use the *Active Load Pull* that is possible by the current generated by the Auxiliary . Current generators provide a sinusoidal current at center frequency 3.5GHz. Since there is a 90° transmission line the current of the auxiliary should have a phase of 90° with respect to the main current so the can be summed up in phase at output node.



a)



b)

Fig. 1.15 Output currents a), Drain voltages b)

As we can see from fig 1.15 the main voltage saturates at half swing of the input voltage . That is possible because the load seen by the main till this point ($V_{in} = V_t/2$) is equal to $2R_{OPT}$.In this way the efficiency is equal to the saturation class B efficiency so 78.8%.Meanwhile the auxiliary is turned off (so the load seen by auxiliary is ∞). While the current of the main increases linearly if the load seen by the main is constant then the efficiency will drop so we

have to decrease the load with the increasing of the inp

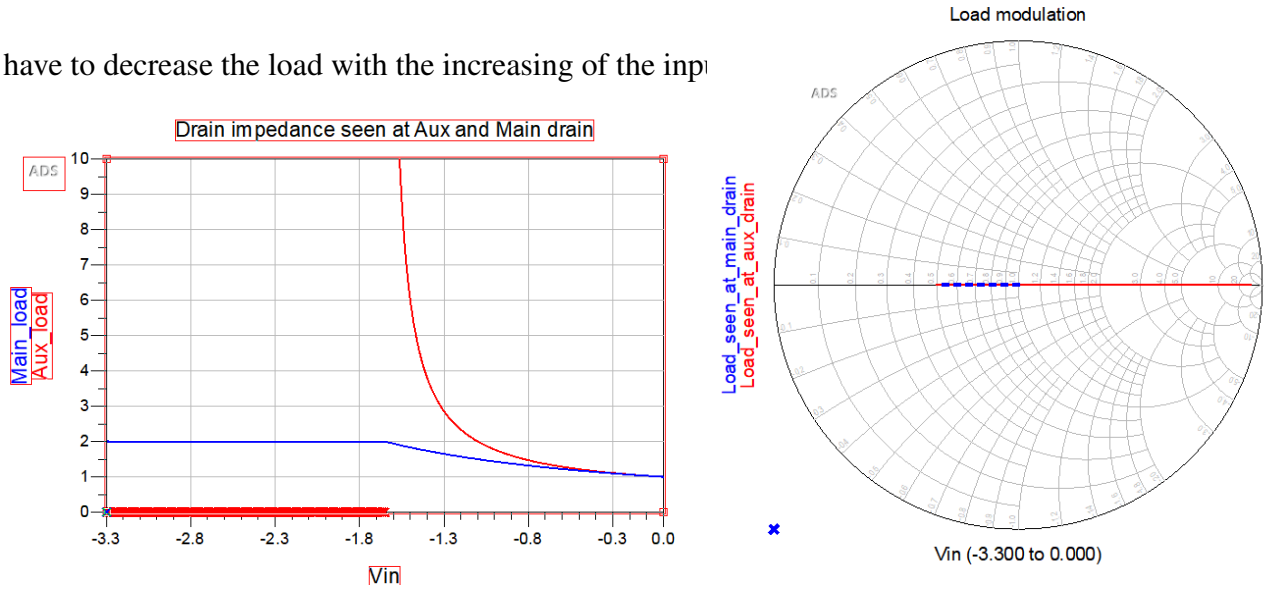


Fig. 1.16 Load modulation

As seen by the simulating the main load is constant and equal to $2R_{opt}$ when the auxiliary is turned off , while load of auxiliary is ∞. The main load is modulated from $2R_{opt}$ to R_{opt} in saturation .Even auxiliary has the same load in saturation since the maximum currents are equal. And finally the graph (fig1.17) of efficiency with the 2 maximum, at saturation and -6dB from saturation.

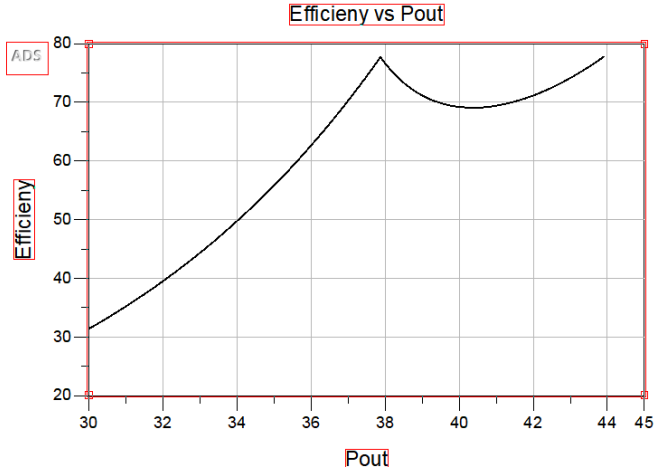


Fig. 1.17 efficiency simulations

1.6 Real Doherty design

Starting with the first difference between the ideal Doherty with current sources and the real Doherty which will be made by two active devices acting as controlled current sources.
In the ideal case the 2 device should operate in Class B ($V_{GS} = V_{TH}$) and the auxiliary one should have a double g_m with respect to the main device so a double gate width .But in a real design we will use the same device so their g_m if they are biased in Class B will be the same and also the second cannot be turned on at back off if without any external circuit .Since even the auxiliary will be in class B than it will be turned on if we transfer some power .So that other solution is available : AB-C Doherty .The main amplifier is biased in class AB while the auxiliary amplifier is biased in deep class C.

This preliminary design is based on the book [P. Colantonio and Limiti (2009)].
To better understand this have to study the waveform of the currents for the 2 classes in order to create the corresponded behaviour of the 2 ideal current sources studied in section 1.5.

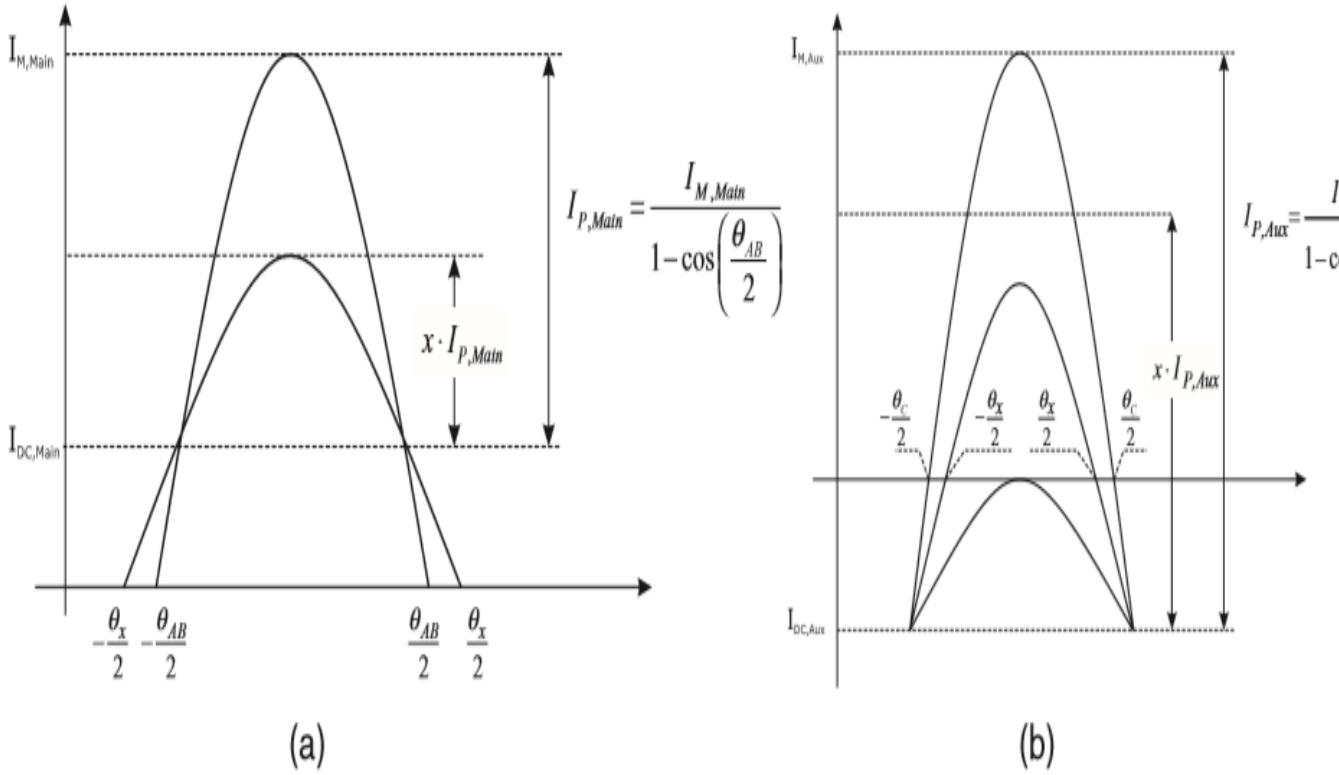


Fig. 1.18 Class AB and C current waveform

The waveform of the main and auxiliary amplifier or class AB and C amplifier to better be studied should be represented by the Fourier series.
I wanted to put a reminder that in this preliminary design some of the parameters will be considered like ideal , for example a constant g_m , current that have a maximum saturation after which the waveform becomes flat at the top , only positive currents.
The DC current(bias current) of the class AB is greater than zero while the DC current of a class C is lower than zero and this is a conventional use because if the current is lower than zero there is no current on the device (device turned off).This will help later to understand in which point should the auxiliary be biased in order to be turned off till the break off .
Let introduce a parameter x (0<x<1) describing the current evolution from DC (x =0) to a maximum value I_M (x=1).x is also an quantity of the input sinusoidal signal .

θ is the current conduction angle by definition and θ_M is the value of the current conduction angle (CCA) arising for x =1.

$$\cos(\frac{\theta_M}{2}) = x\cos(\frac{\theta_x}{2}) \tag{1.7}$$

Analyzing the Fourier series of the waveforms we obtain the formulas for the DC and First harmonic as follows:

$$I_0(x) = \begin{cases} I_{DC}, & \text{if } x < x_{min} \\ \frac{x \cdot I_m}{2\pi} \frac{2 \cdot \sin(\frac{\theta_x}{2}) - \cos(\frac{\theta_x}{2}) \cdot \theta_x}{1 - \cos(\frac{\theta_M}{2})} & \text{otherwise} \end{cases} \tag{1.8}$$

$$I_1(x) = \begin{cases} 0, & \text{if } x < x_{min} \\ \frac{x \cdot I_m}{2\pi} \frac{(\theta_x) - \sin(\theta_x)}{1 - \cos(\frac{\theta_M}{2})} & \text{otherwise} \end{cases} \tag{1.9}$$

The formulas are valid for the main and auxiliary amplifier with their specific values of x_{min} and I_M respectively.For the main amplifier the x_{min} is considered till the point where the total current start to clip(arrives at zero) and the value of x is called x_A while for the auxiliary amplifier x_{min} is the point where amplifier is turned on and is called x_{break}.

Let see the the behaviour of the DC and fundamental of a class AB (biased near class B) amplifier and a deep class C.(see fig 1.19)

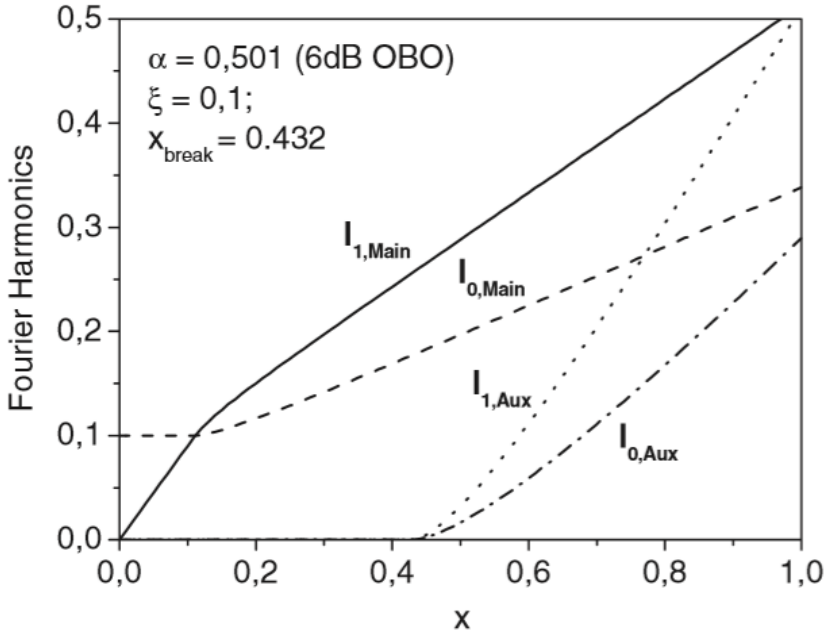


Fig. 1.19 DC and fundamental of Main and Aux

The case of the fig 1.19 is an example of a class AB and C amplifier which graph gives an idea of the behaviour of the currents .As we see the C class amplifier is turned of till the break off then the current is increasing almost twice as fast of that of a class B .This behaviour mimic the behaviour that we expect in case of ideal Doherty with the auxiliary amplifier having double g_m.

The parameters that are defined before the design are , the Bias drain voltage V_{DC}, g_m of the single devices, I_{MAX}.Now we have to find the bias points , the optimal resistance and the power splitting between main.

To find the parameters it is better to divide the analyzes in two regions , first the low power region where the auxiliary is turned off so $[0;x_{break}]$ and doherty region from x=x_{break} till saturation (x=1).

Low power region only the main device is turned on and biased in class AB. The main amplifier see the load resistance transformed by the quarter wave transformer . The optimum load seen by the main device at x=x_{break} should be

$$R_{opt,break} = \frac{V_{DD} - V_{knee}}{I_1(\theta_{x,break})} = \frac{Z_\infty^2}{R_{Load}} \tag{1.10}$$

In Doherty power region, The power generated by the device is current×voltage so since main voltage is at maximum swing so its constant the power from the main is proportional to the current $P_{out,main} \propto I_{out,main}$. Then if we define α the parameter of the ratio

$$\alpha = \frac{P_{main,break}}{P_{main,max}} = \frac{I_1(\theta_{x,break})}{I_1(\theta_{AB})} \tag{1.11}$$

Since the maximum power delivered by the auxiliary device and main are the same then α represents the amplifier Back-Off (OBO). In this project the OBO=6dB as we have mentioned in **??** and the corresponding α=0.5 .

From the above equation and from eq1.9 can find a relation between x_{break} and θ_{AB} as follows

$$x_{break} * [\theta_{x,break} - \sin(\theta_{x,break})] = \alpha * [\theta_{AB} - \sin(\theta_{AB})] \tag{1.12}$$

For the correct load modulation we have to consider both the fundamental of the main (I_{1main}) and that of the auxiliary (I_{1aux}).The output voltage of the main device should be constant and equal to the maximum voltage swing so

$$\frac{R_{opt,break}}{R_{opt,sat}} = \frac{I_{1main}(\theta_{AB})}{I_{1main}(\theta_{x,break})} = \frac{1}{\alpha} \tag{1.13}$$

So based in eq.1.4 we obtain the expression that relates the main and aux current:

$$\alpha \left[1 + \frac{I_{1aux}(\theta_C)}{I_{1main}(\theta_{AB})} \right] = 1$$

Considering the above relation the same as the ideal Doherty analyzed in section1.5 and from the fundamental current formulas of class AB C (eq1.9) the maximum drain current of class C and class AB are not the same if we want the fundamental to be equal.If $I_{1aux}(\theta_C)$=$I_{1main}(\theta_{AB}) \Rightarrow I_{M,main} < I_{M,aux}$. The exact formula is :

$$I_{M,aux} = I_{M,main} \frac{1-\alpha}{\alpha} \frac{1-\cos(\frac{\theta_C}{2})}{\theta_C - \sin(\theta_C)} \frac{\theta_{AB} - \sin(\theta_{AB})}{1-\cos(\frac{\theta_{AB}}{2})} \tag{1.14}$$

$\xi = \frac{I_{DC,main}}{I_{M,main}}$

Design First condition to impose is the maximum current of one of the devices .Since the maximum is the auxiliary choose $I_{M,Aux}$ the maximum device current $I_{M,Aux} = I_{DSS}$.

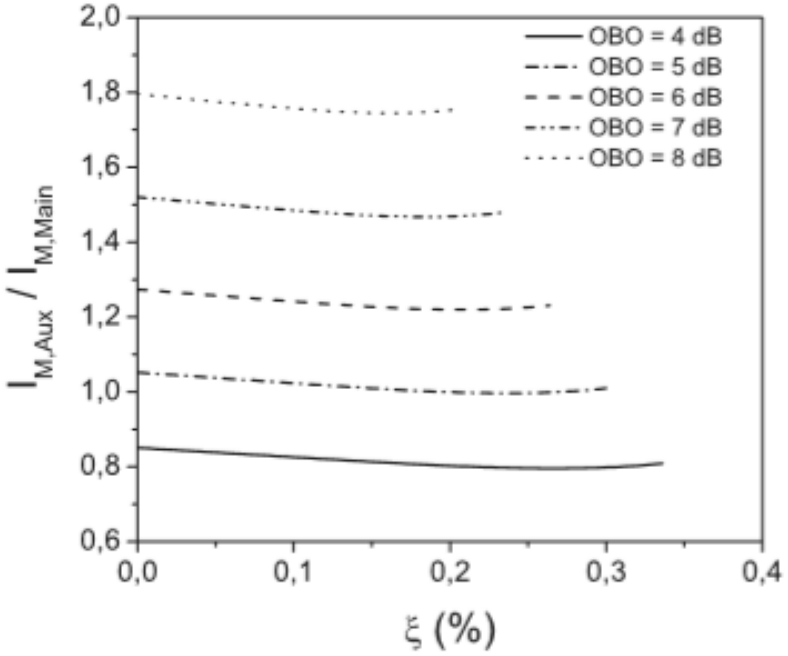


Fig. 1.20 Ratio between $I_{M,Aux}$ and $I_{M,Main}$ as a function of main bias point (ξ)

From eq1.14 we can find $I_{M,MAin}$. To find the $I_{DC,Main}$ the ratio ξ is needed and that is found from a factor the non linearity factor LF that depends in ξ. from the graph..

From the DC currents we can obtain the bias gate voltages $V_{GG,main}$ and $V_{GG,aux}$.

With reference to the design procedure in book Doherty (1936) i have implemented a Matlab code to give me the results of the parameters such as the bias points , the load resistances and the power splitting .

Power Splitting The input power splitting ratio between main and auxiliary which depend on the bias points of the device and even in the input resistances R_{in}:

$$\Lambda_C = \frac{P_{in,Aux}}{P_{in,Main}} = \frac{K_V^2}{\frac{R_{in,Aux}}{R_{in,Main}} + K_V^2}$$

where K_V=$\frac{V_{in,Aux}}{V_{in,Main}}$ with V_{in} tailored at saturation or back-off.

The results for the preliminary design are as follows :

Table 1.1 Preliminary calculation results

$V_{GG,Main}$	$V_{GG,Aux}$	R_L	Z_∞	$\Lambda_A B$	Λ_C
-3.2830	-6.9413	30.9766	61.9531	0.3880	0.9216

Chapter 2

Device parameters

2.1 Device DC characteristics

Before designing the power amplifier is needed to investigate the DC characteristics of the single device . The maximum output curent ,threshold voltage break down voltage,optimum load resistance etc... are the parameters needed for design obtained by the output and transcharacteristics. The trancharacteristics is represented by the drain source current I_{DS} obtained varying the Drain voltage from 0 to a high voltage where we expect the breakdown for each gate voltage.

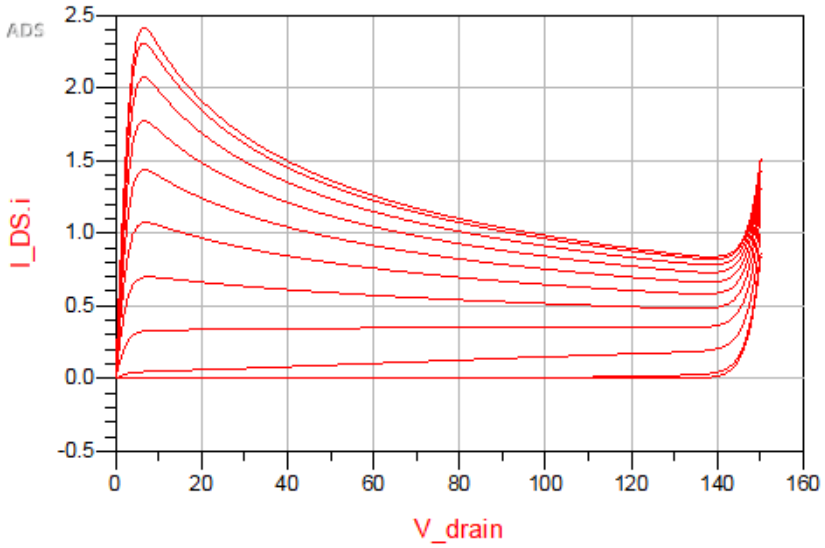


Fig. 2.1 Transcharacteristics

The first thing to notice is the breakdown voltage of around 150V as it is expected since the Cree HEMT is in GaN (gallium nitride) which has a very high critical electric field.
For constant gate voltage the current has a negative slope increasing the drain voltage and this is due to thermic effects. Will retake the figure after considering the output characteristics which is the drain current I_{DS} vs. Gate voltage for a fixed drain voltage . The constant drain voltage should be such that the device is in the saturation region during the gate voltage sweep .Anticipated the bias drain voltage of the power amplifier is 28 V so choosing 28V is a reasonable value seen even by the transcharacteristic (see fig 2.1). The behaviour of the

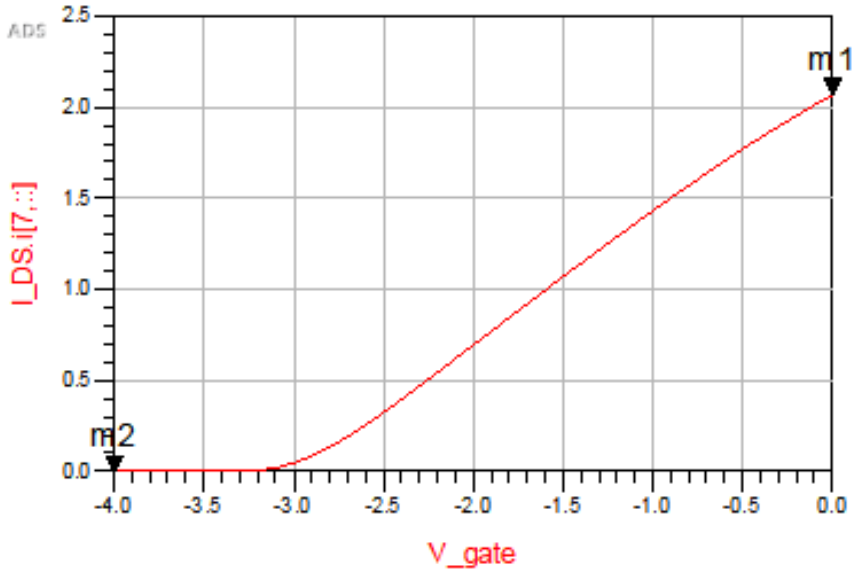


Fig. 2.2 Output characteristic

current is not linear but can be approximated by a linear relation so we can use a constant gm that can approximate the current versus gate voltage(V_G) like :$I_{DS} = g_m * V_G$

- **Threshold voltage** $\mathbf{V}_{TH} \approx 3.2V$
- $\mathbf{g}_m$**=0.646** Ω^{-1}
- $\mathbf{I}_{DSS}$**≈2A**
- $\mathbf{R}_{opt}$**≈25Ω**
- $\mathbf{V}_{knee}$**≈6V**

2.2 Device small signal parameters

HEMT small signal equivalent circuit models the device behaviour in small signal condition around a bias point. The simpliest model is the model in the fig 2.3 with an RL circuit modelling the extrinsic parasitics for 3 ports[M.Pirola (2017)].
The project is about power amplifier so it operates in large signal and the small signal should not be important ,but however some of the parameters can be obtained by SSM model such as the extrinsic parasitics which are constant with amplitude of the signals.

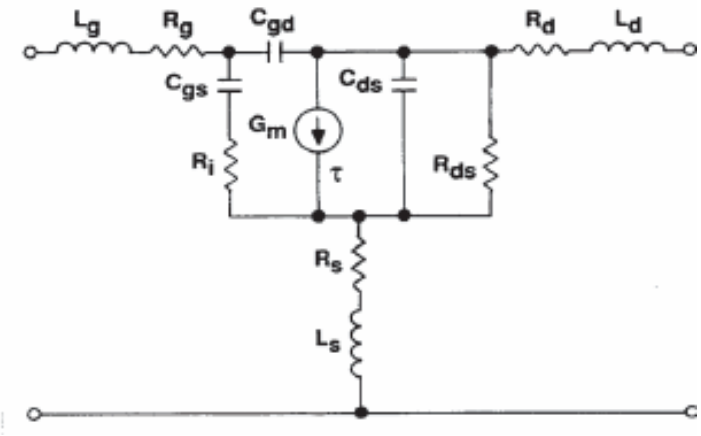


Fig. 2.3 Small signal circuit

Small signal parameters depend on the DC working point so have to know the bias point previously .The bias point are V_{DC}=28V,V_{GS}=-3.15V for the main amplifier and V_{DC}=28V,V_{GS}=-7V for the auxiliary one.
To find the parasitic elements values a two step procedure is needed :
1.Cold Fet measurements
2.Hot Fet measurements

Cold fet measurements

In cold fet condition the device gate channel is in direct conduction since for positive V_{GS} the gate-drain and gate-source behave as a diode .The Drain and Source are grounded and the gate is V_{GS}=4V is in direct conduction (see fig 2.4. The channel resistance can be considered very low w.r.t the extrinsic resistances.So the 3 intrinsic ports can be considered short circuited .

The circuit becomes now a simple T-passive circuit . We have to simulate the ciruit for a single frequency in this case f=3.5GHz,is this project center frequency ,then obtain the S matrix of

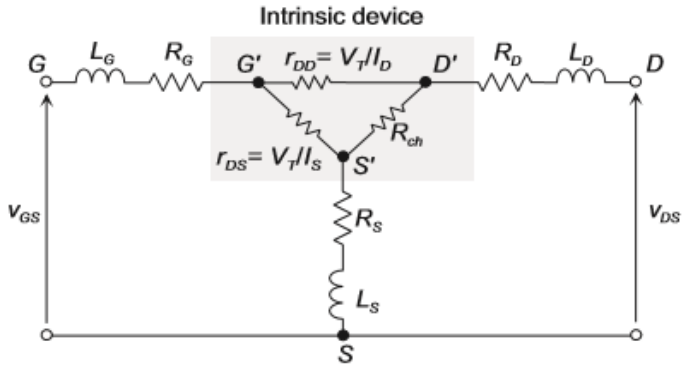


Fig. 2.4 Cold Fet Equivalent circuit

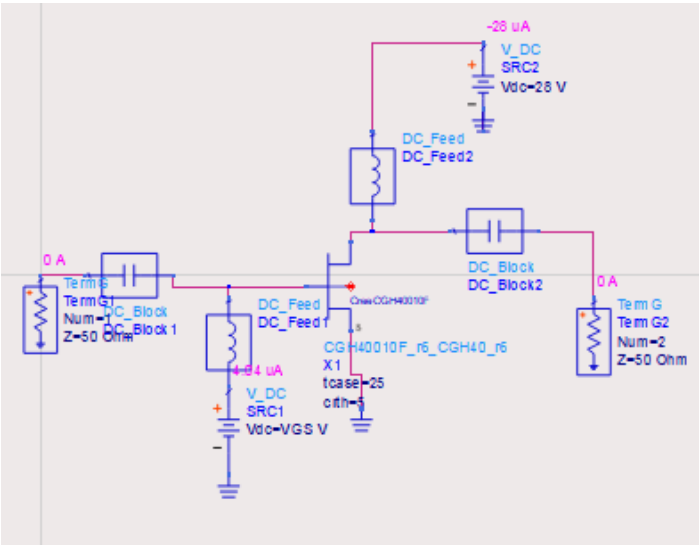


Fig. 2.5 Small signal simulation

Table 2.1 Extrinsic parameters

resistance	value [Ω]	inductance	value [nF]
R_G	1.585	L_G	0.8594
R_D	1.55	L_D	0.86
R_S	1.06	L_S	0.0272

the 2 port circuit (1 port Gate-Source the other Drain-Source) which is transformed into Z matrix .the real part correspond to the resistances while the imaginary to the inductances . In this way we obtain $L_G, L_D, L_S, R_G, R_D, R_S$

Hot Fet measurements In this type of measurements the device is biased in the normal operation point of an amplifier depending where the power amplifier bias point ,since the intrinsic parameters depend on the *bias point* . The parameters for the 2 amplifiers will be different since they are biased in different points(different gate bias ,class AB and C).

We have other 7 unknowns .These can be solved with an linear system of 7 equation . In fact if it is available Z matrix of the 2 port circuit(fig2.3) we have 4 imaginary equations (Z_{11} Z_{12} Z_{21} Z_{22}) so 8 linear equations . From the S parameters can transform the S matrix into Z matrix. Since the extrinsic parameters are already known from the Z matrix and extrinsic parameters can obtain the intrinsic Z matrix(Z_{int}) and take out the extrinsic part which is known (the 3 extrinsic LR circuits are in series with each branch of the T circuit).So we can obtain Z_{int} as :

$Z_{11,int}$=Z_{11}-(R_G-j*L_G)-(R_S-j*L_S)

$Z_{12,int}$=Z_{12}-(R_S-j*L_S)

$Z_{21,int}$=Z_{21}-(R_S-j*L_S)

$Z_{22,int}$=Z_{22}-(R_D-j*L_D)-(R_S-j*L_S)

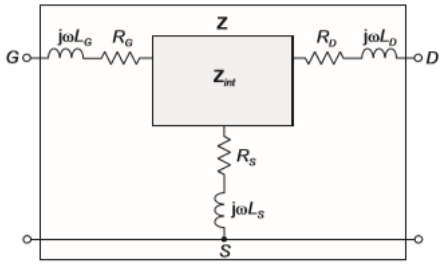


Fig. 2.6 Dembeding the intrinsic parasistic

Then from the equivalent matrix of the intrinsic ciruit can find the relations :

$$Y_{11,int} = \frac{j\omega C_{GS}}{1 + j_{GS} R_I} + j_{GD}$$

$$Y_{12,int} = -j\omega C_{GD}$$

$$Y_{21,int} = \frac{g_m e^{j\omega\tau}}{1 + j\omega C_{GS} R_I} - j\omega C_{GD}$$

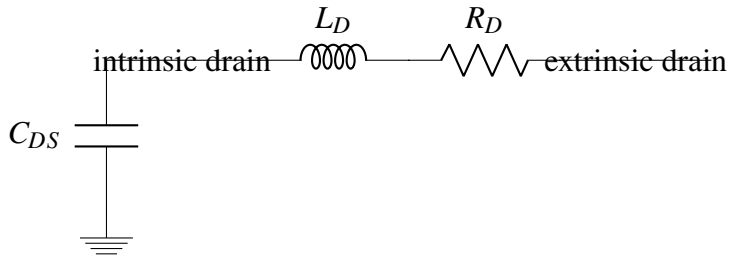
$$Y_{22,int} = j\omega(C_{GD} + C_{DS} + \frac{1}{R_{DS}}$$

Then with deembeding procedure we obtain the intrinsic parameters . As we said these parameters change with bias point and the signal amplitude so why they are important any more if the amplifier will work till saturation ,so will exploit all the range for the signals .

height	value [pF]		value [pF]
C_{GD}	0.21	C_{DS}	0.9594

The values of C_{GD} and C_{DS} were similiar for the class AB bias point and class C . In conclusion the incudtance L_D and the capacitance C_{DS} aprrocimeta cery well the behaviour in this project frequency band [3.2GHz-3.8GHz] .This is also confirmed by another simulation ehich is as follows :

Turning off the device. By fixing the gate voltage to a negative value lower than V_{TH} (in my case V_{GS}=-8V) the channel of the device is not formed so there is no C_{GD} capacitance effect in the output or input and there is no current generation no g_m.So the device input and output are almost separated .By simulating the output drain node with S-parameters will see only the effect of drain extrinsic parameters and C_{DS} which does not depend on the channel creation . With this simulations in the band [3.2-3.8 GHz] single L_S and C_{DS} approximate very well the behaviour of the device in output .



2.3 Capacitance models

Starting from the capacitances which are parameters related to the working principle of the HEMT .The model of the capacitances of a GaN HEMT can be found in the paper [A. Zhang L. Zhang and M. Chan (2014)] First the C_{G_S} changes a lot depending on the bias point of the gate and the gate-channel signal amplitude .We can see in the figure (fig 2.7)

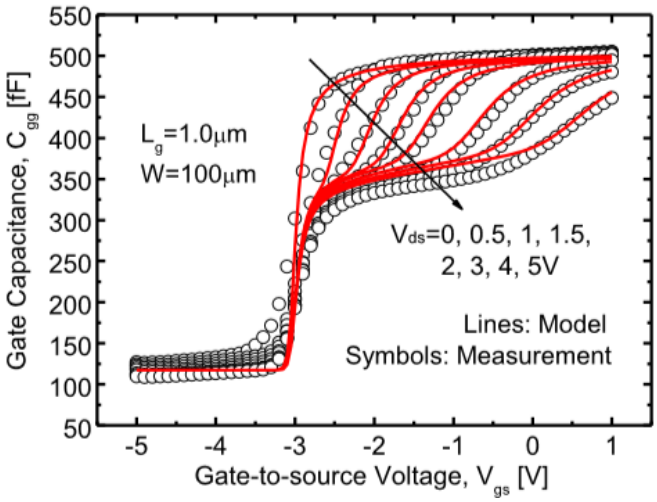


Fig. 2.7 Capacitance Vs gate voltage

As seen even by the transcharacteristics(see fig 2.1) for V_{DS} lower than 5V the device is out of saturation so is not linear anymore . Its better to study the linearity for V_{DS} greater than 5-6V.
In fig 2.7 is shown C_{GG} which is: $C_{GG} = C_{GS} + C_{GD}$

For C_{GD} see fig 2.8 . C_{GD} in first approximation is constant w.r.t to V_{GS} and V_{DS} for values of drain-source voltage V_{DS}>6V . So when the device is in saturation the Gate-Source capacitance C_{GS} is proportional to C_{GG} so is a non linear capacitance that depends strongly by the gate and drain voltage .

In this figure the value of V_{GD} is presented for 2 different values of gate-source voltage and different values of channel length sweeping V_{DS}.As we can see in first approximation when device in saturation the capacitance is almost constant and does not depend on the drain or gate volatges thus does not present nonlinearisties in the amplifier . Similiar consideration can be made for drain to source capacitance which is :$C_{DS} = C_{DD} - C_{GD}$
C_{DD} and C_{GD} are both constant in saturation and not depending on gate voltage so even C_{DS} can be considered constant and does not introduce nonlinearities. Summarizing the the C_{GS} depend srongly on the bias point and on the input signal so analyzing it in small signal

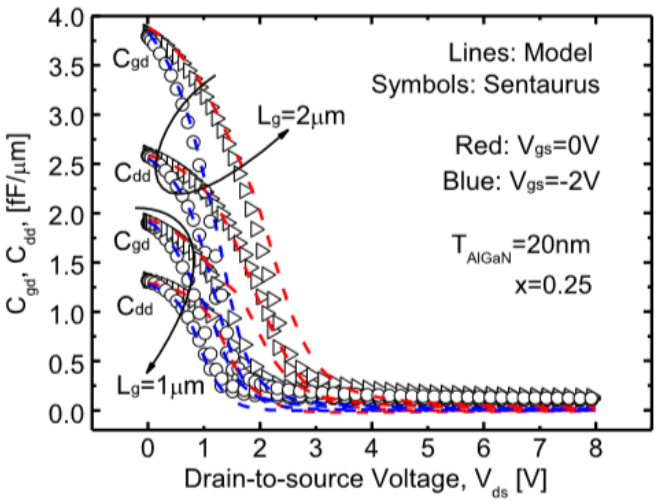


Fig. 2.8 Capacitance Vs drain-source voltage

muasurements is not significantly important fir the design of the amplifier as we will see even later . It also introduces nonlinearities in the amplifier.

While the drain to source C_{DS} and gate to drain C_{GD} capacitances can be considered constant in saturation so their value of small signal measurements if the bias point is in saturation is in first approximation very important for the design of the matching networks especially the output matching network.

Chapter 3

Circuit design

3.1 Predesign simulations

After the theoretical results I implemented the design in ADS to verify with simulations. In the first simulation did not use a splitter so can better understand and optimize the parameters ,instead i used two separate input generators for the main and auxiliary . Also to verify the results the input and output section has to be matched .For this reason I used as e preliminary step not a real matching network but negative components(negative inductors and capacitors) to cancel the effect of the parasitic in all frequencies.The parasitics to negate are the results of the parasitic from table2.1 and the intrinsic capacitances. In the drain part the drain inductance L_D should be negated by a negative inductance in series and then by a shunt capacitance which takes into account the effect of the C_{DS} and the C_{GD} between the intrinsic Drain-Source nodes.The C_{GD} role is given by the Miller effect and the formula in which C_{GD} is equivalent to a shunt capacitance in input and a shunt in output[L. Piazzon (2014)][L. Cótimos Nunes (????)] . The shunt in input is $C_{in,Miller}$=C_{GD}(1+A_v) while

$$C_{out,Miller} = C_{GD}(1 + 1/A_v)$$

Miller capacitance in output is added whith the drain-source parasitic C_{DS}. The gain A_v in formula is greater than 1 so the the term 1/A_v can be neglected in the first view .

$$C_{out} \approx C_{DS} + C_{GD}$$

For the input a series negative inductance which behaves as imaginary part of the optimum input seen get by the load pull measurements(.The same procedure even for each power

generators resistances (see later ...)

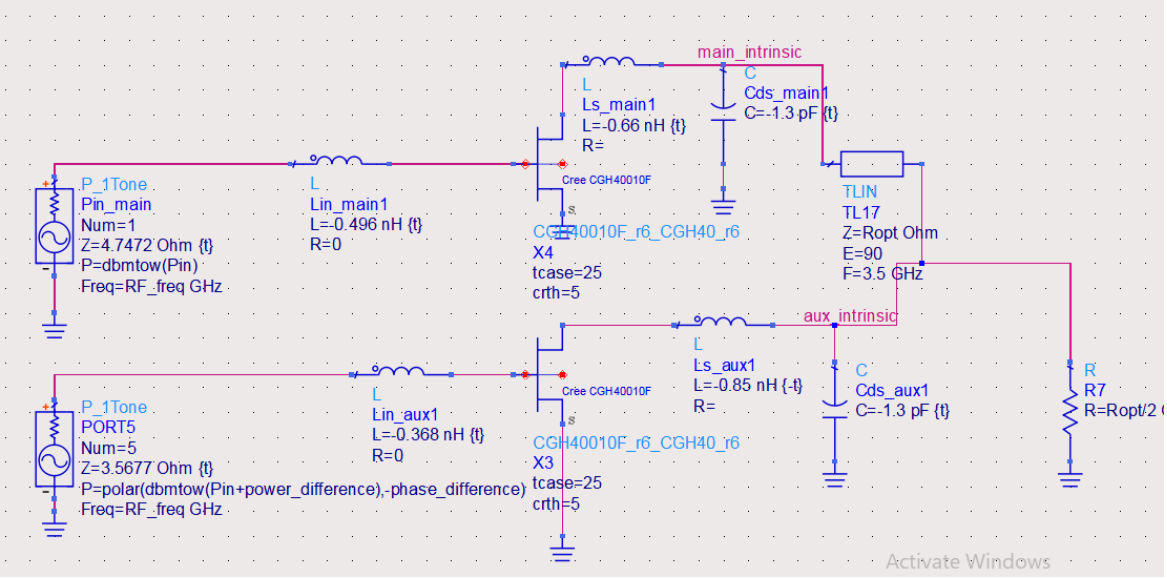


Fig. 3.1 Schematic ADS negate parasitics

The real schematic is found in the project ADS file (...).To be careful this is not real because the bias points and DC Block and Feed are not present (this is done for a more clear figure).

Initially the power source resistances are equal to the real part of the optimum input matching impedance R_G=$\mathscr{R}$e$\{Z_{in,opt}\}$. While the phase of the auxiliary source power is of 90° in retard w.r.t main power source ,in order to compensate the output Q.W.T.Also there is a power difference between the two source power generators to model the power splitting .

The drain bias voltages are fixed at 28V .So the optimum resistance initially will consider as a class B optimum resistance.

$$R_{opt} = \frac{2(V_{DD} - V_{knee})}{I_{DSS}} \approx \frac{2(28-6)}{2} = 22\Omega$$

The DC path of the circuit should be separated by the input source and load (RF part).This is done with the use of Bias Tee circuit .

Bias Tee circuit is ideally made up of two elements, a very big capacitor which is an open at DC while is short circuited in other frequencies greater than 0 and a very big inductor which is shorted at DC and an open circuit at other frequencies .So the DC power of gate and drain are separated by the source power and load respectively . There is no effect on the matching circuits.

Simulations In the first design made even in calculation (sec1.5) the parameters are approximated such are :g_m of the devices are considered as constant ,the drain current has not an abrupt behaviour around threshold V_{TH} (see fig2.2).Also the input resistances of the devices are not constant with power which effects the power splitting . Meanwhile in the output section the parasitcs have not the same effect as the small signal.

To obtain the desired behaviour tunning of parameters is needed in order to fix the different parameters of a Doherty as seen by the theory.Different parameters should be studied as the currents ,voltages and impedances at the same time since they are related .

To begin with the current behaviour and keeping in mind the ideal currents (fig**??**)

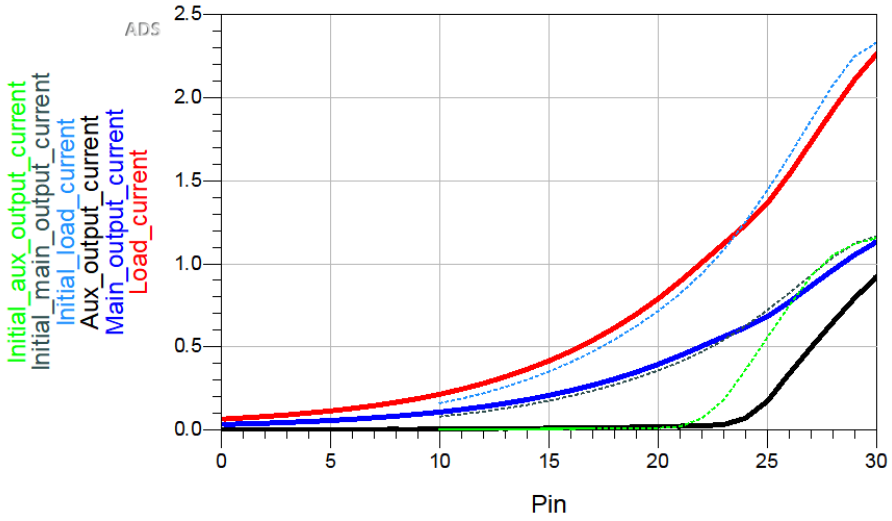


Fig. 3.3 Output fundamental current Aux and Main before and after optimization

Ideally the aux current should be turned on when when the main current is $I_{main}(f_0)$=0.5A.But in the first design (dot line) aux is turned on before so the modulation is not correct .The anticipated turning of the Aux happens when the bias voltage of the aux V_{GG} is higher than it should be or the power splitting should be changed in order to transfer less power at Auxiliary device .The initial calculation for the power spitting is done considering the input resistances of aux and main equal but in fact since they are biased in different points even the optimal input resistance (for power transfer) is different $R_{in,Aux} \neq R_{in,Main}$

As described previously Auxiliary device is turned on before main device voltage arriving at saturation as seen in figure (fig**??** the fundamental voltage of the main device is not saturated and it does not remain constant in saturation in after back off.This happens even because the currents are not summed up in phase at the output .After the correction of power splitting and the output parasitics of the main (solid line) arrives at a larger voltage and remains almost constant . In the first case (dot line) another problem is the insufficient aux fundamental current to correctly modulate the main impedance .To increase Aux fundamental $I_{Aux}(f_0)$ aux device should be biased in deeper class C(so lower V_{GG}).

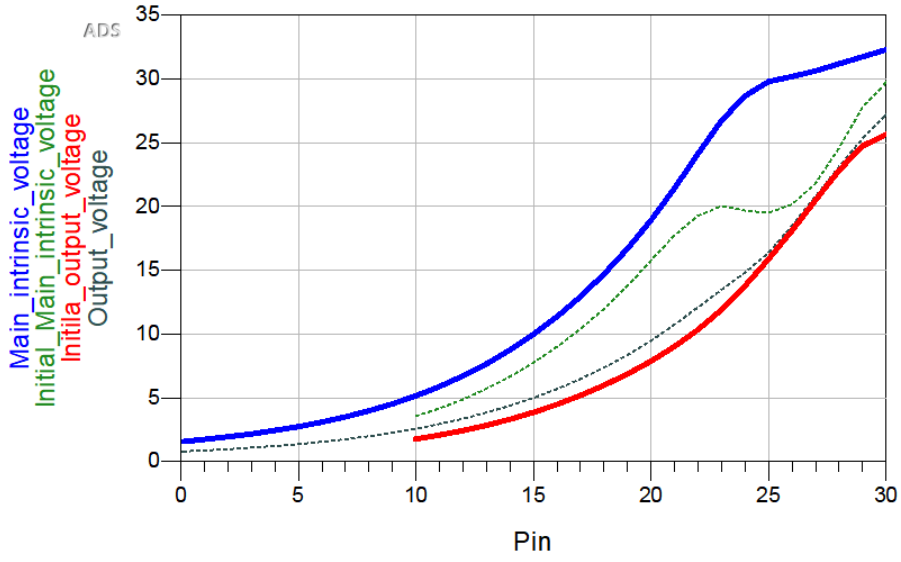


Fig. 3.4 Main and Aux intrinsic fundamental voltages before and after optimization

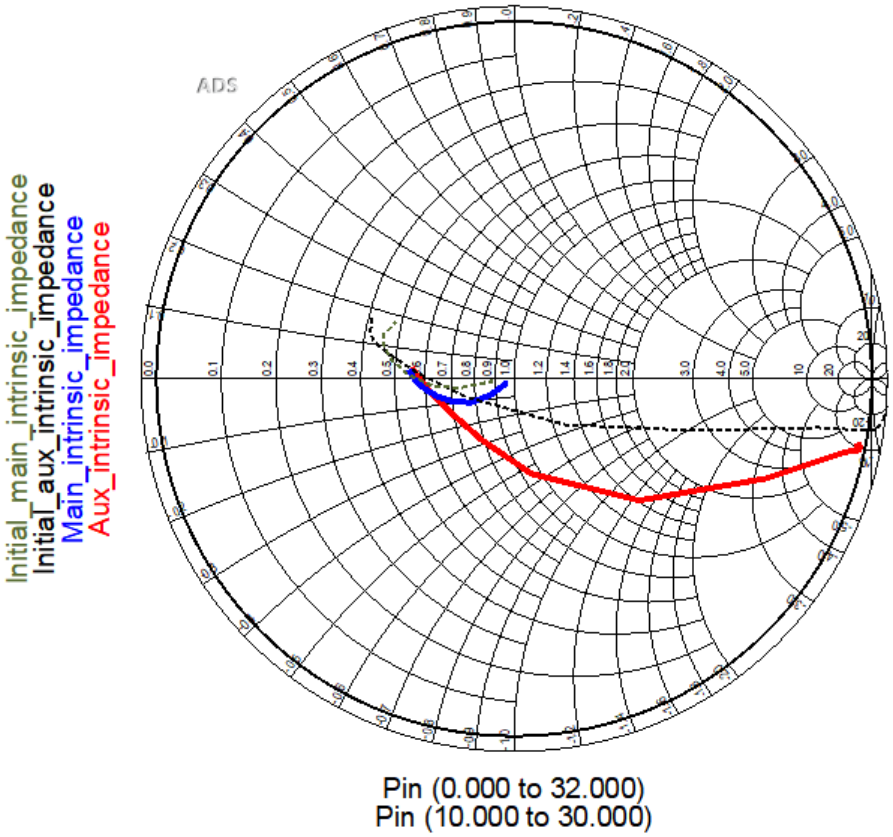


Fig. 3.5 Load modulation at intrinsic drain

The load modulation of the main ideally is from $Z_{main} = 2R_{opt}$ in low power region till R_{opt} in saturation while the Auxiliary from $Z_{aux} = \infty$ till R_{opt} in saturation .If there were no parasitics reactive elements in the output the drain impedances should be resistive see(fig1.13). In the first design the load modulation is incorrect and with the tunning of the parameters describer previously (tunning even of device parasitcs see later) a better modulation (more similiar to the ideal case) is achieved.

Dynamic load line modulation The parasitic tunning is done even to achieve a current dynamic load line modulation .To see the behaviour of current and voltage in the intrinsic drain of the devices is impossible physically but in simulations can be achieved .Adding the negate components of the drain parasitcs we have negated their effect so the current and voltage should be the same as the intrinsic drain .After that adding the another time the parasitcs we have reproduced the same behaviour of the device but also can obtain the intrinsic signal behaviour . The modulation should be that of the fig.3.7.

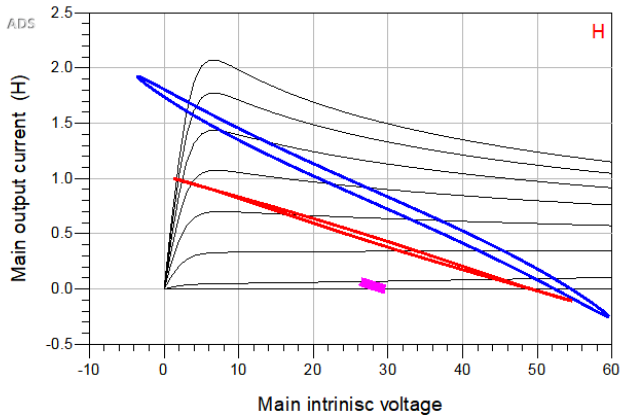


Fig. 3.6 Main dynamic load line modulation – back off and –saturations

For the main device in *Low Power* region shoul be approximately the modulation of a class deep AB ,the load line goes from $I_{ds} \approx 0$ till I_{ds}=1A.In the *Doherty region* the load line pendence is changed and goes from $I_{ds} = 0A$ till 2A.

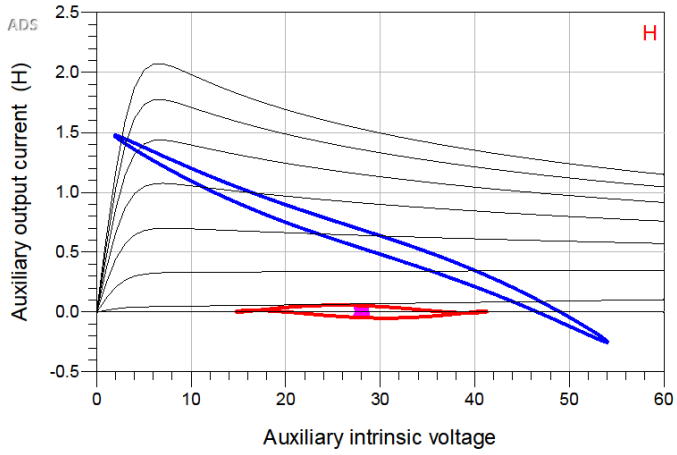


Fig. 3.7 Main dynamic load line modulation – back off and –saturations

Auxiliary in *Low Power region* is turned off while in saturation has the same load line of main device .

for both amplifiers in order to transfer the maximum power the intrinsic drain should see an resistive load at least at the 2 points ,back off and saturation .to have a resistive load means that the load line should be a straig pendent line with the pendence $\frac{1}{2R_{opt}}$ in back off and $\frac{1}{R_{opt}}$ in saturation.

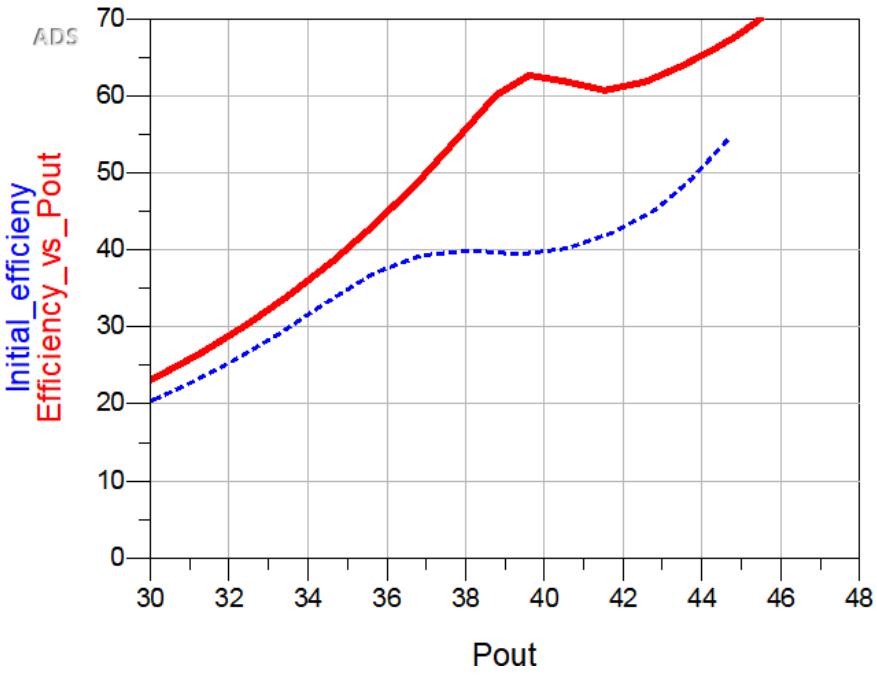


Fig. 3.8 Efficiency before and after optimization

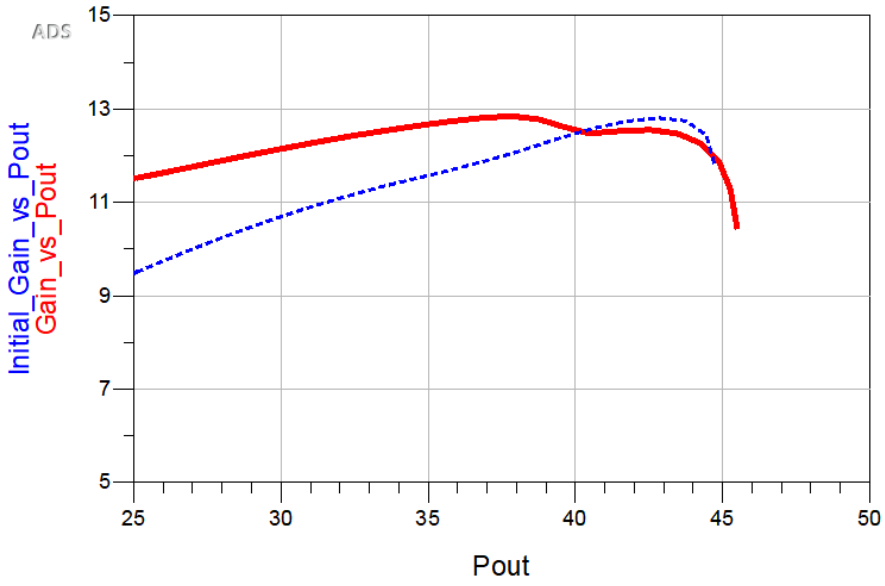
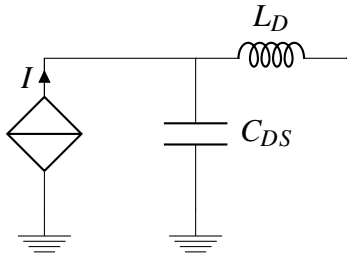


Fig. 3.9 Gain before and after optimization

3.2 Output matching

To understand better the behaviour of a Doherty with real physical device have to add some of parasitics that characterize a real HEMT device . In the previous current source device we can add the drain parasitics (section2.2). The small signal drain parasitics can be modelled with a low pass filter (section2.2) so a drain capacitance C_{DS} in parallel with the current source and a series inductance L_D (drain inductance)



Each current source node which is the intrinsic drain node should see an impedance equal to the optimal resistance R_{OPT} .Taking into account that the parasitics are always present the drain impedance is not any more resistive (not even equal to R_{opt}) to have the maximum power at the output . Matching circuit are added to cancel the effects of the reactive elements with also a reactive circuit which does not dissipate power and makes it possible that the power provided by the current source is transferred to the resistive load .

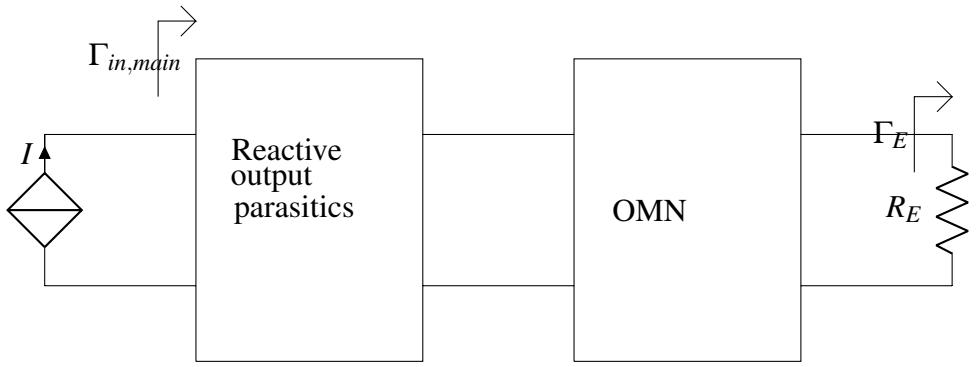
T

The goal is to negate this reactive elements in the band 3.2-3.8 GHz so we have to find a circuit that cancels the effect in the same quantity on the whole band , broad band matching network .

A single device without output matching will not transfer the maximum available power .The current and voltage will not be in phase and so will not achieve the maximum of the fundamental current and voltage at the same time at the intrinsic drain node .The gain and output power will be significantly reduced .What we need is a network (Output matching network OMN) that in series with the parasitics reactive elements will make possible that the intrinsic drain node sees the resistive load R_L transformed at $R_{opt}(R_{opt}/2)$.We want all the power transferred on the load so the OMN should be a reactive element network(reactive element don't dissipate power).

Usually when working with matching networks the S-parameters are used for the design.In the OMN case if from the drain intrinsic node a certain resistance R should be seen in terms of parameters the reflection coefficient (Γ or S_{11}) w.r.t R should be 0. where :

$$\Gamma = S_{11} = \frac{R - Z_{out}}{R + Z_{out}}$$



Resistance seen by the intrinsic node should be R_{opt}(or $2R_{opt}$ in back-off). After the simulation done in previous section the parasitics of the main and aux are different .Also in the first evaluation will neglect the resistive parasitics which are very small and can be neglected.

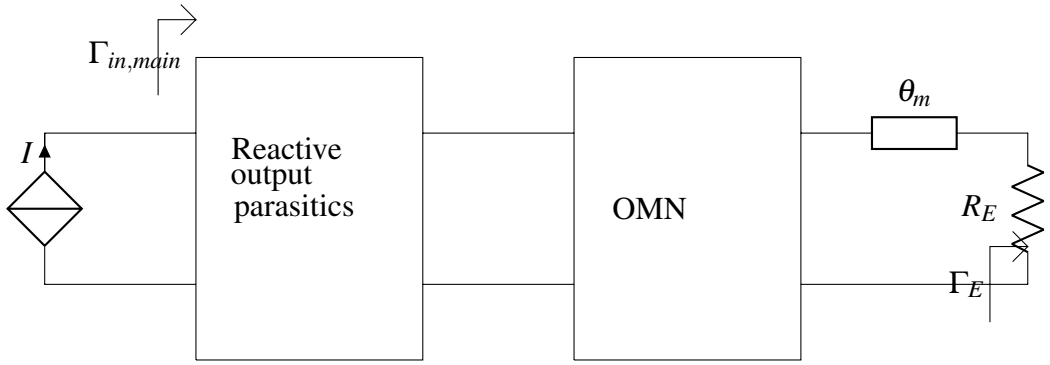
For the Auxiliary device the matching network should transfer the load resistance(modulated) into R_{opt} in saturation .

While for the main device another problem arises,the matching can be when the resistance of the load seen after Q.W.T is $2R_{opt}$ in back-off or R_{opt} in saturation to respectively the same resistance at the intrinsic drain node .To achieve the matching at both points an offset line should be added.

In the main device case we want a certain OMN that together with the parasitics can transform a resitance R_E into the wanted intrinsic resitance $Z_{in,main} = R_A$. But at the same time if R_E is changed by a factor α (αR_E) even the $Z_{in,main} = \alpha R_A$.The reflection coefficient at intrinsic node:

$$\Gamma_{in,main} = \frac{Z_{in,main} - R_A}{Z_{in,main} + R_A} = \frac{S_{11} - \Delta s \Gamma_E}{1 - S_{22}\Gamma_E}$$

Offset line



Considering the S matrix of the Reactive parasitics in cascade with OMN the input reflection can be calulcate as follows :

$$\Gamma_{in,main} = e^{j\angle S_{21}}\Gamma_E|_{R_{E,0}}$$

Where $\Gamma_E|_{R_{E,0}}$ is the reflection coefficient seen by the resistance and with impedance reference equal to $R_{E,0}$.So the reflection coefficient at drain is equal to the reflection coefficient at load with a difference of phase .So if $\Gamma_{in,main}$=0 even $\Gamma_E|_{R_{E,0}}$=0 and viceversa . But if $\Gamma_E|_{R_{E,0}}$ different from 0 when the load R_E is changed to a value $R_E = \alpha R_{E,0}$ the reflection coefficient is different from 0 but since there is the phase difference the input resistance seen by drain is not multiplicated by α.
To achieve the transformation with the same factor an offset line is needed with characteristic impedance $R_{E,0}$ [R. Quaglia and Ramella (????)].The new network formed by the three circuits in cascade (parasitics ,OMN ,offset line) we call it $\tilde{S}$ and the transmission coefficient phase now becomes :

$$\angle\tilde{S}_{12} = \angle S_{12} - \theta_M$$

where θ_M is the degree length of the offset line in centerband. The relation of the two reflection coefficients becomes :

$$\Gamma_{in,main} = e^{j\angle\tilde{S}_{21}}\Gamma_E|_{R_{E,0}} = e^{j\angle S_{21}-\theta_M}\Gamma_E|_{R_{E,0}}$$

If we set electrical lenght of the offset line equal to the phase of S_{21} plus n times π

$$\theta_M = \angle S_{21} + n\pi$$

the modulation of the resistance R_E will be reported with the same factor at the input .

$$\frac{Z_{in,main}}{R_A} = \frac{R_E}{R_{E,0}}$$

For the design of main OMN we consider as the resistance $R_{E,0}$ the resistance of the load transformed by the Q.W.T.Load resistance seen by main is either $R_{opt}/2$ or R_{opt} in saturation due to the modulation by Auxiliary . After the transformation by Q.W.T with characteristic impedance R_{opt} the resistance seen by the OMN is $2R_{opt}$ or R_{opt} respectively.In the center band frequency is not relevant having an offset line characteristic impedance $Z_{offset} = R_{opt}$ or $Z_{offset} = 2R_{opt}$ .What changes is the bandwidth of matching in back-off or in saturation depending in our choice os Z_{offset}.In other words if $Z_{offset} = 2R_{opt}$ the band will be wider in back off then in saturation where in saturation will be a impedance step of the load (R_{opt}) and the transmission line (Z_{offset}) while in back-off load and transmission line resistance is

equal so we obtain a larger bandwidth .The contrary happens if $Z_{offset} = R_{opt}$.
In conclusion ,if we want larger bandwidth in back-off characteristic impedance of offset line $Z_{offset} = 2R_{opt}$ otherwise if we design for larger bandwidth in saturation then $Z_{offset} = R_{opt}$.

Auxiliary offset line

Similiar considerations are done for the auxiliary offset line .The problem for the auxiliary rises when it is turned off.In this region the intrinsic drain of auxiliary behaves as open an without an offset line the open is not correctly reproduces in output .So the main sees a load resistance in parallel with reactive elements of auxiliary (parasitics and aux OMN).

$$\Gamma_{OUT,P|\Gamma G=1} = e^{j2(\angle S_{12}^{(P)} - \theta_P)}$$

where $\Gamma_{OUT,P|\Gamma G=1}$ is the output reflection coefficient of auxiliary when the intrinsic drain is an open .we can obtain $\Gamma_{OUT,P}$=1 if we add a transmission line at the output of auxiliary with characteristic impedance $Z_{P,offset} = R_{opt}$ and electrical length :

$$\theta_p = \angle S_{12}^{(P)} + n\pi$$

Auxiliary OMN

The matching circuits OMN for the auxiliary should transform the modulated load resistance R_{opt} to the same value at the intrinsic drain .Aux OMN is designed only to match in saturation because it is turned off in the Low Power region .

Main OMN

In difference from Aux OMN the main matching network can be designed in different ways . As demonstrated previously for the offset line and even OMN can be designed to obtain the maximum bandwidth in back-off saturation or an intermediate point .This choice depends on the specifics that the designer has planned .

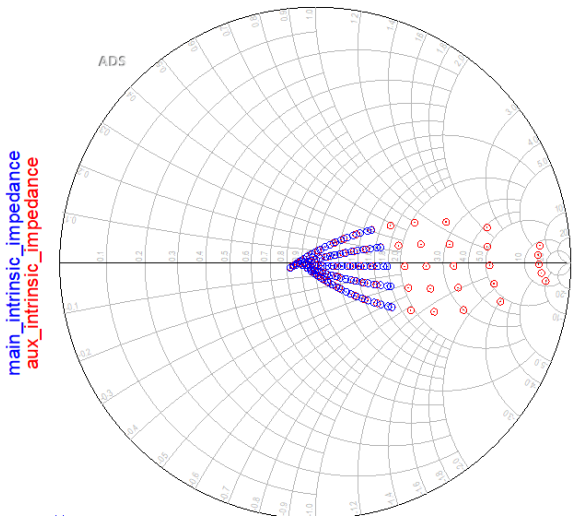


Fig. 3.10 Output matching optimized in saturation

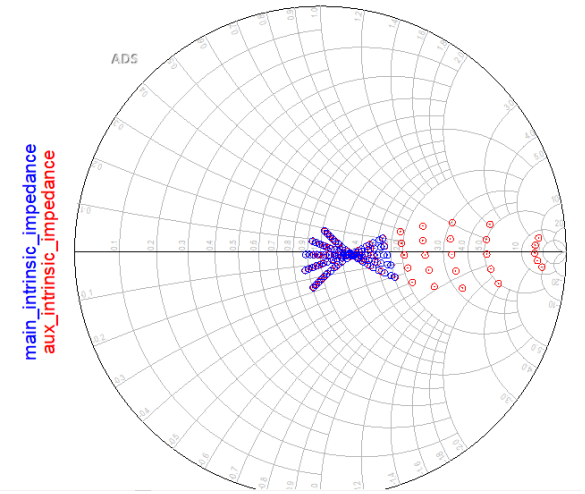
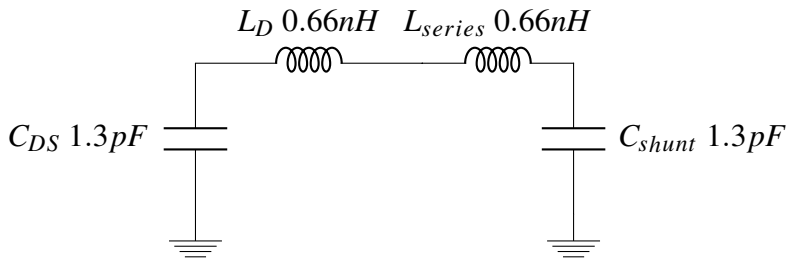


Fig. 3.11 Output matching optimized in back off

OMN Design solution The goal of the matching network in a power amplifier design is not only to obtain the optimum load at the intrinsic point at center frequency but also to obtain larger bandwidth possible. There is a formula to according to which we can get the best solution for the optimum network in order to obtain maximum flat and the lowest reflection coefficient in the design frequency band given by Doherty (1936).The design will be explained in detalis in section **??** .This circuit will be the reference point for OMN design bandwidth.

OMN embedded parasitics My design of the output matching network uses the output parasitics of the devices (aux and main) to implement a quarter wave transmission line . In lumped element a quarter wave transformer can be implemented as a π-network of 2 shunt capacitors and a series inductance .(see figure)



A Q.W.T in lumped element is implemented if the impedance of the capacitance and inductance are equal in the center frequency.In order to obtain this behaviour it is needed to add an inductance in series to the parasitic inductance $\frac{1}{\omega C_{DS}} = \omega(L_D + L_{series})$

The characteristic impedance of Q.W.T is equal to absolute impedance value of each of lumped elements $Z_\infty = \frac{1}{\omega C} = \omega L$ .In this project the center frequency is $f_0 = 3.5GHz$,$C_{DS} =$

$1.3pF$,$L_D = 0.66nH$ for main device.

$$Z_\infty = \frac{1}{2\pi f_0 C_{DS}} = \frac{1}{2 * \pi * 3.5GHz * 1.3pF} \approx 34.98\Omega$$

The matching network has to transform the resistance R_{opt} to $2R_{opt}$ and $\angle\tilde{S}_{21} = n\pi$.The final load in which the power will be transferred is usually the load that models the antenna with value 50Ω.

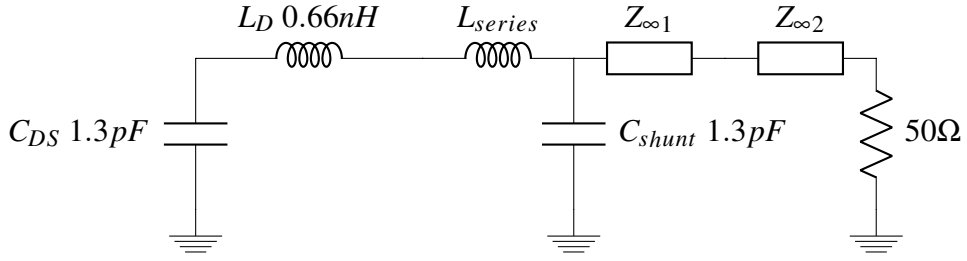
It is needed to make the transformation from 50Ω to 50Ω and while a Q.W.T of 34.98Ω is already present ,at the same time having a inverting network so $\angle\tilde{S}_{21} = n\pi$ a minimum of 3 Q.W.T including the embedded transformer.Now the resistance should be transformed from 50Ω to $\frac{Z_\infty^2}{50}$=24.47Ω with two quarter wave transformers.

An optimum dual frequency transformer for broader band can be obtained according to paper [Monzon (2003)]. The values of the 2 transmission line impedance are :

$$Z_1 = \sqrt{\frac{Z_0}{2\alpha}(R_L - Z_0) + \sqrt{[\frac{Z_0}{2\alpha}(R_L - Z_0)]^2 + Z_0^3 R_L}}$$

$$Z_2 = \frac{Z_0 R_L}{Z_1}$$

Where $Z_0 = Z_{in}$=24.47Ω ,R$_L = 50\Omega$,$\alpha = (\tan(\beta_1 l_1))^2$,$\beta_1 l_1$ electrical length of the first Q.W.T .



The final goal is to design the matching networks in distributed elements.So we have to transform the lumped elements to transmission line.The shunt capacitance can is equivalent at certain frequency to a stub transmission line connected in open.The stub impedance at center frequency is :

$$Z = -jZ_0 \cot(\beta l) = \frac{1}{j\omega C_{shunt}}$$

In the formula there are two degrees of formula :electrical length and characteristic impedance.I choose electrical length βl=30° in order that this stub will become short for the third harmonic.

On the other hand the series inductance (with a relatively small value) can me modelled with a series transmission line that at the same time serves as a connection line for the device (later on the layout).With some tunning of these 2 parameters and optimization can arrive at the same matching as lumped element OMN.

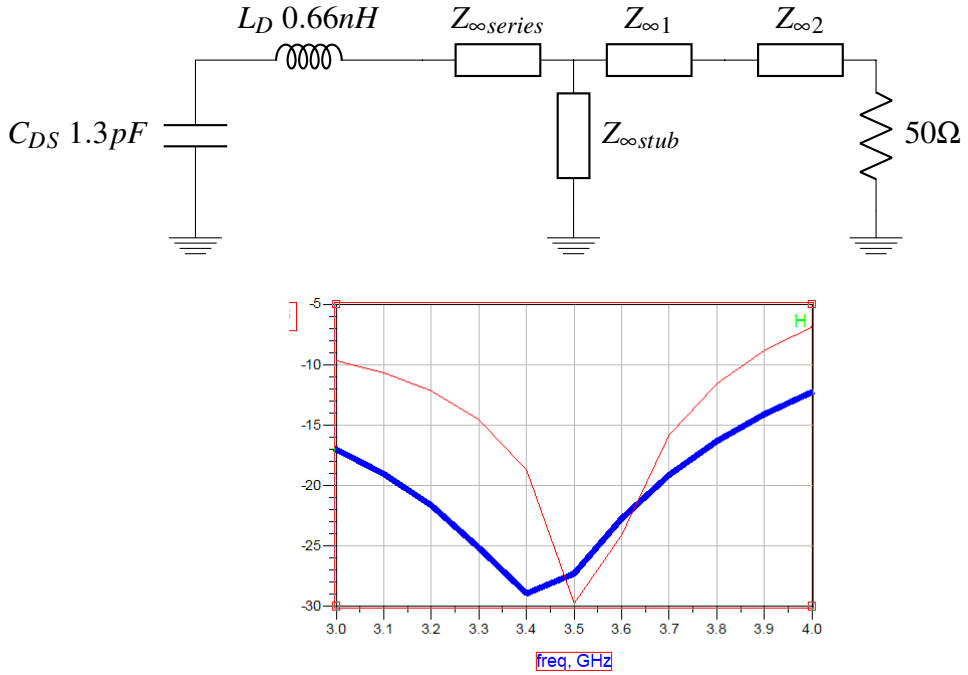


Fig. 3.12 OMN reflection coefficient in back off and saturation

Auxiliary OMN The idea of Auxiliary Output matching network is the same as that of the main OMN but with the difference that here we need an odd number of transformers because it should not be a inverting circuits (when aux is off the open in intrinisc drain is transformed in open at the ouput). So except for the first transformer we have t add another Q.W.T to match the saturation load impedance seen by aux (100Ω) to the optimal resistance (25Ω) the circuit in distributed element is:

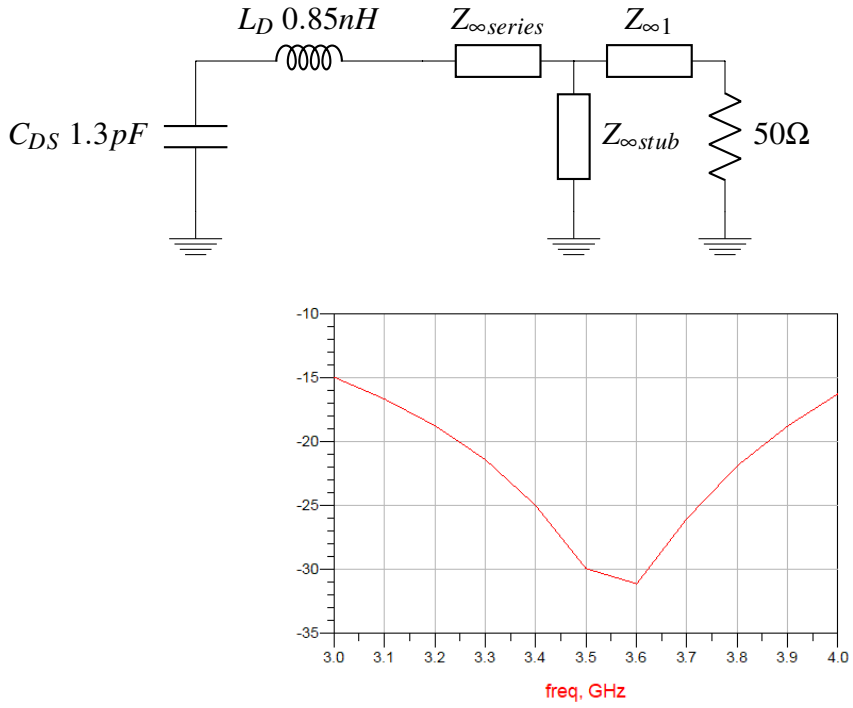


Fig. 3.13 Aux OMN reflection coefficient in saturation

3.3 Stabilization network

Before considering the Input matching network we have to stabilize the circuit which will effect even the optimal IMN.

Stability is an important issue for the design of PA [M.Pirola (2017)]. We want a stable non oscilating device not only for the band frequency but also out of band (especially in low frequency where the amplifiers has more instability problems).
A two-port loaded with generator and load impedances with positive real part is unconditionally stable if (1) the input impedance has positive real part for any value of the load impedance and (2) the output impedance has positive real part for any value of the generator impedance.Or expressed in terms of reflection coefficient we have that for any value of Γ_L (with $|\Gamma_L| < 1$) we have $|\Gamma_i n| < 1$, and for any value of Γ_G (with $\Gamma_G < 1$) we have $|\Gamma_{OUT}| < 1$.
Or on the other hand the circuit is conditionally stable if exists any load or input impedance such that the reflection coefficients $|\Gamma_{in}|$ or $|\Gamma_{OUT}|$ are greater than 1. $|\Gamma_i n| > 1$ does not automatically imply that the circuit will oscillate, since the oscillation condition is in fact $\Gamma_i n \Gamma_G = 1$.This later condition implies that the total loop resistance is zero so we will have an infinite gain (oscillations).
Making the analysis of the reflections coefficients with different terminations using the S-parameters of the device the formula (parameters) that imply unconditional stability can be generated [M.Pirola (2017)]

Two port stability criteria

1.Linville or stability coefficient K:

$$K = \frac{1 - |S_{22}|^2 - |S_{11}|^2 + |\Delta s|^2}{2|S_{21}S_{12}|} > 1$$

2.determinant of the S-parameter matrix

$$\Delta s < 1$$

Both conditions should be simultaneously satisfied in order to have an unconditionally stable amplifier.Since the S-parameter are frequency depended ,so are even the two stability criteria, K and Δs,we have to ensure stability not just in band but also for other frequency especially in low frequency where the amplifiers usually have more problems and have a high gain,while in very high frequency (ex.f>20GHz)the gain is significantly reduced.
Another important parameter for the amplifier is MSG(maximum stable gain) that is defined only for the frequencies where the amplifier is stable and has no significance for other

frequencies :

$$MSG = \frac{|S_{21}|}{|S_{12}|}$$

is the maximum gain that the device can achieve with the correct optimum terminations .Since we are designing a PA the Gain maximum gain is not the main goal but even MSG gives a valuation of the gain reduction when the amplifier will be stabilized .
There are different ways to stabilize a device adding dissipating elements(resistances) in series ,parallel input or output and feedback

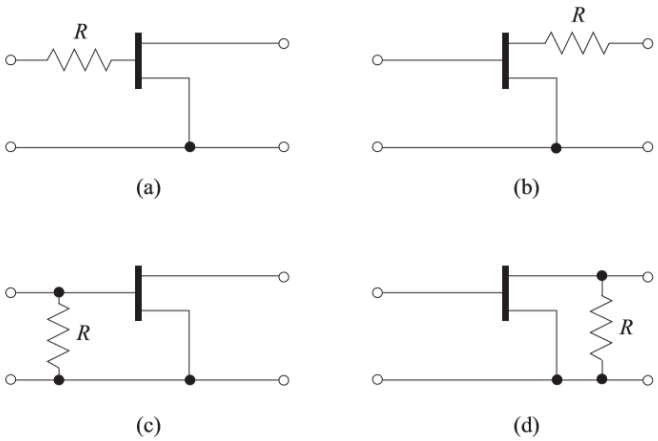


Fig. 3.14 Resistive stabilization

Since the problems are especially in low frequency i used the series gate resistance in parallel with a capacitance .In this way the resistance will have its effect in low frequency but will be a short circuit in high frequency .I added also the parallel resistance (fig 3.10 c)) that should have a inductance in series but can use even a 90◦ degree transmission line, connected with the bias voltage source ,that in band behaves as an open. (will see later).
This dissipative elements will clearly even reduce the gain that can be noticed by the MSG reduction(see)
The simulations are done for the single device in Class A(AB) where the amplifier is turned on and the small signal simulation can be done .the worst case was in fact in deep Class B so i designed the stabilization network with this gate bias voltage and used the same stabilization network then even for the auxiliary device (deep class C)

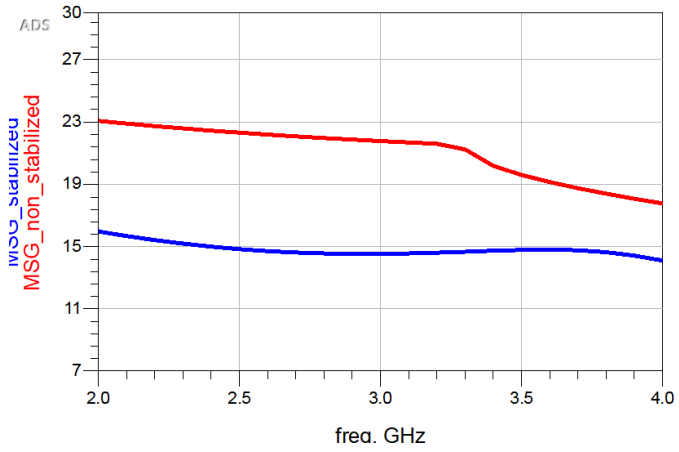


Fig. 3.15 MSG before and after stabilization

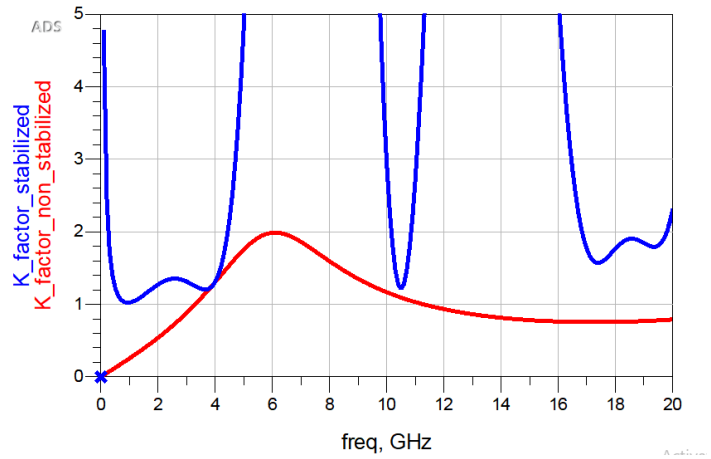


Fig. 3.16 K factor before and after stabilization

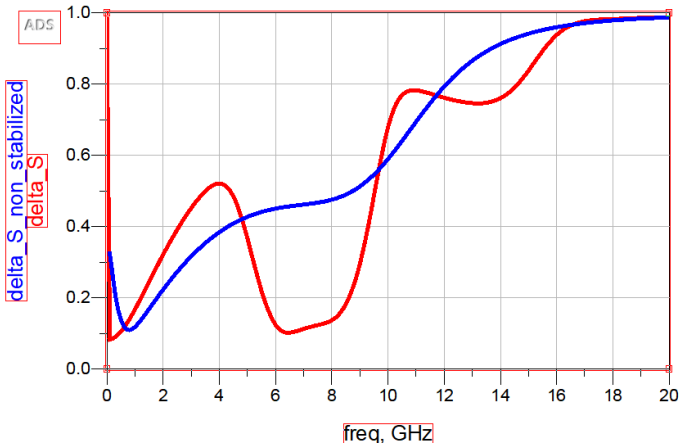


Fig. 3.17 Δ s

3.4 Load pull measurements

To obtain the optimum source impedance for input matching the load pull measurements should be done.The optimum input impedance is the same for maximum power transfer and maximum gain .
Load(source) pull measurements are simulations in which the load(source) loads are swept in different values and the behaviour of gain,PAE and maximum output power is obtained.
In ADS a design guide for Load Pull measurements is already presents . I choose to simulate Load Pull measurements in order to study at the same time PAE and maximum output power P_{OUT} and to find a trade off between the two important parameters for a PA.
In the Load Pull measurements of the ADS design guide it gives even the optimum source load for maximum gain (P_{OUT}).
Separately are simulated the Main and Auxiliary device with their different gate bias points.Together with the device even the stabilization network is already present together with a small transmission line that is needed in series with device to connect it physically with the lumped stabilization network In the design guide graph in ADS i have chosen the point that gives P_{OUT} nearly the maximum power that device can deliver but at the same time to maintain higher PAE possible and lower possible Gain compression. The optimum input source impedance for the Main is :

$$Z_{in,main,opt} = 4.5 - j13\Omega$$

And the optimum input source impedance for the Auxiliary is :

$$Z_{in,aux,opt} = 4.5 - j10\Omega$$

Then later i added in the Doherty design simulation the source resistance that i found above and a series inductance of negative value which impedance at center frequency is equal to imaginary part of the optimum source impedance. After simulations of the Doherty to obtain the desired parameters (P_{OUT} ,Gain,Efficiency) the values of the source resistance and negative inductance (that represents the imaginary part) i found the values below :

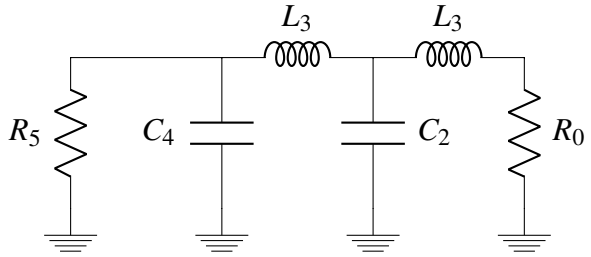
$$R_{in,main,opt} = 4.7472\Omega \quad L_{in,main,opt} = -0.496nH$$

$$R_{in,aux,opt} = 3.5\Omega \quad L_{in,aux,opt} = -0.368nH$$

3.5 Input Matching Network

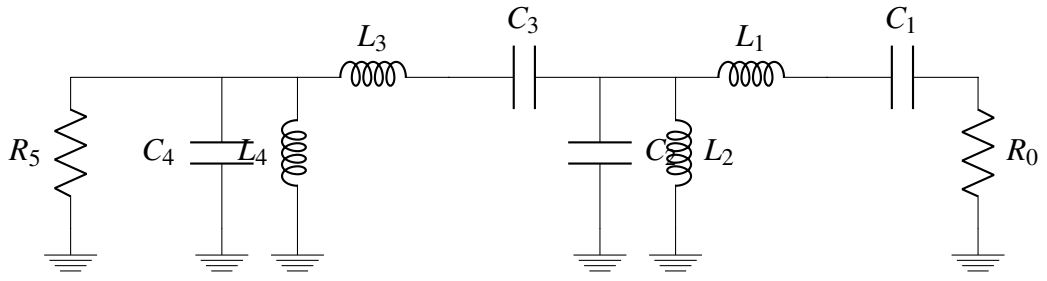
In input source resistance is $R_G = 50\Omega$ so we have to design a reactive matching network which transform the 50Ω impedance into the optimum input impedance found in section 3.4. We have to match an inductance in series with small resistance to 50Ω input source impedance The matching network which gives the minimum reflection coefficient and the most flat response in the band is given in analytical form in the paper [Dawson (2009)]. This kind of matching circuit designed in lumped elements can be of different orders (n=1,2,3,4..) that depends on the number of reactive elements used.Increasing the circuit order its performance in terms of bandwidth increases.In this circuit case i have simulated order 3,4 and 5.Since from the order 3 to 4 there is a significant improvement and after order 4 the improvement is not any more noticable in 3.2-3.8GHz band i chose to designed a 4 order input matching network .

The initial design given by the paper includes a capacitance in series to the resistance and not an inductor but i will explain later how i made the transformations.



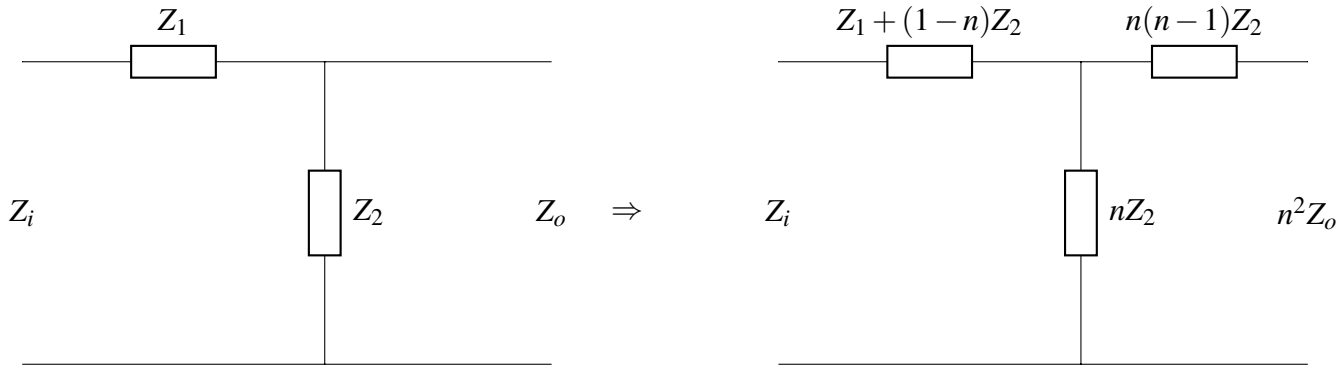
This is a low pass circuit and to transform it in the series inductances are replaced by L-C series resonant circuit and the shunt capactinaces replace by resonant parallel L-C circuit.The lowpass network is formed into a bandpass network by resonating each series or shunt element at the geometric mean frequency $2\sqrt{\pi f_1 f_2}$,where f_1 is the lower band frequency $f_1 = 3.2GHz$ and f_2 the upper band frequency $f_2 = 3.8GHz$

Optimum matching circuit



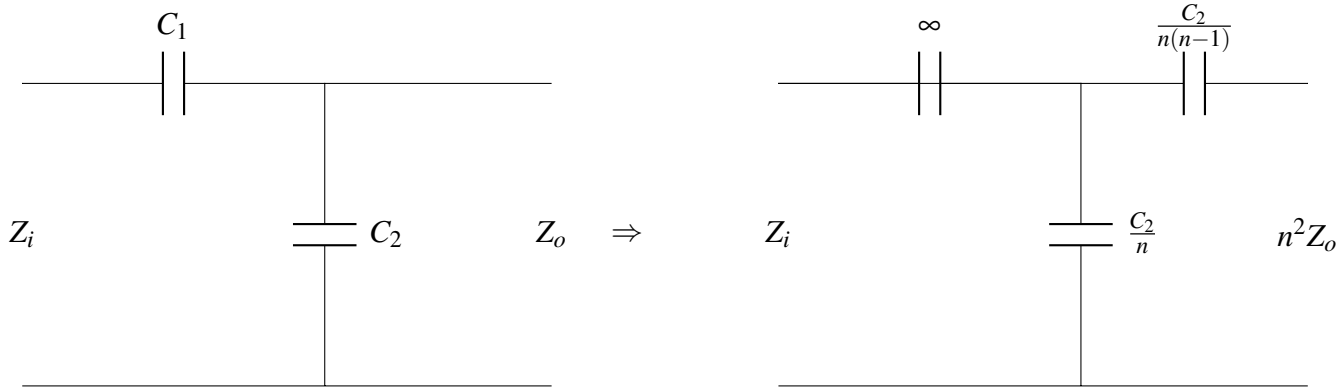
R_0+jL_1 is the conjugate optimal input source impedance that we have to transform at 50Ω. this circuits has a capacitance in series to L_1 which should be short circuited because we have to connect to gate even the bias voltage in short circuited in DC. Even the resistance R_5 is

not equal to 50Ω so some changes should be made.
To transform the capacitance C_1 in a short circuit the Norton transformation should be used.

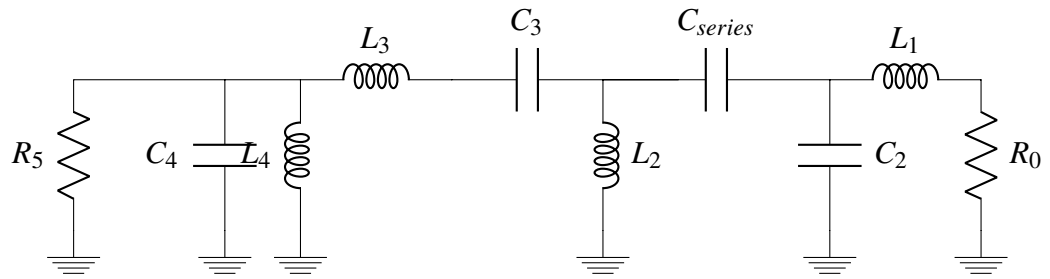


Norton transformation does not effect the bandwidth or Q of the matching network.With this kind of transformation the all the impedances that are found on the right of Z_2 are multiplied by factor n^2 and so this gives another advantage of increasing the value of R_5 towards 50Ω. To make the transformation of the capacitance C_1 to become an short circuit we have to find a valued n such that $C_1 = \infty$.The ciruit part that can make this transformation possible is the capacitance C_1 connected with capacitance C_2 where in this case the impedance Z_1 of the Norton transformation circuit is $Z_1 = \frac{1}{j\omega C_1}$ and $Z_2 = \frac{1}{j\omega C_2}$.
We have to find the value that

$$Z_1+(1-n)Z_2 = \frac{1}{j\omega C_1}+(1-n)\frac{1}{j\omega C_2} = 0 \;\; n = 1.4847$$



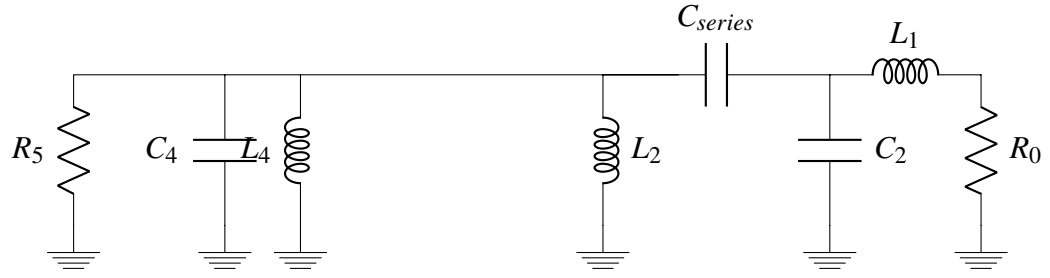
The capacitance C_1 now is short circuited and we have added another capacitance of value $\frac{C_2}{n(n-1)}$ in series with the circuit which will serve even as a DC block for the DC current of bias. The optimum circuit is now transformed as follows (see next page ..)



- $L_{1,main} = 0.496nH$ $C_{series,main} = 2.282pF$ $L_{2,main} = 2.25nH$ $C_{2,main} = 1.381pF$ $L_{3,main} = 0.1nH$ $C_{3,main} = 20pF$ $L_{4,main} = 1.67nH$ $C_{4,main} = 2.91pF$ $R_{5,main} = 10.5\Omega$

- $L_{1,aux} = 0.368nH$ $C_{series,aux} = 3.8pF$ $L_{2,aux} = 1.67nH$ $C_{2,aux} = 1.85pF$ $L_{3,aux} = 0.072nH$ $C_{3,aux} = 27.5pF$ $L_{4,aux} = 0.714nH$ $C_{4,aux} = 2.9pF$ $R_{5,aux} = 7.3\Omega$

We could use still Norton transformations to increase the values of R_5 till source impedance but this would complicate a lot the circuit especially the distributed one in which the lumped will be transformed .So i used the dual impedance transformer(cit.L. Cótimos Nunes (????)) to match R_5 o 50Ω with 2 Q.W.T (Z_1 and Z_2)and the bandwidth is not significantly changed.
$Z_{1,}main = 19.43972\Omega$ $Z_{2,}main = 25.91408\Omega$
$Z_{1,}aux = 12.608\Omega$ $Z_{2,}aux = 31.1806\Omega$
The lumped circuit should be transformed into distributed but before lets make some simplifications.The series L_3 C_3 has a very small value in center frequency (even in band) and if we replace it with short circuit no significant change can be noticed .



Another thing that we have to take care is that a transmission line connected in short circuited is needed for the bias voltage .An inductor or a parallel resonator can be modelled by a short circuit but should not have a DC block in its path from DC voltage to gate of the device .In these case we have to change the C_{series} placement and add a inductor in parallel to C_2 then

after some tunning we can obtain similar bandwidth.The final circuit is lumped form is:

Final lumped circuit

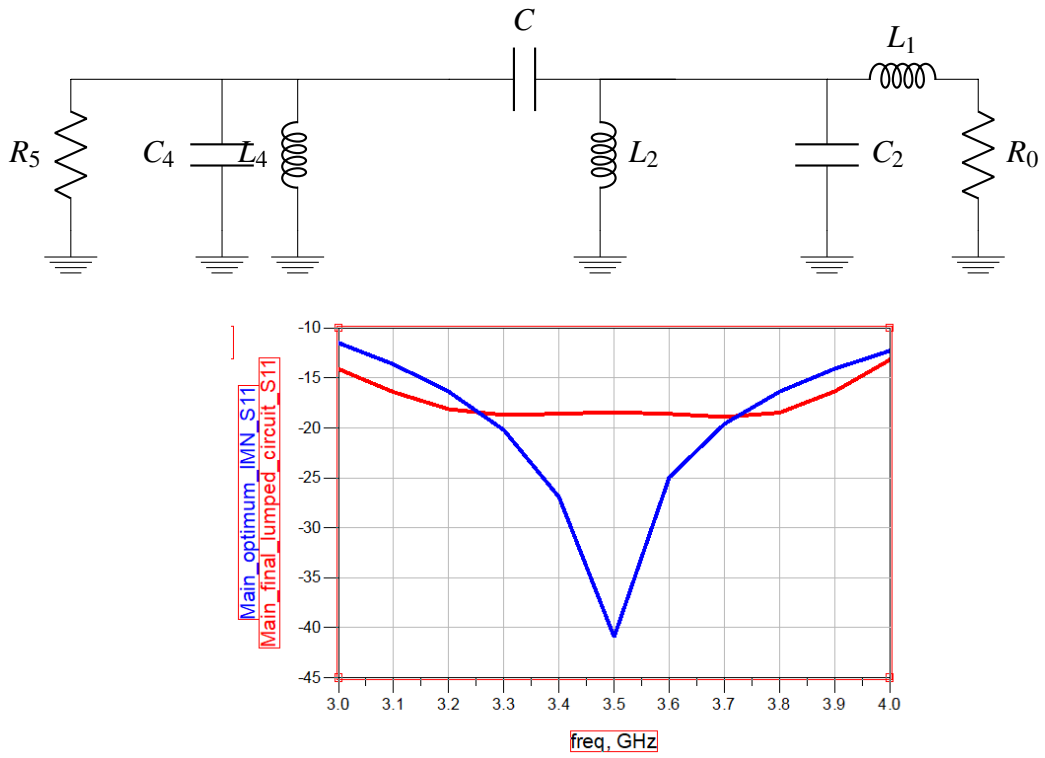


Fig. 3.18 Main optimal IMN vs Final lumped IMN

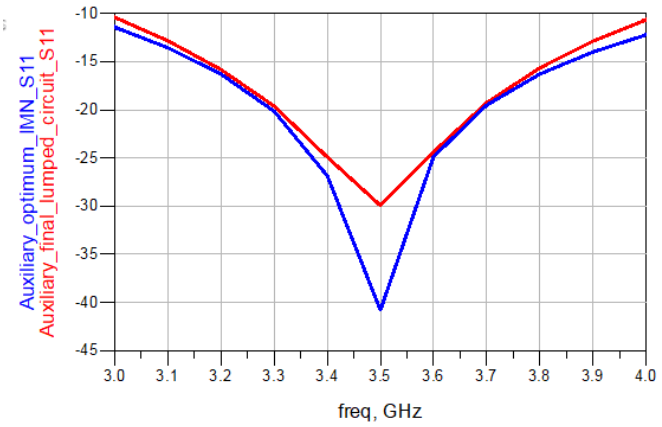


Fig. 3.19 Auxiliary optimal IMN vs Final lumped IMN

Distributed IMN

The two parallel resonating circuits can be transformed in a 90° degree (in resonating frequency) transmission line connected in short circuited.

$$Z_0 = \frac{\pi}{4}\omega L$$

The transmission line impedance is inversely proportional to the line width .Since we don't want very large transmission lines which radiate electromagnetic wave have to control the design previously.In this design the resonating frequency is low for the (L_2-C_2 resonating frequency of both main and aux) and ($C_4 - L_4$ main).To increase the resonating frequency i divide the capacitance into 2 parallel capacitances.

$$example \qquad C_4^{'}//C_4^{''} = C_4 \quad C_4^{'} < C_4 \Rightarrow \quad \omega_{01} = \frac{1}{\sqrt{L_4 C_4}} < \omega_{01}^{'} = \frac{1}{\sqrt{L_4 C_4^{'}}}$$

So now we have a transmission line with higher impedance and also a capacitance (ex.$C_4^{''}$) in parallel that can be modelled with an open stub transmission line .

The series resistance will not be transformed in distributed elements but will be designed in lumped one because at the same time serves as the DC block of the bias current towards input source generator.Now the final circuit of main and aux IMN become

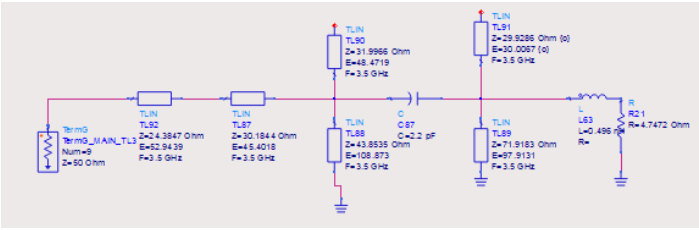


Fig. 3.20 Main distributed IMN

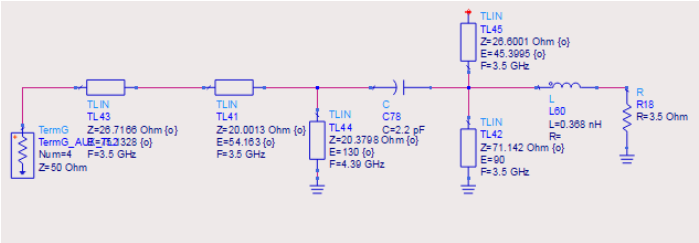


Fig. 3.21 Auxiliary distributed IMN

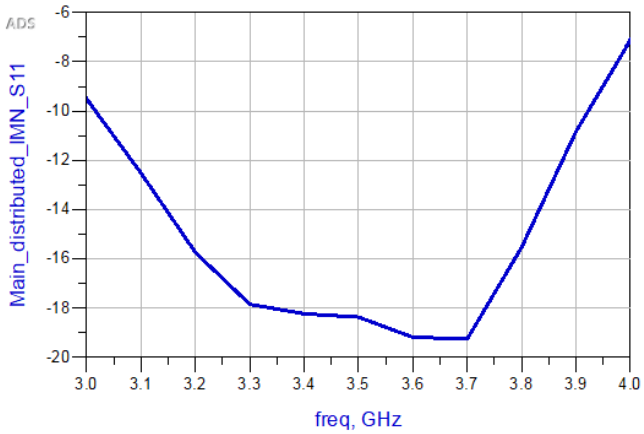


Fig. 3.22 Main IMN Reflection coefficient

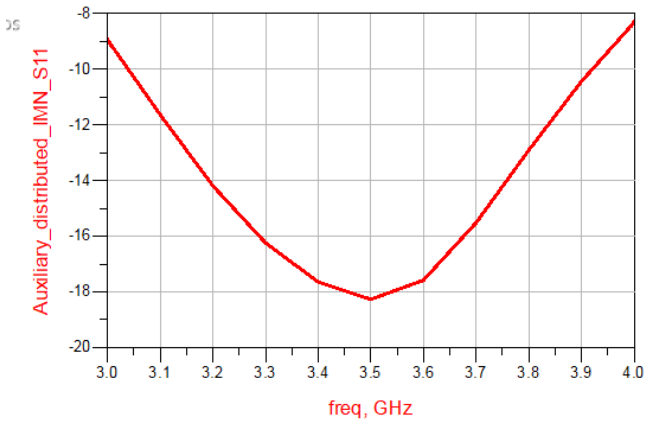


Fig. 3.23 Aux IMN Reflection coefficient

3.6 Doherty implemented with trnasmission line matching

After design of matching networks ,stabilizing circuits and the bias points have to complete the design by making the connection of the DC bias voltage to the gate and drain of the devices.

The circuit that connects the bias voltage should behave as a short in DC and should become an open circuit in band (central frequency).For the gate bias we already have designed the short circuited 90° stub that is part of the IMN .Instead of ground we can add the DC voltage in parallel with capacitances which are short circuited in band so that RF currents does not effect the DC voltage source.

For the output we add a 90° transmission line that since it behaves as open in central frequency but at the same time will short circuited the second harmonic generated by the drain current. The class AB and C as we have mentioned in chapter 1.Also the 90° transmission line stub

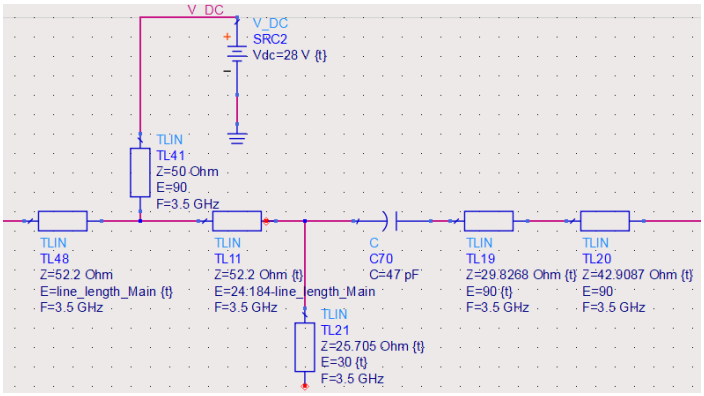


Fig. 3.24 Output OMN circuit

in open will short circuit the 3^{rd} harmonic.The first 2 harmonics are even the more important since the amplitude after the 3^{rd} harmonic are significantly reduced.

A capacitance should be added after the bias transmission line in series of OMN so it serves as DC block at the output.A 47pF capacitance changes slightly the output matching which can be further optimized .

After the implementation of all Doherty circuit it should be further optimized and we should study different variables and parameters.One of the most important for the Doherty as we have mentioned is the correct load modulation.After adding the OMN to study the load modulation we should be able to see at the intrinsic drain of the devices which is possible if we add the negate parasitics and in cascade the parasitics.

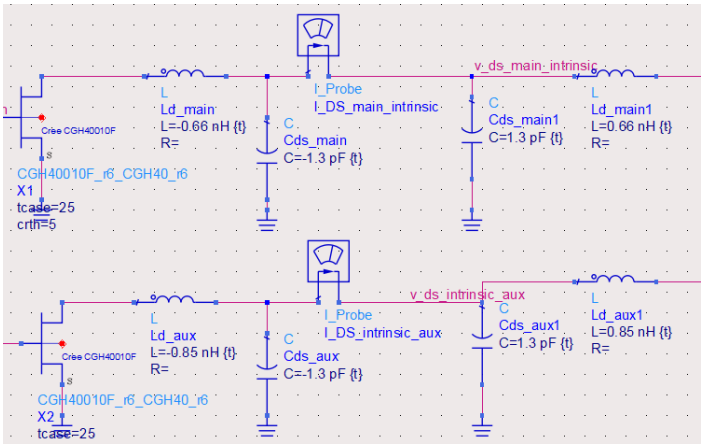


Fig. 3.25 Negate parasitics cascade with parasitcs

Optimization for correct load modulation changing slightly the stubs in input and output matching network .Tunning of the phase difference and power difference of the two separate input ports to obtain maximum efficiency and a trade off with gain compression.

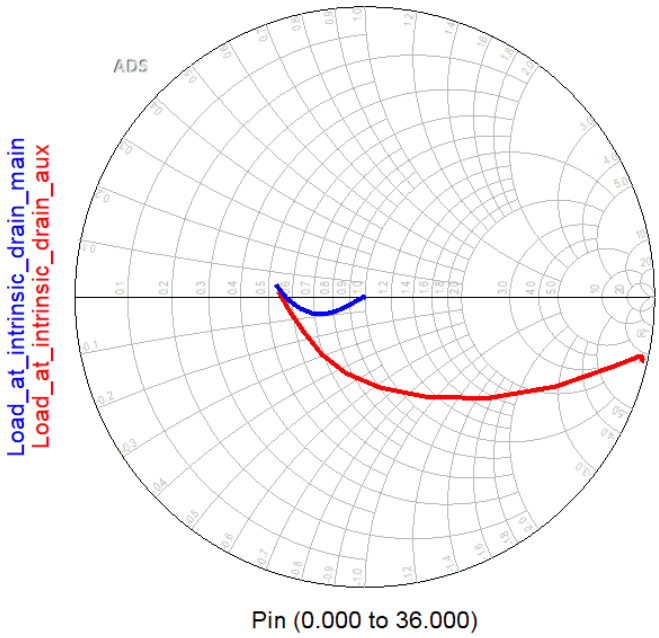


Fig. 3.26 Load modulation at center frequency 3.5GHz of the TL circuit

Efficiency in center frequency can be considered high for a real Doherty with

$$\eta_{Back,off} \approx 64\% \qquad and \qquad \eta_{Sat} \approx 71\%$$

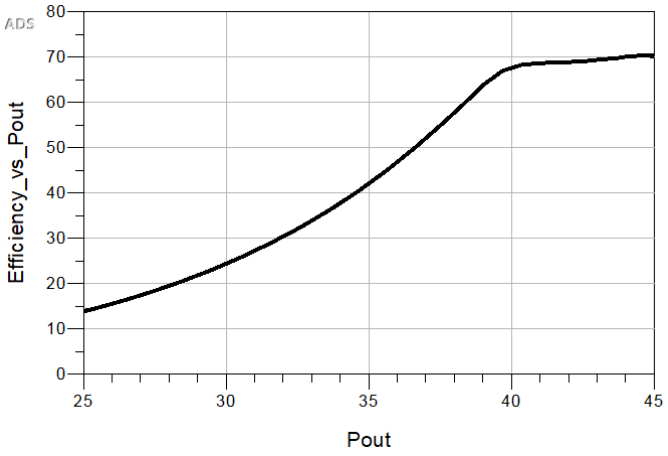


Fig. 3.27 Efficiency at center frequency 3.5GHz of the TL circuit

Gain

The Gain at low power region is almost 12dB and in Doherty region the gain is certainly reduces since Aux is biased in Class C.There is always a trade off between gain compression and efficiency at back off and are inversely proportional.

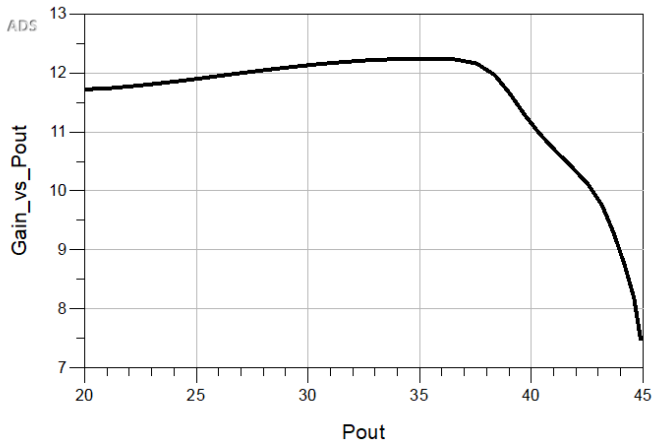


Fig. 3.28 Gain vs P_{out} at center frequency 3.5GHz of the TL circuit

Maximum output power

The maximum power goes from minimum of 43.7dBm till maximum in center frequency of 44.9dBm that is almost the maximum power that the two devices can deliver according to datasheet of the producer.

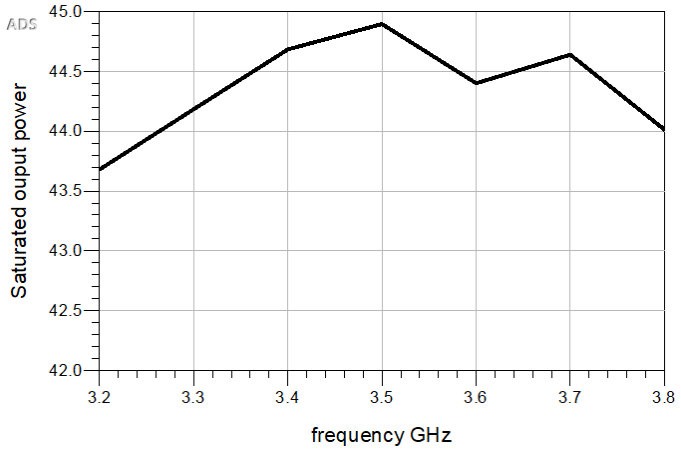


Fig. 3.29 Maximum power Vs frequency

Chapter 4

Implementation and Evaluation

4.1 Microstrip design

The circuit will be implemented in hybrid technology in FR-4 PCB.The devices and lumped elements are externally mounted in PCB .We have to transform the transmission lines into real metal lines .The microstrip single layer PCB is made up by a metal ground layer that covers one face of PCB and metal lines which length is proportional to electric length of transmission line and the width is inversely proportional to the characteristic impedance .
The linear permittivity of FR4 substrate is

$$\varepsilon_r \approx 4.6$$

Height of substrate *h=0.76mm*
Metal thickness *t=0.035mm*

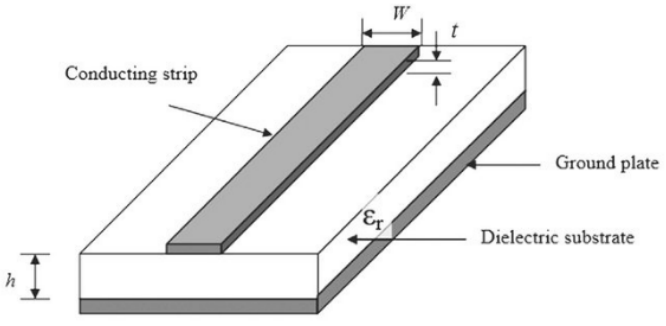


Fig. 4.1 Single layer microstrip

In difference from ideal lines the real microstrip is not completely lossless and cannot be considered a s fully reactive element.Two major source of losses are 1)conductor loss and 2)dielectric loss

1) Conductor losses are present because the metal conductors have a finite value of conductivity and also at high frequencies because of the skip effect the metal resistance becomes complex.This kind of loss is modelled by a distributed series resistance.

$$Z_S = R_S + jX_S = (1+j)\frac{1}{\delta\sigma} \qquad where \quad \delta = \sqrt{\frac{1}{\delta\omega}}$$

1) Dielectric losses are caused by the lossy dielectric which electric permittivity is not real but has even a complex part

$$\varepsilon_{rc} = \varepsilon_r - j\varepsilon_2 = \varepsilon_r(1j - tan\delta)$$

And this loss can be modelled with a distributed parallel conductance

$$G \propto \omega tan\delta$$

The behaviour of losses versus frequency is given in the following figure

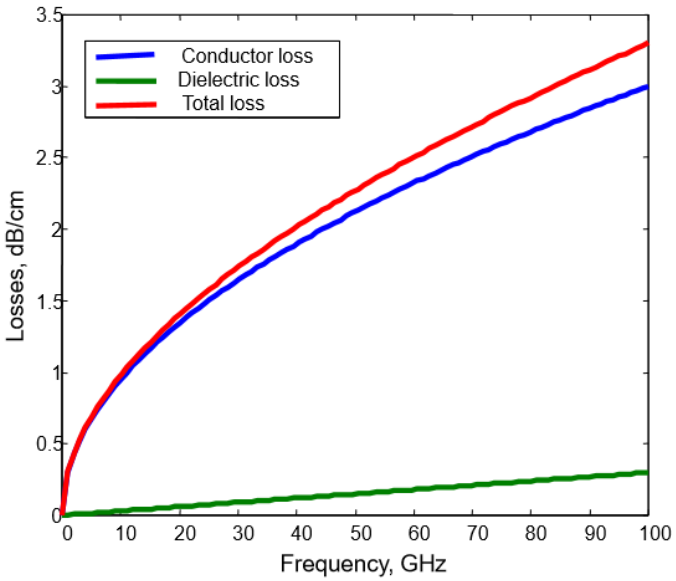


Fig. 4.2 Conductance ,dielectric and total losses vs frequency

To calculate the width and length of microstrip line in order to behave as the ideal transmission line approximation formulas exist .But since the ADS has a microstrip tool to calculate more accurately we will not use these formulas .
Before the design even of ideal lines at least the trend of width and length should be present .Very large width means high losses and will change the behaviour since will be a greater electromagnetic radiation.As i mentioned in IMN i have taken care to choose (and change) the matching networks where the lines would become very wide .For an ides of this behaviour see fig4.3

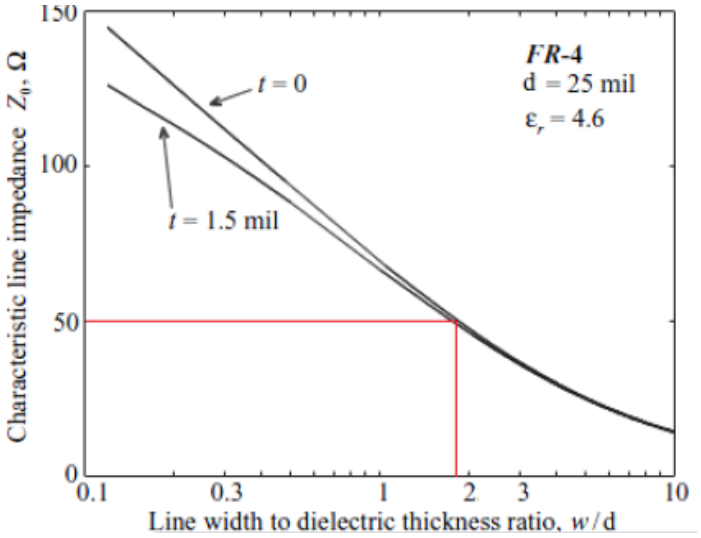
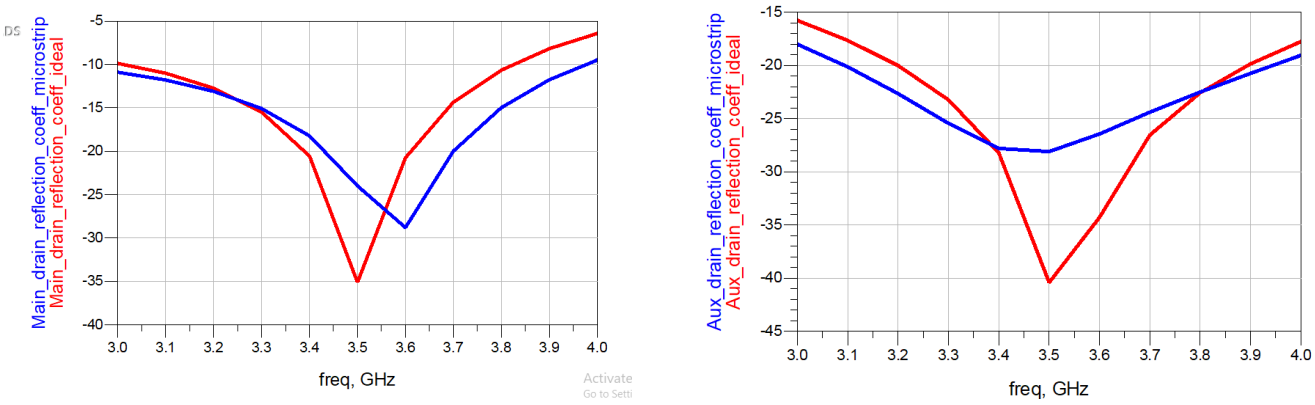


Fig. 4.3 Impedance Vs w/h(width/height) ratio

I have avoided lines with impedance more than 75Ω and less 20Ω .Very narrow lines have higher series losses.

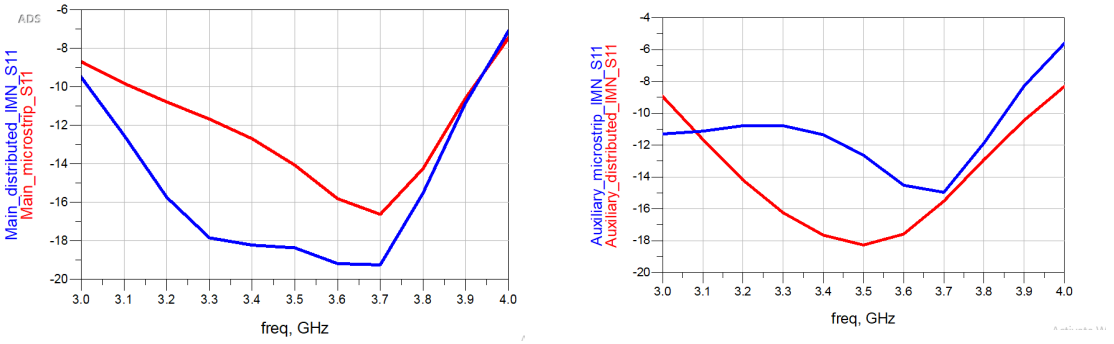
Other sources of non idealities are the T-junctions ,microstrip step,cross junctions and bends which can modelled each of them with reactive elements depending on the dimensions .These discontinuities will change the matching networks previously designed in ideal lines .So we have to tune and optimize in order to obtain similar results. And however the bandwidth of IMN and OMN we don't expect to be the same ,also the output power because of slightly mismatch and losses is expected to be reduced.



(a) Main OMN

(b) Auxiliary OMN

Fig. 4.4 Reflection coefficient of main and aux OMN with comparison between ideal and microstrip OMN



(a) Main IMN

(b) Auxiliary IMN

Fig. 4.5 Reflection coefficient of main and aux IMN with comparison between ideal and microstrip IMN

OMN reflection coefficient at drain (in saturation) as we see in fig4.4 where a comparison between the real microstrip circuit and the ideal one is shown .In band output matching can be considered very similar to the ideal one and as we see a max reflection coefficient of around -15dB for the main and max of around -20dB for auxiliary.

IMN reflection coefficient of a microstrip (fig4.5) compared to the ideal one has some increasing and these is due to the higher number of discontinuities of the lines compared to OMN.At the same time a higher Q factor of the input parasitics is high so it makes it more difficult .However the band of IMN and its response can be considered align with what we have initially designed as optimum IMN.

Input Splitter

We have to design an amplifier with single input power source and we need a circuit to divide the power between main and auxiliary input.The simulations made with two separated input ports which need a not equal input power and the ratio is

$$\frac{P_{in},main}{P_{in},aux} = 0.69$$

if the two input are matched at 50Ω.while there is a phase difference of -72° of the auxiliary input w.r.t main input phase .I add a 50Ω line at the auxiliary input of 18° degree and use a Branch Line Splitter to match the single input power source to the main and auxiliary input.

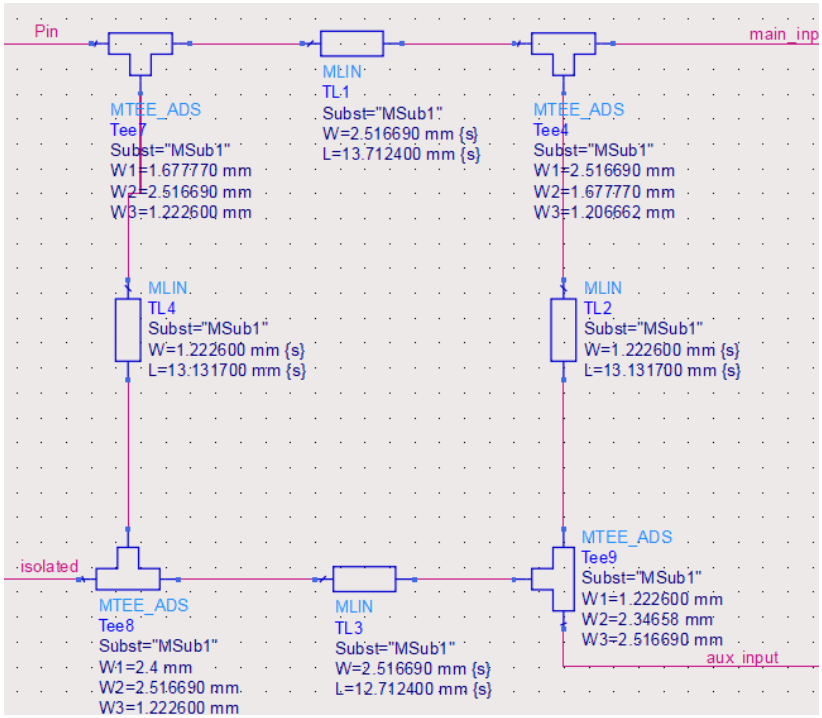


Fig. 4.6 Branch line input splitter

A branch line coupler with 90° phase difference between the 2 outputs (main and aux input) to obtain a 0.69 power ratio need four 90° degree transmission lines as in figure (TL1,TL2,TL3,TL4) with characteristic impedance

$$Z_{0TL1} = Z_{0TL3} = 33.9\Omega$$

$$Z_{0TL2} = Z_{0TL4} = 53.2\Omega$$

Adding the input splitter when the matching network do not perfectly match at 50Ω as we saw in fig4.5 will not give the exact power division between ports.The input splitter is designed for 50Ω termination resistance and the mismatch will give even some difference of power w.r.t the ideal terminations case.
Another problem is the in load pull measurements the optimum input load was significantly different for the higher frequencies of the band (3.7 and 3.8 GHz).In other words if in the low frequencies the input load behaved as a series inductance of value that we matched ,for higher frequencies the imaginary part has an abrupt change as in this case :at 3.5GHz $\Im(Z_{in}) = -10$ while at 3.8GHz $\Im(Z_{in}) = -16$. All this will give a reduced gain and reduced output power for the higher frequencies .At the same time since the matching circuits (especially IMN) had a wider band even for lower frequencies this amplifier will work well in this frequencies.The band can be extended [2.9GHz-3.6GHz].

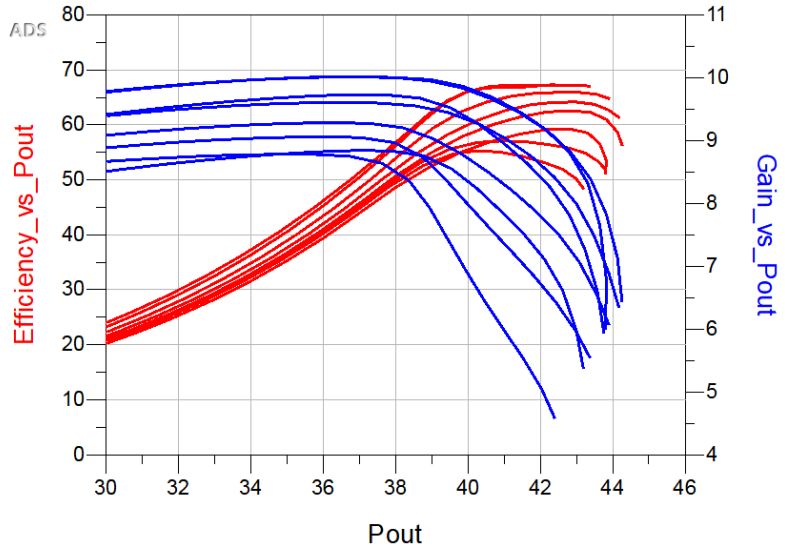


Fig. 4.7 G
Hz band]Efficiency(left) and Gain (right) versus frequency in 2.9-3.6GHz band

4.2 Layout

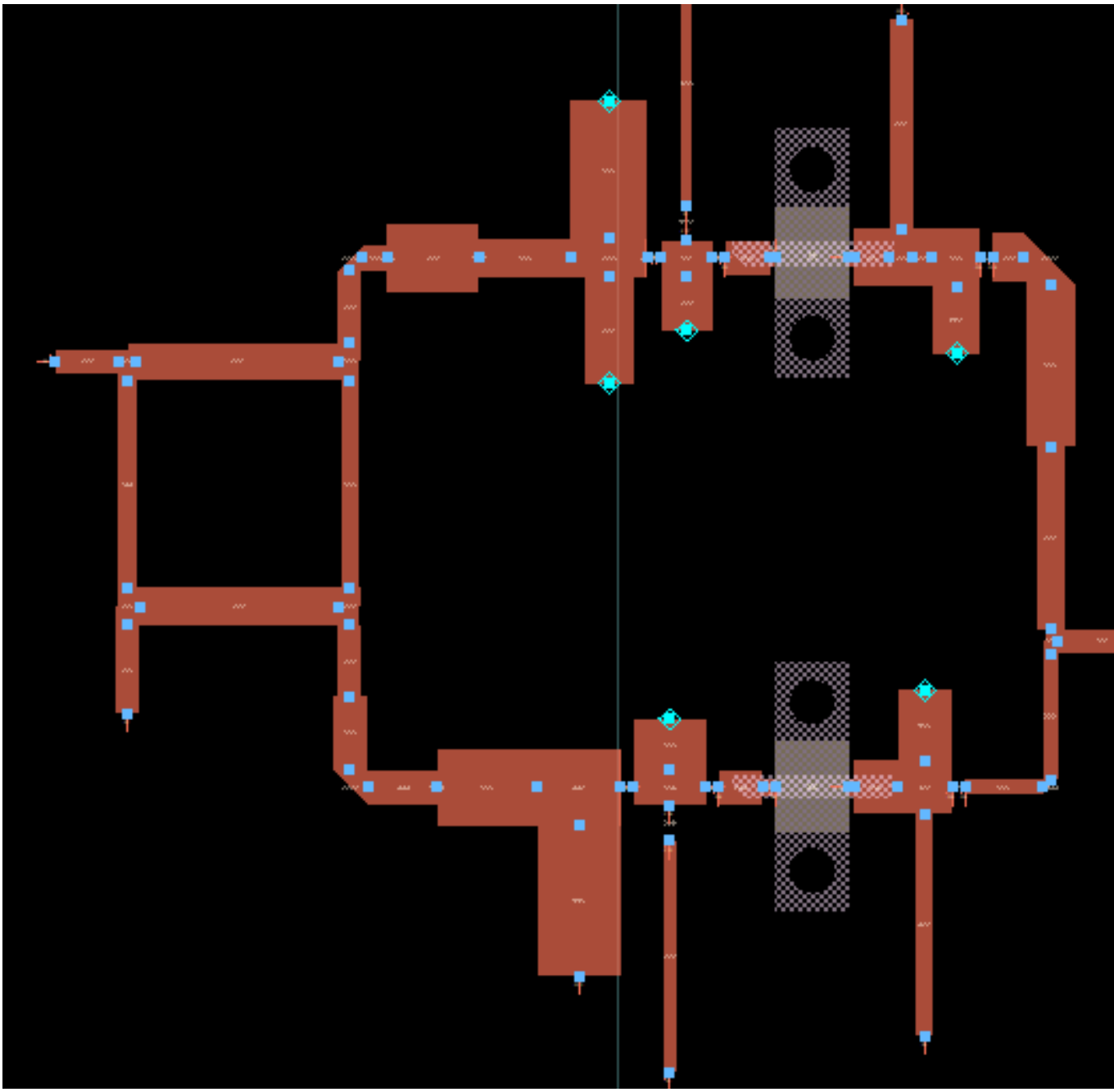


Fig. 4.8 Layout

4.3 Electromagnetic simulations

After generating the layout we have to make an electromagnetic simulation of the circuit which will give more exact results for the behaviour of all amplifier parameters.EM includes and make real simulations of electric and magnetic field on the circuits so it will give the results of interactions between different parts of the circuit that can change our predicted behaviour .
The input network including the splitter is particularly problematic in our case since it has relatively wide lines which radiate and will give losses but even interactions with other lines. At the beginning is better to split the problem by dividing the circuits in different parts and simulate each of them to fix the problems ,if there are .
EM will give results of different parts that are simulated in terms of S-parameters and this S-parameters box will be used in the circuit non linear simulation adding the devices and the lumped elements.
After achieving the correct results a final verification of the layout it is made and the results are similar to the microstrip circuit.

Efficiency in band vs output power

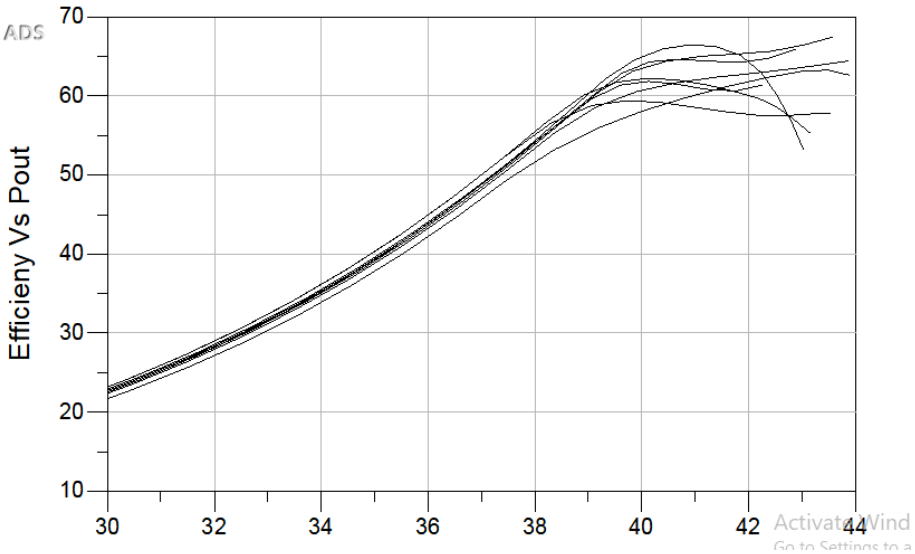


Fig. 4.9 Layout

From the figure can see that the efficiency in band is considerably high with

$$\eta_{Back-off} \in [53-56]\%$$

$$\eta_{sat} \in [56-68]\%$$

Gain in band vs output power

The gain in lower power region as we expect is higher than in saturation and Gain compression in saturation of around 4dB. $Gain_{Low,Power} \in [7.8 - 11]dB$

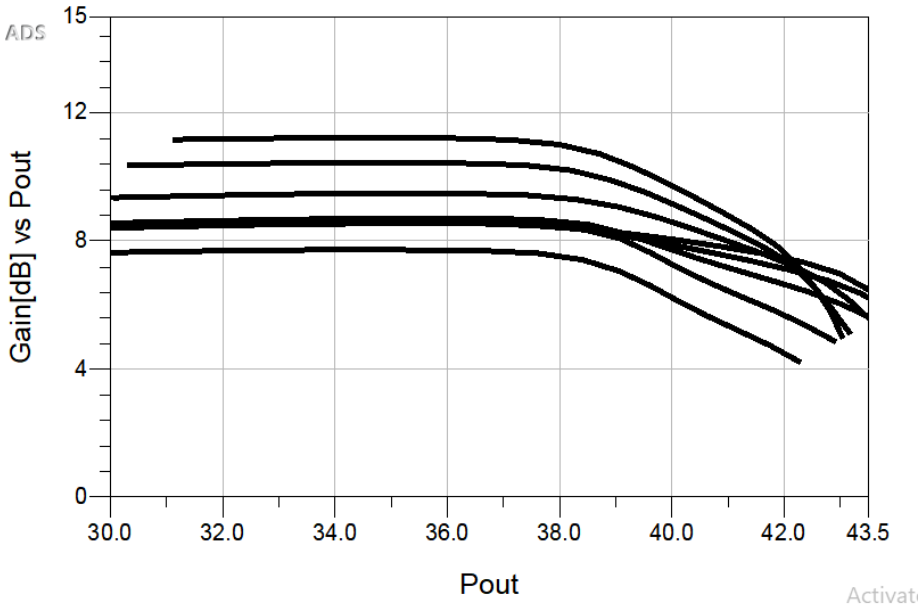


Fig. 4.10 Gain in band vs output power

PAE in band vs output power

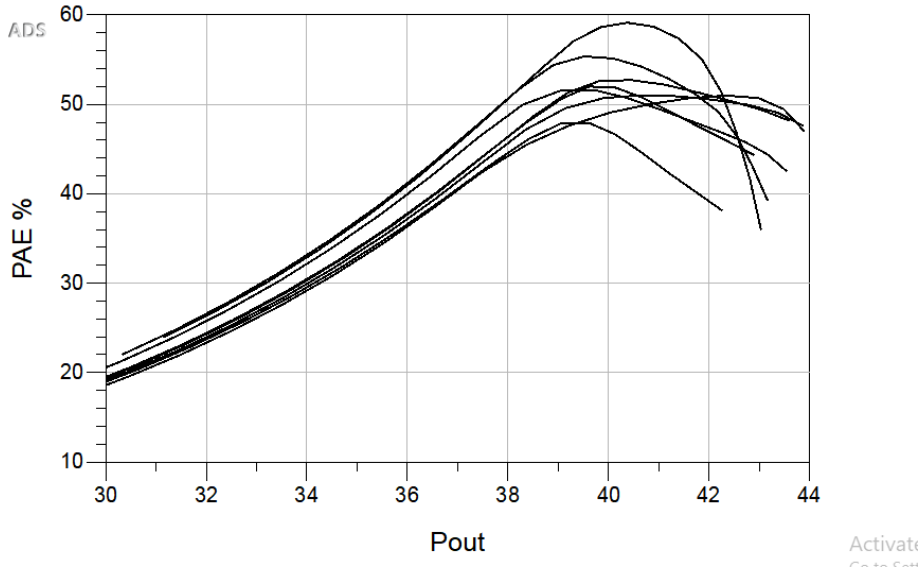


Fig. 4.11 PAE in band vs output power

Maximum output power in band

Saturation power goes from 42.3dB to a maximum of 43.9dB that can be considered aligned with our ideal design taking into account the losses that are introduced by the real circuit.

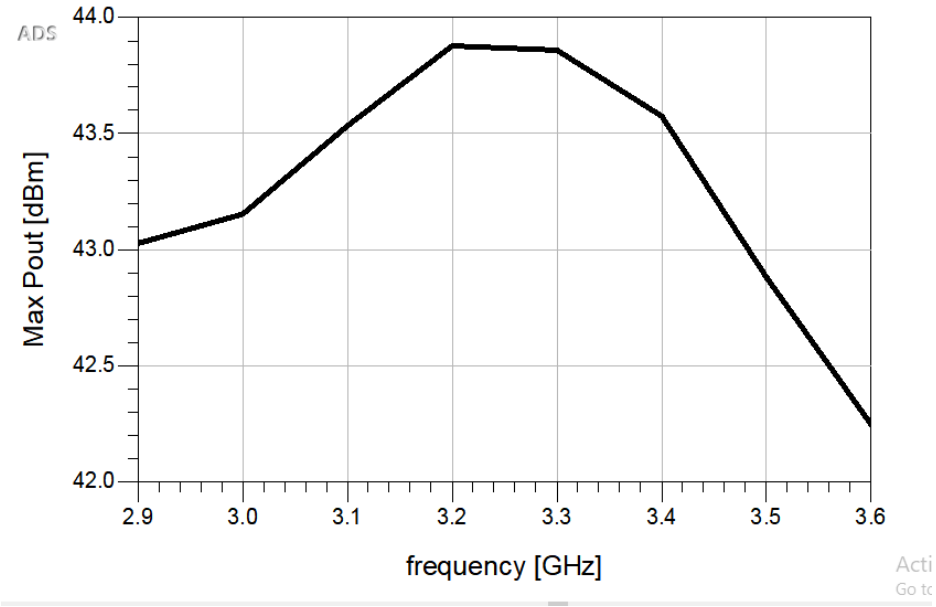


Fig. 4.12 Maximum output power in band

Maximum Efficiency in band

In fig4.13 the maximum efficiency in band is confined between 60% and 68%.

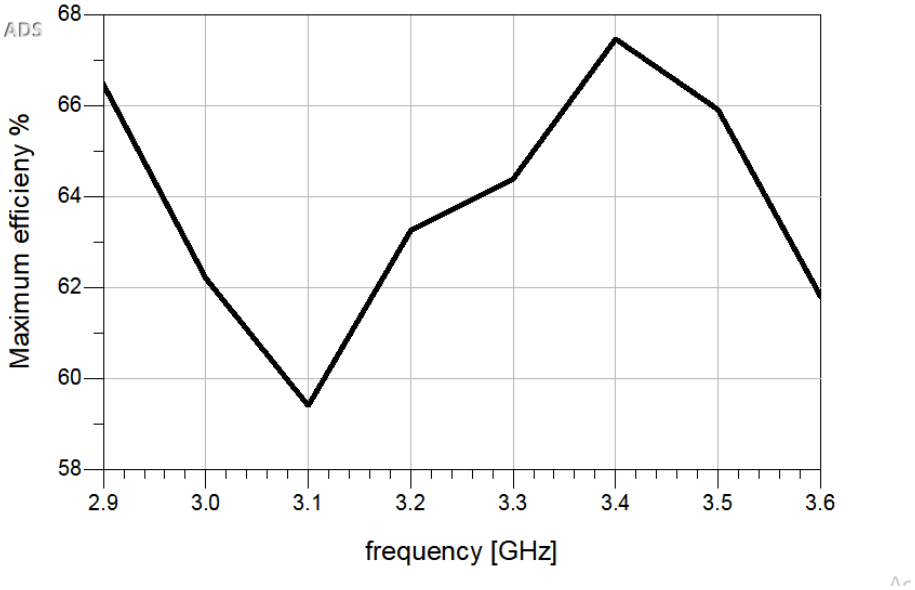


Fig. 4.13 Maximum Efficiency in band

AM-AM distortion The nonlinearites modelled by AM-AM and PM-PM distortion in

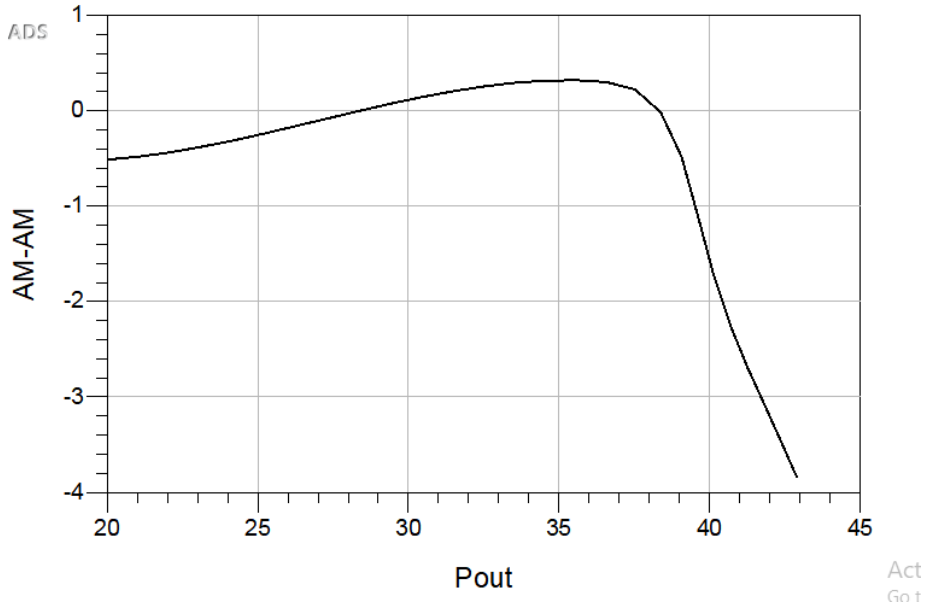


Fig. 4.14 AM-AM distortion

a Doherty are of two causes[L. Piazzon (2014)].The first are due to nonlinearities of the device since its parameters change with frequency .

PM-PM distortion

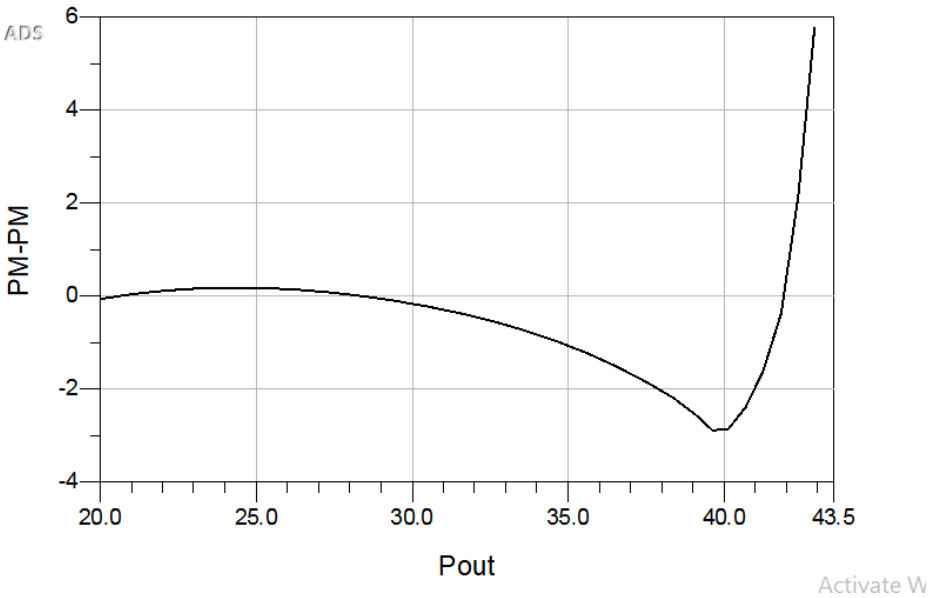


Fig. 4.15 PM-PM distortion

The second cause of nonlinearities is due to the way a Doherty is implemented that give effect especially on Main device where the load modulation will affect output phase and its input matching network .
The most problematic is the phase distortion PM-PM but in this design case it is very limited with a maximum of 5° degree of phase compression.

Third order intermodulation terms

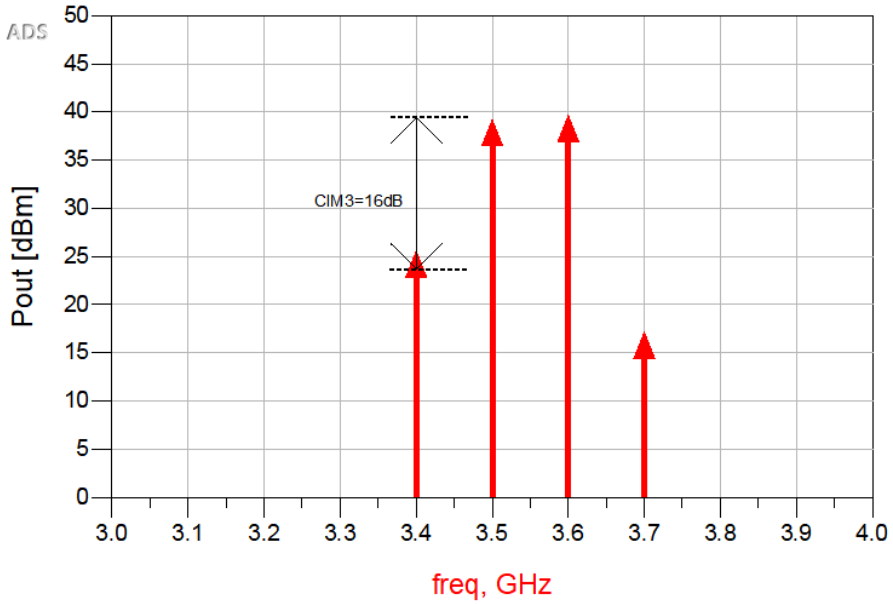


Fig. 4.16 Third order intermodulation terms

The third order modulation terms are measured with a two-tone test implementing an input source with 2 signals of equal power centered each at $f_1 = 3.5GHz$ and $f_2 = 3.6GHz$,so a spacing of 100MHz.The grpahs represents the third order terms near saturation and we see :

$$CIM_3 \approx 16dB$$

FINAL LAYOUT

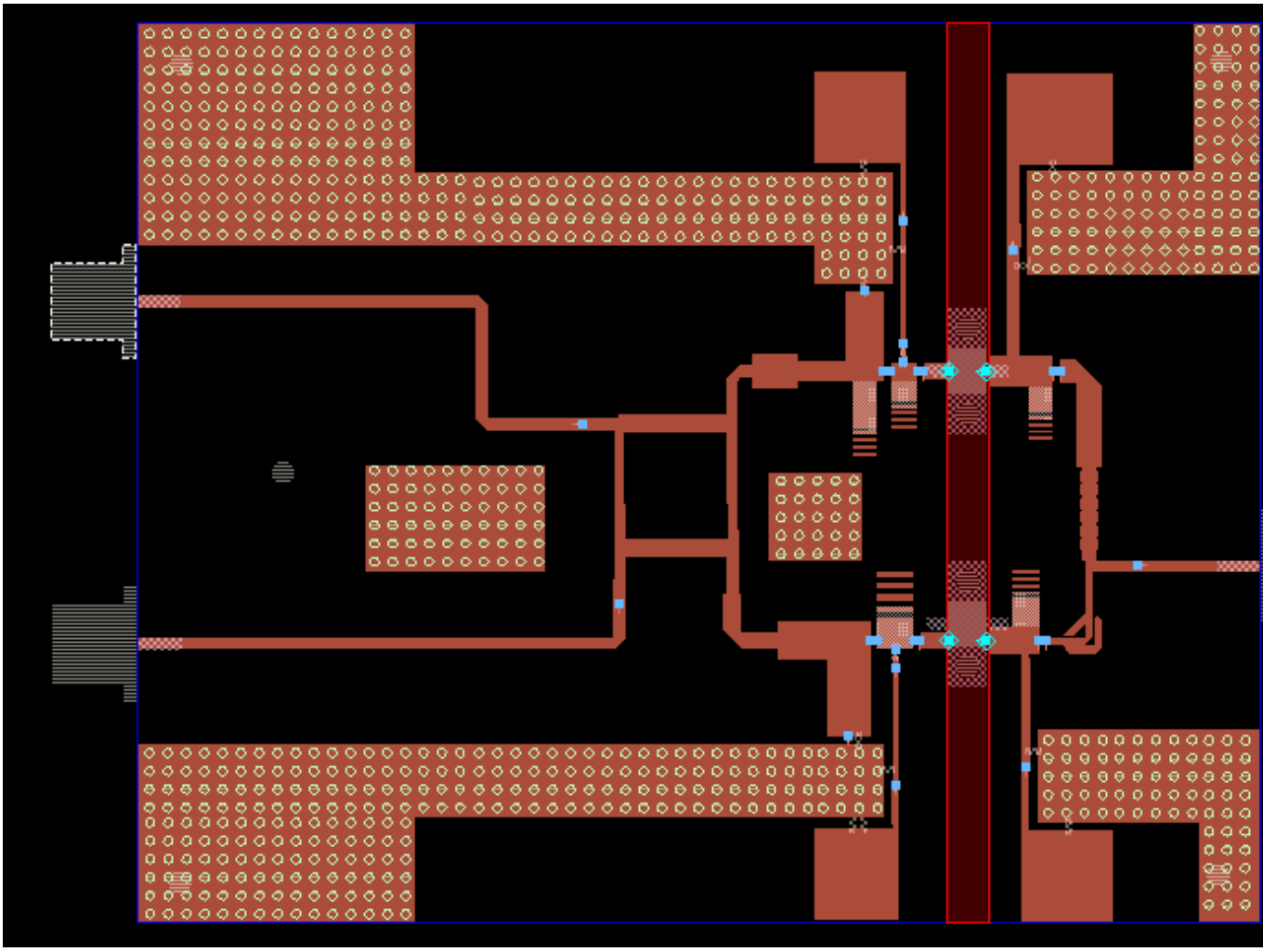


Fig. 4.17 FINAL LAYOUT

Chapter 5

Summary

Fifth Generation (5G) cellular systems are expected to see significant deployment starting from 2020, promising up to 10 Gbps data rate for stationary users. To support the power and cost efficiencies for the wireless modules for the different building block of the transceiver will become even more critical. Therefore, high-efficiency and linear 5G radio-frequency power amplifier design is definitely becoming more challenging and important. The performance of an radio frequency power amplifier can often dominate the overall transmitter performance, namely on its power-added-efficiency which dictates heat dissipation, in addition to the RF output power, linearity, reliability, yield, cost, and size. The power amplifiers can often consume more then 80% of the overall system power budget so their impact on cost of the overall transmitter dictates that their design is becoming fundamental.

The data transmission methods used for 5G will use complex modulation schemes such are quadrature amplitude modulation which use envelope amplitude signals for data transmission. With the increase of complexity of modulation, increases even the peak to peak average ratio, defined as the ratio between maximum and medium power. The peak to peak average ratio have a major impact on performance and it is one aspect of performance that needs to be considered for any 5G modulation scheme. It has a significant impact on the efficiency of the power amplifiers.
For the conventional classes of amplifier (A, AB,B,C) the medium efficiency significantly reduces with the increase of peak to average power ratio and for this reason different solution should be implemented in a transmitter.

At system level different solution exists, such as envelope tracking power amplifiers, in order to increase the efficiency for reduced power levels with respect to the saturation output power. But their implementation is complex, costly and energy spending.

At circuit level Doherty power amplifier is a possible solution for efficiency improvement, especially for base station applications, .Differently from the conventional classes, Doherty is designed to obtain an high efficiency from a reduced output power with respect to the maximum output power level up to saturation.

In this thesis, a hybrid high efficiency Doherty Power Amplifier is presented, working at the upper band of 5G (around 3.5 GHz). The design is consists in 2 packaged GaN-HEMT devices from Cree with a maximum output power of 13W. The design consists in an output matching network embedding the reactive parasitic element of the device and optimized for a power level of -6dB with respect to the saturation output power and and optimized input circuit and splitter in order to achieve wideband response.
The design and simulation are aligned with the state of the art of 5G applications in the upper 5G band . It is achieved a maximum efficiency in center frequency from 58% at power level of -6dB with respect to the saturation power up to 68% in saturation. In center frequency 3.5GHz a maximum saturation output power of 43.8dBm (24W) and a corresponding maximum gain of 11.5dB is obtained.
The designed PCB is ordered for production and as soon as it will be delivered the measurements and verification of the circuit will be made.

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