POLITECNICO DI TORINO
Department of Electronics and Telecommunications
Master degree course in Electronic Engineering

Master Degree Thesis

Low Power Long Term sEMG Monitoring Modular System

Supervisor
prof. Danilo Demarchi

Co-Supervisor:
dott. Paolo Motto Ros

Candidate
Benito Lorenzo Pugliese
matricola: s253862

Academic year 2018-2019

Abstract

The future of rehabilitation medicine will rely on technologies to monitor patients and implement rehabilitation interventions in their home. Technology that is wearable, low-cost, suitable for home use, and capable of operating for long periods of time will be of paramount importance in enabling interventions outside of the clinic.

This thesis is part of *SISTER*, a project conceived by *MITOR*, a collaboration between Politecnico di Torino, Massachusetts Institute of Technology (*MIT*) and Harvard Medical School. The goal of the project is to design and manufacture a wearable device to acquire and elaborate surface ElectroMyoGraphy (*sEMG*) data to characterize aberrant muscle activity patterns that rehabilitation medicine specialist will be able to use to plan clinical interventions. The innovative event-driven approach of Average Threshold Crossing (*ATC*) technique is implemented to drastically reduce the power consumption due to the minimal amount of data to be processed. It is obtained by averaging the number of sEMG Threshold Crossing (*TC*) events in a fixed time window.

Particularly the aim of this thesis project is to develop a modular board to meet the needs of the future testing phases.

The developed system layout has been designed to be compatible with commercial mechanical characteristics that make it an open system which can be easily interfaced with additional analog and digital modules. The main board has an integrated antenna and the microcontroller supports different wireless communication protocols such as Bluetooth Low Energy and others. It features also a micro SD card slot, a micro USB interface and a power management unit. A programmable gain sEMG acquisition module has also been developed improving the precedent versions basic structure. The power consumption optimization of the acquisition channel has been optimized by selecting ultra low power components.

A main board and an analog front end (4.4cm x 8.4cm each) have been thus designed and fabricated. The firmware has been developed and the validation of the final system has been performed.

Preliminary experiments show that the EMG acquisition channel power consumption has been reduced by about 60% and its reliability increased. The system peak power consumption has been reduced by about 50%, relaxing the battery constraints. By using a 2.6Ah battery the system can last more than one week of continuous operation.

Summary

This thesis is part of *SISTER*, a project conceived by *MITOR*, a collaboration between Politecnico di Torino, Massachusetts Institute of Technology (*MIT*) and Harvard Medical School. The goal of the project is to design and manufacture a wearable device to acquire and elaborate surface ElectroMyoGraphy (*sEMG*) data to characterize aberrant muscle activity patterns that rehabilitation medicine specialist will be able to use to plan clinical interventions. The innovative event-driven approach of Average Threshold Crossing (*ATC*) technique is implemented to drastically reduce the power consumption due to the minimal amount of data to be processed. It is obtained by amplifying the sEMG signal and compare it with a threshold. Each time the signal overcomes the threshold a Threshold Crossing (*TC*) event is generated. The ATC parameter is extracted averaging them in a fixed time window.

In this version of the project the system layout has been revolutionized making it modular. In the main board, which features the microcontroller unit, the power unit and a meander antenna, has pin headers to allow the addition of supplementary modules for future application. The acquisition channel module has been thus developed.

Improvements in the signal robustness and in the system reliability has been performed and at the same time the power optimization both from the hardware and software point of view was carried out.
On the hardware side off the shelf ultra low power components have been selected, whereas from the software side the peripherals management has been refined.

The document is organized in six chapters as follow:

1. **Introduction**: provides general information useful to the reader to understand this work. A brief introduction of the muscular system, the

surface electromyography signal and the average threshold crossing technique is present in the first section. The second section is about the state of art of the sEMG wearable devices, of the ATC applied to the sEMG and of commercial devices while the third section regards the previous versions of the system;

2. **Investigation**: in this chapter the analog front end of the previous version of the system is analyzed introducing the hardware targets to be improved in this new version. The two issues related to an instrumentation amplifier stacked in a saturation state and to a periodic dropout voltage present on the power supply line and reflected on the signal acquired are deeply investigated and solutions are presented. Follows the selection of the ultra low power off the shelf components to save power consumption, then the breadboard prototype of the acquisition channel with the new components is presented;

3. **Hardware Implementation**: in this chapter the design of the two board is carried out with Altium Designer. The analog front end module and the main board are thus treated separately and their schematics and PCB layout are presented.

4. **Firmware**: in this chapter is described how the slaves and of the master tasks are translated in software. The slaves firmware is first described showing the peripherals initialized, the algorithm for the threshold definition, the three working mode they can work on and the synchronization routine with the master. The master firmware is then briefly presented;

5. **Experimental Results**:in this chapter tests on the fabricated system have been performed. The verification of the correct behaviour after the issues faced is showed. A characterization of the gain in function of the frequency is reported as well as the tests on the programmable gains and on the three working modes. A measure of the power consumption of the analog acquisition module alone and on the system assembled is reported;

6. **Conclusion**: in this chapter the work done is summed up and possible future developments are presented.

Acknowledgements

Contents

List of Tables 11

List of Figures 12

1 Introduction 17
- 1.1 Muscular System . . . 17
  - 1.1.1 Surface ElectroMyoGraphy (sEMG) . . . 18
  - 1.1.2 Average Threshold Crossing (ATC) . . . 19
- 1.2 State of Art . . . 20
  - 1.2.1 sEMG Wearable Acquisition Devices . . . 20
  - 1.2.2 ATC Applied to sEMG . . . 22
  - 1.2.3 Commercial sEMG Devices . . . 23
- 1.3 Previous Versions . . . 24
  - 1.3.1 Slaves . . . 24
  - 1.3.2 Master . . . 26

2 Investigation 27
- 2.1 Analog Front End Overview . . . 27
  - 2.1.1 Overvoltage Protection . . . 28
  - 2.1.2 Voltage Followers . . . 29
  - 2.1.3 Differential High Pass Filter 30Hz . . . 30
  - 2.1.4 Instrumentation Amplifier . . . 31
  - 2.1.5 Feedback Low Pass Filter 10Hz . . . 32
  - 2.1.6 Driven Right Leg . . . 34
  - 2.1.7 Sallen-Key Low Pass Filter 400Hz . . . 35
  - 2.1.8 Comparator . . . 36
- 2.2 INA Saturation Issue . . . 37
  - 2.2.1 Background . . . 37
  - 2.2.2 Investigation . . . 38

2.2.3 Solutions . . . 42
2.3 Periodic Drop Out Issue . . . 43
2.3.1 Background . . . 44
2.3.2 Solutions . . . 46
2.4 Off The Shelf Changes . . . 48
2.4.1 Instrumentation Amplifier . . . 49
2.4.2 Operational Amplifier . . . 52
2.4.3 Switch SPST . . . 53
2.4.4 Voltage Reference . . . 54
2.4.5 Analog Front End Voltage Regulator . . . 55
2.4.6 Voltage Regulator Main Board . . . 55
2.4.7 Micro SD Card . . . 56
2.4.8 Battery . . . 57
2.5 Breadboard Prototype . . . 58

3 Hardware Implementation 63
3.1 Schematics . . . 63
3.2 Analog Front End . . . 64
3.2.1 Input Stage . . . 64
3.2.2 First Amplification Stage . . . 68
3.2.3 Low Pass Filter Stage . . . 72
3.2.4 Threshold Crossing Stage . . . 74
3.2.5 Analog Voltage Regulator . . . 76
3.2.6 Analog Pin Headers . . . 77
3.3 Main Board . . . 78
3.3.1 Microcontroller . . . 78
3.3.2 Power Management Unit . . . 81
3.3.3 SD Interface . . . 81
3.3.4 Peripherals . . . 81
3.4 PCB Layout . . . 85
3.4.1 Analog Front End . . . 85
3.4.2 Main Board . . . 87

4 Firmware 93
4.1 Slaves . . . 93
4.1.1 Initialization . . . 95
4.1.2 Threshold Definition Algorithm . . . 97
4.1.3 Work Modes . . . 100
4.1.4 Synchronization . . . 103

4.2 Master 103

5 Experimental Tests 107
5.1 INA Saturation 108
5.2 Periodic Dropout 109
5.3 Bandwidth 111
5.4 Programmable Gains 113
5.5 Working Modes 115
5.5.1 Raw Data 116
5.5.2 Envelope 117
5.5.3 ATC 118
5.6 Power Consumption 119
5.6.1 Analog Acquisition Channel 119
5.6.2 Two Module System 120

6 Conclusion 125

Bibliography 127

List of Tables

2.1 Instrumentation Amplifiers table 51
5.1 Power Consumption comparison of the previous and the current version in the three working modes. 120

List of Figures

1.1 Amount of data comparison between the ATC technique and the classic approach . . . 20
1.2 Standard structure of sEMG acquisition chain . . . 21
1.3 Commercial sEMG Devices . . . 23
1.4 Mitor2 slave: Top side (*left*) is reserved for the digital part and bottom side (*right*) is reserved for the analog part . . . 24
1.5 Disposable surface EMG electrode . . . 25
1.6 nRF52840 Development Kit by Nordic Semiconductor . . . 26
2.1 Mitor2 Analog Front End block scheme . . . 28
2.2 Mitor2 Analog Front End Overvoltage Protection circuit . . . 29
2.3 a) Voltage follower, b) 2 channel voltage follower . . . 30
2.4 Second order passive High Pass Filter 33.86Hz . . . 30
2.5 Amplification stage, G=922V/V . . . 31
2.6 Analog Switch between INA reference and output . . . 32
2.7 INA feedback and Low Pass Filter 10Hz for INA reference voltage generation . . . 33
2.8 Driven Right Leg circuit . . . 34
2.9 Driven Right Leg circuit . . . 35
2.10 a) Comparator in Schmitt Trigger configuration, b) Output Hysteresis curve . . . 36
2.11 First acquisition system prototype . . . 37
2.12 Mitor2 slave: Top side (*left*) is reserved for the digital part and bottom side (*right*) is reserved for the analog part . . . 38
2.13 Saturation Issue incriminated part . . . 39
2.14 Analog Front End LTSpice circuit for deeper investigation . . . 39
2.15 INA loop with INA reference forced to high voltage . . . 40
2.16 LTSpice INA output when reference forced to high voltage . . . 41
2.17 INA321 Datasheet showing reference voltage constraint . . . 41
2.18 INA loop with parallel diodes to prevent the reference to exceed the safe range . . . 42

2.19 INA321 Datasheet showing reference voltage constraint 43
2.20 Dropout voltage on the INA reference during the SD periodic writings 44
2.21 Focus on the voltage divider R8,R9 for the INA voltage reference generation 45
2.22 Baseline of sEMG signal acquired influenced by power supply dropout voltage during the periodic SD writings 45
2.23 TPS61099x datasheet load regulation: Output Voltage vs Output Current 46
2.24 Lithium Thionyl Chloride cells coin battery from Tadiran datasheet 47
2.25 Instrumentation amplifier classic structure. Gain adjustable by changing R_G 49
2.26 INA321 internal structure and gain 50
2.27 Operation Amplifier Component 52
2.28 4 Channel Switch SPST structure 53
2.29 Voltage Reference symbol 54
2.30 Shunt Voltage Reference structure 54
2.31 Low Drop Out voltage regulator 55
2.32 Buck-Boost voltage regulator 56
2.33 Apacer micro SD card 56
2.34 Lithium Thionyl Chloride cells coin battery from Tadiran datasheet 57
2.35 Lithium Thionyl Chloride ($LiSOCl_2$) LS14500 datasheet . . . 58
2.36 Breadboard Prototype Analog Acquisition Channel 59
2.37 Analog Acquisition Channel Breadboard Prototype 59
2.38 MSP430FR5969 Launchpad 60
2.39 System composed by the Analog Front End Breadboard prototype and the MSP430FR5969 Launchpad 61
2.40 Gastrocnemio Medialis sEMG signals acquired and processed by the breadboard, sampled by the MSP430 and graphed with Matlab during 14 gaits 62
2.41 Power Spectrum Density signals acquired and processed by the breadboard, sampled by the MSP430 and graphed with Matlab during 14 gaits 62
3.1 Analog Front End Module Block Scheme 65
3.2 Input Stage Schematic: Protection Circuit; Buffers; 30Hz Differential High Pass Filter; Driven Right Leg Circuit 66
3.3 First Amplification Stage: 500 Gain Instrumentation Amplifier; Feedback 10Hz Low Pass Filter; 1.25V Voltage Reference 68

3.4 Programmable Gain Stage: Non Inverting Amplifier with Switch SPST for programmable gain . . . 71
3.5 Low Pass Filter Stage: 400Hz Unitary gain Sallen-Key . . . 73
3.6 Threshold Crossing Stage: Comparator in 44mV Hysteresis Schmitt Trigger configuration . . . 74
3.7 2.5V Linear Drop out Analog Front End Voltage Regulator . . 76
3.8 Pin Headers on the Analog module . . . 77
3.9 Main Board Block Scheme . . . 79
3.10 Microcontroller schematic . . . 80
3.11 Power Management Unit Schematic . . . 82
3.12 SD interface Schematic . . . 83
3.13 Peripherals schematic: DAC, Leds, JTAG, Reset Button, micro USB . . . 84
3.14 Analog Front End PCB Top . . . 85
3.15 Analog Front End PCB Bottom . . . 86
3.16 Analog Front End PCB 3D Top . . . 87
3.17 Analog Front End PCB 3D Bottom . . . 88
3.18 Main Board PCB Top . . . 88
3.19 Main Board PCB Bottom . . . 89
3.20 Main Board End PCB 3D Top . . . 90
3.21 Main Board PCB 3D Bottom . . . 91
4.1 Slave High level flowchart . . . 94
4.2 Threshold Definition Algorithm . . . 99
4.3 Raw Data routine . . . 100
4.4 Envelope routine . . . 101
4.5 ATC routine . . . 102
4.6 Slaves Synchronization flowchart . . . 104
4.7 Master High Level flowchart . . . 105
5.1 Two modules system assembled . . . 107
5.2 Main board top and bottom view . . . 108
5.3 AFE module top and bottom view . . . 108
5.4 Focus on the INA behavior during the startup transient of the Acquisition Channel . . . 109
5.5 Dropout voltage on the INA reference during the SD periodic writings in the precedent versions of the system . . . 110
5.6 Baseline of sEMG signal acquired influenced by power supply dropout voltage during the periodic SD writings in the precedent versions of the system . . . 110

5.7 Dropout voltage on the battery terminals during the SD periodic writings in the new version of the system . . . 111
5.8 Dropout voltage on the buck-boost output during the SD periodic writings in the new version of the system . . . 112
5.9 Dropout voltage on the acquisition channel LDO output during the SD periodic writings in the new version of the system . 112
5.10 Dropout voltage on the acquisition channel 1.25V voltage reference output during the SD periodic writings in the new version of the system . . . 113
5.11 Gain variation with respect to the input signal frequency. Gain of the acquisition channel is set to 500. . . . 113
5.12 Gain 500 test with hundreds of μV in INA differential input . 115
5.13 Gain 1000 test with hundreds of μV in INA differential input . 115
5.14 Gain 1500 test with hundreds of μV in INA differential input . 116
5.15 Gain 2500 test with hundreds of μV in INA differential input . 116
5.16 Gain 3000 test with hundreds of μV in INA differential input . 117
5.17 Wrist extension acquired in Raw Data mode . . . 117
5.18 Wrist extension acquired in Envelope mode . . . 118
5.19 Wrist extension acquired in ATC mode . . . 118
5.20 Analog Front End power consumption analysis during three maximal voluntary contractions . . . 119
5.21 Power consumption analysis during Raw Data mode . . . 121
5.22 Power consumption analysis during Raw Data mode - Focus on the small peaks . . . 121
5.23 Power consumption analysis during Envelope mode . . . 122
5.24 Power consumption analysis during Envelope mode - Focus on the small peaks . . . 123
5.25 Power consumption analysis during ATC mode . . . 124
5.26 Power consumption analysis during ATC mode - Focus on the small peaks . . . 124

Chapter 1

Introduction

This thesis is part of the Mitor project. The Mitor project aim to support the rehabilitation specialist to treat patient with neuromuscular diseases. The study of muscles synergies is infact important to design the correct treatment and to evaluate how it need to be changed according to the patient needs.

The system can be divided in two main part: an analog front end and a digital part.
The analog front end is in charge to acquire and elaborate the electromyographic signal to be then sampled and stored in the SD Card from the digital part.
The previous version of this project have some electrical problem that this version aim to fix and overcome with additional features. Modularity

1.1 Muscular System

The muscular system is an organ system that permits the movement of the body, to maintain the posture to protect the underlying organs and to circulates the blood through the body. It is mostly controlled through the nervous system even though some muscles are completely autonomous. The muscular system and the skeletal system form the musculoskeletal system that is responsible of the body movement.
The muscles can be categorized in the three different type depending on the kind of tissue they are made of:

- Skeletal Muscle: voluntary striated muscle attached by means of tendons to the bones and responsible for the body movement;

- Smooth Muscle: involuntary non-striated muscles controlled by the Autonomous Nervous System;
- Cardiac Muscle: involuntary striated muscles that controls the heart rhythmic contraction.

1.1.1 Surface ElectroMyoGraphy (sEMG)

The electromyography signal represent the neuronal and muscular activities and is the result of the depolarization and re-polarization of the muscle fibers external membrane. The amplitude of the signal strongly depends on the anatomical characteristics of the muscles interested but also on the properties of the electrodes used and on their collocation.
Two different technique are used in the electromyography: intramuscular EMG and surface EMG. The former is made by needle electrodes placed between the muscles and allows a more selective observation of their activation. Signal morphology can be studied with this approach where also there are the absence of muscles filtering and movement artifact. The disadvantages of the this method is the invasiveness and the restriction to not be able to acquire signals dynamically. The surface electromyography instead is a non invasive technique that give information about the muscle activity also during movements. surface electrodes are attached on the skin surface upon the muscle, thus the signal is attenuated and filtered to reach the surface of the skin. Common electrodes used in EMG acquisition are made of silver/silver chloride (A_g/A_gC_l) that have the property of not polarizing.
The source of interference for the sEMG signal are the following:

- Electronic Noise: noise introduced by the components of the acquisition channel circuit;
- Motion Artifact Noise: noise due to the movement of the electrode cables and the sliding of electrode on the skin;
- Muscle Crosstalk: the signal acquire has also contributes of the activation of the close muscles;
- ElectroCardioGraphy Artifact: the ECG signal has a bandwidth up to 100Hz and influence the signal acquired.
- Environment Noise: lights, electronic devices etc. contributes to the noise. Particularly influence is done by the 50Hz.

To reduce the motion artifact noise, a conductive gel can be added to the electrodes to increase the electrode stability.
There two type of EMG acquisition depending on how the electrodes are mounted:

- Monopolar: a single surface electrode and a reference electrode are used. It is more susceptible to external disturbances because it has a large sensing volume;

- Bipolar: two surface electrodes and a reference electrode are used. With this approch the signal is obtained by the difference between the signals acquired by the two electrodes, removing thus the common mode voltages on the two signals.

1.1.2 Average Threshold Crossing (ATC)

The Average Threshold Crossing signal is a Quasi-Digital signal that gives information about the number of events in a fixed time window. The events are generated each time the original signal overcome a certain threshold and are easily obtainable in hardware by means of a comparator and a threshold. The digital signal generated by the events is the Threshold Crossing (TC) signal. The ATC is a Quasi-Digital signal because the information it brings is generated by the distance in time of the events and the time is an analog quantity.
This technique brings a huge amount of power consumption because instead of sampling with an Analog to Digital Converter the sEMG signal, the system can sleep mostly of the time saving power and wake up each time an event is generated (Figure 1.1).

The ATC technique properties can be maximized with the use of the Impulse Radio Ultra Wide Band ($IT\text{-}UWB$) as wireless communication protocol. It is an asynchronous and robust protocol that is extremely suitable for a system that exploits ATC.
With respect to the classic approach, the ATC signal can not be used for diagnosis purpose.

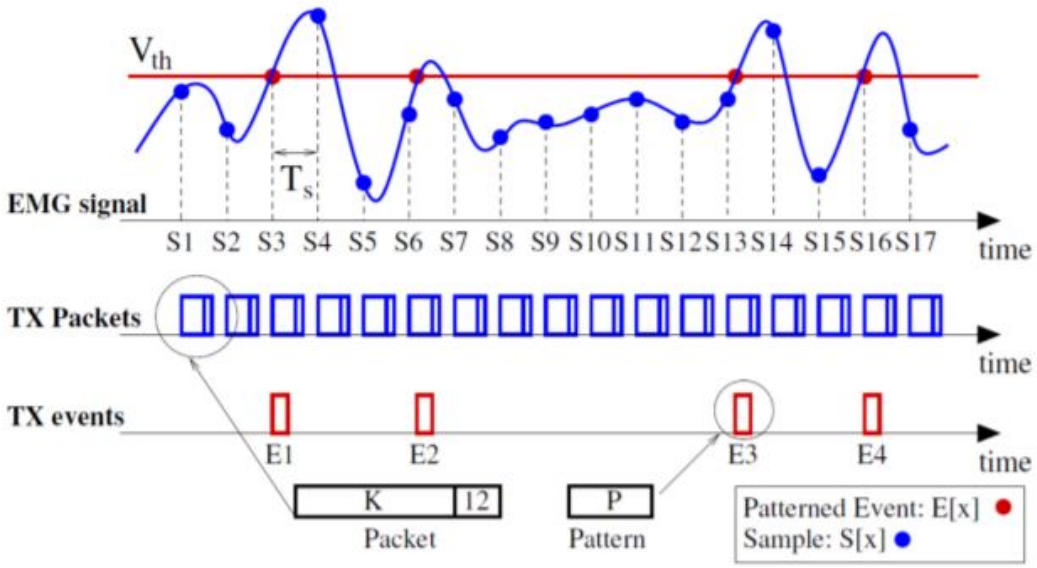

Figure 1.1. Amount of data comparison between the ATC technique and the classic approach

1.2 State of Art

1.2.1 sEMG Wearable Acquisition Devices

Anatomical and physiological studies on the surface ElectroMyoGraphy (*sEMG*) signal has been largely done in the recent years for the diagnostic medicine and the rehabilitation field.
The sEMG acquisitions have a quite standard structure like the one in Figure 1.2.

Three electrodes generally are used because the bipolar acquisition is preferred for this type of application. Two of them are placed above the muscle to be acquired the activity and the other one on a neutral part where a reference voltage can be applied. The acquisition chain acquire the signals from the two electrodes above the muscle while provides a DC voltage on the reference electrodes. The acquisition chain is generally divided in two part, an analog channel to amplify and filter the signal and a digital part to sample it and send the data to a workstation. The input signals ranges from about $50\mu V$ to few mV, and the amplification often used for them is about 1000. Then signal is filtered to save the wanted bandwidth and remove the source of noise outside it. Generally the bandwidth saved is 10Hz-500Hz. An

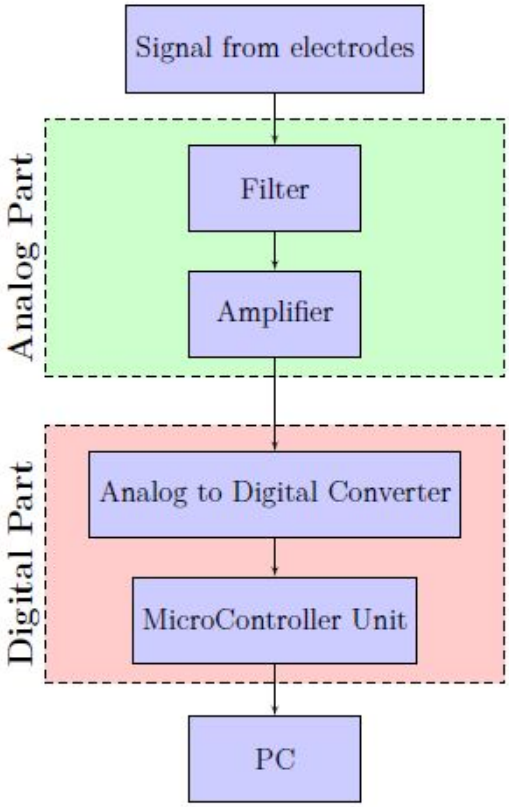

Figure 1.2. Standard structure of sEMG acquisition chain

Analog to Digital Converter (ADC), controlled by a micocontroller, samples the conditioned signal. The data are then stored locally or sent by cable or wireless to a workstation.

Challenges related to the sEMG acquisition are related to the acquisition during a dynamic effort. The signal produced by a static contraction produces good results but the static contraction does not represent a typical movement scenario. Dynamic acquisition have though difficulties related to the introduction of movement artifact noise for the cable movement of for the electrodes slicing and also some possible difficulties in the movement for the presence of the cables that could obstruct it.

To overcome the problems introduced by the cables, the wireless technology is the answer to effectively make the system wearable and thus able to acquire dynamically. A battery to supply the system becomes thus necessary

and the challenges is now shifted on extend its life time.

Ultra low power electronics and the Average Threshold Crossing (ATC) technique are the answer for saving huge amount of power consumption and make the system last longer. The ATC technique does not need the use of an ADC but of a simple comparator to generate the Threshold Crossing signal.

1.2.2 ATC Applied to sEMG

Applying to the surface ElectromyoGraphy signal ($sEMG$) the Average Threshold Crossing (ATC) technique is becoming very useful for its power consumption savings with respect to the classical approach. In some works are reported the validity this technique.

In [8] a wireless system based on the Impulse Radio Ultra Wide Band ($IR\text{-}UWB$) and the ATC technique that can transmit muscle force information is presented. The asynchronous IR-UWB technology consists in short duration pulses and an active Radio Frequency (RF) timing control to reduce the transmission and receiving power consumption. The system acquire the sEMG signal with a bipolar acquisition, amplifies it and each time the signal overcome a threshold a transmission is performed. The Receiver is connect to an Arduino and is in charge of count the number of events generated by the acquisition system and display them on a PC. In the paper, the advantages in term of power consumption of the combination of the ATC and IR-UWB is demonstrated and the ATC parameters extracted are validated. The Average Rectified Value (AVR) of the sEMG signal is compared with ATC parameters showing a correlation of 0.97 ± 0.02 for the former and 0.95 ± 0.02 for the second.

The same team improved the system in [9]. The system system is extended to multiple acquisition channels using the asynchronous handshaking Address-Event Representation (AER) as transmission protocol. The AER is applied to each channel to distinguish the chip address and the input channels. It consist of an event arbiter to manage the concurrent events detection and transmission, an event decoder to generate the individual data packet and a modulator for triggering the event for the IR-UWB. Power consumption advantages are demonstrated in this paper as well as the ATC robustness with respect to event losses, SNR and the amplifier distortion and saturation achieving a tolerance of 70% for event losses and about 5-6dB for SNR.

In [10], the lowest complexity achievable by an ATC system is investigated. The prototype they have produced has a 23 × 34mm size where first order filters are applied to obtain a band of 10Hz-1kHz and an UWB transmitter chip is used for the transmission. The power consumption of this PCB is 5.65mW while the power consumption of the entire system, acquisition unit and receiver is 15.49mW. In vivo isometric and isotonic contraction tests shows that the muscle rest state can be descriminated by the system and that with the increase of force produced the TC events increase too.

In [11] is presented how a dynamic threshold can be generated by a custom digital control logic implementing Dynamic ATC (*D-ATC*) algorithm. The improved robustness with respect to the sEMG variability of the dynamic threshold with respect to the fixed threshold has been shown.

1.2.3 Commercial sEMG Devices

Commercial wearable sEMG devices already exist on the market. The weakness of these devices is the battery life time that is not able to last enough time to monitor patients during more days. Popular devices are reported in Figure 1.3 and their characteristics are briefly explained in the following.

Figure 1.3. Commercial sEMG Devices

- FREEEMG: produced by BTS Engineering, this device supports up to 20 simultaneous probes recording. Its size is $41.5mmx24.8mmx14mm$ and it does not embed a micro SD card for local storing. Its battery life is 6 hours of continuous acquisition;
- PicoEMG: produced by Cometa. It exploits two monopolar electrodes and can support up to 32 devices synchronous acquisition. Continuos signal acquisition can last up to 12 hours with wireless transmission and up to 8 hours for data logging ona a memory on board;

- DataLITE sEMG: produced by Biometrics ltd. Its continuos acquisition can last up to 8 hours and its dimension are $42mmx24mmx14mm$.

1.3 Previous Versions

Three versions of the project have been already prototyped, the first two from Ph.D Abuduwaili Tuoheti and the last one by dott. Giovanni Manzella. The project is composed by a system of 6 slaves and one master. The slaves are in charge of acquire the ElectroMyoGraphic (*EMG*) signal from selected muscles, while the master is in charge to manage the synchronization between them. The signals acquired are stored locally in a micro SD. When the acquisition is completed, the signals are downloaded and elaborated with a Non Negative Matrix Factorization (*NNMF*) to extract the signal of the muscle synergy.

1.3.1 Slaves

The last version of the slave have been designed and prototyped by dott. Giovanni Manzella (Figure 1.4).

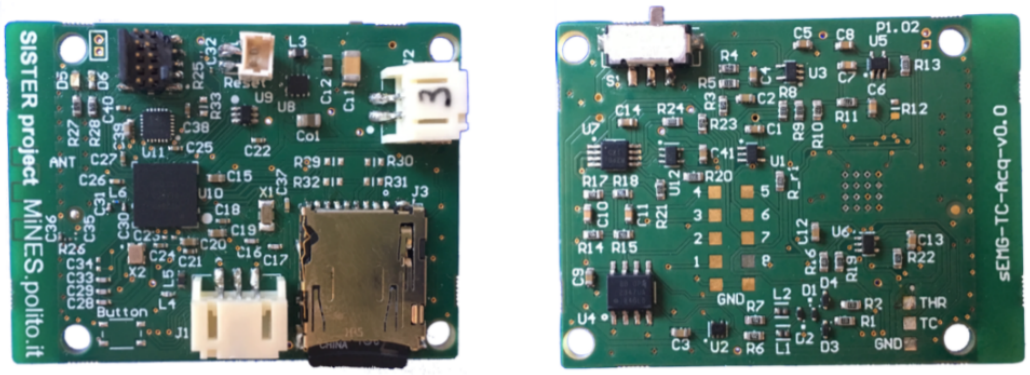

Figure 1.4. Mitor2 slave: Top side (*left*) is reserved for the digital part and bottom side (*right*) is reserved for the analog part

Each slave is a 2-layer board with component on both sides. The top side was reserved for the digital part and the bottom layer for the analog part. The EMG signal is the input of the analog front end. It is acquired by means

of regular disposable surface EMG electrodes (Figure 1.5) from the surface of the skin.

Figure 1.5. Disposable surface EMG electrode

The surface EMG (*sEMG*) signal is filtered and amplified resulting in a signal of bandwidth 30-400Hz and a rail to rail amplitude over 3.3V centered in middle dynamic (1.65V). The output of the analog front end is thus provided both as an analog signal and a Threshold Crossing (*TC*) signal obtained by a comparator and a threshold given by the digital part.
The digital part is in charge of different tasks:

- Manage the synchronization with the master;
- Sample the sEMG signal elaborated by the analog part;
- Count the number of TC events in predefined time windows;
- Provide the threshold to the comparator in the analog front end by means of an external DAC.
- Elaborate data in 3 different modes: Normal sEMG, Envelope and ATC;
- Store data locally in a micro SD.

1.3.2 Master

As master has been used the nRF52840 Development Kit by Nordic Semiconductor (Figure 1.6).

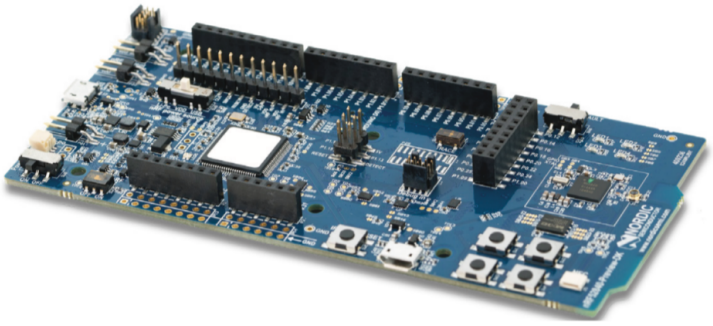

Figure 1.6. nRF52840 Development Kit by Nordic Semiconductor

It is in charge of synchronize the slaves and select one of the 3 slave working modes. One of the 2x2 buttons matrix is used to start and stop the slaves acquisition recording while the other 3 to select one of the 3 slaves working mode:

- Normal sEMG: the slaves store in the micro SD the full sEMG signal;
- Envelope: the data stored in the micro SD are the envelope of the sEMG acquired;
- ATC: the data stored in the micro SD are the Average Threshold Crossing of the sEMG in the time windows.

The structure of the new version is remain unchanged.

Chapter 2

Investigation

During the evolution of this project the acquisition channel has been time to time improved preserving the base structure. An issue that goes along with every prototype is the saturation of the Instrumentation Amplifier (*INA*) in the amplification stage of the chain. In section 2.2 this issue is analyzed and solved.
The last prototype is the Mitor2 project taht was developed with the aim of identify the best synchronization time interval, between slaves and master, to reduce the power consumption and let the system work correctly. In the verification phase a periodic drop out voltage showed up on the signal acquired. This issue is analyzed in section 2.3.
In this chapter the system is first analyzed block to block and then each issue is faced and solved. A power optimization of the analog front end is thus performed by means of a deep research of ultra low power electronics and design changes. A breadboard prototype with the new components will be then presented and tested.

2.1 Analog Front End Overview

The basic structure of the precedent prototypes have been preserved thus the last one will be analyzed in the following. In Figure 2.1 the block scheme of the Mitor2 Analog Front End (*AFE*) is reported. It is supplied by a single positive power supply of 3.6V.

3 Electrodes are applied on the for the muscle to be acquired:

- Reference Electrode: a reference electrode is applied on tendon and it is used to set to a known and middle dynamic potential the muscle;

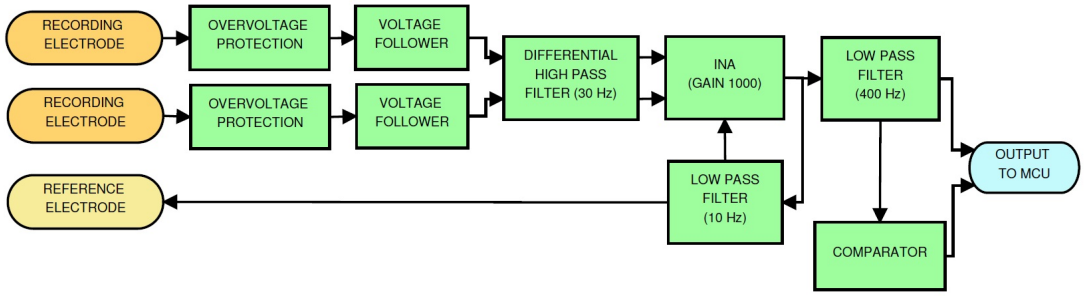

Figure 2.1. Mitor2 Analog Front End block scheme

- 2 Recording Electrodes: the 2 recording electrodes are applied to a point of the muscle where the muscle activity is the strongest.

Voltage and current of the signal acquired are controlled by an overvoltage protection stage and then decoupled with voltage followers.
The signals can now be filtered with a differential High Pass Filter (*HPF*) of about 30Hz to eliminate the contribution of due to the movement artifact. An amplified differential signal is thus obtained by means of an Instrumentation Amplifier (*INA*) with the reference voltage in the middle dynamic. After a Low Pass Filter (*LPF*) stage at about 400Hz the sEMG is finally ready to be sampled from the internal ADC of the microcontroller and thus the first output of the analog front end is obtained.
The same output is used also to obtain the TC signal by means of a comparator and a threshold provided by the digital part.
The focus will be displaced in each stage.

2.1.1 Overvoltage Protection

An overvoltage protection circuit (Figure 2.2) has been inserted to prevent system to be damaged by input voltage spikes over positive power supply of 3.3V.

J1 is a 3 positions connector header, 2 of them are for the sEMG signal and the other one for the output reference. D3 and D4 are TVS Diode (*ESD5Z3.3T1G*) with 3.3V breakdown voltage. They are in charge of suppress all the overvoltages above the positive power supply voltage providing a path to ground for the current.
R1 and R2 are placed to limit the current due to overvoltages to about 10mA

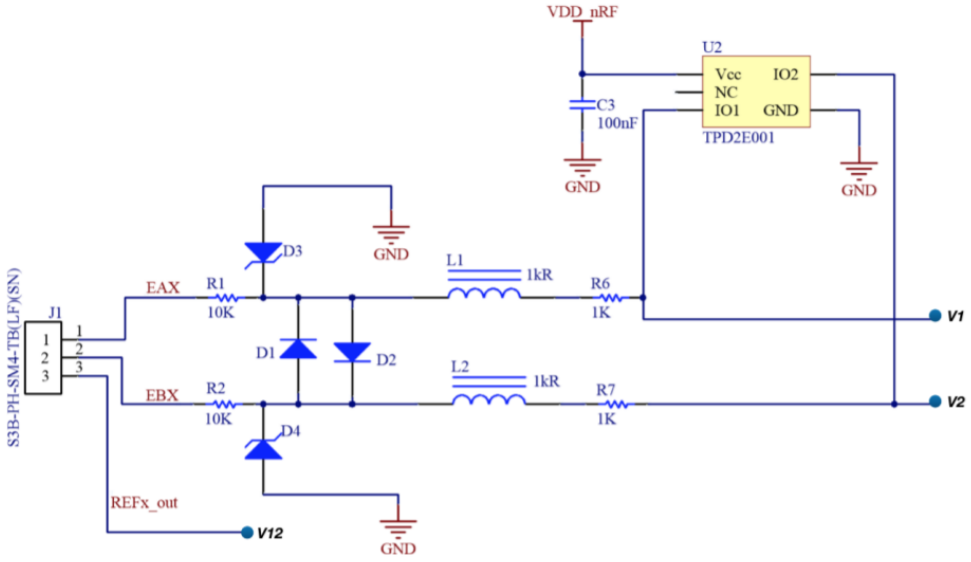

Figure 2.2. Mitor2 Analog Front End Overvoltage Protection circuit

considering a 100V maximum input, infact

$$I_{max} = \frac{100V - 3.3V}{10K\Omega} = 9.67mA \tag{2.1}$$

D1 and D2 are general purpose diodes to prevent the 2 input signal to be too different between them. If they are, they are not sEMG signals.
L1 and L2 are ferrite beads to suppress high frequency ElectroMagnetic Interference (*EMI*) and Radio Frequency Interference *RFI*) electronic noise. They infact act as low pass filter converting radio frequency energy in heat (noticeable only in extreme cases). U2 is based on Electrostatic Discharge (*ESD*) protection diode array.
$100nF$ decoupling capacitor has been placed on the power supply rail.

2.1.2 Voltage Followers

The signals can now pass through a voltage follower to decouple the rest of the circuit (Figure 2.3). Has been chosen a 2 channel chip voltage follower for space optimization. $100nF$ decoupling capacitor has been placed on the power supply rail.

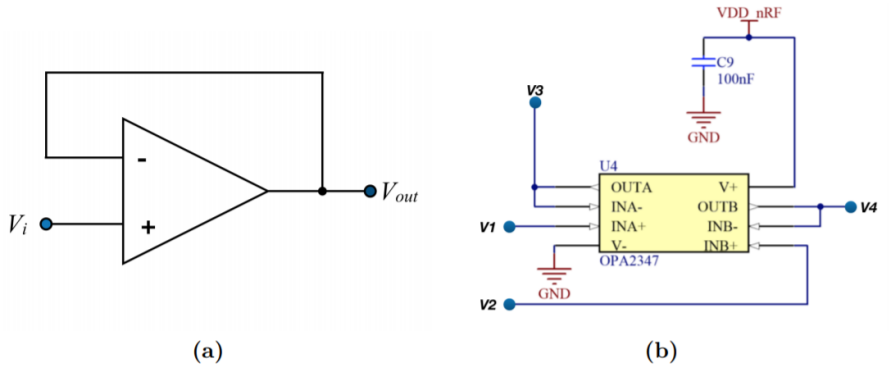

Figure 2.3. a) Voltage follower, b) 2 channel voltage follower

2.1.3 Differential High Pass Filter 30Hz

The 2 signals are now filtered by means of a second order differential high pass filter (Figure 2.4) to attenuate the movement artifact noise.

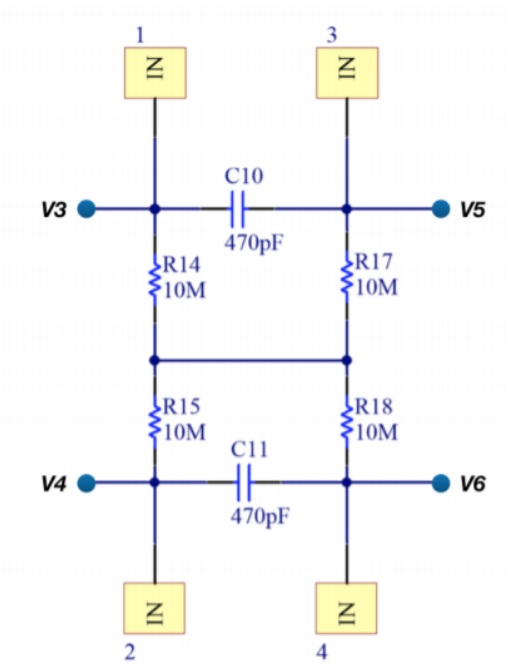

Figure 2.4. Second order passive High Pass Filter 33.86Hz

The cut off frequency of the filter can be calculated as follow:

$$f_{cutoff} = \frac{1}{2\pi RC} \tag{2.2}$$

and thus choosing the write resistor and capacitor cab be achieved the desired bandwidth. In this application has been chosen 470pf as capacitance and 10MΩ as resistance leading to a cut off frequency of 33.86Hz.
Test points are also added for verification purpose.

2.1.4 Instrumentation Amplifier

In this stage an Instrumentation Amplifier (*INA*) is used to amplify the difference between the 2 input signals (Figure 2.5).

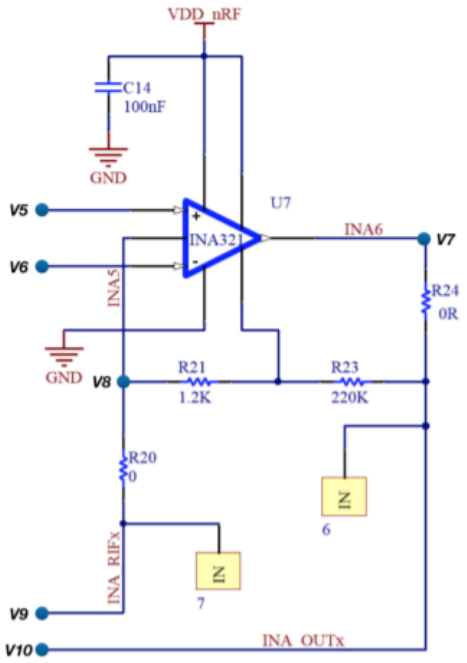

Figure 2.5. Amplification stage, G=922V/V

The one used in this version is the INA321 from Texas Instrument. Its gain can be set by additional resistors, particularly is:

$$G = 5 + 5\frac{R_{23}}{R_{21}} \tag{2.3}$$

Since the sEMG range between less than 50μV up to 30mV, $R_{23} = 220k\Omega$ and $R_{21} = 1.2k\Omega$ have been here chosen leading to a gain of 922V/V. The

0/ohm resistance R_{24} is placed to reconfigure the gain under need.
The INA reference let the amplified differential signal to be centered to a middle dynamic DC voltage and come from LPF of the INA feedback.
In this stage the first issue showed up. When the system is turned on, the INA reference remains stacked at high voltage while the INA output remains stacked at low voltage hiding all the signal. In Mitor2 version this issue is bypassed by placing an analog switch controlled by the microcontroller between the INA reference and output (Figure 2.6).

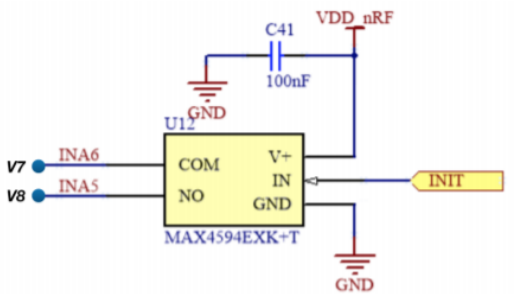

Figure 2.6. Analog Switch between INA reference and output

It is kept open during the normal acquisition and closed for 10ms after 10ms from the power up. Forcing the INA reference and output to the same voltage for the said time let the system start working as it should.
In the section 2.2 this problem is analyzed in detail and solved.
$100nF$ decoupling capacitors have been placed on the power supply rail and test points are also added for verification purpose.

2.1.5 Feedback Low Pass Filter 10Hz

A multiple feedback low pass filter has been used on the INA feedback to eliminate the low frequency component introduced by the INA (Figure 2.7).

Its cut off frequency is given by:

$$f_{cutoff} = \frac{1}{2\pi\sqrt{R_4 R_5 C_2 C_4}} \tag{2.4}$$

Here have been chosen $R_4 = 150k\Omega$, $R_5 = 33k\Omega$, $C_2 = 470nF$, $C_4 = 100nF$, leading to a cut off frequency of 10.43Hz.
In the middle of the bandwidth (almost DC) we can identify two inputs:

- the INA output going through the pin "-" of the OPA.

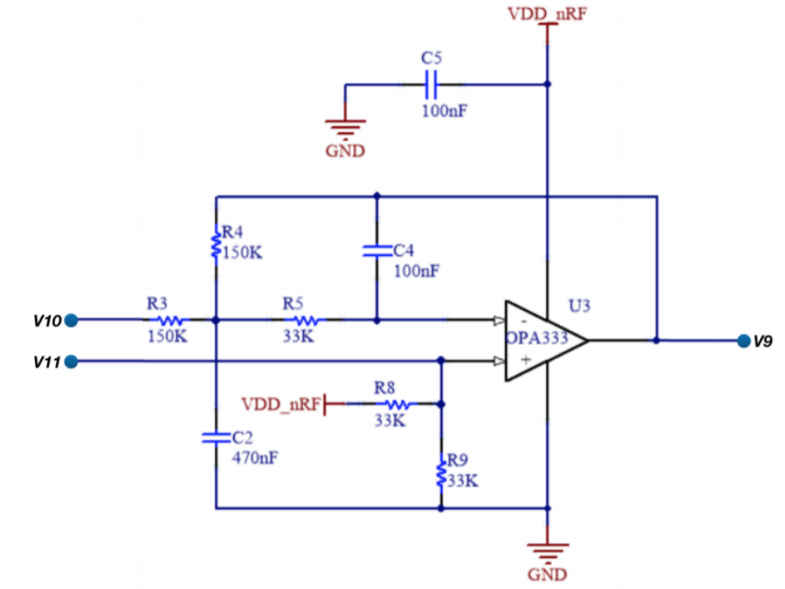

Figure 2.7. INA feedback and Low Pass Filter 10Hz for INA reference voltage generation

- half of the power supply voltage given by a voltage divider with two resistor R_8 and R_9 of 33kΩ.

The INA output sees though an inverting amplifier with gain

$$G_{inv} = -\frac{R_4}{R_3} = -1 \tag{2.5}$$

while the DC input sees a non-inverting amplifier with gain

$$G_{non-inv} = 1 + \frac{R_4}{R_3} = 2 \tag{2.6}$$

The output of this stage is thus

$$V_{INAref} = V_{INAout}Ginv + \frac{VDD_{nRF}}{2}G_{non-inv} = 2\frac{VDD_{nRF}}{2} - V_{INAout} \tag{2.7}$$

The output of this stage is the input of the INA reference. The more increases the INA reference, the more increases INA output. On the other hand when V_{INAout} increases, V_{INAref} decreases. Consequently V_{INAref} and V_{INAout} will follow a dumped oscillation, in opposite way, around middle dynamic stabilizing to it.
Two issued showed up in this stage both related to generation of the voltage suppling the "-" pin:

- The voltage suppling "-" is not exactly $\frac{VDD_{nRF}}{2}$ because of the tolerance of R_8 and R_9. This implies also that each slave has its own reference voltage;
- Fluctuation of power supply is reflected on the reference influencing the signal.

Both issues are analyzed and solved in the section 2.3. $100nF$ decoupling capacitor has been placed on the power supply rail.

2.1.6 Driven Right Leg

The middle dynamic voltage generated in the INA loopback filter by the voltage divider feeds also the reference electrode through a Driven Right Leg (DRL) (Figure 2.8).

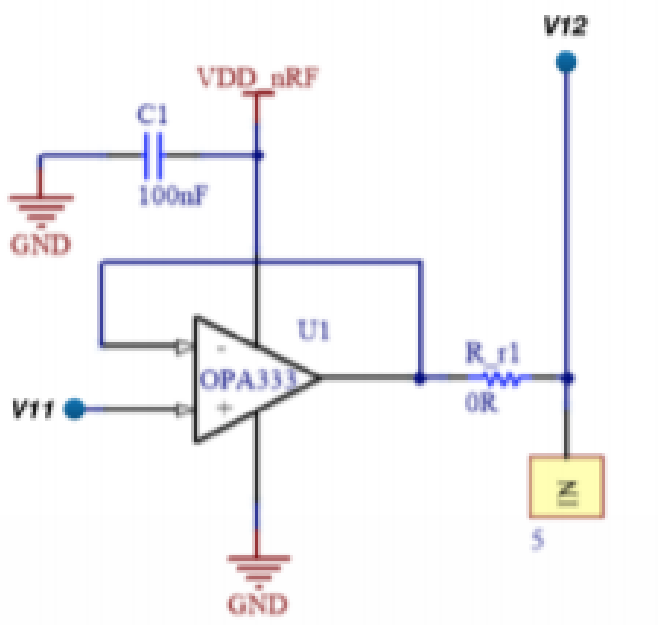

Figure 2.8. Driven Right Leg circuit

It active drive the body to a known voltage that is half of the power supply. The 0Ω resistance is here for the possibility to be substituted with an higher value to limit the current flowing. $100nF$ decoupling capacitor has been placed on the power supply rail and a test point are also added for verification purpose.

2.1.7 Sallen-Key Low Pass Filter 400Hz

A second order Sallen-Key low pass filter is here placed (Figure 2.9 to eliminate the frequency over than 400Hz which are not part of the EMG signal.

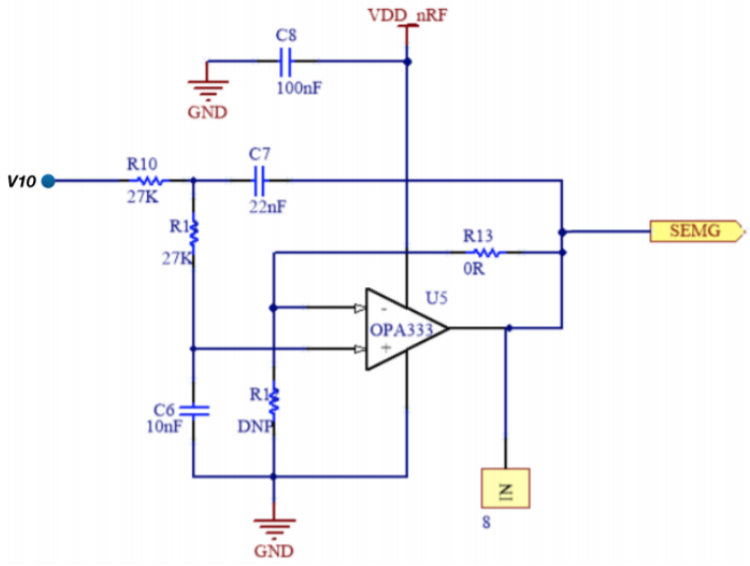

Figure 2.9. Driven Right Leg circuit

The cut off frequency is given by:

$$f_{cutoff} = \frac{1}{2\pi\sqrt{R_{10}R_{14}C_6C_7}} \tag{2.8}$$

Here $R_{10} = R_{14} = 27k\Omega$, $C_6 = 10nF$, $C_7 = 22nF$ and thus $f_{cutoff} = 397Hz$. Do Not Populating (DNP) R_{12} and fixing R_{13} to 0Ω, here is obtained the configuration for unity gain but the possibility to have a different gain is available by sizing the 2 resistor, infact:

$$G = 1 + \frac{R_{13}}{R_{12}} \tag{2.9}$$

The output of this stage is the sEMG signal that is the input of the microcontroller ADC. The output drives also the next stage that generates the Threshold Crossing signal. $100nF$ decoupling capacitor has been placed on the power supply rail and a test point are also added for verification purpose.

2.1.8 Comparator

To obtain the Threshold Crossing signal a comparator and a threshold is needed (Figure 2.10a). The comparator has been closed in a feedback to obtain a Schmitt Trigger.

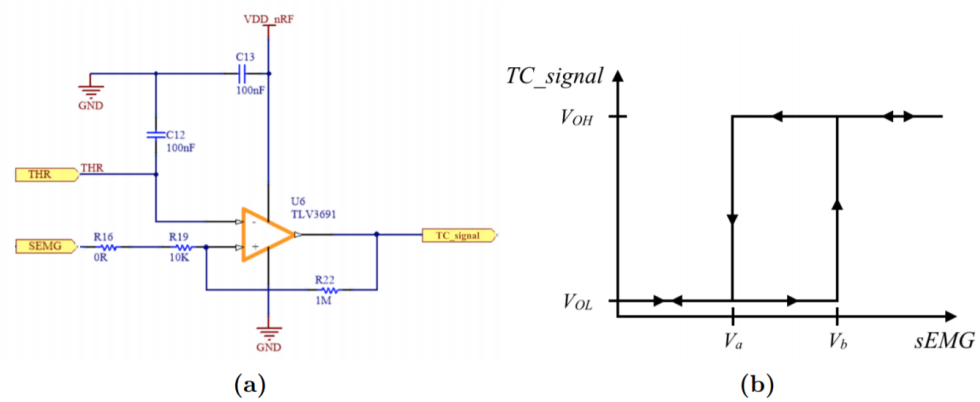

Figure 2.10. a) Comparator in Schmitt Trigger configuration, b) Output Hysteresis curve

Hysteresis on output is infact needed to eliminate the threshold crossing due to the noise. The hysteresis around V_{THR} is:

$$\Delta V_{Hysteresis} = \frac{R_1 9}{R_2 2} VDD_{nRF} = 10mV \tag{2.10}$$

The 0Ω resistance R_{16} is placed here for the possibility to increase the hysteresis if needed.
The TC signal feeds a microcontroller input where a counter is instantiated. $100nF$ decoupling capacitor has been placed on the power supply rail.

2.2 INA Saturation Issue

In this section the INA saturation issue is presented and analyzed following all the steps done to individuate the cause of the problem. Two solutions are proposed and one of them is used for the new prototype version.

2.2.1 Background

Different versions of the analog front end have already been prototyped and, in the course of their realization, a curious issue showed up.
The first version of the AFE had 4 separated channels that could be used also as stand alone ones (Figure 2.11).

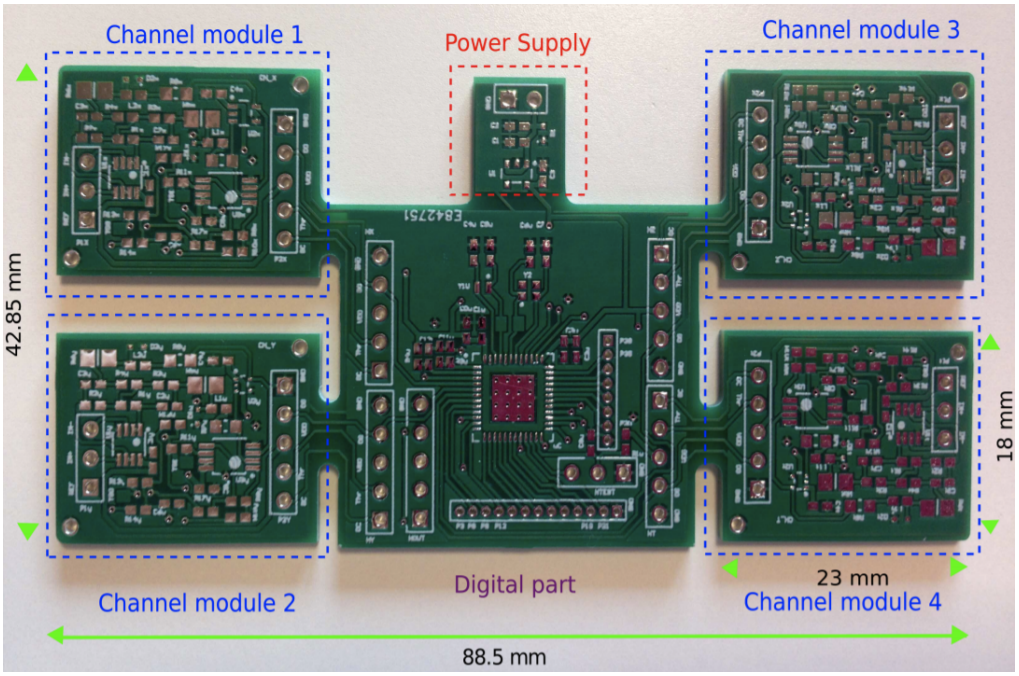

Figure 2.11. First acquisition system prototype

The board was produced bared by the manufactured and then the components were soldered with a reflow soldering process in the Politecnico di Torino.
Of this board, 1 of the 4 channels worked properly while the other 3 presented a issue. Infact in the 3 corrupted boards, when the system is turned on, the INA321 reference remains stacked at high voltage while the INA output remains stacked at low voltage hiding all the signal. From this point on,

the next versions of this system preserved a similar AFE structure and in some board the issue showed up while in others did not.
Experimentally have been seen that if a short circuit is created between the INA reference and output re-establishing the two voltages at the same value for a small time, the system restart to work properly.
In the last version this issue is bypassed by placing an analog switch controlled by the microcontroller between the INA reference and the INA output. The presence of the switch fixes the issue at start up but a solution for issue showing up during normal usage has not been implemented considered. Furthermore the switch need to be controlled by the microcontroller introducing power consumption due also to the its computation and additional space. The best solution is solve the problem from the origin.

2.2.2 Investigation

Known this background and excluded soldering problem, the investigation of the issue started analyzing the signal propagation with the oscilloscope on the last version of system (Figure 2.12).

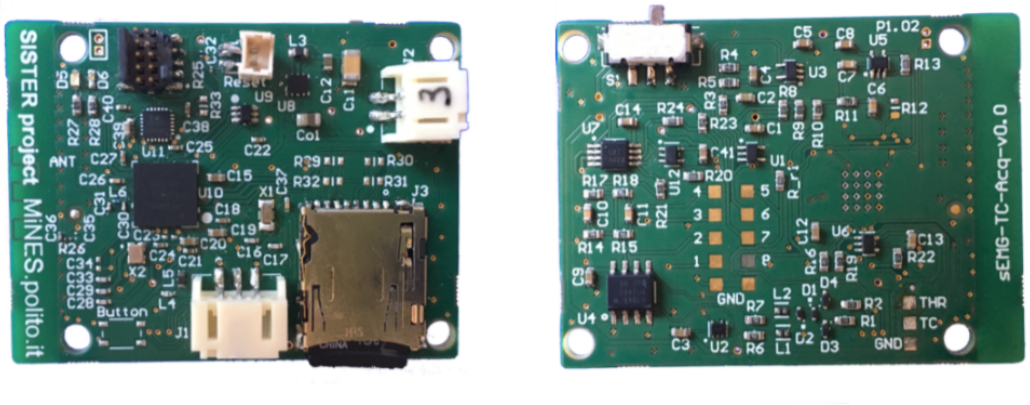

Figure 2.12. Mitor2 slave: Top side (*left*) is reserved for the digital part and bottom side (*right*) is reserved for the analog part

The analysis showed that sEMG signals propagate correctly until the INA inputs while the INA output is corrupted (Figure 2.13).

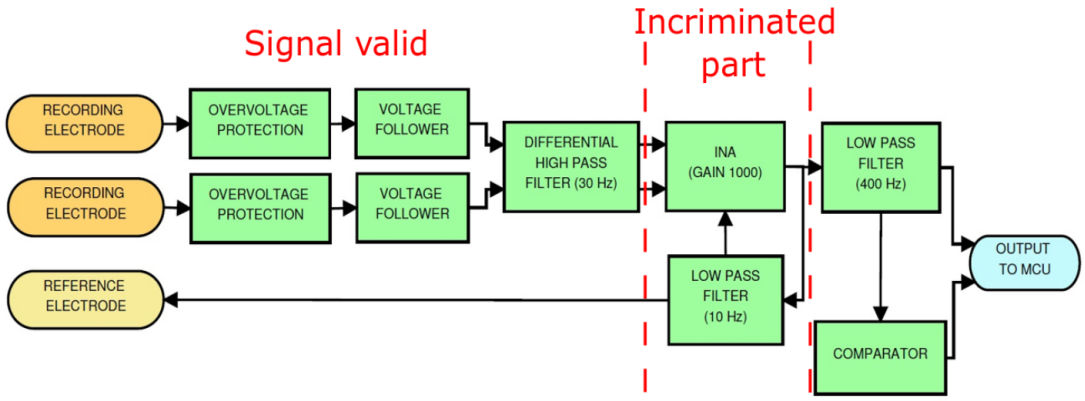

Figure 2.13. Saturation Issue incriminated part

The analog front end has then been replicated entirely in LTSpice (Figure 2.14).

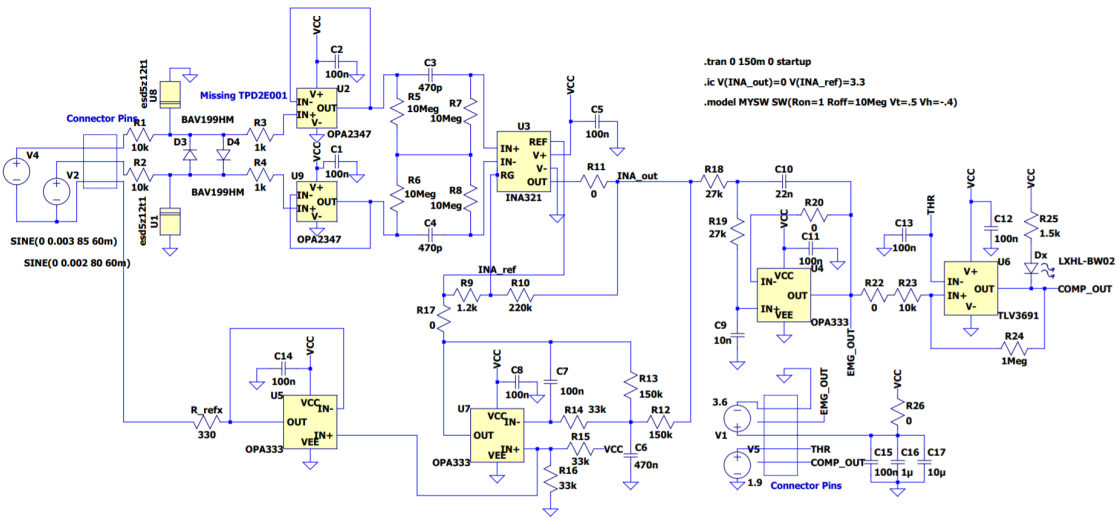

Figure 2.14. Analog Front End LTSpice circuit for deeper investigation

For each Integrated Circuit (*IC*) the LTSpice netlist has been downloaded from the manufacturer website and the component has been created. These netlist does not represent accurately the IC behaviour but a quite approximated one. The simulation, infact, seemed to give correct results and showed no issue related to the INA saturation. Apparently, infact, there is no reason

why the INA output should give a constant low value if its voltage reference is high. INA output should have the reference as DC voltage.
The attention was thus focused on the INA loop (Figure 2.15) and, to force the real situation in the simulation, the INA reference was set to high voltage and the behaviour was observed (Figure 2.16).

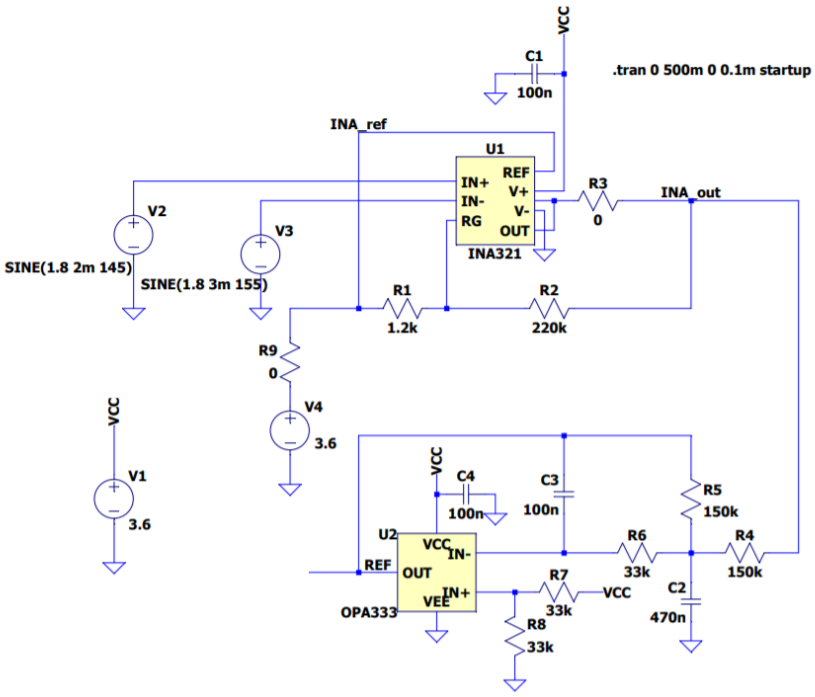

Figure 2.15. INA loop with INA reference forced to high voltage

As inputs 2 sin waves out of phase were chosen, the first with $f_1 = 145Hz$, $V_{ac1} = 2mV$, $V_{DC1} = 1.8V$ and the second with $f_2 = 150Hz$, $V_{ac1} = 3mV$, $V_{DC1} = 1.8V$. The expected output signal saturating when the first sin wave is greater than the second and a rail to rail curve otherwise. The output observed is instead about $180mV$, it suggested that something inside the INA321 was wrong.
The next step was deeper analyzed the INA321 datasheet and what has been revealed is that the INA reference must be $1.2V$ under the positive power supply rail (Figure 2.17).

Figure 2.16. LTSpice INA output when reference forced to high voltage

APPLICATIONS INFORMATION

The INA321 is a modified version of the classic *two op amp* instrumentation amplifier, with an additional gain amplifier.

Figure 1 shows the basic connections for the operation of the INA321 and INA2321. The power supply should be capacitively decoupled with 0.1µF capacitors as close to the INA321 as possible for noisy or high-impedance applications.

The output is referred to the reference terminal, which must be at least 1.2V below the positive supply rail.

Figure 2.17. INA321 Datasheet showing reference voltage constraint

At startup, for a finite time, the INA output is low. The INA output is the input of the feedback low pass filter at 10Hz. In section 2.1.5 have been

seen that the INA reference is:

$$V_{INAref} = 2\frac{VDD_{nRF}}{2} - V_{INAout} \tag{2.11}$$

Of course if $V_{INAout} = 0$, $V_{INAref} = VDD_{nRF}$. The datasheet constraint is thus not been satisfied and the INA321 stops working properly driving the output low and remaining stacked in this situation.

2.2.3 Solutions

The first solution that will confirm the thesis and that can be tested also on the boards is to find a way to force the INA entirely to not enter in this stack. The immediate idea was thus to place some diodes in parallel to the INA reference to prevent the reference to exceed the its safe range (Figure 2.18). The output is reported in Figure 2.19.

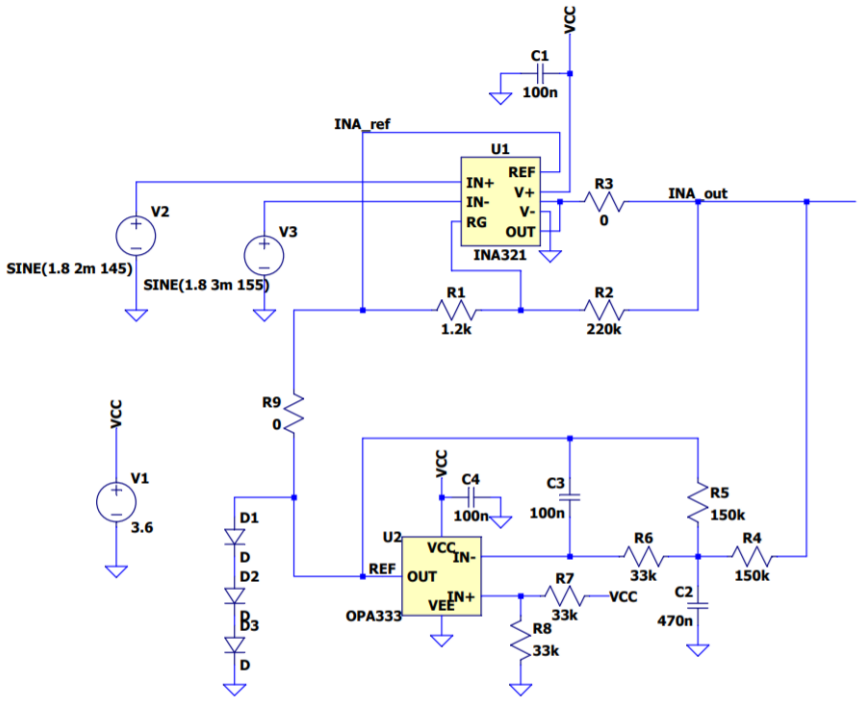

Figure 2.18. INA loop with parallel diodes to prevent the reference to exceed the safe range

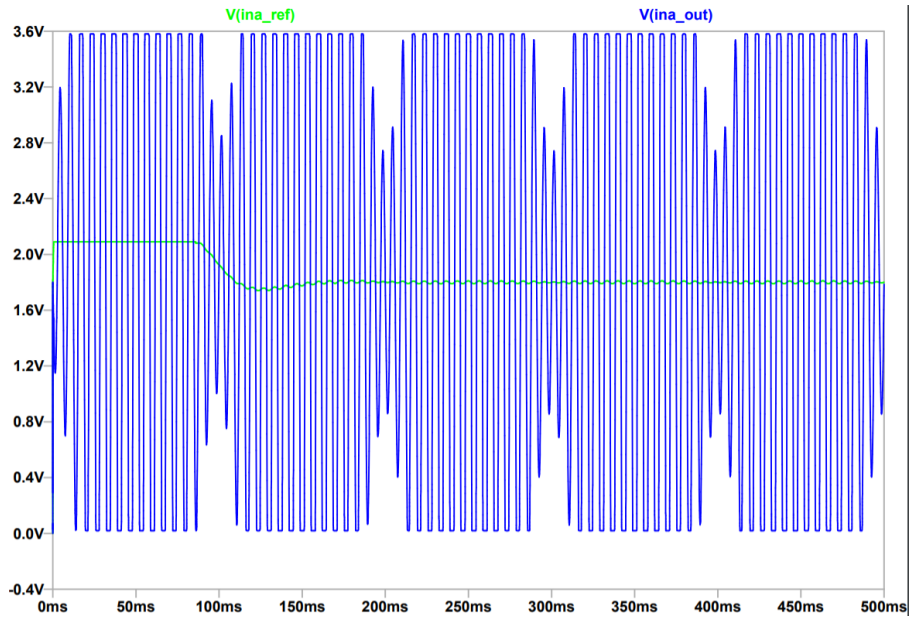

Figure 2.19. INA321 Datasheet showing reference voltage constraint

It can been seen from the graph that at start up the reference voltage tries to reach the high voltage but is stopped by the parallel diodes letting the system to not enter in the critic situation. This solution is also been successfully tested on different acquisition channel boards that are present our laboratory.
This solution let the precedent prototypes work correctly but it introduce addition space and some power consumption for the current flowing in the diodes at startup. The definitive solution adopted is the choose of another Instrumentation Amplifier with no reference constraint. INA333 was chosen (see section 2.4.1).

2.3 Periodic Drop Out Issue

In this section the period drop out issue is presented and analyzed. The measures taken to prevent its manifestation in the next version are thus proposed.

2.3.1 Background

The last versions of the SISTER project embed a micro SD card to store the sEMG data, its envelope or the TC data acquired according to the working mode that have been set in the system. The data are stored in microcontroller internal buffers and when one of these if full the data is transferred in the SD. During the writings the SD requires a peak of current (about 100mA in the precedent version of the board) that cause a power supply voltage drop out that is sensed by all the components (Figure 2.20).

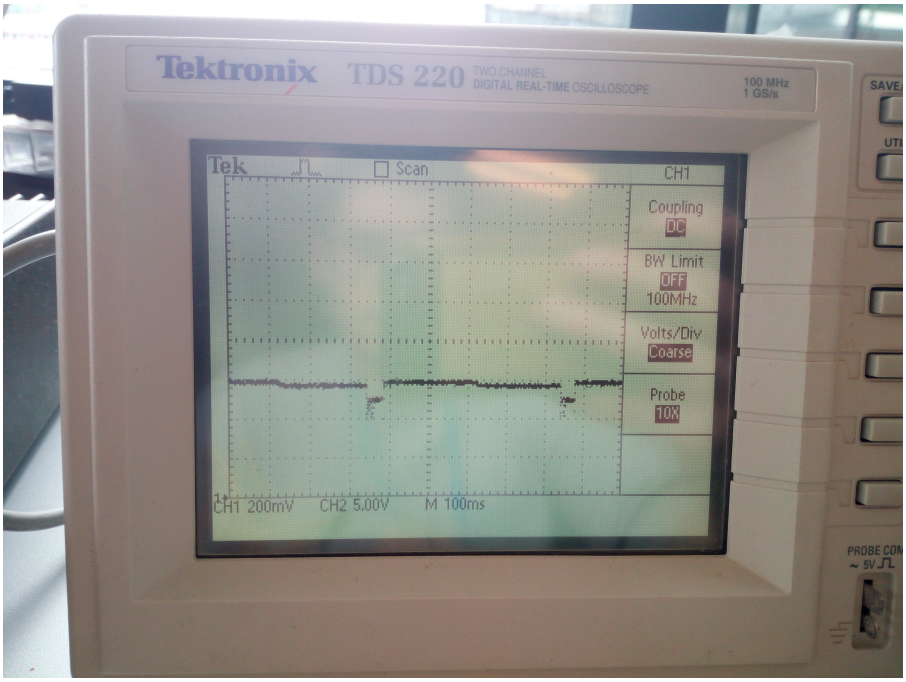

Figure 2.20. Dropout voltage on the INA reference during the SD periodic writings

In the analog front end, the INA voltage reference is generated indirectly by the voltage divider in the INA low pass filter (Figure 2.21).

By the way in which the reference is generated, every variation in the power supply is sensed by the voltage reference influencing the INA output and thus the signal acquired. In Figure 2.22 can be seen the effect of this phenomenon during rest time in which the muscle activation is not presented and the signal acquired is only the baseline. Periodic peak of about 100mV can be seen every half second, that is the period between an SD writing and the other.

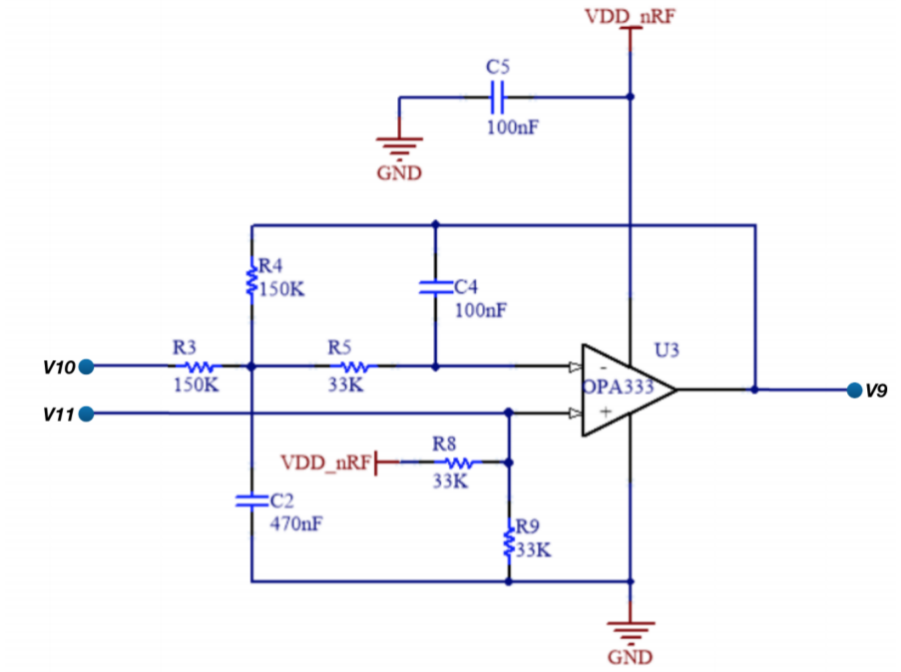

Figure 2.21. Focus on the voltage divider R8,R9 for the INA voltage reference generation

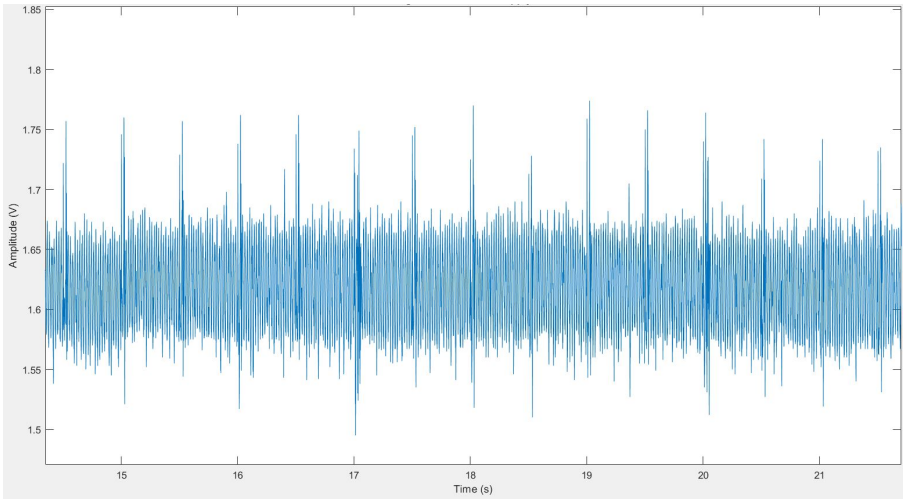

Figure 2.22. Baseline of sEMG signal acquired influenced by power supply dropout voltage during the periodic SD writings

2.3.2 Solutions

The power supply drop out voltage can be due to different causes:

- The voltage regulator to stabilize the battery voltage is not able to drive a 100mA load;
- The battery is not able to provide 100mA of pulse current;
- The board layout shows up inductive and resistive phenomena.

Voltage Regulator

The regulator used is from the *TPS61099x* family. From its datasheet can be seen that with 3.6V input, when the load is greater than 10mA the output voltage suffers of about 100mV drop out (Figure 2.23). To face this issue a different voltage regulator has been chosen for the next version (section 2.4.6).

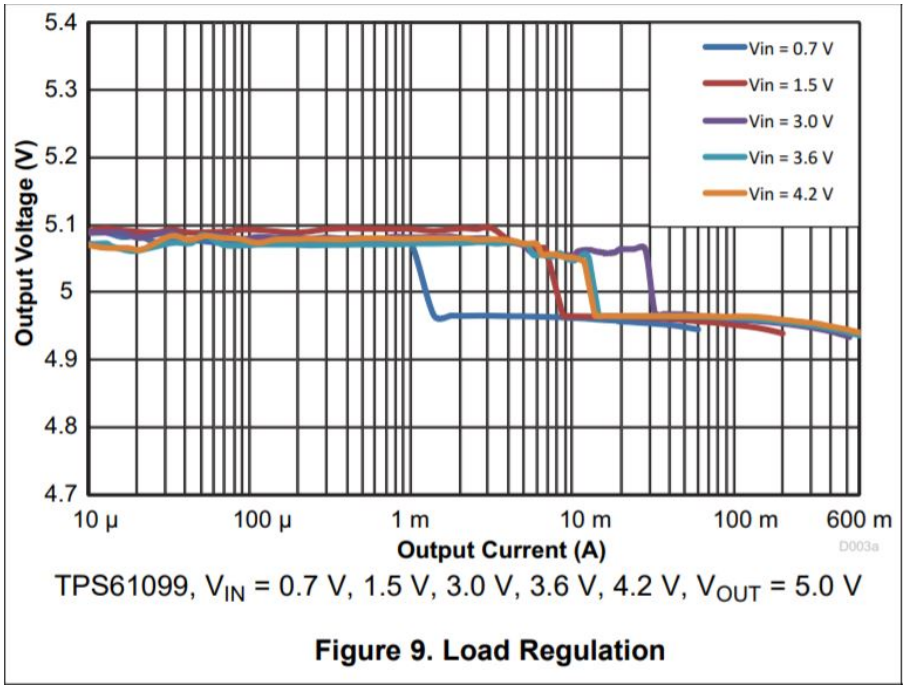

Figure 2.23. TPS61099x datasheet load regulation: Output Voltage vs Output Current

Battery

About the battery, the amper hour battery capability is not a measure of the maximum pulse discharge current capability that is a parameter often omitted from the batteries datasheet if it is not good enough. The battery used in the probematic version is a Lithium Thionyl Chloride cells coin battery from Tadiran. Its pulse discharge current capibility is 10mA as can be seen from the datasheet (Figure 2.24), not enough for this system. A different battery is chosen for the next version (section 2.4.8).

Performance Data
(Typical values for batteries stored at +25 °C for one year)

System	Lithium Thionyl Chloride
Nominal voltage	3.6 V
Nominal capacity	0.42 Ah
Nominal current	0.5 mA
Max. continuous discharge current	5 mA
Pulse current capability	10 mA
Anode surface area	2.4 cm^2
Lithium content	0.13 g
Weight	6 g
Volume	2.1 cm^3
Temperature range	–55 °C ... +85 °C

Figure 2.24. Lithium Thionyl Chloride cells coin battery from Tadiran datasheet

Parasitic Phenomena

To reduce to the minimum the inductive and resistive phenomena, the SD power supply trace have been drawn wide enough and kept as short and close as possible to the voltage regulator (section 3.4.2). Capacitors with different values are placed close to the SD card VDD pin to provide an immediate current source. An high side power switch is thus placed in the power supply trace, near the SD, to extend the capacitors charging time reducing thus the peak current (section 3.3.3).

Voltage Reference

Finally a voltage reference has been chosen (section 2.4.4) to generate the INA reference and substitute the voltage divider in Figure 2.21 so sensitive

to the power supply fluctuation.

2.4 Off The Shelf Changes

Component changes have been performed to select ultra low power components to reduce as much as possible the hardware power consumption. In this section each choice has been reported highlighting the parameters mostly taken into account for each component. The goal is to select the components with the lowest quiescent current I_q. It is the current consumed by the component while there is no load and thus when it is in a quiescent state. Often better I_q implies a worsening of the other parameters, thus each decision taken is the result of a trade off between the component characteristics.
Some components have been kept unchanged for different reasons:

- The microcontroller nRF52840 was previously selected because of its low power characteristic. Furthermore the most part of the firmware was already developed for it;
- the DAC AD5621 because it already had good performances;
- the comparator TLV3691 because is already a nanopower one;
- the leds because are only for a visual verification purpose and can be switched off.

Components that lead to structural changes are also selected in this section:

- 1.25V Voltage Reference: substitutes the voltage divider in Figure 2.21 and it is selected to 1.25 for its extremely low quiescent current with respect to other references (section 2.4.4);
- 2.5V LDO: is inserted to regulate the analog front end power supply voltage and keep the 1.25V INA reference voltage to middle dynamic (section 2.4.5);
- Switch SPST: is inserted to generate a programmable gain stage with a non-inverting amplification configuration. It was preferred to a Programmable Gain Amplifier (PGA) for its extremely reduced power consumption (section 2.4.3).

2.4.1 Instrumentation Amplifier

An instrumentation amplifier is a differential amplifier with high input impedance and, regularly, have gain adjustable by changing just an external resistor (in Figure 2.25 the classic structure).

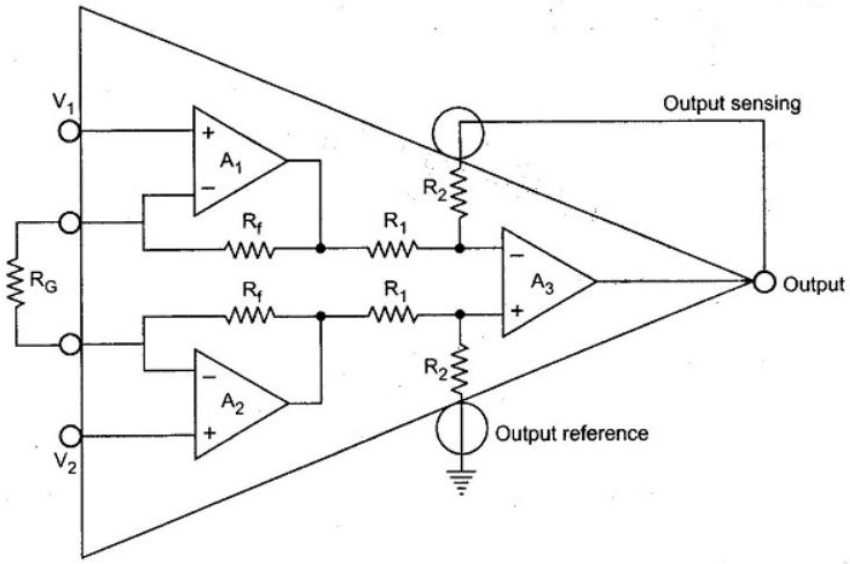

Figure 2.25. Instrumentation amplifier classic structure. Gain adjustable by changing R_G

It is used in the first amplification stage. The INA321 precedently used has an unusual instrumentation amplifier structure (Figure 2.26) and showed problems related to the reference voltage range (section 2.2). It was selected for its low quiescent current ($60\mu A$ maximum) but it is clear that it need to be changed.

Other than the quiescent current, the parameters taken into account for the choice of the substitute component are:

- Bandwidth: the signal to be processed has (30,400)Hz bandwidth thus we want a bandwidth greater than 400Hz;
- CMRR: the Common Mode Rejection Ratio because of course no other offset than the voltage reference need to be in the output signal;
- Input/Output Voltage Range: the signal have to be rail to rail amplified to obtain the best possible Signal to Noise Ratio (SNR);

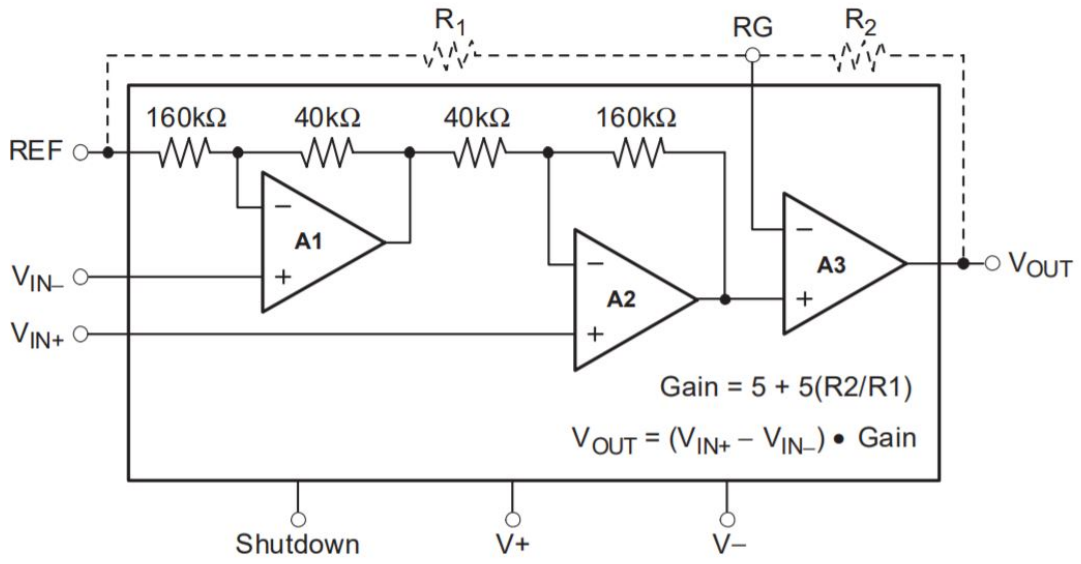

Figure 2.26. INA321 internal structure and gain

- Power Supply Range: the component need to support 2.5V power supply;

- Gain: there is flexibility on this parameter because a second amplification stage will be inserted (section 3.2.2).

The low power rail to rail instrumentation amplifiers have been selected and reported in table 2.1.

In term of power consumption, the best INA is the AD8236 but it can achieve an amplification of just 200 with a bandwidth of 400Hz that is not actually enough since at this cut off frequency the signal loses already 3dB. Furthermore the second amplification stage is programmable and it ranges from 1 to 6 V/V gain thus, since the sEMG signal is about in the range $50\mu V$ to few mV, a first amplification stage of 200V/V is not the best. The INA333 is the second best in term of power consumption. With an amplification of 1000V/V it has a maximum bandwidth of 350Hz that is out of the sEMG signal range. Reducing its gain to 500V/V the bandwidth increase to 700Hz that is enough for this application. It has also a 100dB CMRR and is thus the component selected to substitute the INA321 even though the quiescent current increases by $15\mu A$.

Name	I_q μA	CMRR dB	Gain V/V	BW Hz	Supply V
INA321	60	80	[5,1000]	1000	(2.7, 5.5)
INA333	75	100	[1,1000]	350	(1.8, 5.5)
INA122	85	65	[1,10k]	300	(2.2, 36)
LT17810	95	94	[10,1000]	1500	(2.5, 36)
AD627	85	83	[5,1000]	400	(1.1, 18)
AD8236	40	100	[5,200]	400	(1.8, 5.5)
AD8237	130	114	[1,1000]	1000	(1.8, 5.5)
EL817x	110	100	[10,1000]	13000	(2.4,5.5)
EL8176	90	90	[1,1000]	1000	(2.4,5.5)

Table 2.1. Instrumentation Amplifiers table

2.4.2 Operational Amplifier

Six operational amplifiers (Figure 2.27) are used in the analog front end:

- 3 in a buffer configuration. Among them 2 on the input signals and one on the DRL output;
- 1 in the 10Hz second order active low pass filter in the INA feedback;
- 1 in a non inverting configuration for the second amplification stage;
- 1 for the 400Hz Sallen-Key low pass filter.

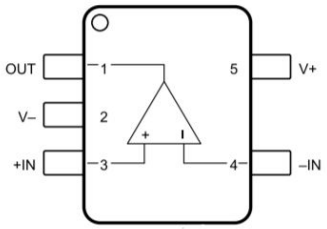

Figure 2.27. Operation Amplifier Component

The parameters to select the operational amplifier, other than the quiescent current, are

- the Gain Bandwidth product (GBW) for the one in the non inverting configuration of the second amplification stage. It reaches a gain of 6, thus a $GBW > 400Hz * 6 = 2.4kHz$ is needed;
- the Slew Rate (SR) for the 400Hz Sallen-Key low pass filter after the amplification chain. At this stage the signal could be rail to rail, thus considering a maximum frequency of 400Hz and a peak voltage of 1.25V around 1.25V reference (the analog power supply is 2.5V), the $SR > \frac{2\pi * 400Hz * 1.25V}{1000} = 3.14V/ms$;
- the output swing need to be robust with respect to the current load to drive;
- low voltage noise density;
- low output voltage offset;

- high common mode rejection ratio;
- high power supply rejection ratio.

The OPAs to be substituted are OPA333, they consumes $25\mu A$ of quiescent current each. The LPV821 consumes $0.79\mu A$ quiescent current, has a GBW product of 8kHz, a SR of 3.3V/ms and an offset of 0.01mV. It has been chosen for the second amplification stage, the Sallen-Key LPF, the INA feedback LPF and the DRL. The 2 channels TLV8542 has instead been selected for the two buffer on the input signals to reduce the space. It has $1.28\mu A$ quiescent current, 8kHz GBW product, 3.5V/ms SR, 3.4mV offset that will be eliminated through the INA.
The choice of this 6 new OPAs lead to a saving of $145{,}56\mu A$.

2.4.3 Switch SPST

A four channel Single Pole Single Throw (*SPST*) Switch (Figure 2.28) has been inserted to achieve a programmable gain, along with a non inverting amplifier, in the second amplification stage (section 3.2.2).This solution has been preferred with respect to a PGA because it consumes unless $170\mu A$. For the choice of the switch, important parameters others than the quiescent current are the resistance when the switch is closed R_{ON} (wanted as small as possible) and the leakage current.

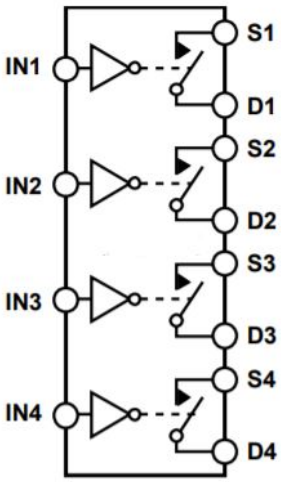

Figure 2.28. 4 Channel Switch SPST structure

The one selected is the ADG711 with a quiescent current of 1nA, an R_{ON} of 2.5Ωand a leakage current of 0.1nA.

2.4.4 Voltage Reference

A Voltage Reference (Figure 2.29 has been introduced to have a more stable and known INA reference voltage. A voltage generated with a voltage divider is infact affected by the resistors tolerance that make the reference of each board different and furthermore reflects all the power supply fluctuation generating a signal that is not stable.

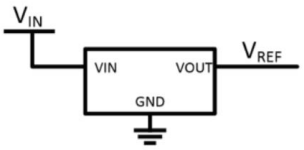

Figure 2.29. Voltage Reference symbol

A shunt voltage reference (Figure 2.30) acts as a Zener Diode. The voltage drop across the component is constant after it reaches a minimum operating current. The current needed is generally higher than the series voltage reference one. Furthermore it requires also an external resistor to set the total supply current. It is better for an application with an high input range.

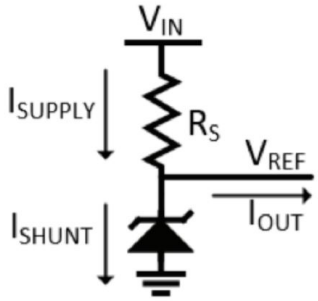

Figure 2.30. Shunt Voltage Reference structure

In this application a series voltage reference has thus preferred. 1.65V would be the voltage to be preferred but voltage references to generate it consumes about $360\mu A$. The most efficient in term of consumption is the LT6656 that consumes only $1.5\mu A$ and generate a voltage of 1.25V. The

savings are huge and it has thus been selected for this application. To keep the signal at middle dynamic, the acquisition module power supply needs to be reduced to 2.5V. (section 2.4.5).

2.4.5 Analog Front End Voltage Regulator

Since to save 2 order of magnitude of quiescent current a 1.25V voltage reference has been chosen, a Low Drop Out (*LDO*) voltage regulator need to be placed to supply the analog acquisition channel and keep the signal to middle dynamic. An LDO (Figure 2.31) has been chosen because a buck-boost regulator is already present in the main board power management unit.

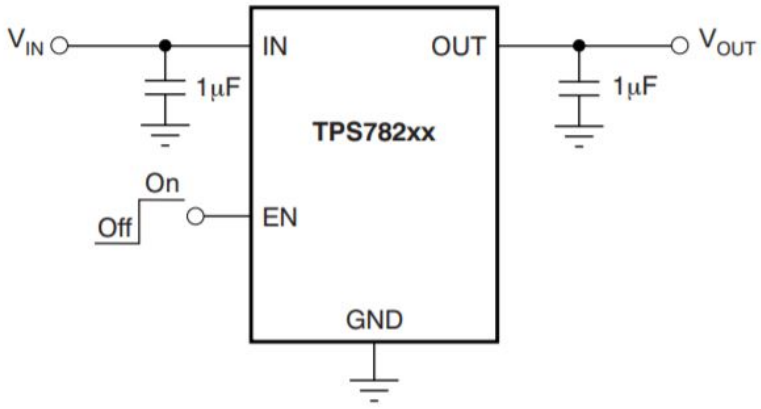

Figure 2.31. Low Drop Out voltage regulator

Th one selected is the TPS782 that has a maximum quiescent current of $1.3\mu A$. The combination of the voltage reference and the LDO consumes thus $2.8\mu A$. The precedent voltage divider had 2 33kΩresistors and 3.6V power supply, thus a current of $I = \frac{3.6V}{33k\Omega+33k\Omega} = 55\mu A$.
A saving of $52\mu A$ along with a reference voltage free from fluctuation is thus obtained.

2.4.6 Voltage Regulator Main Board

The voltage regulator to be substituted is the TPS610995. It consumes only $1.5\mu A$ but has problems driving mA of current as shows in section 2.3. It is a 3.6V boost voltage regulator.

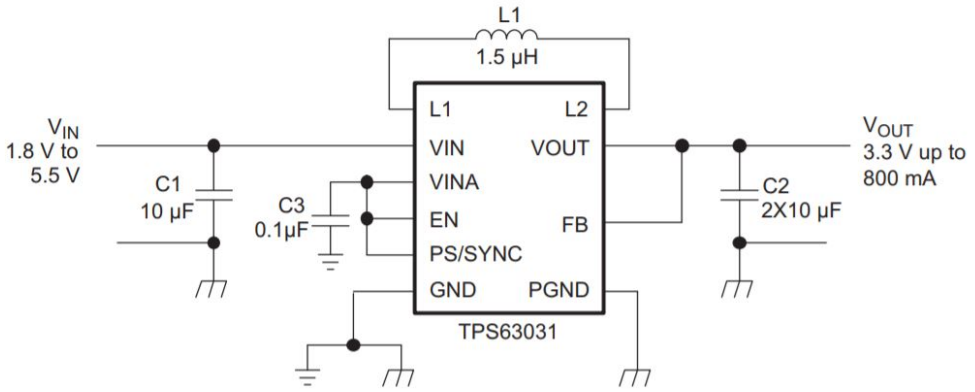

Figure 2.32. Buck-Boost voltage regulator

The voltage regulator selected is the fixed 3.3V buck-boost voltage regulator TPS63031 (Figure 2.32). It does not have the TPS610995 drop out problem at the cost of $41/muA$ current.

2.4.7 Micro SD Card

The SD card has huge current consumption with respect to the other components. In active mode (during writings and readings) its consumption is in the order of hundred of mA. For this reason the writings sessions are not contiguous but the data are accumulated and then burst writings occur. The micro SD card to be substituted is a SanDisk with about 100mA current consumption in active mode. The one selected is an 8GB Apacer (Figure 2.33) with 50mA current consumption in active mode and $100\mu A$ in idle mode.

Figure 2.33. Apacer micro SD card

2.4.8 Battery

The battery need to be chosen properly since the 50mA pulse discharge current required by the SD writings. The one to be substituted is a Tadiran battery whose maximum pulse discharge current is 10mA (Figure 2.34), not enough for the application.

Performance Data
(Typical values for batteries stored at +25 °C for one year)

System	Lithium Thionyl Chloride
Nominal voltage	3.6 V
Nominal capacity	0.42 Ah
Nominal current	0.5 mA
Max. continuous discharge current	5 mA
Pulse current capability	10 mA
Anode surface area	2.4 cm^2
Lithium content	0.13 g
Weight	6 g
Volume	2.1 cm^3
Temperature range	–55 °C ... +85 °C

Figure 2.34. Lithium Thionyl Chloride cells coin battery from Tadiran datasheet

Unfortunately most of the batteries from the commercial suppliers like Digikey and Mouser are from the United States and their shipment is restricted to that country since they cannot fly. The choice thus becomes restricted accordingly.
Small size electrochemical technologies able to provide a big amount of current in a small time are especially the Lithium Sulphur Dioxide ($LiSO_2$) and the Plus Pulse Battery. They are extremely rare and can be purchased from batteries supplier company only in high quantity.
The Lithium Thionyl Chloride ($LiSOCl_2$) batteries are less rare and are made to last long period of time, providing also a good maximum pulse discharge current. The one selected for this application is the LS14500 from SAFT that provides a maximum pulse discharge current of 250mA (Figure 2.35).

	LS 14500
Cell size	AA
Cell construction	Bobbin
Nominal voltage	3.6 V
Nominal capacity	2.6 Ah
Max. continuous current	50 mA
Max. pulse discharge rate	0.25 A
Max. outside diameter	14.55 mm
Max. height	50.3 mm
Typical weight	16.7 g
Operating temperature range	- 60 / + 85°C

Typical values relative to cells stored for one year or less at + 30°C max ; Performances vary according to discharge characteristics (current, duration, frequency), temperature conditions, storage conditions prior to usage and applications acceptable minimum voltage.

Figure 2.35. Lithium Thionyl Chloride ($LiSOCl_2$) LS14500 datasheet

2.5 Breadboard Prototype

Samples of the new selected SMD components have been ordered. They were thus soldered in the appropriate socket in order to assemble them in a breadboard. A breadboard prototype of the core of the analog acquisition channel have been developed to verify the correct response of it. The block scheme of the part assembled in the breadboard is reported in Figure 2.36 and the resulting circuit is in Figure 2.37.

In vivo test wanted to be performed to have an idea of the gains to be introduced in the programmable gain stage. With the help of a MSP430FR5969 Launchpad (Figure 2.38) and Matlab on a PC, the signal processed by the breadboard circuit has been sampled and graphed.

Particularly the launchpad have been programmed to sample an analog signal and send those samples by UART and through the eZ-FET on-board emulator to the PC. The breadboard/MSP430FR5969 system is reported in Figure 2.39.

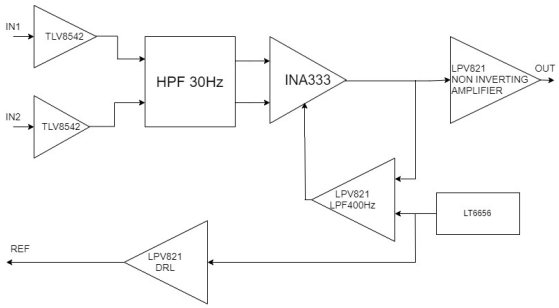

Figure 2.36. Breadboard Prototype Analog Acquisition Channel

Figure 2.37. Analog Acquisition Channel Breadboard Prototype

Running on a PC, Matlab reads the samples from the serial port and graphs the raw data and its Power Spectrum Density (*PSD*). In Figure 2.40

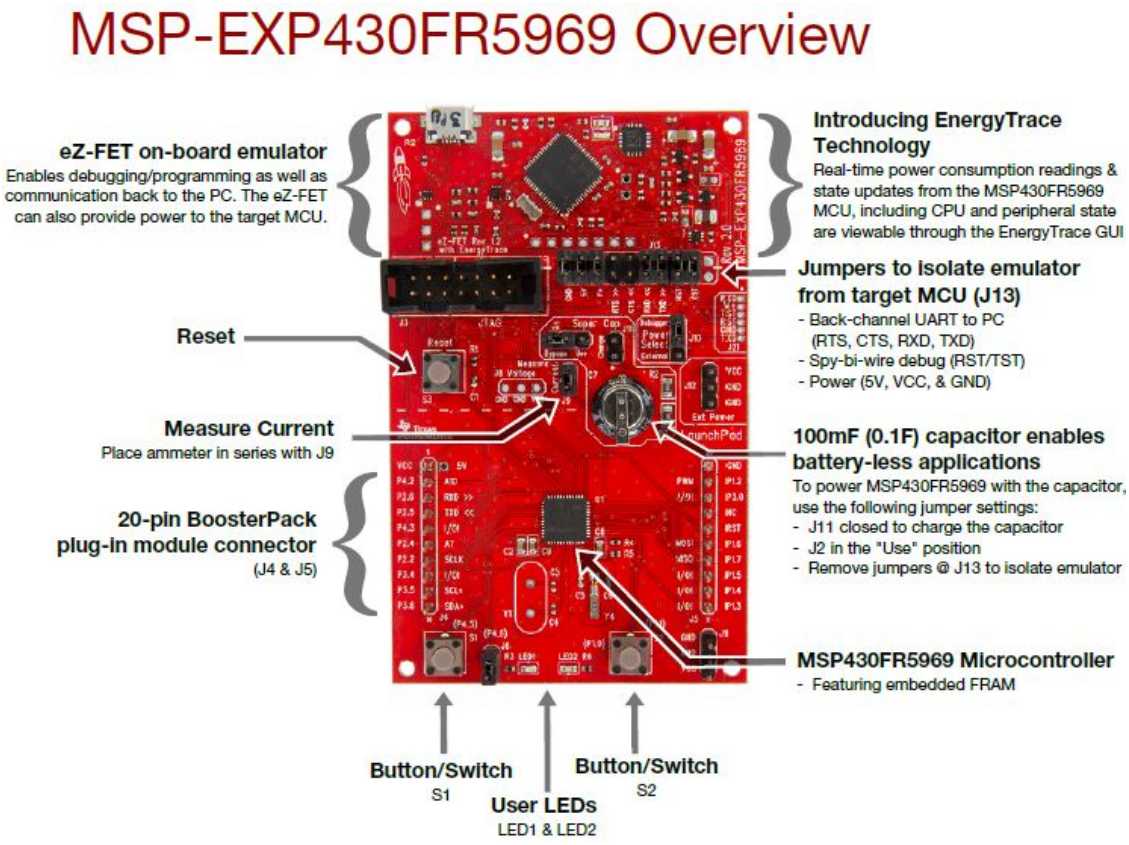

Figure 2.38. MSP430FR5969 Launchpad

the sEMG signals acquired from Gastrocnemio Medialis during 10 gaits and in Figure 2.41 its PSD cut of at the sEMG signals frequencies (400Hz).

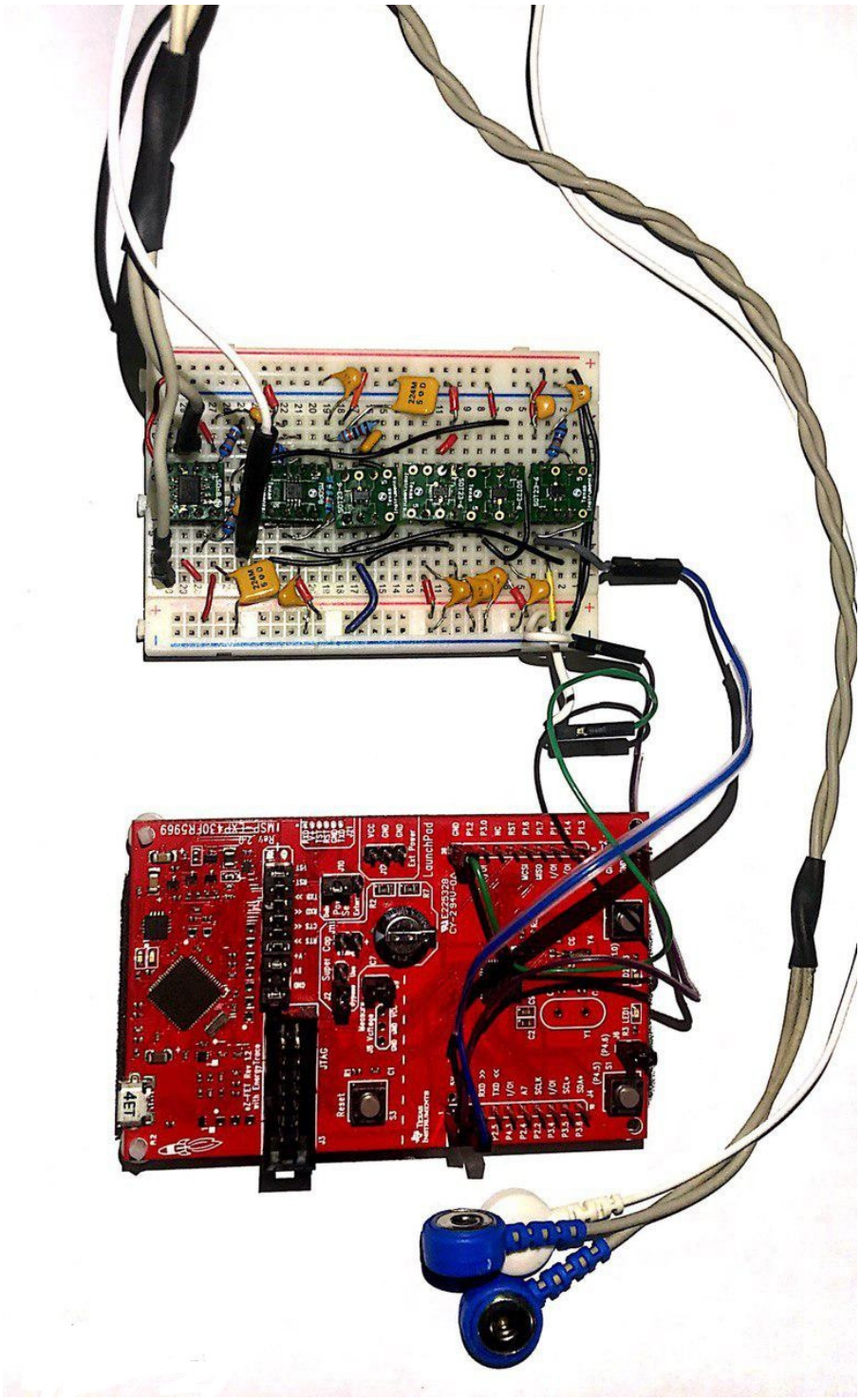

Figure 2.39. System composed by the Analog Front End Breadboard prototype and the MSP430FR5969 Launchpad

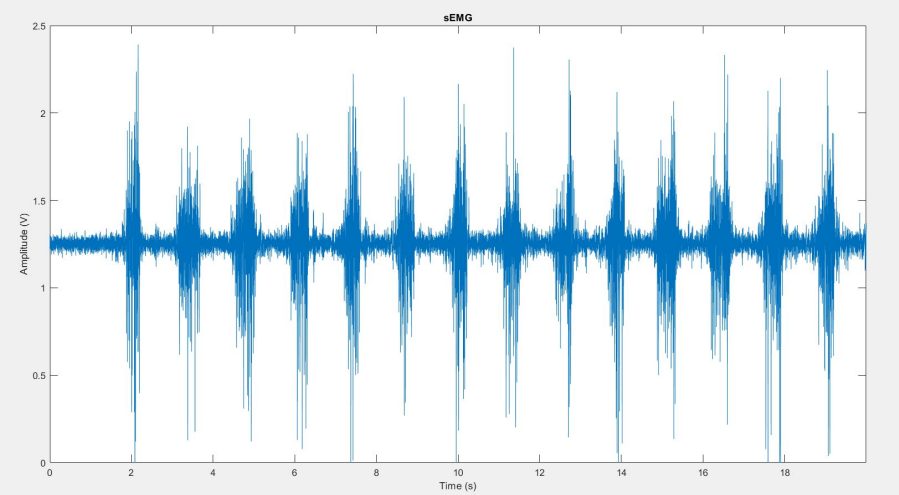

Figure 2.40. Gastrocnemio Medialis sEMG signals acquired and processed by the breadboard, sampled by the MSP430 and graphed with Matlab during 14 gaits

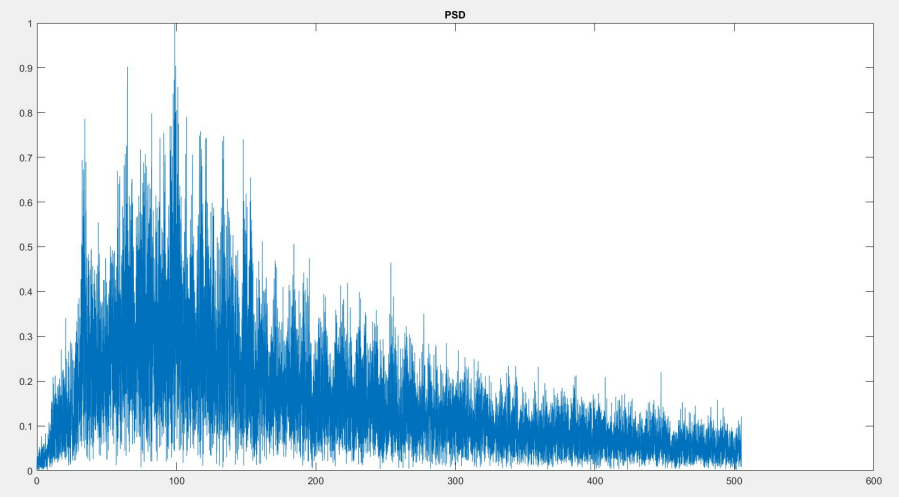

Figure 2.41. Power Spectrum Density signals acquired and processed by the breadboard, sampled by the MSP430 and graphed with Matlab during 14 gaits

Chapter 3

Hardware Implementation

Each slave of the system include 2 board that are interconnected by means of pin headers. The 2 module are:

- Main board: here the microcrontroller nRF52840 is located and it is in charge of keeping the synchronization between other slaves of the system and to store in a μSD card the sEMG signal properly processed by the AFE or its number of threshold crossing events;

- Analog Front End: it is in charge of acquiring and processing the sEMG signal to provide the desired bandwidth and voltage range and the number of its threshold crossing event.

The software used to design the boards is Altium Designer.

3.1 Schematics

In the following the schematics of the Analog acquisition channel module and the main board will be illustrated separately. They will be turned into two different board interconnected one upon the other by means of pin headers. While the main board has a connector header for the power source, the analog front end receive the power supply from two pins of a pin header. In this system the main board provide the supply for the analog module through this header but it can also be used stand alone powering the said pins.

3.2 Analog Front End

It is in charge to acquire and process the sEMG signal. In Figure 3.1 the block scheme of the new Analog Front End (*AFE*) is reported.

It is supplied by a single positive power supply of 2.5V. Then the signals are buffered to decouple them from the inputs and a 30Hz differential high pass filter cut out the movement artifact frequency. The signals are thus subtracted and amplified by 500V/V by means of a Instrumentation Amplifier (*INA*) that adds to this signal an offset to place it in the middle of the dynamics. Here the middle dynamic voltage is also sent to a Driven Right Leg circuit to a known DC voltage the muscle to be acquired. Since Different muscles give different signal amplitudes, a second programmable stage is added to let every kind of signal to range the whole dynamic. A 400Hz low pass filter can now cut out all the frequencies outside the EMG signal bandwidth. At this point the sEMG processed signal can be sent to the main board to be sampled. For the threshold crossing signal a comparator with hysteresis is added. The threshold is provided externally by the main board. For all the capacitance in the filters have been chosen C0G capacitor to obtain a more sharp filter. For the same purpose resistors chosen for filters have 0.1% tolerance.

3.2.1 Input Stage

The input stage (Figure 3.2) includes:

- Protection circuit;
- Buffers;
- 30Hz Differential High Pass Filter;
- Driven Right Leg circuit.

The overvoltage protection circuit is inserted to prevent the system to be damaged by input voltage spikes over positive power supply of 2.5V. J1 is a 3 positions connector header, 2 of them are for the sEMG signal and the other one for the output reference. D1 and D4 are TVS Diode (*ESD5Z2.5T1G*) with 2.5V breakdown voltage. They are in charge of suppress all the overvoltages above the positive power supply voltage providing a path to ground for the current.

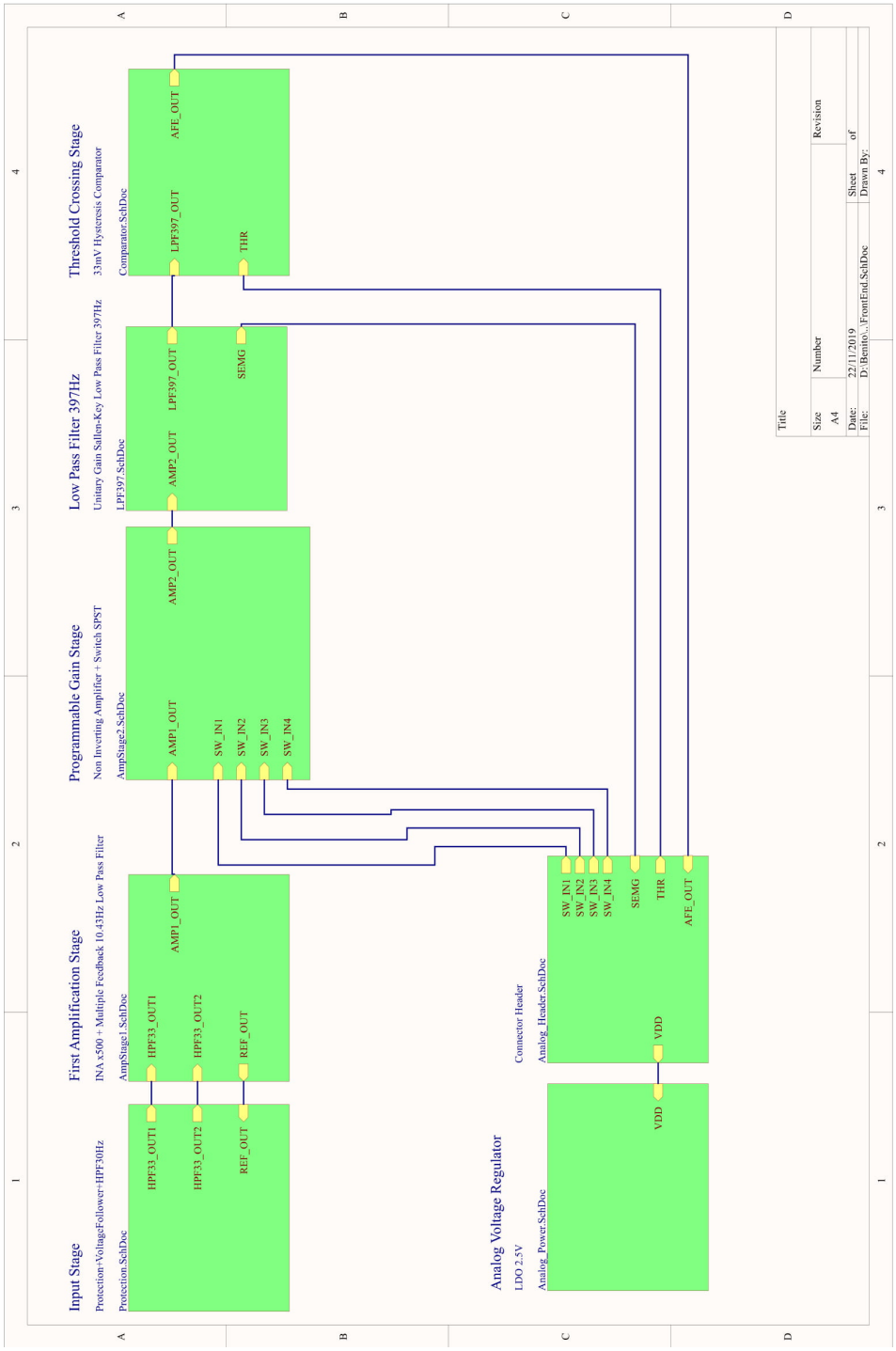

Figure 3.1. Analog Front End Module Block Scheme

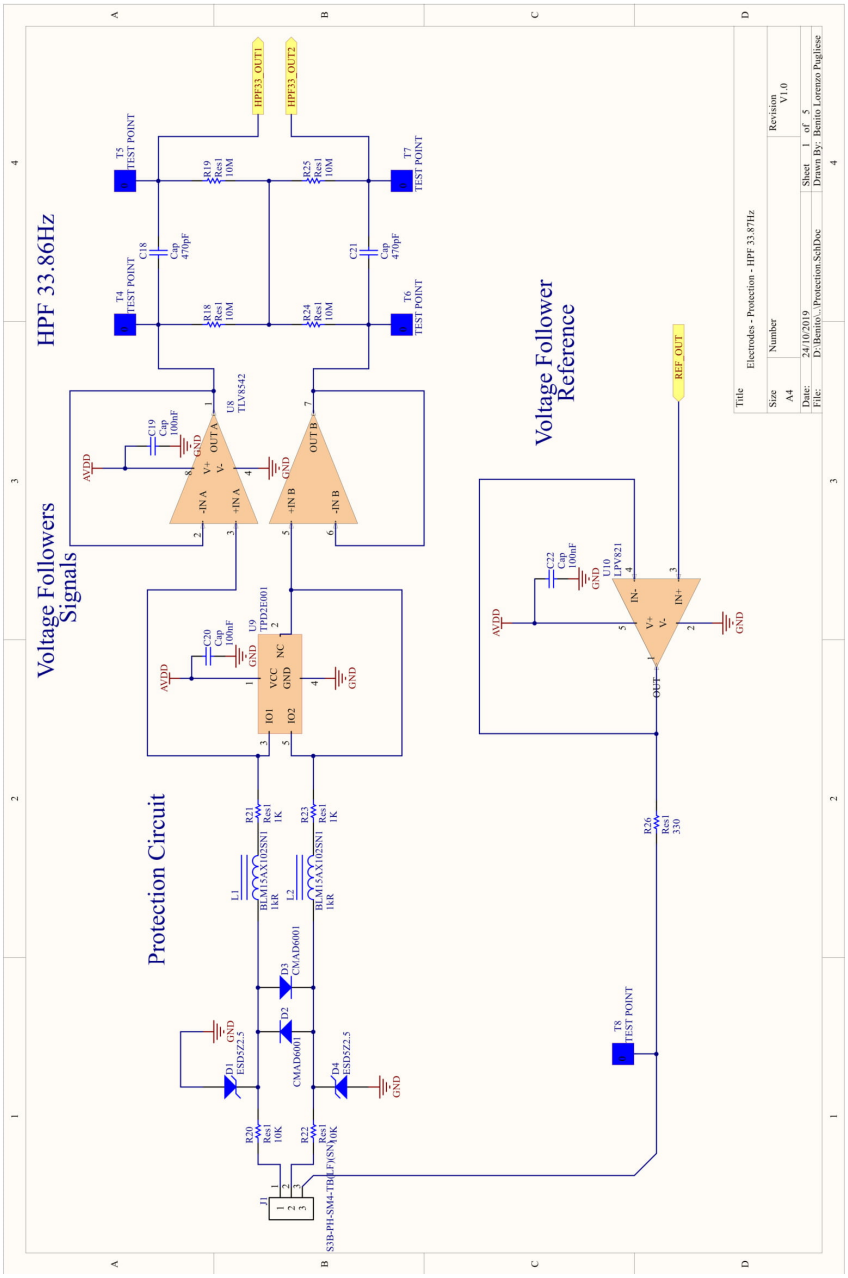

Figure 3.2. Input Stage Schematic: Protection Circuit; Buffers; 30Hz Differential High Pass Filter; Driven Right Leg Circuit

R21 and R23 are placed to limit the current due to overvoltages to about 10mA considering a 100V maximum input, infact

$$I_{max} = \frac{100V - 2.5V}{10K\Omega} = 9.75mA \tag{3.1}$$

D2 and D3 are general purpose diodes to prevent the 2 input signal to be too different between them. If they are, they are not sEMG signals.
L1 and L2 are ferrite beads to suppress high frequency ElectroMagnetic Interference (*EMI*) and Radio Frequency Interference *RFI*) electronic noise. They infact act as low pass filter converting radio frequency energy in heat (noticeable only in extreme cases). U9 is based on Electrostatic Discharge (*ESD*) protection diode array.
$100nF$ decoupling capacitor has been placed on the power supply rails. The signals pass through a voltage follower to decouple the rest of the circuit. Has been chosen a 2 channel chip voltage follower (*TLV8542*)for space optimization. The 2 signals are now filtered by means of a second order differential high pass filter (Figure 2.4) to attenuate the movement artifacts noise. The cut off frequency of the filter can be calculated as follow:

$$f_{cutoff} = \frac{1}{2\pi RC} \tag{3.2}$$

and thus choosing the right resistors and capacitors can be achieved the desired bandwidth. In this application has been chosen 470pf as capacitance and 10MΩ as resistance leading to a cut off frequency of 33.86Hz.
A middle dynamic voltage generated in the next stage is feeds the reference electrode through a buffer. It active drives the body to a known voltage that is half of the power supply.
A 330Ω resistance is placed to limit the current flowing if a connection with ground is made. Test points are also added for verification purpose.

3.2.2 First Amplification Stage

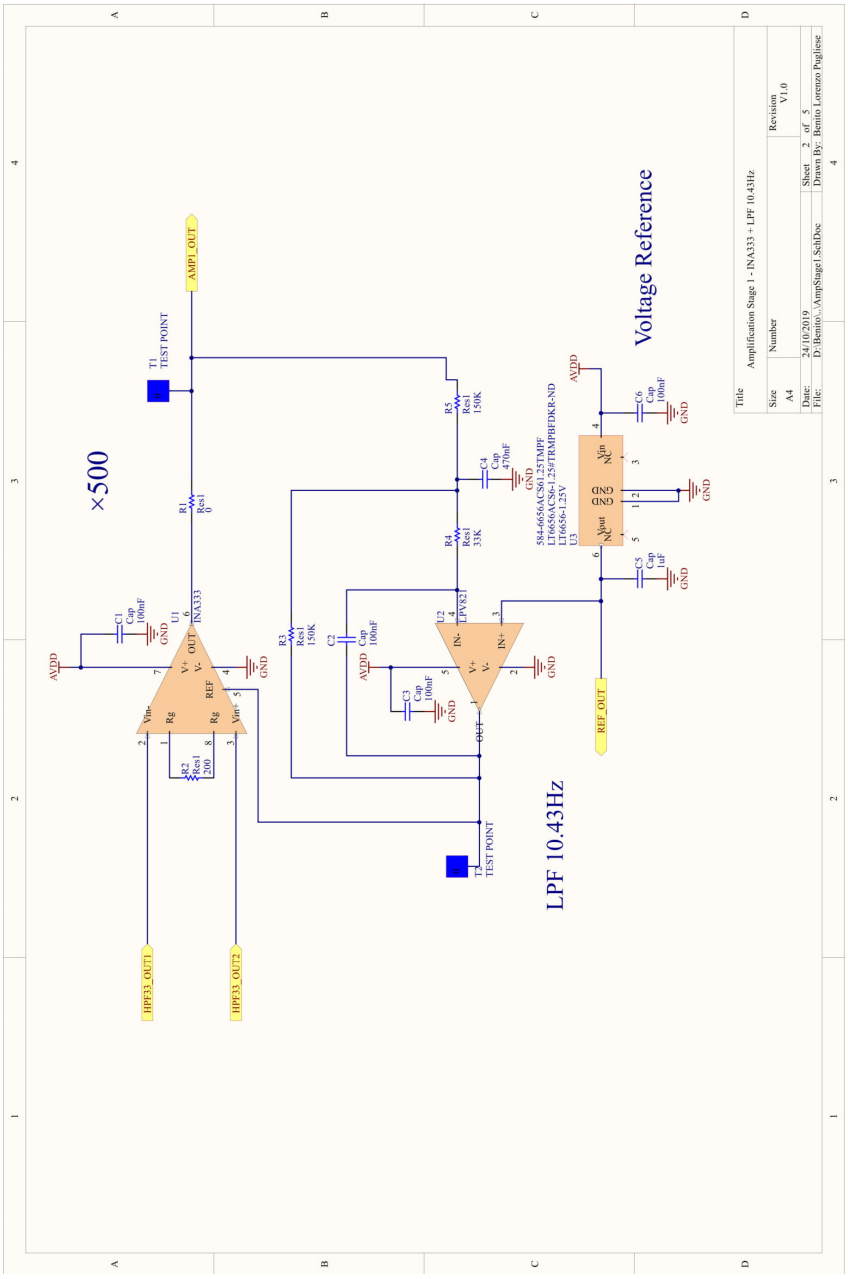

Figure 3.3. First Amplification Stage: 500 Gain Instrumentation Amplifier; Feedback 10Hz Low Pass Filter; 1.25V Voltage Reference

In this stage an Instrumentation Amplifier (*INA*) is used to amplify the difference between the 2 input signals (Figure 3.3).

The one used in this version is the INA333, from Texas Instrument, that overcomes the saturation problem of the precedent version INA321 (section 2.2. Its gain can be set by one additional resistor, particularly is:

$$G = 1 + \frac{100k\Omega}{R_2} \tag{3.3}$$

Since the sEMG range between less than 50μV up to 30mV, $R_2 = 200\Omega$ has been chosen to obtain a gain of 499V/V. The 0/ohm resistance R_1 is placed to reconfigure the gain of the underlying non inverting stage under need.
The INA reference let the amplified differential signal to be centered to a middle dynamic DC voltage and come from the multiple feedback low pass filter of the INA feedback. It is introduced to eliminate the low frequency component introduced by the INA. Its cut off frequency is given by:

$$f_{cutoff} = \frac{1}{2\pi\sqrt{R_4 R_5 C_2 C_4}} \tag{3.4}$$

Here have been chosen $R_3 = 150k\Omega$, $R_4 = 33k\Omega$, $C_4 = 470nF$, $C_2 = 100nF$, leading to a cut off frequency of 10.43Hz.
In the middle of the bandwidth (almost DC) we can identify two inputs:

- the INA output going through the pin "-" of the OPA;
- the middle dynamic voltage (1.25V) generated by the voltage reference. It solves the problem of the power supply fluctuation that corrupt the sEMG signal acquired and keep equal the reference voltage of the different slaves.

The INA output sees though an inverting amplifier with gain

$$G_{inv} = -\frac{R_3}{R_5} = -1 \tag{3.5}$$

while the DC input sees a non-inverting amplifier with gain

$$G_{non-inv} = 1 + \frac{R_3}{R_5} = 2 \tag{3.6}$$

The output of this stage is thus

$$V_{INAref} = V_{INAout} Ginv + \frac{VDD_{nRF}}{2} G_{non-inv} = 2\frac{VDD_{nRF}}{2} - V_{INAout} \tag{3.7}$$

The output of this stage is the input of the INA reference. The more increases the INA reference, the more increases INA output. On the other hand when V_{INAout} increases, V_{INAref} decreases. Consequently V_{INAref} and V_{INAout} will follow a dumped oscillation, in opposite way, around middle dynamic stabilizing to it.
$100nF$ decoupling capacitors have been placed on the power supply rail and test points are also added for verification purpose.

Programmable Gain Stage

Since Different muscles give different signal amplitudes, a second programmable stage is added to let every kind of signal to range the whole dynamic (Figure 3.4).

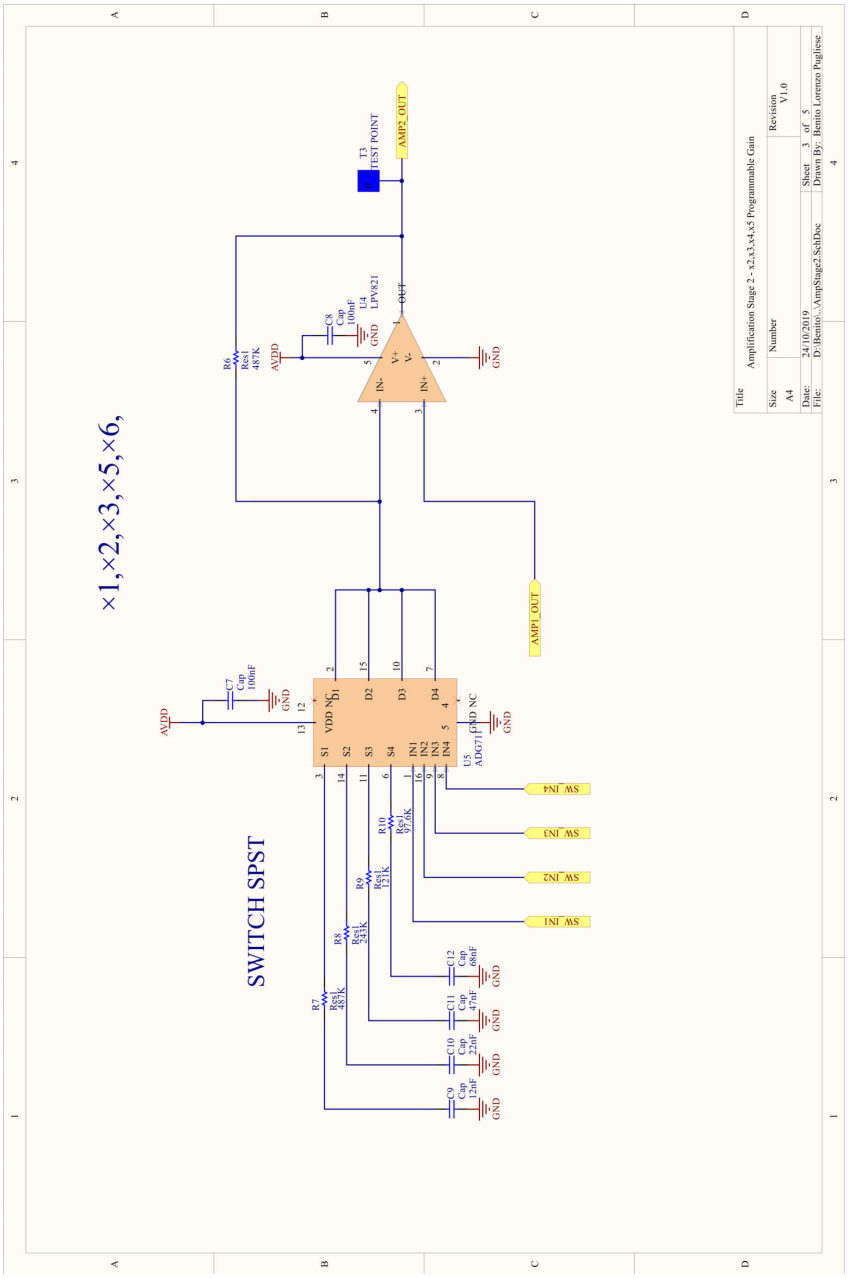

Figure 3.4. Programmable Gain Stage: Non Inverting Amplifier with Switch SPST for programmable gain

Since the power consumption of Programmable Gain Amplifiers are very in the orders of mA, a non inverting amplifier with Switch SPST to select the gain have been preferred.
The amplification of this stage is:

$$G = 1 + \frac{R_6}{R_g} \tag{3.8}$$

R_6 is 487kΩand as R_g integer divider of R_6 have been chosen. They thus range from 97.6kΩto 487kΩ. Only one switch at a time has to be closed to achieve an integer gain and they are controlled by control signal from the main board, they are:

- G=1 if all switch opened;
- G=2 if Switch1 is closed;
- G=3 if Switch2 is closed;
- G=5 if Switch3 is closed;
- G=6 if Switch4 is closed;

The total gain reached until this stage is thus: 500V/V, 1000V/V, 1500V/V, 2500V/V, 3000V/V.
Capacitors in series to the resistances are selected to have a 30Hz High Pass Filter in order to amplify only the signal and not the DC. The DC infact see a buffer stage and remained unaltered in the output.

3.2.3 Low Pass Filter Stage

A second order Sallen-Key low pass filter is here placed (Figure 3.5 to eliminate the frequency over than 400Hz which are not part of the EMG signal.

The cut off frequency is given by:

$$f_{cutoff} = \frac{1}{2\pi\sqrt{R_{16}R_{14}C_{15}C_{17}}} \tag{3.9}$$

Here $R_{16} = R_{14} = 27k\Omega$, $C_{15} = 10nF$, $C_{17} = 22nF$ and thus $f_{cutoff} = 397Hz$.By Do Not Populating (DNP) R_{17} and fixing R_{15} to 0Ω, the configuration for unity gain is obtained but the possibility to have a different gain is available by sizing the 2 resistors, infact:

$$G = 1 + \frac{R_{15}}{R_{17}} \tag{3.10}$$

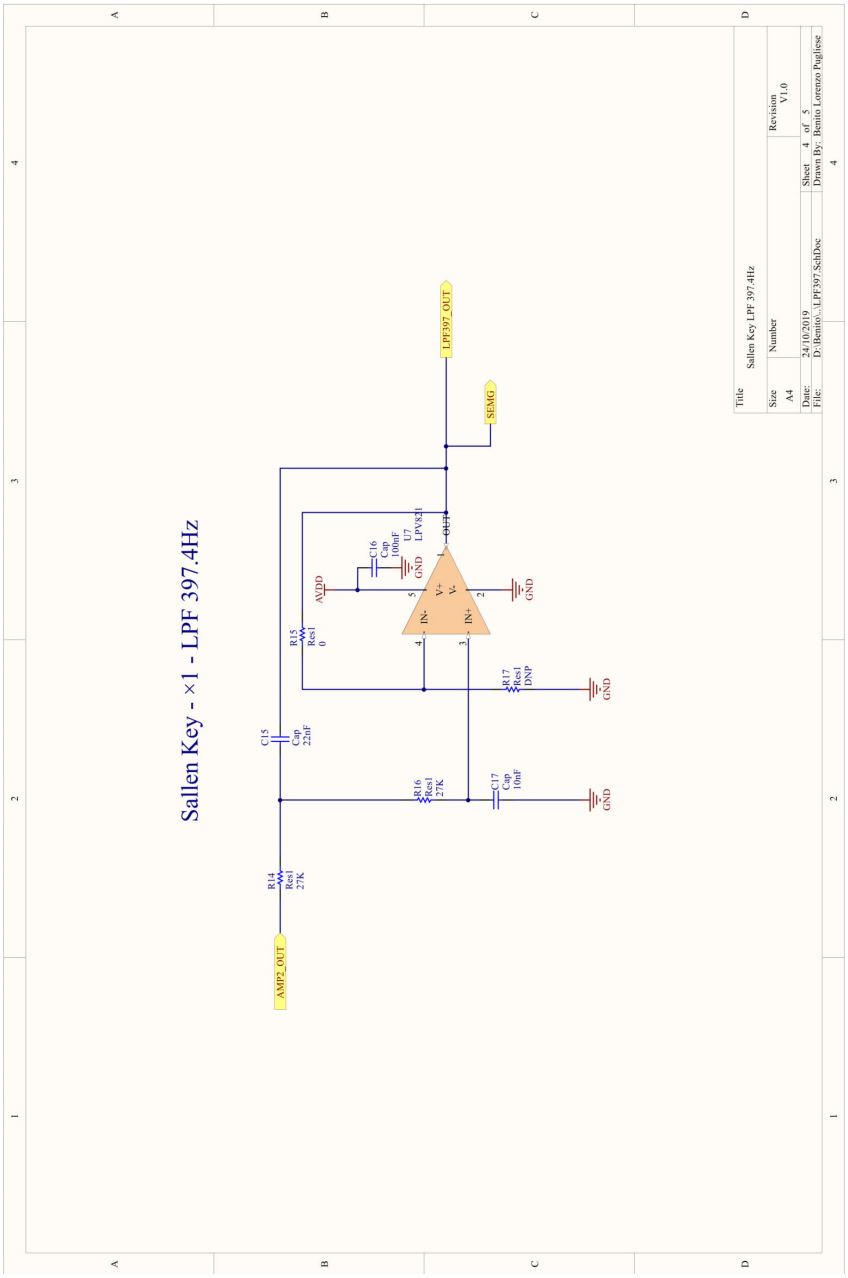

Figure 3.5. Low Pass Filter Stage: 400Hz Unitary gain Sallen-Key

The output of this stage is the sEMG signal that is the input of the microcontroller ADC. The output drives also the next stage that generates the Threshold Crossing signal. $100nF$ decoupling capacitor has been placed on the power supply rail.

3.2.4 Threshold Crossing Stage

To obtain the Threshold Crossing signal a comparator and a threshold is needed (Figure 3.6). The comparator has been closed in a feedback to obtain a Schmitt Trigger.

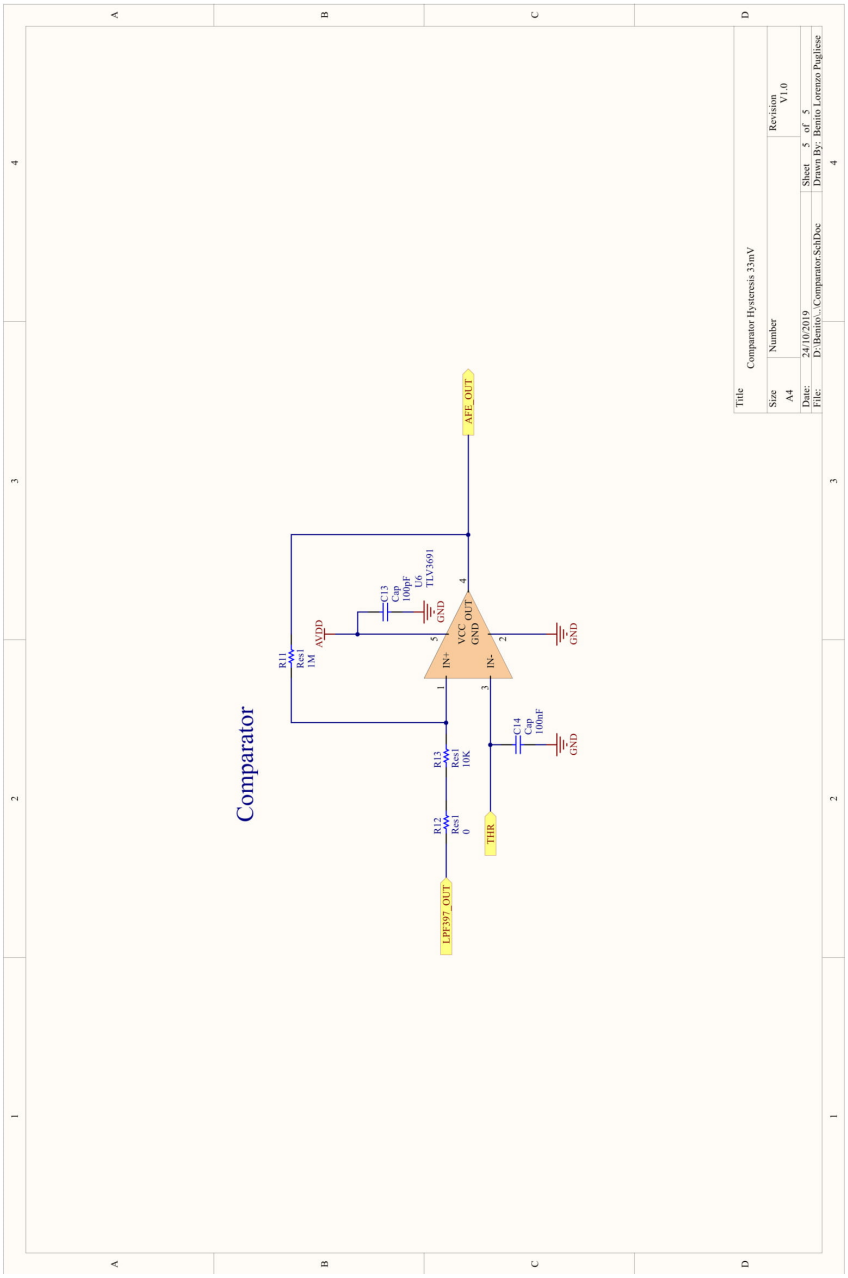

Figure 3.6. Threshold Crossing Stage: Comparator in 44mV Hysteresis Schmitt Trigger configuration

Hysteresis on output is infact needed to eliminate the threshold crossing events due to the noise. The hysteresis around V_{THR} is:

$$\Delta V_{Hysteresis} = \frac{R_1 3}{R_1 1} VDD_{nRF} = 10mV \tag{3.11}$$

The 0Ω resistance R_{12} is placed here for the possibility to increase the hysteresis if needed.
The TC signal feeds a microcontroller input where a counter is instantiated. $100nF$ decoupling capacitor has been placed on the power supply rail.

3.2.5 Analog Voltage Regulator

Since the voltage reference selected in the first amplification stage, because of its extremily low power consumption with respect to other voltages (section 2.4.4), provides 1.25V, a 2.5V linear drop out is needed (Figure 3.7) for regulating the power supply provided by the main board and for centering the signal in the dynamics. Capacitors have been placed as suggested in its datasheet.

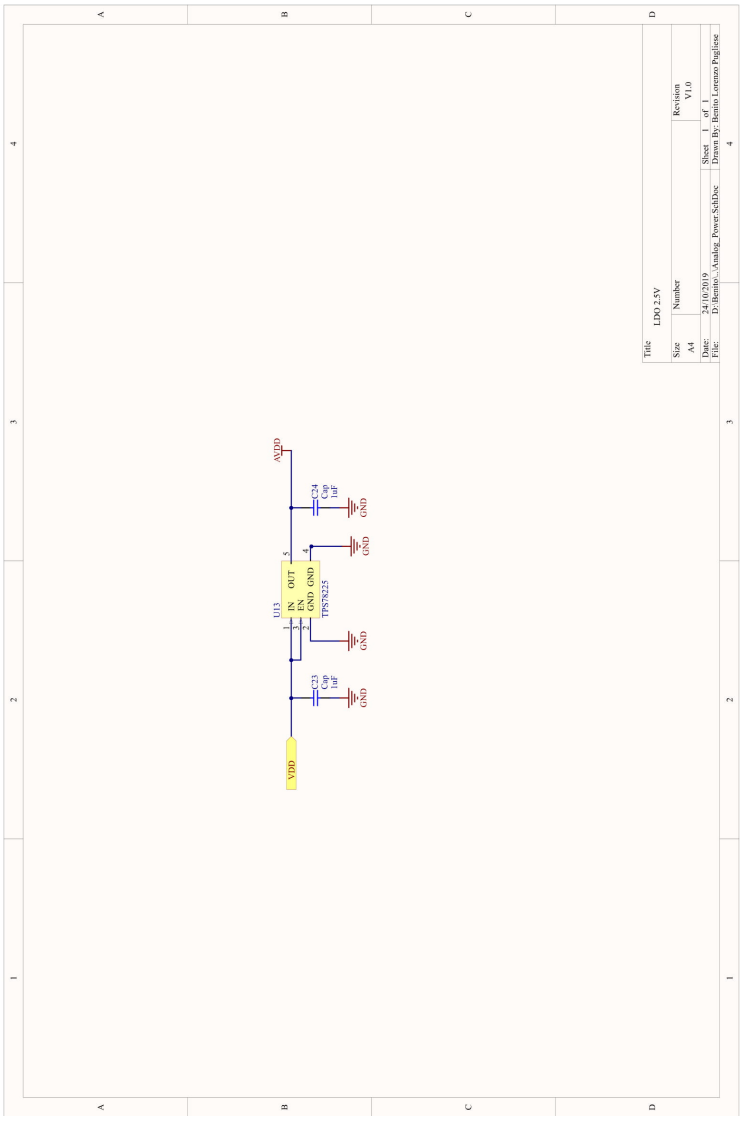

Figure 3.7. 2.5V Linear Drop out Analog Front End Voltage Regulator

3.2.6 Analog Pin Headers

Two lines of pin header are inserted to communicate between the boards (Figure 3.8). The main board and the analog acquisition channel are infact thought to work one upon the other. The AFE provides the whole sEMG signal and the Threshold Crossing signal to the main board, while the main board provides the power supply, the threshold and the control signal for the programmable gain amplifier switch.

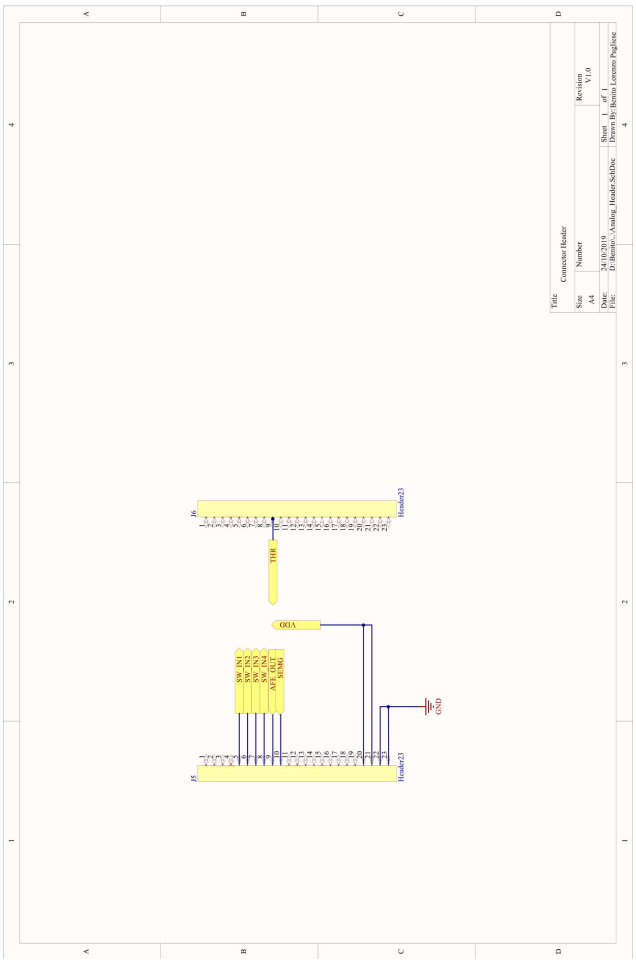

Figure 3.8. Pin Headers on the Analog module

3.3 Main Board

The block scheme of the main board is reported in Figure 3.9. The main board is in charge of storing the desired data into the micro SD and keeping the synchronization between the slaves. It can sample the sEMG signal processed in the analog front end and count its number of threshold crossing events. It generates the threshold to be provided to the threshold crossing stage of acquisition channel module and provides the signals for controlling the programmable amplification stage. A power management unit regulates the battery voltage to 3.3V providing the supply for the AFE and externally in general. All the micro GPIOs are routed out to pin headers to be used easily for future implementation.

3.3.1 Microcontroller

The microcontroller is the nRF52840 selected in the precedent version for its low power consumption (Figure 3.10).

The configuration selected is the one with normal voltage mode and only one internal DC/DC regulator and a RF antenna. The passive elements and the oscillators are selected and places as suggested in its datasheet. R_{27} and C_{39} are placed for antenna impedance matching if needed. The pins to control the programmable gain switch are routed out to the pin header to communicate with the AFE board. The sEMG signal processed by the analog front end and coming from the header is connected to an analog input and the threshold crossing signal to a general purpose GPIO. Other gpios are for the SD card management, to drive leds, to communicate with a micro USB, to set the DAC value and to communicate with the JTAG. The unused pins are routed out to the pin header to be used easily for future implementation. The pin 15 of J7 is leaved unconnected because there will not be its hole in the footprint. This is done to give a direction at the boards and not coonect wrong the analog and digital module. Some ground connections and power supply connections have been routed out to the pin headers to be available for the other additional modules. Capacitors have been placed to the power supply pin header connection to give an immediate source of current if required by other the modules.

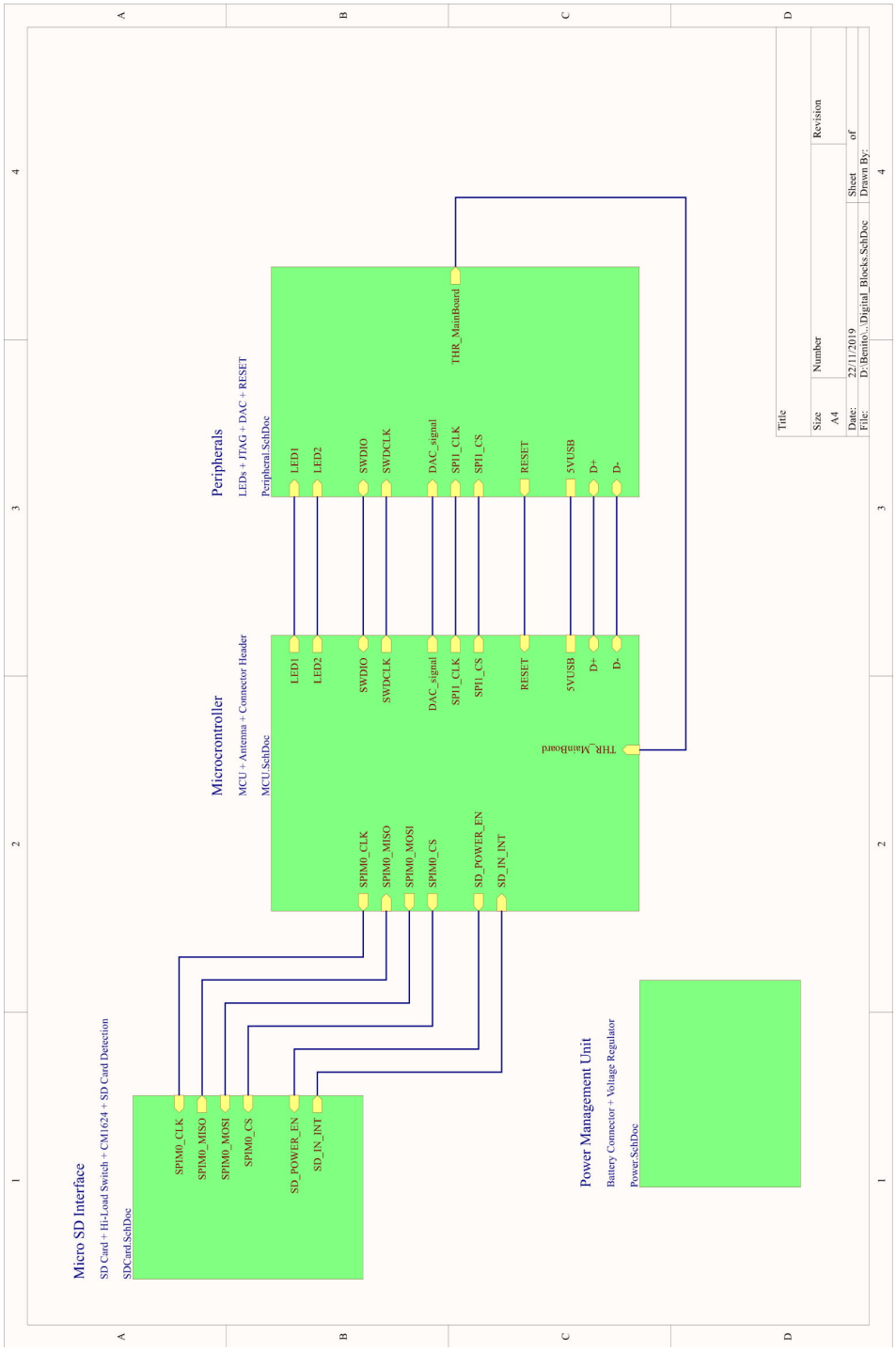

Figure 3.9. Main Board Block Scheme

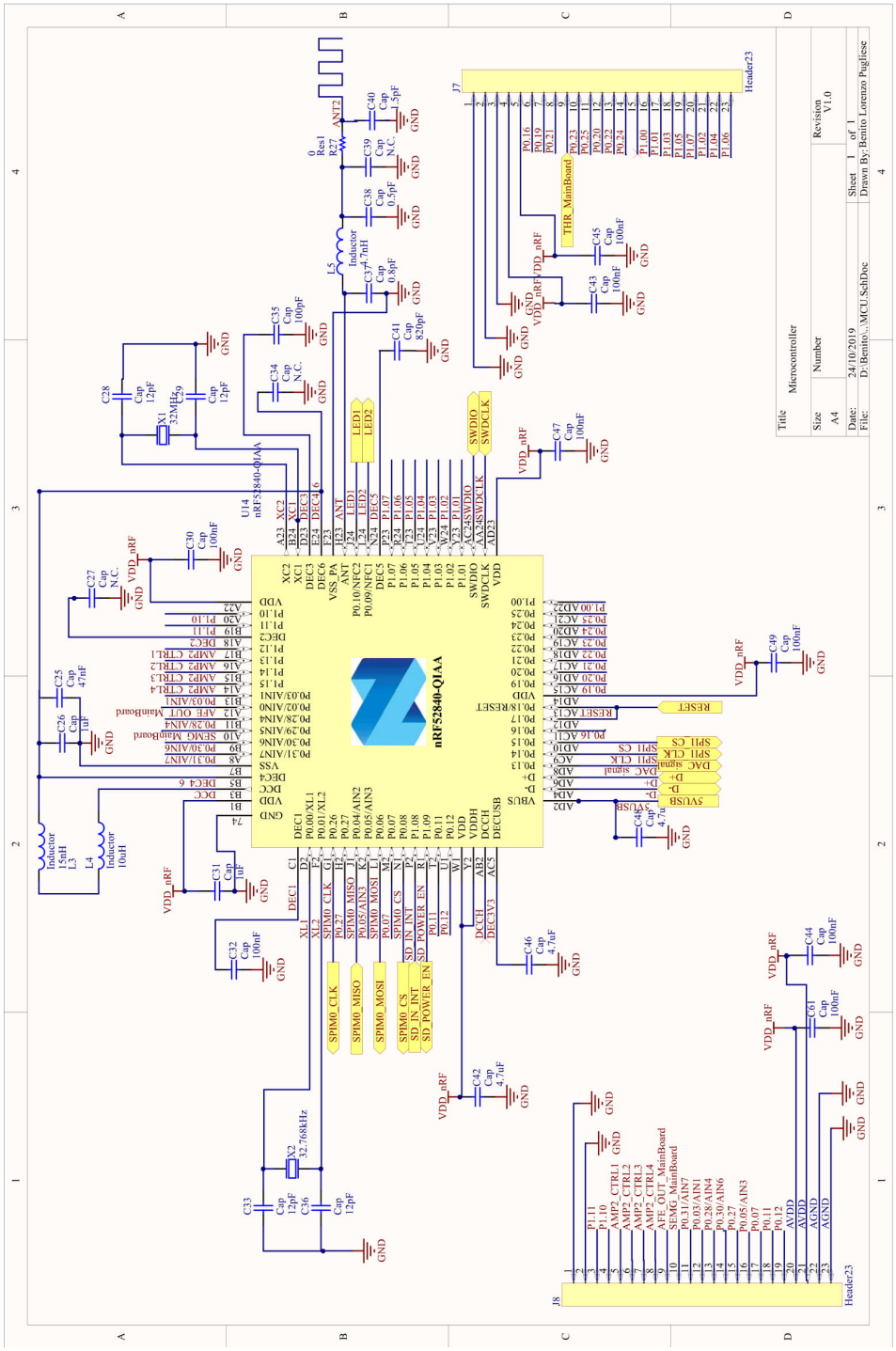

Figure 3.10. Microcontroller schematic

3.3.2 Power Management Unit

The power management unit is in charge to regulate the voltage from the battery (Figure 3.11).

Between the battery and the regulator there is a mechanical switch to let the current supply the system. The regulator used is the TPS63031 buck boost with 3.3V fixed output. The passive element are placed and selected as suggested in the datasheet. The enable pin is stacked high when the system is turned on and the power saving have been permanently disabled to have a more stable output. Test point are placed to verify the correct behaviour.

3.3.3 SD Interface

The SD interface has component to correctly manage the SD Card (Figure 3.3.3).

A low pass filter with 10ms time constant, to dump the insert SD signal fluctuation, and a pull up resistance have been place before the mechanical switch the inform about the presence of the SD.
An high side power switch *ADP191* has been placed to let supply reach the VDD pin only if the SD is inserted and to attenuate the hot insertion effects.
Three capacitance with different value have been placed on the supply trace to immediately provide current during SD operation.
An electromagnetic interference filter *CM1624* has been introduced on the SD communication lines.

3.3.4 Peripherals

In this schematic the peripherals are gathered (Figure 3.13).

The DAC *AD5621* has a 12 bit resolution and is setted by an SPI communication with the microcontroller. It provides the threshold for the treshold crossing generation in the analog front end.
The reset button has a 10ms time constant low pass filter to dump the oscillation during the closing.
Two leds are used to inform about the state of the microcontroller.
A micro USB interface is provided for a possibile future usage.
The JTAG interface is used to flash and debug the microcontroller.

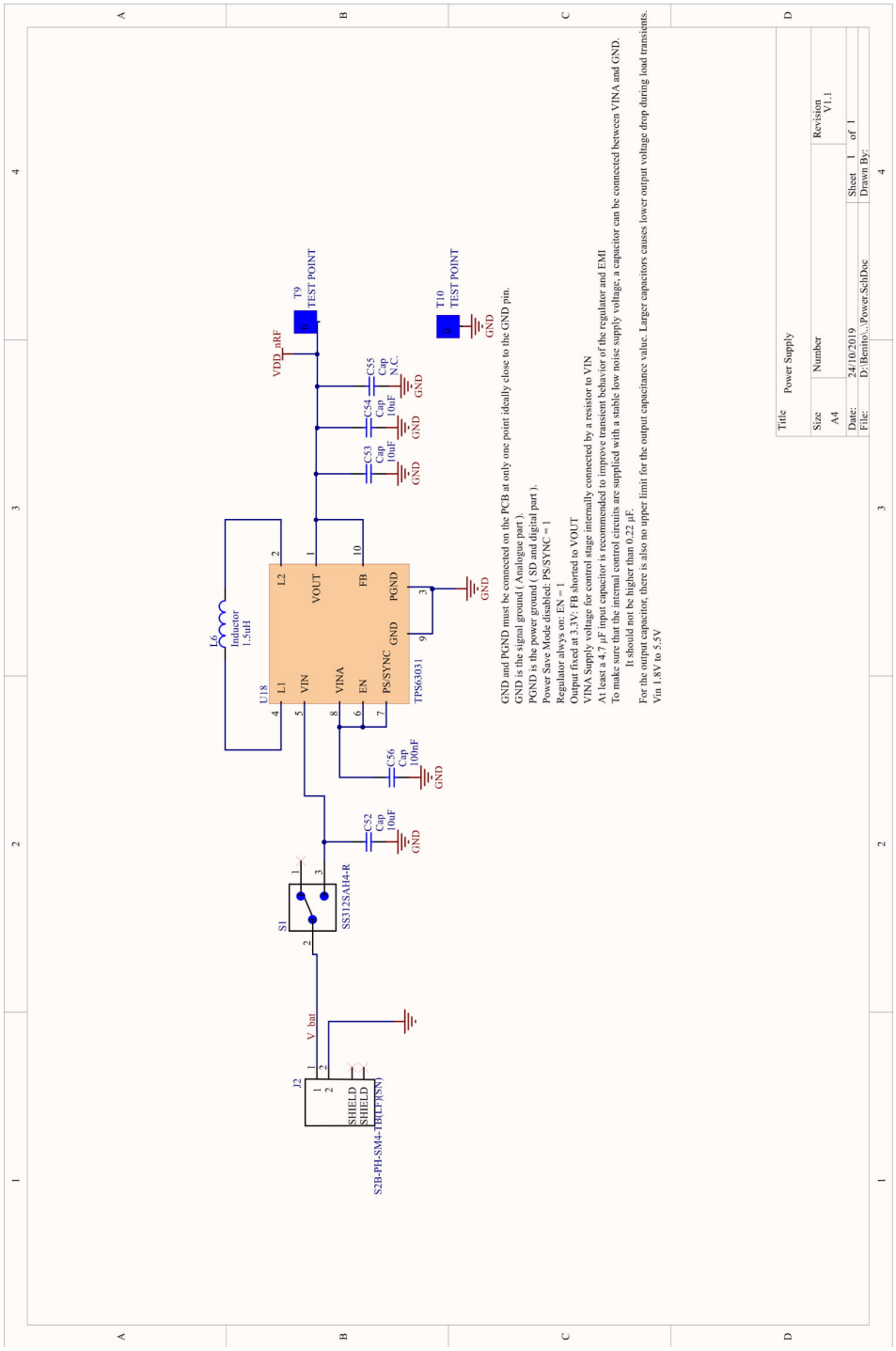

Figure 3.11. Power Management Unit Schematic

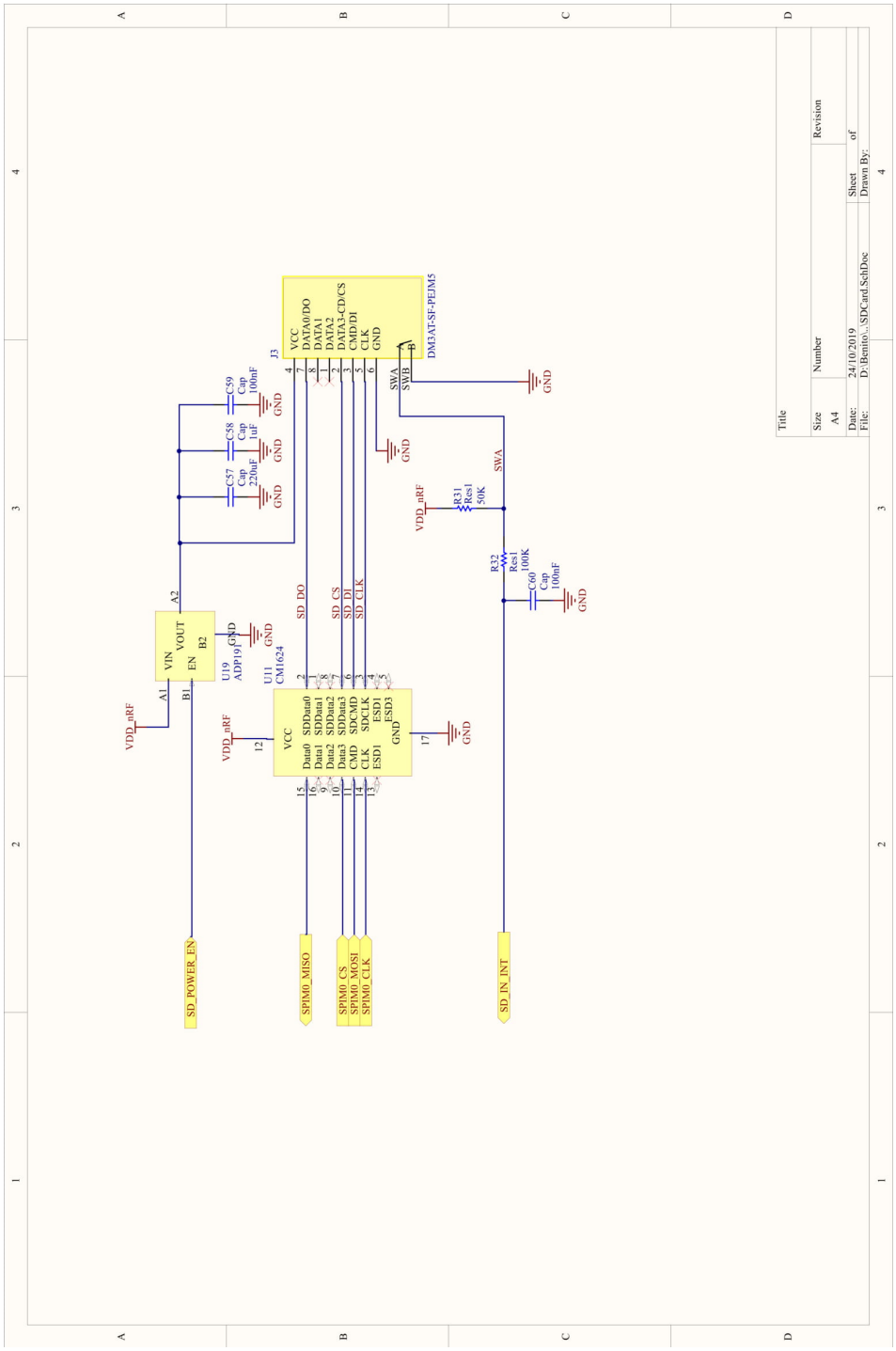

Figure 3.12. SD interface Schematic

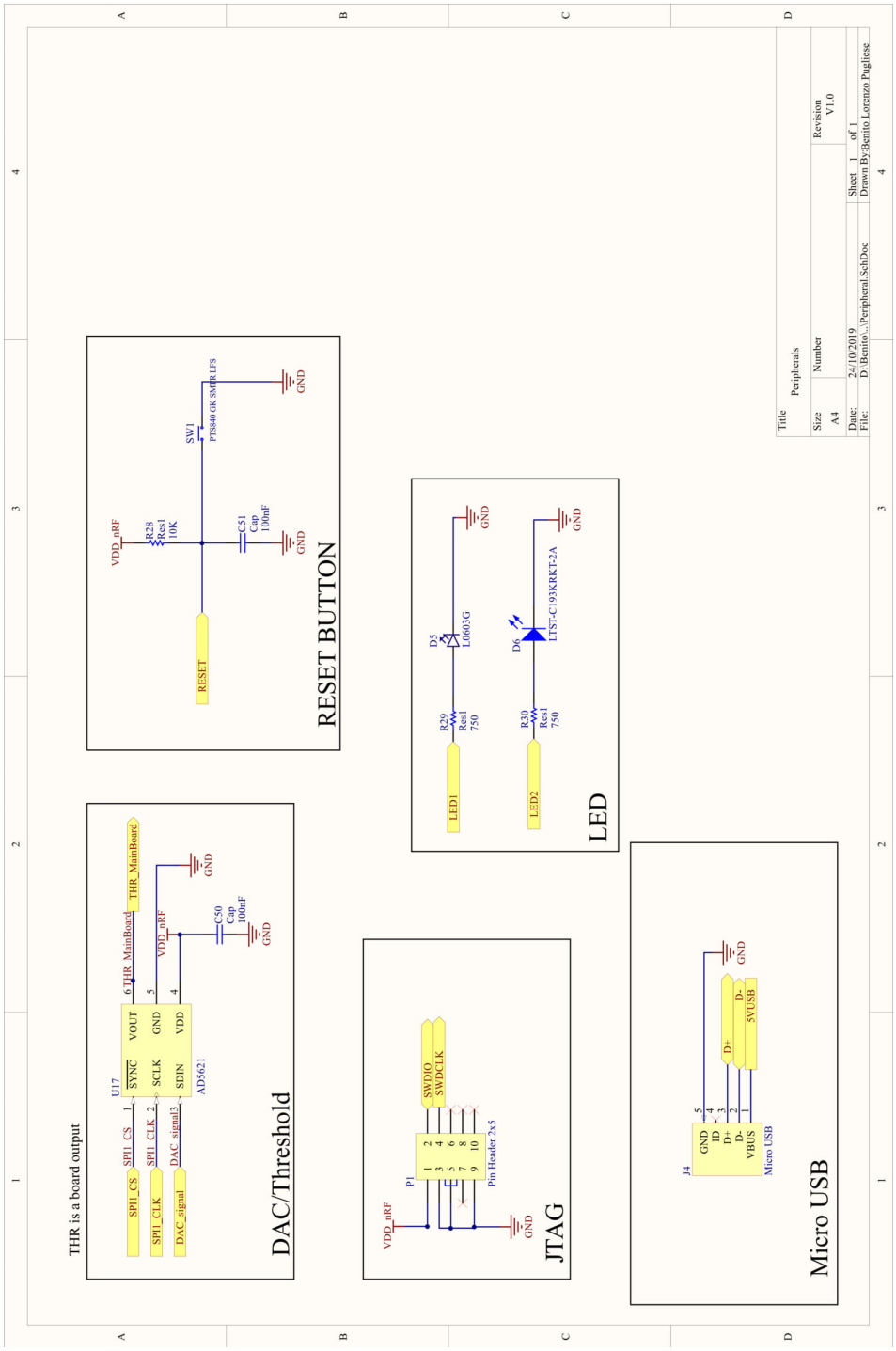

Figure 3.13. Peripherals schematic: DAC, Leds, JTAG, Reset Button, micro USB

3.4 PCB Layout

The system has been designed modular. The main board and the analog acquisition channel module will work together one upon the other. The connection between them is made by connection headers, two for board, that thus need to be at the same distance in both board. The distance has been chosen to be an integer multiple of the board matrix pitch to be compatible with the standard mechanics dimensions. Other usage of the board can be accomplished with the ease usage of the matrix board.
In following sections the analog and digital board PCB will be illustrated separately.

3.4.1 Analog Front End

The routing of the Analog acquisition module has been performed. The size of the resulting two layer board is ruled by the dimension of the main board and is $4.4cmx8.4cm$. The pin headers are displaced an integer multiple of the matrix board pitch ($2.54mm$) to allow the system to be compatible with standard mechanics dimensions and with the main board. Four 3.2mm diameter mechanical holes have been placed to hold the board in a case. Their size have been chosen to be compatible with the smallest common screw (3mm diameter). In Figure 3.14 and 3.15 the Top and Bottom Layer of the board. The components are only on the Top Layer to reduce costs.

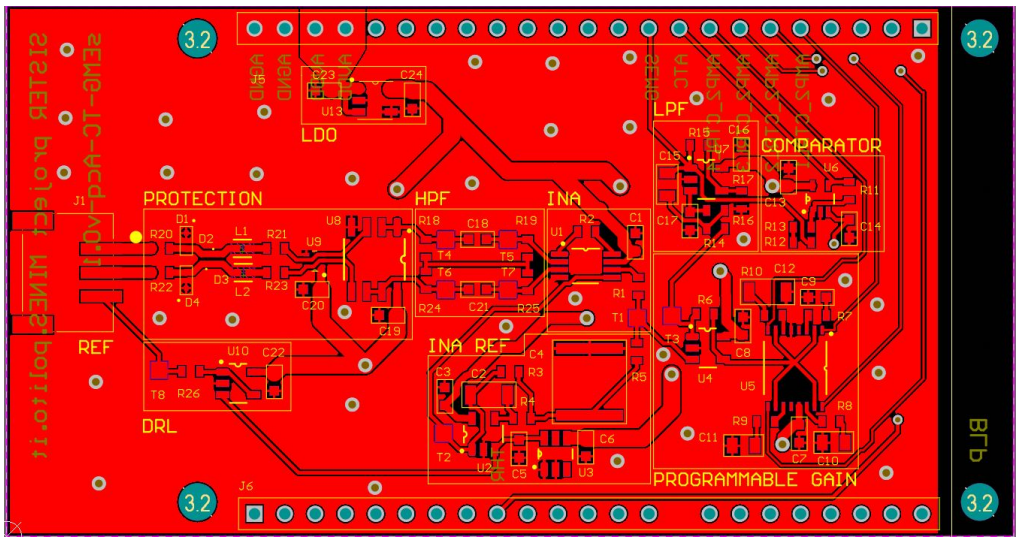

Figure 3.14. Analog Front End PCB Top

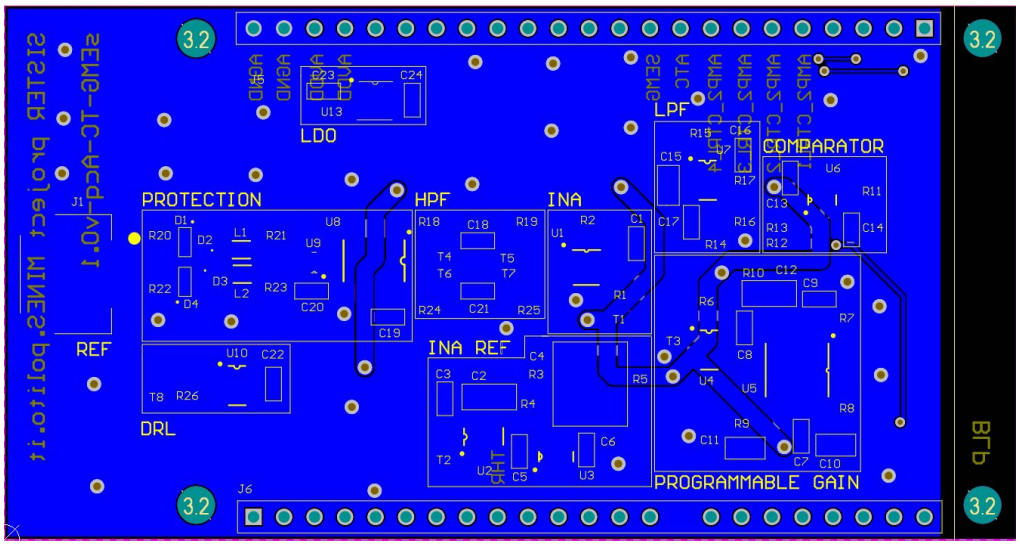

Figure 3.15. Analog Front End PCB Bottom

The connector J1 has been placed in an edge of the board. Here the two sEMG inputs and the output reference connection takes place. It is in the center for aesthetic purpose. The two signals go straight to maintain as possible the same trace length covered. The traces are kept as short and wide as possible to reduce the parasitic resistance. They are placed mostly on the top layer trying to reserve the bottom layer for the ground plane and return currents. The first two pins at the left in J5 are the ground reference of the board. They are connected to the ground plane in the Top and the bottom. From the third and fourth pin of J5 the power source needs to be applied. They are connected to the U13 2.5V linear drop out voltage regulator. From here the power supply traces are routed to each component trying to keep them as short and wide as possible. The decoupling capacitors are places as close as possible to the positive power supply pin of the components. The fifth until the eighth pins of the J5 headers are the control signals of the switch spst to set the desired gain. The ninth is the threshold crossing output and the tenth is the whole sEMG output. Each stage is highlighted and named in the silkscreen to be easily and visibly inspected. Each element has its own reference name for the same purpose. The ground plane is placed also in the Top Layer to reduce the cross talk between the traces. Ground vias have been spread around the ground plane to connect the two ground planes maximizing the equipotentialility in every pint of the plain. Unconnected copper areas are avoided by removing them or by connecting them with the bottom ground plane. The right limit of the ground plane is chosen to be

like in the Figure 3.14 for the possibility to put this module upon the main board and not covering with copper the antenna directivity.
The bottom Layer (Figure 3.15) is mostly reserved for the ground plane and some information. Particularly the name of the project, the group website, the author signature and the name of each headers pin used in this module. In Figure 3.16 and 3.17 the 3D view of the acquisition channel module.

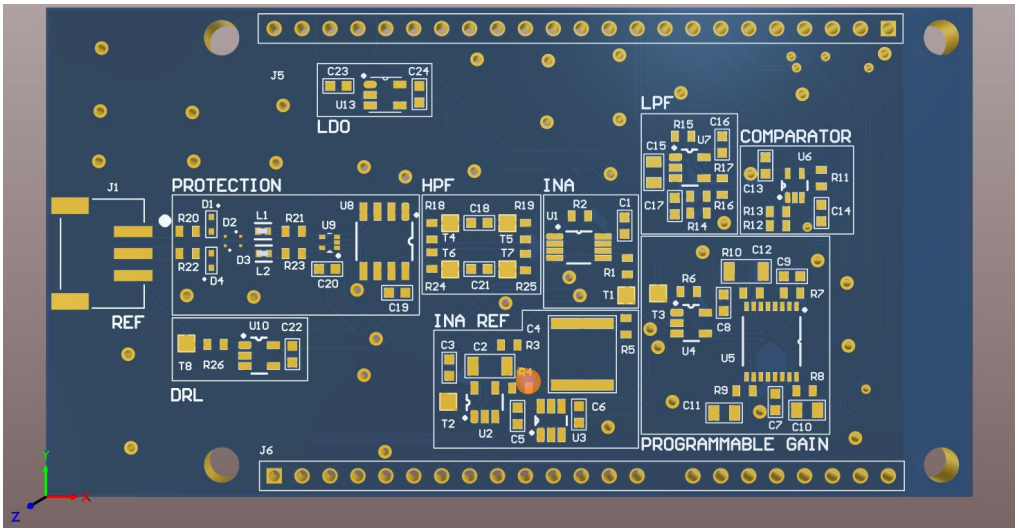

Figure 3.16. Analog Front End PCB 3D Top

3.4.2 Main Board

The routing of the Main Board has been performed. The size of the resulting two layer board is $4.4cmx8.4cm$ and is ruled by the pin headers position for the length and for the components that need to be on the edge of the board for the height. The micro SD interface, the micro USB interface, the mechanical switch and the battery header connector need infact to be on the edge to be accessed externally of a case. The pin headers are displaced an integer multiple of the matrix board pitch ($2.54mm$) to allow the system to be compatible with standard mechanics dimensions and the same value of the acquisition channel module to allow the communication between them. Four 3.2mm diameter mechanical holes have been placed to hold the board in a case and in the same planary position of the AFE board. Their size have been chosen to be compatible with the smallest common screw (3mm diameter). In Figure 3.18 and 3.19 the Top and Bottom Layer of the board.

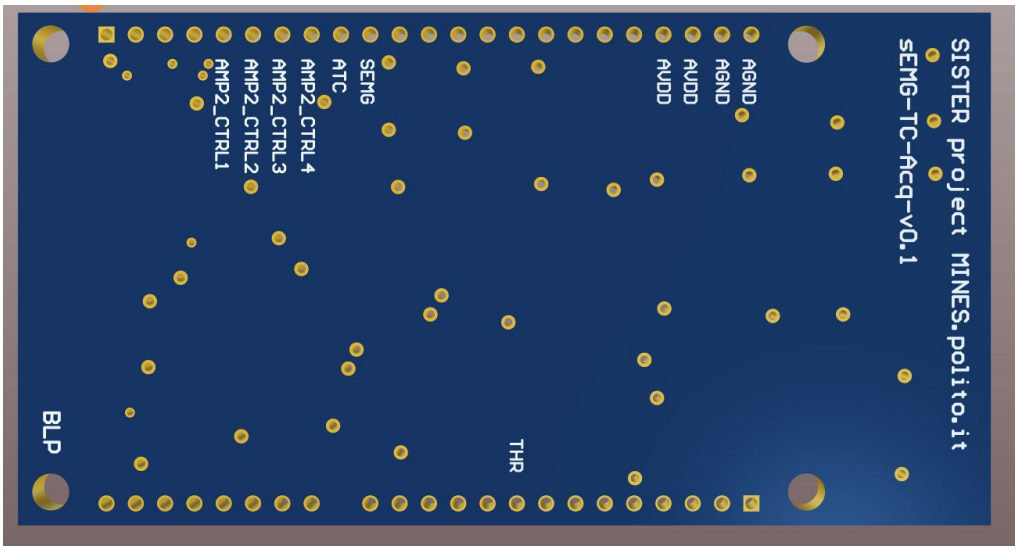

Figure 3.17. Analog Front End PCB 3D Bottom

The components are only on the Top Layer to reduce costs.

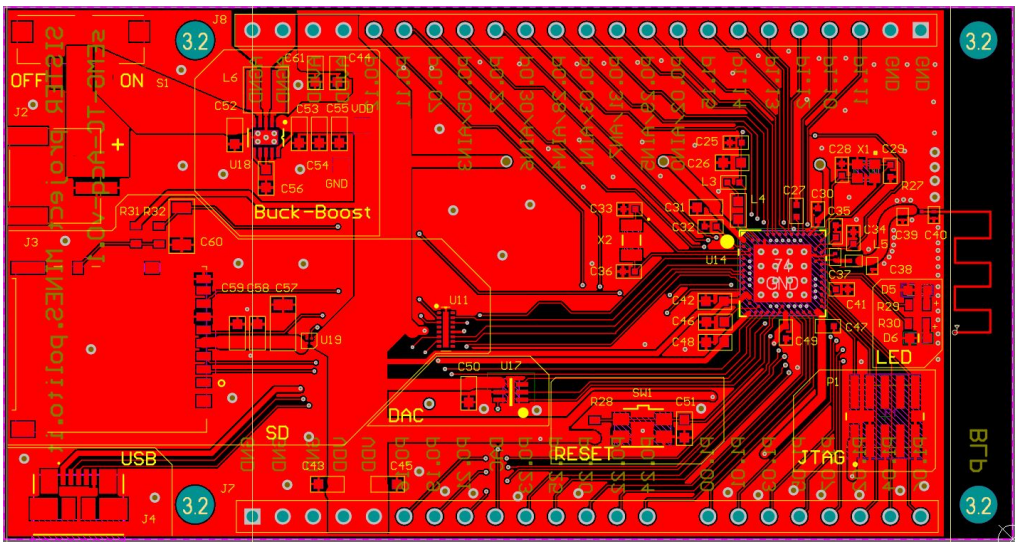

Figure 3.18. Main Board PCB Top

At the left edge of Top Layer the micro USB connector J4, the micro SD connector J3, the power supply connector J2 and the mechanical switch to turn on the system S1. The power supply trace starting from the battery connector is kept huge to allow the current to flow with a parasitic resistance

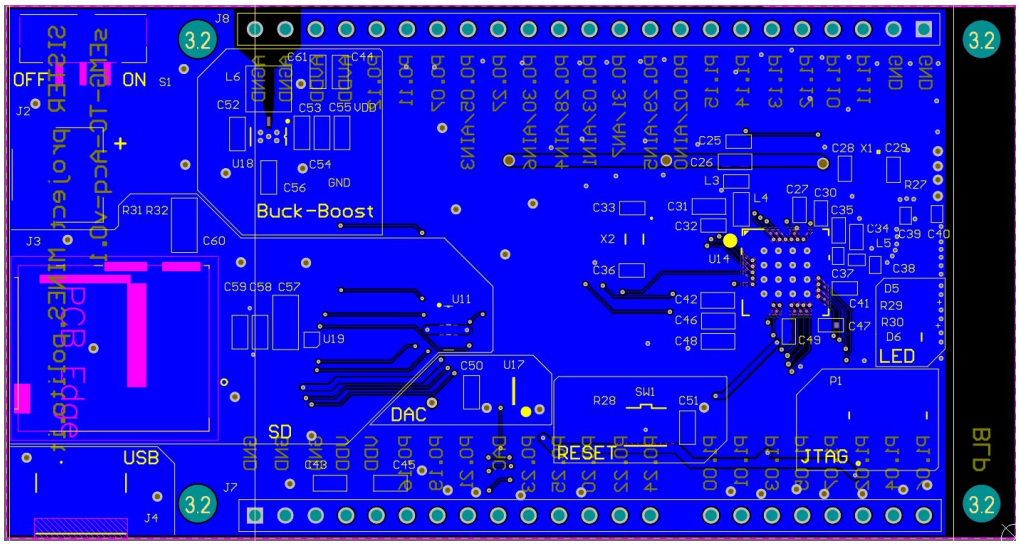

Figure 3.19. Main Board PCB Bottom

as small as possible. This trace reaches the buck-boost U18 when the switch is turned on. The buck-boost has a pin for the analog ground and two for the digital ground (one of these is the ground pad beneath the component). They need to be separated and connected only in one point. The analog ground infact is connected to the ground pad and reaches the first 2 pins at the right of the J8 header. The digital ground plane is removed beneath it to avoid any influence. The power supply regulated by the buck boost flows in a power plane where is divided to supply each components. The third and fourth J8 header pins at the left are close to the regulator output and served for the analog module power supply to reduce as possible the supply fluctuation given by the burst current required by the SD operations. The supply is connected also to the fourth and fifth pins of the J7 header at the left. Near these pins capacitors have been placed for an immediate current request by other modules. Also the SD interface is kept as close as possible to the power supply to provide it current spikes as fast as possible. On the right the meander antenna is placed and the microcontroller is placed as close as possible to it. The impedance matching circuit between them has been imitated from the Nordic Dongle. The microcontroller is a BGA with 2 pins crowns. The microcontroller pad pitch is 0.5mm and their diameter is 0.275mm. The distance between them is thus 0.275mm. Since the minimum track width and distance is 0.1mm for many manufacturer, 0.3mm available are needed to let a trace pass between two pad. The solution used to route

those pins out is the one suggested also by the nRF52840 reference design and is to put filled microvias beneath the pad. These increase the manufacturing costs.
All the decoupling capacitors have been placed near the component power supply pin. The ground plane has been placed on the uncovered area to reduce the traces crosstalk and vias have been spread to achieve an equipotential plane as ideal as possible. An area around the antenna has been kept out from the ground plane to keep the antenna radiation diagram without obstacles. The ground plane would reflect the air signals. On the Top Silkscreen each component and its name are highlighted for an easy visual inspection.
The Bottom Layer (Figure 3.19) is reserved mostly for the ground plane and for some information on the silkscreen. Particularly the name of the project, the website of the group, the signature of the author and the name of each microcontroller pin routed out to the pin headers. The ground plane has been kept out also under the analog ground of the buck-boost.
In Figure 3.20 and 3.21 the 3D view of the acquisition channel module.

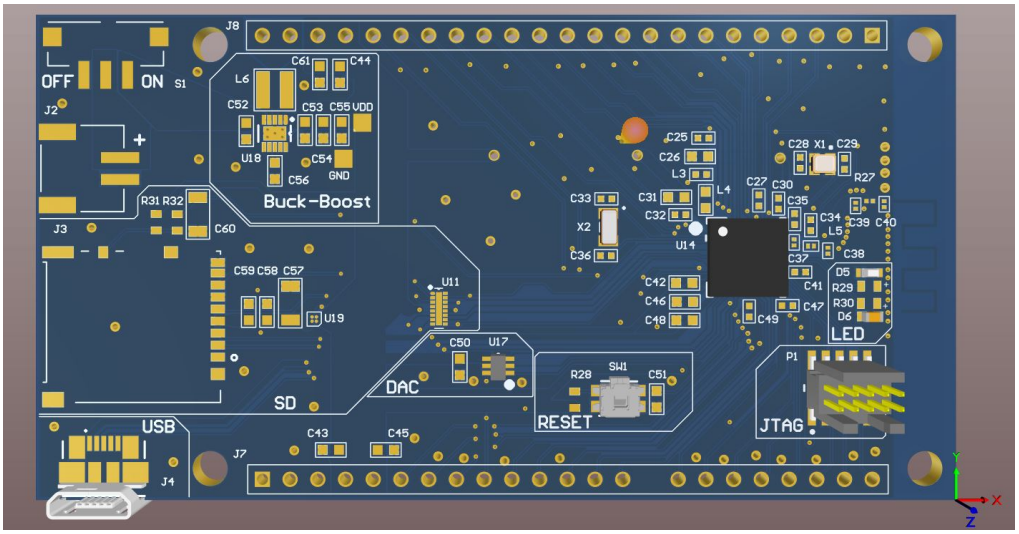

Figure 3.20. Main Board End PCB 3D Top

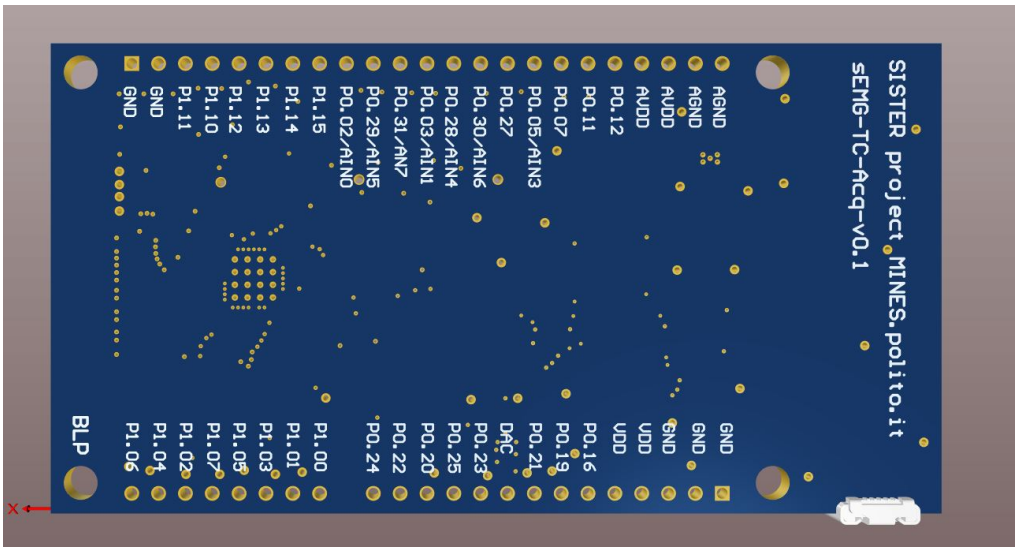

Figure 3.21. Main Board PCB 3D Bottom

Chapter 4

Firmware

A new version of the firmware has been developed in order to adapt it to the new hardware. In particular has been introduced:

- A function to set the Switch SPST control pins to select the wanted gain in the acquisition channel second amplification stage;
- An interrupt for handling insertion of the micro SD card;
- The ADC configuration for the new sEMG voltage range.

Two different firmware are present, one for the slaves and one for the master.

4.1 Slaves

The high level flowchart of the slaves firmware are reported in Figure 4.1. At reset, a first phase consists in the initialization (section 4.1.1) of the peripherals and variables used in the program. Thus the GPIOs, interrupts, Peripheral Programmable Interconnect (*PPI*), timers, power management and radio protocol are initialized. Then the threshold for the Threshold Crossing stage in the acquisition channel is defined by a Threshold Definition algorithm (secton 4.1.2) and the slave can finally enter in RX mode and wait for an event. The first packet to be received from the master brings information about the working mode to operate. The working modes regards which data to process and store in the micro SD card and can be *RawData*, *Envelope* or *ATC* (in section 4.1.3 are analyzed). After set the working mode the slaves wait for the second RX event that brings the start command

flag. The core of the firmware is now reached and here the firmware is constantly woken up from interrupts for the acquisition (section 4.1.3) or the synchronization (section 4.1.4) routines.

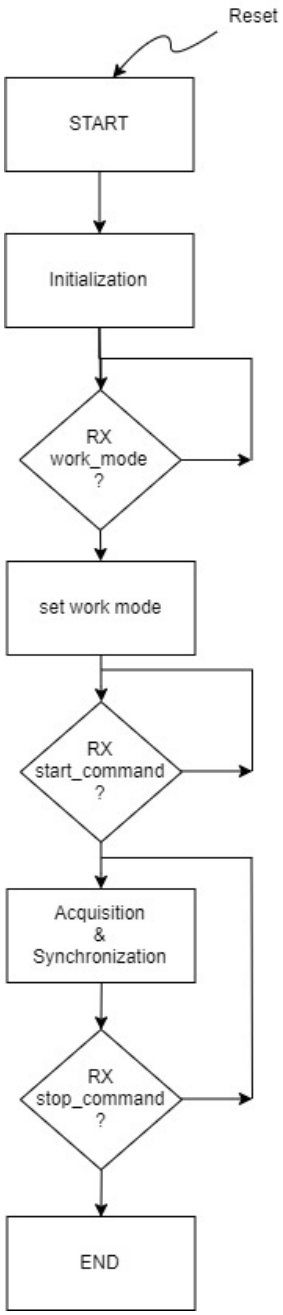

Figure 4.1. Slave High level flowchart

4.1.1 Initialization

The peripherals initialized in the first phase of the firmware are here reported:

- **GPIO**
  2 GPIOs are used to manage the green and reds led present on the board during the different phase of the program and for visual information;
  4 GPIOs are used to manage the Switch SPST control pins to select the wanted gain in the acquisition channel second amplification stage;
  1 for the enable of the high load power switch for supplying the SD card;

- **GPIOTE**
  The GPIO Task and Event (*GPIOTE*) manage the interrupts on the GPIOs.
  1 GPIO is initiliazed to be sensitive to the rising edge of the TC signal;
  1 GPIO is initiliazed to be sensitive to the rising or falling edge of the micro SD insertion to manage its power supply.

- **SAADC**
  The Succesive Approximation Analog to Digital Converter (*SAADC*) is initialized in order to sample the sEMG signal. It is configured to 14-bit resolution. The input range is configured as

$$InputRange = \frac{Reference}{Gain} \tag{4.1}$$

  The reference can be the internal 0.6V or $\frac{VDD}{4}$. $\frac{VDD}{4}$ has been chosen as reference voltage and $\frac{1}{3}$ as gain obtaining as input range 2.475V. The SAADC callback has been defined to work differently according to the working mode set.

- **DAC**
  The external Digital to Analog Converter (*DAC*) is initialized in order to provide the threshold to the be used from the acquisition channel Threshold Crossing stage to generate the TC signal. The SPI to communicate with it is thus initialized and the value generated is decided by the Threshold Definition algorithm (section 4.1.2).

- **Radio Protocol**
  The Enhanced ShockBurst (*ESB*) protocol is initialized. It is a bidirectional low power consumption 2.4GHz wireless communication protocol introduced by the Nordic. It supports a star topology with one Primary

Receiver (the master) and up to 8 Primary Transmitters (the slaves). During communications, if the Primary receiver does not receive a feedback within 30ms an automatic re-transmission is performed, thus for each communication the nodes need to switch from TX to RX and viceversa.

- **Peripheral Programmable Interconnect**
  The Peripheral Programmable Interconnect (*PPI*) uses task and event independent from the CPU to enable peripherals to interact with each other autonomously to eliminate the CPU activity. A set of additional channels can be added to ordinary PPI channels and for each of them an Event End Point (*EEP*) and a Task End Points (*TEP*) are fixed in hardware.

- **Timers**
  Timers are initialized to manage tasks by means of interrupts reducing the CPU process. Three of them are used:

  TIMER1: initialized and started each time a synchronization packet is received, uses the 16MHz external oscillator. Two Capture & Compare (*CC[x]*) registers are used with it.
  CC[0] is used to wait an amount of time such that the master had already sent to all the slaves the packet and had switched to RX mode. After this time the slave composes the tx payload and sends it to the master to let him know that the synchronization packet has been received. The time is function of the number of slaves in the system and particularly is $10ms + 30ms \times (\#slaves - 1)$.
  CC[1] is used to wait an amount of time such that the said functions for the CC[0] is have been completed. After this time the esb is disabled to save power and the Real-Time Counter is initialized and started to re-enable the esb for the next synchronization. The time to wait is function of the number of slaves in the system and particularly is $10ms + 30ms \times (\#slaves + 5)$.

  REAL-TIME COUNTER: initialized and started after each synchronization routine is completed and the esb disabled, it is a low power counter that uses the 32.768kHz external oscillator. It counts the time the esb can be disabled, saving power, until the next synchronization routine. It is ok to re-set the slave in RX mode 500ms before the master should

send the synchronization packet.
CC[0] is used to trigger the end and since the currently the synchronization routine is performed each 5s, it counts 4.5s. After that it is deinitialized.

TIMER4: Initialized only at the beginning of the program, it has multiple functions depending on the phase of the program it is working in and it uses the external 16MHz oscillator.
CC[3] is triggered every ms and it is used to trigger the ADC sampling, to count the 260ms window during the Threshold Definition algorithm (section 4.1.2), to let the slaves start or stop sampling at the same time after the time information sent from the master together with the start_command or the stop_command.

- **Micro SD Card**
  7 First Input First Output (*FIFO*) structure with 500 cells each are initialized in order to save the data to be stored in the micro SD card. To reduce the number of writings and to allow the data acquiring to be independent to the data storing, the data are stored in the FIFO structures and when a FIFO is full, an SD writing is perfomed meanwhile another FIFO block is being filling with the new data. A GPIOTE is initialized to know when the SD is inserted in order to set the enable pin of the high load power switch and thus let the SD to be supplied.

- **Power Management**
  The internal DC-DC regulator has been enabled instead of the LDO for its power consumption savings and the power management is initialized. It is in charge to supply the microcontroller peripherals depending on the current they required and saving power when possible.

4.1.2 Threshold Definition Algorithm

After the initialization phase, the threshold for the Threshold Crossing stage of the acquisition channel is defined. An algorithm is followed in order to find the best fixed threshold that is close enough to the baseline noise to discriminate every activation and at the same time far enough to reject the noise. The flow chart of the algorithm is in Figure 4.2. The threshold is generated by the DAC and an initial value greater than the baseline is set (the baseline is around 1.25V). The threshold is reduced each time by 10

until a first threshold crossing edge is sensed by the GPIOTE connected to the comparator output. The edge sensed can be the baseline noise or just a random spike for a weak contraction. The second part of the algorithm prevents the definition of the threshold due to the spike. Two variable are used to manage the algorithm:

- flag_window: is set to 1 when the first TC is sensed and it set to 2 by a timer after 260ms (double the ATC window) to enter in the second part and it set again to 1 to enter again in the loop of the second part after other 2 time windows have lasted. After two time window, thus, the number of crossing counted are analyzed:
  if $0 <$ TC_events < 4: the threshold is close enough to sense each activation and far enough to not compromise the TC signal by the noise. flag_window is set 0 and the algorithm ends;
  if TC_events ≥ 4: the threshold is too close to the baseline and it is increased by 5;
  if TC_events $= 0$: no other crossing have been counted thus the threshold is too high and the edge sensed in the first part was a spike. It is decreased by 5 until a threshold events is generated. At this point the count variable is increased.

- count: is used to avoid an infinite loop in the algorithm or to discard a threshold due to a random spike. Count is initially set to 0 and it is increased the first time if the algorithm has reached the second part thanks to a random spike. At this point, after other two time window the number of crossing is counted again and the TC_events are evaluated as said. The threshold could remain stacked increasing and decreasing by 5 around its value where the TC_events are 0 when increased and 4 or more when decreased. The variable counts is in this case used to exit from this loop when it reaches the value 3.

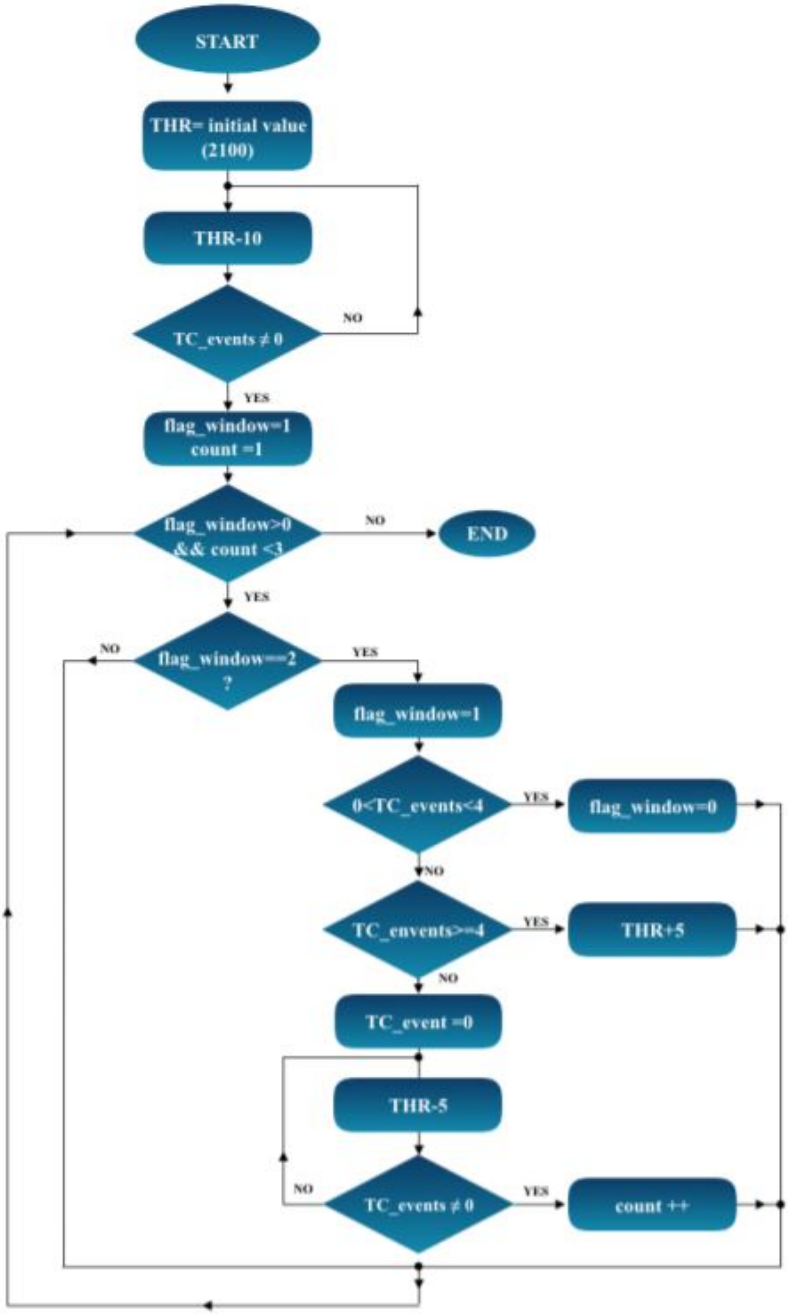

Figure 4.2. Threshold Definition Algorithm

4.1.3 Work Modes

The master sets the slaves working mode with the first wireless packet sent. Three are the working modes: Raw Data, Envelope, ATC. Their routine are triggered each ms by the same timer that triggers the ADC.

Raw Data

In this mode the whole sEMG signal is sampled and stored in the micro SD card (Figure 4.3). The signal is sampled by the ADC each ms, stored in a FIFO and a variable (sample_counter) that counts the number of sampling performed is updated. When the variable reach the FIFO length (500 cells), it is reset, the writing of the FIFO in the SD card is triggered and another FIFO is selected for the next temporary storing. The FIFO available are 7 so that the SD writings and the sampling can be independent. The writing are thus performed each 500ms

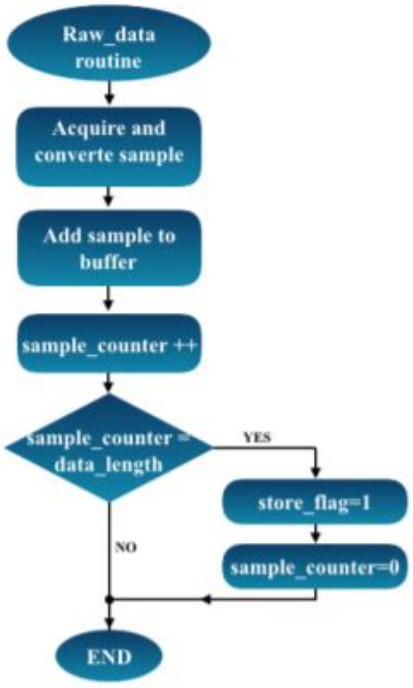

Figure 4.3. Raw Data routine

Envelope

In this mode the whole sEMG signal is sampled, its envelope is performed digitally and saved in the SD Card (Figure 4.4). Each sample pass through a 2^{nd} Order Butterworth High Pass filter to remove the DC and the absolute value is calculated. A 10 Hz 4^{th} order Chebyshev Low Pass filter is then applied to obtain the envelope. Twenty raw samples are thus reduce to an envelope one that is stored in a 500 cells FIFO structure. When the FIFO is full the SD writing is started and another FIFO is selected to store the next samples. The SD writings are performed each 10s.

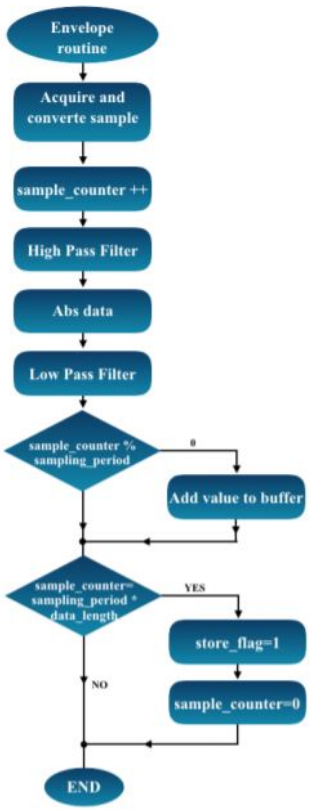

Figure 4.4. Envelope routine

ATC

In this mode the number of threshold crossing events are counted each fixed window of 130ms (this value is used because is suitable to study the gait)

(Figure 4.5). Each ms the variable ATC_counter is increased and when it reach the window size the number of TC_events are stored in a 500 cells FIFO structure. When the FIFO structure is full the SD writing starts and another FIFO is selected to store the new values. In this way a sample is generated each 130ms instead of ms and the SD writings are performed each 65s.

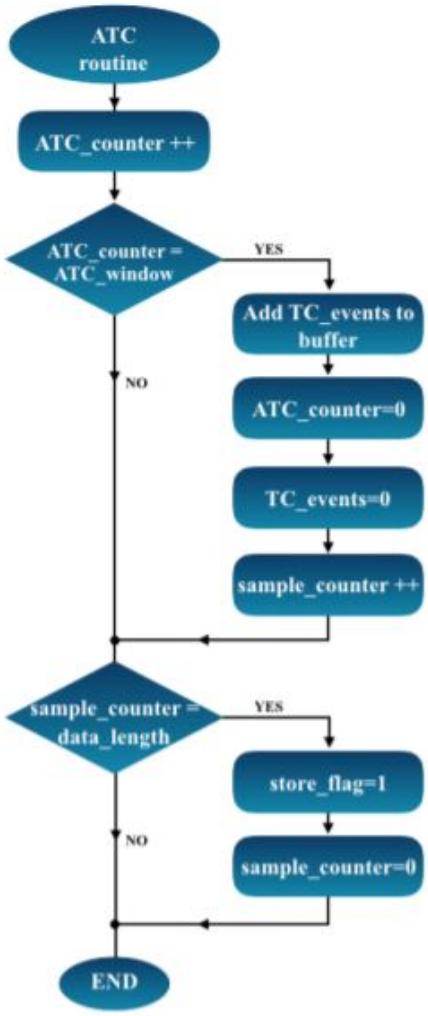

Figure 4.5. ATC routine

4.1.4 Synchronization

In a system with multiple slaves which have to perform concurrent operation the synchronization in important. The slaves synchronization routine is reported in Figure 4.6. With the start command the slaves start operating at the same time. Tolerance of the oscillators can cause desynchronizations of the sampling generating a set of signals acquired that cannot be used together. To avoid this, every 5s the master sends to the slaves a synchronization packet that brings its clocks information so that the slaves can realign their timing with it. The delay of the transmission (*TX_chain_delay*) is firstly added to the timer value sent by the master (*Master_timer*). If with this addition the master timer value exceed the maximum value reachable by the timer (*timer_max_val* equal for master and slave), the maximum value is subtracted obtaining a value in the range. The offset (*timer_offset*) to be load in the slave timer to realign it with the master one can now be found. If the slave timer (*local_timer*) is greater than the master timer, the slave is faster and it need to wait to restart again the timer from zero at the same time of the master. The value to be loaded and reached by the slave timer to resynchronize the system is thus difference between the slave local timer and the master one. If the slave is slower, the value to load is instead the same maximum decreased by how much the master timer is in in front of the slave one. When the slave reached the value loaded the timer restarts to count synchronized to the master one and the variable *Local_counter*, that counts the number of samples, is adjusted to realign the slaves acquisition.

4.2 Master

The high level flowchart of the master firmware are reported in Figure 4.7. At reset, a first phase consists in the initialization of the peripherals and variables used in the program. With respect to the slaves firmware, the ADC, DAC, FIFOs and GPIOTEs to manage the acquisition and the analog channel are not initialed. Four GPIOTEs connected to 4 buttons are instead initialized to set the slaves working mode and to send the start command. After the initialization phase it enters in a wait for event state and is waken up by the pressing of one button:

- Button0 : is used to set the Raw Data slaves working mode;
- Button1 : is used to set the Envelope slaves working mode;

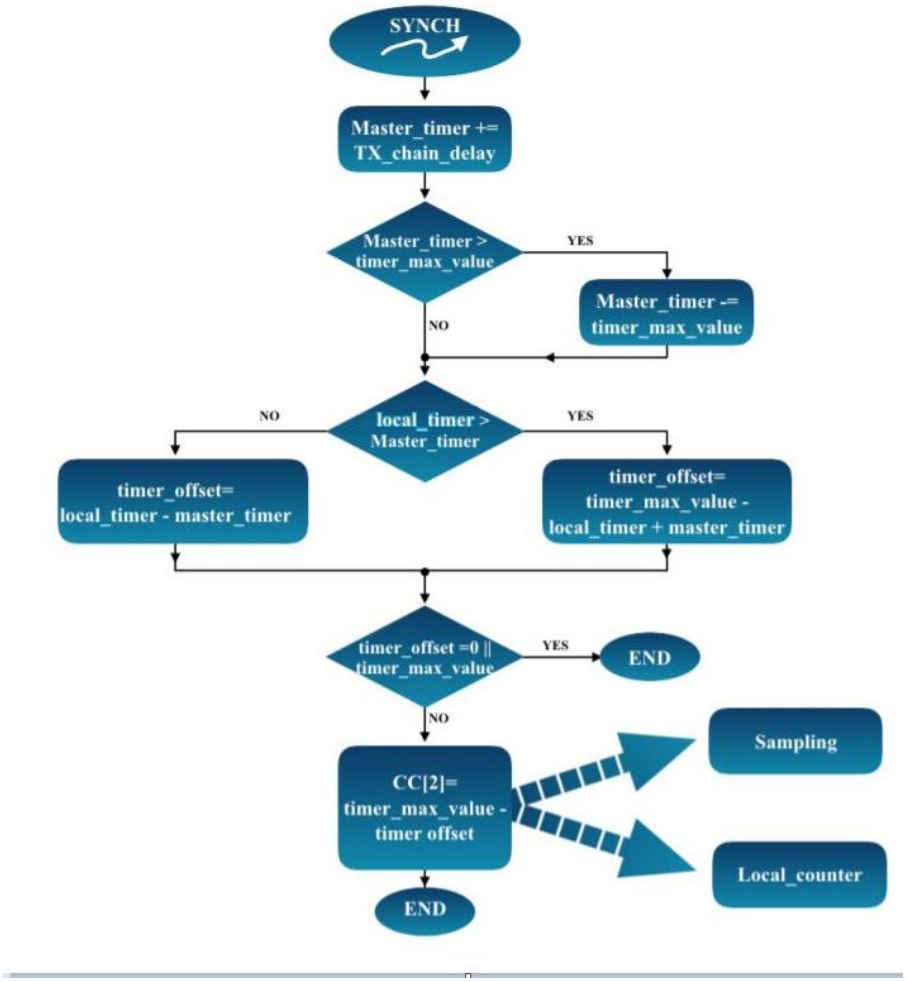

Figure 4.6. Slaves Synchronization flowchart

- Button2 : is used to set the ATC slaves working mode;

When one of them is pressed, the master sends the working mode to the slaves and when receives all the feedbacks from them it enters it is ready to send the start command. It is sent when the Button3 is pressed and from this point the task of the master is to mantain the slaves synchronized. When the synchronization is triggered the master sends its clock information to the slaves which adjust their timer and eventually sample misalignment. With a new pressing of the Button3 the master sends the stop command and the system is turned off.

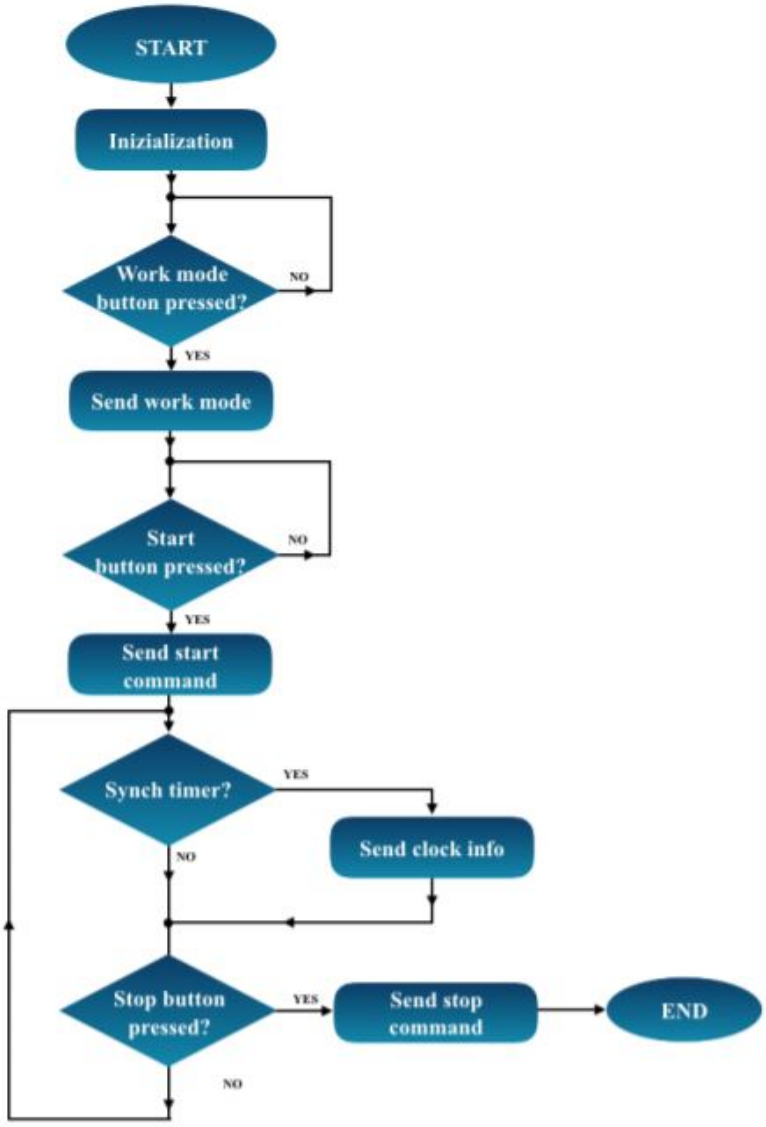

Figure 4.7. Master High Level flowchart

Chapter 5

Experimental Tests

The two boards have been fabricated and soldered by Proto-Electronics, the device assembled has been reported in Figure 5.1, while the analog acquisition channel and the main board alone are reported in Figure 5.3 and 5.2 respectively.

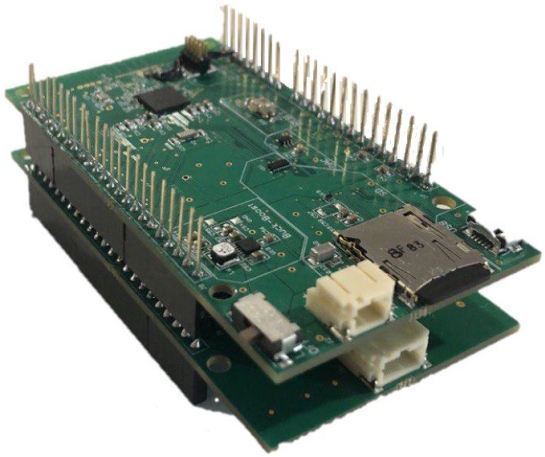

Figure 5.1. Two modules system assembled

In this chapter experimental tests on the two board have been performed, particularly the improvement for the two issues faced in the precedent works (INA Saturation 5.1 and Periodic Drop Out 5.2) have been verified. The bandwidth of the acquisition channel is then characterized (Bandwidth 5.3) and the correct behaviour of the five programmable gains have been tested (Programmable Gains 5.4). The three working modes are then tested (Working Modes 5.5) and in the last section finally the power consumption of the

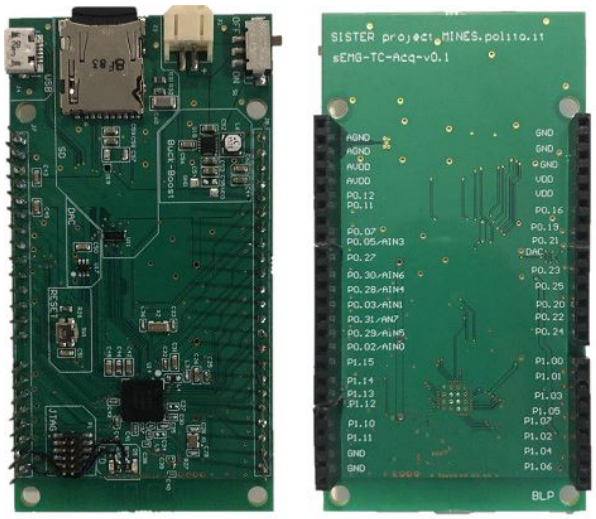

Figure 5.2. Main board top and bottom view

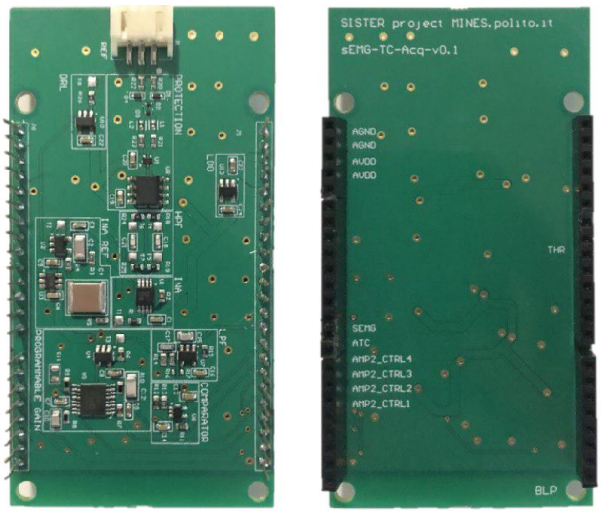

Figure 5.3. AFE module top and bottom view

acquisition channel alone and the one of the system assembled is measured (Power Consumption 5.6).

5.1 INA Saturation

The previous versions of the system had a problem related to the saturation of the instrumentation amplifier. At the startup its reference voltage grows to the positive power supply voltage because it is the difference of the voltage generated by the voltage reference doubled and the INA output that at the startup is zero. The problem of the precedent INA321 is that it could not manage a reference voltage too high and its response was an output voltage low that positively contributed to this loop (section 2.2). To solve this problem another instrumentation amplifier has been properly chosen (section 2.4.1). The startup transient of the new acquisition channel is the one reported in Figure 5.4.
At startup the instrumentation amplifier output is at high voltage, this means that with an high voltage reference as input it is able to provide an high voltage output. The negative loop can thus converge around the reference voltage allowing the system to work properly.

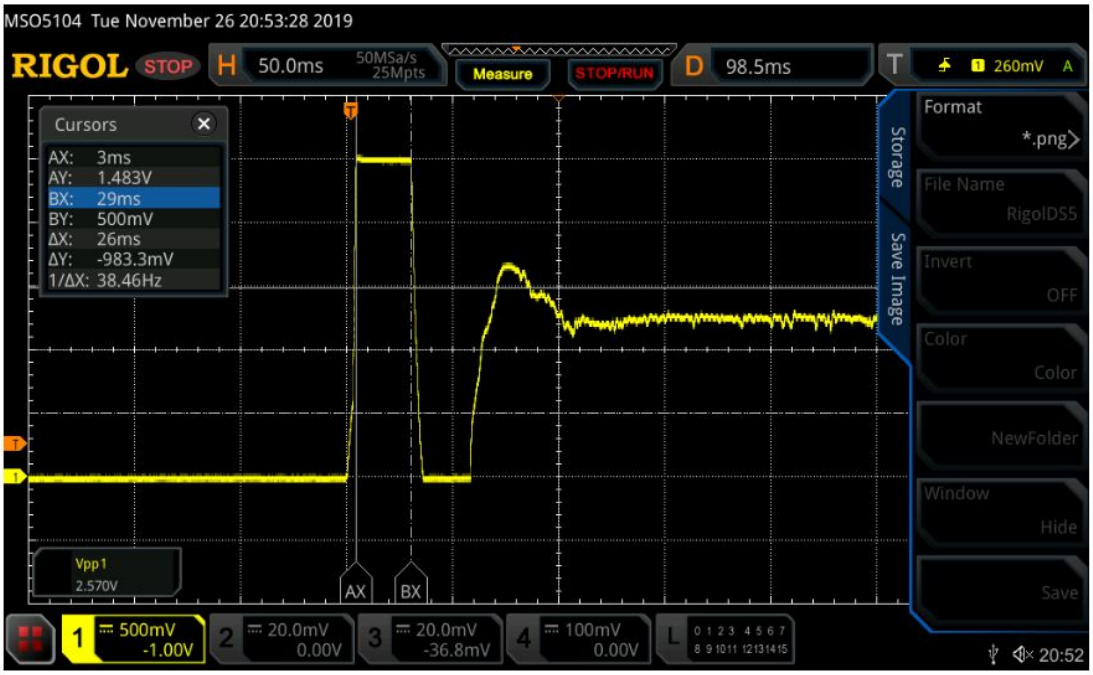

Figure 5.4. Focus on the INA behavior during the startup transient of the Acquisition Channel

5.2 Periodic Dropout

The previous version of the system had a periodic dropout voltage visible in sEMG signal output (section 2.3). This dropout is generated on the power supply by the periodic writings on the SD Card which require a big burst of current that the low drain coin battery alone and the boost voltage regulator used were both not able to provide without lowering the voltage. Since the voltage reference of the INA was generated by resistive voltage divider, each fluctuation on the power supply are reflected on the INA output signal (Figure 5.5 and 5.6).

The voltage regulator has been changed in the new system choosing the buck-boost TPS63031 that can provide a more stable output current and voltage, capacitors on the SD power supply trace and an high load power switch to provide an immediate current source dumping the capacitors recharging, and designing the PCB with power supply traces wider. Furthermore the analog acquisition system has an additional 2.5V low drop out regulator (*TPS782*) and the INA reference is generated by a 1.25V voltage reference

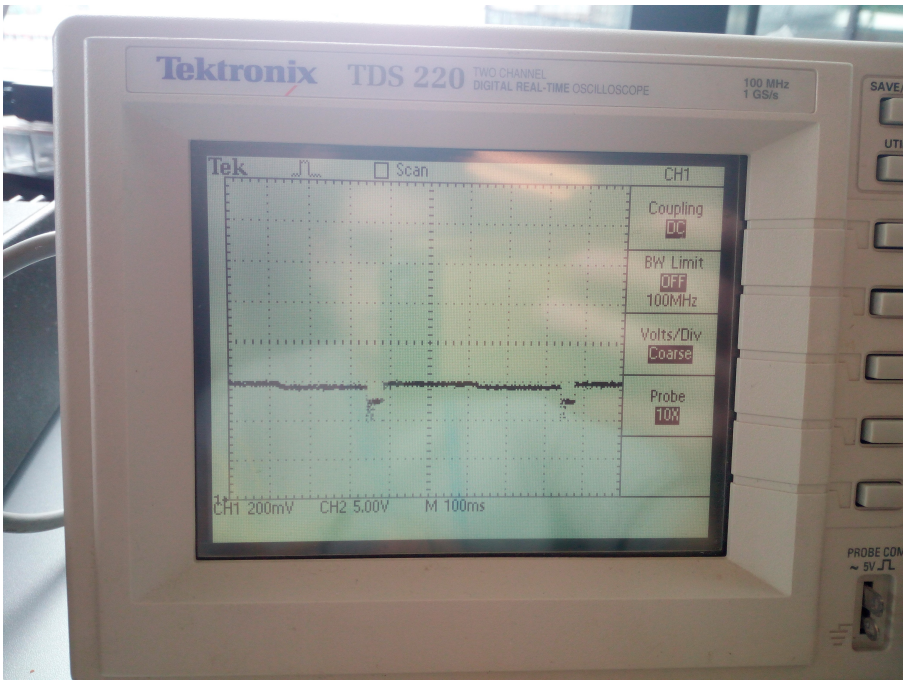

Figure 5.5. Dropout voltage on the INA reference during the SD periodic writings in the precedent versions of the system

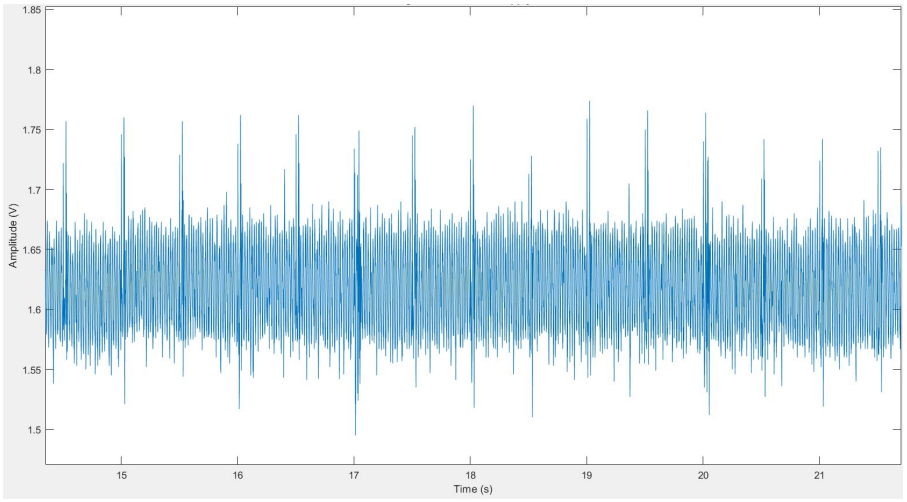

Figure 5.6. Baseline of sEMG signal acquired influenced by power supply dropout voltage during the periodic SD writings in the precedent versions of the system

(*LT6656*).
The power supply has been monitored with the oscilloscope during the SD writings and following its paths through the regulators. Coupling has been set to AC. About 200mV peak voltage drop can be seen on the battery terminals (Figure 5.7). After the buck boost regulation the peak are reduced by 75% (Figure 5.8) obtaining a voltage drop of 47.78mV that does not influence the component on the digital board.

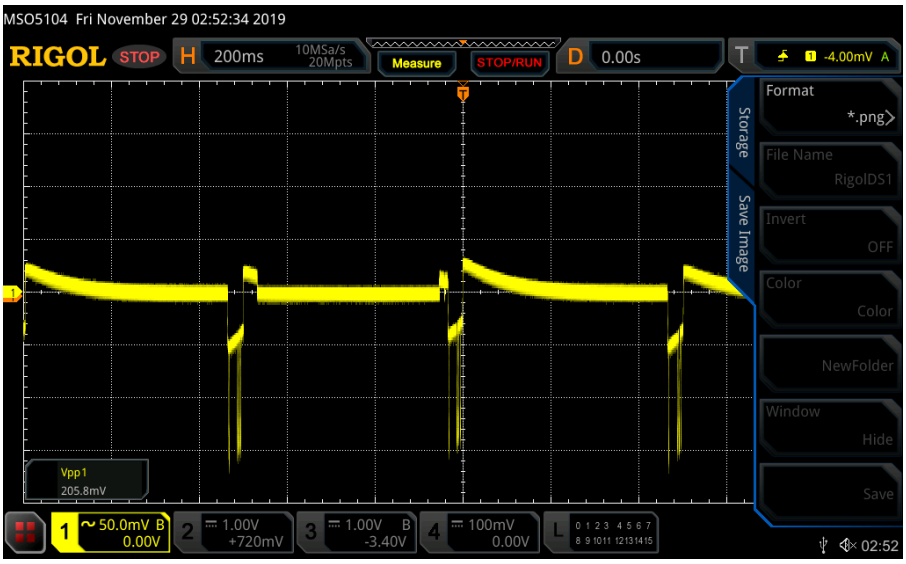

Figure 5.7. Dropout voltage on the battery terminals during the SD periodic writings in the new version of the system

The supply voltage is regulated again in the acquisition channel module by a 2.5V LDO regulator whose output let see only few mV of peaks out of the 2.5V baseline (5.9). The voltage reference then generates the 1.25V INA reference that directly impacts on the INA output. Figure 5.10 shows that the influence of the peaks in the reference voltage generated is negligible.

5.3 Bandwidth

The bandwidth of the system has been characterized by using a sinusoidal signal generated with the signal generator Agilent 33250A, varying its frequency and observing the signal attenuation. To reproduce two signals for the acquisition channel input a resistive voltage divider with 3 resistors has been adopted. Two of them are $2.2k\Omega$ resistors and between them a 10Ω

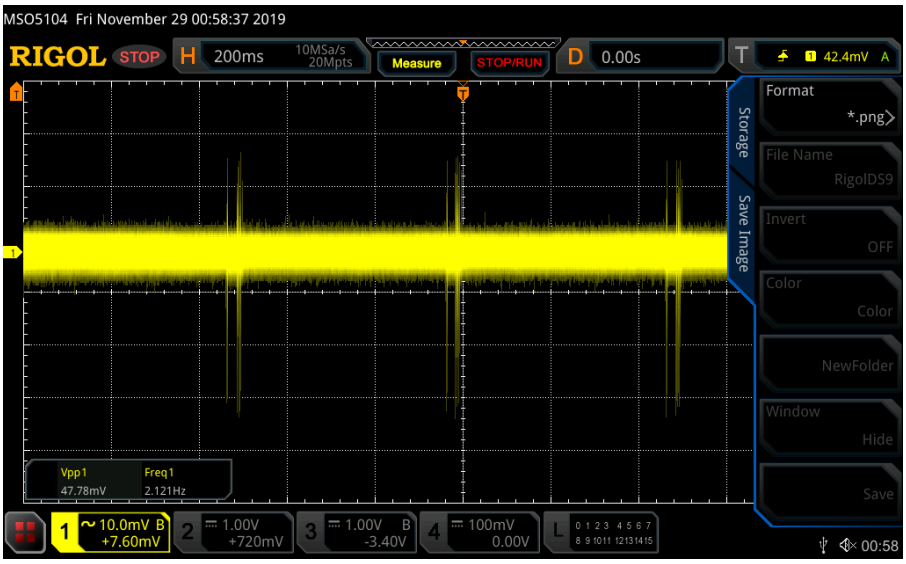

Figure 5.8. Dropout voltage on the buck-boost output during the SD periodic writings in the new version of the system

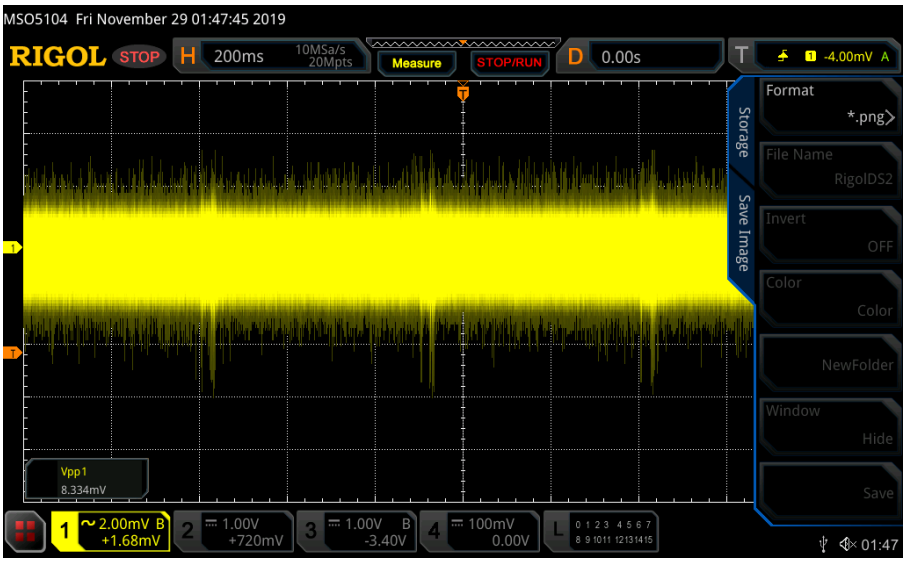

Figure 5.9. Dropout voltage on the acquisition channel LDO output during the SD periodic writings in the new version of the system

resistor has been placed. From its terminals the signal is picked. Since the signal generator output has been reduced by a factor of $\frac{10}{2200+2200+10} = 0.0227$, a sine waveform with 100mV amplitude has been set. The gain has been set to 500 an the actual gain with respect to the frequency is in Figure 5.11.

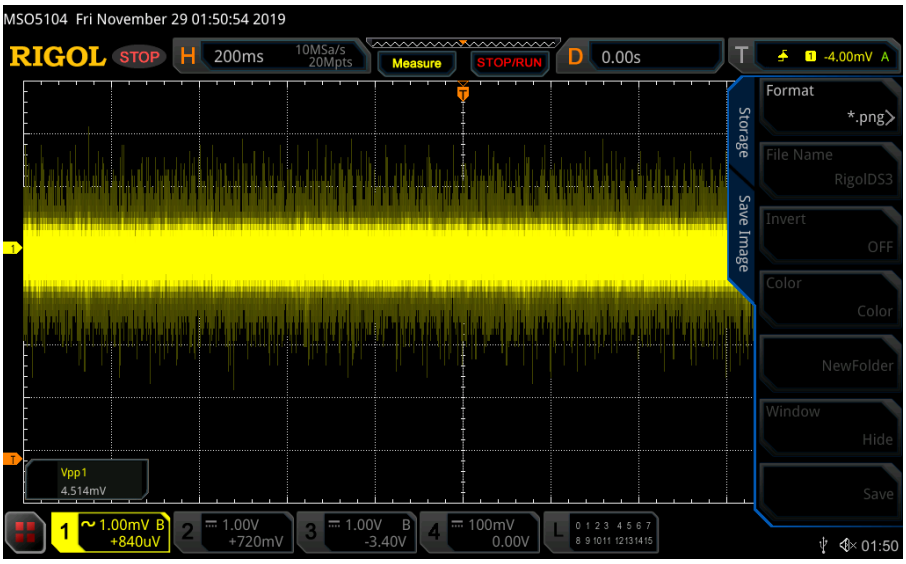

Figure 5.10. Dropout voltage on the acquisition channel 1.25V voltage reference output during the SD periodic writings in the new version of the system

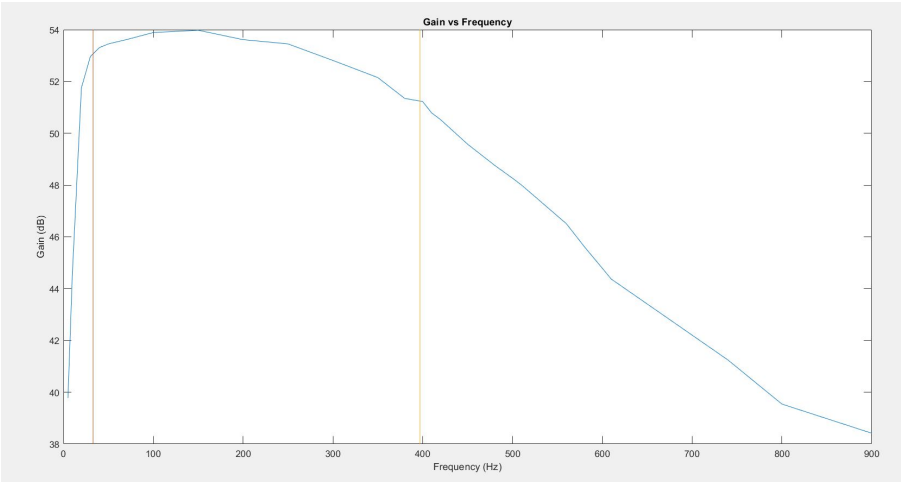

Figure 5.11. Gain variation with respect to the input signal frequency. Gain of the acquisition channel is set to 500.

5.4 Programmable Gains

All the gains have been tested using a sinusoidal signal generated with the signal generator Agilent 33250A. To reproduce two signals for the acquisition channel input a resistive voltage divider with 3 resistors has been adopted.

Since the highest gain is 3000 and thus an INA delta input of $0.83\mu V$ may saturates the dynamic the acquisition channel inputs signals should be correctly attenuated thinking also to the delta DC voltage between them and their tolerance. Two $2.2k\Omega$ of three resistor have been selected and between them a 10Ω resistor has been placed. From its terminals the signal is picked attenuated by other 0.00227V/V. The signal generator has been set to generate a 150Hz frequency, 100mV amplitude sine wave with DC offset 600mV and signal output with the 5 different gains are reported. The amplitude of the differential signal on the board input should $100mV \times 0.00227 = 0.227mV$ that amplified by 500 is around 113.5mV.
Figure 5.12 show the signal output with the 500 gain configuration and thus the second amplification stage acting as a buffer. The signal has an amplitude 390mV because also the contributes of the offset drift on the 10Ω resistor has been amplified.
Figure 5.13 show the signal output with the 1000 gain configuration, thus gain $\times 2$ is selected in the second amplification stage. The signal has an amplitude of 716mV that is close to the ideal $390mV \times 2 = 780mV$.
Figure 5.14 show the signal output with the 1500 gain configuration, thus gain $\times 3$ is selected in the second amplification stage. The signal has an amplitude of 1097mV, close to the ideal $390mV \times 3 = 1170mV$.
Figure 5.15 show the signal output with the 2500 gain configuration, thus gain $\times 5$ is selected in the second amplification stage. The signal has an amplitude of 1858mV, close to the ideal $390mV \times 5 = 1950mV$.
Figure 5.16 show the signal output with the 3000 gain configuration, thus gain $\times 6$ is selected in the second amplification stage. The signal has an amplitude of 2135mV, quite close to the ideal $390mV \times 6 = 2340mV$.

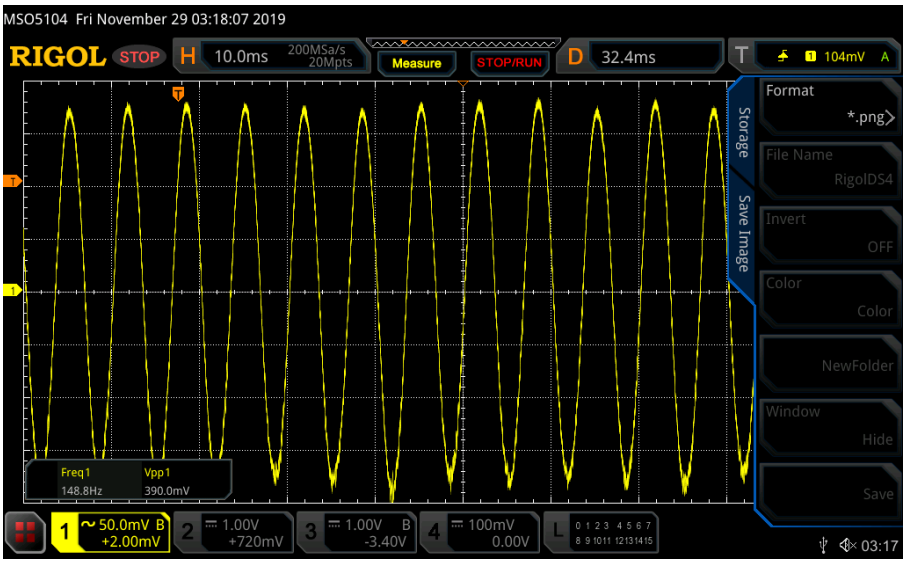

Figure 5.12. Gain 500 test with hundreds of μV in INA differential input

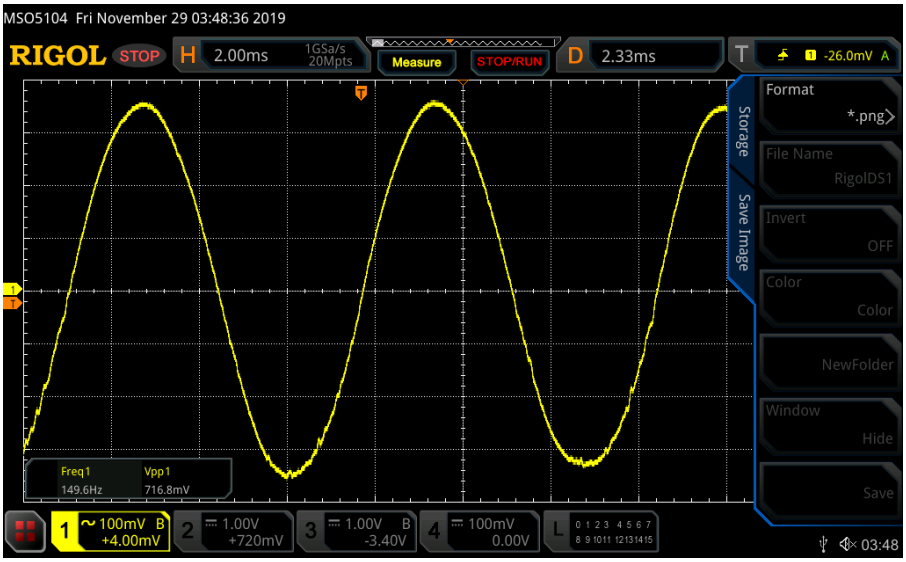

Figure 5.13. Gain 1000 test with hundreds of μV in INA differential input

5.5 Working Modes

Three working mode are present one the system and settable by the master during the first transmission. Data has been recorded with the three modes and plotted using Matlab, in the following section the results are reported.

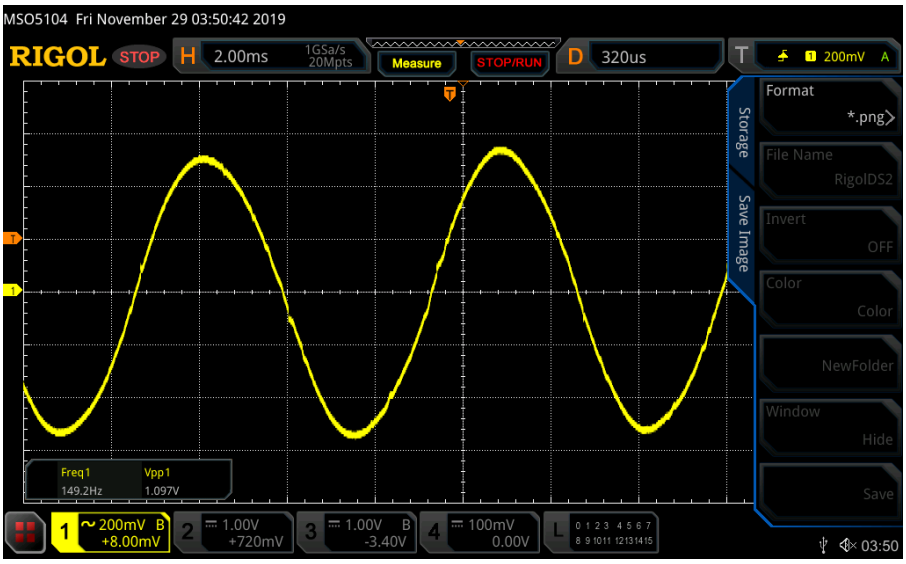

Figure 5.14. Gain 1500 test with hundreds of μV in INA differential input

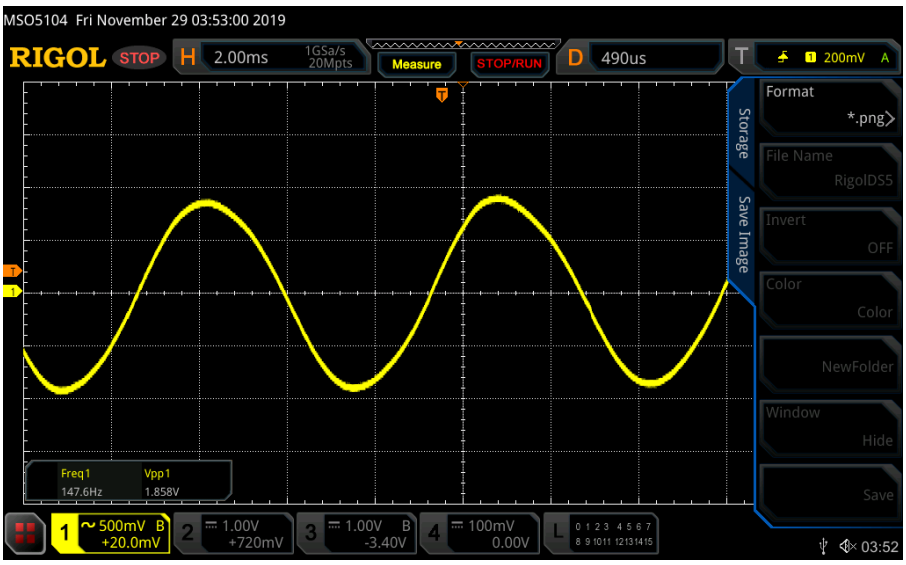

Figure 5.15. Gain 2500 test with hundreds of μV in INA differential input

5.5.1 Raw Data

In Raw Data mode the system samples the whole sEMG signal with a frequency of 1kHz. The signal acquired during the wrist extension is reported in Figure 5.17.

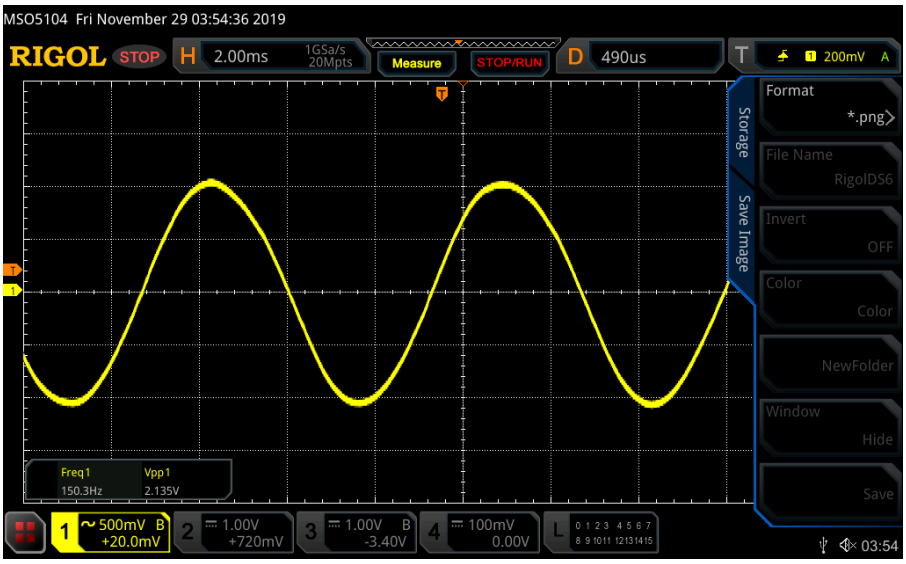

Figure 5.16. Gain 3000 test with hundreds of μV in INA differential input

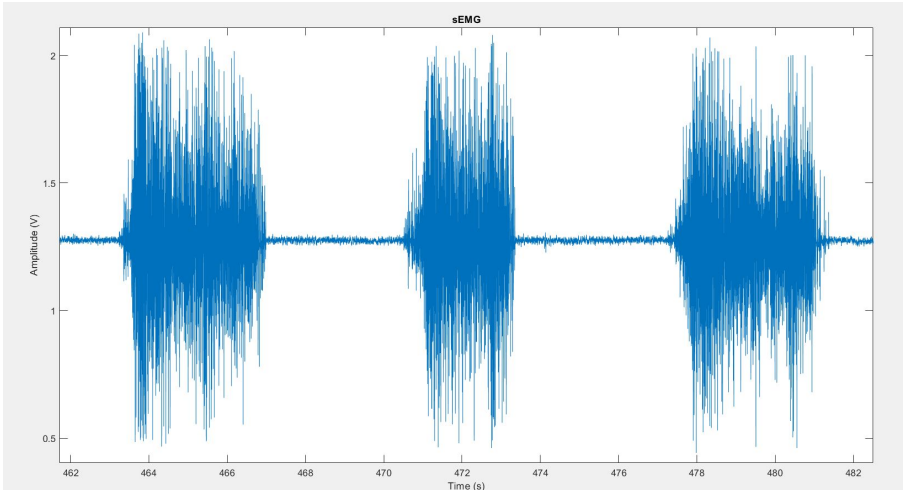

Figure 5.17. Wrist extension acquired in Raw Data mode

5.5.2 Envelope

In Envelope mode the system samples the whole sEMG and post processes it in order to extract the envelope. The signal is sampled at 1kHz and a 2^{th} order Butterworth High Pass filter is applied to remove the DC component. The absolute value is thus calculated and the 10Hz 4^{th} order Chebyshev Low Pass Filter is applied in order to extract the envelope. The enveloped

acquired during the wrist extension is reported in Figure 5.18.

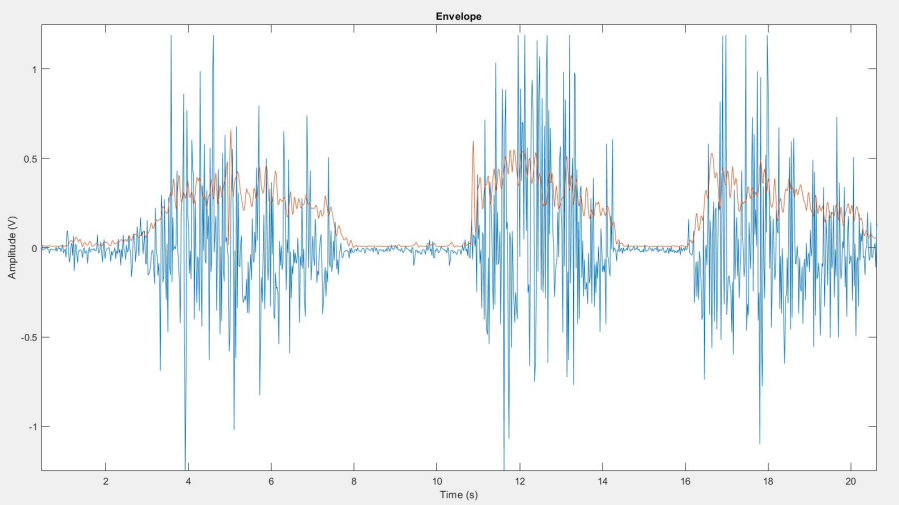

Figure 5.18. Wrist extension acquired in Envelope mode

5.5.3 ATC

In ATC mode the system acquires only the number of sEMG threshold crossing events in a fixed 130ms window. It gives information about the force of the activation. The ATC acquired during the wrist extension is reported in Figure 5.19.

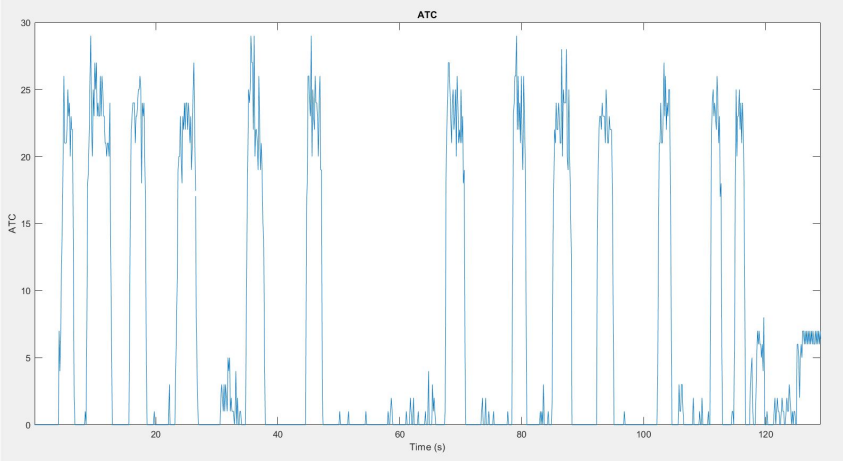

Figure 5.19. Wrist extension acquired in ATC mode

5.6 Power Consumption

The estimation of the power consumption has been performed using the DMM7510 7½-Digit Graphical Sampling Multimeter on the analog acquisition channel alone and on the 2 board system assembled for the three working modes. The results are reported below.

5.6.1 Analog Acquisition Channel

Power consumption analysis has been performed on the analog acquisition module because it can work as a stand alone module. It has been carried out during in vivo test and, as can be appreciate from Figure 5.20 where three maximal voluntary contractions are distinguishable, the power consumption is modulated by the input signals. During the muscle rest states, the current load of the AFE is $55.93\mu A$, whereas reaches a maximum peak of $76.40\mu A$ during the first contraction with an average maximal voluntary contraction current load of $64.62\mu A$. The maximum peak power consumption is thus $200\mu W$ and an improvement of a factor 3 is achieved with respect to the previous version [24].

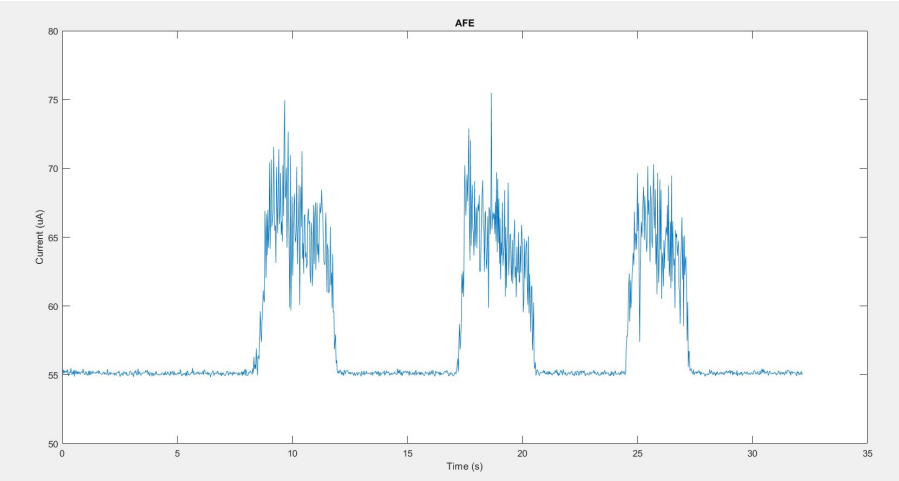

Figure 5.20. Analog Front End power consumption analysis during three maximal voluntary contractions

5.6.2 Two Module System

Power consumption analysis has been performed on the whole system assembled operating in the three different working modes and in the table 5.1 the power consumption optimization achieved is summed up. In the following the power consumption of each of them is analyzed.

Version	Raw Data	Envelope	ATC
Previous	10.56mA	6.48mA	5.65mA
Current	7.98mA	5.58mA	5.07mA
Savings	24%	14%	11%

Table 5.1. Power Consumption comparison of the previous and the current version in the three working modes.

Raw Data

Power consumption analysis during the Raw Data working mode is reported in Figure 5.21. The monitoring is started with system off and at turn on the initialization is performed by the system. It regards the first peak in figure where the main contribute is given by the micro SD card initialization. After that the radio communication is set to RX mode with a power consumption around 16mA. When the working mode is received by the master the slave turns off the radio system and the power consumption falls to around 10mA, from this point every 5s the RX mode is re enabled for the synchronization routine and disabled when expired (the periodic step of 6mA). When the start command is received by the master, the slave turns off all the leds (falling the power consumption to about 5mA). After the amount of time fixed by the master, at 40s the ADC starts sampling. From this point each 0.5s there is a peak for the SD writing of the value sampled. The average power consumption during the acquisition state is $7.98mA$ thus a saving of 24% of Raw Data mode power consumption is achieved from the previous version.

Figure 5.22 shows a focus on the activity. Two synchronization routines can be seen here and each 0.5 the base of the peaks for the SD writings. The less than 1mA peaks regards to the ADC sampling and the writings in the temporary FIFO structures.

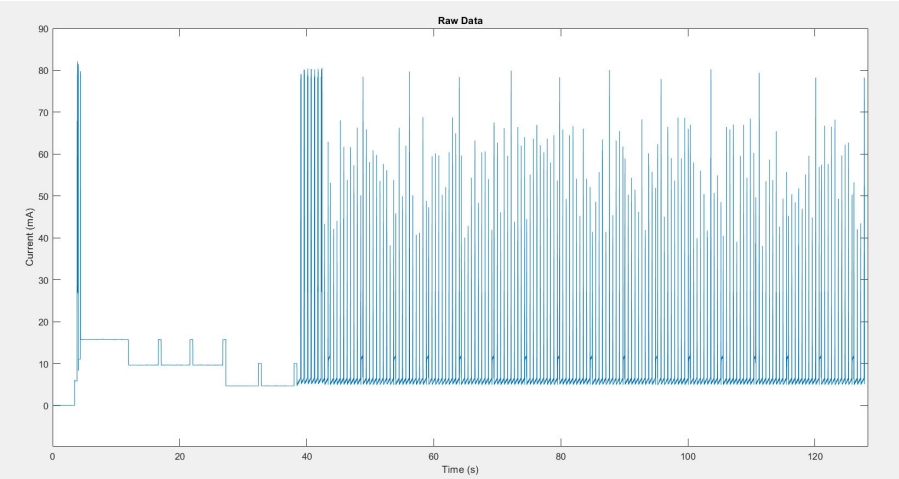

Figure 5.21. Power consumption analysis during Raw Data mode

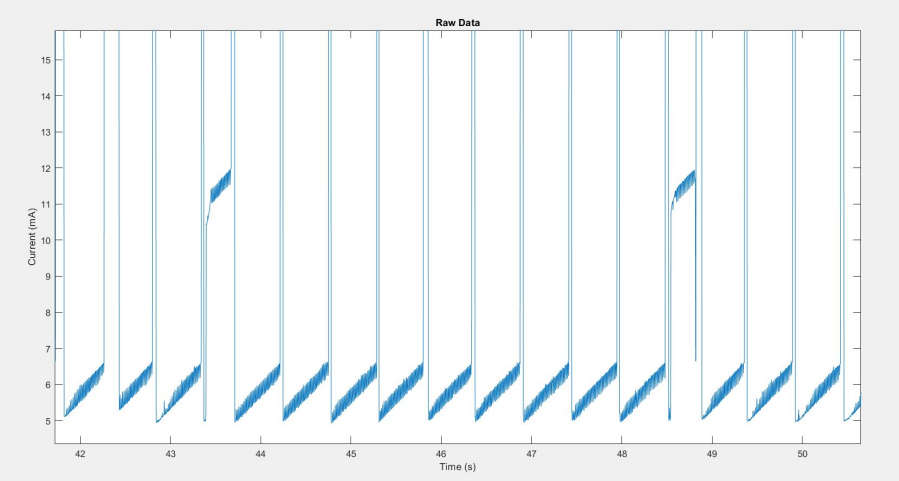

Figure 5.22. Power consumption analysis during Raw Data mode - Focus on the small peaks

Envelope

Power consumption analysis during the Raw Data working mode is reported in Figure 5.23. The monitoring is started with system off and at turn on the initialization is performed by the system. It regards the first peak in figure where the main contribute is given by the micro SD card initialization. After that the radio communication is set to RX mode with a power consumption around 16mA. When the working mode is received by the master the slave

turns off the radio system and the power consumption falls to around 10mA, from this point every 5s the RX mode is re enabled for the synchronization routine and disabled when expired (the periodic step of 6mA). When the start command is received by the master, the slave turns off all the leds (falling the power consumption to about 5mA). After the amount of time fixed by the master, at 40s the ADC starts sampling and the digital filters applied to the samples to extract each 20 samples a point of the envelope. From this point all the high peaks every 10s regard to the SD writings. The average power consumption on the eleven period in figure during the acquisition state is $5.58mA$ thus a saving of 14% of Envelope mode power consumption is achieved from the previous version.

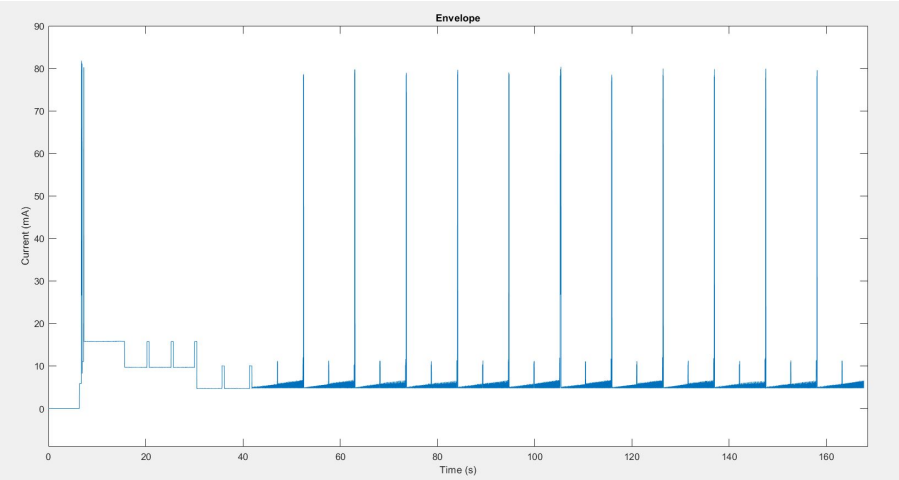

Figure 5.23. Power consumption analysis during Envelope mode

Figure 5.24 shows a focus on the activity. Three synchronization routines can be seen here and the base of two SD writings peaks at about 10s distance. The small peaks regards to the ADC sampling, the digital filters operations and the writings in the temporary FIFO structures. They are less dense the Raw Mode ones because one sample is stored each twenty of them.

ATC

Power consumption analysis during the Raw Data working mode is reported in Figure 5.25. The monitoring is started with system off and at turn on the initialization is performed by the system. It regards the first peak in figure where the main contribute is given by the micro SD card initialization. After that the radio communication is set to RX mode with a power consumption

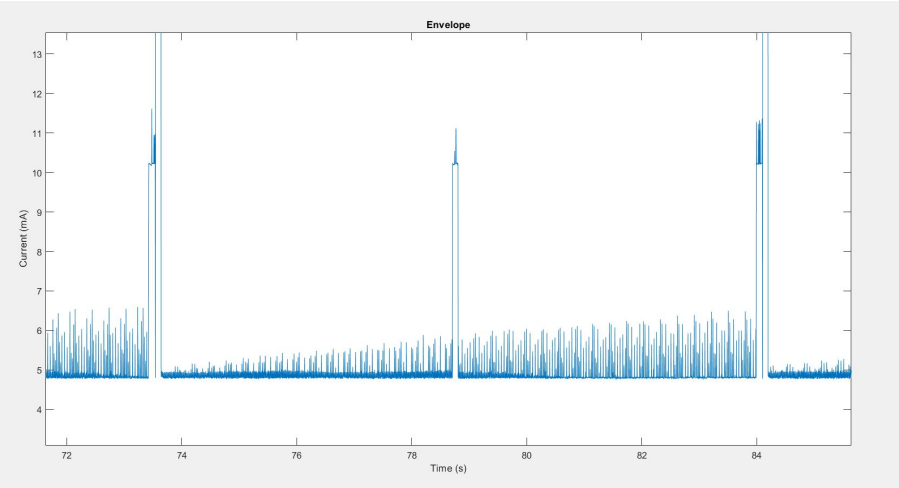

Figure 5.24. Power consumption analysis during Envelope mode - Focus on the small peaks

around 16mA. When the working mode is received by the master the slave turns off the radio system and the power consumption falls to around 10mA, from this point every 5s the RX mode is re enabled for the synchronization routine and disabled when expired (the periodic step of 6mA). When the start command is received by the master, the slave turns off all the leds (falling the power consumption to about 5mA). After the amount of time fixed by the master, the GPIO to count the Threshold Crossing events starts counting. From this point all the two high peaks regard to the SD writings performed much more further in time that the Raw Data and Envelope working mode. The average power consumption on the two period in figure during the acquisition state is $5.07mA$ thus a saving of 11% of ATC mode power consumption is achieved from the previous version.

Figure 5.26 shows a focus on the activity after 66s. After the synchronization routine current consumption, around 0.5mA peaks can been each 130ms. These ones are related to a muscle contraction where the ATC mode has sensed more one or more TC events. They infact regard to the writings in the temporary FIFO structures of values different from zero.

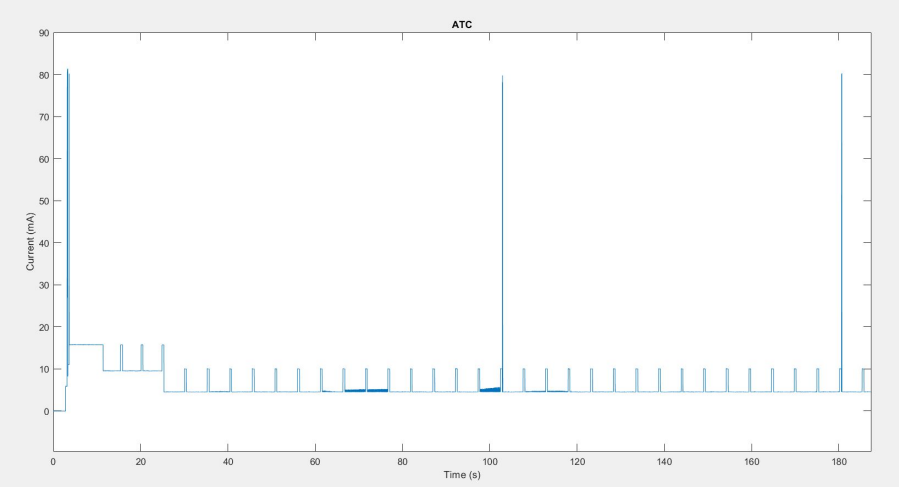

Figure 5.25. Power consumption analysis during ATC mode

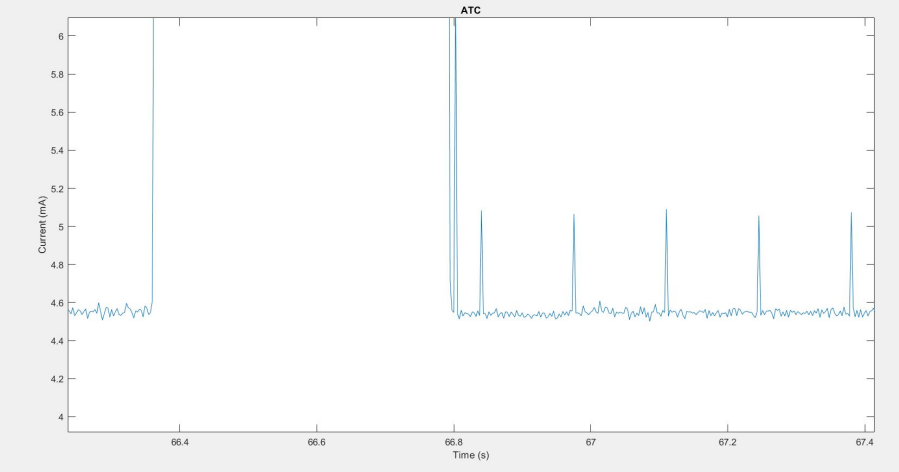

Figure 5.26. Power consumption analysis during ATC mode - Focus on the small peaks

Chapter 6

Conclusion

In this thesis project a low power wearable sEMG monitoring modular board has been designed and fabricated. The system is composed by two boards with the same size of $4.4cm \times 8.4cm$:

- **Main Board**: features the microcontroller unit, the power unit and a meander antenna. It has pin headers compatible with commercial mechanical characteristics that make it an open system which can be easily interfaced with additional analog and digital modules;
- **sEMG Analog Front End Module**: provides both sEMG and TC output signal with a programmable gain of 500/1000/1500/2500/3000 in the bandwidth 34Hz-397Hz.

The system is composed by one master that is in charge of ruling the synchronization of the (up to) eight slaves that are in charge to acquire the data and store it locally on a micro SD card. The master can set three different slaves working mode:

- **Raw Data**: the slaves sample the whole sEMG signal with a frequency of 1kHz and store it locally every 0.5s;
- **Envelope**: the slaves sample the whole sEMG signal with a frequency of 1kHz and a 2^{nd} order butterworth and a 4^{th} order chebyshev digital filters are applied on the samples extracting one point of the envelope every 20 samples and store them locally every 10s;
- **ATC**: the slaves count the number of Threshold Crossing events in fixed time windows of 130ms and store them locally every 65s.

The robustness of the signal acquired and the reliability of the previous prototype version are improved in this version. Particularly the issue related to the instrumentation amplifier stuck in the saturation state has been analyzed and fixed and then improved by selecting a new proper instrumentation amplifier, whereas the issue related to the periodic dropout voltage on the power supply and reflected on signal acquired has been solved by improving the power supply regulation chain as well as selecting a voltage reference to generate the INA reference voltage.

In the firmware the management of the peripherals has been refined. Particularly when the system is in Raw Data or in Envelope mode the GPIO Task and Event to count the TC events has been uninitialized, whereas when in ATC mode the ADC is not initialized and its data processing task is moved from the ADC to a timer.

The analysis on the power consumption showed that the analog acquisition module current load is $55.93\mu A$ during the muscle rest states, whereas during maximal voluntary contractions it reaches a maximum peak of $76.40\mu A$ with an average current load of $64.62\mu A$. The maximum peak power consumption is thus $200\mu W$ and an improvement of a factor 3 is achieved with respect to the previous version [24].
The analysis on the whole system assembled showed that the average current load during the steady state is 7.98mA in Raw Data mode, achieving a power consumption saving of 24% with respect to the previuos version system, 5.58mA in Envelope mode with 14% saving and 5.07mA in ATC mode with 11% saving.
With the 2.6Ah battery selected the new system can thus lasts more than 13 days in Raw Data mode, more than 19 days in Envelope mode and more than 21 days in ATC mode.

Future development of the system regards the addition of shields with sensors, for example an accelerometer is needed to start recording only when in movement. The envelope extraction can be designed in hardware to reduce the ADC sampling frequency and thus power consumption. For the slaves synchronization an Impulse Radio Ultra Wide Band (*IR-UWB*) radio module would reduce the power consumption and successively it could be exploit in combination with the ATC technique to send the data to the master, removing thus the micro SD card. The last step is consequently the miniaturization of the system.

Bibliography

[1] Cindy L Stanfield. *"Principles of Human Physiology"*. Pearson Education UK, 5 edition, 2013.

[2] Frontera W. R., and Ochala J., *"Skeletal muscle: a brief review of structure and function"*, Calcified Tissue International, Vol. 96, No. 3, pp 183-195, March 2015.

[3] Muay Thai Scholar contributors, *"The motor Unit"*. Retrieved: Feb, 18 2016. [Online]. Available: http://www.muaythaischolar.com/wp-content/uploads/2016/02/Motor-Unit-Anatomy.jpg

[4] J. V. Basmajain and C. J. De Luca, *"Muscles Alive: Their Functions Revelead by Electromyography"*, 1985.

[5] M. Raez, M. Hussain, and F. Mohd-Yasin, *"Techniques of EMG signal analysis: detection, processing, classification and applications"*, Biological Procedures Online, 2006. doi:10.1251/bpo115.

[6] C. J. De Luca, *"Surface Electromyography: Detection and Recording"*, 2002.

[7] R. Merletti and P. Parker, *"Electromyography, Physiology, Engineering and Non-invasive Applications"*, 28 January 2005.

[8] M. Crepaldi, M. Paleari, A. Bonanno, A. Sanginario, P. Arianno, D. Tran, and D. Demarchi, *"A quasi-digital radio system for muscle force transmission based on event-driven IR-UWB"*, Proc. IEEE Biomedical Circuits and System Conference, pp. 116–119, 2012.

[9] P. Motto Ros, M. Paleari, N. Celadon, A. Sanginario, A. Bonanno, and M. Crepaldi, *"A wireless address-event representation system for ATC-based multi-channel force wireless transmission"*, in Proc. 5th IEEE InternationalWorkshop Advanced in Sensors and Interfaces, pp. 51–56, 2013.

[10] S. Sapienza, M. Crepaldi, P. Motto Ros, A. Bonanno, and D. Demarchi, *"On integration and validation of a very low complexity ATC UWB system for muscle force transmission"*, IEEE transactions on biomedical circuits and system, vol. 2, April 2016.

[11] A. Shahshahani, P. Motto Ros, A. Bonanno, M. Crepaldi, M. Martina, D. Demarchi, and G. Masera, *"An all-digital spike-based ultra-low-power IR-UWB dynamic average threshold crossing scheme for muscle force wireless transmission"*, Design, Automation & Test in Europe Conference & Exhibition (DATE), 2015.

[12] Muhammad Z. J., *"Signal acquisition using surface EMG and circuit design considerations for robotic prosthesis, Computational Intelligence in Electromyography Analysis - A Perspective on Current Applications and Future Challenges"*, Dr. Ganesh R. Naik Editor, October 2012.

[13] D. A. Fernandez Guzman, S. Sapienza, B. Sereni, and P. Motto Ros, *"Very lowpower event-based surface EMG acquisition system with off-the-shelf components"*, in 2017 IEEE Biomedical Circuits and Systems Conference (BioCAS), pp. 1–4, IEEE, 2017

[14] De Luca C., Gilmore L. D., Kuznetsov M., Roy S. H., *Filtering the surface EMG signal: Movement artifact and baseline noise contamination"*, Journal of Biomechanics, Vol. 43, pp. 1573–1579, 2010.

[15] B. Sereni, *"Desing and development of a low-power wearable device for the acquisition of surface electromyography (semg) signals with average threshold crossing (atc)"*, Bianca Sereni, rel. Danilo Demarchi ; rel. aziendale Paolo Motto Ros, 2016.

[16] Kundu A. S., Mazumder O. and Bhaumik S., *"Design of wearable, low power, single supply surface EMG extractor unit for wireless monitoring"*, in Proc. International Conference on Nanotechnology and Biosensors IPCBEE, IACSIT Press, Singapore, Vol.25, 2010.

[17]] Poo T. S. and Sundaraj K.,*"Design and development of a low cost EMG signal acquisition system using surface EMG electrode"*, in Proc. Circuits and Systems (APCCAS), IEEE Asia Pacific Conference, pp. 24-27, 2010.

[18] Wang J., Tang L. and JBronlund J. E., *"Surface EMG Signal Amplification and Filtering"*, in Proc. International Journal of Computer Applications, Vol. 82, No1, November 2013.

[19] Shobaki M., Malik N. A., Khan S.,Nurashikin A., Haider S.,Larbani S., Arshad A. and Tasnim R., *"High Quality Acquisition of Surface Electromyography–Conditioning Circuit Design2*, in Proc. 5th International Conference on Mechatronics, Vol. 53, No. 1, 2013.

[20] Spinelli E. M., Pallas-Areny R. and Mayosky M. A., *"AC-Coupled Front-End for Biopotential Measurements"*, IEEEIEEE Transaction on Biomedical Engineering, Vol. 50, No. 3, March 2003.

[21] Analog Devices, *"Low Cost Programmable Gain Instrumentation Amplifier Circuit Using the ADG1611 Quad SPST Switch and AD620 Instrumentation Amplifier"*, Rev. 0. url: https://www.analog.com/en/design-center/reference-designs/circuits-from-the-lab/cn0146.html.

[22] Lee S., Kruse J., *"Biopotential electrode sensors in ECG/EEG/EMG systems"*, Analog Devices,January 2008.

[23] Ottaviani G., *"How to design the microSD circuitry"*, Acme Systems.

[24] D. A. Fernandez Guzman, S. Sapienza, B. Sereni, and P. Motto Ros, *"Very low power event-based surface EMG acquisition system with off-the-shelf components"*, in 2017 IEEE Biomedical Circuits and Systems Conference (BioCAS), pp. 1–4, IEEE, 2017.

[25] Texas Instrument, *"INA321 Micropower single-supply CMOS Instrumentation Amplifier"*, Rev. D. 2006. url: http://www.ti.com/product/INA321.

[26] Texas Instruments, *"INA333 Micro-Power (50μA), Zero-Drift, Rail-to-Rail Out Instrumentation Amplifier"*, Rev. D. 2015. url: http://www.ti.com/product/INA333.

[27] Texas Instruments, *"TPS61099x Synchronous Boost Converter with Ultra-Low Quiescent Current"*, Rev. May 2018. url: http://www.ti.com/product/TPS61099.

[28] Texas Instruments, *"TPS6303x High Efficiency Single Inductor Buck-Boost Converter With 1-A Switches"*, Rev. Oct. 2015. url: http://www.ti.com/product/TPS63031.

[29] Texas Instruments, *"TPS782 500-nA I_Q,150-mA, Ultra-Low Quiescent Current Low-Dropout Linear Regulator"*, Rev. J. 2015. url: http://www.ti.com/product/TPS782.

[30] Analog Devices, *"LT6656 - 1μA Precision Series Voltage Reference"*. url: https://www.analog.com/en/products/lt6656.html.

[31] Analog Devices, *"ADG711 - CMOS Low Voltage, 4 Ω Quad, SPST Switches"*, Rev. B url: https://www.analog.com/en/products/adg711.html.

[32] Texas Instruments, *"LPV821, 650nA, Precision, Nanopower, Zero-Drift Amplifier"*, Rev. D. 2017. url: http://www.ti.com/product/LPV821.

[33] Texas Instruments, *"TLV854x 500-nA, RRIO, Nanopower Operational Amplifiers for Cost-Optimized Systems"*, Rev. A. 2018. url: http://www.ti.com/product/TLV8542.

[34] Analog Devices, *"ADP191 - Logic Controlled, High-Side Power Switches"*, Rev. E. url: https://www.analog.com/en/products/adp191.html.

[35] On Semiconductor, *"EMI Filter for T-Flash MicroSD Interfaces"*, Rev. 3. A. 2013. url: https://www.onsemi.com/products/isolation-protection-devices/emi-filters/cm1624.

[36] Analog Devices, *"AD5621 - 2.7V to 5.5V, <100 μA, 8-/10-/12-Bit nanoDAC, SPI Interface in LFCSP and SC70"*, Rev. I. url: https://www.analog.com/en/products/AD5621.html.

[37] Texas Instruments, *"TLV3691 0.9-V to 6.5-V, Nanopower Comparator"*, Rev. N. 2015. url: http://www.ti.com/product/TLV3691.

[38] Nordic Semiconductor, *"nRF52840 Product Specification V1.1"*, Rev. 2019. url: https://www.nordicsemi.com/Products/Low-power-short-range-wireless/nRF52840.