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Design, Simulation and Prototyping of a 20kW Three-Phase Inverter for heavy-duty applications

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Abstract

This thesis concerns the design of a three-phase Voltage Source Inverter for future applications inside heavy-duty vehicles. In particular, all the preliminary aspects that are needed to be considered for a prototype fabrication will be discussed, including: selection of the components, development, design, simulation, circuit schematic and PCB implementation of an evaluation board; the purpose of this prototype is to verify that the hardware implemented is suitable for an application with a DC bus voltage of 700V and a maximum power of 20kW.

The first step of the project deals with the development of a model which is capable to simulate and evaluate the main parameters of the inverter behaviour in different working conditions, in order to obtain a method to compare power electronics components and modulation techniques from the point of view of achievable efficiency and performances. This model is developed using few hardware resources with the aim to run a fast and efficient simulation; furthermore, the validity of the data obtained by implementing this model in MATLAB/SIMULINK environment is checked by a comparison with the results given from some simulators available on different semiconductor manufacturer websites. Once the components have been chosen, the design of the different inverter parts and a first evaluation of the physical dimensions of the system has be done.

The main step in order to evaluate the real performances of the system is the schematic and PCB design; it is carried out taking into account the flexibility, the development time and the maintenance easiness, that are characteristics needed to build an evaluation board of the system.

This Thesis discusses the introductory studies carried out in the framework of a long-term task commissioned to Flag-MS company, which is an innovative small and medium-sized enterprise hosted by the Innovative Enterprise Incubator (I3P) of the Politecnico di Torino and is a member of MESAP, the Innovation Cluster for Smart Products and Manufacturing.

Acknowledgements

At the end of my studies there are so many people that I would like to thanks, I apologize if I forget someone.

The first due thanks go to my parents for the sacrifices and patience spent in these years, to my brother as continuous source of inspiration and security, and to all my family members which have always believed in me.

A special thanks to all the guys of the FLAG-MS for the friendly and cordial work environment in which they welcomed me, especially my tutor Luca Vola Gera who guides me in this project. Thanks also to Professor Francesco Musolino for the time and kindness spent to follow the thesis work.

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Chapter 1

Introduction

In the last decades the energy demand has considerably increased and fossil fuel sources, the main energy source, have become a risk for human health due to the adverse effects of CO_2 emissions in the environment, and, in 2009, it was detected that the 29% of these greenhouse gas emissions was produced by the transportation sector [62]. This pollution figure could be reduced with a progressive penetration of electric vehicles in the transportation sector; thus, both the industrial and automotive world started to invest resources in the electric energy source, leading to an ongoing improvement of the power electronics field because the appeal of an electric vehicle is intensifying globally, with more consumers attracted by a vehicle with an electric powertrain (Figure 1.1). Moreover, observing the research development and investments trend, it can be noticed that the request for new and improved power converters will grow further in the next years. The challenge will be to find the best trade-off: on one hand the market will ask for power converter systems with higher efficiency, higher reliability and functionality, on the other one it will ask for lower costs, weight, volume and development time [32].

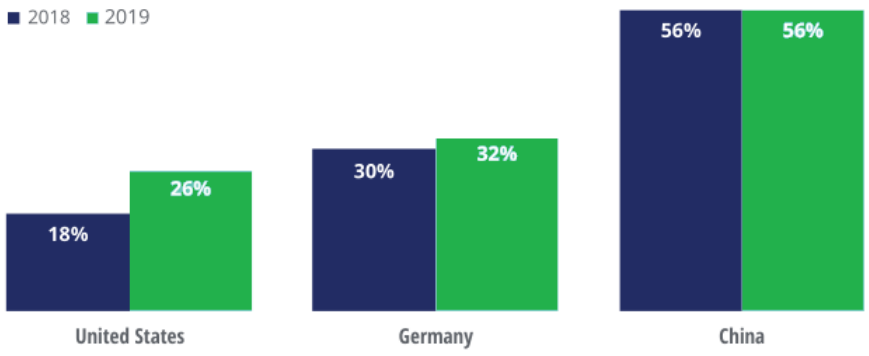


Figure 1.1. Deloitte Global Automotive Consumer Study: comparison of interested consumers in an electrified powertrain between 2018 and 2019. [49]

1.1 The heavy-duty sector

Riding the wave of this electrification trend, different OEMs (Original Equipment Manufacturers) are directing their efforts to realize modern and avant-garde Heavy-Duty Vehicles (HDVs), in order to replace the classic fuel powertrain with a modern electrified one. The word HDV means a vehicle designed for heavy work but with different uses and drive cycles: it can refer to a freight vehicle of more than 3.5 Tonnes (such as trucks) or passenger transport vehicles with more than eight seats (buses and coaches). Even if the HDV fleet is very heterogeneous, most of them have in common the engine typology: they are powered by diesel engines that emit high levels of particulates, nitrogen oxides, and other pollutants. This is the reason why both the European Union and the United States are redacting new HDV emission standards [50], and the only suitable alternative to diesel powertrains for this type of vehicles is an electric powertrain, due to their high torque demand at wheels and controllability requirements [34].

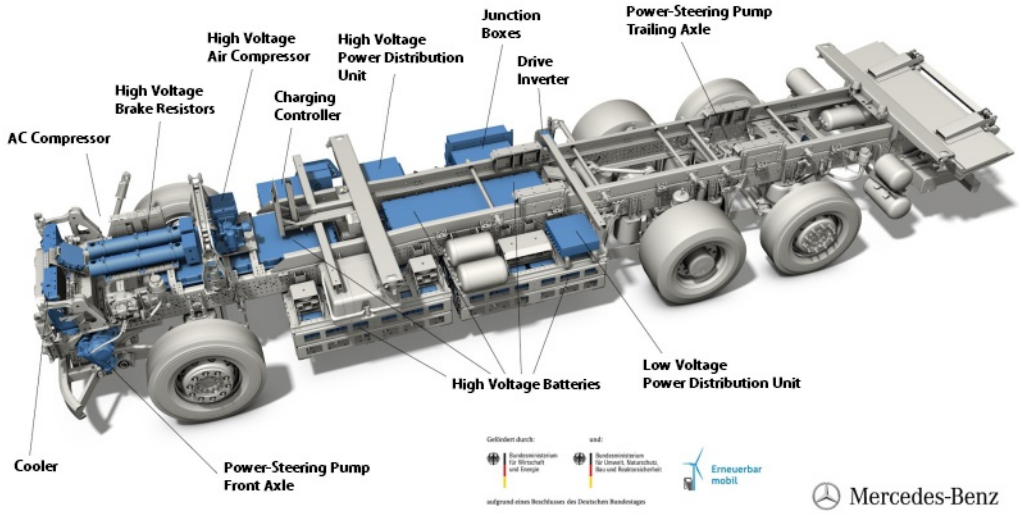


Figure 1.2. In-depth view of a Mercedes-Benz eActors heavy-duty electric truck.

From the situation described above it is clear that the heavy-duty sector is very sizzling: from the first to the third of July of 2019, the IQPC's Powertrain Electrification Conference for medium and heavy-duty vehicles has been held in Berlin. Companies are looking for more capable power units with fewer production costs and the biggest OEMs are trying to overcome as fast as possible the technological obstacles of this segment: high impact on grid power quality, high energy cells, highly efficient systems to increase the range and higher cooling power [53]. The battery voltage range for heavy-duty application is of 600V-700V, whereas the electric cars available in the market have batteries of around 300V. Another issue for

this sector is the technological growth rate because it does not allow for the reduction of power components level costs; the situation is the opposite for high voltage battery: cost reduction in kWh is more visible than power components such as inverter, motor and high voltage auxiliary components. Instead, with power rating lower than 2kW, assembly costs, cable and electrical connectors are the main contributors of costs [33]. The use of DC input voltages above 600V is not an arbitrary choice and it is becoming a standard also in electric cars, proof of this is the new and powerful Porsche Taycan with a DC-bus voltage of 800V. Using higher voltages, the amount of current required to achieve a given power level is reduced and this allows for thinner and lighter cables inside the vehicle, thinner and lighter cables on the fast recharging stations and the motor will sink less current producing less heat. Thus, thanks to the higher voltage level, a smaller and cooler high efficient system can be manufactured.

Figure 1.2 shows one of the few available full-electric heavy-duty vehicle: it is the power distribution configuration of a Mercedes-Benz eActors, and it has recently been adopted by the Dachser company for daily journeys of about 80km.

1.2 Overview of electrified powertrains

Electric vehicles can run on solely electric propulsion or they can have an internal combustion engine working alongside, hence they can be categorized as follows [54]:

- Battery Electric Vehicle (BEV);
- Hybrid Electric Vehicle (HEV);
- Plug-in Hybrid Electric Vehicle (PHEV);
- Fuel Cell Electric Vehicle (FCEV);

HEVs are implemented with two or more types of energy source, storage or converters with at least one of those used to provide electrical energy. However, the goal for the heavy-duty sector is the fabrication of BEV with only batteries to provide power to the drive train but capable to combine acceptable costs and long-range capability. The general powertrain scheme of a Battery Electric Vehicle is reported in Figure 1.3 where the main topic of this Thesis is visible: the inverter.

A power inverter is the most important component for controlling the electric motor, because the DC power coming from a battery pack must be converted into the most suitable AC voltages and currents. Focused about this aspect, the project presented in the next pages is developed with the purpose to obtain an efficient, small and cheap motor driver.

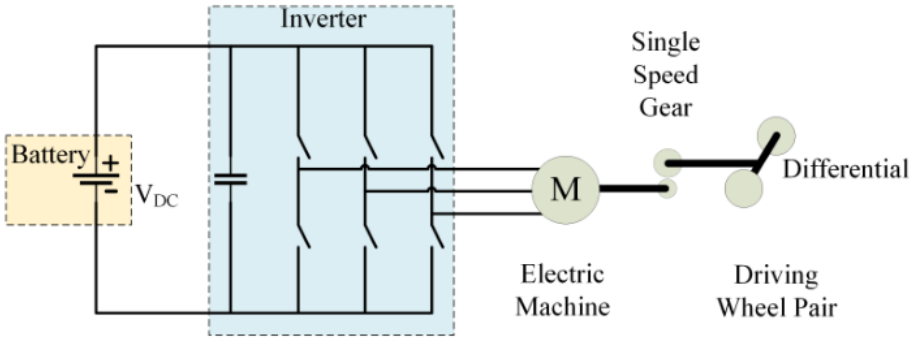


Figure 1.3. Battery Electric Vehicle configuration. [54]

1.3 Thesis organization

The primary aim of this work is to fabricate a prototype of a three-phase voltage source inverter for heavy-duty application fed by a DC bus of 700V and it will stand with a maximum power of 20kW; due to the lack of information at this very beginning stage of the task about the topology of the electric motor that will be implemented in the final application, the Thesis describes the design of a general-purpose AC electric drive. This choice makes possible to define a procedure by which most of the design issues of the inverter can be studied and tackled, increasing the technical competences in this specific sector while letting for future works the integration of this inverter with the electric motor. As for the automotive world, a stand-alone isolated power converter is needed because, unlike a grid-connected system, the generation of power is close to the demand centre. In Chapter 2 the basic background needed in order to develop the project are illustrated.

Considering the biggest challenges of the heavy-duty sector, the main trade-off taken into account during the design is the one between cost and efficiency but, at the same time, keeping the volume the smallest as possible. Thus, looking for a highly power density and highly efficient converter, the semiconductor state-of-the-art transistors, Gallium Nitride (GaN) MOSFET, should be implemented. They are the latest in technology but they have had slow adoption due to cost, yield and reliability concerns [5]. GaN transistors can reach higher switching frequencies compared with Silicon Carbide (SiC) or Silicon (Si) thanks to its higher electron mobility. Their negative aspect consist in their low thermal conductivity, that leads to a fewer power density potential. Furthermore, while the blocking voltages of GaN MOSFETs is limited to around 650V, SiC devices are well suited for applications from around 650V through 1.2kV (and higher) thanks also to their lower cost and robustness, given by the greater maturity of the technology. The best choice for the specific application of this Thesis is SiC technology because, on the contrary of

Silicon, it is a wide band gap semiconductor: higher breakdown voltage compared with Si of the same scale, lower on state resistance and higher thermal conductivity [36].

SiC semiconductors combined with a 700V DC-bus voltage respond to the different needs of the heavy-duty sector because high power density combined with high frequency are essential features for lower overall cost, weight and cooling requirements. Since there are different types of SiC MOSFETs available on the market, a preliminary analysis of their performances, costs and dimension is necessary. In order to allow a better and faster choice and in order to verify the actual improvement of SiC MOSFETs with respect Si MOSFETs or IGBTs, the starting point of this Thesis is the creation of a MATLAB/SIMULINK model: it simulates a typical three-phase inverter application and allows to evaluate the power dissipation of the switches in different operating conditions and with different modulation techniques. The behaviour of a three-phase inverter is simulated with a SIMULINK model while all the analytical calculations are performed with MATLAB functions; the customizable parameters of the simulations are different: power ratings, modulation techniques and modulation parameters (modulation index, frequency). The temperature contribution is not considered and all the temperature-depending parameters are reported with their mean values (between the maximum and the minimum temperature), in fact the thermal design is not addressed in this first step of the three-years project and only electric tests will be performed on the final evaluation Printed Circuit Board (PCB). This model can be used also if in the future the GaN technology will be available for higher power ratings and its implementation is described in the Chapter 3, furthermore it is validated comparing its results with the thermal simulator of an important semiconductor manufacturers.

Another important task performed by the model is the analytical computation of the ripple component of the DC-link current and the evaluation of the input voltage ripple. Inverters are switching converters, hence they are non-linear devices: the output spectrum of both voltages and currents is full of unwanted harmonics, and they are reflected to the DC-side of the inverter in the form of a polluted current. In order to keep the DC voltage clean and stable, complex harmonic filtering systems must be used. Chapter 4 deals with the design and selection of a DC-link capacitor to be connected in parallel with the DC source in order to create a low-impedance path towards ground for the polluted current. However, since the root mean square (rms) and peak value of the ripple DC-link current to be filtered are large suitable capacitors may be heavy, unreliable and expensive; for this reason, other solutions are discussed in Chapter 4.3, even though they will not be implemented in this work.

All the simulations performed together with the selection of the best switches and capacitor for the application is the pillar for the other steps of the design addressed in the Chapter 5; all the aspects concerning the gate driver design, the power supply design and heavy-duty certification criteria (insulation, health issues,

standards) are explored in this Chapter. All the integrated circuits chosen are AEC-Q100 qualified: it is a failure mechanism based stress test qualification for packaged integrated circuits. The purpose of this specification is to determine that a device is capable of passing the specified stress tests and thus can be expected to give a certain level of quality/reliability in the application [2]. Furthermore, also the passive components are adequately chosen to ensure the best reliability for the stressing condition of heavy-duty environments: they are AEC-Q200 qualified, the counterpart stress test qualification for passive components [3].

Finally, the schematic and layout design of an evaluation board has been made, in order to verify all the previous steps and to evaluate the gate drivers and the power supply performance. This board is manufacturer on a two-layer PCB with small sizes, a well suited choice when a cheap and fast delivery system is needed for in house testing purposes. The Thesis ends with the Chapter 7 in which the main contributions and findings of this work are summarized and an outlook on the future perspectives and applications is investigated.

Chapter 2

Inverter

In this Chapter, some basic concepts about switching power converters will be reviewed in order to better describe nd justify some criteria adopted in the design of the inverter for heavy-duty applications. Inverters, are circuits that convert power from a DC source to an AC load in the most efficient way in order to not lose energy, and they can be classified in function of the number of outputs, the type of inputs and the kind of modulation they employ to get energy conversion. Inverters are four quadrants converter with bipolar output voltage and bidirectional output current; this is necessary because the load is usually not resistive but also because bi-directionality can be a desired feature.
Taking into account the number of outputs phases, inverter can be classified into:

- single-phase inverters with one current and one voltage as output;
- three-phase inverters with three different outputs shifted by 120° each to the other.

Taking into account the input, there are:

- VSI (Voltage Source Inverter) with constant input voltage; the amplitude of output voltage does not depend on the load while the waveform of load current as well as its magnitude depends upon the nature of the load impedance;
- CSI (Current Source Inverter) with constant input current; the amplitude of output current is independent of load while the magnitude of output voltage and its waveform is dependent upon the nature of load impedance.

Taking into account the modulation, among several possible techniques [23], must be cited:

- the sinusoidal modulation with a sinusoidal control voltage used to control both the output magnitude and the output frequency;

- the square wave modulation used to control just the output frequency; In order to change the output magnitude it is needed to change the DC input voltage magnitude;

- the voltage cancellation method that it is an improvement of the square wave modulation in terms of spectral purity of the output signal which is suitable only for single-phase inverters.

A single-phase VSI inverter is suitable for low power applications, while a three-phase VSI inverter is recommended for medium and high power applications [48].

The inverter designed in this Thesis has to deal with high power application, so a three-phase VSI inverter has been considered in what follows. Taking into account a three-phase system with a balanced wye-connected load (Figure 2.1), some important relationships for the voltages and the currents of the inverter outputs are reported as follows:

$$P_{out} = \sqrt{3} V_{LL}^{rms} I_{LL}^{rms} \cos(\phi) \tag{2.1}$$

$$V_{LL}^{rms} = \sqrt{3} V_{LN}^{rms} \tag{2.2}$$

$$I_{LL}^{rms} = I_{LN}^{rms} \tag{2.3}$$

where V_{LL}^{rms} is the rms value of the line voltage (see, for example, v_{AB} in Figure 2.1), V_{LN}^{rms} is the rms value of the phase voltage (see, for example, v_{AN} in Figure 2.1), I_{LL}^{rms} is the rms value of the line current and I_{LN}^{rms} is the rms value of the phase current; P_{out} is the active power while $\cos(\phi)$, where (ϕ) is the cosine of the phase angle between current and voltage, is the Power Factor and it is the ratio between the real power absorbed by the load and the apparent power flowing in a circuit.

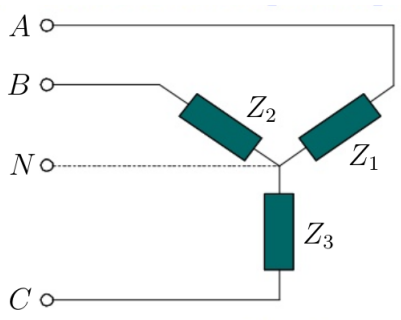


Figure 2.1. Wye-connected balanced load ($Z_1 = Z_2 = Z_3$). A, B and C are called "line" while N is called "neutral". [6]

2.1 Three-phase two-level Voltage Source Inverter

The topology adopted in the following project is a Three-phase two-level Voltage Source Inverter. It is made by three fundamental switching poles (Figure 2.2), one for each phase, called also legs and it is a two level converter because the output voltage can be positive or negative with respect to the mid potential of the DC bus [20].

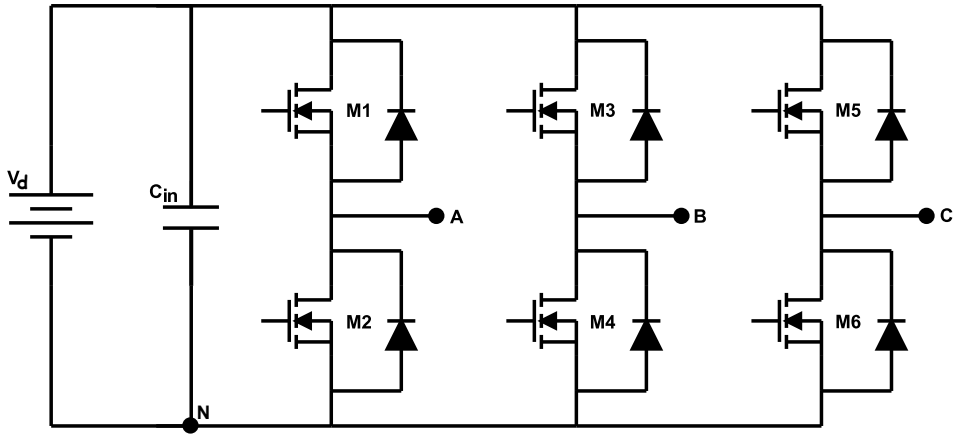


Figure 2.2. 3-phase Inverter.

In order to obtain a four quadrants converter, VSIs have switches capable to manage the bipolarity and the bi-directionality. Moreover, this inverter topology is used for mid to high power applications, so power MOSFETs and IGBTs can be used as switches [59]. Their electrical characteristics must be as close as possible to that of an ideal switch, that means high blocking voltage and high conduction voltage are required. Furthermore, they should be capable to dissipate as low as possible (very low on-resistance) with a high switching frequency.

A power MOSFET is intrinsically a bidirectional device thanks to the body diode while an IGBT is intrinsically unidirectional in current, but they are built with an additional diode inside the same package to allow for conducting current in the opposite direction [59]. Thus, both of them are capable to work in the four quadrant application. For what concerns their features: MOSFETs show lower switching time because they are unipolar devices (only one kind of carriers is involved in conduction), while some IGBTs show lower on-resistance. Since the IGBT is built from the basic structure of a vertical MOSFET, both of them need a control voltage to the input control terminal (the gate terminal) in order to turn-on the device. There are some advantages in using only n-channel MOSFETs and IGBTs due to their lower on-resistance, higher frequency applications and lower costs with respect to p-channel devices. The consequence is that the upper transistor of the

leg (called high-side transistor) is biased as a common drain/collector, while the bottom transistor of the leg (called the low-side transistor) is biased as a common source/emitter. The difficulty is the absence of a common gate and a common source/emitter point and thus there is no way to have a single drive signal for controlling both of the leg transistors [20]. The control signal of each transistor must be separated and isolated from each other beacause the source/emitters are at different potentials. Since all the low-side source/emitters of each leg are connected to the negative side of the DC bus, they are at the same potential and the control signals does not need to be isolated.

2.2 Modulation techniques

In order to have an output voltage with the desired waveform, amplitude and frequency, the control signals for transistor switching can be generated with the carrier-based PWM (Pulse Width Modulation) technique: it defines the on and off states of each switch by comparing one (or more) control voltage v_{CTRL} (modulating signal) with a triangular carrier signal v_{tr} (Figure 2.3) [48]. Since the ratio between the amplitude of the control signal and the amplitude of the carrier signal determines the pulse width, a parameter called modulation index can be introduced:

$$m_a = \frac{\hat{v}_{CTRL}}{\hat{v}_{tr}} \tag{2.4}$$

where the sign ôver the voltages in (2.4) means the peak value.

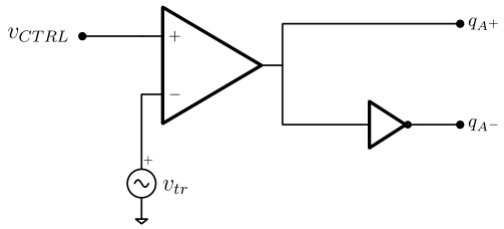


Figure 2.3. PWM modulator. [42]

The modulation index is an important parameter because the amplitude of the output first harmonic of the output voltage of the inverter is determined by the pulse width, as it will be described in what follows. Instead, the ratio between the switching frequency and the control signal frequency takes the name of frequency-modulation index:

$$m_f = \frac{f_{sw}}{f_{CTRL}} \tag{2.5}$$

The switching frequency f_{sw} acts as a sampling signal while the control signal f_{CTRL} acts as the sampled signal; the PWM modulator behaves like a two-tone system, hence the Nyquist–Shannon sampling theorem must be satisfied in order to obtain the right behaviour.

The modulator output is a pulsed waveform obtained from a smooth input signal: this is a non-linear operation and the output spectrum of a non-linear two-tone system presents both harmonics and intermodulation products (IIP) that must be filtered out [43]. It is useful to introduce a quantity in order to taking into account the quality of the AC output voltage or current; this parameter is the Total Harmonic Distortion (THD) [22] and, neglecting the output DC component, it is generally defined as follows:

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} \hat{v}_{o_h}^2}}{\hat{v}_{o_1}} \tag{2.6}$$

where $\hat{v}_{o_1}$ is the amplitude of the fundamental output component and $\hat{v}_{o_h}$ is the amplitude of the harmonic of order h.

There are several implementation methods for the PWM technique and each of them gives different results with respect of the others, not only in terms of the output amplitude and waveform, but also in terms of spectral purity and power dissipation.

2.2.1 Sinusoidal PWM (SPWM)

Since most of the applications need sinusoidal output voltages, the output of a three phase SPWM inverter should be a set of three voltage sine waves with a phase shift of 120° among each other. Thus, the legs are driven by sinusoidal control signals (Figure 2.4.a) with the same frequency and phase difference of the target outputs but with a considerably smaller amplitude. These three modulating signals are compared with a unique carrier signal v_{tr}, whose frequency is equal to the switching frequency.

The phase voltages v_{AN} and v_{BN} (Figure 2.4.b, 2.4.c) have basically the same behaviour of the modulation signal of switches M1 and M3, respectively, with a different amplitude. These phase voltages, as well as v_{CN} (not showed in Figure 2.4), are composed by a DC component and by an AC component v_{LN}. Taking into account the relation (2.4), the first harmonic amplitude of each phase voltage can be written as:

$$\hat{v}_{LN} = \frac{V_d}{2} m_a \tag{2.7}$$

while the amplitude of the line voltages v_{LL} (Figure 2.4.d) is:

$$\hat{v}_{LL} = \frac{\sqrt{3}}{2} m_a V_d \tag{2.8}$$

Equations (2.7) and (2.8) shows that the amplitude of the AC output voltages is a function of the modulation index m_a, but this is always verified only in the linear operation region (i.e. for $m_a \leq 1$, Figure 2.6). This means that the maximum amplitude of the line voltage fundamental harmonic is:

$$\hat{v}_{LL,max} = \frac{\sqrt{3}}{2} V_d \tag{2.9}$$

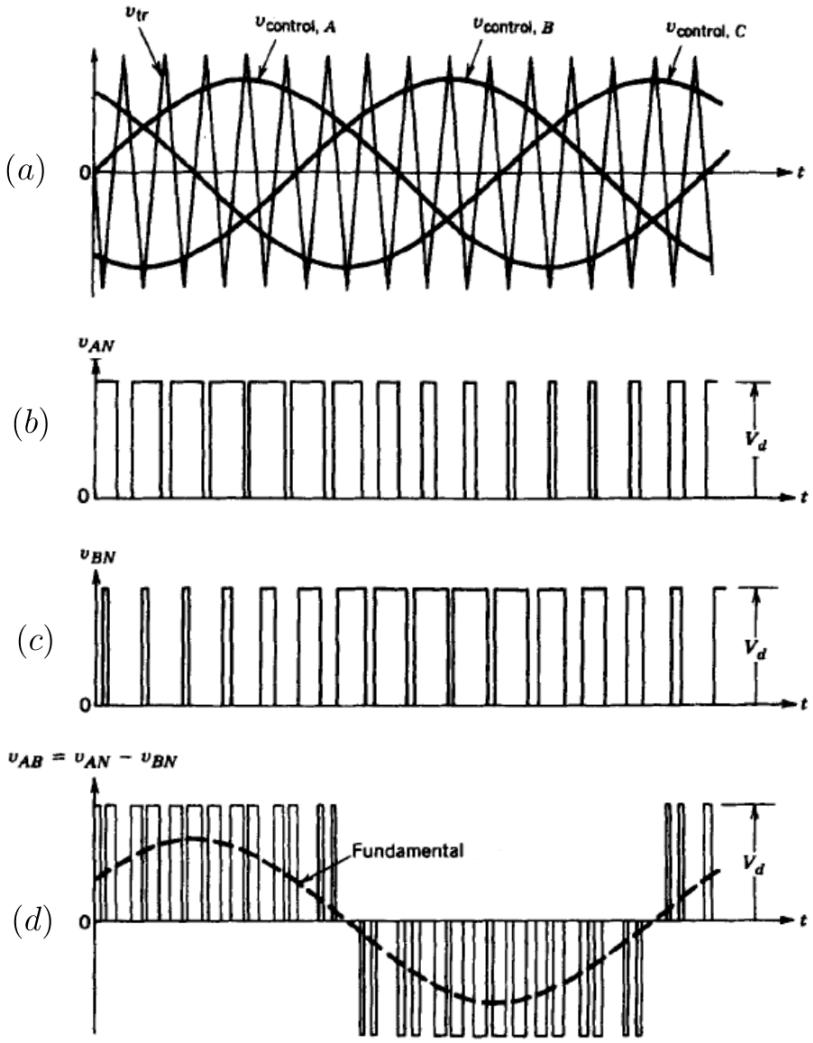


Figure 2.4. Waveforms in a SPWM 3-phase 2-level VSI with delta-load connection: (a) carrier and modulating signals; (b) phase voltage between phase A and neutral; (c) phase voltage between phase B and neutral; (d) AC line voltage between phase A and phase B. [42]

Furthermore, another condition must be satisfied in order to obtain the features of a three-phase SPWM inverter with a single carrier signal: the frequency-modulation index should be an odd multiple of 3 [48]. As Figure 2.5 shows, with this choice only odd intermodulation products (sidebands) appear in the output spectrum.

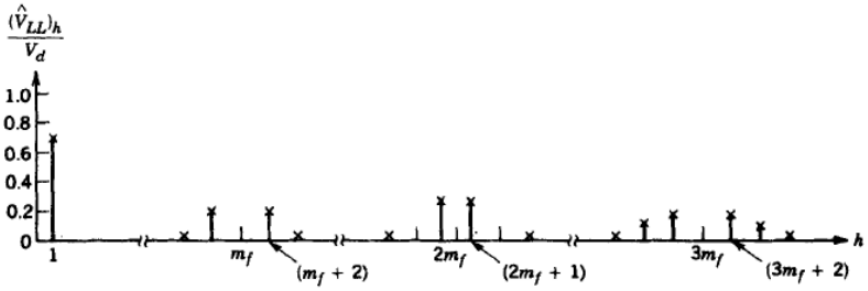


Figure 2.5. Harmonics h of the fundamental in a three-phase SPWM inverter with $m_a = 0.8$ and $m_f = 15$. [42]

2.2.2 Square wave modulation

Supposing to further increase the control signal amplitude $\hat{v}_{CTRL}$ making it larger than the carrier signal amplitude $\hat{v}_{tr}$, the modulation index m_a will be greater than one and the inverter will be driven in the so-called overmodulation region (Figure 2.6).

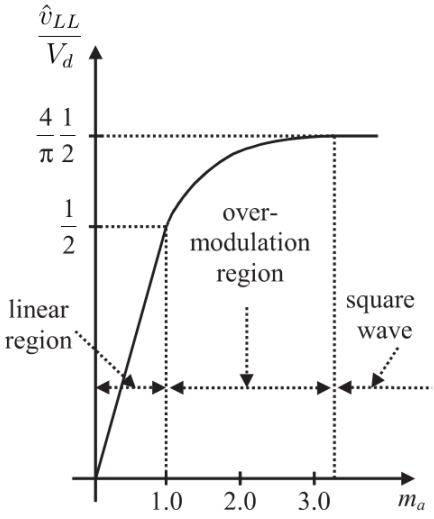


Figure 2.6. Fundamental AC output component of the line voltage in a VSI SPWM inverter. [48]

When the instantaneous value of $\hat{v}_{CTRL}$ is higher than the instantaneous value of $\hat{v}_{tr}$, the output voltage will increase leading to an higher amplitude of the fundamental AC output voltage; on the other hand, low-order harmonics are generated [48]. The linear relation (2.8) is no longer valid because of the saturation effect due to overmodulation.

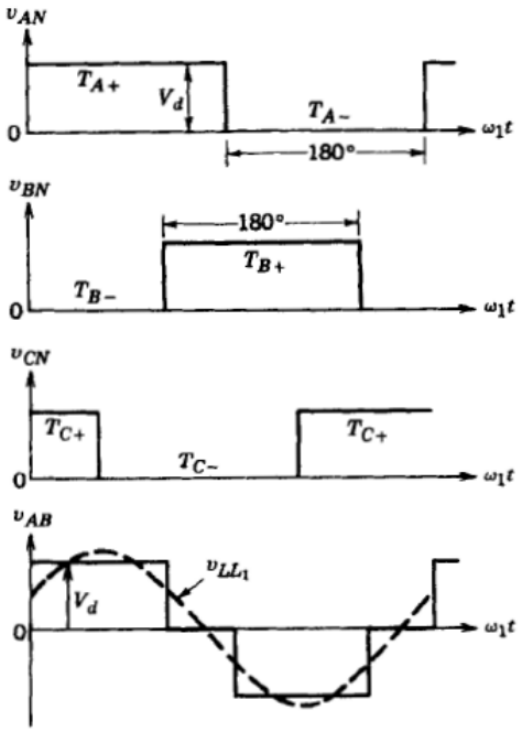


Figure 2.7. Square wave inverter output waveforms: the three phase voltages v_{AN}, v_{BN}, v_{CN} and one of the line voltages v_{AB}. [42]

By further increasing the modulation index, when the output voltage becomes a totally AC square voltage, the square-wave modulating technique (Figure 2.6) is reached. Each transistor conducts for one-half cycle of the ac output period, so during each of the six intervals, three transistors are in the ON-state while the remaining three are in the OFF-state (Figure 2.7). In this region, the fundamental AC line voltage of the output has the following amplitude:

$$\hat{v}_{LL} = \sqrt{3}\frac{4}{\pi}\frac{V_d}{2} \tag{2.10}$$

The relation (2.10) shows that the only way to change the fundamental amplitude is to control the DC input voltage V_d.

The square wave modulating technique allows exploiting simpler control circuit and the switching frequency is significantly lower than in PWM inverters with the

additional beneficial of lower switching losses. The drawback is in the purity of the output spectrum: square wave consists of a superposition of odd harmonics with a magnitude inversely proportional to their order which distort the output voltage and in many applications such distortions are not tolerable, mostly when the use of filter circuits to filter out satisfactorily the harmonics is not suitable.

In this project, the inverter drives an AC motor load which are inductive in nature with the intrinsic property to low-pass filtering the harmonic currents. Despite this inherent quality, the load current can still contain some harmonics, and they cause extra iron and copper losses in the motor but also unwanted torque pulsations. The motor speed hardly changes in response to these torque pulsations and, in some cases, they produce unwanted resonance in the mechanical system of the drive [21]. For these reasons, in the project described in this paper the square wave modulation will not be taken into account.

2.2.3 Third harmonic injection

From the previous analysis, it can be noticed that a SPWM inverter has a good purity in terms of output spectrum, a linear relation between modulation index m_a and fundamental output voltage amplitude $\hat{v}_{LL}$ but the maximum value of $\hat{v}_{LL}$ output voltage is limited. The opposite situation happens considering the square wave inverter, with an higher amplitude of the fundamental $\hat{v}_{LL}$ but with a distorted output voltage due to the presence of many low-order harmonics. The goal is to achieve a higher value of the fundamental without cross the linear region, hence with a maximum value of $m_a = 1$.

Let's consider to use a control signal that is the sum of two tones f_1 and $3f_1$, as shown in Figure 2.8:

$$v_{CTRL} = V_{C1} \sin(\omega_1 t) + V_{C3} \sin(3\omega_1 t) \tag{2.11}$$

In this way, it is possible to obtain an higher fundamental line voltage at the output but at the same time keeping the control voltage amplitude lower the triangular waveform amplitude, which means to work in linear region with $m_a \leq 1$. Furthermore, when the line voltage is considered, the third harmonic component disappear due to the phase shift of the three-phase inverter.

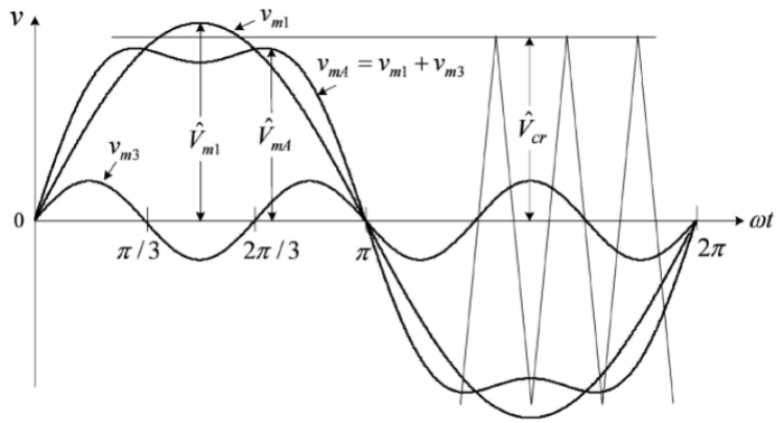


Figure 2.8. Control signal in a third harmonic injection inverter. [42]

It can be shown that, by having $k = V_{o3}/V_{o1} = 1/6$, the maximum amplitude of the fundamental output line voltage is:

$$\hat{v}_{LL,max} = \sqrt{3}\hat{v}_{LN,max} = V_d \tag{2.12}$$

2.2.4 Space-Vector modulation (SV PWM)

With the spread of fast Digital Signal Processors (DSPs), microcontrollers and microprocessors, all the control techniques can be implemented using digital systems and the developing of digital modulation strategies has lead to the Space-Vector modulation, a technique that allows to increase the amplitude of the output voltage fundamental until the value obtained with the third harmonic injection technique and, moreover, to push the harmonics at higher frequency.

Space-Vector PWM has become a popular pulse width modulation strategies for three-phase VSI for AC motor driving because of its different features: high torque to current ratio, large power to weight ratio, higher efficiency, and robustness [37].

The SV PWM is a digital technique with the objective to generate PWM load line voltages that are, on average, equal to given load line voltages [48]. This is done explicitly varying the position of the inactive states of operation of a converter within each half carrier period, in fact it is one of the modulation strategies based on Zero Space Vector Placement and it is based on the Park's transformations [23].

Clarke transform

When a high-side transistor is switched on, the corresponding low-side is switched off because it is not possible to short the input voltage supply. Hence, there are 2^3 possible switching states combinations for the three inverter legs, referred to

the conduction state of three high-sides M1, M3, M5: (000), (100), (110), (010), (011), (001), (101), and (111); the lower phase leg switches (M2, M4, M6) are represented as logical NOT of the upper phase leg switches. Each of these produces a specific combination of the phase and line output voltage: the first and the last one produce a null line voltage, while the other six states produce a voltage applicable to the motor. The Clarke transform is a mathematical representation of these space vectors and it transform the voltage equations in the natural three-phase coordinate system *abc* into the stationary $\alpha\beta$ reference system (Figure 2.9).

Since in a balanced 3-phase system the scalar sum of the three variables u_a, u_b, u_c is zero at any instant, the complex vector that defines *abc* quantities in the $\alpha\beta$ system can be introduced

$$\vec{u}\,(t) = C\left[u_a\,(t) + u_b\,(t)\,e^{j\gamma} + u_c\,(t)\,e^{j2\gamma}\right] \tag{2.13}$$

and it is the representation of the three line voltages in the 2D system $\alpha\beta$:

$$\vec{v}_{\alpha\beta} = \vec{v}_\alpha + j\vec{v}_\beta = C\left[v_{AB} + v_{BC}e^{j\gamma} + v_{CA}e^{j2\gamma}\right] \tag{2.14}$$

where $\gamma = 120°$ and C is a normalization factor used to maintain the amplitude equal across the transform because without it the amplitude of the $\alpha\beta$ variables is higher than the *abc* variables. Placing the factor $C = 2/3$ in order to obtain an amplitude invariant space vector, the following system is obtained:

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1 & 1 & 1 \end{bmatrix}\begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} \tag{2.15}$$

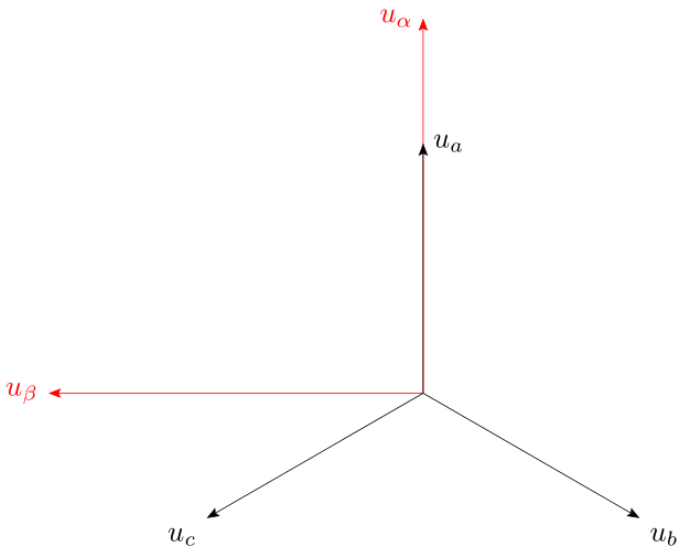


Figure 2.9. Relationship between *abc* reference system and stationary $\alpha\beta$ system. [42]

Table 2.1 shows the valid switch states for a three-phase VSI and the corresponding space-vectors, six active ones (not nulls) and two null ones, obtained from equation (2.15). Assuming a wye-connection at the load, the combination of phase voltages are reported from the third through the fifth column and in the sixth, seventh and eight column the line voltages are showed. The eight space-vector in the last column of Table 2.1 are represented in the complex plane $\alpha\beta$ of Figure 2.10 normalized with respect to V_d. It can be noticed that the six active vectors are separated by 60° and they have a magnitude of

$$||\vec{v}_x|| = \frac{2}{\sqrt{3}} \tag{2.16}$$

Each pair of them forms a sector, while the two null vectors lie in the origin of the system, hence six equal sectors are represented. Two important features can be extrapolated from previous analysis:

1. two adjacent active vectors are just one bit different;
2. the active vectors differ from one of the two null vectors of one only bit.

It is easy to deduce how such a control scheme can be easily implemented with a DSP, and this is one of the reason why in this project the Space-Vector PWM technique is the adopted control method.

State	#	v_{AN}	v_{BN}	v_{CN}	v_{AB}	v_{BC}	v_{CA}	Space-Vector
100	1	$^2/_3V_d$	$-^1/_3V_d$	$-^1/_3V_d$	V_d	0	$-V_d$	$\vec{v}_1 = \left(1 + j\frac{\sqrt{3}}{3}\right) V_d$
110	2	$^1/_3V_d$	$^1/_3V_d$	$-^2/_3V_d$	0	V_d	$-V_d$	$\vec{v}_2 = j\frac{2}{\sqrt{3}}V_d$
010	3	$-^1/_3V_d$	$^2/_3V_d$	$-^1/_3V_d$	$-V_d$	V_d	0	$\vec{v}_3 = \left(-1 + j\frac{\sqrt{3}}{3}\right) V_d$
011	4	$-^2/_3V_d$	$^1/_3V_d$	$^1/_3V_d$	$-V_d$	0	V_d	$\vec{v}_4 = \left(-1 - j\frac{\sqrt{3}}{3}\right) V_d$
001	5	$-^1/_3V_d$	$-^1/_3V_d$	$^2/_3V_d$	0	$-V_d$	V_d	$\vec{v}_5 = -j\frac{2}{\sqrt{3}}V_d$
101	6	$^1/_3V_d$	$-^2/_3V_d$	$^1/_3V_d$	V_d	$-V_d$	0	$\vec{v}_6 = \left(1 - j\frac{\sqrt{3}}{3}\right) V_d$
111	7	0	0	0	0	0	0	$\vec{v}_7 = 0$
000	8	0	0	0	0	0	0	$\vec{v}_8 = 0$

Table 2.1. The eight switch states in a three-phase VSI with the corresponding space vector of each line voltage combination.

Space-Vector Modulated Inverter

The goal is to combine in a proper way the six active vectors and the two null (or static) vectors to build the desired sinusoidal output line voltages. When these three sinusoids are manipulated by the Clarke transform, they correspond to a rotating vector in the $\alpha\beta$ plane with constant magnitude over each cycle. Moreover, every

time instant it is the projection of the line voltages, thus it becomes the base of the control signal and it is called modulating vector $\vec{v}_c$ (Figure 2.10).

The modulating vector is generated by switching between two nearest active vectors and zero vector [27]; supposing to construct it from space vectors $\vec{v}_1$ and $\vec{v}_2$ (Figure 2.11), the modulating vector is defined as:

$$\vec{v}_c = r_1\vec{v}_1 + r_2\vec{v}_2 \tag{2.17}$$

where r_1 and r_2 represent the normalized time interval, with respect to T_{SW}, during which $\vec{v}_1$ and $\vec{v}_2$ are applied and they can be evaluated by geometric analysis:

$$r_1 = \frac{2}{\sqrt{3}}\frac{||\vec{v}_c||}{||\vec{v}_1||}\sin\left(\frac{\pi}{3} - \theta\right) = \frac{1}{V_d}||\vec{v}_c||\sin\left(\frac{\pi}{3} - \theta\right) \tag{2.18}$$

$$r_2 = \frac{2}{\sqrt{3}}\frac{||\vec{v}_c||}{||\vec{v}_1||}\sin(\theta) = \frac{1}{V_d}||\vec{v}_c||\sin(\theta) \tag{2.19}$$

In order to keep the linear operation the condition

$$r_1 + r_2 \leq 1 \tag{2.20}$$

must be imposed, because the total time during which space vectors are applied has to be lower than the modulation switching period T_{SW}.

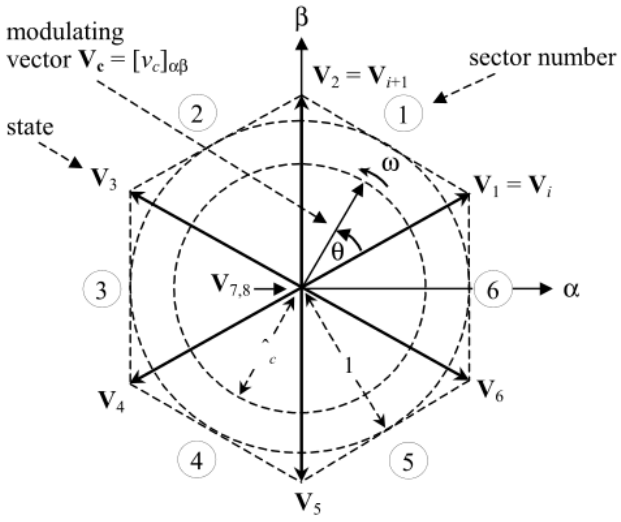


Figure 2.10. Space vector representation in the $\alpha\beta$ complex plane. [48]

Taking into account Figure 2.10, in order to keep linear operation the circle formed by the modulating vector must not exceed the hexagon borders. Furthermore, it can be noticed that the maximum of $||\vec{v}_c||$ corresponds to its radius.

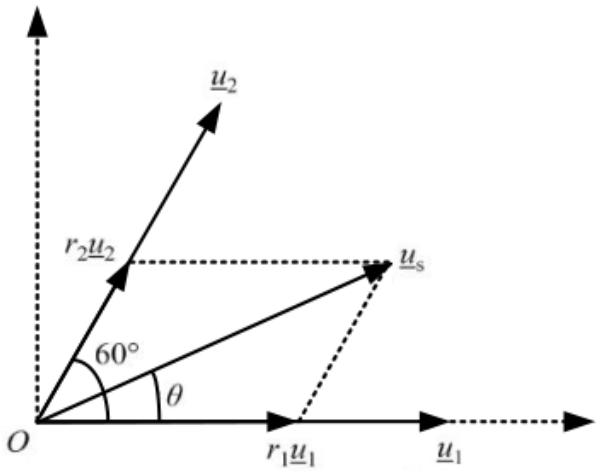


Figure 2.11. Modulating vector construction. [27]

The radius of the circle formed by the modulating vector can be geometrically evaluated

$$\frac{1}{V_d}\,||\vec{v}_c||\sin\left(\frac{\pi}{3}-\theta\right)+\frac{1}{V_d}\,||\vec{v}_c||\sin(\theta)\Big|_{\theta=\theta_t}\leq 1 \tag{2.21}$$

and considering that the limit case $r_1 = r_2 = 0.5$ occurs at $\theta_t = \pi/6$ where

$$\Longrightarrow \quad \frac{1}{V_d}\,||\vec{v}_c||_{max}\,\frac{1}{2}+\frac{1}{V_d}\,||\vec{v}_c||\,max\frac{1}{2}\leq 1 \tag{2.22}$$

one important result is found:

$$||\vec{v}_c|| = \hat{v}_{LL,max} = V_d \tag{2.23}$$

With the Space-Vector PWM technique, the maximum fundamental amplitude of the output line voltage is $^2/\sqrt{3} \simeq 1.15$ higher than the one of the Sinusoidal PWM reported in (2.9) and it has the same amplitude achievable with the third harmonic injection technique obtained in (2.12). Taking into account the linear relation between the modulation index m_a and the fundamental amplitude $\hat{v}_{LL}$, the following relation is obtained:

$$\hat{v}_{LL} = m_a V_d \quad , \quad 0 \leq m_a \leq 1 \tag{2.24}$$

The limit case $r_1 = r_2 = 0.5$ that leads to these results is not always verified when the modulating vector is constructed by averaging the space vectors [23], because the switching period T_{SW} must remain constant.

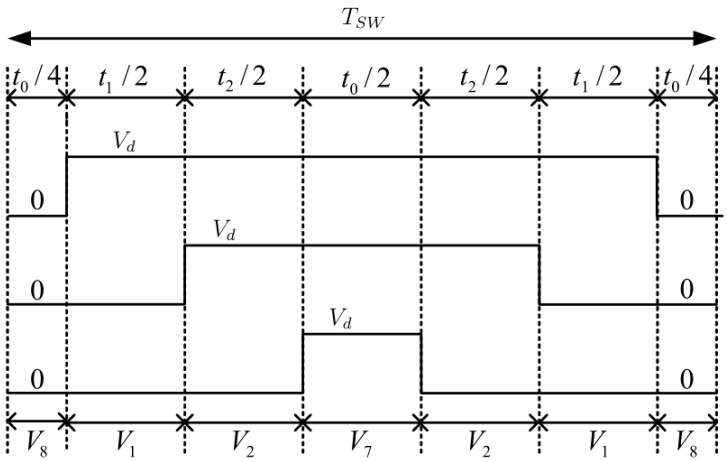


Figure 2.12. SV PWM symmetric switching pattern for Sector 1. [27]

This issue is easily bypassed by properly combining the null vectors with the active vectors. In fact, it is a Zero Space Vector Placement technique and it allows to have the degree of freedom to choose the location and duration of the null vectors within one period T_{SW}. The positioning can be done according to the specific application and, in this project, the pattern of the switching frequency is obtained by centring the active vectors and equally spacing the inactive vectors (Figure 2.12), in such a way that each leg change its sate only once in one switching period [27]. With this symmetric switching sequence, six commutations happen over one switching period leading to another features of this modulation technique: the less commutation are done, the less is the harmonic content at the output; in particular, the symmetric SV PWM has the lowest THD achievable with this technique [24].

Chapter 3

Evaluation of power losses

This chapter focuses on a step-by-step development of MATLAB/SIMULINK model of the inverter controlled by two configurable technique: the Sinusoidal PWM and the Space-Vector PWM. The reason why the square wave modulation technique and the third harmonic injection technique are not implemented in the model is related to their feauters explained in Chapter 2 and some of them are refreshed here:

- the output spectrum of the SPWM and SV PWM techniques, due to their low harmonic content, is more suitable in motor drive application because harmonics leads to resonance in the mechanical system of the drive;
- the third harmonic injection technique requires two oscillators and so it is more expensive;
- the SV PWM method is a intrinsic digital technique and so it is fast and easy implementable in a microcontroller or DSPs.

The main goal of the model is to evaluate the conduction and the switching losses of the three-phase inverter and to derive the current and voltage waveforms necessary fo the electric design.

The analysis carried out in this Thesis concerns a general purpose three-phase VSI because the load requirement will be defined only in further and later developing. Hence, the given specifications reported in Table 3.1 does not contain indications about the motor that the inverter has to drive. From the specifications reported in Table 3.1, a model capable to run an electric simulation of the inverter has been derived. Both IGBTs and MOSFETs behaviour are taken into account because they are the only switches topology available for this power rating.

In particular, four SIMULINK models have been developed in order to choose the right topology and modulation for the given application: two models of the three-phase VSI with IGBT switches, one with Sinusoidal PWM and one with Space-Vector, and two models of the three-phase VSI with power MOSFET switches,

one with Sinusoidal PWM and one with Space-Vector. These SIMULINK models, discussed in what follows and fully reported in Appendix B, and the MATLAB codes necessary for the simulation, also listed in Appendix A, are analysed in the next section. Furthermore, in the computation of the power losses only one transistor of one leg is evaluated because with a balanced load all the legs carry the same shape of the currents during a period.

Max. DC bus voltage V_d	700V
Max. Output Power P_out	20kW
Max. DC current I_d	29A
Max. Switching Frequency	20kHz
Max. Operating Temperature	125°
Typ. Output Frequency f_{out}	50Hz
Min. Power Factor $\cos(\phi)$	0.5
Max Phase Current	60A

Table 3.1. Specifications for the Inverter.

3.1 MATLAB/SIMULINK model

3.1.1 Sinusoidal PWM

The block-diagram of a three-phase two-level Voltage Source Inverter with IGBT switches controlled by a Sinusoidal PWM is shown in Figure B.1 and B.2. The six IGBT switches are inserted in the subsystem $INVERTER$ (Figure B.3) and the modulating technique used to drive them is generated by the subsystem $S\ PWM$ (Figure B.5). As explained in Chapter 2, it consists of three sine waves shifted by 120° that are compared with the triangular carrier signal. The presence of delay blocks can be noticed: they set the dead time of the PWM and it is mandatory to avoid to short-circuiting the leg [60]. Since the load to be driven is not assigned in the project specifications, the SIMULINK block $Three-Phase\ Dynamic\ Load$ is used in order to implements a three-phase, three-wire balanced load where active and reactive power absorbed by the load vary as function of the input PQ (Figure 3.1). This block allows to limit the maximum phase current according to Table 3.1 by controlling the input PQ with the $Current\ control$ function listed in Appendix B.1.

The simulation is initialized with the Matlab script *inverter_parameter* attached in Appendix A.1.1: with this script it is possible to set all the parameter of Table 3.1 and all the modulation parameter illustrated in Chapter 2. The main waveforms obtained from some simulations are reported in the next figures. The value of the simulation parameters can be extrapolated from the script *inverter_parameter*.

The gate control signal generated with the Sinusoidal PWM technique are shown in Figure 3.2: they leads to a pulsed current with a sinusoidal envelope in each IGBT and the one associated with switch $M5$ is reported in Figure 3.3. When the gate signal is high the transistor is turned on and it is turned off when the gate pulse goes low.

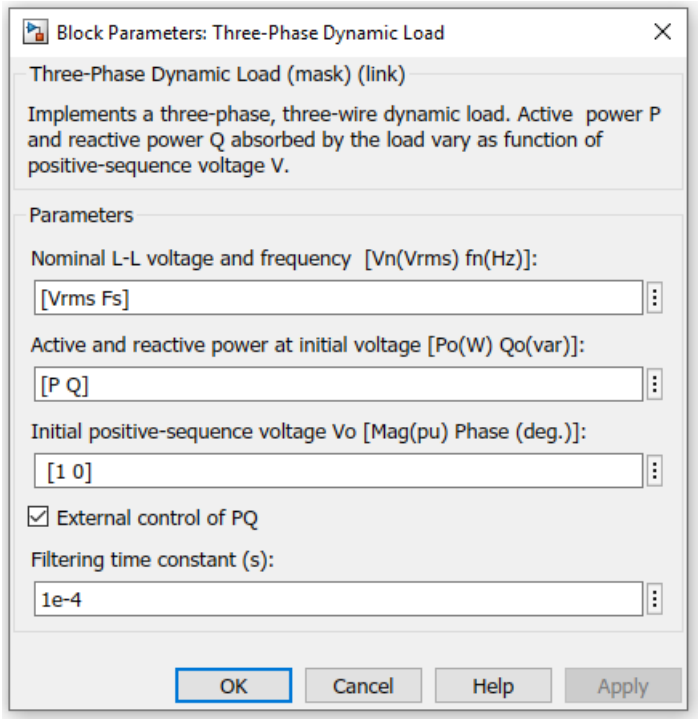


Figure 3.1. Three-Phase Dynamic Load simulation parameters.

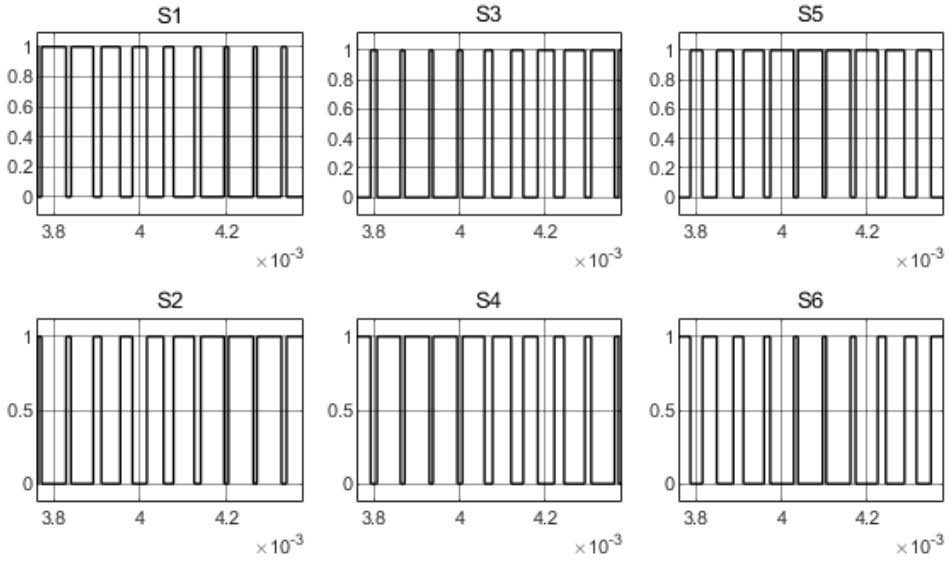


Figure 3.2. PWM control waveform of Sinusoidal modulation with $f_{tr} = 15\text{kHz}$ and $f_{CTRL} = 1\text{kHz}$. On the y-axis the time is expressed in second [s].

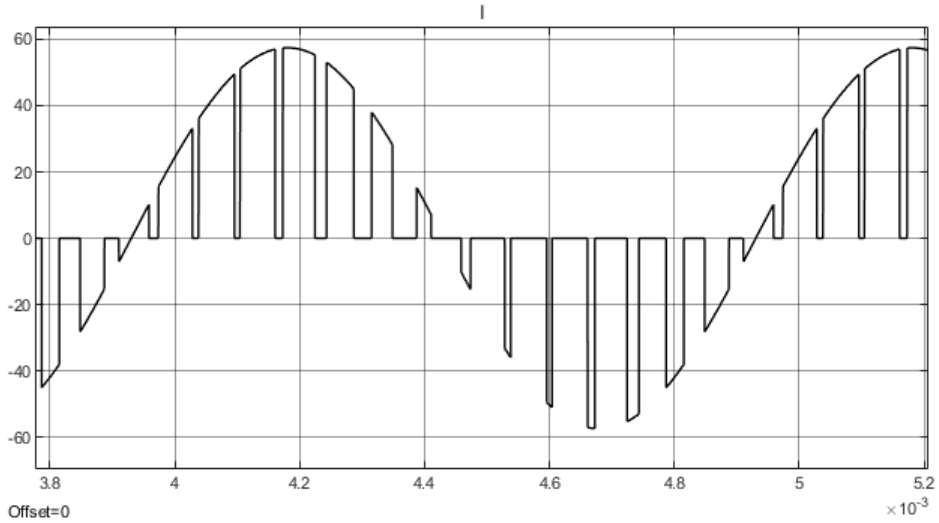


Figure 3.3. Switched current of IGBT $M5$ with $f_{tr} = 15\text{kHz}$, $f_{CTRL} = 1\text{kHz}$ and Sinusoidal PWM. On the y-axis the time is expressed in seconds [s], while on the x-axis the current is expressed in Ampere [A].

The line voltage obtained from the simulation confirms the analysis of Chapter 2: as Figure 3.4 shows, the line voltage has zero mean value and the AC component follows equation (2.8).

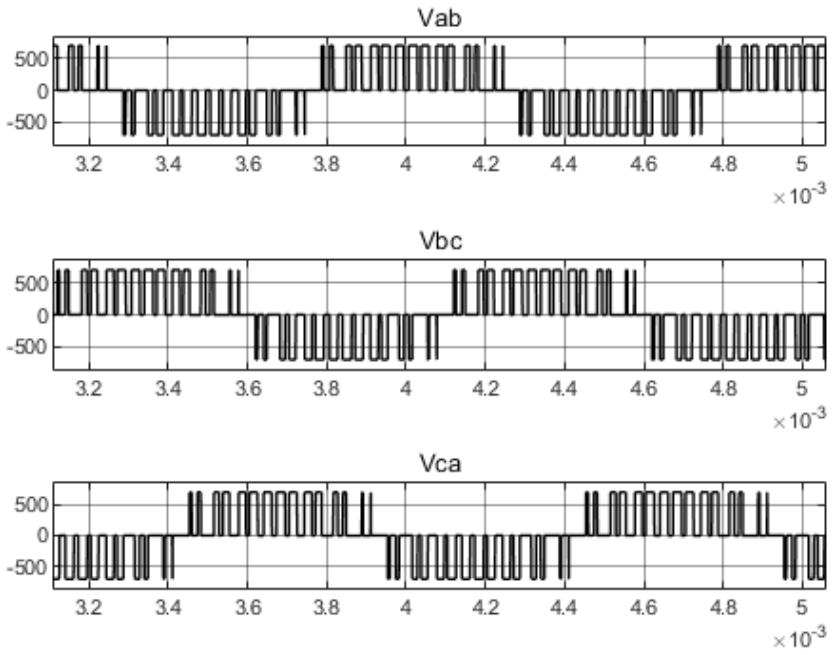


Figure 3.4. Line voltage v_{LL} with f_{tr} = 15kHz, f_{CTRL} = kHz and Sinusoidal PWM. On the y-axis the time is expressed in seconds [s], while on the x-axis the voltage is expressed in Volt [V].

The Sinusoidal PWM works in the linear region, in fact the maximum amplitude of the control voltages v_{CTRL} is equal to $0.7465V$ (Figure 3.5) and it is lower than the maximum amplitude of $v_{tr} = 1V$.

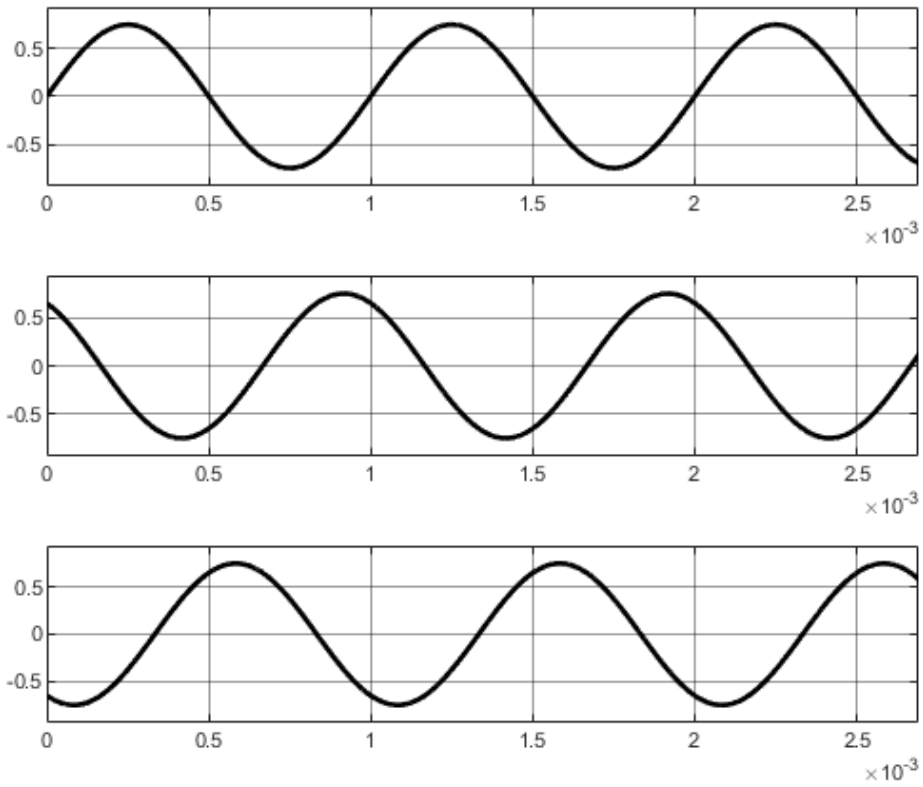


Figure 3.5. Sinusoidal references signals, each one with a phase shift of 120°. On the y-axis the time is expressed in seconds [s], while on the x-axis the voltage is expressed in Volt [V].

The only difference between the model with IGBTs and the one with power MOSFETs consists in the subsystem $INVERTER$ showed in Figure B.11. They are initialized with the same script listed in Appendix A.1.1 and the control subsystem has the same behaviour. The current of power MOSFET $M5$ controlled with the pulsed signal of Figure 3.2 is reported in Figure 3.6.

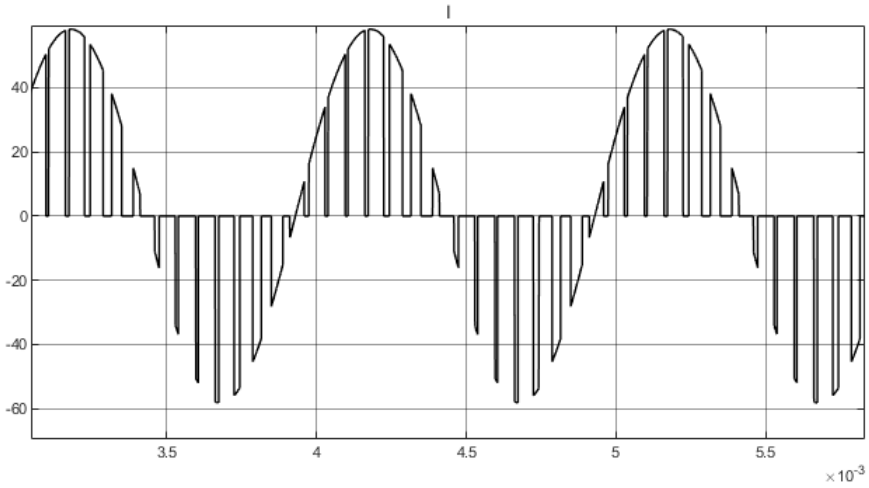


Figure 3.6. Switched current of power MOSFET $M5$ with f_{tr} = 15kHz, f_{CTRL} = 1kHz and Sinusoidal PWM. On the y-axis the time is expressed in seconds [s], while on the x-axis the current is expressed in Ampere [A].

In Figure 3.7 the phase voltage is reported: it is evaluated with the script listed in Appendix B.1 and its rms value is $\sqrt{3}$ times lower than the one of the line voltage of Figure 3.4.

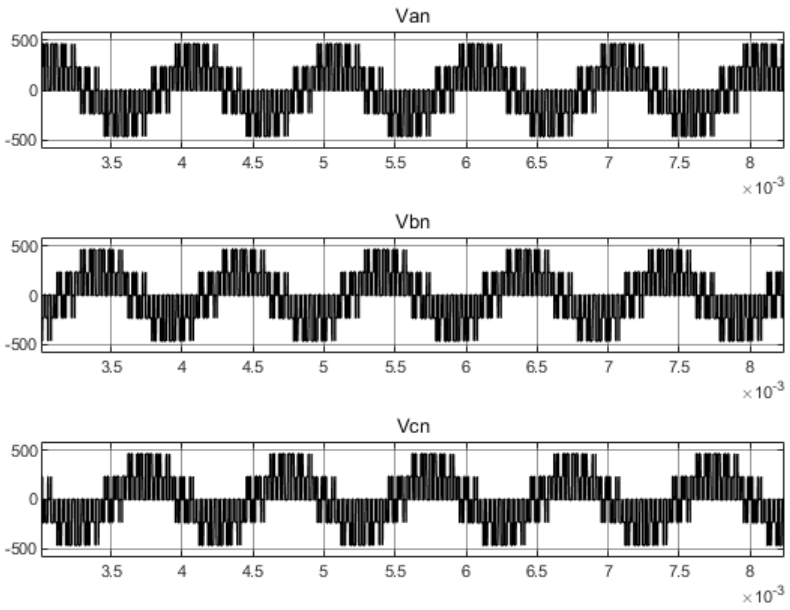


Figure 3.7. Phase voltage v_{LN} with f_{tr} = 15kHz, f_{CTRL} = 1kHz and Sinusoidal PWM. On the y-axis the time is expressed in seconds [s], while on the x-axis the voltage is expressed in Volt [V].

3.1.2 Space-Vector PWM

The main difference between the model with the Sinusoidal PWM and the one with Space-Vector PWM is in the control subsystem $SV\ PWM$, reported in Figure B.8: it is composed of two MATLAB functions that generate the three control signals to be compared with the triangular carrier signal. In order to write these functions, it is necessary to evaluate the average of the output phase voltages referred to the mid potential of the DC bus v_N:

$$v_N = \frac{V_d}{2} \tag{3.1}$$

Taking into account the symmetric switching pattern of Figure 2.12, using the general relation of the mean value of the phase voltages [23],

$$\bar{v}_{AN} = \frac{V_d}{2}(r_1 + r_2)T_{SW}\frac{1}{t_{sw}} \tag{3.2}$$

$$\bar{v}_{BN} = \frac{V_d}{2}(-r_1 + r_2)T_{SW}\frac{1}{t_{sw}} \tag{3.3}$$

$$\bar{v}_{CN} = \frac{V_d}{2}(-r_1 - r_2)T_{SW}\frac{1}{t_{sw}} \tag{3.4}$$

replacing equations (2.18) and (2.19) into equations (3.2), (3.3) and (3.4), imposing the relation (2.24) and taking into account that in the first quadrant

$$0 \leq \theta \leq \frac{\pi}{3} \tag{3.5}$$

it is possible to find, after some simplifications [23], the phase voltage mean values in the first quadrant:

$$\bar{v}_{AN} = \frac{1}{2}m_a V_d \cos\left(\theta - \frac{\pi}{6}\right) \tag{3.6}$$

$$\bar{v}_{BN} = \frac{\sqrt{3}}{2}m_a V_d \cos\left(\theta - \frac{2}{3}\pi\right) \tag{3.7}$$

$$\bar{v}_{CN} = \frac{1}{2}m_a V_d \cos\left(\theta + \frac{5}{6}\pi\right) \tag{3.8}$$

By iterating the previous steps for all the six active sectors, it is possible to obtain the reference voltages of the phase leg of the Space-Vector technique reported in Table 3.2. The outputs *dutyU*, *dutyV* and *dutyW* of the function *Reference Voltage* in the subsystem $SV\ PWM$ (Figure B.8) generate the reference voltage of Table 3.2, taking into account the simulation parameter set with the script *inverter_parameter* listed in Appendix A.1.2.

Sector	Leg A	Leg B	Leg C
1	$\frac{1}{2}m_a V_d \cos\left(\theta - \frac{\pi}{6}\right)$	$\frac{\sqrt{3}}{2}m_a V_d \cos\left(\theta - \frac{2}{3}\pi\right)$	$\frac{1}{2}m_a V_d \cos\left(\theta + \frac{5}{6}\pi\right)$
2	$\frac{\sqrt{3}}{2}m_a V_d \cos(\theta)$	$\frac{1}{2}m_a V_d \sin(\theta)$	$-\frac{1}{2}m_a V_d \sin(\theta)$
3	$\frac{1}{2}m_a V_d \cos\left(\theta + \frac{\pi}{6}\right)$	$\frac{1}{2}m_a V_d \cos\left(\theta + -\frac{5}{3}\pi\right)$	$\frac{\sqrt{3}}{2}m_a V_d \cos\left(\theta + \frac{2}{3}\pi\right)$
4	$\frac{1}{2}m_a V_d \cos\left(\theta - \frac{\pi}{6}\right)$	$\frac{\sqrt{3}}{2}m_a V_d \cos\left(\theta - \frac{2}{3}\pi\right)$	$\frac{1}{2}m_a V_d \cos\left(\theta + \frac{5}{6}\pi\right)$
5	$\frac{\sqrt{3}}{2}m_a V_d \cos(\theta)$	$\frac{1}{2}m_a V_d \sin(\theta)$	$-\frac{1}{2}m_a V_d \sin(\theta)$
6	$\frac{1}{2}m_a V_d \cos\left(\theta + \frac{\pi}{6}\right)$	$\frac{1}{2}m_a V_d \cos\left(\theta + -\frac{5}{3}\pi\right)$	$\frac{\sqrt{3}}{2}m_a V_d \cos\left(\theta + \frac{2}{3}\pi\right)$

Table 3.2. Phase leg reference voltages of Space-Vector PWM.

With a modulation index $m_a = 0.8$ and a control frequency $f_{CTRL} = 1\text{kHz}$, the reference signals of Figure 3.8 are generated. The similitude with the reference voltages of the third harmonic injection technique (Figure 2.8) turns out and this is the reason why Space-Vector PWM produces higher amplitude mean line voltages (equation 2.24) with respect to Sinusoidal PWM: the phase leg reference voltages are generated by sine waves injected with third-harmonic components without the use of more expensive modulator, such as in the case of the third harmonic injection technique.

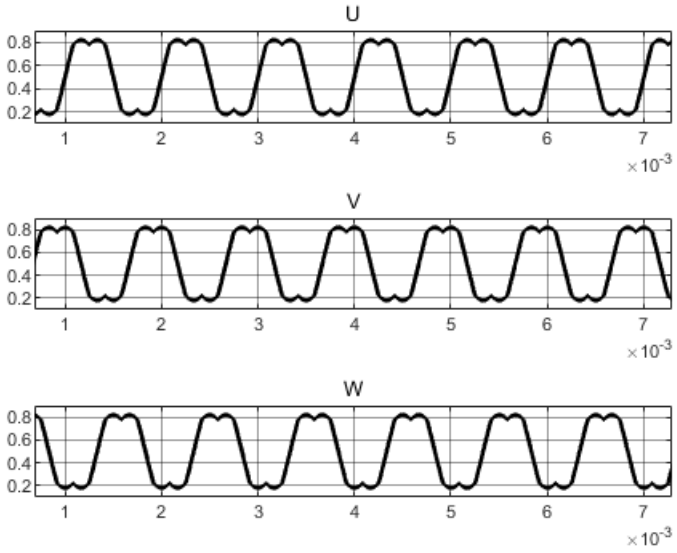


Figure 3.8. Phase leg references signals for leg A (signal U), leg B (signal V) and leg C (signal W). On the y-axis the time is expressed in seconds [s].

The reference voltages of Figure 3.8 are then compared with a triangular carrier frequency with unitary maximum amplitude and the pulsed gate control signal are obtained (Figure 3.9).

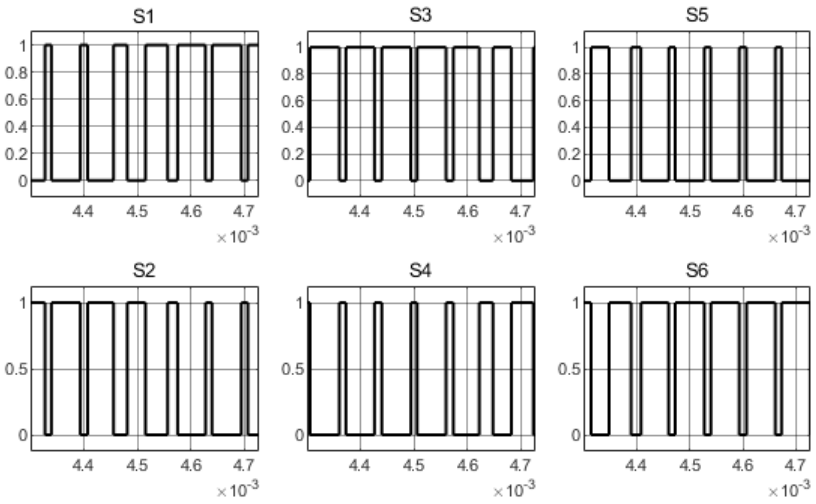


Figure 3.9. PWM control waveform of Space-Vector technique with $f_{tr} = 15\text{kHz}$ and $f_{CTRL} = 1\text{kHz}$. On the y-axis the time is expressed in second [s].

The control signals of Figure 3.9 drive the IGBT gate terminals of Figure B.3 and the pulsed current flowing into the switch $M5$ is reported in Figure 3.10.

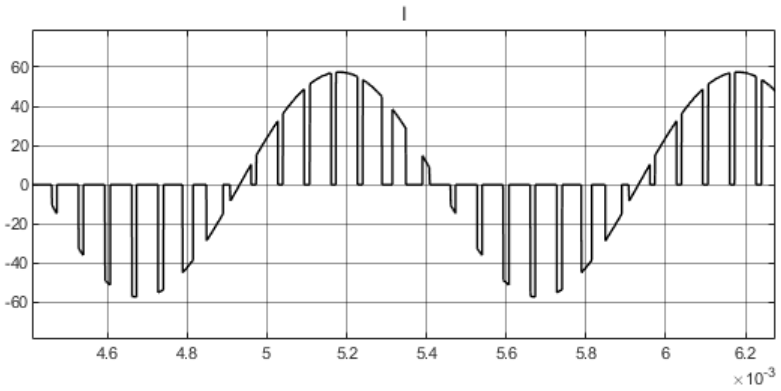


Figure 3.10. Switched current of IGBT $M5$ with $f_{tr} = 15\text{kHz}$, $f_{CTRL} = 1\text{kHz}$ and Space-Vector PWM. On the y-axis the time is expressed in seconds [s], while on the x-axis the current is expressed in Ampere [A].

The line voltages of Figure 3.11, obtained with the parameter values listed in the *inverter_parameter* script in Appendix A.1.2, have the same amplitude of the ones obtained with the Sinusoidal PWM, although the modulation index m_a is different. Taking into account equation 2.24, for the Space-Vector PWM it is obtained $m_a = 0.6465$ while, taking into account equation 2.8, the modulation factor for the Sinusoidal PWM was $m_a = 0.7465$. The ratio between these two

modulation index values is about 1.15 and it confirms the theory analysis carried out in Chapter 2.

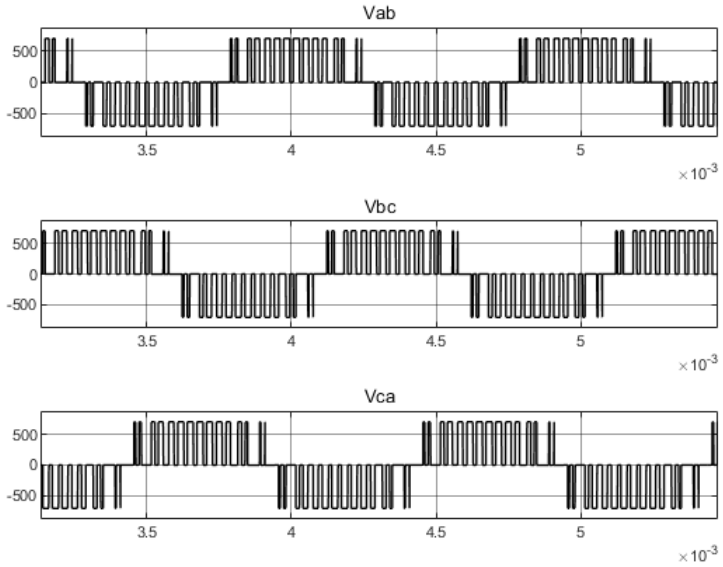


Figure 3.11. Line voltage v_{LL} with $f_{tr} = 15$kHz, $f_{CTRL} = 1$kHz and Space-Vector PWM. On the y-axis the time is expressed in seconds [s], while on the x-axis the voltage is expressed in Volt [V].

For what concern the model with power MOSFET, the block diagram can be seen in Figure B.12 and Figure B.13.

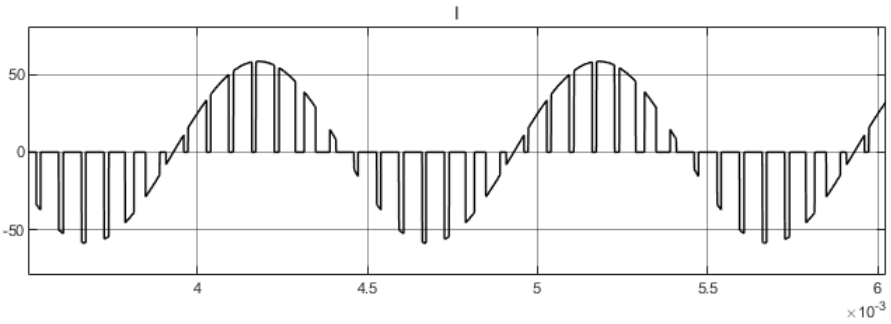


Figure 3.12. Switched current of power MOSFET $M5$ with $f_{tr} = 15$kHz, $f_{CTRL} = 1$kHz and Space-Vector PWM. On the y-axis the time is expressed in seconds [s], while on the x-axis the current is expressed in Ampere [A].

The pulsed current of transistor M5 (Figure 3.12) combined with the pulsed currents of the other five transistors give rise to the load output current showed in Figure 3.13. The frequency of these waveforms follows the frequency of the control

signals f_{CTRL} and the maximum amplitude is limited to 60 Amps thanks to the real-time supervision of the *Current control* function (Appendix B.1).

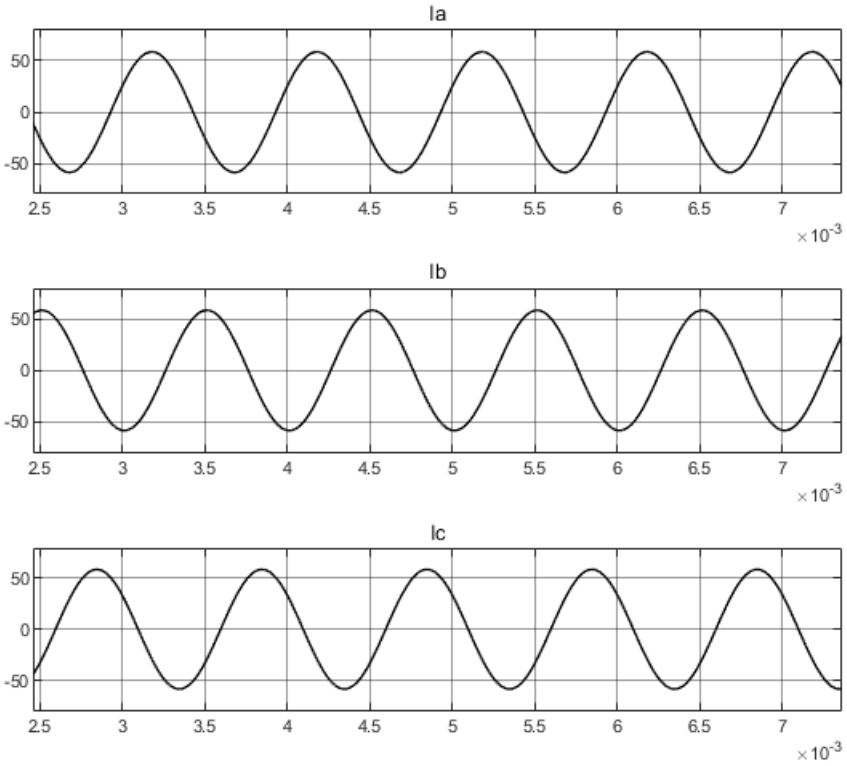


Figure 3.13. Output current of the three-phase VSI with f_{tr} = 15kHz, f_{CTRL} = 1kHz and Space-Vector PWM. On the y-axis the time is expressed in seconds [s], while on the x-axis the current is expressed in Ampere [A].

3.2 Simulation and calculation of losses

All the circuital models illustrated in the previous section have been developed with the aim to obtain the DC-link current of the inverter and in order to evaluate the switching losses of the power switches available on the market and, in order to do this, in Figure B.2, B.7, B.10 and B.13 the SIMULINK block *to workspace* can be noticed; it is used to store the MOSFET pulsed current or the IGBT pulsed current as a time-series in the workspace. The discussion about the DC-link current and the choice of the harmonic filtering solution is postponed to Chapter 4 while this Section is divided into three main parts:

1. research on the market and choice of some IGBTs and power MOSFETs well suited for the application;

2. creation of a library with the losses characteristic of chosen components;

3. simulation and real power losses evaluation;

Selection of the semiconductor switches

Looking on the websites of well-known sellers and of different manufacturers, many solutions are available: single transistors, half-bridge configurations and six-pack modules. A single transistor is a choice that leads to increase the volume of the system because its package is not optimized as a module but it allows bettering thermal dissipation thanks to the bigger size. On the other hand some modules allow to have all the six switches in a small package, furthermore they are optimized from a point of view of parasitic components with the drawback of an higher cost. Half-bridge packaging is a trade off between the other two configurations. The electric ratings of the transistors must be compliant with the specifications of Table 3.1 After many researches, the components reported in Table have been chosen.

	Manufacturer	Configuration	Topology
CM100TX(P)-24T	Mitsubishi	six-pack	IGBT
SEMiX101GD12E4s	Semikron	six-pack	IGBT
SK100GD12T4T	Semikron	six-pack	IGBT
SEMiX101GD12Vs	Semikron	six-pack	IGBT
FS75R12KT4_B15	Infineon	six-pack	IGBT
IRGPS60B120KDP	Infineon/IR	single	IGBT
APTMC120TAM33CTPAG	Microsemi	six-pack	SiC MOSFET
CCS050M12CM2	Cree	six-pack	SiC MOSFET

Table 3.3. MOSFETs and IGBTs suitable for the application of this project.

They have been selected because they have breakdown voltages higher than the DC bus voltage of 700V, they can handle a current higher than 60A also with hotter temperatures and they have a good trade off between cost and performances. Furthermore, all the MOSFETs are SiC devices because they are the state-of-the-art of the MOSFET for this power rating, as already explained in Chapter 1.

Definition of a library of switch parameters

In order to evaluate the losses, some important parameters typically reported on the switch data-sheet must be taken into account: the on-resistance, the voltage drop across the switch during the conduction and the switching energy losses. All these parameters have been evaluated for the device showed in Table 3.3 and, in particular, all the switching energy losses curves have been stored in MAT file

using *Grabit* (Figure 3.14), which is a GUI program capable to manually extract data point from a file and to save it.

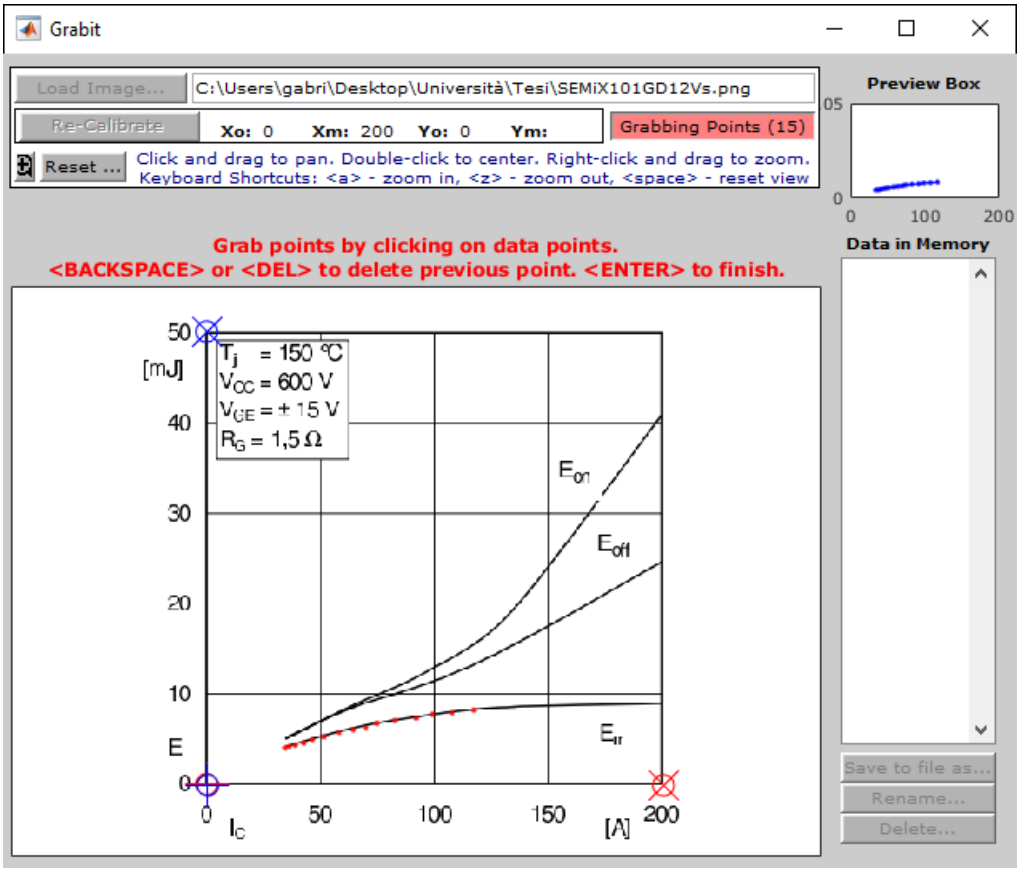


Figure 3.14. Screenshot of the GUI of Grabit while grabbing points.

For what concerns the on-resistance values, in order to neglect the temperature variations (the reason of this is reported in the subsection 3.2), they are reported with its mean value, computed between minimum and maximum value written on data-sheet. The on-state voltage drop values read from the data-sheet are scaled with a correction factor equal to the ratio of maximum and minimum value and then, for an engineering calculation, a safety margin value of 15% is also used [17].

All the MAT files with the switching losses curves have been stored in one file creating a sort of offline library; this allows to make future comparison with newest device, for example when a GaN MOSFET will be available for higher power ratings it will be sufficient acquire its switching energy losses curves, store it in the library and compare its performance with the other ones.

Power losses evaluation

In all the switching devices, power losses might be divided into three groups [59]:

1. conduction losses of the transistor and of the diode; they depend on the load current, junction temperature and duty cycle;
2. switching losses of the transistor and of the diode; they depend on the load current and the electric load type (inductive for the interest of this project), the DC input voltage, junction temperature and the switching frequency;
3. leakage losses, normally neglected because they typically gain importance just in case of blocking voltages higher than $1kW$ and/or with operating temperatures over 150°.

In a Voltage Source Inverter, duty cycle, load current and junction temperature are not constant because they depend on the fundamental frequency of the AC side (in the case of this project $f_{out} = 50Hz$), thus also power losses changes in time [51]. For the purpose of this project a so in-depth analysis is not required, hence the following simplifications can be imposed for estimating the expected power dissipation during converter operation mode in a more practical way:

- switching times are neglected;
- constant junction temperature (approximation due to $f_{out} = 50Hz$) [59];
- linear modulation.

For what concern the IGBT, instantaneous conduction losses p_{CT} can be estimated linearising the IGBT by a series connection of DC voltage source v_{CE0} representing the on-state collector-emitter voltage drop with a collector-emitter on-resistance $r_{CE,on}$; being i_{CE} the current through the collector-emitter terminals [17]:

$$p_{CT}(t) = v_{CE0} i_{CE}(t) + r_{CE,on} i_{CE}^2(t) \tag{3.9}$$

Taking into account the MOSFET instantaneous conduction losses p_{CM}, they can be calculated using a linear model with the drain-source on-resistance $r_{DS,on}$; being i_{DS} the current through the drain-source terminals [18]:

$$p_{CM}(t) = r_{DS,on} i_{DS}^2 \tag{3.10}$$

For what concern the anti-parallel diode, instantaneous conduction losses p_{CD} can be evaluated in the same way, for both IGBT and MOSFET, with a diode approximation composed by a DC voltage source v_{d0} representing the on-state voltage drop, connected in series with the diode on-resistance r_d; being v_d the voltage across the diode and i_f the forward current through the diode [18]:

$$p_{CD}(t) = v_{d0} i_f(t) + r_d i_f^2(t) \tag{3.11}$$

The switching losses are estimated storing the instantaneous current of the switch from the simulation of the SIMULINK models illustrated in the previous section and using it as an input parameter to read the switching energy losses curves stored in the library created with *GRABIT*.

The script used to evaluate the IGBT losses is listed in Appendix A.2.1 while the one used for power MOSFET is in Appendix A.2.2. The difference between the two scripts is mainly in the last part, because the MOSFET reverse conduction opportunities makes the IGBT equations unsuitable for the calculation of MOSFET conduction losses in an inverter system. A very exhaustive numeric method can be found in [57] but, in order to be able to directly compare the MOSFET conduction losses with the IGBT ones, the models must have the same approach. This is the reason why the linearisation approach of [17] and [18] is the reference one used during the implementation of scripts A.2.1 and A.2.2. Furthermore, the SiC MOSFETs selected are with zero reverse recovery current.

Despite the presence of two script, the general flux of the analysis is the same:

1. the first step is loading the parameters of the transistor to simulate by uncomment the section of the script with the switch identification number and commenting the other ones;

2. with the switch parameters stored in the workspace, the *trigger* section of the script loads the data points of transistor current (Figure 3.10) passed by the SIMULINK simulation, and then it selects only one period (Figure 3.15) of this waveform searching the acquisition starting point after ten periods (in order to have the current at steady state condition);

3. the third section of the codes, called *edge detection*, isolates all the current values during the transitions (Figure 3.16) by detecting all the fronts of the waveform and by storing the current values on it; it also stores the conduction current values because they are the ones between a rising and a falling edge;

4. the last part is composed of two sections, one for the evaluation of the conduction losses and one for the evaluation of the switching losses. In section *conductionlosses*, equation (3.9) or equation (3.10) is used during the positive half part of current period, combined with the equation (3.11) that evaluates the diode conduction losses during the negative half part. Section *switching losses* is the only part with cyclic function because the *for* cycle takes the corresponding switching energy value from the library for each current peak isolated in *edge detection* section. The instantaneous on-switching losses are associated with the rising-edge peaks of the positive half part of the current, the instantaneous off ones are associated with the falling-edge peaks of the positive half part of the period, while the instantaneous recovery losses of the diode are significant only during the rising-edge of the negative half period of the current [17], [18], [59]. The average value of the conduction losses is

obtained integrating the instantaneous power losses over the switching cycle and in this case the MATLAB function *trapz* is used.

The code explained in as before has been redacted minimizing the use of cyclic function and maximizing the use of built-in MATLAB function; the result is a code more readable, faster and with few hardware resources used [7], hence the simulation is completed in about six seconds.

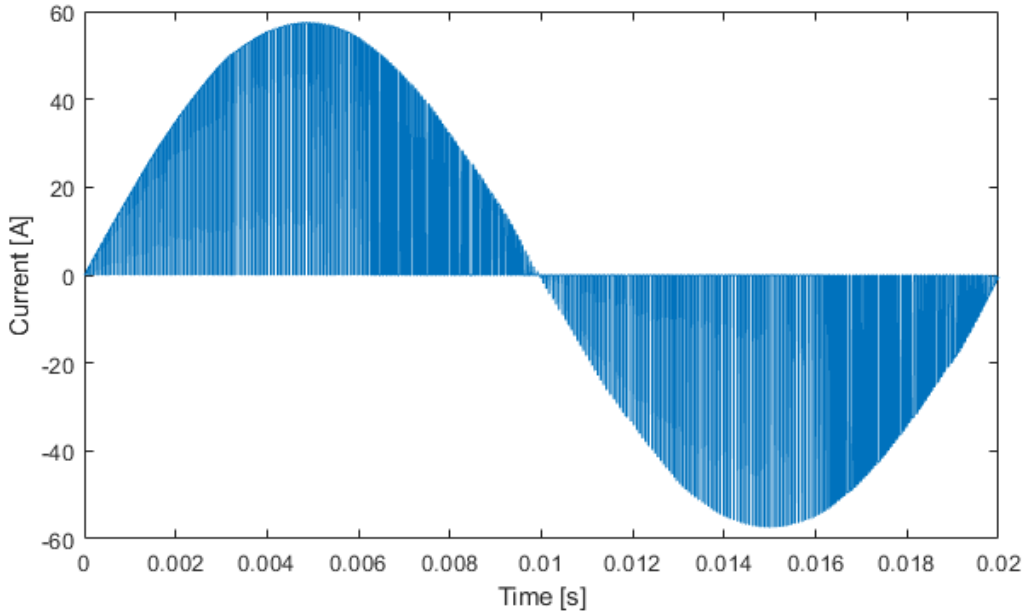


Figure 3.15. One period of the transistor $M5$ current used to calculate losses.

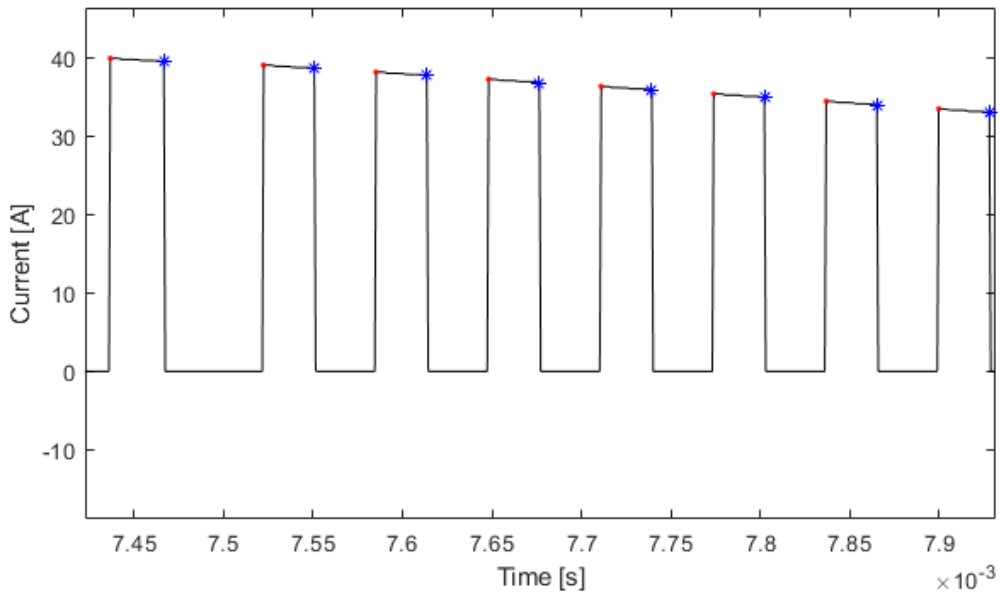


Figure 3.16. Current amplitude values during the transitions.

The inverter parameter for the simulation of losses have been setted following the specifications of Table 3.1 and, for the parameter without restrictions, the values of Table 3.4.

Phase-to-phase output voltage V_{rms}	320V
Output Frequency	50Hz
Power Factor $\cos(\phi)$	0.8
Switching frequency	15kHz
Death time	200ns

Table 3.4. Parameter values for losses simulation.

The conduction losses of the six-pack module Semikron SK100GD12T4T are reported in Figure 3.17. The orange curve is the instantaneous power dissipated in the IGBT while the blue curve is the instantaneous power dissipated during in the diode: it is visible that the transistor technology is typically more optimized than the diode, thus the blue curve is higher than the orange one.

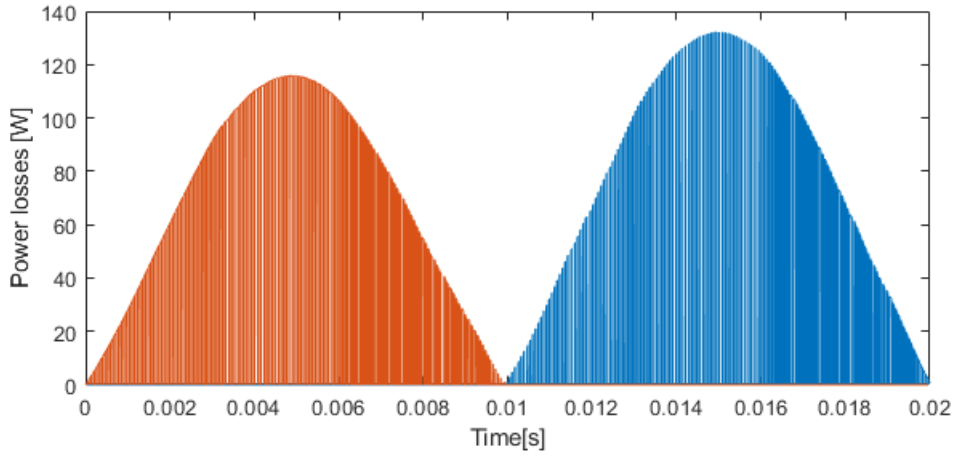


Figure 3.17. Instantaneous conduction losses of Semikron SK100GD12T4T.

Furthermore, Figure 3.18 shows the instantaneous switching energy losses of Semikron SK100GD12T4T: the blue curve reports the switching on losses, the black curve measures the switching off losses and recovery losses associated with the diode are shown in the red curve. The amplitude of these curves is related to the energy curves that the manufacturer includes on the data-sheet (Figure 3.19) where the losses associated with the turn-on are the most relevant while the recovery switching energy plays a minor role.

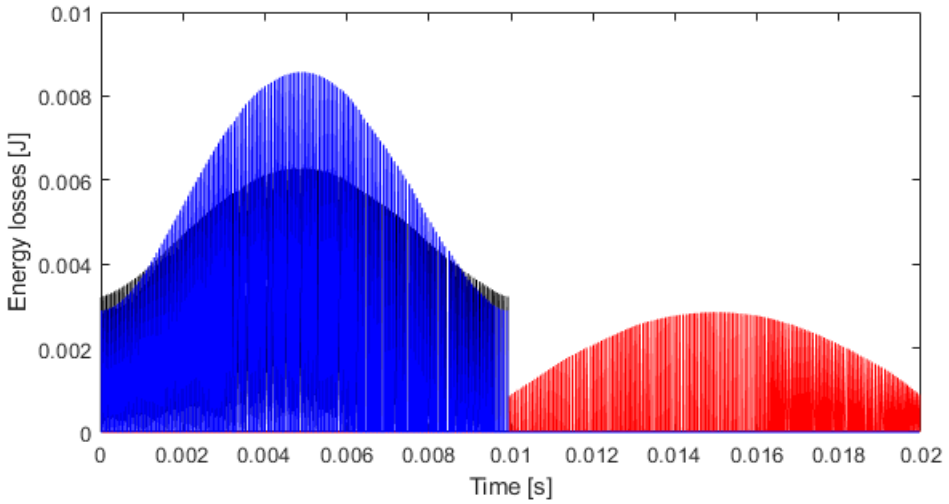


Figure 3.18. Instantaneous switching losses of Semikron SK100GD12T4T.

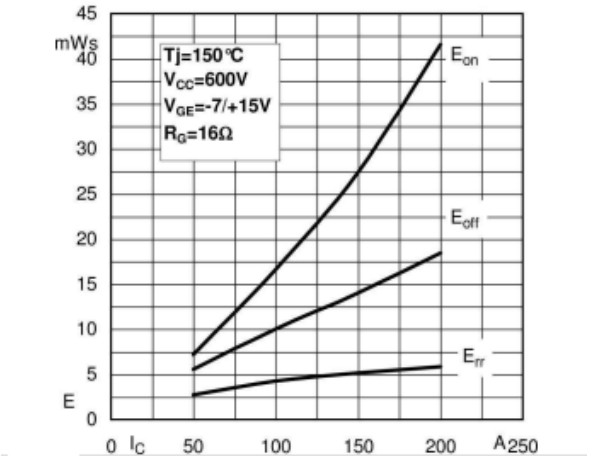


Figure 3.19. Energy losses of Semikron SK100GD12T4T with respect of the collector-emitter current.

These curves have been evaluated for all the switches of Table 3.3 and the total switching losses in the transistor and in the free-wheeling diode have been computed with the following expressions for average powers [17], [18]:

$$P_{MOS} = P_{CM} + P_{switch,MOS} \tag{3.12}$$

$$P_{IGBT} = P_{CT} + P_{switch,IGBT} \tag{3.13}$$

$$P_{DIODE} = P_{CD} + P_{switch,DIODE} \tag{3.14}$$

The simulation result of these simulations are visible in Table 3.5; it can be helpful to remember that all the losses there reported are referred to one period of the output frequency $T_{out} = 0.02s$.

Data of Table 3.5 have to be validated in order to be sure that wrong choices will be not induced by these simulations. So, the IGBT modules manufactured by Semikron have been used as samples to validate the implemented model, because this company has released a free online simulator called *SemiSel* with the aim to help beginners with the design of power converters [59]. In this case, *SemiSel* has been used to make a comparison between the power losses obtained with the script of Appendix A.2.1 and the power losses obtained from this online tool.

	Sinusoidal PWM		Space-Vector PWM	
	P_{IGBT}	P_{DIODE}	P_{IGBT}	P_{DIODE}
CM100TX(P)-24T	88.6529W	37.2269W	84.9944W	34.4521W
SEMiX101GD12E4s	100.8295W	32.0871W	91.4382W	29.2488W
SK100GD12T4T	110.0492W	29.3469W	105.4490W	27.3270W
SEMiX101GD12Vs	102.8282W	38.5035W	100.4630W	34.8016W
FS75R12KT4_B15	78.4410W	36.6533W	76.9027W	33.8027W
IRGPS60B120KDP	80.1774W	36.7392W	78.7267W	34.8611W
	P_{MOS}	P_{DIODE}	P_{MOS}	P_{DIODE}
APTMC120TAM33CTPAG	54.1831W	26.2657W	52.1495W	25.0484W
CCS050M12CM2	52.8522W	25.6065W	51.4272W	24.6259W

Table 3.5. Average power losses for the switches of Table 3.3.

The *SemiSel* simulation outputs are reported in Table 3.6; considering that *SemiSel* takes into account the temperature variations of the IGBT parameters (Figure 3.20), the results are pretty close to the one obtained from the simulator implemented in this Thesis project (Table 3.5) and this validate the developed model described in this Thesis that can be useful for a quick comparison and selection of a suitable switch for the given application.

	P_{IGBT}	P_{DIODE}
SEMiX101GD12E4s	102W	29W
SK100GD12T4T	112W	31
SEMiX101GD12Vs	105W	38W

Table 3.6. SemiSel simulation results.

Carefully analysing Table 3.5 and taking into account that the purpose is to obtain a high power density and high efficient converter, the six-pack module CCS050M12CM2 manufactured by Cree/Wolfspeed has been chosen because it is more efficient, it has higher breakdown voltage compared with Silicon of the same

scale, lower on state resistance and higher thermal conductivity [36]. Furthermore, combined with the Space-Vector modulation technique, it allows to reach high power density combined with high frequency [13]: essential features for lower overall cost, weight and cooling requirements that are the main challenges of the heavy-duty sector.

Device :

Product line	**SEMiX**
Device	**SEMiX101GD12E4s**
Use maximum values	Yes
Max. junction temparature	175°C

Transistor		**Diode**	
E_{tr}	24.1 mJ (@600V)	E_d	6.5 mJ
$V_{CE0.150}$	0.8 V	$V_{T0.150}$	1.1 V
$r_{C.150}$	16 mOhm	$r_{T.150}$	13.7 mOhm
$V_{CE.sat}$	2.40 V	V_f	2.47 V
I_c	100.00 A	I_f	100.00 A
$R_{th(j-c)}$	0.27 K/W	$R_{th(j-c)}$	0.48 K/W
$R_{th(c-s)}$	0.04 K/W		

Data set from 2011/08/01

Calculated losses and temperatures with rated current, at overload and at $f_{min\ out}$:

	Rated current	Overload	f_{min} and Overload
$P_{cond\ tr}$	23 W	23 W	23 W
$P_{sw\ tr}$	79 W	79 W	79 W
P_{tr}	102 W	102 W	102 W
$P_{cond\ d}$	9.89 W	9.89 W	9.89 W
$P_{sw\ d}$	19 W	19 W	19 W
P_d	29 W	29 W	29 W

Figure 3.20. SemiSel simulation results for the SEMiX101GD12Vs.

Thus, after all the theoretical assessments and simulations the choice for the switches topology and their modulation strategy is **Cree/Wolfspeed CCS050 M12CM2 with Space-Vector PWM technique**. The losses simulation of this configuration is reported in Figure 3.21 and Figure 3.22.

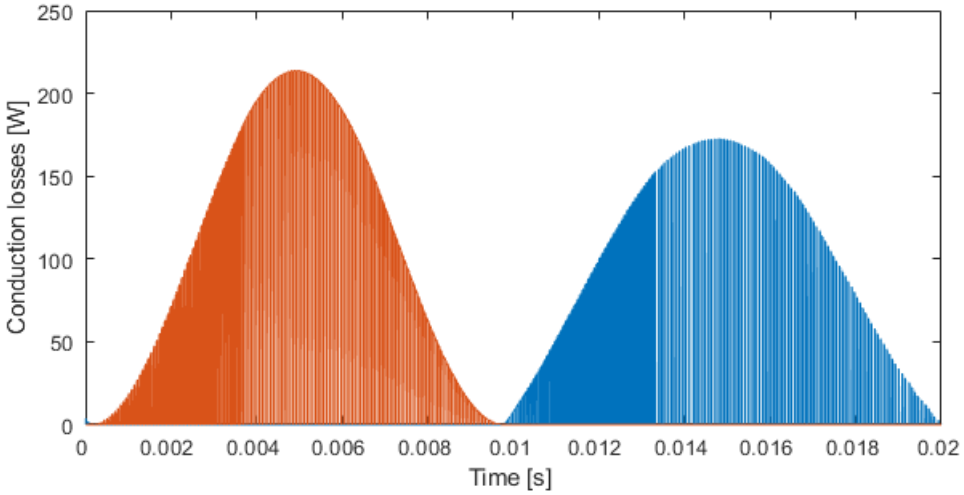


Figure 3.21. Instantaneous conduction losses of Cree CCS050M12CM2 with Sace-Vector PWM. On the left MOSFET conduction losses, on the right body-diode conduction losses.

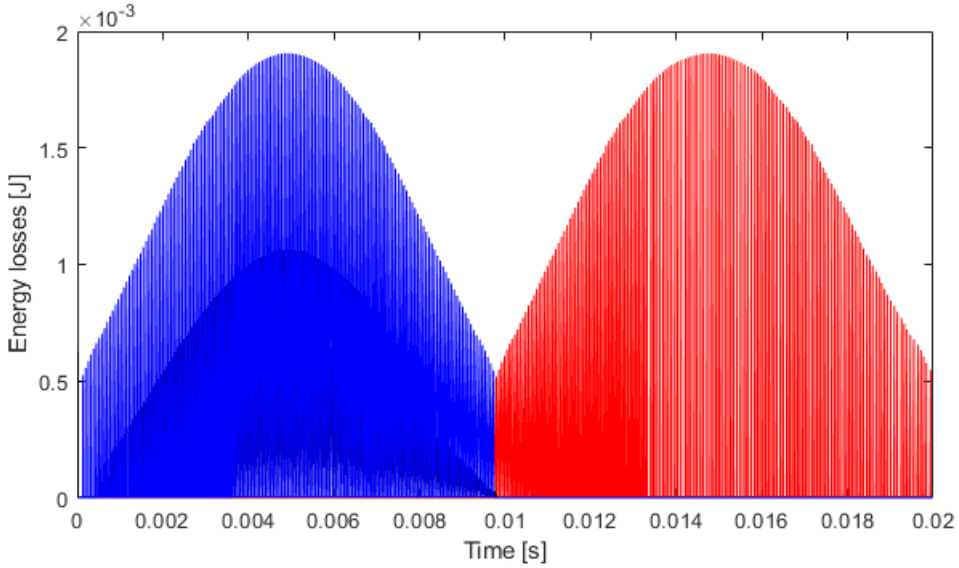


Figure 3.22. Instantaneous switching losses of Cree CCS050M12CM2 with Sace-Vector PWM. Turn-on losses in blu, turn-off losses in black, recovery losses in red.

From Table 3.5, the benefit of the symmetric Space-Vector PWM technique (Figure 2.12) in terms of power losses reduction is not clearly visible. The reason is the relatively low switching frequency: when it is increased and the output frequency is kept constant, the Sinusoidal PWM dissipates much more power and this is showed in Figure 3.23. Nevertheless, Space-Vector PWM technique gives much more advantages in terms of output harmonic reduction [24].

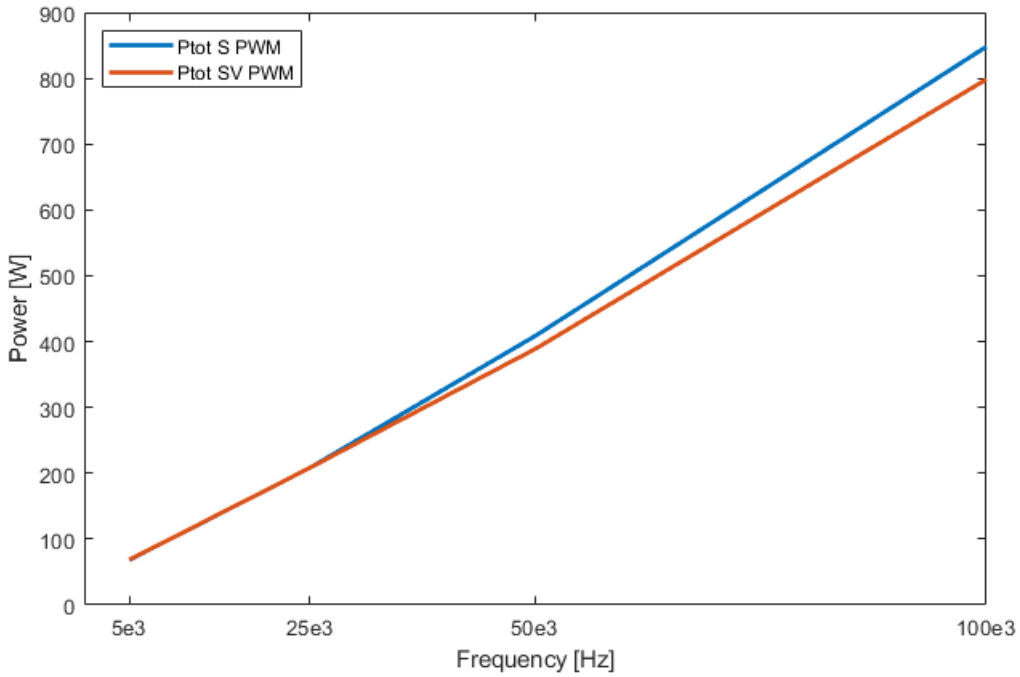


Figure 3.23. Total power losses in function of increasing switching frequency and with different PWM strategies.

Chapter 4

Analysis of the DC-link Current

The DC-link current of a power converter is the input current that it absorbs from the DC source, which is also called DC-link. In automotive and heavy-duty applications, the DC-link current is the current absorbed by the inverter from a rechargeable battery pack and it is the superposition of a DC current provided by the batteries and of an AC component. This last high ripple component must be filtered out by a harmonic filtering system.

In this Chapter the DC-link Current of a three-phase two-level Voltage Source Inverter is evaluated in order to choose the DC-link capacitor: it is necessary to provide reactive power, attenuate ripple current, reduce the emission of electromagnetic interference, and suppress voltage spikes caused by leakage inductance and switching operations [58]. Furthermore, in the last Section of the Chapter, an overview of alternative harmonic filtering solutions is described because DC-link capacitor might be unsuitable for some applications.

4.1 Calculation of DC and AC components of the DC-Link Current

Taking into account Figure 2.2, assuming a lossless three-phase VSI with a three-phase wye-connected balanced inductive load, furthermore, assuming that the inverter does not store energy and no dead-time is needed by the switches the instantaneous power balance assumes the following form:

$$V_d(t)\, I_d(t) = v_{AN}(t)\, i_A(t) + v_{BN}(t)\, i_B(t) + v_{CN}(t)\, i_C(t) \tag{4.1}$$

where $I_d(t)$ is the DC-link current.

If only the average values of equation (4.1) are considered, the following expression holds:

$$\begin{aligned} V_d I_d = \hat{V}_{LL}\hat{I}_{LL}\cos(\omega_{out}t)\cos(\omega_{out}t-\phi) + \\ + \hat{V}_{LL}\hat{I}_{LL}\cos\left(\omega_{out}t-\frac{2}{3}\pi\right)\cos\left(\omega_{out}t-\phi-\frac{2}{3}\pi\right) + \\ + \hat{V}_{LL}\hat{I}_{LL}\cos\left(\omega_{out}t+\frac{2}{3}\pi\right)\cos\left(\omega_{out}t-\phi+\frac{2}{3}\pi\right) \end{aligned} \tag{4.2}$$

and, taking into account also equation (2.1), the DC Component of the DC-Link current can be computed:

$$I_d = \frac{3}{2}\frac{\hat{V}_{LL}}{V_d}\hat{I}_{LL}\cos(\phi) \tag{4.3}$$

where $\hat{V}_{LL}$ is the line voltage amplitude and $\hat{I}_{LL}$ is the line current amplitude. If a Space-Vector modulation strategy is applied to the inverter, the DC bus voltage V_d and the line voltage are related by means of the relation (2.24), so equation (4.3) becomes:

$$I_d = \frac{\sqrt{3}}{2}\hat{I}_{LL}m_a\cos(\phi) \tag{4.4}$$

Equation (4.4) shows that the DC Component of the DC-Link current is time invariant and it changes just in function of the modulation index m_a and of the power factor $\cos(\phi)$.

When equation (4.2) has been obtained, only mean values have been considered: the AC behaviour of the current is lost and so only the DC-Link current has be computed. Now, starting again from equation (4.1), the aim is to evaluate the ripple current that a possible harmonic filtering system should sink. In Chapter 3, the outputs of the SIMULINK models show that the line voltage of the inverter is a square wave composed of variable width pulses (Figure 3.4, 3.11). The spectrum of these type of waveforms is full of harmonics (Figure 2.5) and they affect also the DC-side of the inverter in the form of a polluted current. This AC ripple current can be evaluated in time domain with the switching function approach [16], [29], [40], [39].

Without the use of mean values in equation (4.1), the DC-link current in time domain is:

$$I_d(t) = \frac{v_{AN}(t)}{V_d(t)}i_A(t) + \frac{v_{BN}(t)}{V_d(t)}i_B(t) + \frac{v_{CN}(t)}{V_d(t)}(t)\,i_C(t) \tag{4.5}$$

The ratio on the right side between phase voltages and the DC-link voltage is called the switching function $s_x(t)$

$$\frac{v_{xN}(t)}{V_d} = s_x(t) \tag{4.6}$$

from which an alternative expression for equation (4.5) can be derived:

$$I_d(t) = s_A(t)\, i_A(t) + s_B(t)\, i_B(t) + s_C(t)\, i_C(t) \tag{4.7}$$

Figure 4.1 can be taken as reference in order to have a clearer vision of the switching function concept: a switching function is a logic signal with state 0 or 1 and the transition between these states happens simultaneously with the transition of the PWM control signal of each leg (Figure 4.1.b).

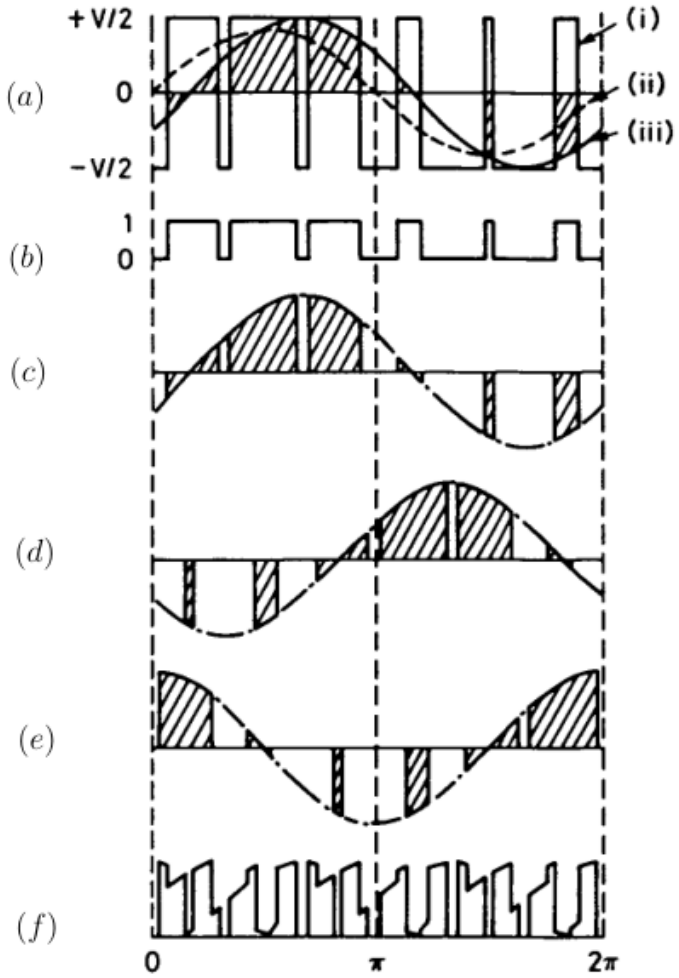


Figure 4.1. Construction of the DC-link current by means of switching functions: (a)(i) inverter leg voltage, (a)(ii)fundamental component of leg voltage, (a)(iii)sinusoidal current; (b) switching function; (c),(d),(e) DC-link current of the three legs; (f) total DC-link current. [16]

The DC-link current of Figure 4.1.c is constructed by multiplying the sinusoidal current of Figure 4.1.a with the switching function of Figure 4.1.b. The currents

of Figure 4.1.d and Figure 4.1.e are the DC-link currents of the other two legs and summed up with the one of Figure 4.1.c give rise to the total DC-link current of a three-phase inverter.

Since switching functions are strictly related to the PWM technique implemented for the inverter, for the choice made in Chapter 3, the switching functions of the symmetric Space-Vector PWM must be found. Following the construction steps of Figure 4.1 and taking into account equation 4.6, the switching functions of the symmetric PWM are computed in the following way:

1. takes the phase leg reference voltages at the commutation poles of Figure 3.8;
2. compare each reference signal with a triangular carrier waveform;
3. each switching function goes in the high state when the amplitude of the reference signal of each leg is higher or equal with respect the carrier, while it goes in the low state in the opposite case.

Figure 4.2 shows an example of this procedure for a carrier frequency $f_{SW} = 60\text{kHz}$ and an output frequency $f_{out} = 5\text{kHz}$.

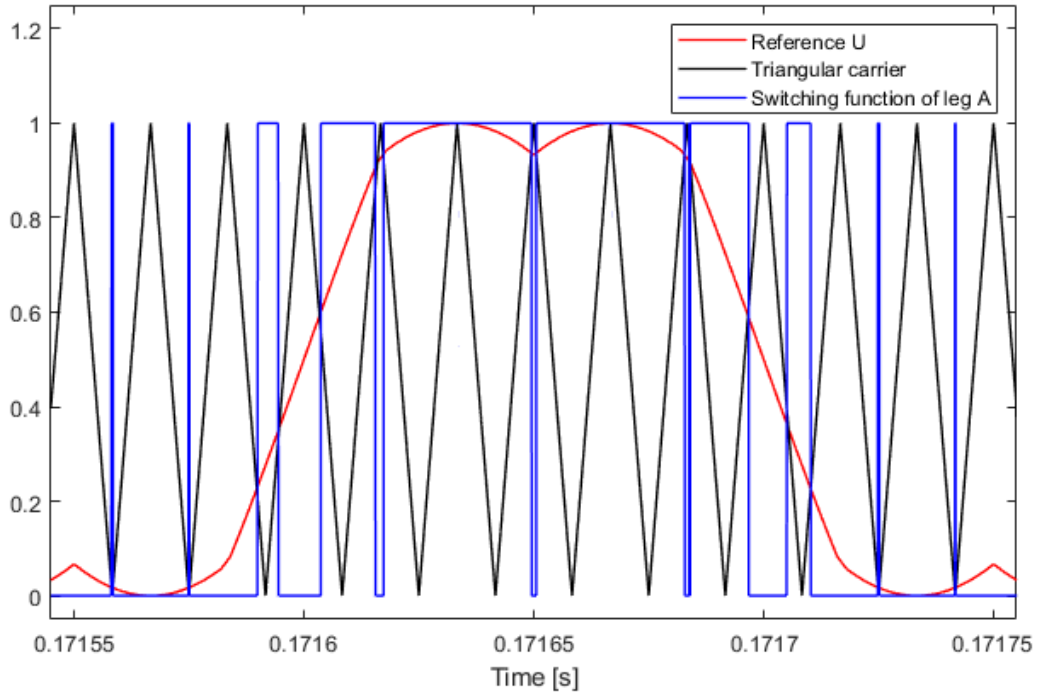


Figure 4.2. Example of switching function construction for leg A.

Multiplying the output currents with the switching functions, a theoretical evaluation of the DC-link current is obtained. Taking into account the specifications of

Table 3.1 and imposing $cos\,(\phi) = 0.8$ the leg A DC-link current for the three-phase VSI can be evaluated (Figure 4.3) and, summing up the DC-link current of all the legs (Figure 4.4), the total DC-link current reported in Figure 4.5 is obtained.

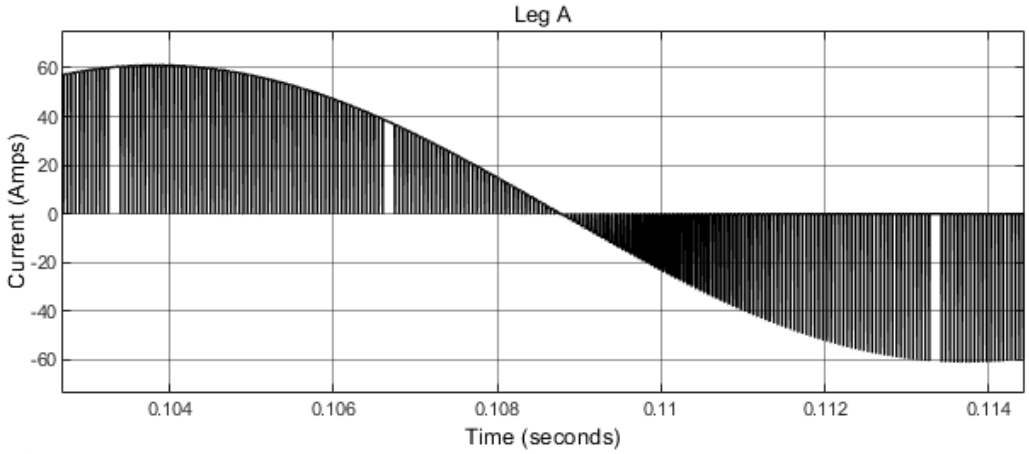


Figure 4.3. DC-link current of leg A.

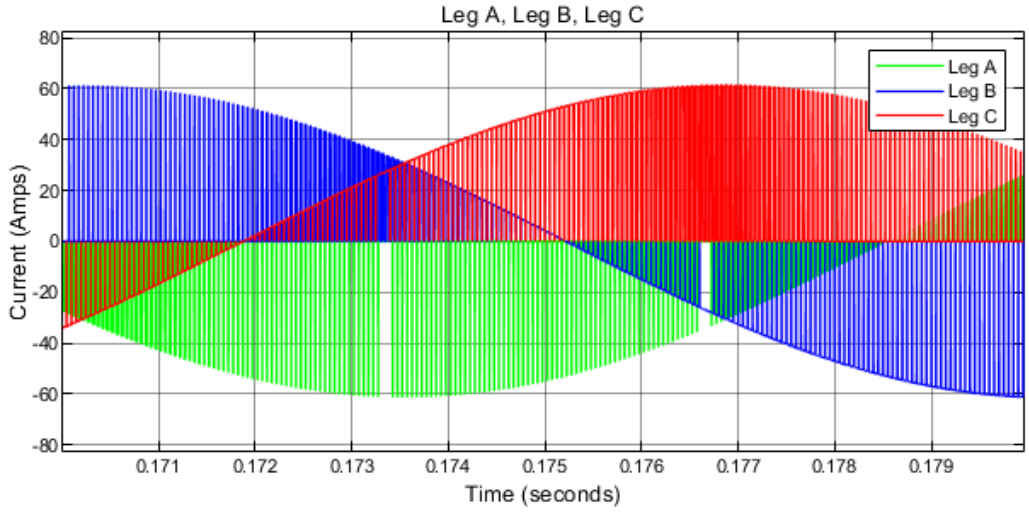


Figure 4.4. DC-link current of the three legs.

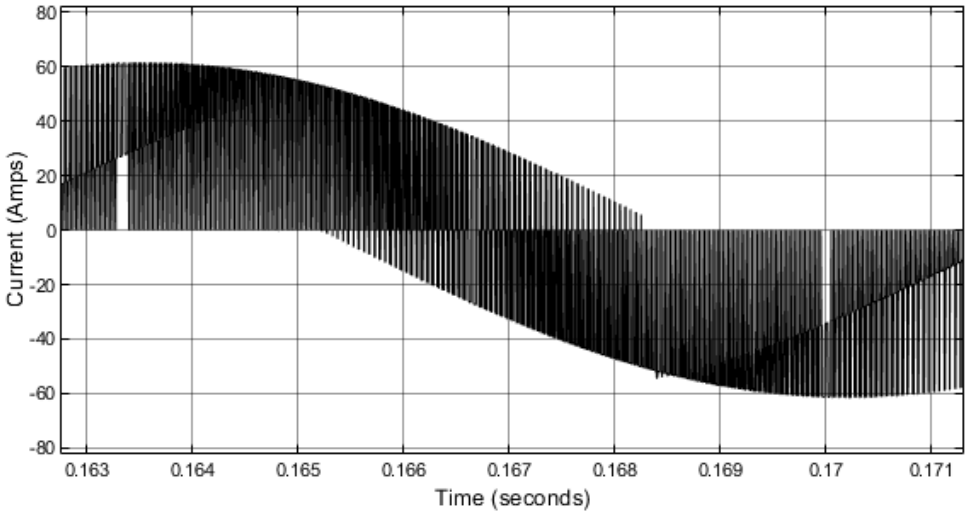


Figure 4.5. Total theoretical DC-link current of the inverter with $f_{SW} = 20kHz$ and $f_{out} = 50Hz$.

4.2 Selection of the DC-link capacitor

In a three-phase two-level Voltage Source Inverter the input capacitor is used for different purposes [29]:

- to supply the input pulsed current of the inverter;
- to reduce the spread of current harmonics into the DC source;
- to supply power during transient-peak and to protect the inverter from transient-peaks of the DC-link voltage.

Important parameters in the selection of a capacitor are the operating voltage and the working temperature because, as established by the Arrhenius Law, if the working temperature is reduced the typical working life doubles for every 10° below the rated temperature [55]. The analysis carried out in section 4.1 is sufficient as first approximation but, in order to choose the right capacitor for the power ratings of heavy-duty applications, he worst-case evaluation of the root mean square of ripple DC-link current and a harmonic current evaluation are fundamental aspects. The problem has been exhaustively resolved in [29] and in this section only the relevant results for the design purposes of this thesis are reported.

The evaluation of a rms value of the inverter harmonic current depends on the relationship between the space vectors of Table 2.1 and the segment of output current used to build the DC-link current: different segments of the output current correspond to different switching states and so to different sectors. The results are

obtained assuming a symmetric ideal three-phase voltage system, a balanced load, a purely sinusoidal shape of the inverter output currents, linear modulation and neglecting the dead-time. Under these assumptions, the expression of the global rms value of inverter input current [29]

$$I_d^{rms} = I_{LN}^{rms} \sqrt{\left[\frac{m_a}{\pi}\left(1 + 4\cos^2(\phi)\right)\right]} \tag{4.8}$$

obtained considering only the fundamental components of the output phase current, is valid in all the sector of the Space-Vector PWM.

As mentioned at the beginning of the Chapter, the inverter input current can be seen as the superposition of two orthogonal component, the DC one coming from the DC source and the AC one sink by the harmonic filtering system. In this project, a capacitor is the selected harmonic filtering system, hence the rms value of the AC component is the one of interest and it is given by [29]:

$$I_{d,AC}^{rms} = I_{LN}^{rms} \sqrt{m_a \left[\frac{1}{\pi} + \left(\frac{4}{\pi} - \frac{3}{2} m_a\right)\cos^2(\phi)\right]} \tag{4.9}$$

In order to size the capacitance, the worst case condition of this current must be identified; thus, the dependence of the ratio between the ripple DC-link current and the phase current

$$\frac{I_{d,AC}^{rms}}{I_{LN}^{rms}}$$

from the power factor $\cos(\phi)$ and from the modulation index m_a is reported in Figure 4.6 and Figure 4.7.

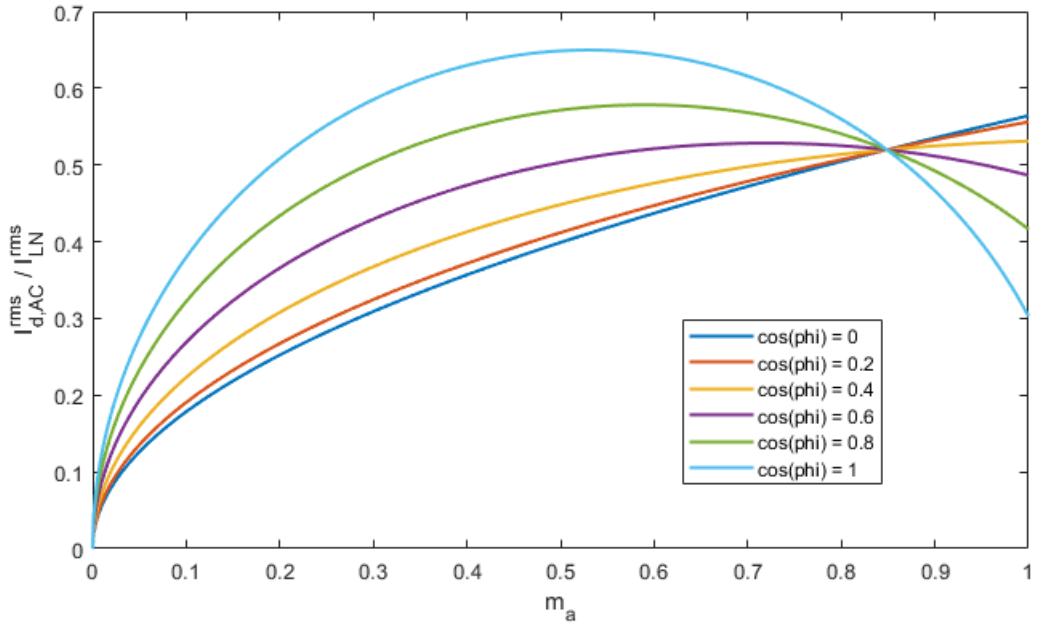


Figure 4.6. Variations of ripple component of the DC-link current with respect to m_a.

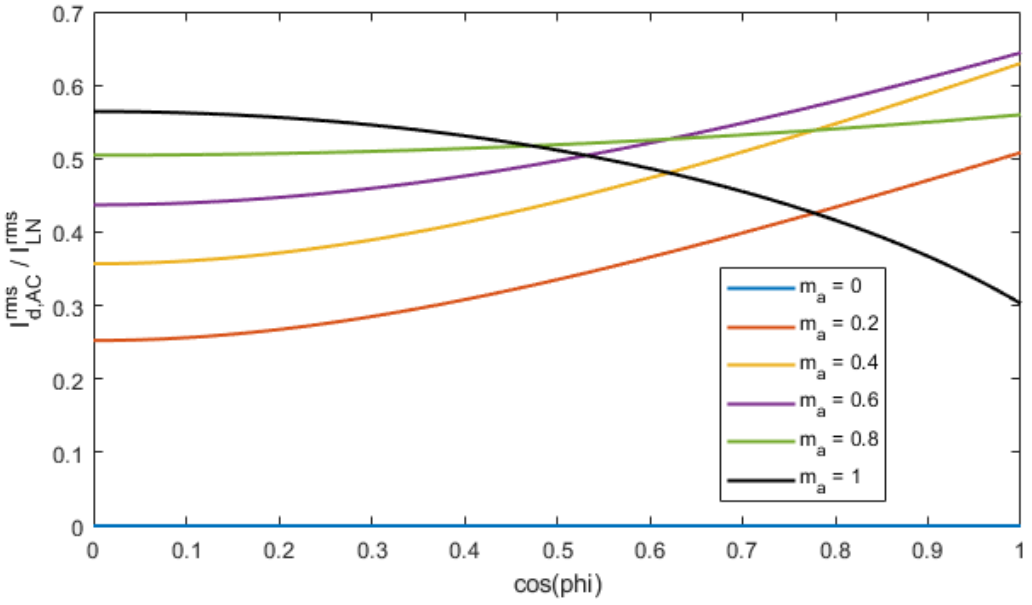


Figure 4.7. Variations of ripple component of the DC-link current with respect to $\cos(\phi)$.

From the analysis of Figure 4.6, the following conclusions can be derived:

- for a modulation index $m_a = {}^{8}/_{3\pi} \simeq 0.85$ the dependence between power factor $\cos(\phi)$ and rms value vanish;
- the maximum rms value of the ripple DC-link current of $I_{d,AC}^{rms} = 0.46 I_{LN}^{rms}$ is at $m_a = \simeq 0.53$ for $\cos(\phi) = 1$ (purely resistive load).

Other interesting considerations can be done taking into account Figure 4.7:

- until the value $\cos(\phi) = 0.43$ is reached, the maximum value of the rms ripple current is obtained with the highest modulation index $m_a = 1$;
- with more resistive load ($\cos(\phi)$ near to one), the rms value increases and this id due to the presence of larger harmonics at the load;
- with more inductive load ($\cos(\phi)$ close to zero), The rms value increases with the modulation index.

Putting together all the evaluations made in the previous statements, the theoretical worst case rms value and the theoretical worst case conditions for the ripple DC-link current is derived:

1. the worst case rms value is $I_{d,AC}^{rms} = 0.46 I_{LN}^{rms} = 0.46 \cdot 60\text{A} = 27.6\text{A}$;
2. the worst case modulation conditions are $\cos(\phi) = 1$ and $m_a \simeq 0.53$.

Theoretical results obtained from equation (4.9) approximate experimental result with a error lower than 8% for the full range of modulation [29]. A further analysis with the SIMULINK model of Chapter 3.1 can be helpful to further validate the above conclusions; the simulation outputs are reported in Figure 4.8 and Figure 4.9, from which the theoretical worst case conditions are widely proven also from the simulation.

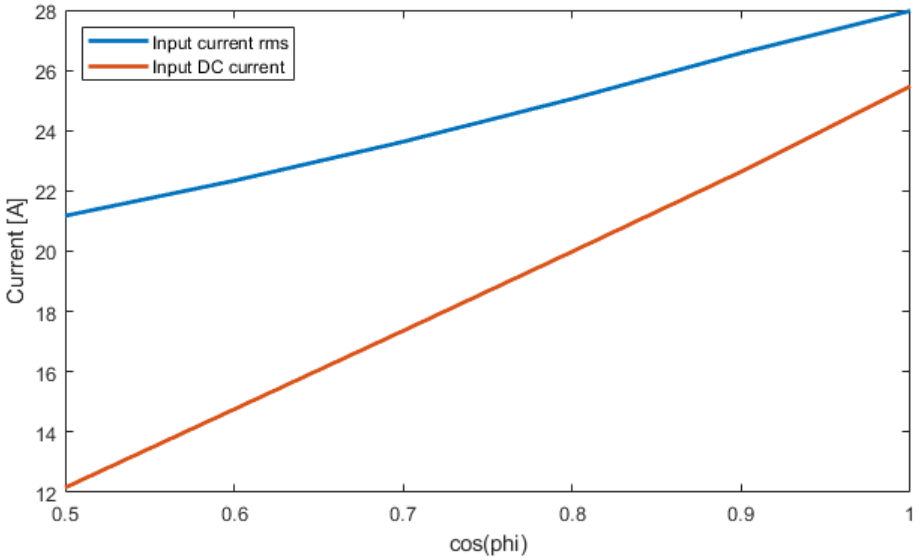


Figure 4.8. Simulation results of the SIMULINK model for different power factor $\cos(\phi)$.

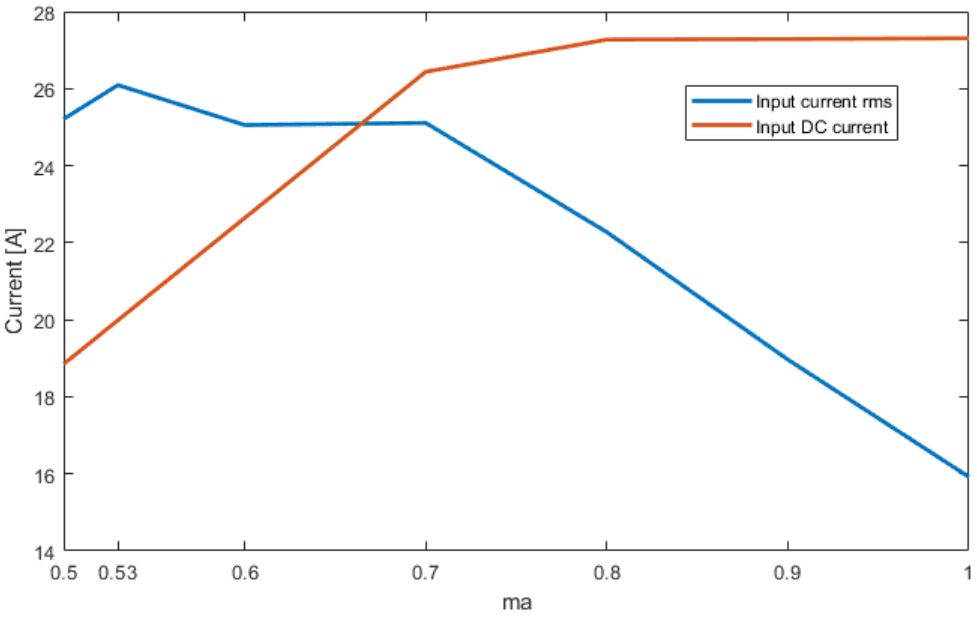


Figure 4.9. Simulation results of the SIMULINK model for different modulation index m_a.

One important step for the choice of a suitable DC-link capacitor is an evaluation of the harmonic content and harmonic characteristics of the DC-link current. This analysis is performed exploiting the MATLAB algorithm for the Fast Fourier Transform which is dependent on the time resolution of the simulation and on the periodicity of the overall waveform [23]. The discrete Fourier Transform code returns a double-sided spectrum, thus the code used in this Thesis, listed in Appendix A.3, shows how to carry out a single-sided spectrum from a double-sided one.

The DC-link current of the three-phase Voltage Source Inverter is stored into the workspace during the simulation thanks to the SIMULINK *to workspace* block, visible Figure B.13 with the name IDC. It is evaluated with the parameter values show in Table 4.1, that means taking into account the project specifications (Table 3.1) under worst-case conditions.

Max. DC bus voltage V_d	700V
Max. Output Power P_out	20kW
Max. DC current I_d	29A
Max. Switching Frequency	20kHz
Output Frequency f_{out}	50Hz
Power Factor $\cos(\phi)$	1
Max Phase Current	60A
Modulation index m_a	0.53

Table 4.1. Parameter values for the evaluation of the DC-link current spectrum.

In Figure 4.10 the total DC-link current is reported while the spectrum of the ripple current is showed in Figure 4.11.

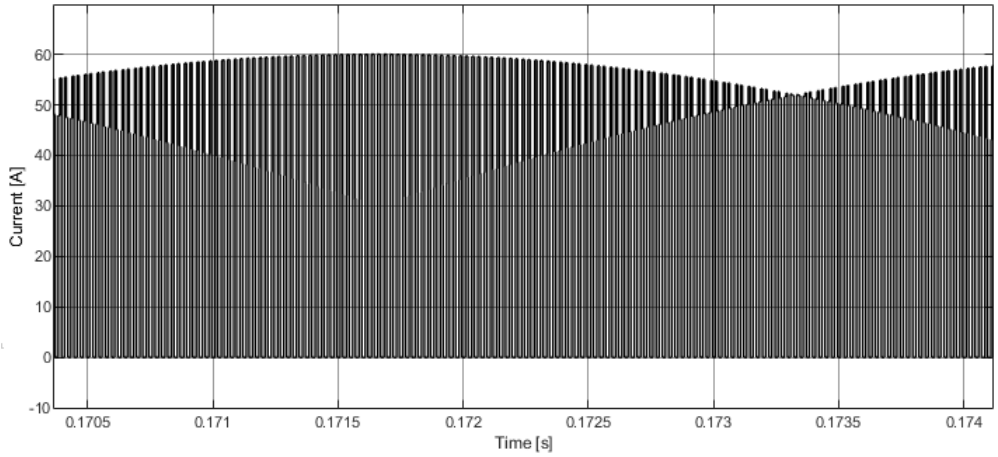


Figure 4.10. DC-link current waveform of the three-phase VSI under RMS worst-case conditions.

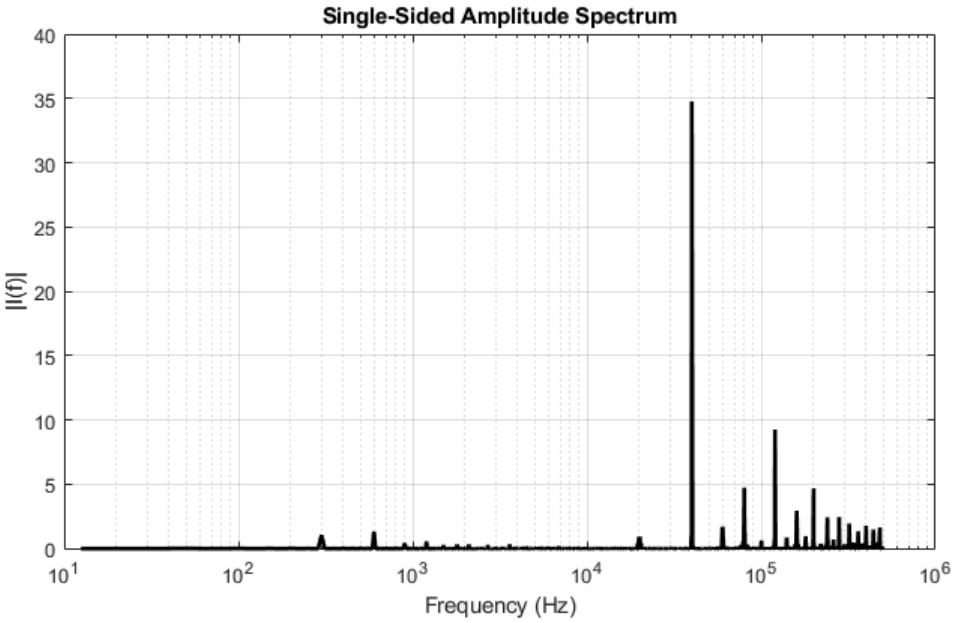


Figure 4.11. Spectrum of the three-phase VSI DC-link current under RMS worst-case conditions.

From Figure 4.11, one of the benefits of the Space-Vector technique is visible: the first harmonic component of the output and of the carrier are suppressed because harmonic energy of the DC-link current are translated to higher frequency. Furthermore, a significant part of this energy is located around the sideband of second switching frequency harmonic. For the design purposes of this Thesis, the largest harmonic component has a frequency two times higher than the switching frequency and its peak amplitude is of 34.75A.

Most of the specifics for the DC-link capacitor has been derived, the last step is the minimum capacitance and minimum Equivalent Series Resistance (ESR) estimation and it is derived by imposing the maximum tolerable ripple of the DC-link voltage. Also in this case, the design is assisted by a MATLAB script (Appendix A.3): it derives the specifications for ESR and capacitance, and furthermore, by setting the variable $nCAP$ it derives the specifications for the combination of different capacitors when the use of only one is not suitable or advisable.

The steps performed by the script are:

1. simulation of the three-phase VSI;
2. DC-link current estimation with the specifics of Table 4.1;
3. evaluation of DC and AC component of this current at regime;
4. computation of the maximum ripple of AC component of the DC-link current;

5. capacitance and ESR estimation in function of the ripples.

The outputs of the code execution are reported in Figure 4.12, 4.13 and 4.14.

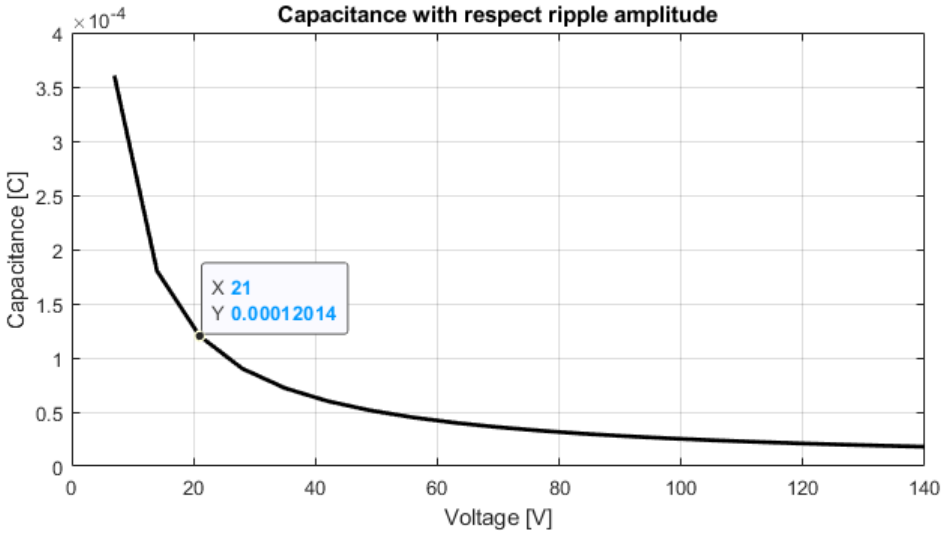


Figure 4.12. Capacitance value versus the DC-link voltage ripple.

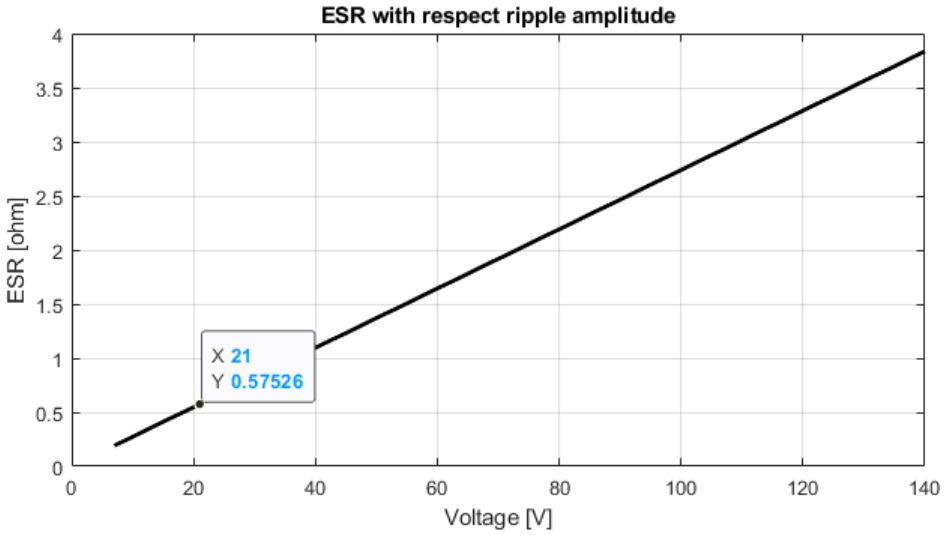


Figure 4.13. ESR value versus the DC-link voltage ripple.

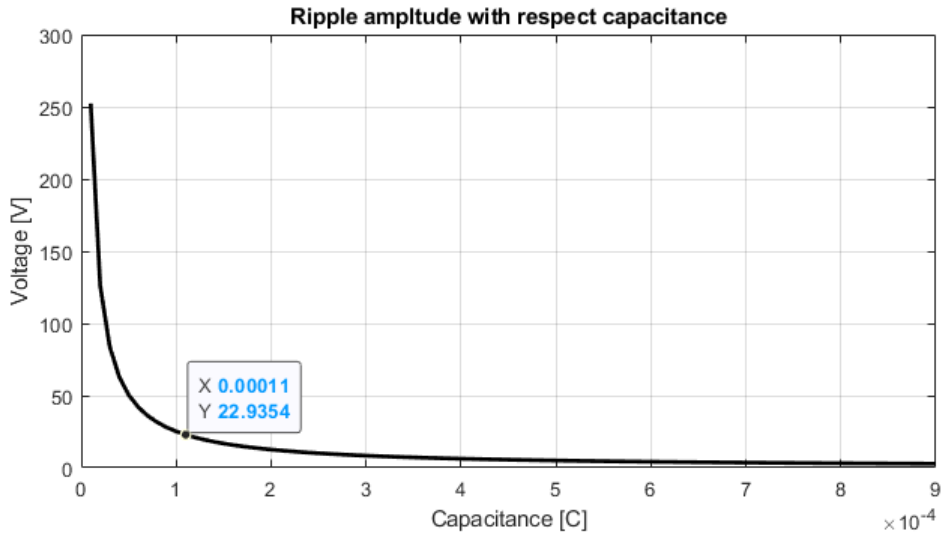


Figure 4.14. DC-link voltage versus the capacitance value.

The goal imposed for the capacitor selection is to obtain a DC-link voltage ripple of about 3%-4% of the DC-link voltage, that corresponds to a maximum ripple of 21V. As Figure 4.12 and 4.14 shows, the minimum capacitance must be of about 120µF and the maximum ESR should be of 580mΩ (Figure 4.13).

Since, at least for the moment, the option of custom-made capacitor must be not taken into account, the capacitor should be selected between the available ones in the market. A capacitor with high capacitance value suitable for high voltage application is heavy and expensive, hence a solution of four parallel DC-link capacitors is adopted and the specifications for each of them are listed in Table 4.2.

Min. Capacitance	30µF
Max. ESR	2.5Ω
Min. Operating Voltage	900V
Min. rms Current	10A

Table 4.2. Constraints for the selection of DC-link capacitors.

After a careful market analysis, the selected capacitor is a **EPCOS/TDK B32778G0406**. It is a film capacitor with a dielectric of polypropylene that allows to sink high rms DC-link currents with low self-heating, and it performs well over the temperature range and frequencies in power electronics applications; furthermore, it is a metallized capacitor, hence its electrode system is composed by a thin layer of vapour deposited aluminium, zinc or alloy blend (aluminium/zinc)

[12]. At the present, film technology is the best passive solution for these types of applications until ceramic capacitors will improve energy density and capacitance stability.

4.3 Overview of alternative harmonic filtering solutions

The main problems of a passive harmonic filtering solution, such as film capacitors, are [12]:

- weight;
- volume;
- lifetime.

The alternative solutions for the filtering problem are active systems or different modulation techniques.

Active solutions

As mentioned in Chapter 1, for heavy-duty applications, stand-alone (off-the-grid) converter are needed and this makes unsuitable the use of Active Power Filters (APF) [41]. Instead, a possible approach to decrease electro-magnetic interference (EMI) and radio-frequency interference (RFI) noises is the use of soft switching technique instead of hard switching one. Soft switching techniques consist of circuits called snubber cells, which allow switching devices to commutate at zero voltage (ZVS) or zero current (ZCS). An example of these type of techniques is the use of parallel resonant DC-link (PRDCL) in order to provide soft switching and PWM operation [44]. The PRDCL circuit is reported in Figure 4.15 and it is composed by a main switch S_1 with an auxiliary transistor T_2, an auxiliary diode D_2 and a resonant tank composed of a centre-tapped inductor L_r and a capacitor C_r. The working principle of the PRDCL soft switching inverter is fully described in [44], here only the advantages of this solution are reported: increased efficiency, very low current stresses on all the circuit components, zero crossing on the dc-link voltage with PWM capability and soft-switching operation of the inverter and so the current harmonics through the resonant tank are very limited and pushed to high frequency, meaning that a capacitor should filter them easier.

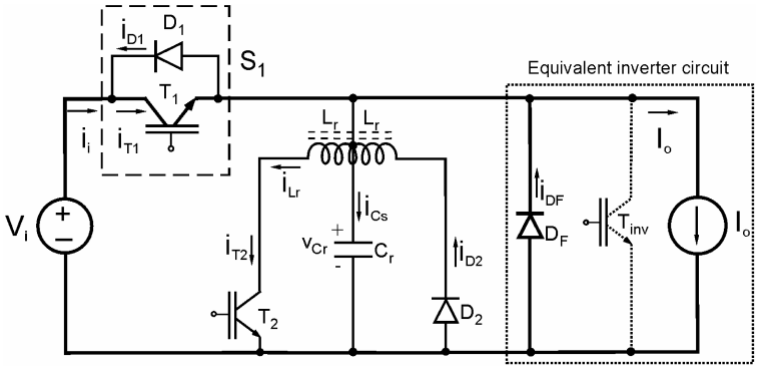


Figure 4.15. PRDCL soft switching inverter. [44]

The recognized drawback of the topology presented in Figure 4.15 is the voltage stress on the main switch S_1 and on the auxiliary transistor T_2: it is twice the voltage of the DC source and this can be a big issue in automotive or heavy-duty applications.

Another alternative circuit topology consists of a shunt-connected converter to provide a current compensation in order to reduce the current passing through the capacitor. The active filter implemented in [8] behaves as a current-fed converter connected in parallel to the DC-link capacitor which provide a current equal in magnitude and opposite in phase with the purpose to compensates the ripple component of DC-link current. This compensating current is constructed with a time-domain technique that easier to implement with respect a frequency-domain technique but it leads to an overall attenuation of harmonics rather than to an individual frequency component attenuation. The simulation results are reported in [8] but no informations about practical feasibility, power density or costs are reported [35]. From these results it is evident that this solution comports higher switching frequency for the active filter and, furthermore, the filter inductor should sink larger currents.

Modulation solutions

In Chapter 2 has been described as different modulation techniques leads to different characteristic of the output spectrum and as a consequence they modify also the DC-link current spectrum. Furthermore, it was described the degree of freedom of a Zero Space Vector Placement technique such as the Space-Vector PWM: the location and duration of the null vectors within one period T_{SW} can be arbitrary selected. The symmetric SV PWM technique adopted in this project allows obtaining a good trade-off between losses and output distortion; in this case, the goal is to combine the space vectors (Table 2.1) in order to reduce the rms value of the DC-link current or in order to push the spectrum at higher frequencies. The

Extended Double Carrier (EDC) PWM strategy, fully explained in [45], has the main feature of reducing the harmonic content of the DC-link current.

The pillar of Extended Double Carrier modulation technique is the utilization reduction of the zero vectors $\vec{v}_7$ and $\vec{v}_8$ in order to reduce the commutations of the DC-link current to zero by constructing the modulating vector from non-adjacent sequences of space vectors and the construction difference with respect the classic SV PWM is reported in Figure 4.16 while the difference in terms of DC-link current produced is showed in Figure 4.17.

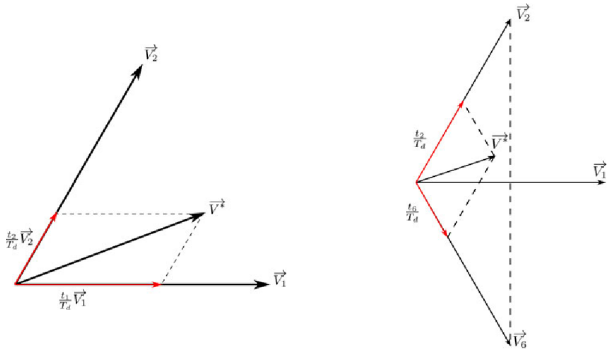


Figure 4.16. Modulating vector construction: on the left the classic SV PWM approach, on the right the EDC PWM approach. [45]

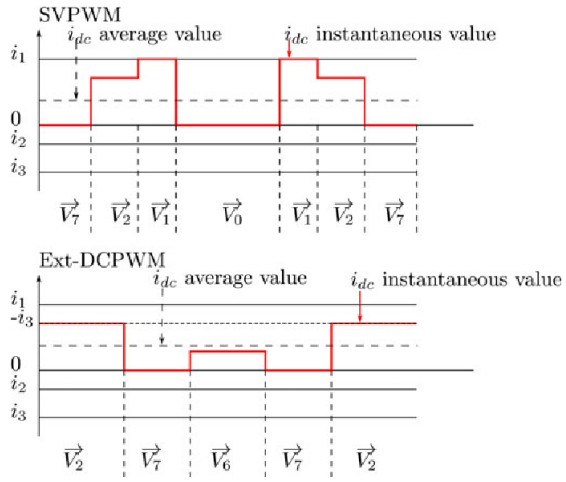


Figure 4.17. Variation of inverter input current during a switching period for SV PWM and EDC PWM. [45]

The modulation sequence of the Extended Double Carrier PWM technique varying with respect modulation index m_a and power factor $\cos(\phi)$, thus a closed-form

equation for the rms value of the DC-link current is difficult to derive; however, the authors of [45] show that EDC modulation provides a 40% reduction of the rms value with respect of SV PWM when the power factor is close to one (worst case condition in this project assumptions). The drawback of this modulation technique lies in an increment of the THD factor (2.6).

Chapter 5

Design of the inverter

In this Chapter all the design aspects of the three-phase Voltage Source Inverter are described, furthermore a discussion and explanation about different decisions adopted is faced up. Taking into account the fact that the application field of this inverter is the heavy-duty sector, the only two energy sources available for the system are a high-voltage battery pack and a low-voltage battery, for instance the car one. This mean that efficient power supplies are needed in order to drive the switching devices with the adequate voltage levels. Moreover, the safety aspect must be considered and so all the components have to guarantee the right insulation level between high-voltage and low-voltage world in order to obtain a safety system for the final user.

Since this is the starting point of a long-term project, only new and performant devices will be used for the design in order to have the certainty to not implement a system with electronic components obsolete within a few months.

5.1 Selection of the electronics components

Until this point two electric components have been selected, the switching devices in Chapter 3 and the DC-link capacitor in Chapter 4; they are, respectively, a SiC module from Cree/Wolfspeed identified as CCS050M12CM2 and the EPCOS/TDK metallized polypropylene film capacitor B32778G0406.

Gate driver

Feeding the power MOSFET module with the right value of voltage is crucial to obtain the best performance, hence a gate driving circuit is needed for:

- minimize turn-on and turn-off time, that means reduce the working time in active region where power dissipation is large;
- interface between the control circuit and the power switches,

- supply the right amount of current in order to charge the gate capacitance;
- provide electrical isolation; with the voltage rating of this project reinforced isolation is needed [28];
- protect the gate from under voltages and over voltages.

The selected gate driver is the **Texas Instruments ISO5452-Q1**, a reinforced isolated AEC-Q100 qualified gate driver with split outputs and active protection features. It has the high Common Mode Transient Immunity (CMTI, i.e. maximum tolerable rate of rise or fall of the common mode voltage applied between two isolated circuits) needed from fast switching devices such as GaN or SiC MOSFETs and its split outputs (Pin 4 and Pin 6 of Figure 5.1) provide a peak source current of 2.5A and a peak sink current of 5A; the higher sink capability allows to minimize the turn-off, usually the critical phase for power losses.

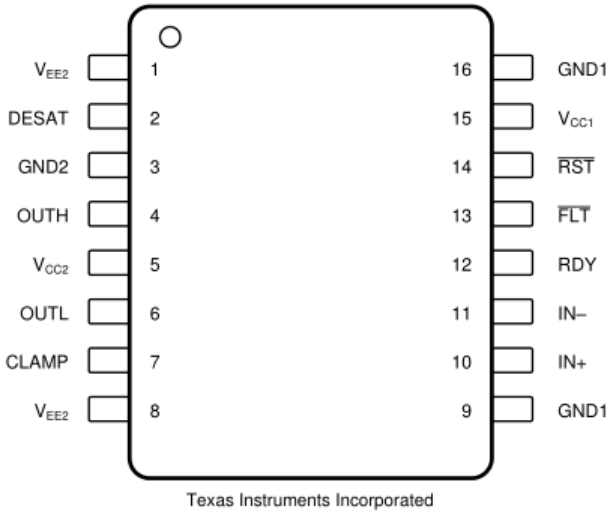


Figure 5.1. Pin configuration of the ISO5452-Q1.

Important active protection features are the desaturation and Miller clamp pins (respectively Pin 2 and Pin 7 in Figure 5.1): the desaturation fault detection recognizes when the transistor is in an over-current condition and starts a soft-turn-off procedure, while the Miller clamp feature prevents the transistor from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. Moreover, its reinforced isolation barrier is compliant with the standards provided in ISO61800-5-1 for variable speed drives. In order to properly drive the high side transistor, the driving circuit must be applied with reference to the source of the MOSFET and each source must have a separated and isolated ground.

Power supply

In order to obtain the best performances from a SiC MOSFET, gate voltage must be kept as high as possible, within the specified range, in order to operate the devices at a lower $r_{DS,on}$, so that the conduction losses can be minimized. Looking to the data-sheet of CCS050M12CM2, the gate-source voltage levels needed are:

$$v_{GS,on} = +20\text{V} \tag{5.1}$$

$$v_{GS,off} = -5\text{V} \tag{5.2}$$

The ISO5452-Q1 can handle voltages from -17.5V to $+35$V, but the right values for the v_{GS} must be derived from the low-voltage battery and, for this project, the car battery with nominal voltage of 12V is used as reference. The minimum value considered is of 9V while the maximum one is 24V. Thus, an isolated power supply must be employed.

Since the aim of the project is to obtain a high power density and high efficient system, the **Texas Instruments LM5180-Q1** is the best choice because it has an integrated 100-V power MOSFET and internal compensation. In fact, it is a primary-side regulated (PSR) flyback converter, hence the isolated output voltage is sampled from the primary-side flyback voltage, eliminating the need for an opto-coupler, voltage reference or third winding from the transformer for output voltage regulation. As the ending part of the component names states, the LM5180-Q1 is AEC-Q100-qualified and this increase its reliability.

In order to properly drive the six gate driving circuits, at least four different reference voltages must be supplied: one for the low-side driver and three for the high-side ones, because, as explained in Chapter 2, only the low-side switches are connected to the same potential and their control signals does not need to be isolated. There are many isolated DC-DC converters that could be used as power supply for the gate drive but, in this project, a flyback converter has been chosen because it allows to obtaining multiple output. The advantage is that only one converter is sufficient and this allows to further maximize the power density.

The LM5180-Q1 flyback controller works in three different modes depending on the load:

1. at high loads, it operates in Quasi-Resonant Boundary Conduction Mode (BCM) with the power MOSFET that turns on when the current in the secondary winding reaches zero to minimize switch-on losses; as the load is decreased, the peak current decreases and the frequency increases to maintain BCM operation;

2. at medium loads, the LM5180-Q1 operates in Discontinuous Conduction Mode (DCM), where it clamps the maximum switching frequency to 350kHz;

3. at light loads, the system operates in Frequency Fold-Back Mode (FFM), and the switching frequency decreases as the load current is reduced.

Another feature that makes the LM5180-Q1 a well suited choice is the wide input swing from 4.5V to 65V. In fact, automotive world is moving towards 48-volt electrical systems, with the 12-volt battery used just for traditional lighting and infotainment while the 48-volt battery supplies more power-hungry components such as power steering, power brakes, water pump, radiator cooling and the low-voltage part of the motor driver. If in a further step of the project the FLAG-MS company will decide to move towards a 48-volt solution, only few passive components will be changed in the design.

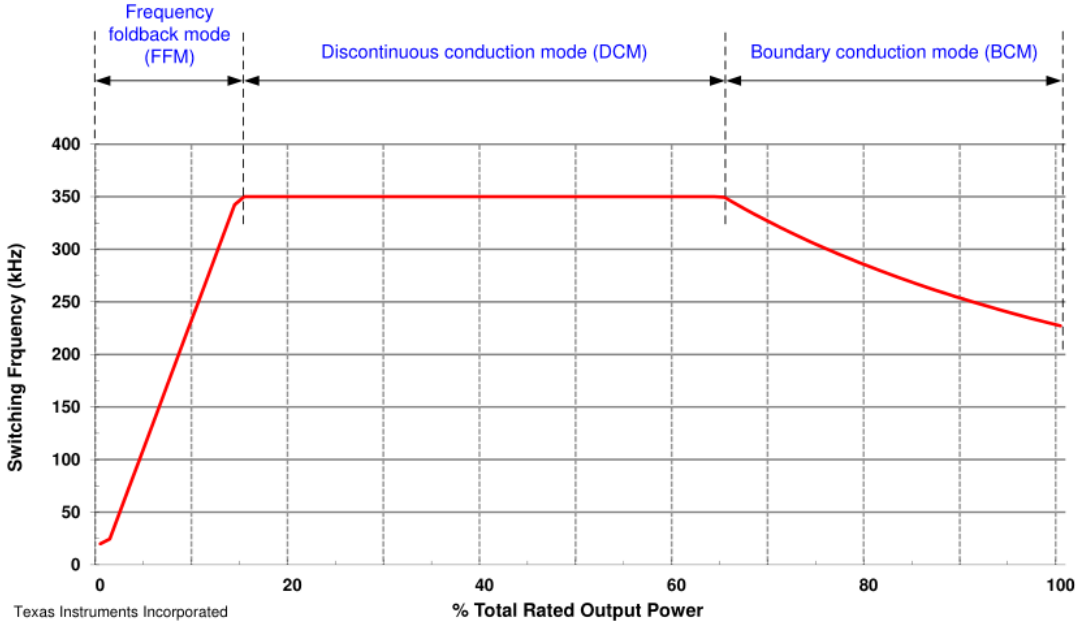


Figure 5.2. Modes of operation for the LM5180-Q1.

Current sense amplifier

Power inverters need high-resolution, accurate, isolated phase current sensing for control loop because it allows to keep under control the current supplied to the motor load and so its torque and angular velocity can be estimated and regulated. Furthermore, the real-time monitoring of the output current allows to prevent fault or over-current transient which could lead to electrical component breakdowns.

There are different options to measure the output current:

- shunt resistors;
- hall-effect sensors;
- flux-gate sensors;

- current transformers.

The reasons to choose the last three options are the high measurement range and the intrinsic galvanic isolation. the drawback consists in lower linearity and bandwidth combined with higher measurement drift with respect a shunt resistor; furthermore, they are more expensive. Taking into account these features, in this project the current sensing is made with a shunt resistor connected to a small reinforced isolated amplifier in order to eliminate the drawback of a resistor-based sensing.

Looking on the available modern products on the market, a precision isolated amplifier with a capacitive isolation barrier is selected: the **Texas Instruments AMC1302-Q1**. Its input are optimized for direct connection to shunt resistors and its low input voltage range of ±50mV allows to reduce the power dissipation through the shunt.

Peripheral circuits

The main electric components have been chosen, but other relevant inverter parts must be analysed because:

1. the low-voltage logic of ISO5452-Q1 circuits work with voltage level from 2.25V to 5.5V;

2. the swing of the low-voltage supply of the AMC1302-Q1 amplifier is from 3V to 5.5V;

3. the high-voltage supply of the AMC1302-Q1 must be in a range between 3V and 5.5V.

For the low-voltage sides, a level of 5V is selected because the system will be tested in a noisy environment and this voltage level allows a higher immunity. As for the flyback, the 5V must be generated by the low-voltage battery and, in order to guarantee a possible future 48 volt compatibility, the **Texas Instruments LM46002-Q1** is used. It is a synchronous buck converter capable of driving up to 2A of load current with an input voltage range of 3.5V to 60V. This converter is internally compensated fixed frequency peak current mode control, in order to ensure a higher integration level in order to achieve a better power density. The peak current command is adjusted with a voltage feedback loop and the converter runs with fixed switching frequency in Continuous Conduction Mode (CCM) but, in the case of lighter load, it can operates with Discontinuous Conduction Mode (DCM) and Pulse Frequency Modulation (PFM) mode to achieve high efficiency across all the load ranges [10].

The use of a power converter to step-up a voltage is the best choice from the point of view of efficiency and voltage stability but the price to pay is a higher space usage. The use of only one LM46002-Q1 allows to supply the low-voltage side of all the

six ISO5452-Q1 and of all the three current sensing circuit, thus the greater surface used is justified because huge amount of current are sink from all these circuit together. For what concerns the high-voltage side of AMC1302-Q1, the same buck converter can't be used because it is on the opposite side of the barrier; moreover, since the current need is low, a cheaper and smaller solution should be used. In a typical traction inverter application, the high-voltage side power supply for these amplifiers is derived from the floating power supply of the high-side gate driver and to minimize noises a low-cost low-dropout (LDO) regulator is used. A small device of this type, capable to handle an input voltage of +20V is the **Texas Instruments TPS7B6950-Q1** because, in a package with sizes of just 2.90mm×1.60mm, it is capable to integrate short-circuit and over-current protections. Also in this case a voltage of 5V is selected.

5.2 Sizing of the components

All the electric devices selected in the previous section need external components to work for proper, such as decoupling capacitors or feedback resistors. All the aspects concerning the dimensioning of these components are described in this section.

Gate driver

One of the advantages of adopted gate driving circuits is that the input control is in CMOS technology and, unlike an optocoupler, it can be directly driven by a microcontroller without external current drivers and biasing circuitry. So, the design requirements include decoupling capacitors on the input and output supplies, a pull-up resistor on the common drain $\overline{\text{FLT}}$ and RDY output signals (Figure 5.1), and a high-voltage protection diode between the MOSFET drain and the DESAT input.

Starting from the bypass capacitors, the recommended one at input supply V_{CC1} is of 0.1µF while at output supply it is of 1µF. The open drain outputs $\overline{\text{FLT}}$ and RDY are passive pulled-up with a 10kΩ resistor. The DESAT pin must be protected with a 1kΩ resistor because switching inductive loads, such as motors, generates large instantaneous forward voltage transient leading to large negative voltage spikes on the DESAT pin which draw significant current out of the device, hence a resistor is needed to limit this current. A further protection is achieved with a Schottky diode, that should be properly selected (Figure 5.3) in order to clamp the DESAT input to the potential of GND2 at low voltage levels.

During the short transition time when the transistor is switching a high voltage ramp rate occurs across it, leading in a current

$$I_{CHARGE} = C_{DST}\frac{dV_{DS}}{dt} \tag{5.3}$$

that charges the diode capacitance C_{DST}. In order to avoid false DESAT triggering a fast switching diode must be used, but its capacitance builds a voltage divider with the blanking capacitor C_{BLANK}.

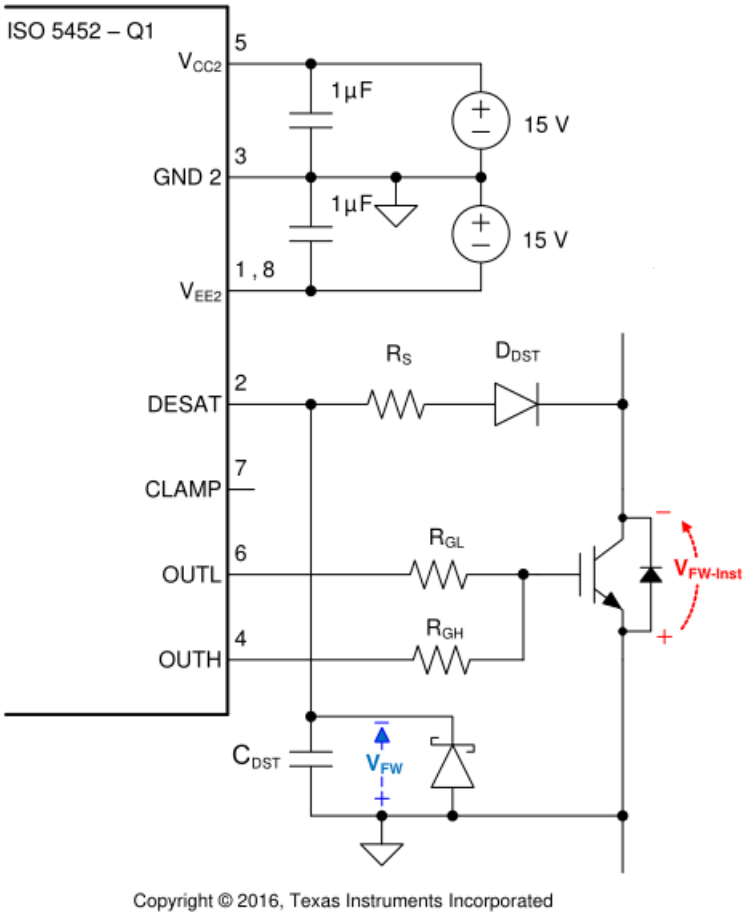


Figure 5.3. Protection of DESAT pin with a resistor R_S and a Schottky Diode.

Since that this capacitance is recommended of 220pF, a **BAT54W** Schottky Diode with a 30pF is used; hence, the collector voltage transients appear at DESAT attenuated by

$$1 + \frac{C_{BLANK}}{C_{DST}} \tag{5.4}$$

Since the voltage at the DESAT pin is the sum of the Schottky diode forward-voltage V_{FW} and of the MOSFET v_{DS}, the drain-source voltage level which triggers a fault condition ca be setted by implementing more than one diode D_{DST}:

$$V_{DS,fault} = 9V - n \cdot V_{FW} \tag{5.5}$$

where n is the number of DESAT diodes. From the data-sheet of the CCS050M12CM2, the typical output characteristics can be evaluated (Figure 5.4) and the desaturation voltage level is selected as 1.3V in order to obtain a maximum output current of 60A (Table 3.1). Thus, taking into account equation (5.5), a **SMBJ5341B** Zener diode with a voltage drop of 6.2V is added in series to the diode D_{DST}, that is one **STM STTH112-Y** with a maximum forward voltage of 1.6V.

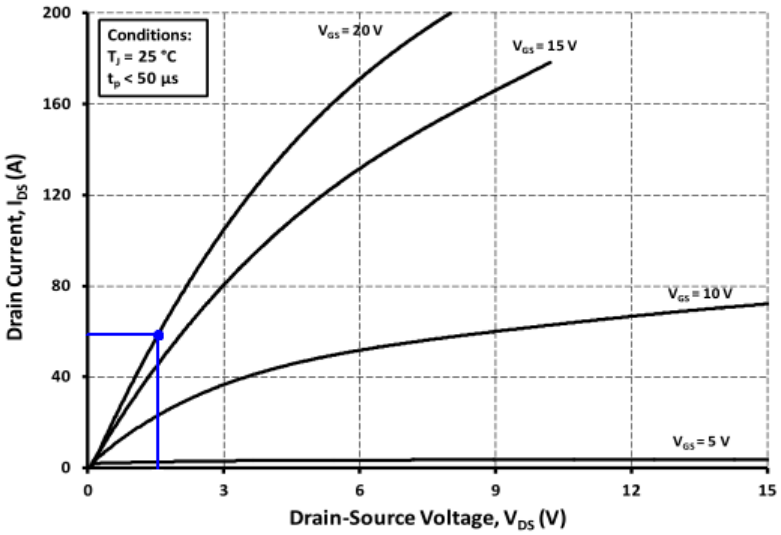


Figure 5.4. Typical output characteristics of the Cree/Wolfspeed CCS050M12CM2 for $T_J = 25°$.

The crucial part of the gate driver design is the right selection of the gate resistor R_G, and in the ISO5452-Q1 they are two (R_{GL} and R_{GH} in Figure 5.3) because of the split outputs. An optimum gate resistor selection is key for a high performance design because [4]:

- small resistor values will result in an overshoot in the gate driving voltage but also result in faster turn-on speed;
- high resistor values will overdamp the oscillation and extend the switching times without offering much benefit for the gate drive design.

Looking on the CCS050M12CM2 data-sheet, the recommended value for the gate resistor is of 20Ω and this means that the source and sink current of the gate driver must be of

$$I_{source} = \frac{v_{GS,on}}{R_G} = 1\text{A} \tag{5.6}$$

$$I_{sink} = \frac{v_{GS,off}}{R_G} = 0.25\text{A} \tag{5.7}$$

and they are inside the current range of the ISO5452-Q1.

At this point, the maximum available dynamic output power $P_{OD,max}$ can be estimated. The maximum allowed total power consumption P_D of each gate driver, reported on the data-sheet, is:

$$P_D = P_{ID} + P_{OD} + P_{OL} = 251\text{mW} \tag{5.8}$$

with

$$P_{ID} = V_{CC1,max} I_{CC1,max} = 5.5\text{V} \cdot 4.5\text{mA} = 24.75\text{mW} \tag{5.9}$$

$$\begin{aligned} P_{OD} &= (V_{CC2} - V_{EE2}) \cdot I_{CC1,max} \\ &= (v_{GS,on} - v_{GS,off}) \cdot I_{CC1,max} \\ &= 25\text{V} \cdot 6\text{mA} = 150\text{mW} \end{aligned} \tag{5.10}$$

hence, the maximum available dynamic output power is:

$$P_{OD,max} = P_D - P_{ID} - P_{OD} = 76.25\text{mW} \tag{5.11}$$

while, the actual dynamic output power under worst case condition is:

$$\begin{aligned} P_{OL,wc} &= 0.5 f_{SW} Q_G \cdot (v_{GS,on} - v_{GS,off}) \cdot \left(\frac{r_{on,max}}{r_{on,max} + R_G} + \frac{r_{off,max}}{r_{off,max} + R_G} \right) \\ &= 12.5\text{mW} \end{aligned} \tag{5.12}$$

where f_{SW} is the maximum switching frequency of Table 3.1, $r_{on,max} = 4\Omega$ is the worst case output resistance in the on-state, $r_{off,max} = 2.5\Omega$ is the worst case output resistance in the off-state.

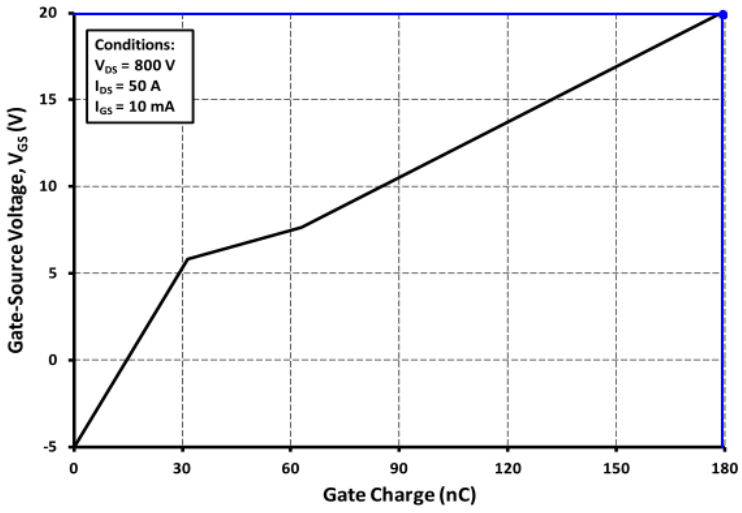


Figure 5.5. Typical gate charge characteristics of the Cree/Wolfspeed CCS050M12CM2.

The term Q_G is the power device gate charge, equal to 180nC, derived from the data-sheet gate charge curve (Figure 5.5): it represent the charge from the origin to the point on the curve at which the driving voltage v_{VGS} equals the desired gate voltage of the device; it is a key parameter to evaluate the time needed to reach the actual gate voltage.

Flyback power supply

The LM5180-Q1 requires only a few external components to convert from a 12-volt battery to more isolated output rails (Figure 5.6): a resistor R_{FB} connected between the SW and FB pins set the fixed output voltage, the input voltage turn-on and turn-off thresholds are established by R_{UV1} and R_{UV2} and a transformer is needed to generate the multiple output rails.

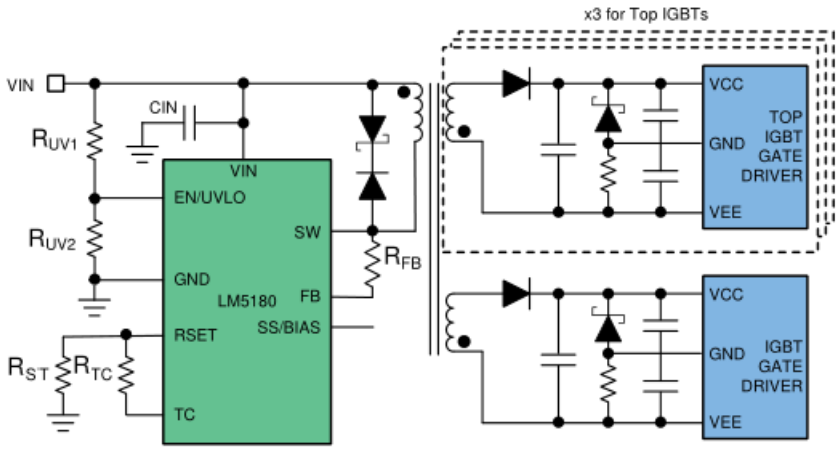


Figure 5.6. Schematic of the power supply circuit. [52]

The EN/UVLO input of the LM5180-Q1 device is enabled when the input rising voltage is higher than 1.5V with a hysteresis of 50mV (Figure 5.7). Imposing to turn-on the device when the rising input voltage reaches $V_{IN,ON} = 9V$ and to turn-off when the falling input voltage reaches $V_{IN,OFF} = 7.5V$, the resistance value can be computed:

$$R_{UV1} = \frac{V_{IN,ON} \cdot \frac{V_{UVLO2}}{V_{UVLO1}} - V_{INOFF}}{I_{UVLO}} = \frac{9\text{V} \cdot \frac{1.45\text{V}}{1.5\text{V}}}{5\mu\text{A}} = 260\text{k}\Omega \tag{5.13}$$

$$R_{UV2} = R_{UV1} \frac{V_{UVLO1}}{V_{IN,ON} - V_{UVLO1}} = 20\text{k}\Omega \tag{5.14}$$

The component that influences the most the next design steps is the transformer, because find it available on the market with four outputs winding, with the right

value of primary inductance and compliant with the required insulation standards has resulted to be difficult. Fortunately, **Wurth Elektronik** has on the catalogue the **750343953**, a custom-made transformer for Texas Instruments that can be ordered from anyone; its main characteristics are reported in Table 5.1.

Primary inductance L_{PRI}	47µH ± 10%
Primary DC resistance	0.08Ω
Saturation current	1.6A
Primary-to-secondary turn ratio N_{PS}	1

Table 5.1. Wurth Elektronik 750343953 characteristics.

The primary inductance of the transformer determines the modes of operation of the converter; taking into account that the LM5180-Q1 has a minimum off- time $T_{OFF,min}$ of 500ns, the magnetizing current should not decrease to zero in minor time periods, hence:

$$L_{PRI} \geq \frac{(V_{OUT} + V_F) \cdot T_{OFF,min} \cdot N_{PS}^2}{I_{SW,PK_{min}} \cdot N_{PS}} \simeq 46\mu H \tag{5.15}$$

where $V_{OUT} = 25V$ is the sum of the on-state and off-state gate voltages, V_F is the forward voltage of the output rail diode and $I_{SW,PK_{min}} = 0.27A$ is the minimum peak primary current of the LM5180-Q1. Thus, the primary inductance of the 750343953 is sufficient for this application.

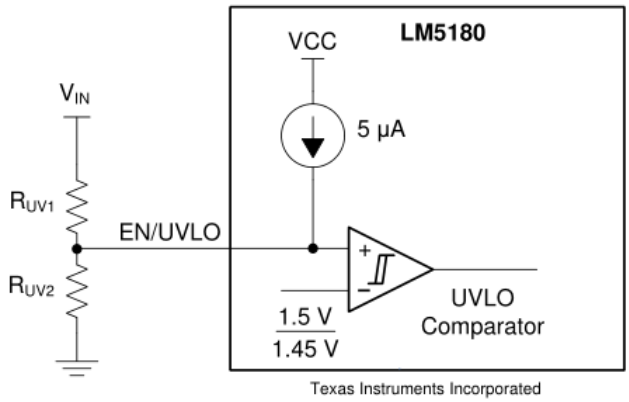


Figure 5.7. Programmable input voltage UVLO with hysteresis of the LM5180-Q1.

The duty cycle in BCM is given by:

$$D = \frac{(V_O + V_F) \cdot N_{PS}}{(V_O + V_F) \cdot N_{PS} + V_{IN}} = 0.68 \tag{5.16}$$

The maximum peak current on the integrated MOSFET allowed is 1.45A, while the actual value will be:

$$I_{SW,PK} = \frac{2 \cdot I_{OUT,tot} \cdot V_{OUT}}{V_{IN} \cdot D \cdot \eta} = \frac{2 \cdot 6 \cdot 0.025\text{A} \cdot 25\text{V}}{12\text{V} \cdot 0.68 \cdot 0.85} = 1.081\text{A} < 1.45\text{A} \tag{5.17}$$

where V_{IN} is the typical 12V-battery voltage, $\eta \simeq 85\%$ is the estimated efficiency for a flyback converter with multiple outputs and $I_{OUT,TOT}$ is the total output current.

The value of $I_{OUT,TOT}$ is selected considering the power to supply to each gate driver:

$$\begin{aligned} P_G &= V_{CC}\, Q_G\, f_{SW} + (Q_G \cdot f_{SW} \cdot \triangle V_G) + (C_{gs} \cdot f_{SW} \cdot \triangle V_G^2) \\ &= 250\text{mW} + (180\text{nC} \cdot 20\text{kHz} \cdot 25) + (8\text{nF} \cdot 20\text{kHz} \cdot 25^2) \\ &= 440\text{mW} \end{aligned} \tag{5.18}$$

where $\triangle V_G = 20\text{V} - (-5\text{V}) = 25\text{V}$ and $C_{gs} = 8\text{nF}$ is the MOSFET capacitance between gate and source evaluated from the data-sheet. Considering a safety margin value, the value of P_G selected is of 625mA, hence the output current provided to each gate driver is:

$$I_{OUT} = \frac{P_G}{\triangle V_G} = \frac{625\text{mA}}{20\text{V}} = 25\text{mA} \tag{5.19}$$

and the total output current $I_{OUT,TOT}$ will be six times the current of each gate driving circuit I_{OUT}.

The built-in MOSFET is rated at 100 V; in the off cycle, when the diode of the output rail is on, the actual voltage v_{DS} across it is:

$$V_{DS,max} = V_{IN,max} + V_{REF} + V_{ring} = 24\text{V} + 25.5\text{V} + 25\text{V} = 74.5\text{V} < 100\text{V} \tag{5.20}$$

where $V_{IN,max} = 24V$, $V_{ring} = 25V$ is the spike in voltage due to resonance and V_{REF} is the primary voltage reflected across the transformer:

$$V_{REF} = N_{PS} \cdot (V_{OUT} + V_F) \simeq 25.5\text{V} \tag{5.21}$$

When the integrated MOSFET is on, the voltage across the output rail diode must be taken into account:

$$V_{diode} = V_{OUT} + \frac{V_{IN,max}}{N_{PS}} + V_{D,spike} = 25\text{V} + 24\text{V} + 25\text{V} = 74\text{V} \tag{5.22}$$

The output voltage is determined by the ratio between R_{FB} and R_{ST}; hence, fixing $R_{ST} = 12.1\text{k}\Omega$:

$$R_{FB} = \frac{(V_{OUT} + V_F) \cdot N_{PS}}{0.1\text{mA}} = 257\text{k}\Omega \tag{5.23}$$

The LM5180-Q1 device has a thermal-compensation circuit in order to adjust the feedback with respect the thermal coefficient of the flyback diode. Selecting a **B2100A-13-F** as flyback diode:

$$R_{TC} = \frac{R_{FB}}{N_{PS}} \frac{3\text{mV}\,^\circ\text{C}^{-1}}{T_{C_{diode}}} = \frac{257\text{k}\Omega}{1} \frac{3\text{mV}\,^\circ\text{C}^{-1}}{1\text{mV}\,^\circ\text{C}^{-1}} = 771\text{k}\Omega \tag{5.24}$$

Important electric components for switching devices are the capacitors. In order to keep under control the input voltage ripple, the following relation must hold:

$$C_{IN} \geq \frac{I_{SW,PK} D \cdot \left(1 - \frac{D}{2}\right)^2}{2 f_{SW} \triangle V_{IN}} = \simeq 2\mu\text{F} \tag{5.25}$$

where the imposed $\triangle V_{IN}$ is the 5% of V_{IN}. Such as for the inverter, in order to select the input capacitor the rms current must be computed (Chapter 4):

$$I_{IN}^{rms} = \frac{D I_{SW,PK}}{2} \sqrt{\frac{4}{3D} - 1} \simeq 0.45\text{A} \tag{5.26}$$

For what concerns the output voltage ripple and to limit it to the 1% of the output voltage, the right output capacitance must be evaluated:

$$C_{OUT} \geq \frac{I_{OUT}}{\triangle V_{OUT}} \frac{L_{PRI} I_{SW,PK}}{V_{IN}} = \simeq 60\mu\text{F} \tag{5.27}$$

furthermore, the capacitor must be selected with a rms current higher than:

$$I_{OUT}^{rms} = I_{OUT} \sqrt{\frac{2 N_{PS} I_{SW,PK}}{3 I_{OUT}} - 1} \simeq 0.16\text{A} \tag{5.28}$$

The 25V generated at the four output rails must be split into a positive voltage of 20V and a negative one of -5V. This can be done in several ways but the one adopted in this project is to use only one winding and to divide the voltage with a Zener polarized by a resistor (Figure 5.6), because the use of two winding for each rail is unfeasible because of the usage of space, considering also the requirements of high-voltage insulation spacing. The less critical bias with respect the accuracy level is the negative voltage one because its role is only to prevent false switch turn-on during high-voltage transient. Since the positive bias is important to turn-on faster the SiC MOSFET, the Zener diode is used to set the 20V while the resistor with a voltage drop of 5V is used to polarize the diode; selecting a Zener with a knee-current of 50µA:

$$R = \frac{5\text{V}}{50\mu\text{A}} = 100\text{k}\Omega \tag{5.29}$$

Lower knee-currents mean higher resistance leading to lower power losses across it.

Current sense amplifier

The first component to choose is the shunt resistor to sense the output phase current; using the Ohm's law:

$$R_{SHUNT} = \frac{V_{SHUNT}}{I_{LN}} = \frac{50\text{mV}}{60\text{A}} \simeq 0.8\text{m}\Omega \tag{5.30}$$

and the power dissipated through it is:

$$P_{SHUNT} = \frac{V_{SHUNT}^2}{R_{SHUNT}} = 3.125\text{W} \tag{5.31}$$

Thus, the **Isabellenhutte BVS-M-R0007** is selected as shunt resistor. It has a resistance of 0.7mΩ with a maximum allowed power dissipation at 100° of 5W.

The recommended decoupling capacitors for both the high-voltage and low-voltage sides are:

- A 0.1µF capacitor placed as close as possible to the V_{DD} pins.
- An additional capacitor from 1µF to 10µF for filtering lower-frequency noise. In this project a 2.2µF capacitor is employed.

Furthermore, an input RC filter is recommended in order to minimize the noise.

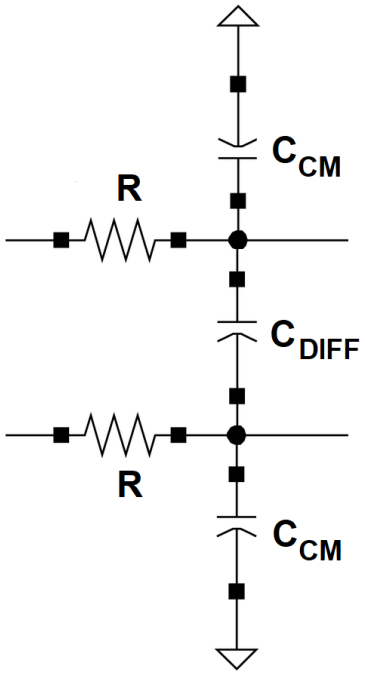


Figure 5.8. RC filter.

The cut-off frequency of this differential filter is:

$$f_c(\text{Hz}) = \frac{1}{2\pi\, 2\, R\, C_{DIFF}} \tag{5.32}$$

thus, selecting $R = 50\Omega$ and $C_{DIFF} = 0.1\mu\text{F}$, a differential cut-off frequency $f_C \simeq 30\text{kHz}$ is obtained. For what concerns the common-mode capacitance:

$$C_{CM} \simeq \frac{C_{DIFF}}{10} = 0.01\mu\text{F} \tag{5.33}$$

hence, $C_{CM} = 0.022\mu\text{F}$ is selected.
These passive components must be carefully chosen because their tolerance values change the Common Mode Rejection (CCM) of the filter according to the following relation:

$$CMR(\text{dB}) = 20\, log_{10}(\frac{R_{TOL}(\%) + C_{TOL}(\%)}{100}) + 20\, log_{10}(\frac{f}{f_C}) \tag{5.34}$$

12V-to-5V step-down converter

The switching frequency of LM46002-Q1 device can be setted by means of the resistor R_T (Figure 5.9); selecting a switching frequency f_{SW} of 500kHz:

$$R_T(\text{k}\Omega) = \frac{40200}{f_{SW}} - 0.6 = \frac{40200}{500\text{kHz}} = 83.2\text{k}\Omega \tag{5.35}$$

Once that the switching frequency is fixed, the buck converter inductance can be computed:

$$\frac{(V_{IN,max} - V_{OUT}) \cdot D}{0.4 \cdot f_{SW} \cdot I_{OUT}} \leq L_{min} \leq \frac{(V_{IN,max} - V_{OUT}) \cdot D}{0.2 \cdot f_{SW} \cdot I_{OUT}} \tag{5.36}$$

$$10\mu\text{H} \leq L_{min} \leq 20\mu\text{H} \tag{5.37}$$

where:

$$D = \frac{V_{OUT}}{V_{IN,max}} = \frac{5\text{V}}{24\text{V}} = 0.21 \tag{5.38}$$

$$I_{OUT} = 2\text{A} \tag{5.39}$$

A higher inductance value gives lower ripple current and so lower output voltage ripple with the same output capacitors; the drawback is the higher size of the inductor. With the purpose to minimize the ripples, an inductance value of $L = 18\mu\text{H}$ is adopted in this Thesis.

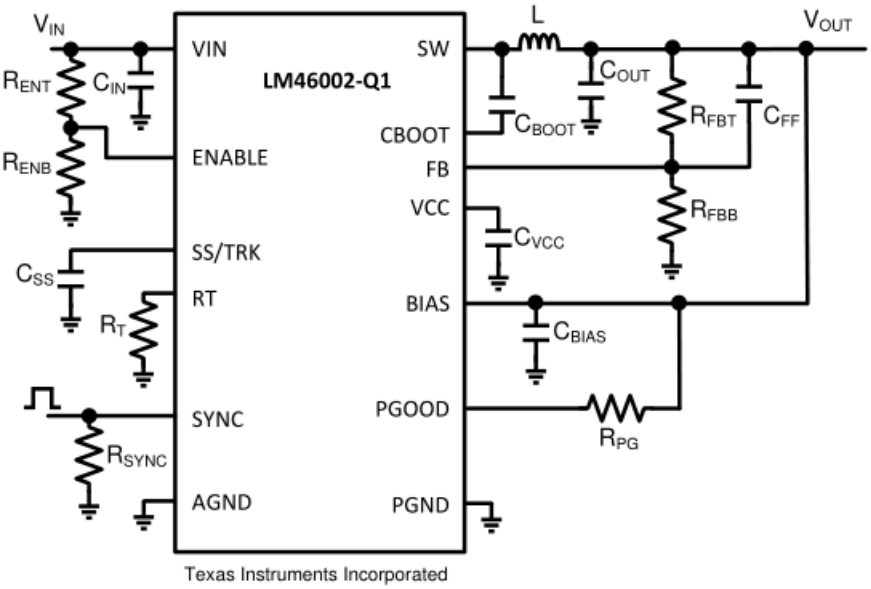


Figure 5.9. Schematic of the LM46002-Q1.

Another important parameter in the selection of the inductor is the rated saturation current:

$$I_{ripple} = \frac{(V_{IN} - V_{OUT}) \cdot D}{L \cdot f_{SW}} \simeq 500\text{mA} \tag{5.40}$$

$$I_{L,PK} = I_{OUT} + \frac{I_{ripple}}{2} = 2.25\text{A} \tag{5.41}$$

It is advised to select an inductor with a larger core saturation margin and preferably a softer roll off of the inductance value over load current. Thus, a well suited inductor for the application is the **Coilcraft MSS1278T-183ML**.

In order to choose the output capacitor, the output voltage ripple must be analysed and it is composed of two parts, one caused by the inductor current ripple through the ESR of the output capacitors and the other by the inductor current ripple charging and discharging the output capacitors:

$$\triangle V_{OUT,ESR} = \triangle I_L \, ESR \tag{5.42}$$

$$\triangle V_{OUT,ESR} = \frac{\triangle I_L}{8 \, f_{SW} \, C_{OUT}} \tag{5.43}$$

Thus, the minimum value for the output capacitance and the maximum value for the ESR are given by:

$$C_{OUT} \geq \frac{1}{f_{SW} \cdot r \cdot \triangle V_{OUT,ESR}/I_{OUT}} \left[\left(\frac{r^2}{12} \, D \right) + (1 - D) \cdot (1 + r) \right] \simeq 20\mu\text{F} \tag{5.44}$$

$$ESR \leq \frac{1 - D}{f_{SW} \, C_{OUT}} \left(\frac{1}{r} + 0.5 \right) \simeq 0.25\Omega \tag{5.45}$$

where:

$$r = \frac{\triangle I_L}{I_{OUT}} \tag{5.46}$$

Furthermore, looking on the data-sheet, the recommended output capacitance should be higher from the value obtained from equation (5.44) and smaller than 1mF, in order to limit potential potential output voltage overshoots as the input voltage falls below the device normal operating range. Thus, two capacitor of 22µF connected in parallel are adopted.

Another capacitor to select is the feed-forward one. The LM46002-Q1 is internally compensated but to improve the phase margin the capacitor C_{FF} is used, added in parallel with R_{FBT}(Figure 5.9):

$$C_{FF} = \frac{1}{2\pi f_x} \sqrt{\frac{1}{R_{FBT} \, (R_{FBT}/R_{FBB})}} = 100\text{pF} \tag{5.47}$$

where the recommended R_{FBB} is 250kΩ; R_{FBT} is chosen of 1MΩ to minimize losses and because

$$R_{FBB} = \frac{V_{FB}}{V_{OUT} - V_{FB}} R_{FBT} \tag{5.48}$$

Instead, the term f_x is equal to:

$$f_x = \frac{4.35}{V_{OUT} C_{OUT}} = 17.5\text{kHz} \tag{5.49}$$

Every LM46002-Q1 design requires a bootstrap capacitor and the recommended one is $C_{BOOT} = 0.47\mu F$ and it should be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability. Moreover, the VCC pin is the output of an internal LDO and to ensure its stability a capacitor of at least 2.2µF must be connected close to it. The input of this LDO is the BIAS pin and a ceramic capacitor of 4.7µF is connected close to it to work as input LDO capacitor.

The VIN pin requires high-frequency input high-quality ceramic capacitor with dielectric of type X5R or X7R, and the recommended value for the total capacitance is from 4.7µF to 10µF. Furthermore, a resistor of 10kΩ between this pin and the EN one must be placed, with the purpose to obtain the recommended rising threshold of 2.1V.

Since the input voltage can be higher than 12V, the PGOOD pin should be left floating. For what concerns the pin SS/TRK, if it is floating a soft-start time of 4.1ms is used; instead, in this project, it is loaded with a capacitance of 0.044µF because:

$$t_{SS} = \frac{C_{SS}}{I_{SS}} = \frac{0.044\mu F}{2.2\mu A} = 20ms \tag{5.50}$$

20V-to-5V LDO

The only two components to size for this small LDO are the input and output capacitors. The output capacitor should be ceramic with a capacitance value between 2.2mF and 100mF with a ESR value between 1mΩ and 2mΩ. The selected one is a ceramic capacitor of 3.3µF with a ESR of 1.3mΩ. For what concerns the input capacitor, a minimum value of 0.1µF must be implemented to better the transient performance; hence, a capacitor of 10µF is selected for this LDO.

The maximum power dissipation of this device is:

$$P_{LDO} = I_{OUT,max} \cdot (V_{IN} - V_{OUT}) = 0.150A \cdot (20V - 5V) = 2.25W \tag{5.51}$$

5.3 Estimation of the efficiency

Once that all design steps have been performed, a first overestimation (some aspects are neglected, such as the power dissipation due to the ESR of the capacitors) of the inverter efficiency can be done.

The power dissipated in one of the six transistors and in each diode of the module is reported in Table 3.5, thus:

$$P_{D,module} = 6 \cdot (51.4272W + 24.6259W) \simeq 456.4W \tag{5.52}$$

It can be noticed that the maximum power dissipated from MOSFETs only is:

$$P_{D,MOS} = 6 \cdot 51.4272W \simeq 309W \tag{5.53}$$

and it is the same of the one declared on the data-sheet, hence a further proof for the validity of the MATLAB/SIMULINK model is found.

The power dissipation due to the LM46002-Q1 buck converter, considering an achievable efficiency of the 90%, is:

$$P_{D,buck} = \frac{I_{OUT} \cdot V_{OUT}}{0.9} = \frac{2\text{A} \cdot 5\text{V}}{0.9} \simeq 11.2\text{W} \tag{5.54}$$

For what concerns the flyback converter, having already considered an achievable efficiency of the 85%:

$$P_{D,flyback} = \frac{I_{OUT,TOT} \cdot V_{OUT}}{0.85} = \frac{625\text{mW}}{0.85} \simeq 800\text{mW} \tag{5.55}$$

Instead, the current sense amplifier has a very low total power dissipation $P_{D,sense}$ of 98.45mW, but the power dissipated of 3.125W through the shunt is much higher and not negligible.

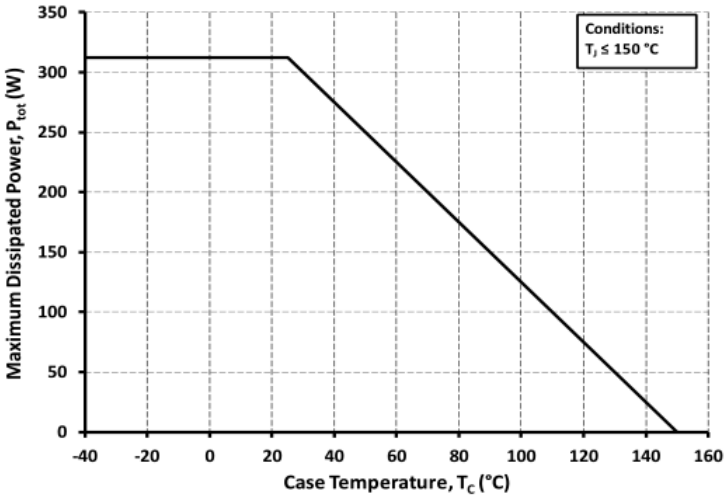


Figure 5.10. Maximum power dissipation for the MOSFETs of the Cree/Wolfspeed CCS050M12CM2 with respect case temperature.

Finally, the overestimated total power losses of the system are:

$$\begin{aligned}
\eta &= \frac{P_{OUT}}{P_{IN}} 100 = \frac{P_{IN} - P_{D,TOT}}{P_{IN}} 100 \\
&= \frac{P_{IN} - (P_{D,module} + P_{D,buck} + P_{D,flyback} + P_{LDO} + P_{SHUNT} + P_{D,sense})}{P_{IN}} 100 \\
&= \frac{20\text{kW} - (456.4\text{W} + 11.2\text{W} + 800\text{mW} + 2.25\text{W} + 3.125\text{W} + 98.45\text{mW})}{20\text{kW}} 100 \\
&\simeq 96\%
\end{aligned} \tag{5.56}$$

Chapter 6

Prototype

In this Chapter, the circuits designed as described in Chapter 5 are implemented in a prototype with the aim to validate the design steps, so the next step is to verify if these components can be implemented in the high-power system of this application. The best way to proceed in this primordial phase of the three-years project is step-by-step, which are:

1. verify the correct design of the flyback power supply;
2. verify the correct design of the gate driving and peripheral circuits;
3. verify the correct design of the current sensing circuit;
4. verify that the selected capacitor is able to filter the current harmonics;
5. verify that the selected SiC module is capable to handle the specifications of Table 3.1;
6. verify that the complete system is suitable to drive a motor load;
7. verify that the performances and efficiency are comparable with the ones estimate in Chapter 3 and 5.3.

The first four steps are the ones performed in this Thesis. In fact, before to test the SiC module, all the other electric circuits of the system must work as designed and it is better to test them separately in order to avoid generation of irreparable damages in the expensive CCS050M12CM2 device.

The prototype is composed of two different PCBs to be connect one to the other: one for the power circuits needed to supply the low-voltage ancillary circuits and one for the inverter including also the gate drivers, current sense amplifier and the peripheral circuits. All the aspects concerning the creation of this prototype are described in this Chapter and the environment used to develop the boards is the open source EDA (Electronic Design Automation) software called KiCad.

6.1 Design of the Printed Circuit Board

Since no motor loads are available in FLAG-MS company, considering also that there is no optimized cooling systems because the thermal design is not faced in this prototyping step, it is sufficient to implement only one leg of the inverter in order to test the validity of the electric design. Instead of the expensive CCS050M12CM2 SiC module, the transistors used to test the gate drivers are two **Cree C3M0120090J** already available in the company; they are two 900V SiC MOSFET with a maximum continuous drain current of 22A and a maximum pulsed current of 50A. Furthermore, in order to reduce the implementation costs of this prototype, the DC-link capacitor available in the warehouse and implemented in tested system is a **EPCOS/TDK Z905352661**, with an operating voltage of 630V and a capacitance of 50µF (1/3 of the capacitance selected for the complete three-phase system).

6.1.1 Electric schematic

The design of Chapter 5 must be changed to be compliant with the new specifics of the C3M0120090J. This SiC MOSFET needs recommended gate-source voltages of:

$$v_{GS,on} = +15\text{V} \tag{6.1}$$

$$v_{GS,off} = -4\text{V} \tag{6.2}$$

and the maximum positive voltage allowed is $v_{GS,MAX} = +18\text{V}$. Hence, the flyback converter must be redesigned in order to supply a maximum output voltage $V_{OUT} = 20\text{V}$ and each output rail should be split in a positive voltage of 15V and a negative one of -5V. The output voltage is dependent on the ratio between R_{FB} and R_{ST} and without varying $R_{ST} = 12.1\text{k}\Omega$:

$$R_{FB} = \frac{(V_{OUT} + V_F) \cdot N_{PS}}{0.1\text{mA}} = 210\text{k}\Omega \tag{6.3}$$

Also the thermal compensation must be recomputed:

$$R_{TC} = \frac{R_{FB}}{N_{PS}} \frac{3\text{mV}\,^\circ\text{C}^{-1}}{T_{C_{diode}}} = \frac{210\text{k}\Omega}{1} \frac{3\text{mV}\,^\circ\text{C}^{-1}}{1\text{mV}\,^\circ\text{C}^{-1}} = 665\text{k}\Omega \tag{6.4}$$

The other components are fully compliant with the specifics, a part from the output rail that must be redesigned to supply the required positive and negative voltage. Since this is a prototype, the output rails have been designed with the aim to try different possible configurations and, how it is visible in Appendix C.1, two diodes and their two polarization resistors are planned in the electric schematic. By testing the board the best configuration will be selected between the following ones:

1. the 15V Zener diode **SMBJ5352B** with its polarization resistor of 330Ω;
2. the 5V Zener diode **SMBJ5338B** with its polarization resistor of 1kΩ;
3. both the 15V and the 5V Zener diodes.

The polarization resistors are chosen in order to guarantee the right bias current to the diodes:

$$I_z = \frac{15\text{V}}{1\text{k}\Omega} = \frac{5\text{V}}{330\Omega} = 15\text{mA} \tag{6.5}$$

These Zener diodes are used because already available in the warehouse of the company; their drawback is the high knee-current that leads to higher power dissipation also through the resistor:

$$P_{R_1} = 1\text{k}\Omega \cdot 15\text{mA}^2 = 225\text{mW} \tag{6.6}$$

$$P_{R_2} = 330\Omega \cdot 15\text{mA}^2 = 75\text{mW} \tag{6.7}$$

$$P_{DIODE_1} = 5V \cdot 15\text{mA} = 75\text{mW} \tag{6.8}$$

$$P_{DIODE_2} = 15V \cdot 15\text{mA} = 225\text{mW} \tag{6.9}$$

Thus, the efficiency of this flyback will be lower than the one computed in Chapter 5, but the determination of the efficiency of the inverter is non a relevant aspect of this prototyping part.

Since two discrete SiC MOSFETs are adopted, they are implemented on the same board of the gate driving circuits, as reported in Appendix C.3, in order to reduce the parasitic inductances between the DC-link capacitors and the transistors. In fact, these components combined with the stray inductance present between the module and the capacitor create a resonant circuits, and the consequence is a voltage overshoot when one MOSFET is turned on, while the other MOSFET is carrying freewheeling current. Furthermore, also the distance between the gate drivers and the transistors must be minimized because another resonant circuit is present due to the MOSFET capacitances and the parasitic inductances. The gate resistors are crucial to reduce the Q-factor of this input resonator and so it design must be optimized. The recommended gate resistance value for the C3M0120090J is 2.5Ω but it is better to choose an higher value because the Q-factor is inversely proportional to it:

$$Q = \frac{\omega L_s}{R_G} \tag{6.10}$$

where L_S is the source inductance. Thus, selecting $R_{GH} = 8\Omega$, $R_{GL} = 5\Omega$ and taking into account the split output of the ISO5452-Q1:

$$I_{source} = \frac{v_{GS,on}}{R_G} = 1.875\text{A} \tag{6.11}$$

$$I_{sink} = \frac{v_{GS,off}}{R_G} = 1\text{A} \tag{6.12}$$

that can be easily supplied by the driving circuit. Since these resistors must be highly reliable and they have to dissipate high power, MELF (Metal Electrode Leadless Face) resistors are implemented because they are able to provide higher levels of performance in terms of long term stability, moisture resistance, reliability.

The gate of a MOSFET must be protected from possible overvoltages, so Schottky two diodes are used to clamp them and a resistor of 10Ω is added between gate and source in the eventuality that the gate driver breaks down. A resistance of 1MΩ is added also in parallel to the DC-link capacitor, in order to discharge it with a long time constant if a fault occurs in the inverter circuit.

All the circuit schematics are reported in Appendix C while the Bill of Materials (BOM) are reported in Table 6.1 and 6.2. Each BOM shows also the part number of the components and, where it is not present, it means that the device is already in the warehouse of the company.

Designator	Designation	Ref
C1,C2,C4,C6,C7,C17,C18	4.7uF	963-HMJ325KC7475KMHP
C12,C13,C14,C15,C23,C24,C25,C26	0.1uF	80-C0805C104K1REAUTO
C3	10uF	661-EMVA500ADA100ME5
C5,C16	220pF	810-CGA2B2C0G2A221J0
C8,C10,C19,C21	10uF	810-CGA6P1X7R1N106K2
C9,C11,C20,C22	22uF	810-CGA6P3X7R1E226M2
D2	SMBJ5373B-TP	
D6,D7,D10,D11	SMBJ18A-TR	
D9,D1,D3,D4,D5,D8	B2100-13-F	621-B2100-F
L1	22uH	
P1	12V	
P2	TOP A	
P3	TOP B	
P4	TOP C	
P5	BOTTOM	
R1	261k	
R10,R12,R13,R15	330	
R2	20k	
R3	665k	
R4	12.1k	
R5,R6	100	603-RC0805FR-13100RL
R8	210k	
R9,R11,R7,R14	1k	603-RC0805JR-131KL
T1	750343953	
U1	LM5180	595-LM5180QNGUTQ1
Z1,Z2,Z5,Z6	SMBJ5338B	
Z3,Z4,Z7,Z8	SMBJ5352B	

Table 6.1. BOM of the flyback board.

Designator	Designation	Ref
C1,C2	22uF	810-CGA6P3X7R1E226M2
C10	100pF	
C11,C12,C17,C33,C34,C43,C44	10uF	810-CGA6P1X7R1N106K2
C21	3.3uF	80-T494B335K020
C26	50uF	
C27,C28	220pF	80-C0805X221J5HAUTO
C29,C8,C15,C19,C23,C24,C30,C39,C40,C37,C38	0.1uF	80-C0805C104K1REAUTO
C3,C31,C32,C45,C46	1uF	963-UMF212B7105KGHT
C35	Cb LS	
C36	Cb HS	
C4,C5,C14,C16,C18,C20	0.022uF	80-C0805C223K5R
C41	Ca LS	
C42	Ca HS	
C6,C22,C25	2.2uF	810-C1608X5R1V225KE
C7	0.47uF	80-C0805C474K5RECTU
C9,C13	4.7uF	963-HMJ325KC7475KMHP
D1,D2	STTH112-Y	
D3,D4,D5,D6	B2100-13-F	621-B2100-F
D7,D8	BAT54W	621-BAT54W-F
H1	BOTTOM	
H2	TOP	
H3	PHASE A	
IC1	LM46002AQPWPRQ1	595-LM46002AQPWPRQ1
L1	MSS1260-183MLB	994-MSS1260-183MLB
P1	PWR1	
P2	PWR2	
P3	12V	
P4	CON 1X10	
Q1,Q2	C3M0120090J	
R1	82.5k	660-RK73H2ATTD8252F
R11,R13	8	594-MMB02070C8208FB2
R12,R14	5	594-MMB02070C5108FB2
R15,R16	1k	603-RC0805JR-131KL
R17,R18	10	660-RK73H2ATTD10R0F
R2	1M	660-RK73H2ATTD1004F
R3,R9,R10,R19,R20,R21,R22	10k	660-RK73H2ATTD1002F
R4	255k	660-RK73H2ATTD2553F
R5	BVS-M-R0007	660-PSJ2NTEBL500F
R6,R7	49.9	71-CRCW080549R9FKEAC
R8	1M	279-CRGCQ2512F1M0
U1	TPS7B6950-Q1	595-TPS7B6950QDBVRQ1
U2	AMC1302-Q1	595-AMC1302QDWVRQ1
U3,U4	ISO5452-Q1	595-ISO5452QDWRQ1
Z1,Z2	SMBJ5341B	

Table 6.2. BOM of the gate driver board.

6.1.2 Layout of the PCB

In order to allow a fast manufacturing and low costs, the layout is designed on a two-layer PCB with sizes lower than 10cm x 10cm. Furthermore, to ensure the compliance with the IEC-60664, the minimum creepage distances of 4mm must be respected (Figure 6.1).

Voltage r.m.s. [1]	Minimum creepage distances								
	Printed wiring material								
	Pollution degree								
	1	2	1	2			3		
	All material groups	All material groups, except IIIb	All material groups	Material group I	Material group II	Material group III	Material group I	Material group II	Material group III [2]
V	mm	mm	mm	mm	mm	mm	mm	mm	mm
10	0,025	0,040	0,080	0,400	0,400	0,400	1,000	1,000	1,000
12,5	0,025	0,040	0,090	0,420	0,420	0,420	1,050	1,050	1,050
16	0,025	0,040	0,100	0,450	0,450	0,450	1,100	1,100	1,100
20	0,025	0,040	0,110	0,480	0,480	0,480	1,200	1,200	1,200
25	0,025	0,040	0,125	0,500	0,500	0,500	1,250	1,250	1,250
32	0,025	0,040	0,14	0,53	0,53	0,53	1,30	1,30	1,30
40	0,025	0,040	0,16	0,56	0,80	1,10	1,40	1,60	1,80
50	0,025	0,040	0,18	0,60	0,85	1,20	1,50	1,70	1,90
63	0,040	0,063	0,20	0,63	0,90	1,25	1,60	1,80	2,00
80	0,063	0,100	0,22	0,67	0,95	1,30	1,70	1,90	2,10
100	0,100	0,160	0,25	0,71	1,00	1,40	1,80	2,00	2,20
125	0,160	0,250	0,28	0,75	1,05	1,50	1,90	2,10	2,40
160	0,250	0,400	0,32	0,80	1,10	1,60	2,00	2,20	2,50
200	0,400	0,630	0,42	1,00	1,40	2,00	2,50	2,80	3,20
250	0,560	1,000	0,56	1,25	1,80	2,50	3,20	3,60	4,00
320	0,75	1,60	0,75	1,60	2,20	3,20	4,00	4,50	5,00
400	1,0	2,0	1,0	2,0	2,8	4,0	5,0	5,6	6,3
500	1,3	2,5	1,3	2,5	3,6	5,0	6,3	7,1	8,0 (7,9) [4]
630	1,8	3,2	1,8	3,2	4,5	6,3	8,0 (7,9) [4]	9,0 (8,4) [4]	10,0 (9,0) [4]
800	2,4	4,0	2,4	4,0	5,6	8,0	10,0 (9,0) [4]	11,0 (9,6) [4]	12,5 (10,2) [4]
1 000	3,2	5,0	3,2	5,0	7,1	10,0	12,5 (10,2) [4]	14,0 (11,2) [4]	16,0 (12,8) [4]

Figure 6.1. Creepage distances to avoid failure due to tracking. [25]

Flyback board

In this section, the layout and the final PCB of the flyback board are reported. It measure 8.5cm x 7.5cm. The output connector with the label BOTTOM must supply the required voltages to the low-side gate driver; it is sufficient only one isolated output because the low-side transistors are all referred to the same potential and the transformers is designed to distribute in this rail three-times of the power of the other ones. The drawback of this transformer is that the creepage distances of 4mm are not respected between the secondary windings, this is the reason why three holes are provided in the PCB.

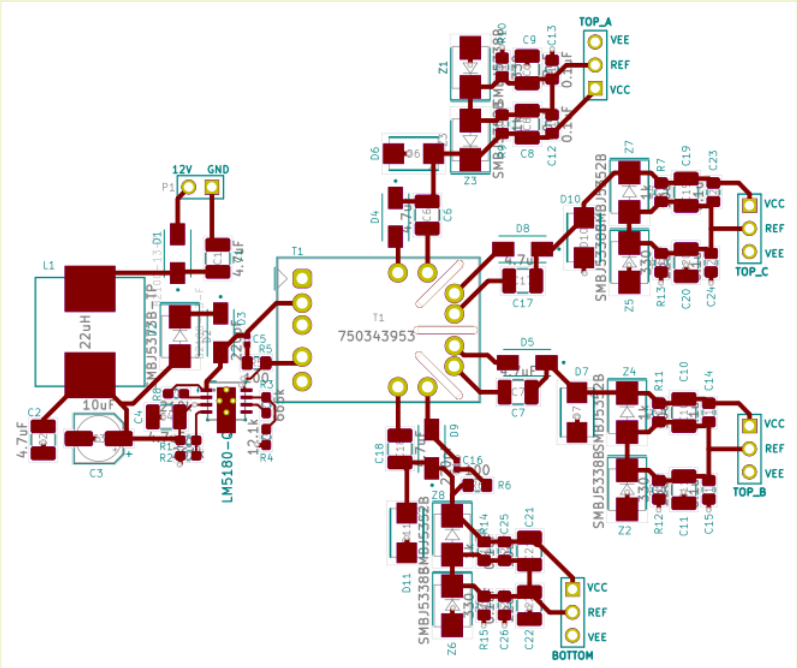


Figure 6.2. Layout of the top side of the flyback board.

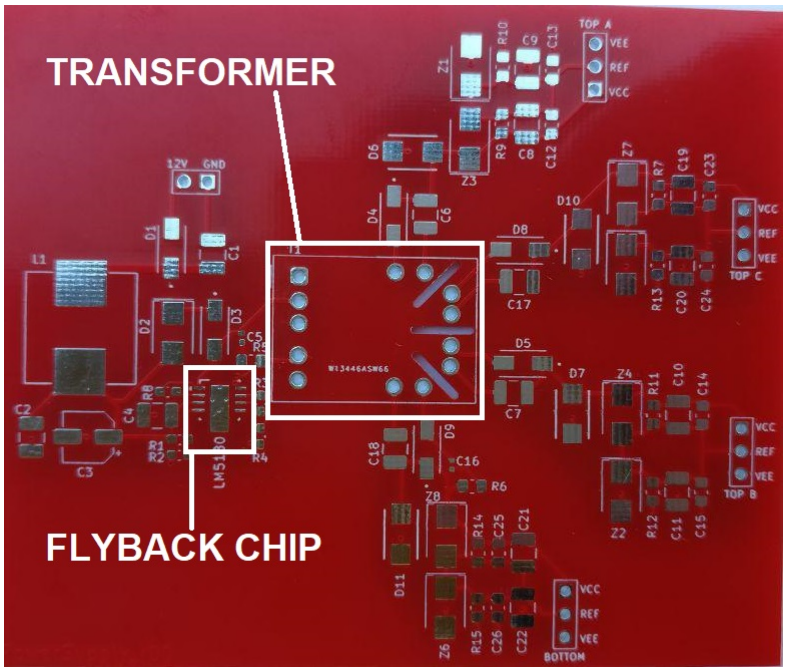


Figure 6.3. Top side of the flyback PCB.

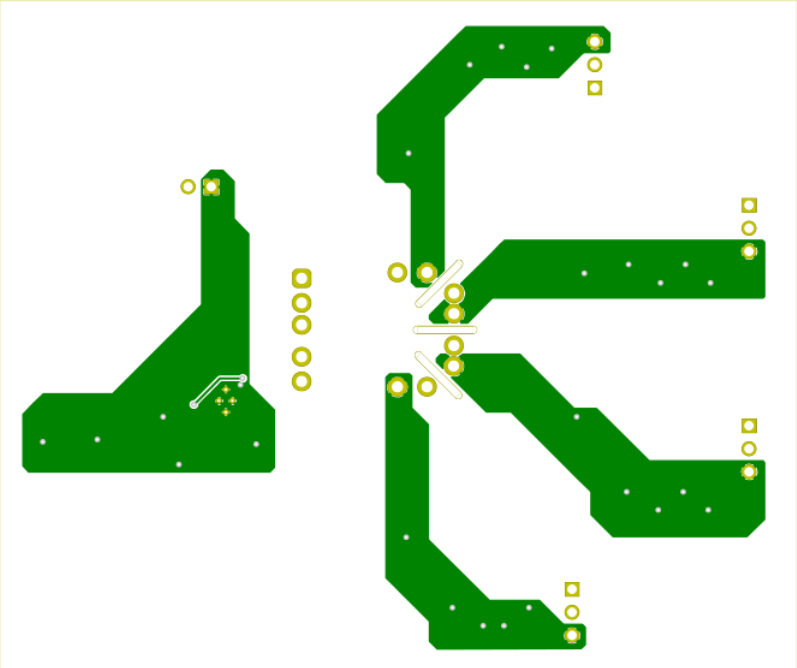


Figure 6.4. Layout of the bottom side of the flyback board.

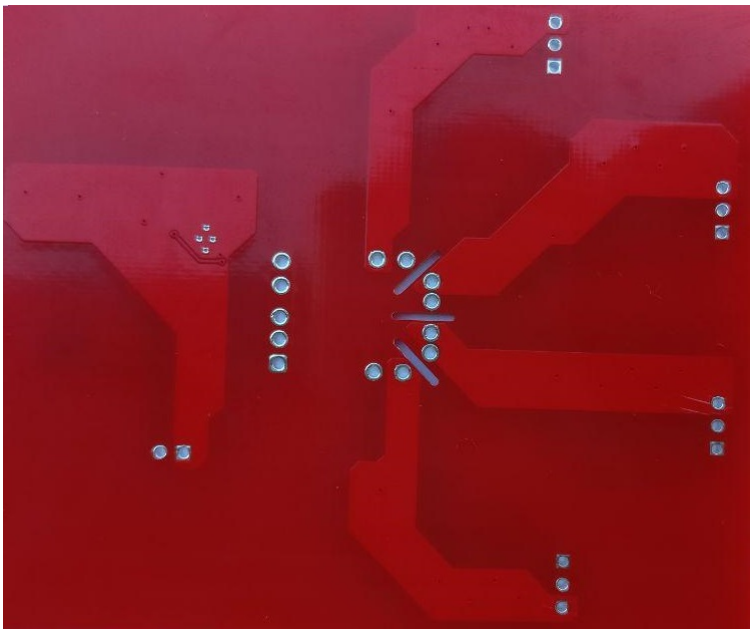


Figure 6.5. Bottom side of the flyback PCB.

Gate driving board

In this section, the layout and the final PCB of the gate driving board are reported. It measure 10cm x 7.5cm.

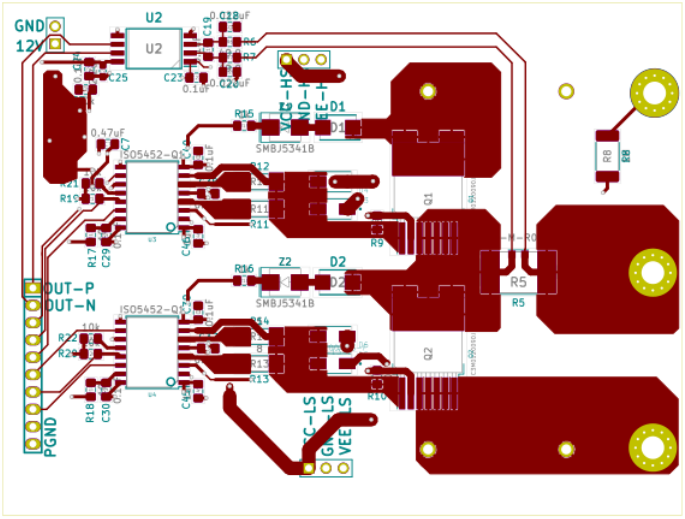


Figure 6.6. Layout of the top side of the gate driving board.

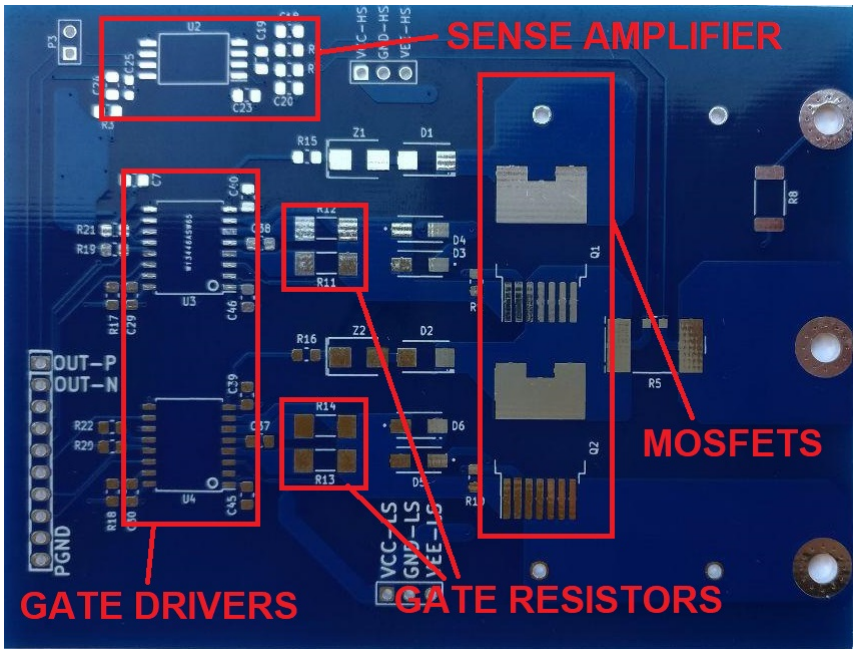


Figure 6.7. Top side of the gate driving PCB.

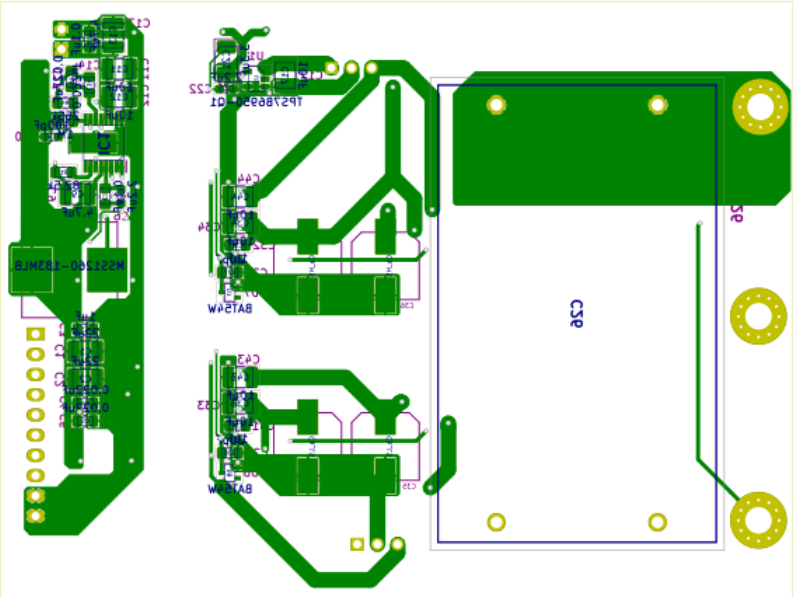


Figure 6.8. Layout of the bottom side of the gate driving board.

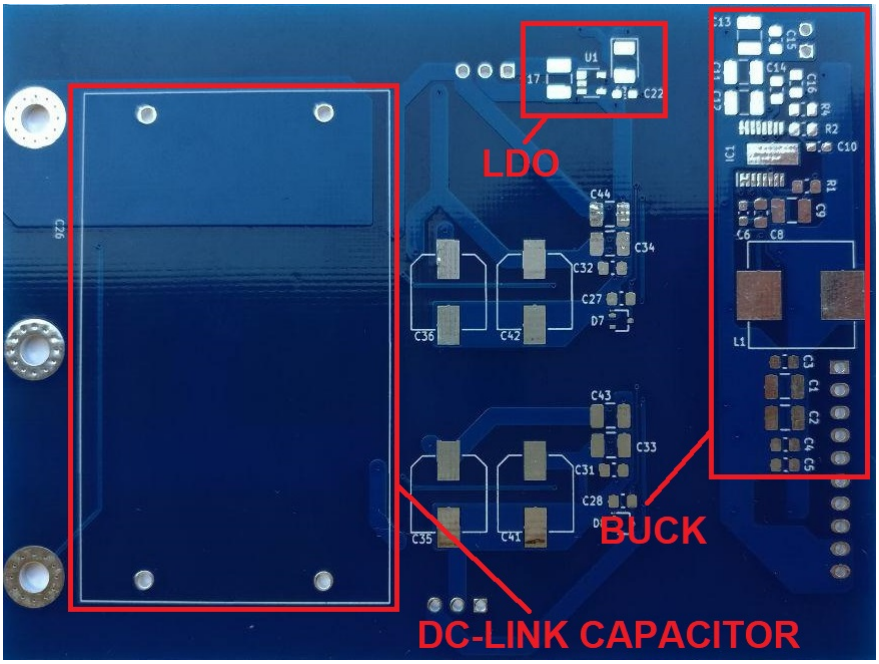


Figure 6.9. Bottom side of the gate driving PCB.

6.2 Experimental results

The instruments and tools of the FLAG-MS company used for the test are listed here:

EA-PSB 9750-60 3U Slave 15000W

Manufacter: Elektro-Automatil
Product Type: Bi-directional Power-Supply
Voltage Range: $0 \div 750$V
Current Range: $0 \div 60$A
Power Rating: 15 000W

Hercules TMS570LS12x Development Kit

Manufacter: Texas Instruments
Product Type: Embedded development hardware board
Main board elements: $TMS570LS1224$, $XDS110$ Class Debug Probe

Fluke 62 MAX+

Manufacter: Fluke
Product Type: Infrared thermometer
Temperature Range: $-30°C \div 500°C$
Spectral Response: $8\,\mu m \div 14\,\mu m$
Optical Resolution: 12 : 1

AC/DC Adapter

Input Voltage Range: $100 \div 240$V
Input Current: 1.6A
Input Frequency: $50 - 60$Hz
Output Voltage: 12V
Output Current: 5A

Fluke 1507

Manufacter: Fluke
Product Type: Isolation Resistance Tester
Measurement range: $0.01M\Omega \div 10G\Omega$
Test Voltage: 50V, 100V, 250V, 500V, 1000V

E3N

Manufacter: Chauvin Arnoux
Product Type: Hall-effect clamp
Rated current: 100A DC or peak
Output signal: DC and AC voltage
Output/input ratio: $100\frac{\text{mV}}{\text{mA}}$, $10\frac{\text{mV}}{\text{A}}$

SI-9002

Manufacter: TiePie
Product Type: Differential probe
Bandwidth: DC to 25MHz (3dB)
Attenuation ratio: 1/20 *or* 1/200

DP832

Manufacter: Rigol
Product Type: Programmable DC Power Sypply
Output: 30V/3A 30V/3A, 5V/3A
Total Power: up to 195W

Wavesurfer 3024

Manufacter: Teledyne LeCroy
Product Type: Oscilloscope
Bandwidth (at 50Hz): 50Hz
Input Impedance: 50Ω ± 2%, 1MΩ ± 2%; 16pF
Sample Rate (Single Shot): 2GS/s

Flyback board

The first board under test is the flyback one. The configuration chosen for the output rail is the one designed in Chapter 5.2: only one Zener diode for stabilizing the 15V, biased from its resistor of 330Ω. In order to verify the behaviour of flyback converter, it is connected to the DP832 and the outputs are loaded with two resistors: a 330Ω resistor is connected between VCC and REF and a 330Ω between VEE and REF, in such a way to obtain the total output power of $20V^2/660 = 610\text{mW}$, near to the maximum designed one of 625mW (Chapter 5). When the Rigol power supply is turned on, a delivered power of around 1.9W can be noticed: the reason is due to the high power dissipation of the output rails. Taking into account equations (6.9), the output rails sink 1.2W of the delivered power dropping the efficiency. Anyway, connecting the output pins to the oscilloscope and setting

the input voltage equal to the nominal one of 12V, Figure 6.10 shows that the output voltage between VCC and VEE is around 20.15V with a ripple of 356mV.

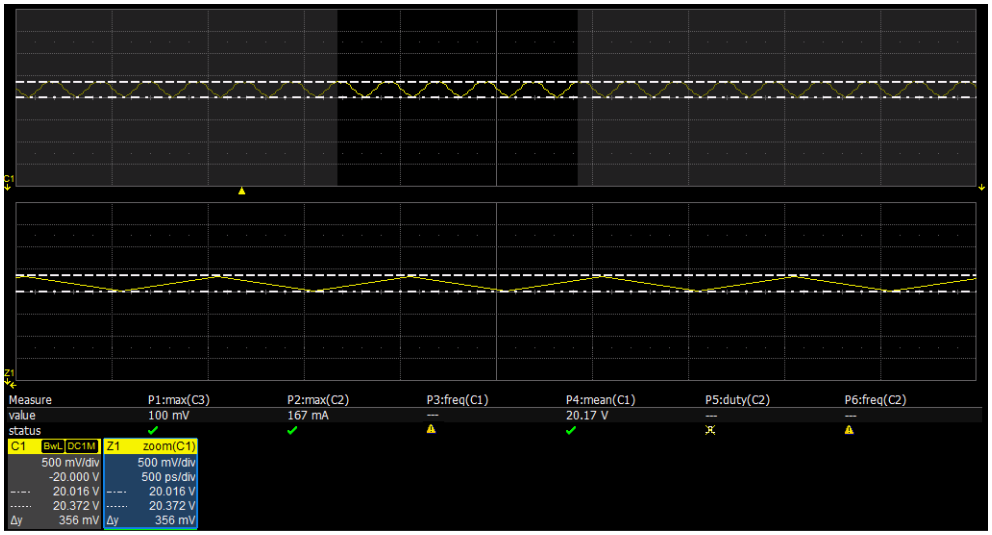


Figure 6.10. Output voltage of the flyback converter with a zoom of its ripple.

Then, the input voltage is sweep from the minimum one of 9V to the maximum one of 24V, and in Figure 6.11 and 6.12 it is visible the good stability and line regulation of the converter.

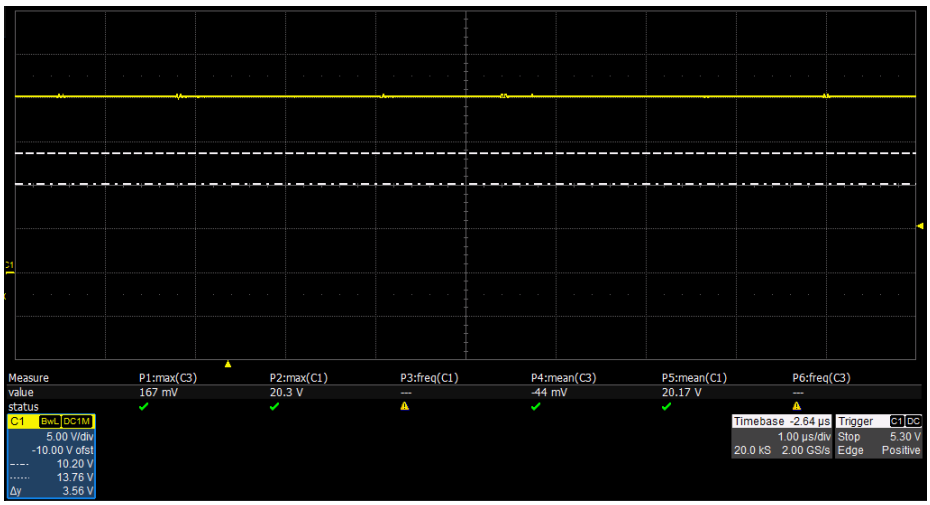


Figure 6.11. Output voltage of the flyback converter with an input voltage of 9V.

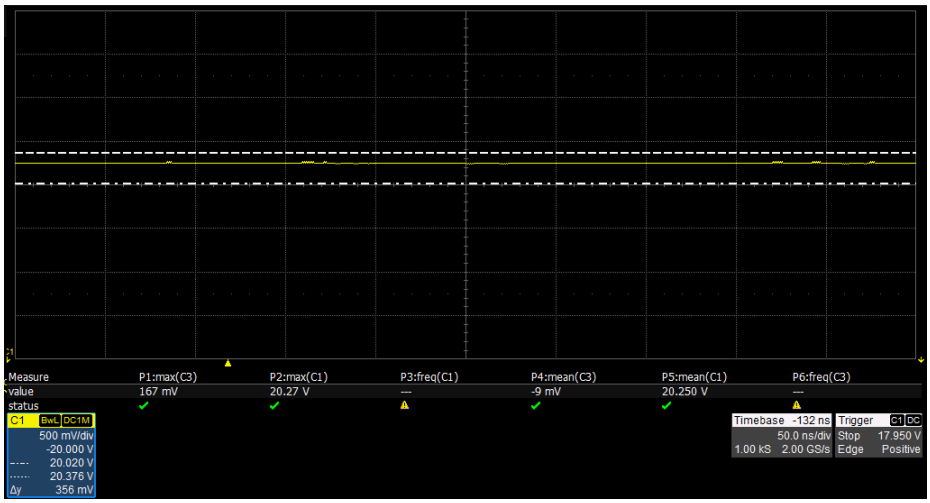


Figure 6.12. Output voltage of the flyback converter with an input voltage of 24V.

The converter is able to supply both 15V and -5V also when the load is changed with two resistors of 4.7kΩ and the power absorbed from the amplifier is reduced because this load sink less current and so less power must be delivered.

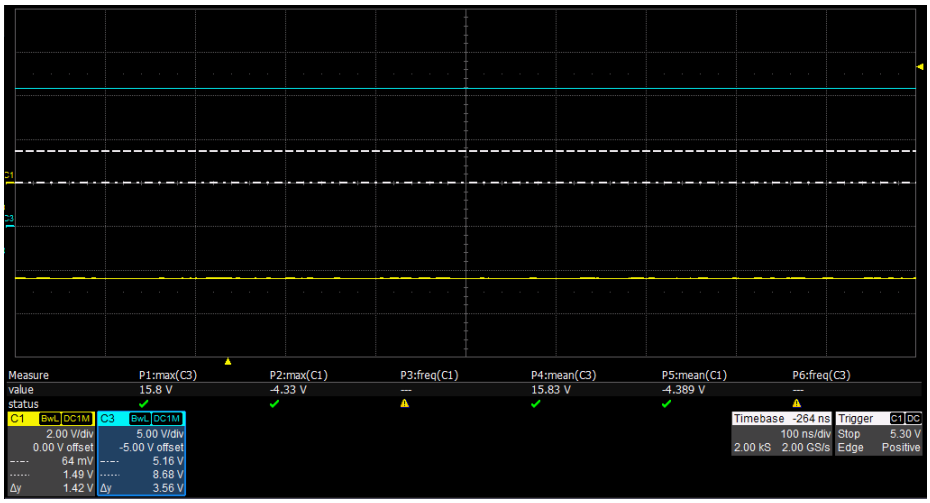


Figure 6.13. The 15V and -5V voltages supplied by the flyback.

As illustrated in Chapter 5, the LM5180-Q1 can operates in BCM, FFM or DCM and it is expected that:

- At full load with low input voltages it should works in BCM.
- At full load with high input voltages it should works in DCM.

Thus, connecting a probe to the pin SW of the device, the converter is supplied with the nominal voltage of 12V, the minimum voltage of 9V and the maximum one of 24V and it can be seen that with 9V and 12V it works in BCM while with 24V it works in DCM; Figure 6.15, 6.14 and 6.16 confirm the theory assumptions and validate the design.

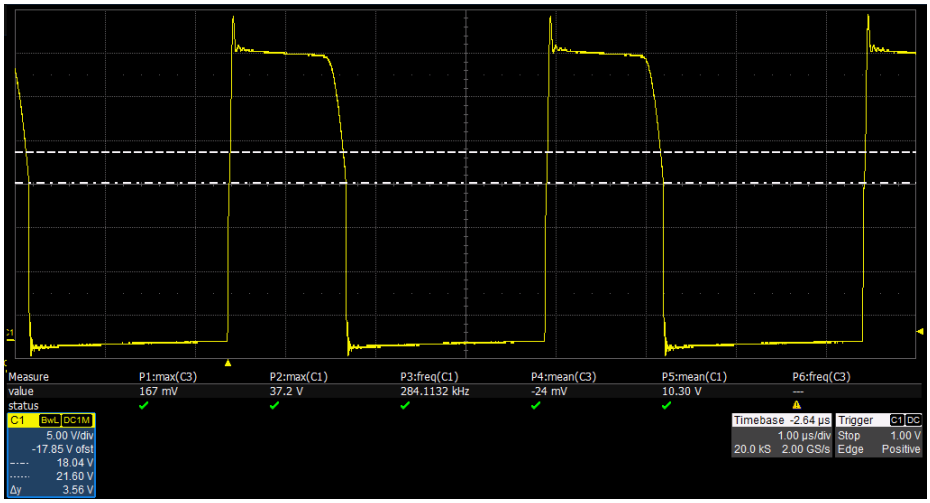


Figure 6.14. Pin SW with respect ground when the nominal voltage is applied.

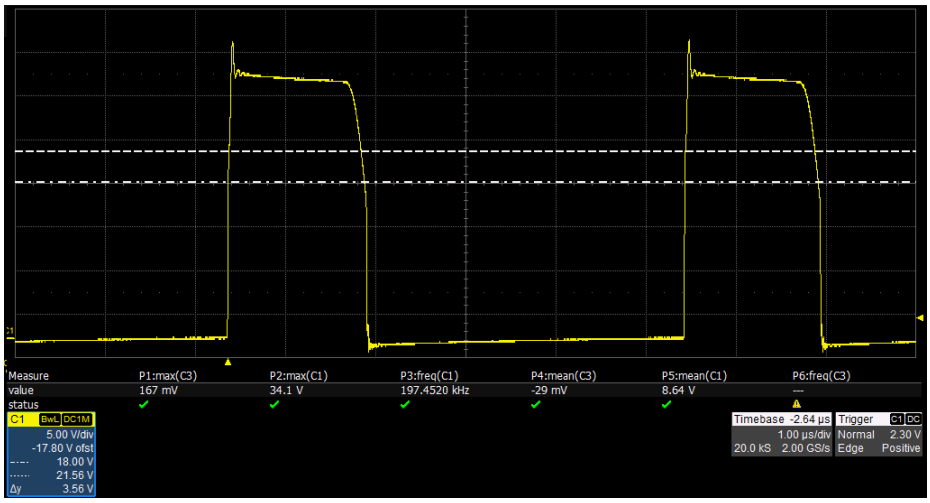


Figure 6.15. Pin SW with respect ground when the minimum voltage is applied.

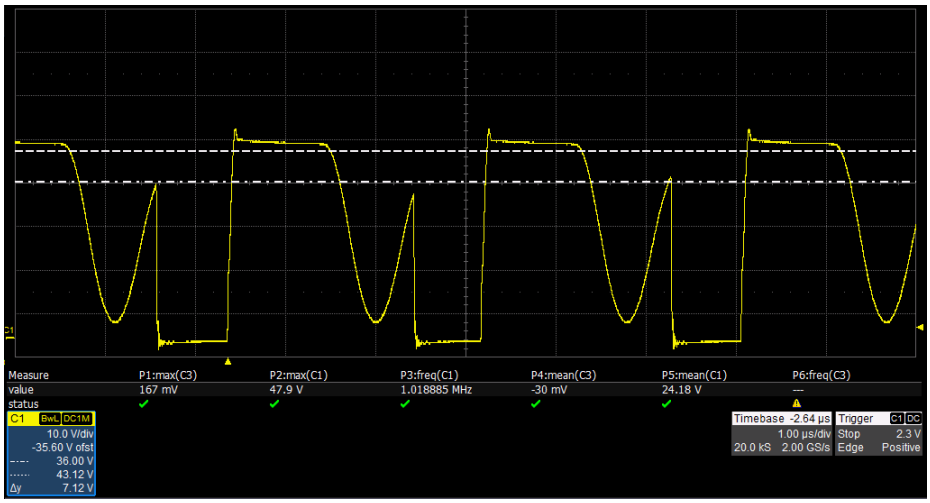


Figure 6.16. Pin SW with respect ground when the maximum voltage is applied.

Gate driving board

The first test to perform on this PCB is to verify the absence of short-circuits, thus VCC, REF and VEE pins of both the high and low-side drivers are connected to the Rigol DP832 while the DC-bus is not connected to any supply or battery. The logic of the ISO5452-Q1 is connected to the Hercules TMS570LS12x Development Kit, where InSight, a software developed by the members of the FLAG-MS, runs. Thanks to its GUI (Graphical User Interface), reported in Figure, it is possible to set and manage all the parameters needed to perform the tests (Figure 6.17):

- Frequency, death-time and duty-cycle of the PWM.
- Period and number of pulses to generate.
- Management of the RESET and FAULT pins of the gate driver.

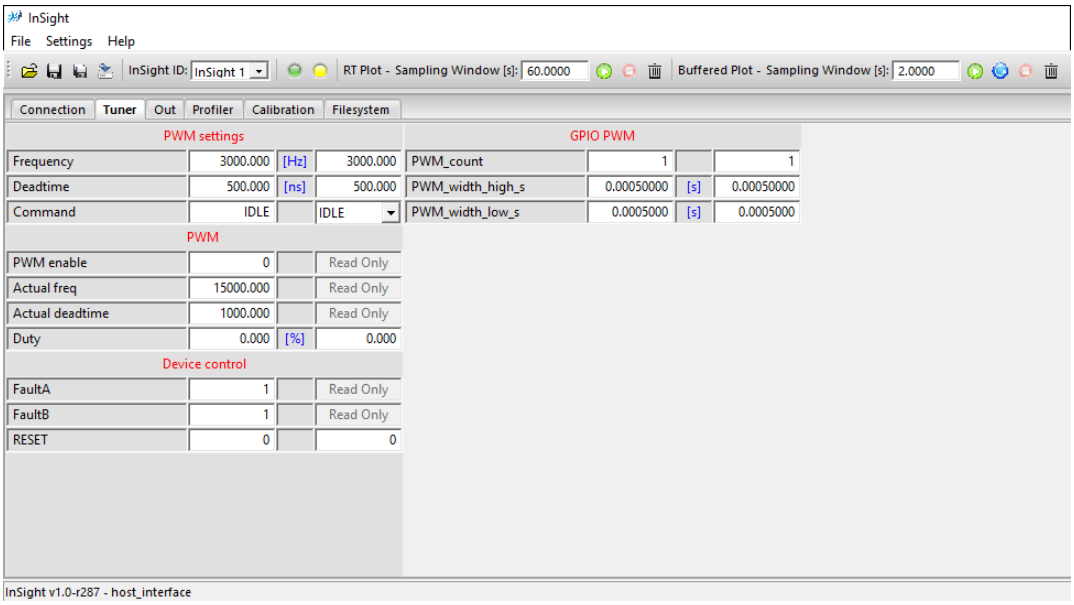


Figure 6.17. Example of an InSight GUI.

By controlling the gate drivers with pulses with different duty-cycles and different death-times, the supply voltages are correctly delivered to the gate pin of both high and low-side transistors (Figure 6.18).

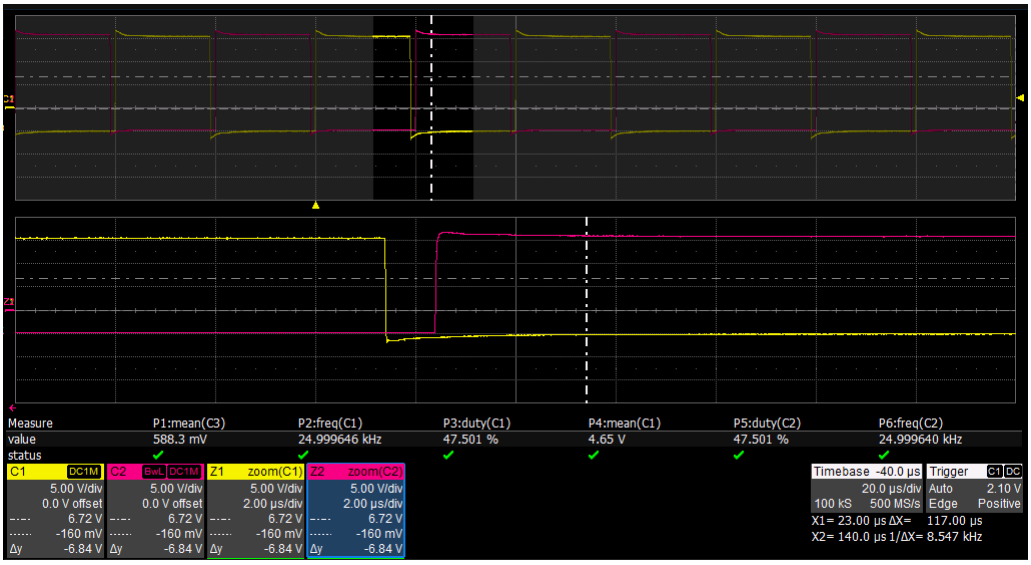


Figure 6.18. Example of the gate drivers controlled by PWM.

Thus, connecting the DC-bus to the Rigol DP832 and supplying the board with 32V and 3.3A, the gate driving board shows the expected behaviour (Figure 6.19).

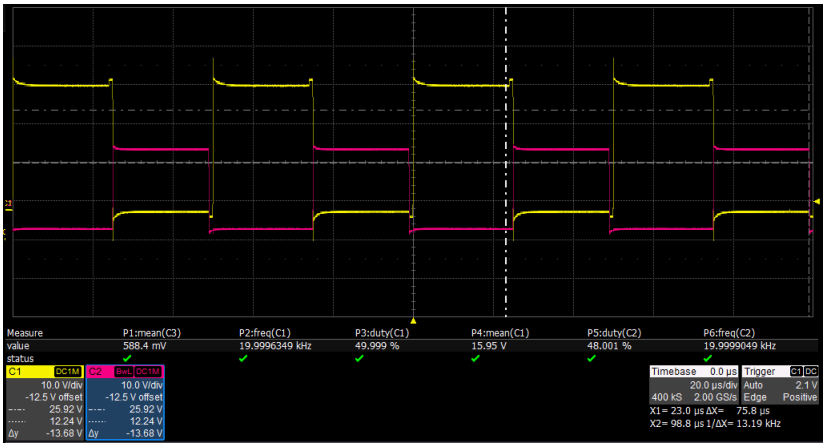


Figure 6.19. Gate of the low-side transistor (red wave) and phase voltage (yellow wave).

Test of the prototype

Since the test performed until now shows that the gate drivers, the buck converter and the flyback power supply behaves in the designed way, the complete prototype can be tested. Before to connect it to the EA-PSB 9750-60, an insulation test must be performed in order to ensure the right safety level during the measurements. The insulation is evaluated using the Fluke 1507, and a resistance of 11GΩ is measured between all the low-voltage pins and all high-voltage ones, meaning that the insulation level for the application is respected.

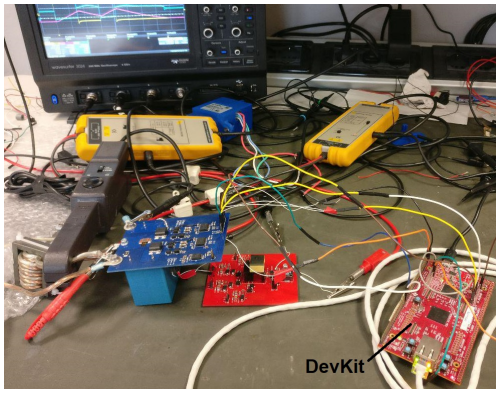


Figure 6.20. Experimental test setup.

The test concerns to drive the gate drivers with waveforms composed of one or two or three pulses, whose duration and distance among each other is setted by the InSight interface. The first transistor under test is the low-side one and the load consists of a hand-made inductor of about 30µH. The results are reported below.

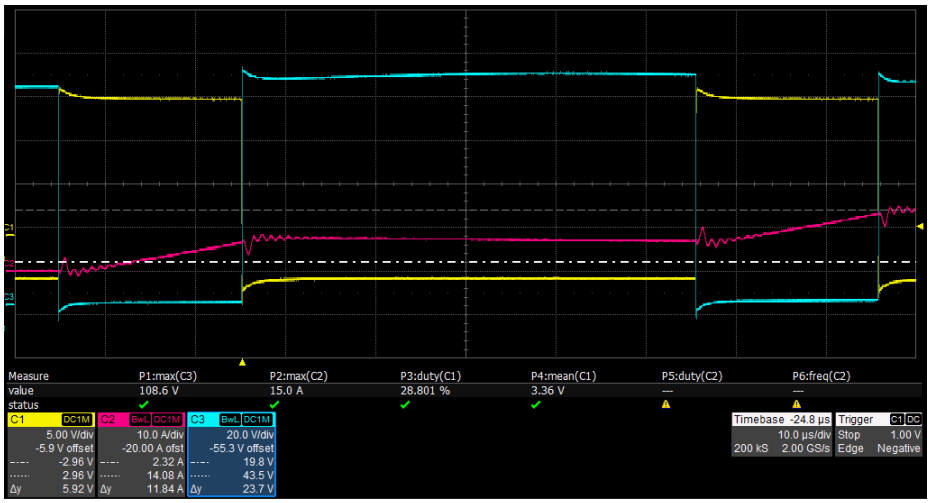


Figure 6.21. Prototype connected to a DC-bus of 100V and driven with two pulses of 20µs distanced by 50µs. The waveform reported are: gate of the low-side transistor (yellow), phase voltage (blue), output current (red).

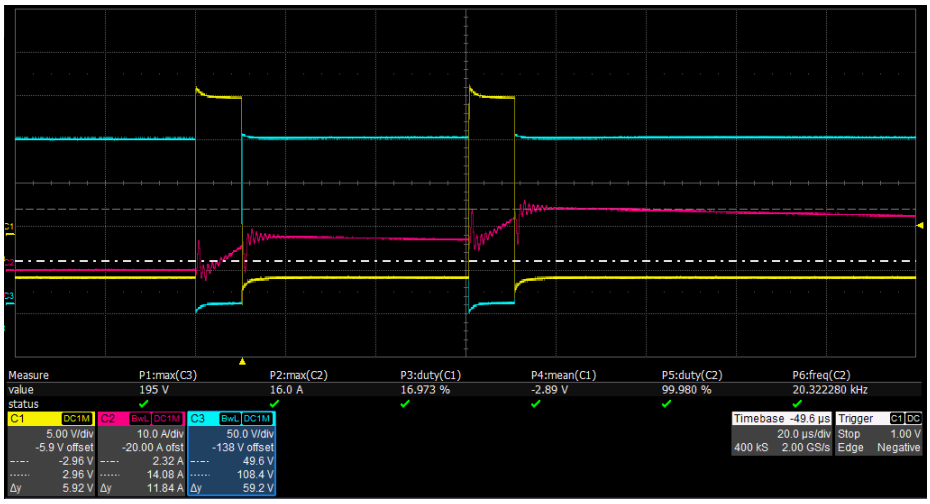


Figure 6.22. Prototype connected to a DC-bus of 200V and driven with two pulses of 10µs distanced by 50µs. The waveform reported are: gate of the low-side transistor (yellow), phase voltage (blue), output current (red).

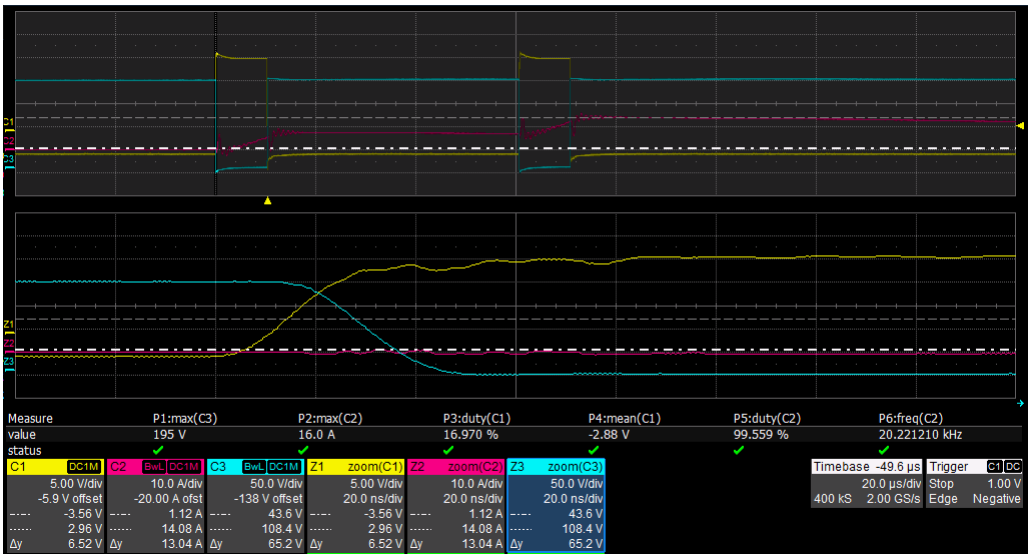


Figure 6.23. Prototype connected to a DC-bus of 200V and driven with two pulses of 10µs distanced by 50µs. Zoom of the start-up with zero output current.

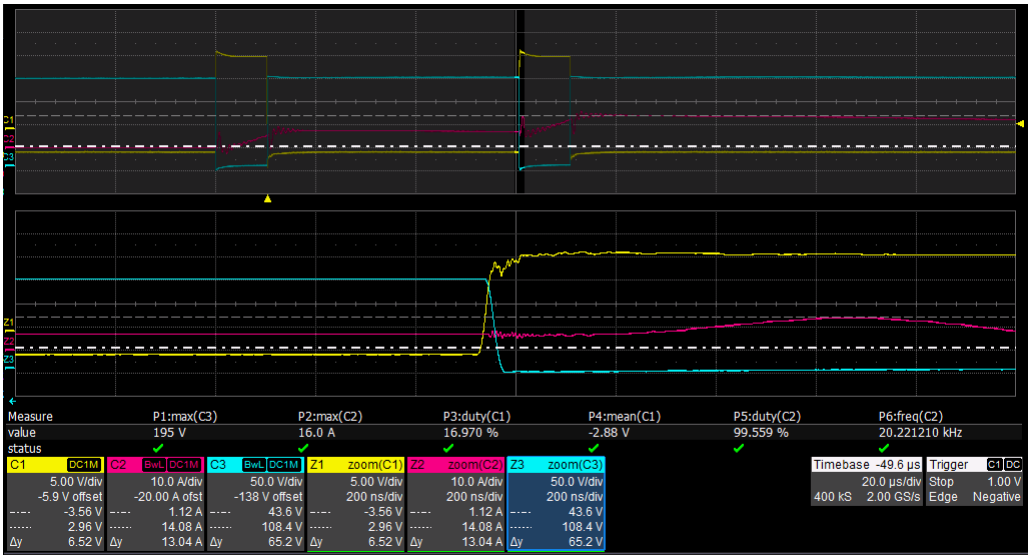


Figure 6.24. Prototype connected to a DC-bus of 200V and driven with two pulses of 10µs distanced by 50µs. Zoom of the start-up with output current different from zero.

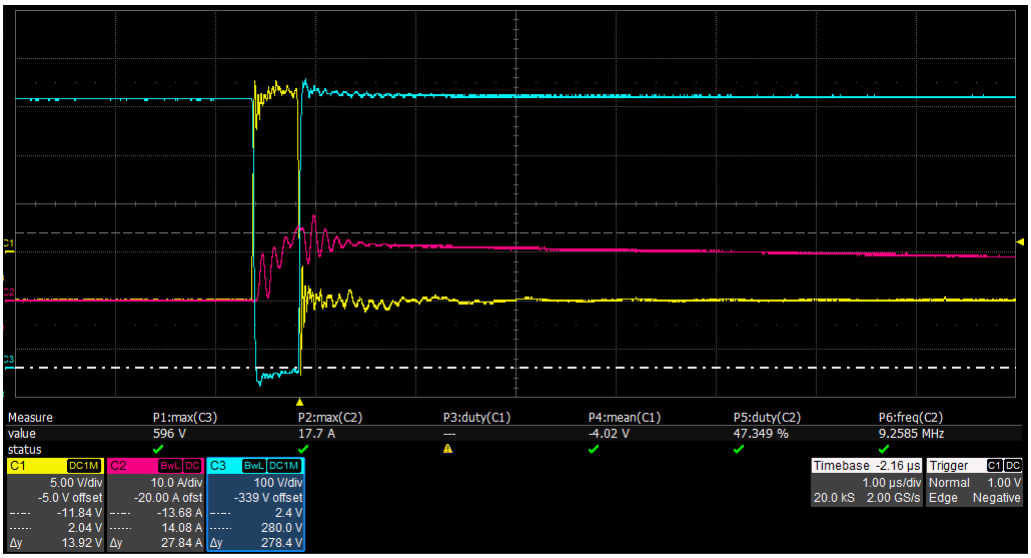


Figure 6.25. Prototype connected to a DC-bus of 550V and driven with one pulse of 0.5µs. The waveform reported are: gate of the low-side transistor (yellow), phase voltage (blue), output current (red).

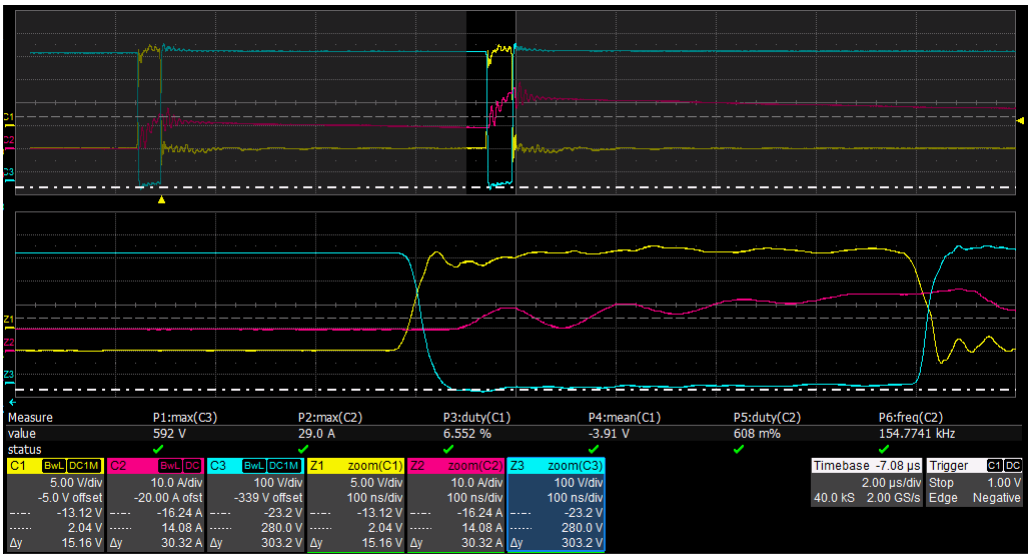


Figure 6.26. Prototype connected to a DC-bus of 550V and driven with one pulse of 0with two pulses of 0.5µs distanced by 6µs. Zoom of the start-up with output current different from zero.

Once that the low-side transistor has been tested, also the behaviour of the high-side one can be evaluated. In this case, instead of monitoring the phase voltage, the differential probe SI-9002 is connected between gate and source of the low-side transistor in order to verify that it is not turned on by the Miller current. The results are reported below.

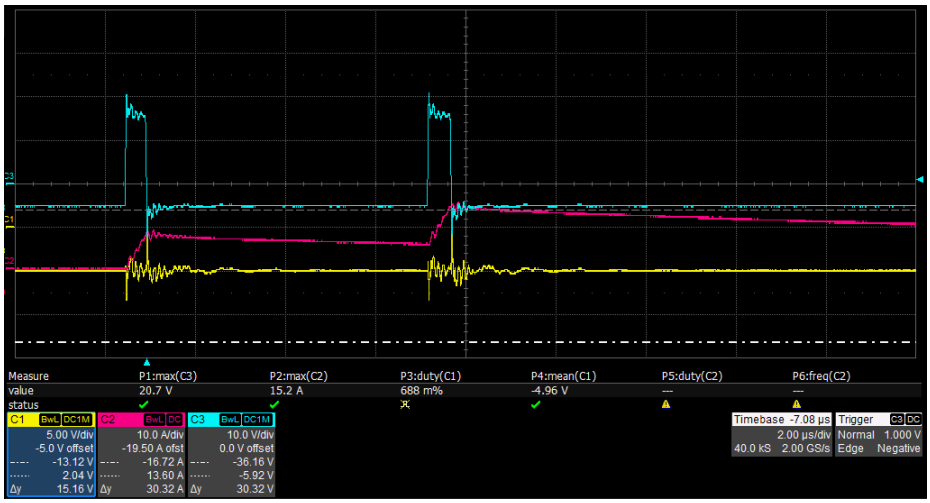


Figure 6.27. Prototype connected to a DC-bus of 350V and driven with two pulses of 0.5µs distanced by 6µs. The waveform reported are: gate of the low-side transistor (yellow), gate of the high-side transistor (blue), output current (red).

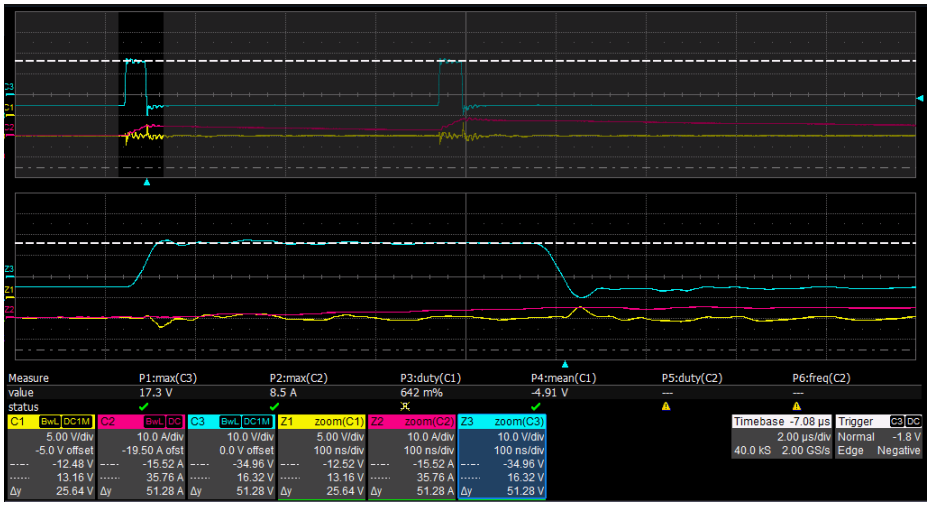


Figure 6.28. Prototype connected to a DC-bus of 350V and driven with two pulses of 0.5µs distanced by 6µs. Zoom of the waveforms.

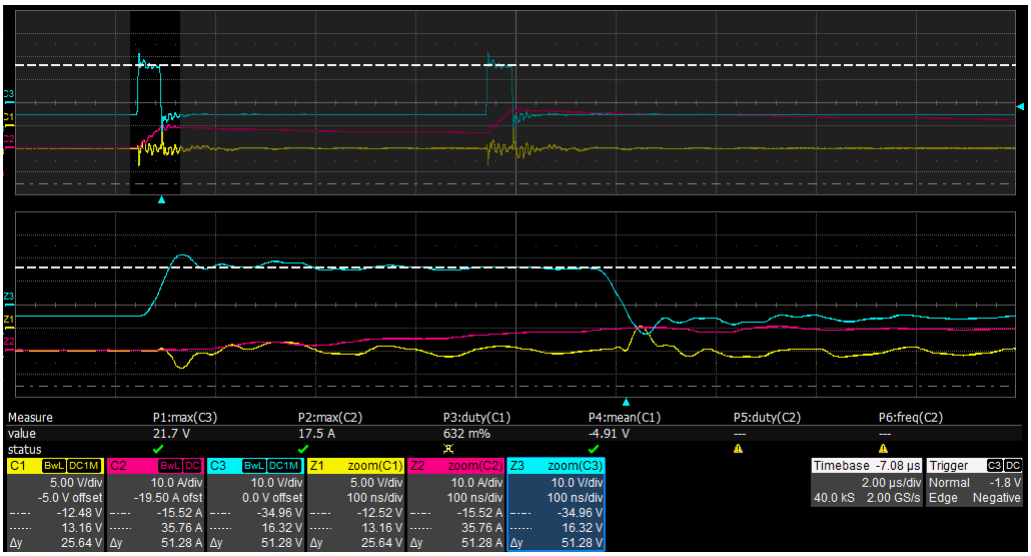


Figure 6.29. Prototype connected to a DC-bus of 400V and driven with two pulses of 0.5µs distanced by 6µs. The waveform reported are: gate of the low-side transistor (yellow), gate of the high-side transistor (blue), output current (red).

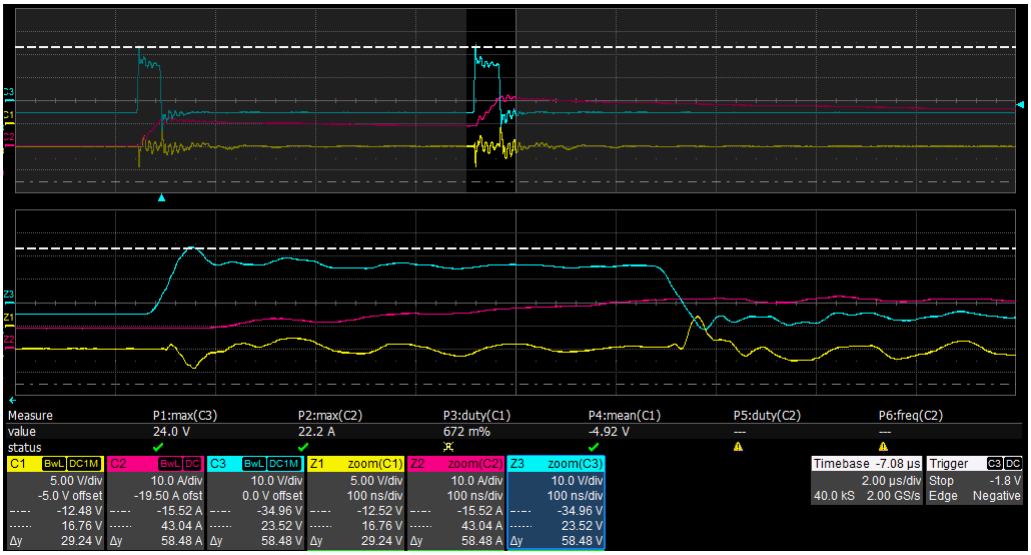


Figure 6.30. Prototype connected to a DC-bus of 500V and driven with two pulses of 0.5µs distanced by 6µs. The waveform reported are: gate of the low-side transistor (yellow), gate of the high-side transistor (blue), output current (red).

The tests show that the Miller clamp feature is able to avoid unwanted turn-on of the transistors due to Miller current. Another important protection feature is the DESAT, fully described and designed in Chapter 5; it must be verified because

it allows to protect the transistor when the current through it becomes higher than the maximum one. The drain-source voltage at which the input voltage of the DESAT pin reaches 9V is around 1.3V , as designed in (5.5), and it corresponds of a maximum allowed current of around 17A for the transistors of the prototype. The figures reported below shows the behaviour of the desaturation feature.

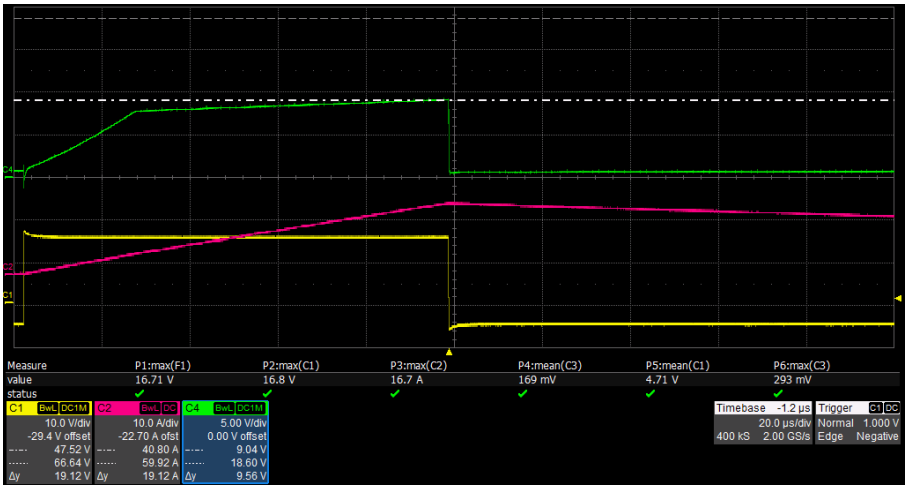


Figure 6.31. Prototype connected to a DC-bus of 200V. The waveform reported are: gate of the low-side transistor (yellow), DESAT pin (green), output current (red).

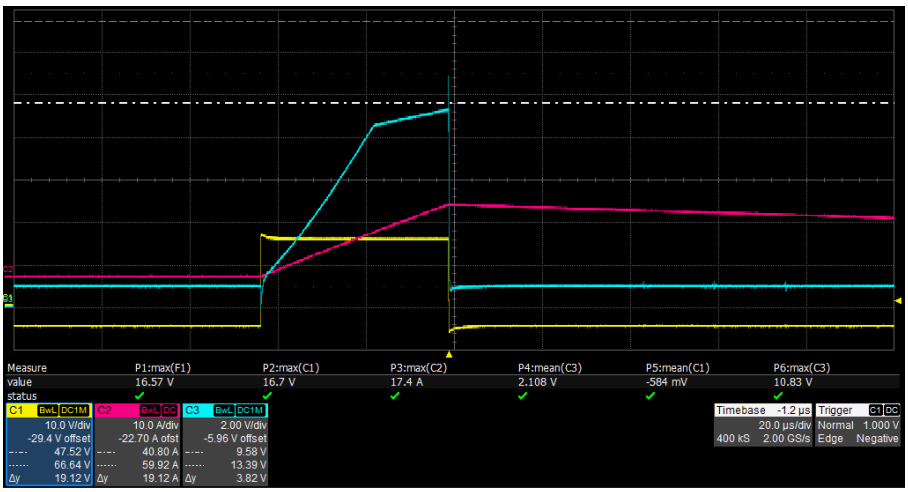


Figure 6.32. Prototype connected to a DC-bus of 550V. The waveform reported are: gate of the low-side transistor (yellow), DESAT pin (blue), output current (red).

One component implemented on this prototype has not been used during the test: the current sense amplifier. Its work will be necessary when the inverter will be test in a closed loop and with a motor load in order to monitoring the main parameters of the motor, such as its torque and angular speed. So, it must be tested and the differential output is reported in the next figure where it is visible that the voltage across the shunt perfectly follows the output current.

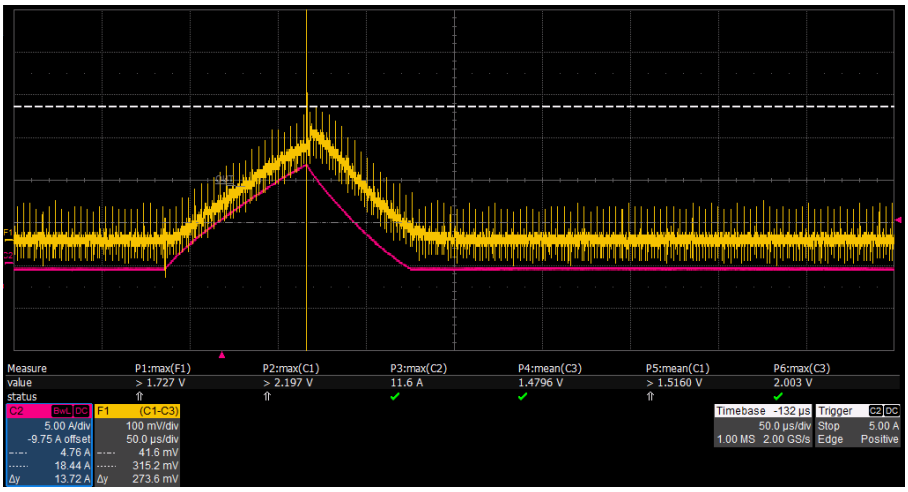


Figure 6.33. Prototype connected to a DC-bus of 250V. The output current is reported in red, while the vltage across the shunt is reported in yellow.

Chapter 7

Conclusions and future works

This work presented the design of the prototype of a three-phase two-level voltage source inverter with the required power level needed from the heavy-duty sector, along with a systematic design flow. In this context, due to the lack of information at this very beginning stage of the task about the topology of the electric motor that will be implemented in the final application, the Thesis described the design of a general-purpose AC electric drive.

The analysis begun with trends in the transportation sector, focusing on the heavy-duty vehicles and the need of electric powertrain in this sector.

The working principle of the three-phase VSI has been presented and some of the most used modulation techniques have been discussed.

The waveforms of the inverter voltages and currents have been derived thanks to the model developed in a MATLAB/SIMULINK environment in order to estimate their effects on the design. Furthermore, the model has been used to evaluate the conduction and switching power losses of the switching transistors and, after a comparison with the simulation results of SemiSel, the best switch topology has been chosen; it consists in a SiC module, a choiche that allows to combine high efficient and high power density.

Thanks to the waveforms derived from the MATLAB/SIMULINK model, and in-depth view of the DC-link current has been made and the right DC-link capacitor for minimizing the ripple of the DC-link voltage has been selected. In particular, it is a metallized polypropylene film capacitor because it can sink high rms DC-link currents with low self-heating.

The selection of the power switches and the DC-link capacitors was the pillar for the successive steps, mainly related to the design of the ancillary circuits of the inverter: the gate drivers for the power switches and their power supply, the current sense amplifier and the peripheral circuits needed to supply all the integrated

circuits of the system. Also a first estimation of the system has been computed, but it considered only the power drop over the switches and the ancillary circuits. A more precise estimation can be done when the type of motor that the inverter has to drive will be defined.

At the end of this design procedure, a prototype has been developed for validation purposes; it is composed of two different PCBs connected one to the other: one for the power circuits needed to supply the low-voltage ancillary circuits and one for the inverter including also the gate drivers, current sense amplifier and the peripheral circuits. The low-power supply and the inverter boards have been tested to verify the absence of short-circuits, the correctness of the electrical connections between parts and that all the voltage levels are correctly delivered as required to the different circuits. Tests also include verification of the galvanic insulation. Experimental tests have been carried out to verify that the required output voltages and output currents are supplied and that they are capable to work properly under all the possible different configurations.

The tests have been performed by loading the inverter with different inductive loads and, by driving it with different pulses. The system has been tested until a DC input voltage of 550V because the DC-link capacitor is rated for an operating voltage of 630V. The experimental tests have shown the correct switching behaviour of the transistors, the correct behaviour of all the protection features of the chip, the reliability of current sensing, the absence of false turn-on of the MOSFET during the high voltage transient.

From the tests on this prototype it can be inferred that all the selected and designed components are suitable to be implemented in a further final release of the inverter. The members of the FLAG-MS company can use this design as starting point for its long-term project and they will implement an improved version of the prototype. The critical aspects highlighted from the tests are the worsted efficiency with respect the designed one of the flyback and the ringing of the output current with high input voltage. The efficiency of the flyback can be increased by simply changing the Zener diodes of the output rails, while the ringing of the currents are related only to the low inductance of the load; in fact, the gate voltages are stable also in the presence of high current ringing.

An important aspect not analysed in this Thesis is the one concerning the electromagnetic compatibility (EMC) because the company has not the right environment to perform this type of test and the booking of anechoic chamber was unfeasible within the developing time of the Thesis. Furthermore, a thermal analysis of the system should be faced in the near future to ensure that the system can be used outside and under the stressing conditions of a heavy-duty application.

Appendix A

MATLAB codes

A.1 Scripts for inverter model simulation

A.1.1 Sinusoidal PWM

inverter_parameter

```
clear all;
clc;

%% DC link
P = 20e3;                       % active power
Vdc = 700;                      % DC-link voltage
Idc = P/Vdc;                    % DC current
Ipk_max = 2*Idc;                % max phase current

%% load
Vrms = 320;                     % nominal phase-to-phase rms voltage
cos_phi = 0.8;                  % power factor
phi = acos(cos_phi);
Q = P*sin(phi)/cos(phi);        % inductive reactive power

%% PWM
fsw = 15e3;                     % switching frequency
Fs = 1e3;                       % control signal frequency
Ts = 1/Fs;
shift = 0;                      % phase shifting control wave
Vt = 1;                         % triangular amplitude
Vph = Vrms/sqrt(3);             % rms phase voltage
ma_SPWM = 2*sqrt(2)*Vph/Vdc; % modulation index S PWM
Vref = ma_SPWM*Vt;              % reference control voltage
dly = 1e-7;                     % death time

%% simulation parameters
Tsamp = 2e-6;                   % sampling time (Nyquist holds)
Tsim = 20/Fs;                   % simulation time

%% power
Il_rms = P/(sqrt(3)*Vrms*cos_phi);  % line current rms
I = Il_rms*sqrt(2);                 % line current peak
```

A.1.2 Space-Vector PWM

inverter_parameter

```
clear all;
clc;

%% DC link
P = 20e3;                       % active power
```

```
Vdc = 700;                      % DC-link voltage
Idc = P/Vdc;                    % DC current
Ipk_max = 2*Idc;                % max phase current

%% load
Vrms = 320;                     % nominal phase-to-phase rms voltage
cos_phi = 0.8;                  % power factor
phi = acos(cos_phi);
Q = P*sin(phi)/cos(phi);        % inductive reactive power

%% PWM
fsw = 15e3;                     % switching frequency
Fs = 1e3;                       % control signal frequency
Ts = 1/Fs;
shift = 0;                      % phase shifting control wave
Vt = 1;                         % triangular amplitude
Vph = Vrms/sqrt(3);             % rms phase voltage
ma = sqrt(2)*Vrms/Vdc;          % modulation index SV PWM
dly = 1e-7;                     % death time

%% simulation parameters
Tsamp = 2e-6;                   % sampling time (Nyquist holds)
Tsim = 20/Fs;                   % simulation time

%% power
Il_rms = P/(sqrt(3)*Vrms*cos_phi); % line current rms
I = Il_rms*sqrt(2);                % line current peak
```

A.2 Script for losses evaluation

A.2.1 IGBT losses

```
%% CM100TX(P)-24T
% V_ce0 = 1.1;
% r_ce = 0.0095;
% V_d0 = 1.3;
% r_d = 0.00625;
% toff = 400e-9;
% ton = 70e-9;
% trr = 18e-9;
% load('CM100TXP_24T_Eoff.mat');                    %load Eoff graph
% load('CM100TXP_24T_Eon.mat');                     %load Eon graph
% load('CM100TXP_24T_Err.mat');                     %load Err graph
% Eoff_IGBT = matfile('CM100TXP_24T_Eoff.mat');     %conversion to matrix of double
% Eon_IGBT = matfile('CM100TXP_24T_Eon.mat');       %conversion to matrix of double
% Err_IGBT = matfile('CM100TXP_24T_Err.mat');       %conversion to matrix of double
% x_off = Eoff_IGBT.CM100TXP_24T_Eoff(:,1);         %x-axis value Eoff
% y_off = Eoff_IGBT.CM100TXP_24T_Eoff(:,2);         %y-axis value Eoff
% x_on = Eon_IGBT.CM100TXP_24T_Eon(:,1);            %x-axis value Eon
% y_on = Eon_IGBT.CM100TXP_24T_Eon(:,2);            %y-axis Value Eon
% x_rr = Err_IGBT.CM100TXP_24T_Err(:,1);            %x-axis value Err
% y_rr = Err_IGBT.CM100TXP_24T_Err(:,2);            %y-axis value Err

%% SEMiX101GD12E4s
% V_ce0 = 0.8;
% r_ce = 0.016;
% V_d0 = 1.1;
% r_d = 0.0137;
% toff = 500e-9;
% ton = 110e-9;
% trr = 25e-9;
% load('SEMiX101GD12E4s_Eoff.mat');                 %load Eoff graph
% load('SEMiX101GD12E4s_Eon.mat');                  %load Eon graph
% load('SEMiX101GD12E4s_Err.mat');                  %load Err graph
% Eoff_IGBT = matfile('SEMiX101GD12E4s_Eoff.mat');  %conversion to matrix of double
% Eon_IGBT = matfile('SEMiX101GD12E4s_Eon.mat');    %conversion to matrix of double
% Err_IGBT = matfile('SEMiX101GD12E4s_Err.mat');    %conversion to matrix of double
% x_off = Eoff_IGBT.SEMiX101GD12E4s_Eoff(:,1);      %x-axis value Eoff
% y_off = Eoff_IGBT.SEMiX101GD12E4s_Eoff(:,2);      %y-axis value Eoff
% x_on = Eon_IGBT.SEMiX101GD12E4s_Eon(:,1);         %x-axis value Eon
% y_on = Eon_IGBT.SEMiX101GD12E4s_Eon(:,2);         %y-axis Value Eon
% x_rr = Err_IGBT.SEMiX101GD12E4s_Err(:,1);         %x-axis value Err
% y_rr = Err_IGBT.SEMiX101GD12E4s_Err(:,2);         %y-axis value Err

%% SK100GD12T4T
V_ce0 = 1.3;
r_ce = 0.0125;
V_d0 = 1.5;
r_d = 0.014;
```

```
toff = 600e-9;
ton = 55e-9;
trr = 40e-9;
load('SK100GD12T4T_Eoff.mat');                    %load Eoff graph
load('SK100GD12T4T_Eon.mat');                     %load Eon graph
load('SK100GD12T4T_Err.mat');                     %load Err graph
Eoff_IGBT = matfile('SK100GD12T4T_Eoff.mat');     %conversion to matrix of double
Eon_IGBT = matfile('SK100GD12T4T_Eon.mat');       %conversion to matrix of double
Err_IGBT = matfile('SK100GD12T4T_Err.mat');       %conversion to matrix of double
x_off = Eoff_IGBT.SK100GD12T4T_Eoff(:,1);         %x-axis value Eoff
y_off = Eoff_IGBT.SK100GD12T4T_Eoff(:,2);         %y-axis value Eoff
x_on = Eon_IGBT.SK100GD12T4T_Eon(:,1);            %x-axis value Eon
y_on = Eon_IGBT.SK100GD12T4T_Eon(:,2);            %y-axis Value Eon
x_rr = Err_IGBT.SK100GD12T4T_Err(:,1);            %x-axis value Err
y_rr = Err_IGBT.SK100GD12T4T_Err(:,2);            %y-axis value Err

%% SEMiX101GD12Vs
% V_ce0 = 1.04;
% r_ce = 0.0152;
% V_d0 = 1.5;
% r_d = 0.0137;
% toff = 550e-9;
% ton = 320e-9;
% trr = 35e-9;
% load('SEMiX101GD12Vs_Eoff.mat');                    %load Eoff graph
% load('SEMiX101GD12Vs_Eon.mat');                     %load Eon graph
% load('SEMiX101GD12Vs_Err.mat');                     %load Err graph
% Eoff_IGBT = matfile('SEMiX101GD12Vs_Eoff.mat');     %conversion to matrix of double
% Eon_IGBT = matfile('SEMiX101GD12Vs_Eon.mat');       %conversion to matrix of double
% Err_IGBT = matfile('SEMiX101GD12Vs_Err.mat');       %conversion to matrix of double
% x_off = Eoff_IGBT.SEMiX101GD12Vs_Eoff(:,1);         %x-axis value Eoff
% y_off = Eoff_IGBT.SEMiX101GD12Vs_Eoff(:,2);         %y-axis value Eoff
% x_on = Eon_IGBT.SEMiX101GD12Vs_Eon(:,1);            %x-axis value Eon
% y_on = Eon_IGBT.SEMiX101GD12Vs_Eon(:,2);            %y-axis Value Eon
% x_rr = Err_IGBT.SEMiX101GD12Vs_Err(:,1);            %x-axis value Err
% y_rr = Err_IGBT.SEMiX101GD12Vs_Err(:,2);            %y-axis value Err

%% FS75R12KT4_B15
% V_ce0 = 0.96;
% r_ce = 0.017;
% V_d0 = 1.25;
% r_d = 0.011;
% ton = 0.15e-6;
% toff = 0.40e-6;
% trr = 0.09e-6;
% load('FS75R12KT4_B15_Eoff.mat');                    %load Eoff graph
% load('FS75R12KT4_B15_Eon.mat');                     %load Eon graph
% load('FS75R12KT4_B15_Err.mat');                     %load Err graph
% Eoff_IGBT = matfile('FS75R12KT4_B15_Eoff.mat');     %conversion to matrix of double
% Eon_IGBT = matfile('FS75R12KT4_B15_Eon.mat');       %conversion to matrix of double
% Err_IGBT = matfile('FS75R12KT4_B15_Err.mat');       %conversion to matrix of double
% x_off = Eoff_IGBT.FS75R12KT4_B15_Eoff(:,1);         %x-axis value Eoff
% y_off = Eoff_IGBT.FS75R12KT4_B15_Eoff(:,2);         %y-axis value Eoff
% x_on = Eon_IGBT.FS75R12KT4_B15_Eon(:,1);            %x-axis value Eon
% y_on = Eon_IGBT.FS75R12KT4_B15_Eon(:,2);            %y-axis Value Eon
% x_rr = Err_IGBT.FS75R12KT4_B15_Err(:,1);            %x-axis value Err
% y_rr = Err_IGBT.FS75R12KT4_B15_Err(:,2);            %y-axis value Err

%% IRGPS60B120KDP
% V_ce0 = 1.5;
% r_ce = 0.022;
% V_d0 = 1.25;
% r_d = 0.015;
% ton = 60e-9;
% toff = 130e-9;
% trr = 32e-9;
% load('IRGPS60B120KDP_Eoff.mat');                    %load Eoff graph
% load('IRGPS60B120KDP_Eon.mat');                     %load Eon graph
% load('IRGPS60B120KDP_Err.mat');                     %load Err graph
% Eoff_IGBT = matfile('IRGPS60B120KDP_Eoff.mat');     %conversion to matrix of double
% Eon_IGBT = matfile('IRGPS60B120KDP_Eon.mat');       %conversion to matrix of double
% Err_IGBT = matfile('IRGPS60B120KDP_Err.mat');       %conversion to matrix of double
% x_off = Eoff_IGBT.IRGPS60B120KDP_Eoff(:,1);         %x-axis value Eoff
% y_off = Eoff_IGBT.IRGPS60B120KDP_Eoff(:,2);         %y-axis value Eoff
% x_on = Eon_IGBT.IRGPS60B120KDP_Eon(:,1);            %x-axis value Eon
% y_on = Eon_IGBT.IRGPS60B120KDP_Eon(:,2);            %y-axis Value Eon
% x_rr = Err_IGBT.IRGPS60B120KDP_Err(:,1);            %x-axis value Err
% y_rr = Err_IGBT.IRGPS60B120KDP_Err(:,2);            %y-axis value Err

%% trigger
current_index = find(out.IGBT_current.Data);   % index with non zero current
i_IGBT = out.IGBT_current.Data(current_index); % non zero current values
t_IGBT = out.IGBT_current.Time(current_index); % time of non zero current values
```

```
time_index = find((t_IGBT >= 4.5*Ts) & (t_IGBT <= (Tsim - 2*Ts))); % time values at regime
current_IGBT = i_IGBT(time_index);                  % non zero current values at regime
positive_index = find(current_IGBT > 0);            % index with positive current at regime
positive_current = current_IGBT(positive_index);    % positive current values at regime
trigger = find(out.IGBT_current.Data == min(positive_current)); % index with smallest value of
    positive current
start_point = out.IGBT_current.Time(trigger); % start point = time value with smallest current
end_point = start_point(1) + Ts;                % end point after one control signal period
T_IGBT = getsampleusingtime(out.IGBT_current, start_point(1),end_point); % one period of current
     at regime
xIGBT = 0:(Ts/(length(T_IGBT.Data)-1)):Ts;          % x-axis values for plot
%plot(xIGBT , T_IGBT.Data);

%% edge detection
index_nz_IGBT = find(T_IGBT.Data);      % index of non zero current over the selected period
index_z_IGBT = find(~T_IGBT.Data);      % index of zero current over the selected period
rising_edges = find(ismember((index_nz_IGBT) , (index_z_IGBT+1))); % searching for on edges
positive_peak = index_nz_IGBT(rising_edges);                        % on edges index
on_peak = T_IGBT.Data(union(positive_peak , index_z_IGBT));         % rising edges current values
x_on_peak = xIGBT(union(positive_peak , index_z_IGBT));             % rising edge time values
%plot(x_on_peak,on_peak,'b.' , xIGBT,T_IGBT.Data);
falling_edges = find(ismember((index_nz_IGBT) , (index_z_IGBT-1))); % searching for off edges
negative_peak = index_nz_IGBT(falling_edges);                        % off edges index
off_peak = T_IGBT.Data(union(negative_peak , index_z_IGBT));         % falling edges current
    values
x_off_peak = xIGBT(union(negative_peak , index_z_IGBT));             % falling edges time values
%plot(x_off_peak,off_peak,'b.' , xIGBT,T_IGBT.Data);
%plot(xIGBT,T_IGBT.Data,'g' , x_off_peak(off_peak~=0) , off_peak(off_peak~=0),'b*' , x_on_peak(
    on_peak~=0),on_peak(on_peak~=0),'r.');
ton_index = find(on_peak >= 0);                 % index of all transistor ton
toff_index = find(off_peak >= 0);               % index of all transistor toff
trr_index = find(on_peak <= 0); % index of all diode ton (diode toff can be neglected)
i_on = round(on_peak(ton_index) , 4).';         % transistor current on ton
x_i_on = x_on_peak(ton_index);                  % time values of i_on
i_off = round(off_peak(toff_index) , 4).';      % transistor current on toff
x_i_off = x_off_peak(toff_index);               % time values of i_off
i_rr = round(on_peak(trr_index) , 4).';         % diode current on ton
x_i_rr = x_on_peak(trr_index);                  % time values of i_rr

%% conduction losses
pct_index = find(T_IGBT.Data >= 0);  % transistor index, transistor is on during the positive
    part
p_ct = abs(T_IGBT.Data(pct_index)).*V_ce0 + (T_IGBT.Data(pct_index).^2).*r_ce;
pcd_index = find(T_IGBT.Data <= 0);  % diode index, diode is on during the negative part
p_cd = abs(T_IGBT.Data(pcd_index)).*V_d0 + (T_IGBT.Data(pcd_index).^2).*r_d;
x_ct = xIGBT(pct_index);
x_cd = xIGBT(pcd_index);
Pcd = trapz(x_cd , p_cd)/Ts;
Pct = trapz(x_ct , p_ct)/Ts;
%plot(x_cd,p_cd , x_ct,p_ct);

%% switching losses
xq = round((0:0.0001:200) , 4);  % generate all the current values of Eoff, Eon, Err
Eoff_data = interp1(x_off , y_off , xq , 'pchip');   % interpolate datasheet curve
Eon_data = interp1(x_on , y_on  , xq , 'pchip');     % interpolate datasheet curve
Err_data = interp1(x_rr , y_rr , xq , 'pchip');      % interpolate datasheet curve
e_on = zeros(1 , length(i_on));                      % pre-allocation
e_off = zeros(1 , length(i_on));                     % pre-allocation
e_rr = zeros(1 , length(i_rr));                      % pre-allocation
e_on(i_on == 0) = 0;
for i = find(i_on)
        on_index = find(ismember(xq , i_on(i))); % find the index of the ton transistor current
            in the Eon graph
        e_on(i) = Eon_data(on_index);            % ton switching power
end
e_off(i_off == 0) = 0;
for i = find(i_off)
        off_index = find(ismember(xq , i_off(i))); % find the index of the toff transistor
            current in the Eoff graph
        e_off(i) = Eoff_data(off_index);           % toff switching power
end
e_rr(i_rr == 0) = 0;
for i = find(i_rr)
        rr_index = find(ismember(xq , abs(i_rr(i)))); % find the index of the trr diode current
            in the Err graph
        e_rr(i) = Err_data(rr_index);                 % trr switching power
end
P_on = sum(e_on , 'all')/Ts;
P_off = sum(e_off , 'all')/Ts;
P_rr = sum(e_rr , 'all')/Ts;
%plot(x_i_rr , e_rr);
%plot(x_i_off , e_off);
%plot(x_i_on , e_on);
```

```
%plot(x_i_rr,e_rr,'r',x_i_off,e_off,'k',x_i_on,e_on,'b');
```

A.2.2 MOSFET losses

```
%% APTMC120TAM33CTPAG
% r_ds = 0.07;
% V_d0 = 2.8;
% r_d = 0.014;
% load('APTMC120TAM33CTPAG_Eoff.mat');                    %load Eoff graph
% load('APTMC120TAM33CTPAG_Eon.mat');                     %load Eon graph
% Eoff_IGBT = matfile('APTMC120TAM33CTPAG_Eoff.mat');     %conversion to matrix of double
% Eon_IGBT = matfile('APTMC120TAM33CTPAG_Eon.mat');       %conversion to matrix of double
% x_off = Eoff_IGBT.APTMC120TAM33CTPAG_Eoff(:,1);         %x-axis value Eoff
% y_off = Eoff_IGBT.APTMC120TAM33CTPAG_Eoff(:,2);         %y-axis value Eoff
% x_on = Eon_IGBT.APTMC120TAM33CTPAG_Eon(:,1);            %x-axis value Eon
% y_on = Eon_IGBT.APTMC120TAM33CTPAG_Eon(:,2);            %y-axis Value Eon

%% CCS050M12CM2
r_ds = 0.063;
V_d0 = 1.8;
r_d = 0.02;
load('CCS050M12CM2_Eoff.mat');                    %load Eoff graph
load('CCS050M12CM2_Eon.mat');                     %load Eon graph
Eoff_IGBT = matfile('CCS050M12CM2_Eoff.mat');     %conversion to matrix of double
Eon_IGBT = matfile('CCS050M12CM2_Eon.mat');       %conversion to matrix of double
x_off = Eoff_IGBT.CCS050M12CM2_Eoff(:,1);         %x-axis value Eoff
y_off = Eoff_IGBT.CCS050M12CM2_Eoff(:,2);         %y-axis value Eoff
x_on = Eon_IGBT.CCS050M12CM2_Eon(:,1);            %x-axis value Eon
y_on = Eon_IGBT.CCS050M12CM2_Eon(:,2);            %y-axis Value Eon

%% trigger
current_index = find(out.MOS_current.Data);       %index with non zero current
i_MOS = out.MOS_current.Data(current_index);      %non zero current values
t_MOS = out.MOS_current.Time(current_index);      %time of non zero current values
time_index = find((t_MOS >= 4.5*Ts) & (t_MOS <= (Tsim - 2*Ts)));  %time index at regime
current_MOS = i_MOS(time_index);                  %non zero current values at regime
positive_index = find(current_MOS > 0);           %index with positive current at regime
positive_current = current_MOS(positive_index);   %positive current values at regime
trigger = find(out.MOS_current.Data == min(positive_current));    %index with smallest value of
    positive current
start_point = out.MOS_current.Time(trigger);  %start point = time value with smallest current
end_point = start_point(1) + Ts;              %end point after one control signal period
T_MOS = getsampleusingtime(out.MOS_current, start_point(1),end_point); %one period of current
xMOS = 0:(Ts/(length(T_MOS.Data)-1)):Ts;          %x-axis values for plot
%plot(xMOS , T_MOS.Data);

%% edge detection
index_nz_MOS = find(T_MOS.Data);          %index of non zero current over the selected period
index_z_MOS = find(~T_MOS.Data);          %index of zero current over the selected period
rising_edges = find(ismember((index_nz_MOS) , (index_z_MOS+1)));  %searching for on edges
positive_peak = index_nz_MOS(rising_edges);                       %on edges index
on_peak = T_MOS.Data(union(positive_peak , index_z_MOS));         %rising edges current values
x_on_peak = xMOS(union(positive_peak , index_z_MOS));             %rising edge time values
%plot(x_on_peak,on_peak,'b.' , xMOS,T_MOS.Data);
falling_edges = find(ismember((index_nz_MOS) , (index_z_MOS-1)));  %searching for off edges
negative_peak = index_nz_MOS(falling_edges);                      %off edges index
off_peak = T_MOS.Data(union(negative_peak , index_z_MOS));   %falling edges current values
x_off_peak = xMOS(union(negative_peak , index_z_MOS));       %falling edges time values
%plot(x_off_peak,off_peak,'b.' , xMOS,T_MOS.Data);
%plot(xMOS,T_MOS.Data,'g' , x_off_peak(off_peak~=0) , off_peak(off_peak~=0),'b*' , x_on_peak(
    on_peak~=0),on_peak(on_peak~=0),'r.')
ton_index = find(on_peak >= 0);                           %index of all transistor ton
toff_index = find(off_peak >= 0);                         %index of all transistor toff
trr_index = find(on_peak <= 0); %index of all diode ton (diode toff can be neglected)
i_on = round(on_peak(ton_index) , 4).';                   %transistor current on ton
x_i_on = x_on_peak(ton_index);                            %time values of i_on
i_off = round(off_peak(toff_index) , 4).';                %transistor current on toff
x_i_off = x_off_peak(toff_index);                         %time values of i_off
i_rr = round(on_peak(trr_index) , 4).';                   %diode current on ton
x_i_rr = x_on_peak(trr_index);                            %time values of i_rr

%% conduction losses
pcm_index = find(T_MOS.Data >= 0);      %transistor index, transistor is on during the positive
    part
p_cm = (T_MOS.Data(pcm_index).^2).*r_ds;
pcd_index = find(T_MOS.Data <= 0);      %diode index, diode is on during the negative part
```

```
p_cd = abs(T_MOS.Data(pcd_index)).*V_d0 + (T_MOS.Data(pcd_index).^2).*r_d;
x_cm = xMOS(pcm_index);
x_cd = xMOS(pcd_index);
Pcd = trapz(x_cd , p_cd)/Ts;
% Pct = trapz(x_cm , p_cm)/Ts;
% Pct = (max(T_MOS.Data(pcm_index)).^2).*((1/8 + (ma_SPWM*cos_phi)/(3*pi))*r_ds);
Pcd = max(abs(T_MOS.Data(pcd_index))).*(V_d0*(1/(2*pi) - (ma_SPWM*cos_phi)/8)) + (max(abs(T_MOS.
    Data(pcd_index))).^2).*((1/8 - (ma_SPWM*cos_phi)/(3*pi))*r_d);
%plot(x_cd,p_cd , x_cm,p_cm);

%% switching losses
xq = round((0:0.0001:200) , 4); %generate all the current values of Eoff, Eon, Err
Eoff_data = interp1(x_off , y_off , xq , 'pchip');   %interpolate datasheet curve
Eon_data = interp1(x_on , y_on  , xq , 'pchip');     %interpolate datasheet curve
Err_data = interp1(x_on , y_on  , xq , 'pchip');     %interpolate datasheet curve
p_on = zeros(1 , length(i_on));                      %pre-allocation
p_off = zeros(1 , length(i_on));                     %pre-allocation
p_rr = zeros(1 , length(i_rr));                      %pre-allocation
p_on(i_on == 0) = 0;
for i = find(i_on)
on_index = find(ismember(xq , i_on(i))); %find the index of the ton transistor current in the
    Eon graph
p_on(i) = Eon_data(on_index);            %ton switching power
end
p_off(i_off == 0) = 0;
for i = find(i_off)
off_index = find(ismember(xq , i_off(i))); %find the index of the toff transistor current in the
     Eoff graph
p_off(i) = Eoff_data(off_index);           %toff switching power
end
p_rr(i_rr == 0) = 0;
for i = find(i_rr)
    rr_index = find(ismember(xq , abs(i_rr(i))));  %find the index of the trr diode current in
        the Err graph
    p_rr(i) = Err_data(rr_index);                  %trr switching power
end
%plot(x_i_rr , p_rr);
%plot(x_i_off , p_off);
%plot(x_i_on , p_on);
P_on = sum(p_on , 'all')/Ts;
P_off = sum(p_off , 'all')/Ts;
P_rr = sum(p_rr , 'all')/Ts;
```

A.3 Scripts for capacitance evaluation

Spectrum of the DC-link current

```
%% input current
DC = mean(out.IDC.Data);
AC = out.IDC.Data - DC;
Ic_rms = rms(AC);
Pdc = Vdc*DC;

%% FFT
dt = out.IDC.Time(2) - out.IDC.Time(1);                          % resolution
Dec_factor = 1;                                                  % decimation factor
Current = repmat(downsample(AC , Dec_factor ) , 1 , 10);
t_s = out.IDC.Time;                                              % sampling period
N = length(Current);                                             % signal length
t = 0:dt*Dec_factor:(N-1)*dt*Dec_factor;                         % time vector
Iac = AC(t > 0.8*t(end));                                        % current at regime
N_fft = length(Iac);
f_fft = 0.5/(dt*Dec_factor)*linspace(0 , 1 , N_fft/2+1);
Iac_FFT = fft(Iac)/N_fft;                                        % single sided FFT

%% plot single-sided amplitude spectrum.
figure;
semilogx(f_fft , 2*abs(Iac_FFT(1:N_fft/2+1)) , 'linewidth', 2);
title('Single-Sided Amplitude Spectrum');
xlabel('Frequency (Hz)');
ylabel('|I(f)|');
grid on;
```

Capacitance value

```
clear all;
clc;

%% DC link
P = 20e3;                                % active power
Vdc = 700;
Idc = P/Vdc;
Ipk_max = 2*Idc;

%% PWM
Fs = 50;                                 % control signal frequency
Ts = 1/Fs;
fsw = 20e3;                              % switching frequency
ma = 0.53;                               % worst case modulation index
dly = 1e-9;                              % blank time

%% load
Vrms = Vdc*ma/sqrt(2);                   % worst case line rms voltage
cos_phi = 1;                             % worst case
phi = acos(cos_phi);
Q = P*sin(phi)/cos(phi);                 % inductive reactive power

%% simulation parameters
Tsamp = 2e-6;                            % sampling time (Nyquist holds)
Tsim = 20/Fs;                            % simulation time

%% simulink
svm = sim('MOS_svpwm');
IDC = svm.IDC.Data;
xIDC = svm.IDC.Time;
SOS = find(xIDC == 15*Ts);
DC = mean(IDC(SOS:end));
AC = IDC(SOS:end) - DC;
Irms = rms(AC);
Pdc = Vdc*DC;
Iph_max = max(svm.IGBT_current.Data);
min_max_Ic = [max(AC) abs(min(AC))];
Ic_max = max(min_max_Ic);
IC = cumtrapz(xIDC(SOS:end) , AC);
% plot(svm.IDC.Time(SOS:end) , IC);
Iripple = max(IC) - min(IC);
Vripple = 0.01*Vdc:0.01*Vdc:0.2*Vdc;
ESR = Vripple/Ic_max;                    % max parasitic resistance
C_vpp = (Vripple.^-1).*Iripple;
Csweep = 10e-6:10e-6:900e-6;
Vrpp = (Csweep.^-1).*Iripple;
figure;
set(0, 'DefaultLineLineWidth', 2);
plot(Vripple , C_vpp , 'k');
title('Capacitance with respect ripple amplitude');
xlabel('Voltage [V]');
ylabel('Capacitance [C]');
grid on;
hold on;
figure;
plot(Vripple , ESR , 'k');
title('ESR with respect ripple amplitude');
xlabel('Voltage [V]');
ylabel('ESR [ohm]');
grid on;
hold on;
figure;
plot(Csweep , Vrpp , 'k');
title('Ripple ampltude with respect capacitance');
xlabel('Capacitance [C]');
ylabel('Voltage [V]');
grid on;
hold on;
Cest = 118e-06;
ESRest = 0.58;
nCAP = 4;                                % number of parallel capacitors
nC = Cest/nCAP;
nESR = nCAP*ESRest;
nDC = mean(IDC(SOS:end).*(nCAP^-1));
nAC = (IDC(SOS:end).*(nCAP^-1)) - nDC;
nRMS = rms(nAC);
```

Appendix B

SIMULINK models

B.1 Inverter with IGBT and Sinusoidal PWM

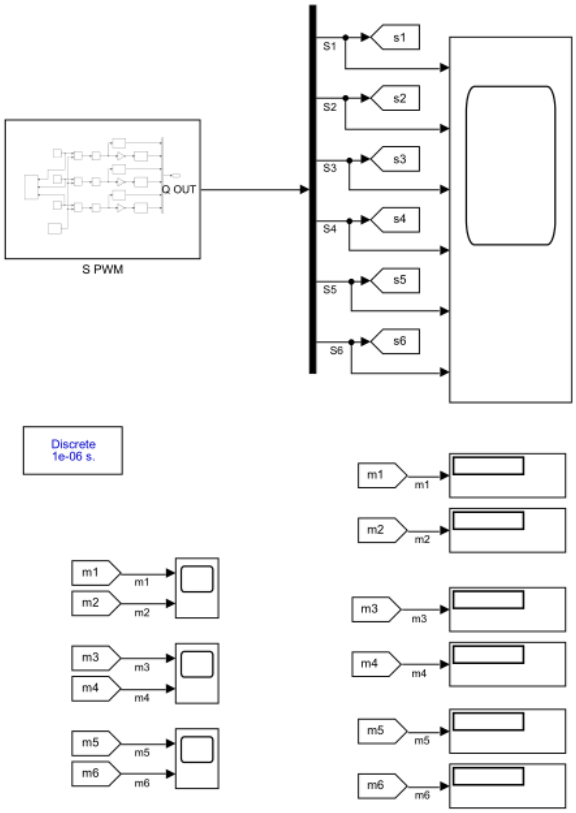


Figure B.1. First section of the SIMULINK model for the evaluation of IGBT losses with Sinusoidal PWM.

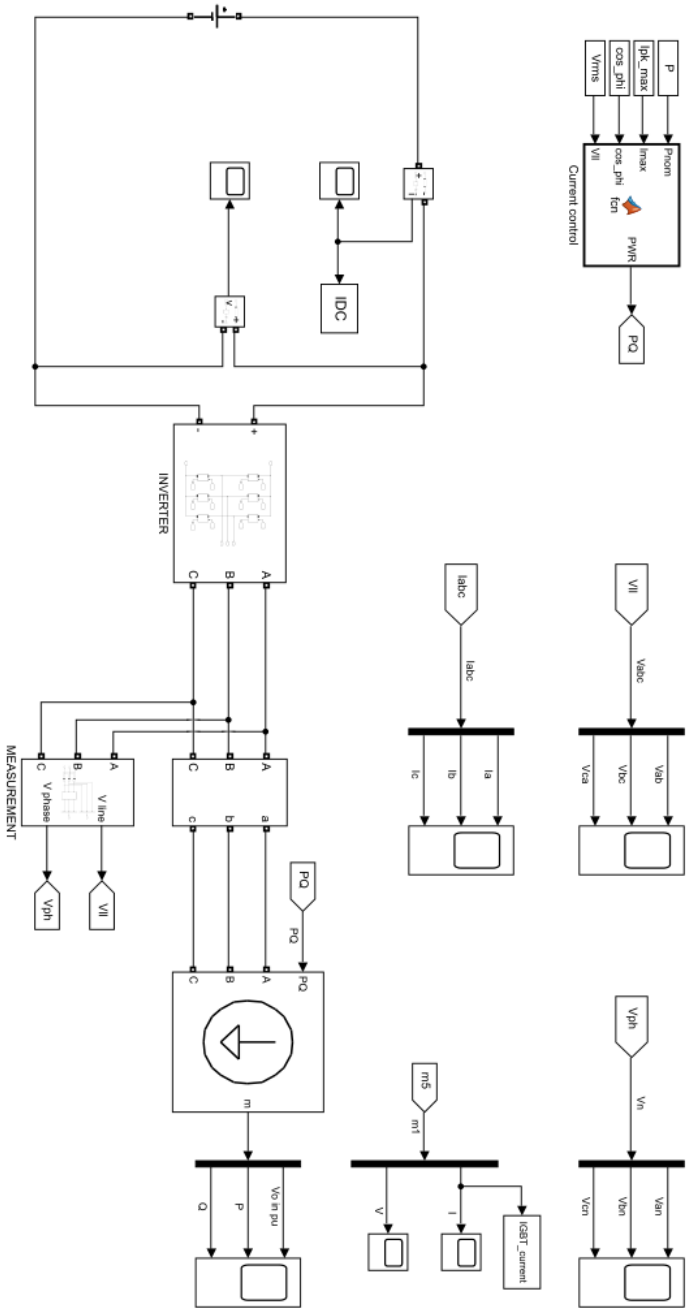


Figure B.2. Second section of the SIMULINK model for the evaluation of IGBT losses with Sinusoidal PWM.

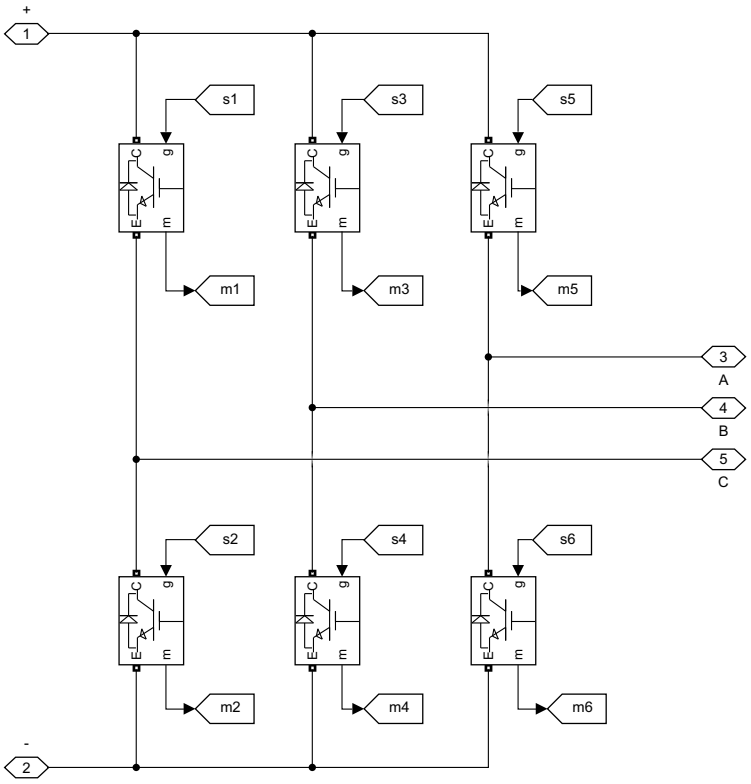


Figure B.3. Subsystem "INVERTER" (Figure B.2) of the three-phase inverter with IGBT transistors.

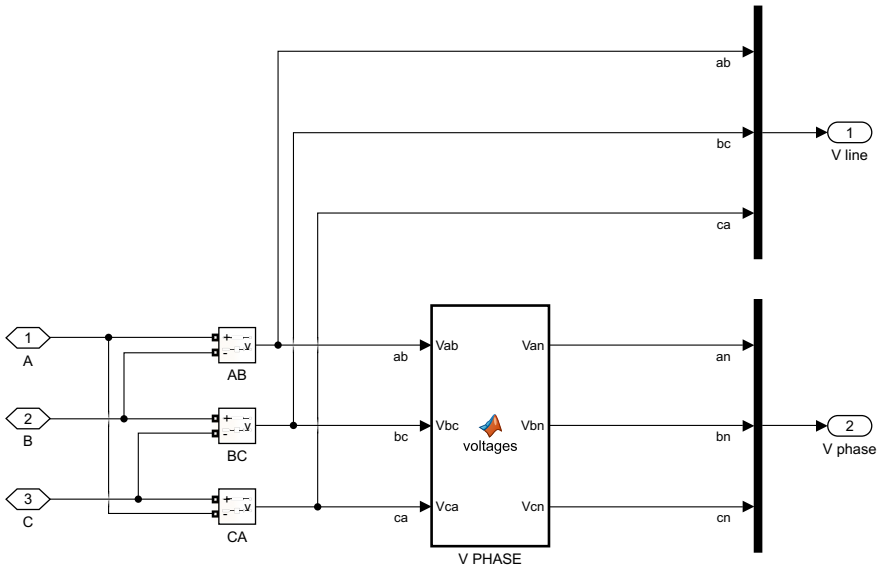


Figure B.4. Subsystem "MEASUREMENT" (Figure B.2) for the evaluation of phase and line voltages.

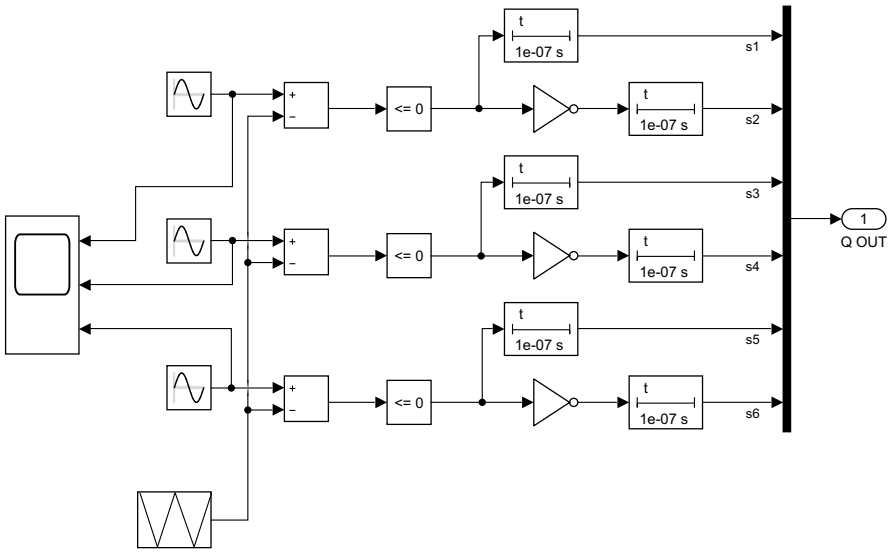


Figure B.5. Subsystem "S PWM" (Figure B.1) for the generation of the Sinusoidal PWM.

Current Control

```
function PWR = fcn(Pnom , Imax , cos_phi , Vll)

Iph = Pnom/(sqrt(3)*Vll*cos_phi);
phi = acos(cos_phi);

if Iph*sqrt(2) >= Imax
        P = sqrt(3/2)*Vll*Imax*cos_phi;
        Q = P*sin(phi)/cos(phi);
else
        P = Pnom;
        Q = P*sin(phi)/cos(phi);
end

PWR = [P Q];
```

V PHASE

```
function [Van, Vbn, Vcn] = voltages(Vab, Vbc, Vca)

Van=(Vab-Vca)/3;
Vbn=(Vbc-Vab)/3;
Vcn=(Vca-Vbc)/3;
```

B.2 Inverter with IGBT and Space-Vector PWM

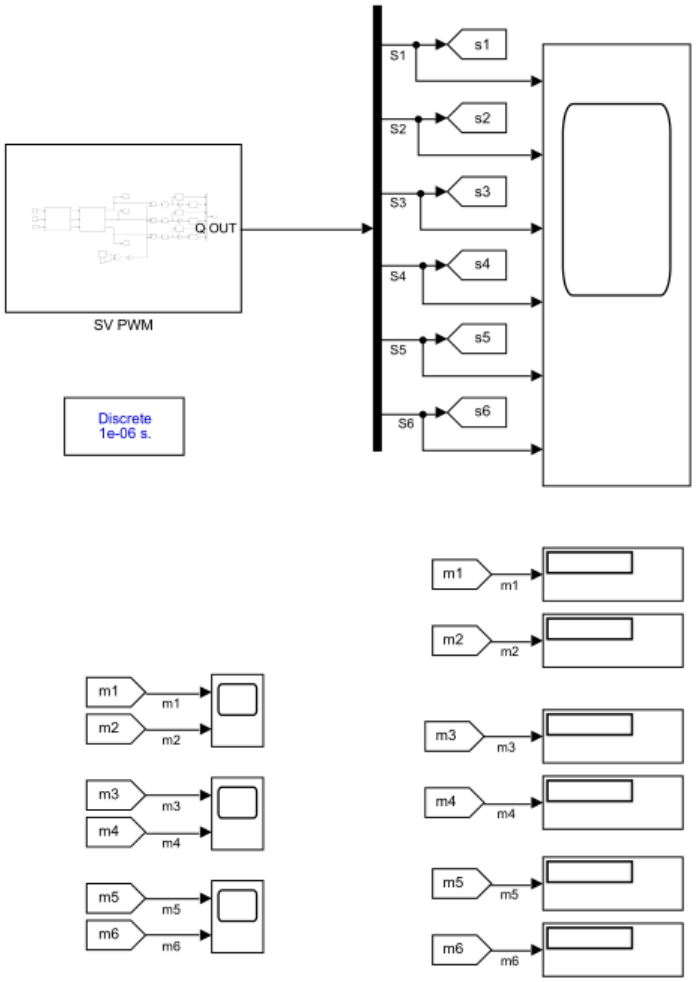


Figure B.6. First section of the SIMULINK model for the evaluation of IGBT losses with Space-Vector PWM.

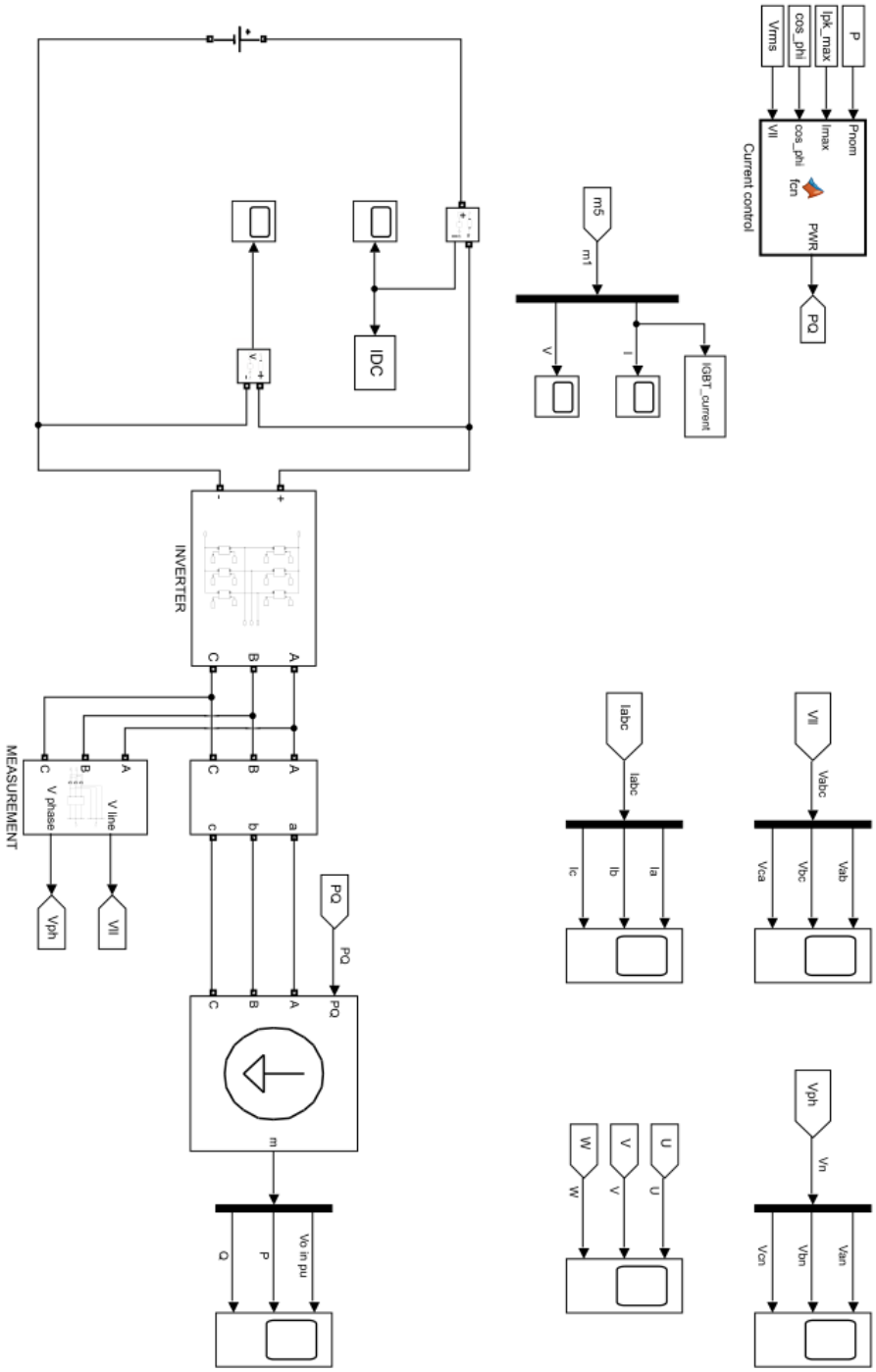


Figure B.7. Second section of the SIMULINK model for the evaluation of IGBT losses with Space-Vector PWM.

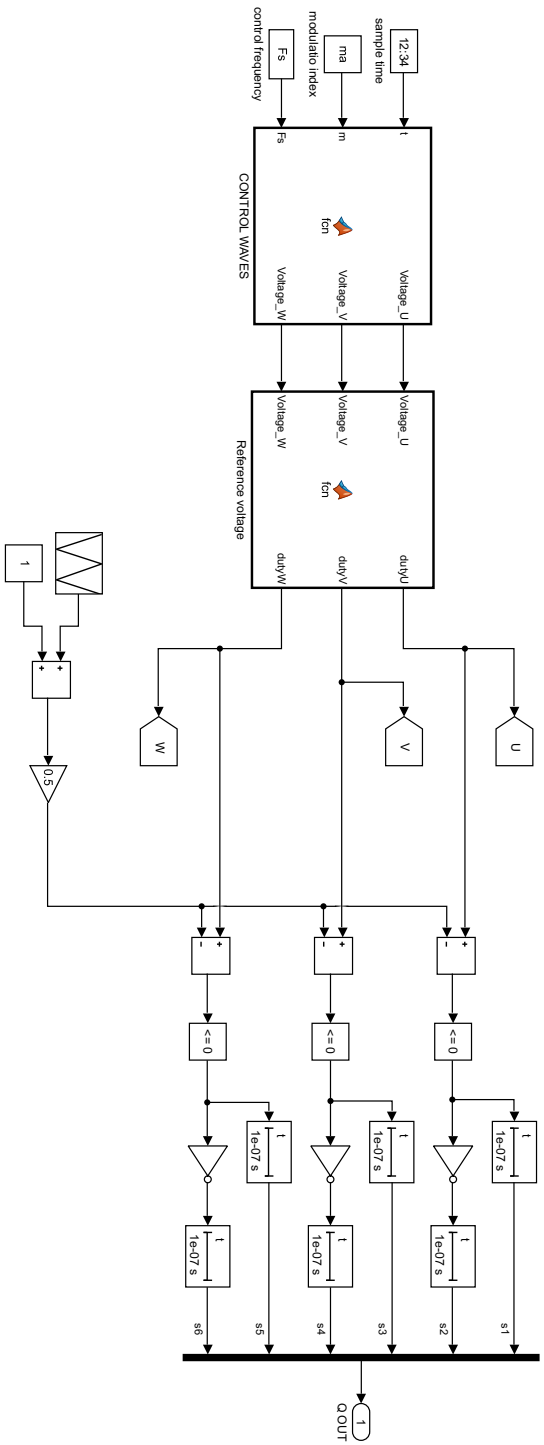


Figure B.8. Subsystem "SV PWM" (Figure B.6) for the generation of the Space-Vector PWM.

B.3 Inverter with power MOSFET and Sinusoidal PWM

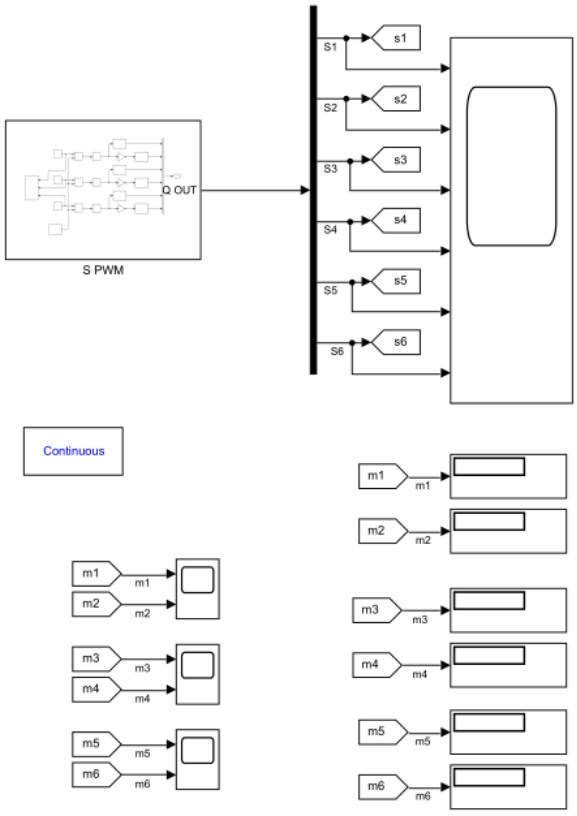


Figure B.9. First section of the SIMULINK model for the evaluation of power MOSFET losses with Sinusoidal PWM.

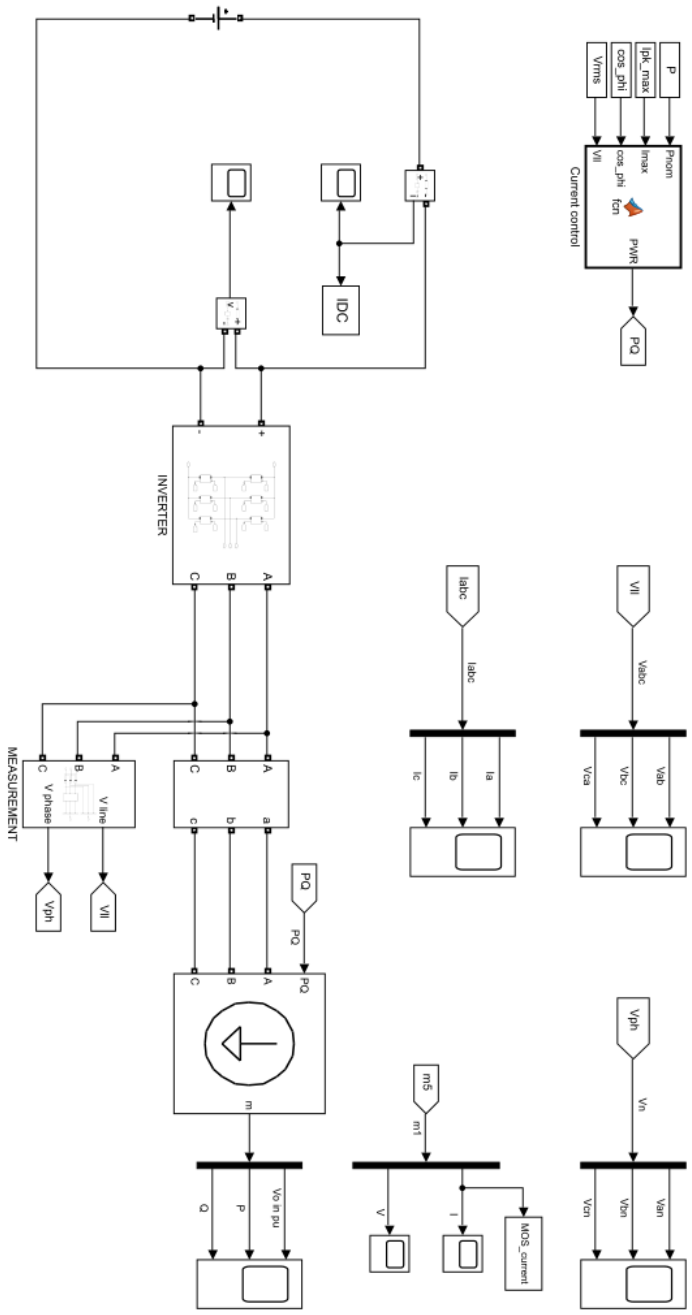


Figure B.10. Second section of the SIMULINK model for the evaluation of power MOSFET losses with Sinusoidal PWM.

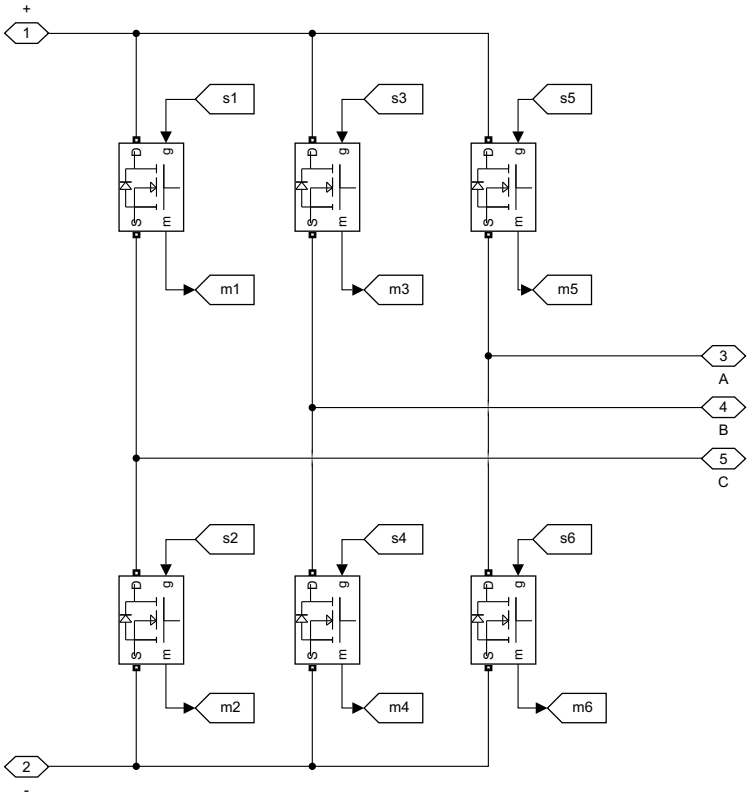


Figure B.11. Subsystem "INVERTER" (Figure B.10) of the three-phase inverter with power MOSFET transistors.

B.4 Inverter with power MOSFET and Space-Vector PWM

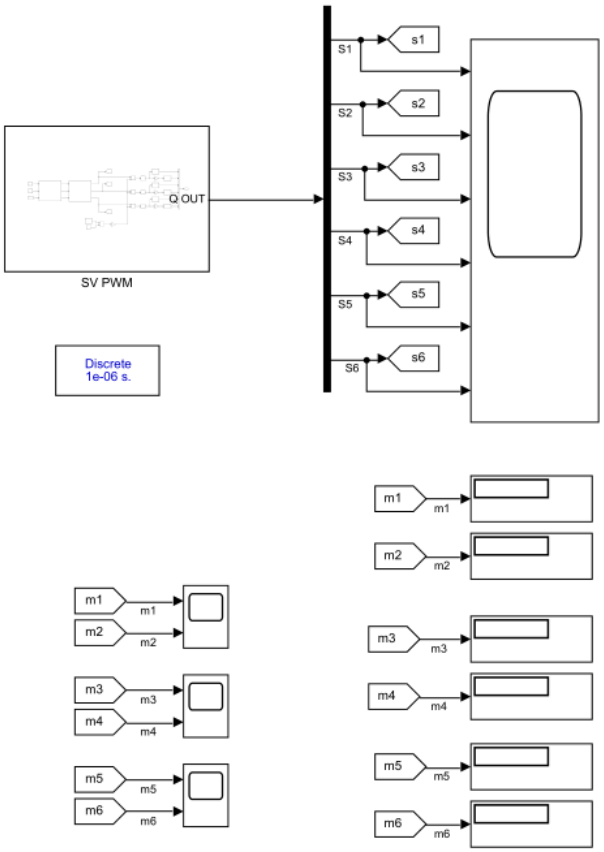


Figure B.12. First section of the SIMULINK model for the evaluation of power MOSFET losses with Space-Vector PWM.

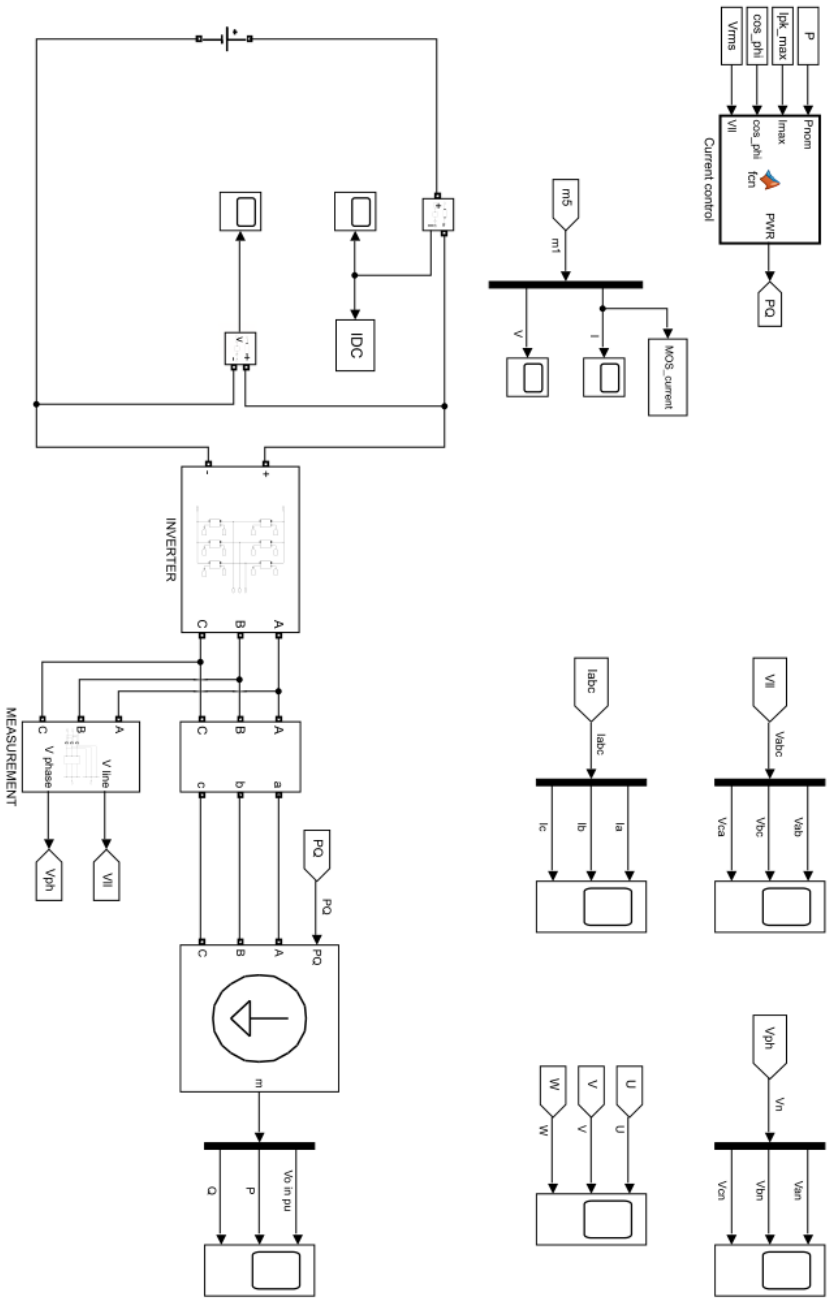
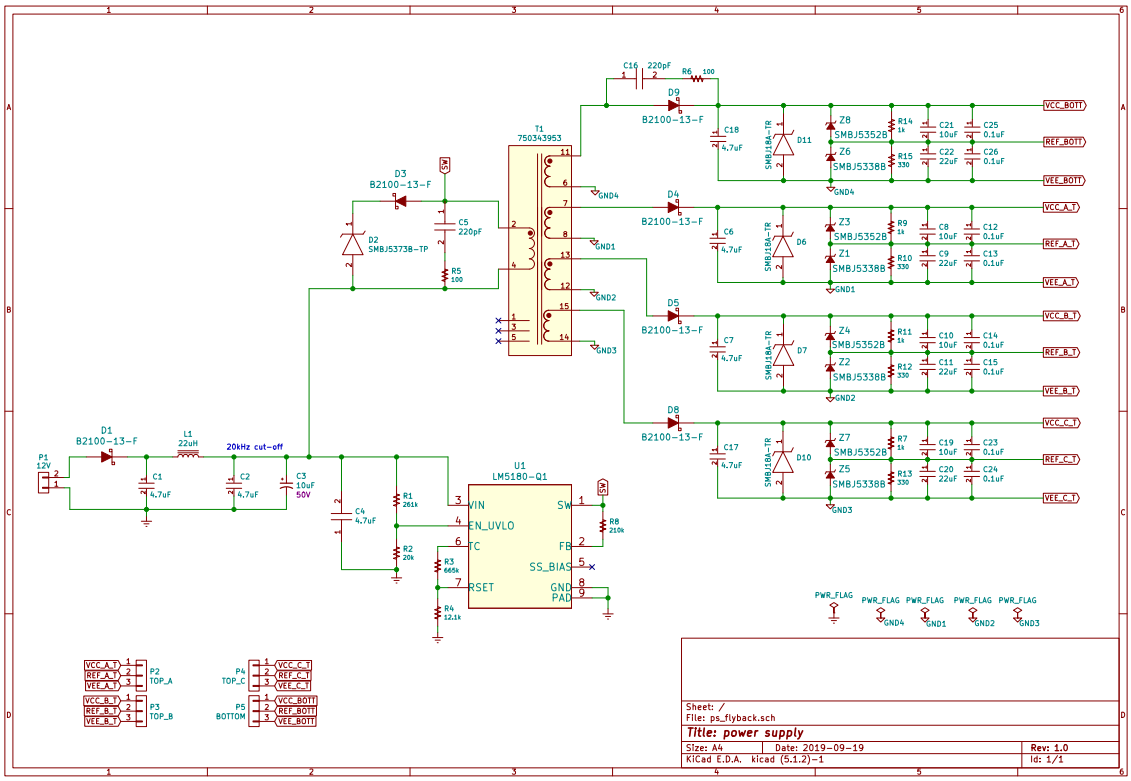


Figure B.13. Second section of the SIMULINK model for the evaluation of power MOSFET losses with Space-Vector PWM.

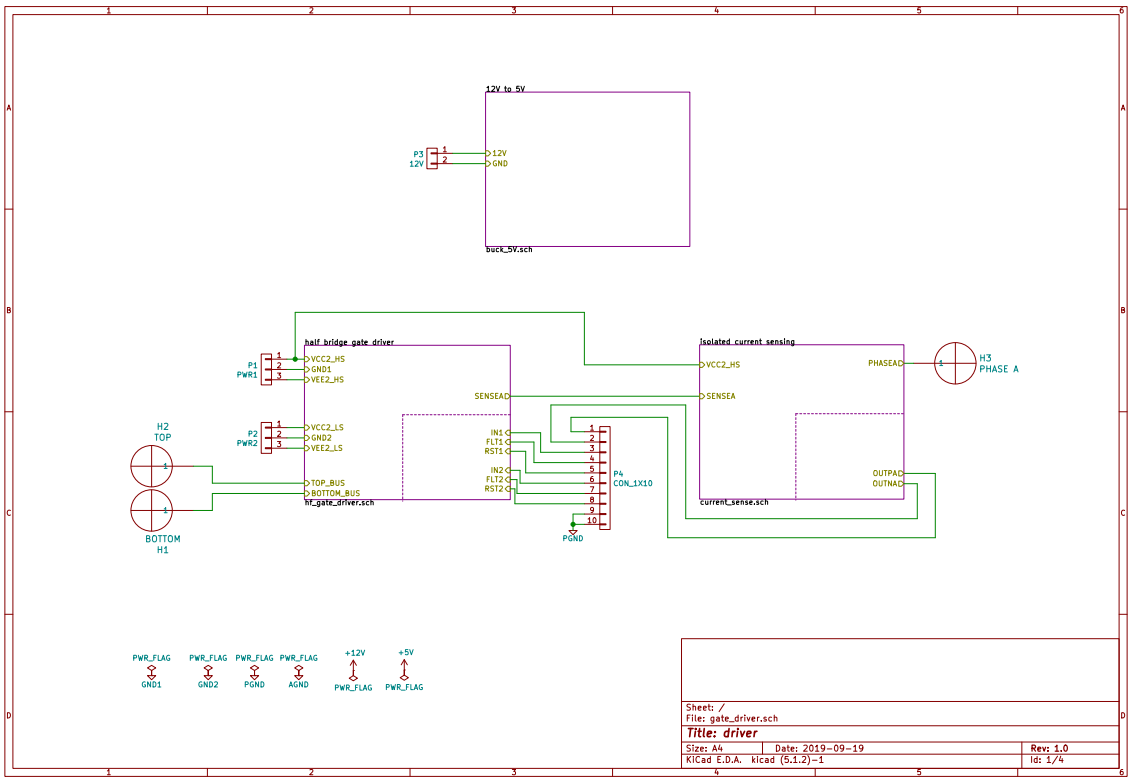
Appendix C

Electric schematic of the prototype

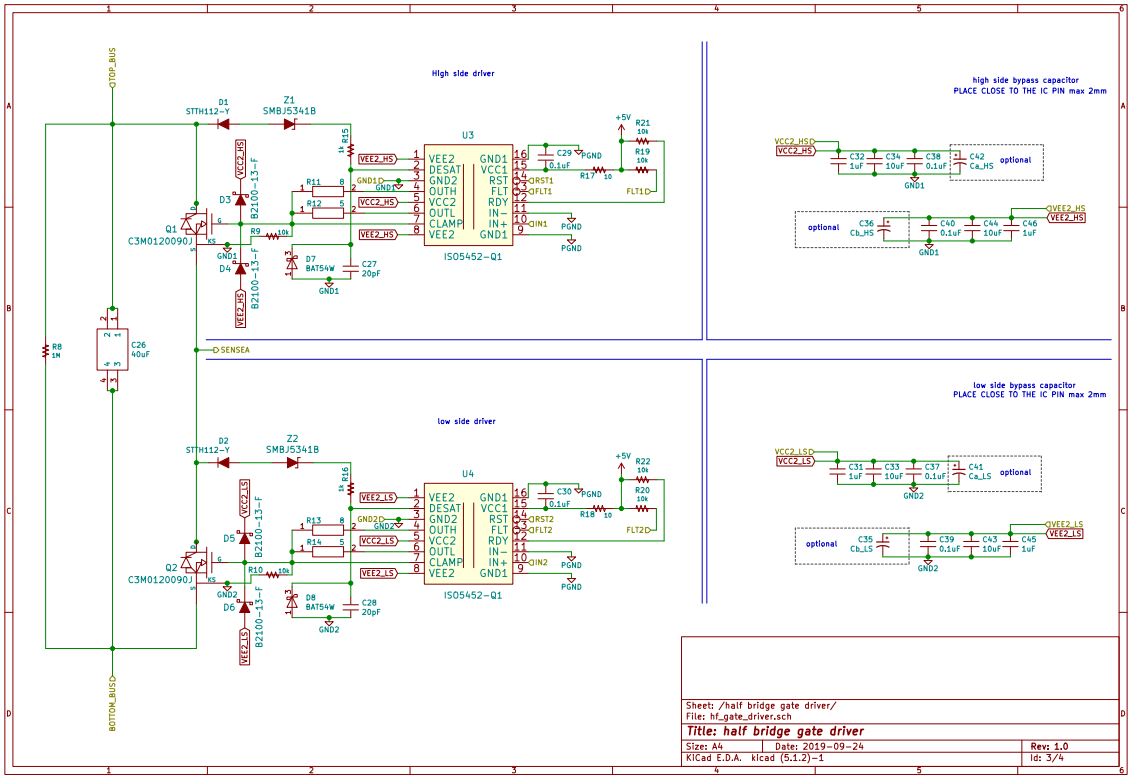
C.1 Flyback power supply



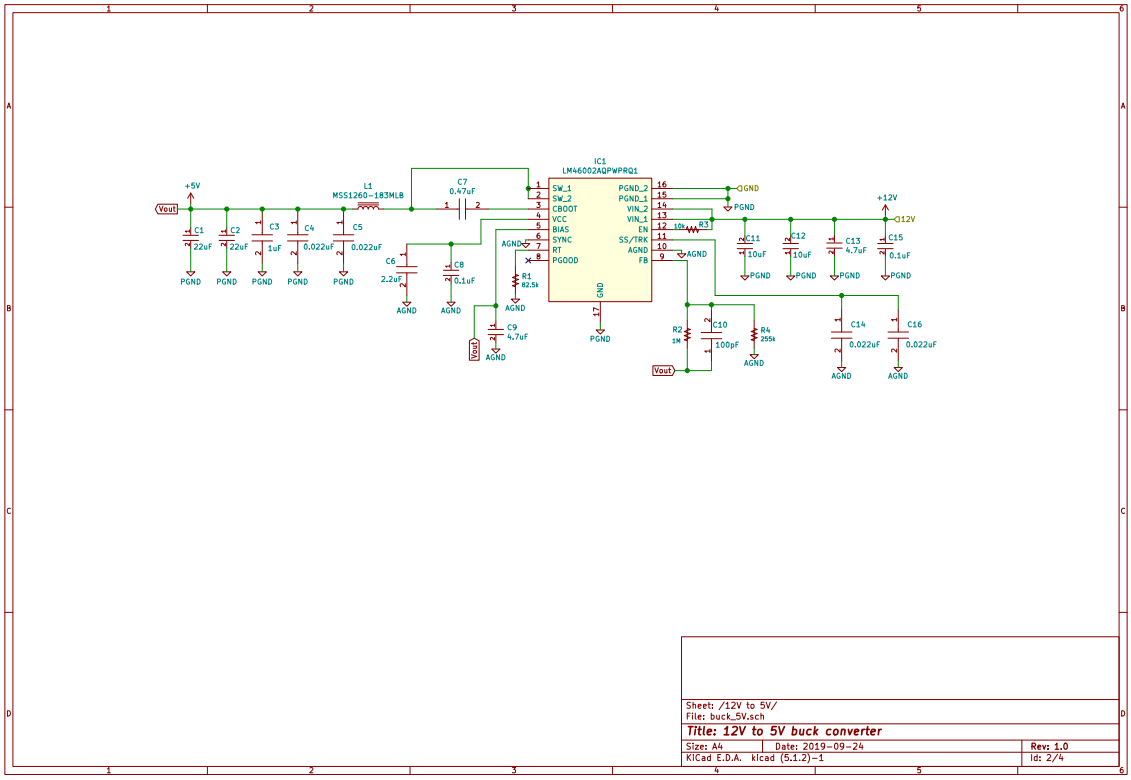
C.2 Blocks of the gate driver board



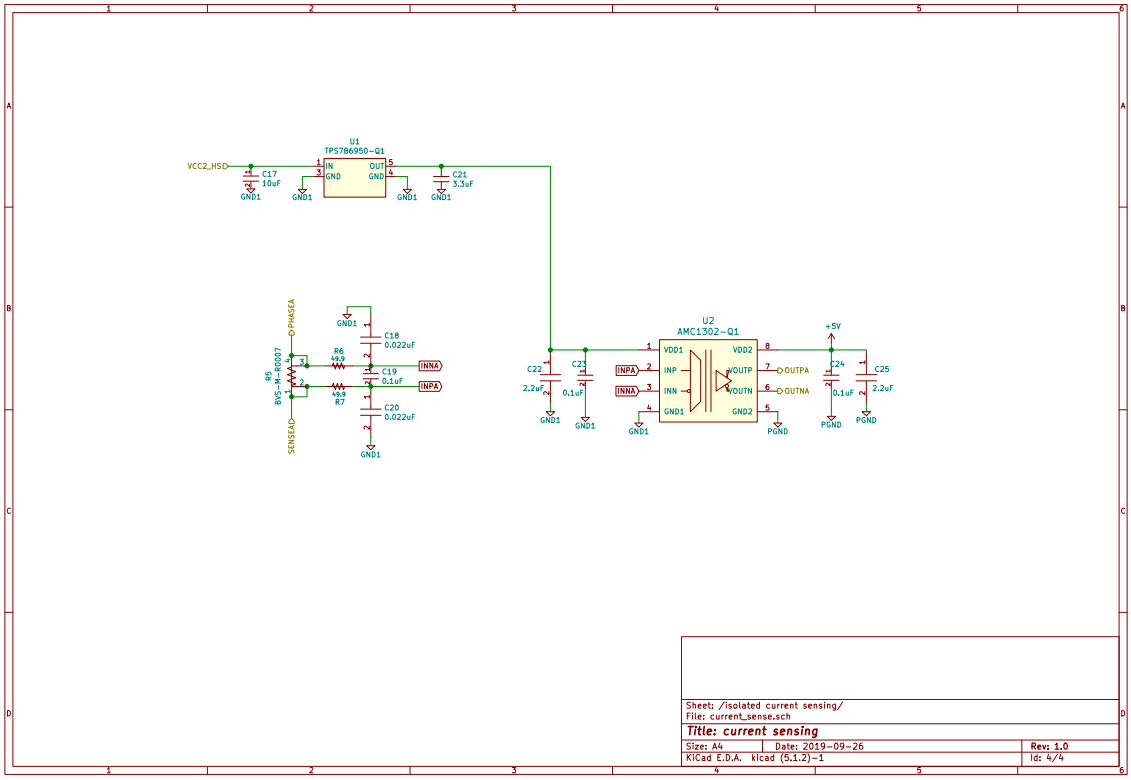
C.3 Gate driver



C.4 12V-to-5V buck converter



C.5 Current sense amplifier and LDO



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