Master of Science in
Nanotechnologies for ICTs

Master Thesis

PZT Process Development for pMUT Actuators

Supervisors:
Prof. Danilo Demarchi
Prof. Carlo Ricciardi

Author:
Vincenzo Pasanisi

External Supervisor:
Dr. David Cheyns

Academic Year 2018/2019

Preface

I would like to thank my IMEC supervisor David Cheyns and mentor Yongbin Jeong, that gave me this fantastic opportunity, followed and helped me in the research work. Another thanks is for my internal supervisors Danilo Demarchi and Carlo Ricciardi, that supported me with all my thesis issues and gave me their greatest willingness. Moreover, I would like to thank the IMEC environment that gave me amazing moments and gratification.
A special thanks go to my family, Rossella and my friends that supported and encouraged me in this important path.

Abstract

The objective of this thesis is a PZT-based process flow development of a piezoelectric Micromachined Ultrasound Transducer (pMUT) for large area applications, and subsequently the characterization of the PZT layer and the entire device.
A brief introduction and a theoretical background is developed in order to have a better understanding of the following experiments (chapter 1 & chapter 2).
A brief lumped element model is explained and the main process flow is discussed, giving a general idea of the steps (chapter 3).
Then, the development of the process is treated (chapter 4), showing some important results related to this exotic ferroelectric material, such as the development of a PZT etching process and a Critical Dimension (CD) of 10 µm for the patterning of it. Moreover, the development of a stable Bosch Process Deep Reactive Ion Etching (DRIE) is tackled and the improvements will be discussed in details. This is the most critical part, being the main cause of the resonance blue shift and small membrane velocity.
Sol-gel and Pulsed Laser Deposition (PLD) PZT are then characterized and compared. Among the PZT Figures of Merit (FoM), the remanent polarization, fatigue, working voltage, breakdown voltage and uniformity are treated. Moreover, an analysis of top electrode material is performed, and a final Ti/Al/Ti top electrode is chosen for the superior remanent polarization ($25\,\mu C/cm^2$), fatigue (nice signal up to 100 hysteresis cycles) and breakdown properties ($60\,V\,\mu m^{-1}$).
Afterwards, the fabricated pMUT device is measured, and a resonant frequency of 1.35 MHz is obtained for a 1 µm thick membrane with 1 mm diameter. In order to verify this resonance, Laser Doppler Velocimetry (LDV), impedance and capacitive (LCR) measurements are performed (chapter 5). The reasons of this large resonance are finally discussed.

Contents

List of Symbols

PZT = Lead Zirconate Titanate
MEMS = Micro Electro-Mechanical Systems
pMUT = piezoelectric Micromachined Ultrasound Transducer
cMUT = capacitive Micromachined Ultrasound Transducer
CMOS = Complementary Metal-Oxide Semiconductor
TFT = Thin Film Transistor
FoM = Figure of Merit
PLD = Pulsed Laser Deposition
CD = Critical Dimension
ECR = Electron Cyclotron Resonance
ICP = Induced Coupled Plasma
RIE = Reactive Ion Etching
DRIE = Deep Reactive Ion Etching
ALD = Atomic Layer Deposition
TMA = Trimethylaluminium
DUT = Device Under Test
PMU = Pulse Module Unit
LDV = Laser Doppler Velocimetry
LCR = Inductance, Capacitance, Resistance
T_C = Curie Temperature
Pr = Remanent Polarization
Ps = Saturation Polarization
E_C = Coercive Field
ER = Etch Rate
ET = Etch Time
φ_{TA} = Tilting Angle at zero applied field
$V_{90\%}$ = Working Voltage
V_{BD} = Breakdown Voltage

List of Figures

List of Tables

Chapter 1

Introduction

Nowadays, microtechnologies are more and more present in our life. The need of integration brings science and engineering to develop new concept for electronic devices. In this perspective, the electronic industry is moving to new aspects of human-machine interaction, such as haptic feedback, that opens up the possibility to feel the screen of our smartphone with the fingers, gesture recognition, in order to understand where the objects are placed, enabling the autonomous drive, or medical imaging, to improve the monitoring and detection techniques for our body and our health.
In this context, the ultrasound waves (from 20 kHz to 10 MHz for these applications) are the optimal way to actuate and sense. The traditional way to work with ultrasound waves was exploiting the bulk piezoelectric transducer, but in the past two decades the Micromachined Ultrasound Transducer (MUT) became more and more important, especially for the higher integration, easier manufacturing, CMOS compatibility, impedance matching, wide bandwidth and high coupling coefficient [1].

The MUTs have two main mechanisms of operation: the piezoelectric (pMUT) and the capacitive (cMUT) actuation and sensing [2]. Both devices are related to the Micro Electro-Mechanical Systems (MEMS) technology. These two mechanisms exploit the flexural properties of a thin suspended membrane to convert electrical energy in mechanical one and vice versa. This membrane must be engineered in order to work in the ultrasound range. The design parameters are several, such as membrane thickness and diameter, Young Modulus, density and Poisson ratio of the employed materials, just to mention a few.

The pMUT exploits the piezoelectric effect of the active material between the bottom and top electrodes, hence a voltage will generate a strain in the membrane and vice versa. With an AC voltage the membrane can vibrate, generating ultrasound waves, while acquiring ultrasound waves from external sources, an AC voltage can be read between the top and bottom electrodes. On the other hand, the cMUT utilizes the charge between two plates, one that is the membrane and the other that is a fixed one. Between the membrane and the fixed electrode an air gap is left, thus the membrane can oscillate and generate ultrasound waves with an applied AC voltage or can collect the ultrasound waves from external sources and detect them reading the AC voltage between the membrane and the fixed electrode. In order to have charge on the two electrodes, a DC voltage is necessary.

In this work the pMUT transducer, with Lead Zirconate Titanate (PZT) as active piezoelectric material, is adopted for large area applications. The main reasons of this choice are the usage of only AC signal with respect to the cMUTs, which requires a DC voltage to have charge on the plates. Moreover, the pMUTs have an higher capacitance with respect to the cMUTs, thus a lower impedance, therefore it is easier to match the device with the actuate/sense external systems [1].
On the other hand, the pMUTs have some drawbacks, linked mainly to the active piezoelectric material. In fact, the PZT contains lead, that is incompatible with CMOS technologies. Moreover, the fabrication of these active materials is not well developed and losses are present, therefore a small coupling coefficient between the electrical and mechanical energies is present, while in the cMUTs could reach almost 100%.
Regarding the incompatibility issue, it is solved employing Thin Film Transistor (TFT) technology to actuate/sense the pMUTs, that allows the integration of PZT structures with the transistors. Moreover, the TFT technology leads to a large area production and flexible electronics, that are the final integration goals of the device application, even if the charge mobility is 2-3 orders of magnitude less than CMOS technology [3]. On the other hand, to increase the coupling coefficient, improvement of process flow and development must be performed.

In order to exploit the high integration of MEMS technology, the single pMUT devices will be then placed in an array. In this way, the waves can be focused with a difference of phase among each single pMUT, hence a boost

signal can be generated. Moreover, the actuation and sensing parts can be divided inside the array zones, creating dedicated and improved sections for each need. Evidently, the smaller the device size is, the better the pixel control will be. The array part will not be covered in this work.

The main part of this thesis is focused on the single pMUT actuator process and characterization, in order to understand the potentialities of the PZT membrane, as well as the related issues and weaknesses.

Chapter 2

Theoretical Background

2.1 Piezoelectricity

2.1.1 Phenomenon

The heart of the pMUT is surely the piezoelectric material.
Piezoelectricity is the ability to generate strain in the crystal when a voltage is applied (direct piezoelectric effect) or to generate electric charge at the ends of the crystal, and thus voltage, when a strain is present (converse piezoelectric effect) [4]. In Figure 2.1 is shown this phenomenon.

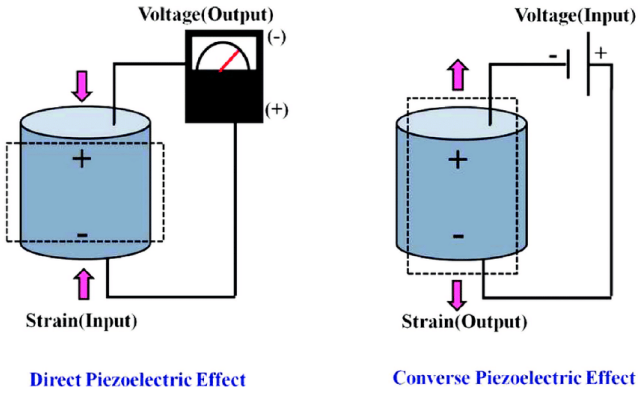


Figure 2.1: Direct and converse piezoelectric effect [4].

In order to see this effect, the crystal must have dipoles. These dipoles

are formed by a net positive and negative charges, thus the distance between these two charges can change. Therefore, during an applied tensile/compressive strain or voltage, a difference of potential or a strain can be present between the terminal sides of the layer, respectively. These dipoles are formed by an asymmetry of charge in the lattice structure, as one could see in Figure 2.2.

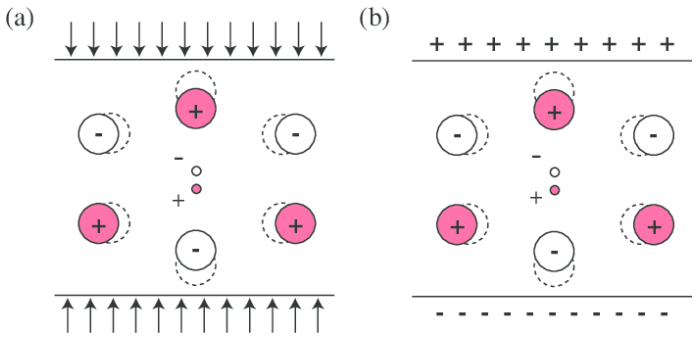


Figure 2.2: Crystal deformation with converse (a) and direct (b) piezoelectric effect. In the first case, the positive and negative charges are moved by an applied strain, hence a voltage appears at the ends of the crystal due to the different distance of the charges. In the second case, the charges are displaced by an applied voltage, thus the crystal changes the dimension due to the attraction/repulsion of the dipole ends [5].

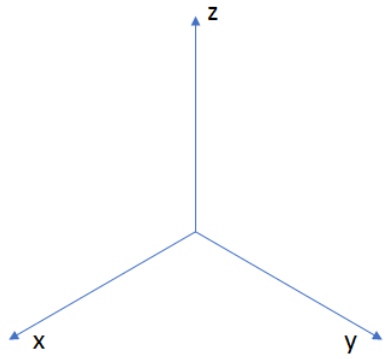
2.1.2 Mathematical Model

The piezoelectric effect can be expressed, mathematically, employing the piezoelectric coefficients, that link the strain to the electric field or vice versa. With a three-dimensional material, these coefficients can be collected in a tensor, which describes all the possible combinations of strain and field.
The electromechanical equations of the piezoelectric material could be written as [6]:

$$S_i = s_{ij}^E T_j + d_{ik} E_k \tag{2.1}$$

$$D_m = d_{mj} T_j + \varepsilon_{mk}^T E_k \tag{2.2}$$

Where S is the strain vector, s^E is the matrix of compliance coefficients at constant electric field, T is the stress vector, d is matrix of piezoelectric strain constants, E is the vector of applied electric field, D is the vector of electric displacement and ε^T is the permittivity at constant stress [2].
The indexes i,j = 1,2,3,4,5,6 and m,k = 1,2,3 refer to the coordinates of the material, as shown in Figure 2.3.
As one can see in Equation 2.1, the strain is related not only to the stress through the compliance coefficients, but also to the electric field, through the piezoelectric strain constants. The same relationship is present with the electrical displacement in Equation 2.2, where the latter is linked to the electric field and applied stress.



Number	Axis
1	x
2	y
3	z
4	Shear around x
5	Shear around y
6	Shear around z

Figure 2.3: Coordinates of the piezoelectric material with legend.

The representation of Equation 2.1 and Equation 2.2 in matrix form can be made explicit through:

$$\begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ S_5 \\ S_6 \end{bmatrix} = \begin{bmatrix} s_{11}^E & s_{12}^E & s_{13}^E & s_{14}^E & s_{15}^E & s_{16}^E \\ s_{21}^E & s_{22}^E & s_{23}^E & s_{24}^E & s_{25}^E & s_{26}^E \\ s_{31}^E & s_{32}^E & s_{33}^E & s_{34}^E & s_{35}^E & s_{36}^E \\ s_{41}^E & s_{42}^E & s_{43}^E & s_{44}^E & s_{45}^E & s_{46}^E \\ s_{51}^E & s_{52}^E & s_{53}^E & s_{54}^E & s_{55}^E & s_{56}^E \\ s_{61}^E & s_{62}^E & s_{63}^E & s_{64}^E & s_{65}^E & s_{66}^E \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} + \begin{bmatrix} d_{11} & d_{12} & d_{13} \\ d_{21} & d_{22} & d_{23} \\ d_{31} & d_{32} & d_{33} \\ d_{41} & d_{42} & d_{43} \\ d_{51} & d_{52} & d_{53} \\ d_{61} & d_{62} & d_{63} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \quad (2.3)$$

$$\begin{bmatrix} D_1 \\ D_2 \\ D_3 \end{bmatrix} = \begin{bmatrix} d_{11} & d_{12} & d_{13} & d_{14} & d_{15} & d_{16} \\ d_{21} & d_{22} & d_{23} & d_{24} & d_{25} & d_{26} \\ d_{31} & d_{32} & d_{33} & d_{34} & d_{35} & d_{36} \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} + \begin{bmatrix} \varepsilon_{11}^T & \varepsilon_{12}^T & \varepsilon_{13}^T \\ \varepsilon_{21}^T & \varepsilon_{22}^T & \varepsilon_{23}^T \\ \varepsilon_{31}^T & \varepsilon_{32}^T & \varepsilon_{33}^T \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \quad (2.4)$$

Another important parameter to estimate the piezoelectric quality is the coupling factor k. Taking the converse piezoelectric effect into account, one could write it as:

$$k^2 = \frac{E_{MC}}{E_{EI}} \quad (2.5)$$

Or, equivalently, employing the direct piezoelectric effect:

$$k^2 = \frac{E_{EC}}{E_{MI}} \quad (2.6)$$

Where E_{MC} is the converted mechanical energy, E_{EI} is the input electrical energy, E_{EC} is the converted electrical energy and E_{MI} is the input mechanical energy. As one could see, the higher the coupling factor is, the better the performances of piezoelectric material are. In fact, k indicates the effectiveness of conversion of electrical energy into mechanical energy or vice versa.

2.1.3 Challenges

Piezoelectric materials have numerous advantages in terms of applications, but one must face with some challenges [7].
First off, the deposition of these materials often requires seed layers to start the correct growth. These layers increase the processing difficulty, because the stack will become more complex and the presence of stress among the layers deteriorates the piezoelectric performances.
Other problems are related to the etching, that is usually slow and not always perfectly controllable.

There are different piezoelectric materials, like Quartz and AlN, and they are

evaluated by the piezoelectric coefficients and coupling factor. For pMUTs actuators, the aim is to exploit the best coefficients, having a huge transduction ratio, especially the d_{33} and d_{31}, related to the strain parallel and perpendicular to the applied field, respectively.

2.2 Ferroelectricity

2.2.1 Phenomenon

When high piezoelectric coefficients are required, the ferroelectric materials must be employed.
Ferroelectricity is the property of some materials of having a spontaneous electric polarization, that could be reversed applying an opposite electric field. It is a subset of piezoelectricity: all the ferroelectric materials are piezoelectric but not all the piezoelectric materials are ferroelectric.
More and more ferroelectric materials become being employed in the electronic area, due to particular superior properties with respect to the piezoelectric ones. In fact, the advantage of ferroelectric materials is the possibility to control the electric dipoles and thus align them. This alignment increases the piezoelectric coefficients because during an applied strain or electric field more dipoles respond with the same direction.

2.2.2 Curie Temperature

The electric dipoles in the ferroelectric materials are present only if the temperature is low enough. Indeed, the asymmetry of charge in the lattice cell is created only under a certain temperature, called Curie Temperature (T_C). Above this temperature, there is no more net positive and negative charge in the lattice cells, therefore the material loses the ferroelectric properties [9]. This is an important issue during the operation of the device, because T_C sets the maximum working temperature.
Morever, if the poling field is applied before the device processing, the development temperature of each step must be lower than T_C, leading to some problems in the integration and process flow.

2.2.3 Hysteresis

The dipoles in the ferroelectric crystal are collected in domains, separated one from the other by domain walls. These domains usually don't have the same orientation, but they could move to follow the applied electric field. On the other hand, the domain walls need energy to move, thus there is an equilibrium between the movement of domain walls and the dipoles alignment with the electric field. The presence of a domain is linked with the formation of positive and negative charges at the domain's ends. These charges create an electric field, called depolarized field (E_d), in the opposite direction with respect to the polarization (P_s), as one could see from Figure 2.4. To minimize the energy associated to this field, the crystal could split in two the domain with opposite polarization, forming a 180° wall if no stress gradient is applied, or 90° wall if the lattice is stress-free.

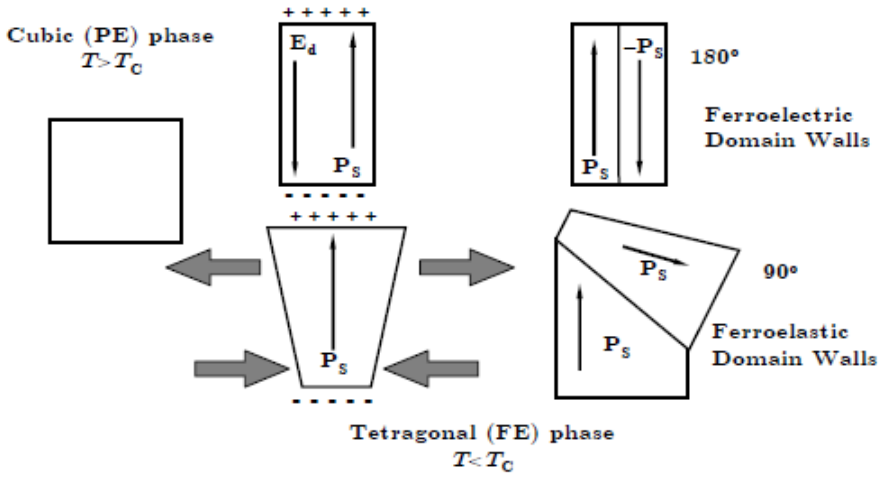


Figure 2.4: Domains in the tetragonal structure of a ferroelectric crystal [8].

Given that, the applied electric field can reverse the spontaneous polarization but the curve has an hysteretic behaviour, as one could see from Figure 2.5.

Starting from the central point of the graph, the material has no polarization, with random-oriented electric dipoles. In fact, first of all, the material must be polarized applying a strong electric field. After the poling step the saturation (P_{sat}) is reached. At this point the electric dipoles in the material

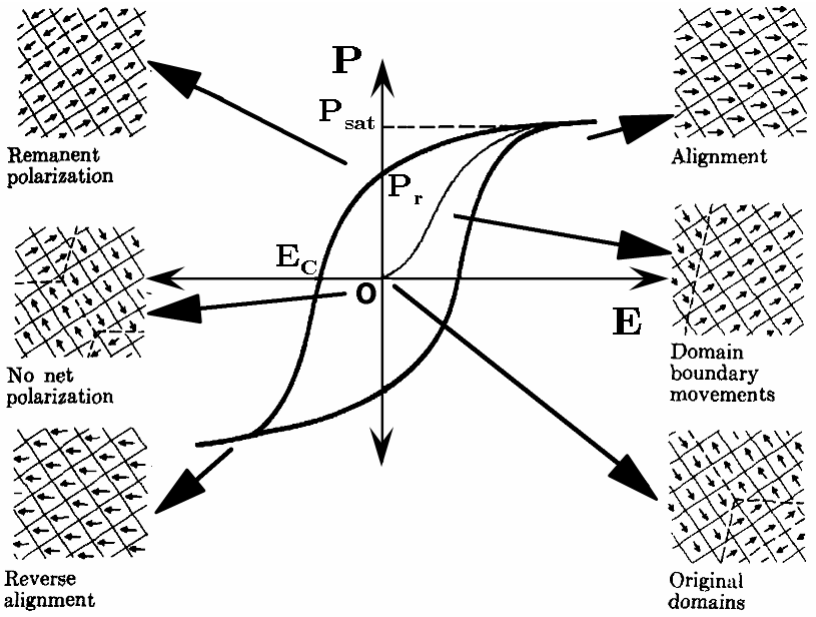


Figure 2.5: Hysteresis plot of a generic ferroelectric material [9]. The main parameters of the hysteresis are shown, like P_{sat}, P_r and E_C.

are mostly aligned with the applied field. Turning off the electric field a polarization, called remanent polarization (Pr), is still present. In this case the electric dipoles maintain essentially the same direction achieved at P_{sat}. This is due to the energy of the domain walls that prevent a fully misalignment with respect to the previous applied field. Applying an opposite electric field, the dipoles start to flip toward the other direction, until no polarization is reached. At this point the dipoles are again randomly-oriented, and the electric field at which this happens is called coercive field (E_C). Then, increasing more the electric field, the new saturation is reached and the same procedure can be applied to reach again the opposite sign saturation. Thus, each ferroelectric material has two coercive fields and two remanent polarizations, one positive and one negative. It is worth mentioning the similarity with the ferromagnets. Indeed, the hysteresis loop mechanism is the same, with a magnetic field and magnetic polarization instead of electric field and electric polarization, respectively, and the presence of domain walls that act in the same way.

2.2.4 Fatigue

The ferroelectric fatigue is defined as the reduction of the remanent polarization as a function of the number of switching cycles [10]. There are several mechanisms of fatigue in literature. They are divided in reversible and irreversible types.

First off, it could be due to microcracking [11]. It usually occurs with large tetragonal lattice distortions or near the phase boundaries. In these cases the fatigue is irreversible, due to a large deformation of the grains.

Secondly, electronic charge trapping and domain wall pinning can contribute to fatigue [11]. In fact, according to this model, the free electronic charges can be trapped inside the domain walls, pinning them.
The domain walls could attract the carriers because a discontinuity of polarization is present in these regions. This phenomenon will reduce the energy of the domain walls, leading to a restriction of domain walls motion, with a consequent decrease of remanent polarization.
To this effect, the field-assisted unpinning should be considered, and at the end the effective fatigue is a dynamic balance of pinning and unpinning inside the domain walls.

Another important effect is the presence of oxygen vacancies close to the electrodes [11]. These vacancies could create a n-doped like layer, that will improve the injection of electronic charges inside the material, with the consequence of domain wall pinning. The usage of oxide electrodes can improve this fatigue, because the oxide will act as oxygen source and so the vacancies will be avoided.

The last two effects are reversible. It means that applying an electric field, increasing the temperature above T_C or using UV light the fatigue effects will disappear. It is worth mentioning, anyway, that even if the initial remanent polarization is achieved, the fatigue will be reach faster afterwards, so it is impossible to delete the whole degradation effect.

2.2.5 Figures of Merit

The Pr and E_C are employed to estimate the quality of the ferroelectric material. In fact, one should exploit a low E_C, in order to switch the polarization with small energy consumption, but a high Pr, because it is linked with the dipole's orientation and so with the piezoelectric coefficients.
Another important Figure of Merit (FoM) is the loop area or, put differently, the integral of the polarization with respect to the applied field. This figure of merit is an energy, and it describes the energy consumption for each cycle. It is worth having this area small, in order to save energy, especially if multiple switching are needed. This is very important for the memories, but in pMUT technology the poling is needed at the beginning, and then few other cycles are employed to maintain the polarization to the same value. In fact, after some time, the dipoles start to move in order to have a random configuration, and a restoring pulse is then needed.

2.2.6 Challenges

The main drawback of ferroelectric materials is the complexity of the compound: there are no ferroelectric materials in single crystal form, like piezoelectric ones. Moreover, most of the cleanrooms see the introduction of ferroelectric materials as a challenge, because they are usually new materials and they are not allowed in etching/deposition tools for the presence of CMOS contaminants, like lead or others. Thus, these materials need dedicated tools and chambers to be processed. Fortunately, the growth of interest in ferroelectric memories is increasing the number of labs in which the processing of these new materials is permitted.

As for piezoelectrity, there are different ferroelectric materials, like Lead Zirconate Titanate (PZT) or PVDF. The right material's choice is dictated by the application requirements.

2.3 PZT

2.3.1 Structure and Composition

Lead Zirconate Titanate (PZT) is an inorganic compound material with unique properties. In particular, it belongs to the class of ceramic perovskite. The perovskite formula can be written as ABO_3 (Figure 2.6), where A is the first cation element, B is the second cation one and O is oxygen. The A cations are placed at the corner of a cubic structure, with the B cations at the body centres and the oxygen at the centre of the faces.

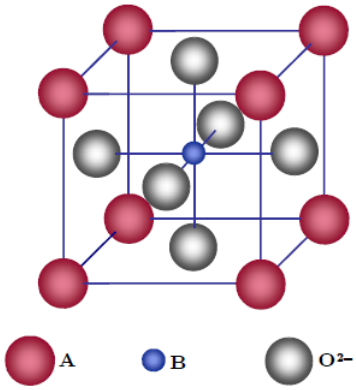


Figure 2.6: Perovskite structure [9].

In the case of PZT, A is Pb and B is a mix of Zr and Ti. The material shows huge piezo and ferroelectric properties. The lattice structure of PZT is shown in Figure 2.7. As one could see, the dipoles are formed only if $T<T_C$, when an asymmetry in the lattice appears. In this case, the central atom of the cell (Ti or Zr) is moved toward one oxygen atom, generating a net positive charge where the atom is moving and a net negative one in the opposite part of the cell, therefore the dipole appears.
It is worth mentioning that this is the ferroelectric tetragonal phase. The same distortion of the atoms is present, but forming a different shape, for other ferroelectric cell structures. Anyway, the net positive and negative charges will appear to form the dipole also for the other cell structures.

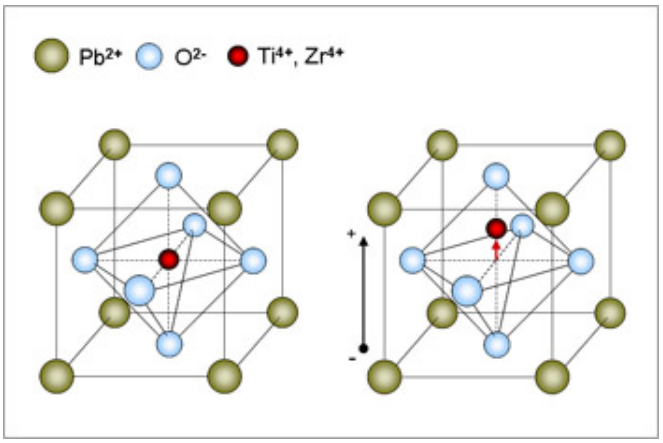


Figure 2.7: Tetragonal lattice structure of PZT under and above T_C [12].

2.3.2 Morphotropic Phase Boundaries

One important feature that characterizes the PZT is the so called morphotropic phase boundaries. In fact, as Figure 2.8 shows, the material is characterized by a variation of phase.

At high content of Zr (left part of the graph), a ferroelectric rhombohedral structure is generated, while at high content of Ti (right part of the graph), a ferroelectric tetragonal structure is formed. Between these two regions, there is a small window (MPC) in which the system has a ferroelectric monoclinical structure. This part is the one with the highest piezoelectric coefficients. Not only the concentration of the Zr and Ti species is important, but also the temperature is a crucial factor. Indeed, as shown in Figure 2.8, if the temperature is increased, a paraelectric cube structure is obtained, without spontaneous dipoles. Thus, depending on the concentration of the species, one could discover the T_C of the material. The PZT is one of the materials with the highest T_C ever measured.

Usually, a good trade off between high T_C and excellent piezoelectric properties is chosen, being able to employ high T processes and having a great material response with external stimuli.

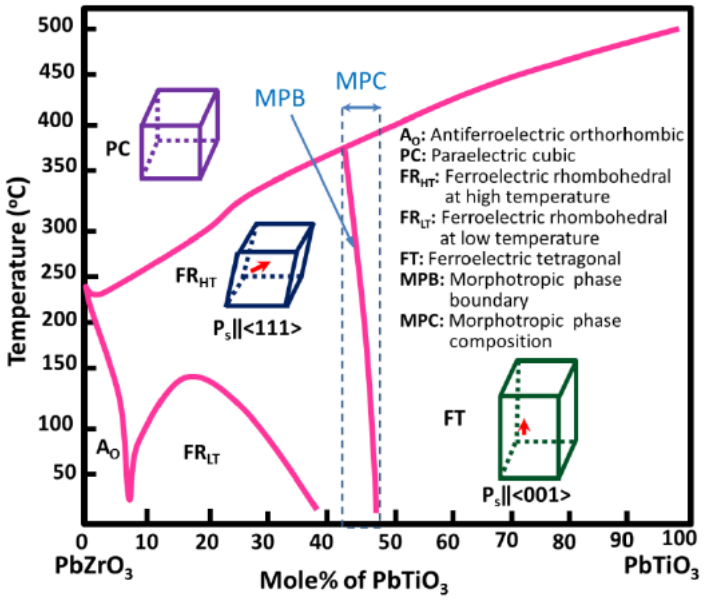


Figure 2.8: Phase diagram of PZT varying the temperature and the content of Zr and Ti [13]. Different paraelectric and ferroelectric zones are present changing these parameters.

2.3.3 Soft and Hard PZT

The addition of dopants in the PZT structure may cause properties' variation. Given that PZT has a perovskite lattice, the atoms can substitute mostly A or B sites (reminding the chemical formula ABO_3). For each kind of sites, one can distinguish three main types of dopants [9]:

- Donor dopants
- Acceptor dopants
- Isovalent dopants

The first category is the donor doping. This kind of additives is also known as soft dopant. These dopants have an higher valence number than the lattice's atoms. One could find La^{3+}, Nd^{3+}, Bi^{3+} or Sb^{3+} in the place of Pb^{2+} and Sb^{5+}, Ta^{5+}, Nb^{5+} or W^{6+} in the place of Ti^{4+} or Zr^{4+}. The main effects of this doping is the increase of piezoelectric coupling coefficient, resistivity and relative permittivity.

To explain these changings, one must see the atom movements after the addition of dopants. Given that the valence of the dopants is larger than the atoms in A, B sites of PZT, the lattice will get a net negative charge. In order to make the lattice neutral, Pb vacancies are created. These vacancies facilitate the movement of atoms and thus the domain walls can move easier in the crystal. This easier movement of the domain walls is linked with a reduction of the coercive field.

The second category is the acceptor doping, know as hard dopants. In this case the valence number is smaller than Pb, Ti and Zr atoms. Thus, Pb^{2+} is substituted by Na^{+} or K^{+} and Ti^{4+} or Zr^{4+} by Fe^{2+}, Fe^{3+}, Mn^{2+}, Mn^{3+}, Al^{3+} or Ga^{3+}. In this case there is a lowering of relative permittivity and, therefore, lowering of dielectric loss and higher quality factor. Moreover, the coercive field increases. The reason behind these effects are linked with the oxygen vacancies. In fact, when the atoms of the lattice are substituted by the hard dopants, oxygen vacancies appears in order to ensure the electroneutrality of the crystal. The acceptor atoms could form dipoles with the oxygen vacancies, that prevent the movement of domain walls in the structure.
The difference between a soft and hard doping hysteresis is shown in Figure 2.9.

The last category is the isovalent doping. These additives have the same valence number of the atoms in the lattice. One could find Ba^{2+} or Sr^{2+} for Pb^{2+} and Sn^{4+} for Ti^{4+} or Zr^{4+}. The effects of these additives are the reduction of the Curie temperature and the increase of the relative permittivity.

2.3.4 Growth and Deposition

The particular stochiometry of PZT makes it a difficult material to grow or deposit. Among the different way, Sol-gel and Sputtering techniques are the most well-known and promising [14].

The Sol-gel technique is an easy and not expensive way to fabricate PZT. The idea is to coat the PZT solution, a mixture of precursors and agents, dipping or spinning the wafer. Then, the wafer is sintered, increasing the temperature from 600°C to 700°C. In this way, the PZT will be crystallized and the solvent will be released. This step could be repeated more times in

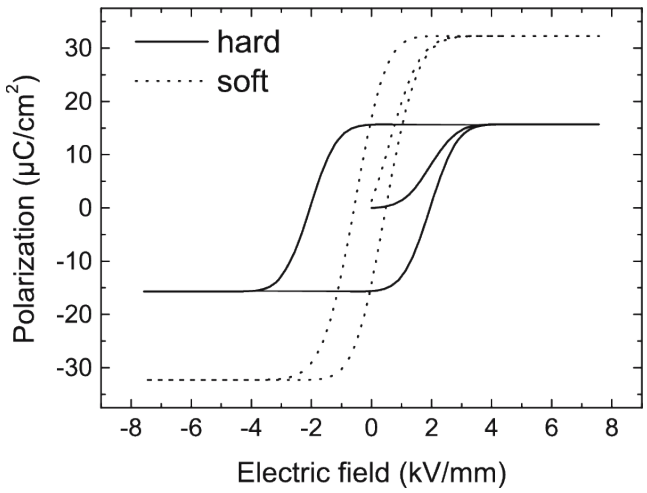


Figure 2.9: Soft and hard hysteresis comparison [15].

order to obtain the required PZT thickness.
This is a very inexpensive technique, because the complete reusability of the precursors, and the stochiometry can be precisely controlled. One can control the PZT crystal quality modifying the sintering temperature. The higher is this temperature, the better are the PZT performances and the crystal size. But the increase of temperature causes some negative side effects, such as loss of PbO from PZT due to the high volatility, the electrode degradation due to the instability of metals in this temperature range or the delamination of PZT due to thermal stresses in the layer. Thus, a trade-off between temperature and features must be found.
It is worth noticing that the Sol-gel method needs a seed layer, like a metal or LNO ($LaNiO_3$), in order to obtain the correct crystal quality.
The Sputtering technique is another way to fabricate PZT, especially the so called Pulsed Laser Deposition (PLD), in which a laser will sputter the target. This is a deposition method. The target is a pure mixture of TiO_2, ZrO_2 and an excess of PbO. This excess is needed to tackle the volatility of PbO, especially in sputtering and annealing steps. For simple sputtering, inert gasses, such as Ar, are employed in order to exploit the physical etching of the target. Moreover, given that the target is made of oxides, an RF sputtering is needed, to prevent the charging. In this case, with respect to Sol-gel technique, the control parameters are much more (temperature of the substrate, pressure of the chamber, flux of gasses, RF power/laser power)

and thus the correct stochiometry is obtained more difficulty. On the other side, the PLD PZT can be deposited not only on metals but also on glass and silicon and no DC/RF bias sputtering is required, but only the laser power.

2.3.5 Etching

The etching of PZT is a quite delicate aspect, because the crystalline structure of this material is complex and contaminants (Pb) are present.
Both dry and wet etching are possible with this material, but each one has particular issues.

The main problem of dry etching is related to the availability of dedicated tools. In fact, the presence of Pb in the lattice, contaminates the chamber of etching and no CMOS technology can be developed after. Thus, it is important to have tools that are employed only for PZT.
It is demonstrated [16] that ECR/RF RIE can be employed with a gas atmosphere of 40% of CCl_4, 40% of CF_4 and 20% of Ar.
There are two main problems with RIE:

- Resist selectivity
- Leak of by-products

The first issue is improved with low pressure and low RF bias.
The second one can be solved with high temperature and low pressure, but high T deteriorates the resist selectivity. A solution could be the employment of an hard mask.

Regarding the wet etching, one can avoid the contamination of the tools because the whole etching could be performed in beaker.
It is known [17] that each element of the PZT compound has a different etchant. In general, HCl removes Pb and Ti, while HF works for Ti and Zr. Thus, a mixture of DH_2O:HCl:HF could be employed, in order to perform the etching in one single step. Moreover, this mixture has a very good selectivity with respect to Pt, that is usually the bottom electrode and seed layer.
Usually in the etching process the Pb is the main problem, because it can escape from the lattice easily and could reach the surface creating PbO species. Moreover, it forms PbClF when HCl and HF is present in the solution. This

compound is insoluble and it will be deposited on the bottom of the etching zones. The addition of HNO_3 will remove these particles, acting as:

$$Pb(Ti,Zr)O_3 + H^+ + F^- + Cl^- \rightarrow [TiF_6]^{2-} + [ZrF_6]^{2-} + [PbCl_4]^{2-} + PbClF \downarrow + H_2O \tag{2.7}$$

$$PbClF + HNO_3 \rightarrow PbCl_2 + Pb^{2+} + NO_3^- + HF \tag{2.8}$$

As one can see, the PbClF is dissolved in soluble compounds and easily removed. It is worth mentioning that this kind of solutions should be employed one time only if a stable and uniform etch rate is needed.

2.3.6 Challenges

If on one hand PZT has tremendous performances, on the other one it has some important issues to deal with. First off, it is a relative new material, thus it is difficult to introduce it in the standard fabs. Then, processing challenges must be taken into account due to multiple atoms structure, especially in the pattering. The species in this particularly lattice structure are not allowed in the standard CMOS processing, especially for the Pb, a strong transistor contaminant. Finally, the Pb is a very toxic element and it precludes PZT to be employed in biomedical and implantable applications.

2.4 pMUT Device

2.4.1 Structure

The structure of the device is a thin suspended membrane (sub-micrometric or micrometric dimension) with a top and a bottom electrodes. Between these two electrodes, a piezoelectric layer is deposited, which is the core of the device. Finally, the membrane is built on a substrate, that clamps the device and acts as sustain and acoustic cavity. The gaseous species inside this cavity could change the resonance modes and the performance of the device, thus an accurate study must be performed. This basic structure is shown in Figure 2.10.

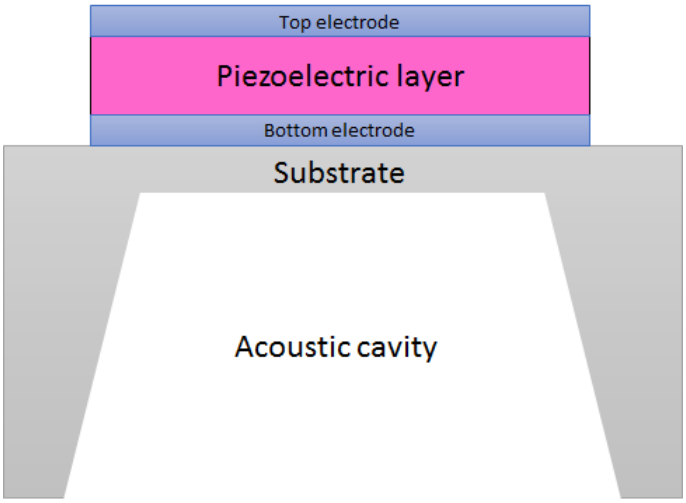


Figure 2.10: Basic structure of a pMUT device.

Sometimes, in order to obtain the correct crystallization of this part, a buffered seed layer such as LNO is deposited, but usually it is not considered in the simulations/design because of the thickness (about 10 nm). Other layers can be deposited on the bottom or top part of the membrane in order to increase the stiffness of the structure and thus the resonant frequency. In order to improve the transmission and reception of the signals toward the medium above the membrane, another layer could be deposited on the top electrode. This layer will match the impedance of the ambient with the one of the device.

2.4.2 Working Principle

The working principle of the device is based on the piezoelectric effect of the core layer. Through the electrodes, the the d_{31} piezoelectric coefficient is exploited, so that the applied field will generate a variation of the strain in the membrane plane, and so a displacement will occur. It is worth highlighting that also the d_{33} coefficient is exploited, but with a lesser part.
If the signal is an AC voltage, the membrane will start to vibrate, and the resonant frequency could be extracted. The resonant frequency depends on different factors, such as material properties, membrane thickness and diameter, type of membrane boundaries and shape of the membrane.

If one supposes that the membrane is composed by only one material and the electrodes' contribution is negligible, the resonant frequency can be written as [18]:

$$f_r = C\sqrt{\frac{Et^3}{\rho a^4(1-\nu^2)}} \tag{2.9}$$

Where C is a constant that depends on the modes, E is the Young Modulus, t is the thickness, ρ is the material density, ν is the Poisson ratio and a is the radius or the side if the membrane is circular or squared, respectively. This model is valid both for a circular and square membrane, and the C coefficients are shape-dependent.

As one could see in the Equation 2.9, among the material properties, the Young Modulus (E) and the Poisson ratio (ν) are the most important.
The first one is the ratio between stress and strain of a material and it represents its stiffness. The larger the E of the membrane is, the larger the resonant frequency is, because the membrane is stiffer.
The second one is the ratio between the deformation in one direction and the deformation in one of the other two directions. A small ν means that the material is less sensitive to lateral deformations when it is compressed or stretched. Thus, to have a large resonant frequency, a small Poisson ratio is required.

It is important to work with these mechanical parameters in order to reach the correct resonant frequency for each specific application.

2.4.3 Integration in the Array

The pMUT devices are then fabricated in order to obtain an array. An idea of the array working principle is shown in Figure 2.11 (Top view), where the rows and columns are controlled by an electronic circuit to read or send the signals. Each device can be driven separately or one rows/columns could be set, in order to have line control instead of pixel control.

The array functionalities could be haptic feedback, medical imaging, gesture recognition, communications or microfluidic actuators, to mention a few. In

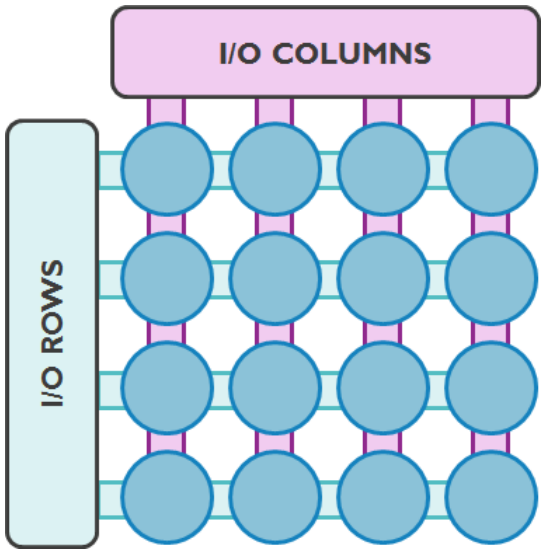


Figure 2.11: 4x4 array structure based on pMUT transducers (Blue circles).

our particular case, focusing on haptic feedback with ultrasound waves, the pMUTs are actuated so that the phase of each device is changed. This will cause the focus of the waves toward a single point or a line, and successively, the ultrasound wave could excite the receptors on the fingers of our hands. With this idea, a reading of the position of objects through an echo effect could be also performed, both to recognize the spaces and to take images of our body.
Moreover, it is possible to create dedicated section of the array, in order to sense and actuate with the best performances.
The readout circuit is designed and fabricated employing the Thin Film Transistor (TFT) technique. That is because the application is thought for large glass area wafers, thus standard CMOS technique is not suitable.

It is worth mentioning that the array is the next step of this thesis work, that is fully focused on the single pMUT actuator.

Chapter 3

Design & Process Flow

3.1 Introduction

In this chapter the design of the pMUT transducer and the related process flow are explained. These two aspects of the MEMS concept are strictly linked together: the design should be feasible in terms of processing, while the processing should exploit innovative mechanisms to fulfill the design goals.

In this general picture, I was in charge of developing the processing part only, given the complexity of the project. The design was performed by the electronic group, from which I extracted the main reasons and goals. It is worth noticing that the process flow was changed different times in order to reach the operation features of the designed model, given that the reality and the concept are always different, and the fabrication issues are usually other sources of failing. Nevertheless, the final process will be described in this chapter.

3.2 Design

3.2.1 General Concept

The general concept of the design could be split in two: device's design and system's design.
The first one is related to the single pMUT. Shape, layer thicknesses and

material properties are the main design parameters.
The second one is related to the array of pMUT, that must be integrated in large area application to exploit the ultrasound wave focusing for haptic feedback or monitoring.

As one could imagine, these two design aspects are very interconnected together, because the single device must be developed in the perspective of the array application and the array itself is a matrix collection of single pMUTs. Thus, the data collected from one field are employed to enhance the performance of the other field and vice versa.

In this general view, the process and integration engineering works in order to give useful parameters and ideas to improve the design part.
In the following part we will discuss in particular the pMUT lumped element model, whose objects will be strictly interconnected with the processing part.

3.2.2 Device Modeling

The lumped element model is a analog representation of the system under analysis. Usually, this scheme is easier to understand and to deal with, especially from the electronic point of view. In Figure 3.1 the lumped element model of a pMUT is shown [19]. As one could appreciate from the scheme, there are two main parts, the electrical and the mechanical ones, that are linked together through a transformer, which converts the electrical energy in mechanical one and vice versa. This transformer is strictly linked with the piezoelectric properties of the active material such as the coupling factor k (look Equation 2.5 and Equation 2.6 in subsection 2.1.2). Moreover, in the case of the actuator, a signal must be sent to the electrical part in order to exploit the piezoelectric effect, so a generator is placed to describe the AC voltage signal from the outside. Measuring the input current (I_{IN}) and calculating the ratio of V_{IN} and I_{IN}, the impedance magnitude and phase can be obtained.

Starting the discussion from the electrical part, one can notice the capacitor C_E and the resistor R_E. C_E is the one formed by the PZT, between the top and bottom electrodes. This is the element that will resonate with the mechanical part and will give the anti-resonance peak. Even if a great

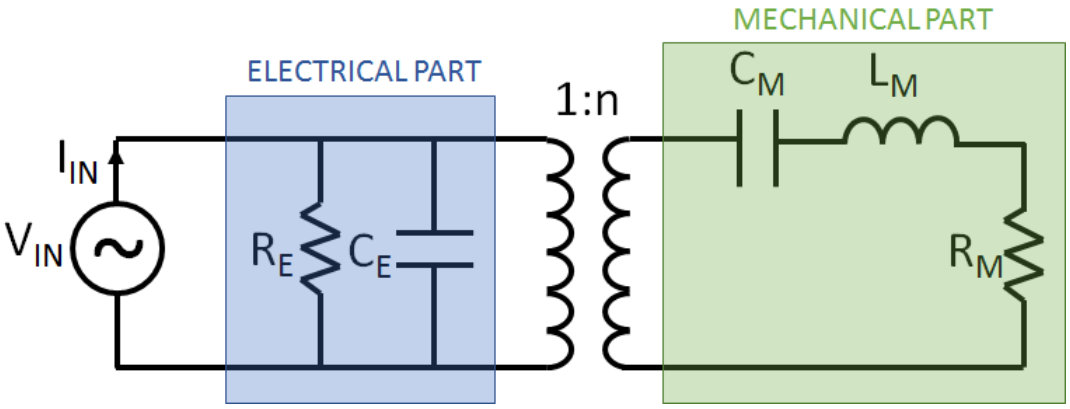


Figure 3.1: Lumped element model of a pMUT. The blue square highlights the electrical part, while the green one the mechanical one.

capacitance value will provide an high signal, it will be also difficult to drive, hence a trade-off between signal intensity and device driving is required. R_E represents the loss of the PZT and it will reduce the height of the resonant and anti-resonant peaks, that otherwise will be infinite. This loss is linked with the defects inside the crystal structure of the material and it can be reduced by improving the PZT processing.

Looking the mechanical part, one can see three other elements: a capacitor C_M, an inductor L_M and a resistor R_M. These three components come from the mechanical model of the membrane. In particular, the mass is converted in an inductor; the elastic part, that is a spring in the mechanical domain, will be the capacitor in the electrical one; the resistor is the mechanical dumping that represents especially the thermo-mechanical dissipation, due to the non-ideality of the pMUT membrane.

The synergy among these elements near the resonance will lead to two important resonant zones. The first one is the resonant frequency, in which C_M resonates with L_M. The second one is the anti-resonant frequency, in which C_E resonates with C_M and L_M. At the resonant frequency the impedance will reach the minimum value, while at the anti-resonant one the maximum value. This behaviour could be seen from the experimental measurements. Nevertheless, as we will discuss in subsection 5.4.3, if the pMUT response is too low, the resonance and anti-resonance could not be noticed from the

measurements.

In order to have a better understanding of the resonance and anti-resonance contributions, one could employ an alternative scheme of the device, shown in Figure 3.2.

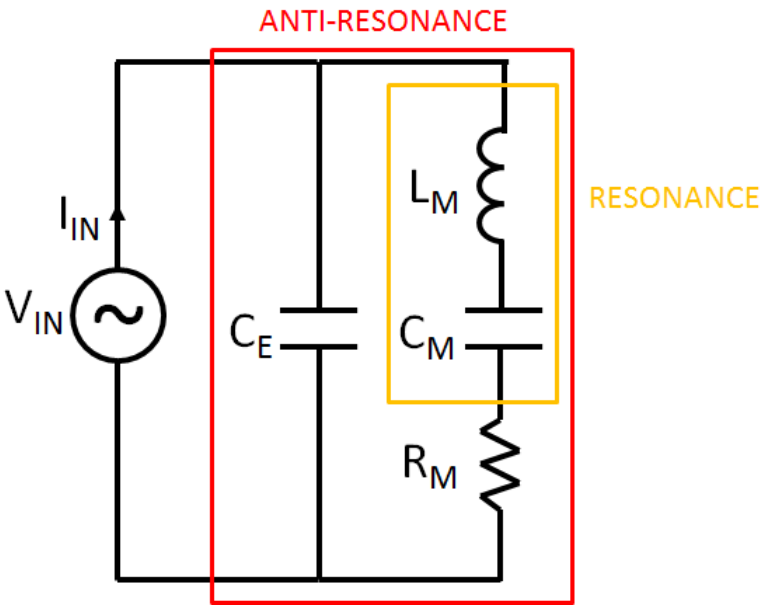
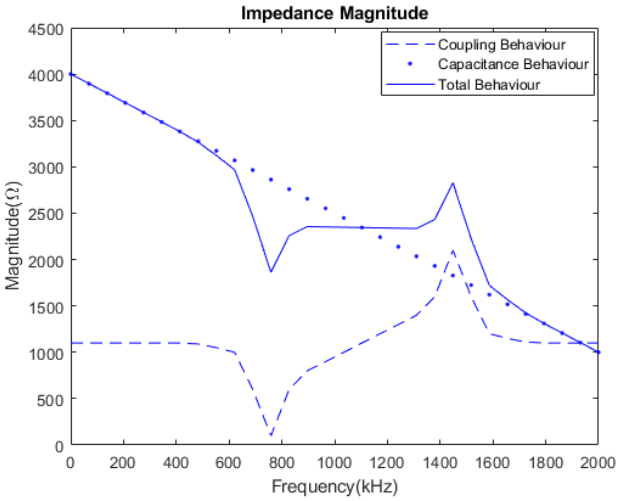


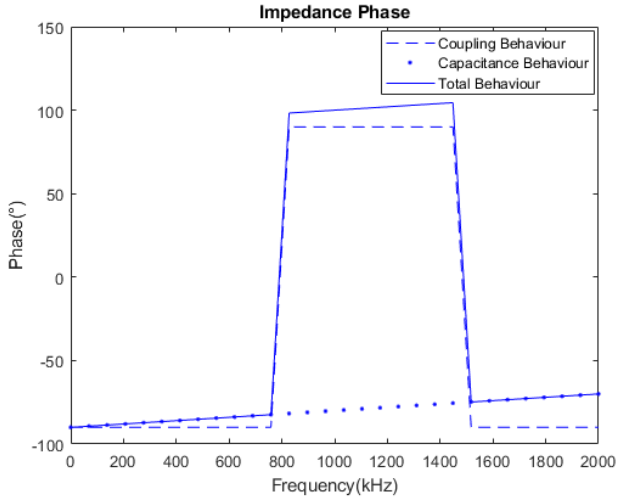
Figure 3.2: Alternative lumped element model of a pMUT. The yellow square highlights the resonance, while the red one the anti-resonance. The R_E is omitted because can be incorporated in R_M.

From the scheme, in the yellow square the elements of the resonance are placed, while in the red one the elements that play a role in the anti-resonance are shown.
At the resonance point, the L_M and C_M are cancelled out and the impedance reaches the minimum value.
For the anti-resonance, both the left and the right branches resonate together, hence the current goes from one branch to the other one. Therefore, the current in the left branch is almost equal to the one in the right one, and utilizing the Kirchhoff law at one node, we can conclude that $I_{IN} \approx 0$. This will lead to a V_{IN}/I_{IN} very high, thus the maximum of impedance is reached at this point.

In Figure 3.3, the magnitude and the phase contributions of the impedance are shown.



(a) Impedance Magnitude.



(b) Impedance Phase.

Figure 3.3: Impedance Magnitude (a) and Phase (b) behaviour in frequency, showing the different contributions.

Discussing the magnitude, the coupling behaviour is linked with the resonance and anti-resonance, because the mechanical and the electrical part of the system are in connection and the minimum and maximum impedance points appear (dashed line).
The capacitance behaviour is linked with the metal/piezo/metal stack, in which the piezoelectric layer acts as a dielectric. This contribution decreases with respect to the frequency because the capacitance becomes more and more resistive (dotted line).
These two contributions are added up in the whole device, and the final graph is created (continuous line).

Regarding the phase, the coupling behaviour shows an increase of the phase from -90° to 90° at the resonance, and a decrease from 90° to -90° when the anti-resonance is reached. This effect is due to the coupling close these two frequencies, that change the transfer function (dashed line). In this case the behaviour changes from a capacitive one (phase equal to -90°) to an inductive one (phase equal to 90°) in between the resonance and anti-resonance frequencies [20].
The capacitance behaviour, given that the metal/piezo/metal stack becomes more and more resistive, shows an increase of phase that is linked with an added resistance contribution (R_E). This contribution can be smaller or larger depending by the process development of the capacitor (dotted line).
These two contributions are added up in the whole device, and the final graph is created also for the phase (continuous line).

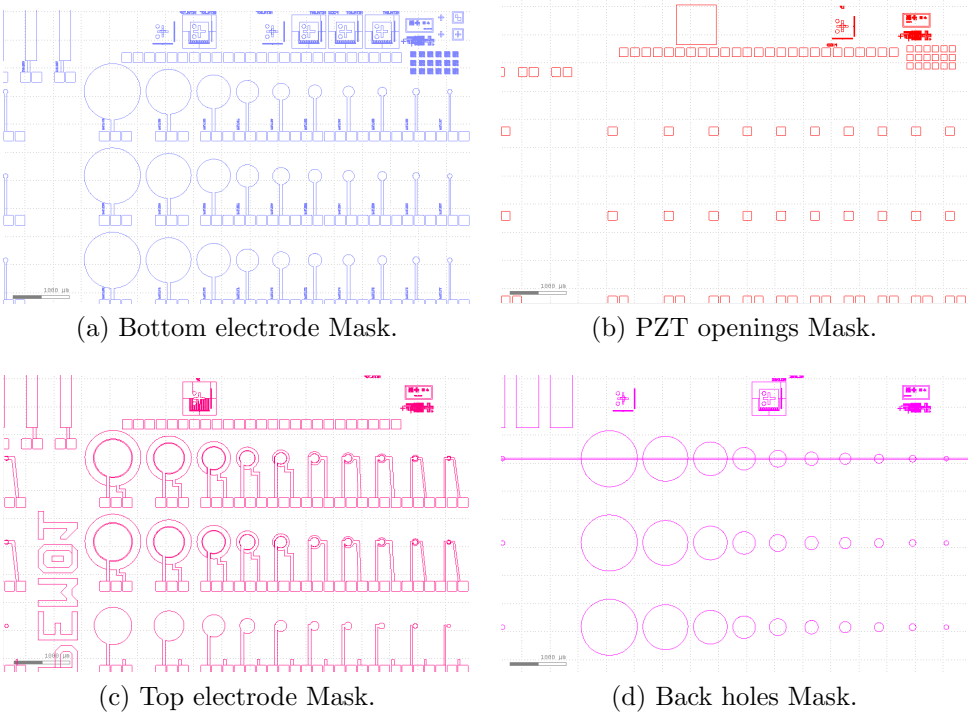
It is worth highlighting that this is an ideal case, but in our case process issues will change these graphs, as we will discuss in section 5.4. Anticipating, the main issues could lead to a lowering of response, both for phase and module, as well as a broadening of the signal shape.

Extracting the parameters from this model, the goodness of the device can be obtained. This is very important for the design of the system. The LCR (inductance, capacitance, resistance) measurements in chapter 5 will be useful for the extraction of these lumped elements. With this, the total input impedance and the PZT capacitance is obtained, thus a better understand of the system is achieved.

3.2.3 Mask Design

Another important aspect of the design is the mask concept. This part is usually the product of all the modeling and analysis about the single device and the entire system, and for this reason it is the last step of the design.
In general, MEMS design has a particular set of design rules and constrictions, and all these aspects must be taken into account during the mask design. Optical Proximity Corrections (OPC) are usually employed in the case of CMOS design, given the smaller size of such circuits, but in our case the scale is of micrometer order, hence it will simplify the mask design.
The masking design in this project is done before, and the main concept will be explained.
Four masks are employed: bottom electrode, PZT openings, top electrode, back holes. Each of these masks has the Bright Field (BF) and Dark Field (DF) version. BF means that the features are covered by a layer of chromium, while outside only glass is present. DF is exactly the opposite: Everything is covered by chromium, except the features. The difference between BF and DF is mainly due to the type of exploited photoresist. Given that the experimental choice is a positive photoresist, the DF version will be employed. Therefore, in this case, where there are holes on the mask, the resist will be removed by developing. The entire mask set is shown in Figure 3.4.

The bottom electrode mask is employed to pattern the bottom metal, that is a stack of Pt/Ti. In this case a lift-off process is chosen. It is worth mentioning that the final device will have a blank bottom electrode, but some tests on bottom electrode patterned PZT will be shown as well.
The PZT openings mask is dedicated for the pattering of the vias through the PZT to reach the bottom electrode.
The top electrode mask is utilized to pattern the top electrode, and like bottom electrode, a lift-off technique is exploited.
Finally, the back holes mask is chosen in order to open the back side of the wafer and release the membrane. This step, that will be explained more carefully in section 4.8, is one of the most critical.



(a) Bottom electrode Mask.

(b) PZT openings Mask.

(c) Top electrode Mask.

(d) Back holes Mask.

Figure 3.4: Employed mask set for the device processing. The bottom electrode mask (a) will not be utilized for the final device, but other tests will exploit the entire set.

3.3 Process Flow

In section 2.4, we discussed about ideal structure of a pMUT transducer. In the reality, the process flow has some constraints that make the structure different.
In this project, a main process flow is developed, followed by ongoing changes in order to obtain the best performances and process integration. It is possible to see the final process flow in Figure 3.5.

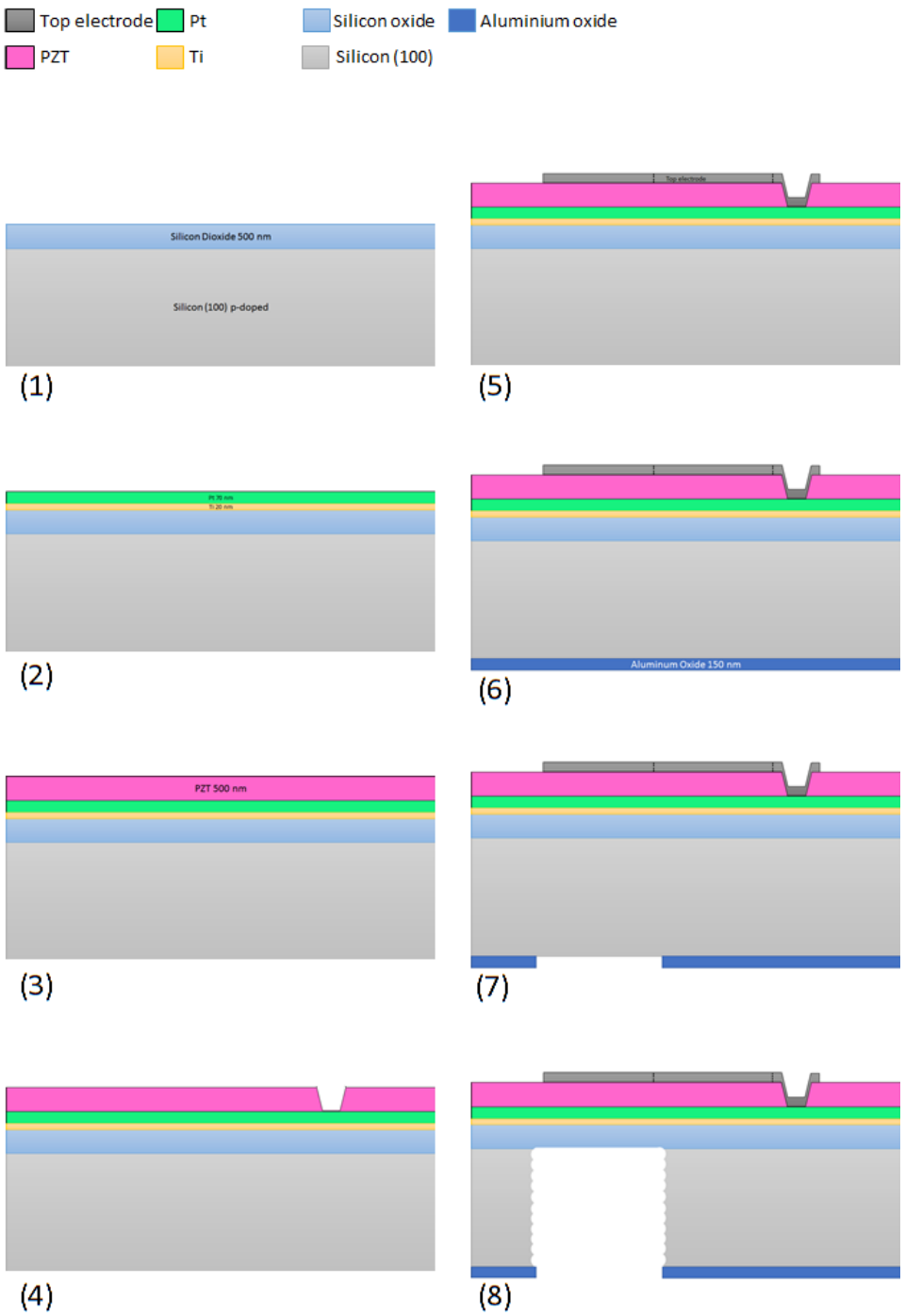


Figure 3.5: Process Flow steps.

1)The process starts with a Boron-doped (100) oriented silicon wafer with 500 nm of thermal SiO_2. This substrate's choice is mainly due to the high processability and to the low cost.
The thermal oxide has two main roles. First, it is a structural layer, thus it will influence the resonant frequency and the mechanical properties of the membrane. Secondly, it is a nice etch-stop layer. It means that, during the back side etching for the release of the membrane, the oxide will make the process slower, avoiding the over etch, hence the perforation, of the pMUT.

2)Then, 20 nm of Ti and 70 nm of Pt are deposited through evaporation. The titanium acts as adhesion layer between the oxide and the platinum, due to the very high affinity with the oxygen inside the SiO_2. On the other side, the platinum is chosen for the good trade-off between chemical and electrical properties: it is inert to the overwhelming majority of the chemical etchings and it has a nice conductivity.
Moreover, platinum acts as seed layer for PZT growth. In fact, Pt(111) orientation forces the PZT to have (110), (111) and (200) PZT crystals, that are strictly linked with the ferro/piezoelectric properties, as we will discuss in section 5.3. In this first version of the device, the bottom electrode is not patterned, but it is a simple uniform film.

3)On top of Pt layer, PZT is deposited by employing Sol-gel technique. The thickness of this layer is around 500 nm, depending on the particular lot. This is due to the process variation of the PZT preparation. The PZT is spin-coated and UV oven-baked several times, until the correct thickness is reached. Each step gives about 200 nm of PZT. When the wanted thickness is reached, a final bake at high temperature is employed in order to crystallize correctly the material. This is a very delicate step in the device preparation, because the PZT is the core of the whole structure, dictating whether the device's properties are suitable for the applications. A deeper understanding about Sol-gel process will be given in chapter 4.

4)The patterning of PZT is performed, employing a multiple steps process of BHF and HCl. The wet etching process is chosen because it is faster and there are no issues related to the contamination of the etching chamber, that is present in dry etching process. As we discussed in subsection 2.3.5, the BHF attacks Ti and Zr, while HCl removes Pb and Ti. This is a pure isotropic step, and it must be short enough to avoid degradation issues in the

PZT. These problems are mainly due to infiltration of the chemical species inside the material, followed by a decrease of the properties and performances.

5)Then, a lithographic step is employed in order to pattern the top electrode through lift-off process, shown in Figure 3.6.

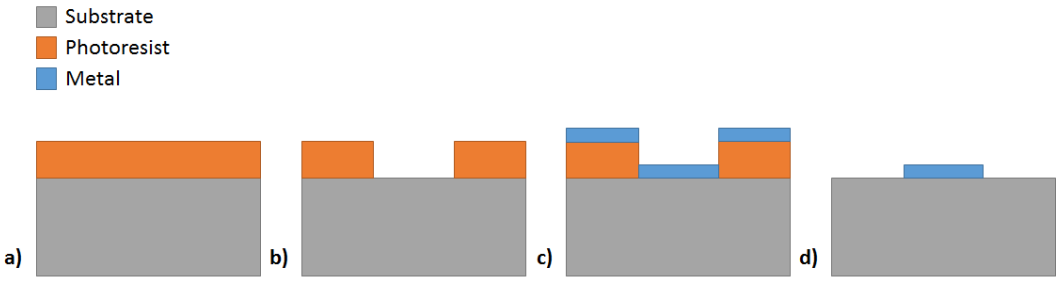


Figure 3.6: Lift-off process steps: a) Photoresist spinning; b) Photoresist patterning; c) Metal deposition; d) Photoresist removal.

The chosen photoresist is a positive type, thus in order to obtain the top electrodes, the patterned photoresist must be present outside where no metal is required. It is worth highlighting that the lift-off process works properly if:

$$R = \frac{t_{PR}}{t_m} > 3 \tag{3.1}$$

Where R is the ratio, t_{PR} is the photoresist thickness and t_m is the metal thickness. Thus, the photoresist thickness must be 3 times or more larger than the metal one to obtain good features. In our case, the resist thickness is larger than 1 µm and the metal is less thick than 100 nm, thus the rule is satisfied.
Four different types of stack are tested: Au, Al, Ti/Al/Ti and Pt/Ti (look section 5.3). All of these materials where deposited through evaporation method. Nevertheless, among these materials, the Ti/Al/Ti stack is the best one in terms of performances. Moreover, this stack is ideal to increase the adhesion and the aging problems: the bottom Ti is employed to improve the adhesion between the PZT and the Al layer, given that PZT has oxygen; the Al increases the conductivity of the contact; the top Ti prevents the oxida-

tion of the contact.

6)A thin layer (about 140 nm) of Al_2O_3 is grown employing Atomic Layer Deposition (ALD) technique. This layer will be patterned and will act as hard mask for the back side etching. The ALD is a chemical deposition in which two main precursors are employed to obtain the aluminum oxide layer as one could see from Figure 3.7.

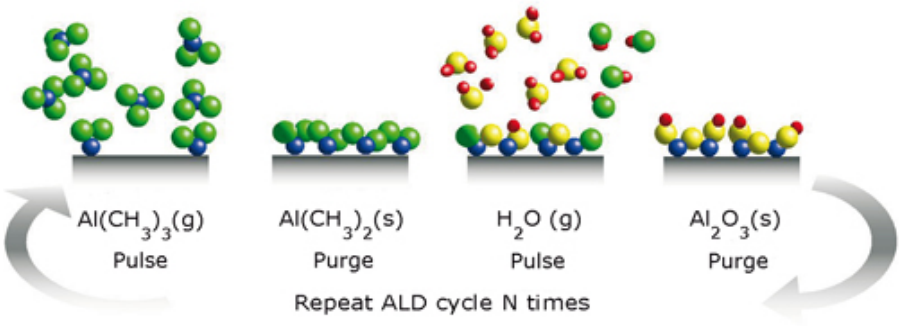


Figure 3.7: ALD process steps [21].

First, the trimethylaluminium ($Al(CH_3)_3$) gas is injected in the chamber through a pulse, then it reacts with the surface, covering it completely after some time. At the end, a mono-layer of Al with tails of $(CH_3)_3$ will cover the whole surface and the excess gas is purged. These tails will react with the second pulse of H_2O gas, forming methane (CH_4) in the chamber atmosphere and growing Al_2O_3 on the surface. The excess water and methane will be purged and finally only a thin mono-layer of aluminum oxide will be obtained. This cycle is then repeated until the required thickness is reached. The ALD is a very long process, but with the advantage of a very pure and crystallized layer, that increase the robustness of the material in harsh environment.
Given that one cycle gives fraction less than 1 nm of thickness, some hundreds of cycles must be employed in our case, with a chamber temperature of 150°C in order to avoid breaking of the top side of the wafer due to high temperature process. The choice of Al_2O_3 is mainly due to the particular chemical inertness of the material in SF_6 and C_4F_8 plasma, so that it can withstand the harsh environment and long time of the back side etching

process. Moreover, this resistance is enhanced by the perfectly crystallized structure obtained by ALD.

7)After the growth of Al_2O_3, it will be patterned with Back Side Alignment (BSA) and isotropic wet etching in BHF bath will be employed. Due to the chemical inertness of the material, several minutes are required to etch it. This long etching time must be taken into account during the choice of the photoresist, employed to pattern the Al_2O_3, because it could peel off, exposing the whole layer to the chemicals.

8)Finally, the back side etching is performed in order to release the membrane. The chosen etch is a dry etching process, called Bosch process. This particular etching gives an exceptional aspect ratio between the hole size and the etching depth. The whole process is shown in Figure 3.8: A mask defines the etching regions (a); then, the sulfur hexafluoride (SF_6) is injected in the chamber and the plasma is turned on (b). At this stage, a DC bias is added in order to increase the vertical anisotropy of the etching; then, the octafluorocyclobutane (C_4F_8) is turned on and only chemical effect is exploited (c). This plasma creates a Teflon-like layer that covers the whole exposed surface, so that the walls are protected by this barrier; finally, the SF_6 is injected again and the DC component will destroy the bottom part of the Teflon-like protective layer, while the chemistry of SF_6 will continue to etch isotropically the silicon (d).
Thus, SF_6 is employed for etching, while C_4F_8 is utilized for passivation. It is worth highlighting that the C/F ratio dictates the polymerization rate. The higher this ratio is, the higher the polymerization is with respect to the etching. That's why C_4F_8 is employed instead of CF_4. The final shape of the sidewalls is not perfectly straight, but they are wavy, due to the isotropic etching of SF_6. This effect is called scalloping. It is worth mentioning that SF_6 is very common in silicon etching technology. The etch rate, the vertical profile and the walls covering are dictated by the time of etching and passivation cycles: the more the etching is, the larger the scalloping and the etch rate will be; the more the passivation is, the smaller the scalloping and the etch rate will be. One should find a good trade-off between passivation and etching time in order to avoid secondary effects. For instance, if the passivation is too long, a micro-patterning due to excess of polymer could happen, creating a bottom part similar to grass.

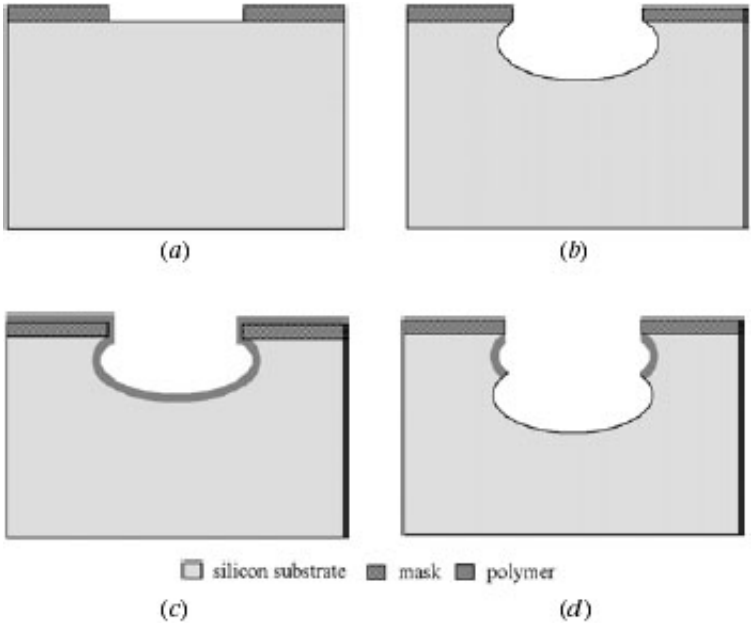


Figure 3.8: Bosch process steps [22].

In this step, three main issues must be taken into account: first, whether the hard mask could withstand the etching; second, a precise etching time estimation in order to prevent the etching of the thermal grown SiO_2 layer too, that, as we discussed in point 2 of the process flow, is a structural layer; third, the protection of the front side of the device, that could be etched by the chemistry. These issues will be tackled in section 4.8.

In conclusion, the pMUTs are fabricated employing standard silicon technology, with the important integration of PZT processing. The cross and front section of the device is better shown in Figure 3.9. All the single steps will be treated more in detail in the chapter 4.

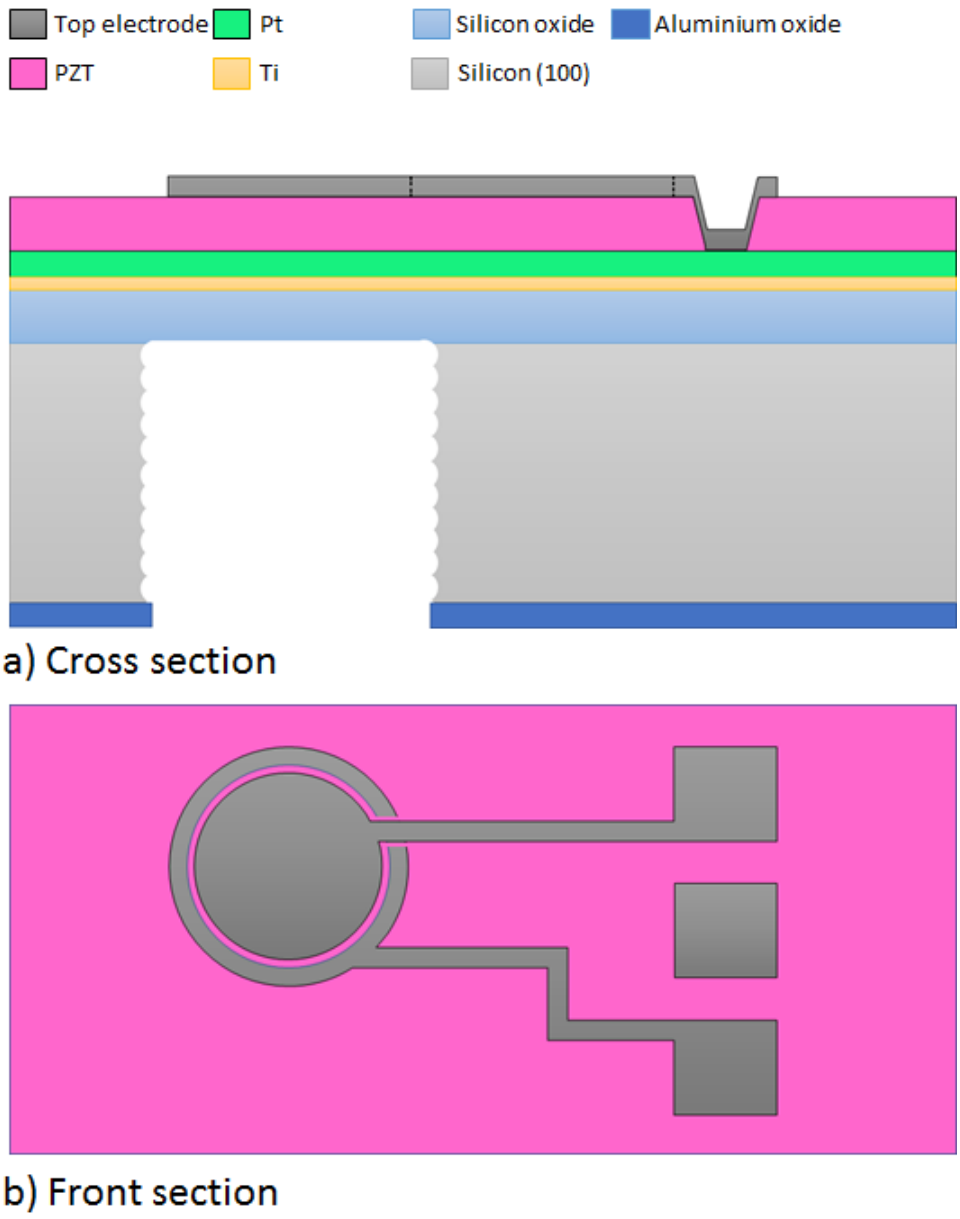


Figure 3.9: Cross section (a) and front section (b) of the pMUT.

Chapter 4

Process Development

4.1 Introduction

In this chapter the development of the process flow steps is debated. Usually in process and integration engineering, for each step, a short loop experiment is carried out, in order to check the possible failures. A short loop means that the process starts from the step of interest and only this step is considered and studied. In this case the additive failure effects from the other steps are reduced and only the ones from the step under exam are detected. This is a very common technique in processing and helps engineers and scientists avoiding waste of time, especially if the processed device requires a long and complex flow. We will discuss all the process flow steps and the related issues in detail.

4.2 Wafer Preparation

As we discussed in section 3.3, the initial steps are the cleaning of the wet oxide on top of the (100) Boron-doped silicon wafer, the Ti/Pt deposition through evaporation and the spinning and baking of PZT layer. These first steps are already done by the company in the first version of the device. After, different experiments involving the PZT are performed, and the results will be shown in the next sections of this chapter. Different wafer dimensions are employed for the tests, but for the final device a 3 cm x 3 cm sample is chosen.

4.3 Bottom Electrodes

The main device is made with a uniform bottom electrode, that connected all the devices together. This choice is mainly due to have good PZT quality. As a matter of fact, if the Pt layer does not cover the whole wafer surface, the PZT would grow with a nice crystallization on the Pt and with a poor quality outside. This could lead to defects formation at the interface of these two regions, decreasing the performances everywhere on the wafer (look subsection 4.4.1).
Despite the fact that the main device is made with a blank bottom electrodes, studies related to the patterning of Pt/Ti stack and subsequently PZT deposition are performed. The reason for these tests is related to the process flow of the final array, in which the first wafer with the array must be reversed and bonded to a second wafer in which the cavities are placed. After this, the first wafer will be etched away and the structures will be released. Thus, in this case, the bottom electrode will be top electrode and vice versa. If the new top electrode is not patterned, it is not possible to control the devices one by one.

4.3.1 Lithography

As mentioned before, for the bottom electrode a double layer of Pt and Ti is chosen. The Pt layer has a thickness of 70 nm, while the Ti one is 20 nm. The presence of Ti is mainly due to improve the adhesion between Pt and SiO_2 underneath. In this case, lift-off technique is the best way to pattern this double layer. To do so, a double spin of two different photoresists is employed. Before the spinning, a cleaning step of the samples is necessary, in order to reduce the contamination and improve the resist adhesion. To do so, a double bath of Acetone and IPA is employed, so that the highest part of organic particles are removed from the surface. After this, the samples are dried with a nitrogen gun and a fast bake is performed. This bake helps the chemical activation of the substrate and SiO_2, improving the adhesion in the spinning step. Then, the first photoresist is spun and then baked. After this step, the second photoresis is spun at higher speed. The final bake is performed, and the time must be carefully set in order to avoid the overbaking of the first photoresist, but at the same time have a nice bake of the second one. Both these photoresists are positive ones: this feature is very important especially for exposure, in order to choose the right mask.

Then, the two photoresists are exposed using the dark field type mask for bottom electrodes, because in this way the resist will be developed in the exposed areas, uncovering the bottom electrodes' regions for the next metal deposition step. The exposure is performed employing MA6 tool by Suss MicroTec. The optimal exposure time is set, employing normal UV light and hard contact mode, in which the mask and the sample are in contact during the exposure.
After the exposure, a development step is carried out in order to remove the exposed photoresist. In this step, developer is chosen for the correct resist compositions. During the development, the samples should be moved, so as to achieve an increase of rate and uniformity of development. Concerning the two layers of photoresist, the first is a standard one, usually employed for micrometric features, while the second is a photoresist that has larger developing width than the first. Therefore, the presence of the latter is strategical to have undercuts below the former. In this way the lift-off is much more efficient, because the metal can easily break due to the discontinuity. This will lead to lower Critical Dimension (CD) and thus it will burst the integration of smaller devices.

4.3.2 Pt/Ti Deposition & Lift-off

Before the deposition of the metal layers, a thickness check must be performed in order to evaluate the feasibility of lift-off. The final thickness of the two photoresists is around 1.19 µm, shown in Figure 4.1.

As one could see, the ratio between the photoresist stack and the metal stack is:

$$\frac{t_{PR}}{t_{metal}} = \frac{1.19\mu m}{90nm} = 13.3 > 3 \tag{4.1}$$

Thus, the photoresist thickness is enough to perform an high quality lift-off. The evaporation technique through e-beam is employed for the deposition of Pt/Ti stack. This technique is suitable with this process flow because the e-beam evaporates the metals without increasing the temperature of the chamber, so that the resist will not be melted.
At the end of the deposition, a uniform film of Pt/Ti covers the entire wafer,

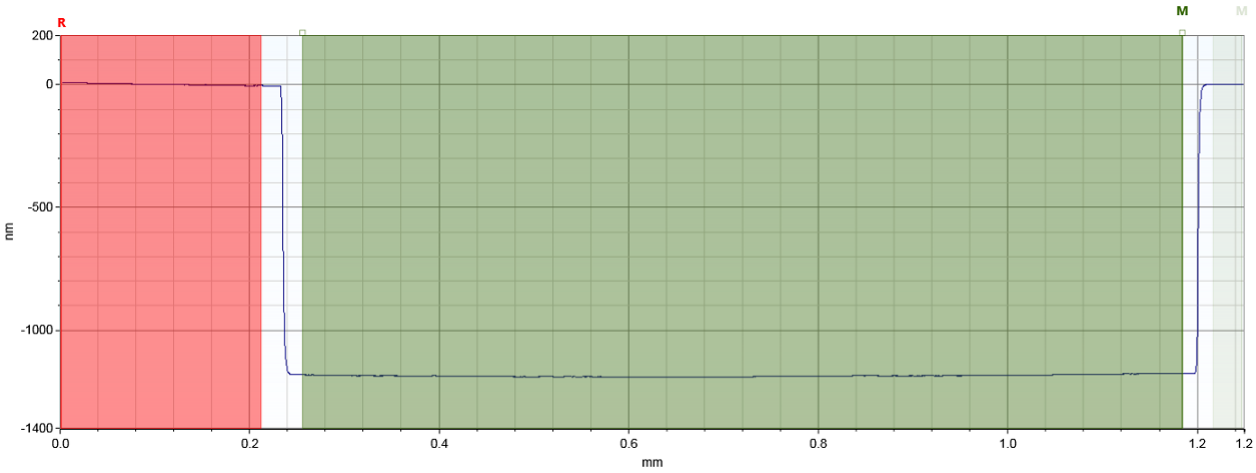


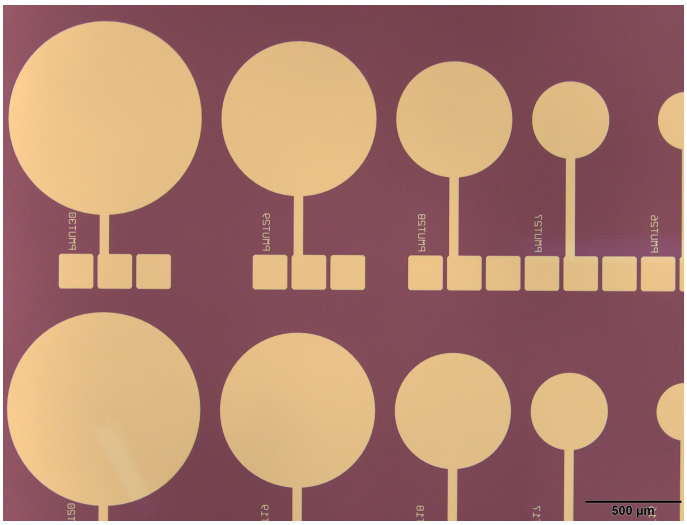
Figure 4.1: Double-layer photoresist profile after development.

both on top of the photoresist and on the opened pads' zones. Then, the sample is dipped in a microstrip solution for long time and heated up. The heat-up is meant to have the best photoresist stripping efficiency. After this step, the beaker is left in ultrasonic bath for few minutes in order to destroy and remove big metal residues. Then, the sample is bathed in a new and clean microstripper in order to remove the residues of resist and finally few minutes in IPA to clean it.

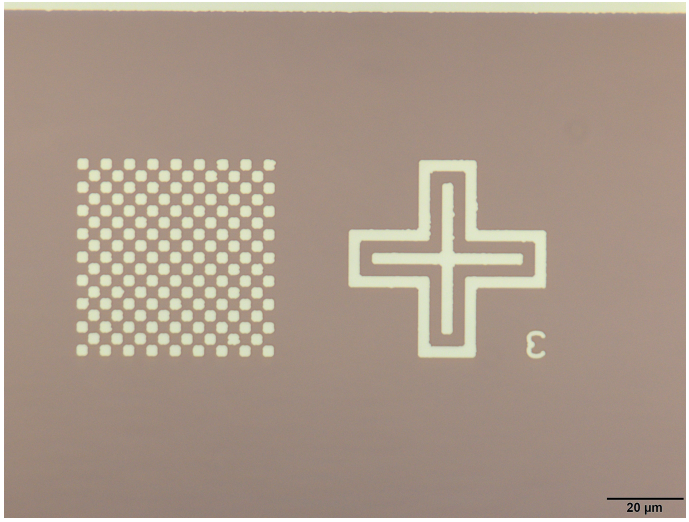
As one could see from Figure 4.2, the achieved CD is about 3 µm, that is a very nice result for our application, given that the smallest dimension of the devices is dictated by the wires, that have a width of 50 µm. Furthermore, the shape of the bottom electrodes has an high definition. In general, lift-off is surface dependent, and the surface properties of SiO_2 with photoresist and Pt/Ti could be different than the ones of PZT. For this reason, the bottom electrode patterning is not a critical step, and we will see the difference of lift-off quality in section 4.5.

4.4 PZT Deposition

On top of the bottom electrode, a layer of PZT is deposited. The test structures are made with the Sol-gel and the Pulsed Laser Deposition (PLD) PZT.



(a) Patterned bottom electrodes.



(b) Detailed resolution of lift-off.

Figure 4.2: Lift-off result of bottom electrodes' shape (a) and a detail of the maximum resolution with this process (b).

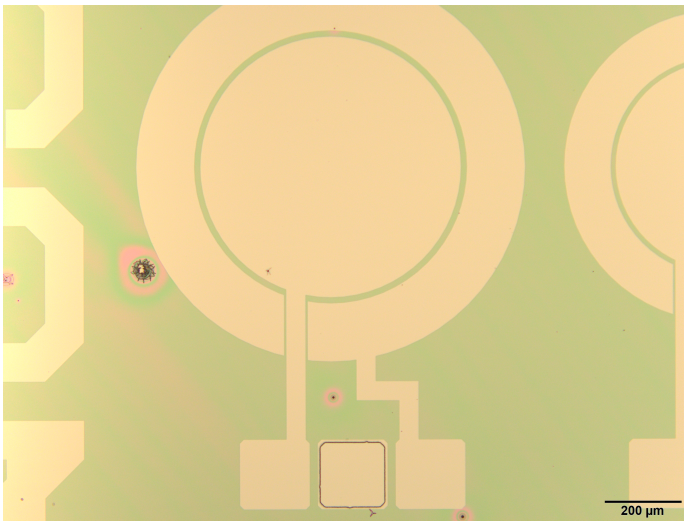
The final device exploits the Sol-gel PZT because the performances are better than the PLD one. We will deepen this topic in section 5.3.
In general, but this is just an anticipation of the next chapters, the Sol-gel PZT has a better uniformity on the wafer, while the PLD one is deposited in

a ring shape, so that the performances change concerning the radius distance from the center of the wafer. Regarding the crystallization, the PLD PZT has a seed layer of LNO (look subsection 2.3.4), therefore the crystals can grow in a more oriented way than Sol-gel one. The main problem of Sol-gel PZT is the presence of particles all around the wafer, mainly due to the organic solution that is employed for Sol-gel technique. Hence, for a large area application, the Sol-gel PZT is the best thanks to the better uniformity, even if it is a less clean process. Moreover, for cost concerns, Sol-gel PZT is cheaper and easier to process than PLD one, increasing the advantages of the former technique of the latter one.

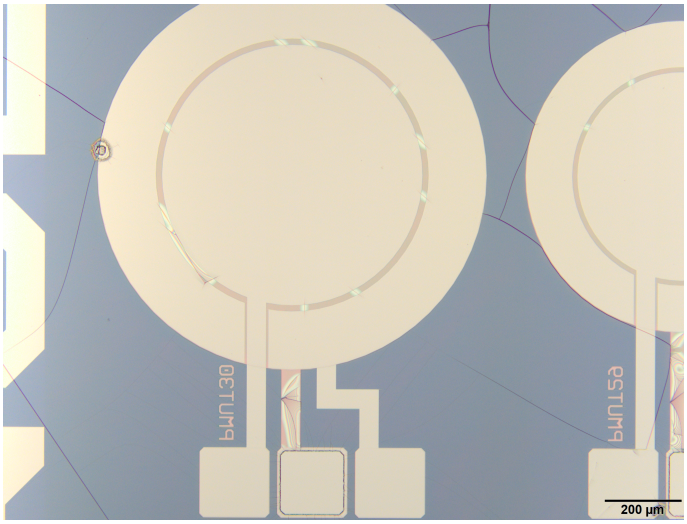
4.4.1 Sol-gel PZT Cracking

In the first part of Sol-gel PZT study, the material is deposited by an external company on blank or patterned Pt/Ti bottom electrodes. The same recipe is employed for both the bottom electrodes' types.

Figure 4.3 shows the difference in PZT quality. The first one (Figure 4.3(a)) has a good quality, with some organic particles as we said before, while the second one (Figure 4.3(b)) has multiple cracks all around the wafer.
From this result, one could conclude that the density of Pt in the bottom electrode is essential for a good growth of PZT. In fact, as we discussed in the theory, the Pt layer acts as seed layer for PZT, helping the crystallization and the orientation. The organic particles in the PZT seem to be the starting points of these cracks, that will expand entering in the device regions.
These cracks are characterized by the AFM team, and, the results show a crack depth of about 500 nm, that is the thickness of the PZT layer. In fact, the cracked devices don't work and the reason should be linked to a short circuit between bottom and top electrodes that appears during the top electrode deposition thanks to the cracks.
In order to solve the problem, different tests are performed. The general idea is to give to PZT the energy and time to recrystallize before the deposition of the top electrode. To do so, a Rapid Thermal Annealing (RTA) is employed. 500°C, 550°C and 600°C are chosen as working temperatures, while 120 s and 150 s are utilized as annealing times. In general, all these tests are successful, and a comparison of dark field microscope images before and after annealing



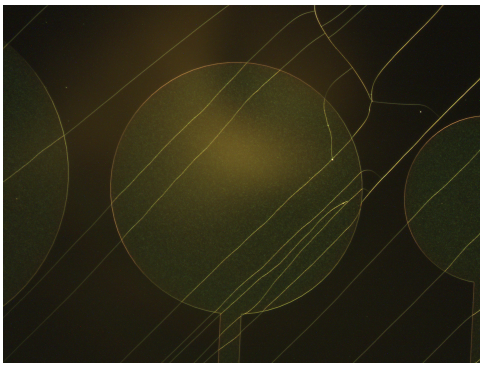
(a) Blank Sol-gel PZT.



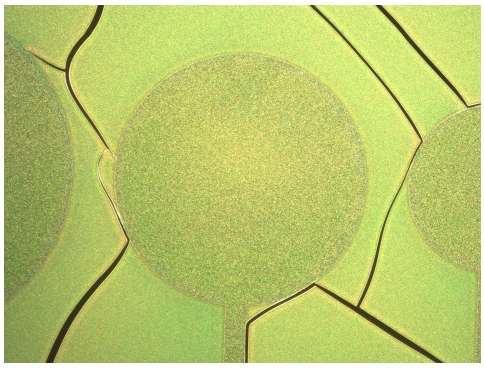
(b) Patterned Sol-gel PZT.

Figure 4.3: Images of a entire pMUT starting from blank (a) and patterned (b) Pt/Ti bottom electrodes.

at 600°C for 150 s is shown in Figure 4.4. Before the annealing the cracks are everywhere, inside and outside the devices area, while after it the cracks are just outside the devices area.



(a) Before annealing.



(b) After annealing.

Figure 4.4: DF images before (a) and after (b) annealing at 600°C for 150 s. After annealing the cracks are placed only outside the devices area.

This change in the recipe will be implemented directly in the IMEC labs, in order to avoid crack formation from the beginning of the process. It is worth highlighting that this improvement will be a further step in the PZT integration and for this reason it is not treated in detail in this thesis.

4.5 PZT Patterning

As we discussed in the theory and process flow, the PZT can be etched in two different ways: dry and wet etching. The chosen method is the wet one for some reasons. First, it is the only allowed in IMEC due to possible contamination of the dry etching tool given the presence of lead inside PZT. Second, it is a fast method to etch this material.

4.5.1 Lithography

Before performing the etching, a lithography is employed to select the etching regions. It is important to have a good resist against strong acids such as buffered hydrofluoric acid (BHF) and hydrochloric acid (HCl). Moreover, the photoresist should be thin enough to release the 3 µm features of the mask.

After the cleaning procedure for the wafer, a priming procedure is applied on the wafer. After this, a baking is employed to set the primer. The role of priming is to improve the adhesion between the sample and the photoresist, that could be poor in this step due to the presence of PZT. Then, the photoresist is spun on top of the primer and subsequently baked. Considering that chosen photoresist is a positive one, a DF mask is utilized. This mask has just the PZT openings to reach the bottom electrodes. The exposure time is set and UV light and hard contact mode are chosen. After this, the sample is bathed in the developer, moving the sample in order to improve the development uniformity.

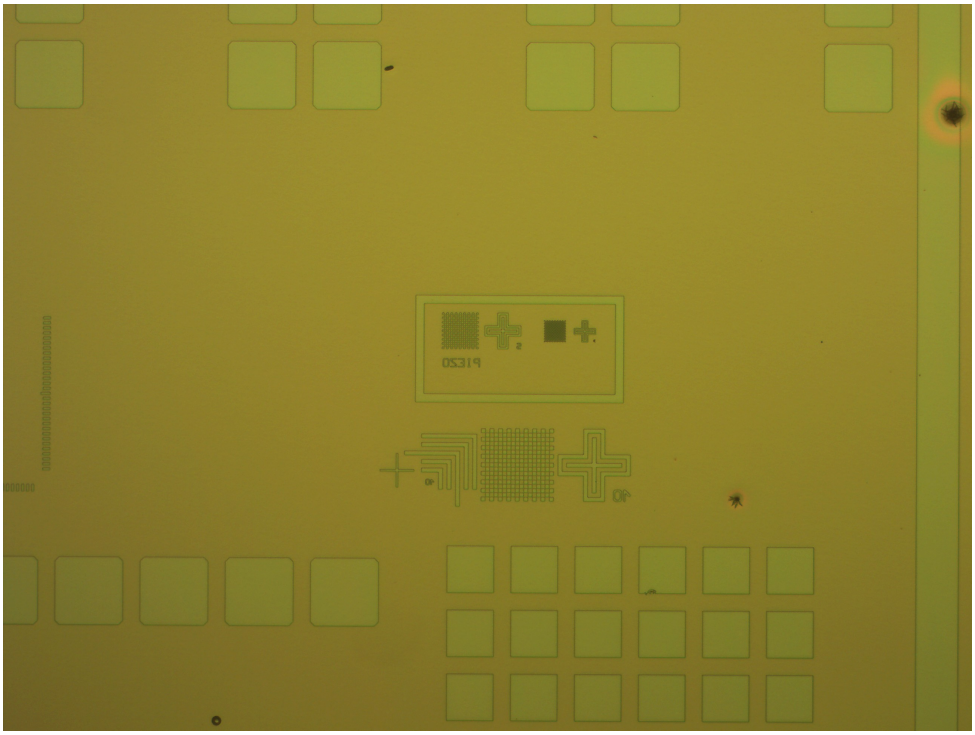


Figure 4.5: Lithographic step.

The final result is shown in Figure 4.5. As one could see from the figure, all the features are open, as well as the 3 µm ones.

4.5.2 Etching

After the lithographic step, the etching is performed. At the beginning, only buffered hydrofluoric acid is utilized, but white residues due to new species formation appeared in the etching zones.
Thus, buffered hydrofluoric acid (BHF) and hydrochloric acid (HCl) are employed to perform the etching. The two chemicals could be mixed together to form a unique solution to etch PZT, but in this case they are utilized separately, with multiple baths, for safety reasons. Nevertheless, the next step will be a mixed solution to integrate this in a fab process flow.
Multiple etching tests are made in order to obtain a good etching quality.

The final recipe is:

- BHF 7:1 concentrated at room temperature
- Fast rinse in DI water
- HCl 37% concentrated at room temperature
- Long rinse in DI water
- Repeated until the bottom electrode is exposed

This recipe works both with 500 nm of Sol-gel PZT and with 1 µm of PLD PZT employing the same number of cycles. The difference in the etching time of the two deposition techniques is probably due to a different density: from the etching results, we could conclude that Sol-gel PZT should be denser than PLD PZT, but no tests are performed to demonstrate this.

Considering that BHF/HCl etching is isotropic, in theory the same amount of material in vertical and lateral direction should be etched. In practice, this is reached only if there is agitation of the system in the liquid, as shown in Figure 4.6. Without agitation, the lateral etch rate would be larger than the vertical one, causing unwanted links among the close structures. Therefore, the sample is agitated both in BHF and HCl.
It is worth noticing that PZT is a polycrystalline material and until now no monocrystalline one has been grown. For this reason, no anisotropic wet etching are available, hence the only option is the isotropic wet etching.

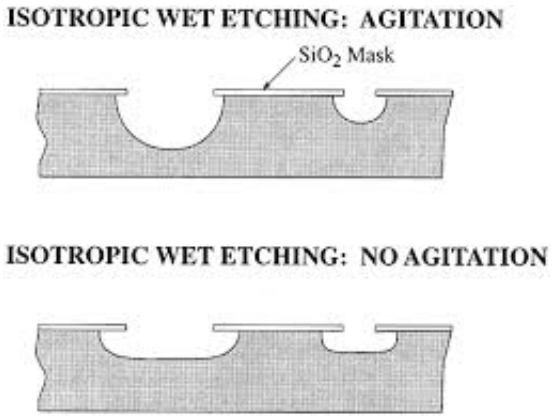


Figure 4.6: Isotropic wet etching with (top) and without (bottom) agitation [23].

The resulting etching is shown in Figure 4.7. Due to the isotropic nature of the etching, just 10 µm features are released, with an almost complete etch of regions with 6 µm and 3 µm features. This is an important result for the feasibility of the process flow, and it dictates a limit for the smallest device that one could fabricate. However, in our case the smallest feature is 50 µm, therefore the obtained CD complies with the specifications. In Figure 4.7 the enlargement of the features can be observed by looking the squares and the big line on top of the image. The features' edge has a double ring, that is typical when an enlargement of the structures is present.

4.6 Top Electrodes

The next step is the deposition and patterning of top electrodes. This part is very similar to the Pt/Ti lift-off. The main difference is the outer ring that some devices have and the smaller dimension of top electrode with respect to the bottom one. This outer ring acts to change the membrane movement shape when the device works.

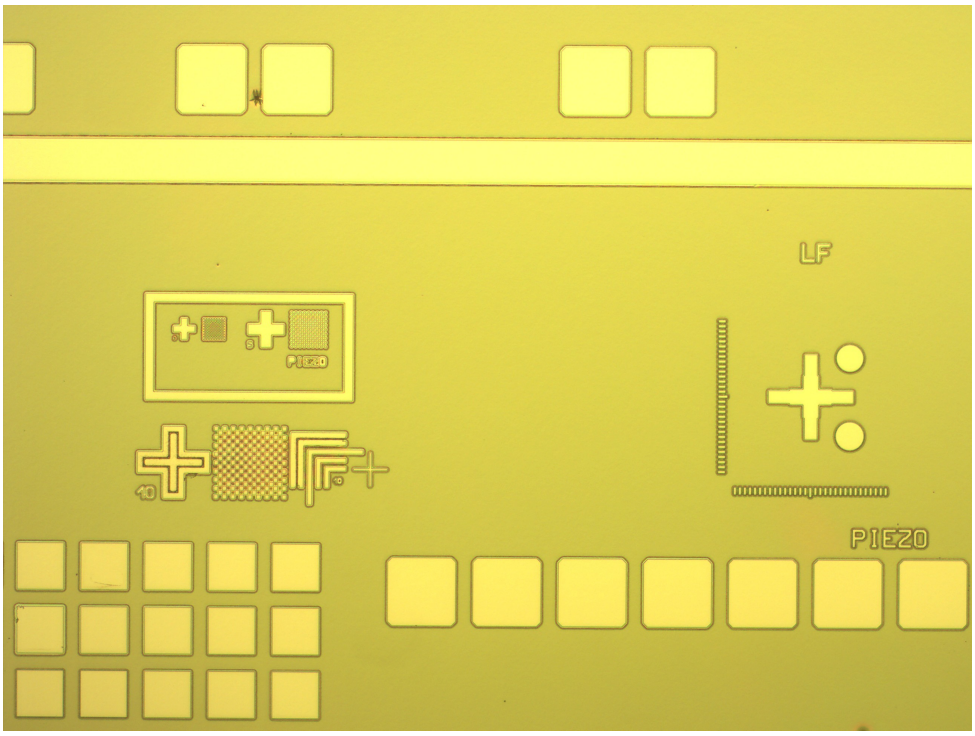
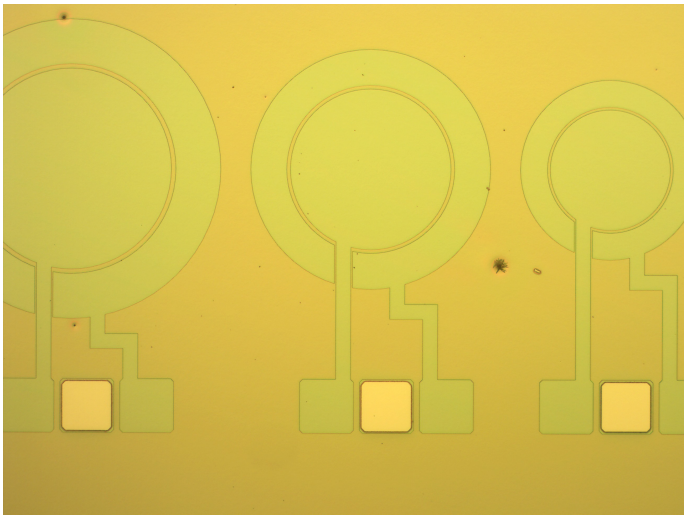


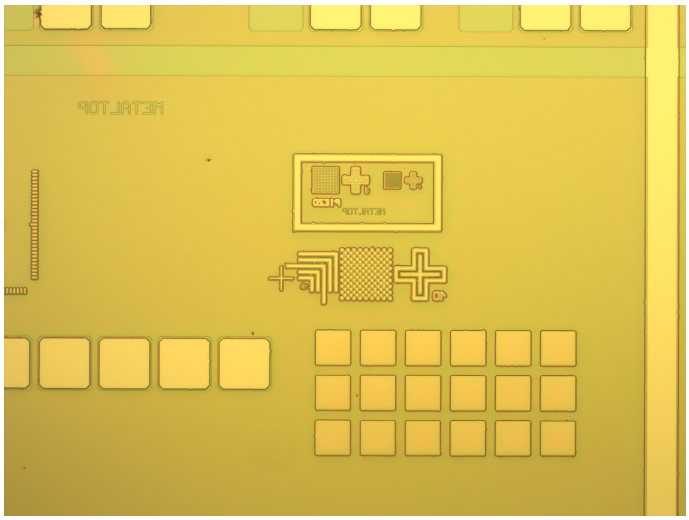
Figure 4.7: Etching of Sol-gel PZT with BHF/HCl cycles. The obtained CD is 10 µm

4.6.1 Lithography

The lithographic process is exactly the same of Pt/Ti.
The first photoresist is spun on top of the clean wafer, and then baked.
After this, the second photoresist is spun followed by a final baking that must be set in order to bake properly both the resists without over or under bake.
Top electrodes DF mask is employed to create the openings where the top electrode should be placed. The exposure time is set with UV light and hard contact mode. Then, the exposed resist is developed.
At the end, the result is shown in Figure 4.8, and one can appreciate the sharpness of the features' angles and the fact that the outer ring is perfectly separated with respect to the inner one. This is a really important aspect for an optimal operation of the device. Moreover, the same resolution of bottom electrodes (3 µm) is reached with this process too. Nevertheless, the final resolution is dictated by the PZT etching (10 µm).



(a) Top electrode features.



(b) Detail.

Figure 4.8: Lithography for lift-off of the device (a) and the small details (b).

4.6.2 Ti/Al/Ti Deposition & Lift-off

After the patterning of the top electrode regions, a triple layer of Ti, Al and Ti is deposited via sputtering. To sum up the deposition:

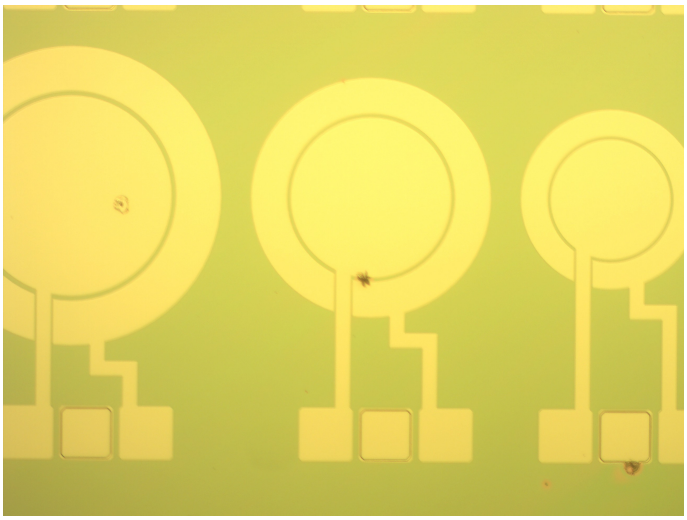
- 30 s Ti pre-sputtering
- 10 s Ti deposition: t=10 nm
- 30 s Al pre-sputtering
- 3 min13 s Al deposition: t=90 nm
- 30 s Ti pre-sputtering
- 10 s Ti deposition: t=10 nm

At the end, a layer of 10 nm of Ti, 90 nm of Al and 10 nm of Ti is deposited all around the sample. Where the photoresist is developed, the triple layer will remain, otherwise it will peel off during the lift-off process.
As we discussed in chapter 3 and we will deepen in chapter 5, Ti/Al/Ti stack is chosen because it has the highest remanent polarization, that is strictly linked with the piezoelectric coefficients and hence it is a very important figure for our device operation.

Also the lift-off is the same of Pt/Ti. The sample is bathed in the microstripper and heated up for several minutes, to reach the best resist stripping efficiency. Then, the ultrasound bath is turned on for few minutes. To remove the remaining residues of photoresist and organic components, a final bath in clean microstripper and IPA for few minutes each is performed.
The final result is shown in Figure 4.9, in which we can appreciate the separation between inner and outer rings of the device, most delicate part in this process step, and the sharpness of the features, especially the wire ones which are the smallest.

4.7 Aluminum Oxide Hard Mask

In order to protect the wafer from back-side etching, an hard mask of Al_2O_3 is employed. The aim of this mask is to protect the regions outside the device membranes. In fact, during the back-side etching, only the circles, in



(a) Top electrode features.

(b) Wire detail.

Figure 4.9: Top electrodes after lift-off of the device (a) and the wire detail (b).

which the membranes should be, must be etched. Outside the membrane zones, the chemical/physical properties of Al_2O_3 will withstand the etching process. This is mainly due to the strong chemical inertness of aluminum oxide with respect to the silicon etching chemistry, that in our case is SF_6 to

etch and C_4F_8 to passivate (look section 4.8).
Savannah tool is employed to do so, that performs Atomic Layer Deposition (ALD). The idea of this technique, as it is explained in section 3.3, is the alternation of two gases. These two gases deposit a thin layer each, and at the end of each cycle, a mono-layer of the desired material is created. This technique gives really high material quality and thus it is chosen for the enhanced chemical and physical properties with respect to other deposition techniques. In this way, the oxide can withstand several hours of etching without being destroyed.

4.7.1 Deposition

First off, the Al_2O_3 is deposited on the back-side of the sample. Before starting the deposition process, a layer of standard photoresist is spun on the front-side, in order to avoid the deposition of aluminum oxide on this part. This unwanted deposition could change completely the operation of the devices, shifting the resonant frequency and increasing the stiffness of the structure.
The sample is inserted in the chamber on a carrier wafer upside down, in order to deposit on the back side of it. The deposition starts at 150°C, with a N_2 flow of 20 sccm to help the removal of species in the chamber. In order to perform the deposition, Trimethylaluminium (TMA) and H_2O peaks are alternated, as shown in Figure 4.10:

- Pulse of 0.022 ms of TMA
- Purging to remove the not reacted gas
- Pulse of 0.03 ms of H_2O
- Purging to remove the not reacted gas
- Repeat for 876 cycles

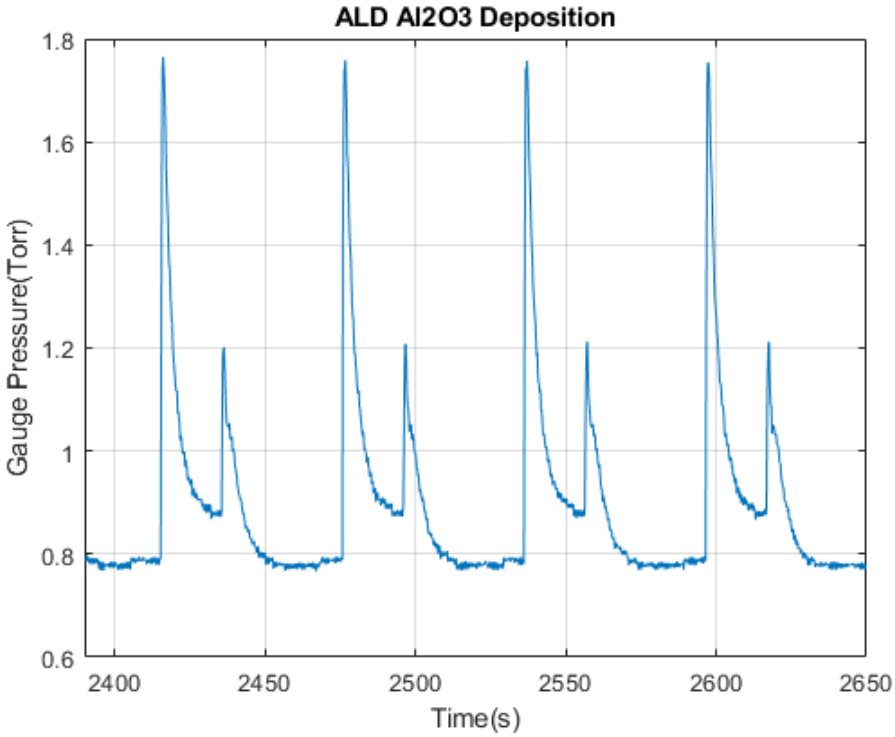


Figure 4.10: Extraction of H_2O and TMA peaks from the deposition parameters. The first peak is TMA, while the second one is H_2O. These peaks are alternated during the whole deposition in order to deposit layer by layer high quality aluminum oxide.

At the end of the 876 cycles, 147 nm of high-quality aluminum oxide are deposited on the back-side of the sample. Hence, for each cycle, a layer of about 0.17 nm is formed. Moreover, the deposition of this material takes 15 hours to be completed, due to the very high chemical control of the tool. As we will see in the next subsection, the wet etching rate of this oxide is really slow thanks to the enhanced properties of ALD.

4.7.2 Back-side Alignment

After the deposition, the thin layer of aluminum oxide is patterned. A back-side alignment must be performed, in order to align the features on the front-side with the openings for releasing the devices on the back-side.

To do so, first the primer is spun to improve the adhesion of the photoresist, that is spun and baked. It is worth noticing that these two resists are spun on the back-side of the sample, where the Al_2O_3 is placed and on the front-side too, because we want to avoid the front-etch of the structures in the wet etching bath.

The exposure is performed with UV light and hard contact mode, employing the DF release mask. This mask has the holes that will be etched with the next steps. Thus, this mask determines the membrane size and shape. To perform the alignment, given that no marks are placed on the back-side of the wafer, a picture of the front-side is taken, and then the back-side is aligned with respect to the front-side picture.

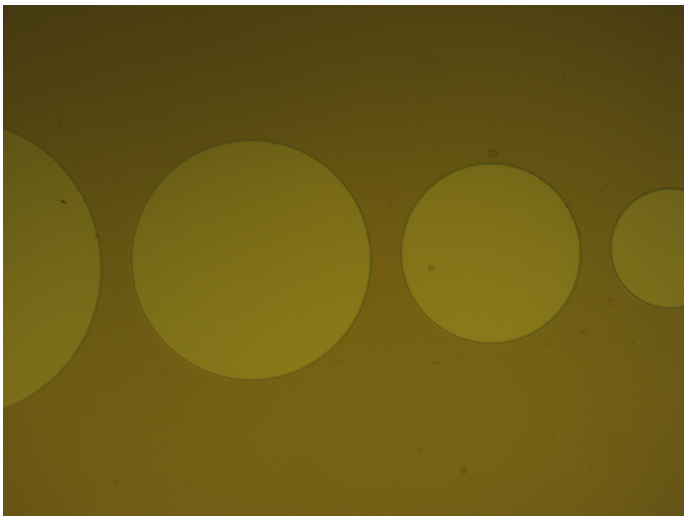
The development of the exposed resist is carried out for 1 min, and the results of the lithography can be seen in Figure 4.11. As we can notice, both large and small holes are perfectly developed, sign that the lithographic process is correctly set.

4.7.3 Etching

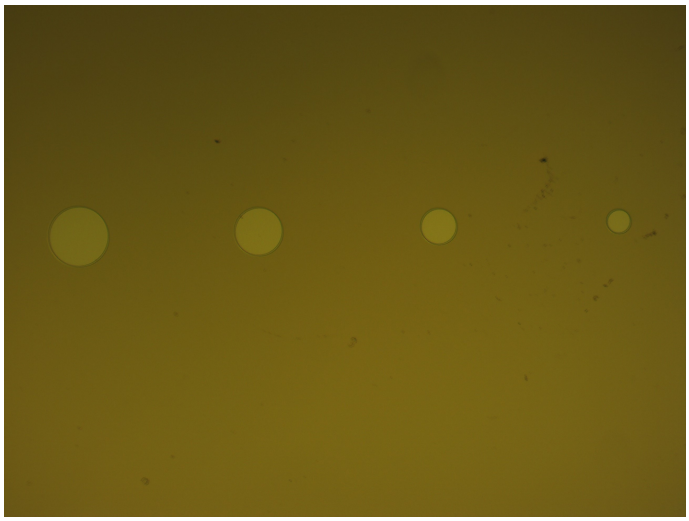
The etching is then performed in order to open the back-side holes. The chosen solution is a bath of buffered hydrofluoric acid (BHF) 7:1 concentrated at room temperature, that has the correct chemistry to attack the aluminum oxide. The Etching Time (ET) is set at 10 min, after which almost all the holes are open. Hence, the Etch Rate (ER) of Al_2O_3 can be calculated through:

$$ER_{Al_2O_3} = \frac{t_{Al_2O_3}}{ET_{Al_2O_3}} = \frac{147nm}{10min} \approx 15\frac{nm}{min} \tag{4.2}$$

Thus, the ER of aluminum oxide is really slow, meaning that the ALD deposition is nicely performed. In fact, one of the parameters that dictates the chemical inertness of a material is the crystal structure. This structure is highly crystallized thanks to ALD. The etched features are shown in Figure 4.12. As one could notice from the figure, some devices have a wavy edge shape. This is probably due to the peeling-off of the photoresist due to the long etching process, hence the edges of the holes are not perfectly protected



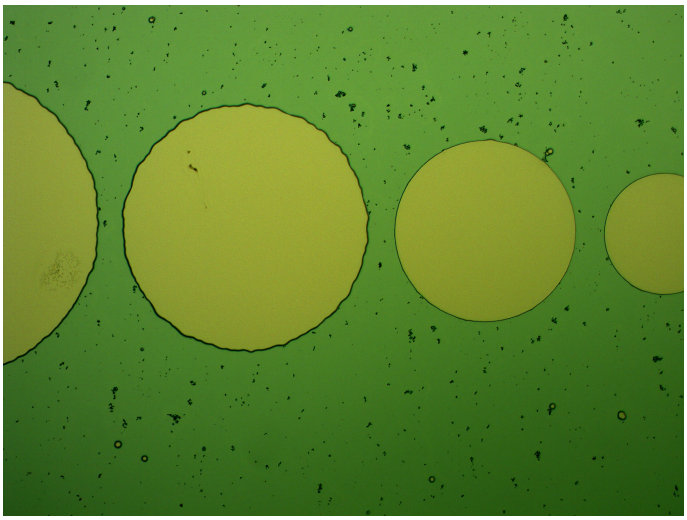
(a) Big features, 1000 µm, 800 µm, 600 µm and 400 µm from left to right.



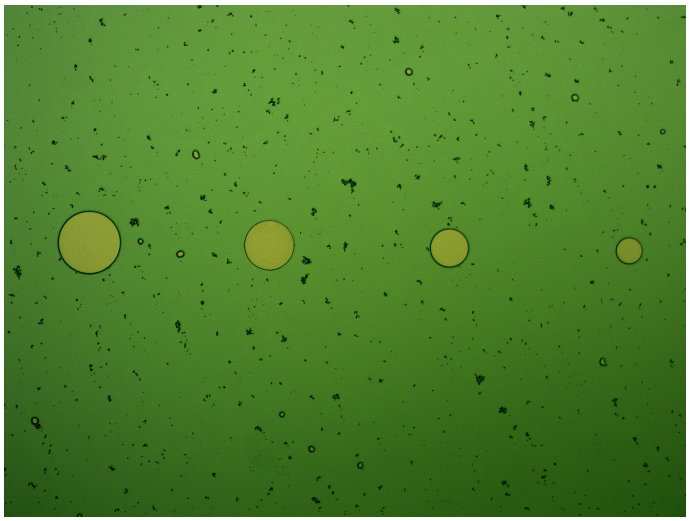
(b) Small features, 200 µm, 160 µm, 120 µm and 80 µm from left to right.

Figure 4.11: Lithography for Al_2O_3 hard mask patterning of the big (a) and small (b) holes. The yellow zones are the ones without photoresist.

anymore.



(a) Big features, 1000 µm, 800 µm, 600 µm and 400 µm from left to right.



(b) Small features, 200 µm, 160 µm, 120 µm and 80 µm from left to right.

Figure 4.12: Etching for Al_2O_3 hard mask pattering of the big (a) and small (b) holes. The yellow zones are the ones without aluminum oxide.

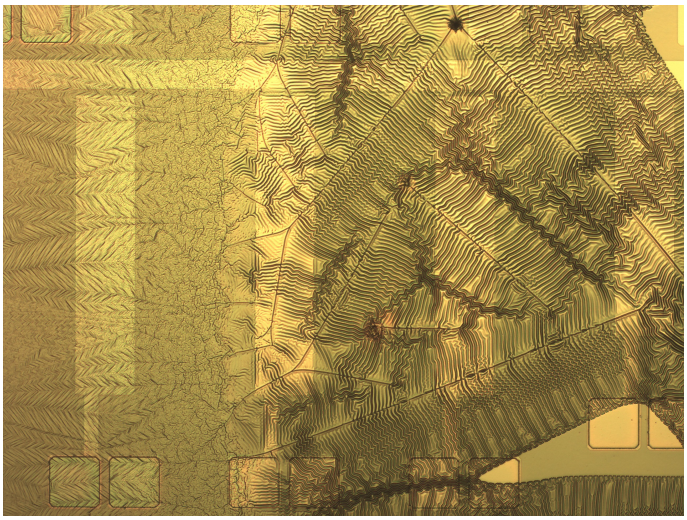
The ET is set at 10 min because after this time the resist starts peeling off from the sample and the whole surface would be exposed to BHF. In this

case, only the biggest structures (from 400 µm to 1000 µm) can be perfectly developed, because the etch rate is size-dependent, hence the smallest structures require more time to be etched properly. This is mainly due to the reduction of exposed hole surface, thus the chemical does not have enough space to act. It is worth mentioning that some small structures are actually etched, and this could be due to different factors, such as thickness variation, chemical variation, position during the etching and so on and so forth. In general, the etch process of the Al_2O_3 is nicely developed and almost all the holes are open.

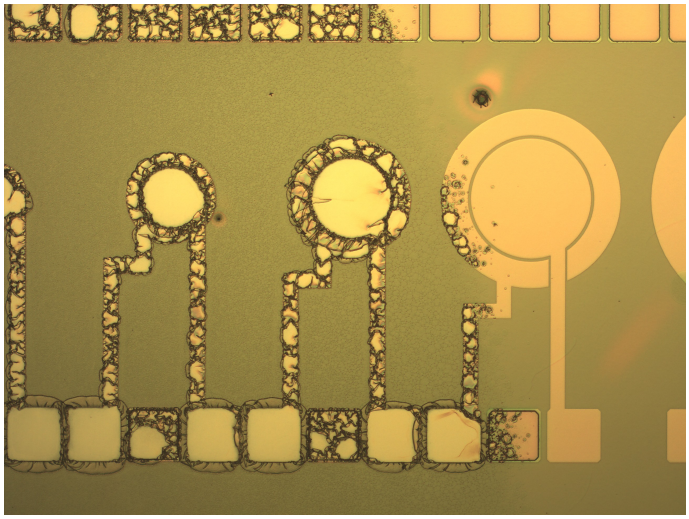
4.7.4 Issues

During the aluminum oxide development there are some issues to deal with. First, during the Al_2O_3 deposition, the resist on the front-side, employed to avoid the deposition on the top part of the membranes, did not withstand the process duration and temperature. In fact, the standard photoresist is usually baked at low temperature for just few minutes, while the deposition in ALD tool exploits a temperature of 150°C for 15 hours. Even if the temperature is not that high to burn completely the photoresist, the long time associated cross-linked the material, as one could see from Figure 4.13. The cross-linking is a phenomenon that could happen when the temperature is particularly high, causing the re-crystallization of the polymeric lattice in a new, more robust shape. Thus, it is really difficult to remove this kind of new resist, due to the different acquired chemical properties.
It is worth saying that, even if the cross-linked resist is still on the membrane, the device operation is modified but not prevented. Nevertheless, the membrane structure is compromised, because the device will have a different frequency response and the piezoelectric properties of the PZT will decrease due to a non-perfect conductivity between the electrodes.
In order to solve this problem, the sample is no longer covered by resist on the front-side but the deposition prevention on the front is performed applying a capton tape all around the sample's edges. In this way no chemical species get inside the space between the carrier and the sample, hence no deposition on front-side could happen.

The peeling-off of the photoresist during the wet etching in BHF is another problem that must be tackled. In fact, after 10 min, the resist begins break-



(a) Cross-link large area.



(b) Cross-link on the devices.

Figure 4.13: Cross-linking problem on the front-side of the sample. The cross-link is not present everywhere, but just in some areas.

ing away from the surface, both front and back side. The uncovered surface will be exposed to the chemical, hence it will be etched. This is a very big problem, especially because it impedes to open the small holes, that usually require more time for the etching. In order to solve the problem, the PAT

photoresist is exploited. This resist is BHF resistant, thus a longer exposure of the resist in the etching bath can be performed. Moreover, this resist is thicker (30 µm), giving an additional barrier for the back-side etching.

4.8 pMUT Releasing

Finally, the device membranes must be released. In order to do so, a Deep Reactive Ion Etching (DRIE) is employed. Before starting the etching process, two different materials, Al_2O_3 and SiO_2, are tested, in order to check the properties under etching condition. This test is performed to choose the correct hard mask for the etching. The requirement is a protection layer that can withstand more than 4 hours dry etching, in order to etch the whole silicon in the holes only.

4.8.1 Deep Reactive Ion Etching Tests

Before starting with the different steps to determine the right hard mask and etching time, a brief overview of the etching process is given.
The tool is an Induced Coupled Plasma (ICP), meaning that two different chambers work:

- The first chamber, placed in a different zone from the etching one, dictates the plasma density.
- The second chamber is the actual etching chamber, and it is the one in which the sample will be placed.

Hence, the plasma from the first chamber is brought to the second chamber when the correct ion density and species are reached.
The species exploited in this etching process are sulfur hexafluoride (SF_6), octafluorocyclobutane (C_4F_8) and oxygen (O_2).
As we discussed in section 3.3, the SF_6 is employed to etch the silicon, while the C_4F_8 is utilized for the passivation of the trench walls. The oxygen is added to the SF_6 in small percentage in order to increase the selectivity of silicon with respect to oxides (especially SiO_2). This small addition increases the concentration of F ions because the oxygen will bond with S ions to form

oxides (SO_2), increasing the Si etch rate and reducing SiO_2 one.
To summarize, the exploited recipe can be described as:

- 130 sccm of SF_6 + 20 sccm of O_2 for 12.5 s at 600 W of RF power and 130 W of DC power to etch the silicon and remove the bottom passivation layer.
- Purging this mixture and starting the injection of the other one.
- 85 sccm of C_4F_8 for 8 s at 600 W of RF power to passivate the trench.
- Purging this mixture and starting the injection of the other one.
- Repeat this cycle until the correct etching depth is reached.

It is worth highlighting that a carrier covered by resist is needed in order to reduce the exposed blank silicon. This silicon can indeed contaminate the whole plasma atmosphere, and consequently the etch rate will be unstable. Moreover, the sample must be placed on the top of this carrier with a thermal conductive glue in order to improve the conductivity between the carrier and the sample, avoiding resist burning. As we will see in the issues part, this will lead to some changes of the membrane quality.

4.8.2 Hard Mask Etching Test

The choice of Al_2O_3 as hard mask is dictated by the properties of the material under dry etching conditions. In particular, the resistance of the material under SF_6 and C_4F_8 for 4 hours etching are studied.

The main idea is to make the process flow as simple as possible in order to reduce the costs for mass production. Hence the first test is performed without hard mask but only standard photoresist. Unfortunately, after 1 hour of etching, the resist is almost fully consumed, due to the small thickness of the resist. In fact 1.14 µm are etched in 1 hour, hence the etch rate is calculated as:

$$ER_{resist} = \frac{t_{resist}}{ET_{resist}} = \frac{1140nm}{60min} = 20\frac{nm}{min} \tag{4.3}$$

Given that the standard photoresist is not suitable for this long time etching,

a layer of silicon oxide is tested. Plasma Enhanced Chemical Vapor Deposition (PECVD) and thermal growth are employed. A thin layer of 140 nm is deposited but after 5 min of etching no more SiO_2 is present, hence the etch rate is:

$$ER_{SiOx} = \frac{t_{SiOx}}{ET_{SiOx}} = \frac{140nm}{5min} > 28\frac{nm}{min} \tag{4.4}$$

Thus, given that large thicknesses of oxide are difficult to make and high cost, the silicon oxide cannot be utilized as hard mask.

At the end, the Al_2O_3 is taken into account to exploit it as hard mask. The ALD deposition is employed and a thin layer of about 147 nm is deposited. As one could see from Figure 4.14, the etching depth of the aluminum oxide in the dry etching plasma for 30 min is about 9 nm, meaning that the etch rate is:

$$ER_{Al_2O_3} = \frac{t_{Al_2O_3}}{ET_{Al_2O_3}} = \frac{9nm}{30min} = 0.3\frac{nm}{min} \tag{4.5}$$

Hence, the etch rate for this hard mask is really slow, mainly because the SF_6 does not attack chemically the aluminum oxide, but only the sputtering part (DC) does, while the C_4F_8 protects the material covering it each cycle. Therefore, the etching actually removes the polymeric layer and does not have a huge penetration in the Al_2O_3.

4.8.3 Back-side Etching

After the hard mask choice, some tests on Si (100) substrate must be performed in order to know exactly the etching time. Indeed, if we look at the structure, after the silicon substrate a thin layer of 500 nm of oxide is present (looking from the back-side to the top-side of the sample). This oxide is integrated part of the device, and it has a mechanical function, increasing the stiffness, hence the resonant frequency of the membrane. Thus, if the etching goes on more than the necessary to remove completely the Si, the SiO_2 will be attacked too.
As one could notice from Figure 4.15, the etched depth increases quasi-linearly, while the etch rate is reduced quadratically with respect to the

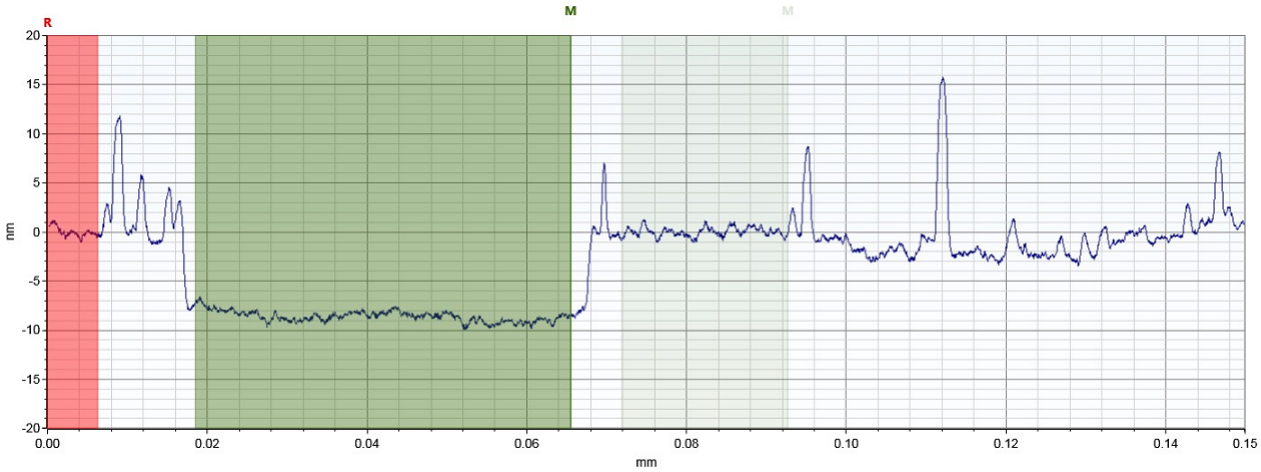


Figure 4.14: Etching depth of Al_2O_3 in SF_6/C_4F_8 plasma atmosphere for 30 min.

time. This is an important problem that must be fixed in order to exploit the etch rate as an indicator. In fact, if the etch rate drops, we know that the SiO_2 layer is reached and so the etching must be stopped.

Therefore, an improvement in the recipe is needed. The main reason of this rapid decrease of etch rate is mainly due to an imbalance between the etching and the passivation cycles. In particular, here the hyphothesis is that we have a passivation cycle that lasts too much, compared to the etching one. Hence, increasing the etching depth, the products of the etching are less and less easy to remove from the hole, while the passivation covers everything, reducing the etch rate. Thus, different tests are performed to improve this issue, obtaining as best result a variation from 12 s to 12.5 s for the etching cycle and from 7.5 s to 8 s. It is worth highlighting that, even if both cycle times are increased by 0.5 s, the etching one has a larger impact in the process due to the presence of the DC sputtering.
After this change, the etch rate is nicely stabilized and the etching of the pMUT can be performed, as shown in Figure 4.16.

We can notice, comparing Figure 4.15 and Figure 4.16, how the etch rate increases after the adjustment from 2.1 µm min^{-1} to 2.2 µm min^{-1}, meaning that the cycle variation of 0.5 s increases more the etching than the passiva-

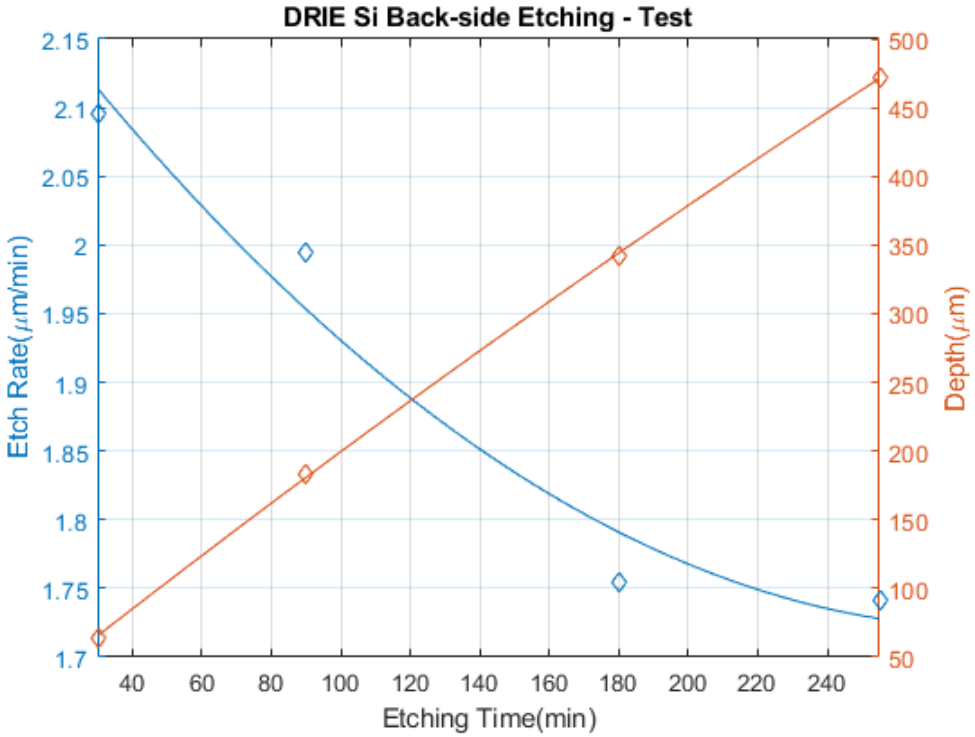


Figure 4.15: Etch rate and etching depth of Si DRIE without any recipe adjustments to make the etch rate constant.

tion.
The etch rate is now fixed until 160 min are reached. After this time, the etch rate drops from about 2.2 µm min^{-1} to 1.2 µm min^{-1}. Given that the silicon oxide etch rate in DRIE atmosphere is about 50 nm min^{-1}, the variation of etch rate means that the SiO_2 is reached. Therefore, the etching process must be stopped in order to avoid rapid consumption of the oxide layer.

The hole edges and the membranes are shown in Figure 4.17 and Figure 4.18, respectively. As one could notice from the figures, the edges are well developed, while the internal part of the membranes has some cracks in various points. This is mainly due to the fragility of the structure, given that it is a very thin suspended membrane 1 µm thick. Nevertheless, few sites contain these cracks, thus the process is an overall success.

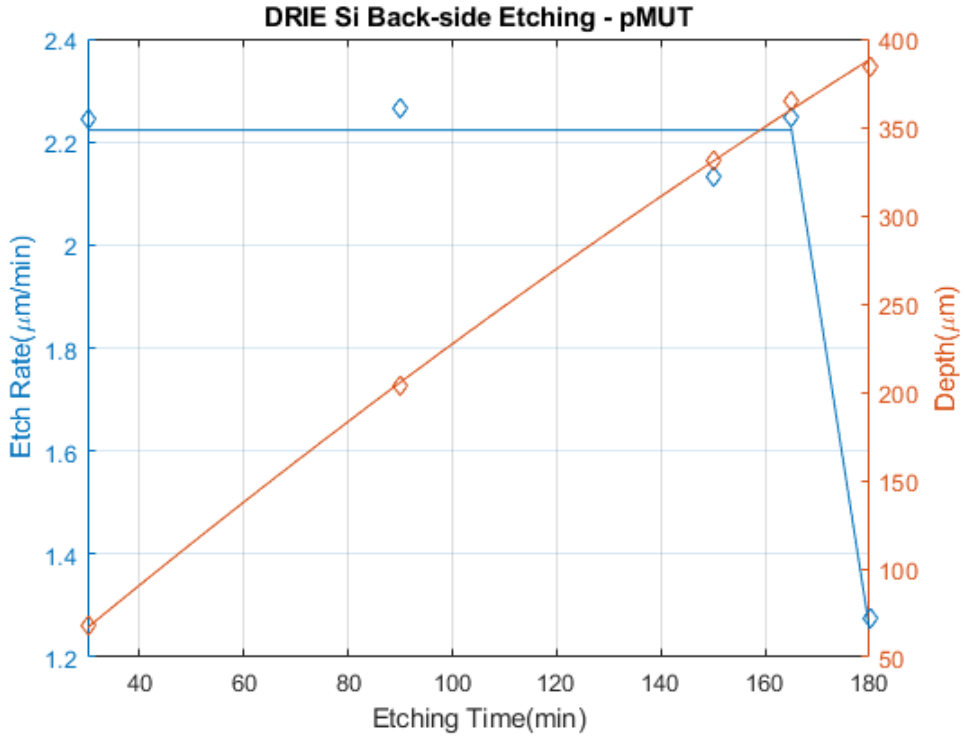
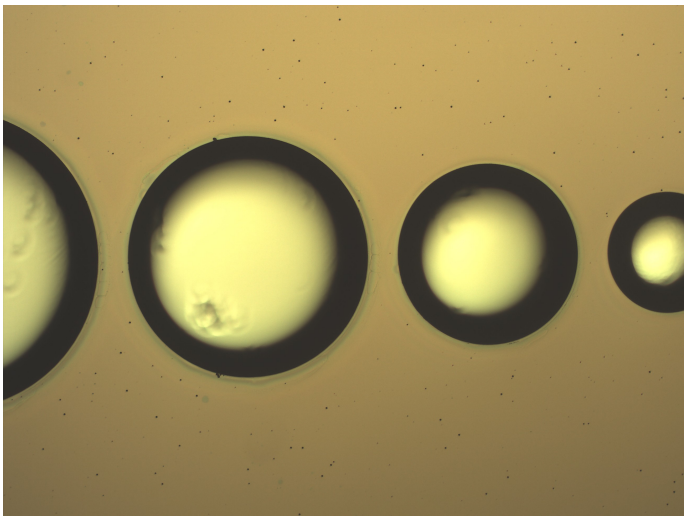


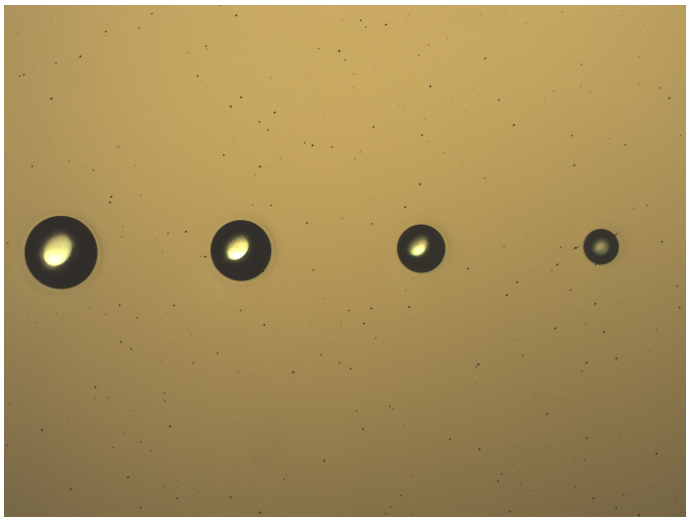
Figure 4.16: Etch rate and etching depth of Si DRIE with the etching cycle variations. After 160 min the etch rate drops down, hence the silicon oxide is reached.

4.8.4 Bosch Process Issues and Analysis

On the other hand, the exploited Bosch process to perform deep reactive ion etching possesses some issues that must be tackled to have the proper membranes. In Figure 4.20, we can highlight the shrinking of the membrane size from 915 µm to 755 µm. Moreover, the etching floor of the cavity is bended, thus a non-uniformity and thickening of the membranes is present. We will discuss this problem comprehensively in chapter 5, anticipating that a shrinking and thickening of the membrane, together with a non-uniformity, will cause a shift of the resonant frequency and a degradation of the resonant peak.
Therefore, improvements in the Bosch process must be performed, and in case no stability will be achieved, new integration solutions must be ex-



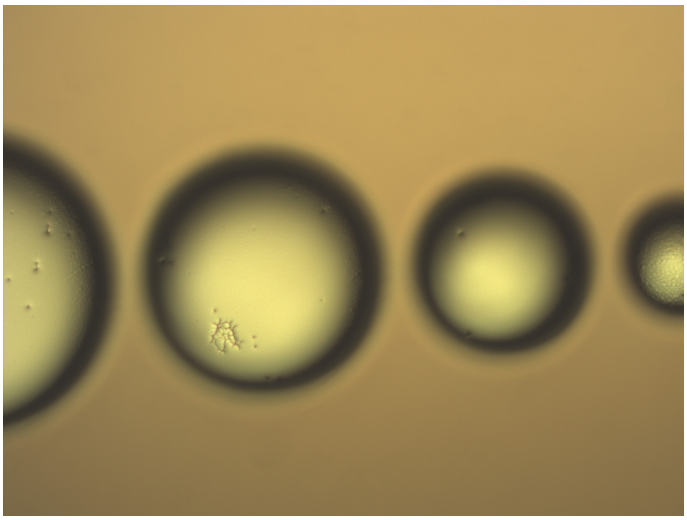
(a) Big back-side holes, 1000 µm, 800 µm, 600 µm and 400 µm from left to right.



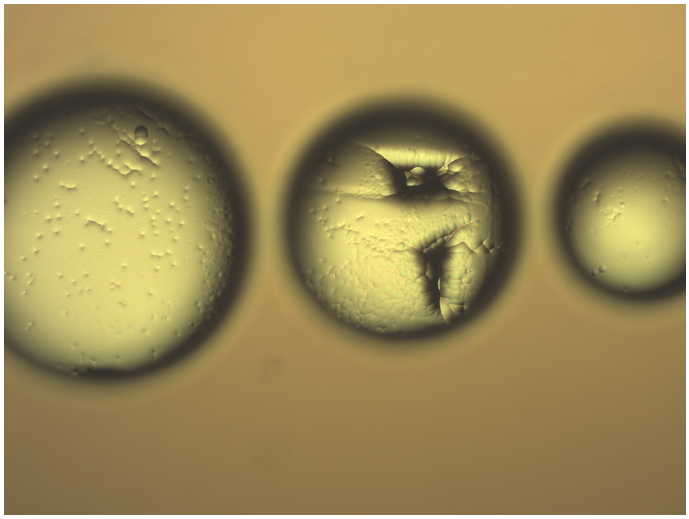
(b) Small back-side holes, 200 µm, 160 µm, 120 µm and 80 µm from left to right.

Figure 4.17: Edges of the large (a) and small (b) back-side holes. Nice features are obtained in this region.

ploited, such as the usage of silicon wafer as sacrificial layer, bonding the membrane on a glass wafer employing a photoresist to make the cavity, as



(a) Well released membranes.



(b) Broken membranes.

Figure 4.18: Inside the back-side membrane region. Some membranes are well released (a), others have some cracks (b) due to the fragility of the structure.

shown in Figure 4.19.

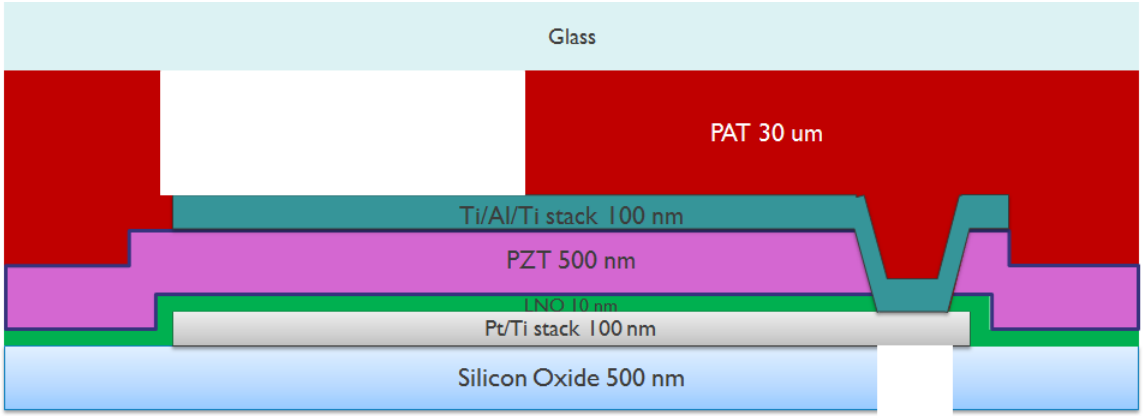
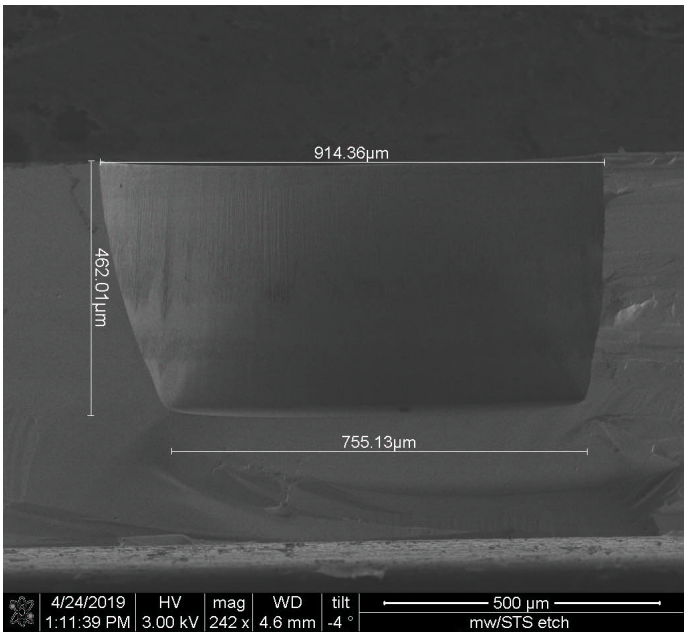
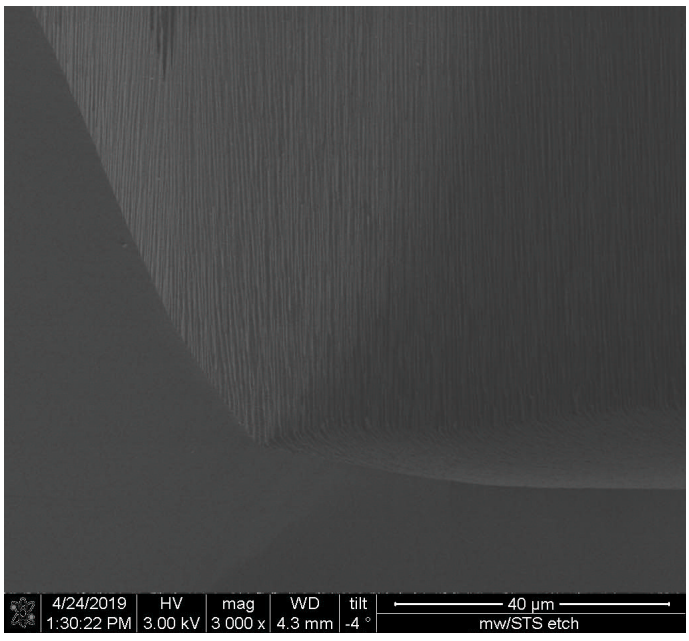


Figure 4.19: Alternative process idea to avoid DRIE. The Si wafer was below the silicon oxide. The Si wafer is bonded with the glass one through the PAT photoresist. After this, the Si wafer is etched away and the SiO_2 is open in the pad regions.

Another problem related to this etching process is the presence of the conductive glue, that is very difficult to remove with standard solvents (Acetone or IPA, for instance). This will lead to a thin layer of glue on top of the membranes, changing the resonant frequency and the device operation. This problem must be solved, for example employing more suitable glues for this kind of etching.



(a) XSEM of the cavity.



(b) XSEM detail of the bottom part.

Figure 4.20: Cavity image (a) and detail of the bottom part of the etched membrane (b). The walls are not straight, sign of a too high passivation, while the bottom of the etching is bended.

Chapter 5

Characterization

5.1 Introduction

In this chapter, the characterization of the PZT material and, subsequently, of the pMUT device is debated. An introduction about the adopted measurement systems is treated. Then, the application of these systems for some studies about the PZT material are investigated, showing some important properties such as the hysteresis loop, the reliability and so on. Afterwards, the pMUT is characterized, mainly in the frequency domain, in order to detect its working point.

5.2 Measurement Systems

5.2.1 Ferroelectric Hysteresis Measurement

One of the main Figures of Merit (FoM) of the PZT material is the hysteresis loop. This FoM is linked with the quality of the crystals and with the leakage current, for instance.

The measurement system procedure is shown in Figure 5.1. The measurement starts with an impulse in time that is sent to the Device Under Test (DUT). In the case of PZT measurement, the DUT is a capacitor where the role of the dielectric is played by the PZT itself. This voltage impulse generates peaks in time in the current characteristic, due to the variation of the

dipoles in the ferroelectric domains. In fact, the domains rotate in order to be aligned with respect to the applied electric field. This motion makes a variation of current in the DUT. After this, the current is integrated over the time and hence the charge is achieved. As we can see from the figure, when the voltage is zero, the current is not zero, as well as the charge, because the domains will not come back to the original, random position, but they tend to maintain the applied field orientation. Finally, the charge is normalized with respect to the area of the DUT and the applied voltage is normalized with respect to the thickness of the DUT. The normalized charge is then plotted with respect to the applied field and the ferroelectric hysteresis loop is achieved. It is worth saying that this kind of measurement will also bias the device, thanks to the sent pulses.

As one could notice, if a leakage current is present in the material, the hysteresis will be modified by this effect, because a superimposition of ideal characteristic and leakage one happens. Ideally, the current should have narrow peaks where the voltage increases or decreases, that will cause an hysteresis loop with a squared shape. Therefore, the larger is the leakage current, the larger is the tilting angle in the hysteresis at zero applied field. Moreover, the remanent polarization (polarization at zero applied field) is strictly related with the charge, hence with the presence of strong dipoles inside the material. It is worth reminding that the dipoles are linked with the piezoelectric effect. Indeed, the net positive and negative charge position of each dipole can vary due to an applied strain and so a voltage is sensed. On the other hand, if a voltage is applied, the dipole distance will vary and hence a strain is sensed. Given that the dipoles are linked with the piezoelectric coefficients, the larger is the remanent polarization, the larger is the piezoelectric quality of the material.

The measurement are performed employing the Keithley 4200, combined with a Pulse Module Unit (PMU) in order to generate the pulses. The other port of the PMU is connected to the probe station, that has the needles for the probing of the DUT. One needle is connected with the bottom electrode, while another one with the top electrode. It is worth highlighting that for each port of PMU and KE4200, the voltage is sent and the current is read, so two cables are needed. In order to probe the small DUT, an optical microscope is employed. One port is for the pulse signal, while the other is for the ground. The maximum pulses that can be sent to the DUT have an

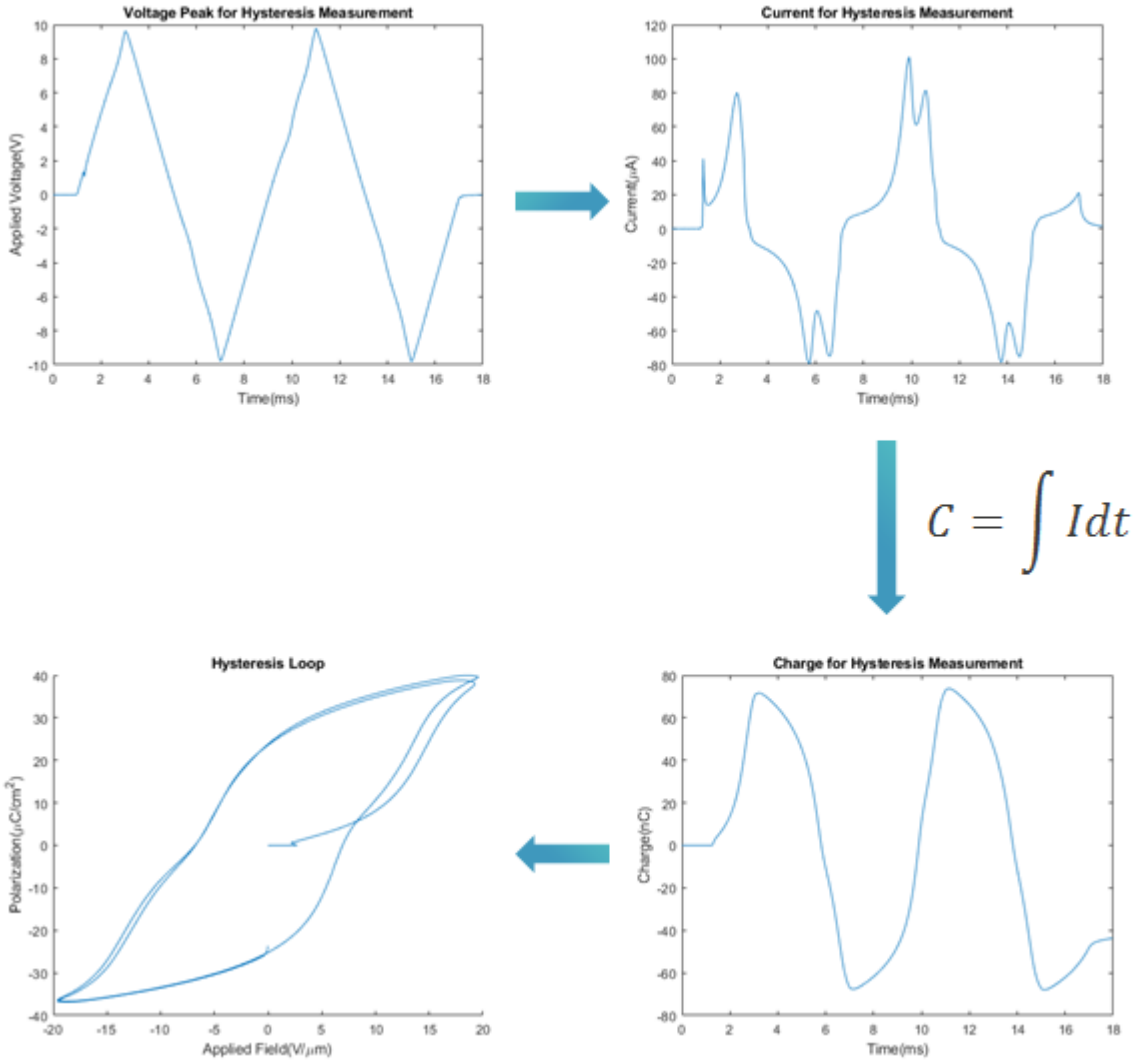


Figure 5.1: Hysteresis loop measurement: First, voltage impulses are sent to the DUT, that generate peaks of current, which are integrated to obtain the charge, and then the charge is normalized by the area of the device and plotted with the applied voltage normalized by the thickness of the capacitor.

intensity of 40 V. The set-up scheme is shown in Figure 5.2.

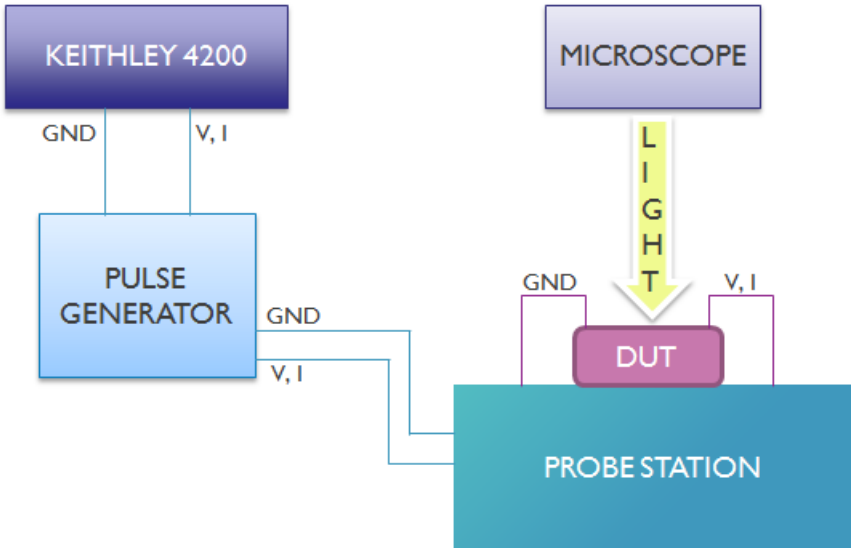


Figure 5.2: Set-up of the ferroelectric hysteresis measurement system. The signal starts from the KE4200, that sets up the pulse and treats the read current. The sent voltage and read current cables are then connected with the pulse generator, in the end connected with the probe station. Finally, the DUT is connected with the probe station through the needles. An optical microscope is utilized to see the DUT.

5.2.2 LDV Measurement

The Laser Doppler Velocimetry (LDV) is a useful measurement technique to detect velocity or displacement of a structure. The working principle is based on the Doppler effect: an object in movement will change the wavelength of the incident laser, thus a shift of the laser frequency is measured. With this effect, one could measure resonant structures, such as PZT capacitors or PZT membranes (due to the piezoelectric effect). It is worth highlighting that the signal must be smaller than the one employed for the polarization of PZT (thanks to Keithley 4200), in order to work in the small signal regime.
This measurement can also detect the displacement, but with less precision because a conversion from velocity to displacement is necessary. In this case, the strain of the material due to the piezoelectric effect can be measured.

The main tool for data treatment of the wavelengths is the Polytec MSU500. The set-up is composed by a laser, a probe station where the DUT is con-

nected with two needles, one for the ground and one for the small voltage signal, that is sent through a wave generator. The wave generator is connected to an oscilloscope, in order to measure and see the wave shape. The laser is perpendicular with respect to the device surface, so when the small signal is applied the reflected beam has a shift of frequency due to the movement velocity of the capacitor or membrane. It is worth noticing that this kind of measurement is possible only if the top part of the DUT is reflective. Given that, in our case we have the top metallic electrode, we can perform the measurement. Finally, the two wavelengths, the original and the shifted one, are treated by Polytec MSU500 in order to obtain the velocity of the capacitor or membrane surface. The set-up scheme is shown in Figure 5.3.

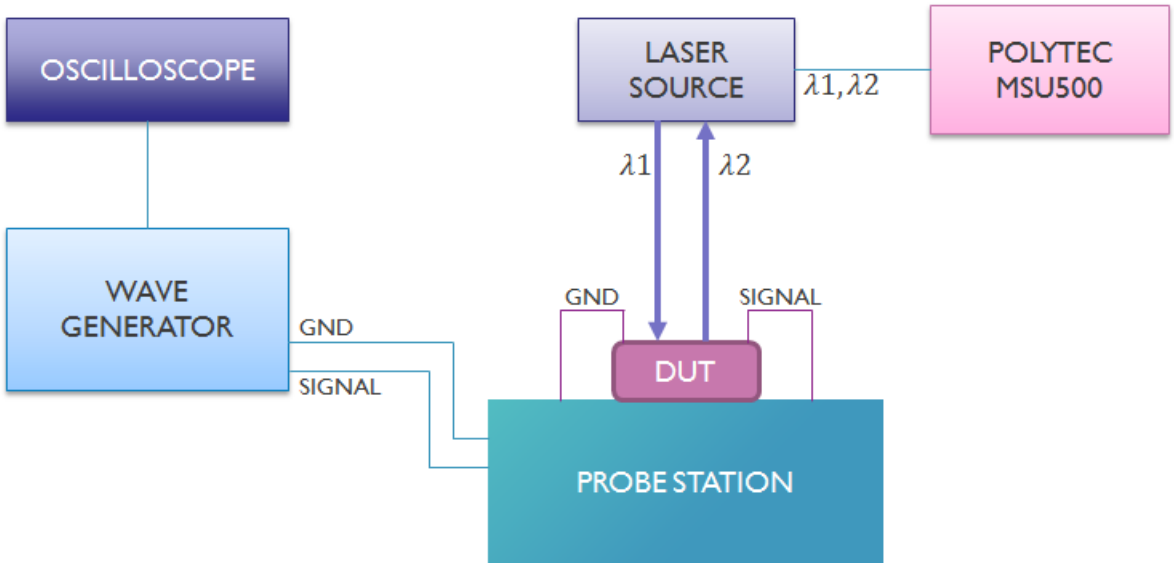


Figure 5.3: Set-up of the LDV measurement system. The voltage signal is generated in the wave generator, displayed by the oscilloscope. The wave generator is connected with the probe station. Finally, the DUT is connected with the probe station through the needles. The laser source sends the light and receives the reflected one, hence the two wavelengths are sent to the Polytec MSU500 for the data treatment to obtain the velocity of the DUT.

5.2.3 LCR Measurement

The last performed electrical measurement regards the inductive, capacitive and resistive behaviour of the DUT. This is an important measurement to link the properties of the DUT with the variation of the dielectric constant, or to detect the loss and compare the variation of it with respect to the resonant frequency. The working principle of this technique is based on the dispatch of a small voltage signal in frequency and the reading of the current. From the ratio between voltage and current, the impedance value is obtained, and from the shift between voltage and current phase, the impedance phase is displayed. Through some filters, only the inductance, capacitance or resistance can be shown. Indeed, it is worth reminding that the impedance has a real part called resistance, that regards the resistive behaviour, and an immaginary part called reactance, that describes the inductance and capacitance behaviour. Hence the role of this filter is to take into account one of these two parts. This measurement is done for each frequencies in a certain domain, therefore the small signal frequency is changed every frequency step.

Moreover, from the capacitance, one could extract the dielectric constant of the material. To do so, we need to look at the capacitance equation:

$$C = \varepsilon_r \varepsilon_0 \frac{A}{t} \tag{5.1}$$

Where C is the capacitance, ε_r is the relative dielectric constant, ε_0 is the dielectric constant in the vacuum, A and t are the capacitor/membrane area and thickness, respectively. The ε_r is material-dependent, so the quality of the PZT can be estimated through this parameter. Moreover, the ε_r is frequency-dependent, with a decreasing behavior with the increase of frequency in the employed frequency range, between 10 kHz and 2 MHz, for the PZT material. This should be due to the lost of a polarization mode. This is a common behaviour of the dielectric constant, that usually drops down with the increase of frequency due to the mode declines. The loss, instead, increases close to the mode decline and then it will decrease again, reaching zero, until another mode decline will be reached.

The main tool for the data treatment is the Keysight E4980A. This tool is connected through two couples of cables to the probe station, one for the signal and one for the ground. The DUT is then probed with two needles by

the station. A small voltage signal is sent and the current is read. These two signals are then treated by the E4980A that measures the magnitude and the phase of them to obtain the properties of the DUT impedance. To probe the small DUT, an optical microscope is employed. The set-up scheme is shown in Figure 5.4.

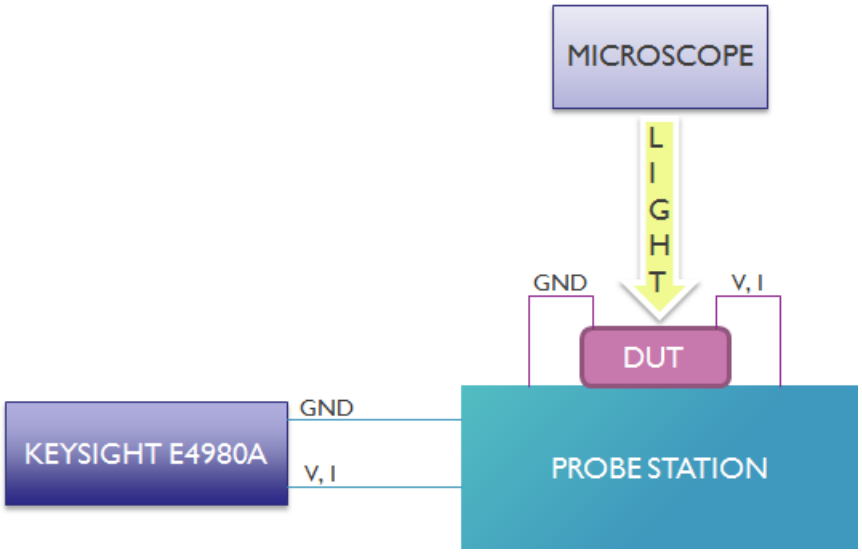


Figure 5.4: Set-up of the LCR measurement system. The voltage signal is sent by the Keysight E4980A, that is connected with the probe station through two couples of cables, one for the signal and one for the ground. The needles of the probe station are then connected to the DUT. An optical microscope is utilized to see the DUT.

5.2.4 XRD Measurement

In order to detect the crystal orientation of the PZT, hence the quality of the material, the X-Ray Powder Diffraction (XRD) is performed. The incident X-ray is sent to the DUT, and the light is scattered with the same angle. The peak is shown if the Bragg law is satisfied:

$$n\lambda = 2d \cdot sin\theta \tag{5.2}$$

Where n is an integer number, λ is the wavelength of the X-ray, d is the

distance between two atoms in the lattice and ϑ is the angle of incidence or reflection of the beam with respect to the surface of the sample. If this law is satisfied, a constructive interference will happen between the reflect beam of the first atom and the other one of the second atom (Figure 5.5).

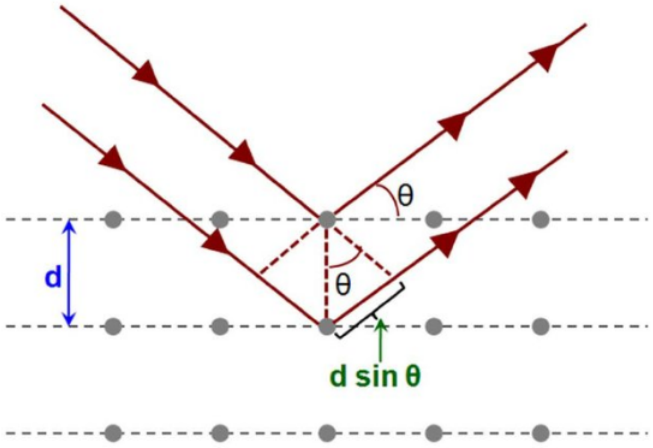


Figure 5.5: Bragg law scheme. The incident light on the sample will be diffracted and if the distance between the atoms is the correct one, a constructive interference appears and the peak is shown on the photodetector [24].

Therefore, this technique is very useful if one wants to detect the orientation of the crystals in a sample and the relative quantity of them. This is extremely helpful in our case, because the properties of the PZT are strictly linked with the relative concentration of orientations (see subsection 5.3.6). The peaks for our stack are shown in Figure 5.6. As one could appreciate, different peaks are present in the picture, but not all of them belong to PZT. One could distinguish four main regions of PZT orientation, collected in Table 5.1. As we will discuss in subsection 5.3.6, PZT (100) and (110) play an important role in the material properties.

Orientation	Angle 2ϑ
PZT (100)	21.5°
PZT (110)	31°
PZT (111)	38.4°
PZT (200)	44°
Pt (111)	39.9°
Si (400)	69°

Table 5.1: Angle 2ϑ for each crystal orientation.

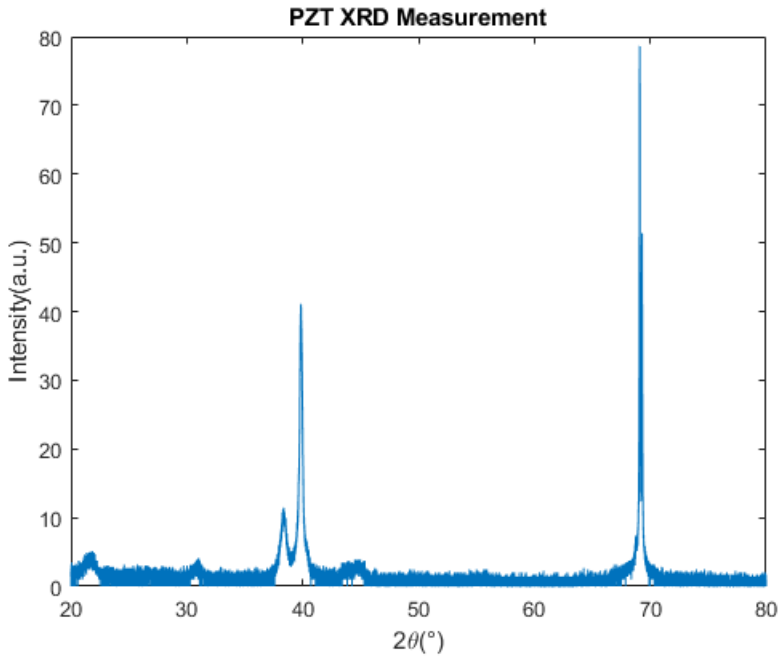


Figure 5.6: XRD peaks for a PZT on Pt/Ti/SiO_2/Si stack.

5.3 PZT Characterization

5.3.1 Introduction

This section contains a deep comparative study between the Sol-gel and the PLD PZT. The reason behind this comparison is to achieve a better understanding of the PZT properties and to know which PZT process is the best

for large area substrate applications. Moreover, four top electrode materials are tested and compared to find the best combination: Au, Al, Pt/Ti, Ti/Al/Ti. For all the tests, a 500 nm thick PZT is employed, with the exception of subsection 5.3.6, where a 1.1 µm is utilized.

5.3.2 Hysteresis Loop Comparison

Given that the bottom electrode is exploited as seed layer for the PZT crystal growth, hence it cannot be changed, a study about the best top electrode material is performed.
The first investigated Figure of Merit (FoM) is the ferroelectric hysteresis. From here, some PZT properties are compared, like the remanent polarization (Pr), that is linked with the dipoles strength and piezoelectric coefficients, or the tilting angle at zero applied field (φ_{TA}), that is linked with the leakage current (see subsection 5.2.1). Four top electrode materials are chosen: Au, Al, Pt/Ti, Ti/Al/Ti. The PZT thickness is 500 nm and 20 V peak-to-peak pulses are employed in the measurement. These tests are performed on the PZT capacitor, that is composed of top electrode, PZT and bottom electrode only.

The hysteresis loops are shown in Figure 5.7. As one could see from the picture, the PLD PZT has lower Pr and higher φ_{TA} than the Sol-gel one, hence the material has a lower dipole strength and higher leakage current. On the other hand, the PLD PZT has lower coercive field (E_C) than the Sol-gel one, thus the poling requires less voltage.
Moreover, as one could appreciate from the figure, the best Pr is obtained with Ti/Al/Ti top electrode. Therefore, we could say that the Sol-gel PZT with Ti/Al/Ti top electrode has the best performances related to the hysteresis loop parameters. Looking at the best Pr for Sol-gel (25 µC/cm^2 with Ti/Al/Ti) and for PLD (11 µC/cm^2) PZT, one could appreciate the huge difference of response.

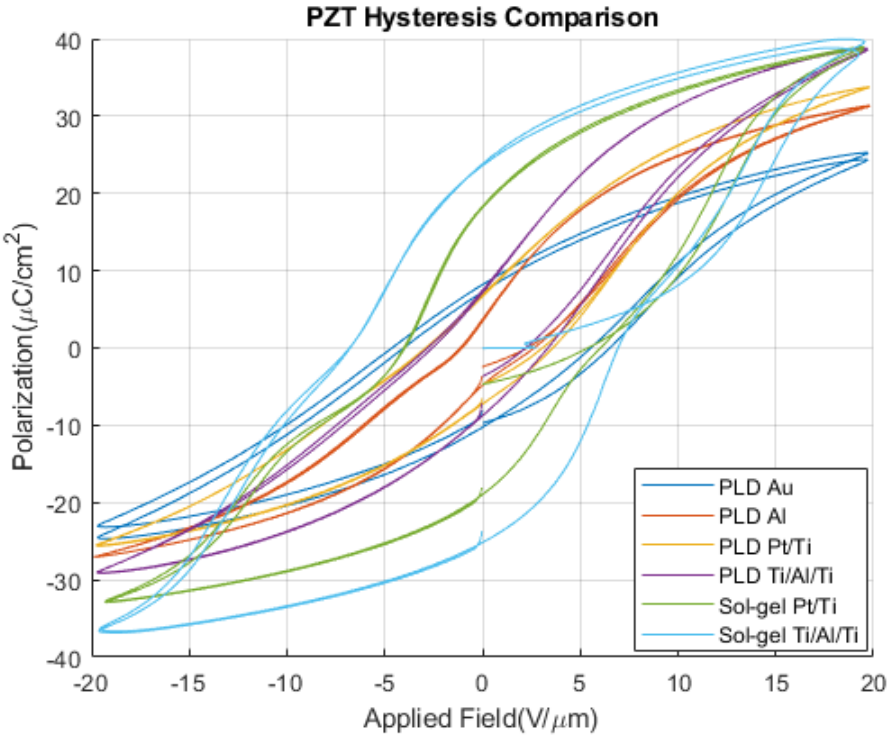


Figure 5.7: PLD and Sol-gel PZT hysteresis loop comparison.

5.3.3 Fatigue Comparison

After the hysteresis loop, the reliability of the PZT is tested, in order to see how many pulsing cycles are necessary to have a degradation of the Pr. This FoM is also called fatigue, as we discussed in subsection 2.2.4. The same materials for the top electrode are utilized, as well as the same 500 nm thick PZT and 20 V peak-to-peak pulses. As well as for the hysteresis measurements, these tests are performed on the PZT capacitor, that is composed of top electrode, PZT and bottom electrode only.

The measurement results are shown in Figure 5.8. As one could see from the figure, the Sol-gel PZT has the largest Pr, but after 10^2 and 10^3 cycles for Ti/Al/Ti and Pt/Ti top electrode, respectively, the Pr drops dramatically. On the other hand, the PLD PZT have a constant behaviour for the entire range of analysis, which is up to 10^5 cycles, with the maximum of Pr

with Ti/Al/Ti electrode. This could be due to a degradation of the switching mechanism, when the ferroelectric domains have to change the orientation according to the applied field. Increasing the cycles the ferroelectric dipoles could respond less and less, reducing the polarizability of the material. Indeed, the PLD PZT has a better mechanism of crystallization, due to the controlled atmosphere of the sputtering process with respect to the Sol-gel PZT, that is crystallized in air, thus more defects can be embedded in the lattice. These defects can reduce the polarizability of the material, due to stress formation in the lattice that impedes the correct switching of the ferroelectric dipoles inside the domains.
Given the superior properties (Pr and fatigue) of Ti/Al/Ti, it will be the final choice for the pMUT top electrode.

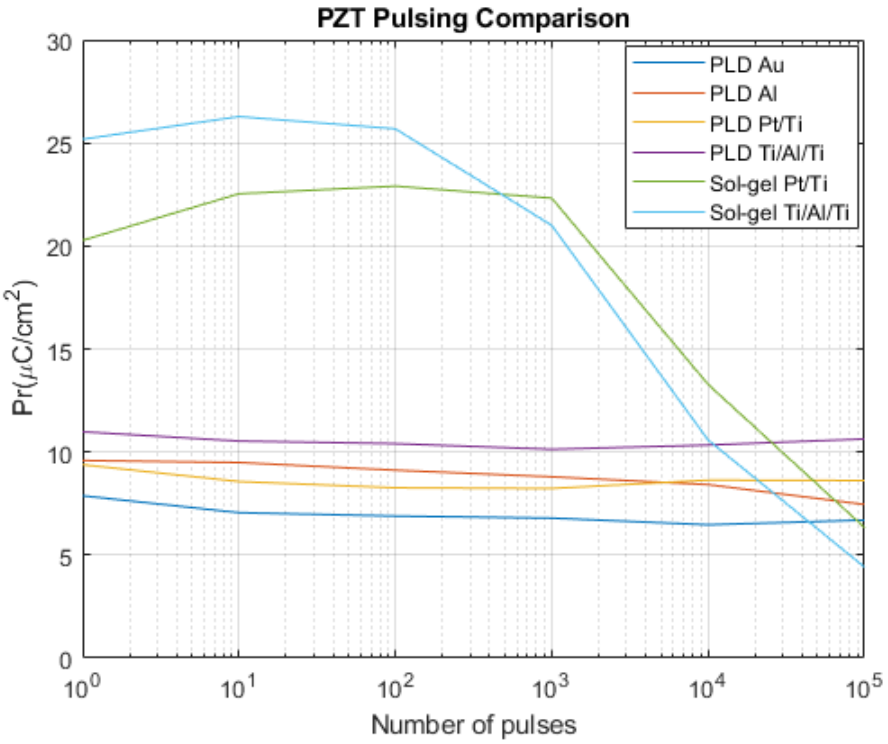


Figure 5.8: PLD and Sol-gel PZT pulsing comparison. Pr versus the number of pulses is plotted. The Pr of Sol-gel PZT is larger but after 10^3 cycles it drops down. Instead, PLD PZT is constant until 10^5 cycles.

5.3.4 Working Voltage Comparison

Another important FoM is the working voltage of the devices. In order to have a criteria to compare the two processing techniques of PZT, a definition of working voltage must be delineated. To do so, the concept of $V_{90\%}$ is introduced: It is the voltage from which an increase of 1 V peak implies an increase of less than 10% of the Pr. In this way, one could know how much voltage is required to have a good value of Pr. In our case, this voltage must be applied before the operation of the pMUT, and then the driving signal will be a smaller one. It is an useful FoM, especially for actuators. Given that the Ti/Al/Ti is the best top electrode material in terms of Pr and fatigue, only the results with this material are shown in Figure 5.9. As one could appreciate from the picture, both Sol-gel and PLD PZT have the same Pr at low voltage. Then, after about 12.5 V µm^{-1}, Sol-gel PZT rises faster with respect to the applied voltage (normalized by the thickness), and the $V_{90\%}$ is reached at 25 V µm^{-1}, while the $V_{90\%}$ for PLD PZT is only 17 V µm^{-1}. This means that the PLD PZT is easier to drive than the Sol-gel one, because with less voltage the majority of the ferroelectric domains can be aligned, hence the piezoelectric effect is boosted. Nevertheless, the Pr of Sol-gel PZT is larger than the PLD one, thus the Sol-gel can be exploited at less working voltage.

5.3.5 Breakdown Voltage Comparison

The working voltage can be increased up to a certain threshold, after which spots appear on the device's surface (Figure 5.10). This threshold is called Breakdown Voltage (V_{BD}), and it is an important FoM to know the quality and the working range of the device.
The measured V_{BD} for different top electrode contacts are collected in Table 5.2. As one could notice from the table, the Sol-gel PZT has much higher breakdown voltage than the PLD one. In general, Pt/Ti and Ti/Al/Ti top electrodes have the best result both for Sol-gel and for PLD PZT. For this reason, probably the surface interactions play an important role in the breakdown process, because both the stacks have titanium as contact metal with PZT. Nevertheless, more studies should be made on this subject, mostly because there is confusion on the topic and the exact breakdown mechanisms are unknown. Principally, we can say that these spots could be due to the

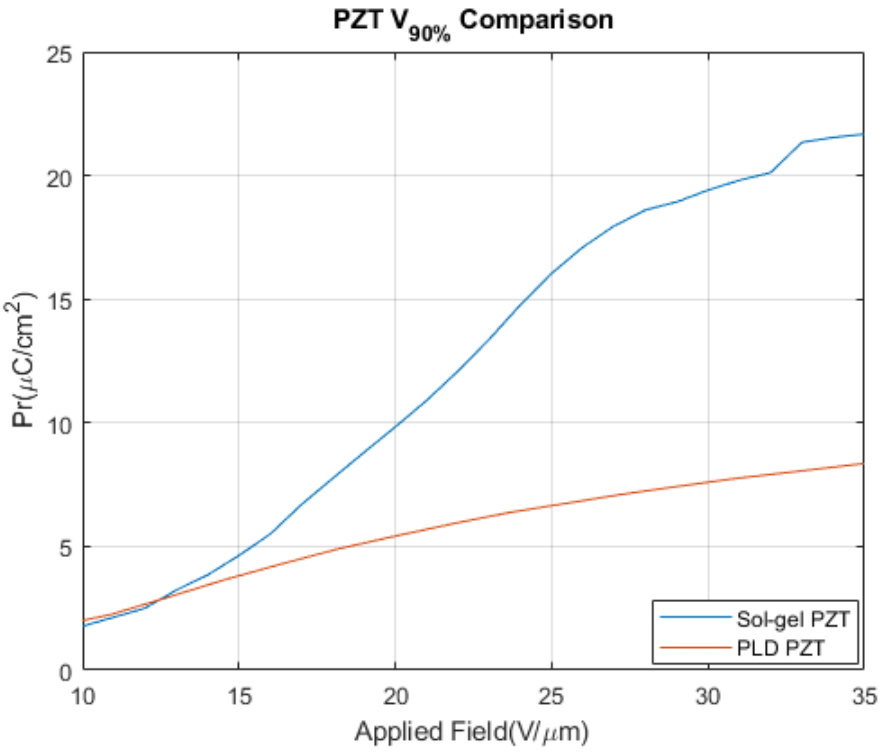


Figure 5.9: PLD and Sol-gel PZT $V_{90\%}$ comparison. The PLD $V_{90\%}$ is $17\,\mathrm{V\,\mu m^{-1}}$, while the Sol-gel one is $25\,\mathrm{V\,\mu m^{-1}}$.

creation of percolation paths inside the material, as for every dielectric materials. Moreover, this mechanism is not only voltage but also time-dependent: The spots can appear with the first or after several pulses. The chosen criteria to set a safe point is the non-presence of spots after 10^5 cycles, that is a very large number of pulses considering that the pulse is employed only to polarize the material, that will remain polarized for long time before a new pulse is needed.
It is worth mentioning that these breakdown voltage values are calculated in the pulsing domain, because in DC voltage these values are almost halved, due to the stronger stress caused in the material. This is extremely important if one wants to polarize the PZT with a constant voltage: in this case, the $V_{90\%}$ must be halved, to prevent the breakdown.

Type	$\mathbf{V_{BD}}$
PLD Au	$30\,\mathrm{V\,\mu m^{-1}}$
PLD Al	$30\,\mathrm{V\,\mu m^{-1}}$
PLD Pt/Ti	$40\,\mathrm{V\,\mu m^{-1}}$
PLD Ti/Al/Ti	$40\,\mathrm{V\,\mu m^{-1}}$
Sol-gel Pt/Ti	$60\,\mathrm{V\,\mu m^{-1}}$
Sol-gel Ti/Al/Ti	$60\,\mathrm{V\,\mu m^{-1}}$

Table 5.2: Breakdown voltage for different top electrode materials and PZT deposition techniques.

Figure 5.10: Breakdown effect on the capacitors. Spots appear on the surface of the devices probably due to the diffusion of the electrode material and the burning of some sites.

5.3.6 PLD PZT Unevenness

In this subsection the reason why PLD PZT is not a suitable process for large area applications will be explained. The tests are made on a 4 inches wafer (100 mm). 1.16 µm of PLD PZT are deposited on top of a 4 inches Si wafer

with 500 nm of SiO_2 and Pt/Ti bottom electrode. The scheme of the wafer is shown in Figure 5.11.

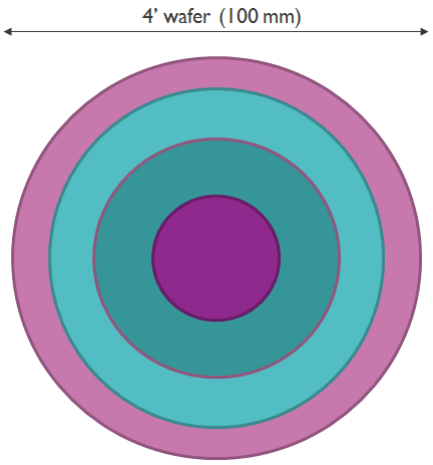


Figure 5.11: Graphic representation of the 4 inches PLD PZT wafer. The wafer appears with concentric rings of different colours.

As one could appreciate from the picture, the wafer has concentric rings of different colours. First, one could think that this effect is due to thickness variation in the deposition process. Therefore, the thickness profile is measured, shown in Figure 5.12. The measurement is done both for x-axis and for y-axis, considering the x-axis parallel to the big flat edge of the Si (100) wafer. but the maximum variation is only 70 nm, that is too small for a change in the colour of the material.

Thus, the XRD measurement is performed in order to check if the colour variation is linked with a crystal orientation variation, associated to a different interaction with the light. As one could see from Figure 5.13, there is a variation of crystal orientation moving along the diameter in x and y directions.

In particular, the (100) orientation is mainly present in the center of the wafer, while after 1 cm is principally (110). After the (100) orientation region, the XRD behaviour is oscillating. A better detail to appreciate this oscillating region is shown in Figure 5.14. This is very coherent with the

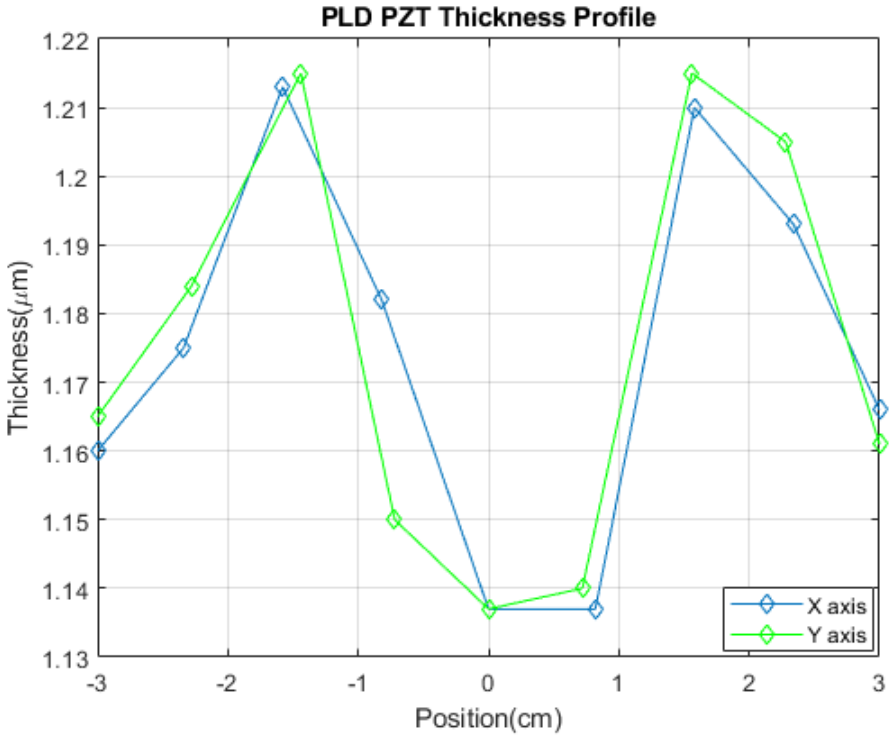
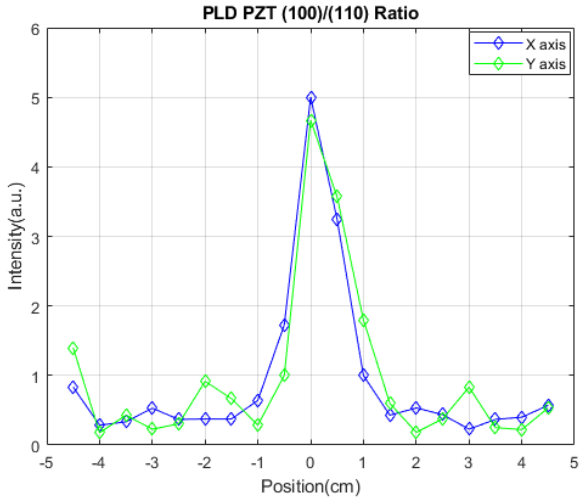


Figure 5.12: Thickness profile of the PLD PZT deposited on 4 inches wafer. The maximum variation of thickness is only 70 nm, hence no colour variation should be linked with this.

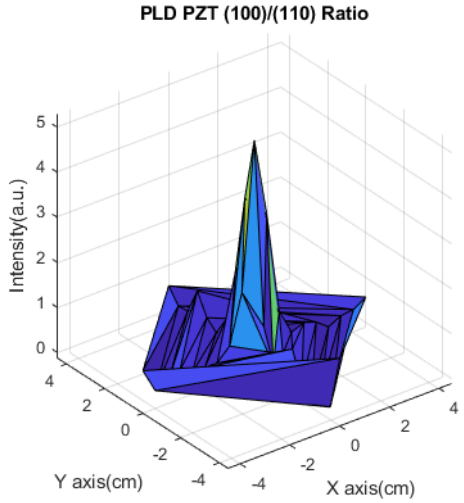
hypothesis of variation of colour due to variation of crystal orientation.

After the XRD measurements, the Ti/Al/Ti top electrode capacitors are fabricated with this wafer and electrically tested. First, the remanent polarization (Pr) is measured along the wafer diameter, for a pulse at $V_{90\%}$ for PLD PZT, that is $17\,\mathrm{V\,\mu m^{-1}}$. The results are displayed in Figure 5.15. As one could notice from the picture, the minimum of Pr appears when the crystal orientation is mainly (100), while it increases when we approach the edges, at (110) orientation. This is very important to understand which orientation is the most useful for our purposes.

Another electrical measurement is the LDV one, that can detect strain in the material. As one could see from Figure 5.16, the maximum value of the



(a) 2D View.



(b) 3D View.

Figure 5.13: 2D View (a) and 3D View of (100)/(110) orientation ratio. (100) orientation is predominant at the center of the wafer, becoming less and less moving along the radius.

strain is reached in the center, where the polarization is the lowest, while decreasing going toward the edges of the wafer. This is another important

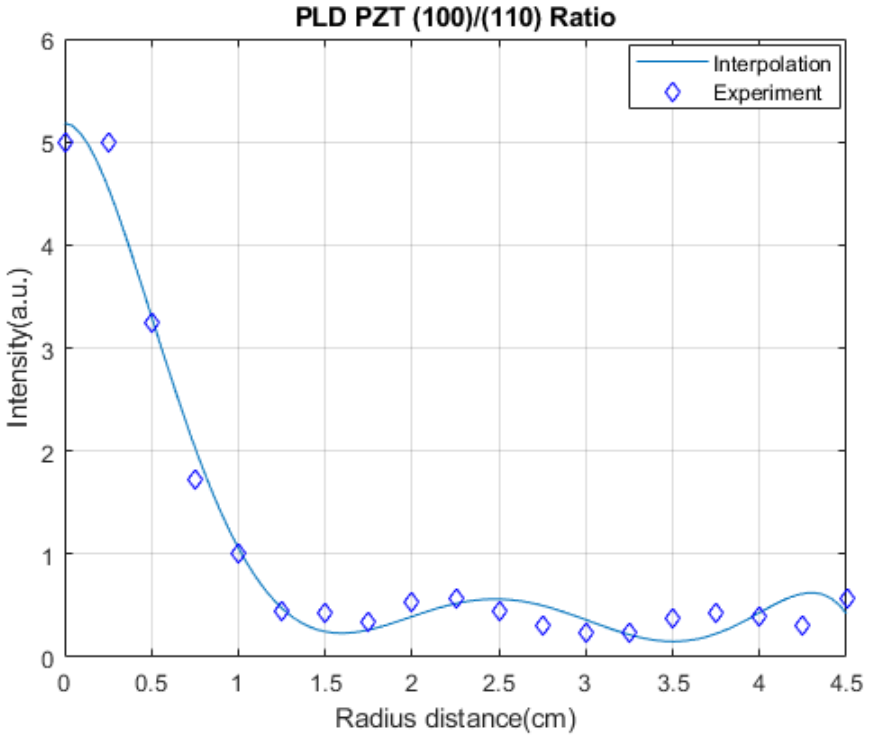


Figure 5.14: (100)/(110) orientation ratio along a radius with more points in order to see the oscillating behaviour after 1.

criterion for the evaluation of the PZT properties.

Thanks to these comparisons among different FoMs, we can say that the (100) orientation gives the minimum Pr but the maximum strain in the material, while (110) is the other way around.

5.4 pMUT Characterization

5.4.1 Introduction

In this section we will discuss about the characterization of the final pMUT device, hence what are the main differences with respect to a capacitor when the membrane is released. The pMUT under study has the Ti/Al/Ti top

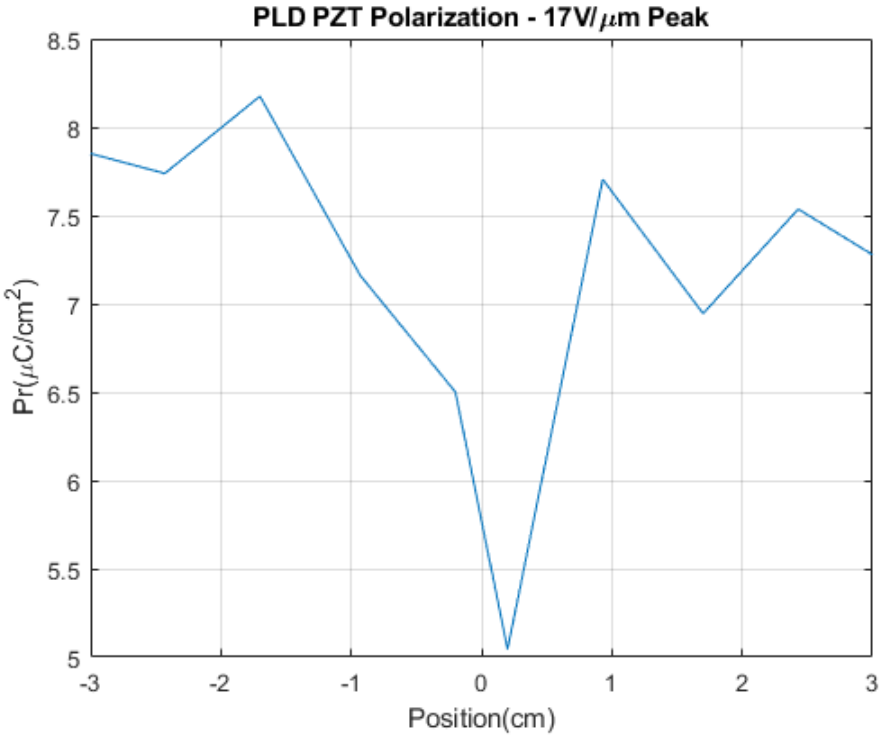


Figure 5.15: Pr along the diameter with a pulse peak of 17 V µm^{-1}. Lowest Pr in the center, where the orientation is mainly (100), becoming larger and larger approaching the edges, where the orientation is practically (110).

electrode, due to the superior properties, and the Sol-gel PZT, due to the higher performances and uniformity than PLD one, as we discussed in section 5.3. The chosen device has a membrane size of 1 mm diameter, with top electrode of 800 µm diameter, which is the largest, and the reason to test this large membrane will be explained. Moreover, the detection of the resonance is treated. For this analysis, LCR and LDV are principally adopted.

5.4.2 Resonance Detection

First, the resonance is detected exploiting the LDV technique. In this way, the velocity of the suspended membrane can be measured and, sweeping over a range between 1 kHz and 2 MHz, the highest response can be detected to see

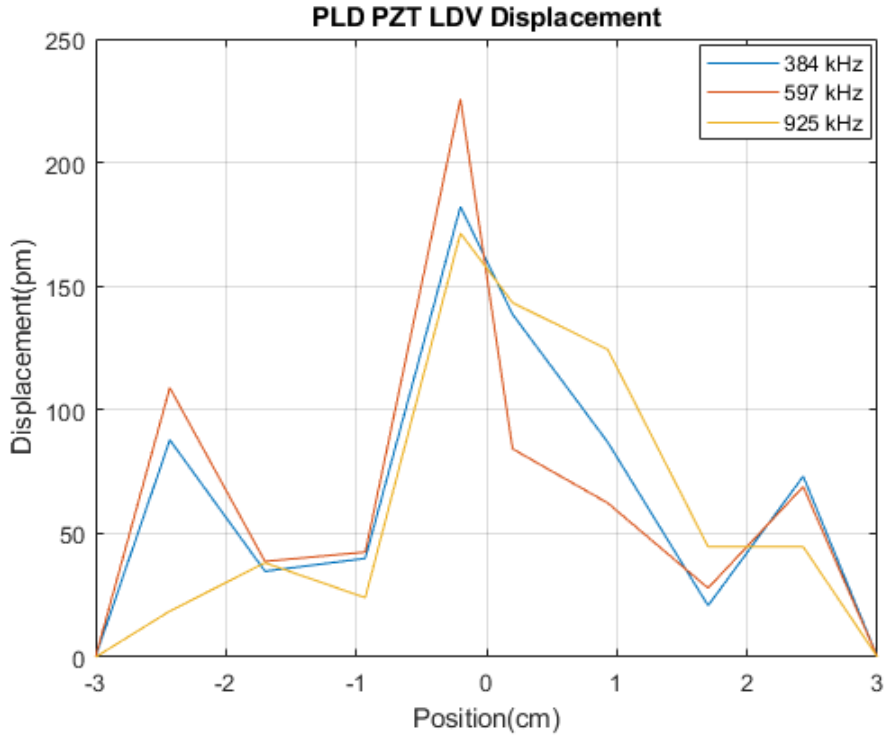


Figure 5.16: Displacement along the diameter with a small signal of $0.86\,\mathrm{V\,\mu m^{-1}}$ for three modes. The maximum strain is present in the center, where (100) orientation is dominant.

the resonance shape and position. As one could appreciate from Figure 5.17, the resonance is displayed at 1.35 MHz. The resonance shows different subpeaks and some noise, and the signal itself is not very high; furthermore the resonance position is at too high frequency comparing to the expectation. In fact, for a 1 mm diameter and 1 µm thick membrane, the resonance should be at hundreds of kHz. These problems are probably due to the Bosch process issues, already explained in subsection 4.8.4, but we will quickly sum up here: The back-side etching with Bosch process, even if corrected to make it stable during time, has some issues related especially to tilted walls and bending of the bottom side of the etching well. Therefore, the tilted walls will reduce the membrane size and so the frequency of the membrane will raise up. On the other hand, the bended bottom side of the etching will create a non-uniform membrane, that is thicker at the edges and becomes

thinner and thinner toward the center. A graphical representation of it is shown in Figure 5.18.

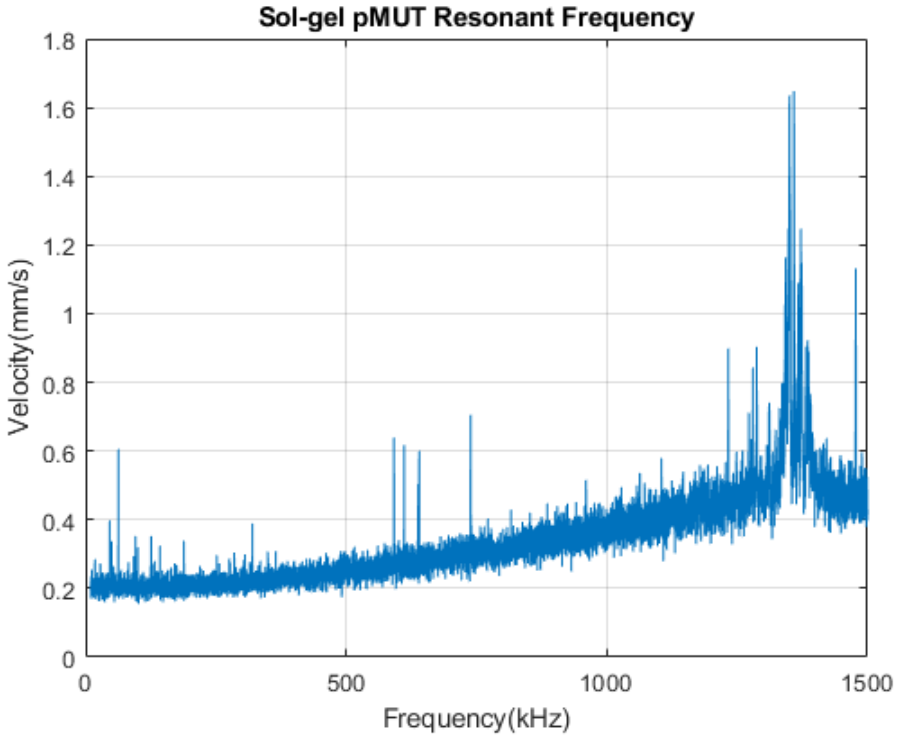


Figure 5.17: LDV Velocity measurement. The resonance is detected at 1.35 MHz

5.4.3 Resonance Consistency

After this analysis, the consistency of the resonance is verified with LCR measurement of impedance and capacitance. In particular, we are interested in the behaviour of the impedance phase and the dielectric loss. The graphs are shown in Figure 5.19.

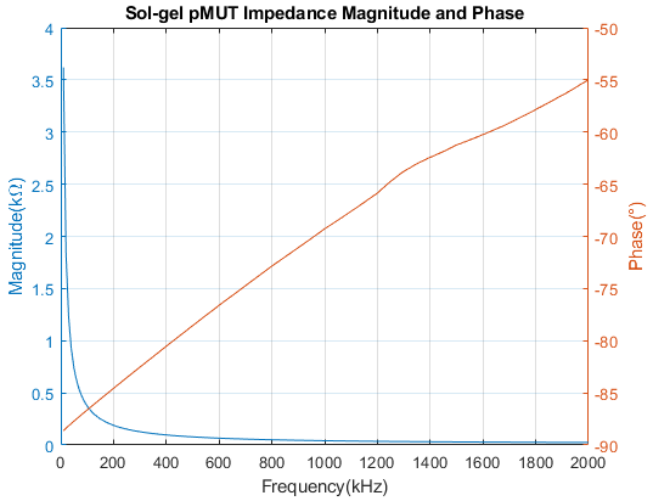
First, we will discuss about the impedance magnitude and capacitive behaviour. The impedance can be easily understood if one thinks about the

Figure 5.18: Graph with the desirable membrane (left) and with the obtained one after Bosch process (right). The radius membrane is reduced, and the bottom part is bended. The electrodes are removed for the sake of clarity.

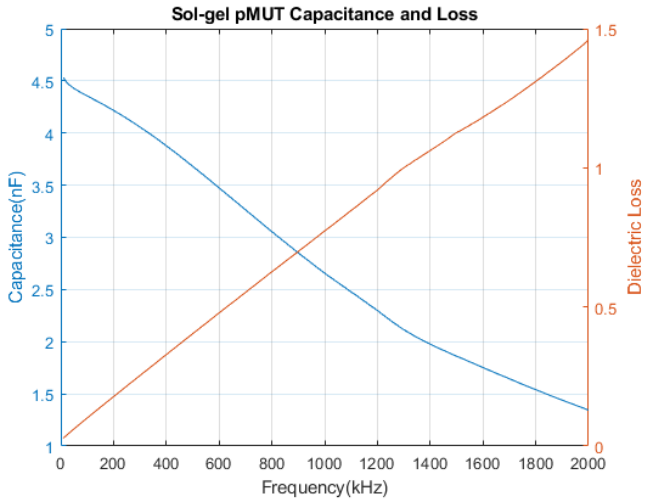
PZT between two electrodes system: at low frequencies, the system is a capacitor, and the dielectric can response well to the applied signal, but if the frequency increases, the capacitor becomes a short circuit and just the resistance is measured. Therefore, at low frequency, a huge magnitude is present, due to the capacitive effect, while at high frequency just the resistance is detected, showing a small magnitude.
On the other hand, looking the capacitance graph, we can see a big capacitance at low frequency, that decreases at high frequency. This problem is due to the loss of polarization modes, that we discussed in subsection 5.2.3. Mainly, the decrease of the capacitance value is linked with a difficulty of the material to polarize itself when a signal is applied.
From the capacitance magnitude, the relative dielectric constant (ε_r) can be extracted, reversing the Equation 5.3 and supposing a linear behaviour of the curve:

$$\varepsilon_r = -k \cdot f + 658 \tag{5.3}$$

Where k is a constant with a value of -2.39·10^{-3}s, and f is the frequency. As one could appreciate from the low value of the dielectric constant, the PZT is affected by a strong leakage, otherwise ε_r would be larger. Furthermore, comparing the pMUT impedance magnitude with the ideal case in the model (Figure 3.3 in subsection 3.2.2), it drops to a low value very quickly, with an hyperbolic behaviour. This can explained again by the leakage that affects the PZT under test. In this case, the material is much more resistive than the ideality.
Therefore, these parameters are another way to estimate the quality of the



(a) Impedance Magnitude and Phase.



(b) Capacitance Magnitude and Losses.

Figure 5.19: Impedance (a) and capacitance (b) behaviour in frequency, between 1 kHz and 2 MHz, employing LCR meter. The resonance and anti-resonance are difficult to detect due to the low response of the membrane.

PZT layer regarding the dielectric properties.

Now, we discuss about the impedance phase and the dielectric loss. Here we

can find the consistency with the resonant frequency of 1.35 MHz. Looking the impedance phase, one could appreciate the linear variation of the phase, starting from -90°, value for a capacitor, and reaching -55°, that means a mix between capacitive and resistive behaviour. But looking at about 1.35 MHz, a little hillock appears.
Now, if we look the dielectric loss, we can see the same increasing behaviour, and a little hillock at 1.35 MHz is present again. These two hillocks are due to the mechanical system that is coupled for that frequency zone with the electrical one. Hence, in this point, the impedance phase has additional lumped elements due to the coupling with the mechanical system linked with a variation of phase. On the other hand, the coupling of energy of the electrical system with the mechanical one causes an increase of the loss, that we can appreciate from the capacitance plot.

Nevertheless, even if the hillocks are displayed, they are tiny, especially if the impendance phase is compared with the ideal case (Figure 3.3 in subsection 3.2.2). This means that a bad coupling of the signal with the system is present, hence this generates a small loss. Moreover, the impedance magnitude should displayed a resonance and anti-resonance, as discussed in subsection 3.2.2, but in this case the signal is so small that a flat curve near the increase of phase (1.35 MHz) is only shown. These effects are probably linked with the Bosch process issues. Further improvement of the pMUT processing must be performed in order to get rid of these problems.

Chapter 6

Conclusion

In conclusion, the process development of the piezoelectric micromachined ultrasound transducer (pMUT) with Lead Zirconate Titanate (PZT) active material was performed, followed by the characterization of the PZT layer and the device.

The device process flow (chapter 3) was discussed and all the process steps were treated in the development part (chapter 4). A nice critical dimension (CD) for PZT patterning was reached with BHF/HCl wet etching cycles (10 µm), but further improvement can be achieved improving the cycling time. Nevertheless the CD of the pMUT masks was 20 nm, therefore the integration objective was accomplished. Moreover, the lift-off patterning of the Ti/Al/Ti top electrode was well developed, achieving a CD of 3 µm. Finally, the back-side etching with Deep Reactive Ion Etching (DRIE) Bosch process employing SF_6 and C_4F_8 gasses was developed and improved. An Al_2O_3 ALD-deposited was utilized as hard mask, thanks to the very low etching rate under the employed plasma atmosphere ($0.3\,\mathrm{nm\,min^{-1}}$). After different tests, the Bosch process was stabilized and a constant silicon etch rate of $2.2\,\mu\mathrm{m\,min^{-1}}$ was achieved. The DRIE process was characterized employing X-SEM, in order to check the cross-section of the etching region.

Then, the PZT was characterized, deposited with two main techniques: Sol-gel and Pulsed Laser Deposition (PLD). The advantages and drawbacks of each one were treated and analyzed, as well as different top electrode materials. In general, the Sol-gel PZT displayed more uniformity, with larger remanent polarization Pr ($11\,\mu\mathrm{C/cm^2}$ for PLD compared to $25\,\mu\mathrm{C/cm^2}$ for

Sol-gel with the best device), smaller leakage-related tilting angle φ_{TA} and larger breakdown voltage V_{BD} ($40\,V\,\mu m^{-1}$ for PLD compared to $60\,V\,\mu m^{-1}$ for Sol-gel with the best device) than the PLD PZT, but the latter showed a better fatigue (no Pr drop after 10^5 hysteresis cycles), smaller working voltage $V_{90\%}$ ($17\,V\,\mu m^{-1}$ for PLD compared to $25\,V\,\mu m^{-1}$ for Sol-gel) and lower deposition temperature. Regarding the comparison among Au, Al, Pt/Ti and Ti/Al/Ti top electrodes, the results showed the maximum of Pr ($25\,\mu C/cm^2$) and the best V_{BD} ($60\,MV\,\mu m^{-1}$) with Sol-gel PZT and Ti/Al/Ti material. For these reasons, the Sol-gel PZT with Ti/Al/Ti top electrode was chosen to perform the back-side etching and release the membrane.
A study related to the PLD PZT non-uniformity was carried out, and important relationships among the crystal orientation, Pr intensity and strain generation were observed. In particular, the higher the (100) orientation is, the smaller the Pr is and the larger the strain is. With the (110) orientation is all the way around. Nevertheless, a deeper study must be performed in order to understand exactly the link among these parameters.
The pMUT with Sol-gel PZT and Ti/Al/Ti top electrode was then characterized, exploiting the LCR and LDV measurements. The resonance was observed at 1.35 MHz for 1 mm diameter membrane, with a small and broad peak. This result is not coherent for a 1 µm thick membrane with 1 mm diameter. In fact, the resonance should be around hundreds of kHz. The reason of the resonance shift and broadening was probably due to the Bosch process step, that we saw having not straight walls and a bended bottom etching part was present. These two issues caused a variation of the actual membrane size, that became thicker and smaller, therefore the larger resonant frequency was explained. Moreover, the bended bottom part of the membrane caused the broadening of the resonance, because the membrane was not ideal anymore.
If Bosch process could not be improved, different process flow solutions must be considered, such as the usage of silicon wafer as sacrificial layer, bonding the membrane on a glass wafer employing a photoresist to make the cavity (Figure 4.19 in subsection 4.8.4).

In conclusion, the development of the pMUT actuator was an overall success:

- The PZT process development part was carried out with a nice CD and low level of damage.

- The Bosch process DRIE was improved and the stability of the process was reached.
- The PZT was studied and important FoMs were obtained and exploited for the final device.
- The Ti/Al/Ti top electrode was chosen thanks to the extracted PZT FoMs comparison.
- The pMUT actuator was not perfectly developed, but even if the membrane did not show a nice resonance, the signal was above the noise level, thus a movement of the membrane was achieved.

In general, a better understanding of the device properties and performances was obtained.
Nevertheless, more effort are needed to strengthen the knowledge about PZT and pMUT and therefore improving the process integration, reliability and resonance. On the other hand, improvement of the Bosch process is the main issue to tackle, in order to enhance the membrane release and resonance quality.

Bibliography

[1] *https://blog.onscale.com/which-transducer-type-is-best-for-ultrasonic-fingerprint-sensing-cmut-pmut-or-pzt*

[2] *Joontaek Jung et al; Review of piezoelectric micromachined ultrasonic transducers and their applications; 2017 J. Micromech. Microeng. 27 113001*

[3] *Ashutosh Kumar Tripathi, Ishan Choudhary, Deepak; Advances in Flexible Thin-Film Transistors and Their Applications; SMC Bulletin Vol. 8 (No. 2) August 2017*

[4] *Suvrajyoti Mishra, Lakshmi Unnikrishnan, Sanjay Kumar Nayak, and Smita Mohanty; Advances in Piezoelectric Polymer Composites for Energy Harvesting Applications: A Systematic Review; Macromol. Mater. Eng. 2018, 1800463*

[5] *Kam K. Leang, Gina Pannozzo, Qingze Zou, Santosh Devasia; A Collaborative Approach to Teach Modeling and Control of Smart Actuators in the Mechanical Engineering Curriculum; ASME 2007 International Mechanical Engineering Congress and Exposition*

[6] *R.S. Dahiya, M. Valle; Robotic Tactile Sensing; Springer Science+Business Media Dordrecht 2013*

[7] *Srinivas Tadigadapa; Piezoelectric microelectromechanical systems — challenges and opportunities; Proc. Eurosensors XXIV, September 5-8, 2010, Linz, Austria*

[8] *D. Damjanovic; The Science of Hysteresis; Volume 3, I. Mayergoyz and G. Bertotti (Eds.), Elsevier, 2005.*

[9] *Kamel, T. M. (2007); Poling and switching of PZT ceramics : field and grain size effects; Eindhoven: Technische Universiteit Eindhoven*

[10] *Dragan Damjanovic;Ferroelectric, dielectric and piezoelectric properties of ferroelectric thin films and ceramics; Rep. Prog. Phys. 61 (1998) 1267–1324*

[11] *Al-Shareef H N, Dimos D, Warren W L and Tuttle; B A 1997 Integr. Ferroelectr. 15 53*

[12] *https://www.ytca.com/lead_free_piezoelectric_ceramics.html*

[13] *Sumit Pramanik, Belinda Pingguan-Murphy, and Noor Azuan Abu Osman; Developments of Immobilized Surface Modified Piezoelectric Crystal Biosensors for Advanced Applications; January 2013 International journal of electrochemical science 8(6):8863-8892*

[14] *G.D. Shilpa et al 2016 IOP Conf. Ser.: Mater. Sci. Eng. 149 012190*

[15] *R. Steinhausen, C. Pientschke, A. Z. Kuvatov, H. T. Langhammer, H. Beige, A. A. Movchikova, O. V. Malyshkina; Modelling and characterization of piezoelectric and polarization gradients; February 2008 Journal of Electroceramics 20(1):47-52*

[16] *Zhipeng Qi, Guohua Hu, Qin Zhu, Lixing Zhang, Manqing Li, and Yiping Cui; Inductively coupled plasmas (ICP) etching of PZT thin films for fabricating optical waveguide with photoresist/aluminum bilayer masking; Proc. SPIE 9365, Integrated Optics: Devices, Materials, and Technologies XIX, 93650Z (27 February 2015);*

[17] *Kelu Zheng et al; A Novel Wet Etching Process of Pb(Zr,Ti)O3 Thin Films for Applications in Microelectromechanical System; 2004 Jpn. J. Appl. Phys. 43 3934*

[18] *Dongqing Li; Encyclopedia of Microfluidics and Nanofluidics; Springer 2015*

[19] *A. Halbach, P. Gijsenbergh, Y. Jeong, M. Billen, C. Chare, H. Gao, G.B. Torri, D. Cheyns, X. Rottenberg, V. Rochus; Modelling of display-compatible piezoelectric micromachined ultrasonic transducers for haptic feedback; 2019 20th International Conference on Thermal, Mechanical*

and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)

[20] *Abdulrahman Alassi, Mohieddine Benammar and Dan Brett; Quartz Crystal Microbalance Electronic Interfacing Systems: A Review; Sensors 2017, 17, 2799*

[21] *https://beneq.com/en/thin-films/technology/atomic-layer-deposition*

[22] *Rongchun Zhou, Haixia Zhang, Yilong Hao and Yangyuan Wang; Simulation of the Bosch process with a string–cell hybrid method; J. Micromech. Microeng. 14 (2004) 851–858*

[23] *http://mx.nthu.edu.tw/ yucsu/4810/Lec04*

[24] *Sulochanadevi Baskaran; Structure and Regulation of Yeast Glycogen Synthase; University of California, Berkeley 2010*