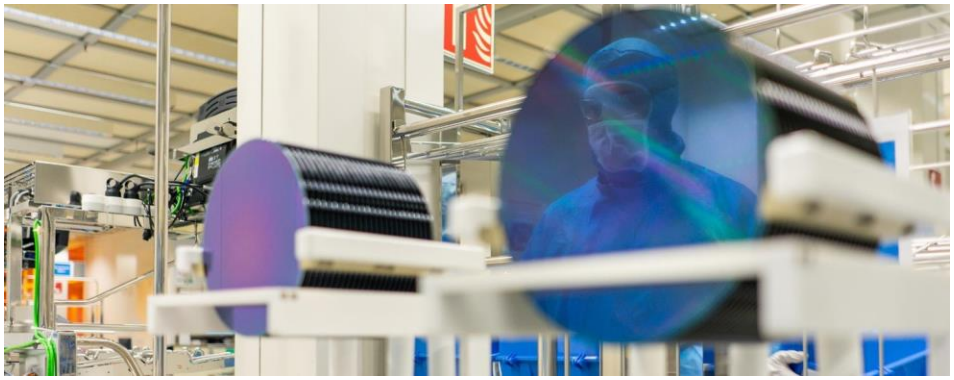

ROBUSTNESS TO SOFTWARE ERRORS IN A SYSTEM ON CHIP INTERCONNECT

STMICROELECTRONICS

Thomas MARTIN

I realized my 6 months internship at STMicroelectronics Grenoble in hardware digital design for a division which is in charge of designing ASICs for Aerospace, defense, microwave communication and mass market applications.

Details on the work carried out during the internship on the verso.

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GRENOBLE-INP PHELMA

NANOTECH

MASTER THESIS

DIGITAL ELECTRONICS

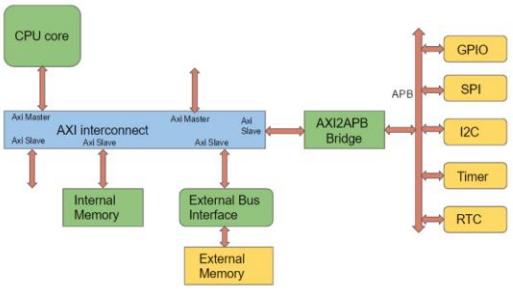
SUPERVISORS:
IGNAZIO URZI (COMPANY)
LORENA ANGHEL (SCHOOL)

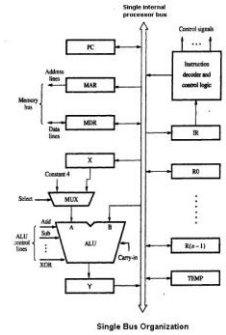
STMICROELECTRONICS

12 Rue Jules Horowitz, 38000 Grenoble

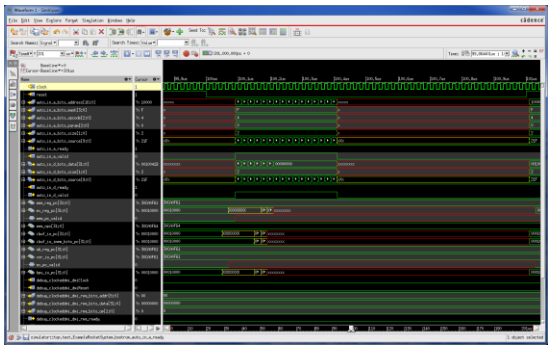
From 2/11/19 to 8/09/19

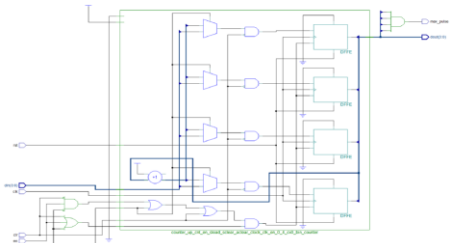
Microcontroller and IC digital group
Aerospace and Microwave Communication division






```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity signed_adder is
  port
  (
    aclr : in  std_logic;
    clk  : in  std_logic;
    a    : in  std_logic_vector;
    b    : in  std_logic_vector;
    q    : out std_logic_vector
  );
end signed_adder;

architecture signed_adder_arch of signed_adder is
  signal q_s : signed(a'high+1 downto 0); -- extra bit wide

begin -- architecture
  assert(a'length >= b'length)
    report "Port A must be the longer vector if different sizes!"
    severity FAILURE;
  q <= std_logic_vector(q_s);

  adding_proc:
  process (aclr, clk)
    begin
      if (aclr = '1') then
        q_s <= (others => '0');
      elsif rising_edge(clk) then
        q_s <= ('0'&signed(a)) + ('0'&signed(b));
      end if; -- clk'd
    end process;

end signed_adder_arch;
```





IPs microarchitecture, RTL design, UVM based standalone functional verification and synthesis have been carried out based on system specifications for enhancing the stability and security of the interconnect of new microprocessors. All the design is fully configurable to be easily integrated into other systems and synthesizable with the required timing constraints of the first targeted SoC.

MICRO-ARCHITECURE

RTL DESIGN

VERIFICATION

SYNTHESIS

LANGUAGES AND TOOLS:

VHDL, VERILOG, SYSTEMVERILOG, IP-XACT, CADENCE, SYNOPSYS, MAGILLEM

SOURCES

All the images used in the poster are non-contractually binding to the real performed activities.

- STMicroelectronics general presentation
- https://anysilicon.com/understanding-amba-bus-architechture-protocols/
- https://github.com/chipsalliance/rocket-chip/issues/1046
-https://vlsi.eelabs.technion.ac.il/experiments/editorial-experiment/

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