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**Consideration of switching process  
oscillation and current transients  
using data from frequency domain  
simulation**

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## Summary

This thesis aims to analyze the common mode currents of a three-phase inverter in the time domain with a low computational effort using data obtained for the frequency domain analysis.

Nowadays, the widespread use of power electronic circuits in many different applications has made relevant the analysis of the common mode currents which are the main responsible for conducted EMI [1]. Usually, the allowed electromagnetic interference is regulated by standard normative issued by international regulatory committees. This work is focused on the EMI in aerospace applications whose norm is defined by RTCA-DO-160 [2]. Filters designed to limit the emitted noise are required to ensure compliance with the reference standard [3]. The design of the filter is usually difficult since it requires detailed knowledge of the whole system. For this purpose, a model of the whole electronic system that can predict the amount of the induced EMI considering different operating conditions can be extremely helpful.

The analysis of the common mode currents described in this thesis has already been carried out in the frequency domain in [4], due to its low computational cost. The most comfortable description of the components to get an affordable analysis in the high-frequency domain is usually through scattering parameters (S-parameters) [5]. The present thesis takes advantage of the system previously described in [4] to obtain a time-domain analysis. In particular, a transmission function, which links the output voltage of the three-phase inverter with the common-mode current in the time-domain, is obtained. This analysis is necessary since the frequency parameters (S-parameters) are usually measured by a vector network analyzer (VNA) through sinusoidal waves at the input of the terminals [6]. This process can provide the S parameters for every component of the system, even though there are some limitations, that have to be taken into account; the input power of the sinusoidal wave is independent from the observation period of the VNA since its power is fixed; in fact the input wave spectrum consists of a single frequency. The real input of the converter system is instead a square wave, which generates EMI due to the fast variation of the voltage during the commutation. Therefore, the input power and the reflected power in a real case application are dependent on the observation period. In order to evaluate if this description through S parameters keeps its validity, an analysis in the time-domain is required. As explained previously, the obtained transmission function provides the behavior of the common-mode current in the time-domain during the switching transient of the inverter. The simulation of the common-mode current in the time domain requires the knowledge of the shape of the voltage on the three phases. Therefore, a double pulse test has been developed in order to evaluate the rise and the fall time of the AC voltages [7]. The measured rise and fall time have been employed to characterize the input voltage for the transmission function. Essentially, the input voltage for the transmission function is the common-mode voltage, which is simply a linear combination of the voltages on the three-phases. In addition, the results of the double pulse test performed on the system have made possible to evaluate the effect of the different switching state of the inverter on the common-mode current. Moreover, the relationship and the coupling between the differential mode and the common mode at the input and at the output of the inverter have been analyzed. In fact, it has been note in [8] that the parasitic capacitance in parallel to the power switches affects the frequency of oscillation of the DC link during the operations.

For this purpose, an analysis on the effect of the parasitic capacitance in parallel to the power transistors of the inverter has been performed as well.

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**Part I**

**Introduction**

# Chapter 1

## EMI in variable speed drive

The rise and the fall time of the power electronic devices are getting smaller and smaller and equally, the voltages which can be employed are getting higher [4]. This process is necessary to reduce the switching losses, which generate an increase in the efficiency of the switching converter. The current trend also increases the  $\frac{dV}{dt}$  [9], [10] during the switching process. According to [11] and [12], the faster change of the voltage during the switching process generates more relevant electromagnetic emission (EMI) . Therefore, the design of the filters to limit the EMI is getting important [13]. For this purpose, it is necessary to find models that allow predicting the behavior of the inverter related to electromagnetic emission. This analysis is usually done in the frequency domain [14], [15], [5] ; this work aims to get a simulation in the time domain. Some models have already been used to get the analysis in the time domain [16], [17] but in this work, the model with low computational effort in the time domain has been derived from models in the frequency domain which have been used in other analysis [4] . This model in the time domain has to deal also with the non-ideal switching characteristic of the switches [18]

The inverter generates an AC output from a DC input [19]. It is usually employed for different applications but one of the most common usages is the supply for adjustable speed drives, which can be driven through a sinusoidal AC output. It is possible to change the magnitude, the frequency and the phase of the aforementioned sinusoidal AC output, which is generated by power switches through a pulse width modulation (PWM). Hence, the AC output consists of discrete values and a filter is required to obtain a continuous function. The most common inverter is the voltage source inverter which can be modeled through a voltage source. In this case, the filtering function is made by an inductor, which serves as a low pass filter.

The basic inverter is the half-bridge or single-phase voltage inverter (see Figure 1.1)

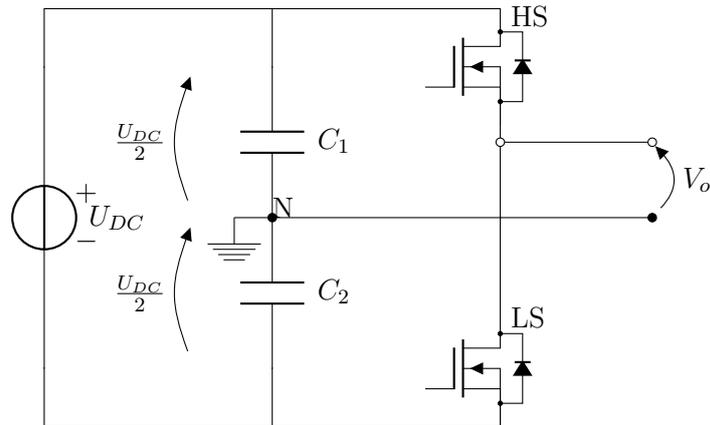


Figure 1.1: Half bridge

The previous system can be modeled through a simplified scheme (see Figure 1.2)

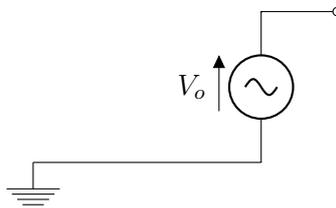


Figure 1.2: Half bridge model

The voltage  $V_o$  is ideally a sinusoidal waveform, but actually, its shape is similar to a square wave (see Figure 1.4). For every application of the converter, it is required that the voltage  $V_o$  follows a certain behavior. Different methods have been developed for this purpose. The most common is the so-called carrier-based PWM and it is based on the comparison between a modulating signal which is usually a triangular wave and the carrier which is usually the signal requested at the output. In many applications, the signal is a simple sinusoidal wave. The high side MOSFET (HS in Figure 1.2) is on when the carrier is larger than the modulating signal and it's off in the other case. The low side MOSFET (LS in Figure 1.2) is instead turned on when the carrier is lower than the modulating signal and off in the other case.

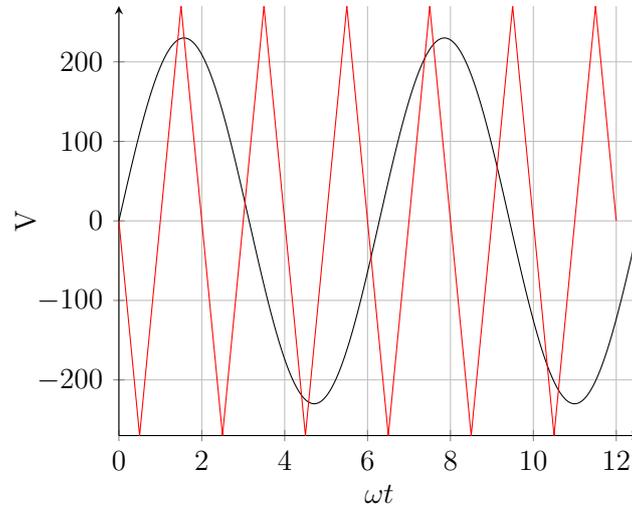


Figure 1.3: Carrier based PWM

The output  $V_o$  by using this modulation is instead depicted in the following Figure 1.4

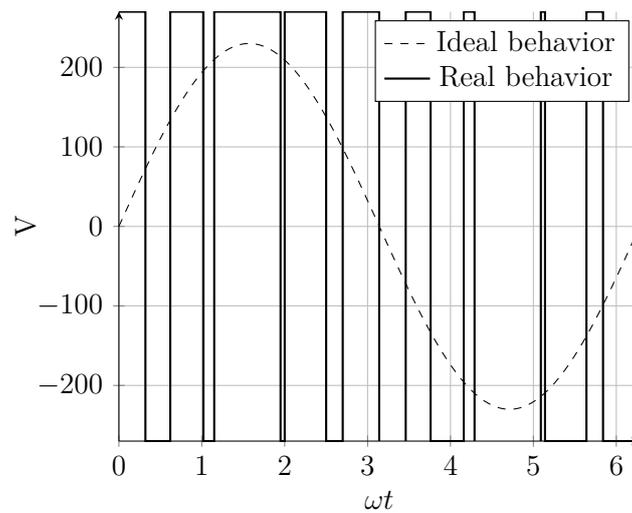


Figure 1.4: Output voltage of the half bridge

The continuous line represents the actual output and the dashed line represents its fundamental component, which is just a sinusoidal wave and which is the only one which remains after the filtering process.

The single phase voltage source is employed mostly for low power application. Medium and high power application are covered instead by the three phase inverter [19].

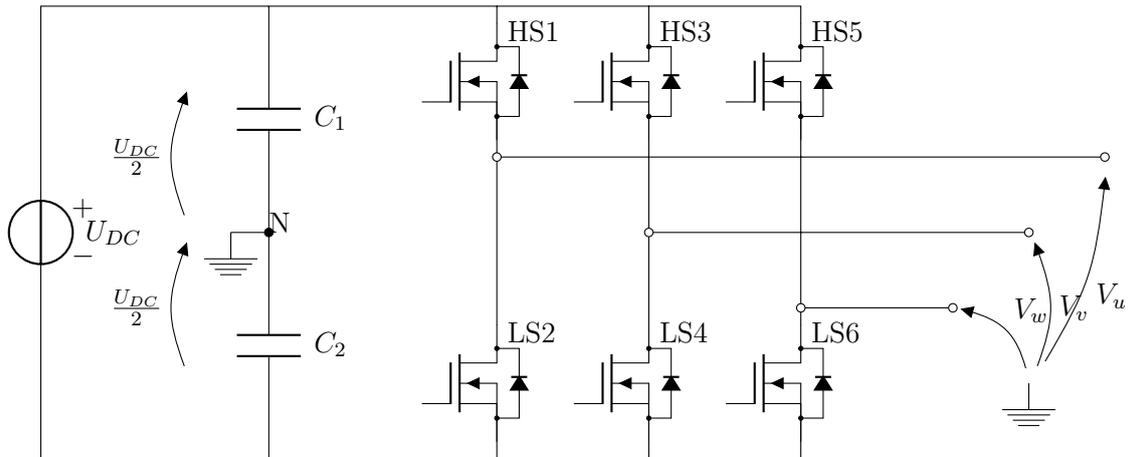


Figure 1.5: Three phase inverter

The three-phase inverter consists simply of three half-bridges which from now on are called legs and which are linked to the same DC voltage. Each of them drives a different output. The model of the three-phase inverter can be represented through three different and independent voltage sources (see Figure 1.6).

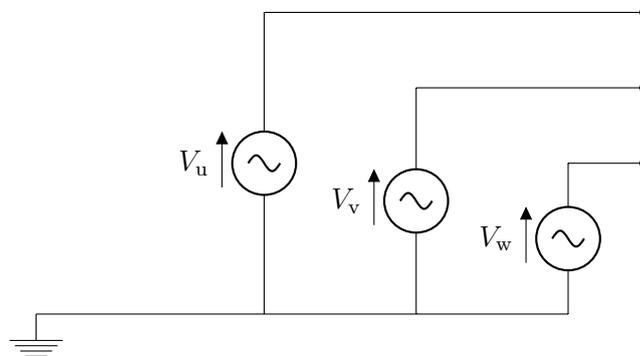


Figure 1.6: Inverter model

Different techniques allow obtaining the voltages which are required on every line. The most simple one is the carrier-based PWM which is just the extension of the method applied for the half-bridge. The only difference is that there are a single modulating signal and three different carriers. Every carrier is associated with a different leg. The vast majority of applications, such as such as electrical drives, requires the three voltages at the output to be equal in magnitude and frequency and a phase difference of  $120^\circ$ . This kind of result is obtained by applying the same delay to the three different carriers (see Figure 1.7)

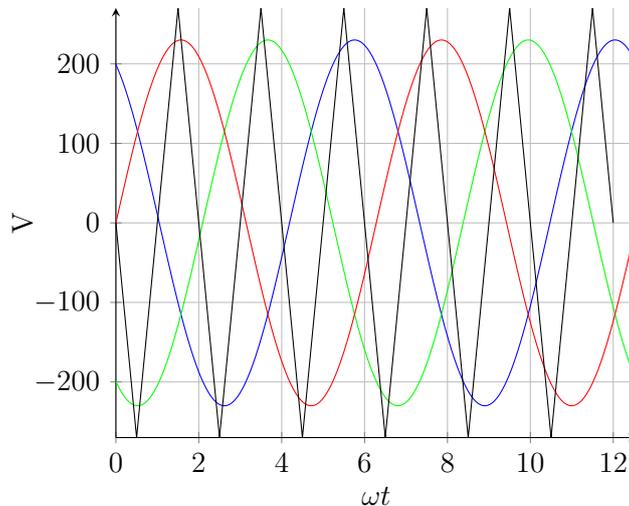


Figure 1.7: Carrier based PWM for the three-phase inverter

The efficiency of the converter depends also on the switching characteristic [11]. SiC switches allow faster voltages' and currents' changes which are interpreted as sources of electromagnetic emission. The electromagnetic emission, when harmful to the equipment, is called electromagnetic interference (EMI) and it is described according to [11] as “*any electromagnetic disturbance that interrupts, obstructs or otherwise degrades or limit the effective performance of electronics/electrical equipment*”. With a higher switching frequency, these disturbances propagates in the system through the parasitic capacitances of the system. Different techniques are used to limit those disturbances such as wideband passive filters but the design of those filters is not easy in high frequency since high-frequency behavior is difficult to predict during the design of the system [20]. The most relevant problem in the case of a power converter, when it is used to drive an adjustable speed drive, is usually associated with a common mode current with high-frequency components that can propagate in the system through the parasitic capacitances between the connection cable and the ground [19]. The definition of the common mode and the differential mode is given in [21] for the three-phase system. Each phase is associated with a different leg of the inverter which is connected through a cable to the asynchronous motor. By a circuital point of view, the common-mode current is defined as the current which flows equally for all the phases and the common-mode voltage is the voltage which is equal for all the lines. The differential mode is instead defined through the components which are different between the lines. Hence, the differential mode voltage is defined as the voltage difference between the 2 phases. The differential mode current is defined as the current which flows among the lines. Therefore, the three-phase system can be defined by a common mode which is equal for all the phases and two differential mode which defines the difference between the lines. The whole system is defined by the common-mode and by two differential mode as depicted in Figure 1.8.

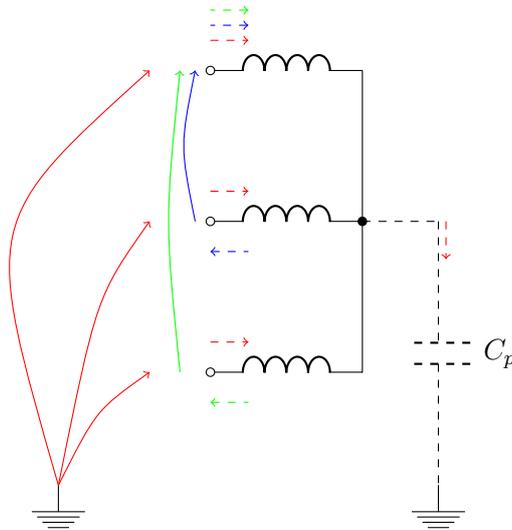


Figure 1.8: Common mode and differential mode of the motor in a three phase system

It is possible to define as well differential-mode impedances and common-mode impedances. The differential mode impedance is considered the impedance between two lines, while the common-mode impedance is defined as the impedance between the lines and the ground. In particular, the parasitic capacitances between the lines are taken into account for the differential mode impedances. For the common-mode impedances, the parasitic capacitances between the lines and the ground have a relevant influence [11]. The output signal on each line is instead described because the common-mode voltage is a combination of the signal on the three lines.

The output of the inverter is a sinusoidal wave with the same behavior of the carrier and with a delay due to the conversion. The real output is a square wave, therefore the first analysis is done with the following signal (see Figure 1.9)

In a first analysis, instead of the real signal, the simple square wave impulse, which is depicted in the following Figure 1.9, is analyzed .

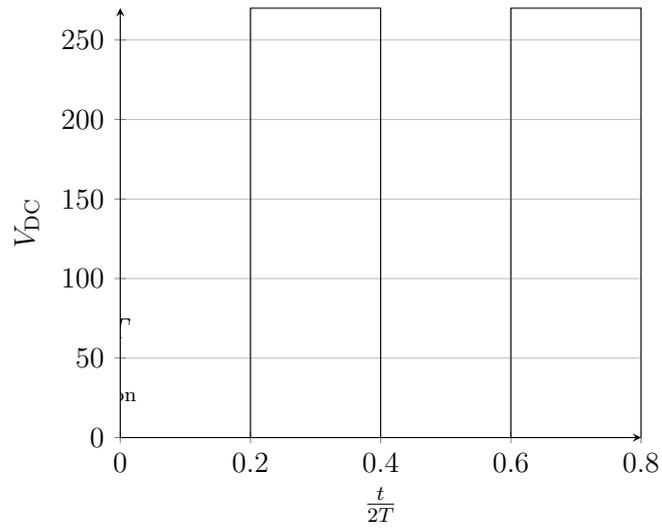


Figure 1.9: Single pulse

The real signal is instead a trapezoidal wave since the fall and the rise time are not equal to 0, as it can be seen from the following Figure 1.10

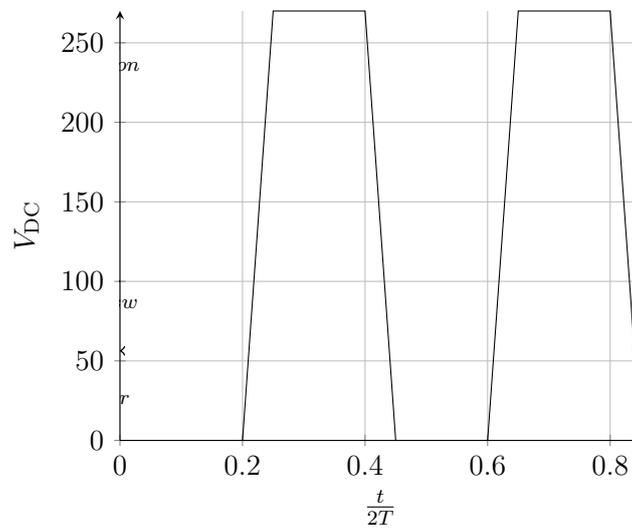


Figure 1.10: Single pulse trapezoidal waveform

That is relevant for the computation of the EMI instead of the actual Fourier analysis of the signal is the so-called envelope, which is just the connection of every relative maximum of the Fourier transform.

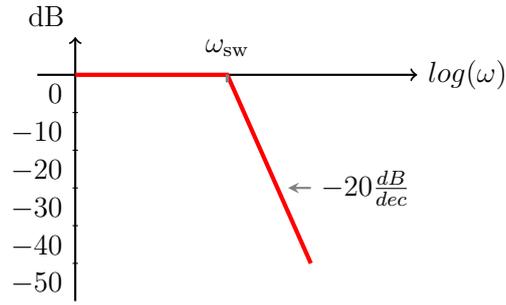


Figure 1.11: Envelope of a square wave

The envelope as explained previously is simply the envelope of the sinc function. From Figure 1.11 it can be noticed that the Fourier transform remains constant until a pole at the switching frequency  $\frac{1}{t_{sw}}$  starts reducing the magnitude with a slope of  $-20 \frac{dB}{dec}$ .

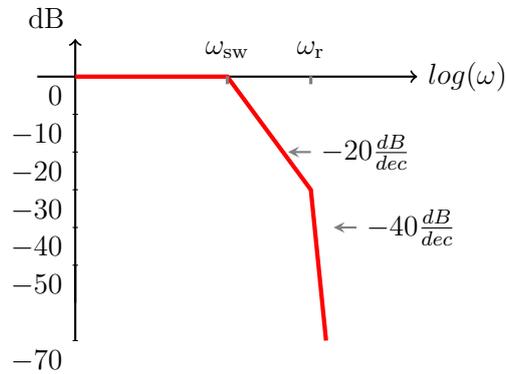


Figure 1.12: Envelope of the trapezoidal waveform

The envelope of the double sinc represents the behavior of the Fourier transform of the trapezoidal wave as it can be seen in Figure 1.12. An extra pole due to the rise and fall time  $t_r$  is added. This added pole lets the envelope decrease of  $40 \frac{dB}{dec}$  from the frequency proportional to  $\frac{1}{t_r}$ . The frequency components of the common-mode current, which as explained previously are related to the EMI, can be estimated with an evaluation of the envelope depicted in Figure 1.12 [19].

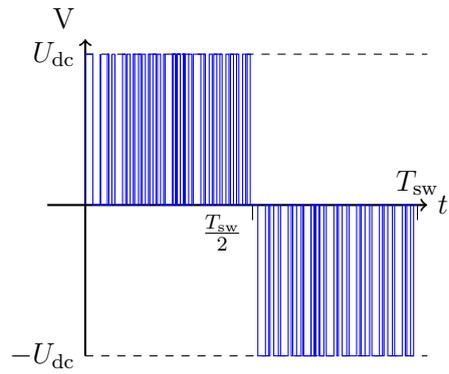


Figure 1.13: Differential mode

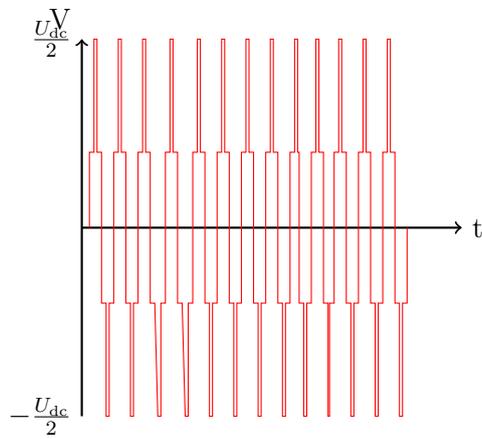


Figure 1.14: Common mode

The behavior of the common and of differential mode, which are already described in [4] in the case of a typical PWM is actually more complicated than the simple square wave. In fact, both the common and differential mode are a combination of the square wave on the three lines and since rise/fall time and duty cycle are variable. Moreover, the rise and fall time are usually different (see Figure 1.14 and Figure 1.13 ).

## Chapter 2

# Frequency domain simulation

Many different models have been developed to describe the components of the power system such as cables [22], [23], EMI filters [20], [3] and motor [24]. These descriptions have provided good simulation results in the frequency domain [15], [25] and in the time domain [17]. Nevertheless, the simulations are mostly done in the frequency domain since the limitations associated with the EMI are usually defined in this domain. Moreover, the frequency analysis allows reaching a high precision with a lower computational cost. At the same time, it has been noticed that there is a coupling between the differential and the common-mode due to the system unbalance [26], [27].

In order to obtain a good analysis of these phenomena, a different method, which can predict the EMI generated by the common mode [28] and the differential mode [29], has been developed. One standard method is based on the description of each component as an n-port network of S parameters. This solution allows taking into account also the coupling between the common mode and the differential mode [30].

As stated in the previous paragraph, the analysis concerning the electromagnetic noise is linked with the common and differential mode of the system (Chapter 1). [4] proposes two different models to simulate the common-mode and differential-mode effects. From those models, a transmission function which can simulate the response in the time domain for the common-mode system has been then developed. This transmission function evaluates the common-mode current for a given common-mode voltage. The description of the process to get the transmission function is depicted in Chapter 10.

The first model proposed in [4] permits to model the system of Chapter 4 in one common-mode circuit (see Figure 2.1) and one differential-mode circuit (see Figure 2.2)

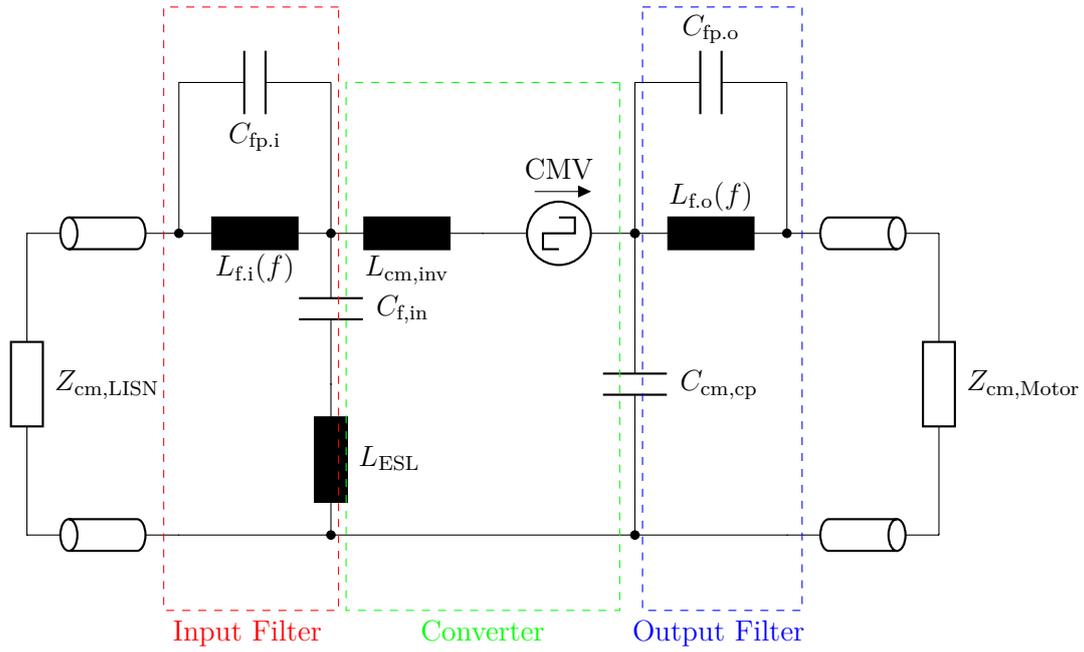


Figure 2.1: Common mode circuit

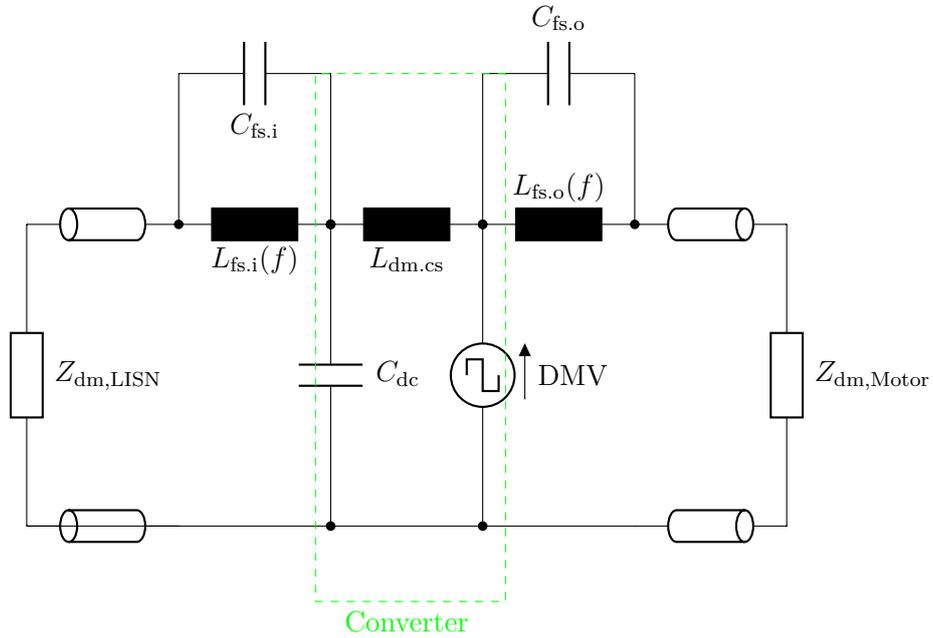


Figure 2.2: Differential mode circuit

These two models allow evaluating the common and the differential mode in every point of the circuit. The measurements of the impedances for both models are made through

a spectrum analyzer in a domain from 1kHz to 30 MHz, the way the measurements are taken, is instead deeply different. The common-mode impedances are taken by linking all the ends of the different lines together and measuring the impedances through these new common terminals. The differential mode is measured by using the network analyzer across different lines. This work is more focused on Figure 2.1, since the analysis is concentrated on the common-mode current. Each component of the previous model (see Figure 2.1) has been modeled through a 2-Port representation such as Z Matrix, Y Matrix or ABCD Matrix [31]. The LISN in the common-mode model is well known and in this case, is defined by the following Figure 2.3 from which it is possible to evaluate the  $Z_{cm,LISN}$ . The LISN is described analytically since it is a well-known circuit. Ideally, it could also be used to get values at frequencies below 1kHz which is the limit of the network analyzer.

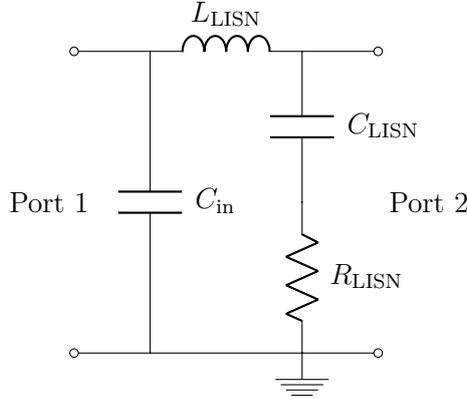


Figure 2.3: LISN

From the circuit in Figure 2.3 it is possible to obtain a 2X2 Z matrix where each component of the matrix consists of a vector of values.

The input transmission cable is defined through (4.1) and (4.2) but the cables are considered lossless therefore  $R=0$  and  $G=0$ . The equation is then  $Z_0 = \sqrt{\frac{L_{cable}}{C_{cable}}}$  and  $\gamma = j\omega\sqrt{L_{cable}C_{cable}}$ .  $L_{cable}$  and  $C_{cable}$  are by definition  $\frac{H}{m}$  and  $\frac{F}{m}$ . Once the parameters of the cable are obtained, it is trivial to write them in the ABCD-matrix called also transmission matrix. The same process has been carried out with the output cable but the characteristic capacitances and impedances are different since the length is 1 meter instead of the 5 meters of the input cable. Moreover, the output cable is a three-phase cable which is characterized by its specific common-mode characteristic.

The input filter is defined by the following Figure 2.4

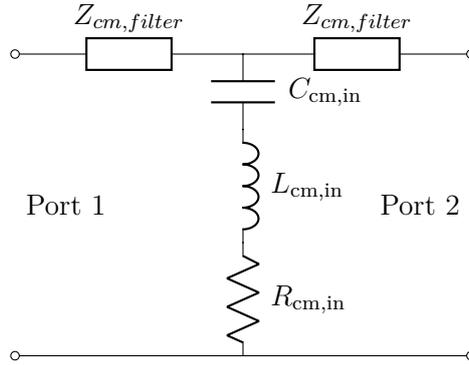


Figure 2.4: Input EMI filter

In this case, the choke is measured with the network analyzer since the development of its model requires a high computational effort [32]. It is possible to obtain the Z matrix from the description in Figure 2.4. The output choke is instead different since it consists only in one choke with no extra component. For the previous reason, it is only measured through the network analyzer.

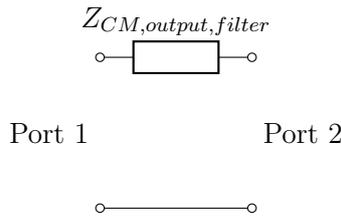


Figure 2.5: Output EMI filter

As it can be seen from Figure 2.5, it isn't possible to describe the previous 2-port network with a Z matrix, therefore, a representation through the Y matrix is employed. The motor is represented with the following Figure 2.6. The 2-port network can be represented only by a Z matrix.

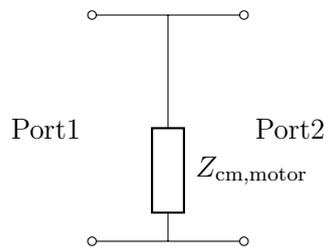


Figure 2.6: Motor

For the analysis, the system in Figure 2.1 is therefore translated into a cascade of different 2-ports defined in frequency domain.

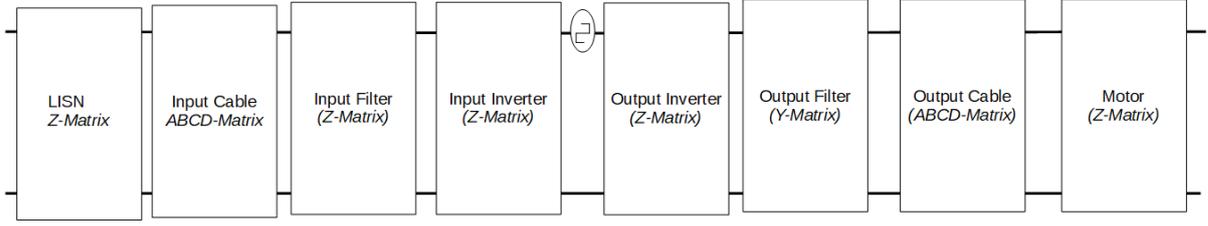


Figure 2.7: System model with matrices

Therefore, the system can finally be represented by a simple cascade of 2-ports with a square wave generator in between as it can be seen from Figure 2.7. From this model some good results are already obtained as explained in Chapter 10, but the main problem is that the upper limit of 30 MHz for the measurements is not enough to get the high-frequencies oscillations which are typical of the common-mode current as explained in Chapter 6. One further limitation is the lack of the coupling between the common mode and the differential mode, which can't be analyzed through this model [33]. The components are described through 6-port networks to overcome this problem. This model is based on the analysis of the whole system. Hence, there is just one model which takes into account both the common-mode and the differential mode. 2 ports are associated with the common mode and the other 4 are associated with the differential mode. In this case, the scattering parameters are measured for each component through a vector analyzer. Each component between the inverter and the motor is a 3-phase component that is defined by 3 port in input and 3 port in output. The scattering matrix (S matrix) is, therefore, a 6X6 matrix. This description is valid for every component which links the motor and the inverter (Motor, Output Filter, Output Cable). The DC side of the system (from the LISN to the inverter) is defined similarly but the resulting S matrix is just a 4X4 matrix since the system in this part is just 2-phase. The inverter has instead a different representation. It is defined by a 4X4 matrix for its input part and by a 6X6 matrix for its output part. These matrices can't be measured directly but they are instead simulated through a high-frequency model which is going to be helpful also for the analysis of Chapter 11. In this way, it is possible to describe the inverter through two different kinds of matrices. It is possible to obtain from every S matrix the associated Z matrix which is in the following form for every 3-phase component (2.1)

$$\begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} & \dots & Z_{16} \\ Z_{21} & Z_{22} & \dots & Z_{26} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{61} & Z_{62} & \dots & Z_{66} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{pmatrix} \quad (2.1)$$

The same result is available for every 2-phase component with the only difference that it is

a 4X4 matrix (2.2)

$$\begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} & \dots & Z_{14} \\ Z_{21} & Z_{22} & \dots & Z_{24} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{41} & Z_{42} & \dots & Z_{44} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{pmatrix} \quad (2.2)$$

The names of the psorts of the matix are depicted in the following Figure 2.8

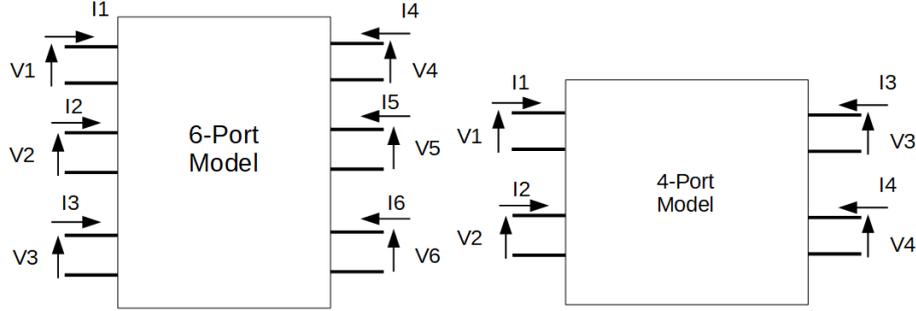


Figure 2.8: Basic blocks

As it can be seen in the previous Figure 2.8, the first three ports (Port 1, Port 2, Port3) represent the input of every 3-phase component and the other three ports (Port 4, Port 5, Port 6) represent the output of every component. The same is valid in the case of the 4 Port with the first 2 port (Port 1, Port 2) which are the input ports and the Port 3 and 4 which represent the output of the 4-port. Therefore, every component can be described by a 6-port block or by a 4-port block. The description of the system in this way, nevertheless, doesn't permit us to obtain direct information on the common and differential mode. It is necessary to manipulate those matrices in order to find a matrix that links the common and differential mode currents with the common-mode voltage and differential-mode voltage. The relation between common-mode voltage and the voltage of the phases is defined as follows and as they are cited in [4].

$$V_{\text{cm,in}} = \frac{V_1 + V_2 + V_3}{3} \quad (2.3)$$

and equally

$$I_{\text{cm,in}} = I_1 + I_2 + I_3 \quad (2.4)$$

while the differential mode is defined through

$$V_{\text{dm1,in}} = V_1 - V_2 \quad (2.5)$$

and

$$V_{\text{dm2,in}} = V_2 - V_3 \quad (2.6)$$

. For the differential currents the following equations are valid

$$I_{\text{dm1,in}} = \frac{2I_1 - I_2 - I_3}{3} \quad (2.7)$$

and

$$I_{dm2,in} = \frac{I_1 + I_2 - 2I_3}{3} \quad (2.8)$$

The same equation can be used to obtain  $I_{cm,out}$ ,  $V_{cm,out}$  and  $V_{dm1,out}$ ,  $I_{dm1,out}$ ,  $V_{dm2,out}$ ,  $I_{dm2,out}$ . It is therefore possible to find a set of coefficients that link the currents and voltages of the 6 ports with the common and differential mode. This set of coefficients defines two different transformation matrices which translate currents and voltages of the standard Z matrix in the required common and differential mode. The transformation matrix for the voltage is defined in (10.12)

$$A = \begin{pmatrix} \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \end{pmatrix} \quad (2.9)$$

The first row gets the input common-mode voltage, the second row the input differential-mode 1 and the third the input differential mode 2. The output is defined equally by the other three rows. A similar matrix is used to obtain the currents (10.13)

$$B = \begin{pmatrix} 1 & 1 & 1 & 0 & 0 & 0 \\ \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} & 0 & 0 & 0 \\ \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & 0 & 0 & \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} \end{pmatrix} \quad (2.10)$$

The 6-port network is defined by (2.1). It is possible to obtain the system previously described with the following transformation

$$AV = AZB^{-1}BI \quad (2.11)$$

The equation provides the new vectors and matrices which are more useful for our analysis. The new definition are explained with (2.12) and (2.13)

$$AV = \begin{pmatrix} V_{cm,in} \\ V_{dm1,in} \\ V_{dm2,in} \\ V_{cm,out} \\ V_{dm1,out} \\ V_{dm2,out} \end{pmatrix} = V_{cm,dm} \quad (2.12)$$

$$BI = \begin{pmatrix} I_{cm,in} \\ I_{dm1,in} \\ I_{dm2,in} \\ I_{cm,out} \\ I_{dm1,out} \\ I_{dm2,out} \end{pmatrix} = I_{cm,dm} \quad (2.13)$$

The new matrix impedance is instead  $AZB^{-1}$ . Therefore the system described in Figure 2.8 changes as shown in Figure 2.9

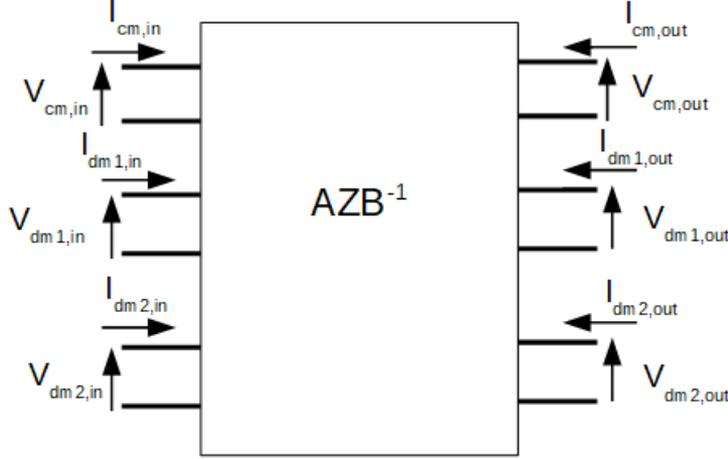


Figure 2.9: 6 Port model with common and differential mode

The same process can be applied to the 4-port. The only difference is that the transformation matrices is just a 4-pole component and there are only two lines (2.14) and (2.15).

$$A_4 = \begin{pmatrix} \frac{1}{2} & \frac{1}{2} & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & \frac{1}{2} & \frac{1}{2} \\ 0 & 0 & 1 & -1 \end{pmatrix} \quad (2.14)$$

$$B_4 = \begin{pmatrix} 1 & 1 & 0 & 0 \\ \frac{1}{2} & -\frac{1}{2} & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & \frac{1}{2} & -\frac{1}{2} \end{pmatrix} \quad (2.15)$$

Therefore the system in the Figure 4.1 is translated into the following Figure 2.10

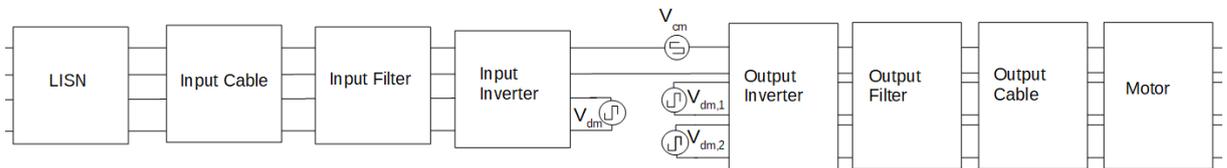


Figure 2.10: 6 Port model

This model has the huge advantage to take into account the coupling between the common mode and differential mode which was observed in the system at 1.8 MHz [4].

This interval provides a very good description in high frequency but the low-frequency boundaries affect the results of the performed simulation of the step response as it is explained in Chapter 10.

These models allow obtaining a good analysis also at the high frequency where the coupling between the differential-mode and the common-mode is particularly relevant because the vector network analyzer can measure the S parameters in an interval between 100kHz and 180 MHz. The aforementioned description is obtained through S parameters which are usually measured through a vector network analyzer (VNA) [6], which can measure the S parameters associated with each terminal of the component. These measurements are obtained through a sinusoidal waveform applied to the terminal which has to be measured. As it was explained in Chapter 1 the real output of the inverter is not a sinusoidal wave but instead a square wave whose Fourier transform is completely different from the Fourier transform of the sinusoidal waveform. Therefore, an analysis has been carried out, in order to prove if this description through the n-port network can provide also a good approximation in the time-domain. This analysis requires the evaluation of the behavior of the inverter during the transient of its switches, which is measured through the double pulse test [34], [18]. The double pulse test (DPT) is described in Chapter 3

## Chapter 3

# Double pulse test and switching behaviour

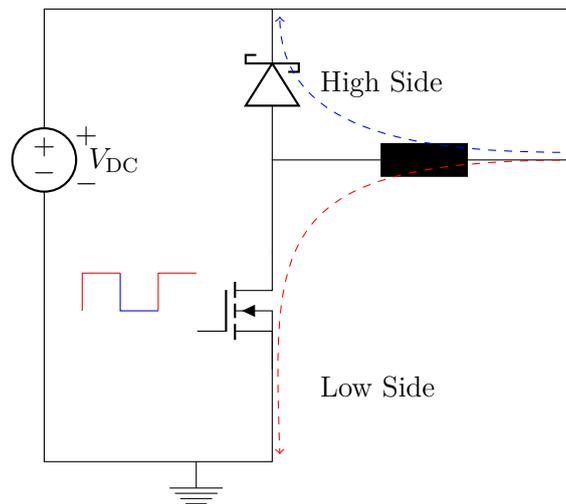


Figure 3.1: Double pulse test

The double pulse test is a process that is used to evaluate switching characteristics such rise and fall time and losses [35]; it is carried out by turning on the transistor under test with a positive pulse applied on the gate. The MOSFET is linked to a freewheeling diode and with a high inductive load (Figure 3.1) to consider the current constant for a given amount of time  $T_1$  (Figure 3.3). During this first period, the current starts increasing and it flows as depicted by the red line in Figure 3.1 [18]. At this point, the MOSFET is turned off for a time  $T_2$  and the current commutates to the freewheeling diode. The diode has to be turned on with a positive voltage between the anode and the cathode. In this phase, the current which is supposed constant at a given value  $I_0$  charges the capacitance  $C_{ds}$  of the MOSFET (left circuit of the Figure 3.4). An overshoot of the voltage takes place and it turns on the diode (right circuit of the Figure 3.4). This first commutation defines the rise

time. After the switching process is finished, the DUT is turned on again with a second pulse on the gate and the current commutates from the diode to the MOSFET (Figure 3.5), but the diode has to be turned off and this time is usually defined as reverse recovery time and it is constant (Figure 3.5) since the MOSFET is already on. This second pulse allows evaluating the fall time. It is easy to realize that the rise time is dependent on the parasitic capacitance and the current, while the fall time is dependent just by the parameters of the body diode or of the diode in parallel to the low-side MOSFET. The commutation of the current during the different pulses is depicted in Figure 3.1. The switching frequency and the rise and fall time of a device are fundamental to define the frequency behavior of the system and, in particular of the switching components such as inverters [10].

The rise time is defined as the time required to the  $V_{ds}$  of the component to go from the 10% of the supply voltage to the 90% the fall time is instead the time required for the voltage to in the reversed direction.

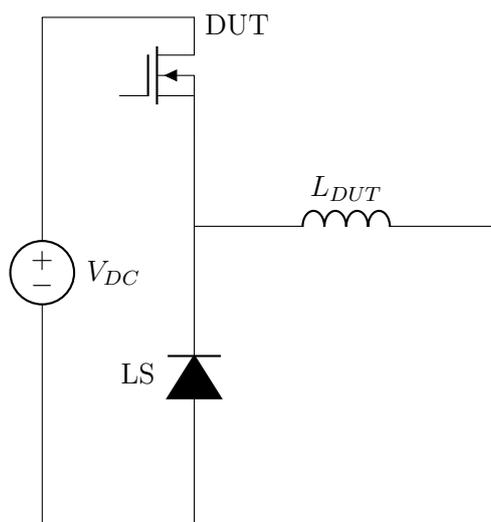


Figure 3.2: Double pulse test circuit

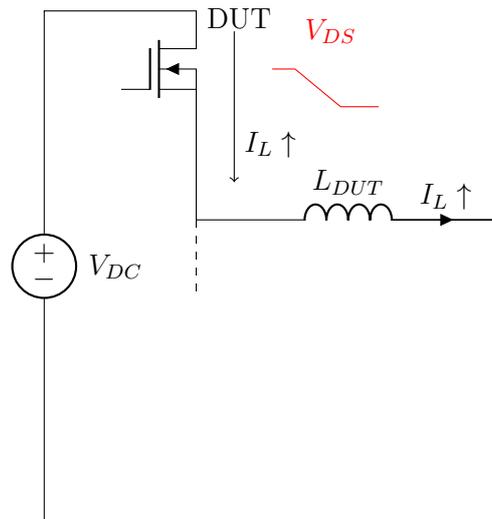


Figure 3.3: Double pulse test circuit during the first pulse

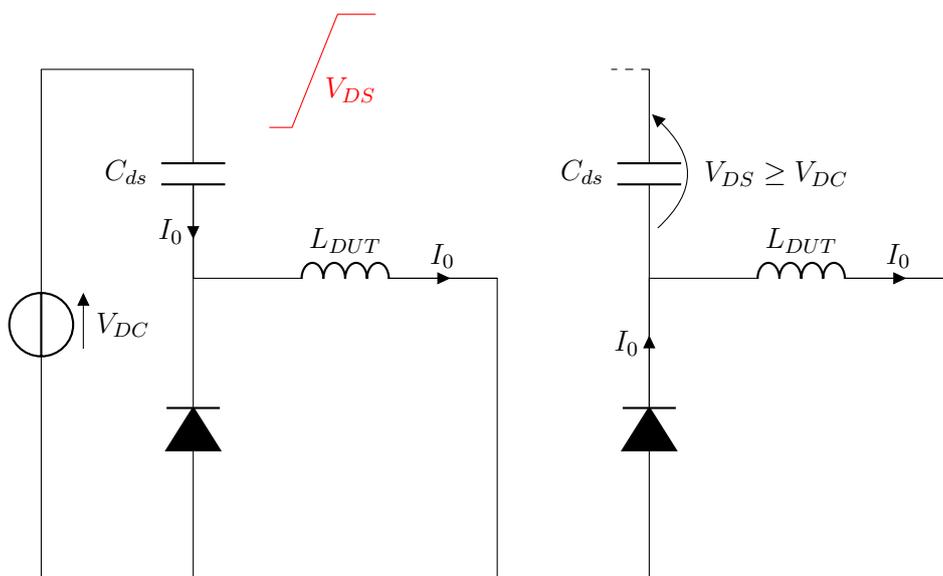


Figure 3.4: Double pulse test circuit during the off time

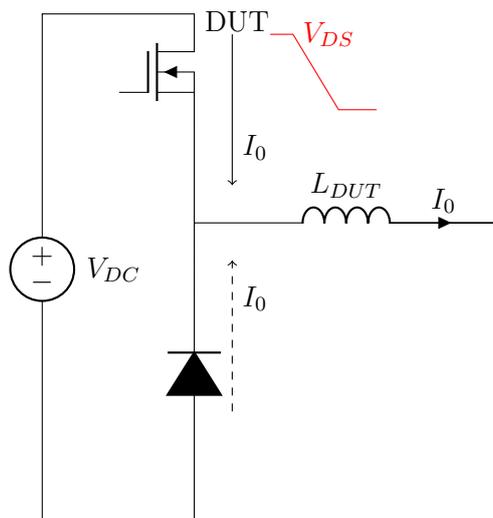


Figure 3.5: Double pulse test circuit during the second pulse

The behavior of the  $V_{ds}$  during the double pulse test is depicted below in Figure 3.6

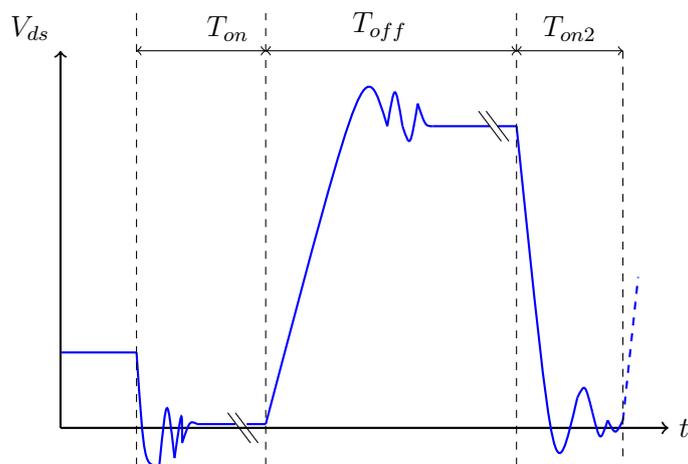


Figure 3.6:  $V_{ds}$  behavior during the double pulse test

The second pulse is not required to be as long as the first one since it is employed to measure the fall time. The first  $T_{on}$  is instead necessary to charge the inductor and the  $T_{off}$  allows to measure the rise time. The  $V_{ds}$  behaves in the way depicted in Figure 3.6. The behavior of the  $V_{gs}$  and of the  $V_{ds}$  are depicted in the following Figure 3.7 for the turn-on and in Figure 3.8 for the turn-off

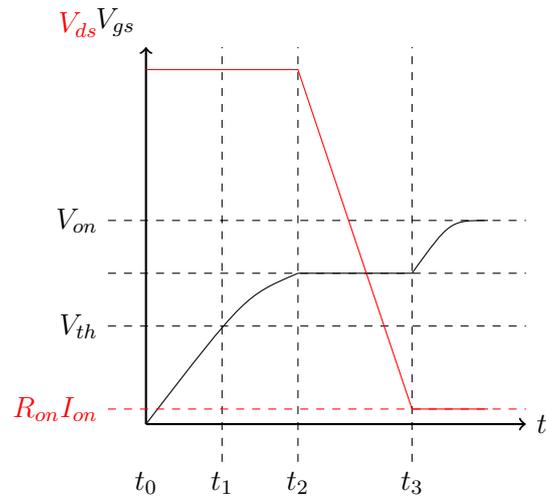


Figure 3.7:  $V_{gs}$  and  $V_{ds}$  behavior during the turn on

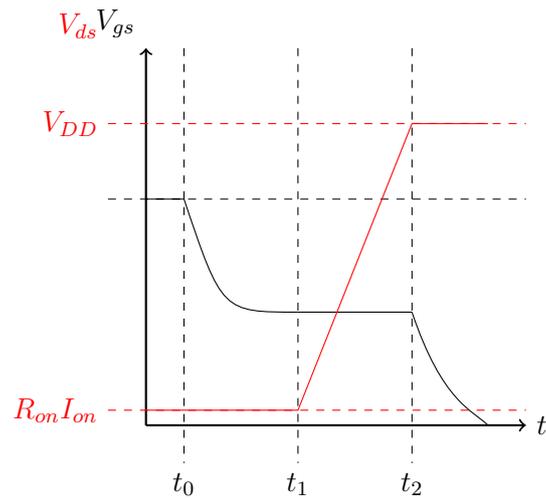


Figure 3.8:  $V_{gs}$  and  $V_{ds}$  behavior during the turn off

As it was explained in the Chapter 1 this time  $t_2 - t_1$  in Figure 3.7 is called also rise time defines also the output in the frequency domain and how the square wave at the output behaves at high frequencies. The fall time is instead the time  $t_3 - t_2$  in Figure 3.8

**Part II**

**System Description**

## Chapter 4

# Hardware Description

The system used in this work is the typical setup system to measure the conducted noise according to RTCA DO-160 which defines noise limits in a range from 115 kHz up to 30 MHz.

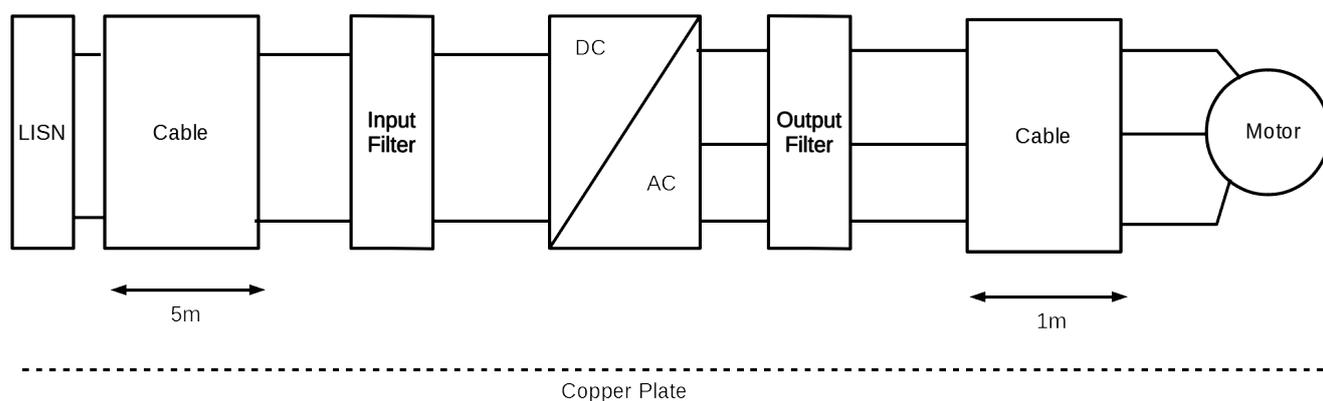


Figure 4.1: Model of the system used for the measurements

The previous Figure 4.1, which is the same system described in [4], consists of the line impedance stabilization network (LISN) at the side of the DC voltage. The connection from the LISN to the input of the inverter is made according to the standard RTCA DO-160 with a cable of 5 meters. Filters are placed at the input and the output of the inverter to reduce the electromagnetic emission and to make it compliant to the standard RTCA DO-160. The inverter drives the motor through a 1-meter long cable. The whole system is placed on a copper plate. The measurement of the common-mode current is made through a large bandwidth current probe around the cable which links the motor and the inverter. In this way, only the common-mode current is measured. In particular, the RTCA DO-160 norm requires to measure the common-mode current as near as possible to the inverter, therefore it is measured just after the output filter. The current probe is depicted in the following Figure 4.2.



Figure 4.2: Current probe

The motor is a asynchronous motor with 2 poles and defined by 400V of voltage supply 50 Hz and 11 kW The motor is instead type ACM160MA -2HE of 116.6 Kg with the characteristics described in the following table 4.1:

Table 4.1: Motor characteristic

Motor characteristic						
V	Hz	kW	$Co s\lambda$	rpm	A	$\eta\%$
$\Delta 400Y690V$	50	11	0.89	2940	2011.6	89.4%
$\Delta 460Y795V$	60	13.2	0.89	3525	20.812.1	89.4%

The inverter is made with six SiC Mosfet ROHM SCT2080KE and 6 diodes ROHM SCS220KG with the relevant information depicted in the table 4.2 below:

Table 4.2: Electrical characteristic

SCT2080KE	
$V_{ds}$	1200V
continous $I_{ds}$	40A
$V_{gs}$	-6 to +22V
SCS220KG	
Reverse Voltage	1200V
continous $I_{ak}$	20A
Forward Voltage	1.4V

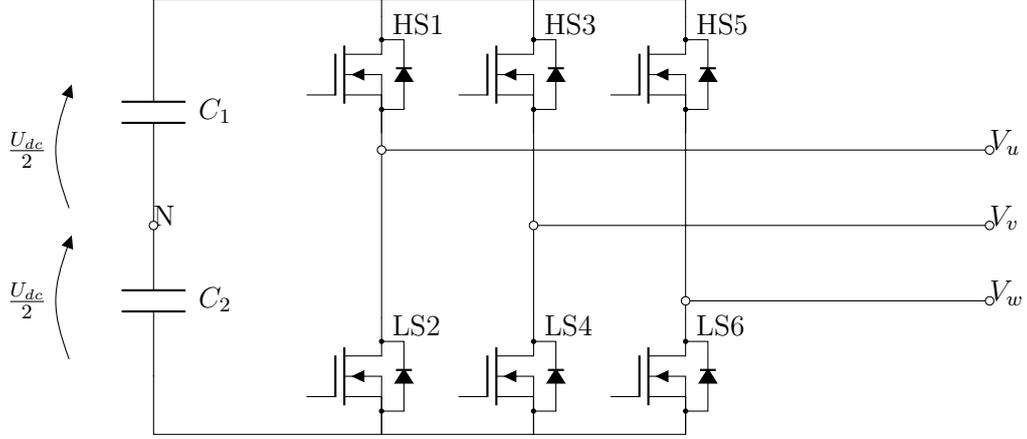


Figure 4.3: Three phase inverter

The scheme of the inverter is depicted in Figure 4.3. Each MOSFET is of the type SCH2080KE and every diode is of the type SCS220KG. The classical inverter has 2-phase in input where the DC voltage is applied and 3-phase in output. The supply voltage is 540 V. The DC voltage is split between two capacitances in series. The output voltage can be either 270V or -270V. Each output line can be considered independent with respect to the other two. The description of the inverter is described more in detail in Chapter 1. The cables which link the system are different not only in the length. The input cable is a 2-phase unshielded cable, while the output cable is a 3-phase shielded cable. The cables are both modeled as transmission lines [2] and they are defined by the characteristic impedance in (4.1) and by the propagation constant in (4.2).

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (4.1)$$

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (4.2)$$

The filters depicted in Figure 4.1 are EMI filters, which have the aim to reduce the emissions of the system in the high frequency during the typical operation of the inverter. The core block of every EMI filter is usually the common mode choke which usually consists of a ferromagnetic material or a nanocrystalline [20]. The common-mode choke is usually just a ferromagnetic material with a specific coil for every phase which is used. The output filter has, therefore, three different coils and the input filter has two coils. The used common mode choke for this experiment is made of nanocrystalline VITROPERM, which is an alloy based on iron with silicon and boron with an addition of niobium and copper. The behavior of this material in the frequency domain is not linear [36].

This is the system (see Figure 4.1) on which the double pulse test (DPT) has been performed (Chapter 3). During the double pulse test, the following electrical quantities depicted in Figure 4.4 are measured.

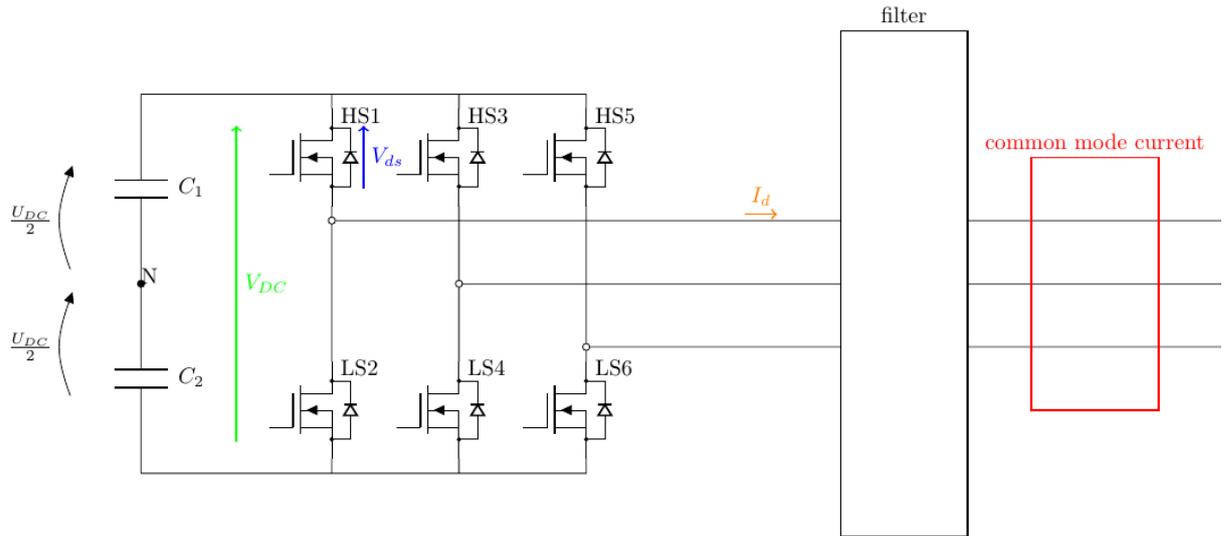


Figure 4.4: Measured voltages and currents

It is measured the voltage at the input of the inverter called DC link, which is relevant since it is mostly affected by the differential mode. The measurement of this voltage allows evaluating if there is any effect of the common-mode on the input of the converter. The drain current of the MOSFET in which the gate signal of the double pulse test is applied has been also measured. The drain current which is assumed constant during all the switching process is relevant for the rise and fall time evaluation as explained in Chapter 3. Moreover, a large bandwidth current probe has been used to measure the common-mode current. According to the standard DO-160, the common-mode current has to be measured at the output of the filter. The current probe is around the 3-phase cable. In this way, the differential-mode currents aren't taken into account since they flow between the cables in opposite directions and only the common-mode remains (Chapter 1). The description of the digital system and the description in detail of the double pulse system employed is explained in Chapter 5 and the results are depicted in Chapter 6. The double pulse test can be slightly changed to evaluate the effect of the common-mode on the DC link. Usually, the differential mode is the only one that affects the DC link. In order to prove this effect, the double pulse test applies a signal which is equivalent to a differential mode equal to 0 (all the HS of the legs turned on and off simultaneously as shown in Chapter 5) to evaluate the effect of the common-mode on the DC link.

## Chapter 5

# Three phase Double Pulse Test

The usual switching characteristic of the device during the DPT is different from the characteristic during normal usage. This difference is due to the impedance which isn't optimized for the switching operation. Secondly, in a normal application parasitic capacitances and inductors are usually added [37]. The switching characteristic of the MOSFET in the real application is evaluated by applying a specific double pulse test on the inverter in a typical layout. Through this test, it is possible to evaluate the effect that the other legs of the three-phase inverter have in the switching characteristic. The effects of the power cables and the motor are also taken into account through this specific DPT. The switching process of the double pulse test is performed on the first leg only. The other two legs are kept fixed. The DPT is designed to evaluate all the possible switching cases which are usually used in a simple SVPWM. SVPWM is a digital modulation method which generates voltages on every line which are equal on average for each sampling period to the reference one [19].

The SVPWM represents each set of possible voltages at the output of each leg in a complex plane through the following transformations ( 5.1) and (5.2)

$$v_{c\alpha} = \frac{2}{3}[V_u - 0.5(V_v - V_w)] \quad (5.1)$$

$$v_{c\beta} = \frac{\sqrt{3}}{3}[V_v - V_w] \quad (5.2)$$

With the previous transformations, if the desired reference voltages are the three sinusoidal wave with a phase delay of  $120^\circ$  and a frequency  $\omega$ , on the complex plane, they will be represented on the complex plane with a vector with a constant amplitude and a frequency  $\omega$ . Moreover, thanks to the SVPWM when a leg is switching the other two keep their state. The SV transformation is also applied to the different possible states of the output voltages and their associated vectors, which are used to approximate every reference voltage, are depicted in the following table 5.1.

Table 5.1: Space vectors definition with respect of the state of the legs

Vector of the SVPWM			
$V_u$	$V_v$	$V_w$	Name
$-\frac{v}{2}$	$-\frac{v}{2}$	$-\frac{v}{2}$	$u_{s7}$
$\frac{v}{2}$	$-\frac{v}{2}$	$-\frac{v}{2}$	$u_{s1}$
$-\frac{v}{2}$	$\frac{v}{2}$	$-\frac{v}{2}$	$u_{s3}$
$\frac{v}{2}$	$\frac{v}{2}$	$-\frac{v}{2}$	$u_{s2}$
$-\frac{v}{2}$	$-\frac{v}{2}$	$\frac{v}{2}$	$u_{s5}$
$\frac{v}{2}$	$-\frac{v}{2}$	$\frac{v}{2}$	$u_{s6}$
$-\frac{v}{2}$	$\frac{v}{2}$	$\frac{v}{2}$	$u_{s4}$
$\frac{v}{2}$	$\frac{v}{2}$	$\frac{v}{2}$	$u_{s8}$

Their representation on the complex plane is instead depicted in the following Figure 5.1 and it can be seen that there are two zero vectors  $u_{s7}$  and  $u_{s8}$ .

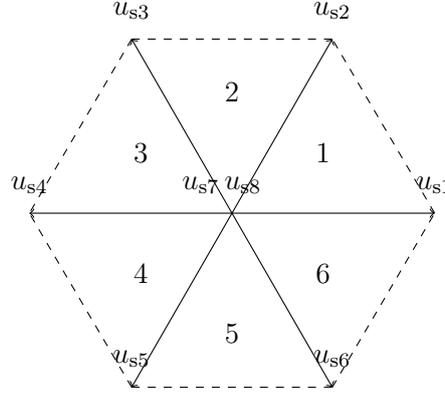


Figure 5.1: Space vector

If the reference voltage is in the first sector the inverter applies the following vectors in the following order:

$$u_{s7} \rightarrow u_{s1} \rightarrow u_{s2} \rightarrow u_{s8} \rightarrow u_{s2} \rightarrow u_{s1} \rightarrow u_{s7}$$

In the second sector the modulation has instead the following order:

$$u_{s8} \rightarrow u_{s2} \rightarrow u_{s3} \rightarrow u_{s7} \rightarrow u_{s3} \rightarrow u_{s2} \rightarrow u_{s8}$$

Equally they can be obtained for all the other sectors. In the third:

$$u_{s7} \rightarrow u_{s3} \rightarrow u_{s4} \rightarrow u_{s8} \rightarrow u_{s4} \rightarrow u_{s3} \rightarrow u_{s7}$$

In the fourth:

$$u_{s7} \rightarrow u_{s5} \rightarrow u_{s4} \rightarrow u_{s8} \rightarrow u_{s4} \rightarrow u_{s5} \rightarrow u_{s7}$$

In the fifth:

$$u_{s7} \rightarrow u_{s5} \rightarrow u_{s6} \rightarrow u_{s8} \rightarrow u_{s6} \rightarrow u_{s5} \rightarrow u_{s7}$$

And finally in the sixth:

$$u_{s8} \rightarrow u_{s6} \rightarrow u_{s1} \rightarrow u_{s7} \rightarrow u_{s1} \rightarrow u_{s6} \rightarrow u_{s8}$$

As explained previously the double pulse test is performed by switching the first leg only. Therefore in each series, only the change of vectors which is associated with the switch of the first leg is observed. In this way, it is possible to fix the other two legs, to be able to perform a DPT in every situation which can appear during the normal operation. In particular, the first sector has a switch from  $u_{s7}$  to  $u_{s1}$  which means that the two other legs are kept during the whole test with the low side on. The second sector instead has the switch of the first leg between  $u_{s2}$  to  $u_{s3}$  which means that the second leg is kept with the high side on and the third with the low side on. The third series instead requires to have the second and the third leg both with the high side turned on. The fourth and the fifth series don't provide any other different case than the first and the third case. The sixth case instead provides the last possible switching combination which is associated with the second leg with the low side on and the third leg with the high side on Figure from 5.2 to 5.5.

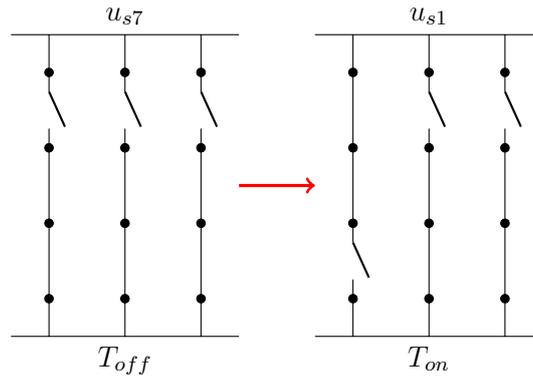


Figure 5.2: Inverter combination during the double pulse test with the first sector

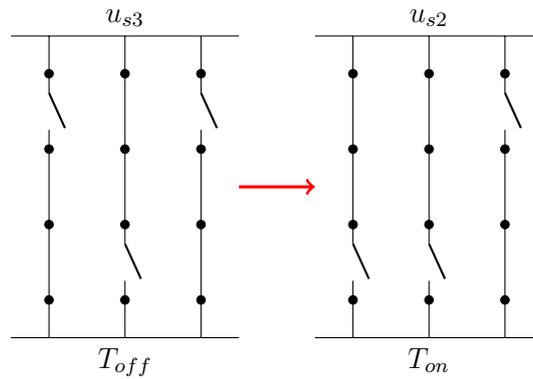


Figure 5.3: Inverter combination during the double pulse test with the second sector

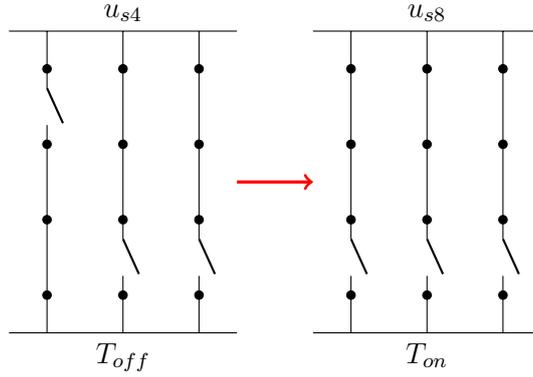


Figure 5.4: Inverter combination during the double pulse test with the third and fourth sector

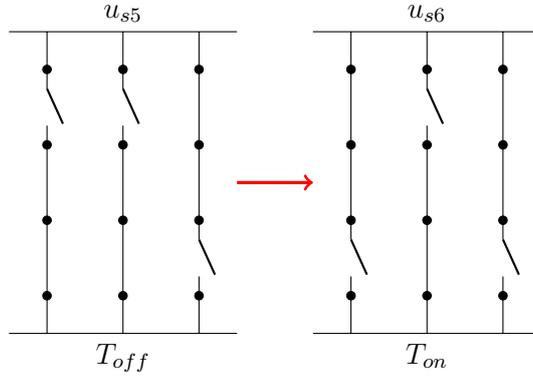


Figure 5.5: Inverter combination during the double pulse test with the fifth and sixth sector

It can be noticed from Figure 5.4 that this case is different since during the on-time a zero- state vector is applied. Therefore, the measurements with this characteristic are different from the measurements obtained in other cases. Moreover, to have the same drain current from the high side Mosfet of the first leg it is necessary to evaluate case by case the inductance at the output of the inverter since the other two legs affect the overall inductance.

It is moreover added an extra set of measurements with a particular double pulse test. The switch from  $u_{s7}$  (all the low sides MOSFETs turned on) to  $u_{s8}$  is also performed (all the high side MOSFETs turned off) (see Figure 5.6). This double pulse test is atypical since there is no current flowing. This double pulse test provides line voltages which are equal in every phase and it is a switching process which isn't usually employed in a normal application. It provides just the common-mode since the differential-mode is equal to 0 for the whole test. By performing this test, it is, hence, possible to determine if the common-mode voltage affects the DC link, which is usually affected mostly by the differential mode. Moreover, the common-mode voltage, in this case, has the highest  $\frac{dV}{dt}$  since it goes from 0 to 540V

( $V_{DC}$ ) and it is possible to evaluate the behavior of the common mode choke under such an extreme excitation.

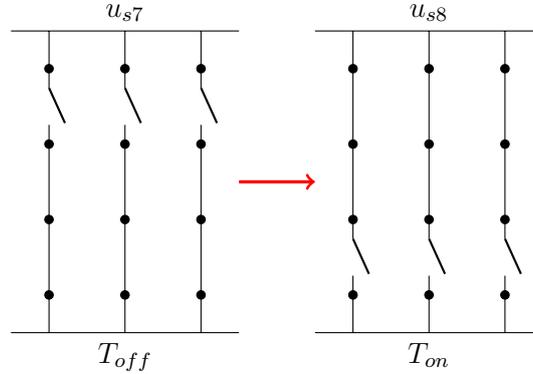


Figure 5.6: Double pulse test with the two zero-vectors

After these considerations, the implemented system to perform the double pulse test can now be described.

The system consists of a processor which receives the values of current by command line and a two-pulse block which drives the gates of the 6 SiC Mosfet, in order to perform a double pulse test (DPT) on the real inverter. The end of the process is given to the processor by a one-bit signal of the two pulse block when it arrives at the end of the second  $T_{on}$ . The value of the time of the various counters is given through the console of the processor (see Figure 5.8). The current which has to be reached and the decrease which we want during  $T_{off}$  are given through command line. The required time is obtained since the alimentation is known and the inductance depends on the switching state. The double pulse test is done on the high side of the first leg of the inverter. Therefore the system drives only the first leg (see Figure 5.7); the other two legs are kept in the different possible states described previously (see Figure 5.2, 5.3, 5.5)

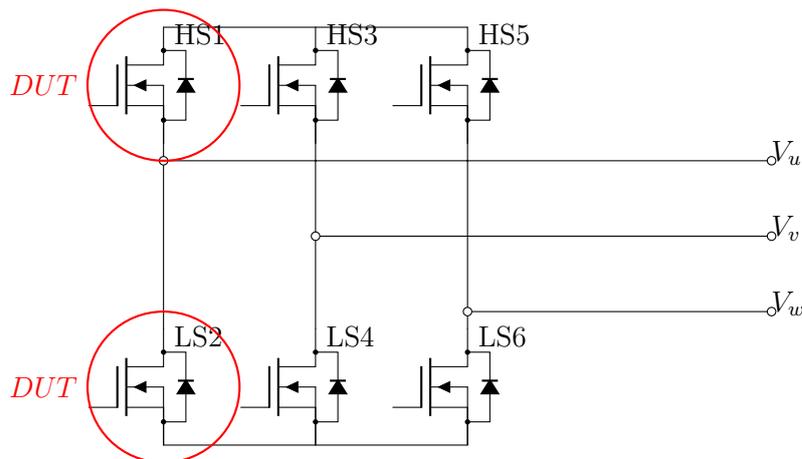


Figure 5.7: Device under test

## 5.1 Double pulse test FPGA description

A block which receives as input the following parameter depicted in table 5.2 has been implemented:

Input		
Name	bits	description
Reset	1	active low asynchronous reset
$T_{on1}, T_{on2}, T_{off}, T_{dead}$	32	length of the pulses and dead time
Quadrant	2	define the states of the other 2 legs of the inverter

Table 5.2: Input of the two pulse block

The scheme of the double pulse block is described in the following Figure 5.8

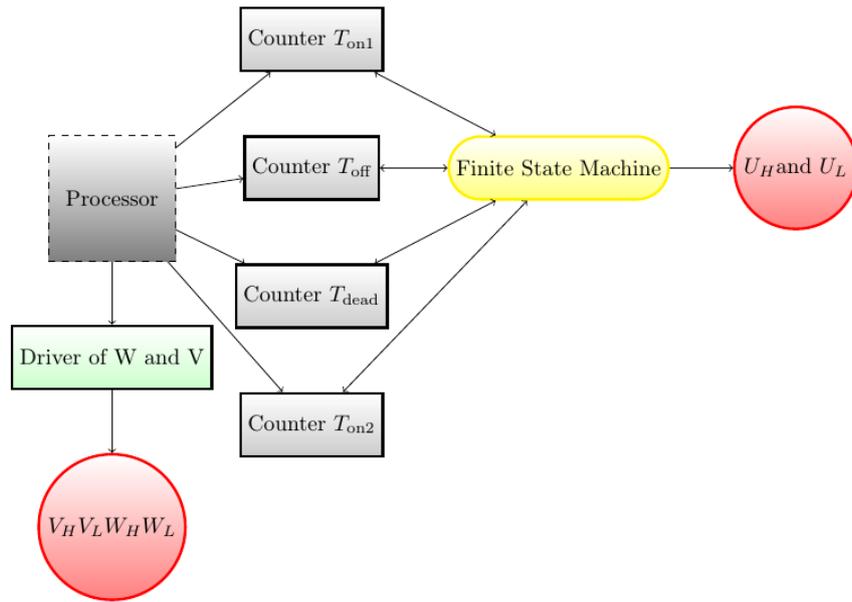


Figure 5.8: Double pulse block

It can be seen from Figure 5.8 that the system implemented on the FPGA consists of 4 counters. Each counter is set by the processor with the amount of time required. There is therefore a counter which defines the length of the first pulse (called  $T_{on1}$  in Figure 5.8), a counter with the dead time ( $T_{dead}$  in Figure 5.8), a counter for the off-time ( $T_{off}$  in Figure 5.8) and a counter with the length of the second pulse ( $T_{on2}$  in Figure 5.8). Each of these counters has a start signal which is activated by the finite state machine called FSM in Figure 5.8. Moreover, the counters send signals to the FSM which are used to change

state. The finite state machine drives the first leg to perform the double pulse test, while the other two legs are driven by digital logic circuits (Driver of W and V in Figure 5.8) according to the value of the two bits placed in a register which is written by the processor.

## 5.2 Finite State Machine

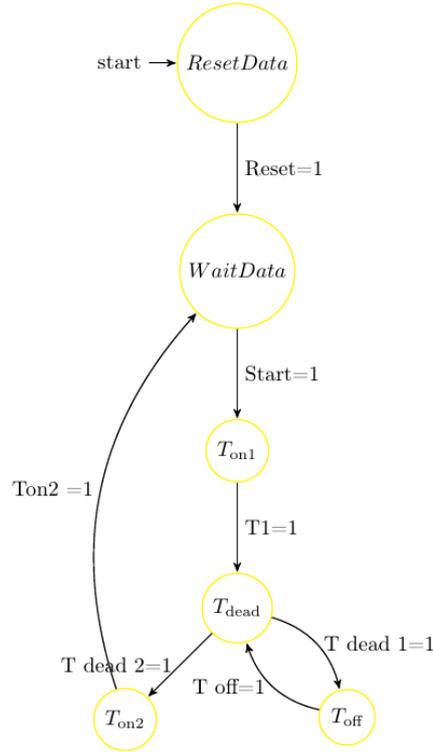


Figure 5.9: Finite state machine

It can be seen from Figure 5.9 that the Wait Data is the so-called idle state where the system waits to receive the value to set the counters. Once that information is received, the system enters the state  $T_{on1}$  where the first counter starts counting for the period of the first pulse. In this period the high side of the first leg is on. After the counter has reached its threshold, it sends the signal  $T1 = 1$  and the system moves in the state  $T_{dead}$  which is constant and it is usually 0.5 ns. In this state, both sides are off. At the end of the first  $T_{dead}$ , the system enters in the state  $T_{off}$  where the low side is on. When the counter associated to the off-time has finished, the FSM goes again in state  $T_{dead}$  and at the end of this second count, it enters in the second pulse period. At the end of this second pulse, the system returns in the idle state Wait Data. In the state Wait Data, all the leg have the low side turned on ( $u_{s7}$ )

The whole behavior of the gate signal of the first leg is depicted in Figure 5.10.

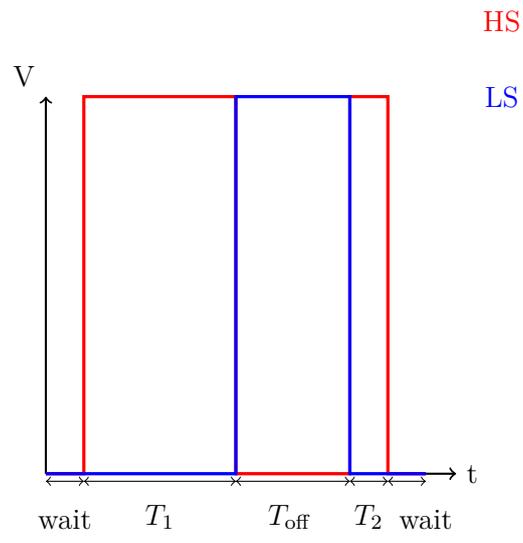


Figure 5.10: Signal gates

**Part III**

**Measurements**

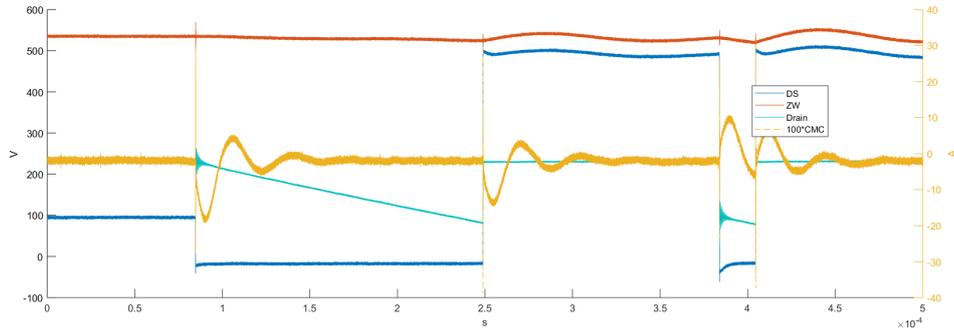


Figure 5.11: Double pulse test measurements

The measurements are performed through the oscilloscope Keysight Infinium S-Series DS0s054A with a bandwidth of 500MHz, 10 bit ADC vertical resolution and 4 channels. The device works in the single-shot mode. It records simply the double pulse test and at the end of the acquisition, the oscilloscope stops the sampling process. The first channel is employed to measure the DC link which can be considered the input of the converter and it provides information about the differential mode. The second channel instead is used to measure the drain-source voltage  $V_{ds}$  which can be considered the output of our system since the voltage on the output cable is  $V_{DC} - V_{DS}$  with  $V_{DC}$  considered constant. The  $V_{DS}$  is relevant to measure the rise and fall time as explained previously in Chapter 3. The drain current is measured through a Rogowski coil since the current is impulsive. The Rogowski coil doesn't allow to measure the common-mode current since the coil hasn't a bandwidth large enough to get all the components of the common-mode current. At this purpose, a wide bandwidth probe is used to measure the output CM current.

## Chapter 6

# Measurements under different currents

The first set of measurements is made by varying the drain currents, which means actually different  $T_{on}$ . The measurements are performed with 20 A, 15 A and 10 A (Figure 6.1).

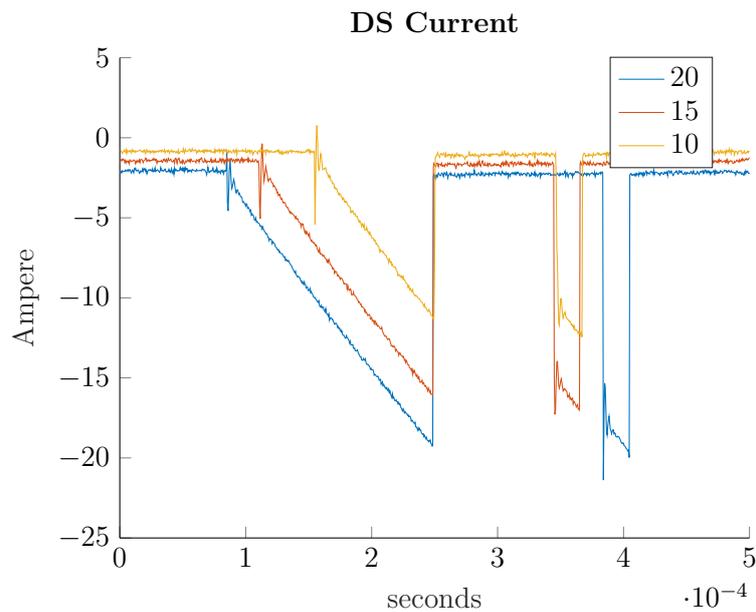


Figure 6.1: Different drain current measurements

This first set of measurements is relevant to evaluate the effect of the drain current on the common-mode current and it is used to evaluate the rise time which is dependent on the drain current. The measured common-mode current is depicted in the following Figure 6.2

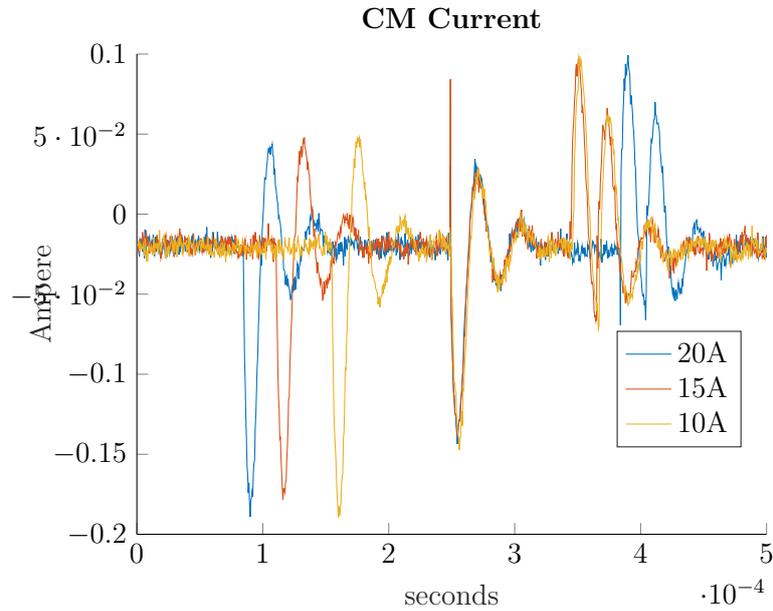


Figure 6.2: Common mode current measured with different drain current

From the previous picture, it can be seen that the behavior of the common-mode current is independent of the drain current. This analysis is confirmed also in the frequency domain (Figure 6.3)

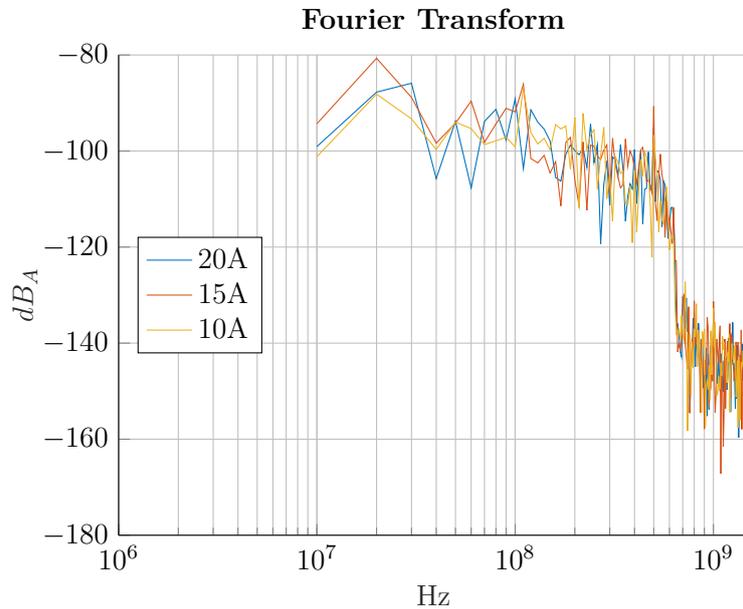


Figure 6.3: Common mode current in frequency domain

From this first comparison, it can be noticed that the drain current does not influence

the common-mode current. This information is used in the simulation to evaluate one single case, since it has been proved that the length of the pulse doesn't affect the common-mode current. In the modelization of the system for the common mode current, the inverter is considered as a single voltage generator which generates just the equivalent common-mode voltage, without taking into account the behavior of the single transistor. Instead, the drain-source voltage's behavior and the DC link oscillations are described through consideration on the parasitic components of the MOSFET. As explained in Chapter 3 the rise time of the  $V_{ds}$  during the double pulse test change according to the parasitic capacitance  $C_{ds}$ . In this case, it is necessary to consider the transistors and their switching behavior.

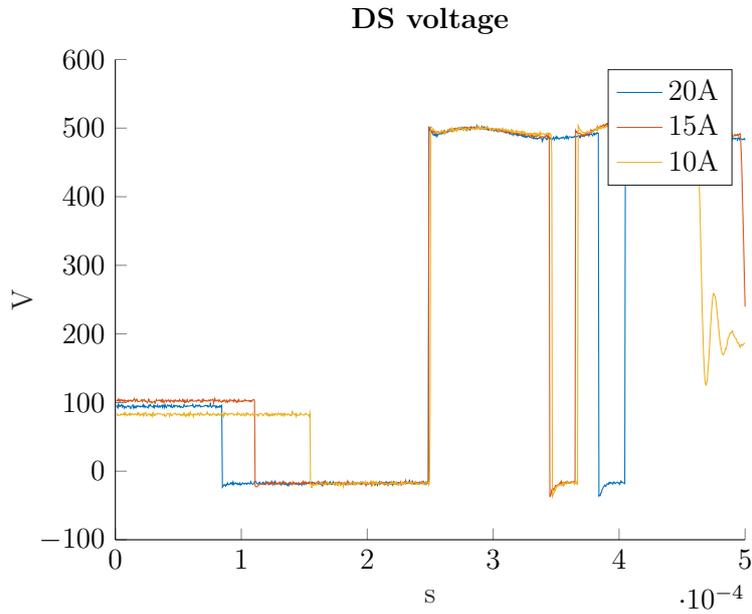


Figure 6.4: Drain Source voltage with different  $T_{on}$

From Figure 6.4 the rise and the fall time can be analyzed according to the theory in Chapter 3. In particular, from this first analysis, the parasitic capacitance in parallel to the MOSFET can be estimated with a first approximation, since it is considered voltage-independent. Moreover, the current is assumed constant for the whole switching process and the threshold of the diode is neglected. In particular (6.1) is valid.

$$t_{rise} = \frac{C_{ds}V_{DC}}{I_L} \quad (6.1)$$

From Figure 6.4 the rise and fall time are measured. As explained in Chapter 3, in this case, the rise time depends on the current which is flowing in the high side MOSFET of the device, while the fall time remains constant. As it can be seen from Figure 6.5, the rise time is characterized by an overshoot which turns on the diode. A  $t_{rise} = 17ns$  and a fall time  $t_{fall} = 30.3ns$  have been measured. The measured rise time is compliant to the rise time obtained from (6.1)

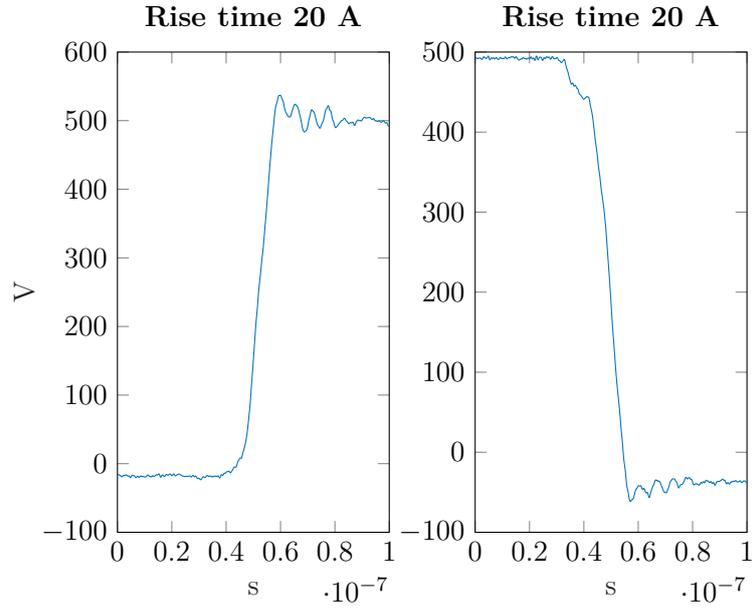


Figure 6.5: Rise and fall time with 20 A flowing

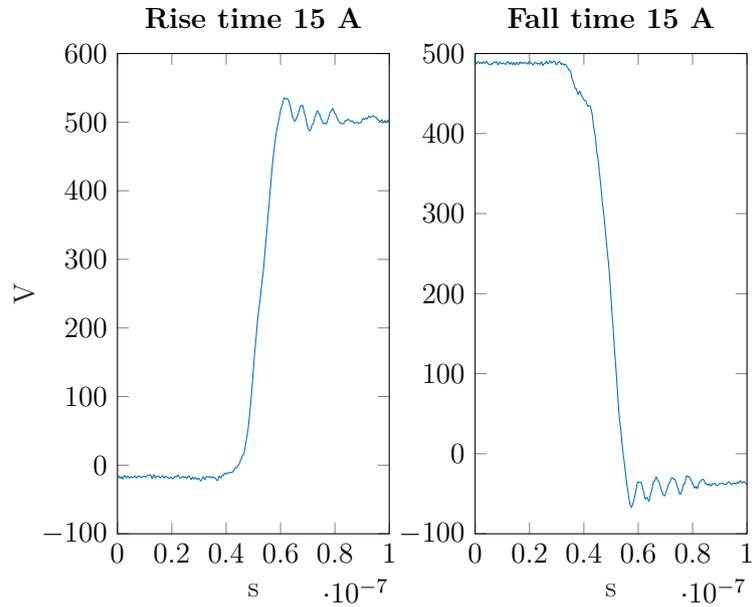


Figure 6.6: Rise and fall time with 15 A flowing

The Figure 6.6 shows the rise and the fall time obtained with 15 A. The  $t_{rise} = 18.8ns$  and the  $t_{fall} = 30.5ns$

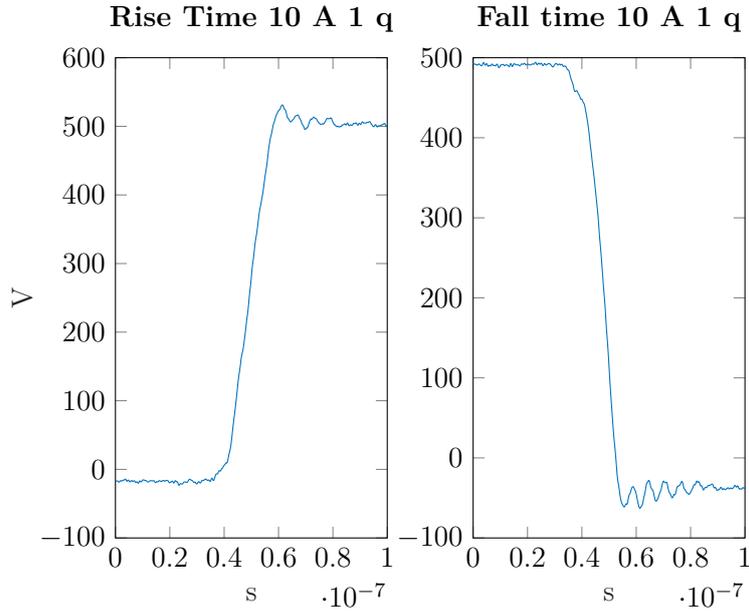


Figure 6.7: Rise and fall time with 10 A flowing

Equally, it is noticed that with 10 A the The  $t_{rise} = 23.8ns$  and the  $t_{fall} = 30.8ns$ . This rise time are also predicted by (6.1)

In this first set of measurements, the DC link behavior for the different drain current has been also analyzed. An further analysis has been carried out with respect to the different switching vectors. At the same time, this kind of measurement doesn't provide any other additional information. The DC link has the following behavior during the double pulse test as depicted in the following Figure 6.8

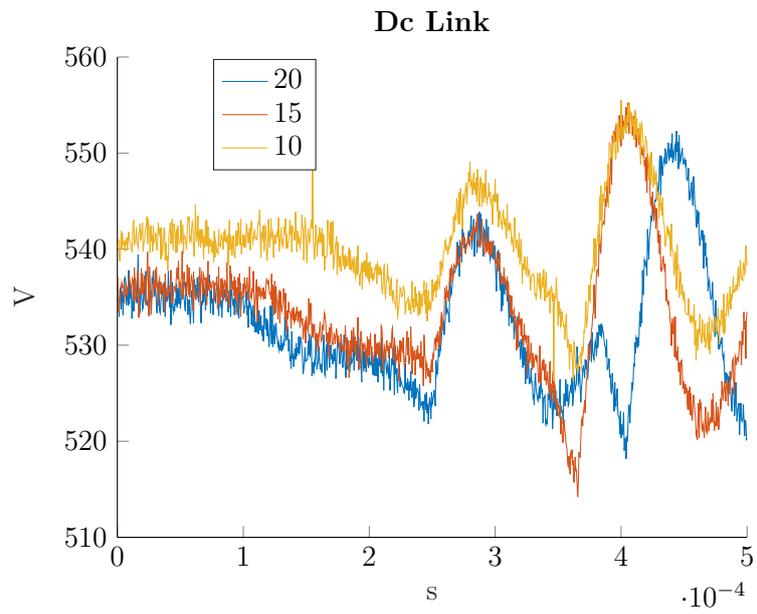


Figure 6.8: DC Link with different current flowing

## Chapter 7

# Double pulse test with different vectors

The second analysis is instead performed by considering the different vectors which were explained in Chapter 5.

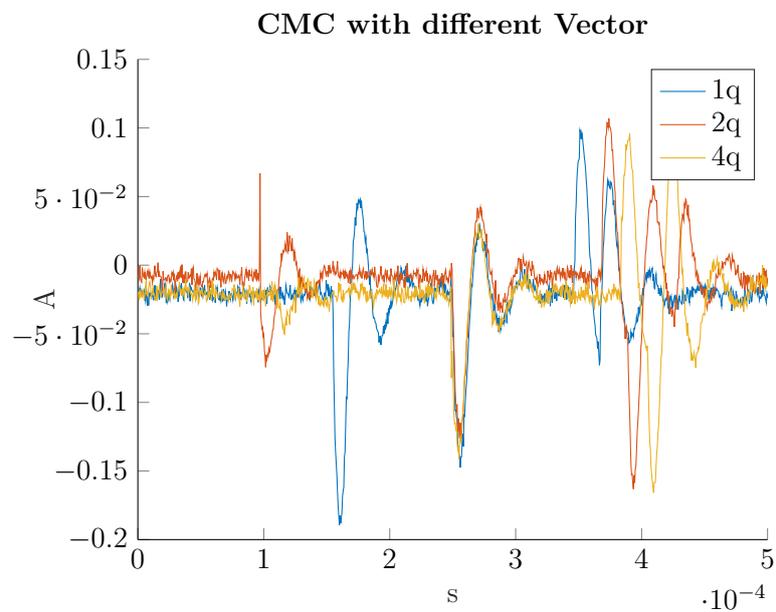


Figure 7.1: Common mode current measured with different vectors switching

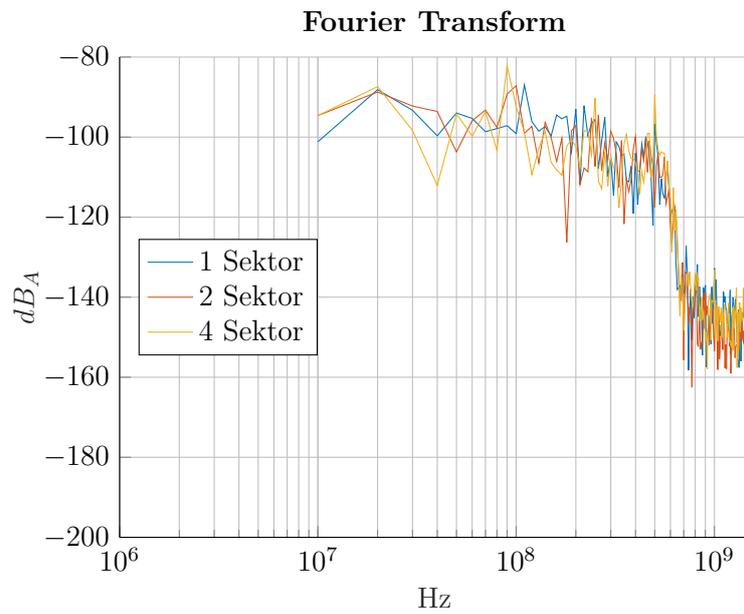


Figure 7.2: Common mode current in frequency domain with different vectors switching

As it can be seen from Figure 7.1 and 7.2 also the state of the other 2 legs has no effect on the common mode current. Therefore the simulation can be performed also by considering only 2 switching vectors. The analysis of the DC link during this test doesn't provide any other information.

# Chapter 8

## Special Vector

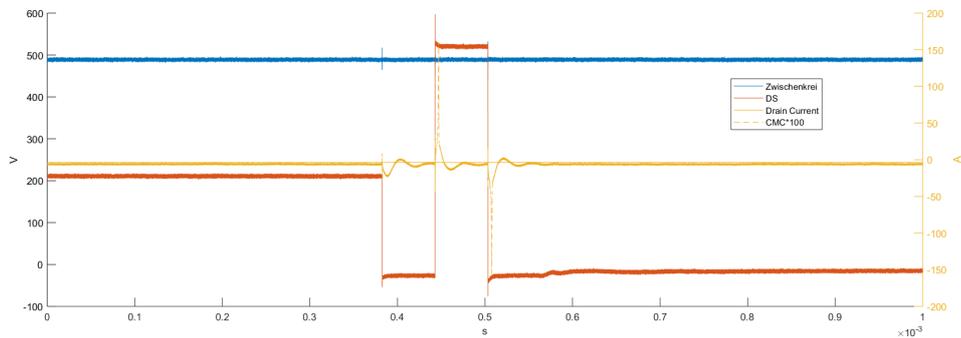


Figure 8.1: Measurement obtained with a specific double pulse test

A set of measurements with a specific double pulse test between the vectors  $u_{s7}$  and  $u_{s8}$  is recorded (see Chapter 5). As explained previously, this kind of double pulse test allows applying on the whole system just the common mode. The result is depicted in Figure 8.1. There is no current flowing during the whole measurement since only the zero vectors of the SVPWM are applied. The analysis is focused on the DC link (Figure 8.3) and the common-mode current (Figure 8.2).

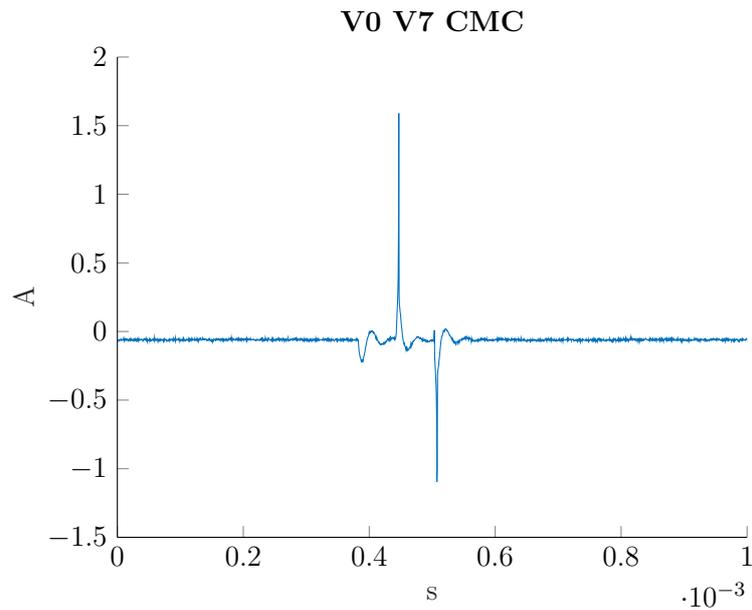


Figure 8.2: Measurement of the common mode current with a specific double pulse test

As it can be seen in Figure 8.2 the common-mode choke saturates in this case. This is because the common-mode voltage springs from 0 to the value of the DC link. This double pulse test doesn't affect the DC link, which means that the common-mode does not affect the input of the inverter as it was expected according to the ideal model as shown in Figure 8.3.

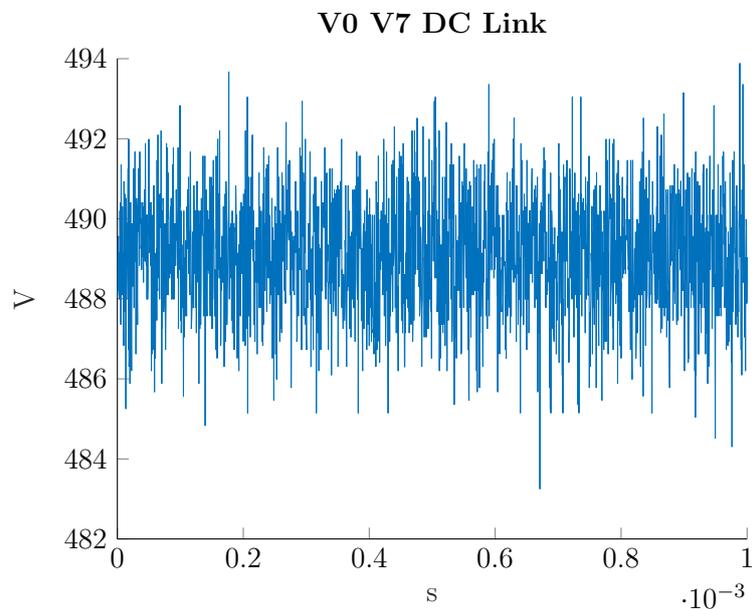


Figure 8.3: Measurement of the common mode current with a specific double pulse test

## Chapter 9

# Oscillation at the DC side

In the previous analysis, the inverter was modeled just like a voltage source which generates a square wave. This representation has the drawback that the information associated with the switching characteristic of the device is lost. Hence, it is not possible to simulate the effects on the system due to the non-ideal behavior of the switches with the previous models. In particular, the oscillations on the DC link are associated mostly to the differential mode. The frequency of this oscillation is correlated to the parasitic capacitance among the drain and the source of the device ( $C_{ds}$ ). This last section has the aim to evaluate if it is possible to evaluate these phenomena due to the parameters of the device at a low computational cost with sufficient precision.

The analysis starts with the observation of the oscillation during the double pulse test. As explained in Chapter 6, during the double pulse test the DC link is also measured. Therefore, a capacitance of  $1nF$  is added in parallel to every single device and the double pulse test is repeated. In this way, the effect of the parasitic capacitances on the oscillation of the DC link can be estimated. The second step is to evaluate if it is possible to foresee this oscillation through any kind of computation. The previous models aren't able to evaluate these oscillations as explained previously. Hence, a PCB description of the converter is used. This model is then exploited to perform a simulation where on each  $V_{ds}$  of the 6 switches of the inverter is applied the equivalent voltage  $V_{ds}$  which happens during the double pulse test. In this way, the behavior of the inverter during the double pulse test is simulated.

## 9.1 Measurements with and without the added Capacitance

The first step of this analysis is the evaluation of this phenomenon through a double pulse test. The double pulse test has been performed with different current, which means different  $T_{on}$ . The second set of measurements has been taken after that 1 nF capacitance is added to all the components of the converter (Figure 9.1)

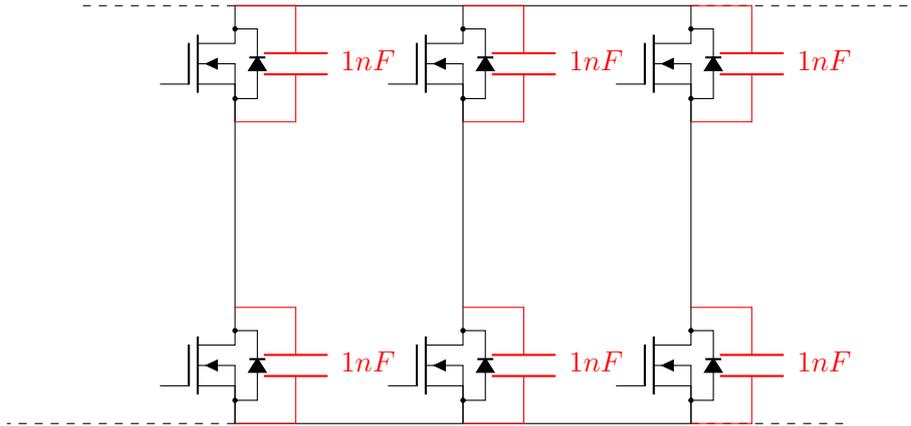


Figure 9.1: System with extra capacitances

The measurements are described in Figure 9.2 and in Figure 9.3.

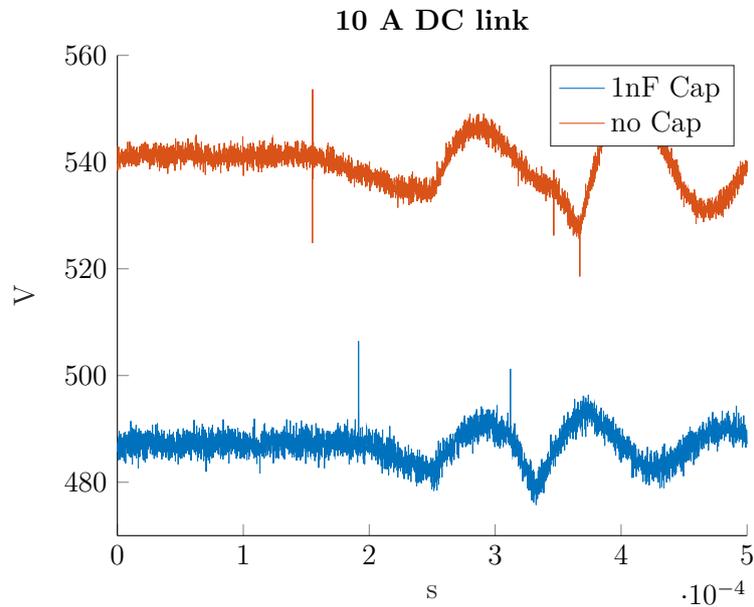


Figure 9.2: Oscillation of the DC Link with the addition of the 1nF capacitance and a drain source of 10A

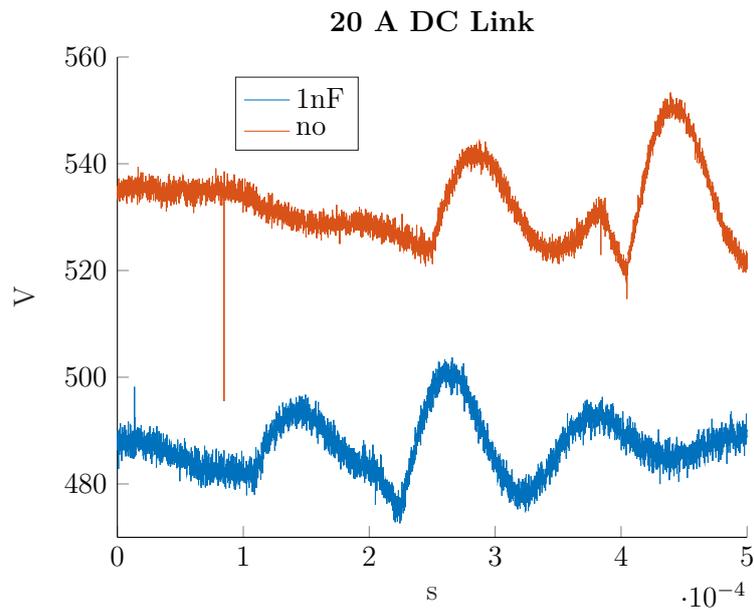


Figure 9.3: Oscillation of the DC Link with the addition of the 1nF capacitance and a drain current of 20 A

From these measurements in the time domain, the effect of the capacitances is not clear on the oscillations. More information are obtained through a Fourier analysis. The result is depicted in the following Figure 9.6

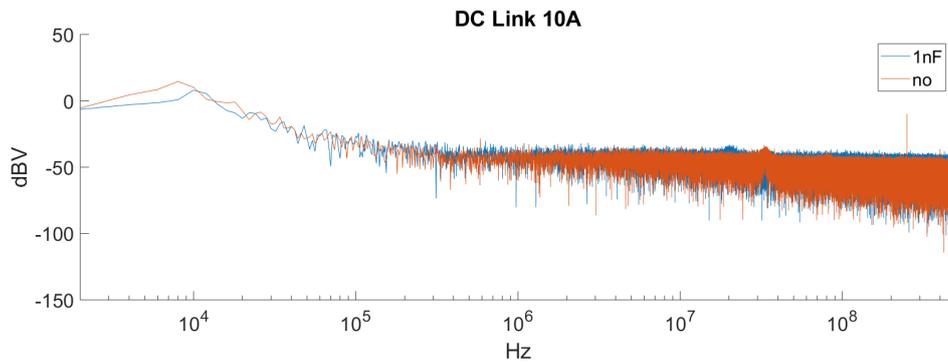


Figure 9.4: Fourier analysis of the DC Link oscillation with 10 A

It can be seen from Figure 9.6 that the frequency of the oscillation has shifted to lower frequencies in the case of the extra capacitance added in parallel. In the following Figure 9.7 a movement to lower frequencies (from 32MHz to 20 MHz) of the oscillation of the DC link can be seen.

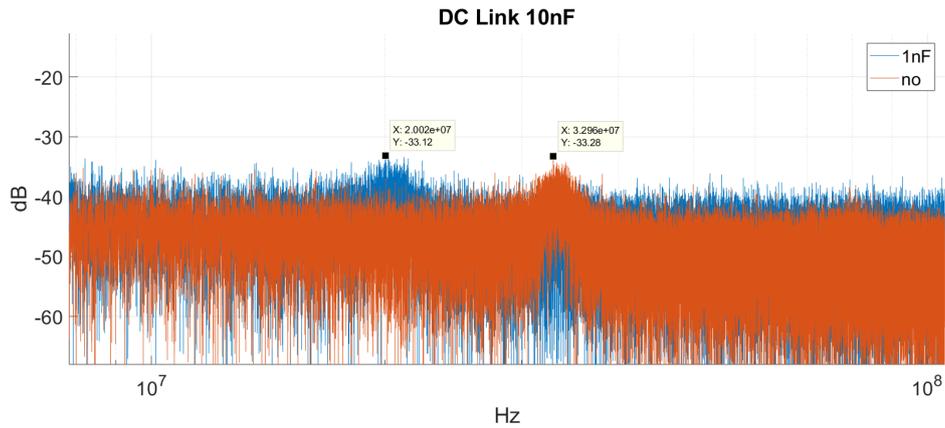


Figure 9.5: Fourier analysis of the DC Link oscillation with 10 A Zoom

The same Fourier analysis is performed on the measurements taken with 20 A

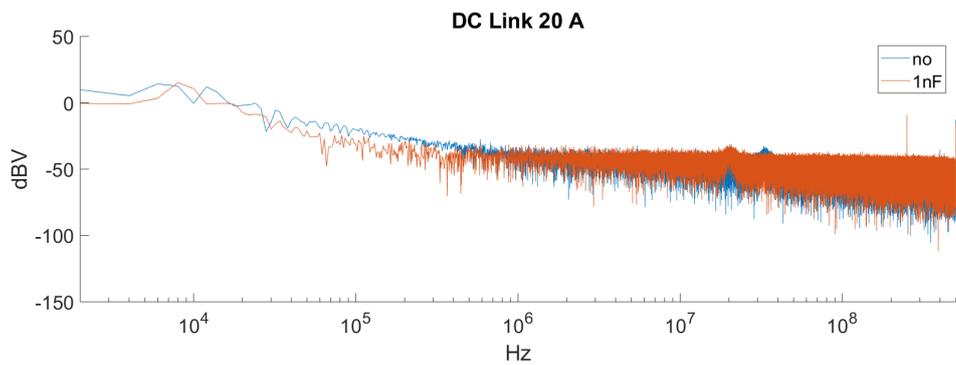


Figure 9.6: Fourier analysis of the DC link oscillation with 20 A

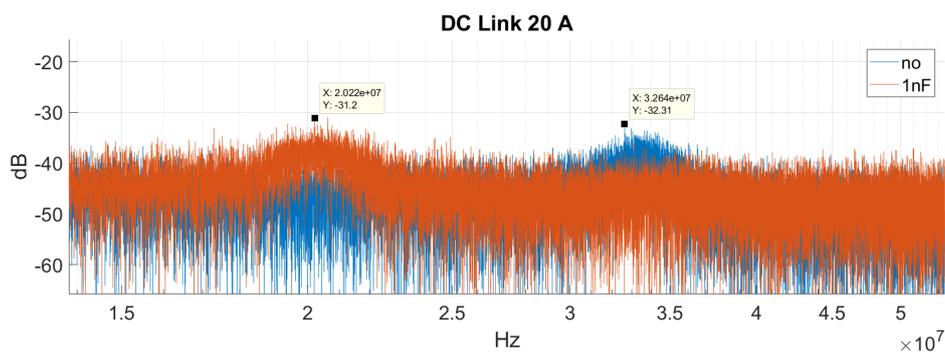


Figure 9.7: Fourier analysis of the DC link oscillation with 20 A Zoom

The frequency of the oscillation is considerably reduced because of the added capacitances. No influence of the different current on the oscillations can be seen. At the same

time, it can be noticed that the frequency of these oscillations is entirely due to parasitic parameters of the device and it has no correlation with the current.

**Part IV**

**Simulations**

# Chapter 10

## Common mode current Simulation

### 10.1 Analysis with simplified Model

After the measurements described in Chapter 6, a function, which allows estimating the behavior of the common-mode current, has been developed. This function links the common-mode current at the output of the 3-phase EMI filter with the common-mode input voltage, which is related to the voltage of the three legs according to the equations described in Chapter 2. During the measurements in Chapter 6 the effect of the length of the pulse and of the different switching vectors on the common-mode current has been analyzed and it has been empirically shown that there is no effect on the common-mode current. Therefore, all the simulations were carried out by using always the same switching vectors and the same  $T_{on}$ . In the next part, it is described how the depicted system is manipulated to get the desired transmission function  $\frac{I_{cm, f.o}}{U_{cm}}$  which links the common mode current at the output of the filter and the common-mode voltage of the inverter. The first analysis is done by using the model depicted in Figure 2.7. Each component of the system is described through a Z matrix or a Y matrix. It is necessary to represent all the components with matrices. For this purpose, the easiest method is to convert all the Z matrices into transmission matrices [38].

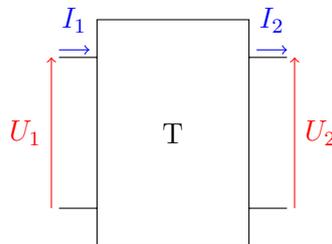


Figure 10.1: Transmission Matrix

The relations which define the transmission matrix are described in (10.1).

$$\begin{pmatrix} U_2 \\ I_2 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} U_1 \\ I_1 \end{pmatrix} \quad (10.1)$$

The transmission matrix has two properties which are helpful for the computations. Firstly, the overall matrix of a cascade of transmission matrices is simply the multiplication of the transmission matrices in the order they appear. For example, with two matrices  $T_1$  and  $T_2$  the total matrix is  $T_{tot} = T_1T_2$ , if  $T_1$  is the input matrix and equally is  $T_{tot} = T_2T_1$ , if  $T_2$  is the first one. The second property is that  $T^{-1}$  puts into relation  $U_1$  and  $I_1$  with respect of  $U_2$  and  $I_2$ . The system is therefore described as depicted in the following Figure 10.2

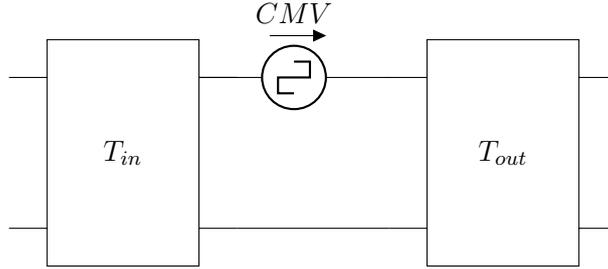


Figure 10.2: System

In the picture we have obtained  $T_{out}$  and  $T_{in}$  through the following equations respectively (10.2) and (10.3).

$$T_{out} = T_{out,inv}T_{out,filter}T_{out,cable}T_{motor} \quad (10.2)$$

$$T_{in} = T_{in,inv}T_{in,filter}T_{in,cable}T_{LISN} \quad (10.3)$$

The two matrices can be converted back to the Z matrix. In this way, it is possible to obtain a voltage divider which allows evaluating the part of the common-mode voltage which falls on the output side (Figure 10.3).

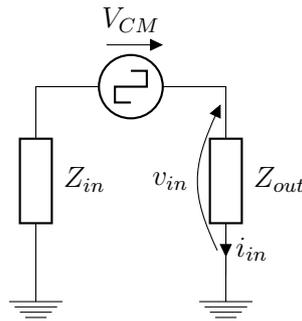


Figure 10.3: Voltage divider for the common mode current

In order to evaluate the common-mode current, we are interested in the input voltage  $V_{in}$  and the input current  $I_{in}$ .

$$V_{in} = V_{CM} \frac{Z_{out}}{Z_{out} + Z_{in}}$$

and

$$V_{in} = \frac{V_{CM}}{Z_{out} + Z_{in}}$$

Once the input of the system has been analyzed then the model depicted in the following Figure 10.4 is employed.

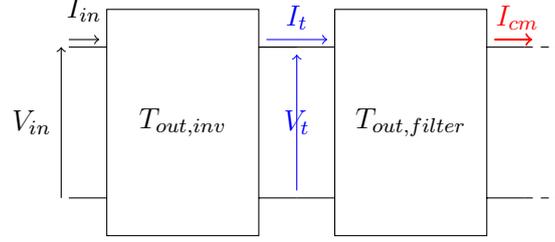


Figure 10.4: Common mode model to compute the common mode current at the output of the filter

As it can be seen from Figure 10.4, it is possible to link  $V_{in}$  and  $I_{in}$  to  $V_t$  and  $I_t$ . The relation for the voltage  $V_t$  is given in (10.4).

$$V_t = A_1 V_{in} + B_1 I_{in} \quad (10.4)$$

The equation for the current  $I_t$  is instead described in (10.5).

$$I_t = C_1 V_{in} + D_1 I_{in} \quad (10.5)$$

The current  $I_{cm}$  is at the output of the second transmission matrix, therefore it is described in the following (10.6).

$$I_{cm} = C_2 V_t + D_2 I_t \quad (10.6)$$

By using (10.4) and (10.5), (10.7) is then obtained.

$$I_{cm} = C_2 \left( A_1 V_{CM} \frac{Z_{out}}{Z_{out} + Z_{in}} + B_1 \frac{V_{CM}}{Z_{out} + Z_{in}} \right) + D_2 \left( C_1 V_{CM} \frac{Z_{out}}{Z_{out} + Z_{in}} + D_1 \frac{V_{CM}}{Z_{out} + Z_{in}} \right) \quad (10.7)$$

It is possible from (10.7) to get the desired transmission function (10.8).

$$\frac{I_{cm}}{V_{CM}} = \frac{Z_{out}}{Z_{out} + Z_{in}} (C_2 A_1 + D_2 C_1) + \frac{1}{Z_{out} + Z_{in}} (C_2 B_1 + D_2 D_1) \quad (10.8)$$

The transmission function in (10.8) consists just in a set of discrete values which were measured in the frequency domain. It is, therefore, necessary to obtain from this set of points in the frequency domain a function in the time domain. The vector fitting allows computing from a set of data in frequencies domain a function of the form described in (10.9) [39].

$$F(s) \approx \sum_{n=1}^M \frac{c_n}{s - a_n} + d + sh \quad (10.9)$$

Once all the poles and the coefficients are obtained, a transmission function  $F(s) = \frac{I_{cm}}{V_{cm}}$  can be written. From this function, the time response of the common-mode current is computed through a simple convolution product

$$I_{cm}(t) = f(t) * V_{cm}(t)$$

The input used for the computation is depicted in the following Figure 10.5. The rise and the fall time are associated to the measured rise and fall time in the case of 20 A and the vector  $u_{s1}$ .

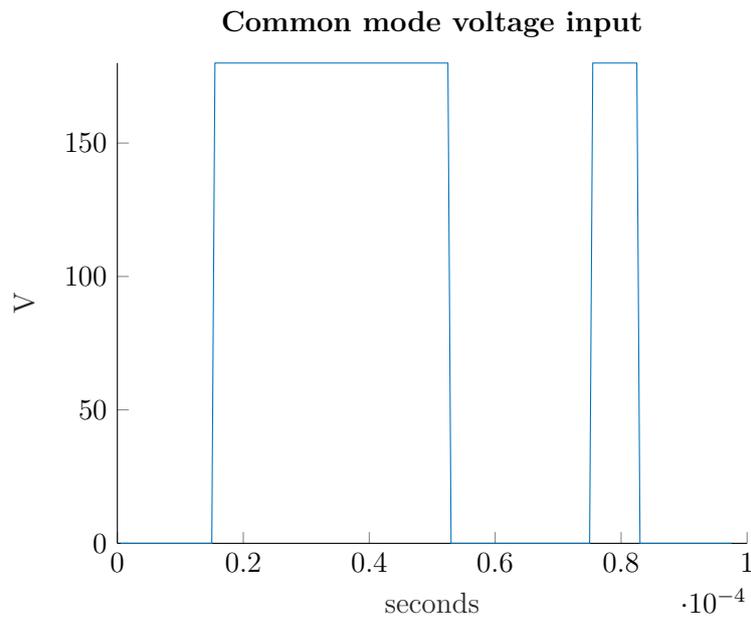


Figure 10.5: Common mode voltage used as input

The result obtained with the depicted transmission function is depicted in Figure 10.6

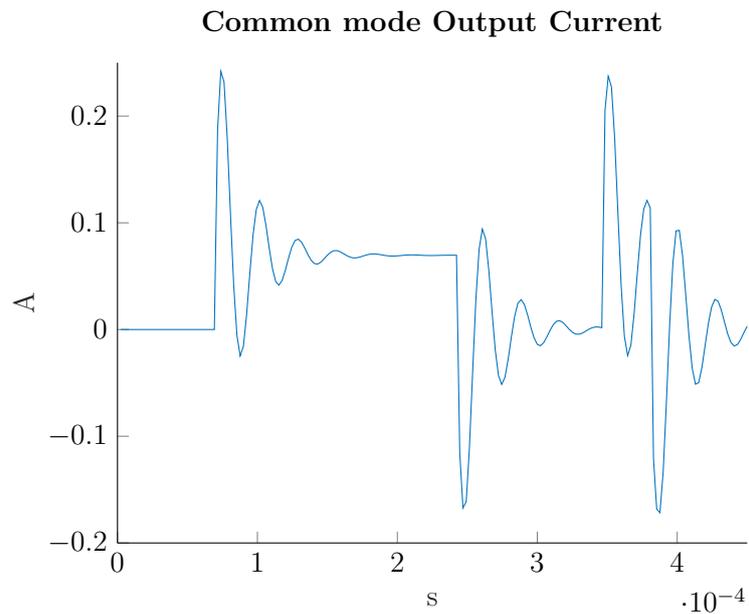


Figure 10.6: Common mode Current obtained with the previous model

The desired behavior is similar to the measured common-mode current. It is clear at the same time that the high frequencies oscillations are not represented. This result was expected; as explained in Chapter 2, the frequency parameters which are used to describe the transmission function are measured up to 30 MHz. This upper limit is not high enough to describe perfectly the system. This same analysis is confirmed by the Fourier transform and its comparison with the real common mode current (Figure 10.7)

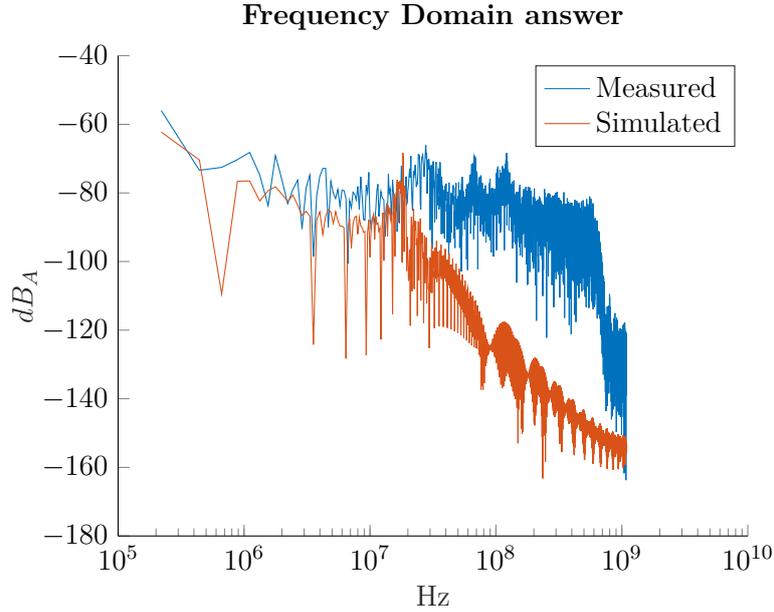


Figure 10.7: Common mode Current simulated and measured in frequency domain

It can be clearly seen that the simulated result is valid up to the MHz region. At higher frequency the transmission function is no longer valid and its behavior differs from the real one.

## 10.2 Analysis with 6 port Model

The limits described in the previous section can be solved through an analysis that provides a description also at very high frequencies. The 6-port model provides measurements up to 150 MHz, as explained in Chapter 2. In this model, each block has three ports at input and three ports at the output. 2 ports are associated with the common mode. They are defined by  $I_{cm,in}$ ,  $I_{cm,out}$  and  $V_{cm,in}$ ,  $V_{cm,out}$ . The other 4 ports are associated with the input and the output differential mode. In our analysis, voltages for the differential mode and the output common mode of the last element (the motor) have been considered equal to 0. Therefore, these ports are short-circuited. The 6-port matrix describes the following model (10.10).

$$\begin{pmatrix} V_{cm,in} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} & \dots & Z_{16} \\ Z_{21} & Z_{22} & \dots & Z_{26} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{61} & Z_{62} & \dots & Z_{66} \end{pmatrix} \begin{pmatrix} I_{cm,in} \\ I_{dm1,in} \\ I_{dm2,in} \\ I_{cm,out} \\ I_{dm1,in} \\ I_{dm2,in} \end{pmatrix} \quad (10.10)$$

. The matrix 6X6 is divided in 4 different matrix which are only 3X3.

$$Z = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \quad (10.11)$$

where A is defined as follows (10.12).

$$A = \begin{pmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{32} & Z_{33} \end{pmatrix} \quad (10.12)$$

and equally all the other sub-matrices. Where B is defined in (10.13), C in (10.14) and D in (10.15).

$$B = \begin{pmatrix} Z_{14} & Z_{15} & Z_{16} \\ Z_{24} & Z_{25} & Z_{26} \\ Z_{34} & Z_{35} & Z_{36} \end{pmatrix} \quad (10.13)$$

$$C = \begin{pmatrix} Z_{41} & Z_{42} & Z_{43} \\ Z_{51} & Z_{52} & Z_{53} \\ Z_{61} & Z_{62} & Z_{63} \end{pmatrix} \quad (10.14)$$

$$D = \begin{pmatrix} Z_{44} & Z_{45} & Z_{46} \\ Z_{54} & Z_{55} & Z_{56} \\ Z_{64} & Z_{65} & Z_{66} \end{pmatrix} \quad (10.15)$$

Matrix A links the input currents to the input voltages, B the output currents to the input voltages, C links the output voltages with the inputs currents and D correlates just the output voltages with the output currents. Our system is described with a six-port model but to evaluate the transmission function the ports 1 and 4 associated to the common-mode are sufficient. In order not to lose the correlation between the differential mode and the common-mode, it is necessary to manipulate the whole system. The common-mode impedances  $Z_{in}$  at port 4 of the chain of the 4X4 matrices and the  $Z_{out}$  at port 1 in the chain of the 6X6 matrices are required to proceed with the computation. The  $Z_{in}$  is obtained by using the 4X4 matrix instead of the 6X6 but the process is similar. As follows the process for the 6X6 side is described.

$$\vec{V}_{in} = \begin{pmatrix} V_{cm,in} \\ 0 \\ 0 \end{pmatrix} \quad (10.16)$$

$$\vec{V}_{out} = \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix} \quad (10.17)$$

$$\vec{I}_{in} = \begin{pmatrix} I_{cm,in} \\ I_{dm1,in} \\ I_{dm2,in} \end{pmatrix} \quad (10.18)$$

$$\vec{I}_{out} = \begin{pmatrix} I_{cm,out} \\ I_{dm1,out} \\ I_{dm2,out} \end{pmatrix} \quad (10.19)$$

$$\begin{cases} \vec{V}_{in} = A\vec{I}_{in} + B\vec{I}_{out} \\ 0 = C\vec{I}_{in} + D\vec{I}_{out} \end{cases} \quad (10.20)$$

The following system is valid and has to be solved by obtaining only  $\vec{V}_{in}$  and  $\vec{I}_{in}$ . The solution is obtained and provides a 3x3 matrix called F from which is possible to get  $\frac{V_{cm}}{I_{cm}}$  (10.22).

$$\vec{V}_{in} = (A - B(D^{-1}C))\vec{I}_{in} \quad (10.21)$$

$$F = (A - B(D^{-1}C)) \quad (10.22)$$

The system which has to be solved is now the following (10.23).

$$\begin{cases} V_{cm,in} = F_{11}I_{cm,in} + F_{12}I_{dm1,in} + F_{13}I_{dm2,in} \\ 0 = F_{21}I_{cm,in} + F_{22}I_{dm1,in} + F_{23}I_{dm2,in} \\ 0 = F_{31}I_{cm,in} + F_{32}I_{dm1,in} + F_{33}I_{dm2,in} \end{cases} \quad (10.23)$$

The solution of the previous system (10.23) allows to evaluate the impedance  $Z_{cm,out}$  of Figure 10.2.

$$Z_{cmout} = F_{11} + AF_{12} + BF_{13} \quad (10.24)$$

where A is

$$A = \frac{F_{33}F_{21} - F_{31}F_{23}}{F_{32}F_{23} - F_{33}F_{22}} \quad (10.25)$$

and B is

$$B = -\frac{F_{21}}{F_{23}} - A\frac{F_{22}}{F_{23}} \quad (10.26)$$

A similar process can be done for the input side with some simplifications since the matrix is only a 4X4 and it is reduced to a simple 2X2 with the same process. Once the voltage divider has been derived from the 6-port matrices, the next step is to use the transmission matrix to evaluate the common mode current at the output of the inverter. In this case, the 6X6 transmission matrix of the inverter and the transmission matrix of the output filter are multiplied, to have just a single transmission matrix, which is converted in Y matrix in order to consider also the coupling between the common and differential mode. The rest of the common-mode circuit is taken into account by adding at the port 4 the common-mode impedance of the system of cable and motor, which is also measured by multiplying the two transmission matrices. To keep into account also the coupling of this system in the evaluation of the impedance of the concatenation of motor and cable, it is necessary to work with the Y matrix and then to get the associated Z matrix. This solution allows us to have only 2 input  $V_{cm,in}$  and  $V_{cm,out}$  instead of the 6 input with the Z matrix. It is obtained the following system in Figure 10.8.

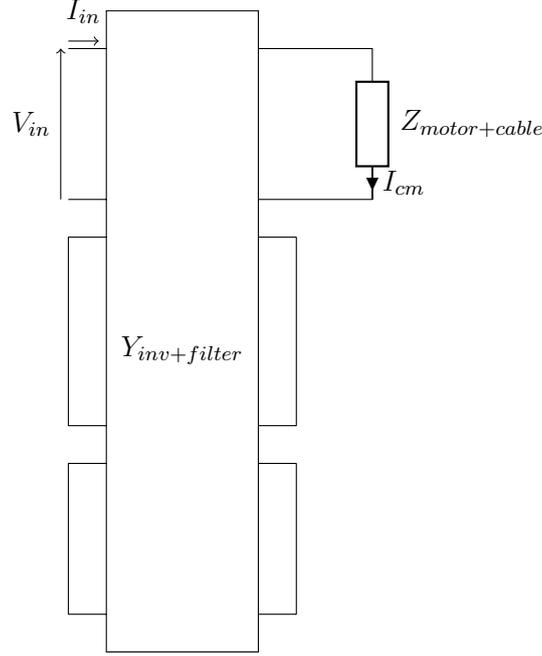


Figure 10.8: 6 Port network

The Y matrix of the matrix defined by output filter and inverter defines the following system (10.27) which can be used to get the transmission function  $\frac{I_{cm,out}}{V_{cm,in}}$ .

$$\begin{pmatrix} I_{cm,in} \\ I_{dm1,in} \\ I_{dm2,in} \\ I_{cm,out} \\ I_{dm1,out} \\ I_{dm2,out} \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} & \dots & Y_{16} \\ Y_{21} & Y_{22} & \dots & Y_{26} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{61} & Y_{62} & \dots & Y_{66} \end{pmatrix} \begin{pmatrix} V_{cm,in} \\ 0 \\ 0 \\ V_{cm,out} \\ 0 \\ 0 \end{pmatrix} \quad (10.27)$$

Moreover it is valid the following equation (10.28).

$$V_{cm,out} = Z_{motor+cable} I_{cm,out} \quad (10.28)$$

In order to solve the system, it has also to be remembered that the currents in this representation are always entering in the port. The required transmission function  $\frac{I_{cm,out}}{V_{cm,in}}$  is described in (10.29).

$$\frac{I_{cm,out}}{V_{cm,in}} = - \left( \frac{Y_{11} \frac{Z_{cm,out}}{Z_{cm,out} + Z_{cm,in}}}{(1 - Y_{14}) Z_{motor+cable}} + \frac{Y_{41} \frac{Z_{cm,out}}{Z_{cm,out} + Z_{cm,in}}}{(1 - Y_{44}) Z_{motor+cable}} \right) \quad (10.29)$$

This transmission function is the basis to get the interpolated result through a vector fitting operation and the required result is depicted in the following Figure 10.9

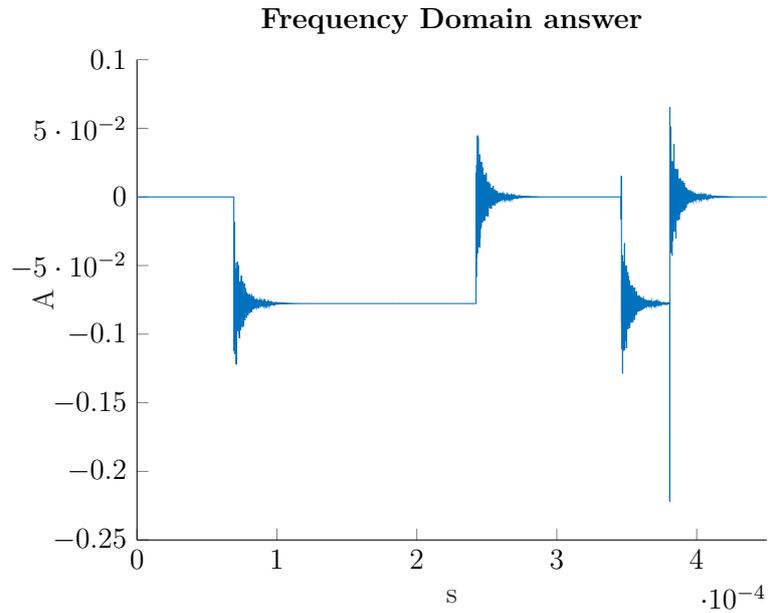


Figure 10.9: Common mode current derived through a vector fitting

The oscillations at lower frequencies in this model are not described since the model description starts from 100 kHz. As shown in Figure 10.10 the behavior at high frequency is similar to the one measured and the peak at 100 MHz is also represented in the same position.

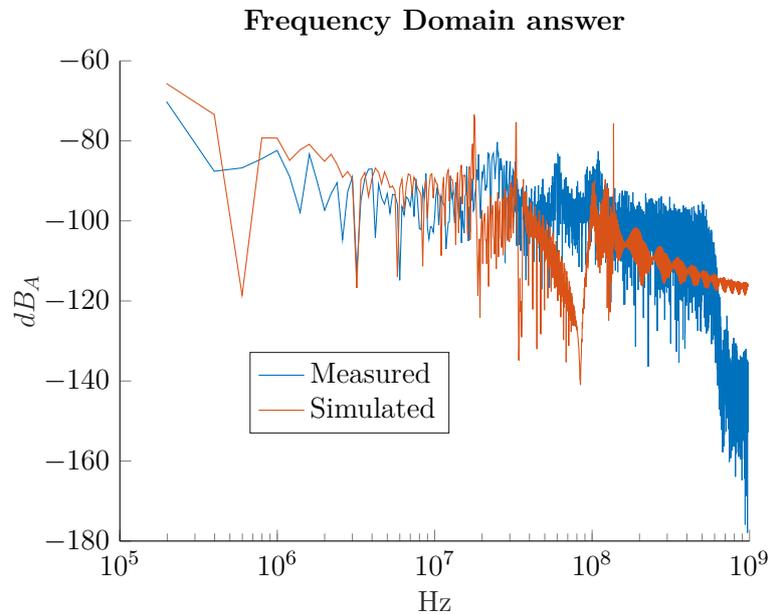


Figure 10.10: Fourier Analysis of the simulated signal and comparison to the real one

### 10.3 Combination of the 2 different transmission function

It is clear from the previous paragraphs that the transmission function depicted in (10.8) provides good results at lower frequencies, while the transmission function depicted in (10.29) provides a better representation at higher frequencies. This difference is due to the different frequencies where the components are measured. The first transmission function is defined by a network analyzer that can measure the impedances from 1 kHz up to 30 MHz, while the second transmission function is described through S-parameters from 100 kHz up to 150 MHz. A function that works sufficiently well at low and at high frequencies requires a combination of the two different functions. The first and easiest solution is obtained by using the first transmission function from 1kHz to 100 kHz and the second function between 30 MHz and 180 MHz. In the frequencies where both functions are valid, the sum of the two different transmission functions with a coefficient of 0.5 is used. The obtained solution is depicted in (10.30)

$$F_{final} = \begin{cases} F_1 & f < 100kHz \\ \frac{F_1+F_2}{2} & 100kHz < f < 30MHz \\ F_2 & f > 30MHz \end{cases} \quad (10.30)$$

The result from the function obtain from (10.30) can be seen in the following Figure 10.11

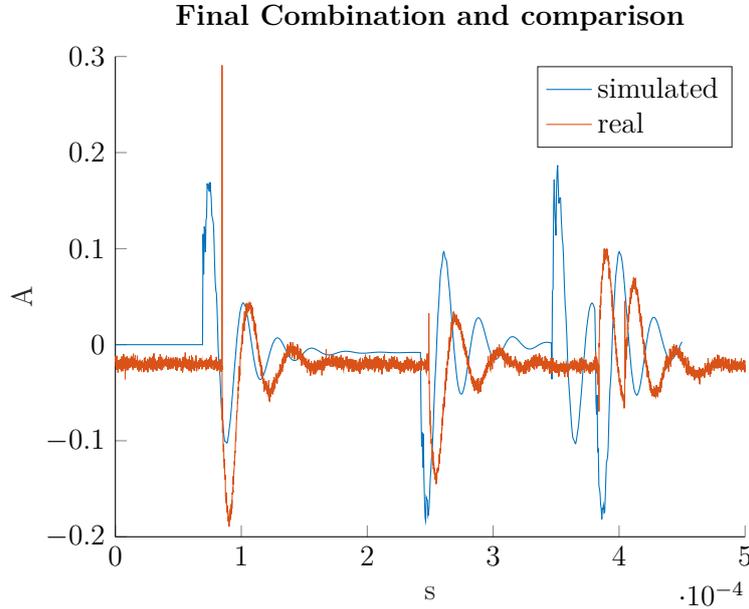


Figure 10.11: Result obtained through the equation 10.30

The analysis in frequency domain is depicted in the following Figure 10.12

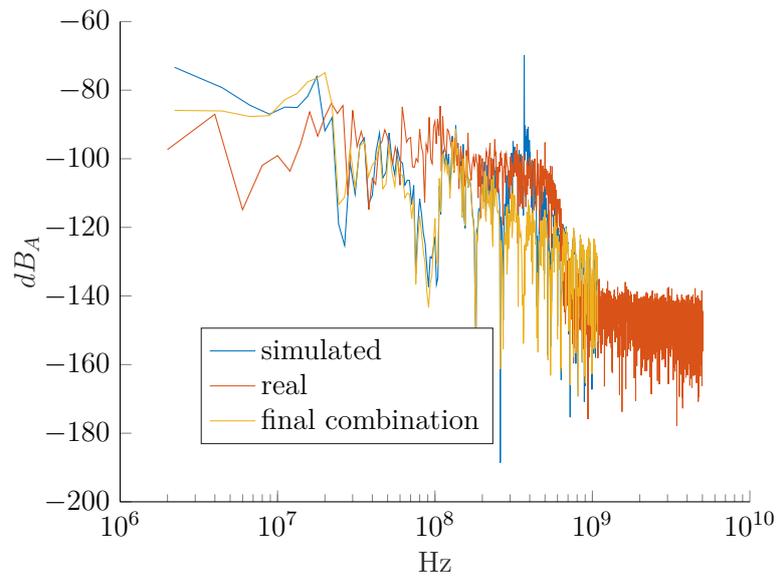


Figure 10.12: Combination analyzed in frequency domain

It can be noticed that with this specific combination it is possible to get a good description of the peaks also up to 100 MHz. The behavior starts to be different above 200 MHz but this is due to the limitation of the bandwidth of the oscilloscopes in the real measurements.

# Chapter 11

## Oscillation Simulations

The analysis is done through CST which provides a FEM simulation of the inverter. The modelization of the inverter is done through a PCB description of the system. The only additions required for the simulation are the parasitic components such as  $C_{ds}$ . This model was employed to evaluate the S-parameters of the converter. With this software, it is possible to evaluate also the transient in the time domain when different signals are applied. In particular, as explained previously 6 different signals have been applied. For the high side MOSFET of the first leg, the voltage applied is depicted in Figure 11.1. The low side of the first leg has the  $V_{ds}$  equal to the  $V_{DC}$  when the high side has the voltage equal to 0 and vice-versa. The other two legs have the high side always with a  $V_{ds}$  equal to  $V_{DC}$  and the low side with a voltage always equal to 0. In this way, the switching process associated with the first vector is simulated.

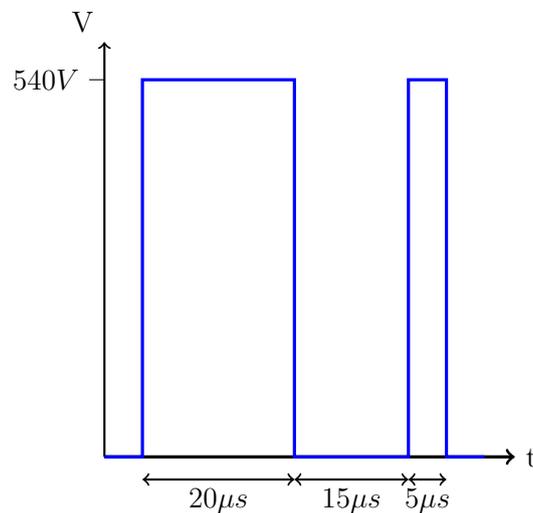


Figure 11.1: Voltage applied to the Mosfet which is switched during the double pulse test

The input of the inverter is an open circuit. The transient during the double pulse test is therefore measured at this output. The test is repeated later by adding a capacitance of

1nF in parallel to every device, which means in the same configuration depicted in Figure 9.1 and the simulation is repeated.

The results obtained through this simulation are depicted in the following Figure 11.2

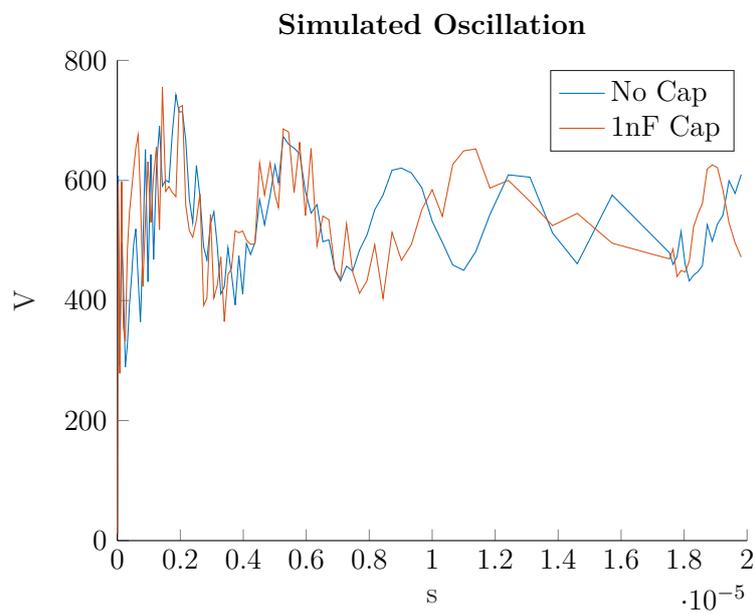


Figure 11.2: Oscillation of the DC Link with the addition of the 1nF capacitance simulated through CST

The simulation provides almost no difference with respect to the case without capacitance.

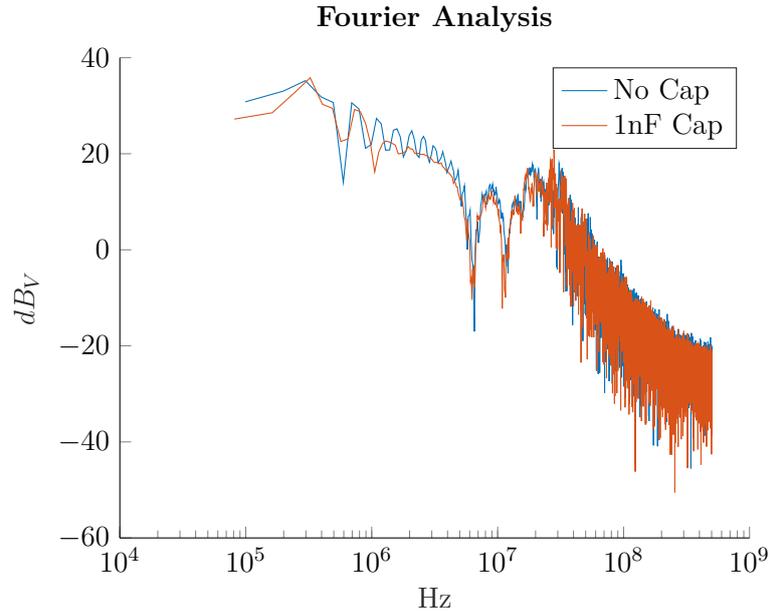


Figure 11.3: Oscillation of the DC Link in the frequency with the addition of the 1nF capacitance simulated through CST

Figure 11.3 shows that this first simulation doesn't provide any relevant result. The problem with the previous simulation is linked to the modelization of the capacitance. In fact, the capacitance of each transistor is not constant as it is supposed in the simulation but it is dependent on the voltage as it can be seen from the datasheet of the device.

In order to get a better result, a Spice model for the MOSFET and the diodes is therefore obtained from the company which produces the components used in the inverter. This Spice models are linked in parallel to the drain and source terminals of the real component in order to simulate the real parasitic capacitance of the device. In this case, the simulation of the double pulse test is performed by switching on and off the parasitic device. The shape of the applied voltage is similar to the signal depicted in Figure 11.1 for the high side MOSFET but the voltage is lower since it is used just to turn on the MOSFET in parallel to the inverter. The input of the inverter has a  $V_{DC} = 540V$  applied. In this way, the effective value of the capacitance during the double pulse test can be simulated. The obtained result is described in the following Figure 11.4. It can clearly be seen that the oscillations in the case of the extra capacitances (the blue curve in Figure 11.4) have a lower frequency with respect to the oscillations without the capacitances.

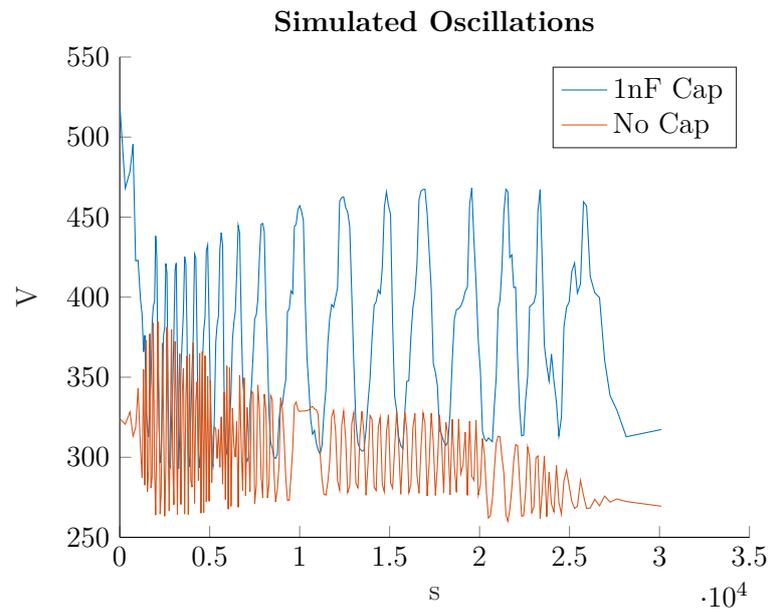


Figure 11.4: Oscillation of the DC Link with the addition of the 1nF capacitance simulated through CST and the extra Spice Models

At the same time, it can be also noticed from the Fourier analysis of the previous simulation, that the shape is relevantly different from the measured oscillations. Moreover, it is also clear that the decrease of the oscillation's frequency is not as important as expected (Figure 11.5).

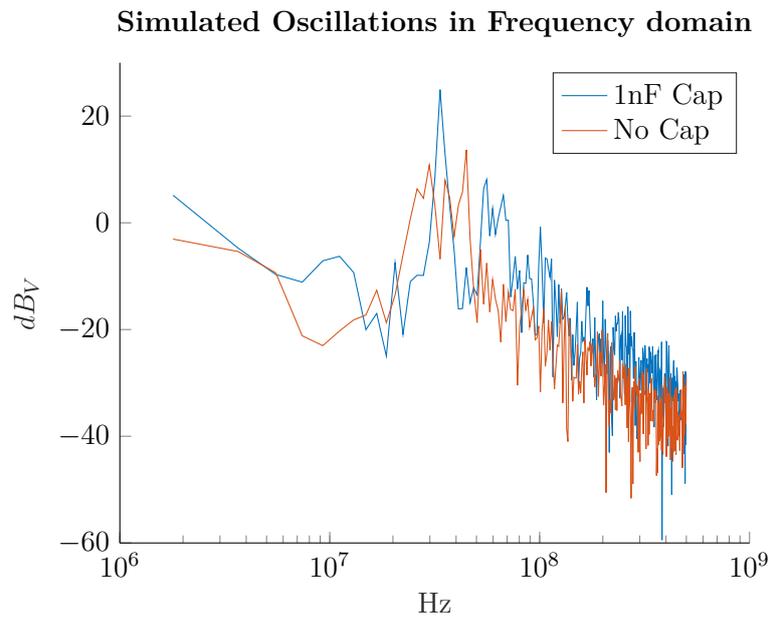


Figure 11.5: Frequency analysis of the oscillation of the DC Link with the addition of the 1nF capacitance simulated through CST and the extra Spice Models

**Part V**

**Final Conclusion**

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The work, which has been described in the previous chapters, had the main purpose to investigate the application of the model depicted in [4]. It was necessary to evaluate if the description of the system through scattering parameters can provide also a good analysis in the time domain. This analysis has required to evaluate the switching behavior of the system. For this purpose, a specific double pulse test on the inverter in the layout of a real application has been implemented. Secondly, it has been evaluated if it is possible to simulate the effect of the parasitic capacitances of the switches during the transient with a low computational cost.

The results of the double pulse test allow evaluating the parameters of the switching characteristics which play a role in the common-mode current. In particular, it has been observed that the drain current has no effect on the common-mode current behavior. Equally it has been discovered that the state of the other two legs is also not relevant and doesn't affect the common-mode current. The special test with the two 0 vectors (Chapter 5) has shown the saturation of the common-mode choke. The saturation can't be foreseen through the measurements of the scattering parameters or the measurements of the impedances. Through the double pulse test, it is, nevertheless, possible to evaluate the condition when the saturation happens. This special double pulse test has allowed showing that there is no effect of the common-mode on the DC link as it was expected from the theory. The two zero states provide exclusively common-mode excitation. The double pulse test has provided also the result of further confirmation of the behavior of the MOSFET during the switching process. It can be seen from the measurements of the  $V_{ds}$  with a positive current that the rise time is dependent on the value of the current, while the fall time is dependent on the reverse recovery time. In the case of a negative current, the rise time is limited by the diode and it is constant, while the fall time is dependent on the current that flows into the device.

Once the analysis of the measurements of the double pulse test was finished, the measured rise and the fall time have been used to define the real common-mode voltage associated with the double pulse test. This input voltage has been used later as the input of the obtained transmission function. Two different representations have been used, in order to get the transmission function as it was explained in Chapter 10. The first representation offers a description of the impedances of all the system's components from 1 kHz up to 30 MHz. From this description, it has been possible to write a 2-port network for every basic component. Through the concatenation of 2-port networks, it has been possible to obtain a transmission function, which is a vector of values in the frequency domain. From this set of values in the frequency domain, it is possible to extrapolate a transmission function in the time domain which is a sum of exponentials. Once this function is obtained, it is possible to get the answer in the time domain. The solution obtained through this process provides a good approximation to evaluate the low-frequency oscillations of the common-mode current. At the same time, this model shows some problems to represent the high-frequency oscillations. This lack of precision in high frequency can also be seen in the Fourier transform of the simulated common-mode current. The 6-port model that has been implemented in [4] has been used to overcome those limitations. This model is described from 100kHz up to 180 MHz through the measurements of the scattering parameters for each basic block of the system. The process to obtain a transmission function is similar, but some mathematical manipulations are required. In the analysis, the voltages of the block are supposed to be 0 which means that all the port of the 6-port model are

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supposed to be short-circuited apart the port associated to the common mode. The transmission function obtained through this mathematical model provides good results in high frequency since in the time domain the high-frequency oscillations of the common-mode current are simulated but it doesn't seem able to foresee also the low-frequency oscillations. Moreover, it isn't possible to evaluate the effect of the differential mode on the common-mode current since the differential mode input voltage is set for the calculation to 0. In order to get the common-mode current in the time domain, it is therefore used a linear combination of the two results. This solution allows obtaining a good result in the time domain and secondly allows also to foresee the peaks of the Fourier transform of the common-mode current in the right position also at very high frequencies.

The double pulse test has been performed also by slightly varying the inverter. In fact, a double pulse test has been performed with and without an extra parasitic capacitance of  $1nF$  in parallel to every switch. These measurements have been carried out to evaluate if the oscillation of the DC link during the double pulse test is affected by the parasitic capacitance of the switch. The double pulse test has shown that the oscillation decreases its frequency when the capacitance is added.

The next step has been to investigate if it is possible to estimate the shift from an analysis of the parameters of the inverter. The inverter had already been described through a PCB model. From this model, the analysis to simulate the oscillation at the DC link has been carried out. Two different tries have been carried out. The first try has been made by considering the capacitance  $C_{ds}$  independent from voltage and then evaluating under this assumption the oscillation at the DC link with and without the extra capacitance through a FEM simulation. This first solution provides very fast simulation but the result has been far from the measured behavior. The second try has been carried out by adding instead of an independent capacitance a Spice model of the switch in parallel to the actual switch. In this way, it has been possible to simulate the actual behavior of the parasitic capacitance of the device concerning the voltage. This solution has the disadvantage that the time required for the simulation is considerably longer. On the other hand, this model provides a better solution since the displacement of the frequency of oscillation can be seen through the Fourier analysis.

The next step to continue this analysis could be the implementation of the other components of the system. The analysis of the common-mode current instead could be deepened by adding also the influence of the differential mode on the transmission function. In this case, the input ports associated with the differential mode shouldn't be short-circuited. It would be nevertheless necessary to evaluate firstly what kind of effect is due to the differential mode in the time domain of the common-mode current.

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