Master Thesis

Design of a Low Cost Single Gate Planar Junctionless Transistor over FD-SOI Wafer

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Abstract

Owing to the simple and cost-effective fabrication process and enhanced performance with respect to conventional MOSFETs, junctionless transistors are becoming a significant topic of research. In fact they are characterized by the absence of any pn junctions in their physical structure, thus avoiding one of the most expensive and difficult step in transistor fabrication, that is the implantation of source and drain contacts. After the fabrication of the first junctionless transistors (nanowire) in 2010, many others were proposed such as junctionless FinFETs, GAAFETs, double gate, and planar. The critical point is that these devices, even if easier to fabricate with respect to conventional transistors, are anyway very expensive, thus restricting the possibility to realize prototypes in research and industrial field. For this reason a low cost planar junctionless transistor is proposed. First the design of its structure is carried out, by sizing and deciding its physical components on the basis of parametric computations and analytical models; the designed transistor has a channel length of 500nm, a device layer thickness of 600nm, a low doping concentration ($1e15cm^{-3}$), and is characterized by an operating range of 1V. The metallization material is aluminum. Next a low cost fabrication process that does not require any implantation step is proposed and discussed in detail, considering also source of non-idealities. Then the simulations results obtained through COMSOL Multiphysics are reported, confirming the expected principle of operation of the designed transistor. At the end two papers written for this master thesis are attached. The first one is a paper review that provides a classification and critical analysis in terms of performance engineering of the various junctionless transistors. It was decided to write such state of the art because most of the reviews about junctionless transistors were written in 2010-2013, thus not containing the last developments. The second one is a journal article in which a method for the extraction from CAD software of one of the most important parameters in junctionless transistors, that is the depletion width extension, is proposed. The algorithm fit the analytical model, and allows to quantitatively distinguish the carrier concentration at the depletion region boundary.

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Finally, I would like to express my gratitude to my parents for providing me with unfailing support and continuous encouragement throughout my years of study.

Arian Nowbahari

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Chapter 1

Introduction

The concept of junctionless transistor (JLT) was introduced by J.E. Lilienfeld in 1925 [1]. The main characteristic of the Lilienfeld device was the absence of any pn junction in the physical structure of the transistor. By controlling the voltage at the gate terminal of this semiconductor device, Lilienfeld was able to deplete the carriers in a localized region of the substrate. In this manner, it was possible to control the resistivity of the device and therefore the electrical current through the transistor. But the technology of that time did not allow him to realize a working device [2], which required the fabrication of a nanometric substrate layer. Only in 2010 at the Tyndall National Institute, the first junctionless transistor [2] was successfully manufactured; J.P. Colinge et al. fabricated a $10nm$ thick and $1\mu m$ long highly doped ($10^{19}cm^{-3}$) junctionless nanowire transistor. The device represents the first one of a new generation of transistors. In fact after its realization, many others were proposed such as: FinFETs, Gate-All-AroundFETs (GAAFETs), planar (PJLT), double gate (DGJLT), thin-filmFETs (TFT), and tunnelFETs (TFET). The advantages of a junction-free structure are numerous such as the absence of doping concentration gradients [3], which are difficult to precisely control in the nanometric regime, the absence of junction leakages, simple fabrication process and lower fabrication cost (since no implantation for source and drain are required) [4]. In addition, these transistors can provide greater performance with respect to conventional transistors, such as reduced short-channel effects (effective channel length not reduced by pn junctions) [5] and less degradation of carrier mobility (current flows in the bulk of the substrate) [6]. For all these reasons it was decided to propose a design and fabrication of a low cost junctionless transistor. From a fabrication process point of view, the simplest junctionless transistor is the planar one, which is usually realized through FDSOI (fully depleted silicon on insulator) technology. The critical problem is that the clean room available in the facility is a MEMS one. Therefore this project aims to provide a simple fabrication process, compatible with the available machines in the laboratory, that could lower the fabrication cost of the device. The project is carried out by two master students: one has to find a low cost fabrication method for the realization of SOI wafers, while the other one has to design and simulate the transistor. This thesis, which has as target the design and simulation of the transistor, it structured in two parts: the first one (Sect.3) treats the design of the planar single gate junctionless transistor on the basis of the project specifications and it is divided as it follows:

- design of the device layer thickness on the basis of the doping concentration;

- design of the source and drain contacts, in terms of material and geometry, on the basis of a parasitic resistance model;
- design of the metal gate, by considering influence of the physical parameters on the main electrical quantities;
- step by step fabrication process;
- masks.

The second part (Sect.4), treats the simulation of the device, which is carried out by means of COMSOL Multiphysics, with the aim of:

- verify the designed junctionless transistor in terms of qualitative operation;
- extract the important electrical quantities (e.g. threshold voltage) and compare them to the analytical values.

Besides the design and the simulation of the junctionless transistor, two papers for this thesis were written:

1. *Analysis and Classification of Junctionless Transistors: a Paper Review*;
2. *A Numerical Method to Extract the Depletion Region Width of Planar Junctionless Transistors.*

The first paper is a state of the art of junctionless transistors. The motivation to write a state of the art relies on the fact that most of the paper reviews about this topic were published in 2010-2013, thus not considering the latest developments. The paper (which is in Appendix B.1) analyzes a total of 118 papers in order to provide a complete overview of the main involved figure of merits. The transistors are classified as it follows:

- Nanowire;
- FinFET;
- Gate-All-Around;
- Planar;
- Thin-Film;
- Double Gate;
- TunnelFET.

And the paper distribution is the one depicted in Fig.1.1.

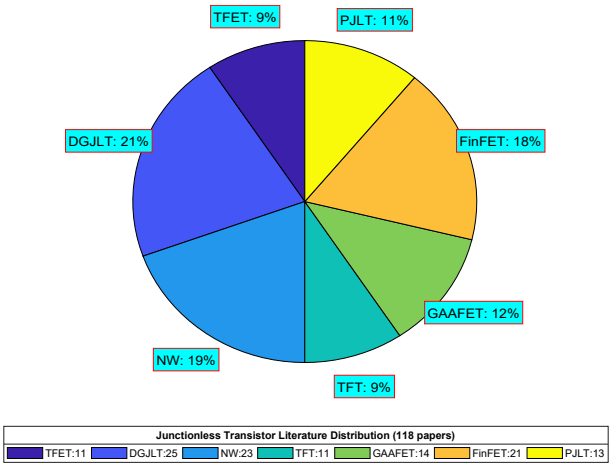

Figure 1.1: Junctionless transistors literature distribution.

The graphical representation of the analyzed literature is shown in Fig.1.2 in the next page. The second paper (Appendix B.2) instead was written in order to provide a method to extract the depletion width from CAD software. The motivation to write it relied on the fact that during the simulations it was not possible to precisely define the boundary between the depleted and undepleted part, thus not allowing a qualitative interpretation of the simulations results. By the implementation of the method was possible to verify the limits of the analytical depletion width model. Moreover the application of the algorithm to different structures demonstrated that the carrier concentration at the boundary of the depletion width is approximately half the doping concentration.

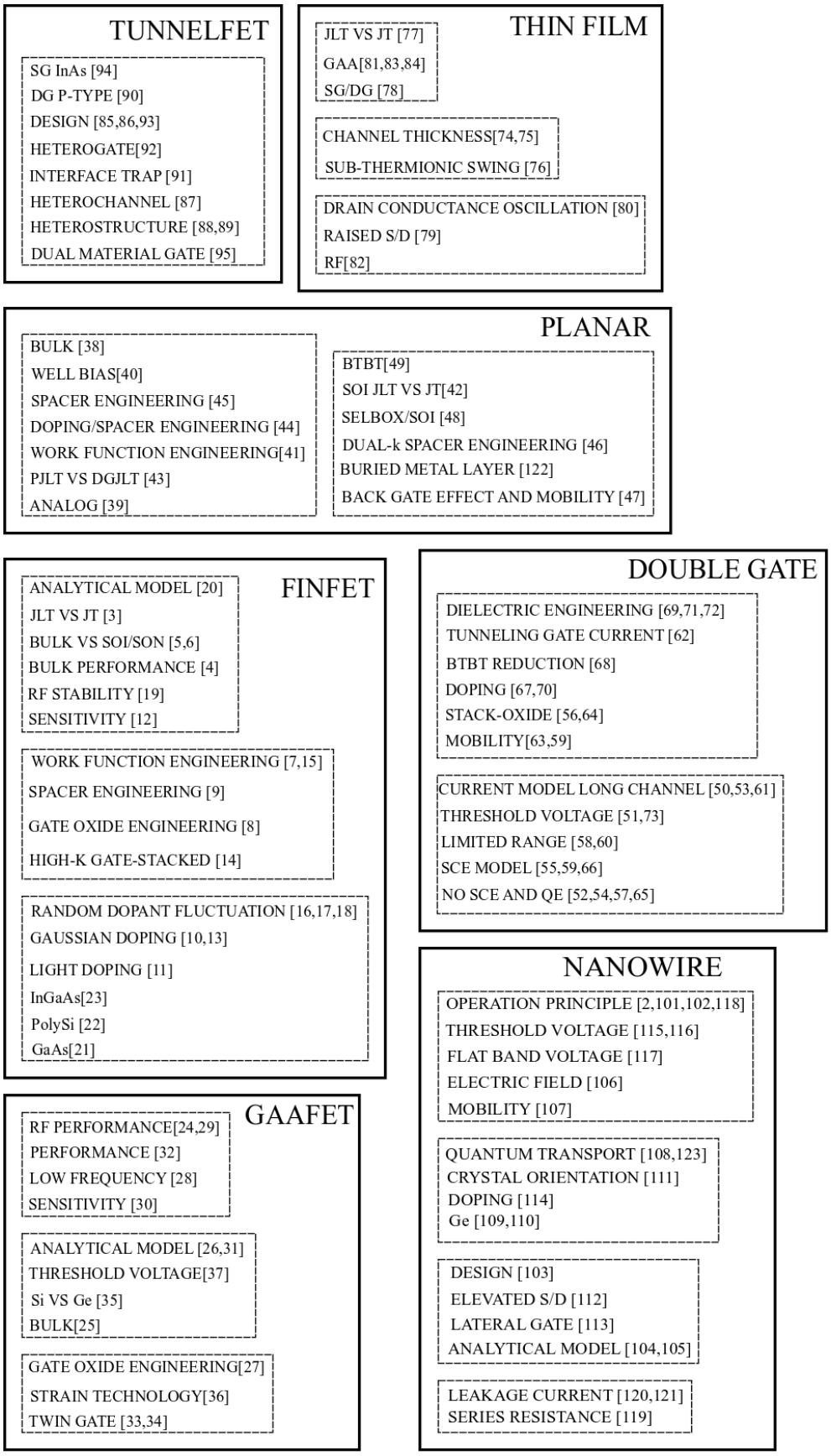

Figure 1.2: Graphical representation of the distribution of the analyzed literature in the attached paper (Appendix B.1).

Chapter 2

Proposed Device

2.1 Structure

The proposed device is a planar single gate junctionless transistor over FD-SOI (fully depleted silicon on insulator [7]), depicted in Fig.2.1(a). The main difference with respect to conventional MOSFETs is the absence of any pn junction in the device layer. A planar junctionless transistor (PJLT) realized on FD-SOI is characterized by three layers: a handle substrate (silicon), an insulating layer (BOX, that is buried oxide), and a thin device layer (silicon).

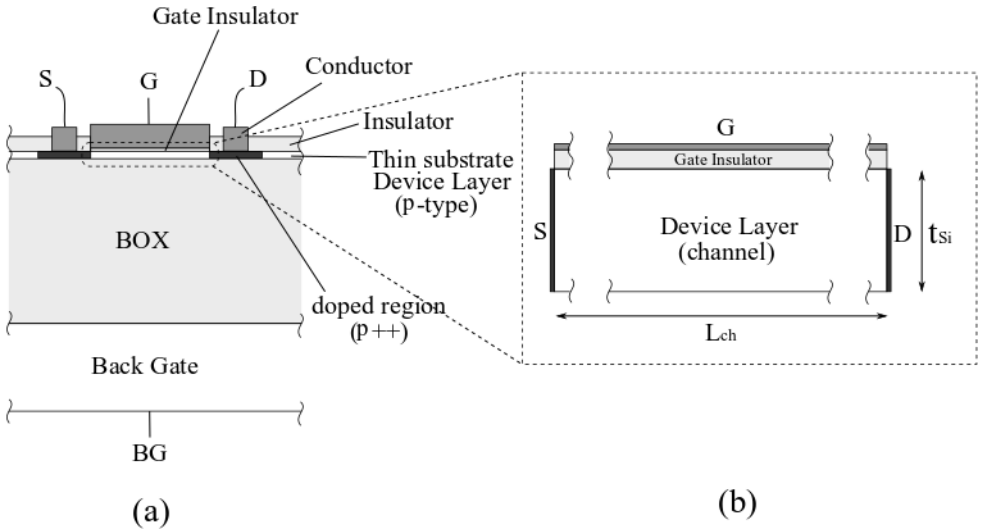

Figure 2.1: P-type PJLT Physical Structure. (a) Complete Structure on FDSOI wafer. (b) Simplified Structure.

As explained in the attached papers (Appendix B), the device layer is typically thin and highly doped in order to allow a correct device operation. The handle substrate does not require to be doped unless the designer decides to use it as second gate terminal or back gate; since the proposed device is a planar single gate junctionless transistor (PJLT), the simplified structure in Fig.2.1(b) is considered. The device layer of a PJLT can be uniformly doped if it is highly doped ($> 1e19cm^{-3}$) and has a thickness about $10nm$ [8]: in fact, if the doping concentration is very high and the film is very thin, the parasitic resistance associated to the regions below the source and drain contacts is very low. But such thickness is not usually easy to achieve,

since most of the SOI wafers available on the market have a thickness in the range of micrometers. Therefore a possible solution consists into realizing highly doped drain and source wells in order to minimize the parasitic resistances between the channel of the transistor (conductive part of the device layer between the wells) and the source and drain metallizations. In particular, if the device layer is n-doped, then the source and drain wells must be heavily doped with donors (n++). On the other hand, if the device layer is p-doped, then the source and the drain wells must be heavily doped with acceptors (p++). These wells are represented with black regions in Fig.2.1(a).

2.2 Operation

A junctionless transistor works differently with respect to inversion mode devices [3]. The principle of operation, which is verified in Sect.4, can be qualitatively described as in Fig.2.2: when the gate voltage is lower than the threshold one, the device layer is fully depleted (Fig.2.2(a)). As the gate voltage is increased to more positive values, electrons are attracted towards the oxide/semiconductor interface, and the depletion region width is reduced, thus a path between the source and the drain below the depletion region is created, and a bulk current is formed (Fig.2.2(b)). If the gate voltage is then increased over the flat band voltage, many electrons are attracted to the semiconductor/oxide interface, thus forming an accumulation layer at the surface (Fig.2.2(c)).

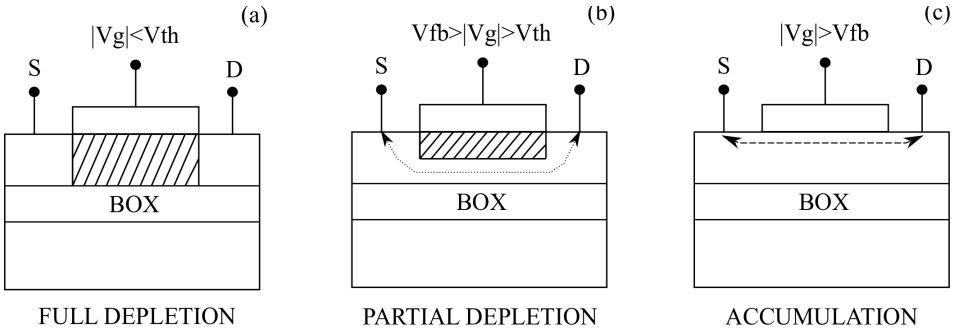

Figure 2.2: PJLT principle of operation. (a) Full depletion: no conduction. (b) Partial depletion: bulk conduction. (c) Accumulation: surface conduction.

As a consequence the positions of the threshold and flat band voltage is very different for inversion mode, accumulation mode, and junctionless transistors (Fig.2.3(a3)).

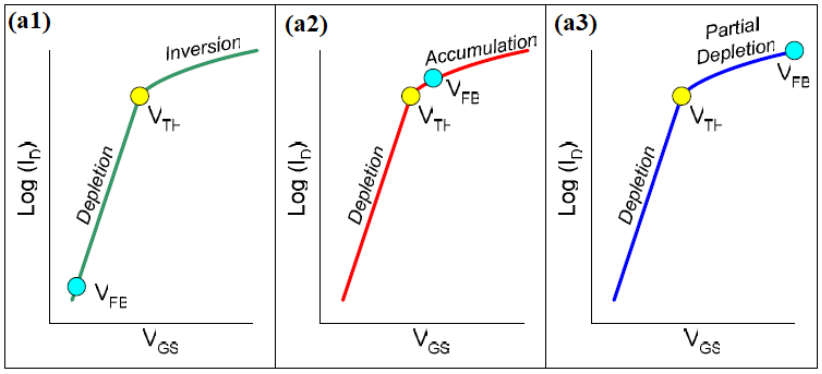

Figure 2.3: Current behavior comparison. (a1) Inversion mode device. (12) Accumulation mode device. (a3) Junctionless transistor [9].

For junctionless transistors the threshold voltage is defined as the gate voltage that fully depletes (OFF state) the device layer (Fig. 2.3(a1)). Thus they are more similar to accumulation mode devices (Fig.2.3(a2)) in terms of threshold voltage definition. Regarding the current, two components can be distinguished: a bulk and an accumulation current. When the gate voltage is greater than the threshold one, partial depletion takes place creating a path in the substrate for the bulk current. As the gate voltage overcomes the flat band, an accumulation layer is formed at the oxide/semiconductor interface (ON state).

2.3 Specifications

The design specifications are the following ones:

- single gate planar junctionless transistor;
- fabrication process compatible with the MEMS clean room;
- photolithographic resolution of maskless machine of $350nm$;
- photolithographic resolution of the mask aligner $2\mu m$;
- mask alignment of $100nm$ (nominal value).

The PJLTs to be designed are going to be fabricated in a MEMS clean room; this implies constraints on the available machines and resolution. For instance no CVD reactors are present, and the only system available for the deposition of materials is a sputtering system. Regarding the photolithography, two machines are present: a mask aligner mainly used for MEMS devices with a resolution of $2\mu m$, and a maskless machine with a resolution of $350nm$. The latter works on the basis of a serial process which is very slow as compared to the MEMS mask aligner. The idea is therefore to use the maskless machine for the critical dimensions, and the mask aligner for the large ones. Regarding the mask alignment, a nominal value of $100nm$ is provided. Concerning the available wafers, the ones with characteristics in Tab.2.1 are present, and their resistivity is provided in a range ([5-10] Ωcm).

Table 2.1: Wafers characteristics.

Parameter	**Value**
Number	3
Type	BSOI
Dopant	p-Boron
Resistivity	[5-10] Ωcm
Diameter	$100mm$
Device Layer Thickness	$20\mu m$
BOX thickness	$0.5\mu m$
Handle Thickness	$380\mu m$

Chapter 3

Design

In this section the proposed design is reported: first the needed device layer thickness is decided, on the basis of the estimated doping concentration; then a parasitic resistance model is analyzed for sizing the geometrical parameters of the device, and finally the fabrication process, together with the masks, is provided.

3.1 Device Layer Thickness

3.1.1 Maximum Depletion Width

In order to ensure fully depleted SOI technology, i.e. to guarantee that the device layer can be entirely depleted and thus the transistor correctly switched off, it is necessary that [10]:

$$X_{dep} = \sqrt{\frac{4\epsilon_{Si}\Phi_{n,p}}{qN_{D,A}}} > T_{Si} \tag{3.1}$$

where:

- $q = 1.602 \times 10^{19}$ (C) is the elementary electric charge;
- $\epsilon_{Si} = 11.7\epsilon_0$ (F/cm) is the dielectric constant of the device layer;
- $\epsilon_0 = 8.854 \times 10^{-14}$ (F/cm) is the vacuum permittivity;
- $N_{D,A}$ $(atoms/cm^3)$ is the device layer donor/acceptor concentration;
- $q\Phi_{n,p} = k_B T\, ln(N_{d,a}/n_i)$ (eV) is the n-type/p-type Fermi potential;
- $k_B = 8.6173303 \times 10^{-5}$ (eV/K) is the Boltzmann constant;
- $T = 293.15$ (K) is the temperature;
- $n_i = 5.29 \times 10^{19}(T/300)^{2.54}e^{-6726/T}$ $(atoms/cm^3)$ is the intrinsic carrier concentration [11].

That is, the maximum depletion width has to be larger than the silicon device layer thickness T_{Si} to ensure the device full depletion. Thus the maximum depletion width (X_{dep}) as a function of the doping concentration (Eq.3.1) was implemented in MATLAB [12] (Appendix A.1), and the plot in Fig.3.1 was obtained.

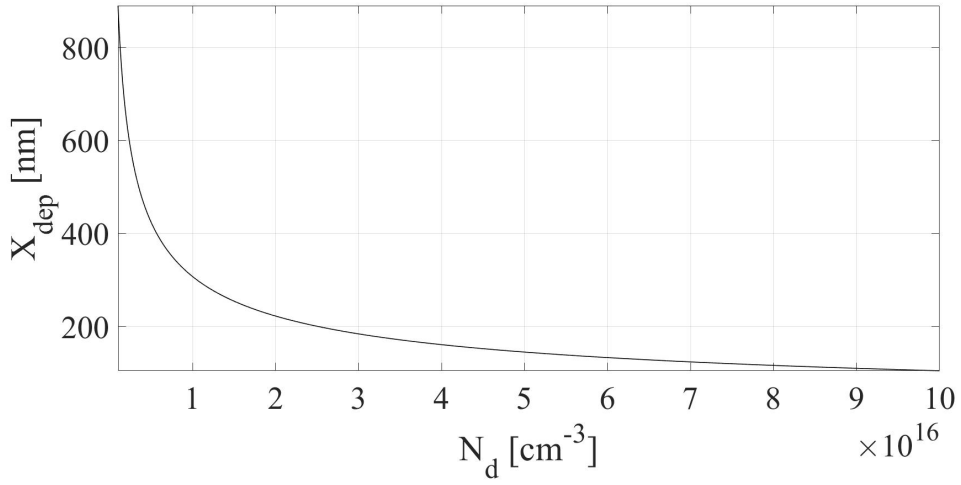

Figure 3.1: Maximum Depletion width as a function of the doping concentration.

As can be observed in Fig.3.1, the maximum depletion width decreases with increasing doping. Considering a wafer with a doping concentration of $5 \times 10^{15} cm^{-3}$, the corresponding maximum depletion width is $432.7nm$; therefore in order to ensure full depletion a $T_{Si} < 432.7nm$ has to be obtained (e.g. $400nm$). Clearly for that doping concentration ($5 \times 10^{15} cm^{-3}$) also a value of $10nm$ would guarantee full depletion, but such thin film is more difficult to obtain from a fabrication process point of view. In order to correctly design the silicon device layer thickness, the doping concentrations of the wafers available for the fabrication process have to be estimated.

3.1.2 Doping Concentration Estimation

Since the resistivity instead of the doping concentration is provided in Tab.2.1, it was decided to implement an iterative algorithm (Fig.3.2) in MATLAB (Appendix A.2) that on the basis of the provided resistivity can estimate the doping concentration [13]. The algorithm consists of the following steps:

1. Define a mobility value μ.
2. Compute the associated doping concentration with the given resistivity by means of: $N_A = \frac{1}{q\rho\mu}$.
3. Compute $\mu' = \frac{\mu_{max} - \mu_{min}}{1 + (N/N_{ref})^{\alpha}}$.
4. Compute $\mu' - \mu$, and verifiy if the difference is below a certain tolerance. If it is not, define $\mu = \mu'$ and repeat the algorithm until the tolerance is not satisfied.

Regarding the parameters, they were chosen according to [13]:

- Initial guess: 450 cm/Vs.
- Maximum hole mobility: $\mu_{max} = 495$ cm/Vs.
- Minimum hole mobility: $\mu_{min} = 47.7$ cm/Vs.

- Reference concentration: $N_{ref} = 6.3 \times 10^{16}\ cm^{-3}$.
- Fitting parameter: $\alpha = 0.76$.
- Tolerance: $tol = 0.1\ cm/Vs$.

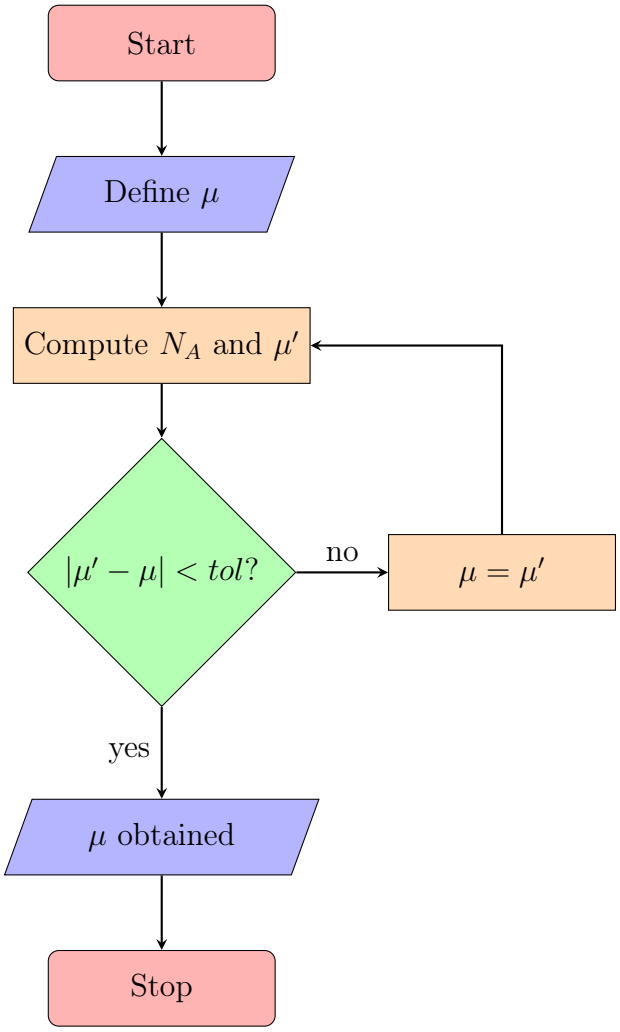

Figure 3.2: Flow chart of the algorithm implemented in MATLAB for the mobility estimation.

The considered resistivity is $5\Omega cm$, since it represents the worst case analysis: lower the resistivity, higher the doping concentration, and smaller the needed device layer thickness (which is more difficult to obtain from a fabrication point of view). The estimated doping concentration by means of the algorithm is $2.73 \times 10^{15} cm^{-3}$, while the hole mobility is $472 cm^2/(Vs)$. The associated maximum depletion width is $560nm$. Another possible tool is to use the graph in Fig.3.3; the value obtained with the algorithm is coherent with the graph.
Since the device layer thickness is of critical importance for ensuring the correct operation of the transistor, it was decided to measure, with the four probe method, the *real* wafer resistivity and then to apply again the algorithm.

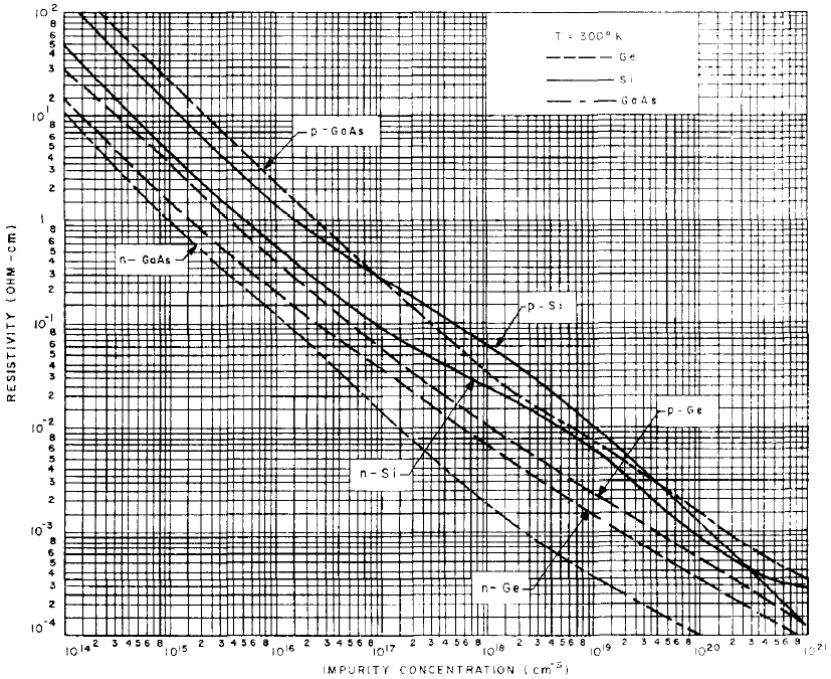

Figure 3.3: Graph of the resistivity versus impurity concentration at $300K$ [14].

3.1.3 Resistivity Measurement

The wafer resistivity can be computed with a four probe collinear measurement [15], and the basic setup is shown in Fig.3.4. A current is applied to two probes, and the voltage between the other two probes is measured. Then the wafer resistance is computed as V/I.

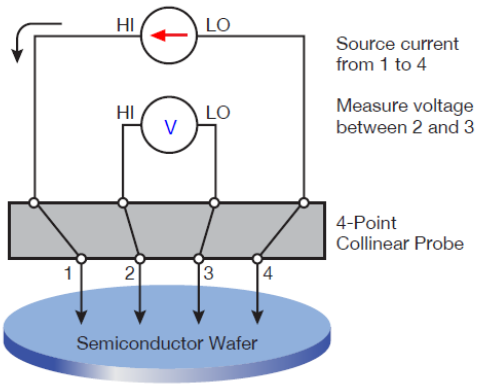

Figure 3.4: Schematic of a collinear four probe measurement setup [16].

Once the resistance is computed, the resistivity can be expressed as [15]:

$$\rho = 2\pi s F \frac{V}{I} \tag{3.2}$$

where:

- $s = 1mm$ is the spacing between two adjacent probes;

- V is the voltage measured between two probes;
- $I = 1mA$ is the current applied to the other two probes;
- $F = F_1F_2F_3$ is the correction factor;
- $F_1 = \frac{t/s}{2ln\{[sinh(t/s)]/[sinh(t/2s)]\}} = 0.0144$ is the correction factor for non-conducting bottom surface;
- $t = 20\mu m$ is the wafer thickness;
- $F_2 = \frac{ln(2)}{ln(2)+ln\{[(D/s)^2+3]/[(D/s)^2-3]\}} = 0.9991$ is a geometrical correction factor;
- $D = 100mm$ is the wafer diameter;
- F_3 is a boundary proximity correction factor that can be neglected [15] since the measurement is taken in the middle of wafer and the ratio of the distance between the boundary and the probes is large.

The measurements on the three wafers were carried out (measuring the voltage approximately every $60s$) by means of a probe station PWS (Pacific Western System Inc) Probe II (Fig.3.5), a Keithley signal generator (for the application of constant current $I = 1mA$), and a Keithley multimeter (for the voltage measurement). The results are reported in Tab.3.1.

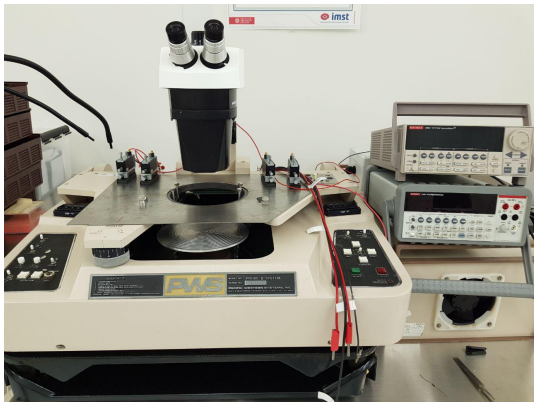

Figure 3.5: Probe station used for the resistance measurement in the clean room.

As can be observed in Tab.3.1, the resistance gradually increases with time. This can be attributed to the fact that the applied current raises the wafer temperature, thus increasing its resistivity.

Table 3.1: Wafers resistances measurement data.

Wafer	**Test 1**	**Test 2**	**Test 3**
L	450Ω	500Ω	520Ω
C	450Ω	550Ω	650Ω
R	550Ω	650Ω	700Ω

In order to compute the resistivity through Eq.3.2, a MATALB code (Appendix A.3) was developed. The computed resistivities, together with the associated doping

concentrations computed with the algorithm in Fig.3.2 and the resulting maximum depletion widths are reported in Tab.3.2.

Table 3.2: Computed wafers resistivities, doping concentrations, and maximum depletion widths.

Wafer	$\boldsymbol{\rho}$	$\mathbf{N_a}$	$\mathbf{max\ X_{dep}}$
L	$4.44\Omega cm$	$3.08 \times 10^{15} cm^{-3}$	$530nm$
C	$4.98\Omega cm$	$2.73 \times 10^{15} cm^{-3}$	$560nm$
R	$5.74\Omega cm$	$2.35 \times 10^{15} cm^{-3}$	$600nm$

Therefore the device layer thickness has to be lower of the three reported values in order to ensure full depletion; for instance the maximum depletion width of the wafer L is $530nm$. This means that a value smaller of $530nm$ has to be used to guarantee full depletion (e.g. $500nm$). Clearly also a value of $10nm$ would guarantee full depletion, but such thickness is more difficult to obtain from a fabrication process point of view.

3.2 Source and Drain

Now that a characterization of the doping concentration level in the three wafers is provided, it is possible to start the design of the source and drain contacts, which implies decisions on the use of the material as well as on the geometrical parameters of the transistors (width and extensions).

3.2.1 Material Selection

When realizing a source/drain contact a metal-semiconductor junction is formed [17], and one of the most important parameter is the Schottky-barrier height, that is defined as:

$$\Phi_{bn} = \Phi_M - \chi \tag{3.3}$$

$$\Phi_{bp} = E_g - (\Phi_M - \chi) \tag{3.4}$$

for n-type and p-type semiconductor respectively, where Φ_M is the metal work function, χ is the silicon electron affinity, and E_g the energy band gap. Other important quantities are the semiconductor work functions defined as:

$$\Phi_{s,n} = \chi + \frac{Eg}{2q} - \Phi_n \tag{3.5}$$

$$\Phi_{s,p} = \chi + \frac{Eg}{2q} + \Phi_p \tag{3.6}$$

for n-type and p-type semiconductor respectively. They are of critical importance since on the basis of their value with respect to the metal work function the following cases can be distinguished:

- Schottky-diode contact on n-type semiconductor ($\Phi_m > \Phi_{s,n}$);
- Schottky-diode contact on p-type semiconductor ($\Phi_m < \Phi_{s,p}$);
- Ohmic contact on n-type semiconductor ($\Phi_m < \Phi_{s,n}$);
- Ohmic contact on p-type semiconductor ($\Phi_m > \Phi_{s,p}$).

An example of energy band diagrams of a metal-semiconductor (p-type) junction with $q\Phi_m < q\Phi_{s,p}$ is depicted in Fig.3.6. As a forward bias is applied (Fig.3.6(c)) the barrier height reduces, and a hole current from the semiconductor to the metal dominates. By reverse biasing the junction (Fig.3.6(d)), the barrier height increases and a very low current due to thermionic emission from the metal to the semiconductor flows [18]. Therefore the junction is rectifying.

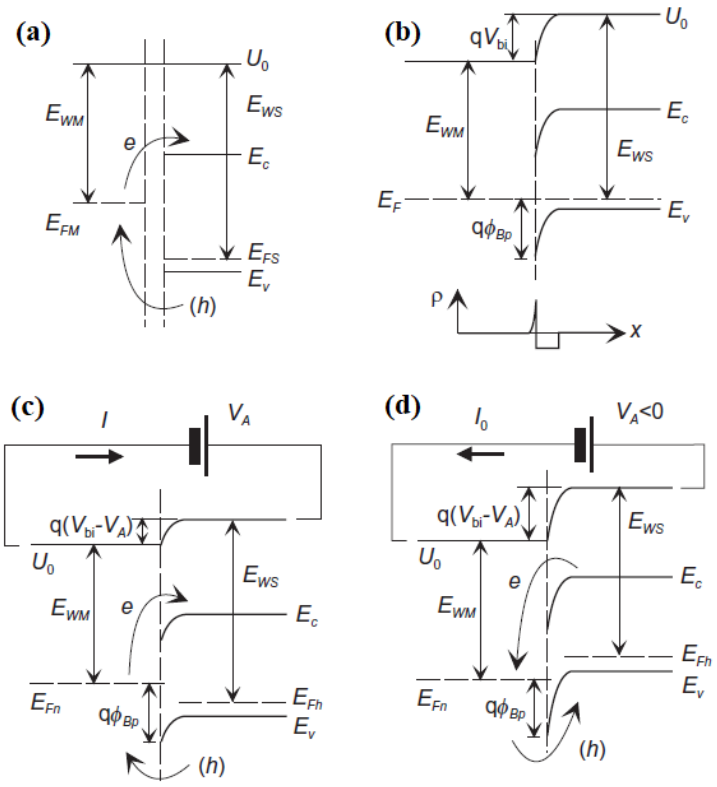

Figure 3.6: Energy band diagrams of a metal-semiconductor (p-type) junction with $q\Phi_m < q\Phi_{s,p}$. (a) Before contact. (b) In equilibrium. (c) Forward bias. (d) Reverse bias [19].

Clearly for the source/drain metallization a non-rectifying (ohmic) contact it is needed. In order to understand the contact behavior as a function of the selected materials, the data in Tab.3.3 were collected where a p-type doped ($1e15cm^{-3}$) semiconductor with $q\Phi_{s,p} = 4.92eV$ and electron affinity of $4.05eV$ [19] is considered. The selected doping concentration does not coincide with the one of the three wafers but this is not critically important in this qualitative discussion because as shown in Sect.3.1.1 the Fermi potential doping concentration dependence is logarithmic.

Table 3.3: Contact behavior as a function of different materials.

Material	$\mathbf{q\Phi_M}$	**Behavior**
Al [18]	$4.10eV$	rectifying
Ti [20]	$4.33eV$	rectifying
W [19]	$4.55eV$	rectifying
Cu[21]	$4.65eV$	rectifying

The obtained results need to be carefully interpreted mainly for two reasons:

1. The metal work function is a complex parameter at which can not be associated a unique value [22]: for instance aluminum work function values from $4.06eV$ to $4.26eV$ can be found in the literature; this is due to the fact that it depends on the surface material properties (e.g. atoms configuration [23]).

2. The presented discussion is based on energy band diagram, thus it is based on a model that can not truly describe the considered physical device. For instance it does not consider any fabrication process consequence on the contact properties.

Therefore a design based only on work function values is not reliable, since they can not be univocally defined. In order to make ohmic a rectifying contact a typical solution [24] consists into highly dope the semiconductor near to the contact regions. The reason can be understood by considering that when a rectifying contact is realized, a depletion region on the semiconductor side is formed [17], with expression:

$$X_{dep} = \sqrt{\frac{2\epsilon_{Si}(V_{bi} - V_a)}{qN_a}} \tag{3.7}$$

where V_{bi} is the associated built it voltage, and V_a the applied voltage. If the doping concentration is very high ($> 1e19cm^{-3}$) then the depletion width on the semiconductor side is so small that tunnelling takes place, thus making the rectifying contact behaving as an ohmic one (Fig.3.7). This is one of the reasons for which conventional MOSFETs present highly doped *pn* junctions for the source and drain contacts [25], realized through an implantation step. Another solution can be instead to use silicidation technology, which allows through the deposition of a metal and a successive annealing to reduce the contact resistance. But the first solution is not compatible with the design specifications since it implies the presence of a *pn* junction that by definition is absent in junctionless transistors, while the second one it would make the process more complex and expensive, since an additional material has to be deposited and the annealing process has to be controlled.

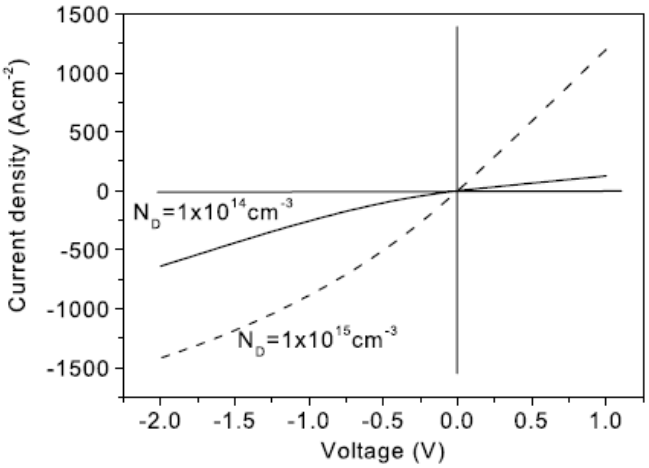

Figure 3.7: *IV* curve for two different doping concentrations [26].

Considering that the available wafers are p-doped, the simplest solution is to consider aluminum as contact material, since it is a p-type dopant for silicon [27], [28]. The resulting *pp++ junction* can be fabricated by deposition and successive thermal diffusion avoiding in this way implantations and thus design specifications violation. Regarding n-type junctionless transistors, they can be fabricated by using the receipt given in [28].

3.2.2 Parasitic Resistance Model

In order to decide how to geometrically size the junctionless transistor under analysis, it was modelled, in terms of resistances, as in Fig.3.8 where R_c is the contact resistance, R_{sub} the resistance associated to the region between the channel and contacts, and R_{ch} that is the channel resistance. The latter is not considered in this section because its behavior, that depends on the applied voltage, is treated in Sect.4. The model in Fig.3.8 clearly resembles the one for conventional MOSFETs (besides the absence of the resistance associated to the extension and S/D-substrate junctions).

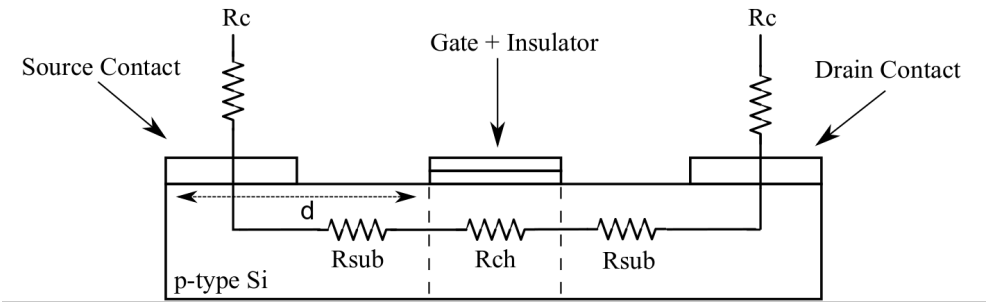

Figure 3.8: Schematic of the resistance modelling of the junctionless transistor.

Resistance R_{sub}

Regarding R_{sub}, it can be modelled as a resistive rectangular box (Fig.3.9) of length d (spacing between source/drain and gate in Fig.3.8), width W (that is the width of the transistor), thickness T_{Si}, and resistivity ρ (measured in Sect.3.1.3). R_{sub} can be then expressed as:

$$R_{sub} = \rho \frac{d}{W T_{Si}} \tag{3.8}$$

That is the resistance associated to the region between the S/D contacts and the channel boundary is modelled through the Pouillet's law. Clearly this model will provide an overestimation of the parasitic resistance since the current flows along the less resistive path during operation and not in all the box.

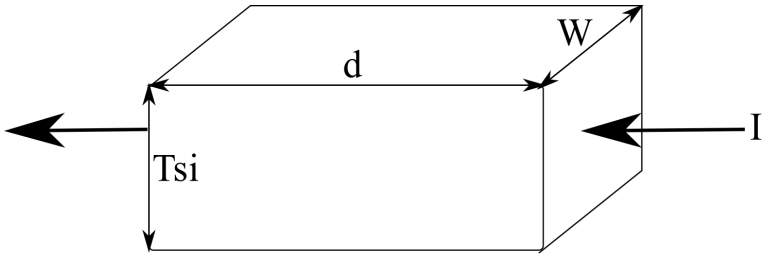

Figure 3.9: Modelling R_{sub} as a rectangular box: T_{Si} is the device layer thickness, d the spacing between the S/D and the gate, W the width of the transistor.

In order to understand the influence of the width W and the S/D-gate spacing d on R_{sub}, two cases are considered:

1. Fixing W to a certain value, and computing R_{sub} as a function of d.

2. Fixing d to a certain value, and computing R_{sub} as a function of W.

Case 1: fixed width W

Since the minimum photolithographic resolution of the mask aligner is $2\mu m$, the width W is fixed to a larger value, that is $5\mu m$. Then the resistance R_{sub} is computed with the implementation of a MATLAB code (Appendix A.4), and plotted as a function of d in Fig.3.10. Regarding T_{Si} and ρ, a value of $500nm$ and $4.44\Omega cm$ were respectively selected; that is the worst case analysis is considered (Wafer L in Tab.3.2), since the smallest T_{Si} leads to the largest resistance. As can be observed, increasing the distance d, the resistance R_{sub} increases, and this is expected since d is in the numerator in Eq.3.8.

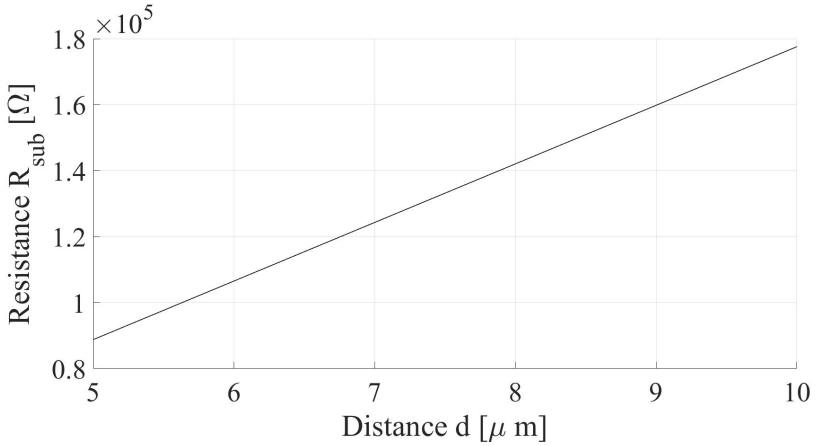

Figure 3.10: Case 1: Fixed W ($5\mu m$). Plot of R_{sub} as a function of the separation region d, which is ranging from $5\mu m$ to $10\mu m$. Wafer under analysis is L (Tab.3.2).

Case 2: fixed separation d

The separation region d was fixed to $5\mu m$, and the resistance R_{sub} was computed as a function of W, while the other parameters are the same as in Case 1. The result (Fig.3.11) is expected: as the transistor width is increased the resistance decreases.

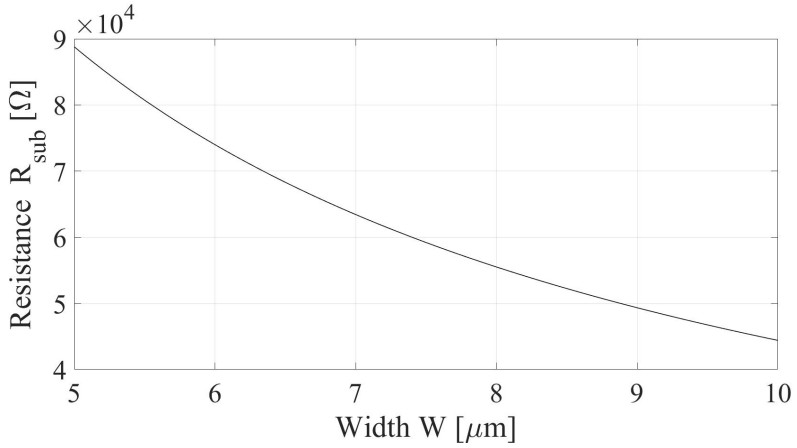

Figure 3.11: Case 1: Fixed d ($5\mu m$). Plot of R_{sub} as a function of the transistor width W, which is ranging from $5\mu m$ to $10\mu m$. Wafer under analysis is L (Tab.3.2).

On the basis of the two computations it is clear that d should have minimum value (that is its dimension coincides with the contact length), while W should be large. The **critical** point is that whatever the value of d and W, the estimated resistance R_{sub} value ($\sim 1e5\Omega$) is unacceptable. The technological **solution** is to increase the doping concentration in all the regions excepts under the channel (Fig.3.12), since changing the doping in that region would implies a change in the needed device layer thickness (Eq.3.1). This can be obtained through a deposition of aluminum followed by diffusion (treated in Sect.3.2.3). On the basis of these considerations, the structure schematic up to now is the one depicted in Fig.3.12.

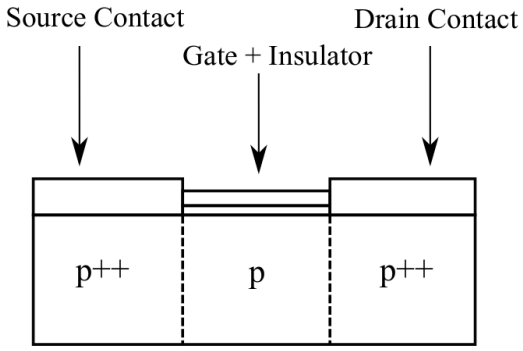

Figure 3.12: Proposed structure schematic for the reduction of the high parasitic resistance R_{sub} (not in scale).

The structure in Fig.3.12 is clearly representing an impracticable device, since the metallization contacts are next to the metal gate, thus short circuiting the transistor. A more correct schematic is that in Fig.3.13, where the contacts are connected to the highly doped region through a via, and an insulator separates them from the metal gate.

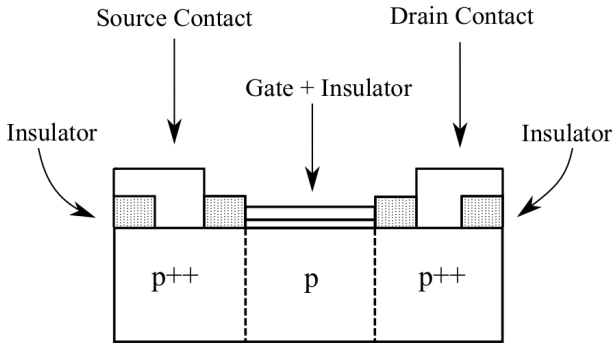

Figure 3.13: More realistic structure schematic for the reduction of the high parasitic resistance R_{sub} (not in scale).

Regarding the transistor width, it has to be considered that from a mask design point of view, the aspect ratio between the width and the length of the S/D contact, as well as of the gate, should not be too large [29]. But a well defined criterion can be selected only by considering other parameters as the contact resistance, since the latter is dependent on the transistor width.

Resistance $\mathbf{R_c}$

The contact resistance is defined as [30]:

$$R_c = \left(\frac{\delta J}{\delta V}\Big|_{V=0} \right)^{-1} \tag{3.9}$$

where $J = J_{SM} - J_{MS}$ is the total current density and V the applied voltage. The critical problem is that accurate quantum transmission functions have to be considered in order to find a closed form of Eq.3.9[31]. In [30] the contact resistance of aluminum on silicon as a function of doping concentration for different barrier heights is reported (Fig.3.14). But is difficult to interpret the plot, because for p-type silicon only barrier heights lower than $0.5eV$ are reported, which are not consistent with the the theoretical barrier height that is at least $0.8eV$ (Eq.3.4).

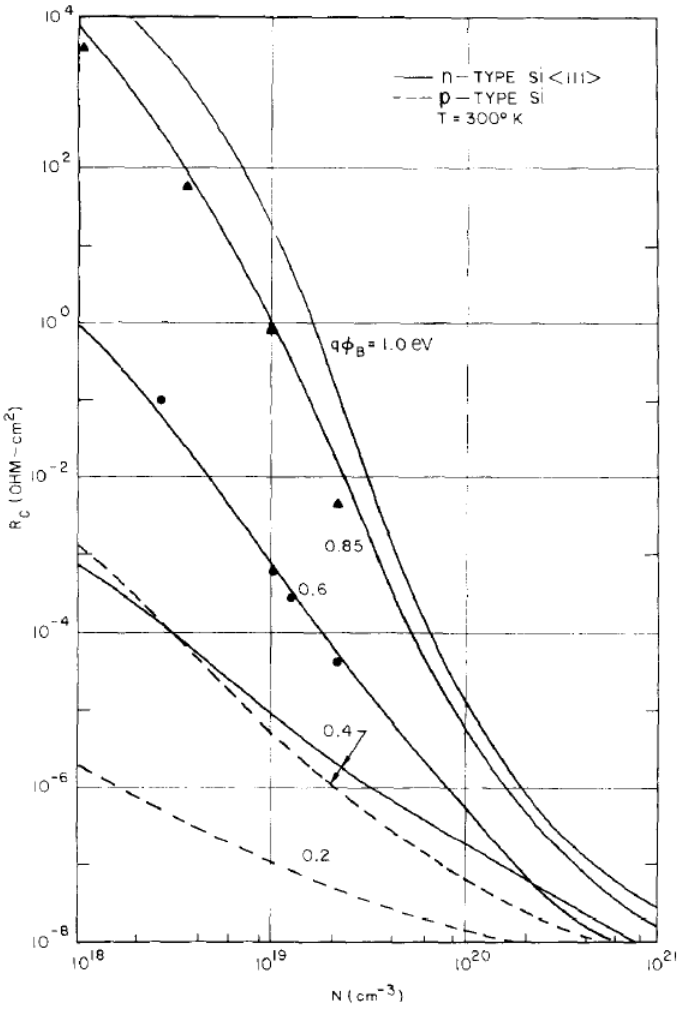

Figure 3.14: Contact resistance of aluminum as a function of doping concentration for different barrier heights. Solid line (n-type silicon), dotted line (p-type silicon) [31].

Thus a different approach has to be considered; in [32] the contact resistance of aluminum on p-type silicon is reported as a function of the silicon resistivity (Fig.3.15). Since we are considering a $p{+}{+}$ region under the contact area, the expected dop-

ing concentration is at least $1e20cm^{-3}$ [25], at which corresponds a resistivity of approximately $0.001\Omega cm$ [14].

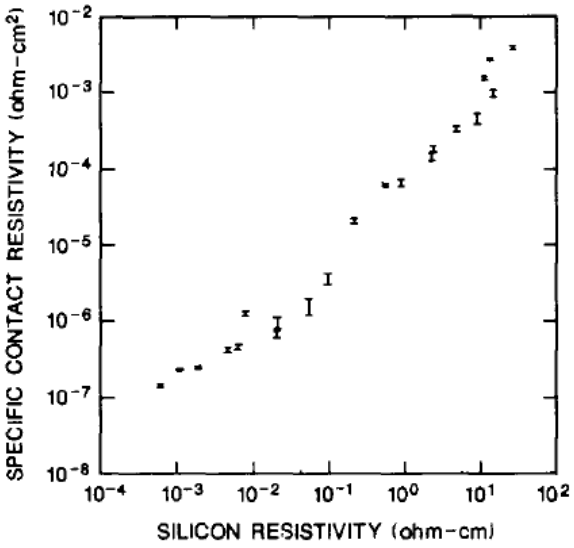

Figure 3.15: Contact resistance of aluminum as a function of resistivity [32].

Therefore on the basis of the plot in Fig.3.15, a specific contact resistivity of approximately $1\times10^{-7}\Omega cm^2$ is expected; dividing this value by the product $WL_{contact}$, where the width W and the contact length $L_{contact}$ have values larger than the minimum photolitographic resolution ($W = 5\mu m$ and $L_{contact} = 5\mu m$), the value of the contact resistance is $R_c \cong 0.4\Omega$. For the same width and doping concentration R_{sub} results to be around $2 \times 10^{-5}\Omega$ which is negligible with respect to R_c. This means that if a current of $1mA$ flows in the transistor, a voltage drop of $0.4mV$ is associated to the parasitic resistance, which is not critical for junctionless transistors whose threshold voltage is in the $1V$ range; therefore a width and contact length around that value ($5\mu m$) ideally guarantees a low parasitic resistance. It also has to be considered that for higher doping concentration under the contact regions ($1e22cm^{-3}$), R_c can be further reduced. Moreover in this analysis the contact area is considered to cover the whole width of the transistor, while usually the latter presents an array of contacts [33]. Up to now the schematic of the designed transistor is the one shown in Fig.3.16.

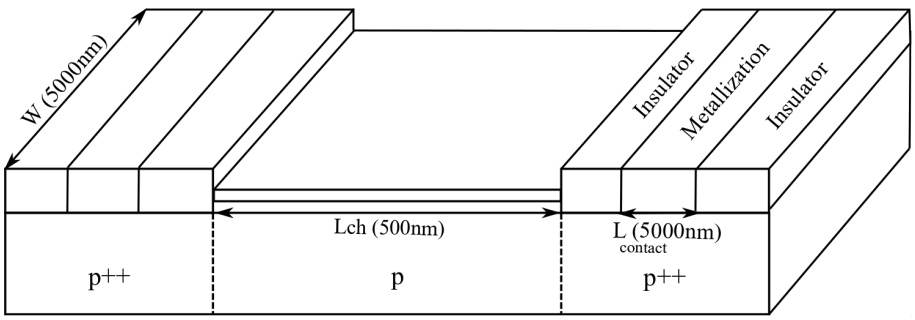

Figure 3.16: Schematic of the junctionless transistor structure after resistance modelling (not in scale).

There are mainly two reasons for which array of contacts (Fig.3.17) are implemented in transistor fabrication process:

- Reliability, that is by placing many contacts closed to each other, microcracks in the deposited metal layer can be reduced, thus improving surface uniformity [34];
- Performance, that is by placing more than one contact is possible to reduce the contact resistance [29].

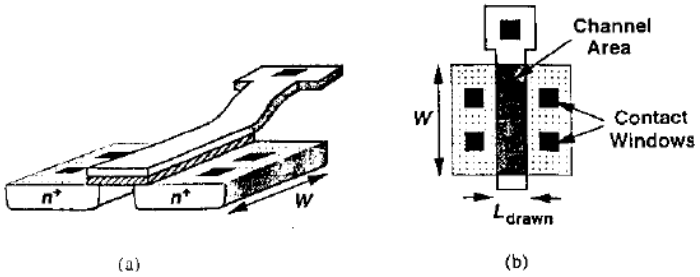

Figure 3.17: Array of contact in a MOSFET [33].

The reason for which the contact resistance can be reduced can be understood by reasoning as follows: if, for example, for one contact window the contact resistance is $R_{c,1} = 200\Omega$ (Fig.3.18(a)), in the case in which an additional contact windows is added to the structure (Fig.3.18(b)), then the new resistance $R_{c,2}$ is in parallel to $R_{c,1} = 200\Omega$, thus providing an overall contact resistance of 100Ω. Clearly also the parasitic resistance associated to the metal has to be considered, but given the low resistivity of aluminum, it could be neglected in this qualitative discussion.

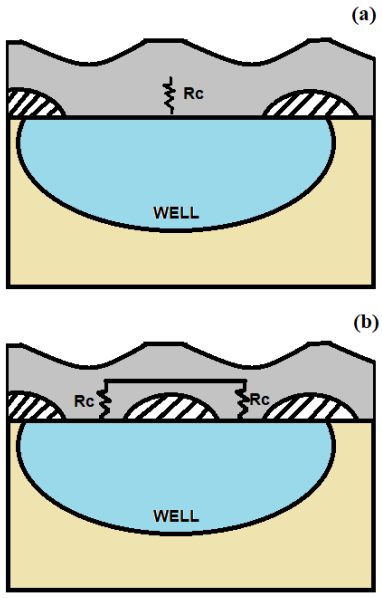

Figure 3.18: (a)Considering only one contact window. (b) Considering two contact windows. The resistance R_m associated to the metal is not shown.

It is important to remark that the structure schematics provided in the previous sections do not represent the definitive device; for instance, it is well know that the diffusion profile is never completely flat, thus making impossible a doping profile as the one indicated in Fig.3.16, but it was decided to follow this kind of discussion flow in order to make clearer the involved problems. The values of all the geometrical parameters are reported in Sect.3.5.

3.2.3 Aluminum Deposition and Diffusion

Deposition

In order to have an estimation of the deposition rates of aluminum (and silicon oxide), the following process was tested in the clean room:

- deposition through sputtering of $20nm$ of SiO_2;
- measurement of deposited SiO_2 film thickness through an ellipsometer;
- deposition through sputtering of $100nm$ of Al;
- photoresist (PR) deposition, exposure, development;
- measurement through a profilometer of PR with respect to Al;
- Al etching, and measurement through profilometer of PR with respect to SiO_2.

Regarding the deposition process, it was realized with the Sputter AJA (AJA International Inc.) shown in Fig.3.19 giving as results the data provided in Tab.3.4.

Figure 3.19: Sputter AJA used for testing the aluminum deposition rate in the clean room.

Table 3.4: Process parameters for aluminum and silicon oxide deposition.

Target	Thickness	Pressure	Power	Ar Flow	Dep. Rate	Time
SiO2	$20nm$	$4mtorr$	$100W$	$10sccm$	0.11	$30min$
Al	$100nm$	$4.1mtorr$	$80W$	$10sccm$	0.2	$1.38h$

The deposition rates (provided by the machine itself) are quite low, thus suggesting an overall minimum deposition process time of about two hours. After the silicon oxide deposition, three measurements with an ellipsometer were taken giving as results the data collected in Tab.3.5, while an example of the ellipsometer output is given in Fig.3.20.

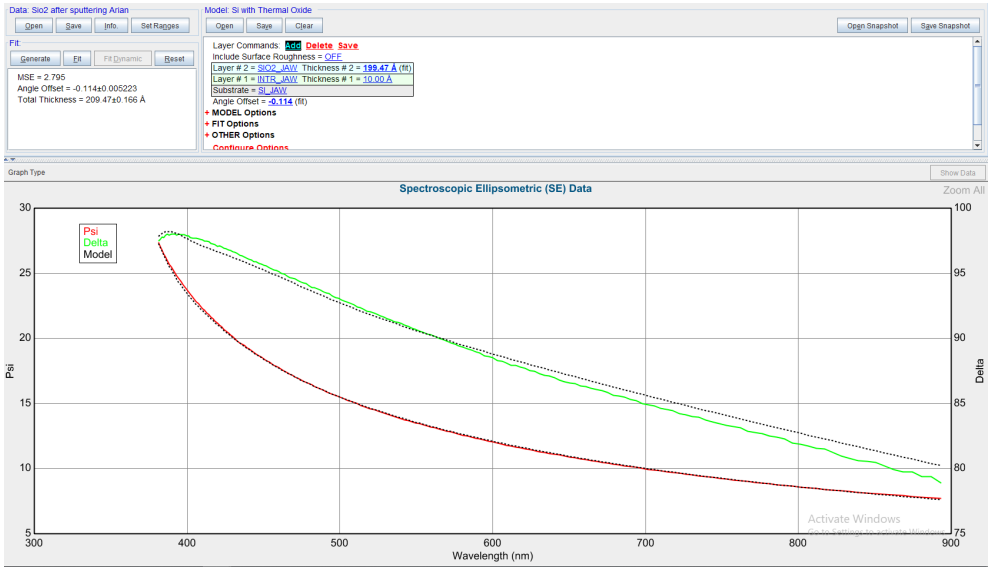

Figure 3.20: Third ellipsometer measurement for the silicon oxide thickness.

The measurement results are consistent with the inputs provided to the sputtering machine: the oxide thickness is around $20nm$.

Table 3.5: Ellipsometer measurement data for the silicon oxide thickness.

Measurement 1	$20.974nm \pm 0.17.7nm$
Measurement 2	$20.970nm \pm 0.17.6nm$
Measurement 3	$20.947nm \pm 0.16.6nm$

After the silicon oxide thickness measurement, aluminum was deposited (Tab.3.4) and the following procedure was followed for the photoresist deposition:

- wafer cleaned with Isopropanol;
- bake $2min$ at 115°C;
- spin coating, through Spinner 2 AB Plast Spin 150, of positive PR $s1813$:
  - time: $30s$.
  - speed: $3000RPM$.

- bake $1min$ at 115°C.

and then were exposed through a Mask Aligner EVG 620, where the used mask was composed of arrays of squares, giving as result the structure in Fig.3.21.

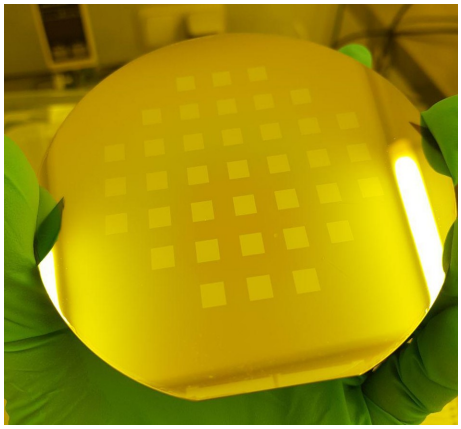

Figure 3.21: Wafer used for testing the deposition process after exposure.

Then the exposed photoresist was developed with $MF3189$, and through a Profilometer DEKTAK 150, three measurements in a row in the middle of the wafer were carried out giving as results the data collected in Tab.3.6.

Table 3.6: Profilometer measurement data for the estimation of the photoresist thickness in three different squares.

Measurement 1	$1009.60nm$
Measurement 2	$1005.08nm$
Measurement 3	$1003.32nm$

Therefore approximately a $1\mu m$ thick PR layer was deposited. Then the aluminum was etched with Aluminium Etch 16:1:1:2, and the structure in Fig.3.22 was obtained.

Figure 3.22: Wafer used for testing the deposition process after aluminum etching. The dark areas are made of silicon oxide.

Then three measurements (along the same squares in of Tab.3.6) with the profilometer were taken, providing the data in Tab.3.7.

Table 3.7: Profilometer measurement data for the estimation of the aluminum thickness in three different squares.

Measurement 1	$1122.40nm$
Measurement 2	$1120.10nm$
Measurement 3	$1120.16nm$

It is important to remark that every measurement is done in the same associated square (that is Measurement 1 in Tab.3.6 is taken on the same square on which then Measurement 1 in Tab.3.7 is carried out) in order to have a coherent result. Subtracting the measurements in Tab.3.6 from the ones in Tab.3.7, gives an estimation of the deposited aluminum thickness (Tab.3.8):

Table 3.8: Profilometer measurement data for the aluminum thickness.

Al thickness 1	$112.80nm$
Al thickness 2	$115.02nm$
Al thickness 3	$116.84nm$

The thickness of the deposited aluminum layer is larger than the expected one ($110nm$), but this is not considered critical for the fabrication process, since the aluminum is going to be used as metallization material.

Diffusion

Once the aluminum is deposited, a diffusion process is necessary in order to make it diffuse in the silicon, thus lowering the semiconductor resistivity. The process can be modelled as a *constant dose* diffusion process, that is the concentration is assumed to have a gaussian distribution [35]:

$$N(x,t) = \frac{Q_0}{\sqrt{\pi Dt}} e^{-\left(\frac{x}{2\sqrt{Dt}}\right)^2} \tag{3.10}$$

where:

- Q_0 $(atoms/cm^3)$ is the deposited dose;
- $D = D_0 e^{-\left(\frac{E_a}{kT}\right)}$ (cm^2/s) is the diffusion coefficient;
- D_0 (cm^2/s) is an extrapolated constant;
- E_a (eV) is the activation energy;
- k (eV/K) is the Boltzmann constant;
- T (K) is the temperature;
- t (s) is the time.

The critical point is to understand how to set the time t and temperature T in order to obtain a quasi constant distribution in the $p{+}{+}$ regions, and how to estimate the

deposited dose Q_0. The latter is a complex parameter, since its value is dependent on the crystalline structure of the deposited material, and the deposition technique. But a simple estimation can be done in the following way:

$$Q_0 = \frac{N_0 \rho_{Al} T_{Al}}{m_{Al}} \tag{3.11}$$

where:

- N_0 $(mol^{-1})$is the number of Avogadro;
- ρ_{Al} (kg/cm^3) is the aluminum density;
- T_{Al} (cm) is the thickness of the deposited layer;
- m_{Al} (g/mol) is the aluminum molar mass.

That is, multiplying the density by the thickness of the deposited layer the surface density is obtained. So dividing the latter by the molar mass the number of moles square centimeter is obtained. Multiplying the latter by the Avogadro number provides the number of atoms per square centimer. Regarding the choice of the time and the temperature, they are critically important since the dependence in Eq.3.10 is exponential. Thus a MATLAB code was implemented (Appendix A.5) to understand the influence of these parameters on the estimated diffusion process; a fixed temperature of $1300K$ (which is the maximum achievable temperature in the facility) was assumed, and the concentration profile was computed for different diffusion times, giving as results the plots in Fig.3.23.

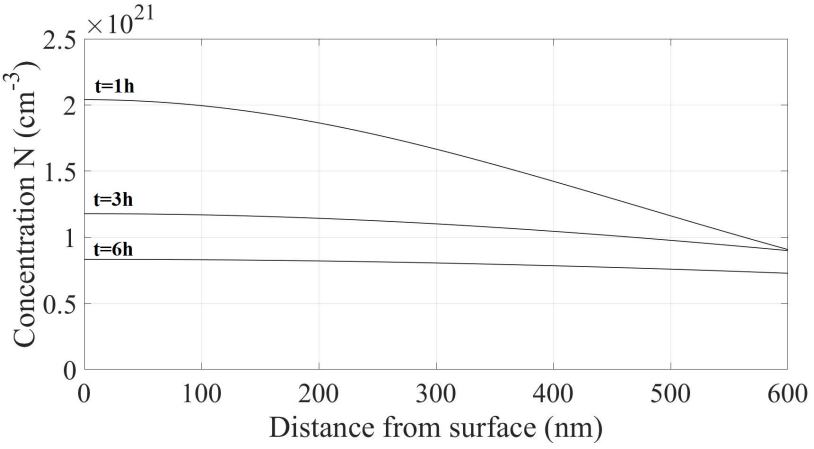

Figure 3.23: Concentration profile assuming a temperature of $1300K$ and a predeposited layer of $20nm$ for different diffusion times.

As expected, by increasing the time, the concentration is lowering at the surface, and the profile is less steep [35]. If instead of an aluminum deposited layer of $20nm$, a thickness of $200nm$ is considered, the concentration profile presents higher dopants at the surface (Fig.3.24). This makes sense since in the expression provided for the dose estimation (Eq.3.11), the latter is obtained by multiplying the area density by the deposited layer thickness, so it is assumed that thicker is the deposited layer, and higher is the *constant dose* at the surface.

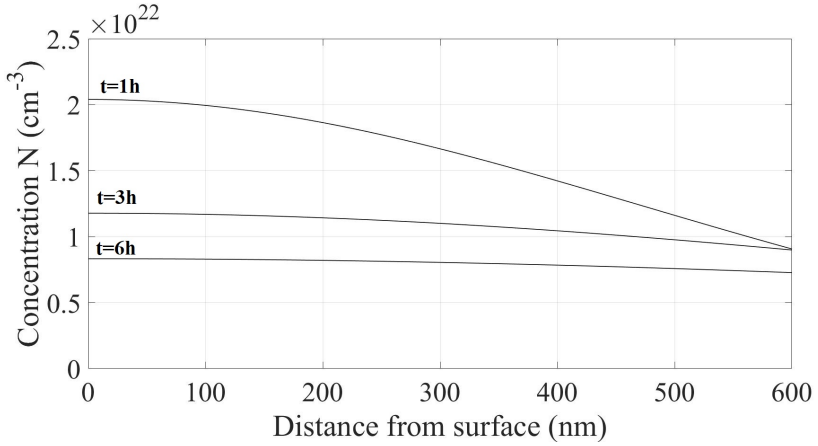

Figure 3.24: Concentration profile assuming a temperature of $1300K$ and a pre-deposited layer of $200nm$ for different diffusion times.

Since a high doping concentration implies a reduction of the parasitic resistance, a deposition of $200nm$ of aluminum is considered. Regarding the diffusion, a $3h$ process at $1300K$ guarantees, at least ideally, a more flat profile.
It is important to remark that the presented analysis is not considering fabrication process effects such as lateral diffusion, and diffusion caused by the deposition temperature during the layer deposition step. Thus it represents a theoretical estimation.

3.3 Gate

3.3.1 Material Selection

The gate material is of critical important, since the flat band voltage, and consequently the threshold voltage, is by the definition expressed as the gate/semiconductor work function difference [21] that for n-type and p-type transistors are respectively defined as:

$$V_{FB,n} = q\Phi_M - q\Phi_{s,n} = q\Phi_M - (q\chi + Eg/2 - q\Phi_n) \tag{3.12}$$

$$V_{FB,p} = q\Phi_M - q\Phi_{s,p} = q\Phi_M - (q\chi + Eg/2 + q\Phi_p) \tag{3.13}$$

The threshold voltage, instead, is defined as the gate voltage at which the device layer is fully depleted, where by full depletion its meant that the depletion width is equal to the device layer thickness. The expression for the depletion width of n-type and p-type semiconductors are respectively defined as:

$$X_{dep,n} = -\frac{\epsilon_{Si}}{C_{ox}} + \sqrt{\left(\frac{\epsilon_{Si}}{C_{ox}}\right)^2 - \frac{2\epsilon_{Si}}{|q|N_d}(V_G - V_{FB})} \tag{3.14}$$

$$X_{dep,p} = -\frac{\epsilon_{Si}}{C_{ox}} + \sqrt{\left(\frac{\epsilon_{Si}}{C_{ox}}\right)^2 + \frac{2\epsilon_{Si}}{|q|N_a}(V_G - V_{FB})} \tag{3.15}$$

where $C_{ox} = \frac{\epsilon_{ox}}{T_{ox}}$ (F/cm^2) is the capacitance per unit area, defined as the ratio of the insulator dielectric constant and the insulator thickness. Regarding threshold voltage expressions, they are obtained by imposing $X_{dep} = T_{Si}$, and solving for V_G:

$$V_{th,n} = V_{FB} + \frac{|q|N_d}{2\epsilon_{Si}}\left[\frac{\epsilon_{Si}^2}{C_{OX}^2} - \left(t_{Si} + \frac{\epsilon_{Si}}{C_{OX}}\right)^2\right] \tag{3.16}$$

$$V_{th,p} = V_{FB} - \frac{|q|N_a}{2\epsilon_{Si}}\left[\frac{\epsilon_{Si}^2}{C_{OX}^2} - \left(t_{Si} + \frac{\epsilon_{Si}}{C_{OX}}\right)^2\right] \tag{3.17}$$

Therefore the principle of operation of the junctionless transistor can be expressed as:

$$\begin{cases} V_{G_{ON}} = V_{FB} \\ V_{G_{OFF}} = V_{th} = V_{FB} + \frac{|q|N_d}{2\epsilon_{Si}}\left[\frac{\epsilon_{Si}^2}{C_{OX}^2} - \left(t_{Si} + \frac{\epsilon_{Si}}{C_{OX}}\right)^2\right] \end{cases} \tag{3.18}$$

for the n-type junctionless transistor, and:

$$\begin{cases} V_{G_{ON}} = V_{FB} \\ V_{G_{OFF}} = V_{th} = V_{FB} - \frac{|q|N_a}{2\epsilon_{Si}}\left[\frac{\epsilon_{Si}^2}{C_{OX}^2} - \left(t_{Si} + \frac{\epsilon_{Si}}{C_{OX}}\right)^2\right] \end{cases} \tag{3.19}$$

for the p-type one.

The depletion width expression can be derived by applying the Poisson equation under well defined assumptions, which are discussed in details in the attached paper "*A Numerical Method to Extract the Depletion Region Width of Planar Junctionless*

Transistors" (Appendix B.2) attached to this thesis. In order to understand the influence of the gate material on the flat band and threshold voltages, an analysis in term of doping concentration is carried out by considering first polylisilicon and the aluminum as gate materials.

Flat Band Voltage

A MATLAB code (Appendix A.6) was implemented in order to observe the dependence of the flat band voltage on the doping concentration (Eq.3.12). A first analysis was done by assuming as a gate material polysilicon, which is considered both p-doped and n-doped with work functions of $5.15eV$ and $4.05eV$ respectively [36]; that is the n-type polysilicon gate is assumed to have a work function equal to the electron affinity, while the p-type one is considered to have a work function equal to the electron affinity plus the energy band gap. Considering a n-type junctionless transistor, its flat band voltage behavior is depicted in Fig.3.25. As can be observed, for a p-type gate, the flat band voltage is positive, and for a difference of one order of magnitude in N_D, its value is around $1V$.For the n-type gate, instead, it is negative and around $0V$.

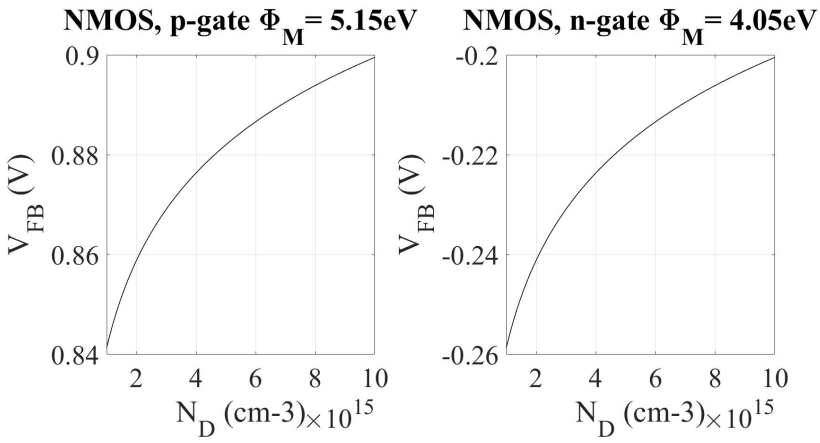

Figure 3.25: Flat band voltage behavior as a function of the doping concentration for an n-type junctionless transistor.

Therefore the gate material has an influence on the polarity of the power supply, since in the case in which the flat band voltage is positive and the threhsold voltage is negative, a dual power supply is needed; if instead both the voltages are negative (or positive) then a single power supply system can be considered, thus lowering the circuit complexity. For a p-type junctionless transistor the behavior is similar, in the sense that, as can be seen in Fig.3.26, for a p-type gate the flat band voltage is positive, while for the n-type gate, instead, it is negative. But while the p-gate implies a flat band voltage value around $0V$, the n-gate one implies a value around $-1V$. This observation is particularly important in the case in which $CMOS$ processes are considered.

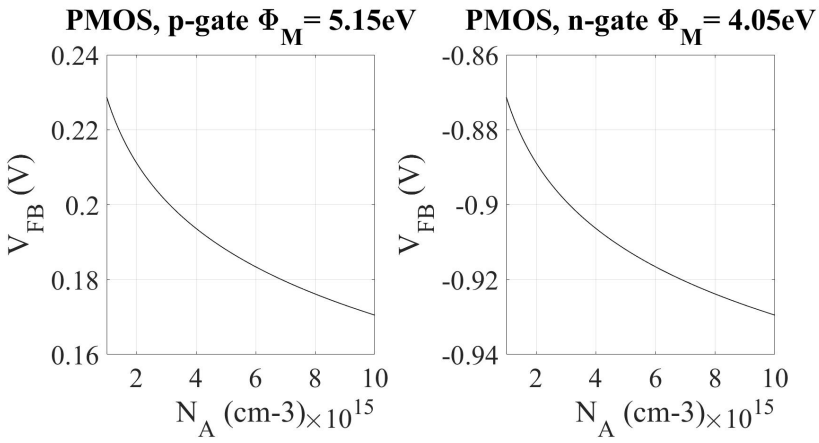

Figure 3.26: Flat band voltage behavior as a function of the doping concentration for an p-type junctionless transistor.

One of the typical problem related to the implementation of polysilicon gate in conventional MOSFET is the polydepletion effect [37]; it is remarkable that since junctionless transistors do not work in *inversion*, they do not suffer of such effect. But the practical problem, from a fabrication process point of view, is that polysilicon is not available in the facility; moreover it would require a doping process in order to increase its concentration to at least $1e20cm^{-3}$ (value for which it can be considered to *work* as a metal [38]), thus increasing the fabrication process complexity. In standard CMOS process a further doping implantation for doping the polysilicon gates is not required, since they are doped during the implantation step (the polysilicon is used as a mask for the channel). Therefore it is not convenient to consider polysilicon as gate material. A possible solution is to use, instead, aluminum ($q\Phi_m = 4.1eV$), which is available in the facility and does not require doping processes. In this case the flat band voltages for the p-type junctionless transistors under analysis are those indicated in Tab.3.9.

Table 3.9: Analytical flat band voltages considering aluminum as gate material and the measured doping concentrations of Tab.3.2.

JLT on wafer:	$\mathbf{N_A}$	$\mathbf{V_{FB}}$
L	$3.08 \times 10^{15} cm^{-3}$	$-0.8498V$
C	$2.73 \times 10^{15} cm^{-3}$	$-0.8467V$
R	$2.35 \times 10^{15} cm^{-3}$	$-0.8429V$

Threshold Voltage

As can be seen in Eq.3.16, the threshold voltage depends also on the oxide capacitance, which is defined as the ratio of the oxide permittivity and oxide thickness. The latter can be sized by considering, for instance, the dielectric strength, that is the maximum electric field that the oxide can sustain before breaking. For silicon oxide this value is greater than $10MV/cm$ [25]. Then assuming that the junctionless transistor has a threshold voltage smaller than $5V$, the power supply voltage can be assumed to have a value $V_s = 5V$. Considering an oxide thickness $\leq 10nm$, the rigidity is then given by $6.25MV/cm$ which is less than $10MV/cm$. Therefore in the

following analysis a value for the oxide thickness of $10nm$ is considered. Regarding the permittivities of silicon and silicon oxide, they are considered to be 3.9 and 11.7 [39]. Thus a MATLAB code was implemented (Appendix A.7) in order to understand the threshold voltage behavior as a function of the doping concentration; the device layer thickness was set equal to $300nm$, thus a meaningful range of doping concentration is $[1e15, 1e16]cm^{-3}$ since, as shown in Fig.3.1, the maximum depletion width has to be larger than the silicon device layer thickness. In Fig.3.27 the threshold voltage of a n-type junctionles transistor (with aluminum gate) is shown.

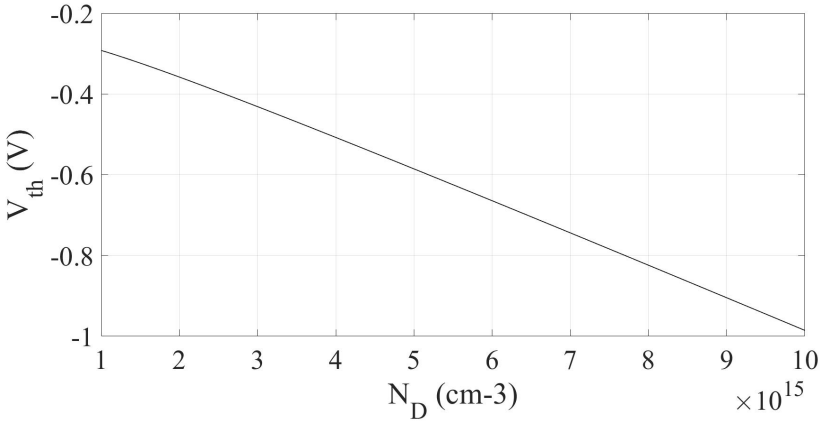

Figure 3.27: Threshold voltage behavior as a function of the doping concentration for an n-type junctionless transistor ($t_{Si} = 300nm$).

As can be observed, the threshold voltage of an n-type junctionless transistor increases (in absolute value) with increasing doping concentration. This can be explained as it follows: as the electron concentration increases, a greater voltage (in absolute value) is needed in order to repel the free electrons. A complementary explanation (that is reasoning in terms of holes) can be given for the threshold voltage of a p-type junctionless transistor, which is shown in Fig.3.28.

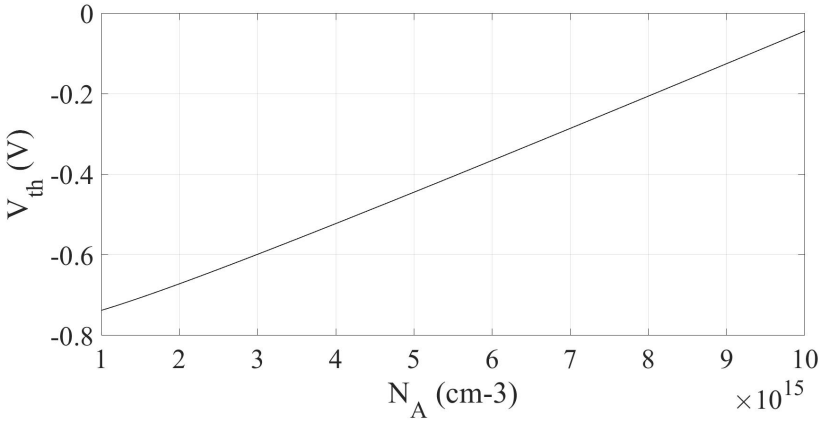

Figure 3.28: Threshold voltage behavior as a function of the doping concentration for an p-type junctionless transistor ($t_{Si} = 300nm$).

Considering the three available wafers, the analytical threshold voltages can be then computed, assuming a gate oxide thickness of $10nm$ and a device layer thickness

T_{Si} that is $30nm$ less than the maximum depletion width. The analytical threshold voltage values are reported in Tab.3.10.

Table 3.10: Analytical threshold voltage considering aluminum as gate material and and a gate oxide thickness of $10nm$

JLT	$\mathbf{N_a}$	**Max** $\mathbf{X_{dep}}$	$\mathbf{T_{Si}}$	$\mathbf{V_{FB}}$	$\mathbf{V_{th}}$
L	$3.08 \times 10^{15} cm^{-3}$	$530nm$	$\sim 500nm$	$-0.8498V$	$-0.1829V$
C	$2.73 \times 10^{15} cm^{-3}$	$560nm$	$\sim 530nm$	$-0.8467V$	$-0.1866V$
R	$2.35 \times 10^{15} cm^{-3}$	$600nm$	$\sim 570nm$	$-0.8429V$	$-0.1904V$

The operating range of the designed device is therefore less than $1V$; this implies that the device is a **low voltage** transistor.

Depletion Width

The depletion width analysis is not reported here, since it is treated in the attached paper to this thesis. But for a sake of completeness the curve for the JLT built on the wafer C is reported in Fig.3.29.

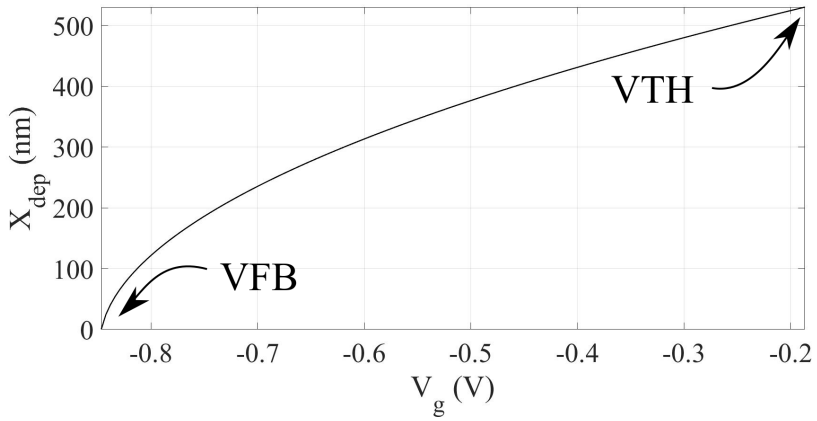

Figure 3.29: Analytical Depletion width of the p-type JLT built on wafer C. The threshold and flat band voltages are indicated.

As can be observed in Fig.3.29, the depletion width is equal to zero for $V_G = V_{FB}$ (ON state), while is equal to T_{Si} for $V_G = V_{th}$ (OFF state) as expected.

3.4 Fabrication Process

In this section an ideal fabrication process for the designed device is proposed where by ideal is meant:

- all the involved processes (deposition, diffusion, exposure, etching) are considered to be unaffected by source of non-idealities (e.g. contamination);
- misalignment is not considered.

3.4.1 Process Flow

Transistors Separation

The starting point is a SOI wafer with a device layer thickness thin enough to ensure full depletion, depicted in Fig.3.30.

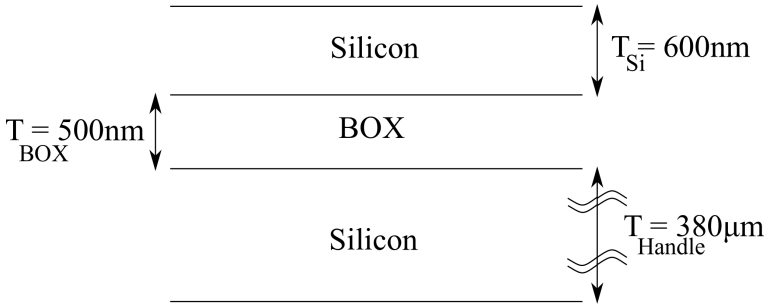

Figure 3.30: PROC_0: starting point of the proposed fabrication process.

In order to separate the transistors an idea could be to cover the wafer with photoresist (PR) as in Fig.3.31, and then through MASK_0 obtain, after exposure and PR development, the structure in Fig.3.32

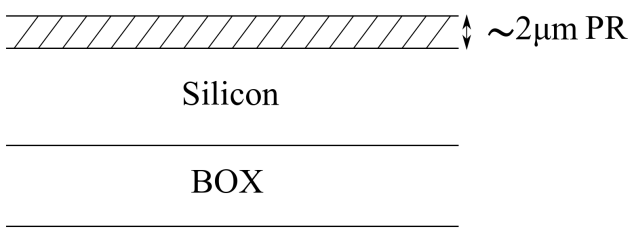

Figure 3.31: PROC_1: wafer covered with PR. The handle substrate is not shown.

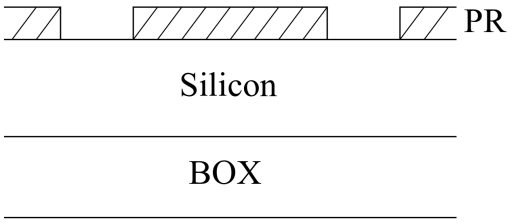

Figure 3.32: PROC_2: wafer after PR exposure and development.

Then through a Deep Reactive Ion Etching (DRIE), the silicon device layer thickness is etched, using the PR as a mask (Fig.3.33). Two considerations have to be done:

- successive DRIE processes could burn the photoresist, making its removal difficult; this implies that the same photoresist layer has not to be used more than one time. Alternatively a layer of SiO_2 can be patterned to avoid using PR as DRIE mask.

- in the clean room it was verified that the SiO_2 beyond the Si layer is not etched by the DRIE, that is it acts as an **etch stop layer**.

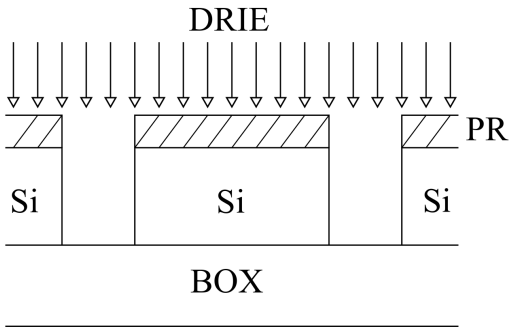

Figure 3.33: PROC_3: DRIE using the PR as mask and the SiO_2 as etch stop layer.

Now that the transistors separation is ensured, only the the device layer of one transistor is considered in the next sections, that is only the pillar in the middle of Fig.3.33 will be depicted in the following schematics.

Highly doped p++ regions

In order to obtain the highly doped regions necessary for the reduction of the parasitic resistances, the PR has to be removed, and again spanned on the entire wafer. It follows exposition through MASK_1 and development. Then the structure in Fig.3.34 is obtained.

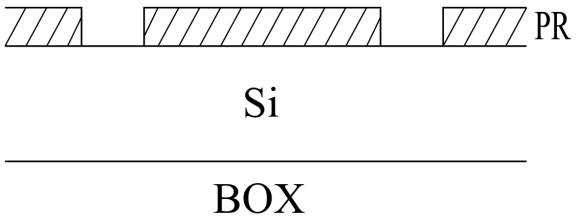

Figure 3.34: PROC_4: Wafer after redeposition of PR, exposure, and development.

Successively a $200nm$ layer of aluminum is deposited through sputtering (Fig.3.35).

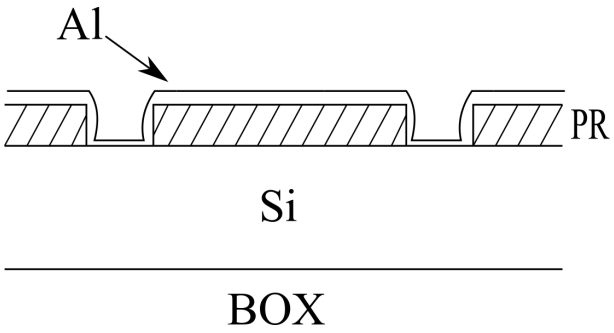

Figure 3.35: PROC_5: Aluminum deposition throgh sputtering.

Then lift off is performed, and ideally the structure in Fig.3.36 is obtained. A typical rule of thumb for the efficiency of the lift off process is that the thickness of the deposited layer has to be smaller that one third of the photoresist thickness. Since the standard spin coating process in the clean room produces PR layers with thickness between around $2\mu m$, the lift off process, at least ideally is expected to work. It is important to point out that the sputtering process could burn the photoresist, since the sputtered target material (Al) hits the wafer during the process; but assuming that the photoresist layer thickness is very high, and that its surface properties are not significantly changed by the sputtering process, it possible to consider lift off as solution of the selective aluminum removal.

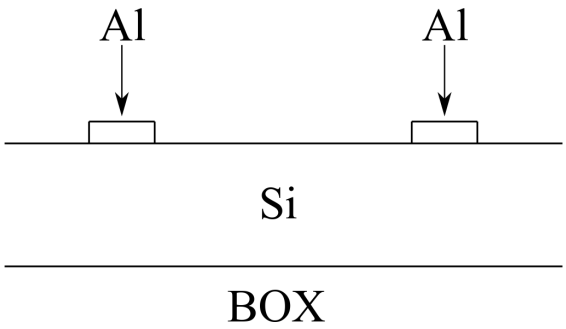

Figure 3.36: PROC_6: after lift off process; corner effects not considered, ideal process.

So the diffusion process is performed, leading to the structure in Fig.3.37.

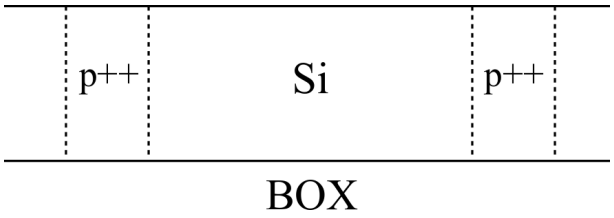

Figure 3.37: PROC_7: after diffusion process.

Before proceeding in the discussion, it is important to remark that:

- the structures in Fig.3.37 is obviously ideal, since flat doping profile concentrations are not realistic;
- all the structures in this section are not in scale. The number of every geometrical parameter will be given in the Sec.3.5.

Gate Insulation and Definition

In order to insulate the metal gate for the source and drain contact, a thick ($1\mu m$) layer of SiO_2 is deposited through sputtering on the wafer, and then patterned through MASK_2, leading to the structure in Fig.3.38.

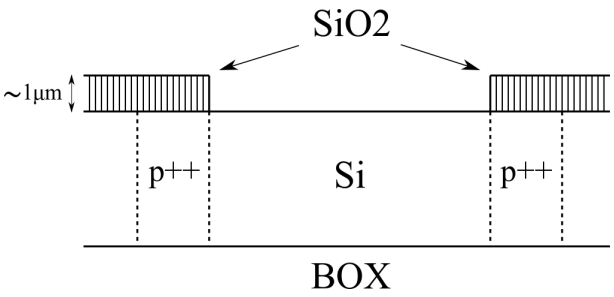

Figure 3.38: PROC_8: after deposition and patterning of SiO_2.

Clearly the situation depicted in Fig.3.38 is *unrealistic*, since it is impossible to obtain a perfect alignment; it is more likely to happen the situation depicted in Fig.3.39.

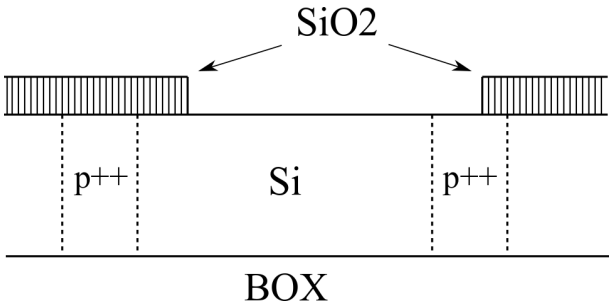

Figure 3.39: How PROCESS_8 could be affected by mask misalignment.

Then a $10nm$ layer of SiO_2 is deposited through sputtering on the whole wafer. This layer is the gate oxide. The reason for which two oxide films are deposited is that the oxide in Fig.3.38 is used for separating the metal gate from the metal contact,

and thus have to be thick to ensure insulation; while the oxide deposited in Fig.3.40 is used for the gate oxide thus has to be thin to ensure gate controllability.

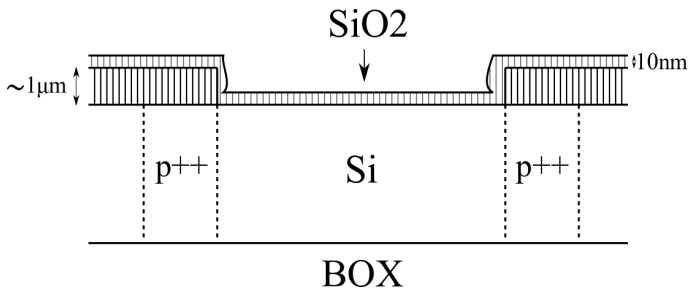

Figure 3.40: PROC_9: deposition of a thin layer $SiO2$ (gate oxide).

Then again PR is deposited, exposed with MASK_3, and developed leading to the structure in Fig.3.41. Next a $500nm$ aluminum is deposited through sputtering for the metal gate, and another lift off process is done, and the structure in Fig.3.42 is (ideally) obtained.

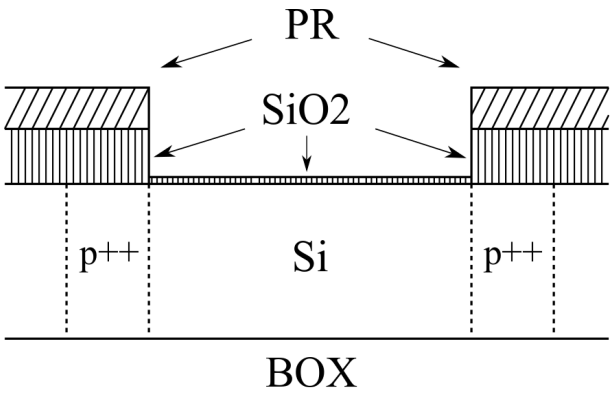

Figure 3.41: PROC_10: structure after PR development.

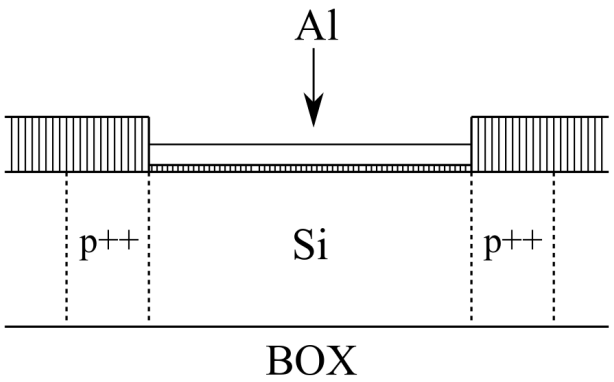

Figure 3.42: PROC_11: Structure after aluminum deposition and lift off.

Metallization

In order to provide a connection for the source and drain contacts, a via is defined through MASK_4 (Fig.3.43) by patterning the SiO_2 layer.

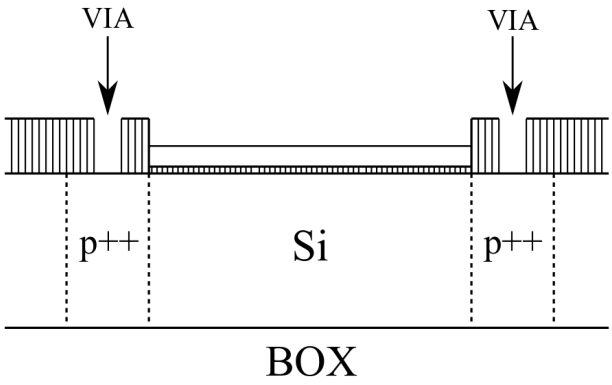

Figure 3.43: PROC_12: Via definition.

Finally PR is deposited again, exposed with MASK_5, and the structure in Fig.3.44 is obtained; the transistor fabrication process is finished.

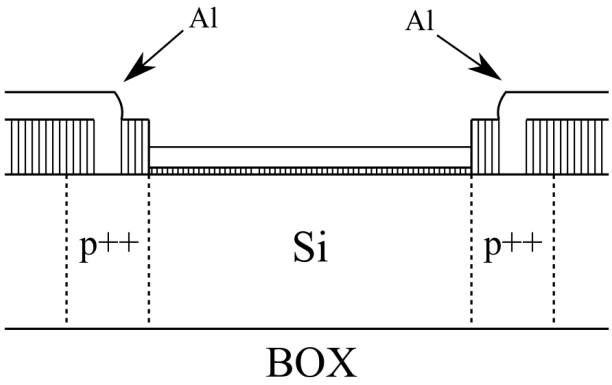

Figure 3.44: PROC_12: final structure

3.4.2 Mask

In this ideal fabrication process six masks are used:

- MASK_0: transistor separation;
- MASK_1: p++ regions definition;
- MASK_2: gate definition;
- MASK_3: gate metallization;
- MASK_4: via definition;
- MASK_5: source/drain metallization.

The first mask is used to separate the transistors, and is depicted in Fig.3.45. This means that in an area of $500\mu m \times 500\mu m$ a transistor will be placed. The area is very large compared to the typical values, but this choice is dependent on the size of the pads which has to be large to allow correct measurements with the probes available in the facility.

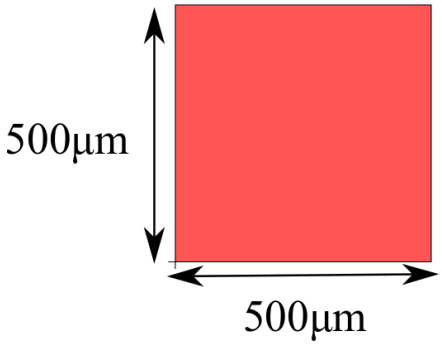

Figure 3.45: MASK_0: transistor separation

The second mask is used to define the highly doped regions, and is depicted in Fig.3.46 superimposed to the first mask.

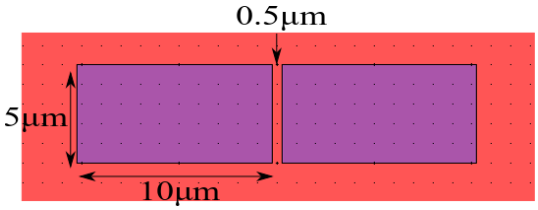

Figure 3.46: MASK_1: p++ regions definition.

The third mask is used to define the gate contact, and is depicted in Fig.3.47. Since a resolution of $500nm$ is needed, the maskless machine has to be used (nominal resolution $350nm$). Clearly also a value of $350nm$ an be selected, but since the latter value is a nominal one, it was decided to select a slightly larger value. Therefore MASK_2 establishes the channel length.

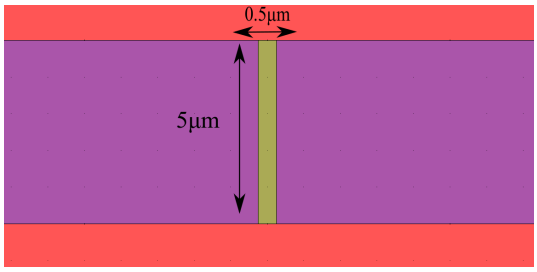

Figure 3.47: MASK_2 : gate definition.

The fourth mask is used for the gate metallization and gate pad, and is depicted in Fig.3.48. The pads are very large, since the probes that will be used for the device testing are large as well.

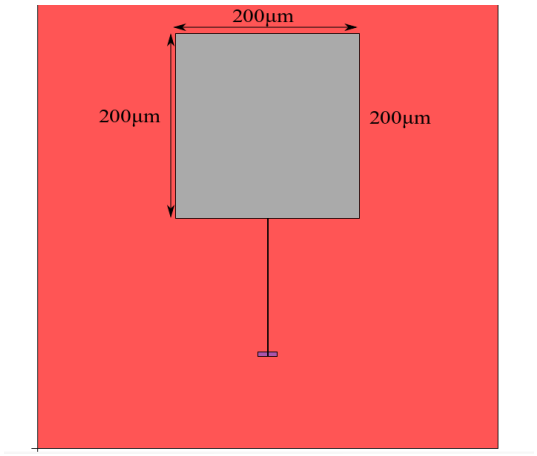

Figure 3.48: MASK_3: gate metallization.

The fifth mask is used for the definition of the vias (Fig.3.49). A distance of $2\mu m$ separates the two contacts, in order to avoid misalignment problems. The width of the via is chosen to be $3\mu m$, while the length $2\mu m$. These values guarantee a low contact resistance, and are larger than the nominal MEMS photolithographic resolution ($2\mu m$).

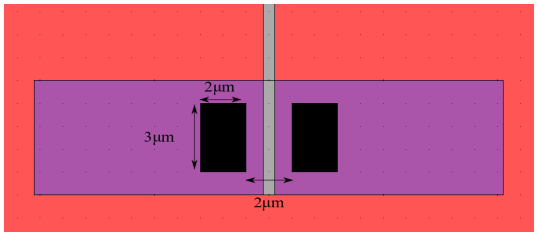

Figure 3.49: MASK_4: via definition.

Finally the last mask, that is used for the metallization of the source and drain pads (Fig.3.50).

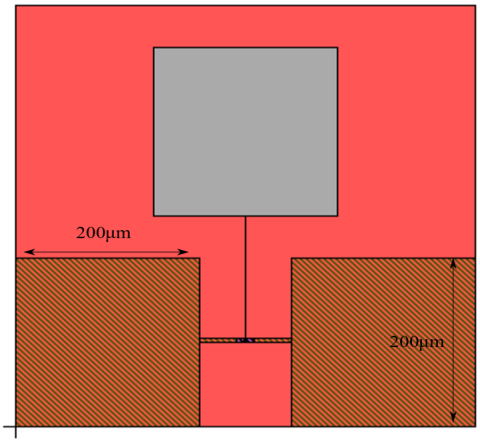

Figure 3.50: MASK_5: source and drain metallization.

Remark: all the depicted masks in this section were designed with the software TANNER L-Edit (v2016), from Mentor Graphics, and the license was provided by the University of South-Eastern Norway.

3.5 Final Structure

On the basis of the design carried out in the previous sections, the transistor (shown in Fig.3.51) results to be characterized by the geometrical parameters in Tab.3.11.

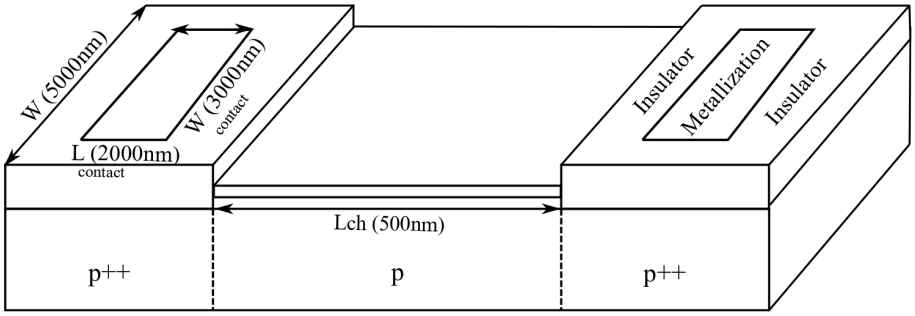

Figure 3.51: Proposed single gate planar junctionless transistor; the BOX is not shown (not in scale).

Table 3.11: Geometrical parameters of the designed transistor.

Parameter	**Value**
Channel Length	$500nm$
Transistor Width	$5\mu m$
Contact Length	$2\mu m$
Contact Width	$3\mu m$
Oxide Thickness	$10nm$
Device Layer Thickness L	$500nm$
Device Layer Thickness C	$530nm$
Device Layer Thickness R	$570nm$

Regarding the materials, the proposed transistor is characterized by those indicated in Tab.3.12.

Table 3.12: Materials of the designed transistors.

Component	**Material**
Device Layer	Silicon
Gate	Aluminum
Gate Oxide	Silicon Oxide
BOX	Silicon Oxide
Source/Drain Contacts	Aluminum

While the doping concentration, threshold voltage, and flat band voltage are those in Tab.3.13.

Table 3.13: Doping Concentration, threshold voltage, and flat band voltage of the designed transistor.

JLT	$\mathbf{N_a}$	$\mathbf{V_{FB}}$	$\mathbf{V_{th}}$
L	$3.08 \times 10^{15} cm^{-3}$	$-0.8498V$	$-0.1829V$
C	$2.73 \times 10^{15} cm^{-3}$	$-0.8467V$	$-0.1866V$
R	$2.35 \times 10^{15} cm^{-3}$	$-0.8429V$	$-0.1904V$

The transistor geometrical parameters are not optimized with respect to modern devices, considering that a single device occupies an area of $500 \times 500 \mu m^2$. But as explained in Sect.2.3 the target of the project is to build a low cost transistor for ICs applications in a MEMS clean room. The doping concentration is very low as compared to conventional transistors, and the OFF/ON voltages are in the range of $1V$; the proposed transistor is therefore a low doped low voltage electronic device.

Chapter 4

Simulation

In this section the simulations results obtained through COMSOL Multiphysics [40] of a junctionless transistor are reported. The simulations are used to verify the expected device behavior, that is:

- if the current versus the gate voltage, for a fixed source voltage, is equal to zero at the analytical threshold voltage;
- if an accumulation layer is observed for gate voltages greater than the flat band;
- if the current versus the source voltage, for different gate voltages, has an output characteristics similar to that of MOSFETs.

4.1 Model definition

4.1.1 Structure

The structure of the proposed p-type junctionless transistor is depicted in Fig.4.1(a). But as explained in detail in the attached paper (Appendix B.2), a simplified structure (Fig.4.1(b)) is considered.

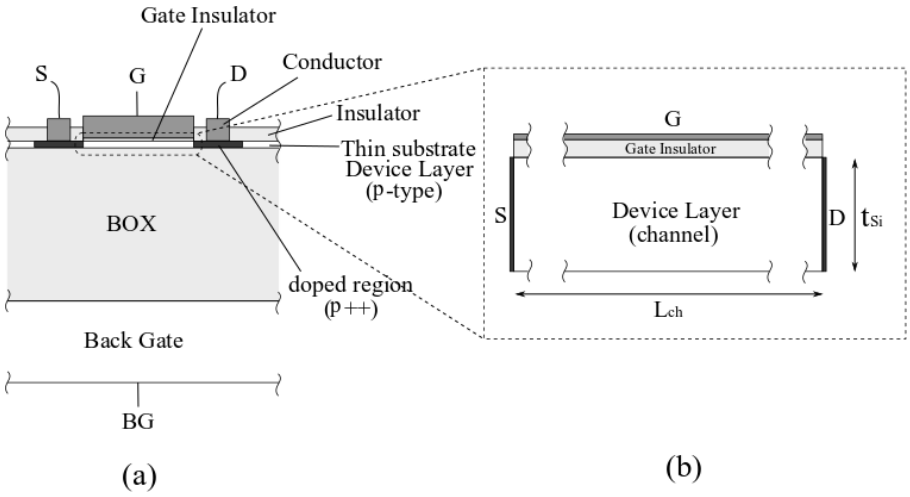

Figure 4.1: P-type PJLT Physical Structure. (a) Complete Structure on FDSOI wafer. (b) Simplified Structure.

4.1.2 Parameters

Since the target of the simulations is to verify the device behavior, is not important which designed transistor is going to be implemented in COMSOL Multiphyisics. Considering the wafer L (Tab.3.10), the parameters used in the simulation are those in Tab.4.1, while the implementation in COMSOL Multiphysics is shown in Fig.4.2.

Table 4.1: Parameters used for the COMSOL Multiphysics simulation.

Parameter	Value
N_a	$3.08e15cm^{-3}$
T_{Si}	$500nm$
L_{ch}	$500nm$
E_g	$1.13eV$
$q\chi$	$4.05eV$
ϵ_{Si}	$3.9\epsilon_0$
T_{ox}	$10nm$
ϵ_{ox}	$11.7\epsilon_0$
$q\Phi_M$	$4.1eV$
T	$293.15K$
Carrier Statistics	Fermi-Dirac

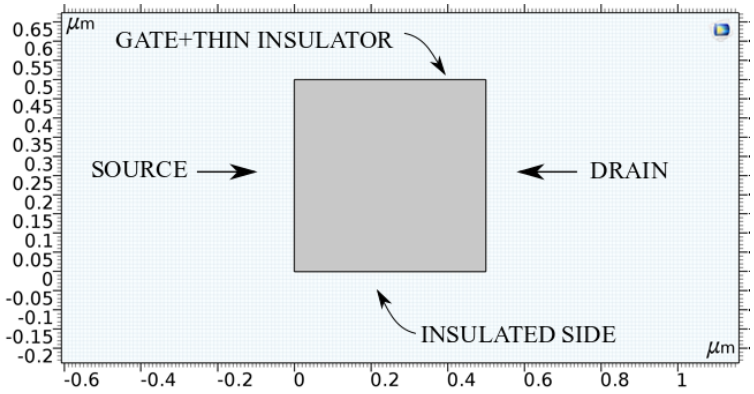

Figure 4.2: Implementation in COMSOL Multiphysics of the p-type junctionless transistor.

4.2 Simulations results

4.2.1 I_s vs V_g

The p-type junctionless transistor was simulated for a fixed V_s of $10mV$, for V_g sweeping in the range $[-3V, 0.25V]$. The simulation range is larger than the one analytically needed to observe the principle of operation, that is $[V_{FB}, V_{th}] = [-0.85V, -0.18V]$. But it allows to observe what happens for voltages greater then the threshold and the flat band ones. Once simulated, the data were exported in MATLAB (Appendix A.8), providing as result the curve shown in Fig.4.3. Regarding the source voltage, a small value ($10mV$) is selected in order to allow the current to flow between the source and the drain.

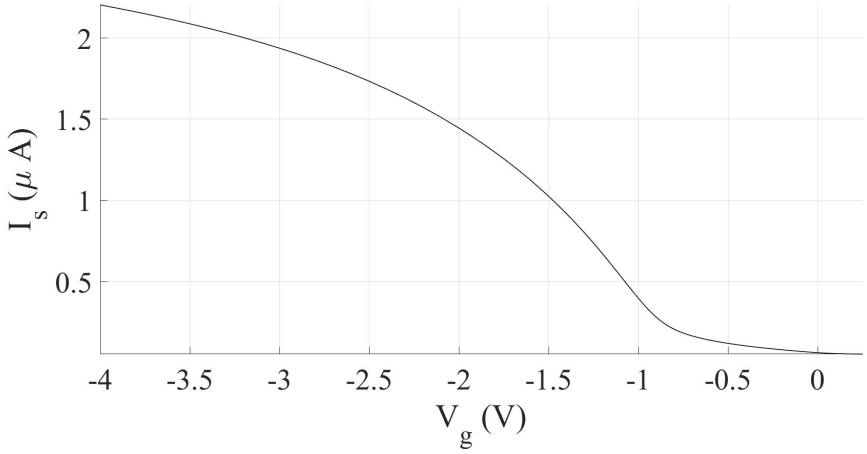

Figure 4.3: I_s vs V_g for a fixed source voltage $V_s = 10mV$.

Threshold Voltage Extraction

As can be observed in Fig.4.3, the current is not zero around $0V$ (although is very small, about $50nA$), while for voltages greater (in absolute) than $-1V$ the current is less steep. In order to correctly interpret the result, it is important to remark that the threshold voltage definition in Eq.3.16 is not the one that has to be considered for the extraction of its value. In fact, while Eq.3.16 is an analytical threshold voltage expression defined in terms of depletion width and *independent* of the current behavior, the threshold voltage of an IV curve is instead defined on the basis of different extraction methods [41]. It was decided to implement the ELR (extrapolation in the linear region) method which considers the threshold voltage as the gate-voltage axis intercept of the linear extrapolation of the $IdVg$ curve at maximum slope (i.e. maximum transconductance) plus $V_d/2$ (Fig.4.4).

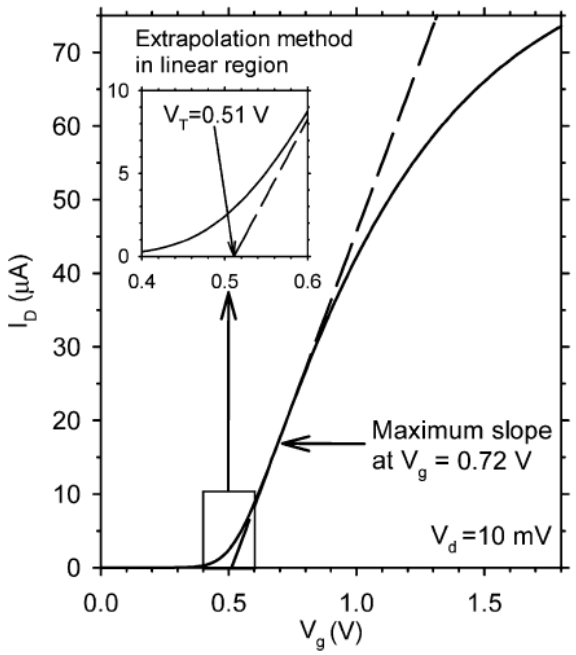

Figure 4.4: ELR method: linear extrapolation in the linear region [41].

But the method, as proposed, is valid only for n-type transistors. For a p-type it has to be modified as the gate-voltage axis intercept of the linear extrapolation of the $IsVg$ curve at maximum slope (i.e. maximum (in absolute value) transconductance) minus $V_s/2$, since the current is mirrored with respect to the y-axis. By using a MATLAB code (Appendix A.8), the plot in Fig.4.5 is obtained, with a threshold voltage value of $-0.71V$, while the analytical value is $-0.18V$; the difference is of $0.53V$. The discrepancy between the two values can be explained by considering that the analytical model, defined and analyzed in the attached paper, resembles the device behavior only for high doping concentration, that is it implicitly assumes that the semiconductor is a *good* conductor, while the device under analysis has a doping concentration in the order of $1e15cm^{-3}$.

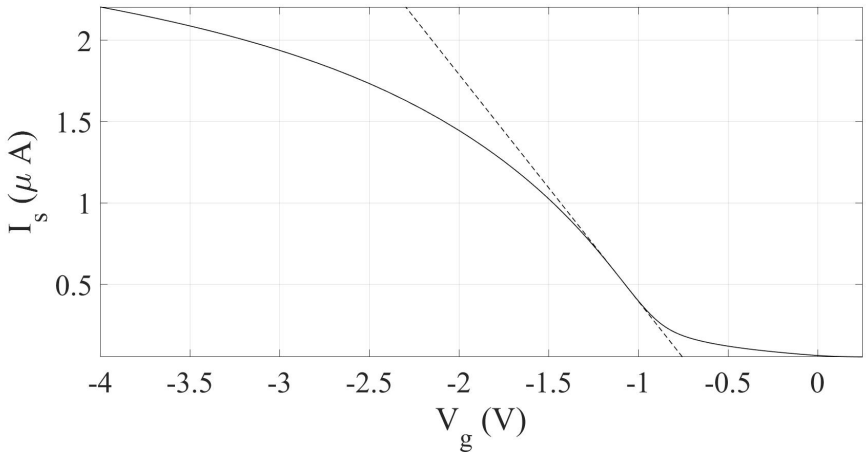

Figure 4.5: Application of the ELR method for the threshold voltage extraction. Solid: I_s/V_g. Dashed: linear extrapolation of I_s/V_g at maximum slope.

In order to verify the ELR method, the transconductance versus gate voltage was plotted, and its minimum observed (Fig.4.6).

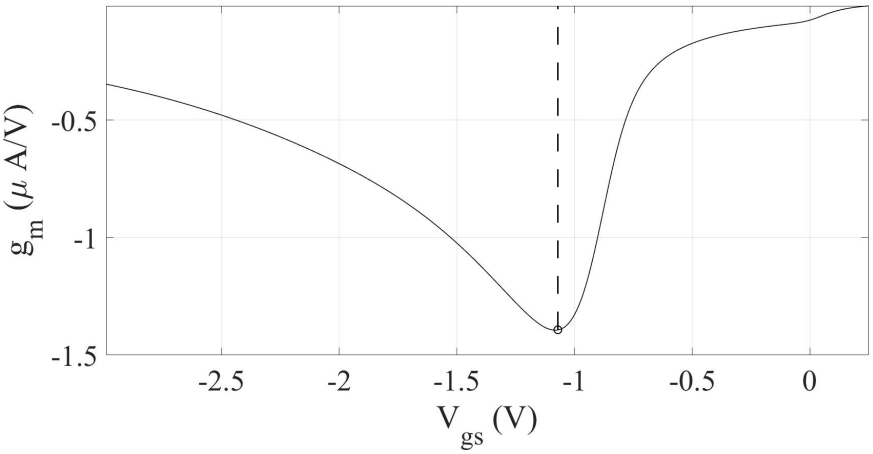

Figure 4.6: Solid: transconductance vs gate voltage. Dasehd: vertical line passing for the minimum. The intercept with the gate voltage axis is at $-1.08V$.

The intercept with the gate voltage axis is at $-1.08V$, and this is coherent with Fig.4.7.

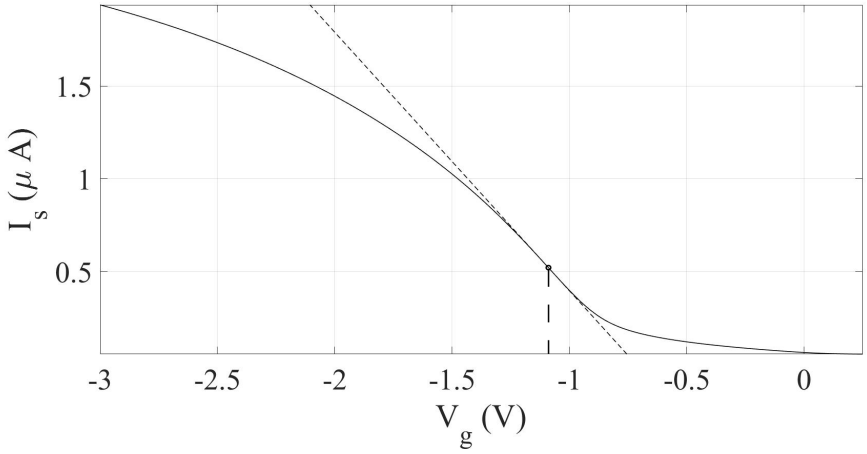

Figure 4.7: Solid: source current vs gate voltage. Dashed: linear extrapolation of I_s/V_g at maximum slope.

Flat Band Voltage Extraction

The analytical flat band voltage is expected for a gate voltage of $-0.85V$. Graphically this value seems to be around the point in which the curve in Fig.4.5 starts to be less steep, that is the point at which the slope of the transconductance is maximum. Therefore in order to extract its value, it was decided to plot the transconductance versus the gate voltage (Fig.4.8).

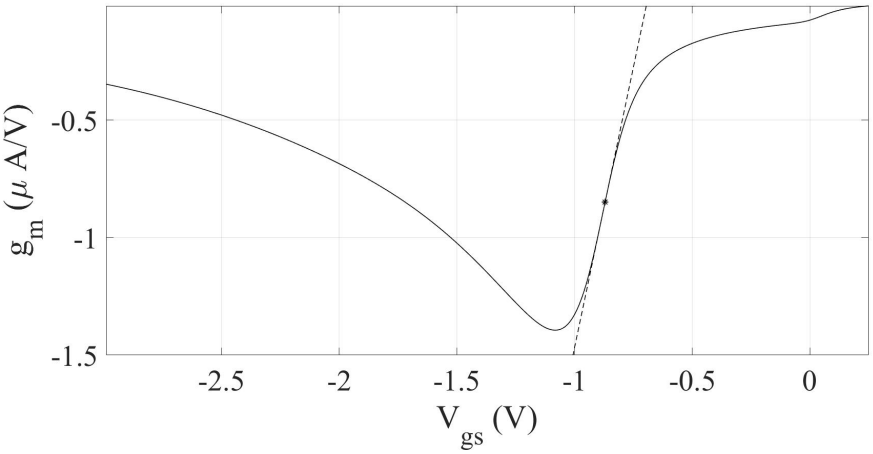

Figure 4.8: Solid: transconductance vs gate voltage. Dashed: linear extrapolation of g_m/V_g at maximum slope. The x-coordinate of the indicated star corresponds to the extracted flat band voltage

The value of the gate voltage for the point of maximum slope is $-0.87V$, that is $20mV$ smaller than the analytical one.
Therefore on the basis of the simulations results it is possible to define:

- the threshold voltage as the gate-voltage axis intercept of the linear extrapolation of the $IsVg$ curve at maximum slope (i.e. maximum (in absolute value) transconductance) minus $V_s/2$.

- The flat band voltage as the gate-voltage axis intercept of the line that is perpendicular to the linear extrapolation of the g_m/V_g curve at maximum slope.

Hole concentration analysis

In order to understand how the carriers are behaving, the surface concentration of the device is analyzed. In Fig.4.9 the hole concentration for a gate voltage of $0V$ is depicted.

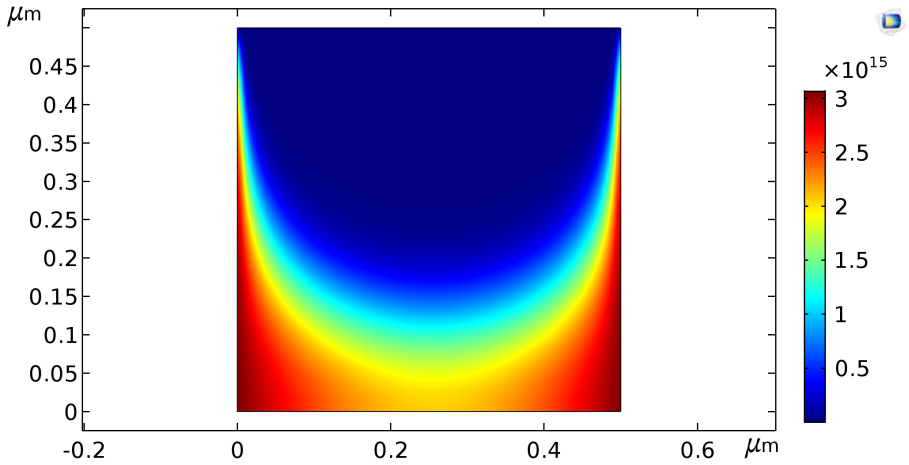

Figure 4.9: Hole surface concentration for $V_g = 0V$.

As can be observed in Fig.4.9, the hole concentration in the blue region is very low, while in the red regions is higher. The critical problem in the observation of this plot is that is not possible to quantitatively distinguish the depletion region boundary, although qualitatively is expected to be in the transition region. This was the main motivation behind the decision to write the attached paper. By decreasing the gate voltage (that is by making it more negative), we expect to attract more holes towards the surface, thus a reduction of the *depletion region* (that is approximately the blue one) is expected. In Fig.4.10 the simulation for $V_G = -0.5V$ is shown.

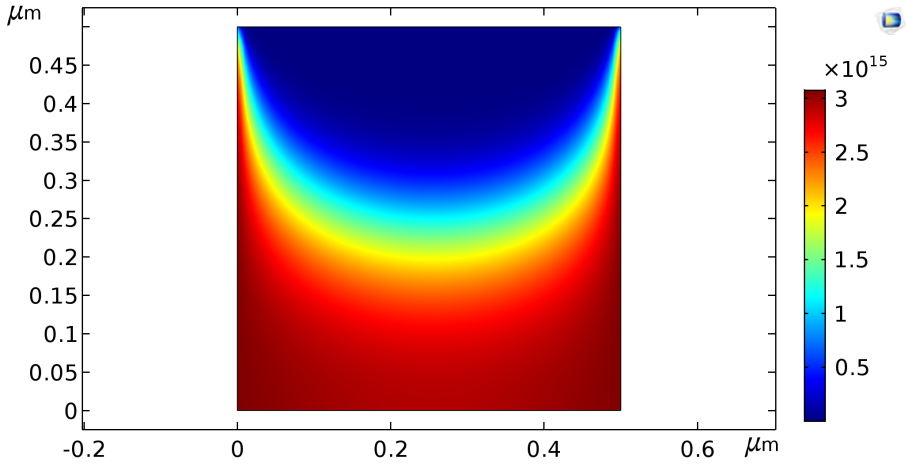

Figure 4.10: Hole surface concentration for $V_g = -0.5V$.

For $V_G = -0.5V$ the blue region is reduced, and more holes are present in the device layer. The device is therefore in partial depletion. For a $V_g = -0.75V$ the concentration in Fig.4.11 is obtained.

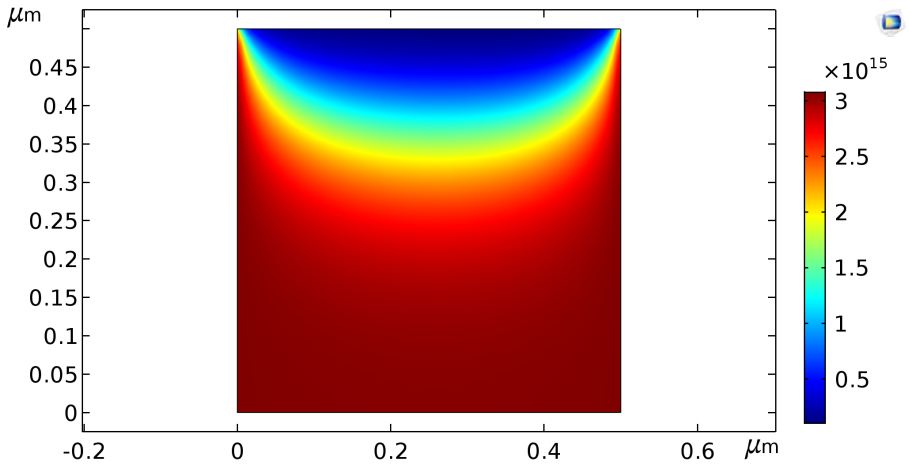

Figure 4.11: Hole surface concentration for $V_g = -0.75V$.

The device is working as expected: by decreasing the gate voltage, the depletion width is gradually reduced, and the current in the behavior increases (Fig.4.3). If a gate voltage smaller than the flat band one is applied, an accumulation layer is expected to be observed. By simulating for $V_g = -1V$, the surface concentration in Fig.4.12 is obtained.

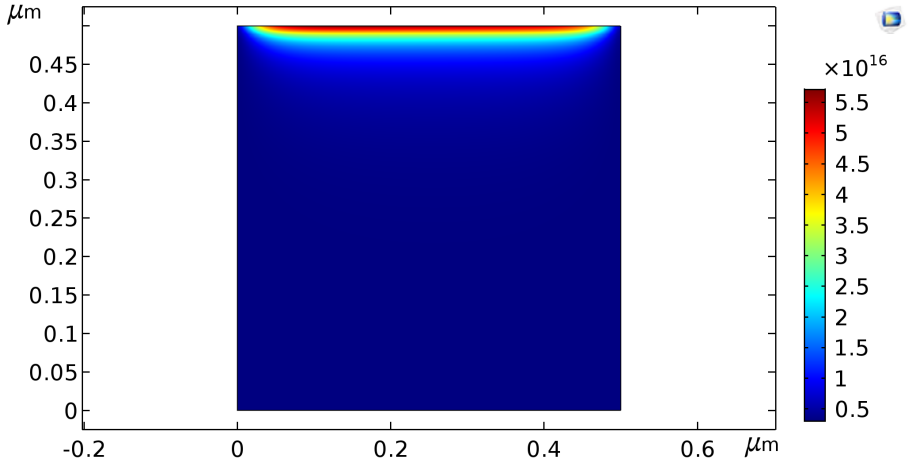

Figure 4.12: Hole surface concentration for $V_g = -1V$.

Clearly an accumulation of holes at the oxide/semiconductor surface is present. On the basis of the obtained results it is therefore possible to understand the I_s/V_g curve behavior: the characteristics is approximately linear when the device is in partial depletion, while it starts to be less linear (Fig.4.3) when an accumulation layer is formed in the device layer. This makes sense since many holes are attracted and accumulated in a very small region.
It is important to remark that the selected device layer thickness ($500nm$) is only $30nm$ less than the maximum analytical depletion width ($530nm$). If, for the same

doping concentration, the device layer thickness is reduced to $300nm$, the full depletion is surely ensured for the same gate voltage ($V_g = 0V$) as observed in Fig.4.13.

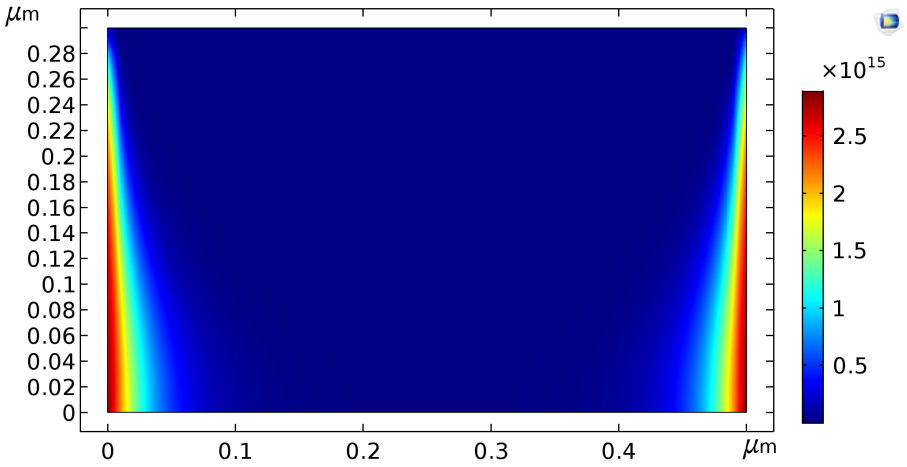

Figure 4.13: Hole surface concentration for $V_g = 0V$ and $T_{Si} = 300nm$.

4.2.2 I_s vs V_s

In order to observe the device output characteristics, a simulation for different gate voltages was carried out, by sweeping the source voltage in the range $[-6V, 0V]$, thus the current is expected to be negative since the source is at negative potential. The output characteristics is shown in Fig.4.14.

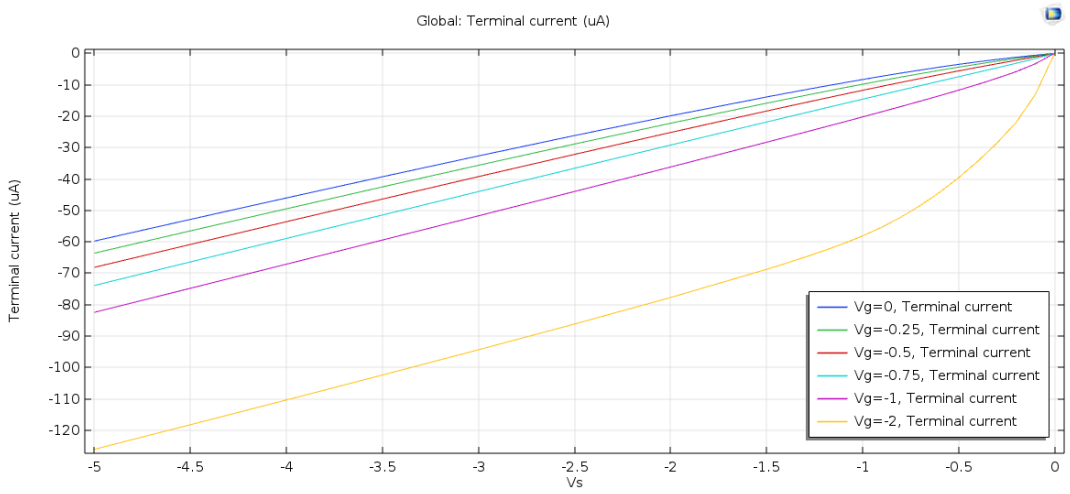

Figure 4.14: I_s/V_s for different gate voltages.

As can be observed the curve resembles the typical MOSFET output characteristics, thus confirming the expected device behavior. In Fig.4.15 the simulation for $V_g = -1V$ is depicted. The linear region is very limited, as well as the triode, and the channel modulation effect is observed, since instead of being flat the curve has a linear behavior in the saturation region.

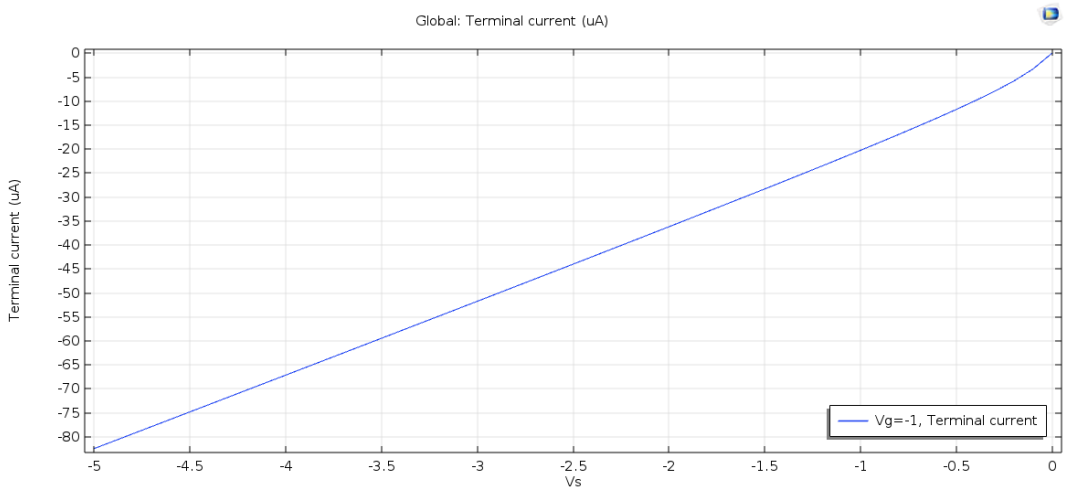

Figure 4.15: I_s/V_s for $V_g = -1V$.

In Fig.4.16 the simulation for $V_g = -2V$ is depicted. In this case it is possible to better distinguish the linear and triode region. The current is higher, since for $V_g = -2V$ many holes are attracted in the accumulation layer.

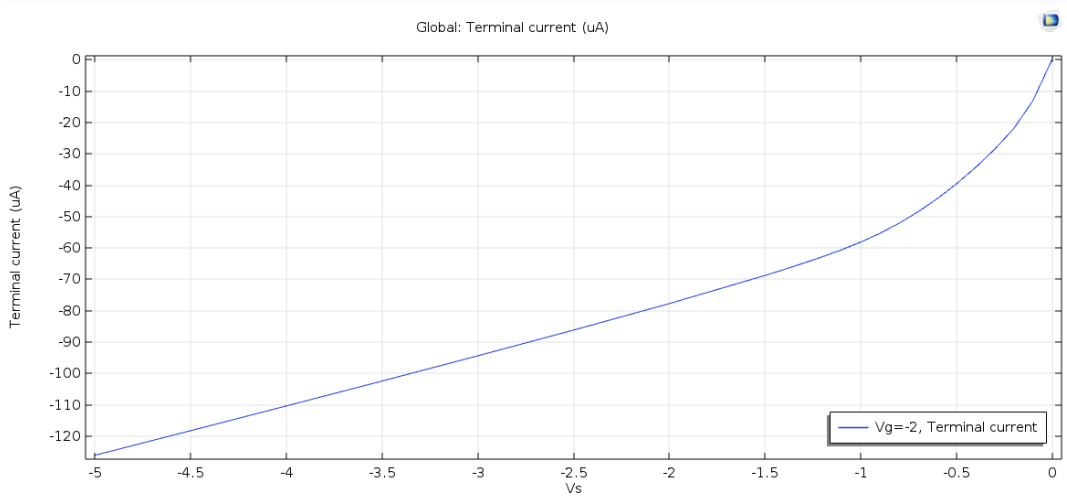

Figure 4.16: I_s/V_s for $V_g = -2V$.

Thus a junctionless transistors has an output characteristics similar to that of inversion mode devices, in the sense that the linear, triode, and saturation regions are present. But is important to remark that the principal of operation is quite different as explained in Sect.2.2. The simulations results therefore confirmed the expected behavior of the device.

Chapter 5

Conclusion

In this thesis a planar single gate junctionless transistor over FD-SOI wafer is proposed as a simple and cost effective solution with respect to conventional MOSFETs. The achieved results are the following ones:

- a paper review about junctionless transistors was written with the aim of providing an updated state of the art of such devices; a classification of the transistors was proposed as well as a critical comparison in terms of performance engineering;
- a p-type junctionless transistor was designed according to the given specifications. It is a low voltage electronic device, and its operating range is of $1V$;
- a low cost fabrication process compatible with the available equipment in the facility was proposed; the transistor does not require any implantation steps, thus lowering the process cost and complexity;
- simulations of the transistor were carried out, confirming the expected device behavior. Moreover a extraction method for the flat band voltage was proposed;
- a journal article was written to provide a method for the determination of the depletion width boundary in junctionless transistors. The curves obtained by means of the proposed algorithm fit the analytical ones.

Appendix A

MATLAB Codes

A.1 Maximum Depletion Width

MATLAB implementation of the maximum depletion width as a function of the doping concentration.

```
%% Device Layer Thickness as a function of the Doping Concentration

q  = 1.602e-19;     %[C]
k  = 8.6173303e-5;  %[eV/K]
T  = 293.15;        %[K]
Vt = k*T;           %[V]

eps0  = 8.854e-14;  %[F/cm]
epsSi = 11.7;
eps   = epsSi*eps0; %[F/cm]

ni = 5.29e19*(T/300)^2.54*exp(-6726/T); %[cm^-3]
Nd = linspace(1e15, 1e17, 1000);        %[cm^-3]
Phi_n = Vt*log(Nd/ni);

Xdep = sqrt((4*eps*Phi_n)./(q*Nd)); %[cm]
Xdep = Xdep*1e7;                    %[nm]

figure(1)
plot(Nd,Tdep, 'k')
axis([min(Nd) max(Nd) min(Xdep) max(Xdep)])
ylabel('X_{dep} [nm]')
xlabel('Nd [cm^{-3}]')
grid on
```

A.2 Mobility Estimation

MATLAB implementation of the algorithm for the estimation of the mobility.

```
1
2  %% Wafer doping estimation
3
4  q  = 1.602e-19;%[C]
5
6  muh = 450;      %[cm^2/Vs]
7  mu_maxh = 495;  %[cm^2/Vs]
8  mu_minh = 47.7; %[cm^2/Vs]
9  alphah = 0.76;  %Fitting paramter
10 Nrefh = 6.3e16; %[cm-3]
11
12 %% BSOI wafer
13
14 rho_OKMETIC_B_1_max = 5;  %[Ohmcm]
15 Na_OKMETIC_B_1_max = 1/(q*muh*rho_OKMETIC_B_1_max);
16
17 mun_OKMETIC_B_1_max = mu_minh+(mu_maxh-mu_minh)/(1+(
       Na_OKMETIC_B_1_max/Nrefh)^alphah);
18
19 diff_OKMETIC_B_1_max = muh-mun_OKMETIC_B_1_max;
20
21 while(abs(diff_OKMETIC_B_1_max)>0.1)
22 muh = mun_OKMETIC_B_1_max;
23 Na_OKMETIC_B_1_max = 1/(q*muh*rho_OKMETIC_B_1_max);
24 mun_OKMETIC_B_1_max = mu_minh+(mu_maxh-mu_minh)/(1+(
       Na_OKMETIC_B_1_max/Nrefh)^alphah);
25 diff_OKMETIC_B_1_max = mun_OKMETIC_B_1_max-muh;
26 end
27
28 fprintf('->OKMETIC 1 BSOI:\n')
29 disp(['Maximum:  ' num2str(Na_OKMETIC_B_1_max,'%10.2e') ' cm-3 ']);
```

A.3 Resistivity Measurement

MATLAB code for the computation of the wafers resistivities, measured through a four probe collinear method.

```
%% Resistivity computation

t = 2e-3; %Device Layer:  20um  [cm]
D = 10;   %Diameter:      100mm [cm]
s = 0.1;  %Probe Spacing: 1mm   [cm]

%% Measured resistances

RL_values = [450,500,520];
RL = mean(RL_values);

RC_values = [450,550,650];
RC = mean(RC_values);

RR_values = [550,650,700];
RR = mean(RR_values);

%% Correction Factors

F1 = (t/s)/(2*log(sinh(t/s)/sinh(t/(2*s))));  % Non conducting bottom
    surface
F2 = log(2)/(log(2)+log(((D/s)^2+3)/((D/s)^2-3)));

F=F1*F2;

%% Resistivity

rhoL=2*pi*s*RL*F;
rhoC=2*pi*s*RC*F;
rhoR=2*pi*s*RR*F;

%% Display

fprintf('->Resistivities:\n')
disp(['RhoL =  ' num2str(rhoL) ' ohm-cm ']);
disp(['RhoC =  ' num2str(rhoC) ' ohm-cm ']);
disp(['RhoR =  ' num2str(rhoR) ' ohm-cm ']);
```

A.4 Parasitic resistance analysis

MATLAB code for the computation of parasitic resistance R_sub.

```
1
2  %% Parasitic resistance R_sub
3
4  W = 5e-4;                  %Width 5um           [cm]
5  Res = 5e-5;                %Minimum resolution [cm]
6  resistivity = 4.44;        %Reistivity         [ohm-cm] -> L=4.44, C
       =4.98, R=5.74
7  Tsi = 5e-5;                %Silicon thickness   [nm]    -> L=510 , C
       =540, R=580
8
9
10 %% Fixed W, variable separation distance d
11 d = linspace(5e-4, 10e-4, 1000); %S/D-G separation [cm]
12 R = resistivity*d/(W*Tsi);       %Rsub             [Ohm]
13
14 figure(1)
15 hold on
16 grid on
17 plot(d*1e4, R, 'k')
18 xlabel('Distance d [\mu m]')
19 ylabel('Resistance R_{sub} [\Omega]')
20 xlim([5 10])
21
22 %% Fixed d, variable width W
23 W = linspace(5e-4,10e-4,1000);
24 d = 5e-4;
25 R = resistivity*d./(W*Tsi);
26
27 figure(2)
28 plot(W.*1e4, R,'k')
29 grid on
30 xlabel('Width W [\mum]')
31 ylabel('Resistance  R_{sub} [\Omega]')
32 xlim([5 10])
```

A.5 Diffusion Modelling

MATLAB code for the estimation of the diffusion profile.

```
1
2  %% Diffusion Model
3
4  Nb = 1e15;                          %background concentration
5  xj = 6e-5;                          %junction depth = Tsi
6  x  = linspace(0,6e-5,1000);
7
8  %% Diffusion coefficient Al
9
10 Ea =  3.46;                         %Activation Energy [eV] 3.47
11 k  = 8.617e-5;                      %Boltzmann [eV/K]
12 T  = 1300;                          %Temperature [K]
13 D  = D0*exp(-Ea./(k*T));            %Diffusion Coefficient[cm-2/s]
14 D0 =  8;                            %[cm-2/s]
15 t=1*3600;                           %time [s]
16
17 %% Aluminum parameters
18
19 Avogadro = 6.02e23;                 %[mol^-1]
20 molar_mass_Al = 26.981539;          %[g/mol]
21 density_Al = 2.7;                   %[g/cm-3]
22 T_Al = 2e-6;                        %Thickness deposition layer [cm]
23 N_Al = Avogadro*density_Al*T_Al/molar_mass_Al; %Dose [atoms/cm^3]
24
25 %% Concentration Profile
26 N = (N_Al./(sqrt(pi.*D.*t))).*exp(-(x./(2.*sqrt(D.*t))).^2);
27
28 figure(1)
29 plot(x.*1e7,N,'k')
30 grid on
31 hold on
32 xlabel('Distance from surface (nm)')
33 ylabel('Concentration N (cm^{-3})')
34 line([0 xj],[Nb Nb]) %it is too low, that is the diffused layer
      doping concentration is always higher of Nb; added for sake of
      completness.
```

A.6 Flat Band Voltage

MATLAB code for the computation of the flat band voltage as a function of the doping concentration.

```
1
2  %% Flat Band voltage
3
4  q  = 1.602e-19;                          %[C]
5  k =  8.6173303e-5;                       %[eV/K]
6  T =  293.15;                             %[K]
7  Vt =  k*T;                               %[V]
8  ni = 5.29e19*(T/300)^2.54*exp(-6726/T); %[cm^-3]
9  Chi = 4.05;                              %Electron Affinity [eV]
10 Eg = 1.13;                               %Bandgap Si [eV]
11
12 %% Doping
13 Nd = linspace(1e15,1e16);
14 Na = linspace(1e15,1e16);
15
16 %% Gate work functions
17 Phi_Mp = 5.15;                    %p-type Gate workfunction [eV]
18 Phi_Mn = 4.05;                    %n-type Gate workfunction [eV]
19
20 %% Fermi potential
21 Phi_n =  Vt*log(Nd/ni);           %n-substrate Fermi Potential [eV]
22 Phi_p =  Vt*log(Na/ni);           %p-substrate Fermi Potential [eV]
23
24 %% Semiconductor work function
25 Phi_sn = Chi + Eg/2 - Phi_n;      %n-substrate work function [eV]
26 Phi_sp = Chi + Eg/2 + Phi_p;      %p-substrate work function [eV]
27
28 %% Flat band voltage
29
30 Vfb_n_pgate = (Phi_Mp - Phi_sn); %n-substrate Vfb & p-gate [V]
31 Vfb_n_ngate = (Phi_Mn - Phi_sn); %n-substrate Vfb & n-gate [V]
32
33 Vfb_p_pgate = (Phi_Mp - Phi_sp); %p-substrate Vfb & p-gate [V]
34 Vfb_p_ngate = (Phi_Mn - Phi_sp); %p-substrate Vfb & n-gate [V]
35
36 %% Plot
37
38 figure(1)
39 subplot(1,2,1)
40 plot(Nd, Vfb_n_pgate,'k')
41 title(['NMOS, p-gate \Phi_M= ' num2str(Phi_Mp) 'eV'])
42 xlabel('N_{D} (cm-3)')
43 ylabel('V_{FB} (V)')
44 xlim([Nd(1) Nd(end)])
```

```
45 grid on
46
47 subplot(1,2,2)
48 plot(Nd, Vfb_n_ngate,'k')
49 title(['NMOS, n-gate \Phi_M= ' num2str(Phi_Mn) 'eV'])
50 xlabel('N_{D} (cm-3)')
51 ylabel('V_{FB} (V)')
52 xlim([Nd(1) Nd(end)])
53 grid on
54
55 figure(2)
56 subplot(1,2,1)
57 plot(Na, Vfb_p_pgate,'k')
58 title(['PMOS, p-gate \Phi_M= ' num2str(Phi_Mp) 'eV'])
59 xlabel('N_{A} (cm-3)')
60 ylabel('V_{FB} (V)')
61 xlim([Na(1) Na(end)])
62 grid on
63
64 subplot(1,2,2)
65 plot(Na, Vfb_p_ngate,'k')
66 title(['PMOS, n-gate \Phi_M= ' num2str(Phi_Mn) 'eV'])
67 xlabel('N_{A} (cm-3)')
68 ylabel('V_{FB} (V)')
69 xlim([Na(1) Na(end)])
70 grid on
```

A.7 Analytical Threshold Voltage

MATLAB code for the computation of the threshold voltage as a function of the doping concentration.

```
1
2
3  %% Threshold Voltage
4
5  q  = 1.602e-19;                          %[C]
6  k =  8.6173303e-5;                       %[eV/K]
7  T =  293.15;                             %[K]
8  Vt =  k*T;                               %[V]
9  ni = 5.29e19*(T/300)^2.54*exp(-6726/T); %[cm^-3]
10 Chi = 4.05;                              %Electron Affinity [eV]
11 Eg = 1.13;                               %Bandgap Si [eV]
12 Nd = linspace(1e15,1e16);
13 Na = linspace(1e15,1e16);
14 Tsi= 3e-5;                               %Device layer thickness [cm]
15 Phi_M = 4.1;                             %Gate workfunction (Al) [eV]
16 Phi_n = Vt*log(Nd./ni);                  %Fermi Potential [eV]
17 Phi_p = Vt*log(Na./ni);
18 Phi_sn = Chi + Eg/2 - Phi_n;             %Semicon. work function [eV]
19 Phi_sp = Chi + Eg/2 + Phi_p;
20 Vfb = (Phi_M - Phi_sn);                  %Flatband voltage [V]
21 Vfb_p = (Phi_M - Phi_sp);
22 eps0  = 8.854187e-14;                    %[F/cm]
23 epsSi = 11.7*eps0;
24 epsox = 3.9*eps0;
25 Tox   = 10e-7;                %Oxide thickness   [cm]
26 Cox = epsox/Tox;              %Oxide capacitance [F/cm^2]
27
28 %% Vth
29
30 Vth=Vfb+q.*Nd./(2*epsSi)*((epsSi/Cox)^2-(Tsi+epsSi/Cox)^2);
31 Vth_p=Vfb_p-q.*Na/(2*epsSi)*((epsSi/Cox)^2-(Tsi+epsSi/Cox)^2);
32
33 figure(1)
34 plot(Nd, Vth,'k')
35 xlabel('N_{D} (cm-3)')
36 ylabel('V_{th} (V)')
37 xlim([Nd(1) Nd(end)])
38 grid on
39 figure(2)
40 plot(Na, Vth_p,'k')
41 xlabel('N_{A} (cm-3)')
42 ylabel('V_{th} (V)')
43 xlim([Na(1) Na(end)])
44 grid on
```

A.8 Extracted Threshold Voltage

MATLAB code for the extraction of the threshold voltage with the ELR method.

```
%% Is Vg analysis

Vs=0.01; %[V]

%% 500nm p-type junctionless transistor

infile = 'isvg.txt';
data1 = load(infile, '-ascii');
x1 = data1(:,1);
y1 = data1(:,2);

slope1 = diff(y1)./diff(x1);
x01 = x1(slope1==min(slope1));
y01 = y1(x1==x01);
z1=min(slope1)*(x1-x01)+y01;

Vth1=interp1(z1,x1,0)-Vs/2;

figure(1)
plot(x1,z1,'k--')
xlabel('V_{g} (V)')
ylabel('I_{s} (\mu A)')
hold on
grid on
plot(x1,y1,'k')
xlim([x1(end) x1(1)])
ylim([y1(1) y1(end)])

dyy=diff(y1)./diff(x1); %transconductance [muA/V]
x1=x1(1:end-1);         %using diff removes one element in the array

figure(2)
sloper = diff(dyy)./diff(x1);
x01r = x1(sloper==max(sloper));
y01r = dyy(x1==x01r);
z1r=max(sloper)*(x1-x01r)+y01r;

L1r(1,:)=x1;
L1r(2,:)=z1r;
L2r(1,:)=x1;
L2r(2,:)=dyy;
Par = InterX(L1r,L2r);
plot(x1,dyy,'k')
hold on
```

```
46 plot(x1,z1r,'k--')
47 plot(Par(1,2),Par(2,2),'k*')
48 grid on
49 xlabel('V_{gs} (V)')
50 ylabel('g_{m} (\mu A/V)')
51 xlim([x1(end) x1(1)])
52 ylim([-1.5 max(dyy)])
```

Appendix B

Papers

Two papers were written for this master thesis:

- *Analysis and Classification of Junctionless Transistors: a Paper Review.*
- *A Numerical Method to Extract the Depletion Region Width of Planar Junctionless Transistors.*

B.1 Analysis and Classification of Junctionless Transistors: a Paper Review

MDPI

Review

Analysis and Classification of Junctionless Transistors: a Paper Review

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Abstract: Recent advances in semiconductor technology brought researchers all over the world to face the problem of integrating transistors, down to the nanometer scale. One of the most promising solution, to overcome this technological issue, consists in realizing junctionless transistors. After 2010, when the first junctionless device was fabricated and proved to be functional, many other transistors of this kind have been proposed and investigated, such as FinFET, gate all around, planar, and tunnel-FET. All of these semiconductor devices present the same function and principle of operation, but they differ from each other when considering the influence of technological parameters on the performance. After a deep investigation of the current literature of junctionless transistors we noticed that a proper classification of the latest junctionless semiconductor devices was missing. Therefore, the aim of this paper review is to provide a simple but complete classification of junctionless transistors, which were proposed in the last decade. The criteria utilized for our classification are based on geometrical structure, analytical model and electrical characteristics of the electronic devices. Finally, by using the performance figure of merits (Ion/Ioff, DIBL, SS), we have discussed advantages and disadvantages of each category of junctionless transistors. Overall, the paper aims to provide a better understanding about this technology.

Keywords: Junctionless; Review; Transistor; Nanowire; Double Gate; Gate All Around; FinFET; Thin Film.

1. Introduction

The junctionless transistor (JLT) concept was introduced for the first time by J.E. Lilienfeld in 20*s* [1], since he proposed a device characterized by the absence of pn junctions. The operating principle of such device resembles the one of modern transistors: by applying a voltage to the gate terminal, the device resistivity can be modulated, and consequently the current between the other two terminals controlled. But at the beginning of the 20th century the technology did not allow to realize such transistor, since in order to work very thin films (nanometer regime) and high doping concentrations ($\sim 1e19cm^{-3}$) are needed. Hence it tooks more than 80 years to realize the first junctionless transistor [2]: a nanowire characterized by the absence of any doping gradients, fabricated at the Tyndall Institute by Colinge et al., that turned out to be the first device of a new generation of transistors. In fact after its realization many others were proposed such as: FinFETs [3–23], Gate-All-Around (GAAFETs) [24–37], planar (PJLT) [38–49], double gate (DGJLT) [50–73], thin-film-FETs (TFT) [74–84], and tunnel-FETs (TFET) [85–95]. Although these devices share the same operating principle and are all defined as junctionless transistors, they are very different in terms of structure, performance, and optimization techniques one from each other. It is therefore difficult for readers interested in the understanding of

such devices to have a complete overview of this family of transistors. Moreover most of the paper reviews about junctionless transistors in the scientific literature were written in 2010-2014 [96–100], thus not providing a complete classification on the basis of the latest developments. Therefore in this paper we provide a critical classification and analysis of such devices in terms of structure engineering and performance comparison. The work is organized as follows: in Sect.2 a classification of the devices is proposed; in Sect.3.1 the junctionless nanowire transistor is analyzed, since it is the first ever fabricated device. Next in Sect.3.2 FinFETs are reported, since their structure is the more similar to that of nanowires, while in Sect.3.3 GAAFETs are analyzed. Then planar junctionless transistors (Sect.3.4) and thin-film transistors (Sect.3.5) are described, followed by double gate (Sect.3.6) and tunnelFETs (Sect.3.7), which share a similar gate structure. Finally in Sect.4, the conclusions are reported.

2. Classification

The main difference among the various junctionless transistors relies on the structure of the device layer, that is they can be distinguished depending on the geometrical shape of their channel. For instance if the channel of a junctionless transistor is a fin, then it is defined as a junctionless FinFET. But in the scientific literature, JLTs are distinguished also on the basis of material composition or gate structure: a planar junctionless transistor with a thin channel made of polysilicon instead of silicon is referred as thin film transistor, and not as planar junctionless transistor. The same reasoning applies when considering gate-all-around structures, in the sense that both a nanowire and a FinFET can be considered as GAAFETs, if their channel (whatever the shape) is entirely surrounded by the gate. Therefore in order to provide a a well defined classification of junctionless transistors, we analyzed a total of 118 papers and we divided them on the basis of the name that is given by the authors of each paper to the device under analysis. The obtained distribution, shown in Fig.1, suggests the main categories in which junctionless transistors can be distinguished, while in Fig.2 the analyzed scientific literature is divided on the basis of the proposed classification.

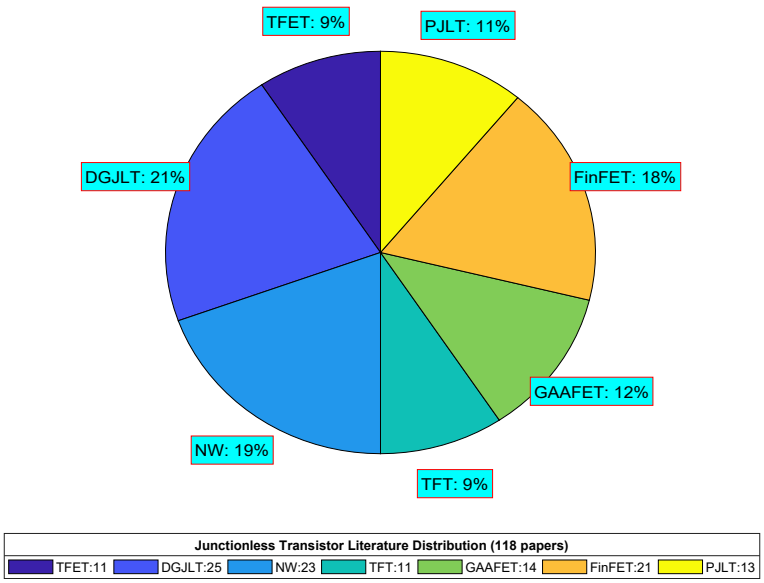

Figure 1. Junctionless transistor literature distribution analyzed in this work.

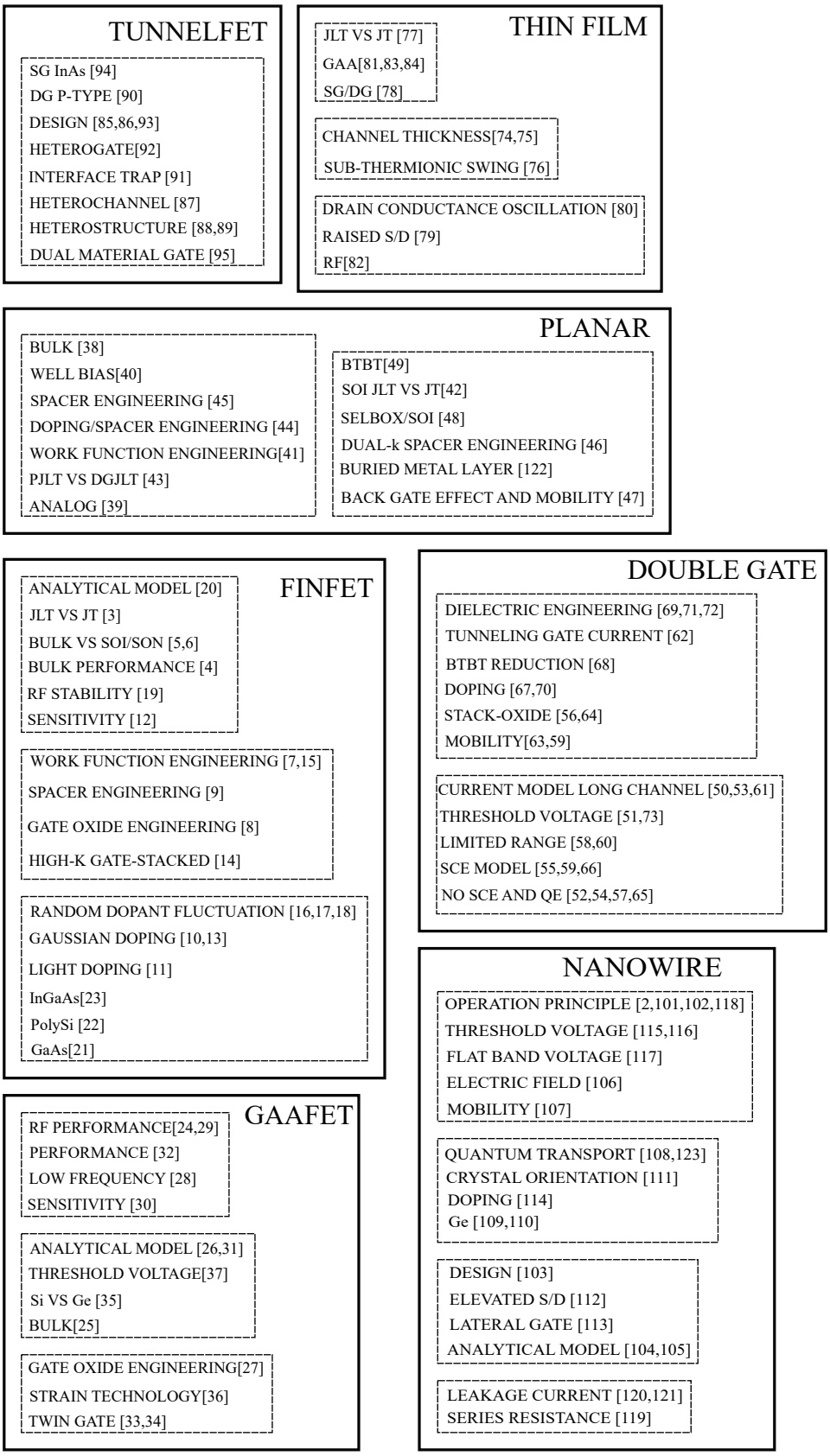

Figure 2. Graphical representation of the distribution of analyzed scientific literature.

3. Analysis

3.1. Nanowire

In 2010 J.P. Colinge et al. fabricated the first junctionless transistor (Fig.3(a)) at the Tyndall National Institute (Ireland): a heavily doped nanowire with a silicon thickness of $10nm$ and and a channel length of $1\mu m$ [2]. The fabrication process did not require any implantation step for the source and the drain [101], therefore no gradient doping concentrations are present, resulting in a lower thermal budget process as compared to conventional junction transistor fabrication process. But on the other hand a high doping concentration ($\geq 1e19cm^{-3}$) is needed to obtain an appreciable current in the ON state, while the thickness of the device layer has to be thin enough to ensure full depletion in the OFF state [102]. The output characteristics (I_D/V_D) is shown in Fig.3(b), and it resembles the typical MOSFET curve, but the conduction mechanism is quite different.

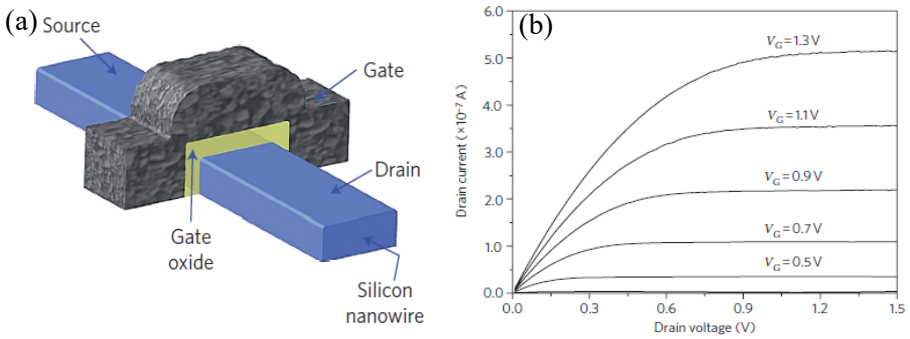

Figure 3. (a) Structure of the junctionless nanowire fabricated by Colinge. The buried oxide below the silicon nanowire is not shown. (b) Drain current as a function of the drain voltage for different gate voltages of the Colinge n-type junctionless nanowire [2].

In fact junctionless transistors do not behave as inversion mode devices [103], since the threshold voltage is defined as the gate voltage that fully depletes (OFF state) the device layer (Fig. 4(b3)). Thus they are more similar to accumulation mode devices (Fig.4(b2)) in terms of threshold voltage definition; also from an analytical point of view they can be modelled starting from accumulation mode device descriptions [104,105], since the current flowing in the device can be decomposed in two components: a bulk and an accumulation current. In fact when the gate voltage is greater than the threshold one, partial depletion takes place creating a path in the substrate for the bulk current. As the gate voltage overcomes the flat band one the whole channel becomes conductive (ON state) [102], and an accumulation current is formed at the semiconductor/insulator interface and added to the bulk one. In Fig.4(a) the electron concentration above the threshold voltage is depicted: conductive channels at the semiconductor/insulator interface are present in accumulation and inversion mode devices, while in junctionless transistors the conductive channel is in the bulk.

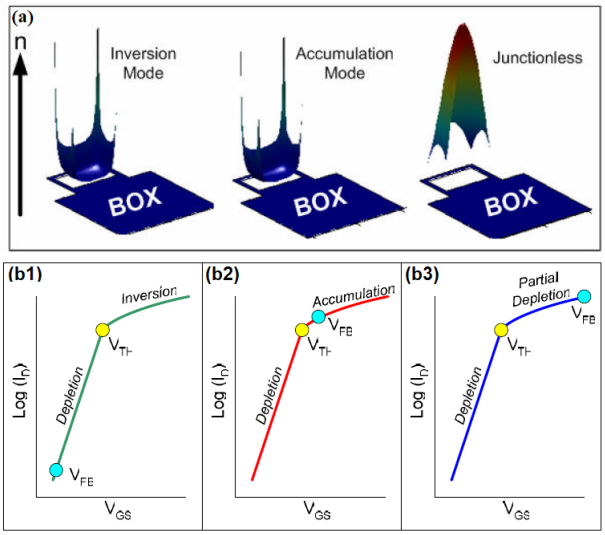

Figure 4. (a) Electron concentration for inversion mode (IM), accumulation mode (AM), and junctionless transistors above threshold voltage. (b) Current behavior in IM (b1), AM (b2), and junctionless transistors (b3) [103].

Another important difference with respect to accumulation and inversion mode devices is the electric field behavior in the device layer [106]: in inversion (and accumulation) mode devices most of the carriers at the semiconductor/insulator interface are localized in high electric field regions, and this is due to the gate attraction. But in junctionless transistors the peak of the electron concentration is instead localized in region of lowest electric field, thus implying higher mobility. An enhanced mobility in junctionless nanowire is also due to the reduction of the scattered impurities caused by an overall smaller charge of ionized impurities [107]. Since the junctionless nanowire conduction mechanism is localized in the middle of the channel, quantum confinement could take places [76]: in [108] the $1D$ transport through two subbands is analyzed; the nanowire, for low drain voltages, showed a quantized drain current and step-like transconductance (Fig.5(c)). In [76] instead the doping concentration effect on the quantum transport is analyzed: by decreasing the doping concentration from $1e19cm^{-3}$ to $2e18cm^{-3}$ a threshold voltage fluctuation from $0V$ to $0.6V$ is observed, and this is attributed to the higher ionization ratio in heavily doped nanowires, that is because of higher doping concentration the conduction path is filled by many quantum dots, resulting in a larger statistical variation (Fig.5(a)).

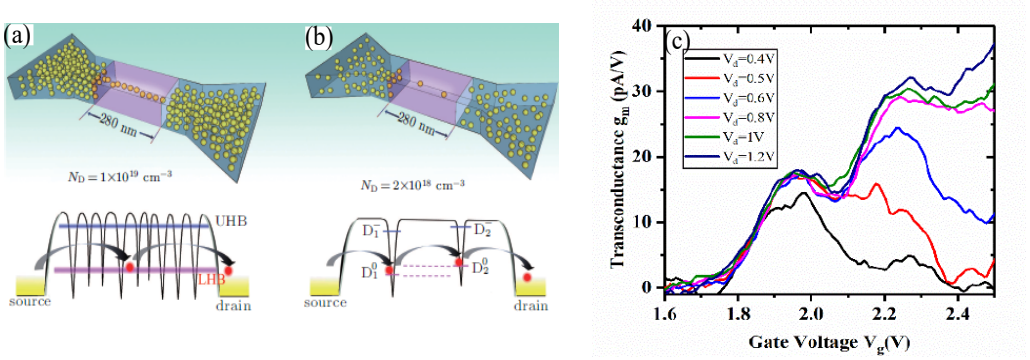

Figure 5. (a) Nanowire doped with $1e19cm^{-3}$ and possible potential distribution [76]. (b) Nanowire doped with $2e18cm^{-3}$ and possible potential distribution [76]. (c) Step-like transconductance behavior [108].

An analysis in the ballistic transport regime is provided also in [109], where junctionless nanowire are investigated in terms of crystal orientations and material channel (germanium and silicon) and

compared to inversion mode nanowires: the junctionless nanowire resulted to be less sensitive to short channel effects, presenting smaller SS, reduced DIBL, and higher I_{on}/I_{off} ratio. Germanium nanowire along the $\langle 110 \rangle$ direction on (010) wafers results to be slightly more sensitive than silicon to short channel effects, but on the other hand it presents competitive electrostatic control [110]. In the case in which, instead, silicon nanowire along the $\langle 100 \rangle$ direction are built on (100) wafers, a degradation of the performance was measured [111]. The performance is also dependent on the transistor structure: in [112] a nanowire with elevated source and drain is reported; the device allows a higher current to flow in the device in the ON state. In [113] instead a lateral gate structure is presented, which besides having a high SS provides a high I_{on} current. The comparison in terms of SS and I_{on}/I_{off} for the reported junctionless nanowire is reported in Tab.1.

Table 1. Reported SS and I_{on}/I_{off} values for different junctionless nanowire transistors.

Nanowire	$\mathbf{T_{Si}}$ (nm)	$\mathbf{L_g}$ (nm)	**W** (nm)	$\mathbf{N_D}$ (cm^{-3})	$\frac{\mathbf{I_{on}}}{\mathbf{I_{off}}}$	**SS** (mV/dec)	**Ref.**
Trigate	10	1000	30	$> 1e19$	$> 1e6$	~ 60	[2]
Trigate	7	25	-	$1e18$	-	79.8	[114]
Lateral Gate	100	100	95	-	$2e6$	160	[113]
Elevated S/D	100	130	-	-	$> 1e6$	200	[112]

Regarding the threshold and flat band voltages, they are of critical importance, since they determine the operating range of the device [2]. In [115] the threshold voltage is analytically modelled and defined as the gate voltage at which the curve g_m/I_D (where g_m is the transconductance) drops at half of its maximum value, while the same author in [116] analyzes its behavior in terms of different parameters: the threshold voltage increases (in absolute value) with increasing doping, while decreases with increasing gate oxide thickness, nanowire width and length. An analysis of the doping concentration influence on the threshold voltage is also reported by [114]: by increasing the doping concentration from $1e14cm^{-3}$ to $1e18cm^{-3}$ the threshold voltage decreases from $0.455V$ to $0.37V$; this is attributed to the fact that the higher the doping concentration and the stronger the field needed for the carrier depletion. The flat band voltage, instead, is analyzed in [117] by studying the dg_m/dV_g characteristics as a function of the temperature: it decreases by $0.6mV/K$ as the temperature increases from $50K$ to $350K$. A similar ($0.5mV/K$) behavior is observed for the threshold voltage too. For lower temperature ($4.2K$), an analysis is reported in [118], where it is explained that for high doping concentration ($1e19cm^{-3}$) and low temperature, the thermal energy is not strong enough to ionize all the dopants, resulting in an incomplete ionization that in the source and drain regions causes an increment of the series resistance which in terms reduces the current. Therefore if junctionless nanowire transistors present a reduction of short channel effects compared to inversion mode devices, on the other hand they are highly sensitive to the series resistance, which was modelled in [119]: they considered the total resistance as a sum of the channel resistance R_c and parasitic resistances R on the source and drain sides (Fig.6(a)); by simulating a nanowire with channel length of $100nm$ and doping concentration $1e19cm^{-3}$ the computed an intrinsic source/drain resistance of $5.5k\Omega$. Decreasing the doping to $5e18cm^{-3}$, the resistance reached a value of $11k\Omega$. As shown in Fig.6(b) this can be critical, since the current can be decreased by one order of magnitude. The performance of junctionless nanowire transistors can also be affected by current leakages [120,121] associated to gate tunneling, with the latter being directly proportional both to the length and width of the transistor (so to the gate area), and to the temperature.

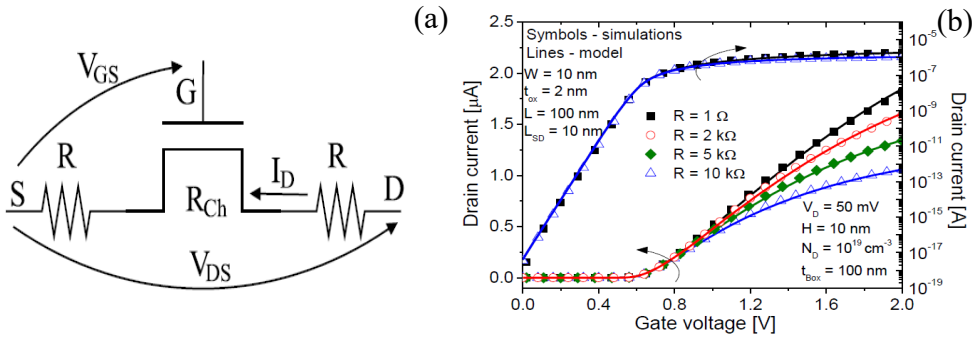

Figure 6. (a) Junctionless nanowire resistance model representation. (b) Current behavior as a function of the gate voltage of a 100nm junctionless nanowire transistor for different series resistances [119].

3.2. FinFET

The structure of a bulk junctionless FinFET is shown in Fig.7, and the design of the depicted geometrical parameters could strongly affect the transistor performance: increasing the fin width W (shown in Fig.7) from 6nm to 15nm can lead to a variation of approximately 60% and 42% for $DIBL$ and SS respectively, while changing the gate length L_g from 12nm to 21nm can lead to a variation of approximately 52% and 14% for $DIBL$ and SS respectively [12]; variation in the fin height H are instead more critical in terms of analog parameters [19]. The junctionless FinFET presents lower I_{off} with respect to the inversion mode counterpart, because of the low carrier concentration and high electric field in the OFF state, while with respect to SOI FinFETs it presents an additional degree of freedom in the design, that is by varying the doping concentration of the substrate from $1e18cm^{-3}$ to $1e19cm^{-3}$, a change of 30% in the threshold voltage can be obtained [4]. Furthermore it also provides lower SS and $DIBL$ with respect to SOI FinFETs (which can be modelled starting from conventional triple gate structures [20], although with respect to the latter a difference in performance is observed [3]) and SOI nanowires (Tab.2) [5,6]. But the lowest SS and $DIBL$ are observed for the SON (silicon on nothing) FinFET, in which the silicon layer is isolated from the substrate through the selective lateral etching of $SiGe$ that is sandwiched between the two silicon layers, thus implying a more complex fabrication process with respect to bulk structures [5].

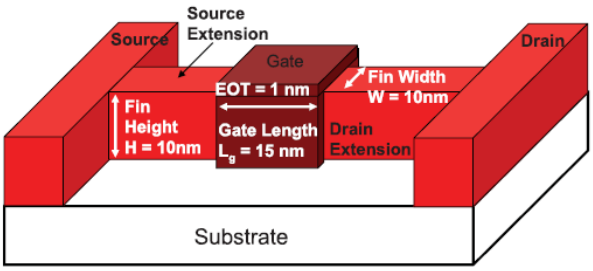

Figure 7. Bulk FinFET structure [4].

In order to optimize junctionless FinFETs different approaches can be followed: gate work function engineering, to reduce I_{off} (by changing the work function from $4.5eV$ to $5.4eV$ I_{off} can be reduced by five order of magnitudes) [7]; spacer engineering, to improve performance (e.g. an optimal design can provide an improvement in I_{on} of the 72.5% and in $DIBL$ of 37.8%) [9]; doping engineering, by using a Gaussian doped channel (a different threshold voltage model it is required [13]), which can lead to an increase in I_{on} of 21.1% [10], or a lightly doped channel, which allows a better gate control on the device [11]; gate oxide engineering, to provide higher performance (in terms of I_{on}/I_{off} and $DIBL$) by the implementation of complex hetero gate oxide structures (e.g. the double hetero gate in Fig.8(a) allows to obtain a higher I_{on}/I_{off}, as shown in Fig.8(b), with respect to conventional and triple/quadruple hetero gate oxide structures) [8]. Besides the number of hetero gate oxides regions,

it is important to consider also their dielectric number: although for high values ($k = 40$) the $DIBL$ is reduced (Tab.2), the analog performance is degraded [14]. Regarding, instead, dual-k structures with intermediate values of the dielectric constant ($k = 22$, HfO_2), it was observed that they provide better figure of merits (Tab.2) with respect to those with low dielectric constant ($k = 3.9$, SiO_2) when considering random dopant fluctuation in the fin [16]. The latter is a critical phenomenon especially for junctionless FinFETs (when compared to conventional structures), since they are more likely to be affected by random dopant variability [17]; moreover random dopant fluctuations and work function variability are considered to be more dominant with device dimension scaling [18].
It is important to remark that the results reported for the junctionless FinFETs are not necessarily the same reported for other junctionless transistors: for instance both junctionless GAA (Gate-All-Around) nanowire and junctionless FinFET are slightly affected by variations in the work function in terms of SS , but the latter is more sensitive to such variations, in terms of threshold voltage, with respect to $GAAs$ transistors [15].

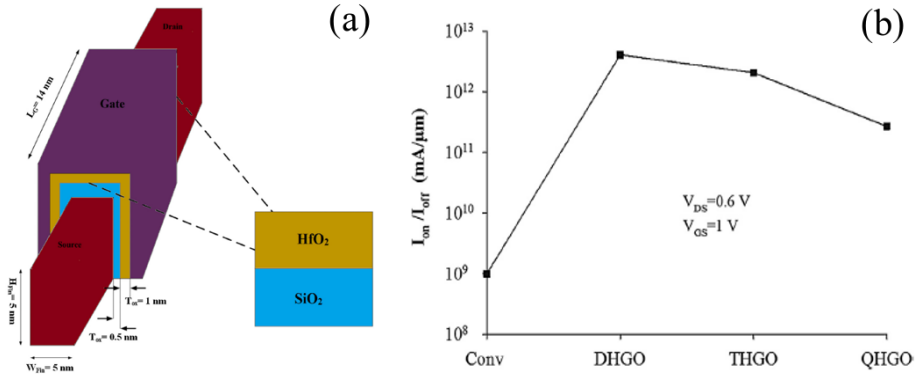

Figure 8. (a)Double hetero gate oxide FinFET structure. (b) I_{on}/I_{off} for different hetero gate oxide structures [8].

An important difference in terms of structure, with respect to nanowires, is that FinFETs were analyzed by considering different materials for the device layer: a FinFET made of polycrystalline silicon is reported as a cost-effective solution with respect to conventional devices made of silicon [22]. A $GaAs$ FinFET with an I_{off} of $1 \times 10^{-15} A$ compared to a Si FinFET with an I_{off} of $1 \times 10^{-8} A$ was proposed. The better performance was attributed to a higher potential difference and depletion of majority charge carriers in the channel [21]. Also more complex structures were reported, as an $InGaAs$ junctionless FinFET with alloyed Ni-$InGaAs$ source and drain [23]. The main figure of merits of the reported FinFETs are collected in Tab.2.

Table 2. Reported figure of merits of junctionless FinFETs.

FinFET	L_g (nm)	H (nm)	EOT (nm)	N_D (cm^{-3})	SS (mV/dec)	DIBL (mV/V)	$\frac{I_{ON}}{I_{OFF}}$	Ref.
Bulk	15	10	1	$1e19$	~ 65	~ 30	$\sim 1.2e5$	[6]
Bulk	15	10	1	$1.5e19$	~ 79	-	$2.9e7$	[7]
Bulk	15	10	1	$1e18$	78.27	95.48	-	[5]
SOI	15	10	1	$1e18$	~ 100	~ 40	-	[6]
SOI NW	15	10	1	$1e18$	87.3	121.65	-	[5]
SON	15	10	1	$1e18$	63.20	82.68	$1e5$	[5]
NO HGO	14	5	1.5	$5e19$	70	52	$1e9$	[8]
DHGO	14	5	1.5	$5e19$	64	20	$4.3e12$	[8]
THGO	14	5	1.5	$5e19$	64	20	$2.08e12$	[8]
QHGO	14	5	1.5	$5e19$	64	20	$2.7e11$	[8]
TG $k = 3.9$	5	6	-	$1e19$	61.5	20	-	[14]
TG $k = 40$	5	6	-	$1e19$	63.3	12.5	-	[14]
Dual $k = 3.9$	13	6.4	0.64	$1e19$	66.659	23	$\sim 1.3e8$	[16]
Dual $k = 22$	13	6.4	0.64	$1e19$	64.959	11	$\sim 2.7e8$	[16]
InGaAs	60	-	2.1	$1e19$	96	106	$5e5$	[23]

3.3. Gate All Around

The cross-sectional view of a conventional junctionless Gate-All-Around transistor is shown in Fig.9. The device, as the name suggests, is characterized by a channel entirely surrounded by the gate. Therefore solutions to the Poisson equations are more complex, since for such structures cylindrical coordinates have to be introduced [26,31]. Also GAAFETs with rectangular channels are reported, but with respect to those with cylindrical shape they present performance degradation because of corners effects [25]. An important parameter in the design of GAAFETs is the channel length: for a channel radius of $10nm$, as the channel length is reduced from $40nm$ to $16nm$ the $DIBL$ increases from $12mV/V$ to $123mV/V$, while the SS increases from $62mV/dec$ to $82mV/dec$ [29]. The channel radius, instead, determines the device speed: lower is and faster is its operation [26].

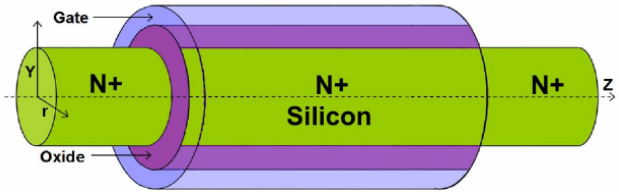

Figure 9. 3D structure of a cylindrical junctionless GAAFET [29].

With respect to inversion mode devices, junctionless GAAFETs present higher I_{on}/I_{off} ratio and less short channel effects [30]. But this is not true if the inversion mode device is considered to be low doped ($1e15cm^{-3}$) with respect to the junctionless one ($1e19cm^{-3}$): in fact while the inversion mode device is less sensitive, in term of transistor width variations, to roll-off voltage, SS, and $DIBL$, junctionless GAAFET because of the higher doping can presents, for a width of $24nm$ an SS greater than the $120mV/dec$ and a $DIBL$ of approximately $80mV/V$ greater [25]. Regarding the LFN (low-frequency noise), in junctionless GAAFETs is almost not sensitive to gate bias, doping concentration, or frequencies [28]. The gain and cutoff frequency, instead, were observed to be degraded by the hot carrier effect: in fact, a relative degradation of 15.44% for both the analog parameters was reported [32]. The analog performance can be optimized by adding source and drain extension (Fig.10): in fact a relative improvement of 92.6%, 66.6%, and 85.7% was reported for VIP_3, VIP_2, and IIP_3 respectively [24]. The structure depicted in Fig.9 can be further modified in order to increase the device performance: for instance a gate insulator made of hafnium oxide (HfO_2) instead of silicon oxide (SiO_2) can enhance parameters as $DIBL$; similarly to FinFETs, the SS could

be decreases and ratio I_{on}/I_{off} could be increased by considering gate oxides with high values of dielectric permittivity [27].

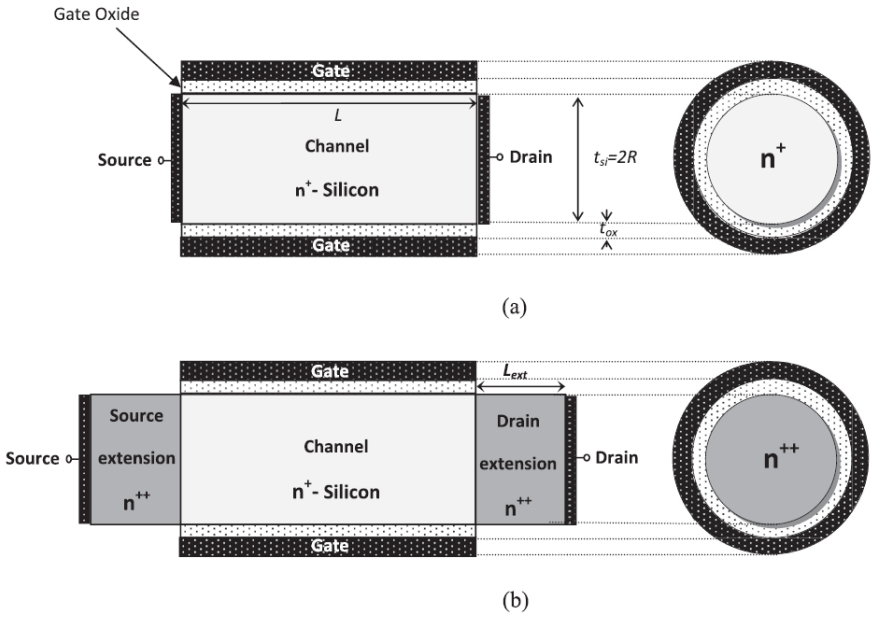

Figure 10. (a) Cross section of conventional cylindrical GAAFET. (b) Cross section of improved cylindrical GAAFET through addition of source and drain extensions. [24].

Besides engineering the gate oxide structures, it is possible to modify the numbers of gates that is considering two channels connected to the same source and drain (Fig.11 (a)). In this case the structure is defined as a twin gate transistor, where the two gates are separated by a dielectric (Fig.11(b)), and it allows to easily implement logic gates, since it presents two inputs instead of one (Fig.11(c)) [34]. The twin gate structure can also be applied to a double channel GAAFET, as shown in Fig.11(d), where the device layer is composed of polysilicon [33]; the fabricated device has a large I_{on}/I_{off} ratio (7*e*8), a $DIBL$ of $83mV/V$, and a SS of $105mV/V$. Besides polysilicon channel junctionless GAAFETs, also devices made composed of other materials were reported: a gallium arsenide junctionless GAAFET was simulated, leading an SS value near to the theoretical limit ($58.2mV/dec$ at $293.15K$) [27]. In [35] a comparison between germanium and silicon junctionless GAAFETs is presented: the germanium transistor has lower $DIBL$ and SS, but the silicon one has larger I_{on}/I_{off} ratio (data in Tab.3) [35]. The channel material composition is important also in terms of threshold voltage sensitivity to the temperature [37]: the threshold voltage decreases as the temperature increases; considering silicon, gallium arsenide, indium arsenide, and indium phosphide, the minimum and maximum threshold voltages were observed for indium arsenide and silicon, respectively.

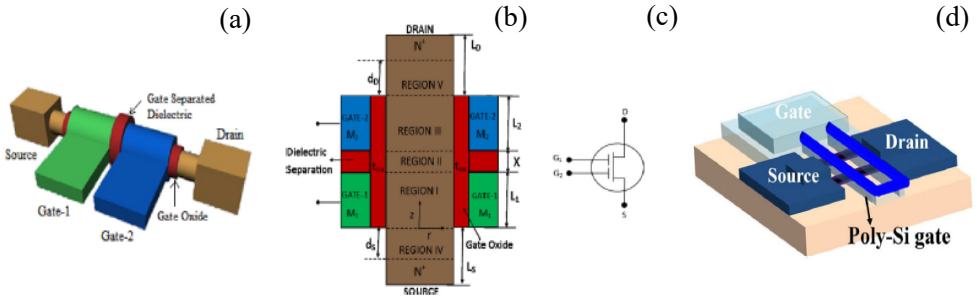

Figure 11. (a) Structure of a twin gate single channel GAAFET [34]. (b) Cross-sectional view of the device in Fig.11(a) [34]. (c) Circuit symbol of the device in Fig.11(a) [34]. (d) Structure of a twin gate double channel GAAFET [33].

In order to further increase the device performance, it is possible to use strain technology: in [36] a fabricated junctionless GAAFET is reported, which is strained through the deposition of SiN layer; the type of strain (compressive or tensile) depends on the SiN deposition conditions. The figures of merit of reported junctionless GAAFETs are collected in Tab.3.

Table 3. Reported figure of merits of junctionless GAAFETs.

GAA	L_{ch} (nm)	W_{ch} (nm)	N_D (cm^{-3})	SS (mV/dec)	$\frac{I_{on}}{I_{off}}$	Ref.
Bulk	-	21	1.5e19	70	-	[25]
Strained	-	20	-	65	$>$ 1e9	[36]
Si	20	10	2e19	70.94	4.3e5	[35]
Ge	20	10	2e19	67.88	5e5	[35]
PolySi	20	45	-	105	7e8	[33]

3.4. Planar

The bulk planar junctionless transistor is shown in Fig.12(a), and with respect to the *SOI* counterpart Fig.12(b) provides more control on the device characteristics because of the well doping and bias [38]. For instance, by positively biasing the well it is possible to improve the hot carrier effects and the I_{off} current although parameters as the threshold voltage decreases while $DIBL$ and SS increase: if the well bias is increased from $0V$ to $0.2V$, the $DIBL$ increases from $120mV/V$ to $140mV/V$ for a channel length of $20nm$; the degradation is even more relevant if the channel length is reduced to $10nm$ [40]. Regarding the well doping concentration, the lower is and the higher is the I_{on}; but a low I_{off}, instead, is obtained for low substrate doping. However the higher I_{on}/I_{off} is obtained for high doping concentration of the substrate [44]. On the other hand it has to be considered that if a bulk junctionless transistor has a physical thickness of $10nm$, the effective thickness is of $5nm$, because of the built-in junction potential [38]. But in terms of analog performance, it presents better (output) transconductance, output resistance, Early voltage, as well as intrinsic gain with respect to the *SOI* counterpart [39]. The planar junctionless transistor was observed to be more sensitive to the ratio T_{Si}/W_{Si}, and to provide a lower I_{on} as compared to the junction transistor; this is attributed to the highly doped channel which increase the scattering effect, thus lowering the mobility [42].

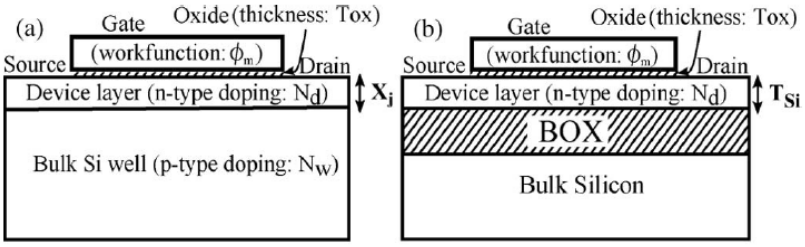

Figure 12. (a) Cross-sectional view of bulk planar junctionless transistor. (b) Cross-sectional view of SOI planar junctionless transistor [38].

To optimize the planar junctionless transistor more possibilities are available to the designers: gate work function engineering can lead to an improvement of 29% in the I_{on}/I_{off} ratio [41], while a non uniform doping (Gaussian) concentration through the device layer can reduce the I_{off} [43] although the planar junctionless transistor is more sensitive, with respect to the double gate structure, to the peak position of the non uniform doping profile; the comparison between planar and double gate in terms of uniform and non uniform doping concentration through the device layer thickness is reported in Tab.4.

Table 4. Comparison between planar and double junctionless transistor in terms of I_{off} for uniform ($N_D = 1e19cm^{-3}$) and non uniform doping concentration.

Structure	L_{ch} (nm)	T_{Si} (nm)	N_D (cm^{-3})	σ (nm)	I_{off} $(A/\mu m)$
Planar	20	10	uniform	0	2.16×10^{-4}
Double Gate	20	10	uniform	0	1.49×10^{-11}
Planar	20	10	non-uniform	6	1.31×10^{-9}
Double Gate	20	10	non-uniform	6	1.48×10^{-15}

As for FinFETS and GAAFETs, an improvement of the electrostatic characteristics of the transistor can be obtained through the implementation of high-k spacers (structure in Fig.13(a)): since junctionless transistors, with respect to conventional MOSFETs, have a higher vertical electric field in the *OFF* state and ideally zero electric field in the *ON* state, it is possible through to obtain an enhancement of the fringing electric fields, thus allowing, through the spacers, to deplete the device not only below the gate but also laterally. This implies an increment of the effective channel length which in terms improve the *SS* [45]. But this is not the only parameter that can be enhanced through the spacer implementation: the mobility, which is reduced with gate length scaling can be enhanced through S/D engineering [47], while a dual-k spacers structure could further reduce I_{off} and increase I_{on} [46].

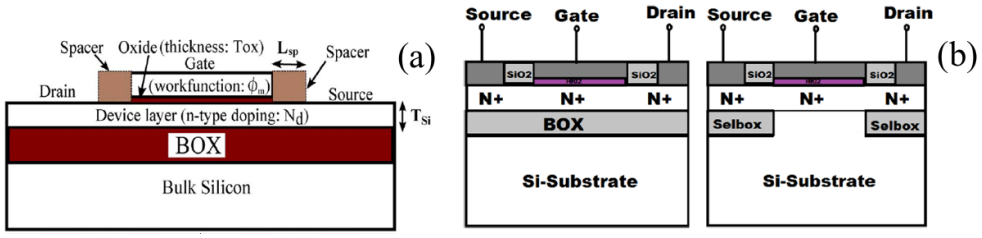

Figure 13. (a) Planar junctionless transistor with high-k [45]. (b) SOI and SELBOX planar junctionless transistors [48]

Besides bulk and *SOI* structures, other typologies were proposed to increase the junctionless planar transistor; for instance the *SELBOX* structure, shown in Fig.13(b), which is a variant of the conventional *SOI*. One of the reason for which such structure was introduced is related to the thermal isolation *SOI* structures, which is responsible for the increment of the transistor temperature. The reduction of the

thermal isolation leads to an increment for the I_{on}/I_{off} of 6 orders of magnitudes (from 2.31e3 to 1.5e9) in $SELBOX$ structures [48]; moreover such structure allows to increase the gate control on the device, since a pn junction between the highly doped channel and the substrate is formed, thus allowing the depletion of that part of the device layer thickness. The latter phenomenon can be obtained also by adding a a metal layer on the top of a SOI structure: by doing that a Schottky junction is formed, which could help to fully deplete the transistor in the OFF state [122].
Regarding leakages in junctionless transistors, one of the most critical is that associated to the parasitic BJT (bipolar junction transistor) depicted in Fig.14: as electrons tunnel from the valence to the conduction band (band-to-band-tunneling), they leave holes in the channel that can raise its potential. This phenomenon *triggers* a parasitic BJT between the source, the channel, and the drain in the OFF state [49].

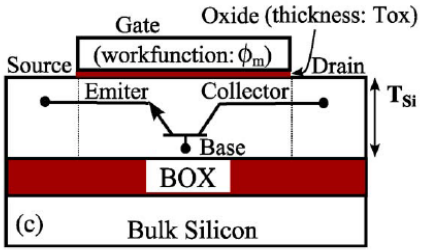

Figure 14. Parasitic BJT in planar junctionless transistor [49].

The charge associated to the holes accumulated in the floating body of the channel can causes a forward bias of the junction associated to the source/channel; if this bias turns on the parasitic BJT, then a large leakage current is observed, which critically influences the OFF state behavior. A possible solution is to employ thin film transistor, which can reduces the band-to-band-tunneling, and therefore the associated leakage.

3.5. Thin film

Thin film junctionless transistors (Fig.15) are characterized by an ultra thin channel thickness ($\leq 10nm$) and very high doping concentration ($\geq 1e19cm^{-3}$), which allow high current to flow in the device. As for the other junctionless transistor, the conduction is not due to an inversion layer, but to the whole channel region; a thin film is therefore needed also to assists the full depletion in the OFF state [75]. A difference with respect to planar junctionless transistor characterized by thin device layer thickness is that the majority of the reported junctionless thin film transistors is composed of polycrystalline silicon as channel material. Another difference with respect to the planar version is that they can present also double gate structure, which ensures lower I_{off}, since the depletion width is controlled by two gates instead of one, and higher I_{on}/I_{off} ratio [78].

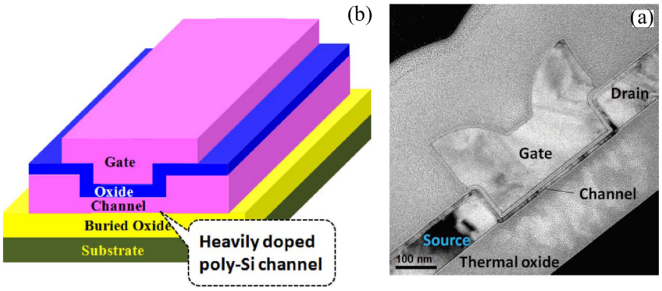

Figure 15. (a) Structure schematic of a PolySi junctionless thin film transistor [75]. (b) Cross-sectional view of a fabricated PolySi junctionless thin film transistor with channel thickness, gate oxide thickness, channel length of 10nm, 8.5nm, and 400nm respectively [74].

Not only planar and double gate junctionless thin film transistors were reported, but also thin film GAAFETs [81,83,84], and double/triple gate thin film nanowires, which were investigated in terms of grain boundaries [80]: the polycrystalline silicon, in fact, is composed by many crystallites connected by grain boundaries (Fig.16(a)); when electrons get trapped in the boundaries (Fig.16(b)), a space charge potential is created which can be (un)stable on the basis of the applied drain voltage. If the latter is too high, trapped electrons could become unstable, thus making unstable the potential associated to the grain boundaries. This phenomenon can lead to drain conductance oscillation, which is more critical in double gate than in triple gate, because the higher mobility in the former allows the electrons to easily destroy the trapped one, thus increasing the oscillation [80]. The implementation of PolySi is therefore limited by the potential barrier that is presents at the grain boundaries. But for high doping concentration such barrier could be less effective [74].

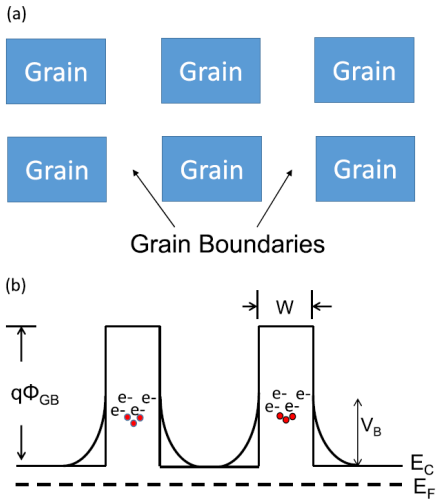

Figure 16. (a) Crystallites organization in polycrystalline films. (b)Energy band diagram showing the trapped electrons in the grain boundaries [80].

Compared to junction transistors, the junctionless one presents smaller transconductance g_m and drain conductance g_d, which implies a larger Early voltage, as well as improved low frequency noise (LFN) and higher signal-to-noise-ratio SNR [82], and thus the capability to be implemented in analog applications [77]. Regarding the performance of thin film junctionless transistor, it is mainly dependent on the film thickness and the doping concentration. If the doping concentration is very high, the channel is full of carriers and therefore a high I_{on} is ensured; but the high doping concentration lower the SS because the charges associated to the space regions could screen the electric field induced by the gate, thus making the control of the latter on the bottom of the channel more difficult. The SS thus decreases with decreasing device layer thickness [123]. As reported in [79], the SS, as well as the threshold voltage, it is dependent on the temperature, that is when the latter is increased the threshold voltage decreases (in absolute value) and the SS increases. This is attributed to the fact that the energy band gap E_g decreases with temperature, thus increasing the carrier concentration. The figure of merits of the reported thin film junctionless transistors are collected in Tab.5.

Table 5. Reported figure of merits of junctionless thin-film transistors.

Thin film	L_{ch} (nm)	T_{Si} (nm)	N (cm^{-3})	SS (mV/dec)	$\frac{I_{on}}{I_{off}}$	Ref.
Planar	400	10	$\geq 1e19$	240	$1e7$	[74]
Planar	1000	10	–	329	$1.45e5$	[78]
Planar	400	9	–	309	$8e7$	[82]
Planar (IM)	400	9	–	305	$1e7$	[82]
Planar (IM)	400	50	–	326	$3.2e4$	[82]
Double Gate	1000	10	–	160	$1.1e7$	[78]
NW raised S/D	500	–	$4e19$	100	$3.85e8$	[79]
NW GAA	60	2	–	61	$1e8$	[83]
NW GAA	–	12	–	199	$5.2e6$	[81]
NW GAA (IM)	–	12	–	184	–	[81]
NW GAA (Si)	–	0.65	–	59	$> 1e8$	[84]

3.6. Double Gate

The structure of a double gate junctionless transistor is shown in Fig.17, and the majority of the scientific literature is focused on its behavioral modelling. In fact many analytical models for double gate junctionless transistor were proposed, and the difference among them depends on the approximations involved in the derivation and the considered effects. For instance many models do not consider short channel and quantum effects [52,54,57,65], others are valid only for certain doping concentrations and device layer thickness ranges [58,60]. The reason for which quantum effects are important relies on the fact that they can affect the threshold voltage [73]. A semi-empirical model for symmetric DGJLTs that instead considers short channel effects is given in [55], where it is explained that the critical issue is modelling the transition between the depletion and the accumulation, since the physical behavior is not the same in the two operating regimes. To reduce the complexity of the models it is possible, for example, to consider high doping concentration, which allows to simplify the depletion width approximations [61], or to use separation of variable in the Poisson equation [66].

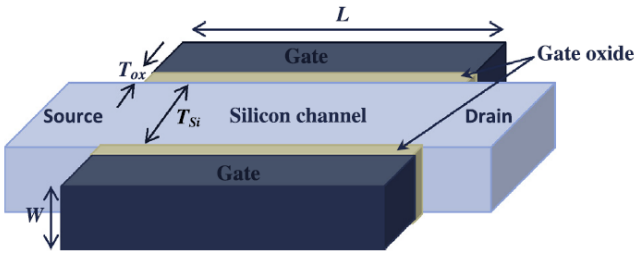

Figure 17. Schematic of a double gate junctionless transistor [54].

In [50] a model for symmetrical long channel n-type DGJLTs was proposed, in which starting from the $1D$ Poisson-Boltzmann equation a unique expression for the current in all the different conduction regimes is obtained. A model, derived starting from the 1D Poisson equation, for the threshold voltage of p-type DGJLTs was instead proposed by [51]: it allowed to observe that the threshold voltage becomes more positive as the device layer thickness, the doping concentration, and the oxide thickness are increased. In [53], instead, a model for long channel DGJLTs is proposed, by analytically modelling the current, the threshold voltage, and the electric field.

Regarding the device performance, it could be influenced by the BTBT tunneling (explained in thin film transistor section), which increases the leakage current. In order to reduce it, a possible solution is to implement the structure in Fig.18, which presents a thicker gate oxide near to the gate edges. It was, in fact, observed that by changing the indicated geometrical parameters the energy bands of the carriers under the gate are modified [68].

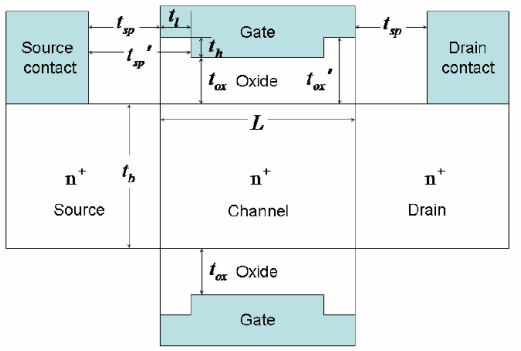

Figure 18. Improved DGJLT structure for the BTBT reduction [68].

As for the other junctionless transistors, also DGJLTs with stacked-oxide structures were proposed [56,64]: with respect to the conventional architecture it presents higher I_{on}/I_{off}, and lower SS and $DIBL$. Moreover if the dielectric constant is high (e.g. HfO_2), a reduction of the leakage current could be observed [62] as well as an improvement of the analog parameters [69]. Besides gate oxide engineering also spacer engineering could lead to a performance improvement, since the spacers have an influence on the lateral extension of the depletion width, thus having an impact on the effective channel length [71,72]. Besides gate oxide engineering, also optimization in terms of doping concentration can be considered: it was reported that a concentration of $1e18cm^{-3}$ can significantly improve the DGJLT performance, since the threshold voltage sensitivity was reduced by $70\% - 90\%$ with respect to the device layer and gate oxide thickness [67].A graded doping profile, instead, can reduces I_{off} by six order of magnitude [70]. Regarding the mobilities, because of screening effects the bulk mobility is lower than the accumulation one which can be extracted by taking the second derivative of the $1/I_{acc}$ curve. The bulk mobility, instead, can be obtained by the I_{bulk} expression, which requires to know the flat band voltage [63]. Their values can be degraded in case in which high voltages are applied [59]. The critical issue in modelling the mobility is that it could require the implementation of complex equations (Schrödinger) as well as the the knowledge of parameters such as impurities and surface roughness scattering mechanisms [124].

3.7. Tunnel FET

The structure of a triple gate junctionless tunnel field effect transistors is depicted in Fig.19(a): the device layer is uniformly doped, and by correctly fixing the voltages on the side gates the tunneling effect can be triggered, that is the n+n+n+ structure is *converted* (in terms of energy band diagram) in a p-i-n one Fig.19(b). The high-k dielectric below the gate (Si_3N_4, $k = 7.5$) increases the gate control (by improving the internal electric field [92]), while the low-k spacers (SiO_2, $k = 3.9$) isolate them [85]; by increasing the dielectric constant of the low-k spacers it is possible to reduce I_{off}, while increasing the doping concentration leads to an increment of both I_{on} and I_{off}, with the latter being more sensitive. Regarding SS, its value decreases from $290mV/dec$ to $47mV/dec$ as the doping concentration decreases from $2e19cm^{-3}$ to $1e19cm^{-3}$ (one of the main advantage with respect to conventional JLFETs is in fact the possibility to achieve sub $60mV/dec$ SS, since the conduction mechanism is based on tunneling). Reducing the channel length causes instead an increment of $DIBL$, and thus of the I_{off} [85].

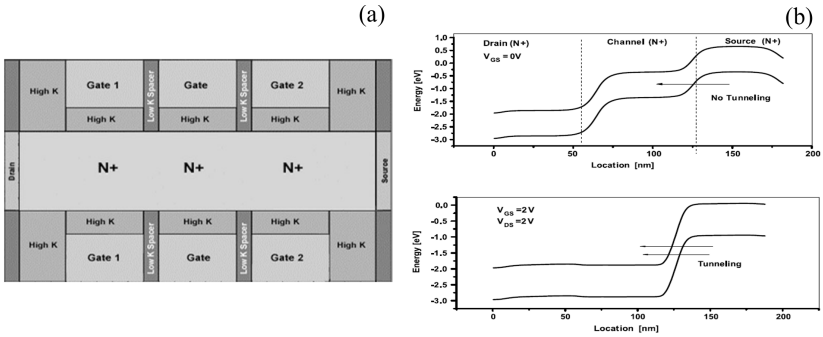

Figure 19. (a) Cross-sectional view of a junctionless tunnel field effect transistor. (b) Energy band diagrams of tunnel field effect transistor [85].

Regarding, instead, DG devices it is reported that an increment of the dielectric constant k leads to an improvement of the I_{on}, as well as an increment in the insulation layer thickness causes an improvement in both I_{on} and SS, despite and increment of the parasitic capacitance [86,90]. A more complex approach used to improve the robustness of junctionless TFETs is based instead on the selective introduction of dielectric materials in the gate oxide: they can reduce the variations in the coupling capacitance, thus allowing a higher immunity in terms of the sensitivity [91]. The performance can be further increased by the implementation of dual material gate (Fig.20(b)) or heterojunctionless structures (Fig.20(a)) in which as for TG and DG by correctly setting the voltage on the side gates, a p-i-n region is obtained through the work function difference. The heterojunctions are employed because on the basis of the energy bandgap a higher I_{on}, I_{on}/I_{off}, and low SS can be obtained [87–89]. A simpler solution instead can be to use only one material, but different from silicon: for instance in [94] a TFET with a device layer made of indium arsenide is proposed. The figure of merits of the reported junctionless transistors are collected in Tab.6.

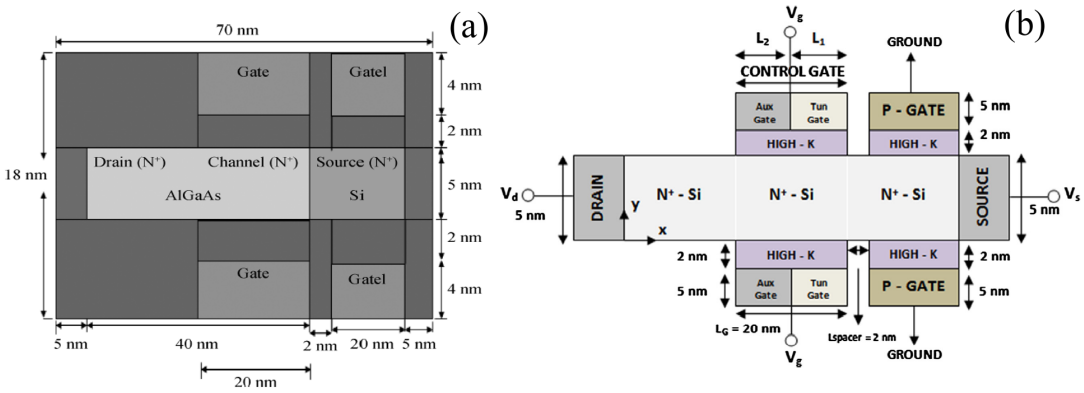

Figure 20. Cross-sectional view of a TFET with heterostructure [88].

Table 6. Reported figure of merits of junctionless tunnel field effect transistors.

TunnelFET	L_{ch} (nm)	T_{Si} (nm)	N (cm^{-3})	SS (mV/dec)	$\frac{I_{on}}{I_{off}}$	Ref.
SG $(InAs)$	20	10	$1e19$	7	$2e10$	[94]
DG	20	5	$1e19$	41	$1e7, 1e8$	[88]
DG	20	5	$1e19$	49	$1e10$	[90]
DG	25	5	$2e19$	11	$6e11$	[93]
DG	20	5	$1e19$	84	$8e7$	[87]
DG (La_2O_3)	20	5	$1e19$	87	$3.5e8$	[86]
DG (HfO_2)	20	5	$1e9$	91	$3e8$	[86]
DG (TiO_2)	20	5	$1e19$	70	$6e8$	[86]
DG $(Si : Si_{.3}Ge_{.7})$	20	5	$1e19$	32	$8e6$	[87]
DG $(GaAs : Si)$	20	5	$1e19$	74	$2e8$	[87]
DG $(Si : InAs)$	20	5	$1e19$	44	$8e5$	[87]
DG $(GaAs : Ge)$	20	5	$1e19$	16	$2e12$	[87]
DG $(AlGaAs/Si)$ (HfO_2)	20	5	$1e19$	48.2	$1e8$	[92]
DG $(AlGaAs/Si)$ (La_2O_3)	20	5	$1e19$	47.2	$1e8$	[92]
DG $(AlGaAs/Si)$ (TiO_2)	20	5	$1e19$	43.9	$1e8$	[92]
Dual Material DG	20	5	$1e19$	17	–	[95]
TG	50	8	$1e19$	47	$1e9$	[85]

4. Conclusions

Depending on the design choices, all the typologies of junctionless transistors can present high ION/IOFF ratio, as well as quasi-ideal subthreshold slope and optimal values of DIBL; it is not therefore possible to distinguish, on the basis of performance parameters, which is the best junctionless transistor. But more complex the structure, and more flexible the optimization: the TFET, which can present a TG structure, is more difficult to design, since the gate voltage have to be carefully fixed, and the work function differences have to guarantee the tunnel behavior. The DGJLT, which has a less complex structure with respect to TFET, presents an additional degree of freedom and enhanced gate control with respect to PJLT and TFT. The latter presents high performance parameters only if the device layer, made of polysilicon, is very thin. FinFETs, with respect to nanowires, present higher ION/IOFF ratio and more flexibility in terms of structure engineering; the electrostatic control of both devices can be increased by surrounding the entire gate (GAA configuration).

Therefore in this work the junctionless transistors were classified on the basis of the channel structures, but considering that certain definitions can be common to more devices or dependent on the material composition. For each device the main figure of merits (ION/IOFF,DILB,SS) are reported, and design techniques as oxide/doping/spacers engineering are described. Moreover the main source of leakages, together with the technological solutions to the performance degradation, are reported.

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Abbreviations

The following abbreviations are used in this manuscript:

JLT	Junctionless transistor
JT	Junction transistor
PLJT	Planar junctionless transistor
NW	Nanowire
GAA	Gate All Around
FET	Field effect transistor
TFT	Thin film transistor
TFET	Tunnel field effect transistor
SG	Single gate
DG	Double gate
TG	Triple gate

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B.2 A Numerical Method to Extract the Depletion Region Width of Planar Junctionless Transistors

MDPI

Article

A Numerical Method to Extract the Depletion Region Width of Planar Junctionless Transistors

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Abstract: In this paper, we present a numerical method to extract the depletion region width from simulation results generated in COMSOL Multiphysics software. The proposed algorithm was verified by performing simulations, of n-type planar junctionless transistors characterized by a substrate thickness in the range of $[10-20]nm$ and high level of doping in the range of $[10^{18}-10^{19}]cm^{-3}$. Simulation results show that the numerical data generated by the proposed algorithm fit the analytical model of the depletion region width. Furthermore, this method can be used to determine the position of the depletion region boundary in graphical representations generated by COMSOL Multiphysics, simplifying the analysis of the device operation. Finally, by extrapolating the data generated by our method, we found that the concentration of carriers at the boundary of the depletion region is usually 0.55-0.57 times the doping of the substrate.

Keywords: Junctionless Transistor; Depletion Region; Electron Concentration; COMSOL.

1. Introduction

The concept of junctionless transistor (JLT) was introduced by J.E. Lilienfeld in 1925 [1]. The main characteristic of the Lilienfeld device was the absence of any PN junction in the physical structure of the transistor. By controlling the voltage at the gate of this semiconductor device, Lilienfeld was able to deplete the carriers in a localized region of the substrate. In this manner, it was possible to control the resistivity of the device and the electrical current through the transistor. Although, the idea and the operation of this device were verified through analytical formulas, the technology of that time did not allowed him to realize a working device [2], which required the fabrication of a nanometric substrate layer. Only in 2010 at the Tyndall National Institute, the first junctionless transistor [2] was successfully manufactured; J.P. Colinge et al. fabricated a $10nm$ thick and $1\mu m$ long highly doped ($10^{19}cm^{-3}$) junctionless nanowire transistor. The advantages of a junction-free structure are numerous such as the absence of doping concentration gradients [3], which are difficult to be precisely controlled in the nanometric regime, the absence of junction leakages, simple fabrication process and lower fabrication cost (no implantation for source and drain) [4]. In addition, junctionless technology can provide greater performance with respect to conventional transistors, such as reduced short-channel effects (effective channel length not reduced by PN junctions) [5] and less degradation of carrier mobility (current flows in the bulk of the substrate) [6]. Junctionless transistors can be realized in different shapes and dimensions. Most often they are characterized by a three dimensional (3D) structure (ex: nanowire, finFET [7], GAA [8], etc.), which allows an improved control on the channel of the transistor. On the other hand, the implementation of two dimensional (2D) or planar solutions have been recently investigated by numerous researchers, because they are simple and easy to fabricate [9–12]. During

the last decade, numerous implementations of junctionless transistors were proposed such as single gate [10,11], double gate [13], thin-film [12], tunnel-FET [14], just to mention some. These structures are characterized by different geometries, however, their operation is based on the same working principle. In spite of the fact, that the analytical models described in literature have been proved through measurements on real prototypes, the simulation of a PJLT at device level remains one of the most useful tool to design customized junctionless devices. Unfortunately, not many papers have been published on the comparison between simulation results and analytical models. In particular, to the best knowledge of the authors, no paper has been found regard the comparison between the analytical model of the depletion region width and simulated results of PJLT. For this reason, we decided to investigate on this issue, by simulating a single gate PJLT using COMSOL Multiphysics software [15]. The major challenge in performing this operation is to correctly determine the boundary of the depletion region from the simulated results obtained in COMSOL. Therefore, we developed an algorithm, which in combination with the analytical formula of the depletion region width, allows us to accomplish our goal. The paper is organized as follows. Section 2 introduces to the working principle of a planar junctionless transistor, section 3 describes the idea behind the algorithm used to identify the depletion region from COMSOL simulation results and section 4 reports the simulation results. The paper ends with conclusions and future works in section 5.

2. Single Gate Planar Junctionless Transistors

2.1. Physical Structure of PJLT

The physical structure of a planar junctionless transistor is shown in Figure 1(a) [11,16].

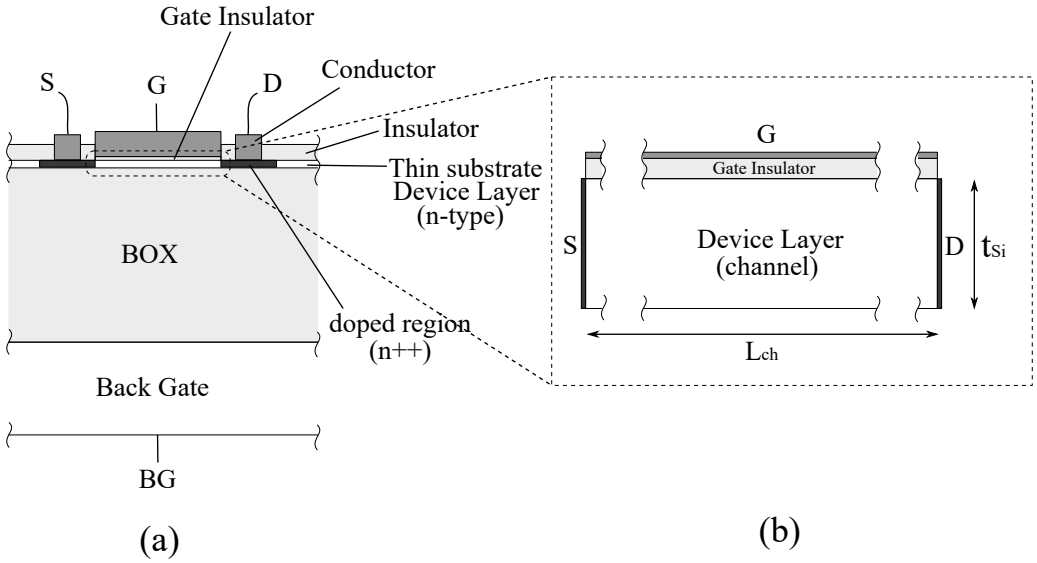

Figure 1. N-type PJLT Physical Structure . (a) Complete Structure on FDSOI wafer. (b) Simplified model of the JLT physical structure.

A PJLT is typically realized on a fully depleted silicon on insulator (FD-SOI) wafer [17], which is characterized by three layers: a handle substrate (silicon), an insulating layer often referred as buried oxide or BOX since it is made of silicon dioxide and a thin silicon layer also known as device layer (silicon). In order to realize PJLT on FD-SOI wafers, the device layer is usually highly doped and characterized by a thickness in the range of tens to hundred of nanometers. The device layer can be uniformly doped with acceptor or donor atoms. For this reason, we have to distinguish two categories of PJLT: p-type PJLT and n-type PJLT. The particular case of an n-type PJLT is represented in Fig.1. The handle substrate does not require to be doped unless the designer decides to use it as second gate terminal or back gate. In this paper, we focus on a single gate PJLT, therefore, we will neglect the back

gate terminal. The physical structure of a single gate PJLT resembles a MOSFET, however in PJLT there are no PN junctions. Although, the operation of a PJLT is possible with a uniformly doped device layer, better performance are achieved by realizing highly doped drain and source wells.These ones minimize the parasitic resistances between the channel of the transistor (conductive part of the device layer between the wells) and the actual source and drain metallizations. In particular, if the device layer is n-doped, then the source and drain wells must be heavily doped with donors (n++). On the other hand, if the device layer is p-doped, then the source and the drain wells must be heavily doped with acceptors (p++). These wells are represented with black regions in Fig.1(a). Finally, a very thin insulating layer separates the gate terminal of the PJLT and the device layer beneath.

2.2. Working Principle of Single Gate PJLT

Current literature describes PJLT as gated resistors [2] in which the amount of electrical current through the device is controlled by the gate voltage [3]. In order to clarify this definition, we will consider a simplified model of the single gate PJLT shown in Fig.1(b). An electrical current, typically known as drain current, flows through the channel of the transistor, only when a voltage difference is applied between the drain and the source terminals. For the case shown in Fig.1(b), the channel is fully enhanced (completely conductive), hence the amplitude of the drain current is only limited by the electrical resistance of the device layer. This resistance depends on the device layer resistivity ρ_{Si} and the geometrical dimensions of the channel such as channel width W_{ch}, channel length L_{ch} and channel thickness t_{Si} ($R_{ch} = \rho_{Si} L_{ch}/(W_{ch} t_{Si})$). However, if we vary opportunely the gate voltage of this transistor, we can affect the distribution of the charge inside the device layer modifying the effective dimensions of the channel, therefore varying the resistance and the electrical current through the transistor. In order to provide more details about this phenomenon, we will describe the operation of the n-type PJLT shown in Fig.2(a). In this paper, we want to analyze only the effect of the gate voltage on the channel, so we have grounded the drain and the source terminals. In this case, the default state of the transistor consists of a fully conductive channel. Next, by reducing the gate voltage to negative values, the electrons under the gate insulator will be repelled and moved away from their initial position. In this region, the atoms will be depleted of carriers, hence, a non conductive region known as depletion region will start to create (Fig.2(a)).
Fig.2(b) shows that, if the gate voltage becomes sufficiently negative, then the channel of the transistor will be fully depleted of carriers and there will not be any conductive path between the drain and the source terminals. When this event occurs, the transistor is said to be turned off and no current can ideally flow between drain and source. The PJLT previously described is said to work in depletion mode and it is characterized by the fact that the device layer is fully conductive when no gate voltage is applied. On the other hand, a PJLT is said to work in enhancement mode, if the channel is fully depleted at zero gate voltage. The operation of the PJLT in depletion and enhancement mode is schematically represented in Fig.2(b). The gate voltage value at which the transistor turns off is usually referred as threshold voltage V_{th}, while the gate voltage value at which the transistor channel can be considered fully conductive (transistor turned on) is known as flat band voltage V_{FB}. The latter one depends on the material used to implement the device layer and the gate electrode. The analytical model of this parameter is shown in Eq.(1) for an n-type PJLT and Eq. (2) for a p-type PJLT [18].

$$V_{FB,n} = |q|\Phi_M - |q|\Phi_{sn} = |q|\Phi_M - (|q|\chi + Eg/2 - |q|\Phi_n) \tag{1}$$

$$V_{FB,p} = |q|\Phi_M - |q|\Phi_{sp} = |q|\Phi_M - (|q|\chi + Eg/2 + |q|\Phi_p) \tag{2}$$

Where: $q\Phi_M$ is the gate work function, $q\chi$ is the electron affinity, E_g is the energy band gap, and $q\Phi_{n,p}$ is the bulk potential which is defined as $k_B T\, ln(N_{D,A}/n_i)$, k_B is the Boltzmann constant, T the temperature, and n_i the intrinsic carrier concentration.

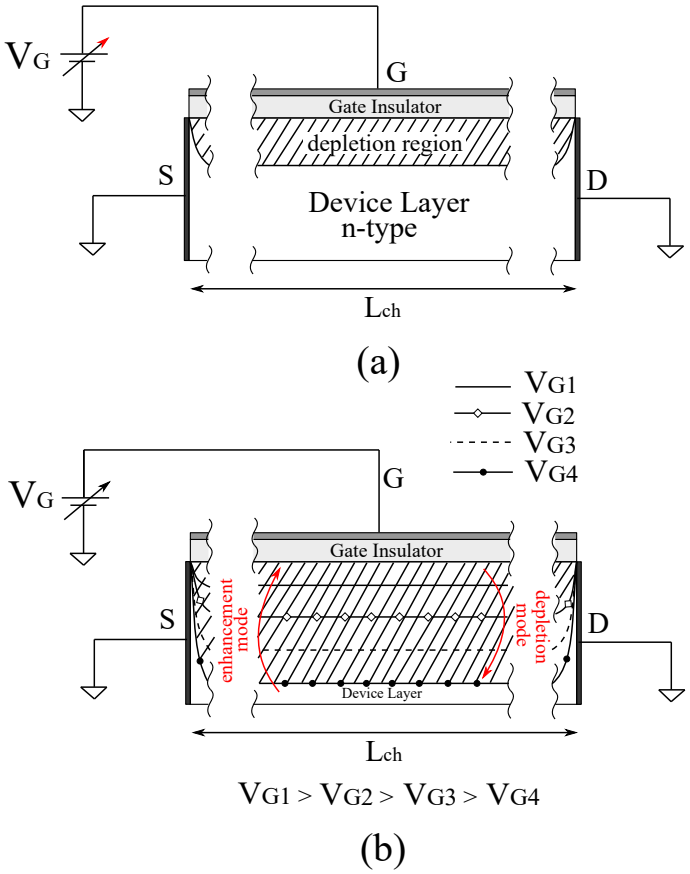

Figure 2. N-type PJLT Working Principle. (a) State of the PJLT for a generic value of gate voltage (b) Depletion region for different values of gate voltage.

The depletion region width of a PJLT can be extracted by performing a quantitative analysis of the carrier concentration during the normal operation of the transistor. This analysis has been summarized in Appendix A and the result is the formula shown in Eq.(3) for an n-type PJLT.

$$X_{dep} = -\frac{\epsilon_{Si}}{C_{ox}} + \sqrt{(\frac{\epsilon_{Si}}{C_{ox}})^2 - \frac{2\epsilon_{Si}}{|q|N_d}(V_G - V_{FB})} \tag{3}$$

A similar formula can be found for a p-type PJLT as shown in Eq.(4).

$$X_{dep} = -\frac{\epsilon_{Si}}{C_{ox}} + \sqrt{(\frac{\epsilon_{Si}}{C_{ox}})^2 + \frac{2\epsilon_{Si}}{|q|N_a}(V_G - V_{FB})} \tag{4}$$

Where: ϵ_{Si} is the dielectric constant of the device layer, C_{ox} is the capacitance per unit area of the oxide used to implement the thin gate insulating layer, q is the electric charge of an electron, N_d is the donor concentration used to dope the device in n-type PJLT, N_a is the acceptor concentration used to dope the device layer in p-type PJLT, V_G is the gate voltage and V_{FB} is the flat band voltage. These analytical formulas provide numerous information about the operation of the transistor. For the case of an n-type PJLT working in depletion mode, the depletion region exists only for $V_G < V_{FB}$, while for the p-type PJLT the depletion region exists only for $V_G > V_{FB}$. In both cases, at $V_G = V_{FB}$ the depletion region is practically negligible and the channel can be considered fully conductive. This is the reason why, V_{FB} represents the voltage at which the transistor is considered turned on. There is a third situation, which can occur during the operation of PJLT when $V_G > V_{FB}$ (for n-type PJLT), however, in this paper, we restrict the analysis to the range [V_{th},V_{FB}], which simplifies the description of the transistor operation.

The formulas for threshold voltage V_{th} can be derived from Eq.(3) or Eq.(4) by assuming $X_{dep} = t_{Si}$. The on and off gate voltage values of an n-type PJLT are shown in Eq.(5).

$$\begin{cases} V_{G-ON} = V_{FB} \\ V_{G-OFF} = V_{th} = V_{FB} + \frac{|q|N_d}{2\epsilon_{Si}} \left[\frac{\epsilon_{Si}^2}{C_{OX}^2} - (t_{Si} + \frac{\epsilon_{Si}}{C_{OX}})^2 \right] \end{cases} \tag{5}$$

Similar formulas are valid for the p-type PJLT, which are shown in Eq.(6).

$$\begin{cases} V_{G-ON} = V_{FB} \\ V_{G-OFF} = V_{th} = V_{FB} - \frac{|q|N_a}{2\epsilon_{Si}} \left[\frac{\epsilon_{Si}^2}{C_{OX}^2} - (t_{Si} + \frac{\epsilon_{Si}}{C_{OX}})^2 \right] \end{cases} \tag{6}$$

More details about the difference between the operation of an n-type and a p-type PJLT can be extracted by analyzing the plots of the formulas in Eq.(3) and (4), shown in Fig.3.

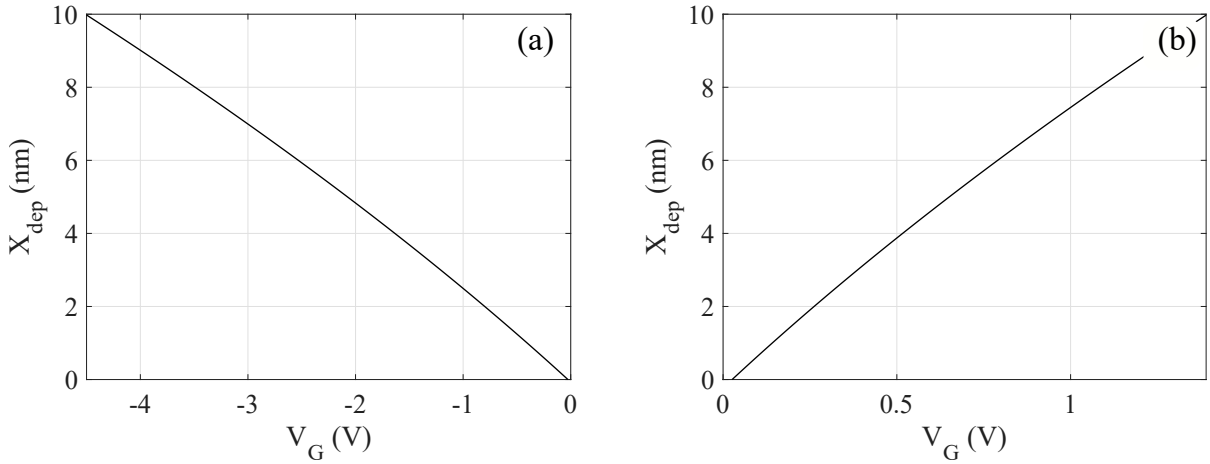

Figure 3. Analytical depletion width as a function of the gate voltage computed with the data in Table 1. (a) N-type PJLT. (b) P-type PJLT.

These graphs were extracted by using the parameters shown in Table.1.

Table 1. Depletion PJLTs Parameters

	N-type PJLT	**P-type PJLT**
Parameter	**Value**	
Materials		
Device layer	Si/n-type	Si/p-type
insulating gate layer	SiO_2	
Gate electrode	N-type Poly-Si	P-type Poly-Si
Material proprieties		
Device layer Doping concentration ($atoms/cm^3$)	$N_d = 10^{19}$	$N_a = 3.05 \times 10^{18}$
Intrinsic carrier concentration : n_i ($atoms/cm^3$)	5.4×10^9 at 293.15 K	
Dielectric constant device layer : ϵ_{Si} (F/cm)	$11.7\epsilon_0$	
Dielectric constant insulator : ϵ_{ox} (F/cm)	$3.9\epsilon_0$ (SiO_2)	
Dimensions		
Channel length : L_{ch} (nm)	500	
Device layer thickness : t_{Si} (nm)	10	
Gate oxide thickness : t_{ox} (nm)	8	
Derived Parameters		
Electron affinity: $q\chi$ (eV)	4.05	
Energy band gap: E_g (eV)	1.13	
Bulk potential : $q\Phi_{n,p} = k_B T\, ln(N_{d,a}/n_i)$ (eV)	0.539	0.509
Oxide capacitance per unit area : $C_{ox} = \epsilon_{ox}/t_{ox}$ (F/cm^2)	4.32×10^7	
Gate work function: $q\Phi_M$ (eV)	4.05 (PolySi/n-type)	5.15 (PolySi/p-type)
Flat Band Voltage : V_{FB} (V)	-0.026	0.026

The n-type PJLT associated to the plot shown in Fig.3(a) is characterized by a device layer made of n-doped silicon, a gate insulating layer made of silicon dioxide and a gate electrode made of n-type poly-silicon. On the other hand, the p-type PJLT associated to the plot shown in Fig.3(b) is characterized by a device layer made of p-doped silicon, a gate insulating layer made of silicon dioxide and a gate electrode made of p-type poly-silicon.

The doping concentration and the thickness of the device layer in the n-type PJLT are similar to the one used by Colinge in [2] and they ensured that the channel of the transistor can be fully depleted by applying a precise value of gate voltage V_{th}. A different criterion was used to decide the doping concentration and the thickness of the device layer for the p-type PJLT. In this case, we set these two parameters in order to obtain a unipolar gate voltage range characterized by a flatband voltage of approximately 0V. This choice allows to use both transistors in analog and digital circuits characterized by single power supply. The channel length of the transistor was chosen to be sufficiently long so that the drain and source electric potentials would not affect the carrier distribution in the middle of the channel. In this way, we can study the dependency of the depletion region width due the only effect of the gate electric potential. Next, the dielectric constants in Table 1 were found in [19]. The thickness of the gate insulating layer t_{ox} was set in order to provide a sufficiently high dielectric strength. In fact, this insulator layer has to withstand the electric field created by the gate electrode when its potential sweeps within the range $[V_{FB}, V_{th}]$.

By using the parameters listed in Table 1, we calculated the threshold voltage for both the n-type ($V_{th} = -4.51V$) and p-type (V) PJLT. The values calculated are $V_{th} = -4.51V$ and $V_{th} = 1.39V$ for n-type and p-type PJLT respectively. This means that in order to turn on and turn off these transistors, the gate voltage has to vary within the range $[-0.026V, -4.51V]$ and $[0.026V, 1.39V]$ for the n-type and p-type PJLT respectively. In the n-type PJLT, the depletion region increases if the gate voltage becomes more negative than the electrical potential of the device layer, while in the p-type PJLT, the depletion region width increases when the gate voltage becomes more positive than the electrical potential of the device layer. This is due to the fact that the depletion region in n-type PJLT expands if negative electrical charges accumulate at the gate electrode, so that the free electrons beneath the insulating gate layer are repelled. On the other hand, in p-type PJLT, the depletion region expands only if positive electrical charges accumulate at the gate electrode. This ensures that the holes beneath the

gate insulating layer are repelled. Fig.3 shows that the operating range of the p-type PJLT is smaller than the one for the n-type. This situation occurs because these two ranges are proportional to the doping concentration in the substrate of these two devices, as shown in Eq.(5) and Eq.(6).
Next, we used COMSOL Multiphysics software to provide a graphical representation of the depletion region along the symmetric axis of an n-type PJLT. The physical structure of the PJLT simulated in COMSOL is shown in Fig.4, which was electrically connected as shown in Fig.2(a).

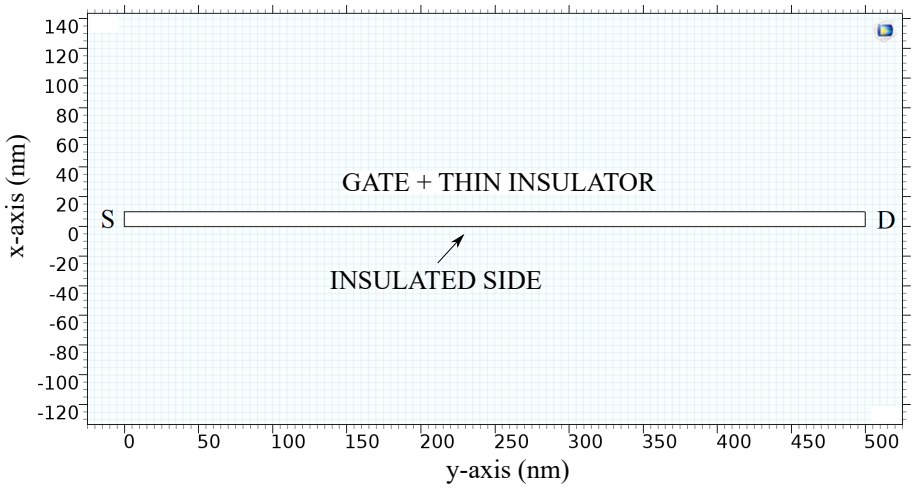

Figure 4. Geometrical dimensions of PJLT simulated in COMSOL Multiphysics.

The input parameters used to set-up this simulation are listed in Table 1. In addition, the simulator was set to use the Fermi-Dirac statistics. Simulation results are shown in Fig.5.

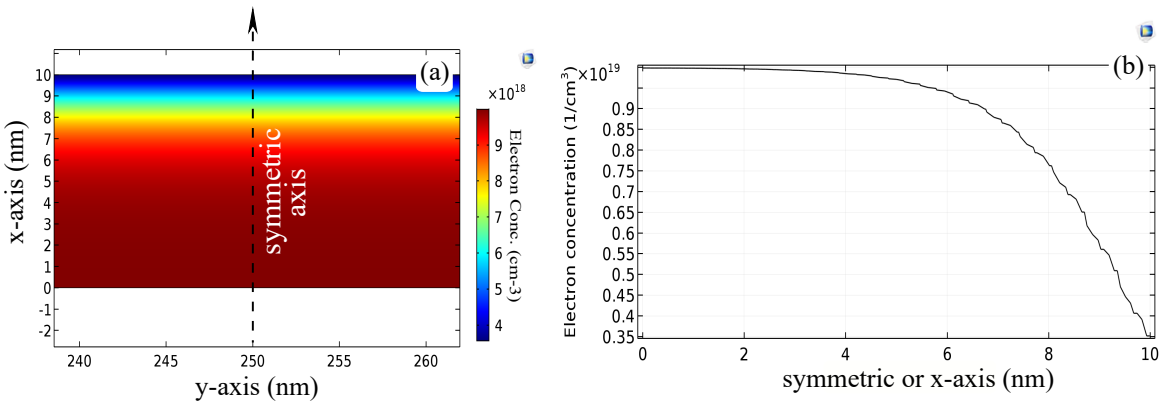

Figure 5. Carrier analysis in COMSOL Multiphysics. (a) Electron concentrations for $t_{Si} = 10nm$ and $V_g = -0.5V < V_{FB}$ (Depletion). (b) Electron concentration distribution along the line defined in Figure 5(a).

Fig.5(a) shows the electron concentration in the middle region of the channel when $V_G = -0.5V$. For this case, we expected a depletion region of approximately $1nm$. However, the boundary of the depletion region is difficult to identify since the carrier concentration in the device layer changes gradually along the perpendicular direction to the substrate. This phenomenon is shown clearly in Fig.5(b), which represents the carrier concentration extracted along the symmetric axis of the channel, shown in Fig.5(a). Therefore, we developed an algorithm to extract a fictitious carrier concentration, from the simulation results generated by COMSOL Multiphysics, which can be used to identify the location of the depletion region boundary.

3. Algorithm

In order to identify the depletion region boundary of a PJLT simulated in COMSOL Multiphysics, we propose the following algorithm:

1. Choose the geometry and the materials for the PJLT.
2. Calculate the depletion region width X_{dep}, for different gate voltage values uniformly distributed in the range $[V_{FB}, V_{th}]$. These calculations can be performed by using Eq.(3).
3. Set up COMSOL Multiphysics, in order to perform simulations of the structure designed in step 1 and connect the transistor as shown in Fig.2(a). The output of each simulation has to be the plot of the carrier concentration along the symmetric axis of the device layer as shown in Fig.5.
4. From the plot generated by COMSOL multiphysics, find the point, where the x coordinate is equal to $t_{Si} - X_{dep}(V_G)$ and record the value of carrier concentration associated to this position. This parameter represents the carrier concentration at the ideal location of the depletion region boundary for a particular value of gate voltage $n(X_{dep})$.
5. Repeat the previous step for each value of gate voltage used in step 2 and record both $n(X_{dep})$ and V_G for each simulation.
6. Create a graph by using all the recorded values of $n(X_{dep})$ and the associated gate voltages as shown in Fig.6(a).
7. Filter out, the numerical error introduced by COMSOL Multiphysics, from the previous plot. (In this paper, we performed this operation by approximating our data with a high order polynomial function. However, other methods can be used.)
8. By using the filtered data, define the range of carrier concentration in which there is the highest density of data points. (In this paper, we define this range by measuring the peak to peak amplitude of the ripple created by the polynomial approximation as shown in Fig.7(b). However, other methods can be used, such as by performing statistical analysis on the data.)
9. Calculate the mean value of the range defined in the previous step, in order to find the best approximation of the carrier concentration at the boundary of the depletion region ($n(X_{dep})_{opt}$).

4. Simulation Results

Finally, simulations in COMSOL Multiphysics of an n-type PJLT, were performed in order to verify the operation of the proposed algorithm. The geometrical dimensions and the input parameters used to run this software are shown in Fig.4 and Table.1. In this case, the flat band voltage and the threshold voltage are $V_{FB} = -0.026V$ and $V_{th} = -4.51V$, respectively. Therefore, the value of V_G was swept in the range $[-0.026V, -4.5V]$ with a step of 0.25V (step 5 of the algorithm). The result of this procedure provides a curve, which represents the electron concentration $n(X_{dep})$ extracted at the boundary of the depletion region for different values of gate voltage (step 6 of the algorithm). The resulting curve is represented in Fig.6(a).

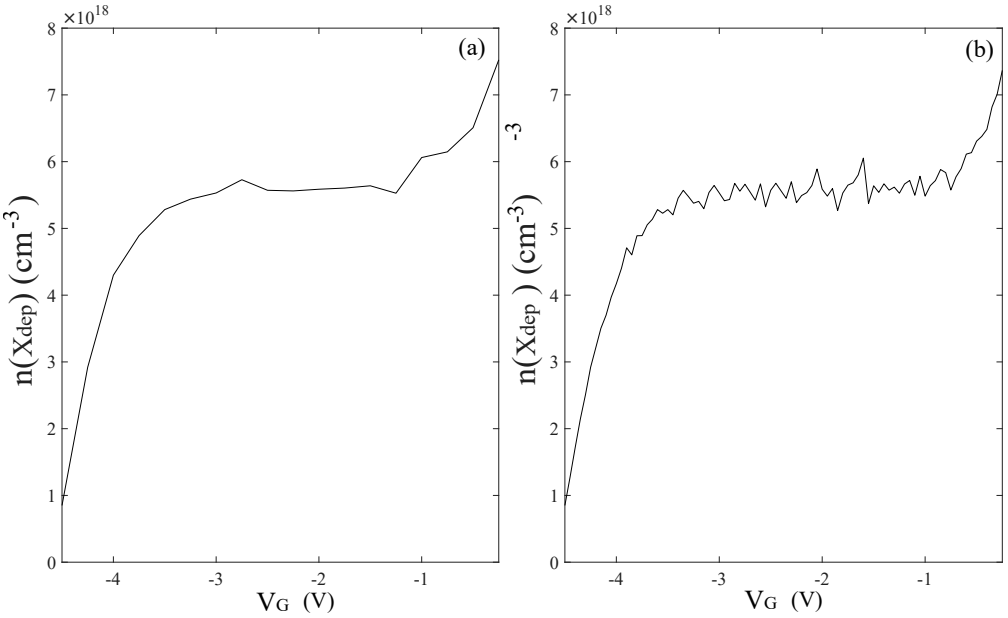

Figure 6. Electron concentration at the boundary of the depletion region extracted for different values of gate voltage step. (a) V_G swept in $[V_{FB}, V_{th}]$ with step of 0.25V (b) V_G swept in $[V_{FB}, V_{th}]$ with step of 0.05V.

The behaviour of this curve was quite unexpected, because $n(X_{dep})$ is supposed to be constant and not dependent on the amount of gate voltage applied to the transistor. Furthermore, the dependency of $n(X_{dep})$ on V_G makes it difficult to define a unique value of carrier concentration, which can be used to identify the boundary of the depletion region. Nevertheless, a deep analysis of the collected numerical data shows that the values of $n(X_{dep})$ are affected by two source of error when V_G approaches to V_{th} or V_{FB}, which are inaccuracy of the analytical model used to determine $n(X_{dep})$ and the numerical error introduced by COMSOL Multiphysics. In order to exploit the effect of low accuracy of the analytical model, we need to analyze the simulation results shown in Fig.8. Each curve in this plot represents the electron concentration along the symmetric axis of the channel for a given value of gate voltage. For values of gate voltage approaching to V_{FB} and V_{th}, the difference between the carrier concentration in the channel and depletion region is reducing. When V_G approaches to V_{FB} the depletion region is so thin that this region is not completely emptied of carrier as assumed in the analytical model of the depletion region width. On the other hand, when V_G approaches to V_{th}, the channel of the transistor becomes so thin that the carrier concentration in this region is not sufficiently high to mimic the behaviour of an ideal conductive material as assumed by the analytical model. For all the other values of V_G (in this case between -3V and -1.5V), the channel of the transistor and the depletion region are characterized by very different values of carrier concentration, which provide a better approximation of the ideal situation described by the analytical model. However, this situation is also affected by a certain error due to the fact that the carrier concentration changes gradually and not abruptly as defined in the depletion region model. Overall, we can conclude that, the use of the analytical model in the proposed method introduces a certain error during the estimation of the carrier concentration at depletion region boundary. In addition, this error increases as V_G approaches V_{th} or V_{FB}. On the other hand, when V_G approaches V_{FB} or V_{th}, the size of the mesh used for performing the simulations in COMSOL becomes comparable to the thickness of the depletion region or the thickness of the channel respectively. Thus, this situation turns out to introduce a numerical error in the simulation results. By taking into account all of these source of error, we conclude that the most reliable value of $n(X_{dep})$ are those one associated to a gate voltage values far from V_{th} and V_{FB}, which correspond to the center part of the curve shown in Fig.6(a). In this range, $n(X_{dep})$ is almost constant, but a close inspection of the curve in Fig.6(a) shows that the data between -3V and -1.5V are quite "noisy" due to numerical

errors introduced by COMSOL. To prove this point, we have compared the simulation results when the sweep of V_G was done with a step of 0.25V and a step of 0.05V as shown in Fig.6.
The resulting curves from these simulations follow the same trend, but they are characterized by different numerical error in the middle range of V_G. In order to remove this numerical error from our data, we have decided to interpolate this curve with a high order polynomial approximation, which in this case is of 10th order (step 7 of the algorithm). By doing so, we obtain a smoother curve shown in Fig.7(a).

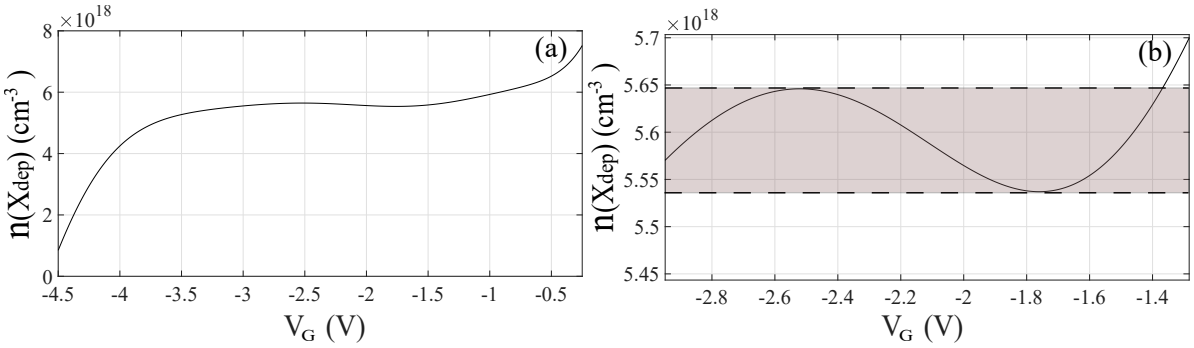

Figure 7. Polynomial approximation of the curve represented in Fig.6. (a) Full View (b) Zoom of the curve in the range [-2.9V,-1.3V]. ($t_{Si} = 10nm$).

The resulting polynomial curve doesn't show any high frequency "numerical error", however, there is a low frequency oscillation in the middle range of this plot. This oscillation still provides an ambiguity on which value of $n(X_{dep})$ must be chosen, but due to the small peak to peak amplitude ($\simeq 0.1 \times 10^{18} cm^{-3}$) of this oscillation, we have limited the domain of the target solution to $[5.54, 5.65] \times 10^{18} cm^{-3}$ (step 8 of the algorithm). Finally, the best approximation of $n(X_{dep})_{opt}$ is found by calculating the mean value of this range, which results in approximately $5.55 \times 10^{18} cm^{-3}$ (last step of the algorithm). This is the value, that best approximates the carrier concentration at the boundary of the depletion region for the PJLT simulated in COMSOL Multiphysics. By using $n(X_{dep})_{opt}$, we can extract a numerical approximation of the analytical model described in Eq.(3). In order to obtain this curve, first we need to extract the carrier concentration along the symmetric axis of the transistor channel for different values of V_G as shown in Fig.8.

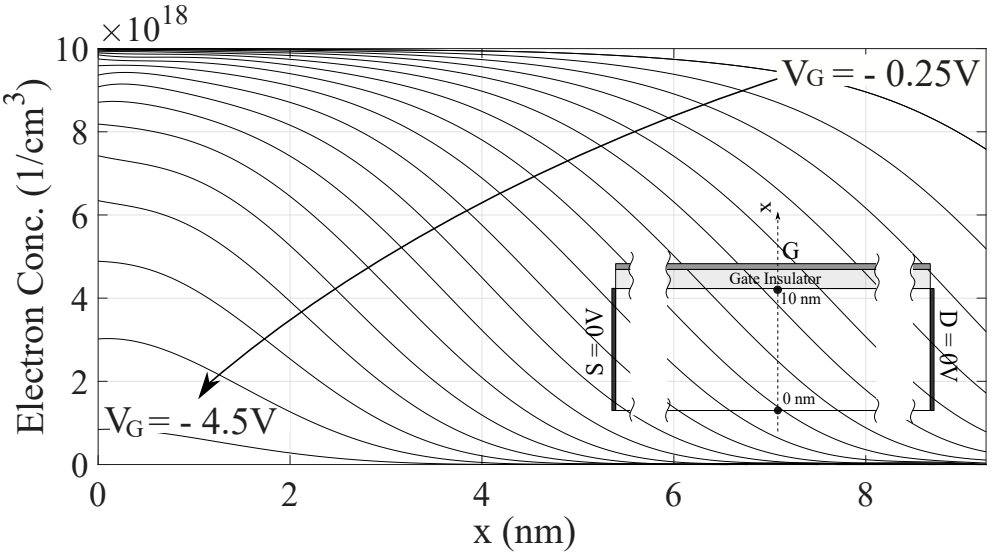

Figure 8. Electron Concentration along the symmetric axis of the transistor, for different values of V_G swept in the range $[V_{th}, V_{FB}]$, with a step of 0.25V. The parameters related to this simulations are summarized in Table 1.

Then the intersection points between the curves extracted in Fig.8 and $n(X_{dep})_{opt}$ must be determined, as shown in Fig.9.

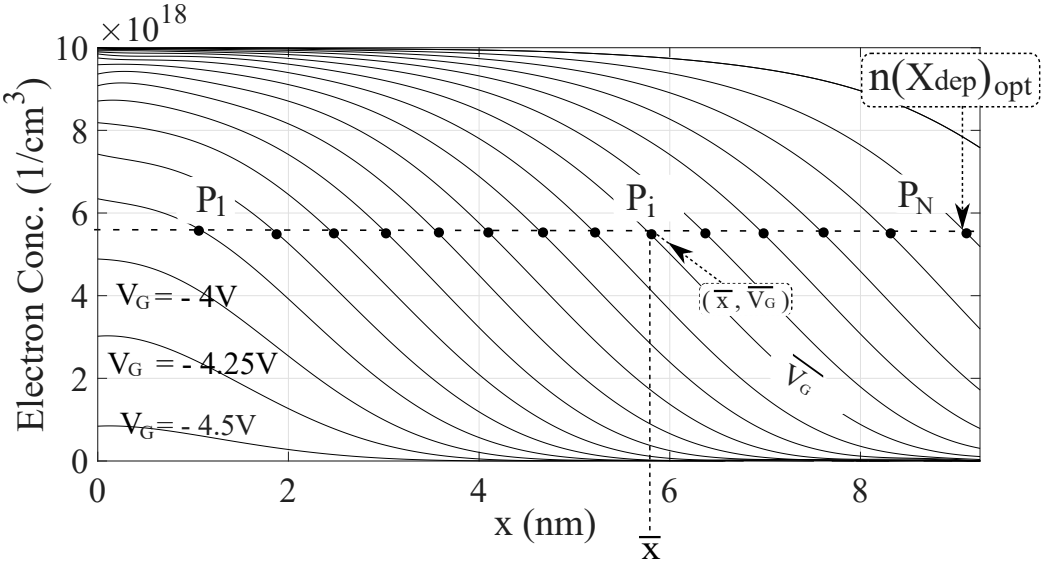

Figure 9. Extraction of the depletion region width for different values of gate voltage.

Each intersection point will be associated to a couple of numbers $(t_{Si} - \overline{x}, \overline{V_G})$. Where: $\overline{x}$ represents the x coordinate of the intersection point and $\overline{V_G}$ represents the gate voltage used to extract the curve over which the intersection point is placed. After that, we can use all these couples to create the target plot in the plane X_{dep} vs. V_G as shown in Fig.10.

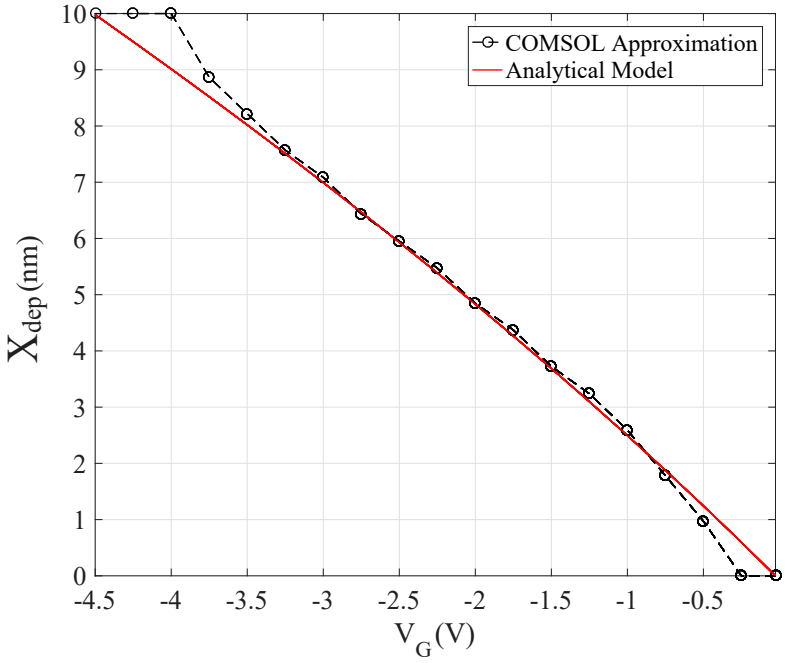

Figure 10. Comparison between analytical model of the depletion region width and its numerical approximation found by using the proposed method.

Simulation results show that we can get a good approximation of the analytical model of the depletion region width by using $n(X_{dep})_{opt}$, which validates the proposed algorithm. The reasons

why these two curves diverge when V_G approaches to V_{FB} and V_{th} are again the inaccuracy of the analytical model in these range of gate voltage ($V_G \simeq V_{th}, V_{FB}$) and the numerical error introduced when the channel or the depletion region become comparable with the dimensions of the mesh used in COMSOL. Finally, we can use $n(X_{dep})_{opt}$ to identify the depletion region boundary from the graphical results generated by COMSOL Multiphysics. To perform this task, we set COMSOL software to create a "countour plot", in the region where the carrier concentration is equal to $n(X_{dep})_{opt}$. Simulation results are shown in Fig.11.

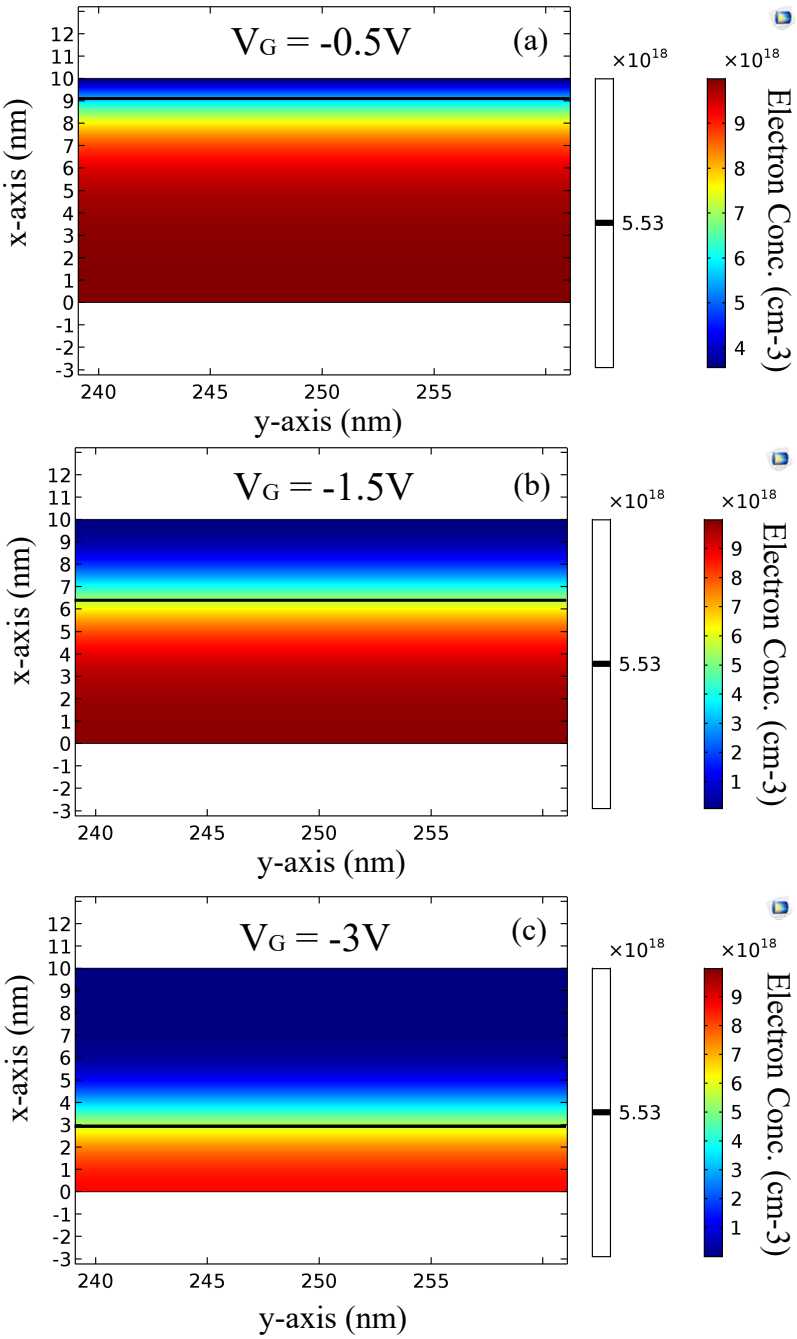

Figure 11. Electron concentration generated by COMSOL Multiphysics, for $t_{Si} = 10nm$ and $V_d = 0V$. The black line represents $n(X_{dep})_{opt}$ (a)$V_g = -0.5V$. (b)$V_g = -1.5V$. (c)$V_g = -3V$.

Fig.11 shows that we can now use COMSOL Multiphysics to determine the position of the depletion region boundary for different values of gate voltage. With this method, we can use the graphical results of COMSOL to determine the depletion region width and the state of the transistor. In addition, we

can use $n(X_{dep})_{opt}$ for those cases when source and drain are connected to different electrical potentials as shown in Fig.12.

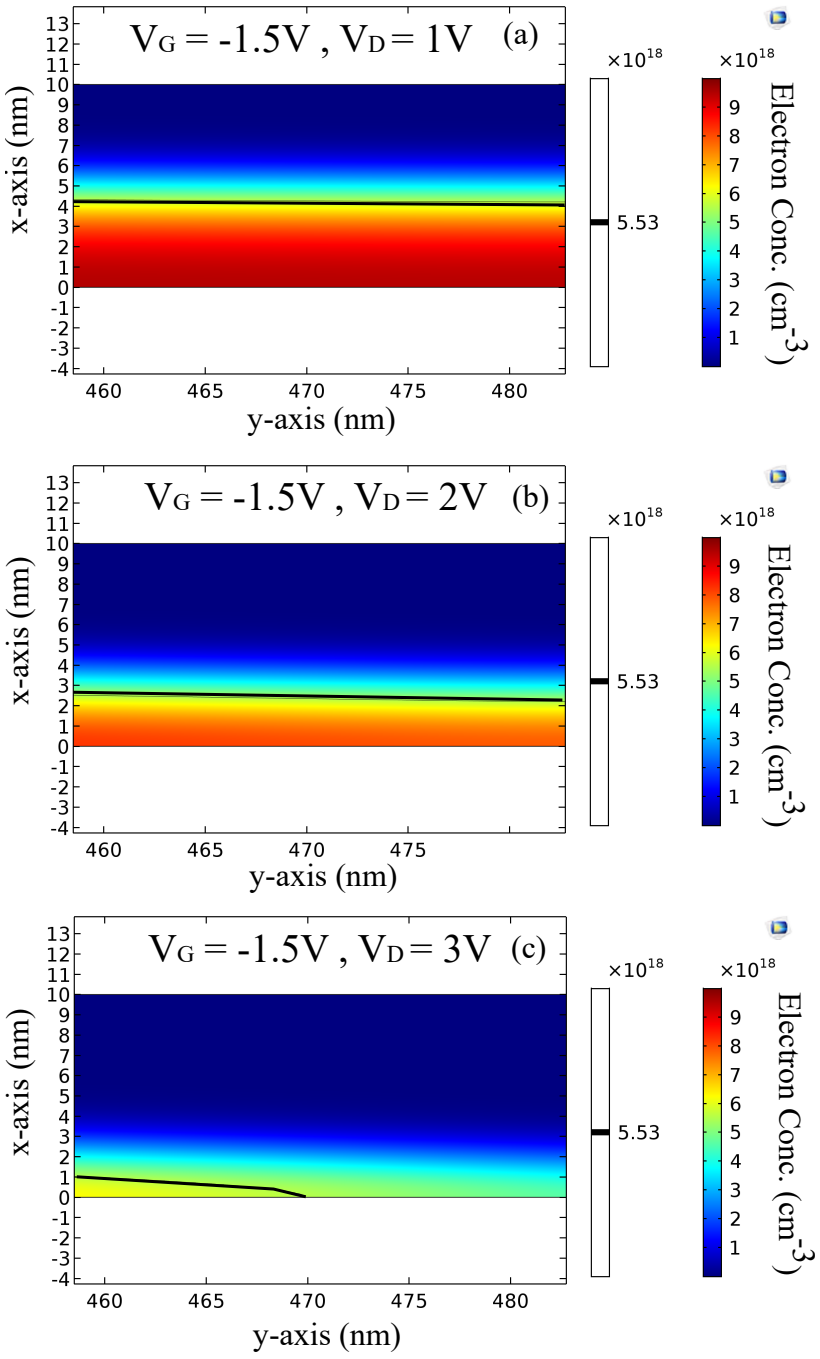

Figure 12. Electron concentration generated by COMSOL Multiphysics, for $t_{Si} = 10nm$ and $V_g = -1.5V$. The black line represents $n(X_{dep})_{opt}$. (a)$V_d = 1V$. (b)$V_d = 2V$. (c)$V_d = 3V$.

From the previous simulation results, we observe that the depletion region tilts as the drain voltage increases. This phenomenon is similar to the channel modulation effect that occurs in MOSFETs. Our method allows to analyze the phenomena inside the PJLT by simply looking to the graphical results provided by COMSOL Multiphysics. The proposed method was then repeated for PJLTs characterized by device layer thickness of 15nm, 20nm with device layer doping of $N_D = 6.12e18cm^{-3}$ and $4.24e18cm^{-3}$ respectively. These values were chosen in order to keep the same gate voltage range.

In this way, all the simulated transistors can be used in real electronic circuits characterized by a single power supply of 5V. Simulation results for these two transistors are shown in Fig.13.

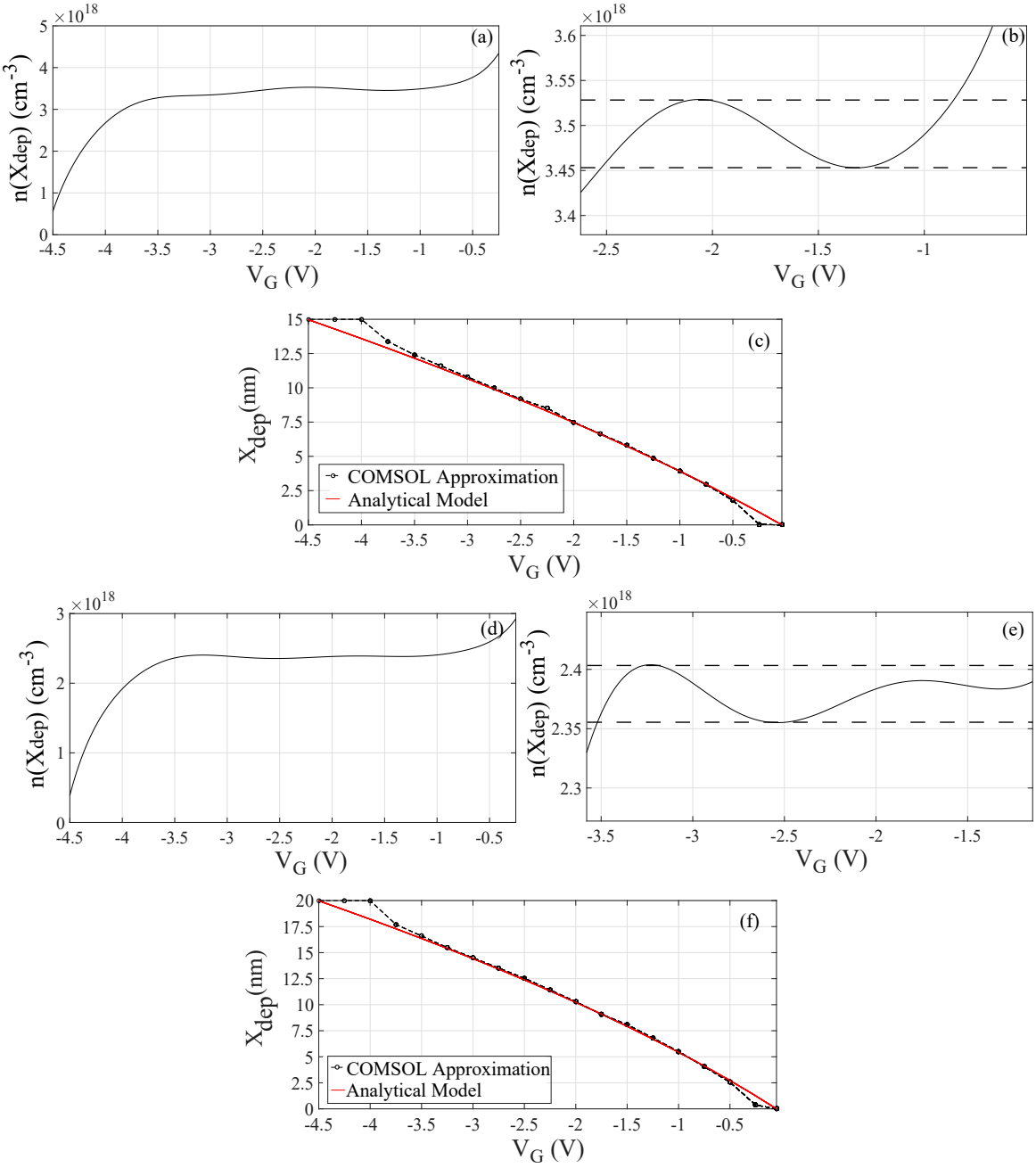

Figure 13. Simulation results for two n-type PJLT. Simulation results for PJLT characterized by $t_{Si} = 15nm, N_D = 6.12 \times 10^{18}$: (a) Electron concentration at the boundary of the depletion region for different values of V_G swept in the range $[V_{FB}, V_{th}]$. (b) Zoom in the middle range of the curve shown in (a). (c) Comparison between the analytical model of the depletion region width and the numerical approximation provided by using the proposed method. Simulation results for PJLT characterized by $t_{Si} = 20nm, N_D = 4.24 \times 10^{18}$: (d) Electron concentration at the boundary of the depletion region for different values of V_G swept in the range $[V_{FB}, V_{th}]$. (e) Zoom in the middle range of the curve in shown (d). (f) Comparison between the analytical model of the depletion region width and the numerical approximation provided by using the proposed method.

Fig.13(a,b,c) show the simulation results for the case $t_{Si} = 15nm$. These plots are similar to the one obtained for the case of $t_{Si} = 10nm$, but the value of $n(X_{dep})_{opt}$ is now $3.49 \times 10^{18} cm^{-3}$. On the

other hand, Fig.13(d,e,f) show the simulation results for the case $t_{Si} = 20nm$. This time, the best value of carrier concentration at the boundary of the depletion region was found to be $n(X_{dep}) = 2.40 \times 10^{18} cm^{-3}$. In both cases, the numerical approximations of the depletion region width shown in Fig.13(c) and (f) seem to fit quite well with the analytical model. This proves that the proposed algorithm provides reasonable results for different values of thickness and doping concentration of the device layer. Finally, Table 2 reports a summary of the values of $n(X_{dep})_{opt}$ found for the three transistors simulated in this paper.

Table 2. Summary of Final Results.

Tsi (nm)	**Device Layer Doping (N_D)** (cm^{-3})	$\mathbf{n(X_{dep})_{opt}}$ (cm^{-3})
10	10^{19}	5.55×10^{18}
15	6.12×10^{18}	3.49×10^{18}
20	4.24×10^{18}	2.40×10^{18}

Interestingly, the results obtained show that $n(X_{dep})opt \simeq (0.55 - 0.57)N_D$.

5. Conclusions

The algorithm proposed in this paper, allows to recognize the depletion region boundary from the graphical results generated in COMSOL Multiphysics. We have found that the carrier concentration at the depletion region boundary is approximately half of the initial doping of the device layer. We have proved that we can extract an approximated curve for the depletion region width by using the proposed method, which fits the analytical model found in literature. Furthermore, we observed that this analytical model doesn't provide a good estimation of the depletion region width when the gate voltage approaches the flat band voltage and the threshold values. The proposed method provides an effective tool, for the design and analysis of a PJLT. Most of all, this method allows to calculate the effective dimensions of the channel, which is fundamental to derive its resistance and the drain current passing through the transistor when there is an electric potential difference between the source and drain terminals. It is worth mentioning that all the results refer to the case of a high doped PJLT. For the case of low doped PJLT, the analytical model provides a greater error and the effects of this error on the proposed method must be investigated.

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Appendix A. Depletion Region Width Analytical Formula

The purpose of this appendix is to clarify the procedure to find the analytical model of the depletion region width in a PJLT. The structure analyzed in this paper is an n-type PJLT shown in Fig.A1.

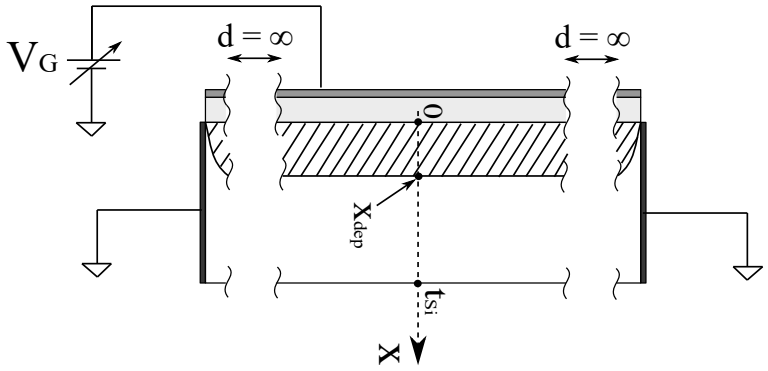

Figure A1. N-type PJLT Ideal Physical Structure

The relation between the gate electric potential and the carriers in the device layer, can be derived by using the differential form of the Gauss Law (Maxwell Equation), which is shown in Eq.(A1).

$$\nabla \vec{E} = \frac{\rho}{\epsilon_{Si}} \tag{A1}$$

Where: $\nabla \vec{E}, \rho$ are the gradient of the electric field and the charge density inside the device layer, while ϵ_{Si} is the dielectric constant of the device layer. The solution of this differential equation can be found by considering a few assumptions.

1. **Uniform material characteristics for the device layer** : $\rho = const. = -|q|N_d$ and $\epsilon_{Si} = const.$ Where: N_d is the doping concentration and q is the charge of an electron (n-type PJLT is considered in this work).
2. **Analysis of a planar JLT** : the physical structure of the JLT analyzed in this work is a planar JLT shown in Fig.A1. This means that Eq.(A1) can be solved just in two dimensions.
3. **Evaluation of the depletion region far from drain and source terminals**: the purpose of this analysis is to evaluate the effect of the gate voltage on the depletion region width. This means that the source and drain electric potential must not affect the shape of the depletion region, in the area where we are supposed to evaluate this parameter. Therefore, in this analysis we consider the case of a PJLT with drain and source terminals infinitely distant from the channel of the transistor as shown in Fig.A1. By doing so, we expect a uniform depletion region beneath the gate insulating layer.
4. **Evaluation of the depletion region along the symmetric axis of the device layer:** since the depletion region is expected to be uniform, then we can limit the domain of Eq.(A1) to a specific direction perpendicular to the substrate of the semiconductor device as shown in Fig.A1. In this way, Eq.(A1) reduces to a differential equation with a single variable (1D problem) as shown in Eq.(A2).

$$\frac{\mathrm{d}E_x(x)}{\mathrm{d}x} = -\frac{|q|N_d}{\epsilon_{Si}} \tag{A2}$$

Where: x is the direction perpendicular to the substrate surface of the device as shown in Fig.A1. Known that the electric potential is related to the electric field by $-\nabla\Phi(x) = \vec{E}$, we obtain the relation between the electric potential and the charge of the carriers inside the device layer, shown in Eq.(A3). This equation is usually known as 1-D Poisson equation [20].

$$\frac{\mathrm{d}^2\phi(x)}{\mathrm{d}x^2} = -\frac{|q|N_d}{\epsilon_{Si}} \tag{A3}$$

Next, by integrating once Eq.(A3), we can find the general solution for the electric field inside the device layer shown in Eq.(A4).

$$E_x(x) = \frac{|q|N_d}{\epsilon_{Si}} x - c_1 \tag{A4}$$

By integrating Eq.(A4) once more we obtain the general solution for the electrical potential inside the device layer as shown in Eq.(A5).

$$\phi(x) = -\frac{|q|N_d}{2\epsilon_{Si}} x^2 + c_1 x + c_2 \tag{A5}$$

Where: c_1 and c_2 are arbitrary constants. To find the value of these two arbitrary constants, we need to define two boundary conditions. The first one can be found by evaluating the electric potential at the interface between the device layer and the thin gate insulating layer. This interface correspond to the potential at $x = 0$. The electrical potential in this point is equal to surface potential ϕ_s, which can be expressed as shown in Eq.(A6).

$$\phi_s = V_G - V_{FB} - V_{OX} \tag{A6}$$

Where: V_G is the electric potential at the gate terminal, V_{FB} is the flat band voltage due to the interface between the device layer and the thin gate insulating layer and V_{OX} is the drop voltage across the thin gate insulating layer. A useful formula of V_{OX} is shown in Eq.(A7). This one can be calculated by integrating the Poisson equation from the metal oxide interface to the bottom of the device layer.

$$V_{OX} = -\frac{|q|N_d}{C_{ox}} X_{dep} \tag{A7}$$

A second boundary condition can be found by introducing an additional approximation.

5. **Device Layer as an Ideal Conductor**: Let's consider the case, that a depletion region is created inside the PJLT. The depletion region is ideally emptied of free carriers (insulator). If we consider the doping of the device layer sufficiently high to mimic the behaviour of an ideal conductor then we can assume that the electric field created by the gate electrode becomes zero ($E_x(X_{dep}) = 0$) at the boundary of the depletion region. In addition, also the electrical potential at the boundary of the depletion region can be assumed to zero, because the device layer has been electrically grounded through the drain and the source terminal ($\phi(X_{dep}) = 0$). By using $\phi(x = 0) = \phi_s$ and $E(x = X_{dep}) = 0$, we can solve the system of equations shown in Eq.(A8) [12].

$$\begin{cases} E_x(x) = \frac{|q|N_d}{\epsilon_{Si}} x - c_1 \\ \phi(x) = -\frac{|q|N_d}{2\epsilon_{Si}} x^2 + c_1 x + c_2 \\ E(X_{dep}) = 0 \\ \phi(0) = \phi_s \end{cases} \tag{A8}$$

The particular solutions of the system is shown in Eq.(A9).

$$\begin{cases} E_x(x) = \frac{|q|N_d}{\epsilon_{Si}} \ (x - X_{dep}) \\ \phi(x) = \phi_s + \frac{|q|N_d}{\epsilon_{Si}} \ X_{dep}\, x - \frac{|q|Nd}{2\epsilon_{Si}} x^2 \end{cases} \tag{A9}$$

Where the arbitrary constants were found to be : $c_1 = \frac{|q|N_d}{\epsilon_{Si}} X_{dep}$ and $c_2 = \phi_s$. Finally, by using Eq.(A6) and Eq.(A7) in Eq.(A9) we can find the formula of the depletion region width shown in Eq.(A10).

$$X_{dep} = -\frac{\epsilon_{Si}}{C_{OX}} + \sqrt{(\frac{\epsilon_{Si}}{C_{OX}})^2 - \frac{2\epsilon_{Si}}{|q|N_d}(V_G - V_{FB})} \tag{A10}$$

Similar procedure can be used to derive the formula of the depletion region for a p-type PJLT. The formula for this case is shown in Eq.(A11).

$$X_{dep} = -\frac{\epsilon_{Si}}{C_{OX}} + \sqrt{(\frac{\epsilon_{Si}}{C_{OX}})^2 + \frac{2\epsilon_{Si}}{|q|N_a}(V_G - V_{FB})} \tag{A11}$$

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