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Master degree in
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Master Thesis

Efficiency optimization and design of analog circuits for a resonant DCDC converter for the LHC experiments upgrade

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Abstract

CERN (the European Organization for Nuclear Research) runs the largest particle physics laboratory in the world. Particle accelerators (in particular the Large Hadron Collider, LHC) and detectors are used at CERN to perform state-of-the-art experiments involving the collision of highly energetic particles.
The High Luminosity LHC upgrade will allow performing more collisions per second, leading to a larger amount of data that can be collected by the detectors. This upgrade entails higher power consumption of the front-end circuits of the detectors and a minimization of the material used, so to optimize the physics performances of the experiments.
Within this context, a specific power distribution system based on two steps of voltage conversion has been proposed, in order to properly supply the front-end circuits. The voltage conversion steps are performed by DCDC converters located close to the collision points, in a harsh environment characterized by high levels of radiations and high magnetic field (up to $4T$). To face this challenge, radiation and magnetic field tolerant DCDC converters based on an Application Specific Integrated Circuit (ASIC) are in development, and several prototypes have been produced.
A Resonant Switched Capacitor converter that targets the last step in the voltage conversion chain has been proposed, designed and prototyped. This converter steps down the voltage from $2.5V$ to $1.2V$ or $1V$, providing a load current up to $3A$. Two different output voltages are required so to properly supply, respectively, the analog and digital front-end circuits.
The first part of this master thesis project has been devoted to the characterization and optimization of this prototype converter, in order to maximize its efficiency and minimize its mass and volume. A full electrical characterization of the converter has been performed together with an efficiency optimization, that has been achieved thanks to a careful choice of the most important passive discrete components.
Basing on the results of the characterization campaign, the re-design of several analog blocks has been carried out in this work: in particular, an improved phase-locked loop (PLL) and a voltage-controlled oscillator (VCO) have been developed. Furthermore, the control circuitry has been modified so to improve the converter performances and reliability.

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Chapter 1

Introduction

1.1 CERN

This Master Thesis project has been developed in the Microelectronics section of CERN, Switzerland, in collaboration with the Institute of Electrical Engineering of EPFL (École Polytechnique Fédérale de Lausanne), Switzerland. CERN (Conseil Européen pour la Recherche Nucléaire) is the European Organization for Nuclear

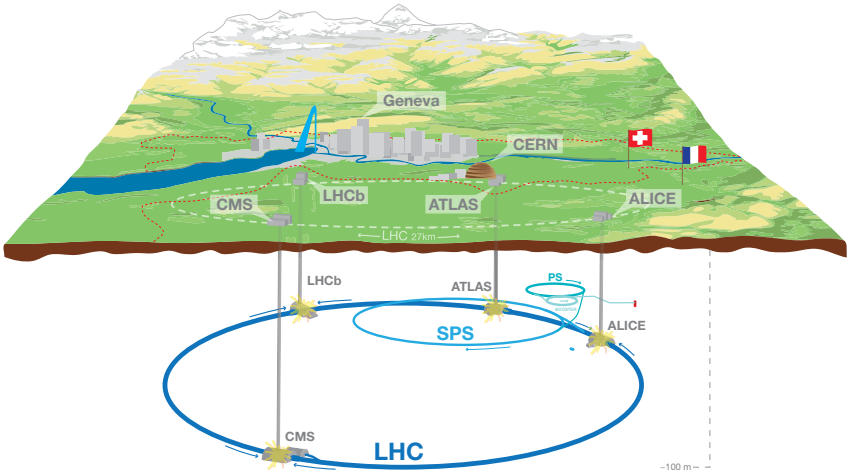


Figure 1.1: LHC: the Large Hadron Collider accelerator.

Research. It has been founded in 1954 as an European research facility that could be a world-class excellence in nuclear physics [1]. Its main mission is to push further the boundaries of human knowledge, investigating the structure of matter.
In this field, many important achievements have been obtained: for example, the first evidences of the weak force were found between the 1970s and 1980s, and more recently (in 2010) the Higgs boson was detected for the first time. While fundamental research is the main focus at CERN, the development of new technologies is vital in order to provide physicists the proper research tools. As an example, the most famous tool developed by CERN scientists is without doubts the World Wide Web.
In this framework, many research groups work for the future upgrades of the experimental apparatus, among these also the Microelectronics group plays an important role.

CERN uses high-energy collisions between charged particles (protons or heavy ions) in order to study the behaviour of particles and to detect new ones. Indeed, the particles are accelerated at a speed that is very close to the speed of light, and the protons collision energy is about 13TeV.
CERN experimental apparatus is very complex and is composed in particular of two elements:

- accelerators:
  once the particle beam is created, it moves through a series of accelerators that progressively increase the energy of the charged particles. The last element in this acceleration chain is the LHC (Large Hadron Collider), a 27km long ring accelerator that is located about 100m deep underground (as depicted in Figure 1.1). Inside the LHC, two counter-rotating beams of protons or heavy ions run, guided by superconducting magnets. The collisions between the beams occur in different points of the ring, where detectors analyze the products of the collisions;

- experiments:
  a detector and its related infrastructure constitute an experiment. Four main experiments are located along the LHC: ALICE, ATLAS, CMS and LHCb. In particular, ATLAS and CMS are the biggest experiments, they have been designed to be able to detect the largest possible range of particles. Moreover, producing the collisions in more than one experiment is fundamental for the cross confirmation of data and new discoveries.

The experiments are complex apparatus gathering different sub-detectors together, in order to provide as much information as possible on the particles produced during the collisions. In particular, the main devices employed inside each experiment are the following:

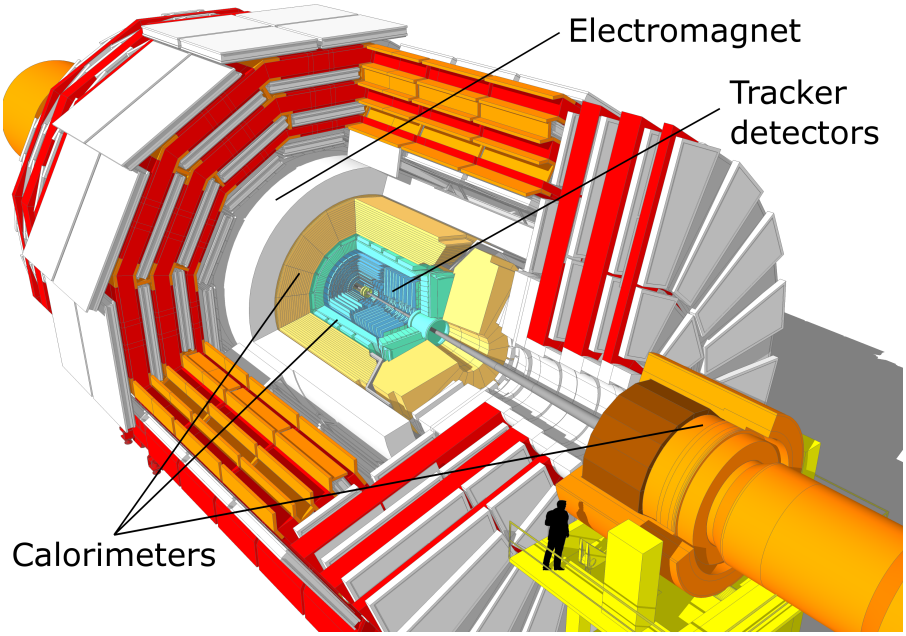


Figure 1.2: Structure of the CMS experiment.

- electromagnet: it is a magnet that generates a strong magnetic field inside the experiment, this bends the trajectory of the charged particles;
- calorimeters: passive layers of materials that are used to stop and absorb the travelling particles, gathering information about their energy;
- tracker detectors: an ensemble of devices that record the path followed by charged particles.

The structure of the CMS experiment is shown together with its most important components in Figure 1.2.

The whole apparatus is subjected to a high level of radiation. Therefore, all the electronics that are installed inside each experiment must be radiation tolerant, withstanding a total ionizing dose up to hundreds of Mrad during their lifetime ($1rad = 0.01J/kg$).

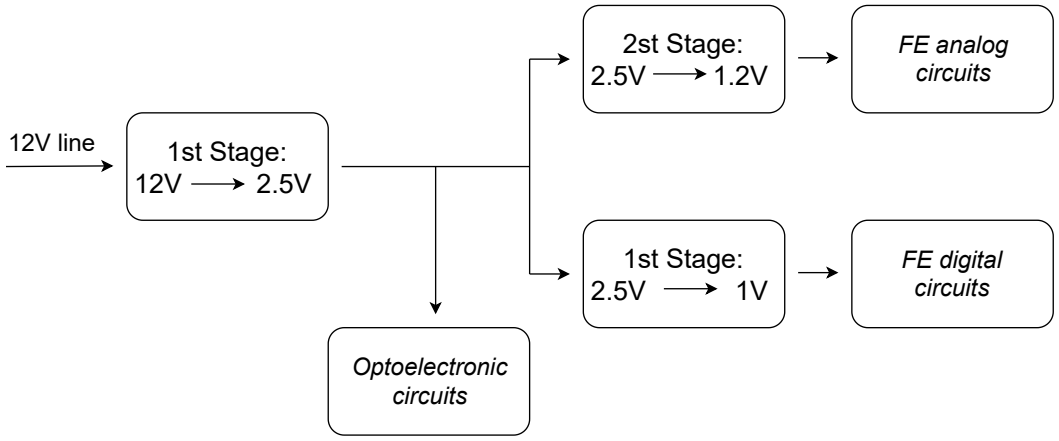


Figure 1.3: Power distribution architecture for the LHC experiment upgrades.

1.2 Development of DCDC converters for the LHC experiment upgrades

The front-end electronic circuits detect the products of the collisions and are located in proximity to the collision point. Currently, they are mostly powered by supplies located outside the experiment cavern. The current flowing inside the long cables used produces power losses equal to $P_{loss} = RI^2$.
The High-Luminosity LHC experiment upgrades will enable the collection of significantly more data compared to the current run. Increased power consumption is expected from the front-end circuits, while the amount of material used must be minimized, not to interfere with the physics performances of the experiments. The resistance of the cables could be minimized in order to reduce the power dissipation, however this involves the usage of bulkier cables. The usage of thin cables could reduce the amount of material, but the heat produced by the additional power losses would involve an increased load for the cooling system.
A proposal that entailed a re-thinking of the power distribution system has been approved and pursued [2]: The power could be transferred at a higher voltage (lower current) through the long cables, and then it could be locally converted to the proper voltage required by the front-end modules. In this way, it is possible to transfer power using thin cables and to lower the power dissipation thanks to the reduced electric current that flows through the cables.
As depicted in Figure 1.3, different voltage domains have to be generated in order to properly supply the Optoelectronic circuits, the Analog and Digital Front End circuits: an efficient and compact power distribution system for this purpose steps down in different stages.

The voltage conversion is performed by DCDC converters located inside the detectors, exposed to a harsh environment characterized by radiations and magnetic field. In this framework, the research activity aiming to design radiation-hard and magnetic field tolerant DCDC converters begun in 2008. [3]. The converters are based on Application Specific Integrated Circuits (ASICs) and use some discrete components, among which an inductor. Due to the large magnetic field present in the experiments (up to 4T), no ferromagnetic-core inductor can be used, and the bulkier air-core inductors must be adopted. In order to reduce the size and weight of the converter (not to affect the physics performances of the experiments, and to allow an easier integration), the inductor size must be minimized.
The chosen topology for the first stage of conversion is that of the buck converter, thanks to its simplicity and its overall high efficiency.
For the second stage, two converters employing different architectures are in development: a buck converter and a Resonant Switched Capacitor converter. The latter is characterized by smaller dimension and weight with respect to the buck converter, still providing comparable efficiency, at the price of a more complex architecture.
The current loads that this converter should be able to supply falls in the range:

$$0A < I_{load} < 3A \tag{1.1}$$

The first objective of this work is to fully characterize a prototype Resonant Switched Capacitor converter based on an ASIC (presented in [4]), optimizing its performances by selecting the proper discrete components and ASIC configuration.
The second objective is to design analog blocks that improve the converter performances, basing on the results of the characterization campaign.

Chapter 2

Analysis of a ReSC converter

2.1 Switched Capacitor (SC) converters

Switched Capacitor (SC) DCDC converters use only capacitors and switches to achieve voltage regulation, differently from inductor-based converters (such as the buck converter), which employ also bulky magnetic components. Indeed, SC power supplies have been developed in order to reduce the volume occupied by the converters, so to be easily integrated on chip [5, 6, 7]. Therefore, this could have been an interesting architecture for the DCDC converter necessary for the upgrades of the LHC experiments. However, the reduced size comes at the price of large electrical stress on the employed components: indeed, large current spikes occur at the switching instants, also causing significant losses. Another drawback of this family of devices is the sensitivity of its efficiency to line or load variation: in order to achieve an efficient voltage conversion over a wide range of $\frac{V_{in}}{V_{out}}$ ratios, complex

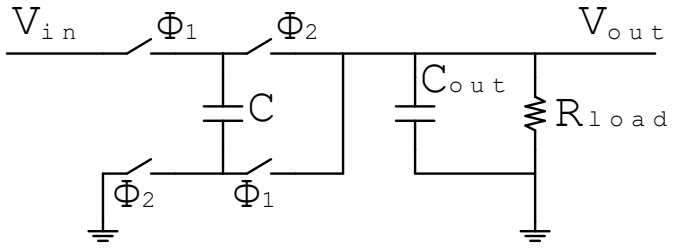


Figure 2.1: Switched capacitor converter achieving $\frac{Vin}{Vout} = \frac{2}{1}$ voltage conversion.

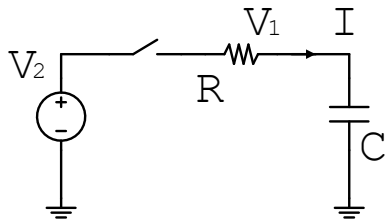


Figure 2.2: Power dissipation mechanism for a single switched capacitor.

architectures should be employed.
As an example, the schematic depicted in Figure 2.1 shows a Switched Capacitor converter with ratio $\frac{V_{out}}{V_{in}} = \frac{1}{2}$.
The voltage across capacitor C is switched between $V_{in} - V_{out}$ and V_{out} with 50% duty cycle; assuming $C_{out} \gg C$, lossless operation and zero load, the conversion ratio can be calculated as follows:

$$\begin{aligned} \Phi_1 : V_C &= V_{in} - V_{out} \\ \Phi_2 : V_C &= V_{out} \\ \frac{V_{out}}{V_{in}} &= \frac{1}{2} \end{aligned} \tag{2.1}$$

In a real application, any capacitor has a non-zero series parasitic resistor. For a single switched capacitor as the one represented in Figure 2.2, it is possible to derive the expression of the current that charges the capacitor, which produces at the same time losses in the parasitic resistor.

$$I_{charge}(t) = \frac{V_2 - V_1}{R} e^{-\frac{t}{RC}} \tag{2.2}$$

The instantaneous power loss in the parasitic resistor at time t is equal to: $P_{loss}(t) = RI^2_{charge}(t)$. By integrating the current over the time needed to fully charge the capacitor, it is possible to find the value of the energy dissipated in a complete charging process.
In particular, considering the charging period $t_{on} \gg RC$, the energy loss would be:

$$E_{loss} = \int_0^{t_{on}} RI^2(t)dt \approx \frac{1}{2}C(V_2 - V_1)^2 \tag{2.3}$$

As suggested by equation 2.3, the charging and discharging process introduces losses even for a null parasitic resistance when $V_2 \neq V_1$. This implies that the efficiency of

a SC converter is always degraded when the conversion ratio is different from the ideal one (i.e. $\frac{1}{2}$ for the converter shown in Fig. 2.1) [8, 9].
Moreover, the exponential shape of the current shown by equation 2.2 suggests that at each commutation current spikes might occur, causing an increased current stress for the used devices, while also leading to higher switching losses.

Since high efficiency is a crucial requirement for the upgraded LHC detectors, this type of converter has not been considered as a possible alternative to the buck converter.

A Resonant Switched-Capacitor converter can be obtained from the SC converter shown in Figure 2.1 by employing an additional small inductor in series with the switched capacitor. This allows to improve significantly the performances, as detailed in the followings.

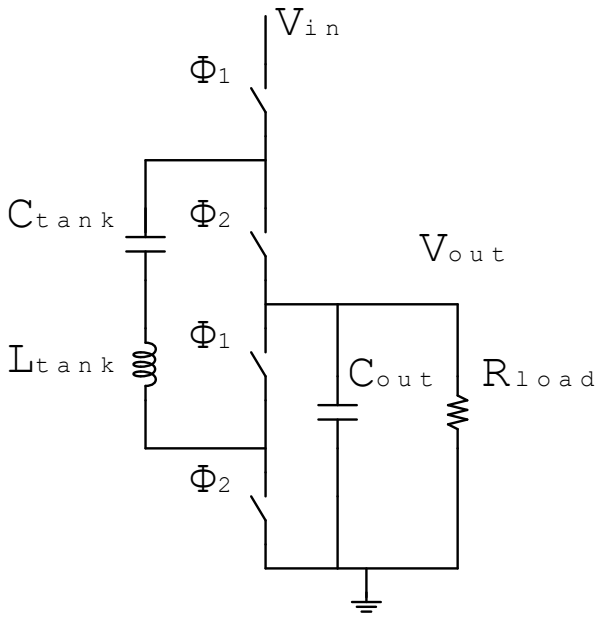


Figure 2.3: Resonant Switched-Capacitor converter.

2.2 Resonant Switched Capacitor converters

Resonant Switched Capacitor (ReSC) converters have been introduced by [10]. As SC converters, they use a capacitor as the main energy storage device, while in the ReSC architecture a small inductor is added in series to allow soft charging [11, 12]. This last element prevents the occurrence of voltage steps on the capacitor and it eliminates the current spikes that occur at the switching instants in SC converters. In addition, the ReSC architecture can achieve Soft Switching, a lossless process that will be detailed in section 2.2.2.
These improvements come at the price of using an additional inductor. Still, this converter allows to reach efficiencies that are comparable to those of a buck converter, while featuring a much smaller inductor, as shown by [13].
The schematic of a 2:1 ReSC converter is shown in Figure 2.3. The LC circuit is periodically connected with 50% duty cycle to $V_{in} - V_{out}$ (during ϕ_1) and to V_{out} (during ϕ_2).
Due to its low volume and to its high efficiency, the ReSC architecture has been chosen for the application in the upgraded LHC detectors.

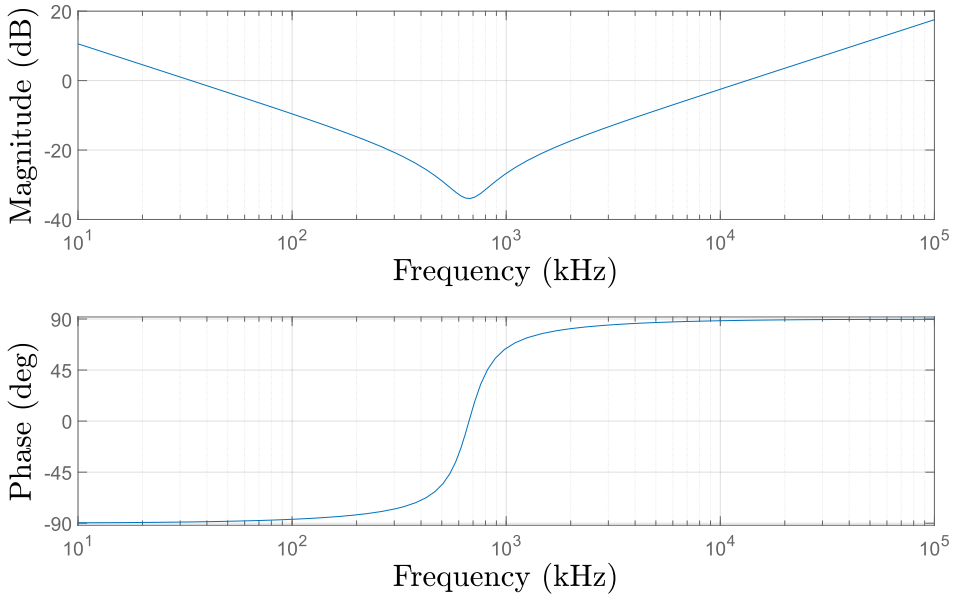


Figure 2.4: Tank impedance characteristics in frequency.

2.2.1 Tank circuit properties

The LC tank is formed by lossless elements that are able to store energy either in their electric or their magnetic field.
An important property of this circuit is that it is characterized by a resonance frequency, which is defined as the frequency at which the net reactance of the tank is zero:

$$Z = Z_L + Z_C = j\omega L + \frac{1}{j\omega C}$$
$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \tag{2.4}$$

In response to a voltage step across the LC circuit, the capacitor voltage and the inductor current (called the state variables) show a sinusoidal shape at the resonant frequency: the energy is periodically exchanged between the capacitor and the inductor.

However many elements introduce losses in a real circuit: the on resistance of the power switches, the interconnections and the series parasitic resistances of the inductor and of the capacitor. The resulting RLC circuit is still characterized by its resonance frequency, but the amplitude of the state variables response to an input voltage step decreases in time.

The damping effect is due to the presence of the series parasitic resistance: indeed, the energy that is transferred between the capacitor and the inductor is partially dissipated each time the charges flow through the resistor while being exchanged from one lossless element to the other.
The impedance magnitude and phase of the RLC series circuit is shown in Figure 2.4 (for $L_{tank} = 12nH$, $C_{tank} = 4.7\mu F$ and $R = 20m\Omega$, which are realistic values for a second-stage ReSC DCDC converter for the LHC experiments).
A key parameter that evaluates how much energy is dissipated at resonance with respect to the energy stored is the quality factor:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{2.5}$$

Considering the Kirchhoff voltage law and the constitutive equation of each element, it is possible to obtain the differential equation that fully describes the evolution of the tank current:

$$\frac{d^2}{dt^2}I(t) + 2\alpha\frac{d}{dt}I(t) + \omega_0^2 I(t) = 0 \tag{2.6}$$

where α is the attenuation and is defined as $\alpha = \frac{R}{2L}$.
A parameter related to α, to the resonance frequency and to the quality factor is the damping factor:

$$\zeta = \frac{\alpha}{\omega_0} = (2Q)^{(-1)} = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{2.7}$$

Depending on the value of the damping factor ζ, so depending on the values of the RLC circuit components, the differential equation 2.6 has three different solutions.
This means that three different transient current responses of the circuit to a voltage excitation are possible depending on the tank characteristics:

- $\zeta > 1$: overdamped response, the transient current decays exponentially without oscillations;
- $\zeta = 1$: critically damped response, the transient current decays exponentially behaving as an overdamped response, showing the fastest possible decay;
- $\zeta < 1$: underdamped response, the transient current oscillates (at frequency $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$) and its amplitude decays exponentially in time.

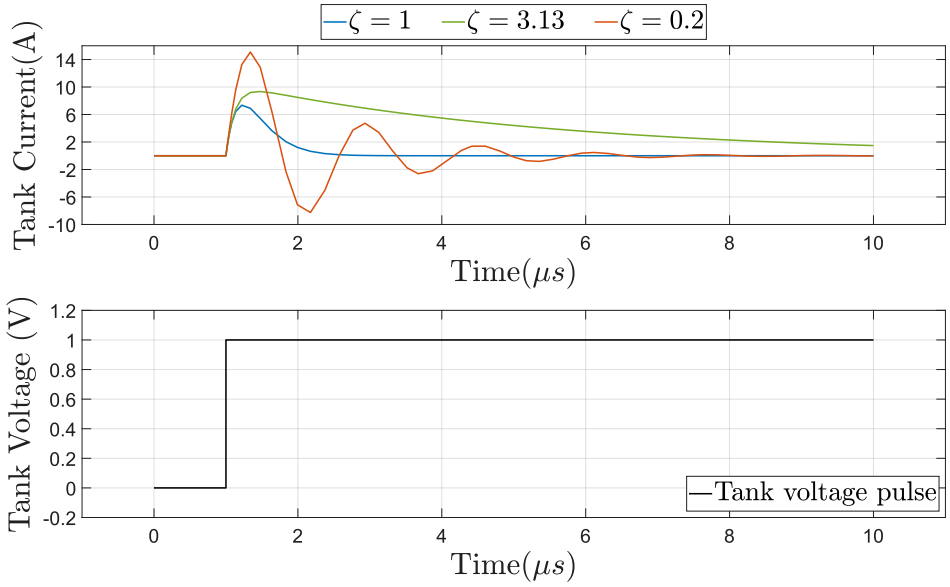


Figure 2.5: Voltage excitation and current responses of different tank circuits.

The three different types of current responses are reported in Figure 2.5.
For this simulation, a voltage excitation of amplitude $V_{tank} = 1V$ has been applied to different tank circuits, and the initial conditions for both state variables have been set to zero.
The following components for the tank have been selected in order to show the three different current responses:

- overdamped response:
  $C_{tank} = 47\mu F \quad L_{tank} = 12nH \quad R_{tank} = 100m\Omega \quad \zeta = 3.13;$
- critically damped response:
  $C_{tank} = 4.7\mu F \quad L_{tank} = 12nH \quad R_{tank} = 101m\Omega \quad \zeta = 1;$
- underdamped response:
  $C_{tank} = 4.7\mu F \quad L_{tank} = 12nH \quad R_{tank} = 20m\Omega \quad \zeta = 0.2.$

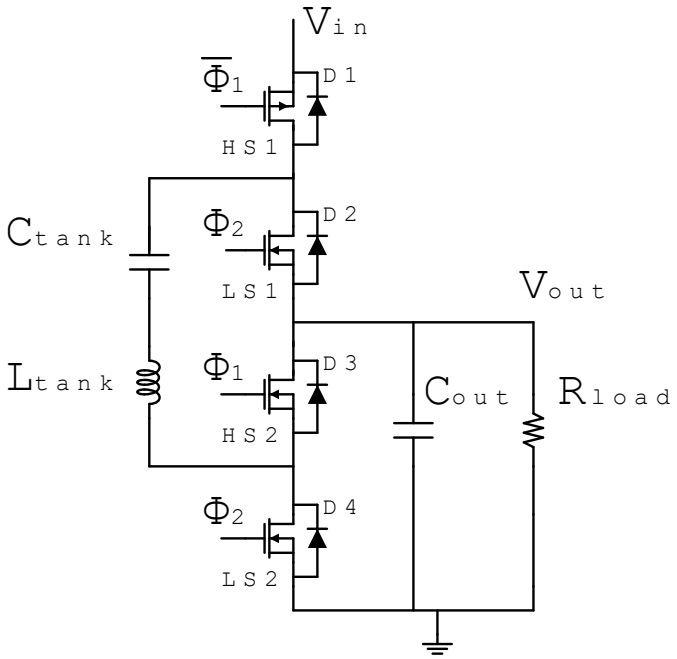


Figure 2.6: Resonant Switched Capacitor converter and bulk diodes.

2.2.2 Soft Switching

The ReSC converter can take advantage of Soft Switching mechanisms: Zero Current (ZCS) and Zero Voltage switching (ZVS) [14]. In particular, this happens if the transistors are switched on or off while either their current (I_{ds}) or respectively their voltage (V_{ds}) is zero. These processes suppress the switching losses, allowing the device to work at high frequency while maintaining high efficiency.
Figure 2.6 shows the schematic of the ReSC converter including the switching transistors, their bulk diodes and their control signals. The following simplified analysis aims at explaining how the soft switching process can be achieved for a single transistor of the ReSC converter.
The forward voltage of the bulk diodes is assumed to be zero. The tank is periodically connected between $V_{in} - V_{out}$ (during $\Phi 1$) and V_{out} (during $\Phi 2$): this results in a square wave excitation of the tank V_t.
Supposing that the excitation occurs at a frequency $f_{switching}$ close to the resonant frequency and that the tank is underdamped, the current I_t flowing in the tank can be well approximated by a sinusoidal waveform I_{t0} with frequency $f_{switching}$. The current response at higher harmonics of V_t can be neglected.

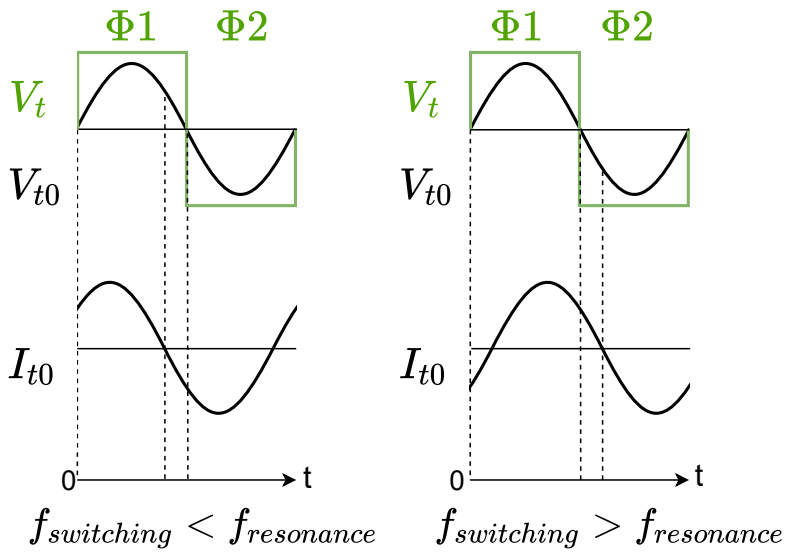


Figure 2.7: Voltage and current waveforms of the ReSC above and below resonance.

At switching frequencies lower than resonance the tank impedance is dominated by the capacitor (as shown in Figure 2.4), and the current response of the tank shows a phase lead with respect to the fundamental component of the tank voltage excitation V_{t0}. The tank current and voltage waveforms are shown in Figure 2.7. At the beginning of phase $\Phi 1$, transistor $HS1$ starts conducting a positive current. Before the switching instant, the current changes its sign becoming negative, it stops flowing through $HS1$ and it passes through diode $D1$. At this point the transistor $HS1$ can be turned off without any power dissipation. This process is called Zero Current Switching.

On the other hand, when the switching frequency is higher than resonance the tank impedance is dominated by the inductor, so the tank current shows a phase lag with respect to the fundamental component of the voltage excitation V_{t0}. As shown in Figure 2.7 just before the transistor $HS1$ is turned on ($t < 0$) the tank current is negative and it flows through $D1$. Since the drain-to-source voltage of $HS1$ is zero the transistor can be turned on without losses. In this case when the current presents a phase lag with respect to the voltage it is also possible to switch off $HS1$ without losses if the capacitance between the source and the drain of $HS1$ is large enough. Indeed, the drain-to-source capacitance can keep the V_{ds} of $HS1$ to a negligible value during the turn-off operation.

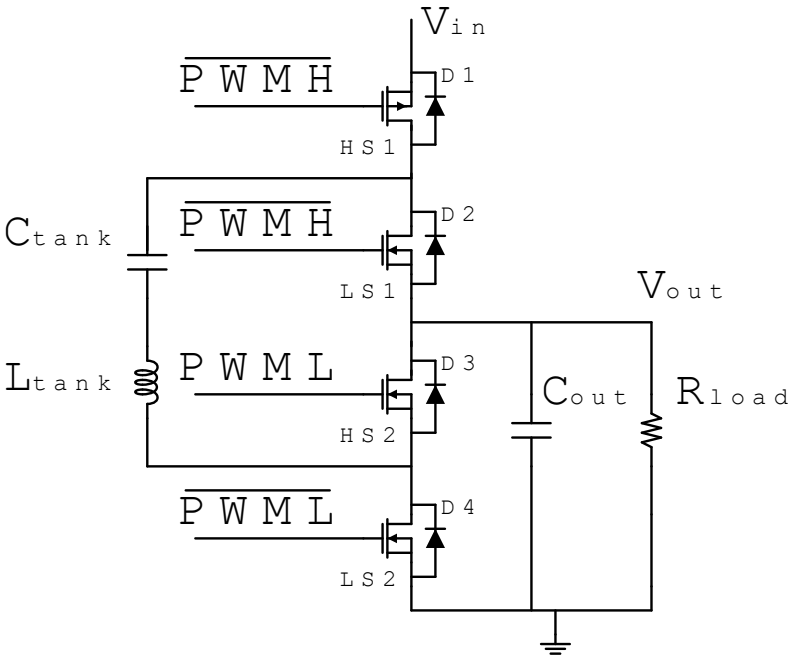
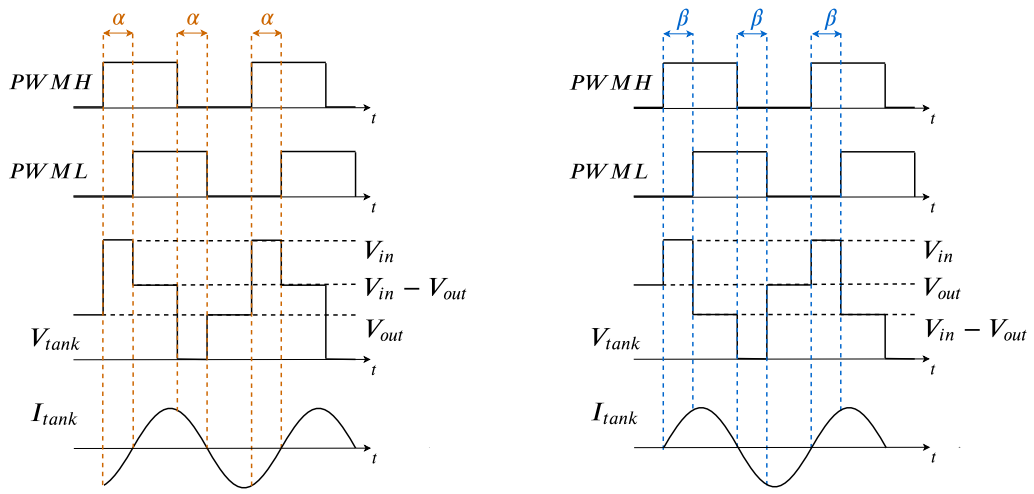


Figure 2.8: ReSC schematic with the real driving signals for the switches.

2.3 ReSC operation modes

A prototype radiation and magnetic field tolerant 2:1 ReSC converter has been developed at CERN [15]. It is based on an ASIC designed in a 130 nm CMOS technology. Such prototype features a novel control circuitry that optimizes the efficiency at all loads by using different operation modes [4].
The Normal operation mode ensures high efficiency at high load currents ($I_{load} > 1A$), while it is inherently inefficient at lighter loads.
Therefore, alternative modes have been developed in order to achieve high efficiency at low load currents ($I_{load} < 1A$): the Burst mode and Medium/Light load operation modes.



(a) α mode (b) β mode

Figure 2.9: Voltage and current waveforms of the ReSC in normal mode.

2.3.1 Normal mode

In Normal mode, the switching frequency is larger than the tank resonant frequency, and the output voltage regulation is achieved by tuning the phase shift between the driving signals $PWMH$ and $PWML$ signals (see Figure 2.8).
Using this driving scheme, it can be shown that the converter can achieve output voltage regulation for a wide range of conversion ratios.

When $V_{out} < \frac{V_{in}}{2}$, the control circuit forces $HS2$ and $LS2$ (driven by PWML) to switch synchronously with the tank current, while it imposes a phase lead α of PWMH (the driving signal of $HS1$ and $LS1$) from PWML. This mode of operation is called α mode: its related current and voltage waveforms are shown in Figure 2.9a. Since the first harmonic of the tank voltage always has a phase lead from the tank current, the switching frequency is above the tank resonance.
Being $PWML$ synchronous with the tank current, $HS2$ and $LS2$ are switched at Zero Current, while Zero Voltage Switching is achieved for $HS1$ and $LS1$. Indeed, when $PWMH$ switches to the logic high value, $HS1$ is switched on while the negative tank current flows through its bulk diode $D1$, allowing $HS1$ to turn on at zero voltage. Analogously, when $PWMH$ switches to the logic low value $D2$ starts conducting the positive tank current before the corresponding MOSFET $LS1$ is turned on at zero voltage.

On the other hand, when $V_{out} > \frac{V_{in}}{2}$ $HS1$ and $LS1$ are forced to switch at the zero-crossing instants of the tank current, while $PWML$ has a phase lag β from

$PWMH$. This mode of operation is called β mode: its related current and voltage waveforms are shown in Figure 2.9b. Similarly to α mode, the tank voltage excitation has a phase lead from the tank current, forcing the converter to work above resonance.
$HS1$ and $LS1$ are switched at Zero Current, while $HS2$ and $LS2$ switch at Zero Voltage. When $PWML$ switches to the logic high value, $LS2$ is turned off and the positive tank current flows through diode $D3$, allowing transistor $HS2$ to switch on at zero voltage. When $PWML$ switches to the logic low value, the diode $D4$ starts conducting the negative tank current before its corresponding transistor $LS2$ is turned on at zero voltage.

The developed controller imposes a phase shift between the tank excitation voltage and the tank current. Such phase shift correspond to a certain frequency of operation, according to the tank impedance shown in Figure 2.4. The tank current is delivered to the load when $PWMH$ and $PWML$ are '1'(Phase 2 in Figure 2.10) and when $PWMH$ and $PWML$ are '0' (Phase 4 in Figure 2.10).

As the load current decreases, the switching frequency increases in normal mode: a progressively decreasing load current requires a smaller amplitude of the tank current. Therefore, the tank impedance magnitude must be made larger, and thus the controller makes the switching frequency higher. This however leads to a large degradation of the efficiency at low load currents ($I_{load} < 1A$), due to the increased driving losses and inductor resistance (due to skin effect). For this reason, different operation modes have been developed in order to achieve high efficiency at low load currents ($I_{load} < 1A$).

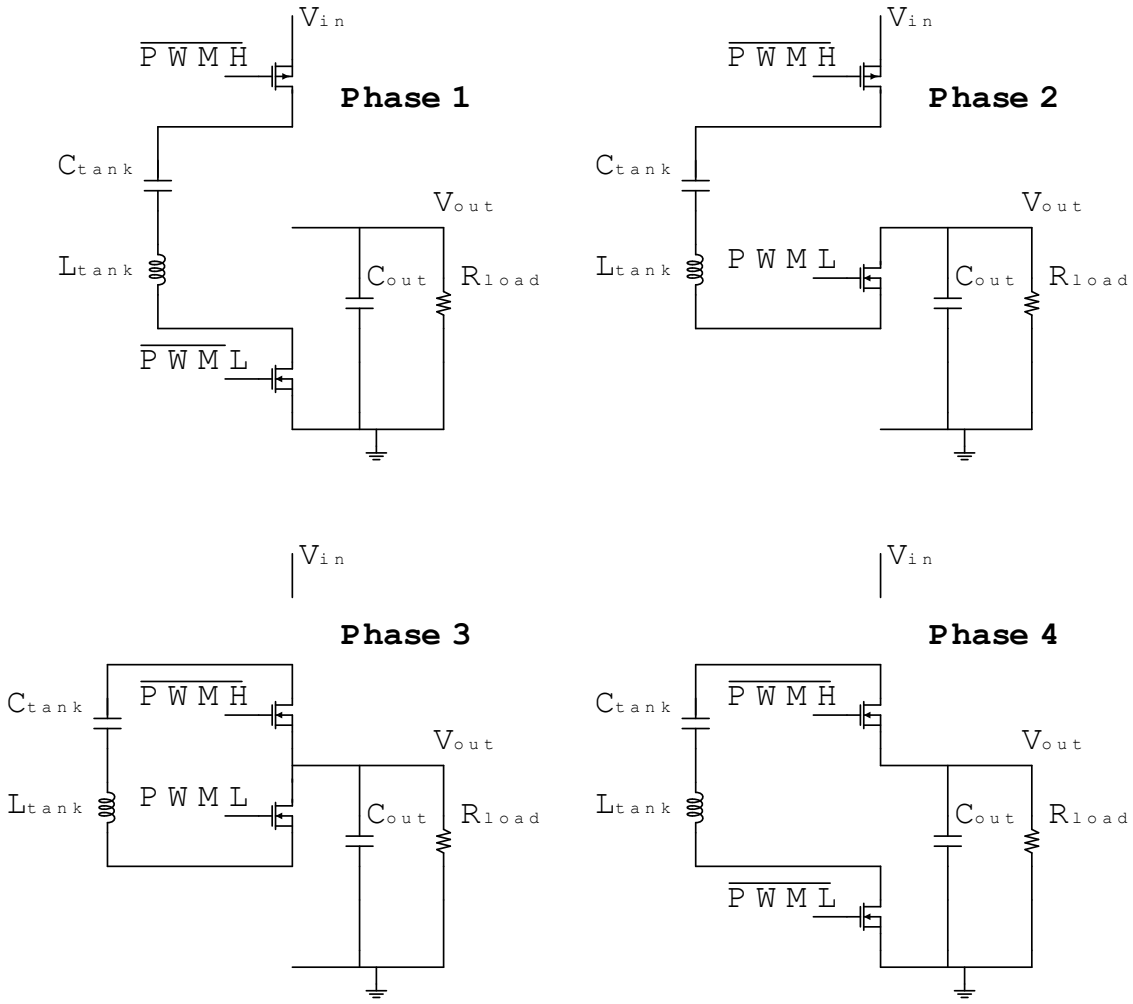


Figure 2.10: Four phases excitation of the ReSC converter.

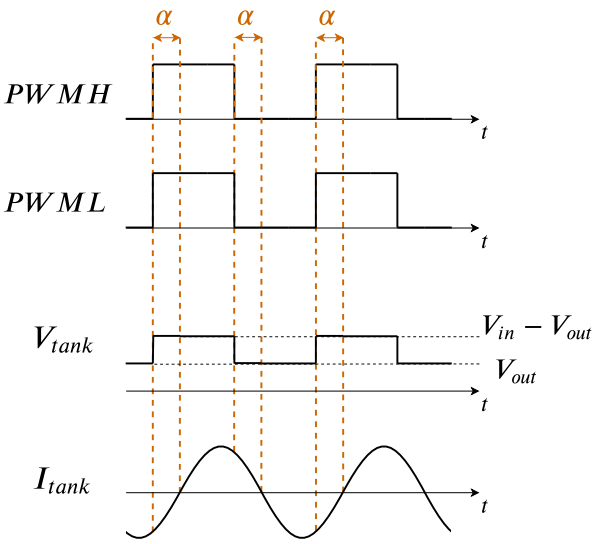


Figure 2.11: Voltage and current waveforms of the ReSC in medium-load mode.

2.3.2 Medium-load mode

The Medium-load operation mode has been designed to intervene when the normal operation mode becomes too inefficient. In this case, the $PWMH$ and $PWML$ waveforms are forced to be synchronous (the tank voltage can be either $V_{in} - V_{out}$ or V_{out}, and they both exhibit a phase lead α from the tank current waveform (see Figure 2.11. Therefore, the converter works above resonance.
The amplitude of the tank excitation voltage is reduced compared to normal mode, and a certain amplitude of the tank current in medium-load mode is achieved at lower frequencies compared to normal mode. This is the main advantage of this operation: it allows achieving voltage conversion at a lower switching frequency compared to normal mode for the same load current, limiting the impact of the frequency-dependent losses.

As in normal mode, the soft switching mechanism plays an important role in boosting the overall efficiency in medium-load mode. Indeed, when $PWML$ and $PWMH$ switch to the logic state '1', the diode $D1$ conducts the negative tank current before $HS1$ is turned on, leading to zero voltage switching for this MOSFET. At the same time, zero current switch off is obtained for $LS2$, while $LS1$ can be turned off at zero voltage if its source-to-drain capacitance is large enough.
On the other hand, when both driving signals become '0', it is possible to switch on $LS1$ at zero voltage, while $HS2$ is turned off at zero current. If the source-to-drain

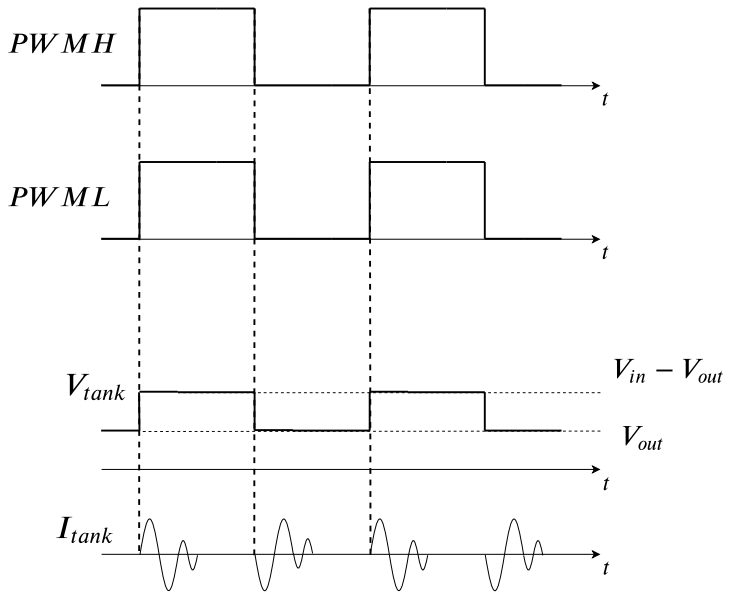


Figure 2.12: Voltage and current waveforms of the ReSC in light-load mode.

capacitance of $HS1$ is large enough, this transistor can be switched off at zero current.

However, as shown in Figure 2.11 part of the current injected towards the load is negative. The impact of the negative portion of the current that is driven towards the load increases with the increase of the phase lead α, leading to a large tank RMS current for large α.
Consequently, moving to very low current loads ($I_{load} < 0.5A$) in medium-load mode would cause a large degradation of the efficiency, due to the increased switching frequency and to the increased impact of the negative current injected on the load.

2.3.3 Light-load mode

This operation mode has been designed to intervene when the medium-load operation becomes too inefficient ($I_{load} < 0.5A$). As in medium-load, $PWMH$ and $PWML$ are synchronized (the tank excitation voltage can be either $V_{in} - V_{out}$ or V_{out}, see Figure 2.12), but in this case the switching frequency is below resonance. Since the switching frequency is below resonance, the tank impedance is characterized by a capacitive behaviour, leading to lower the switching frequency when the load current is decreased (since the tank impedance magnitude increases for a lower frequency). Even if the soft switching operation is not achieved in light-load mode, the low frequencies employed largely reduce the frequency-dependent losses and make this operation efficient for very low current loads.
The main drawback of this operation is that it is characterized by a greater output voltage ripple with respect to normal and medium-load modes.

2.3.4 Burst mode

This operation mode is an alternative to the medium-load and light-load modes and it consists of an intermittent normal operation mode.
When working at low load currents in normal mode ($I_{load} < 1A$) the frequency of operation would increase a lot leading to a large degradation of the efficiency; by imposing a limitation on the phase shift α, it is possible to limit the switching frequency. However this would limit the minimum current value that can be provided to the load.
If the frequency is limited and the converter works in normal mode at too low load currents, the current delivered to the load is higher than necessary. This makes the output voltage increase above the desired value. If the converter stops switching, the output voltage is instead naturally discharged by the load.
The burst mode allows the converter to achieve voltage regulation at low current loads by periodically stopping the switching operation of a tank whose switching frequency has an upper limit. This however intrinsically causes a considerable output voltage ripple.

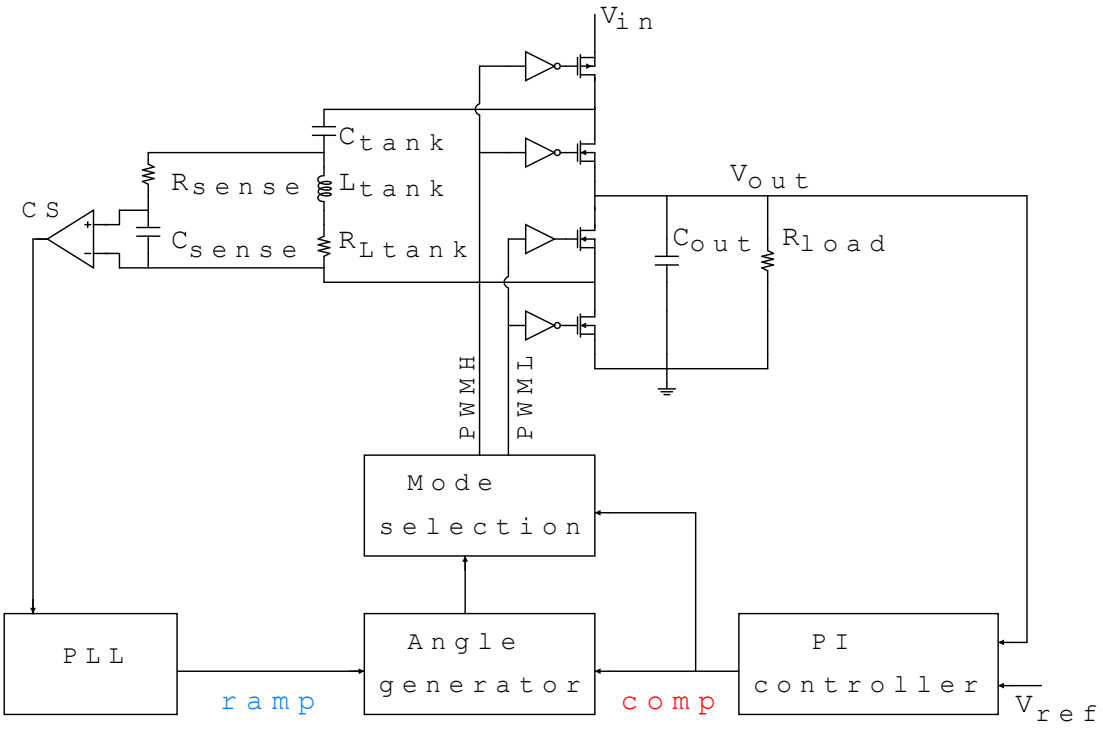


Figure 2.13: Block diagram of the control circuit of the prototype ReSC converter.

2.4 Closed Loop control of the ReSC

The prototype ReSC converter developed for the upgraded LHC experiments features a novel control circuit [4], whose schematic is shown in Figure 2.13. This system is designed to provide the proper phase shift between $PWMH$ and $PWML$ in order to achieve output voltage regulation. It is based on a zero crossing detector for the tank current, which uses an RC filter located in parallel to the tank inductor L_{tank} (see Figure 2.14a).
Indeed, it can be shown that the voltage across the capacitor C_{sense} is:

$$V_{C_{sense}} = I_{L_{tank}} R_{L_{tank}} \frac{1 + s\frac{L_{tank}}{R_{L_{tank}}}}{1 + sR_{sense}C_{sense}} \tag{2.8}$$

If the pole and the zero of the transfer function coincide ($\frac{L_{tank}}{R_{L_{tank}}} = R_{sense}C_{sense}$), then the voltage across the sense capacitor $V_{C_{sense}}$ reproduces the tank current. This signal is fed to a voltage comparator, allowing the detection of the zero-crossing instants of the tank current. In particular, the output signal of the comparator is called CS and it is in logic state '1' when the tank current is positive and in logic

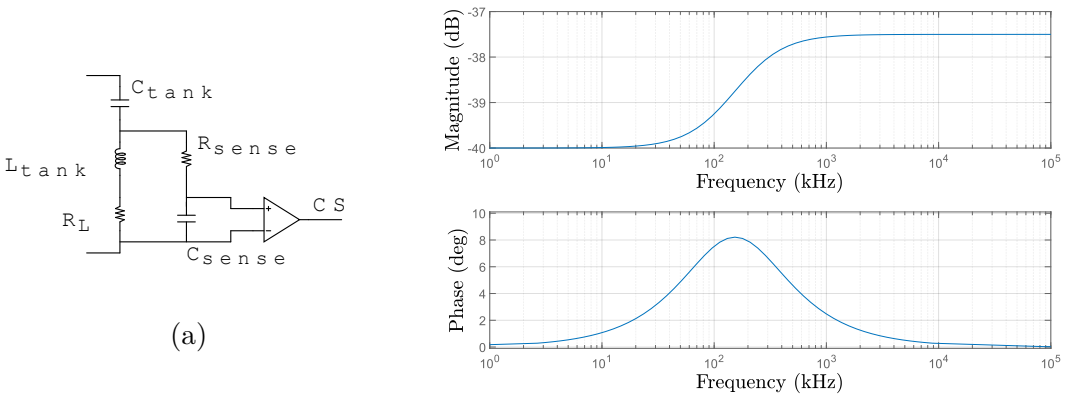


Figure 2.14: (a) Schematic of the tank current zero-crossing sensing circuit and (b) Bode diagram of the $\frac{V_{Csense}}{I_{L_{tank}}}$ transfer function.

state '0' when the tank current is negative.
The zero and the pole frequencies of the transfer function 2.8 can also be mismatched to obtain an amplification of the voltage signal $V_{C_{sense}}$, as shown in Figure 2.14b. This makes the design of the zero-crossing comparator less demanding, but it introduces a phase shift between the tank current and $V_{C_{sense}}$.

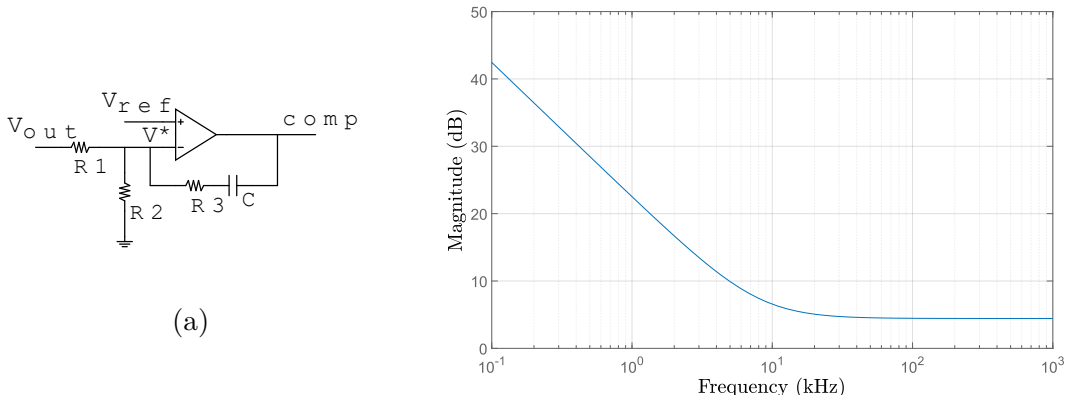
A key feature of the control circuit is the generation of the phase shift between $PWMH$ and $PWML$: the values of α and β are determined so to achieve voltage regulation. For this purpose, a Phase Locked Loop (PLL) has been designed in order to generate a ramp synchronized with every switching instant of CS (the ramp thus has double frequency compared to CS). A proportional-integral controller (PI controller), that has as inputs a scaled version of output voltage V^* and a reference voltage V_{ref}, generates an error signal called *comp*. Figure 2.15a shows the schematic of the proportional-integral controller. The reference voltage $V_{ref} = 0.3V$ is generated by an on-chip bandgap circuit. $R1 = 300k\Omega$, while the value of $R2$ depends on the desired output voltage:

$$\begin{aligned} V_{out} = 1.2V &\longrightarrow R2 = 100k\Omega \\ V_{out} = 1V &\longrightarrow R2 = 128k\Omega \end{aligned} \tag{2.9}$$

The AC behaviour of this circuit is characterized by its transfer function:

$$\frac{comp}{V_{out}} = -\frac{1 + sR3C}{sR1C} \tag{2.10}$$

The magnitude characteristic in frequency of this transfer function is reported in



(a) (b)

Figure 2.15: (a) PI controller schematic and (b) Bode plot of its transfer function.

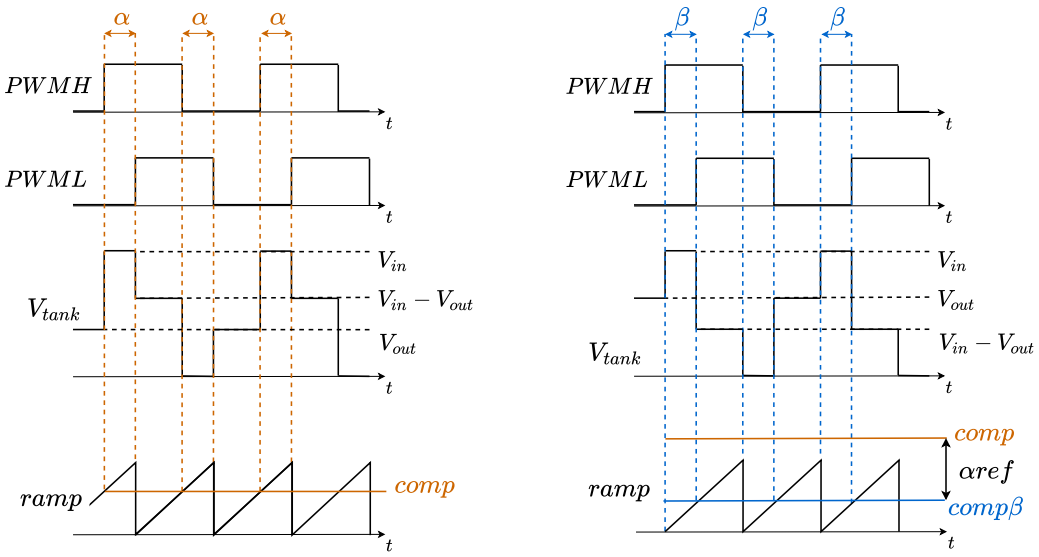
Figure 2.15b. The high DC gain of the PI controller ensures an accurate converter output voltage.

The *comp* signal is a key parameter in the closed loop operation: indeed, it is used by the angle generator block together with the ramp voltage created by the PLL in order to generate the $PWMH$ and $PWMH$ in all the operation modes. Moreover, inside the mode selection block the *comp* signal is compared to some voltage reference values, so to determine which operation mode should be adopted for the desired load current.

In normal mode, the signal *comp* is directly compared to the ramp voltage generated by the PLL, in order to determine the value of the phase lead α when $V_{out} < \frac{V_{in}}{2}$ (see Figure 2.16a). Since the phase lead α decreases at high loads as required for the proper operation of normal mode (described in 2.3.1), the value of *comp* increases at high current loads.
On the other hand, when $V_{out} > \frac{V_{in}}{2}$ the value of the *comp* signal is larger than the ramp voltage, so that $\alpha = 0$ (see Figure 2.16b). In this case, a new signal $comp\beta$ is generated, where:

$$comp\beta = comp - \alpha ref. \tag{2.11}$$

αref is a voltage signal slightly lower than the *ramp* amplitude. By comparing $comp\beta$ to the *ramp* voltage, it is possible to generate the phase lag β. In this case, the phase lag β increases at high loads, as required for the proper operation of normal mode described in 2.3.1. In other words, the voltages *comp* and $comp\beta$ increase for higher current loads.



(a) α shift generation

(b) β shift generation

Figure 2.16: Generation of (a) α and (b) β phase shifts in normal operation mode.

In medium-load mode the generation of the phase lead is identical to the one employed in α mode.
In light-load mode instead the closed loop operation changes significantly: the zero crossing detection and the PLL *ramp* voltage are not used anymore, while the signal *comp* is directly provided as an input to a Voltage Controlled Oscillator (VCO). The square wave at the output of such VCO coincides with the $PWML$ and $PWMH$ signals, whose frequency is proportional to the value of *comp*. As required by the proper operation of the light load mode described in 2.3.3, as the current load decreases also the magnitude of the *comp* signal and the switching frequency decrease.

Overall, the value of R_{tank} affects dramatically the converter efficiency and its reliability. The switches on-resistances, the interconnects (both on-chip and on the PCB), the inductor and capacitor ESR contribute to the total value of R_{tank}. While the value of the DC resistance is well known and it has been optimized at design level, R_{tank} exhibits a dependence on the frequency (e.g. due to skin effect), and for the used switching frequencies its value is significantly larger than at DC. An accurate estimation of the total R_{tank} in the developed converter could not be achieved with the available design tools. Therefore, while in the design phase the chosen values of the tank components are $L_{tank} = 12nH$ and $C_{tank} = 4.7\mu F$, the final choice of the passive discrete components that optimize the converter efficiency can be done only in the characterization phase. The results of such characterization campaign are reported in Chapter 3.

Chapter 3

Experimental analysis and efficiency optimization of a ReSC prototype

3.1 Experimental setup

The experimental characterization that is detailed in the following has been performed using a dedicated test system that is shown in Figure 3.1.
In particular, the following instruments have been used for the analysis of the converter performances:

- Keithley 2231a-30-3: a triple channel DC power supply to provide the input voltage;
- BK Precision 8502: a programmable DC electronic load to set the desired load current;
- Keithley 2000: several bench multimeters to measure the input voltage/current and the output voltage/current;
- Lecroy WaveSurfer 44Xs: an oscilloscope to visualize the most important signals of the device.

The power efficiency has been calculated as follows:

$$efficiency = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{out}}{V_{in}I_{in}} \tag{3.1}$$

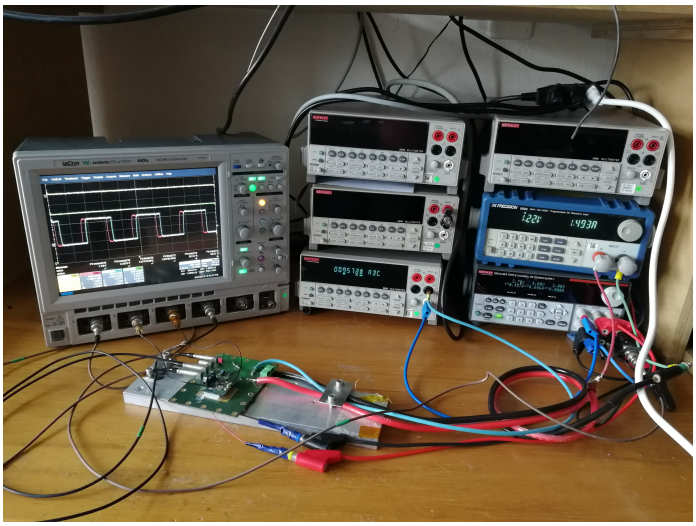


Figure 3.1: Test system used to characterize the ReSC converter.

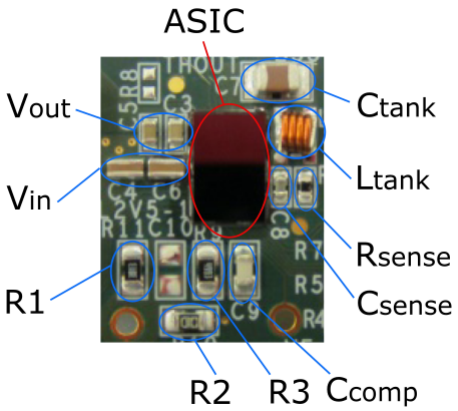


Figure 3.2: ReSC prototype.

The prototype that has been characterized is shown in Figure 3.2. The four power transistors ($HS1, LS1, HS2, LS2$), together with the control circuitry, have been integrated on chip (ASIC).
While, the tank (L_{tank}, C_{tank}), the compensation filter ($R1, R2, R3, C_{comp}$) and the sense circuits elements (R_{sense}, C_{sense}) have been installed as discrete components. So, it was possible to change these passive elements, in order to observe their impact on the converter behaviour and efficiency.

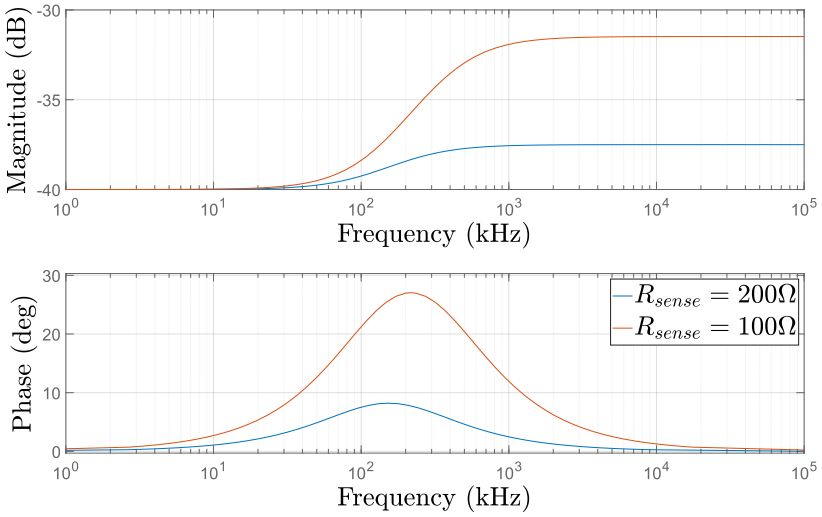


Figure 3.3: Impact of a variation in R_{sense} on the transfer function of the tank current sensing circuit, for $C_{sense} = 4.7nF$, $L_{tank} = 12nH$, $R_{L_{tank}} = 10m\Omega$.

3.2 Optimization of the tank current zero-crossing sensing circuit

The RC filter used to sense the inductor current (see Figure 2.14a) plays a fundamental role in the control circuitry of this ReSC converter, since it is responsible for the detection of the zero-crossing instants of the tank current. Depending on the value of the resistor R_{sense}, the voltage signal across the capacitor C_{sense} for the same inductor current changes its magnitude and phase (as shown in Figure 3.3). In particular, the usage of a small resistance allows to boost the amplitude of the voltage signal. At the same time, if the switching frequency is sufficiently low, the voltage signal across C_{sense} could present a phase lead compared to the tank current.
Therefore, by tuning R_{sense}, it is possible to introduce a phase lead on the switching instants of the CS signal compared to the zero-crossing instants of the inductor current. This causes a variation in the operating point of the converter (leading to a variation in its switching frequency and in its efficiency) for a given V_{in}, V_{out} and load.
The sensing resistance can be therefore adjusted to achieve an optimal efficiency, and this has been done for several load currents. The measurements have been carried out in normal mode for the high current loads, while for the low current loads medium and light load operations were used.

In Figure 3.4, the efficiencies obtained with $V_{in} = 2.5V$ and $V_{out} = 1.2V$ are shown.

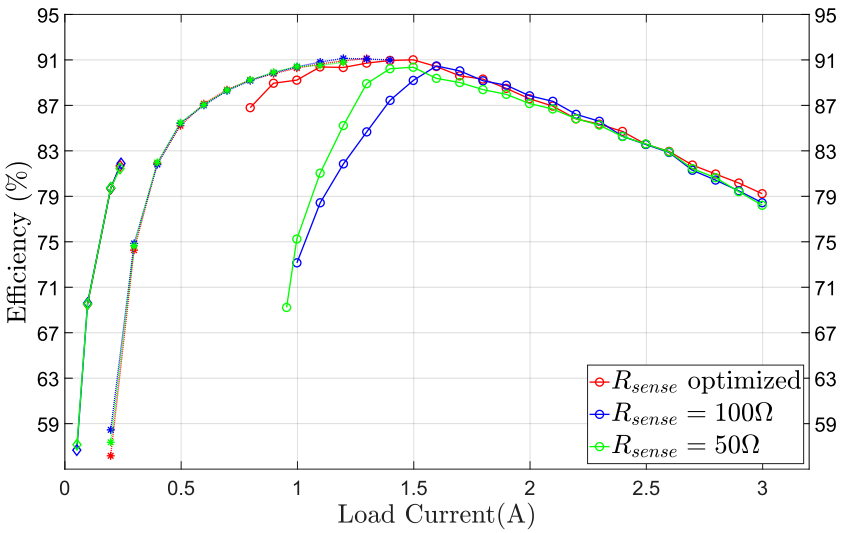


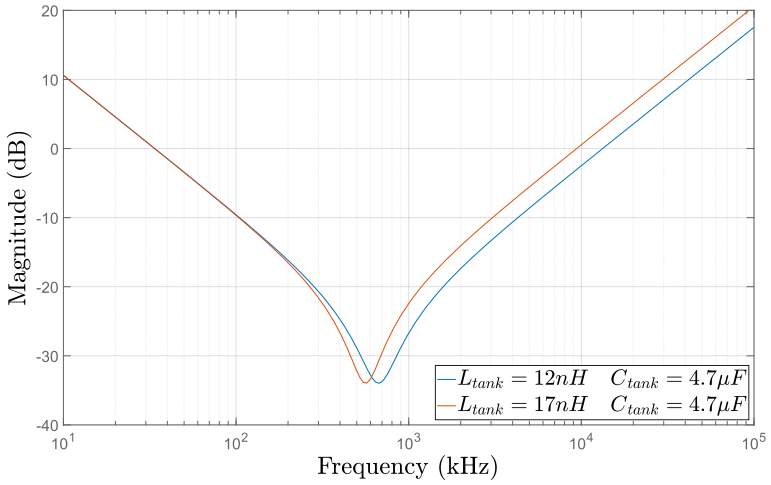
Figure 3.4: Impact of the value of the sensing resistance R_{sense} on the measured efficiency ($V_{in} = 2.5V, V_{out} = 1.2V$).

It is possible to see that the impact of the sensing resistance in normal mode can be important: a higher resistance is needed at high current loads, while a lower one provides better results at low current loads. Instead, the effect of the sensing resistance variation is negligible in medium and light load operations.

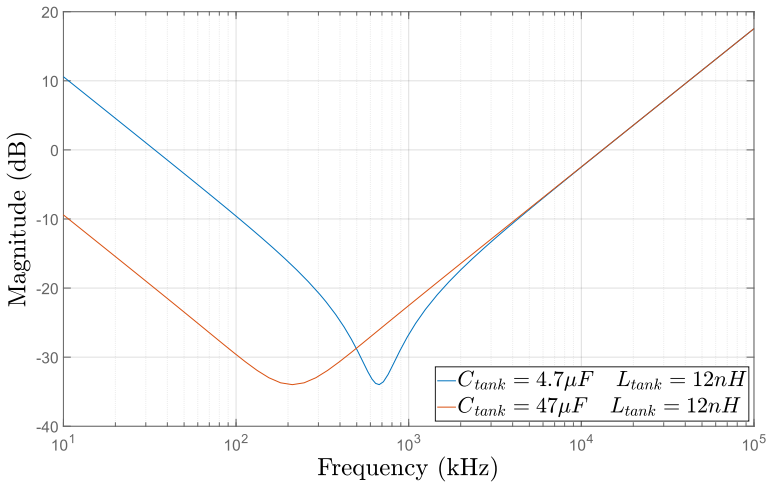
Considering that in the application in the HL-LHC experiments this converter is expected to operate with a fixed current load of $2.5A < I_{load} < 3A$, the optimization can be performed by choosing the value of R_{sense} that optimizes the efficiency in this range of current loads. This optimization allows to boost the performances of the converter without affecting its size.

3.3 Tank optimization

The core of the Resonant Switched Capacitor converter is the LC tank. By tuning the tank inductance or the tank capacitance, the resonance frequency (and consequently the switching frequency) change, affecting the efficiency of the converter. Several values for both components have been adopted in this characterization campaign, and the impact of the variation of these elements on the converter performances is detailed in the following. The technical information regarding the inductors and capacitors used are reported in Tables 3.1, 3.2; the shape and dimensions of the tank inductor are sketched in Figure 3.6.



(a) L_{tank} variation



(b) C_{tank} variation

Figure 3.5: Variation of the tank impedance magnitude when using (a) different inductors, or (b) different capacitors.

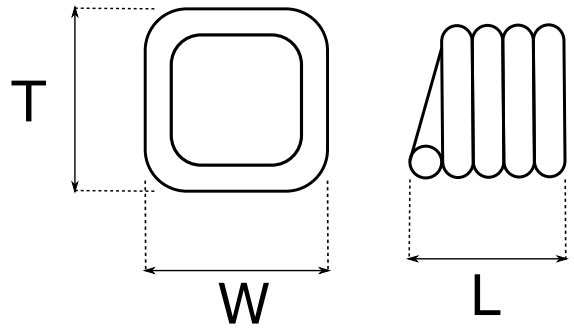


Figure 3.6: Length (L), Width (W) and Thickness (T) of the tank inductor.

3.3.1 Tank inductor optimization

Inductor by Coilcraft	Inductance (nH)	Rs (mΩ) @DC	Weight (mg)	L - W - T (mm)
0908SQ-8N1_L_	8.1	6	12.8	1.47 - 2.13 - 1.83
0908SQ-12N_L_	12.1	7	16.9	1.85 - 2.13 - 1.83
0908SQ-17N_L_	16.6	8	21.1	2.21 - 2.13 - 1.83
1508-9N0_L_	9	3.4	65	3.94 - 4.19 - 2.01
A04T_L_	12.5	3.4	65	3.94 - 4.45 - 3.15
A05T_L_	18.5	3.9	78	3.94 - 4.45 - 3.15

Table 3.1: Tank inductors technical information.

The tank inductor is the largest discrete component of the converter: a bulky air-core inductor must be used due to the high magnetic field which is present in the LHC experiments, and the minimization of its volume is crucial to avoid interference with the physics performances. Figure 3.5a highlights the variation of the tank impedance when the value of the inductor is changed.
The complete technical information regarding the tank inductors that have been used for this efficiency optimization are reported in Table 3.1. In particular, these coils belong to two different families:

- Coilcraft Air Core Inductors, 0908SQ series: such coils have a reduced volume and a larger series resistance;
- Coilcraft Mini Spring Air Core Inductors: they are characterized by a low series resistance and by a relatively large volume.

As in the previous section, the measurements have been carried out in normal, medium and light load operation modes.

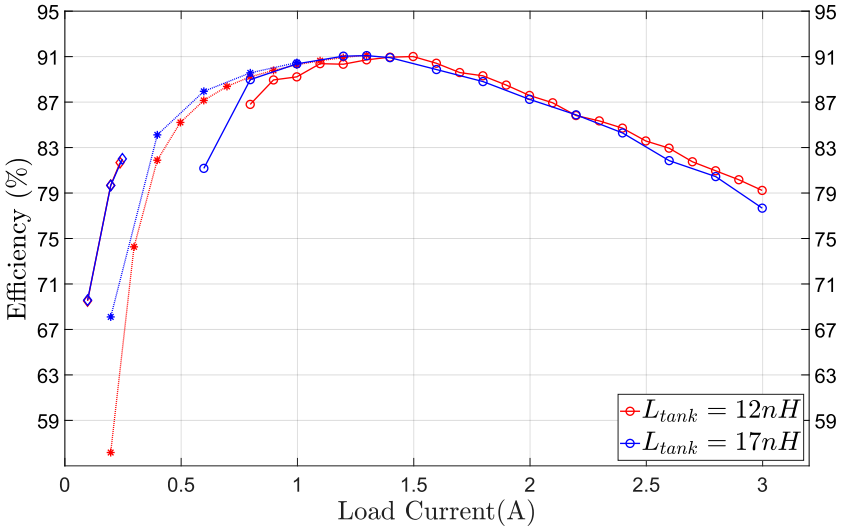


Figure 3.7: Measured impact of variations of the tank inductor (Coilcraft 0908SQ series) on the converter efficiency. An optimized R_{sense} has been used. $C_{tank} = 4.7\mu F$, $V_{in} = 2.5V, V_{out} = 1.2V$.

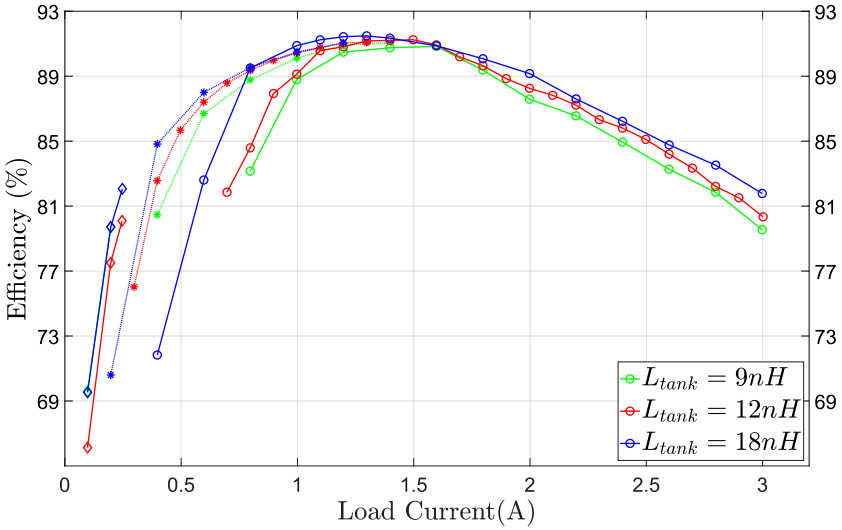


Figure 3.8: Measured impact of variations of the tank inductor (Coilcraft series having reduced series resistance) on the converter efficiency. An optimized R_{sense} has been used. $C_{tank} = 4.7\mu F$, $V_{in} = 2.5V, V_{out} = 1.2V$.

Figure 3.7 reports the results obtained for two inductors of the 0908SQ series (0908SQ-12N_L_, 0908SQ-17N_L_). The bigger inductor leads to a reduced resonant frequency, and thus to a lower switching frequency for the same V_{in}, V_{out} and load. This ensures higher efficiency in normal mode at lower current loads, when the switching frequency is higher and the frequency-dependent losses are dominant. However, the 17 nH inductor has a larger series resistance compared to the 12 nH inductor. The efficiency obtained with the larger inductor is thus lower at high current loads, where the tank current amplitude is larger and the conduction losses dominate.

Figure 3.8 shows the efficiency measured by employing the inductors of the Mini Spring Air Core Inductors series (1508-9N0_L_, A04T_L_, A05T_L_). These components exhibit a similar series resistance for all the different inductors, as reported in Table 3.1. In this case, an increase in the inductor value provides an efficiency boost in normal mode, both at low and high current loads: the conduction losses are low even at heavy loads (since the inductor series resistance is small), and the reduction in the frequency-dependent losses allowed by a larger inductor is dominant.

A trade-off between volume and efficiency emerges comparing the results obtained by the inductors 0908SQ-12N_L_ and A04T_L_ (both presenting $L = 12nH$, but different series resistances). Indeed, at $I_{load} = 3A$ the latter inductance features higher efficiency ($\sim 1\%$ higher). Therefore, the usage of an inductor that features lower series resistance improves the converter efficiency, but it affects the size of the converter.

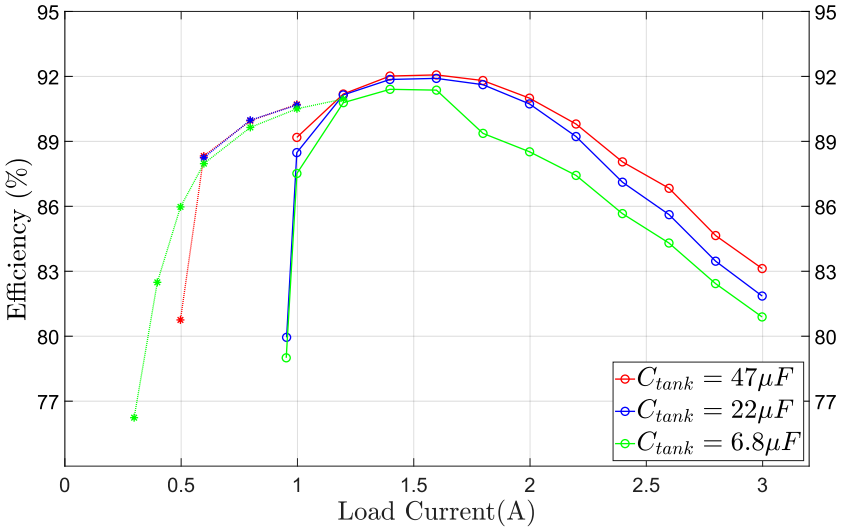


Figure 3.9: Tank capacitor variation impact with optimized R_{sense}; $L_{tank} = 12nH$ ($V_{in} = 2.5V$ $V_{out} = 1.2V$).

3.3.2 Tank capacitor optimization

Capacitor by TDK	Capacitance (μ F)	Rs (mΩ) @(100k-1M-10M)Hz	L - W - T (mm)
C2012X5R1H475K125AB	4.7	4.8 - 2.3 - 8.8	2 - 1.25 - 1.25
C2012X7R1A685K125AC	6.8	4.0 - 2.1 - 9.3	2 - 1.25 - 1.25
C2012X5R1A226K125AB	22	2.7 - 1.6 - 7.8	2 - 1.25 - 1.25
C2012X5R0J476M125AC	47	1.3 - 1.1 - 6.5	2 - 1.25 - 1.25

Table 3.2: Tank capacitors technical information.

The resonant frequency of the LC tank can be modified also by tuning the tank capacitor (see Figure 3.5b). By increasing its value, the switching frequency and consequently the frequency-dependent losses are expected to be reduced.
Figure 3.9, shows the measured efficiencies obtained with different tank capacitors. The components technical information are reported in Table 3.2, these capacitors were chosen since they feature low series resistance. As expected, the efficiency of the converter increases significantly with the tank capacitance. However, some issues appear when using $C_{tank} = 47\mu F$: the light load operation is no more working properly and the transitions between modes become unreliable.
It is important to remark that the larger efficiency allowed by an increased tank capacitance does not affect at all the dimensions of the converter, since all the capacitors use a 0805 package.

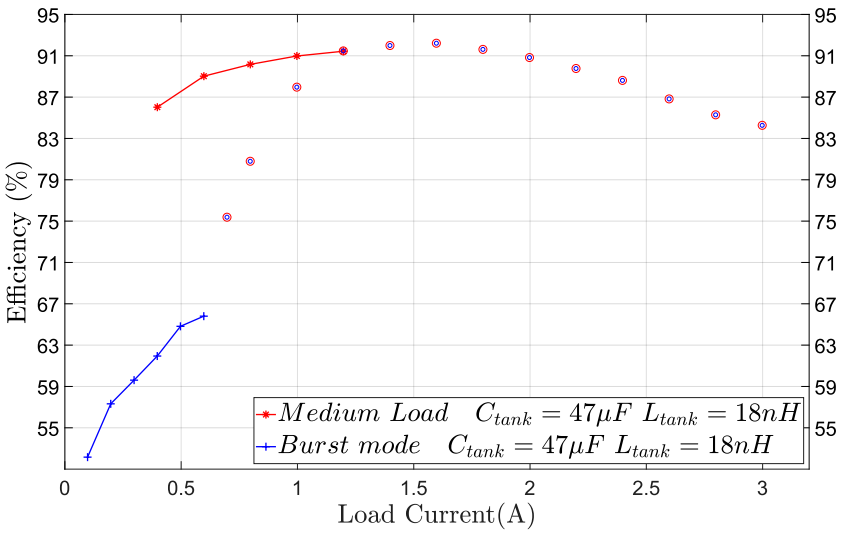


Figure 3.10: Efficiency comparison between Medium load and Burst mode, with optimized R_{sense} ($V_{in} = 2.5V$ $V_{out} = 1.2V$).

3.4 Burst mode efficiency analysis

For all the measurements reported in the previous sections, the medium and light load operations were analyzed for low load currents. As explained in section 2.3.4, an alternative solution to achieve voltage conversion at low current loads is burst mode.
The purpose of this section is to highlight the benefits and the drawbacks of this operation mode. Figure 3.10 shows a comparison between the efficiency achieved in medium and burst mode.
It is clear that, in all conditions, burst mode provides lower efficiency. Moreover, the output voltage shows a greater ripple in burst mode than in all the other operation modes.
On the other hand, burst mode guarantees an improved transition from/to normal mode compared to medium and light load mode. Furthermore, this converter is targeted to work at load current $2.5A < I_{load} < 3A$, so the optimization of the efficiency at low current loads has a lower impact compared to the optimization performed for the normal operation mode.

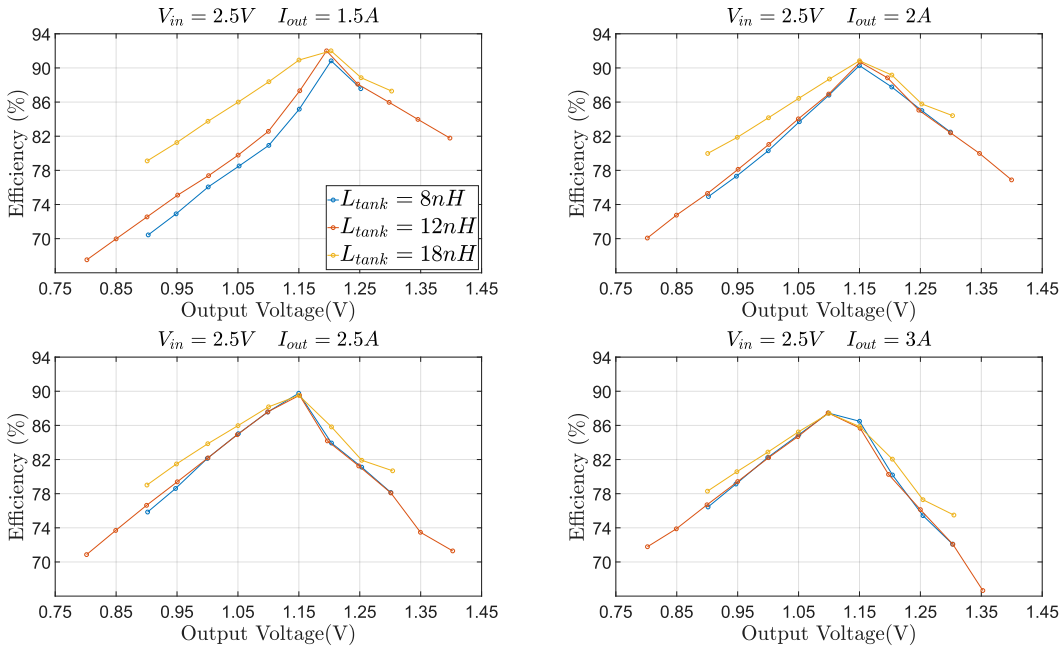


Figure 3.11: Measured efficiencies vs. output voltage at different load currents, for $V_{in} = 2.5V$.

3.5 Efficiency vs. Input/Output voltage ratio

The following experimental analysis is devoted to study the dependence of the efficiency on the conversion ratio (V_{in}/V_{out}) at different load currents. Figure 3.11 reports the measurements done with different components for the LC tank:

- $L_{tank} = 8nH$ (0908SQ-8N1_L_), $C_{tank} = 47\mu F$ (C2012X5R0J476M125AC);
- $L_{tank} = 12nH$ (0908SQ-12N_L_), $C_{tank} = 47\mu F$ (C2012X5R0J476M125AC);
- $L_{tank} = 18nH$ (A05T_L_), $C_{tank} = 47\mu F$ (C2012X5R0J476M125AC).

A bigger tank inductance generally provides higher efficiency, while it leads to a reduced dependence of the efficiency on the conversion ratio. The peak value of the efficiency is instead almost constant for the different tank inductance, and it changes with the output current. It can be shown that considering zero tank series resistance, the converter exhibits minimal switching frequency and RMS tank current for $V_{in}/V_{out} = 0.5$. This conversion ratio should thus provide the best efficiencies. As shown in Figure 3.11, the peak efficiency is nevertheless found for $V_{out} < \frac{V_{in}}{2}$. Moreover, the conversion ratio where the peak efficiency is found is larger for an increased load current.
This can be explained considering the voltage drop on the tank series resistance. It can be shown that this drop shifts the conversion ratio that guarantees the best

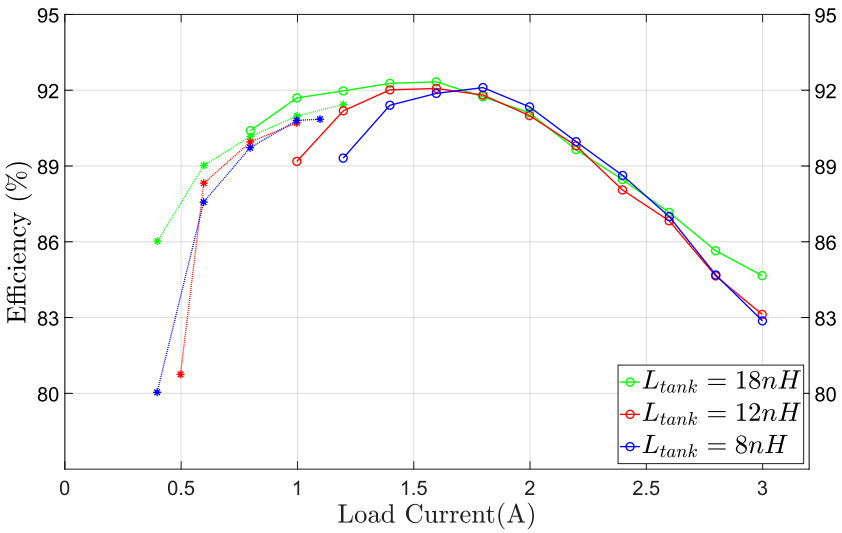


Figure 3.12: Efficiency obtained with three different inductors, using the optimal tank capacitance $C_{tank} = 47\mu F$. The $8nH$ inductor (blue line) is the optimal solution to minimize the converter size, while the best efficiencies are obtained using $L_{tank} = 18nH$ (green line). The $12nH$ inductor (red line) leads to a good compromise between the converter volume and its efficiency. R_{sense} has been tuned to obtained an optimal efficiency in each case. For these measurements, $V_{in} = 2.5V$ and $V_{out} = 1.2V$.

performances, and that the drop increases with the tank current amplitude. Since the load current is proportional to the tank current amplitude, the peak efficiency shift increases with the load.

3.6 Choice of the optimized tank circuit

As introduced in the previous sections, the volume and the efficiency of a Resonant Switched Capacitor converter are determined by the choice of the tank components. The optimized tank capacitor has been chosen to be the biggest available ($C_{tank} = 47\mu F$), since it boosts the efficiency without affecting the converter volume, as explained in the previous section.
The choice of the inductor, on the other hand, influences both the size and the efficiency of the converter. In particular, a larger inductor can be employed if very high efficiency is needed. On the other hand, reducing the converter volume by using a smaller inductor leads to an efficiency degradation. This trade-off is unavoidable and intrinsically connected to the nature of this converter. In Figure

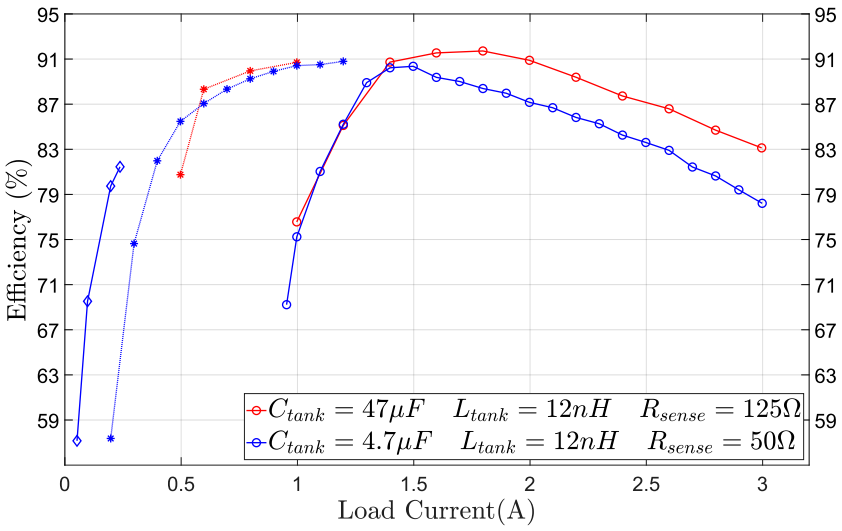
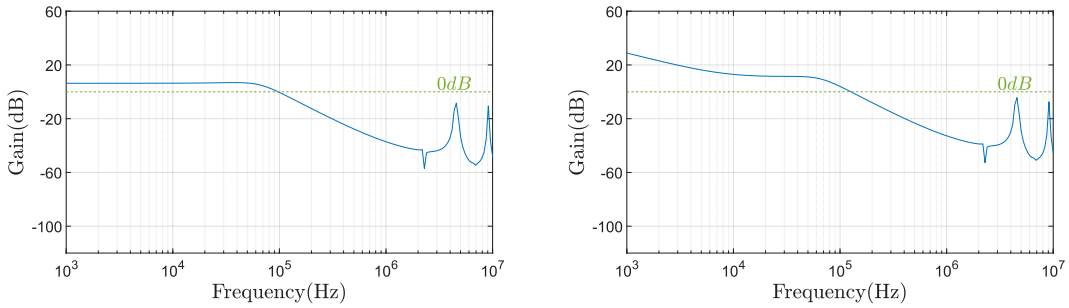


Figure 3.13: Comparison between the efficiencies obtained using the optimized tank (red line) and the one obtained with the default tank components (blue line). $V_{in} = 2.5V$ and $V_{out} = 1.2V$.

3.12, the efficiency achieved by three possible optimized tank are compared:

- $L_{tank} = 18nH$ (A05T_L_) $C_{tank} = 47\mu F$ (C2012X5R0J476M125AC); this tank provides the best efficiency but the inductor is considerably big;
- $L_{tank} = 12nH$ (0908SQ-12N_L_) $C_{tank} = 47\mu F$ (C2012X5R0J476M125AC); this tank provides average efficiency, the inductor is small;
- $L_{tank} = 8nH$ (0908SQ-8N1_L_) $C_{tank} = 47\mu F$ (C2012X5R0J476M125AC). this tank provides lower efficiency, the inductor is considerably small.

The $8nH$ inductor is the optimal solution to minimize the converter size, while the best efficiencies are obtained using $L_{tank} = 18nH$. The $12nH$ inductor leads to a good compromise between volume and efficiency, and it has therefore been chosen for this application. Using the selected tank, the efficiency is comparable to the one obtained from a buck converter designed for the same application, while the converter volume is significantly reduced.
Figure 3.13 shows the comparison between the efficiency obtained using the original tank ($L_{tank} = 12nH$, $C_{tank} = 4.7\mu F$) and the chosen optimized tank solution. This experimental optimization has been crucial, since it allowed to boost the converter efficiency, without affecting the converter volume.



(a) (b)

Figure 3.14: Open-loop transfer function of the converter either not considering (a) or taking into account (b) the contribution of the compensation network.

3.7 Issues to be addressed

The experimental analysis of the ReSC converter allowed to better understand its properties and limitations. The optimization allowed to boost the efficiency of the converter (of about 4% at $I_{load} = 3A$) without increasing its volume. However, the large increase in the value of the tank capacitor compared to the one for which the converter had been designed ($47\mu F$ vs. $4.7\mu F$) generates several issues in the converter operation. Indeed, this modification has a major impact on:

- the resonant frequency of the tank:
  $f_{resonance} = 670kHz \longrightarrow f_{resonance} = 212kHz$;
- the damping factor of the tank (supposing $R_{series} = 50m\Omega$):
  $\zeta = 0.49 \longrightarrow \zeta = 1.56$

The control circuitry had not been designed to deal with these values of resonant frequency and attenuation factor, and this leads to the malfunctioning of some parts of the control circuitry. In order to guarantee the proper operation, these problems must be investigated and solved at design level.

3.7.1 Frequency related issues

The open-loop transfer function of the converter allows to evaluate the DC accuracy of the output voltage, the loop stability and its dynamic performances. In order to achieve an accurate value for the output voltage, the DC gain of the open-loop transfer function must be large. At the same time, the unity gain frequency of the loop must be significantly lower than the switching frequency, in order to achieve a stable operation of the control circuitry.
The gain of the open-loop transfer function without considering the contribution of the PI-controller has been simulated and is reported in Figure 3.14a. The dominant

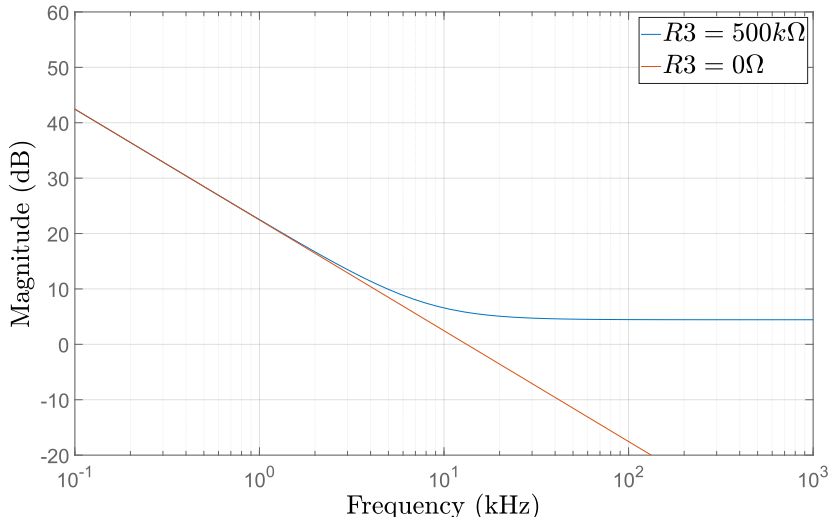


Figure 3.15: Variation of the compensation filter transfer function.

pole induces a unity gain frequency around $f = 100kHz$.
The gain of the complete open-loop transfer function has been simulated considering also the compensation network contribution, and the result is shown in Figure 3.14b. The unity gain frequency of the complete open loop transfer function is around $f = 125kHz$, the attenuation at $f = 200kHz$ is equal to $gain = -8dB$.
The PI-controller provides the necessary high DC gain, while it ensures that the unity-gain frequency is significantly lower than the switching frequency.

However, the lowering of the resonance frequency due to the efficiency optimization represents an issue for the stable operation of the converter. Indeed, the optimized resonance frequency and the unity gain frequency of the open-loop transfer function are close, and this could induce some instabilities.
For this reason, a re-tuning of the compensation filter is necessary. The unity gain frequency can be lowered by replacing the resistance $R3$ of the proportional-integral controller with a short circuit (see Figure 2.15a).
The transfer function of the modified compensation filter is:

$$\frac{comp}{V_{out}} = -\frac{1}{sR1C} \tag{3.2}$$

The comparison between the transfer functions of the original and the modified compensation network is showed in Figure 3.15. This adjustment, however, causes a reduction of the circuit bandwidth, inducing a slower response to transient variations of V_{out}. The modification of the compensation filter affects the complete open-loop transfer function: the gain that is achieved thanks to the removal of $R3$ is shown in Figure 3.16.

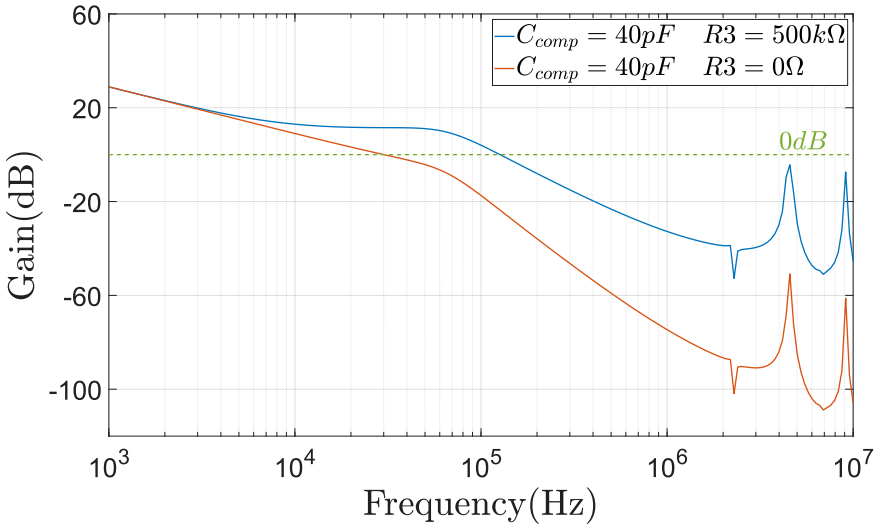


Figure 3.16: Effect of the compensation filter variation on the magnitude of the complete open-loop transfer function of the converter.

This improved transfer function exhibits a unity gain frequency around $f = 30kHz$, well below the resonant frequency of the optimized tank.

Another element of the control circuitry that should be adapted to the optimized resonance frequency is the PLL that generates the ramp signal synchronized with the switching instants of CS. In the original implementation, the frequency of CS was in the range $1MHz < f_{CS} < 10MHz$. The optimized tank extends this frequency range to $200kHz < f_{CS} < 10MHz$, and a proper ramp signal cannot be generated by the existing PLL for low values of f_{CS}.

Moreover, the Voltage Controlled Oscillator (VCO) that provides the $PWMH$ and $PWML$ waveforms in light load mode showed various issues during the measurements, both with the original and the optimized tank:

- converter equipped with the original tank:
  the light-load mode works properly, but as the load decreases (and so the switching frequency), the duty cycle of its output voltage waveform drifts significantly from its ideal value of 0.5;

- converter equipped with the optimized tank:
  the light-load mode does not work properly at low current loads ($I_{load} < 1A$).

3.7.2 Attenuation related issues

The optimization of the tank components induces also a variation in the damping factor from $\zeta = 0.49$ to $\zeta = 1.56$. As detailed in section 2.2.1, this means that the optimized tank shows an over-damped current response to a voltage excitation, while the response of the original tank was under-damped. This variation of the current response can be a critical problem when the zero crossing detection is supposed to be found while the tank current, in absolute value, is decaying (during Phase 2 and Phase 4). Indeed, this issue emerges for the over-damped tank, since its decaying current presents an exponential shape that never crosses the zero value. This occurs in β mode: the over-damped tank current does not cross the zero value anymore, so the signal CS stops its switching operation and the output voltage drops to zero.
The over-damped response of the tank is not an issue in α mode, since the zero crossing of the tank current is detected during Phase 1 or Phase 3.

Chapter 4

Design level optimization

4.1 Design software and constraints

The design software used for this project are:

- SIMetrix by SIMPLIS for the quick simulation of a simplified model of the converter;
- Virtuoso Schematic Editor and Analog Design Environment by Cadence for the design and simulations of the converter at transistor level.

Different simulations have been performed using the two software, exploiting the fast overview on the converter behavior provided by SIMPLIS and the possibility to accurately simulate the designed circuits in Cadence Virtuoso.
The analog blocks designed in this work are not powered directly by the input voltage of the converter, but by a $1.2V$ rail created by internal linear regulators. The circuits have to be functional even in the following corner cases:

- temperature: $-30°C < T < 100°C$
- power supply: $1.08V < V_{dd} < 1.32V$
- process corners for active and passive components
- radiation corners that take into account the radiation-induced degradation of the used devices

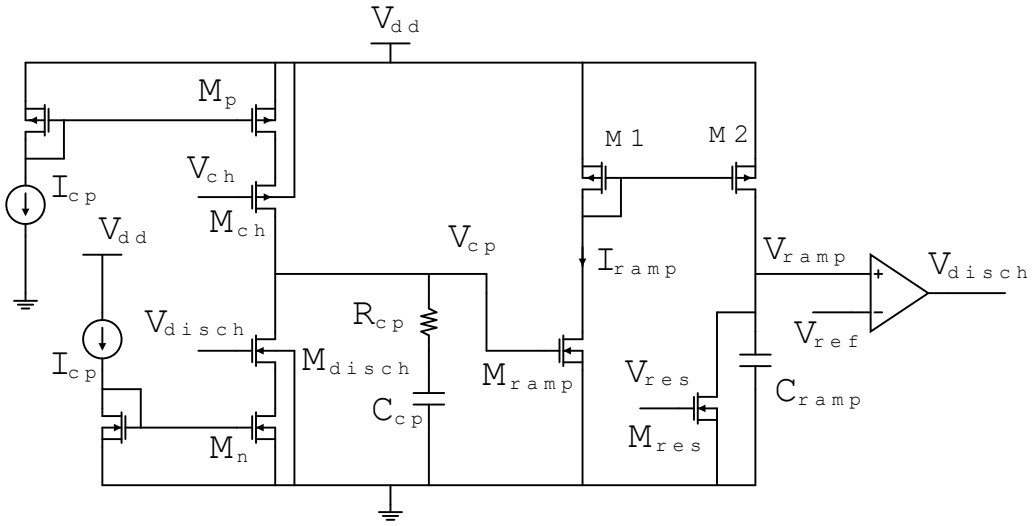


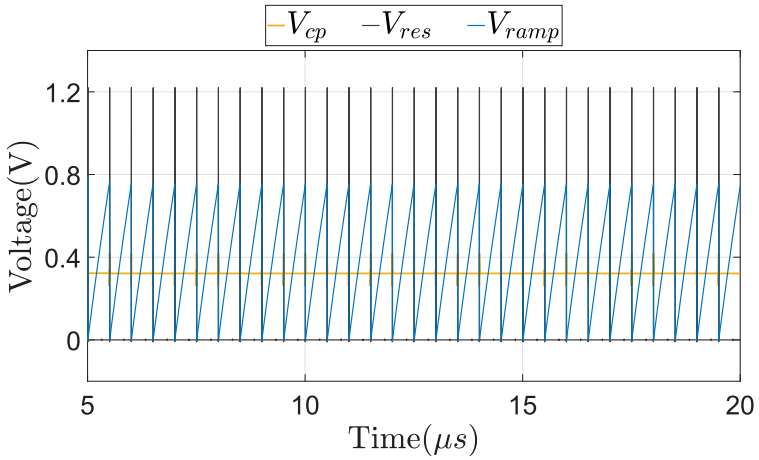
Figure 4.1: Schematic of the original PLL.

4.2 PLL

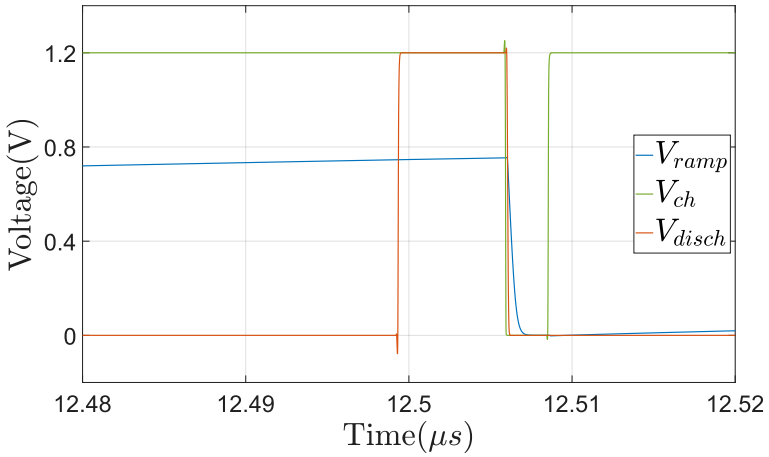
The Phase Locked Loop is a core element of the control circuitry. As explained in section 2.4, it provides the voltage ramp waveform that is used together with the *comp* signal in order to determine the phase shifts α and β between $PWMH$ and $PWML$. Therefore, it is vital that this element works properly, providing a stable ramp waveform for all the possible switching frequencies. The original schematic of the used PLL is shown in Figure 4.1. The circuit is characterized by a closed loop operation and it is constituted of:

- a charge pump formed by two bias transistors (M_n , M_p) that drive the current I_{cp} and by two switches (M_{disch} , M_{ch}) that periodically connect either M_n or M_p to the capacitor C_{cp};
- a voltage-controlled ramp generator: a capacitor C_{ramp} is charged by the current I_{ramp} to create the ramp signal V_{ramp}. I_{ramp} is generated by the transistor M_{ramp} and it is proportional to the voltage V_{cp}.

At each falling or rising edge of the tank current zero-crossing signal CS, the ramp capacitor C_{ramp} is discharged to ground (by a pulse on V_{res} that switches on transistor M_{res}). At the same time, a pulse of V_{ch} with fixed time length t_{ch} charges C_{cp}. The discharge of C_{cp} is driven by the signal V_{disch}, that takes the logic value '1' only when the ramp voltage V_{ramp} overcomes the reference voltage V_{ref}.
As the equilibrium is reached for a certain switching frequency, the net quantity of



(a) Ramp generation.



(b) Charge pump mechanism.

Figure 4.2: Simulated proper operation of the PLL: (a) overall operation, and (b) detail of the charge pump mechanism.

charges injected on C_{cp} should be zero for each cycle of the loop. Therefore, the voltage V_{cp} is constant, providing a ramp waveform V_{ramp} of stable frequency. It can be shown that the ramp amplitude V_{ramp} at equilibrium is:

$$V_{ramp} = V_{ref} \frac{1}{1 - 2 f_{switching} t_c} \tag{4.1}$$

This shows that the ramp amplitude is approximately V_{ref}, and it exhibits a weak dependence on the switching frequency (increasing for higher $f_{switching}$).

Figure 4.2 shows the simulation results of the PLL during its proper operation. The original circuit was designed and sized to work in the frequency range

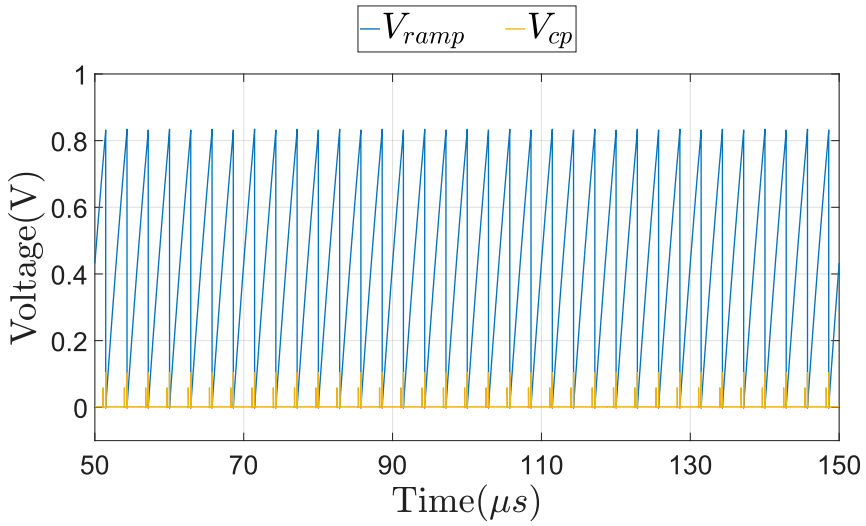


Figure 4.3: Simulated waveforms of the PLL when the leakage current of $M2$ becomes dominant (issue detected at $T = 27°C, f = 175kHz$.

$1MHz < f_{switching} < 10MHz$. As the switching frequency becomes lower than $1MHz$, the following problems are found:

- the source-to-drain leakage current of transistor $M2$ becomes larger than the current needed to obtained the desired ramp amplitude. This issue is enhanced at low frequency, where the current I_{ramp} needed is lower;
- the closed loop operation becomes unstable.

An example of the first issue is shown in Figure 4.3: the ramp voltage is generated even though the voltage V_{cp} is zero (and consequently I_{ramp} should be zero). In this situation, the amplitude of the ramp is not controllable anymore, and it is determined only by the leakage current of $M2$.

The second issue is related to the stability of the loop, and causes the ramp amplitude to be unstable and oscillating around the desired value. If the amplitude of the ramp voltage does not reach the reference voltage value, then, the comparator that determines V_{disch} does not switch and the discharge of V_{cp} does not take place. An example of the resulting discharge pulses in an unstable operation is shown in Figure 4.4.
The plot shown in Figure 4.5 reports the time instants at which a pulse of V_{disch} takes place, as a function of the total number of pulses. In case the PLL works properly, with a stable closed loop operation, the pulses are expected to exhibit the same period as the CS signal, and the plot would show a straight line. In the case of an unstable operation, some pulses would be missed, so the time of simulation

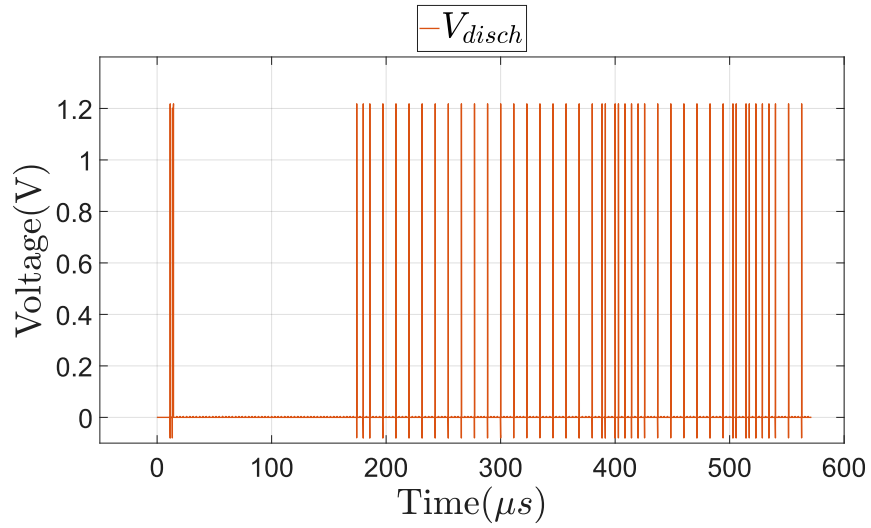


Figure 4.4: Simulated instability of the discharge process at $T = 27°C, f = 175kHz$.

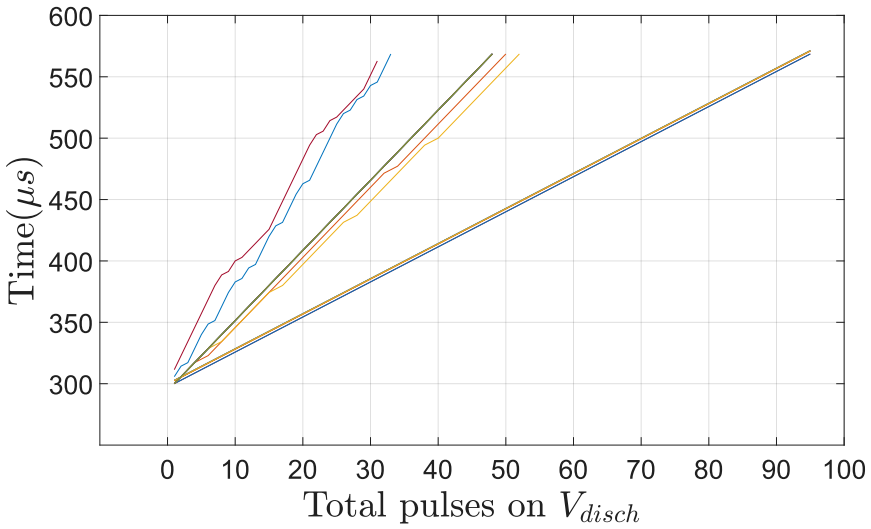


Figure 4.5: Original PLL stability issue at $T = 27°C, f = 175kHz$.

would increase while the counter does not: the resulting plot would show a broken line characterized by a steeper slope.

Figure 4.5 shows the data regarding a simulation of the PLL considering all the process corners. It is clear that the closed loop operation of the original PLL is unstable in some corner cases.

These problems have been addressed at the schematic level by implementing the

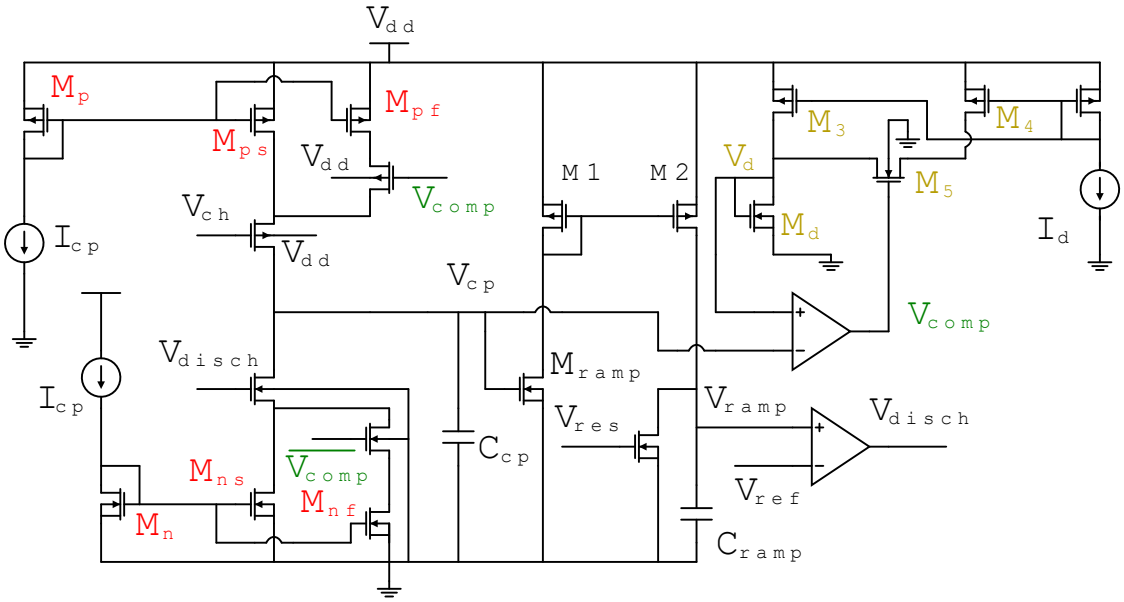


Figure 4.6: Improved schematic of the PLL.

following solutions:

- Different PMOS transistors with an increased threshold voltage have been used for M1 and M2, in order to suppress the leakage current;
- a new charge pump whose speed is adjusted according to the switching frequency has been designed, in order to improve the stability of the closed loop operation.

The improved schematic of the PLL is shown in Figure 4.6.
The charge pump should be made slower for lower switching frequencies to guarantee the stable operation of the PLL. Nevertheless, it is desirable to keep the original speed of the charge pump for higher switching frequencies, in order to ensure a fast dynamic response. The dual-speed charge pump designed in this work automatically becomes slower when the switching frequency is below approximately $1MHz$, while it keeps the original speed at higher frequencies. This has been done by reducing the current that charges and discharges C_{cp} at low frequencies. Another solution to slow down the operation of the charge pump would be increasing the size of C_{cp}, leading to an increased area consumption.
As shown in Figure 4.6, the dual-speed charge pump system is slightly more complex compared to the original one. A scaled copies of the current I_{cp} is created by means of transistors M_n, M_{ns}, M_{nf} for the discharge, and by means of M_p, M_{ps}, M_{pf}

for the charge side. Naming respectively $\left(\frac{W}{L}\right)_{M_n}$ and $\left(\frac{W}{L}\right)_{M_p}$ the $\frac{W}{L}$ ratios of M_n and M_p, the transistors have been sized as follows:

$$\begin{aligned} \left(\frac{W}{L}\right)_{M_{ns}} &= \frac{1}{5}\left(\frac{W}{L}\right)_{M_n} & \left(\frac{W}{L}\right)_{M_{nf}} &= \frac{4}{5}\left(\frac{W}{L}\right)_{M_n} \\ \left(\frac{W}{L}\right)_{M_{ps}} &= \frac{1}{5}\left(\frac{W}{L}\right)_{M_p} & \left(\frac{W}{L}\right)_{M_{pf}} &= \frac{4}{5}\left(\frac{W}{L}\right)_{M_p} \end{aligned} \tag{4.2}$$

So, the currents driven by the different transistors are:

$$\begin{aligned} I_{M_{ns}} &= \frac{1}{5}I_{cp} & I_{M_{nf}} &= \frac{4}{5}I_{cp} \\ I_{M_{ps}} &= \frac{1}{5}I_{cp} & I_{M_{pf}} &= \frac{4}{5}I_{cp} \end{aligned} \tag{4.3}$$

When $V_{comp} = 0V$, both the bias current branches are active. Then, the current that performs the charge and discharge operation is: $I_{fast} = I_{cp}$, and the PLL operation is equal to the original one. In this way, if $V_{comp} = 0V$ the PLL operation in the frequency range $1MHz < f_{switching} < 10MHz$ is not affected by the schematic modifications.
On the other hand, when $V_{comp} = V_{dd}$ transistors M_{nf}, M_{pf} cannot drive any current, and the charge and discharge process is performed by a small current: $I_{slow} = \frac{1}{5}I_{cp}$. V_{comp} is the output of a comparator that compares the node V_{cp} to a voltage reference V_d. Being V_{cp} proportional to the switching frequency, it is possible to tune the value of the reference voltage V_d to adjust the value of the switching frequency for which the transition between slow and fast operation occurs.
Still, the value of V_{cp} does not depend only on the switching frequency; indeed the current driven by M_{ramp} in saturation is:

$$I_{ramp} = \mu C_{ox}\frac{1}{2}\left(\frac{W}{L}\right)_{M_{ramp}}(V_{cp} - V_{th})^2 \tag{4.4}$$

Considering a fixed frequency (consequently a certain current I_{ramp} is needed in order to charge the ramp capacitor in the fixed period), a temperature variation would affect the mobility μ and the threshold voltage V_{th}, while process variations can change the values of C_{ox} and V_{th}. In this case, the voltage V_{cp} is the only free parameter that can vary in order to compensate the temperature- and process-induced variations so to provide the needed current I_{ramp}. Therefore, the voltage V_{cp} depends on the switching frequency and on the temperature of operation, while it is also affected by process variations. The current I_{ramp} can be expressed also as:

$$V_{ramp} = \frac{I_{ramp}}{C_{ramp}2f_{switching}} \rightarrow I_{ramp} = 2C_{ramp}V_{ramp}f_{switching} \tag{4.5}$$

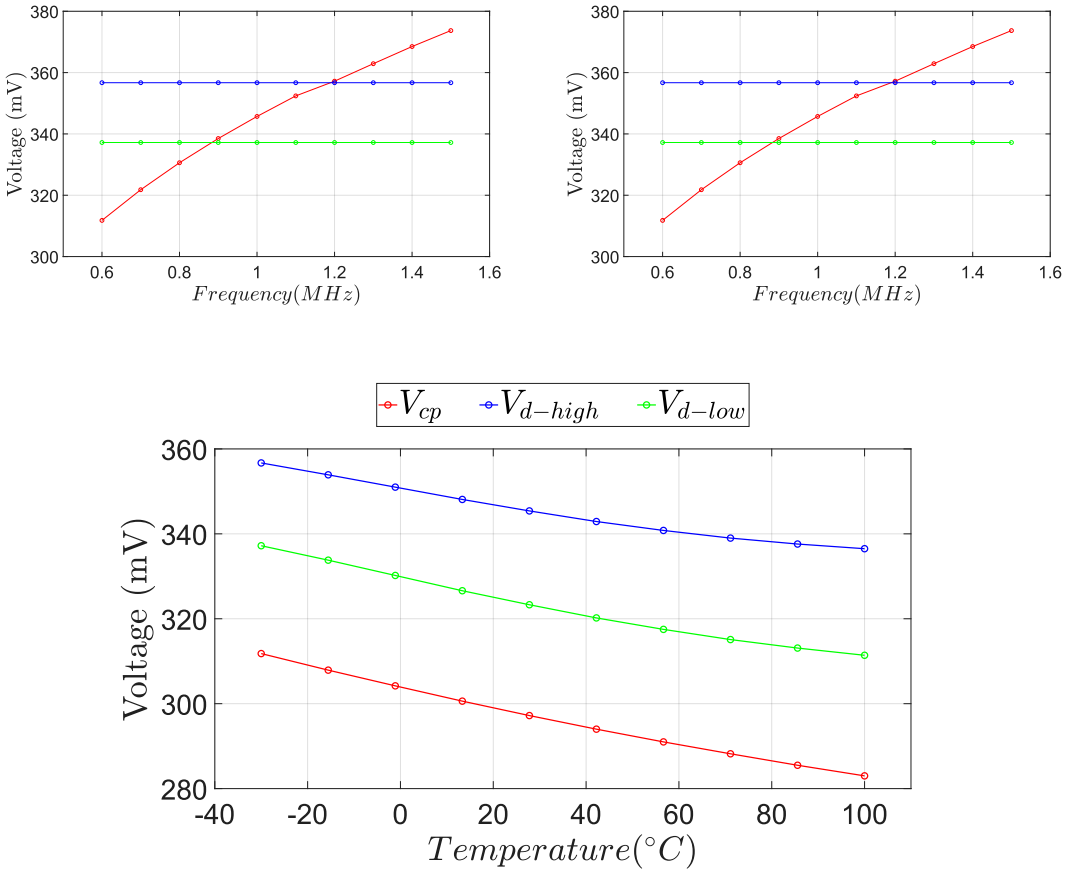


Figure 4.7: Simulated charge pump output voltage V_{cp} and threshold V_d (a) vs. frequency at $T = -30°C$, (b) vs. frequency at $T = 100°C$ and (c) vs. temperature, for $f_{sw} = 1MHz$. Thanks to the used design strategies, the frequency at which the charge pump changes speed is independent on the temperature.

Considering equations 4.4, 4.5, the voltage V_{cp} is:

$$\mu C_{ox}\frac{1}{2}\left(\frac{W}{L}\right)_{M_{ramp}}(V_{cp}-V_{th})^2 = 2C_{ramp}V_{ramp}f_{switching}$$
$$V_{cp}(f_{switching},T) = V_{th}+\sqrt{\frac{4C_{ramp}V_{ramp}f_{switching}}{\mu C_{ox}\left(\frac{W}{L}\right)_{M_{ramp}}}} \tag{4.6}$$

However, the frequency threshold for which the developed dual-speed charge pump changes its speed should be independent of temperature and process. Therefore, the reference voltage V_d should move with temperature and process variations as V_{cp} does.
This result is achieved by creating V_d using the V_{gs} of the diode connected transistor M_d, whose bias current I_d is a temperature- and process-independent current reference.
The reference voltage V_d can be found by inverting the equation of I_d:

$$I_d = \mu C_{ox}\frac{1}{2}\left(\frac{W}{L}\right)_{M_d}(V_d-V_{th})^2$$
$$V_d = \sqrt{\frac{2I_d}{\mu C_{ox}\left(\frac{W}{L}\right)_{M_d}}}+V_{th} \tag{4.7}$$

The comparator that determines V_{comp} and consequently the speed of the charge pump switches when:

$$V_{cp} = V_d \tag{4.8}$$

Therefore, considering equations 4.1, 4.6, 4.7 the instant at which the comparator switches is:

$$V_{th}+\sqrt{\frac{4C_{ramp}V_{ramp}f_{switching}}{\mu C_{ox}\left(\frac{W}{L}\right)_{M_{ramp}}}} = \sqrt{\frac{2I_d}{\mu C_{ox}\left(\frac{W}{L}\right)_{M_d}}}+V_{th}$$
$$f_{threshold} = \frac{I_d\left(\frac{W}{L}\right)_{ramp}}{2\left(C_{ramp}\left(\frac{W}{L}\right)_d V_{ref}+tcI_d\left(\frac{W}{L}\right)_{ramp}\right)} \tag{4.9}$$

This result shows that the charge pump speed selection depends only on the switching frequency.
An hysteresis has been introduced for the V_d-to-V_{cp} comparison to avoid rapid oscillations of the charge pump between fast and slow mode. This has been done by applying an additional scaled version of the I_d current (driven by transistor M_4) on the diode connected transistor, when the slow speed mode for the charge pump

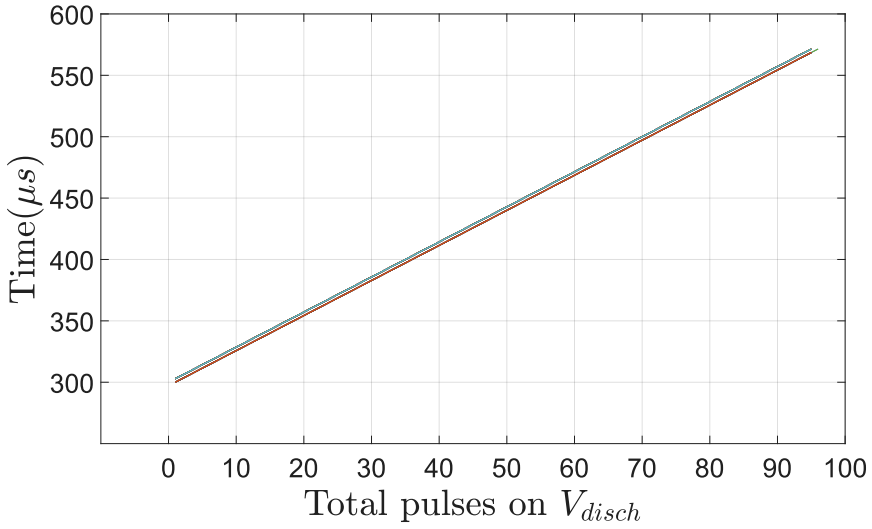


Figure 4.8: New PLL schematic behaviour at $f = 175kHz$.

is activated.

The simulation results reported in Figure 4.7 prove that the voltages V_d and V_{cp} move similarly with temperature and process, and that only the switching frequency determines the value of V_{cp} at which the comparator switches.
The proper operation of the new PLL has been simulated for all the corners detailed in section 4.1. In order to prove that its closed loop operation is stable at low frequencies, the same kind of plot reported in Figure 4.5 for the original schematic has been reproduced for the new one in Figure 4.8. The results shows a smooth operation of the newly designed PLL.

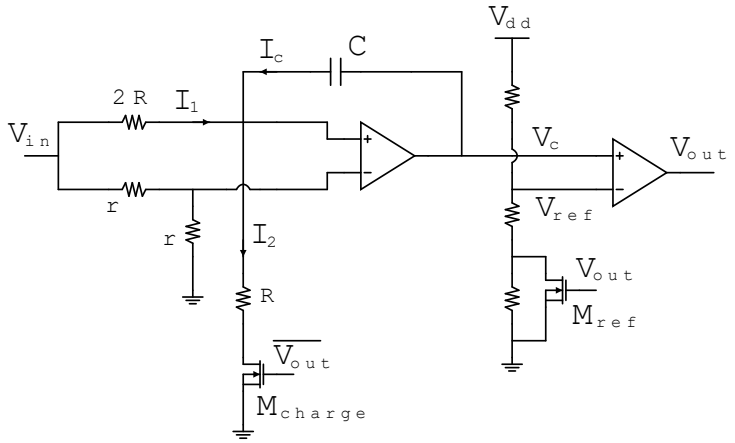


Figure 4.9: VCO original schematic.

4.3 VCO

The Voltage Controlled Oscillator (VCO) is the element that provides the $PWMH$ and $PWML$ waveforms in light-load operation mode. In this particular case, the closed loop characteristics of the converter change drastically compared to the normal operation mode. The zero current detection system and the PLL together with the α and β generation are disabled: the control circuit only relies on the VCO for driving the tank excitation. In particular, the VCO determines the frequency of the PWM signals according to the value of the control signal *comp*.
The schematic of the original VCO is shown in Figure 4.9: it is composed by the series of an integrator and of a comparator. The input voltage V_{in}, being applied to the resistance $2R$, generates a reference current I_1:

$$I_1 = \frac{\frac{V_{in}}{2}}{2R} \tag{4.10}$$

If the output voltage V_{out} is a logic '0', the transistor M_{charge} results to be on, and the currents I_2 and I_c assume the following values:

$$\begin{aligned} I_2 &= \frac{\frac{V_{in}}{2}}{R} \\ I_c^{charge} &= \frac{\frac{V_{in}}{2}}{2R} \end{aligned} \tag{4.11}$$

Being I_c positive, the integrator capacitor C is charged, and it generates an increasing voltage ramp on the V_c node. This voltage is compared to a reference voltage V_{ref} by the comparator.

The voltage appearing on V_{ref} is generated by a voltage divider applied directly to the power supply, and it may assume two different values depending on the output voltage V_{out}. Indeed, when V_{out} is low it assumes the higher value V_{ref}^{high} (since M_{ref} is off). On the other hand, when V_{out} is high M_{ref} is turned on and it determines the lower value of the reference voltage, V_{ref}^{low}.
Supposing that initially $V_c = V_{ref}^{low}$, the charge current increases V_c until:

$$I_c^{charge} t_{charge} = C\Delta V = C\left(V_{ref}^{high} - V_{ref}^{low}\right) \tag{4.12}$$

Once the ramp voltage V_c reaches V_{ref}^{high}, the comparator output voltage switches to $V_{out} = V_{dd}$. This event drives M_{ref} to lower the value of V_{ref}, at the same time M_{charge} is turned off and the currents I_2 and I_c assume the following values:

$$\begin{aligned} I_2 &= 0 \\ I_c^{discharge} &= \frac{\frac{-V_{in}}{2}}{2R} \end{aligned} \tag{4.13}$$

Being I_c negative, the integrator capacitor is discharged and it generates a decreasing voltage ramp on V_c, that is compared to V_{ref}^{low}. The integrator capacitor is discharged until:

$$I_c^{discharge} t_{discharge} = C\Delta V = C\left(V_{ref}^{low} - V_{ref}^{high}\right) \tag{4.14}$$

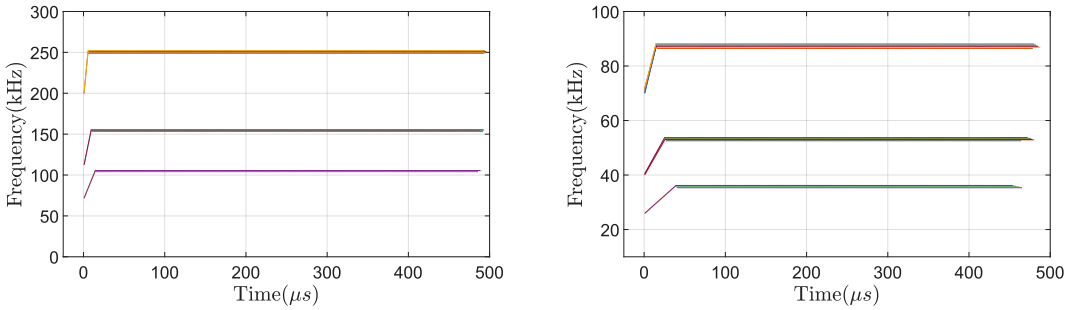
Once the comparator switches again the cycle restarts. By substituting equations 4.11, 4.13 in 4.12, 4.14 the charge and discharge times result to be symmetrical:

$$\begin{aligned} \frac{\frac{V_{in}}{2}}{2R} t_{charge} &= C\left(V_{ref}^{high} - V_{ref}^{low}\right) \rightarrow t_{charge} = \frac{C\left(V_{ref}^{high} - V_{ref}^{low}\right) 4R}{V_{in}} \\ \frac{\frac{-V_{in}}{2}}{2R} t_{discharge} &= C\left(V_{ref}^{low} - V_{ref}^{high}\right) \rightarrow t_{discharge} = \frac{C\left(V_{ref}^{high} - V_{ref}^{low}\right) 4R}{V_{in}} \end{aligned}$$

Therefore, the output voltage that results from this operation is a 50% duty cycle square wave, that can be used to drive the tank excitation. The frequency of the output voltage is directly proportional to the input voltage value:

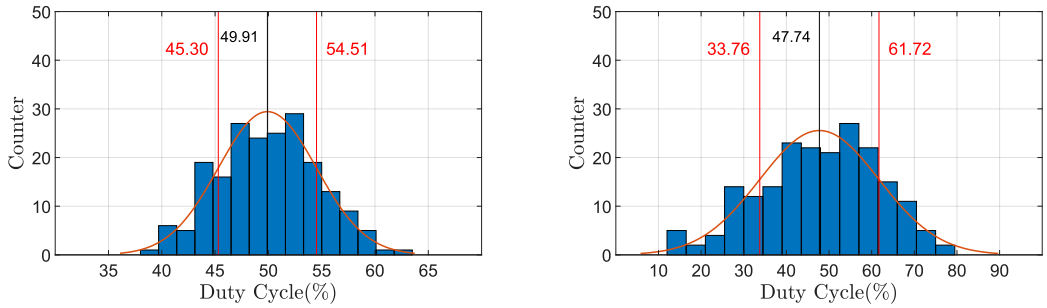
$$f_{V_{out}} = \frac{1}{(t_{charge} + t_{discharge})} = \frac{V_{in}}{8RC\left(V_{ref}^{high} - V_{ref}^{low}\right)} \tag{4.15}$$

This circuit presents however several issues. The first problem to be addressed is related to resistors variations induced by technological process corners: for the technology used the resistances vary up to ±40 % from their nominal value. These variations of R and $2R$ induce different charge and discharge currents that lead the VCO to produce a significantly different output frequency from lot to lot, for



(a) $V_{in} = 150mV$ (b) $V_{in} = 50mV$

Figure 4.10: Frequency variation due to passive corners with high (a) and low (b) input voltage.



(a) $V_{in} = 150mV$ (b) $V_{in} = 50mV$

Figure 4.11: Output voltage duty cycle degradation with high (a) and low (b) input voltage.

the same input voltage. This variability of the output voltage frequency caused by process corners both on active and passive devices has been widely simulated, and Figure 4.10 reports the simulation results.

Another issue is that most measured prototypes of the ReSC converter include a VCO that exhibits a duty cycle that increasingly differs from 50 % as the input voltage decreases. This problem can be analyzed by considering an offset voltage appearing at the operational amplifier inputs. This offset is generated in case of mismatch between the transistor pairs that belong to the integrator. Considering this offset, I_2, I_1 and I_c during charging time (M_{charge} on) are:

$$I_2 = \frac{\frac{V_{in}}{2} + V_{offset}}{R}$$

$$I_1 = \frac{V_{in} - (\frac{V_{in}}{2} + V_{offset})}{2R} = \frac{\frac{V_{in}}{2} - V_{offset}}{2R}$$

$$I_c^{charge} = \frac{\frac{V_{in}}{2} + V_{offset}}{R} - \frac{\frac{V_{in}}{2} - V_{offset}}{2R} = \frac{\frac{V_{in}}{2} + 3V_{offset}}{2R} \tag{4.16}$$

While during the discharging period (M_{charge} off) the currents assume the following values:

$$I_2 = 0$$
$$I_1 = \frac{V_{in} - (\frac{V_{in}}{2} + V_{offset})}{2R} = \frac{\frac{V_{in}}{2} - V_{offset}}{2R}$$

$$I_c^{discharge} = \frac{\frac{-V_{in}}{2} + V_{offset}}{2R} \tag{4.17}$$

As shown by equations 4.11,4.16 and 4.13,4.17, the charging and discharging currents result to be equal in case of perfect matching, different in case of mismatch, thus causing the output duty cycle to differ from 50%.
Moreover, the impact of the offset voltage on $I_c^{charge/discharge}$, and consequently on the duty cycle, is more and more important as the input voltage decreases as shown by equations 4.16,4.17. Several Monte Carlo mismatch simulations have been performed in order to highlight this phenomenon. The results obtained for two different input voltages are reported in Figure 4.11. As expected, the lower is the input voltage, the larger is the impact of mismatch on the duty cycle.

In this framework, a new VCO schematic that overcomes these issues has been designed, and it is shown in Figure 4.12. This schematic features the following solutions:

- the bias current generation is provided by transistor M_{load}, that is designed to be in linear region;
- the integrator has been substituted by a new ramp generation system: the bias current directly charges (through M_3) and discharges (through M_4) capacitor C.

Transistor M_1 should satisfy the following condition in order to stay in linear region:

$$V_{ds} < V_{gs} - V_{th} \rightarrow V_g > \frac{V_{bg}}{2} + V_{th} \tag{4.18}$$

The current I_l injected towards transistor M_1 has been sized in order to induce a sufficient gate voltage V_g, so to keep M_1 in linear region. Considering the expression of the drain current in triode, the on-resistance of M_1 can be written as:

$$R_{on,M_1} = \frac{\frac{V_{bg}}{2}}{I_l} = \frac{1}{\mu C_{ox} \left(\frac{W}{L}\right)_{M1} (V_g - V_{th})} \tag{4.19}$$

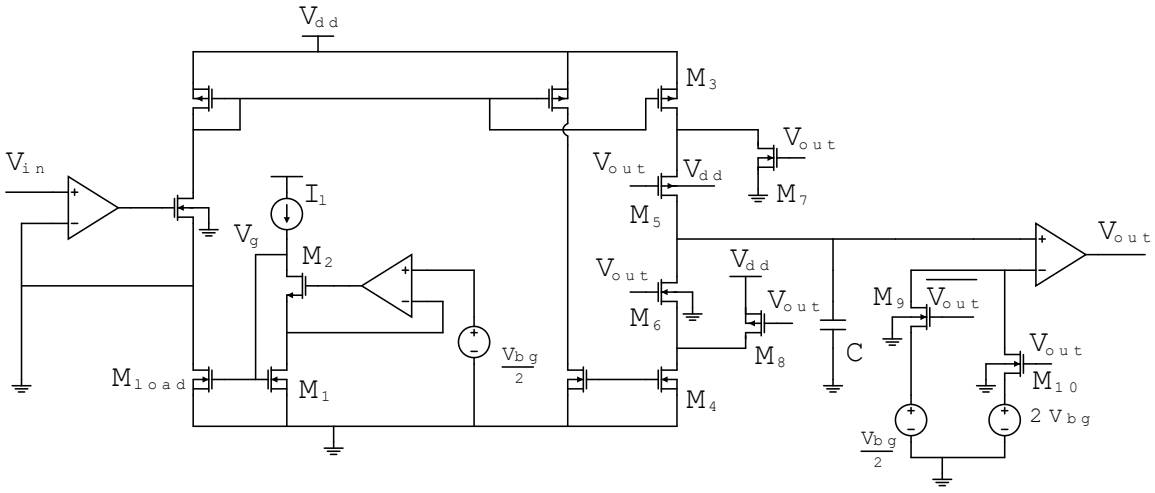


Figure 4.12: New schematic of the VCO.

V_{bg} and I_l have been designed to be independent of temperature and process variations, and thus R_{on,M_1} shares the same properties. Variations related to temperature or technological process would affect the values of μ, V_{th} and C_{ox}, and the gate voltage V_g would change accordingly. Therefore, transistor M_1 results to be equivalent to a resistor independent of temperature and process variations.

Voltage V_{in} is a scaled version of the *comp* signal, that is used also to choose the operation mode, its maximum value reachable in light load mode is about $V_{bg}/2$. The linearity condition for M_{load} is always satisfied in light-load operation:

$$V_g > V_{in-max} + V_{th} \tag{4.20}$$

Considering $\left(\frac{W}{L}\right)_{M_{load}} = \left(\frac{W}{L}\right)_{M_1}$, $R_{on,M_{load}} = R_{on,M_1}$. The on-resistance of M_1 is mirrored on the on-resistance of M_{load}, which thus exhibits the same independence on temperature and process variations. This solution overcomes the lot-to-lot variations in the output frequency for the same V_{in} found in the original VCO.

In this new schematic the effect of the mismatch affects the performance of the circuit in a different way compared to the original one. Indeed, the duty cycle could differ from 0.5 in case of mismatch on the current mirrors constituted by $M3$ and $M4$: in this case the charging and discharging current would be asymmetrical, causing different time lengths for t_{charge}, $t_{discharge}$. In order to mitigate this effect, since the mismatch effect on the threshold voltage depends on the transistor dimensions ($\sigma_{V_{th}} \propto \frac{1}{\sqrt{WL}}$), $M3$ and $M4$ are designed to occupy large areas ($W_{M3} = 5\mu m$, $L_{M3} = 5\mu m$, $W_{M4} = 10\mu m$, $L_{M4} = 8\mu m$).

Still, mismatch could induce an offset voltage on the input operational amplifier. In this case the voltage applied on M_{load} could vary from chip to chip, inducing slightly

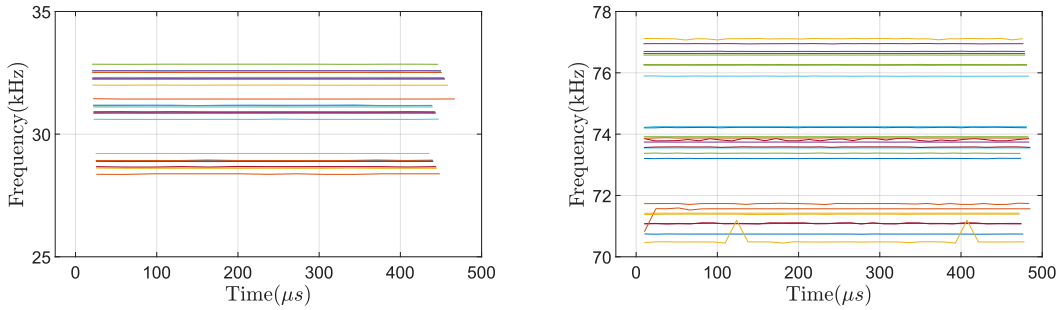
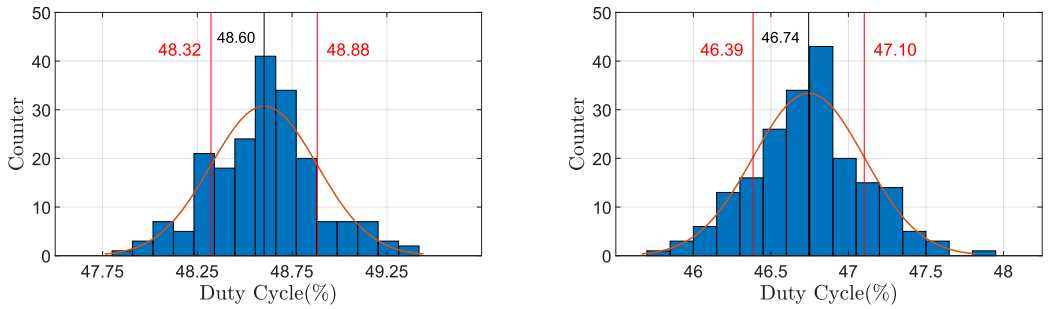


Figure 4.13: Frequency variation due to passive corners with (a) $V_{in} = 150mV$ and (b) $V_{in} = 0mV$.



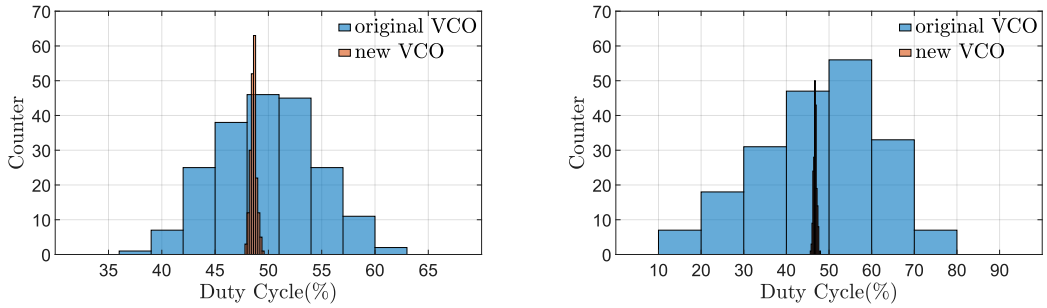
(a) $V_{in} = 150mV$ (b) $V_{in} = 50mV$

Figure 4.14: Output voltage duty cycle degradation with high (a) and low (b) input voltage.

different bias current and consequently varying the output voltage frequency for the same V_{in}.

The results for the same simulations reported in Figure 4.11 and 4.10 are shown in Figure 4.14 and 4.13. Moreover, so to highlight the benefits achieved by the new design, the comparison between the original and the new schematic simulation results regarding the duty cycle degradation are reported in Figure 4.15.

Then, the new design of the VCO has been embedded inside the full Resonant Switched Capacitor converter schematic in order to simulate the complete circuit. The results show that, the switching frequency required by the optimized tank, at current loads $I_{out} < 0.3A$ falls below 50kHz. This represents a serious issue for the stability of the open-loop operation. Indeed, as explained in section 3.7, if the unity gaing frequency of the open-loop transfer function becomes comparable to the switching frequency, then oscillations are induced on the signal *comp*. This



(a) $V_{in} = 150mV$ (b) $V_{in} = 50mV$

Figure 4.15: Duty cycle degradation induced by mismatch in the original and new VCO, with high (a) and low (b) input voltage.

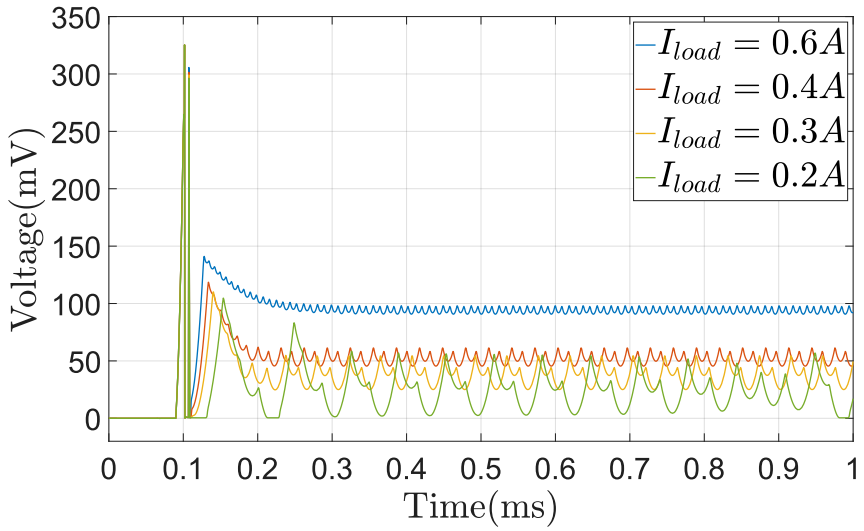


Figure 4.16: Input voltage oscillations induced by the optimized tank lowered frequency.

signal, after being scaled properly, is also used as the input voltage of the VCO. The resulting oscillations of V_{in} at low load currents are reported in Figure 4.16. The extremely low switching frequencies required by the optimized tank induces the *comp* signal oscillations. The light load operation mode becomes unstable in this condition, and it cannot be used when $I_{load} < 0.3A$.

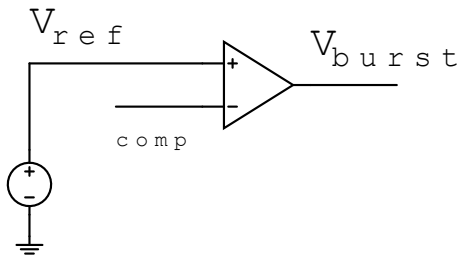


Figure 4.17: Burst control signal generation.

4.4 Burst mode

Burst mode can be used at low load currents ($I_{load} < 1A$) as an alternative to medium and light load modes. The purpose of this section is to better analyze the benefits and drawbacks of burst mode and to improve its operation.
The working principle of this operation has been introduced in section 2.3.4: it consists of a normal mode operation that is periodically turned on and off. The value of the control signal *comp* governs this intermittent operation.
As shown in Figure 4.17, the *comp* signal is compared to a reference voltage V_{ref} by means of a comparator with hysteresis. The output voltage V_{burst} is a control signal that allows the converter to work in normal mode when it is a logic '1', while

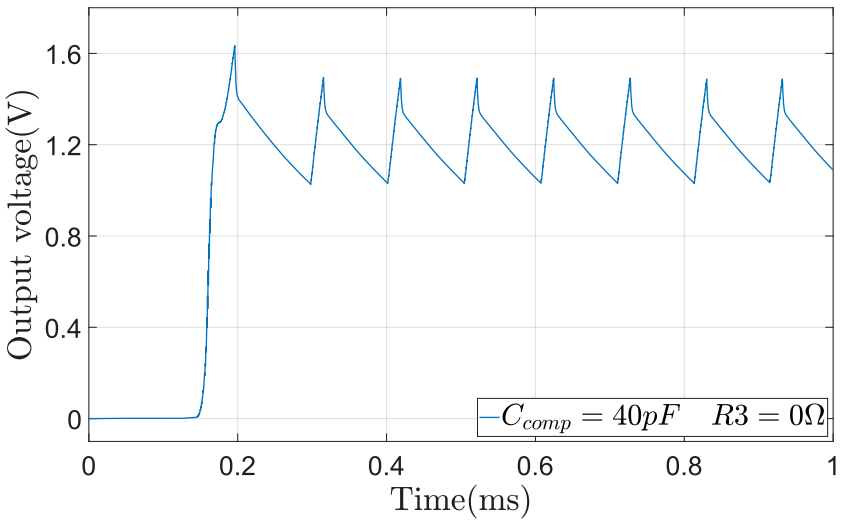


Figure 4.18: Output voltage ripple amplitude obtained due to the bandwidth degradation.

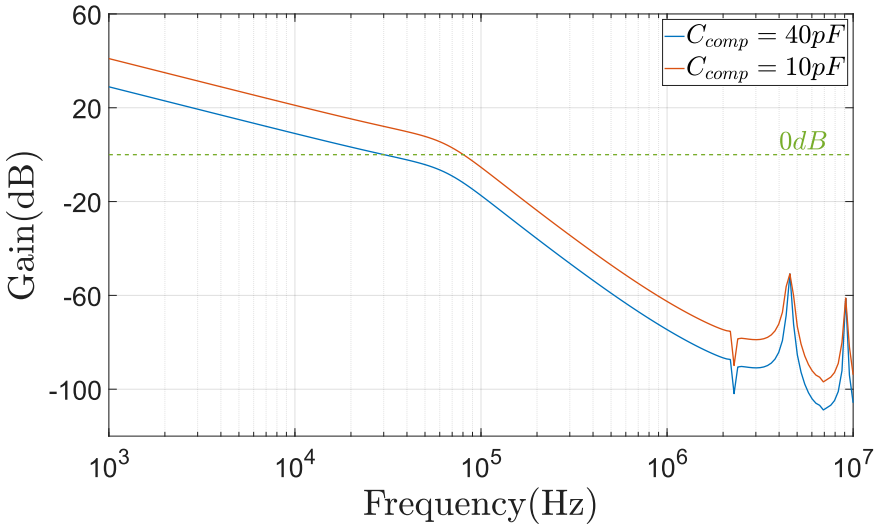


Figure 4.19: Impact of the compensation capacitance variation on the open-loop transfer function cutoff frequency.

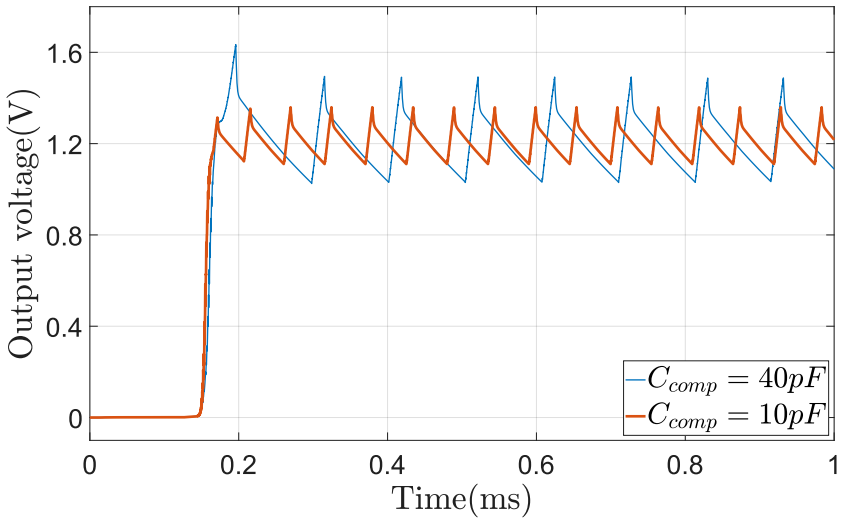


Figure 4.20: Output voltage ripple amplitude achieved thanks to the compensation finer tuning.

it stops the tank voltage excitation when it becomes '0', preventing $PWMH$ and $PWML$ from switching.

The main drawback of this mode is the significant output voltage ripple, that is intrinsically generated due to the intermittent operation. The amplitude of this

ripple is determined by two parameters:

- the hysteresis of the burst comparator;
- the bandwidth of the open-loop transfer function.

As explained in section 3.7, the efficiency optimization of the converter led to the lowering of the resonant frequency, which entailed a re-tuning of the compensation filter. The stable operation with this reduced resonant frequency is guaranteed by decreasing the unity gain frequency of the open-loop transfer function to values that are well below the switching frequencies. Figure 3.15 presents an example of the reduction in bandwidth of the open-loop transfer function
This bandwidth degradation induces a slower response of the signal *comp* to output voltage variations, increasing the output voltage ripple in burst mode.
The impact of the bandwidth degradation has been observed and simulated, and the result is shown in Figure 4.18. The output voltage ripple amplitude is about $500mV$, that is an unacceptable value. Therefore, it is necessary to intervene at design level in order to mitigate this issue.

A first solution entails a finer tuning of the compensation network in order to achieve both good attenuation at resonance and an increased bandwidth. This can be achieved varying the value of the compensation capacitance C_{comp}. As shown from Figure 4.19, by using a capacitance $C_{comp} = 10pF$ in place of the original one ($C_{comp} = 40pF$) it is possible to increase the unity gain frequency from $30kHz$ to $80kHz$, keeping it reasonably lower that the minimal switching frequency (i.e. the resonant frequency, $f = 200kHz$) .
The impact of this solution on the output voltage ripple in burst mode has been simulated, and Figure 4.20 shows the achieved improvement: the ripple decreases from $500mV$ to $250mV$.
However, the ripple amplitude achieved is still too large. It would be dangerous to further decrease the compensation capacitance, since it would bring the unity gain frequency too close to the switching frequencies. Therefore, it is necessary to reduce the comparator hysteresis to limit the ripple on the *comp* signal in burst mode, allowing a reduce output ripple for the same loop bandwidth.

The schematic of the regenerative comparator is shown in Figure 4.21. Supposing that initially the signal *comp* assumes a low value, then transistor $M1$ results to be on, driving the current I_{M1} equal to I_{bias}, while $M2$ is off. Therefore, $M6$, $M5$ and $M9$ do not drive any current and voltage V^- is low. At the same time, $M3$, $M4$, $M7$ and $M8$ mirror the bias current, thus driving voltages V^+ and V_{out} high.

Then, as signal *comp* increases, $M2$ drives a portion of I_{bias} while I_{M1} decreases. At a certain point, current I_{M2} exceeds I_{M4} and the comparator switches: at this

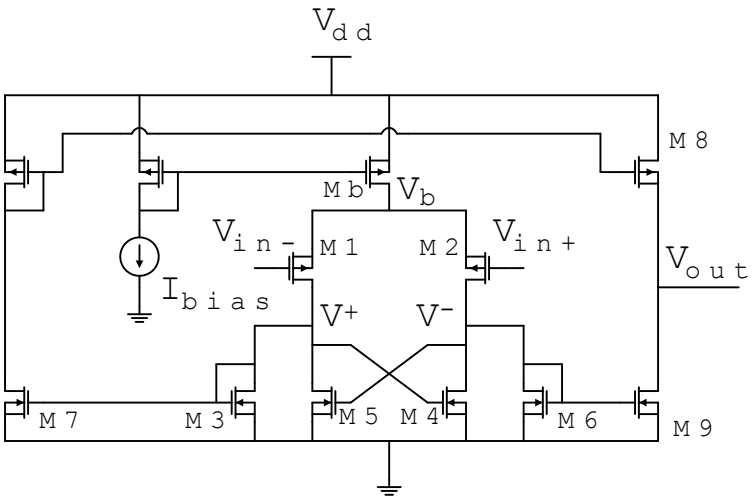


Figure 4.21: Regenerative comparator schematic.

point $M6$, $M5$ and $M9$ drive a current higher than the one that flows through $M3$, $M4$, $M7$ and $M8$. Therefore, voltage V^+ decreases, V^- rises and V_{out} is discharged by $M9$.
Then, if *comp* decreases again, the comparator would switch back to the initial state as I_{M1} overcomes I_{M5}.

A tunable hysteresis can be achieved by varying the dimensions of the transistors $M5$ and $M4$, so acting on the k parameter:

$$k = \frac{\left(\frac{W}{L}\right)_{M4}}{\left(\frac{W}{L}\right)_{M3}} = \frac{\left(\frac{W}{L}\right)_{M5}}{\left(\frac{W}{L}\right)_{M6}} \tag{4.21}$$

Considering the drain current of the devices in weak inversion negligible, the currents at equilibrium (just before the high-to-low transition of V_{out}) are:

$$I_{M2} = I_{M4} \quad I_{M4} = kI_{M3} \quad I_{M3} = I_{M1} \quad I_{bias} = I_{M1} + I_{M2} \quad I_{M5} = I_{M6} = 0 \tag{4.22}$$

that lead to:

$$I_{M1} = \frac{I_{bias}}{1+k} \quad I_{M2} = \frac{kI_{bias}}{1+k} \tag{4.23}$$

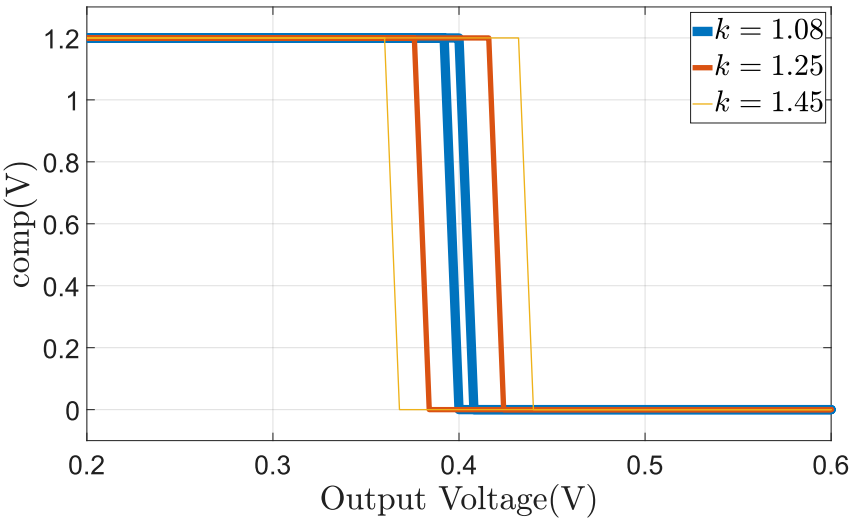


Figure 4.22: Comparator hysteresis amplitude variation with the k parameter.

Assuming that the differential pair transistor $M1$ and $M2$ are in strong inversion, the currents assume the following values:

$$\frac{I_{bias}}{1+k} = \mu C_{ox}\frac{1}{2}\left(\frac{W}{L}\right)_{M1}(V_{sg1}-V_{Th})^2 \rightarrow V_{sg1} = V_{Th} + \sqrt{\frac{2I_{bias}}{\mu C_{ox}\left(\frac{W}{L}\right)_{M1}(1+k)}} \tag{4.24}$$

$$\frac{kI_{bias}}{1+k} = \mu C_{ox}\frac{1}{2}\left(\frac{W}{L}\right)_{M2}(V_{sg2}-V_{Th})^2 \rightarrow V_{sg2} = V_{Th} + \sqrt{\frac{2kI_{bias}}{\mu C_{ox}\left(\frac{W}{L}\right)_{M2}(1+k)}} \tag{4.25}$$

Considering that $\left(\frac{W}{L}\right)_{M1} = \left(\frac{W}{L}\right)_{M2} = \left(\frac{W}{L}\right)_{dp}$ and the reference voltage is connected to the positive input, the value of the negative input of the comparator for which its output switches from high to low can be calculated as:

$$V_{H+} = V_{ref} + \sqrt{\frac{2I_{bias}}{\mu C_{ox}\left(\frac{W}{L}\right)_{dp}(1+k)}}\left(\sqrt{k}-1\right). \tag{4.26}$$

Symmetrically, the value of the negative input of the comparator for which its output switches from low to high is:

$$V_{H-} = V_{ref} - \sqrt{\frac{2I_{bias}}{\mu C_{ox}\left(\frac{W}{L}\right)_{dp}(1+k)}}\left(\sqrt{k}-1\right). \tag{4.27}$$

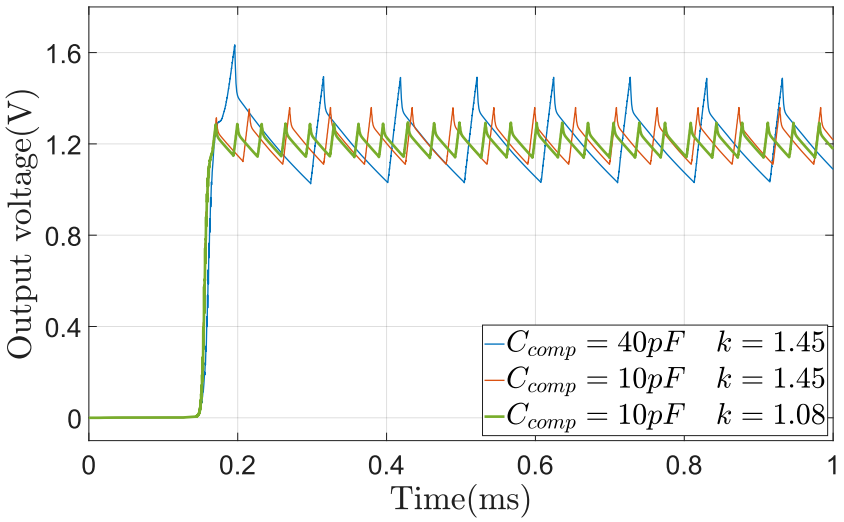


Figure 4.23: Output voltage ripple amplitude achieved thanks to the comparator hysteresis tuning.

The hysteresis amplitude ($\Delta V_H = V_{H+} - V_{H-}$) is then:

$$\Delta V_H = 2\sqrt{\frac{2I_{bias}}{\mu C_{ox}\left(\frac{W}{L}\right)_{dp}(1+k)}}\left(\sqrt{k}-1\right). \tag{4.28}$$

Equation 4.28 shows clearly that only if $k > 1$ the comparator exhibits an hysteresis, and that its amplitude (ΔV_H) can be tuned by modifying the parameter k.

In the original comparator $k = 1.45$. This parameter has been varied in order to reduce the amplitude of the hysteresis, with the aim of reducing the output voltage ripple of the converter in burst mode. The results obtained from the simulations, for different values of k, are shown in Figure 4.22. The value $k = 1.08$ has been chosen, and the complete converter operation has been simulated in burst mode. As depicted in Figure 4.23 the comparator with the improved hysteresis allows to achieve an output voltage ripple amplitude of $150mV$, that can be considered an acceptable value.

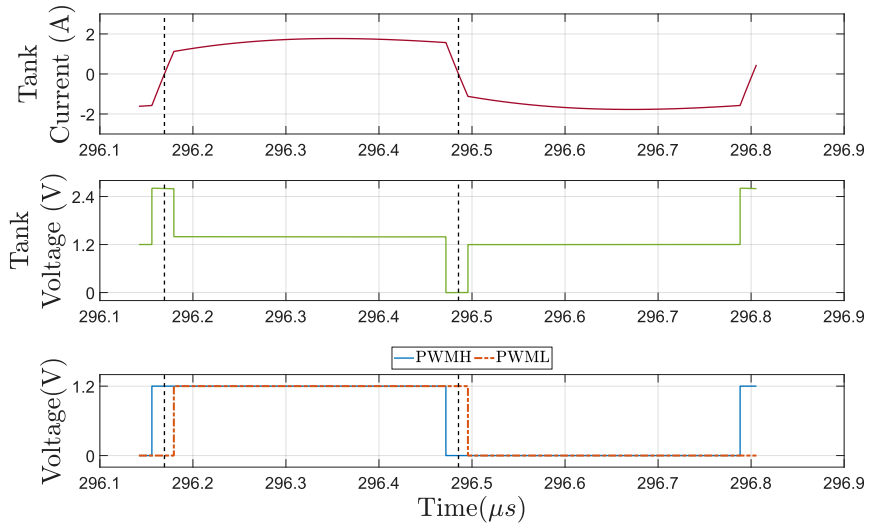


Figure 4.24: Proper functioning of the original control circuit in α operation ($V_{in} = 2.7V$ $I_{load} = 1.5A$).

4.5 Improved β mode

The shape of the current response of the tank to a voltage excitation depends on its damping factor, which in turn depends on the values of the tank components (see section 2.2.1). The efficiency optimization that has been pursued in order to boost the converter performances led to the variation of the tank capacitor. Consequently, the attenuation factor increased form $\zeta = 0.48$ to $\zeta = 1.56$, as detailed in section 3.7.2. Therefore, the optimized tank is characterized by an overdamped current response, that exhibits an exponential decaying behaviour (as depicted in Figure 2.5).
The control logic provides the $PWMH$ and $PWML$ signals to the power transistors ($HS1$, $LS1$, $HS2$, $LS2$), ensuring the proper tank voltage excitation. The generation of $PWMH$, $PWML$ is based on the signal CS, whose switching instants correspond to the detected zero-crossing instants of the tank current. The exponential decaying behaviour of the over-damped current may be a critical issue for the control circuitry, since in certain conditions it does not provide a zero crossing of the tank current, differently from the sinusoidal under-damped response. In the absence of a zero-crossing for the tank current, the switching operation stops and the converter output voltage drops to zero. In the following, the zero crossing occurrence in normal mode and the tank current shape are analyzed, in order to understand in which conditions this issue can be found.
The proper functioning of the converter has been simulated in normal mode, both in α and in β operation. In particular, the original under-damped tank has been

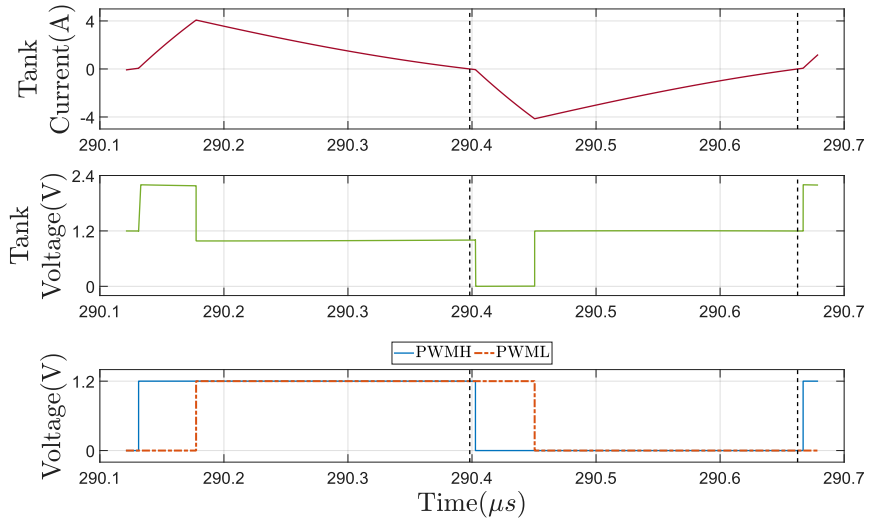


Figure 4.25: Proper functioning of the original control logic in β operation($V_{in} = 2.2V$ $I_{load} = 1.5A$).

employed ($C_{tank} = 4.7\mu F$, $L_{tank} = 12nH$), and the obtained results are shown in Figures 4.24, 4.25.

The tank current and voltage excitation obtained for α mode are reported in Figure 4.24. In this condition, the control circuit provides a phase lead of $PWMH$ from CS (which should switch at the zero crossing instants of the tank current), while $PWML$ is synchronized with CS. However, the comparator that evaluates the sign of the current (providing the signal CS at its output) and the rest of the control logic introduce a delay between the tank current zero crossing and the switching instants of CS. $PWML$ is therefore not perfectly synchronized with the zero crossing instants, but it exhibits a small delay from them. In general, in α operation the tank current is supposed to cross the zero value during Phase 1 and Phase 3 (see Figure 2.10).

On the other hand, in β operation the signal $PWML$ has a phase lag compared to CS, while $PWMH$ is synchronized with CS. In this case, the delay caused by the control logic imposes a delay of $PWMH$ from the tank current zero crossing instants, as shown in Figure 4.25. The zero crossing in β mode occurs during Phase 2 and Phase 4 (see Figure 2.10).

The voltage excitation and the initial tank conditions (tank current and voltage across the capacitor) determine the tank current slope and its shape in each phase. These conditions are different for every input/output voltage ratio and each load

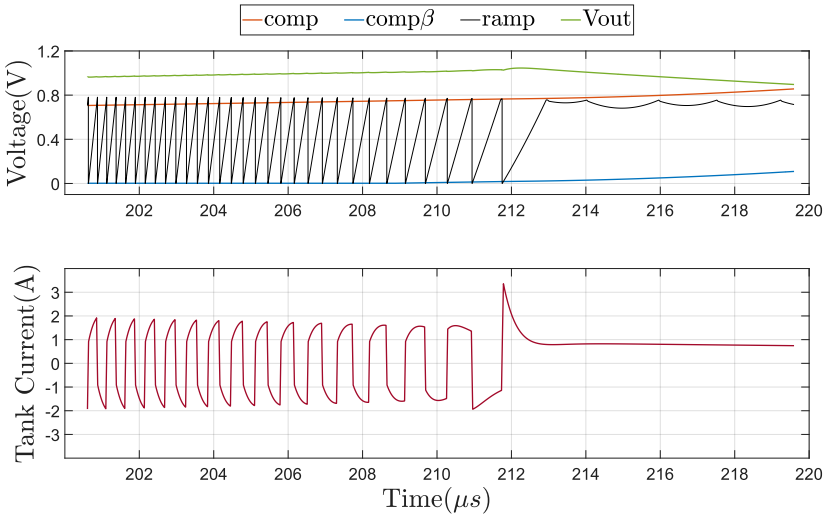


Figure 4.26: Failure of the control logic in β operation in a converter equipped with the optimized tank.

current. In general, during Phase 1 and Phase 3 the tank inductor is subjected to a larger voltage step compared to the other two phases. This determines a steep tank current slope, and the zero crossing always occurs (both for under-damped and for over-damped tanks). Instead, during Phase 2 and Phase 4, a small voltage is applied to the inductor, thus the tank current slowly decays in absolute value. It can be shown that in these phases the current decay towards zero is exponential for an over-damped tank, and the zero crossing does not occur.

Since the current does not cross the zero value, the signal CS does not switch, and consequently $PWMH$ and $PWML$ also stop switching. Then, the tank excitation vanishes and no current is provided to the output node. The load current quickly discharges the output voltage causing the failure of the converter.
This mechanism has been observed during the measurements, when using the tank components that optimize the efficiency (which lead to the increased damping factor). Then, it has been widely simulated in order to analyze it. An example of the converter failure is shown in Figure 4.26. As soon as the converter enters β mode, the over-damped tank current does not provide the zero crossing anymore, the tank excitation vanishes and the output voltage is discharged.

A solution has been proposed in this work to solve this critical issue at design level. The idea is to move the zero crossing instants from Phase 2 and Phase 4 to Phase 1 and Phase 3, in β mode. This can be achieved by imposing a phase lead on the $PWML$ signal from CS.

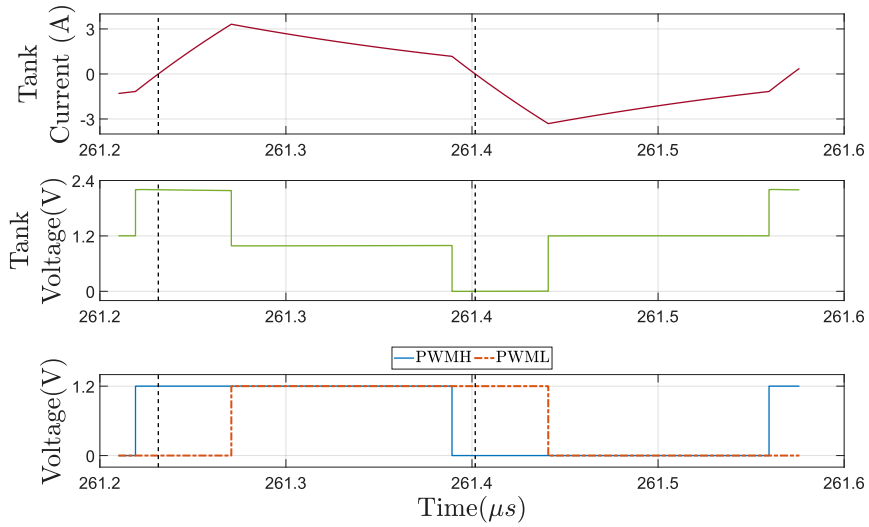


Figure 4.27: Proper functioning of the control logic in the improved β operation ($V_{in} = 2.2V$ $I_{load} = 1.5A$).

A voltage reference αmin has been generated by properly scaling the stable bandgap voltage. In particular, the value of the signal αmin is tuned to be slightly lower than the *ramp* amplitude.
The value of $comp\beta$ is then defined as:

$$comp\beta = comp - \alpha min \tag{4.29}$$

As the converter enters β operation (when signal *comp* exceed the value of αmin), the angle generator block (see Figure 2.13) uses signals αmin and $comp\beta$ in order to generate respectively the phase lead of $PWML$ and the phase lag of $PWMH$ from the switching instants of CS. The operation in α mode does not change: only the signal *comp* is used to generate the phase lead of $PWMH$.
The effectiveness of this solution has been proven in simulation: Figure 4.27 shows the correct operation of the improved β mode, ensuring the zero detection during Phase 1 and Phase 3.
Figure 4.28 reports the main signals that characterize this operation.

In the original β operation, the time delay introduced by the zero crossing comparator and by the control logic does not allow the soft turn on of $HS1$ and $LS1$, leading to increased switching losses and degraded efficiency.
An extra feature of the improved β operation is that it could also restore the soft switching mechanism for $HS1$ and $LS1$, improving the power efficiency of the converter.
Indeed, as shown in Figure 4.27, when $PWMH$ switches to the logic high value,

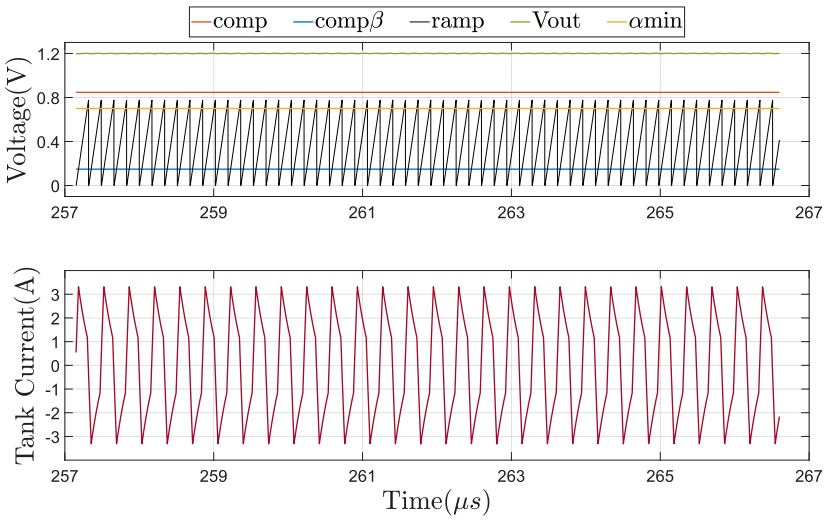


Figure 4.28: Main signals introduced for the improved β operation ($V_{in} = 2.2V$ $I_{load} = 1.5A$).

the tank current is negative and flows through the bulk diode $D1$, allowing $HS1$ to turn on at zero voltage. Analogously, when $PWMH$ switches to the logic low value $D2$ conducts the positive tank current as long as transistor $LS1$ is turned on at zero voltage.

The new β mode ensures the converter safe operation, both for under-damped and over-damped tank circuits. At the same time, it promises improved power efficiency thanks to the restored soft switching mechanism.

Chapter 5

Conclusions

The High Luminosity LHC experiments upgrade requires a custom power distribution system, in order to properly supply the front-end circuits. This is divided in two stages of voltage conversion that are performed by radiation and magnetic field tolerant DCDC converters. Such DCDC converters must use a minimal amount of material, in order not to interfere with the physics performances of the experiments. Due to its reduced mass and volume compared to conventional solutions and to its high efficiency, a Resonant Switched Capacitor (ReSC) converter has been proposed for the last stage of the voltage conversion: it must step down the voltage from $2.5V$ to $1.2V$ or $1V$, supplying a load current in the range $0 : 3A$. This converter was designed and prototyped by the Microelectronics group at CERN.

The ReSC converter features different operation modes that maximize the power efficiency in the whole range of load currents. Accurately estimating the efficiency of the developed ReSC converter in the design phase is very complex, especially due to the contributions of the used inductor and of the PCB to the total parasitic resistance at the switching frequencies. The optimization of the converter efficiency must be therefore carried out in the characterization phase. This has been the first objective of this master thesis project, and such efficiency optimization has been pursued by carefully tuning the passive discrete components of the converter. In particular, special focus has been applied to the selection of the elements of the resonant LC tank.
The optimized tank elements have been chosen by taking into consideration both their impact on the efficiency and on the volume of the converter. Three possible choices have been presented in section 3.6, and the one featuring $L_{tank} = 12nH\, C_{tank} = 47\mu F$ has been chosen. Indeed, this solution achieves an improvement of the efficiency of about 4% at $I_{load} = 3A$ compared to the one obtained with the values of the original tank components chosen in the design phase ($L_{tank} = 12nH\, C_{tank} = 4.7\mu F$), while keeping the same converter volume.

Compared to the original LC circuit, the selected tank elements lead to a variation in the resonant frequency and in the tank damping factor. Several issues arose due to the variation of these parameters. The emerged issues have been investigated and solved at design level.

The lowered resonant frequency causes a general reduction of the switching frequencies. Therefore, the Phase Locked Loop that provides the ramp voltage has been modified so to extend its frequency range of operation.
Also the Voltage Controlled Oscillator that provides the tank excitation voltage in light load mode suffers from the lowering of the switching frequencies. Its schematic has been modified in order to improve its performances, focusing on its rejection of mismatch and process variations. However, the very low switching frequencies imposed by the optimized tank drive the light load mode to failure for current loads $I_{load} < 0.3A$. An additional operation mode should be designed to achieve voltage conversion in the load current range $0A < I_{load} < 0.3A$.

An alternative to the light load operation is burst mode. Such mode has been improved in this work by adopting several design solutions to reduce its output voltage ripple.
Considering the issues arose in light load mode, the burst mode has been selected as the most promising operation that could be adopted for low load currents. Indeed, even if it provides low efficiency, it guarantees a very smooth transition from/to normal mode.

Finally, β mode has been improved by introducing a fixed phase lead of the driving signal $PWMH$ from the tank current zero crossing. This modification ensures the safe operation of the converter even when using an over-damped tank. Moreover, this modification could improve the efficiency of the converter in β operation, since it guarantees soft switching.

A refined ReSC converter, featuring the optimized tank, the new PLL and the improved β mode, together with the optimized burst operation could be prototyped to further continue this project. At high current load ($I_{load} = 3A$), this converter could provide an efficiency comparable to a buck converter designed for the same application, while presenting a much smaller volume.

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